CHAPTER 7
INTERLEAVED DCM SINGLE-STAGE PFC CONVERTER WITH REDUCED EMI AND BOOST INDUCTOR SIZES

7.1 INTRODUCTION

Among the S^2PFC techniques introduced in recent years, in general, the DCM S^2PFC converters are simple and need only a small boost inductor, but they have high current stress on the switch and high current ripple on the rectifier input. A large EMI filter is normally required in the DCM S^2PFC converter. On the other hand, the CCM S^2PFC converters have low switch current stress and low input current ripple, but the converters need a large boost inductor and more passive component(s) to achieve CCM ICS functionality. Generally, the DCM S^2PFC is only suitable for very low power applications (e.g. output power less than 100W). For higher power applications, the CCM S^2PFC techniques are more suitable.

To due with universal-line input, the VD S^2PFC techniques have been proposed with reduced hold-up capacitance and improved converter performance. The comparison and experimental data show that the CCM VD S^2PFC has smaller total inductors' size and better efficiency than the CCM boost PFC converter does. As concluded in Chapter 6, the CCM VD S^2PFC techniques provide a cost-effective solution for IEC class D equipment with input power up to 600W.

Even though, it is possible to further reduce the magnetic component size and increase the power density of the VD S^2PFC converter, by taking the advantages of both the DCM and CCM S^2PFC techniques. In this chapter, a novel interleaved DCM S^2PFC technique is proposed,

with reduced EMI filter and boost inductors' size. The results of a 5V/90A-output prototype prove the performance of the proposed technique is comparable to the CCM S^2PFC techniques.

7.2 TOPOLOGIES AND PRINCIPLE OF OPERATION

7.2.1 Topologies of the proposed interleaved DCM S^2PFC converters

To reduce the input current ripple of the DCM S^2PFC converter and the related differential-mode (DM) EMI filter size, a novel interleaved DCM S^2PFC technique is proposed. Figure 7.1 shows one circuit topology of the proposed technique. In this circuit, the dc/dc output stage is a symmetric half-bridge dc/dc converter. The dc/dc transformer TR has two additional windings N_1 and N_2, which are in series with the boost inductor L_1 or L_2 and the boost diode D_{B1} or D_{B2}, respectively. The turns-number of N_1 equals to N_2 and boost inductance L_1=L_2. Therefore, the S^2PFC front-end has two identical DCM input-current-shaping paths except N_1 and N_2 have opposite directions so that the winding voltages on N_1 and N_2 always have 180-degree phase shift between each other. As a result, the switching-cycle boost inductor current i_{LB1} and i_{LB2} is interleaved with 180-degree phase shift. As explained in Section 7.2.2, the inductor current ripple cancels each other, and the input current has reduced ripple and doubled ripple frequency.

To achieve this kind of interleaving effect, it is necessary to point out that the output DC/DC stage converter has to have a symmetric-driven waveform on the DC/DC transformer TR. Therefore, the DC/DC stage can also be implemented with symmetric-driven full-bridge or push-full dc/dc converters, though Fig. 7.1 only shows the half-bridge dc/dc implementation. The circuit in Fig.7.1 is proposed for converter with narrow input line-voltage range, i.e., either the U.S. or European line range only. The detailed circuit operation principle will be presented in Section 7.2.2.

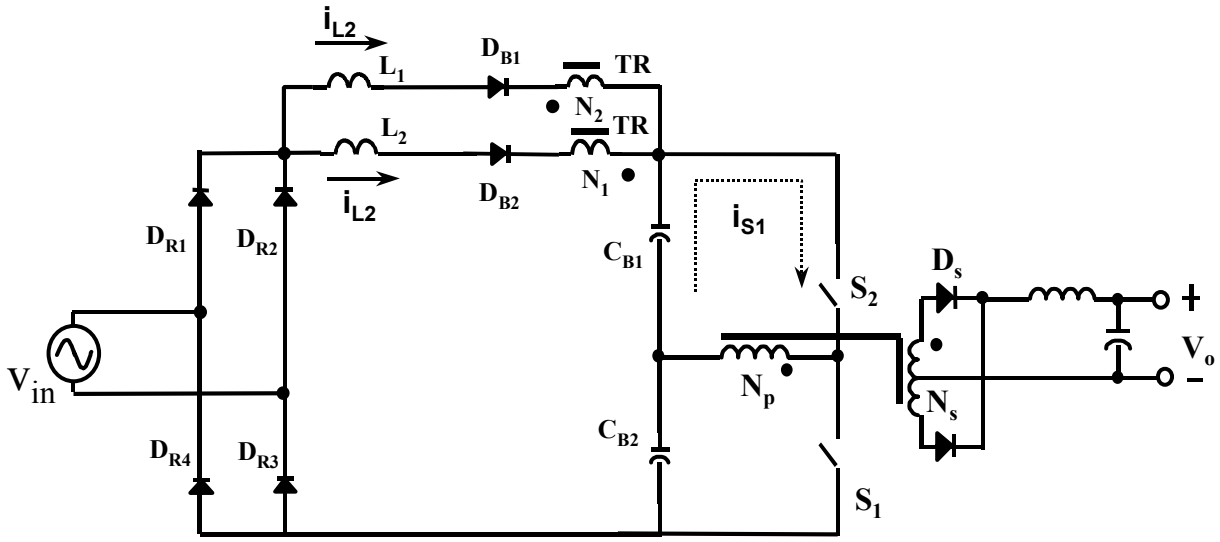


Figure 7.1 Circuit diagram of the proposed interleaved DCM S^2PFC converter with symmetric-driven half-bridge DC/DC stage (N_1=N_2 < 2·N_P)

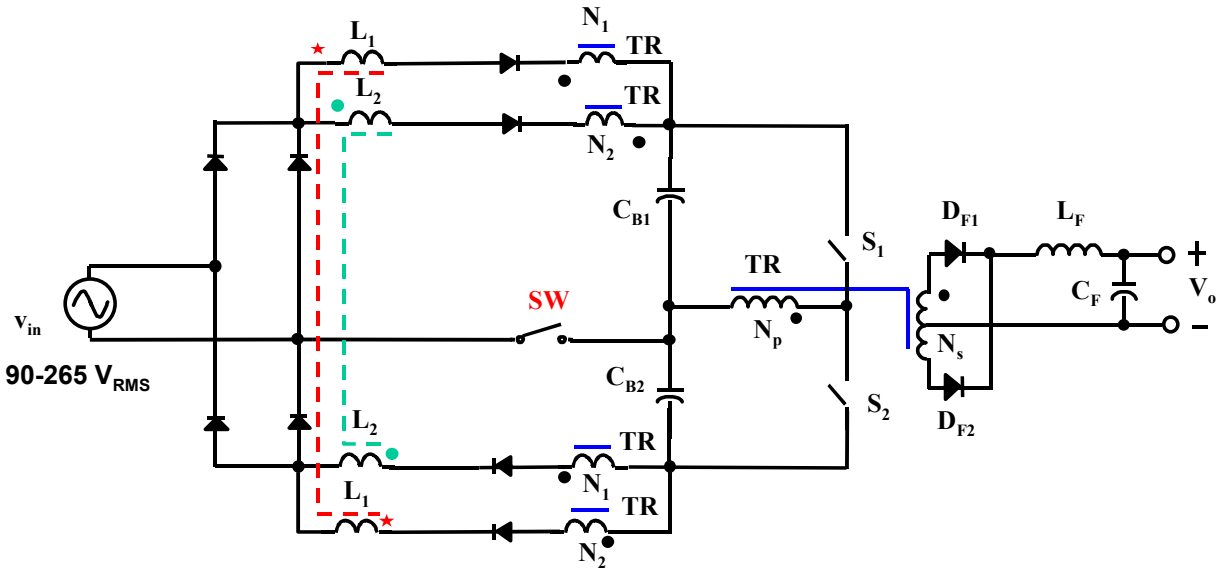


Figure 7.2 Voltage-douber version of the proposed interleaved DCM S^2PFC circuit with universal line input (N_1=N_2 < N_P)

To deal with universal line input, Fig. 7.2 shows the proposed technique with voltage-doubler rectifier (VDR) front-end configuration. In the circuit in Fig. 7.2, the switch SW is the low-frequency range-selection switch, which is always closed with the U.S. line input or opened with the European line input. Again, to achieve horizontally symmetric structure of the VD S^2PFC, L_1, L_2, N_1, N_2 has to be split into two windings, respectively. In this case, the DC/DC converter will need totally 6 windings and 8 bobin pins on the primary high-voltage side. But the total winding area is not necessarily increased. With this VD S^2PFC structure, the total capacitor voltage is doubled at low line compared to the circuit in Fig. 7.1. Therefore, the hold-up capacitance can be minimized and the converter performance can be significantly improved.

7.2.2. Principle of operation

7.2.2.1 Interleaved DCM S^2PFC converter with narrow input voltage range

The circuit in Fig. 7.1 is used with a narrow line input-voltage range. The boost inductor L_1 and L_2 are designed to always be in DCM mode. To achieve good inductor current interleaving, the conduction path of L_1 should be designed identical as the L_2 conduction path except the polarities of N_1 and N_2 are opposite. To provide proper operation of the "magnetic switch" [B14], the turns-number of N_1 or N_2 should be equal or less than $2 \cdot N_p$.

To facilitate the analysis of operation, Fig. 7.3 and 7.4 show the topological stages and key waveforms of the interleaved DCM S^2PFC circuit, at low line, full load condition. To simplify the analysis, it is assumed that all semiconductor components are ideal. In additional, the magnetizing current in the half-bridge transformer is ignored. The input voltage of the converter is considered constant during a switching cycle because that the switching frequency is much higher than the line frequency.

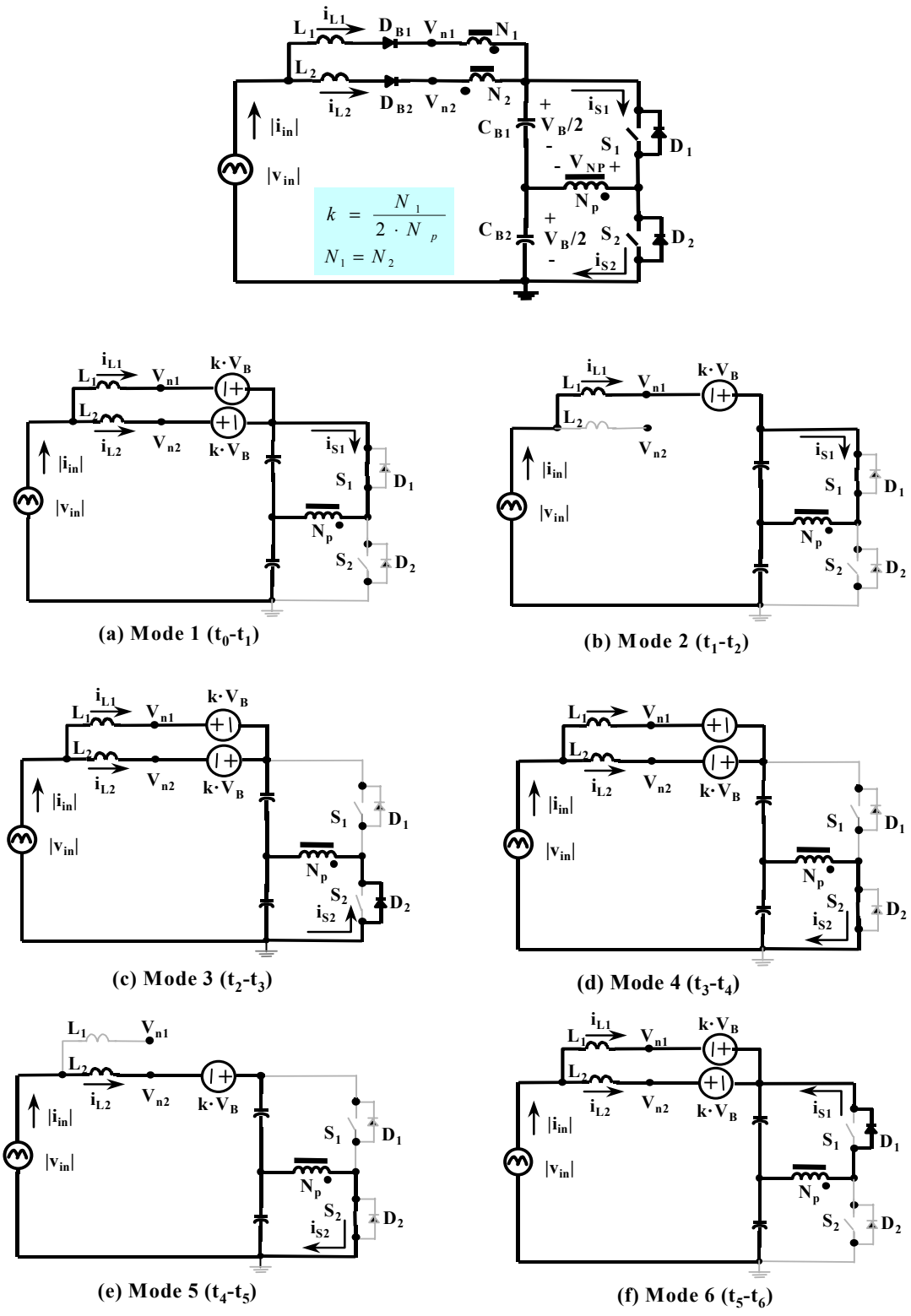


Figure 7.3 Equivalent circuit in each operation mode (high-voltage side only) at low line, full load condition

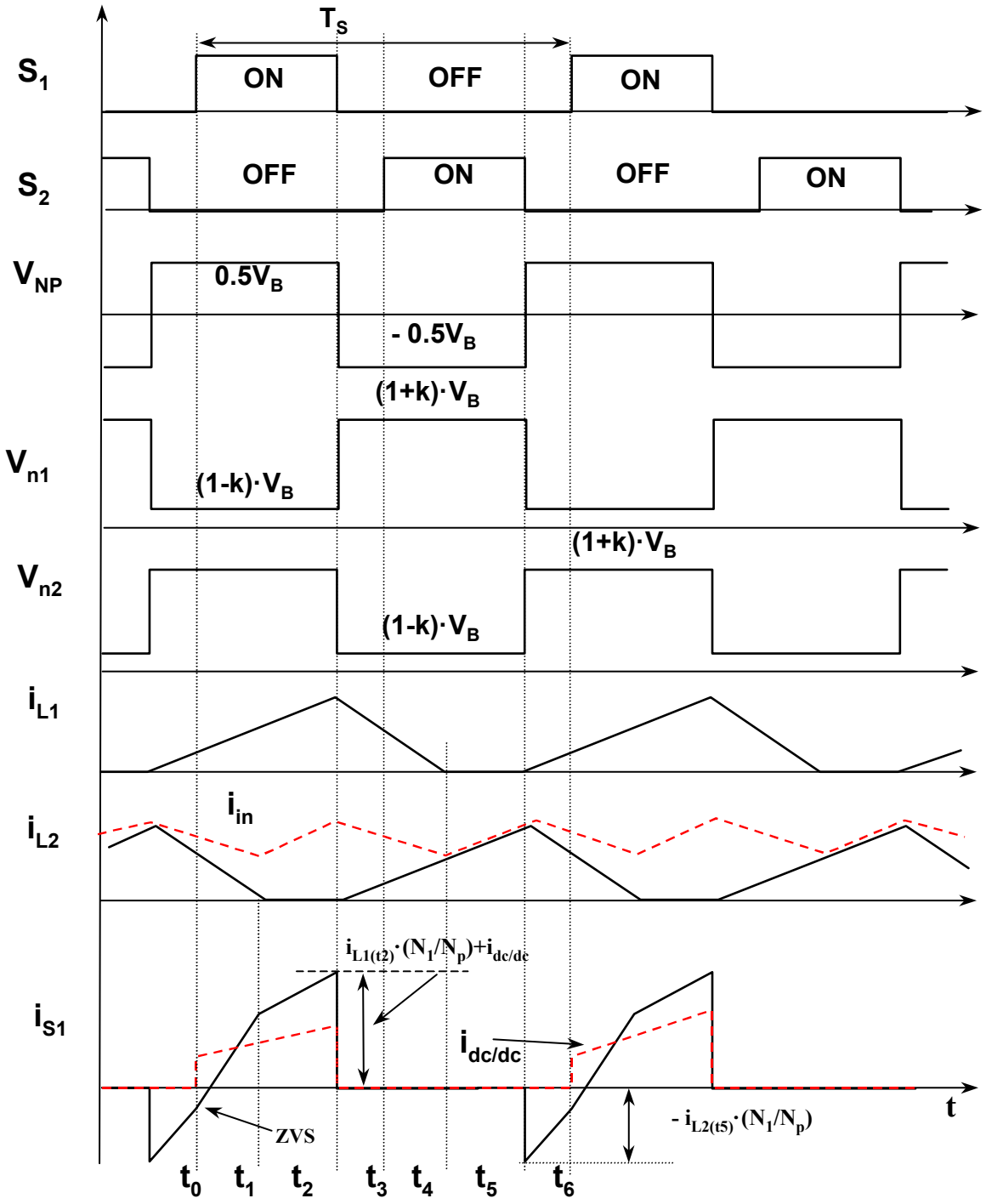


Figure 7.4 Theoretical switching-cycle waveforms of the proposed converter

(At low line, full load condition)

Finally, the waveforms in Fig. 7.4 are for the converter operating at the peak of the instantaneous input voltage. Under the above assumptions, Fig. 7.3 and Fig. 7.4 show that there are six equivalent operation modes in one switching cycle T_s:

Mode 1 (t_0-t_1): Just before time t_0, the switches S_1 and S_2 are off. The winding N_p sees the boost inductor currents coupled through winding N_1 and N_2. Since $i_{L1}>i_{L2}$, The winding N_p current goes through the anti-parallel diode (or body diode) D_1 to the capacitor C_{B1}. Therefore, at time t_1, the switch S_1 is ZVS turned on. In the t_0-t_1 time interval, the converter has an equivalent circuit as in Fig. 7.3(a), in which, the winding N_1 and N_2 equal to two voltage sources with opposite directions. The voltage magnitude of the voltage source is determined by the turns-ratios of N_1/N_p. The absolute values of the node voltages (refer to ground) v_{n1} and v_{n1} are given as:

$$v_{n1} = v_{n2} = V_B \pm \frac{N_1}{N_p} \cdot \frac{V_B}{2} = V_B \pm k \cdot V_B \qquad 7.1$$

In the t_0-t_1 time interval, the inductor L_1 is charged by voltage ($|v_{in}|+k\cdot V_B-V_B$). At the same time, the inductor current L_2 is discharged by voltage ($k\cdot V_B+V_B-|v_{in}|$), until i_{L2} reach zero at t_1. Besides, in mode 1, the current through switch S_1 can be given as:

$$i_{S1} = i_{dc/dc} + (i_{L2} - i_{L1}) \cdot \frac{N_1}{N_p} \qquad 7.2$$

where the $i_{dc/dc}$ is the half-bridge dc/dc converter current go to the output. As can be seen, current i_{L1} reduces the S_1 switch current stress in mode 1. Besides, as mentioned before, the switch S_1 can achieve ZVS turn-on at t_0 moment if the sum of Equation (7.2) is negative. This condition can be met with at low line while the boost inductor current is high. Of course, to achieve ZVS turn on, the turn-ratio of N_1/N_p should be properly designed too.

Mode 2 (t_1-t_2): when the inductor current i_{L2} is discharged to zero at t_1 moment, the inductor L_2 enters DCM mode and the circuit has an equivalent model as Fig. 7.3(b). In this mode, L_1 is continuously charged by voltage ($|v_{in}|+k\cdot V_B-V_B$). The switch current i_{S1} can be calculated as

$$i_{S1} = i_{dc/dc} + \frac{N_1}{N_p} \cdot i_{L1} \qquad 7.3$$

Mode 3 (t_2-t_3): at t_2 time instant, the switch S_1 is turned off. Since inductor current i_{L1} is going out of the dot of the winding N_1, the coupled current on the primary winding N_p should be going into the dot. Because S_1 is already turned off, the anti-parallel diode (or body diode) D_2 should conduct current. The equivalent circuit is shown in Fig. 7.3(c). The primary winding voltage v_{NP}=-0.5·V_B. The winding voltages cross N_1 and N_2 also change their polarities. As the result, inductor current i_{L1} starts to be discharged by voltage ($k\cdot V_B+V_B-|v_{in}|$) from its peak value and inductor current i_{L1} starts to be charged by voltage ($|v_{in}|+k\cdot V_B-V_B$) from zero.

Mode 4 (t_3-t_4): at time t_3, the switch S_2 is turned on. Since the body diode D_2 has been conducting the current, switch S_2 achieves ZVS turn-on. After the diode D_2 current reaches zero and switch S_2 starts conduct current, the equivalent circuit model is shown in Fig. 7.3(d). In this mode, i_{L2} is continuously increasing and i_{L1} is continuously decreasing. Mode 4 is the symmetric mode of mode 1.

Mode 5 (t_4-t_5): at time t_4, the inductor current i_{L1} reaches zero. Then the circuit enters mode 5, as shown in Fig. 7.3(e). Mode 5 is the symmetric mode of mode 2.

Mode 6 (t_5-t_6): at time t_5, S_2 is turned off while i_{L2} reaches its peak value. Because i_{L2} is going into the dot of the winding N_2, the current through N_p must go out of dot. The anti-parallel diode D_1 starts conduct current. Therefore, the voltage cross N_p changes its polarity again and equals to

$0.5 \cdot V_B$. At the result, the winding N_1 and N_2 voltages also change their polarities. The current i_{L2} starts to decrease and the current i_{L1} starts to increase. The circuit model is shown in Fig. 7.3(f), which is in the symmetric mode of mode 3. At time t_6, S_1 is turned on and the circuit enters mode 1 again.

Several advantages of the proposed circuit can be concluded according to the above conduction-mode-analysis. First, due to the symmetric voltage waveform on the dc/dc transformer winding N_p, the boost inductor current i_{L1} and i_{L2} are also symmetric with 180-degree phase shift. As the interleaved input current waveform i_{in} from Fig. 7.4, a good interleaving on the input current can be achieved with reduced current ripple and doubled ripple frequency. The can significantly reduce the EMI filter size. Second, the semiconductor switches can achieve ZVS turn-on, especially at low line, full load while the inductor current is high. This can reduce the switching loss when the switches are turned on at time instant t_0 or t_6. Besides, since the boost inductors are operated in DCM mode, the reverse-recovery loss of the boost diode can be eliminated. Finally, in mode 1 and mode 2, the switch current is the dc/dc current plus the difference of two inductor currents, instead of the sum of the absolute values of the inductor currents. The switch current stress as well as the switch conduction loss can be reduced. As the conclusion, even this circuit is operated in the DCM mode with high inductor current ripple, the converter efficiency is not necessary less than the efficiencies of other CCM S^2PFC converters.

7.2.2.2 Interleaved DCM S^2PFC converter with universal-line input voltage

Figure 7.2 shows the voltage-doubler version of the proposed interleaved DCM S^2PFC circuit for the universal line input (e.g. 90-265V_{RMS}).

When the input voltage is in the high line range (180-265V_{RMS}), the range switch SW is always open so that the circuit operation is identical to the circuit in Fig. 1, except the windings N_1, N_2 and inductor L_1, L_2 are split into two windings, respectively. When the input voltage is in the low line range (90-135V_{RMS}), the range switch SW is always open. Therefore, the upper half circuit and the bottom half circuits work alternatively, depending on the polarity of the line voltage. In each half line cycle, the operation of the active half circuit is identical to the circuit operation with narrow line range. But the total dc bus voltage is the sum of two boost output voltages, which is doubled by the voltage-doubler rectifier. So that the hold-up capacitance and the converter power loss can be minimized.

7.3 COMPARISONS AND EVALUATION

To evaluate the proposed interleaved DCM S^2PFC techniques, a brief comparison between the proposed circuit in Fig. 7.2 and the CCM VD CS-S^2PFC in Fig. 7.5 has been done. Both circuits are designed with universal-line-input and 5V/90A-output. The switching frequency is designed to be 100 kHz in both circuits. Both circuits are designed to meet IEC1000-3-2 standard with about 15% margin on the input current harmonics. Simulation models of both circuits have been developed to analysis and compare the input current ripple and differential-mode (DM) EMI filter size.

Figure 7.6 shows the simulated CCM S^2PFC circuit input current waveform (without EMI filter) and its current ripple spectrum, at $90V_{ac}$ line-voltage and full load. With the boost inductor L_B=40μH (each winding) and the CS PFC inductor L_1=16μH (each winding), the line current ripple has 0.32A magnitude at 100KHz switching frequency. Figure 7.7(a) shows the simulated interleaved DCM S^2PFC circuit input current waveform (without EMI filter) at the same line and load condition. In the DCM S^2PFC circuit, boost inductor L_1=L_2=7μH, which has a much smaller inductance than the CCM S^2PFC inductance. Figure 7.7(b) shows the input current spectrum of the DCM S^2PFC circuit without interleaving. It has a 2.7A ripple current at the switching frequency, which is about 9 times larger than the CCM S^2PFC current ripple at the same frequency. Figure 7.7(c) shows the input current ripple spectrum of the interleaved DCM S^2PFC circuit. As can been seen, the current ripple at the switching frequency (100KHz) has been significantly reduced to 0.21A, which is even lower than the CCM S^2PFC current ripple. In the interleaved circuit, the dominated current ripple appears at the doubled switching frequency (200KHz).

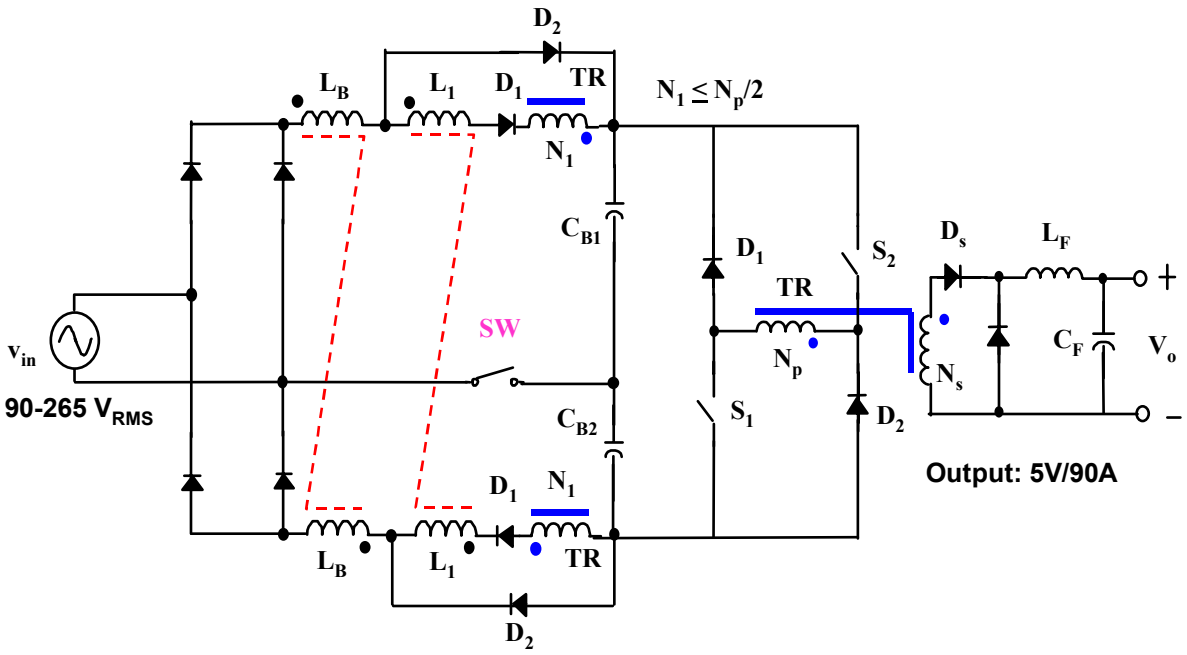
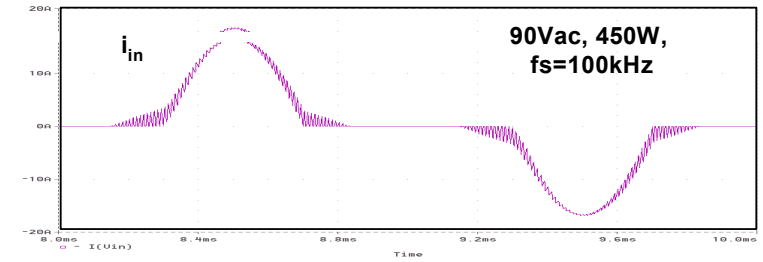
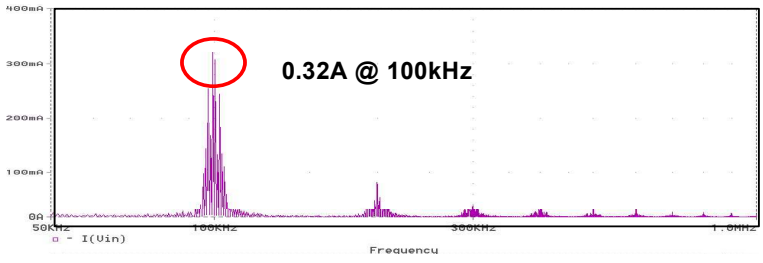


Fig. 7.5 CCM VD CS-S^{2}PFC converter for comparison (Universal line input, 5V/90A output)



(a)



(b)

Figure 7.6. Simulation waveforms of the CCM S^{2}PFC converter in Fig. 7.5: (a) Input current waveform (without EMI filter), (b) Input current ripple spectrum

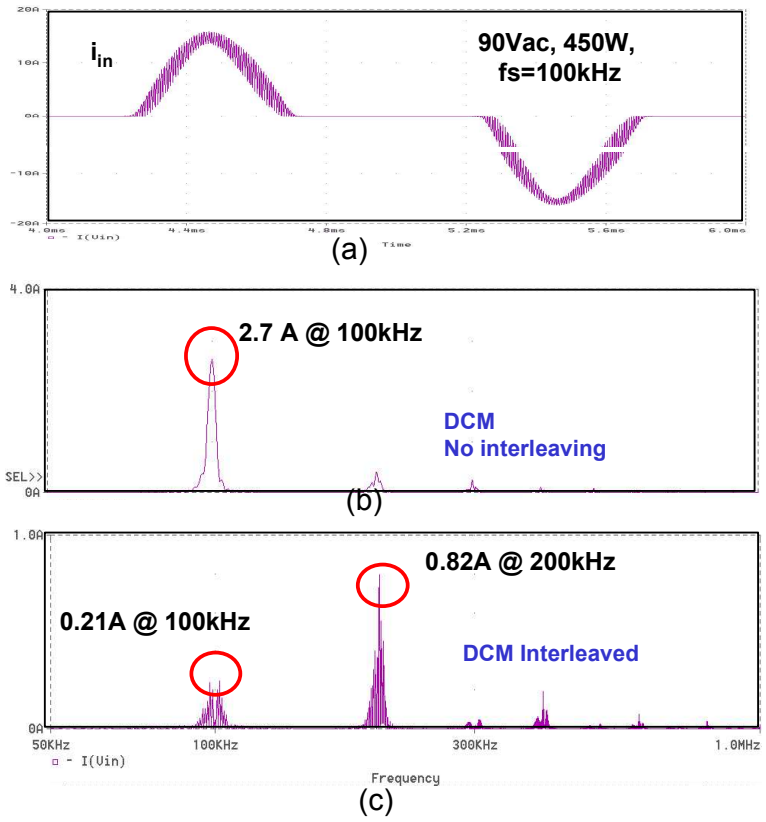


Figure 7.7 Simulation waveforms of the interleaved DCM S^{2}PFC converter in Fig. 7.2:
(a) Interleaved input current waveform (no EMI filter)
(b) Input current ripple spectrum of the DCM S^{2}PFC converter without interleaving
(c) Input current spectrum of the interleaved DCM S^{2}PFC

Table 1. Boost inductor value and core size comparison
(Universal-line input, 5V/90A output)

Circuit	Boost inductors	Peak Inductor current	Core	Total core size
CCM CS-S^{2}PFC	L_B=40µH L_1=16µH	16 A each	E41/17/2 E30/15/7	**15.5 cm^3**
Interleaved DCM S^{2}PFC	L_1=7µH L_2=7µH	18 A each	2* E30/15/7	**8 Cm^3**

Two design programs have been developed to evaluate the core size of the boost inductors in both circuits. Table 7.1 shows the comparison of the core parameters and effective core size, which shows that the interleaved DCM S^2PFC converter has only the half of total core size of the CCM S^2PFC converter. There are two reasons for the small core size in the interleaved DCM S^2PFC converter. First, the DCM boost inductance is much smaller than the CCM boost inductance. Besides, each channel in the interleaved DCM circuit only handles half of the input power, while in the CCM circuit, both inductor L_B and L_1 handle the full input power.

After the boost inductors have been compared, it is also necessary to compare the DM-EMI filter component size in both circuits. Figure 7.8 shows the filter structure and its simulation evaluation model. Based on the current ripple spectrums, the design programs have been developed to design the EMI filter for both circuits to meet VDE Class B standard. Figure 7.9 shows the DM-EMI filter comparison of both circuits. If the total filter capacitance is chosen to be the same value in both circuits, the total filter inductance (=48μH) in the interleaved DCM circuit is much smaller than the total filter inductance (=70μH) in the CCM circuit. The interleaved DCM circuit has small EMI filter size because of the current rippled is small at the switching frequency and the dominated ripple appears at the doubled switching frequency. As the conclusion, both the boost inductors and the DM EMI filter in the interleaved DCM S^2PFC converter are smaller than the correspond components in the CCM S^2PFC converter.

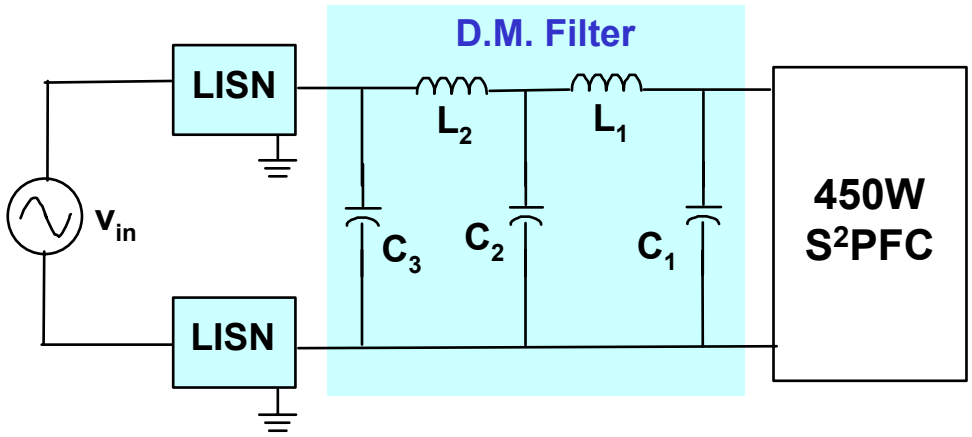


Figure 7.8 Simulation model for EMI filter evaluation

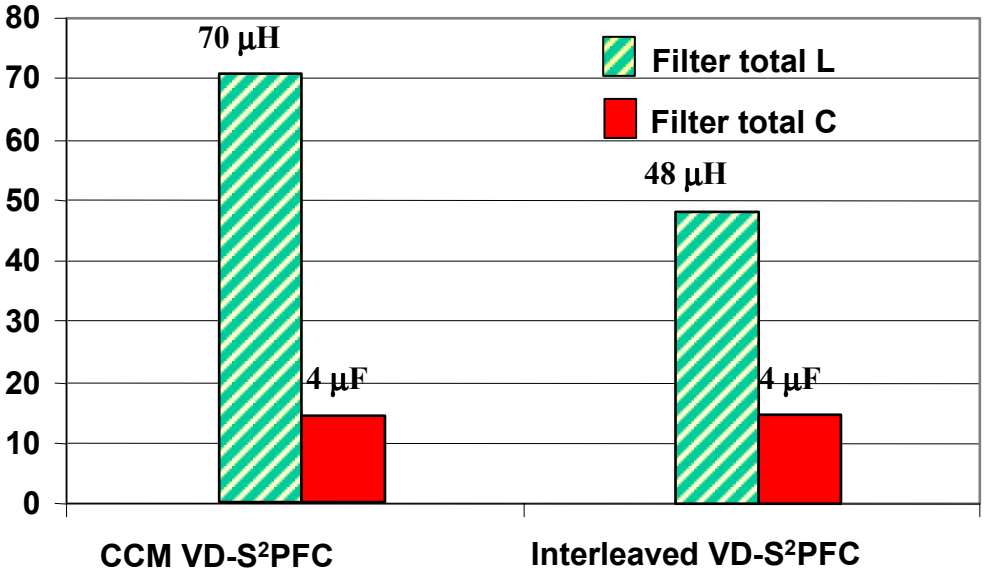


Figure 7.9 DM EMI filter components comparison

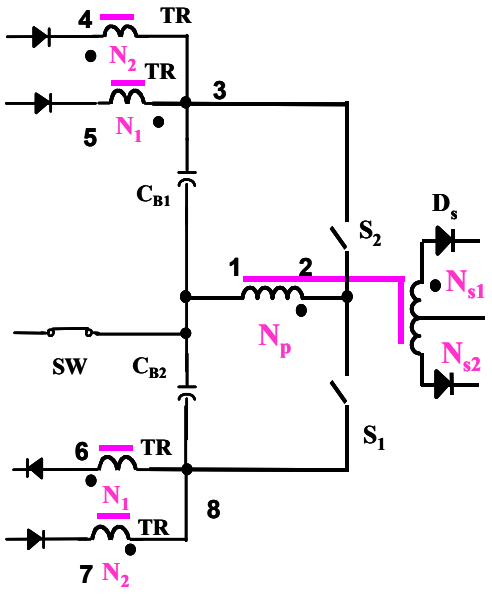
On the other side, compared to the CCM S^2PFC circuit, the interleaved DCM S^2PFC circuit has some disadvantages too. As can been seen from Fig. 7.2, to implement two interleaving channels, the dc/dc transformer should have more windings than the dc/dc transformer in the CCM S^2PFC circuit does. Though more windings does not necessarily require more window area in the transformer since each winding N_1 or N_2 only handles half of the input current, **two** more bobin pins on the primary side of the transformer are needed. So a customized bobin may be required for the DCM S^2PFC transformer. Besides, to achieve interleaving, the dc/dc converter in the proposed circuit must have a topology with a symmetrical driven transformer, while the dc/dc stage in the CCM S^2PFC can be any PWM dc/dc topologies. Therefore, the interleaved DCM S^2PFC may not be suitable for low-power applications, where single-switch dc/dc converters are preferred.

As to the efficiency comparison, as presented in Section 7.2.2, the interleaved DCM S^2PFC can achieve ZVS turn on and has reduced current stress with winding arrangement. Therefore, the proposed converter should at least have comparable efficiency as the CCM S^2PFC does. The experimental comparison on efficiency will be given in Section 7.4.

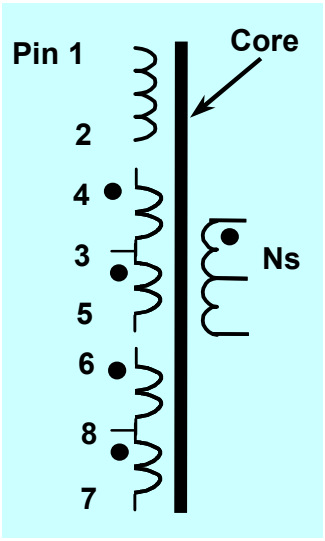
7.4 EXPERIMENTAL VERIFICATION

To verify the operation and performance of the proposed S^2PFC technique, a 5V/90A output, universal line voltage (90-265Vac) interleaved DCM S^2PFC converter shown in Fig. 7.2 was built with 70KHz switching frequency. The following components were used in the implementation of the circuit: L_1=L_2=10μH, Philips E30/15/7-3F3 cores; $C_{B1,2}$ - 1000μF/250V; $S_{1,2}$ – IRPF460 (600V, 0.27Ω); Transformer – Philips E42/21/15-3F3 core with N_p=17T, N_s=1T, N_1=N_2=4T each; $D_{F1,2}$ – 2*81CNQ45; L_F=1.0μH, C_F - 4*2200μF/16V. The control circuit was implemented with the PWM control chip UC3824.

Figure 7.10 shows the winding structure design of this prototype converter. As shown in Fig. 7.10(a), there are five coupled windings on the transformer primary side. Figure 7.10(b) shows that these primary side windings can be grouped into three windings with tapping. In this case, there are altogether 8 pins needed by the primary side windings. The output winding N_{S1} and N_{S2} are implemented with 1-inch wide copper foils to handle the high output current (90A), therefore, N_{S1} and N_{S2} are directly soiled on the PCB board. In this case, a standard Philips E42/21/15 bobin has exact 8 pins to meet the requirement. Figure 7.10(c) shows the winding layer structures of the transformer. A good coupling between the primary winding N_P and secondary winding N_S is very necessary to reduce the leakage inductance on these two windings. On the other side, since the windings N_1 and N_2 are in series to the boost inductors, they do not require good coupling with other windings. Compared to the transformer in previous CCM VD CS-S^2PFC converter, the transformer in the interleaved DCM S^2PFC converter has similar winding area and uses the same core.



(a)



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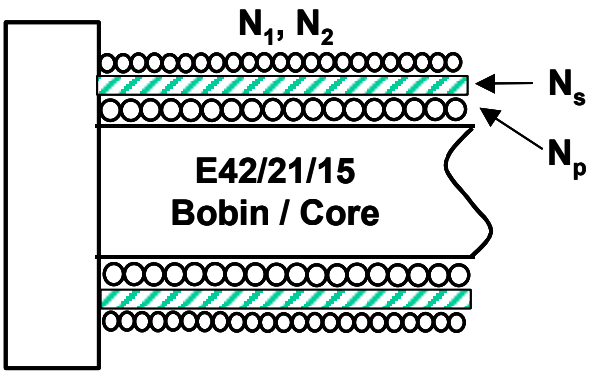

N_1, N_2: 4T each, AWG#18 wire
N_p: 17T, AWG#16 wire
N_s: 1T each, 1" copper foil
Np - Ns need good coupling

(c)

Figure 7.10 Transformer winding structure of the interleaved VD DCM S^2PFC prototype (Universal-line input, 5V/90A-output)

(a) Circuit diagram, (b) windings and pins arrangement, (c) winding layers arrangement

Figure 7.11 shows the measured line voltage v_{in} and the interleaved boost inductor current $i_{L1}+i_{L2}$ waveforms at the nominal line voltage and full load. The total current ripple is already very small. As can been seen in Figure 7.12, the input current harmonics have sufficient margins (~15%) to meet both the IEC1000-3-2 Class D limits at high nominal voltage and its corresponding Japan limits at low nominal voltage. Figure 7.13 shows the switching cycle waveforms of the switch voltages $v_{ds1,2}$ and the boost inductor current $i_{L1,2}$. The two inductor currents have identical, but 180-degree phase-shifted waveforms. Figure 7.14 shows the bulk capacitor voltage stress with the output power changes, with the maximum input line voltage. The total capacitor voltage is always lower than 410V, so that there is sufficient margin for two 250V rated capacitor.

Figure 7.15 shows the measured converter efficiency at the full line range and full load (5V/90A-output). The lowest efficiency is 79.8% at 90Vac, which was measured with the DM-EMI filter. The efficiency value is close to the 450W CCM S^2PFC converter at same line and load condition (80.5% as in Section 6.4.3). At the lowest efficiency point, which happens at 90 V_{RMS} input, the difference on the low-line efficiency is as small as 0.6%.

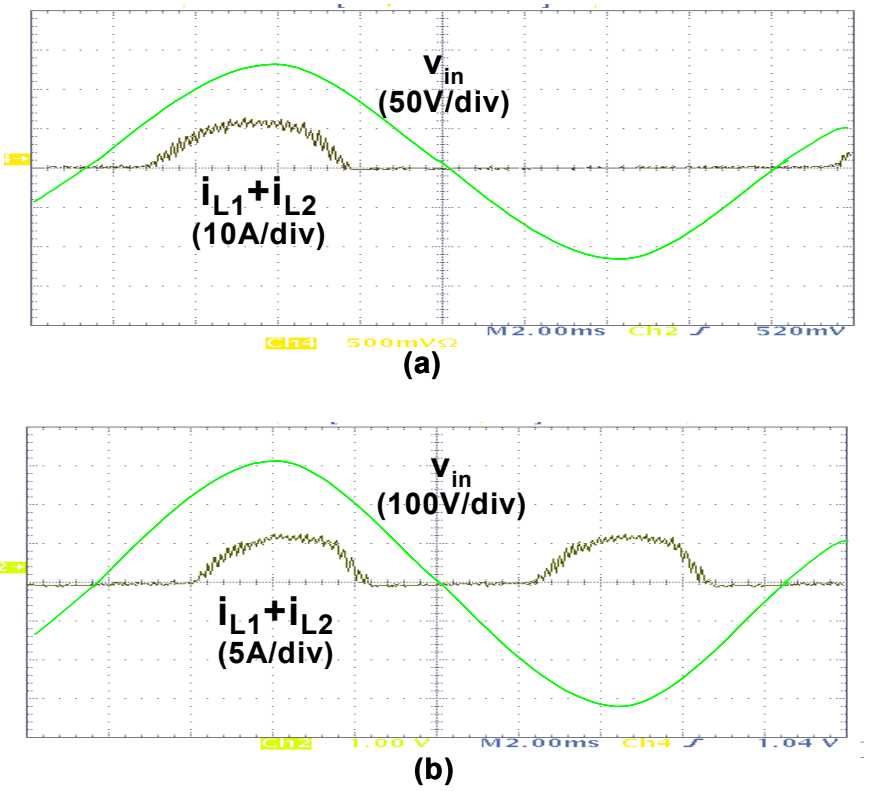

Figure 7.11 Measured input voltage and the interleaved current waveforms at nominal line and full load
(a) V_{in}=100Vac, (b) V_{in}=230Vac

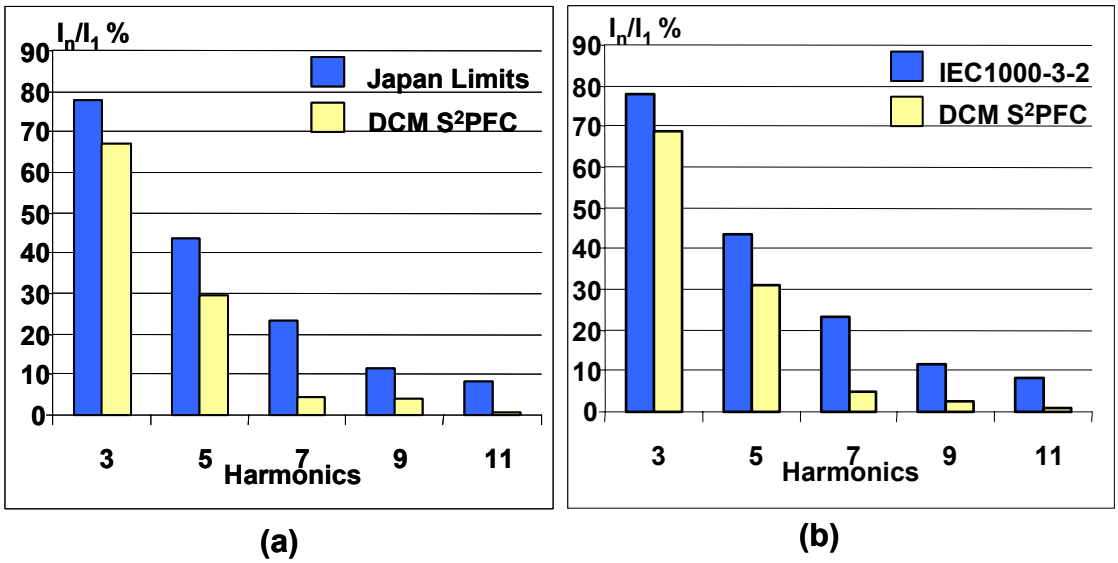

Figure 7.12 Measured input current harmonics comparison
(a) Vin=100Vac, full load.
(b) Vin=230Vac, full load

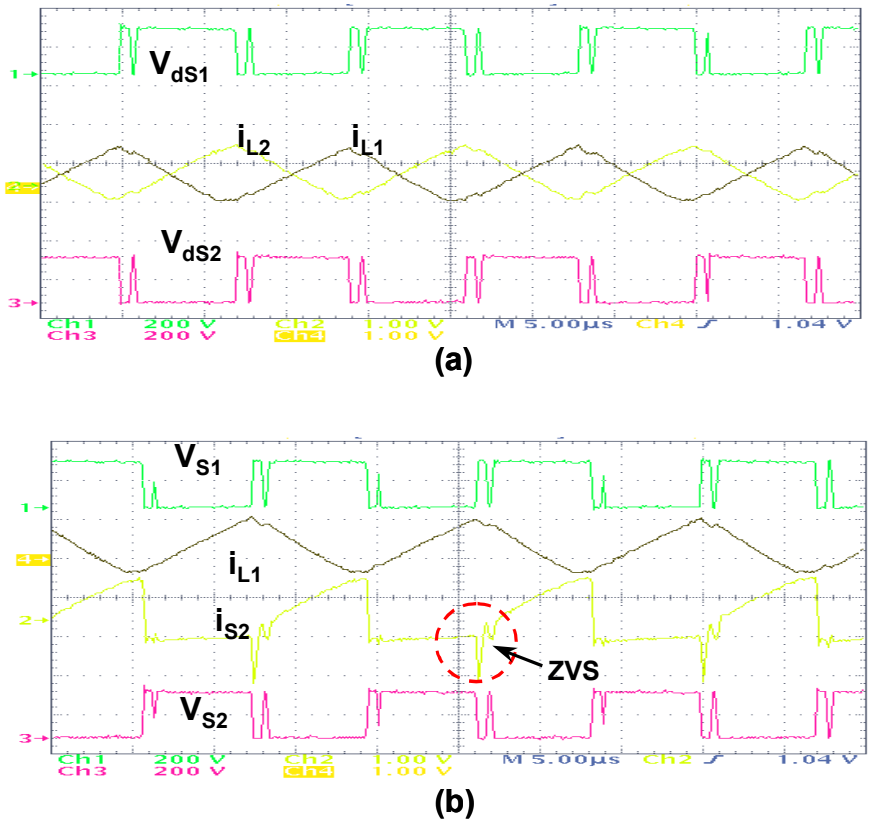

Figure 7.13 Measured switching cycle waveforms (at 90V_{ac} input, 5V/90A output)

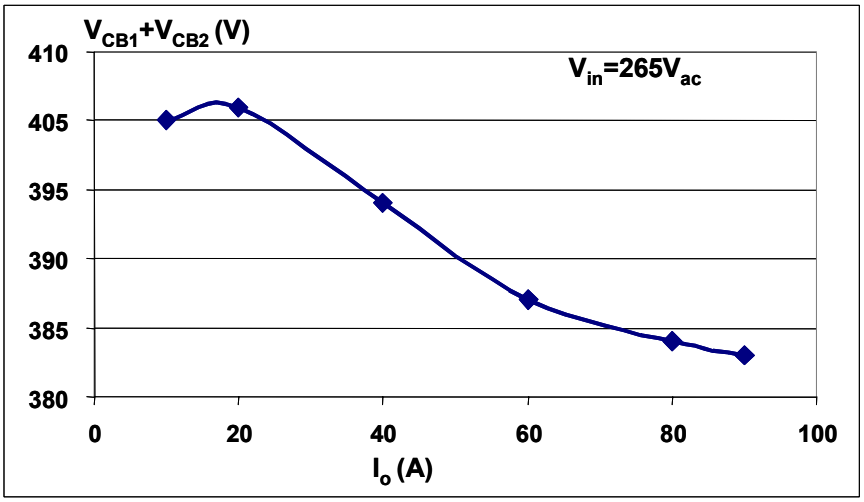

Figure 7.14 Measured bulk-capacitor voltage stress vs. output current (V_{in}=265V_{ac})

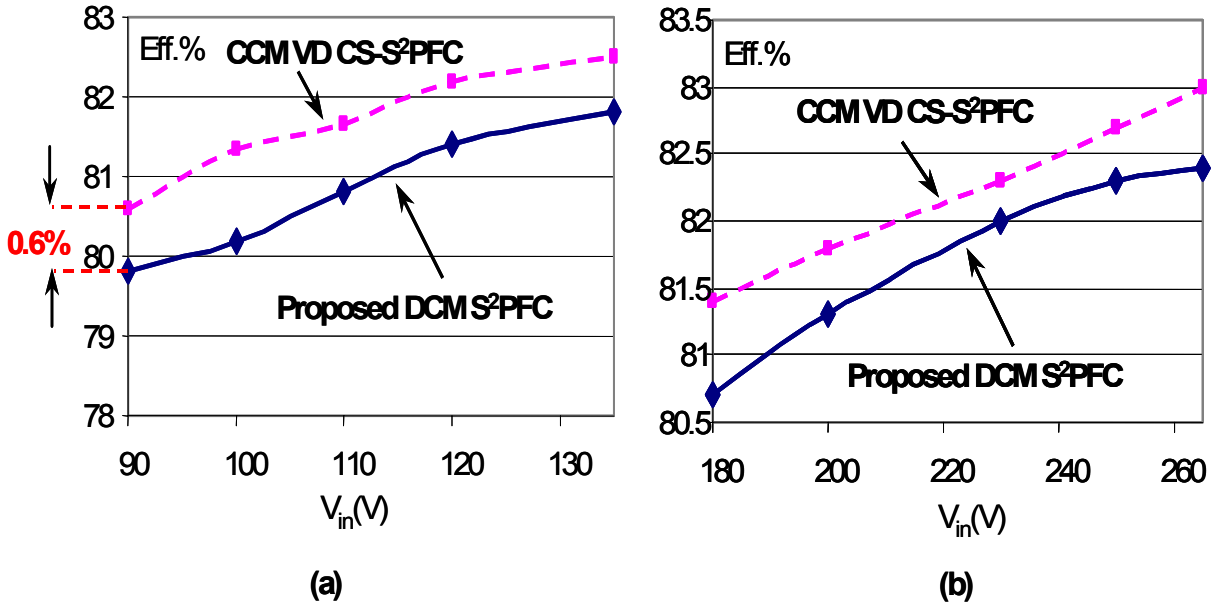

Figure 7.15 Measured efficiency of the interleaved DCM S^2PFC converter with VDR (compared to the CCM VD S^2PFC, both with universal-line input, 5V/90A output)

(a) Low line efficiency, (b) high-line efficiency

7.5 SUMMARY

This chapter proposes a novel interleaved DCM S^2PFC technique. To reduce the input current ripple and input DM-EMI filter size, two interleaving channels are implemented in one S^2PFC circuit with symmetrically driven dc/dc transformer. Besides, in the proposed circuit, the boost inductors also have small total size, since they are operated in DCM mode with small inductance and each inductor handles only half of the input current.

Analysis and comparison show that the proposed circuit has following advantages over the CCM S^2PFC converter:

- Reduced boost inductor and EMI filter size
- Eliminated boost diode reverse-recovery loss
- Zero voltage turn-on of the dc/dc switches
- Reduced switch current stress

On the other side, compared to the CCM S^2PFC converter, it is necessary to point out that the proposed technique has following limitations or disadvantages:

- The DC/DC stage transformer has to be symmetrically driven. Therefore, the DC/DC stage is limited to be symmetric half-bridge, push-pull and full bridge topologies.
- The proposed technique is not suitable for single-switch power supply in the low power range. (i.e. < 200-300W)
- The DC/DC stage transformer needs two additional pins on the primary side bobin.
- The conversion efficiency is slightly lower than that of the CCM S^2PFC converter. (0.6% in the measurement)

Experimental results verify the circuit operation and performance, which shows that the proposed technique has comparable performance to the CCM S^2PFC technique. In general, the interleaved DCM S^2PFC technique can be an alternative solution for high-density and low-cost power supplies with input power from 200-300 to 600 Watts.