Investigation of Power Semiconductor Devices for High Frequency High Density Power Converters

by

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ABSTRACT

The next generation of power converters not only must meet the characteristics demanded by the load, but also has to meet some specific requirements like limited space and high ambient temperature etc. This needs the power converter to achieve high power density and high temperature operation. It is usually required that the active power devices operate at higher switching frequencies to shrink the passive components volume.

The power semiconductor devices for high frequency high density power converter applications have been investigated. Firstly, the methodology is developed to evaluate the power semiconductor devices for high power density applications. The power density figure of merit (PDFOM) for power MOSFET and IGBT are derived from the junction temperature rise, power loss and package points of view. The device matrices are generated for device comparison and selection to show how to use the PDFOM. A calculation example is given to validate the PDFOM. Several semiconductor material figures of merit are also proposed. The wide bandgap materials based power devices benefits for power density are explored compared to the silicon material power devices.

Secondly, the high temperature operation characteristics of power semiconductor devices have been presented that benefit the power density. The electrical characteristics and thermal stabilities are tested and analyzed, which include the avalanche breakdown voltage, leakage current variation with junction temperature rise. To study the thermal stability of power device, the closed loop thermal system and stability criteria are developed and analyzed. From the developed thermal stability criterion, the maximum switching frequency can be derived for the converter system design. The developed thermal system analysis approach can be extended to other Si devices or wide bandgap

devices. To fully and safely utilize the power devices the junction temperature prediction approach is developed and implemented in the system test, which considers the parasitic components inside the power MOSFET module when the power MOSFET module switches at hundreds of kHz. Also the thermal stability for pulse power application characteristics is studied further to predict how the high junction temperature operation affects the power density improvement.

Thirdly, to develop high frequency high power devices for high power high density converter design, the basic approaches are paralleling low current rating power MOSFETs or series low voltage rating IGBTs to achieve high frequency high power output, because power MOSFETs and low voltage IGBTs can operate at high switching frequency and have better thermal handling capability. However the current sharing issues caused by transconductance, threshold voltage and miller capacitance mismatch during conduction and switching transient states may generate higher power losses, which need to be analyzed further. A current sharing control approach from the gate side is developed. The experimental results indicate that the power MOSFETs can be paralleled with proper gate driver design and accordingly the switching losses are reduced to some extent, which is very useful for the switching loss dominated high power density converter design.

The gate driving design is also important for the power MOSFET module with parallel dice inside thus increased input capacitance. This results in the higher gate driver power loss when the traditional resistive gate driver is implemented. Therefore the advanced self-power resonant gate driver is investigated and implemented. The low gate driver loss results in the development of the self-power unit that takes the power from the power bus. The overall volume of the gate driver can be minimized thus the power density is improved.

Next, power semiconductor device series-connection operation is often used in the high power density converter to meet the high voltage output such as high power density boost converter. The static and dynamic voltage balancing between series-connected IGBTs is achieved using a hybrid approach of an active clamp circuit and an active gate control. A Scalable Power Semiconductor Switch (SPSS) based on series-IGBTs is developed with built-in power supply and a single optical control terminal. An integrated package with a

common baseplate is used to achieve a better thermal characteristic. These design features allow the SPSS unit to function as a single optically controlled three-terminal switching device for users. Experimental evaluation of the prototype SPSS shows it fully achieved the design objectives. The SPSS is a useful power switch concept for building high power density, high switching frequency and high voltage functions that are beyond the capability of individual power devices.

As conclusions, in this dissertation, the above-mentioned issues and approaches to develop high density power converter from power semiconductor devices standpoint are explored, particularly with regards to high frequency high temperature operation. To realize such power switches the related current sharing, voltage balance and gate driving techniques are developed. The power density potential improvements are investigated based on the real high density power converter design. The power semiconductor devices effects on power density are investigated from the power device figure of merit, high frequency high temperature operation and device parallel operation points of view.

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To my wife and son

Junhong Zhang and Tyler Wang

Also to my parents

Tiguan Wang and Hongyong Yang

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Chapter 1 Introduction

1.1 Background

High power density converter remains an important topic, and the corresponding studies have been conducted along the development of the power semiconductor devices and power electronics conversion technologies. This work focuses on the high frequency high power semiconductor devices study for high frequency and high power density converter applications. In this chapter, a background description and review will help to define this work and its novelty. Furthermore, we will identify challenges related to the power semiconductor devices issues in the high power density converter design.

1.1.1 Importance of Power Semiconductor Devices for Power Density

The future power converters not only must meet the characteristics demanded by the load, but also have to achieve high power density with high ambient temperature, high efficiency and high reliability. High power density is one of the key drivers and metrics for the advancement of power conversion technologies. Many applications like aircraft with limited space are required to have high power density.

The development of power density for power conversion systems is shown in Fig. 1-1 [1-1]. In the early seventies, the power density is relatively low due to the switching device limitation and passive components volume. With the availability of high switching frequency and high power devices, the power density improves with devices. The power density has been almost linearly increasing from last century to present and the power density number is about ten times improvement. This trend will continue keeping going in the future with the new material power devices introduction. In the near future, with the advent of wide bandgap power devices with even lower power losses and higher switching frequency, much higher power density converters are expected [1-2]-[1-3]. This indicates a fast development of active and passive devices technology and high

demand for high power density converter requirement due to the limited available space and achieved power electronic technologies [1-4]-[1-5].

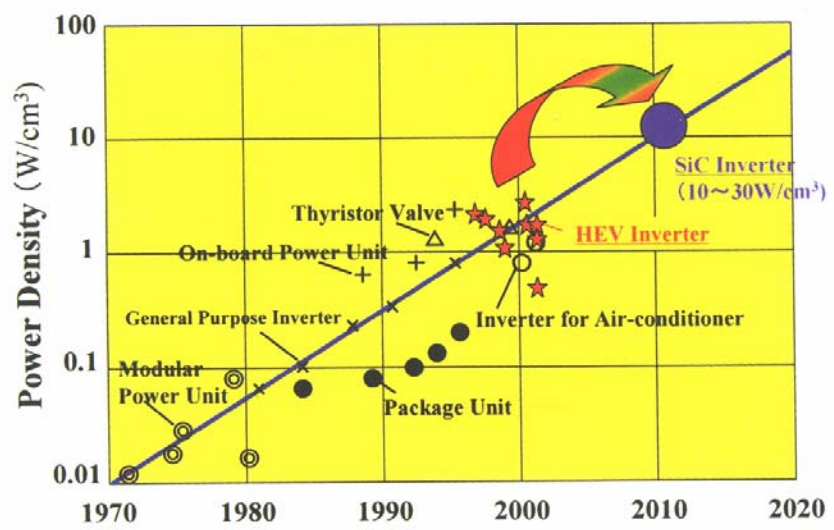
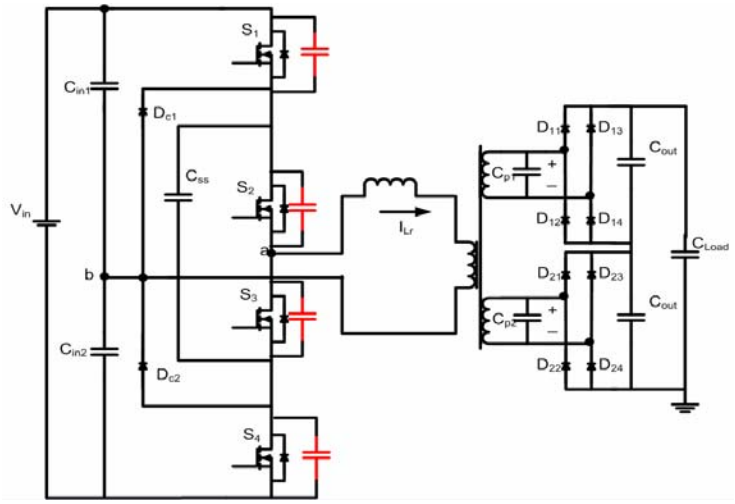


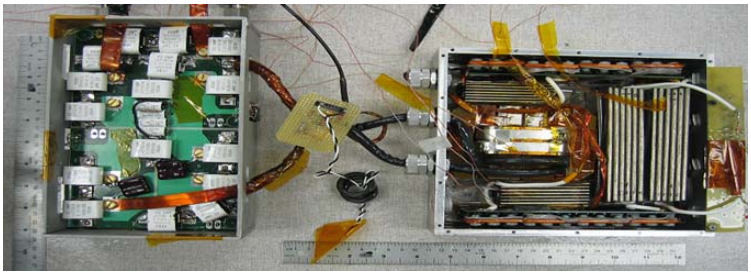
Fig. 1-1 Trend of power density development in power converters [1-1]

To achieve high power density, various topologies and power devices can be selected [1-6]-[1-12]. It is hard to determine which kinds of topologies and devices are much better than others. Normally the soft switching technology and high speed power devices are preferable to low power loss and push high switching frequency. Other approaches like new topology, minimizing power loss, minimizing converter volume, advanced thermal management, and system packaging can also benefit the power density improvement.

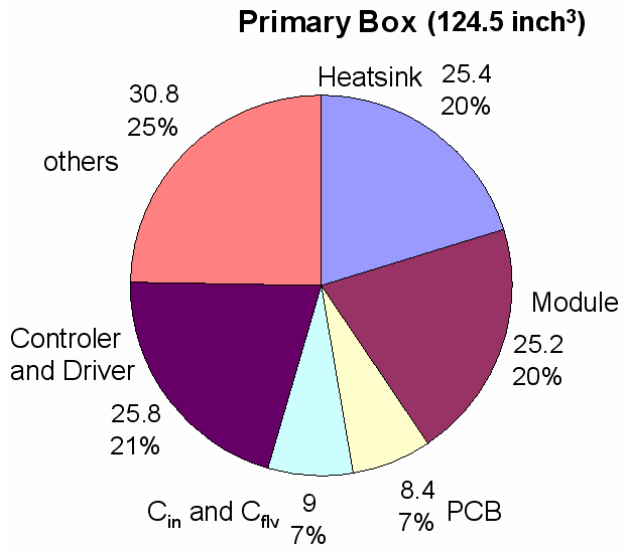
Power density is mainly determined by passive components and thermal management system if the semiconductor devices are properly selected [1-13]-[1-15]. A design example is shown in Fig. 1-2 for a 30 kW parallel resonant converter (PRC). The system structure and control strategy are optimized to achieve the better performance. The passive components and cooling system are customized. The components volumes of the whole system breakdown are shown in Fig. 1-2. It is shown that the passive components (transformer and capacitor) contribute big volume space, which lowers the system power density [1-16]-[1-18].

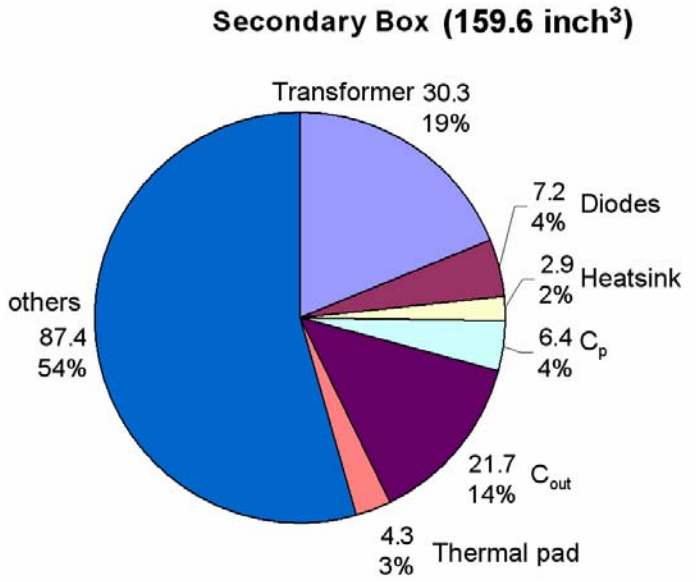


(a) Schematic



(b) Hardware implementation





(c) Components volume breakdown

Fig. 1-2 A 30 kW parallel resonant converter (PRC) and its volume breakdown (Power density: primary side: 241 W/inch^3, secondary side: 188 W/inch^3, whole converter: 106W/inch^3)

Basically there are two approaches to achieve high power density. One is to reduce the converter volume, the other one is to increase the power level as shown in Fig. 1-3. To realize the first approach, the common practices are to select devices with smaller package, and to decrease passive components and cooling system volumes. To select small volume power devices, the low loss, high speed and better thermal performance power devices are preferable. For how to reduce passive component volume from the magnetic technique point, many works have been done by other researchers [1-14]-[1-15]. Also by using advanced cooling system it can reduce heat sink size and improve heat dissipation effect. However, all these approaches may result in device power loss increase and heat sink temperature rise. On the other hand, adding more silicon in the converter is also an effective way to increase power density. This approach is related to the novel power device development or optimum usage of existing power devices [1-19]. So the high current and high voltage devices with fast switching speed are desirable. However the high power, low loss and fast switching devices are not easily available.

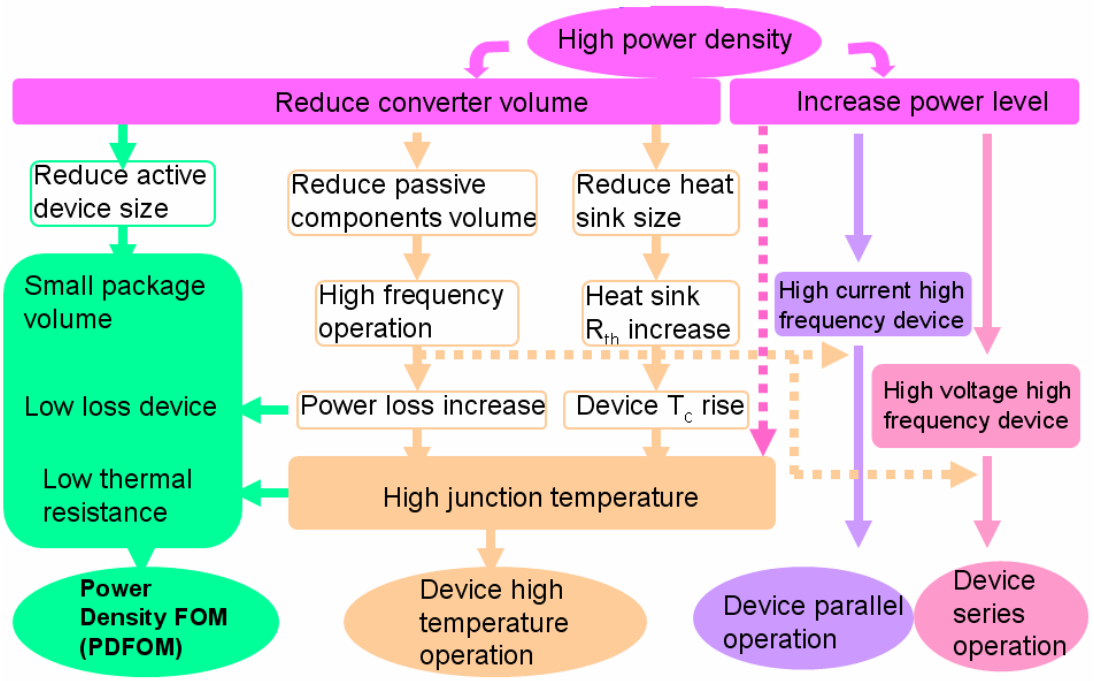


Fig. 1-3 Approaches to achieve high power density

All the approaches discussed above may benefit from the device to operate at high switching frequency. From the power density standpoint, the higher switching frequency operation can help to reduce the passive components size. Also the system dynamic performance is improved. However, the power losses associated with the high switching can prohibit semiconductor devices from operation at higher frequencies. The device thermal system for high temperature operation may be unstable and eventually leads to the destruction of the power devices. High switching frequency and high power devices can be achieved by parallel or series the low power device, because the low power devices have better thermal performance and can operate at high frequency. The future "ideal" power switches are expected to have the attributes like minimal conduction loss, switching loss and low thermal resistance.

1.1.2 State-of-the-art Power Semiconductor Devices for High Power Density

The advancement of power semiconductor devices is the main driving force behind the rapid development of power electronics technology [1-20]-[1-21]. High switching frequency and low loss are often desirable for performance, cost, and size benefit of a

system [1-22]-[1-23]. For example, high switching frequency can lead to smaller passives components – inductors, capacitors, and transformers; low loss can lead to better thermal performance for a given power converter. In addition, the dynamic performance can be improved with increased control bandwidth, which is directly related to the switching frequency.

Power electronics converters mainly employ semiconductor components. However, power devices for switching mode converters have distinct characteristics, like high operating frequencies, thermal performance, and safe operation area etc. In practice, the power devices are complex components, often at the heart of circuit performance and easy to damage. **Fig. 1-4** shows the typical applications for different power levels and switching frequencies of power devices [1-17].

Power semiconductor devices always drive the power converter high power density development. In the early seventies, the silicon controlled rectifier (SCR) and gate turn-off thyristor (GTO) operate at less than hundreds of Hz. In the high power converters where the switching frequency is not a big concern, the SCR, GTO etc bipolar power devices are mainly selected. The power converter based on these devices have very bulky volume and low power density.

With the advent of voltage controlled devices like insulated gate bipolar transistor (IGBT) and power MOSFET, high frequency high power density converter comes into being. In industrial medium- and high-power (hundreds of kWs to MWs), and medium- and high-voltage (>2kV) converter applications, the state-of-the-art semiconductor switching devices are high voltage Insulated Gate Bipolar Transistors (IGBT) and hard-driven Gate-Turn-off (GTO) thyristors such as Integrated Gate Commutated Thyristors (IGCT). High voltage IGBT has significantly improved switching performance over the conventional GTO but their switching frequency is still limited to about 1-10 kHz.

In the low power applications, high speed power devices are preferable to improve the switching frequency and shrink the passive components volume. Even higher power density converters are expected with the availability of high frequency low loss wide bandgap power devices. However the device power rating may limit their application in high power converters.

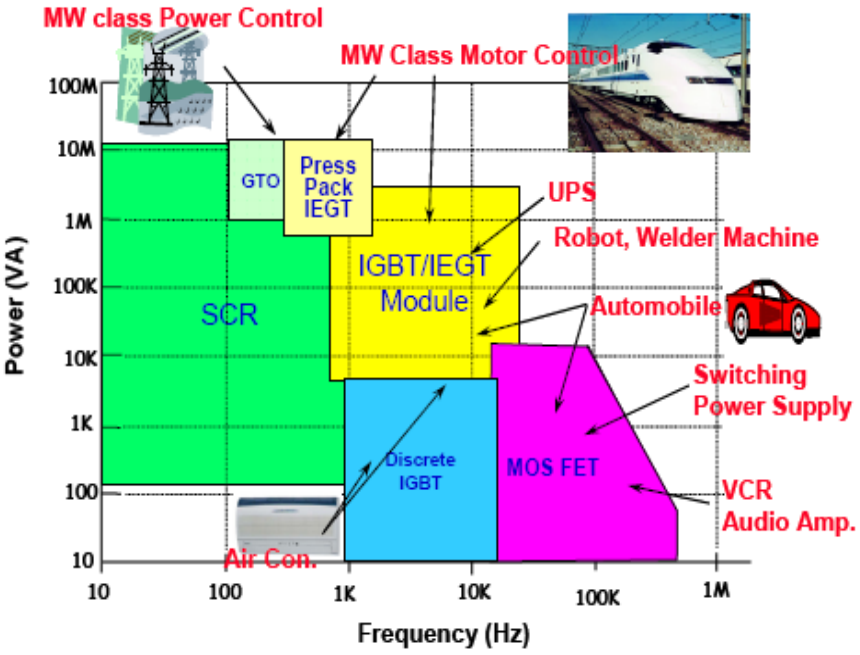


Fig. 1-4 Power device applications VS switching frequencies

The future 'ideal' power devices are expected to have the attributes listed in Table 1-1. Research into new power device is simultaneously achieved as many of these ideal conditions in one device as possible. Power bipolar structures, such as bipolar transistors, PIN diodes, IGBT and thyristors have very low on-state losses because their stored charge modulates the on-state resistance [1-20] [1-24]-[1-26]. Because bipolar devices operate on the principle of stored charge, they require significant power to control and switch slowly. They have relatively high switching losses and are relatively difficult to use. Power MOSFETs on the other hand require nearly no stored charge to operate. They switch very fast and have very low switching losses, require very little power for their control, and are relatively easy to use. However they have a very high on-state resistance and thus dissipate a large amount of power in the on-state.

Table 1-1 Attributes of the ideal power semiconductor devices

- ✧ Minimal power loss in the on state
- ✧ Minimal power loss during switching
- ✧ Minimal power loss in the off state
- ✧ Minimal power required to control operation

- ✧ Easy to use
- ✧ Inexpensive

1.2 Research Challenges and Scopes

The approaches to improve the power density from the active device part form the starting point of this research. To realize these approaches, many challenges still exist although some works have been done.

Firstly, when design the high power density converter, how to select the power devices becomes an important issue [1-25]. In the high power density conversion application, the smaller volume of the components are required, the operating frequency of power circuits must increase to hundreds kilohertz range, which makes the power loss of semiconductor devices more important. To design the high power density converter, the smaller package and lower power loss semiconductor power devices are preferable. In studying the total power dissipation of power devices, it is usual to consider the conduction loss by the on-resistance and the switching loss by the charging and discharging of the input capacitance. For the smaller package area power devices, the higher thermal resistance combining the power losses may generate high junction temperature rise, which limits the power devices high frequency operation. From the power density standpoint, a new power semiconductor device figure of merit is needed to evaluate the commercial devices for high power density converter design. Several device figures of merit have been developed by previous researcher. However no figure of merit is available from the power density point of view.

Secondly, to improve the power density, the practical ways are to minimize the converter volume, increase the switching frequency, or operate the power devices at high case temperature to shrink heatsinks size. The power devices high case temperature and high frequency operation generate higher power losses that further improve the device junction temperature. One way to achieve high temperature operation is to use devices with intrinsic high temperature capability, such as future devices based on wide bandgap semiconductors – SiC or GaN. It is equally important to understand the true physical

limitations for a semiconductor device – Si based commercial devices as well as future SiC devices, and to fully utilize its capability for given applications. The previous work mostly concentrates on the device structure, processing limitation on the high temperature operation. Some papers talk about the conduction loss, switching loss change performance at high junction temperature [1-27]-[1-32]. However, the thermal stability issue at high temperature needs to study further.

Thirdly, to improve the switching frequency operation to reduce passive components volume, the low loss, low thermal resistance, high voltage, and high current devices are needed for high power density converters. Among the state of art power devices, the power MOSFET has nearly no stored charge, switches very fast with low power losses. However they have a high conduction resistance and their current rating often does not meet the requirement for a high power converter. Therefore, the power MOSFETs paralleling operation are preferable to decrease the conduction loss and for high current output [1-33]. However, the power MOSFETs parameters may exhibit some discrepancies, and the temperature has strong effects on the conduction resistance. These may bring about the conduction current unbalance during the steady state and switching transient, which results in power loss difference for different MOSFETs, making one device worse than others. The dynamic balance is especially important in power converters employing high frequency, requiring high efficiency or utilizing large pulse currents if the switching loss dominates the total power losses.

It has been reported that power MOSFETs parallel application as the main switch are used in the power factor correction circuit, DC-DC converter and resonant soft-switching inverter etc year ago [1-34]-[1-36]. It is normally believed that the power MOSEFT conduction resistance has a positive temperature coefficient such that the parallel performances are analyzed without paying much attention to the current sharing. The power MOSFETs paralleling operation performances need to be studied further for the high frequency high power density converter.

Next, low voltage, low current device can operate at high switching frequency and has low thermal resistance, so it is a common practice to use low voltage device series connection to achieve high voltage output. Usually, the low voltage IGBT devices are rated high current with low conduction voltage drop and low thermal resistance. However

their voltage rating may not meet the output voltage requirement. The series connection operation of IGBTs is needed for the high voltage output.

One key issue associated with the device series connection is to ensure static and dynamic voltage sharing across the series-connected IGBTs [1-37]-[1-41]. Static balancing can be achieved relatively easily by connection of resistors in parallel with each IGBT. Dynamic voltage sharing is more difficult to achieve. The methods reported thus far for dynamic voltage balancing can be divided into two groups: one concentrates on the power device side (collector to emitter), and the other on the gate side. These methods either have bulky passive components or very complicated gate circuitry which is noise sensitive. More flexible approach needs to be studied for further improvement.

Finally, the gate driving techniques associated with the device parallel and series operation are key factor to achieve better performances. Better gate driving design can minimize the current and voltage unbalance across the devices to achieve low power loss and safe operation. Although many gate driving techniques have been reported so far such as how to minimize the switching loss and gate drive loss, the approaches to balance the current and voltage across the devices from the gate side are not completely done. Therefore the gate driving design considerations are explored from the power devices parallel and series operation standpoint.

1.3 Dissertation Organizations

The above approaches and challenges form the motivations of the dissertation. The dissertation is organized as follows.

In **Chapter 2**, based on the reviews of the related power device figures of merit, several new power semiconductor devices figures of merit are developed to compare and select the device for high power density converter design. These figures of merit can help to evaluate the power devices from power loss, thermal performance and power density points of view. For the future wide bandgap material power devices, the benefits for high power density are also investigated. The practical design example is conducted to validate the power density figure of merit.

In **Chapter 3**, the power device high temperature operation characterizations are investigated. Firstly the power MOSFETs DC blocking characteristics are studied experimentally and analytically to identify the electrical and thermal limitations at higher junction temperature. The loss characteristics including the switching loss, conduction loss, and leakage power loss are tested and analyzed at higher junction temperature. Then the thermal stability criterion is developed to investigate the high frequency operation at increased case temperature. Some of the analyses are applied to SiC based power MOSFETs, whose high temperature operation performances are predicted and compared with Si power MOSFETs. The thermal stability model and pulse power characterizations are developed to provide the design guideline for high temperature pulse power converter application. The high temperature operation effects of power devices on power density are also investigated.

In **Chapter 4**, the power MOSFETs parallel operation analysis is presented for understanding and controlling the conduction state and switching transient current sharing between parallel MOSFETs. The power MOSFETs parameters mismatch effects are introduced firstly. The conduction state and switching transient current unbalance are analyzed for the selected power MOSFETs considering the temperature effect, power stage parasitic inductance and gate driving design. The current balancing approach is developed and verified with the experiments, which can reduce the switching losses to some extant.

Due to the power MOSFET die parallel with increased input capacitance, high gate driving loss is generated. The gate driving design techniques are explored for the device parallel operation. A self-power resonant gate driver is proposed and implemented, which can save the external driving power supply and driving power loss.

Then, **Chapter 5** presents the development of the device series operation based on series-connected, low voltage, high frequency IGBTs to achieve higher voltage ratings while preserving high switching frequency capability. The active gate control with the over voltage sensing is implemented in the device series connection. The voltage balancing and IGBT tail current control techniques are developed and discussed firstly. Then, the schemes on gate driving, communication, power supply, and packaging are described. Based on the developed series technique the scalable power semiconductor

switch (SPSS) concept is proposed. The hardware implementation is conducted and the concept is verified by the experimental results. A scalable power semiconductor switch based on series connection of IGBTs is developed. The SPSS prototyping and experimental results are presented. The results show that all design specs for SPSS are fully met and the SPSS is a viable concept to achieve high voltage, high power, and high frequency switching capability.

Finally, the conclusions and future research plan are presented.

Chapter 2 Power Semiconductor Device High Power Density Application

2.1 Introduction

In the high power density conversion application, the smaller volume of the components are required, and the switching frequency of power circuits should be increased to hundreds kilohertz range, which makes the power loss of semiconductor devices more important. To design the high power density converter, the smaller package and lower power loss semiconductor power devices are preferable. In studying the total power loss of power devices, it is a common practice to consider the conduction loss by the on-resistance and the switching loss by the charging and discharging of the input capacitance. For the smaller package area power devices, the higher thermal resistance combining the power losses may generate high junction temperature rise, which limits the power devices high frequency operation.

There are many device figures of merit to describe the device performances from different standpoints. In this chapter, firstly gives a brief review of several existing figures of merit related to the power device loss and thermal characteristics which are the main concerns for the high power density converter design. The advantages and shortcomings of the reviewed device figures of merit are analyzed. Then from the power density point of view, a new power density figure of merit (PDFOM) is derived which is directly relative to the device power loss, and dependent on the semiconductor and package materials. To evaluate the impact of wide bandgap power devices on the power density, several unipolar power devices figures of merit are derived for comparison. At last, a design example is shown to develop the design approach for the high power density converter application based on the new figure of merit.

2.1.1 Power Device Figures of Merit Review

Referring to the previous literatures, several figures of merit relative to the power device characteristics have been performed, which can be used to evaluate the semiconductor materials, power loss and package performances.

In 1983, Baliga derived a figure of merit [2-1]

$$BFOM = \varepsilon\mu E_G^{\,3} \tag{2-1}$$

where ε is the dielectric parameter, μ is the mobility and E_G is the bandgap of the semiconductor. The BFOM especially applies to systems that operate at lower frequencies where the conduction losses are dominant. In the high switching frequency application where the power MOSFET switching loss is dominate, it is not accurate to evaluate the device loss performance by BFOM.

In Baliga's paper published in 1989 [2-2], it was assumed that the switching losses are caused by the charging and discharging of the input capacitance of the power FET. A good indication of the power device quality can be obtained by considering the conduction loss and switching loss together. Use the product of these parameters and define a figure of merit for devices operating at high frequencies.

$$BHFFOM = \frac{1}{R_{on,sp} C_{in,sp}} \tag{2-2}$$

where $R_{on,sp}$ and $C_{in,sp}$ are the specific on-resistance and input capacitances. This figure of merit has the dimension of frequency. It is appropriate for evaluating the high frequency switching capability of power devices.

In 1995, Kim [2-3] proposed the power device figure of merit. Under an inductive or capacitive load, the switching loss of the device mainly results from the output capacitance C_{oss} rather than the input C_{iss}. The on-resistance R_{on} and output capacitance C_{oss} are closely related to the device area by their specific values. This leads to the figure of merit by taking the product of them as follows,

$$NHFFOM = \frac{1}{R_{on,sp} C_{oss,sp}} \tag{2-3}$$

where $C_{oss,sp}$ is the specific output capacitance. Also this figure of merit has the same dimension of frequency. In the low power converter, the device switching speed is very fast. It is a good indicator for including the output capacitor induced power loss. For the

high power devices, the switching loss is mainly determined by the switching time and frequency. This will bring more error to compare the total power loss for different power devices by NHFFOM.

The previous three figure-of-merits evaluate the power devices from the power loss point of view. In the high power density application, the thermal and structural characteristics as well as the electrical characteristics of high power devices are also important. Guidelines should be provided to make the optimum selection for high frequency and high power uses.

In 1990 Ohmi and Takeuchi [2-4] proposed a figure of merit(O) for power devices.

$$FOM\ (O) = \frac{V_c I_c}{V_{on} t_{off} S} \tag{2-4}$$

where V_c is the rated voltage, I_c is the rated current, V_{on} is the on-state voltage, t_{off} is the turn-off time, and S is the chip area. The FOM(O) is almost independent of the power rating, because it represents the electrical performance of the semiconductor chip.

In 1993, another figure of merit was proposed by Hisao Shigekane etc that take into account thermal and structural factors of the package [2-5]. From the practical viewpoint, this figure of merit takes into account thermal and structural factors, such as thermal resistance and stray inductance in the package.

$$FOM\ (F) = \frac{V_c I_c}{V_{on} t_{off} S R_{th} L_s} \tag{2-5}$$

where R_{th} is thermal resistance, L_s is stray inductance. Hisao indicated that although the FOM(O) for IGBT is greater than that for GTO, which means that the chip performance is superior for IGBT, the FOM(F) for IGBT is lower than for GTO. This can be attributed to the difference in package structures between the two devices. The GTO is assembled into a flat package with lower R_{th} and L_s as compared with those of module type packages into which IGBTs are built.

The previous power device figures of merit can be used to evaluate the power devices from different aspects. However no figure of merit is available for the power device in the high power density conversion. Today high power density converters are required due

to the harsh environment and limited space. It is important to develop the new figure of merit to make the optimum selection of power devices for high frequency and high power density conversion.

2.2 Derivation of New Power Device Figures of Merit

In the high power density converter application, low power loss devices are preferable. In order to minimize the power losses in the power devices, many efforts have been done to reduce the on-resistance of the device. This can be achieved by increasing the device die area and by reducing the specific on-resistance. In high frequency application, as the die size increases, the increase in the input capacitance produces a corresponding increase in the switching losses that offsets the reduction in the conduction losses achieved by the decrease in the on-resistance. Thus it is necessary to not only reduce the on-resistance but the input capacitance as well.

It is possible to quantify the benefits of power devices for the high power density converter design. It is clear that the lowest power losses can be achieved by reducing the on-resistance and input capacitance. The high power density requirement can be achieved by reducing the package area and high frequency operation to shrink passive components volume. However the device may be heated due to the increased power losses and thermal resistance. From the thermal stability point of view, the junction temperature limits the power device for high power density application [2-6]-[2-8]. The proposed figures of merit is derived from the power loss standpoint and expressed in terms of the device's electrical characteristics, thermal and package performances [2-9]-[2-10].

The capacitances of MOSFET affect the overall switching performance. During the turn-on and turn-off transients, the capacitance C_{gs}, C_{gd} and C_{ds} are not constants but vary with the voltage applied across them. In particular, the switching losses generate due to charging and discharging of the gate input capacitance. The power MOSFET turn-on process is sketched in Fig. 2-1.

During Q_{gs} period, gate current charges capacitance C_{gs}. When the gate voltage rises to threshold voltage, the MOSFET current begins to increase. At the end of Q_{gs} it reaches the steady state value i_D. And the gate voltage reaches the miller flat value. Then gate

current begins to charge capacitance C_{gd} which leads to the decrease of the drain-to-source voltage. At the end of Q_{gd} the drain-to-source voltage reaches zero. Then the gate voltage continues to increase to the gate driver bus value. From the turn-on plots it can be derived that the switching loss generates during gate charge interval Q_{gs} and Q_{gd}. The gate charge time can be calculated by,

The drain current rise time:

$$t_1 = \frac{C_{iss} \cdot i_D / g_m}{i_g} \tag{2-6}$$

The drain-to-source voltage fall time:

$$t_2 = \frac{Q_{gd}}{i_g} \tag{2-7}$$

where C_{iss} is the input capacitance, g_m is the transconductance, i_g is the average gate current. Normally, the gate-to-source charge is much smaller than the gate-to-drain charge. Here only consider the contribution of gate-to-drain charge to the switching loss. For turn-off process, similar calculation can be derived.

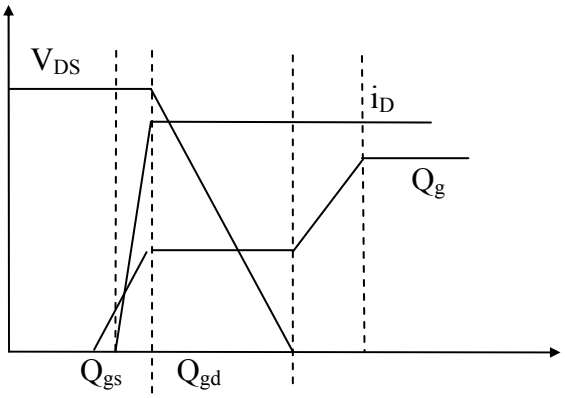


Fig. 2-1 Switching transient waveforms for a power MOSFET (turn-on)

For power MOSFET application in the high frequency power conversion system, the total power loss can be derived as,

$$P_{loss} = I_{rms}^2 R_{on} + V_s i_s f Q_g / (2 i_g) \tag{2-8}$$

where the first term stands for the conduction loss, the second term stands for the switching loss. f is the operating frequency and $Q_g(i_g)$ is the gate charge (current) during the switching period. Note that the switching power loss term accounts for both the charging and discharge of the input capacitance during each cycle. V_s and i_s are the switching voltage and current respectively. I_{rms} is the current that generates the conduction power loss. R_{on} is the conduction resistance.

During the switching period, the gate-to-drain capacitance charge Q_{gd} dominates the switching loss. Here we only consider the Q_{gd} 's contribution to the switching loss. And the on-resistance and the input capacitance are related to the area of the device by their specific values. So the above equation can be rewritten as

$$P_{loss} = I_{rms}^2 R_{on,sp} / A + V_s i_s f Q_{gd,sp} A/(2i_g) \tag{2-9}$$

where $R_{on,sp}$ and $Q_{gd,sp}$ are the specific on-resistance and gate charge, A is the chip area. These device parameters are both determined by the material characteristics and the device cell design. A good measure of the device quality can be obtained by considering the two parts.

As the area of the device increase, the first term decreases and the second term increases. Consequently, the power loss exhibits a minimum value when $dP_{loss}/dA = 0$.

$$P_{loss,\min} = 2I_{rms}\sqrt{V_s i_s f/(2i_g)\cdot R_{on,sp} Q_{gd,sp}} \tag{2-10}$$

In the case of an abrupt one-dimensional junction fabricated in a uniformly doped semiconductor layer, the voltage is supported in a depletion layer with a linearly decreasing electric field. This field has its maximum value at the junction, and is equal to the critical electric field E_c at breakdown. From this field distribution, the doping concentration N_B and the depletion width W_B required to support the voltage V_B can be derived.

$$N_B = \varepsilon E_c^2/(2qV_B) \tag{2-11}$$

$$W_B = 2V_B / E_c \tag{2-12}$$

Using the above doping and thickness, the ideal specific on-resistance is given by.

$$R_{on,sp} = 4V_B^2 / (\varepsilon \mu E_c^3) \tag{2-13}$$

where μ is the carrier mobility.

The gate charge per unit area is given by,

$$Q_{gd,sp} = kV_s \varepsilon / W_s = k\sqrt{V_s / V_B}\,\varepsilon E_c / 2 \tag{2-14}$$

where the depletion width W_s has been assumed to be due to the applied drain to source block voltage V_s, k (<1) is the gate to drain overlap ratio. From above equation (2-13) and (2-14), one can derive equation (2-15).

$$R_{on,sp} Q_{gd,sp} = 2kV_B \sqrt{V_B V_s} / \mu E_c^2 \tag{2-15}$$

So the minimum power loss can be expressed as,

$$P_{loss,\min} = 2I_{rms} V_B \sqrt{V_s i_s f / i_g} \cdot 1/(E_c \sqrt{\mu}) \tag{2-16}$$

From equation (2-16), we can see that the minimum power loss is inversely proportional to $k_p = E_c \sqrt{\mu}$. It can be concluded that the best semiconductors for high frequency power switching applications should exhibit a large critical electric field for breakdown and should have higher carrier mobility. This results in minimizing the power loss.

From the power loss equation (2-16), it can be concluded that in order to improve the efficiency of power converter, it is desirable to maximize the value of k_p. A quantitative comparison is provided in Fig. 2-2, where the power loss is plotted as a function of k_p for some specific frequencies of operation, 100 kHz, 200 kHz and 500 kHz. This calculation is based on a high power density resonant converter operation conditions with resonant

peak current of 180A. The power MOSFET rating voltage/current is 600V/437A, switching at 300V/80A.

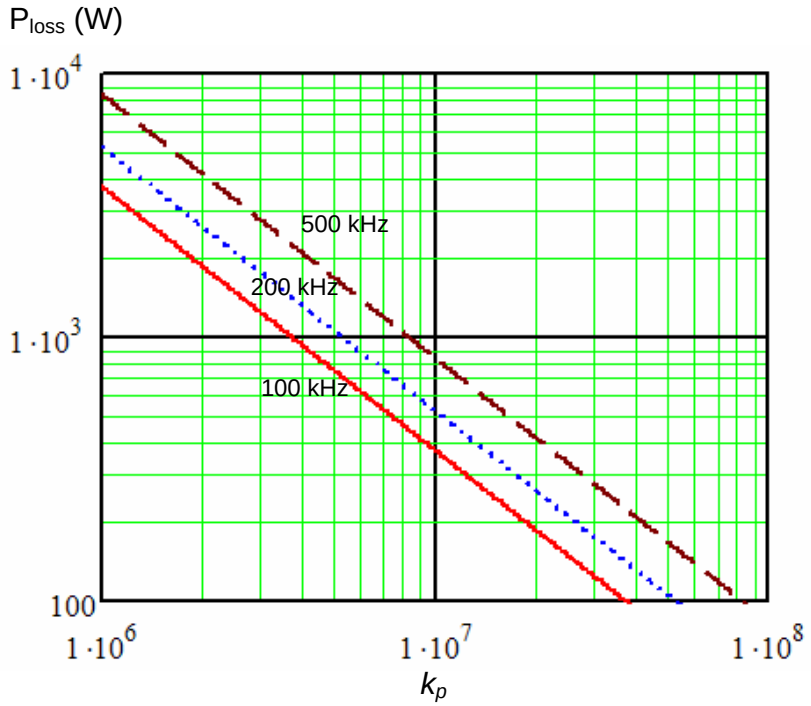


Fig. 2-2 Power loss for a power MOSFET as a function of k_p

To compare devices thermal handling capability, the junction to die attachment thermal resistance can be express as

$$R_{th} = \frac{W_{die}}{\sigma_{th} A_{opt}} \tag{2-17}$$

Here W_{die} is the semiconductor die thickness, σ_{th} is the thermal conductivity of the material and A_{opt} is the optimum die area. Therefore, we can calculate the device's junction to die attachment temperature rise as

$$\Delta T_{\max} = P_{loss,\min} R_{th} = P_{loss,\min} \frac{W_{die}}{\sigma_{th} A_{opt}} \tag{2-18}$$

Utilizing (2-16), one has

$$\Delta T_{\max} = \frac{2V_D I_D f W_{die}}{i_{g,av}} \frac{Q_{gd,sp}}{\sigma_{th}} \tag{2-19}$$

Further utilizing equation (2-19) and $W_{ie}=2V_B/E_c$, one has

$$\Delta T_{\max} = \frac{4kV_D^{3/2} I_D f \sqrt{V_B}}{i_{g,av}} \frac{\varepsilon}{\sigma_{th}} \tag{2-20}$$

From (2-20), we can define a high temperature figure of merit (TFOM) for switching power devices.

$$TFOM = \frac{\sigma_{th}}{\varepsilon} \tag{2-21}$$

The above equation is only determined by the semiconductor material thermal conductivity and dielectric constant. The higher the TFOM, the lower the temperature rise under the optimum chip area and minimum power losses.

Table 2-1 Comparison of TFOM for Various Semiconductor Materials (Normalized Against Silicon)

Semiconductor material	Bandgap (eV)	Electron Mobility μ_n(cm^2/Vs)	Hole Mobility μ_h(cm^2/Vs)	Critical Breakdown field Ec (V/cm)	Relative dielectric constant ε	Thermal conductivity σ_{th} (W/m-K)	TFOM $=\sigma_{th}/\varepsilon$
InAs	0.354	44,000	500	40,000	14.5	26.5	0.14
InP	1.344	5,400	200	500,000	14	68	0.44
GaAs	1.424	8,500	400	400,000	13.1	46	0.32
GaN	3.44	900	10	3,000,000	9	110	1.1
Ge	0.661	3,900	1,900	100,000	16	58	0.33
Si	1.12	1,400	450	300,000	11.7	130	1
GaP	2.26	250	150	1,000,000	11.1	110	0.89
SiC(6H,α)	2.86	330~400	75	2,400,000	9.66	700	6.52
SiC(4H,α)	3.25	700	80	3,180,000	9.7	700	6.5

From equation (2-21), we can see that the lower junction temperature rise is inversely proportional to *TFOM*. The calculated *TFOM* for some semiconductor materials is shown in Table 2-1. The semiconductor material data refer to reference [2-7]. It can be concluded that the best semiconductors for high temperature power switching applications should exhibit a large thermal conductivity for power dissipation and should

have smaller dielectric constant. The SiC power devices are estimated 6 times lower junction temperature rise than Si power devices for the same power rating.

From the power density standpoint, to design the high density power converter one has to consider the device area. For the same voltage rating devices, the die thickness is assumed the same. The equation (2-18) is further developed as.

$$\Delta T_{\max} A_{opt} = P_{loss,\min} \frac{W_{die}}{\sigma_{th}} \tag{2-22}$$

Consider the power loss equation, one has

$$\Delta T_{\max} A_{opt} = 2 I_{rms} V_B \sqrt{V_s i_s f / i_g} \cdot \frac{1}{E_c \sqrt{\mu}} \frac{W_{die}}{\sigma_{th}} \tag{2-23}$$

For the same semiconductor material devices and same operation conditions, the right side in (2-23) is constant. This corresponds to the idea device case. For the commercial power devices, one has to consider the device package area A_{pack} which is usually bigger than the bare die area. However if the device package approaches the die dimension and has negligible thermal resistance, this device has the optimum smallest volume for high power density converter design. Also the low junction temperature rise is required for high frequency operation. From this standpoint, the low junction temperature rise and small package area devices are preferable for high density power converter design.

For a real commercial device, one can get,

$$\Delta T_{\max} A_{pack} = P_{loss} R_{th} A_{pack} = (I_{rms}^2 R_{on} + \frac{V_s i_s f Q_g}{2 i_g}) R_{th} A_{pack} \tag{2-24}$$

Further develop the equation (2-24), one can get the minimum value.

$$(\Delta T_{\max} A_{pack})_{\min} = k_c \sqrt{R_{on} Q_g} R_{th} A_{pack} \tag{2-25}$$

where k_c is a parameter related to the device operation conditions. The above equation includes two parts. The first term relates to the device operation circuit conditions. The

second part relates to the device conduction loss, switching loss, package area and thermal characteristics. From equation (2-25), a new figure of merit is derived to evaluate the power MOSFET for high power density application.

$$PDFOM_{MOSFET} = \frac{1}{\sqrt{R_{on}Q_{gd}}\,A_{pack}R_{th}} \tag{2-26}$$

From a general power device standpoint, the PDFOM can be used to compare not only the same semiconductor material devices, also wide bandgap unipolar power semiconductor devices. The state-of-the-art power MOSFETs from a number of vendors are listed in Table 2-2. The calculated PDFOM $_{MOSFET}$ from the datasheet information shows that different commercial devices have different PDFOM $_{MOSFET}$ values which indicate different power density potential improvement for the converter design.

2.3 State-of-the-art Power Device Comparisons

Solid-state devices are being incorporated into many high power density applications to generate fast, high power, high repetition rate pulses. The vendors' datasheets provide a starting point for selecting solid-state devices to design the high power density converter. The methodology to evaluate the power device for high power density application is developed. The power MOSFETs, IGBTs and power Diodes from a number of vendors have been evaluated to determine which kind of device is suitable for high power density based on the switching time, power loss, thermal handling capabilities, and package information consideration. Then the wide bandgap materials based power devices are investigated to see their advantages from the power density point of view.

Table 2-2 State-of-the-art Power MOSFETs comparison matrix

	MOSFET					
Matrix	APT60M75L2LL (APT)	APT60M60JFLL (APT)	APT77N60JC3 (APT)	IXKN75N60C (IXYS)	SPW47N60C2 (INFINEON)	IRFPS40N60K (IR)
$V_{blocking}$(V)	600	600	600	600	600	600
V_{DClink}(V)	300	300	300	300	300	300
$I_{DC}@V_{dclink}$ (A)(25C)	73	70	77	75	47	40
Rds (ohm) (125°C)	0.156	0.126	0.074	0.06	0.13	0.31
Qgd (nC) (300V)	102	125	213	228	114	119
Thermal Resistance Rthjc (K/W)	0.14	0.18	0.22	0.22	0.3	0.22
Package(mm^3)	TO-264 MAX (26*20*5)	SOT-227 (38*25*12)	SOT-227 (38*25*12)	SOT-227B (38*25*12)	P-TO247 (21*16*5)	TO-247AC (21*16*5)
$(Rds*Qgd)^{1/2}*Rthjc*Area$ $((ohm*nC)^{1/2}*K/W*mm^2)$	290	679	830	773	388	449
PDFOM $(10^{-3}/((ohm*nC)^{1/2}*K/W*mm^2)$	3.44	1.47	1.21	1.29	2.58	2.23
Notes	MOS 7	MOS 7	CoolMOS	CoolMOS	CoolMOS	HEXFET

2.3.1 Power MOSFET Comparisons

The state-of-the-art power MOSFETs from a number of vendors are listed in Table 2-2. The calculated $PDFOM_{MOSFET}$ from the datasheet information shows that different commercial devices have different PDFOM values for power MOSFETs which indicate different power density application. Among the listed devices, the power MOSFET from Advanced Power Technology has small normalized thermal resistance and low power loss which allow them use for high power density converter.

2.3.2 Power IGBT Comparisons

The IGBT combines the advantages of the MOS gate structure with the superior low conduction losses of bipolar transistors [2-11]-[2-12]. Two basic concepts are currently sharing the market, the punch-through and non-punch-through concept. The techniques for fast switching comprise a further reduction of lifetime for PT concept and a further reduction of p-emitter efficiency for NPT concept. The basic idea of the field stop-IGBT is to combine the PT and NPT concept together with the very low-doped n-layer and low

emitter efficiency [2-13]-[2-16]. In recent years the soft punch through, trench field stop IGBT come into application [2-17]-[2-22]. Also, IGBT chips have different types of packages. From power loss point of view, derives a high power density figure of merit for IGBT devices comparison.

The IGBT typical output characteristics and switching loss curves as a function of collector current are shown in Fig. 2-3 and Fig. 2-4. Using linear approximation technique, we can get

$$\begin{aligned} V_{ce} &= V_{ce0} + k_v i_c = K_v i_c , \quad K_v = V_{ce0} / i_{co} + k_v \\ E_{on} &= E_{on0} + k_{on} i_c = K_{on} i_c , \quad K_{on} = E_{on0} / i_{co} + k_{on} \\ E_{off} &= E_{off\,0} + k_{off} i_c = K_{off} i_c , \quad K_{off} = E_{off\,0} / i_{co} + k_{off} \end{aligned} \tag{2-27}$$

The IGBT total power loss is the sum of conduction loss and switching loss.

$$P_{loss} = V_{ce} i_{avg} + f(E_{on} + E_{off}) \tag{2-28}$$

The IGBT maximum junction temperature rise can be expressed as the following equation. Here we normalize the conduction loss coefficient to the device area $K_v = k_1 / A_{pack}$.

$$\begin{aligned} \Delta T_{\max} &= P_{loss,\min} R_{th} \\ &= \left(K_v \cdot i_c \cdot i_{avg} + \left(K_{on} + K_{off}\right) \cdot i_c \cdot f\right) \cdot R_{th} \\ &= \frac{2 i_c \cdot f}{K_v} \cdot \left(K_v \left(K_{on} + K_{off}\right) R_{th}\right) \\ &= \frac{2 i_c \cdot f}{k_1} \cdot \left(K_v \left(K_{on} + K_{off}\right) R_{th} A_{pack}\right) \end{aligned} \tag{2-29}$$

From the above equation, we define the IGBT power density figure of merit as,

$$PDFOM_{IGBT} = \frac{1}{K_v (K_{on} + K_{off}) R_{th} A_{package}} \tag{2-30}$$

This term indicates that the bigger the $PDFOM_{IGBT}$, the higher switching frequency the IGBT can operate with the same junction temperature rises.

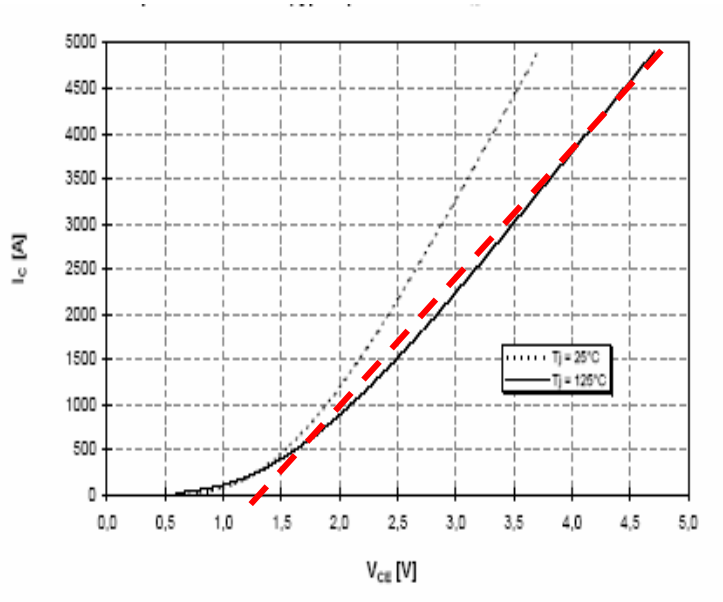


Fig. 2-3 IGBT output characteristics

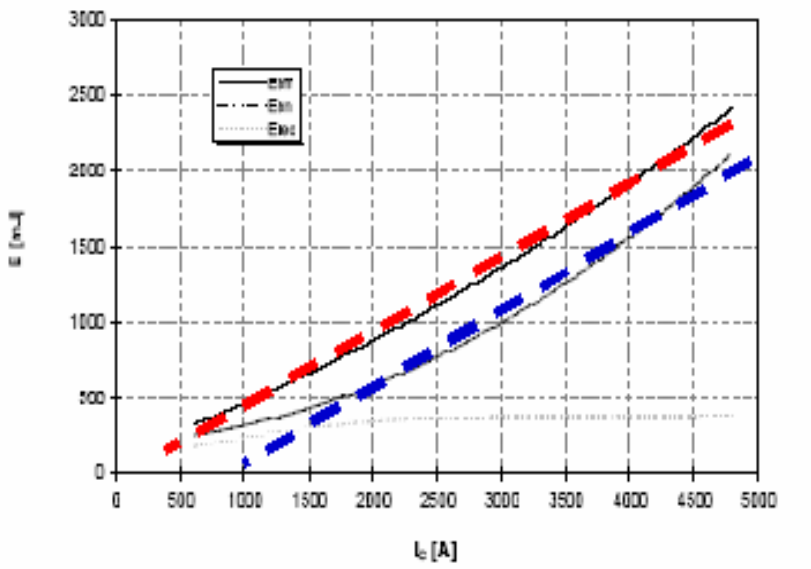


Fig. 2-4 IGBT switching losses as a function of collector current

The state-of-the-art IGBTs from a number of vendors are listed in Table 2-3. The calculated $PDFOM_{IGBT}$ from the datasheet information shows that IGBT (APT65GP60L2DF2) from APT company can provide higher power density compared to other products.

Table 2-3 State-of-the-art IGBTs comparison matrix

	IGBT								
Matrix	APT65GP60L2DF2 (APT)	APT60GT60BR (APT)	GP500LSS06S (DYNEX)	BSM300GB60DLC (EUPEC)	SKM300GB063D (SEMIKRON)	APTGU200A60 (APT)	CM300DY-12NF(PWRX)	FMG2G400US60 (FAIRCHILD)	MG300J2YS50 (TOSHIBA)
$V_{blocking}$ (V)	600	600	600	600	600	600	600	600	600
V_{DClink} (V)	300	300	300	300	300	300	300	300	300
I_{DC}@V_{dclink} (A)	100	100	500	300	300	200	300	400	300
Vces(V) /Kv (125°C)	2.1(65A) /0.03231	2.4(60A) /0.04	2.3(500A) /0.0046	2.2(300A) /0.00733	2.4(300A) /0.008	2.1(200A) /0.0105	1.7(300A) /0.00567	2.5(400A) /0.00625	2.5(300A) /0.00833
Eon(mJ) /Kon (300V,125°C)	0.605(65A,5Ω) /0.00931	1.6(60A,10Ω) /0.02667	50(500A,5Ω) /0.1	6.5(300A,3.3Ω) /0.02167	14(300A,6Ω) /0.04667	2.31(200A,0.83Ω) /0.01155	4.7(300A,2.1Ω) /0.01567	11(400A,2Ω) /0.0275	18(300A,1.8Ω) /0.06
Eoff(mJ) /Koff (300V,125°C)	1.47(65A,5Ω) /0.02262	2.4(60A,10Ω) /0.04	65(500A,5Ω) /0.13	11(300A,3.3Ω) /0.03667	13(300A,6Ω) /0.04333	3.69(200A,0.83Ω) /0.01845	10.5(300A,2.1Ω) /0.035	26(400A,2Ω) /0.065	13.5(300A,1.8Ω) /0.045
Rthjc(K/W) (single)	0.15	0.25	0.05	0.1	0.09	0.12	0.16	0.11	0.096
Package (mm^3) (single)	TO-264 MAX (26*20*5)	TO-247 (21*16*5)	107*62*36	107/2*62*30	107/2*62*30	108/2*62*22	94/2*48*30	108/2*62*30	108/2*62*30
Kv(Kon+Koff) *(Rthjc*Area)	0.080496	0.224028	0.350939	0.141968	0.21492	0.126567	0.103607	0.212866	0.281232
PDFOM	**12.42**	**4.46**	**2.85**	**7.04**	**4.65**	**7.9**	**9.65**	**4.7**	**3.56**
Notes	PT,100kHz@ 400V/54A	NPT,Thunder-bolt IGBT	_	half bridge	NPT,SEMITRANS,half bridge	PT,half bridge	IGBTMOD, half bridge	half bridge	half bridge

2.3.3 Power Diode Comparisons

The basic requirements for the secondary rectifier diode are low reverse recovery charge for low switching loss, low forward voltage drop for low conduction loss. Normally the high voltage rating diode has high reverse recovery charge which brings about high switching loss and safe operation issue [2-23]-[2-27]. The series connected diodes are used to achieve high output voltage. The series connection diodes need voltage balance circuit which enlarges the converter volume. There is a trade off among these considerations. Also if the diode has low thermal resistance, it will permit them to operate at high switching frequency under certain junction temperature rise, and small package dimension for high power density.

The diode forward voltage drop and reverse recovery loss are function of conduction current. Use linear approximation technique they are written as,

$$\begin{aligned} V_{ce} &= V_{ce0} + k_v i_c = K_v i_c , \quad K_v = V_{ce0} / i_{co} + k_v \\ E_{rr} &= E_{rr0} + k_{rr} i_c = K_{rr} i_c , \quad K_{rr} = E_{rr0} / i_{co} + k_{rr} \end{aligned} \tag{2-31}$$

The minimum total power loss can be derived with global minimization.

$$P_{loss} = V_{ce} i_{avg} + f E_{rr} \tag{2-32}$$

$$P_{loss,\min} = 2\sqrt{i_c^2 i_{avg} f}\sqrt{K_v K_{rr}} \tag{2-33}$$

So the maximum junction for the diode is derived as follows.

$$\begin{aligned} \Delta T_{\max} &= P_{loss,\min} R_{th} \\ &= \left(K_v \cdot i_c \cdot i_{avg} + K_{rr} \cdot i_c \cdot f\right) \cdot R_{th} \\ &= \frac{2 i_c \cdot f}{K_v} \cdot \left(K_v K_{rr} R_{th}\right) \\ &= \frac{2 i_c \cdot f}{k_1} \cdot \left(K_v K_{rr} R_{th} A_{pack}\right) \end{aligned} \tag{2-34}$$

where, k_1 is coefficient to normalize the conduction loss to package area, $K_v = k_1 / A_{pack}$.

In the above equation, the first term relates to the circuit operation conditions while the second one relates to the device information. Here, define a high power density figure of merit for power diode as follows.

$$PDFOM_{diode} = \frac{1}{K_v K_{rr} R_{thjc} A_{package}} \tag{2-35}$$

Using this figure of merit, one can evaluate the state-of-the-art power diodes for high power density application.

Table 2-4 State-of-the-art power diodes comparison matrix

	Diode				
Matrix	APT60D120B (APT)	APT30D120B (APT)	IDP30E120 (INFINEON)	RHRG75120 (FAIRCHILD)	RHRP30120 (FAIRCHILD)
$V_{blocking}$ (V)	1200	1200	1200	1200	1200
V_{DClink} (V)	800	800	800	800	800
I_{DC} (A)(25C)	60	30	30	75	30
VF@11A (V) (125C)	0.9	1.2	1.2	1.2	1.4
Recovery Charge (nC)	1820 (60A,480A/μs, 650V)	1640 (30A,240A/μs, 650V)	4700 (30A,850A/μs, 800V)	–	–
Reverse recovery time(ns)	130 (60A,480A/μs, 650V)	160 (30A,240A/μs, 650V)	355 (30A,850A/μs, 800V)	100 (75A,100A/μs)	85 (30A,100A/μs)
R_{thjc} (K/W)	0.42	0.9	0.9	0.8	1.2
Package (mm^3)	TO-247 (22*16*5)	TO-247 (22*16*5)	TO-220 (16*10*5)	TO-247 (22*16*5)	TO-220 (16*10*5)
PDFOM	11.15	1.54	1.44	-	-
Notes	ULTRAFAST SOFT RECOVERY	ULTRAFAST SOFT RECOVERY	–	–	–

2.3.4 Wide Bandgap Power Devices Comparisons

Power semiconductor devices made from materials with bandgap energies larger than Si have been investigated for many decades [2-28]-[2-29]. The potential advantages of these wide bandgap devices include higher achievable junction temperatures and thinner drift regions because of the associated higher critical electric field values. This can result in much lower on-resistance and smaller chip compared to Si. To evaluate the impact of wide bandgap power devices on the power density converter, several unipolar power device figures of merit are derived for comparison.

In the switching power converter, the minimum power loss of the unipolar power device can be calculated by:

$$P_{loss,\min} = 2I_{rms}\sqrt{V_D I_D f/(i_{g,av})R_{on,sp}Q_{gd,sp}} \tag{2-36}$$

where, f is the switching frequency, V_D and I_D are switch voltage and current, where $R_{on,sp}$ and $Q_{gd,sp}$ are the specific on-resistance and specific gate-drain charge respectively.

$$R_{on,sp} Q_{gd,sp} = 4kV_B \sqrt{V_B V_D} / \mu E_c^2 \tag{2-37}$$

From the above two equations, we can get,

$$P_{loss,\min} = \{4 I_{rms} (V_B V_D)^{3/4} \sqrt{k I_D f / i_{g,av}}\} / (E_c \sqrt{\mu}) \tag{2-38}$$

The term $(E_c \sqrt{\mu})$ is then defined as the new material figure-of-merit called HMFOM

$$HMFOM = E_c \sqrt{\mu} \tag{2-39}$$

Further derive the equation, one has

$$A_{opt} = \frac{I_{rms}}{\sqrt{V_D I_D f / (i_{g,av})}} \sqrt{\frac{R_{on,sp}}{Q_{gd,sp}}} = \frac{2 I_{rms} V_B^{5/4}}{V_D^{3/4} \sqrt{k I_D f / (i_{g,av})}} \frac{1}{\varepsilon \sqrt{\mu} E_c^2} \tag{2-40}$$

Here, define a new device chip area figure of merit (HCAFOM)

$$HCAFOM = \varepsilon \sqrt{\mu} E_c^2 \tag{2-41}$$

To compare devices thermal handling capability, one can calculate the device's junction to die attachment temperature rise by further utilizing the above equations,

$$\Delta T_{\max} = \frac{2kV_D^{3/2} I_D f W_{die}}{i_{g,av} \sqrt{V_B}} \frac{\varepsilon E_C}{\sigma_{th}} \tag{2-42}$$

Here define a new thermal figure of merit for switching power devices (HTFOM)

$$HTFOM = \frac{\sigma_{th}}{\varepsilon E_C} \tag{2-43}$$

The calculated unipolar power switching figures of merit are shown in Table 2-5. According to HMFOMs from the material point of view, it can be concluded that the best semiconductors for high frequency power switching applications should exhibit a large critical electric field for breakdown and should have higher carrier mobility. 4H-SiC material, for example, has a HMFOM about 7.4 times higher than silicon. Table 2-5 also compares the HCAFOM of various materials. The larger the HCAFOM, the smaller the chip area. It is clear that 4H-SiC will have 7 times lower loss than silicon, and 65 time smaller chip area if designed for similar operation conditions. From HTFOM point of view, according to Table 2-5, The higher the HTFOM, the lower the temperature rise under the condition that device chip area is given by A_{opt} and losses are given by $P_{loss,min}$. It is clear that 4H-SiC devices will have 7.4 times lower losses than silicon, and 65 smaller chip area, and about 60% high temperature rise if both are designed to operate under similar conditions.

Table 2-5 Comparison of Various Semiconductor Materials - based on the HMFOM, HCAFOM and HTFOM (normalized against silicon)

Semiconductor Materials	Electron mobility μ (cm^2/V-s)	Relative dielectric constant ε	Critical field E_c (kV/cm)	Thermal conductivity σ_{th} (W/m-K)	HMFOM = $E_C\sqrt{\mu}$	HCAFOM= $\varepsilon E_C^2\sqrt{\mu}$	HTFOM = $\frac{\sigma_{th}}{\varepsilon E_C}$
GaAs	8,500	13.1	400	55	**3.29**	**4.90**	**0.28**
GaN	900	9	3,000	110	**8.02**	**61.68**	**0.11**
Ge	3,900	16	100	58	**0.56**	**0.25**	**0.98**
Si	1,400	11.7	300	130	**1**	**1**	**1**
GaP	250	11.1	1,000	110	**1.41**	**4.45**	**0.27**
SiC(6H,α)	330	9.66	2,400	700	**3.88**	**25.65**	**0.82**
SiC(4H,α)	700	9.7	3,180	700	**7.50**	**65.87**	**0.61**
Diamond	2200	5.7	5,700	2000	**23.82**	**220.47**	**1.66**

As a study example for wide bandgap materials, a SiC power MOSFET is designed to see the impact on high power density conversion. Silicon Carbide (SiC) has been attracting much attention because of its potential to make high performance power devices with the capability of operating at high temperature. Its avalanche breakdown field is ten times higher than silicon, and its thermal conductivity is higher than copper at

room temperature. The unipolar power devices such as MOSFET can be developed based on SiC to take advantage of the faster switching speed inherent in unipolar devices. Its bandgap is approximately three times larger than silicon. The wide bandgap allows devices to operate at higher junction temperatures. This capability can be expected to reduce cooling requirements, improve reliability, and increase power density.

To investigate the impact of SiC power device on high power density conversion, a SiC DMOS with specific resistance 0.0064 $\Omega*cm^2$ is designed with Finite Element Method. Fig. 2-5 gives specific resistance $R_{on,sp}$ as a function of breakdown voltage BV_{ds}. The SiC device specific resistance is much smaller than Si device which means the SiC power device can operate at high switching frequency with same conduction resistance as Si device. Table 2-6 lists comparisons of conduction loss, switching loss, device package area, junction temperature rise etc for Si MOSFET and SiC DMOS power device with high frequency application. Assuming the SiC DMOS has the same conduction resistance value as Si MOSFET, the conduction loss will be the same for both. When parallel ten times SiC DMOSs device, the conduction loss decreases ten times. Because the SiC DMOS has smaller chip area, its switching loss is much smaller than Si MOSFET with the same switching frequency. The switching frequency can be increased much higher to decrease the passive component size. When the SiC DMOS operates ten times higher switching frequency, its switching loss is about three times higher than Si MOSFET. The total loss is about the same for both. If the SiC DMOS has the same specific thermal resistance as Si MOSFET, its thermal resistance is much greater due to the smaller chip area. The junction temperature rise for SiC DMOS is much higher than Si MOSFET, which is estimated at 113^0C. If the ambient temperature for the converter is about 90^0C, the SiC DMOS junction will operate at about two hundred degree, which is within the safe value. From the comparisons for Si MOSFET and SiC DMOS, it is estimated that SiC MOSFET has the potential to operate at ten time higher switching frequency and can reduce the footprint by at least four times.

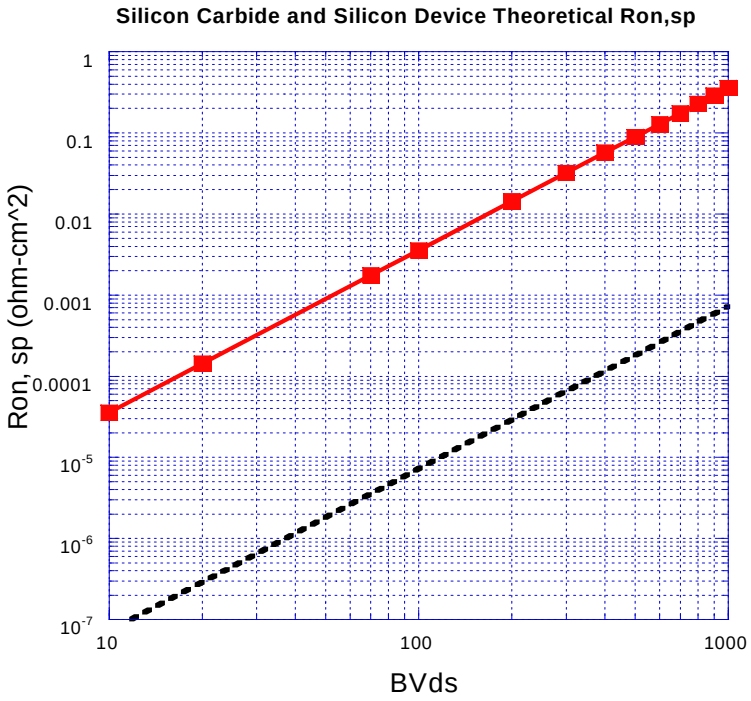


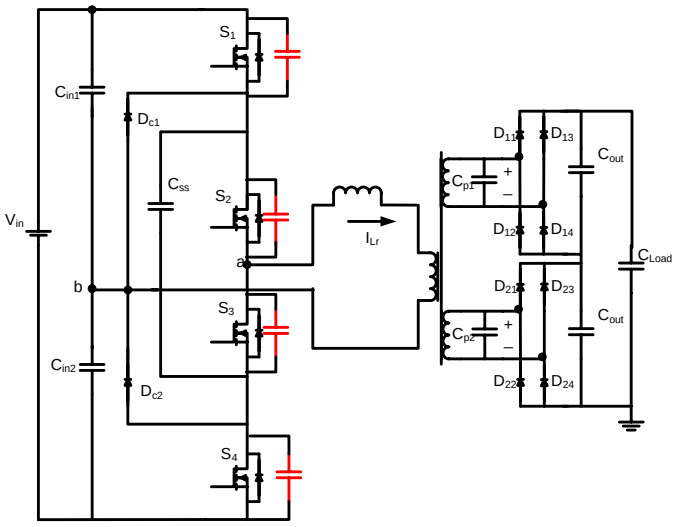
Fig. 2-5 Specific resistance $R_{on,sp}$ as a function of breakdown voltage BV_{ds} (solid line: Si, dotted line: SiC)

Table 2-6 Comparisons of Si MOSFET and SiC DMOS power devices with high frequency application

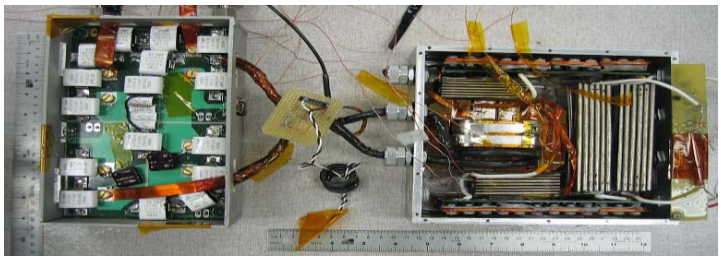
Device	MOSFET APT50M38JLL	SiC DMOS	SiC DMOS
Device number	12x4=48	120x4=480	120x4=480
Switching frequency (kHz)	200	200	1000/2000
R_{ds} /each (Ω)	0.038	0.038	0.038
$R_{ds\text{-}sp}$ (Ω*cm^2)	0.25	0.0064	0.0064
Q_{gd} (nC)	138	80	80
Conduction loss(kW)	4.8	0.48	0.48/0.48
Switching loss(kW)	2.0	0.61	3.05/6.1
Device loss (kW)	6.8	1.09	4.53/6.58
Chip area (cm^2)	6.579	0.168	0.168
Case area (cm^2)	9.58	0.245	0.245
R_{th} (K/kW)	180	8210	8210
$R_{th\text{-}sp}$ (K/kW*cm^2)	1180	1180	1180
Total device area(cm^2)	460	120	120
Temperature rise (K)	26	18	78/113

2.4 Application of Power Density Figure of Merit

A parallel resonant high power density converter (600V/30kW) is designed using power MOSFET #1 operation in parallel shown in Fig. 2-6. The resonant tank peak current is about 180A. The power devices turn on at 76A/300V, turn off at 112A/300V and switch at 225 kHz. The estimated and measured junction temperature is about 125^0C with ambient temperature 90^0C. To realize the same power conversion, power MOSFET #2 and #5 can also be selected as the main switch. Due to the device current rating difference, the number of device in parallel may vary for different kinds of devices. The estimated junction temperature and power density for primary side and whole converter are shown in Table 2-7. It can be concluded that the high power density figure of merit power device has the potential improvement for the high power density converter design.



(a) System schematic



(b) Hardware implementation

Fig. 2-6 A high power density parallel resonant converter

Table 2-7 Comparisons of power converter performances with different switching power devices

	Power MOSFET #1 APT60M75L2LL	Power MOSFET #2 APT60M60JFLL	Power MOSFET #5 SPW47N60C2
Number of devices in parallel / current (A)	3 / 219	3 / 210	5 / 235
Junction temperature (^{0}C)	125	123	121
Primary side (W/inch^3)	241	133	224
Whole converter (W/inch^3)	106	78	102

2.5 Summary

In this chapter, the new figures of merit have been proposed for power semiconductor devices operating in high frequency high power density converter. These figures of merit are derived based on the device power loss, thermal characteristics and package considerations. The high temperature figure of merit can be used to compare junction temperature rise for different semiconductor material devices. The power density figure of merit can be used by device manufacturers to compare devices performance once power loss, thermal and package are known. And it also provides the optimum selection for power devices to design the high power density converters.

To evaluate the impact of wide bandgap power devices on the power density, several unipolar power devices figures of merit are derived for comparison. A new material figure of merit (HMFOM), a new chip area figure of merit (HCAFOM) and a new thermal figure of merit (HTFOM) for switching power devices are derived based conduction and switching loss considerations. The HMFOM can be used to compare the relative loss advantage of devices based on different materials, and the HCAFOM can be used to compare optimal chip area, and HTFOM can be used to compare junction temperature rise. The predicted loss advantage of wide bandgap materials, such as 4H-SiC, is much less than previously predicted due to the larger gate charge in wide bandgap unipolar power devices. However, the optimal chip area of the 4H-SiC is still much

smaller than the silicon. Other useful equations shown in this chapter can be used for further analysis of device capabilities under different operation conditions (current, voltage, switching frequency).

An application example of the power density figure of merit is conducted to see how the PDFOM power devices benefit the converter system power density improvement. The power converter is a three level parallel resonant converter. Three kinds of power MOSFET in parallel are calculated as the main switch. Due to the power loss, thermal performance and package area differences for these power MOSFETs, the different switching frequencies, converter volumes and thus power density can be achieved for similar junction temperature rise. The high PDFOM power devices have the potential to improve the converter power density.

Chapter 3 Power Semiconductor Device High Temperature High Frequency Operation Characterizations

3.1 Introduction

In the high power density conversion application, the practical ways are to minimize the converter volume and increase the switching frequency, or the power devices high case temperature operation to shrink heatsinks size. The power devices high case temperature and high frequency operation generate higher power losses that further improve the device junction temperature.

All power semiconductor devices have temperature limitations. State of the art commercial silicon devices such as power MOSFETs usually have a maximum junction temperature rating of 125^0C, with some devices rated for operation up to 150^0C. It may be advantageous and desirable in some applications to have power semiconductor devices operate at high temperature, for increased loss handling capability. Higher loss handling capability can lead to potential increase in switching frequency capability, which can in turn lead to more compact converters and better electrical performances [3-1]-[3-3]. In certain other applications, it is necessary to operate at high temperature due to the harsh environmental conditions.

One promising approach to achieve a high temperature operation is to use devices with intrinsic high temperature capability, such as future devices based on wide bandgap semiconductors – SiC, GaN or even diamond. The other approach is to exploit the high temperature potential of the available silicon devices. In either case, it is equally important to understand the true physical limitations for a semiconductor device – a silicon based device as well as a future wide bandgap device, and to fully utilize its capability for given applications. This chapter focuses on investigation of high temperature capability and limitations of silicon power devices. The study can be extended to other silicon or wide bandgap devices.

There have been considerable previous researches on temperature limitations for semiconductor devices. As discussed in [3-1], any semiconductor has a ceiling temperature at which thermal carrier generation begins to dominate and ultimately overwhelms the carrier concentrations due to ionized doping and injection, among other things, leading to excessive leakage current. Other limitations include the temperature effects on device long term reliability, thermal stress and life expectancy, and heat generation. Therefore, there are two basic concerns when operating semiconductor devices at high temperature, the stable operation that will not lead to unacceptable performance and damage, and the second is degradation of the device reliability and life. In practice, the rated junction temperature is determined mainly based on the limit of maximum leakage current. The temperature limit is also set with the knowledge that it is acceptable from the standpoint of the reliability and life time, though in the design, care must be taken to deal with reliability issues associated with power and thermal cycling, which is also related to packaging. For given device temperature rating, the device package is designed accordingly. As a result, the package can also become a limiting factor for device operating at high temperature.

The existing design practice for device temperature can be summarized as follows: The device junction temperature should be limited such that the loss and thermal management will not lead to thermal runaway and eventual failure; at the same time, the reliability of the device should not be compromised [3-4]-[3-5]. In addition, the leakage current should be negligible and the rated temperature selected appropriately is a convenient way to achieve this goal. The problem with a simple absolute temperature limit is that on one hand, it does not guarantee the system thermal stability, and on the other hand, it may be too conservative.

This research investigates the power MOSFETs high temperature operation from the standpoint of thermal stability. The study is conducted based on experimental evaluation of selected commercial devices. The objective is to clearly identify the electrical and thermal limitations to high temperature and high frequency application of silicon power MOSFETs, and to provide guidelines on how to use them safely and reliably for high temperature operation. This research develops a design and operation rule for device high temperature operation based on the thermal stability criterion and application

requirements. The temperature range of interests is above the normal 125^0C or 150^0C. Compared with the previous work in this area [3-3]-[3-7], this work includes the leakage current as part of the design consideration [3-8].

While the temperature should have significant impact on device and packaging reliability, it is not included in this study. Many failure modes are related to packaging and are not suitable to study with a given commercial device with normal temperature package. The issues can be separately addressed.

The whole chapter is organized as follows. Firstly the power MOSFETs DC blocking characteristics are studied experimentally and analytically to identify the electrical and thermal limitations at high junction temperature. Secondly, the loss characteristics including the switching loss, conduction loss, and leakage power loss are tested and analyzed at higher junction temperatures. Then the thermal stability criterion is developed to investigate the high frequency operation at increased case temperature. Some of the analyses are applied to SiC based power MOSFETs, whose high temperature operation performances are predicted and compared with Si power MOSFETs. The power MOSFET junction temperature prediction technique and the thermal model are developed. The power MOSFET pulse power and continuous power characteristics are analyzed. The power devices high temperature operation effects on the power density are investigated. For the pulse power the power devices can operate much higher switching frequency than that for continuous power. So the passive components volume and heat sink size can be minimized thus the power density are improved. Finally, conclusions are drawn to provide the design guideline for high temperature power converter application.

3.2 Power Device DC Blocking Characteristics

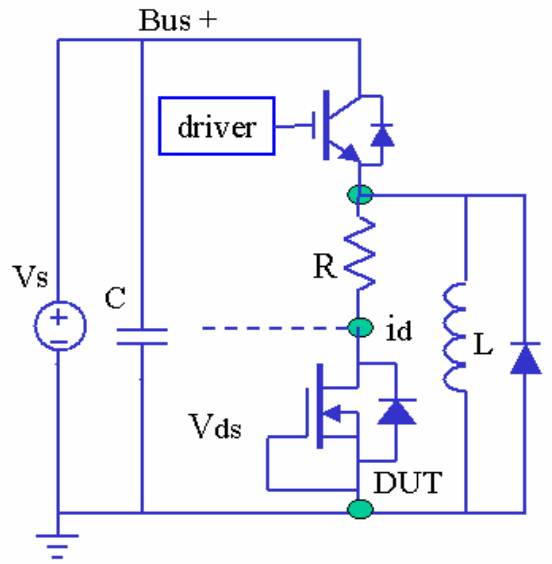
To investigate the thermal stability including the effect of leakage current for power devices, the DC blocking characteristics are studied firstly to identify how the breakdown and leakage current change with temperature. The basic device temperature rating is generally associated with the leakage current. At high temperature, the silicon material intrinsic carrier concentration increases rapidly. At a sufficiently high temperature, more electron and hole pairs are generated, leading to high leakage current.

Experiments are conducted to investigate the temperature effects on breakdown voltage and leakage current. The schematic for test setup is shown in Fig. 3-1. The device under test (DUT) is a commercial power MOSFET rated at 600V/73A. An electric heater is used to regulate the device junction temperature. Note that during the blocking state, the loss is relatively small and therefore, the junction temperature can be regarded the same as the case temperature regulated by the heater. When the loss caused by leakage current becomes significant, its impact on the junction temperature must be accounted for.

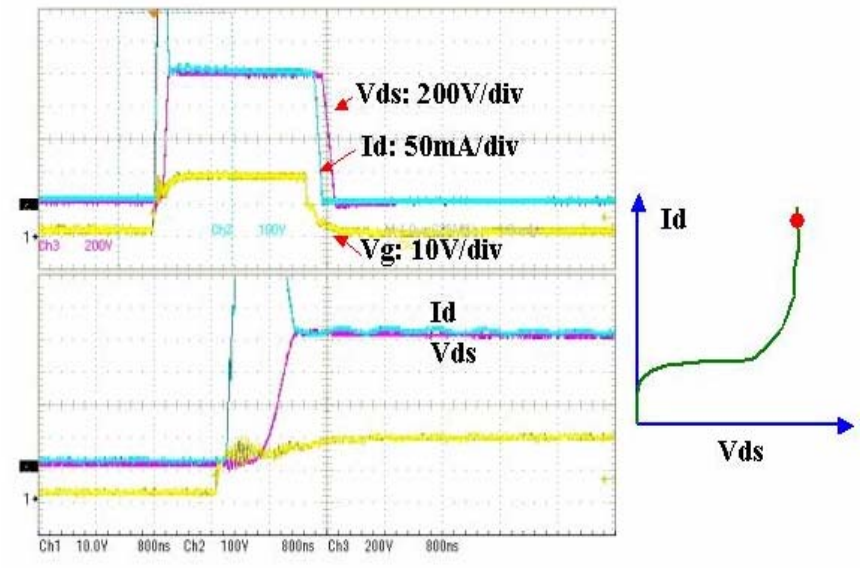
To avoid the junction temperature drift during the measurement, the high leakage is only allowed for a very short period of time. An IGBT is used as the control device for measurement. Since the IGBT is kept at the low temperature, when the IGBT is off, the leakage current through the MOSFET DUT is negligibly small. The inductor in parallel with the MOSFET also helps to keep the voltage on the MOSFET and leakage through it is low when the IGBT is off. When the IGBT is turned on, the source voltage Vs is directly applied to the MOSFET, the corresponding current through the MOSFET is measured by the small shunt resistance R in series with the MOSFET and is the leakage current at the given temperature. The IGBT turn-on period is chosen to be only a few microseconds to ensure that the leakage current loss will have negligible effect on the MOSFET junction temperature. Note that the IGBT turnoff transition is relatively slow. Thus the parallel inductor is necessary to help the voltage across the MOSFET to go near zero quickly when the IGBT is being turned off and therefore to reduce the leakage current quickly when the measurement period is over. Fig. 3-1 shows the waveforms of the MOSFET leakage current for one measurement at 210^0C.

During the test, the bus voltage applied to the off-state MOSFET is adjusted point by point to observe the breakdown voltage and leakage current change. The test is repeated for different temperature settings. At a high junction temperature point, such as 200^0C, the leakage current is significantly higher compared to that at the room temperature. For any given temperature, at some voltage points, the leakage current starts to increase dramatically when the bus voltage only increases slightly, indicating the device is approaching the avalanche breakdown condition. By this approach at different junction temperatures the corresponding avalanche breakdown voltages can be measured. The

final results in Fig. 3-2 show that the breakdown voltage increases from 740V at room temperature to 815V at 200^{0}C for the selected 600V MOSFET. The test results on breakdown voltages are consistent with the theoretical prediction using the impact ionization coefficient a_n [3-9]-[3-13]. The breakdown voltage is not a limiting factor for power MOSFET operation at high temperatures.

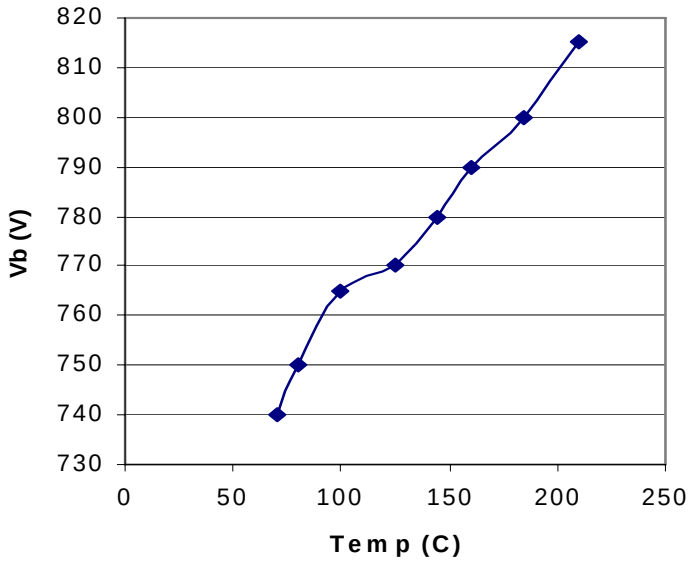


(a) Test setup schematic



(b) Power MOSFET leakage current @210^{0}C

Fig. 3-1 Power MOSFET avalanche breakdown voltage and leakage current test



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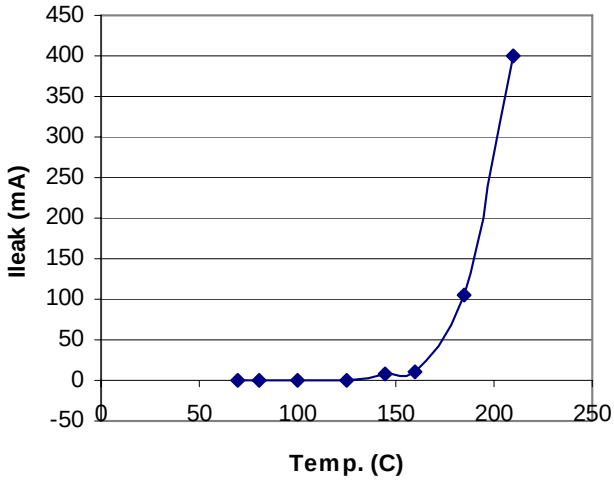


(b)

Fig. 3-2 Avalanche breakdown voltage (a) and leakage current (b) as a function of junction temperature

Fig. 3-2 shows the test results of leakage current as a function of temperature with the applied voltage fixed at 300V. The leakage current does not change much below 150^0C.

Above 150^0C, it increases almost exponentially due to the electron-hole pair generation at high junction temperatures.

The characteristics of the leakage current can be explained according to basic device physics. During the power MOSFET DC blocking state, considering the main p-n junction only, the total leakage current includes space charge leakage current with density J_{scg} and diffusion leakage current with density J_{DLL} [3-14]-[3-15]. The generation of the hole-electron pairs in the depletion region results in space charge leakage current, with J_{scg} determined by the intrinsic carrier concentration n_i, depletion layer thickness W_c and space charge generation lifetime t_{sc}. Their relationship can be expressed as in equation (3-1)

$$J_{scg}(V_{br}, T_{br}) = \frac{qW_c(V_{br})n_i(T_{br})}{t_{sc}} \tag{3-1}$$

where, V_{br} is the breakdown voltage, and T_{br} is the junction temperature.

The diffusion leakage current is generated when the minority carriers in the neutral regions diffuse to the depletion region and is swept to the opposite side by the electric field in the depletion region. The diffusion leakage current density J_{DLL} is the sum of the diffusion current density components from the p region and the n region as expressed in Equation (3-2).

$$J_{dLL}(T_{br}) = \sqrt{\frac{k_o T_{br}\mu_p(T_{br})}{t_p} q}\,\frac{n_i(T_{br})^2}{N_{d0}} + \sqrt{\frac{k_o T_{br}\mu_n(T_{br})}{t_n} q}\,\frac{n_i(T_{br})^2}{N_{a0}} \tag{3-2}$$

where, μ_p, μ_n are the hole and electron mobility respectively, t_p, t_n are hole and electron lifetime, and N_c, N_{ao} are donor and acceptor doping concentrations.

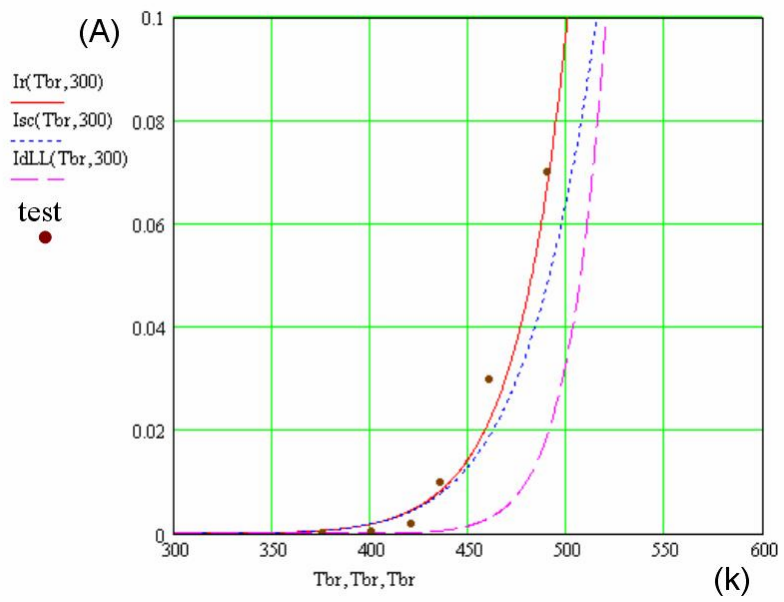


Fig. 3-3 Leakage current changes as a function of local temperature

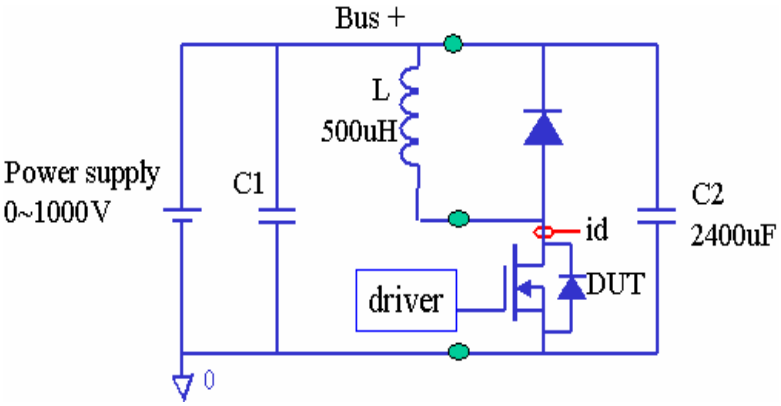
Based on equations (3-1) and (3-2), the total leakage current as a function of the junction temperature is calculated and shown in Fig. 3-3 based on the tested power MOSFET. At low temperature, the space charge leakage dominates, and as the junction temperature increases, the diffusion leakage current eventually exceeds the space charge leakage current and becomes dominant.

Clearly, the avalanche breakdown voltage is not a limit to the device high temperature operation. The increased leakage current at high temperature will cause additional power loss and possible thermal instability.

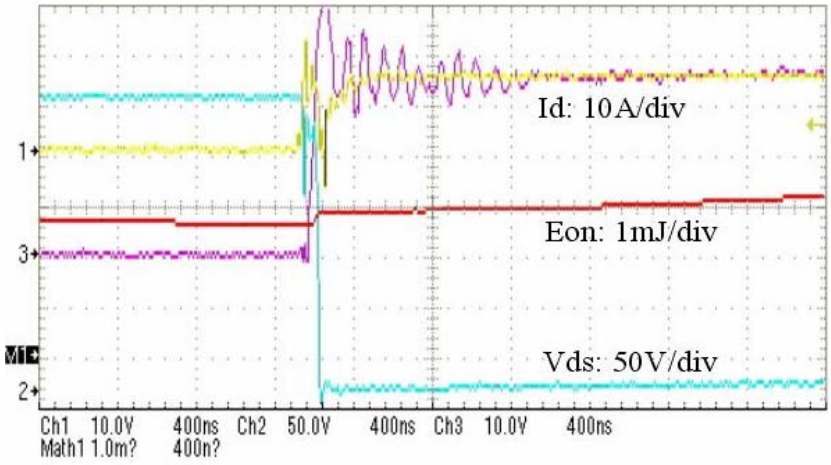
3.3 Loss Characteristics of Power MOSFETs

Loss characteristics of power MOSFETs at high temperatures directly affect the system thermal stability. In this chapter, the loss characteristics are studied through measurement of device switching loss and conduction loss at different temperature points and current levels under a given voltage. The switching losses are measured using a test setup with its schematic shown in Fig. 3-4. The device under test is again the same commercial MOSFET used in DC blocking characteristics study with a rating of 600V/73A. With an electric heater controlling the device junction temperature, the turn-on and turn-off losses

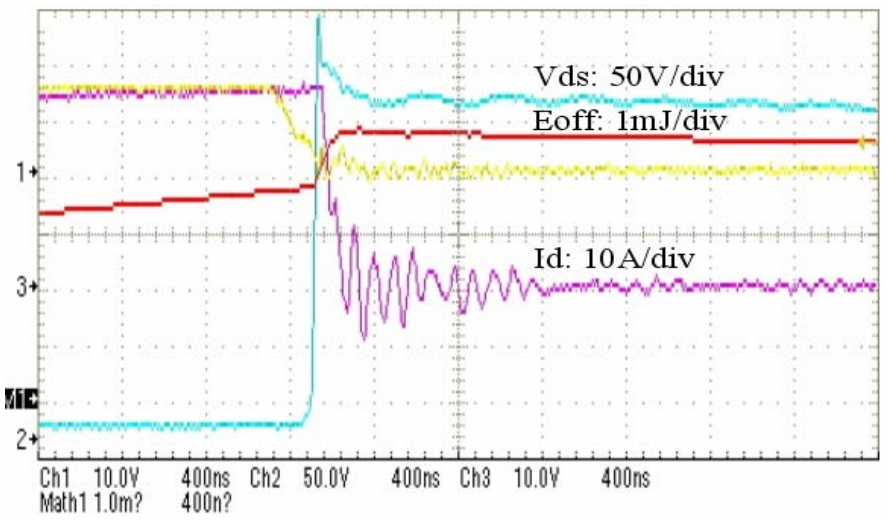
at different temperatures are measured using a double pulse testing. Fig. 3-5 shows the variation of switching losses with temperature. The power MOSFET switching losses increase slowly with temperature, unlike bipolar power devices such as IGBT whose switching loss changes dramatically with junction temperature rise where the bipolar conduction modulation dominates. Note that the switching loss is a strong function of gate control or gate resistance R_g. Fig. 3-5 corresponds to $R_g = 10\Omega$, which is within the normal range of the recommended values. Different gate resistances will change the switching losses but the analysis approach will stay the same.



(a) Test setup schematic



(b) Turn-on waveforms @150^{0}C



(c) Turn-off waveforms @150^{0}C

Fig. 3-4 Switching loss of power MOSFETs at high junction temperature

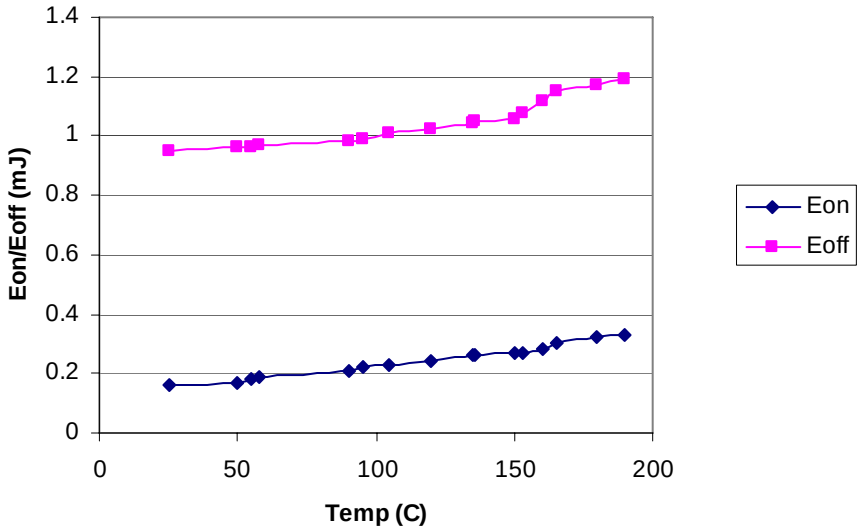


Fig. 3-5 Power MOSFET switch losses as a function of temperature

(R_g=10 Ω, switch @300V/35A)

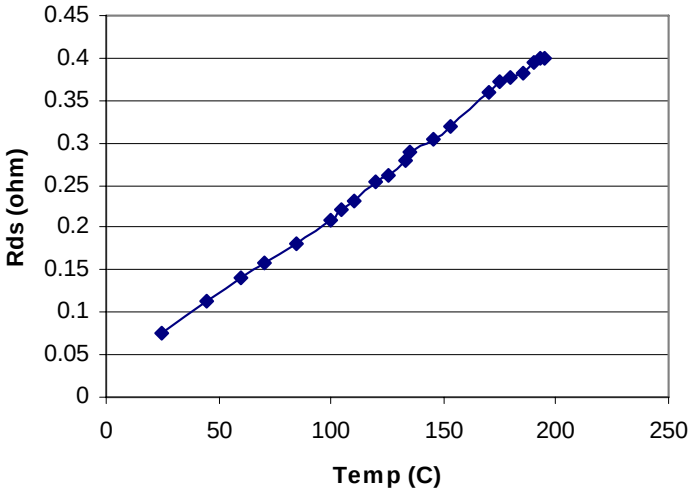


Fig. 3-6 Power MOSFET R_{ds} resistance VS junction temperature

The conduction loss of the power MOSFET depends on the conduction current and forward voltage drop. The forward voltage drop is a function of temperature. The MOSFET channel voltage has a strong positive temperature coefficient because of mobility reduction with increased temperature. The voltage drop across the wide base region is affected by lifetime increase and carrier mobility reduction. By measuring the power MOSFET conduction resistance R_{ds}, the conduction loss can be derived. Fig. 3-6 shows the tested R_{ds} change with the device junction temperature. When the junction temperature increases up to 200^0C, the R_{ds} value is nearly four times higher than that at the room temperature. This is mainly caused by the channel electron carrier mobility reduction. Compared to the switching loss, the conduction loss increases much faster for a given switching frequency.

3.4 Thermal Stability Analysis

The losses generated from power MOSFET operation, including switching, conduction, and leakage losses, must be transferred away from the switching junction. Thermal impedance represents the ability for heat transfer, and depends on the semiconductor material and packaging. Because of the temperature dependence of losses, a closed-loop thermal system exists as illustrated in Fig. 3-7. The total loss can be written as,

$$P_{total}(T_j, f_s, I_D) = [E_{on}(T_j) + E_{off}(T_j)]f_s + DV_{ds}(T_j)I_d + (1-D)V_{dc}I_{leak} \tag{3-3}$$

where, $E_{on}(T_j)$, $E_{off}(T_j)$ account for the temperature dependence of the turn-on and turn-off losses respectively, the second term stands for the conduction loss, and the last term for the leakage current loss during the off state; D is the switching duty cycle; and I_D is the drain current. Then, the junction temperature can be written as,

$$T_j = T_a + R_{th}P_{total} \tag{3-4}$$

where, R_{th} is the thermal resistance from junction to ambient environment. The operating junction temperature (T_j) must be kept under a maximum temperature rating ($T_{j\max}$) which are determined by materials and may not be the same as maximum junction temperature provided by the manufacturers' data sheet. However, in order to stabilize the thermal circuit, the gain of the loop shown in Fig. 3-7 must be kept below unity. Thus, the constraint conditions can be given as,

$$\frac{dP_{total}(T_j)}{dT_j}R_{th} \le 1$$

$$T_j \le T_{j\max} \tag{3-5}$$

The temperature effects on all the losses – switching, conduction, and leakage need to be considered. These effects are also dependant on the operating current, voltage, and circuit topology. A comprehensive experimental study is conducted for various cases. Fig. 3-8 shows the power MOSFET losses change at two different junction temperatures. When the junction temperature increases to 200^0C, the switching loss and conduction loss almost doubled compared to 90^0C. The leakage current loss is negligible compared to the switching loss and conduction loss at low junction temperature. But at high junction temperature, the leakage current increases so quickly that the leakage current loss is

comparable to the switching and conduction loss. This is the main reason for the device thermal instability at high temperature.

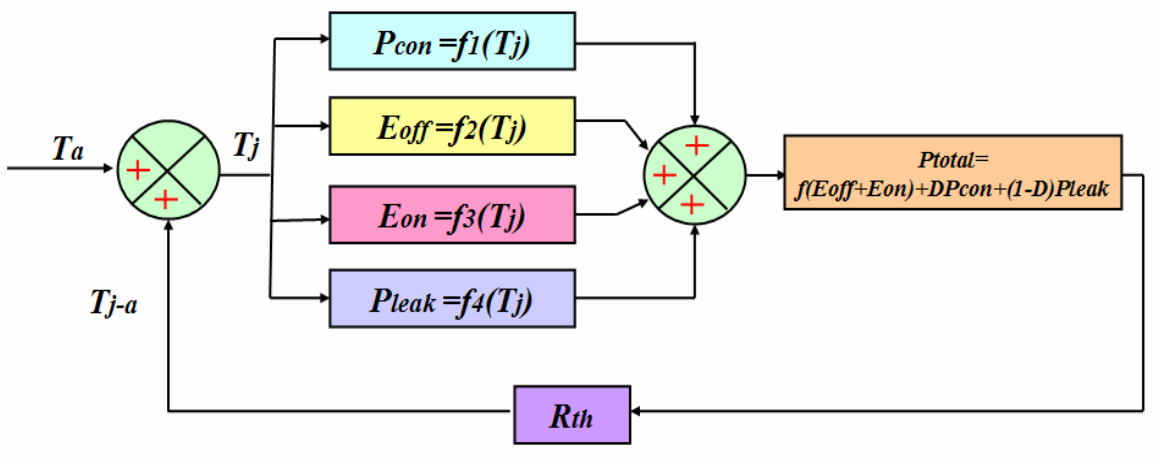


Fig. 3-7 Power MOSFET thermal stability system

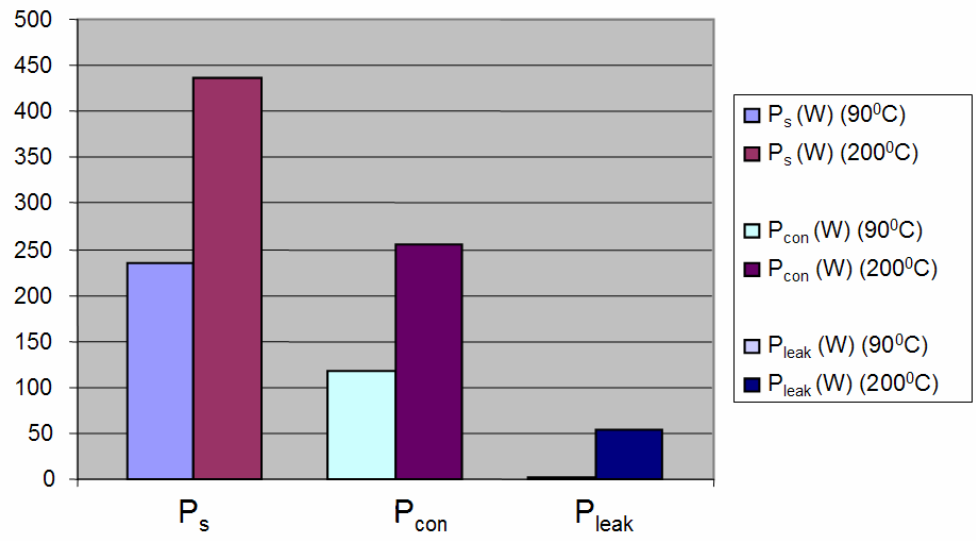


Fig. 3-8 Power MOSFET thermal characteristics comparisons (Switching @300V/35A/100kHz (90^{0}C and 200^{0}C))

To further analyze the thermal effects on the power MOSFET operation stability, we can obtain the total power loss curves using equation (3-3) and power dissipation lines

using (3-4). Losses versus temperature curves at five frequencies are shown in Fig. 3-9 together with the thermal load line (or power dissipation curve). At a frequency of 100 kHz, the loss curve crosses the thermal load line at two points, one stable point and another unstable point. At the unstable point, change rate of losses is higher than the thermal conductance, indicating an unstable thermal state. When the frequency increases to 150kHz, the loss curve becomes tangential to the thermal load line, with the intersection point corresponding to the highest possible stable operating temperature under the given operating voltage and current condition. Any further loss increase (as result of frequency increase in this case) will result in no common point between the loss curve and the power dissipation line. Therefore because of the higher increase rate at higher temperatures, there is a maximum junction temperature and maximum frequency for a device at each current level before thermal runaway.

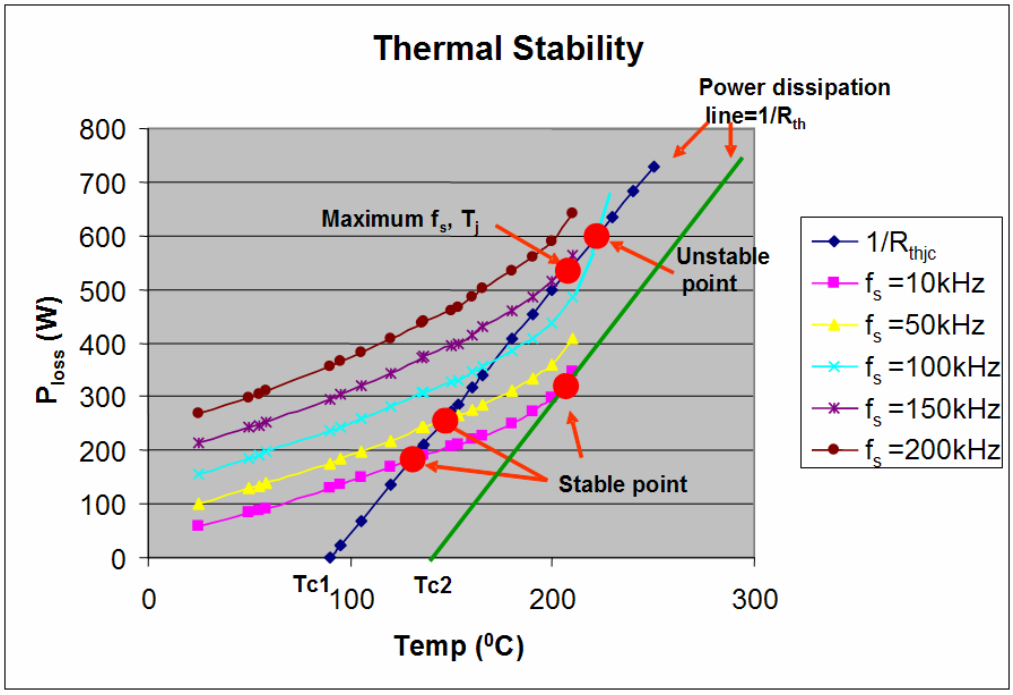


Fig. 3-9 Power MOSFET thermal stability graph

On the other hand, when the device operates at high ambient temperature, the power dissipation line will move horizontally to the right side with the device case temperature increases. If the device switching frequency is kept the same, the power MOSFET case

temperature can be improved to make sure the power dissipation line has only one tangential point. Under this condition, the power MOSFET operates at high temperature environment and the junction temperature is in the steady and unstable state boundary. If one designs the power converter operate at high ambient temperature, one can derive the maximum switching frequency for the converter to make sure the device operate at the stable point.

3.5 Predicted Wide Bandgap SiC Power MOSFETs Thermal Stability

Power semiconductor devices based on SiC have higher blocking voltage and higher current densities than silicon based devices [3-16]-[3-20]. The wide bandgap energy and low intrinsic carrier concentration of SiC also permit this type of semiconductor to have a better behavior under higher temperatures. This work presents comparison of Si power MOSFET and a hypothetical SiC power MOSFET based on thermal stability criterion described above.

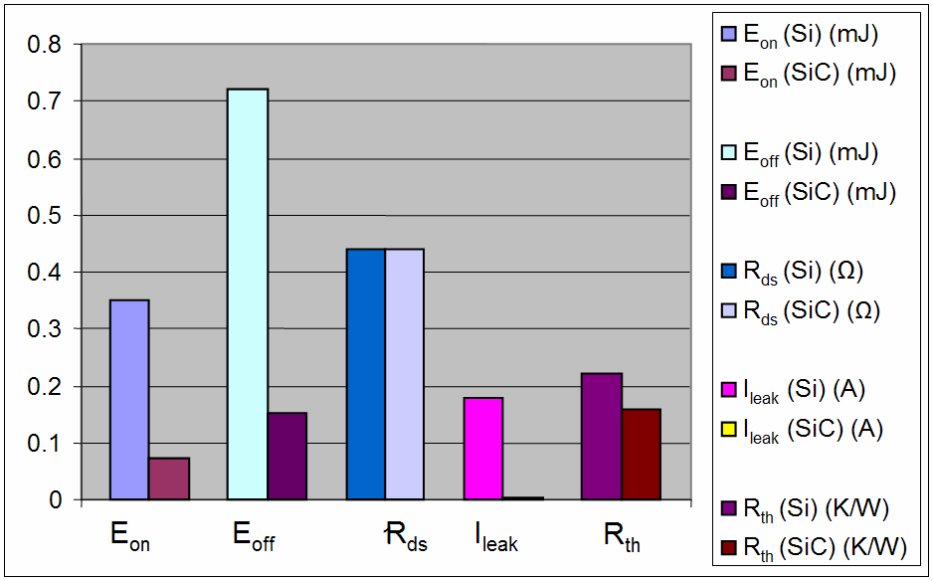


Fig. 3-10 Comparisons of Si and SiC power MOSFET thermal characteristics @300V/35A/200^{0}C

The power losses breakdown and thermal resistance for Si and SiC power MOSFETs are compared in Fig. 3-10. Here the designed SiC power MOSFET has the same

conduction resistance R_{ds} as Si power MOSFET APT6013LFLL. Then the turn-on and turn-off loss can be derived according to the device scaling. Due to the small SiC chip area, the switching time dependant power losses are correspondingly decreased. The significant improvement for the SiC device is the leakage current reduction, almost negligible at high junction temperature. This will improve thermal stability at high junction temperature operation. Another factor for this is the low thermal resistance for SiC material that further improves the thermal stability.

The predicted thermal stability graph of wide bandgap SiC power MOSFET is shown in Fig. 3-11. Power losses versus temperature curves at seven frequencies are shown together with the thermal load line. Compared with the Si power MOSFET, the power losses lines change nearly linearly, because the leakage current loss is almost zero. The power losses lines have only one intersection stability point even at higher frequency and junction temperature. The thermal stable point can be pushed much higher to operate the device at high junction temperature and high switching frequency. When the ambient temperature rises, which means the power dissipation line moves horizontally to the right side, the device can still operate in the stable state.

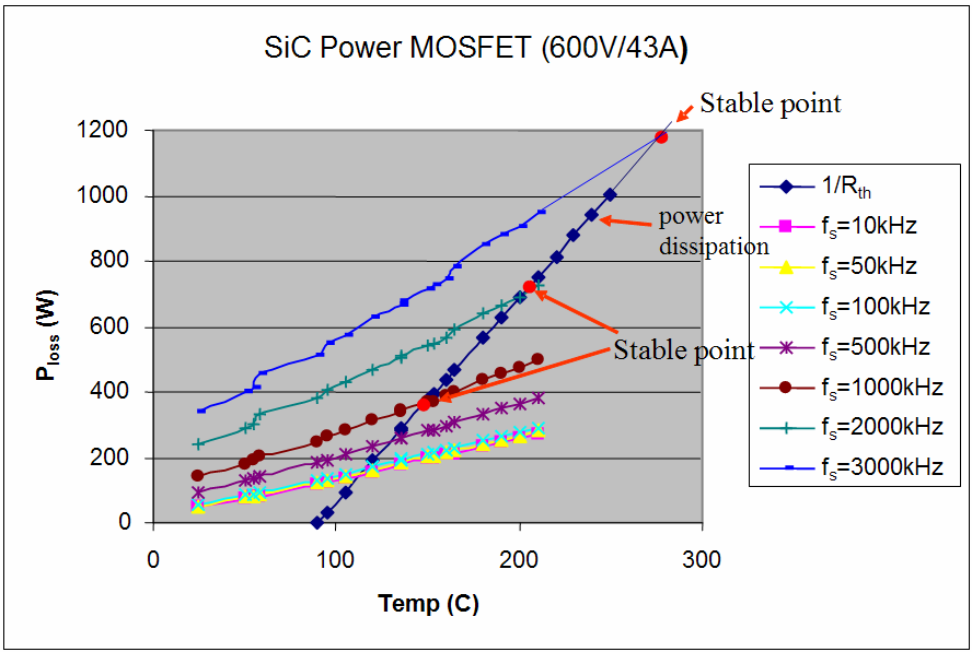


Fig. 3-11 Predicted SiC power MOSFET thermal stability @300V/35A

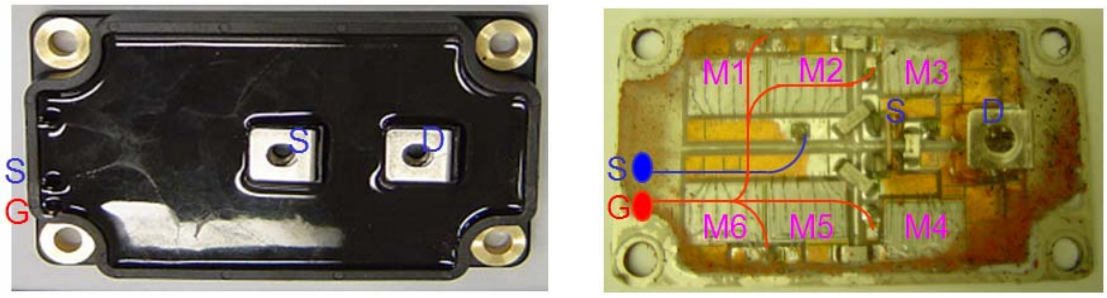
The above discussed thermal stability graph is very useful for the power devices in the steady state operation. For the power converters in the continuous mode operation where the power dissipation is approximately constant, the steady state thermal resistance is only considered and sufficient to predict the maximum junction temperature. However, in the high frequency switching power converters, the thermal flow path may behave some capacitance. For pulse power application, the junction temperature transient needs to be further studied.

3.6 Junction Temperature Prediction Technique

To study the power device thermal stability, the power device switching loss, conduction loss, leakage current power loss and thermal resistance are needed. Precise calculation of these information is difficult. Normally the experimental studies are conducted. However theoretical analysis can provide some predictions for the power device failure and reliability operation. To verify the calculated junction temperature of power device, the experimental junction temperature prediction technique is developed and conducted in the test. The thermal model for the junction temperature rise is proposed.

The power device under test is the single switch custom power MOSFET module (APTM60UM13F-AlN) shown in Fig. 3-12. It has the following features,

- Six APT60M75L2FLL dice in parallel, large current rating
- Fast Recovery Epitaxial Diode (FRED)
- Low R_{dson}, input and Miller capacitance
- AlN substrate for improved R_{thjc}
- Isolated package
- High switching performance
- Same intrinsic package structure as commercial module
- Better power bus layout
- Large gate parasitic components



(a) (b)

Fig. 3-12 Custom power MOSFET module

The basic principle for the junction temperature prediction is to measure the voltage drop across the power MOSFET during the conduction state. Then the conduction resistance can be calculated. According to the relationship between the resistance and temperature, the junction temperature can be predicted. For single power MOSFET, it is easy to do this because the single power MOSFET die has small parasitic package inductance. This parasitic inductance has great effect on the voltage drop across the drain-to-source terminals, because the current flowing through the power MOSFET is a high frequency resonant current waveform, not a DC current. Considering the power MOSFET module's structure, the equivalent circuit can be drawn as a conduction resistance in series with a parasitic inductance. To measure the voltage drop across the module, the external circuit is added which is composed of resistor, capacitor and high voltage schottky diode. An external power supply is applied across the RC network to force the diode conducting for voltage drop measurement across the module. The measured voltage drop is the sum of the diode forward voltage drop, inductor voltage and resistor voltage. For the sinusoid current waveform flowing the power MOSFET module, the resistor and inductor can be expressed as in equation (3-6) and (3-7).

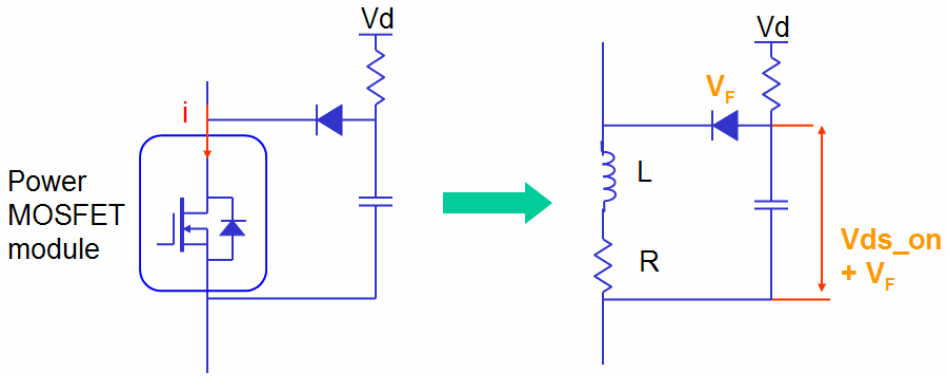


Fig. 3-13 Equivalent circuit of power MOSFET module

$$R = \frac{V_{ds\_on}}{i}\cos\varphi \tag{3-6}$$

$$L = \frac{1}{2\pi f}\frac{V_{ds\_on}}{i}\sin\varphi \tag{3-7}$$

where, f is the frequency of current flowing through the module. φ is the phase angle between the voltage and current waveforms.

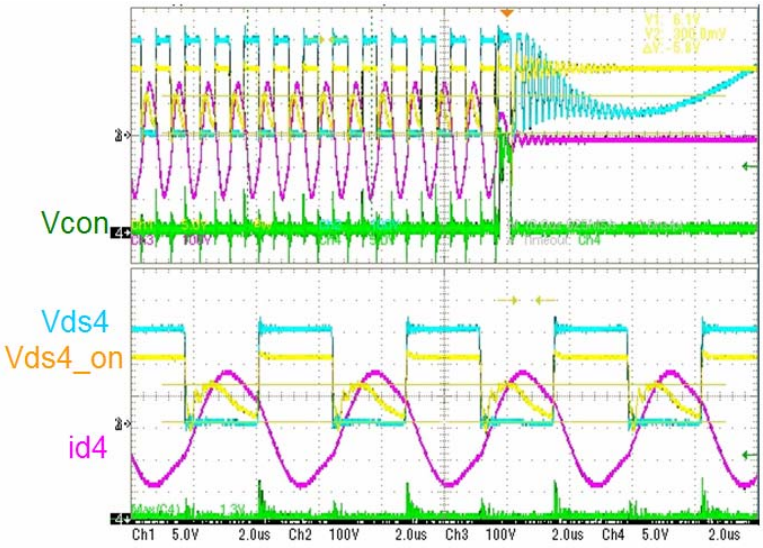


Fig. 3-14 Power MOSFET module switching waveforms at case temperature 90°C

The experiments are conducted under variety of operation conditions for the module like different bus voltages, resonant frequencies etc. A special test has been done for the different case temperatures from the room temperature 25^0C to 90^0C. The case temperature is adjusted by the heated oil flowing through the heatsink. When the case temperature reaches the thermal steady state, the power MOSFET module starts to switch a resonant current for a short time (<0.5 second) at the bus voltage of 600V. The measured typical waveforms are shown in Fig. 3-14. The voltage drop across the power MOSFET module can be calculated from curve V_{ds4_on} minus the diode forward voltage drop.

Table 3-1 Calculated power MOSFET module R and L for different case temperatures (from 30 ^{0}C to 90 ^{0}C)

Tc (^{o}C)	V (V)	I (A)	dt (ns)	f (kHz)	R (mΩ)	L (nH)
30	5.2	178	520	241	17	11.07
55	5.6	178	520	241	18	12.12
65	5.7	178	480	241	20	11.61
75	5.9	178	440	241	22	11.26
80	6.0	178	440	241	22	11.49
90	6.1	178	420	241	23	11.26

According to the equations (3-6) and (3-7), the calculated power MOSFET module conduction resistance R and parasitic inductance L are listed in Table 3-1 for different case temperatures (from 30 ^{o}C to 90 ^{o}C). As the case temperature increases, the measured voltage increases from about 1V due to the conduction resistance temperature dependence. The resonant current frequency can be calculated from the resonant tank value or measured waveforms. The voltage and current phase shift is calculated from the time delay between the two waveforms. The calculated conduction resistance and inductance show that the resistance has a positive temperature coefficient which can be used to predict the junction temperature rise. While the inductance has an almost constant value which implies that the proposed junction temperature prediction approach is

validated. To estimate the junction temperature, the conduction resistance thermal coefficient needs to be known. From offline measurement, the conduction resistance is drawn as a function of junction temperature in Fig. 3-15. The resistance almost linearly increases with the temperature rise.

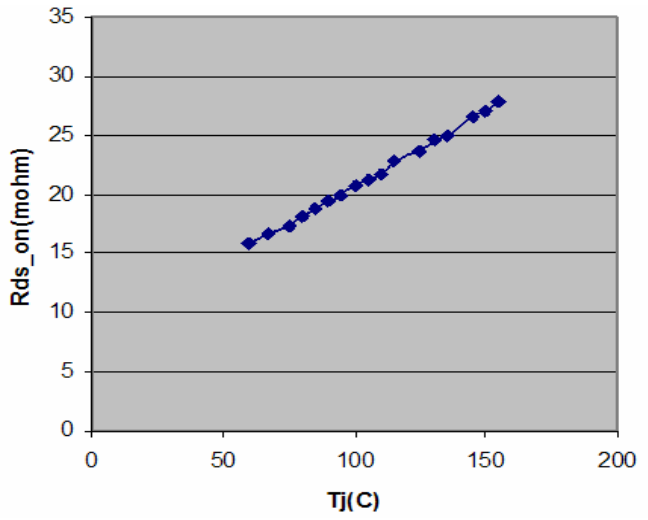


Fig. 3-15 Conduction resistance as a function of junction temperature

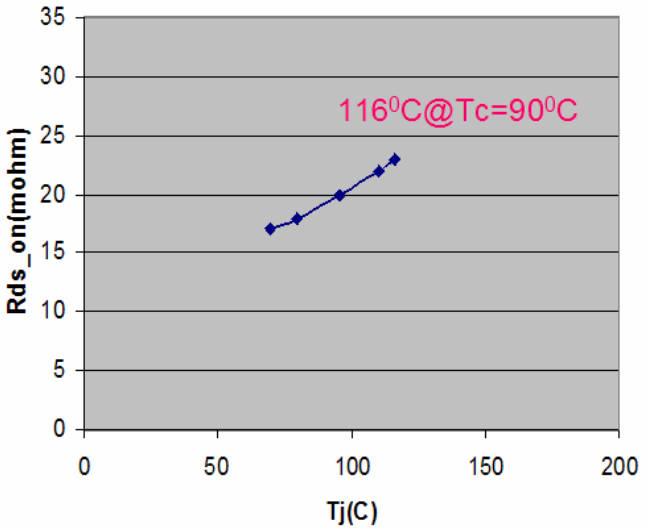
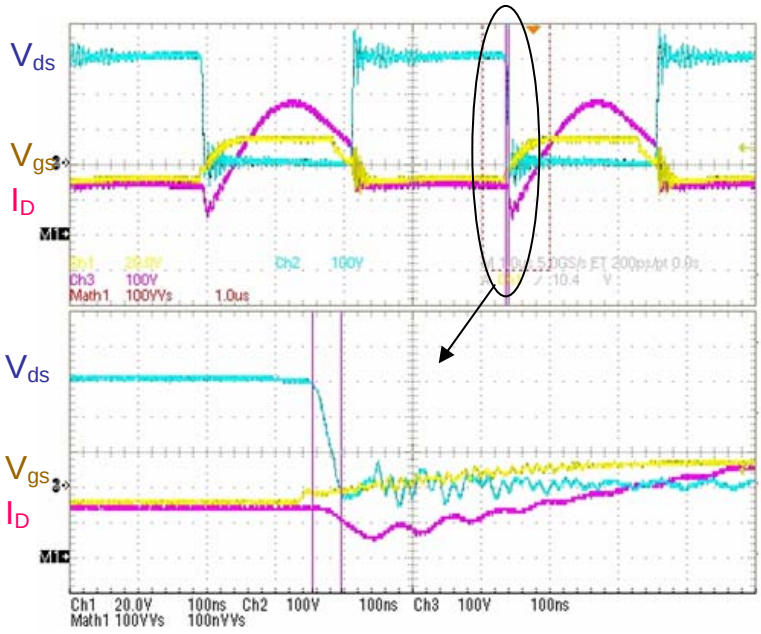


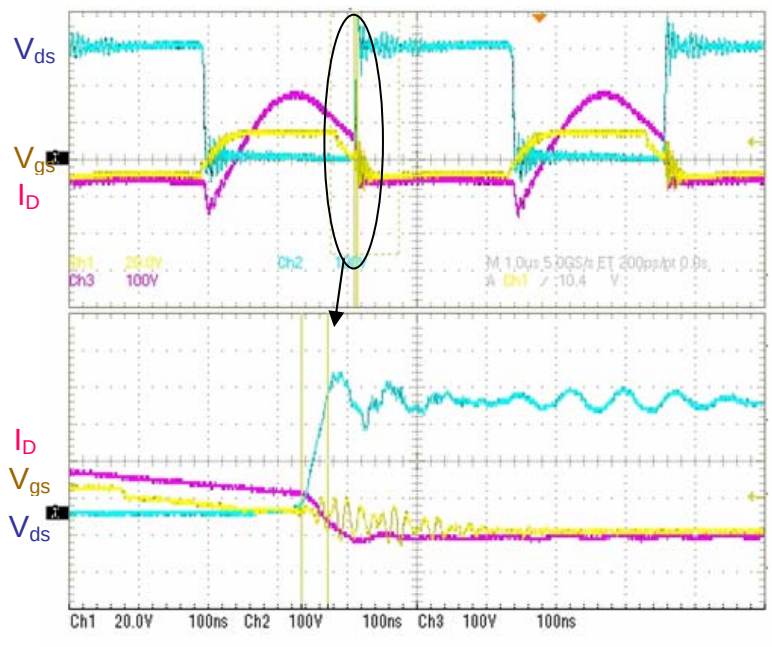
Fig. 3-16 In-circuit measured R_{ds_on} VS junction temperature T_j

The conduction resistance of the power MOSFET module can be measured in circuit by the proposed approach above. Refer to the offline measured curves, the junction temperature can be predicted. The power MOSFET module is tested in circuit for different case temperatures (30^0C ~ 90^0C). The predicted junction temperature is shown in **Fig. 3-16** for the operation condition 300V/180A.

To verify the junction temperature, the theoretical analysis is conducted based on the thermal system in circuit. The device thermal resistance, thermal interface and heatsink thermal resistance are shown in the Fig. 3-18. The power loss can be calculated from the power MOSFET module switching waveforms. According to the turn-on and turn-off voltage and current, the switching loss E_{on} and E_{off} are 0.12mJ and 0.767mJ respectively. The resonant current peak value is about 180A. The switching frequency is 225 kHz. The total calculated power loss for each power MOSFET module is about 400W. The predicted junction temperature is about 112^0C, which is very close to the measured value.



(a) Turn-on waveforms



(b) Turn-off waveforms

Fig. 3-17 Switching waveforms of the power MOSFET module

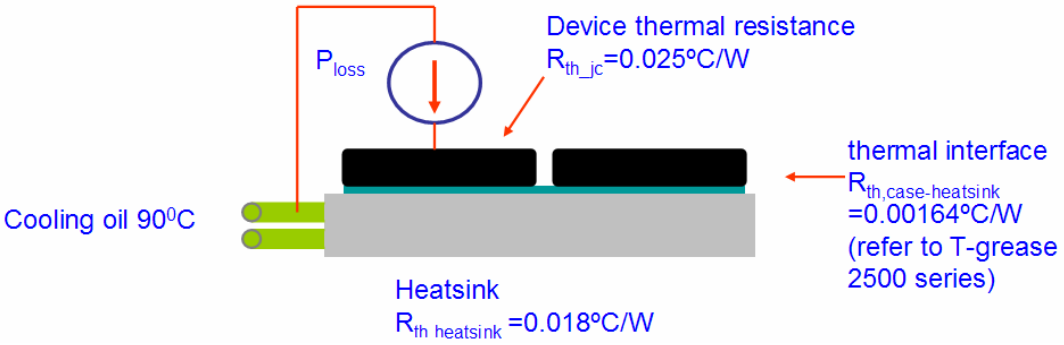


Fig. 3-18 Thermal system for the power MOSFET in circuit

3.7 Power Semiconductor Device Pulse Power and Continuous Power Characterizations

The thermal stability of power semiconductor devices limits their continuous mode operation for high frequency high temperature operation. In the continuous mode

operation, the thermal capacitance is not considered. For the pulse power, the thermal capacitance can storage the power loss and delay the junction temperature rise. During the charge period, the junction temperature rises slowly and during the dead time it decreases almost exponentially.

For the pulse power operation mode, the equation (3-4) can be written as,

$$T_j = T_a + Z_{th} P_{total}(T_j) \tag{3-8}$$

where, Z_{th} is the thermal impedance from junction to ambient, $Z_{th} = \frac{R_{th}}{1 + j\omega R_{th} C_{th}}$. C_{th} is the thermal capacitance from junction to ambient. ω is the switching frequency.

For the thermal balance condition, the equation (3-8) is derivative with junction temperature T_j.

$$\left| \frac{dP_{total}(T_j)}{dT_j} \right| = \frac{1}{R_{th}} \sqrt{1 + (\omega R_{th} C_{th})^2} \tag{3-9}$$

For different switching frequencies and thermal capacitance, the equation (3-9) puts a relax constrain to the thermal stability criteria compared to equation (3-5).

In the pulse power converters like capacitor charger or short pulse generator with high power dissipation, the transient thermal impedance should be considered to calculate peak junction temperature. Many power device manufacturers provide such kinds of transient thermal impedance curves. Fig. 3-19 shows the power device transient temperature rise for the pulse power converters. For constant switching frequency and duty cycle, a series of equations can be derived to predict the maximum junction temperature.

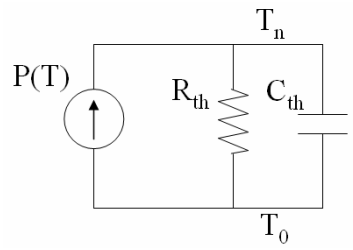
$$T_1 = T_0 + \frac{P}{R_{th}} (1 - e^{-\frac{t_{on}}{R_{th} C_{th}}}) \tag{3-10}$$

$$T_2 = T_1 e^{-\frac{t_{off}}{R_{th} C_{th}}} \tag{3-11}$$

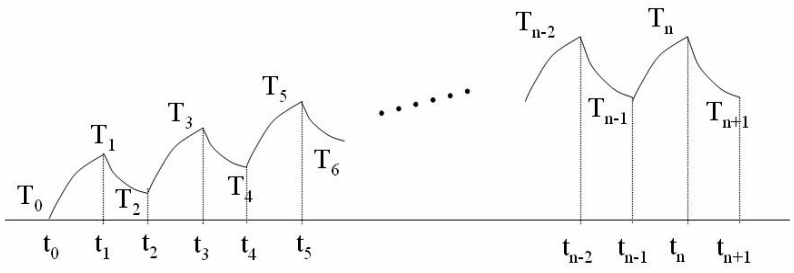
$$T_n - T_{n-2} = [(1-A)k]^{\frac{n-3}{2}}(T_3 - T_1) \tag{3-12}$$

where, $A = \frac{P}{R_{th}}(1 - e^{-\frac{t_{on}}{R_{th}C_{th}}})$, $k = e^{-\frac{t_{off}}{R_{th}C_{th}}}$

From equation (3-12), the switching time t_s to reach steady state can be derived, which is equal to $n(t_{on} + t_{off})$. This is the maximum transient time for the junction temperature to reach steady state. Actually, the maximum junction temperature should be determined combining the thermal stability and transient temperature response. If the switching time is limited, the maximum junction temperature can be higher than the predicted value from the thermal stability graph.



(a) Equivalent thermal network



(b) Transient junction temperature rise

Fig. 3-19 Power device transient temperature rise for pulse power converter

To further understand this phenomenon, a design example is shown in Fig. 3-20. During the charge period, the junction temperature rises slowly and during the dead time it decreases almost exponentially. The power device thermal stability graphs for two

kinds of heatsink with different thermal impedances are shown in Fig. 3-21. This calculated example is also based on the experimental results. Two different kinds of heatsinks with different thermal resistance are used in the experiments. For the continuous mode operation, as an example of switching frequency 300 kHz, the heatsink 2 with higher thermal resistance can result in higher junction temperature rise compared to the heatsink 1. However, in the pulse power mode operation, the heatsink thermal impedance can be neglected if the pulse charge time is much smaller compared to the heatsink thermal time constant. Thus the power MOSFET junction temperature rise is much lower than that of continuous mode operation shown in Fig. 3-21. For some switching frequencies like 500 kHz that the continuous mode operation is not stable for heatsink 2, the pulse power mode operation is stable with lower junction temperature rise.

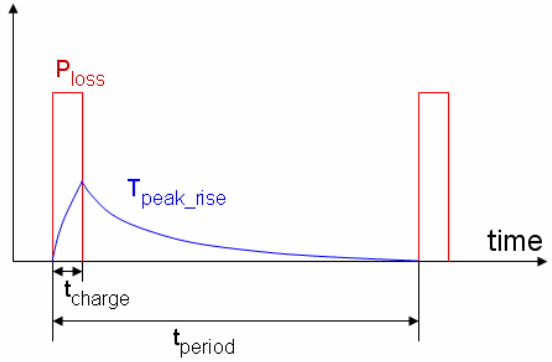
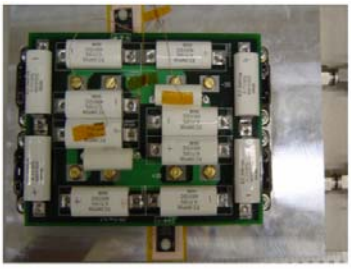


Fig. 3-20 Pulse power charge profile



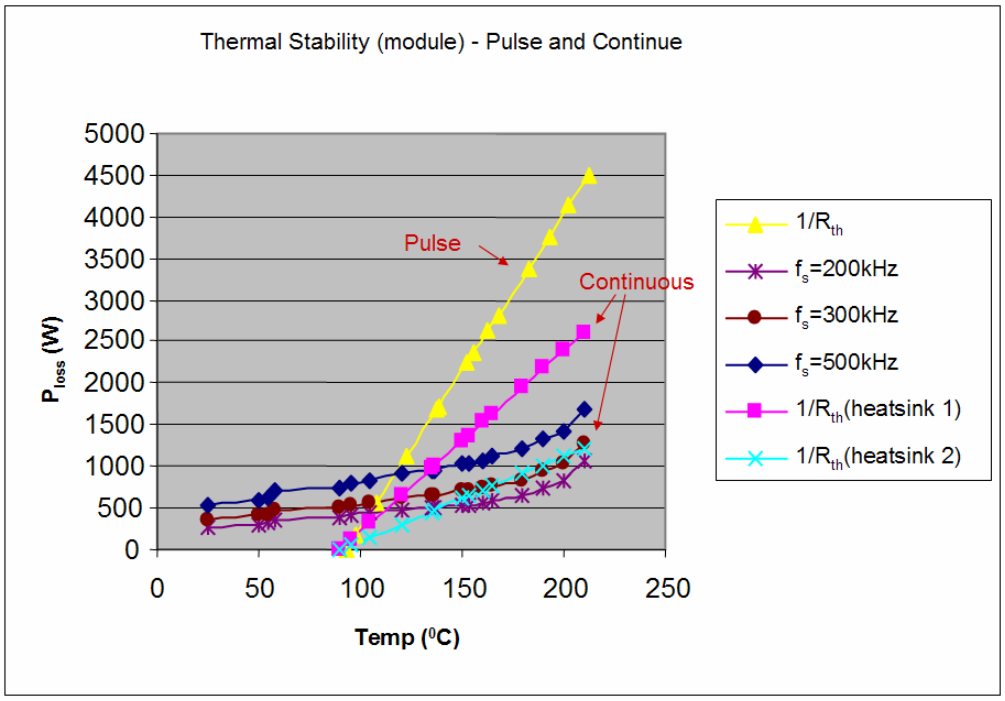
$R_{th\_hs} = 0.0048^{\circ}C/W$

$C_{th\_hs} \approx 2000J/K$

$R_{th\_hs} = 0.018^{\circ}C/W$

$C_{th\_hs} \approx 1000J/K$

(a) Heatsink 1 (left) and heatsink 2 (right)



(b) Thermal stability graphs

Fig. 3-21 Power MOSFET module (6 dice in parallel) thermal stabilities for continuous and pulse power conditions

The high temperature operations of power semiconductor devices are highly affected by the leakage current power loss for continuous and pulse power applications. At high junction temperature the leakage current power loss determines the thermal stability. If not consider the leakage current effect, it seems like both the continuous and pulse power modes are stability even for the higher switching frequency 500 kHz shown in Fig. 3-21, because the slopes of power dissipation lines are always higher than those of the power loss lines. In reality these are not true due to the almost exponential increase of the leakage current power loss which results in that the power loss lines exceed the power dissipation lines shown in Fig. 3-21.

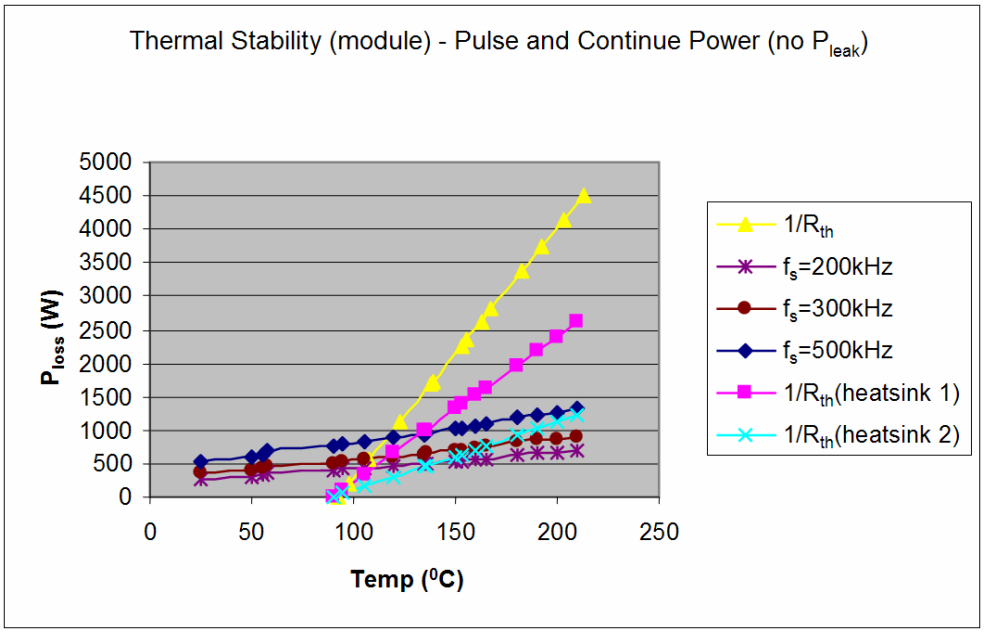


Fig. 3-22 Power MOSFET module thermal stabilities for continuous and pulse power conditions without leakage current effect

From Fig. 3-21 it is shown that the power MOSFET module junction temperature is about 170^{0}C for switching frequency 300kHz and heatsink 2. At this junction temperature the leakage current caused power loss may not contribute much to the thermal stability. There are still some margins to push the device operating at higher junction temperature. Some approaches to realize this and help to benefit the converter system include paralleling fewer devices, using smaller size heatsink or increasing switching frequency. Due to the big size of the power MOSFET module, the power MOSFETs in parallel are preferable to improve power density. The thermal stability graph for the two single power MOSFETs in parallel is shown in Fig. 3-23 for continuous and pulsed power conditions. For the continuous mode the ambient temperature is 90^{0}C. However for the pulse mode the heatsink has certain temperature drop. These result in different intersection points on the x-axial for the power dissipation lines. From the thermal stability graph it is shown that the junction temperature is about 210^{0}C for the heat sink 2 under pulse power mode. At this point, the leakage current caused power loss may cause the thermal instability due to the rapid leakage current increasing.

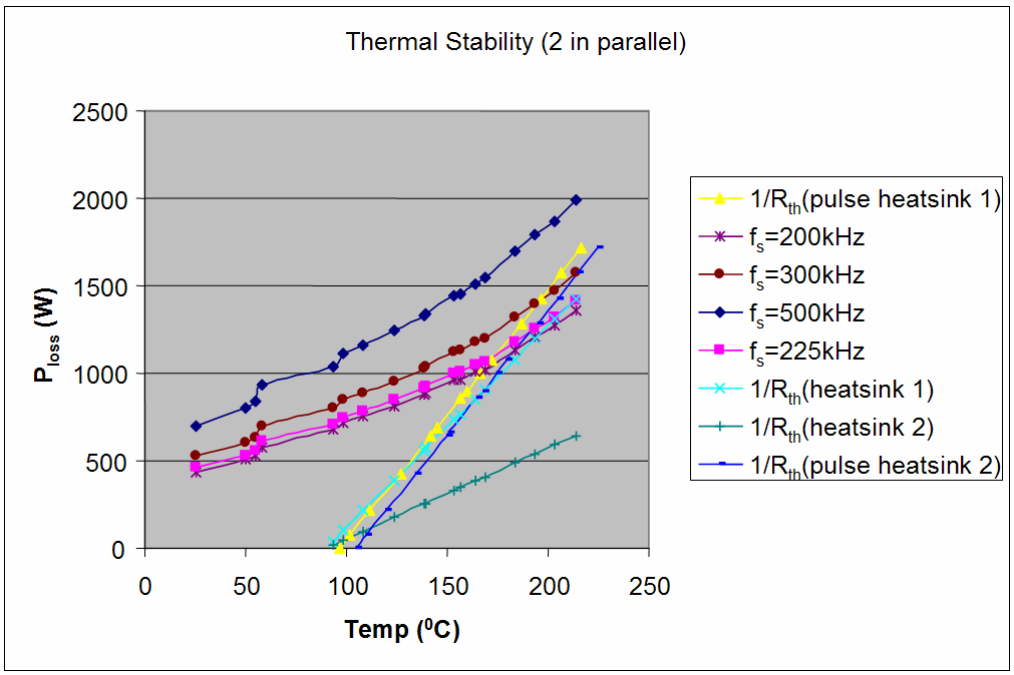


Fig. 3-23 Power MOSFETs (2 dice in parallel) thermal stabilities for continuous and pulse power conditions

3.8 High Temperature Operation Effect on Power Density

The power density is always demanded by the application. To improve power density, three approaches can be implemented,

- Push the switching frequency higher
- Reduce heatsink size
- Increase power level beyond the present level (30kW).

The above are all related to the power device high temperature operation. The higher the switching frequency, the higher the switching loss is. Because the heatsink thermal resistance $R_{th\_heatsink}$ is nearly constant, the power device case temperature T_{case} increases. So the converter power density is mainly determined by the operation switching frequency. From thermal stability point of view, the junction temperature T_j may be higher than 150^{0}C as the device datasheet specified and can be still safe operation. However, in the hardware implementation tests, the measured and predicted junction temperatures T_j are less than 120 ^{0}C for 30 kW power rating, which is much less than the manufacturer provided value T_{j_max} (150^{0}C)

The high junction temperature operation is investigated for power density improvement. For the same 30kW power rating, one approach is to decrease the power device parallel number and push the switching frequency. Thus the active and passive components volumes are decreased. The thermal stability for 3 power MOSFETs in parallel as a main switch is plotted in Fig. 3-24 for continuous and pulse power conditions. For the continuous power operation and heatsink 2 with high thermal resistance, it is not stability even for 200kHz operation. However for the pulse power and heatsink 2, the switching frequency can be pushed up to 500kHz, the junction temperature is about 160^0C for 30kW and the power converter can operate at the stable state. Compared to the existing experiment system,

- Switching frequency increase from 225kHz to 500kHz
- Device footprint decrease by half
- Passive value (L, C) decrease by half
- Heatsink area decrease by half

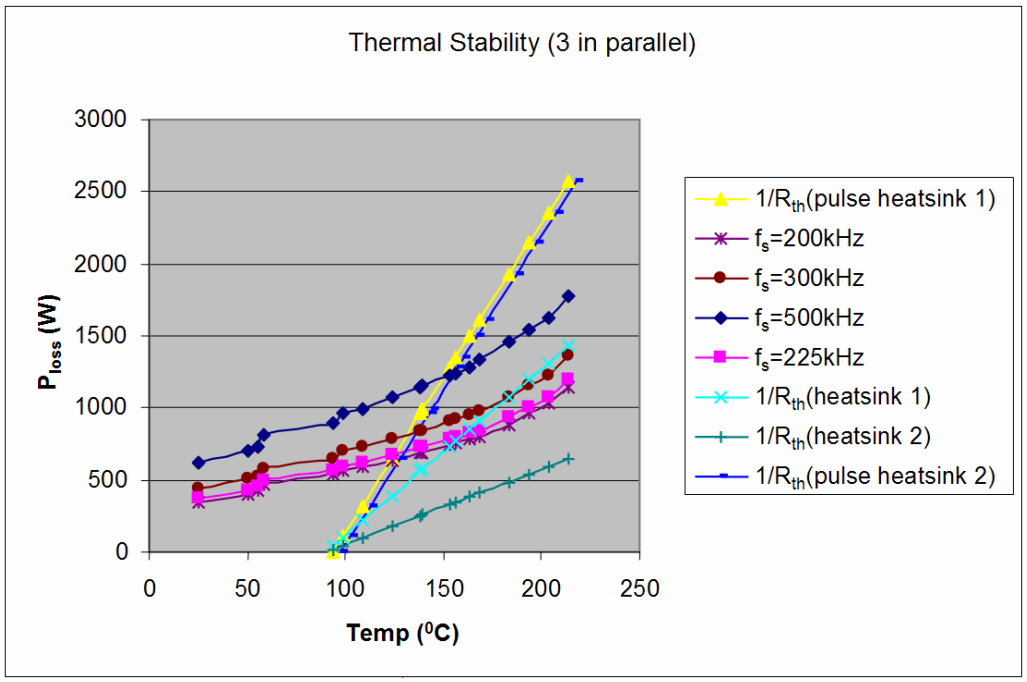


Fig. 3-24 Power MOSFETs (3 dice in parallel) thermal stabilities for continuous and pulse power conditions

From above it can be expected power density improvement for high T_j operation compared to the case that switching frequency is 225 kHz with predicted T_j equal to 130^0C for 30kW pulse power level.

To push the power device operation at the thermal limitation, there is still some margin to increase the switching frequency. When the switching frequency is up to 800 kHz, the power loss line is tangent to the power dissipation line, which is the boundary for the stability with the heatsink 2 for pulse power operation shown in Fig. 3-25. The estimated junction temperature is beyond 200^0C for 30 kW, which is higher than the manufacture provided value. Compared to the existing experiment system,

- Switching frequency increase from 225kHz to 800kHz
- Device footprint decrease by half
- Passive value (L, C) decrease by 3.5 times
- Heat sink area decrease by half

Therefore, high power density is expected to achieve for high junction temperature T_j operation.

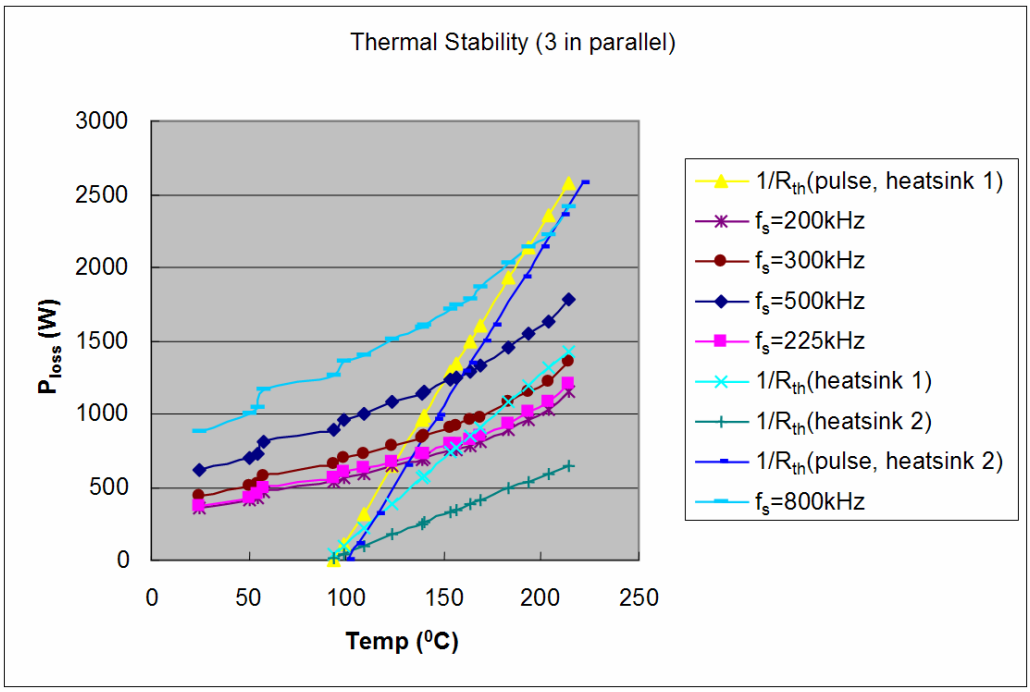
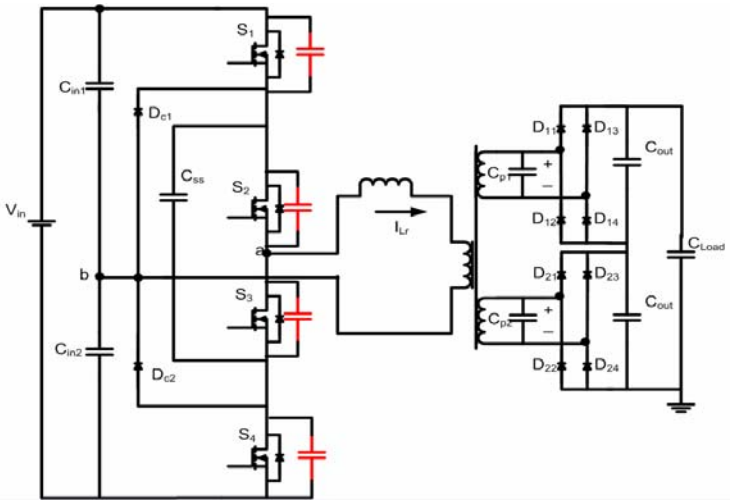


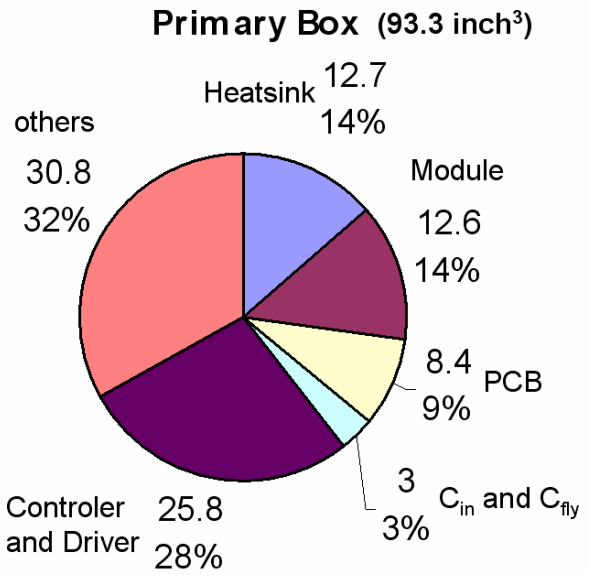
Fig. 3-25 Power MOSFETs (3 dice in parallel) thermal stabilities for continuous and pulse power conditions at high switching frequency

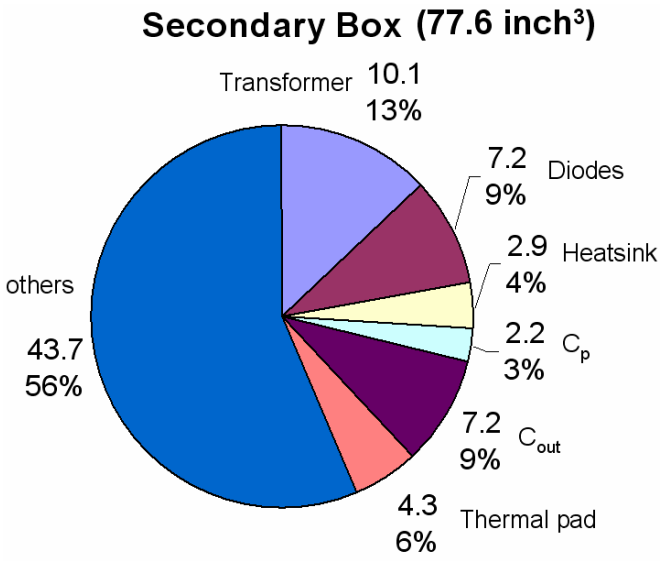
To further decrease the power MOSFET number and push switching frequency, it will become unstable for 2 power MOSFETs in parallel. This case is not considered in the hardware implementation.

According to the Fig. 3-25, the estimated maximum switching frequency is about 800 kHz from the power device thermal stability standpoint. Compared to the existing experiment system, the estimated power density improvements for the pulse power converter high temperature operation are shown in Fig. 3-26.



(a) Schematics





(b) Components volume breakdown

Fig. 3-26 Power density improvement for pulse power high temperature operation (Power density: primary side: 321 W/inch^3, secondary side: 386 W/inch^3, whole converter: 175W/inch^3)

3.9 Summary

The high temperature operation characteristics of power MOSFET have been presented. The device voltage breakdown and thermal stability are tested and analyzed. The variation of the avalanche breakdown voltage with junction temperature rise is verified. Leakage current increases exponentially with junction temperature rise, which contributes to the thermal instability. To study the thermal stability of power device, the closed loop thermal system and stability criteria are developed and analyzed. At low junction temperature and high switching frequency operation, the switching loss determines the thermal stability. At high junction temperature, the leakage current power loss causes the thermal instability. From the developed thermal stability criterion, the maximum switching frequency can be derived for the converter system design. The power device transient temperature rise for pulse power converters is developed. The developed thermal system analysis approach can be extended to other Si devices including IGBT or wide bandgap devices such as SiC power devices. For SiC power MOSFET, the predicted

thermal stable point can be pushed much higher to operate the device at high junction temperature.

To study the power device thermal stability and verify the calculated junction temperature of power device, the experimental junction temperature prediction technique is developed and conducted in the test. The thermal model for the junction temperature rise is proposed. The measured and calculated results match pretty well.

The thermal stability of power semiconductor devices limits their continuous mode operation for high frequency high temperature operation. In the continuous mode operation, the thermal capacitance is not considered. For the pulse power, the thermal capacitance can storage the power loss and delay the junction temperature rise. The power semiconductor device pulse power and continuous power characterization are investigated. It is shown that the power devices can operate much higher switching frequency for the pulse power than that for continuous power. The passive components volume and heat sink size can be minimized thus the power density are improved.

Chapter 4 Power Device Parallel Operation

4.1 Introduction

In order for power converters to achieve high power density, one effective practice is to operate the power converter at a higher switching frequency, reducing the passive components size. However, the high switching losses can prohibit semiconductor devices operating at high switching frequencies. In this case, it is desirable to use power switches with a lower switching loss. Among the state-of-the-art power devices, the power MOSFET has nearly no stored charge, switches very fast and has very low power losses. However, these devices have a high conduction resistance and their current rating often does not meet the requirements for a high power converter. Therefore, the power MOSFETs parallel operation is needed to decrease the conduction loss and increase the high current output [4-1, 4-2].

Fig. 4-1 shows the half-bridge three-level parallel resonant converter developed for a 600V input voltage, 30kW high density capacitor charging application. The power MOSFETs parallel operation is chosen to achieve high switching frequency, low power loss and small package size. However, the power MOSFETs parameters may exhibit some discrepancies, which can be worse as temperature varies. These discrepancies can lead to conduction current unbalance during both a steady state and a switching transient, resulting in power loss and corresponding thermal stress difference for different MOSFETs. The dynamic balance is especially important in power converters employing high frequency, requiring high efficiency or utilizing large pulse currents if the switching loss dominates the total power losses. Clearly, the power MOSFETs parallel operation performances need to be studied for the high frequency high power density converter.

Another issue associated with the power MOSFETs parallel operation is the gate driving power loss due to the increased input gate capacitance. For the conventional resistive gate driving circuit, the gate driving loss is relatively high especially for high switching frequency operation. This may lead to the destruction of the gate driver. So a resonant gate driving technique is applied to reduce the gate driving losses. The proposed

gate driver in this chapter features further reduced power loss, self-power function, thus achieve smaller gate driver size and high power device driving application.

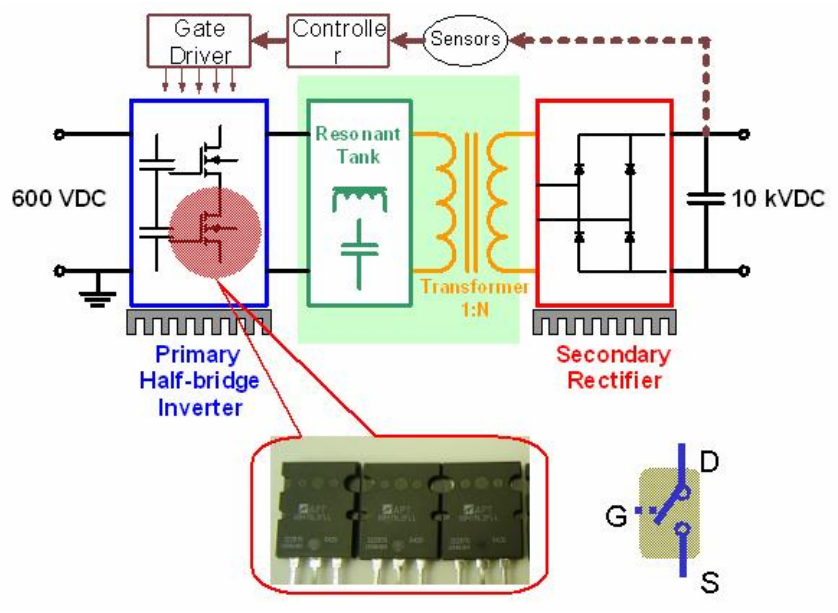


Fig. 4-1 Three-level PRC converter with power MOSFETs parallel as the main switch

It has been reported that power MOSFETs parallel application as the main switch are used in the power factor correction circuit, DC-DC converter and resonant soft switching inverter etc before [4-1]-[4-3]. Normally, it is believed that the power MOSEFT conduction resistance has a positive temperature coefficient, such that the parallel performances are analyzed without paying much attention to the current sharing. Someone adds the voltage snubber circuit individually for each power MOSFET instead of directly paralleling them together to decrease the turn-on loss related to the diode reverse recovery shown in Fig. 4-2 [4-1]. In paper [4-3], the power MOSFETs are directly paralleled and used in the resonant soft switching inverter without balancing switching transient currents, which results in the uneven power dissipation among the devices. Recently, the current and thermal distribution under avalanche voltage condition was investigated for the paralleled power MOSFETs as a single switch to investigate the safe operation area shown in Fig. 4-3 [4-4]-[4-5]. Actually, current sharing is more difficult for power MOSFETs than for IGBTs although these two are all voltage-

controlled devices because the turn-on/off time is much shorter for power MOSFETs [4-6]-[4-7]. To meet the demand for a high power high density converter, the power MOSFETs parallel is still a promising approach for high frequency operation to reduce the passive components size. However, the increased switching loss associated with the transient current unbalance may limit the device thermal performance.

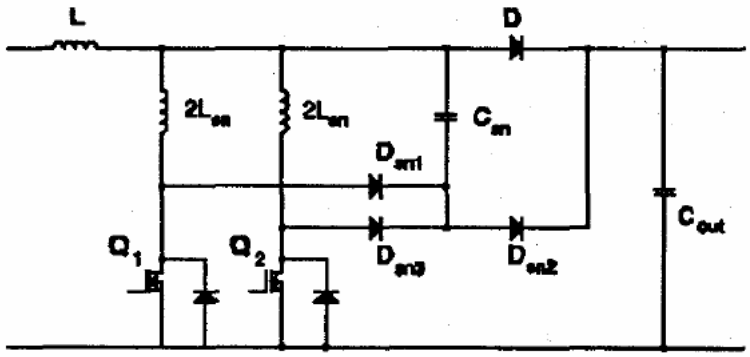
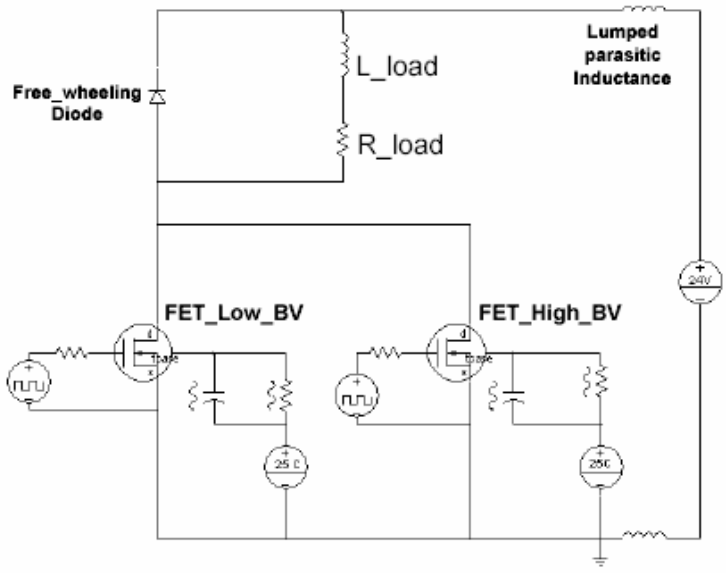
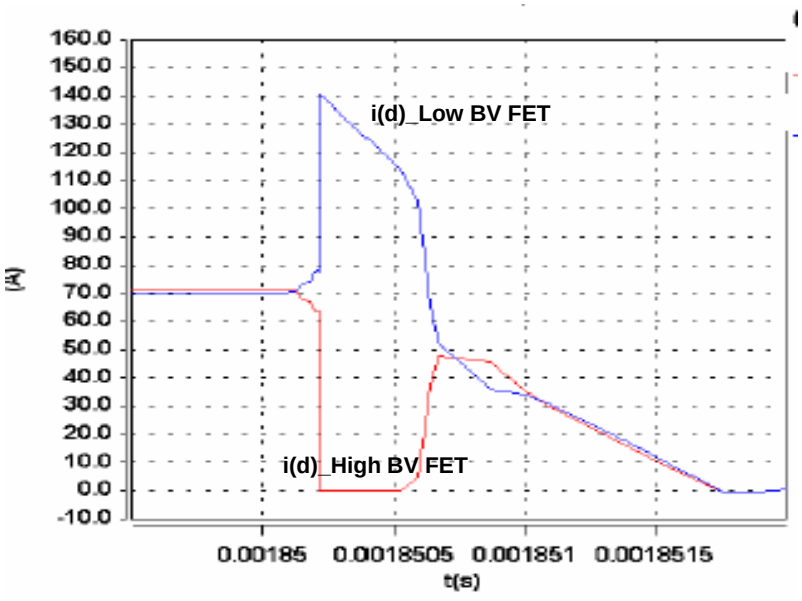


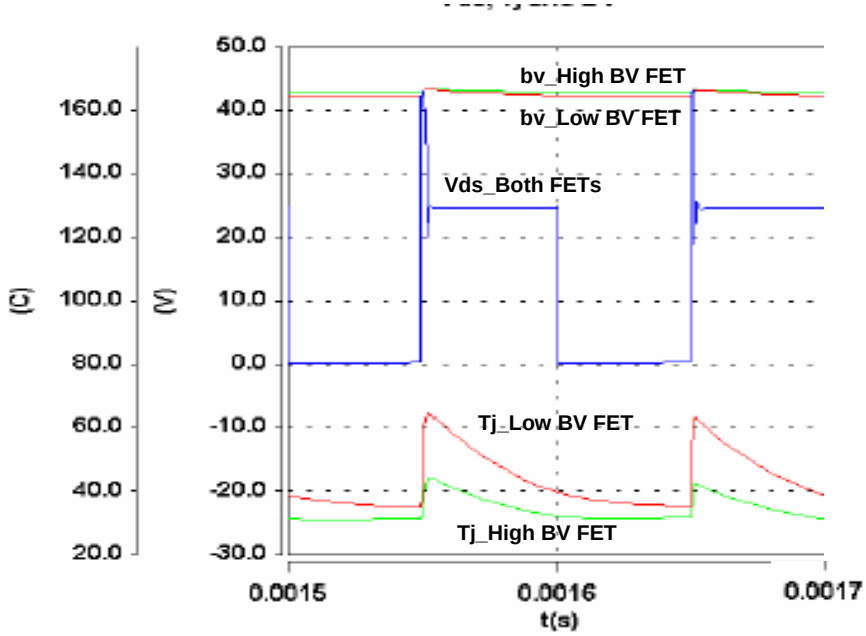
Fig. 4-2 Paralleling power MOSFETs with snubber circuits in power factor correction circuit [4-1]



(a) Thermal behaviors under avalanche operation



(b) Current unbalance due to avalanche process



(c) Thermal behavior

Fig. 4-3 Current and thermal behaviors under avalanche operation for paralleling power MOSFETs [4-4]-[4-5]

This chapter first presents an analysis for understanding the conduction state and switching transient current sharing among parallel power MOSFETs. The power

MOSFETs parameters mismatch effects are introduced. The conduction state and switching transient current unbalance and power loss are analyzed for the selected power MOSFETs considering the temperature effect, power stage parasitic inductance and gate driver design. A dynamic current balancing approach is developed and verified with the experiments, showing the benefit of the reduced switching losses. Then the advanced gate driving technique is developed. The proposed gate driver in this chapter features further reduced power loss, self-power function, thus achieve smaller gate driver size and high power device drive application.

4.2 Conduction State Current Sharing

There can be a number of causes for current unbalance when power MOSFETs are in parallel operation. The MOSFET parameters may exhibit potential mismatch during the fabrication processes. These differences between power MOSFETs may result in a particular device exceeding its peak current or continuous thermal rating. These parameters include the on-state drain-to-source resistance, threshold voltage, input-to-output transconductance, the parasitic gate-to-source and gate-to-drain capacitance etc. Some of them can have stronger effect on the current unbalance than others. Individually or combined together, mismatch between these parameters may produce serious unbalance. Table 4-1 shows the parameter range from the datasheet for the selected power MOSFETs (APT60M75L2FLL). The threshold voltage may have a 50% difference between the devices. Most importantly, the transconductance or gain factor mismatch is up to 80%, which is extremely critical for the switching transient current sharing. The normal conduction resistance is about 75mΩ with the tolerance of 30%. However the junction temperature has a great influence on the resistance value, making the resistance difference even larger.

In addition, the parasitic components in the power stage circuits and gate loop can also cause the current unbalance, even leading to gate loop or power stage oscillation.

Table 4-1 Parameters range of the selected power MOSFETs

Source	Parameter Range		
	Threshold voltage, V_T	Transconductance or Gain Factor, GF	ON Resistance $R_{DS(on)}$
Data Sheet	4V (3-5V,2V)	14.4 A/V^2	0.075Ω
Extremes min/max Δ=	75-125%, 50%	60-140%, 80%	70-130%, 60%

The power MOSFETs are voltage controlled devices, and the drain currents are inherently limited by the gate-to-source voltage. During the on-state, assuming the gate voltages for all the parallel MOSFETs are the same, the current sharing is limited by the conduction resistance. The worst case is that one of the parallel power MOSFETs has a different conduction resistance from the others. To analyze this phenomenon during the on-state, a simplified circuit is used in Fig. 4-4. Assuming R_1 is the first power MOSFET conduction resistance, the rest are expressed as $R_2/(N-1)$, where R_2 is the remaining single power MOSFET resistance.

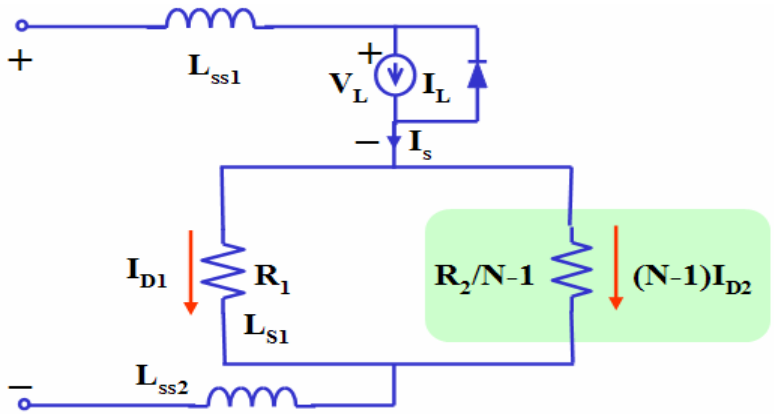


Fig. 4-4 Simplified circuit during the conduction state

The current unbalance will cause different power loss. If the thermal resistance is constant and not affected by the temperature, the junction temperature difference may exist between the parallel MOSFETs. To analyze the current sharing, the temperature

effect should be considered for the steady state. The measured conduction resistance is plotted as a function of junction temperature for the selected power MOSFETs shown in Fig. 4-5. It increases almost linearly with the temperature due to the carrier mobility reduction. When the temperature is up to 150^0C, the conduction resistance is about three times higher than that in room temperature. This increased resistance will generate more conduction loss, which heats the device again. The developed high power density capacitor charging converter operates at an ambient temperature of 90^0C. The junction temperature may go even higher under the current unbalance and conduction resistance changing condition.

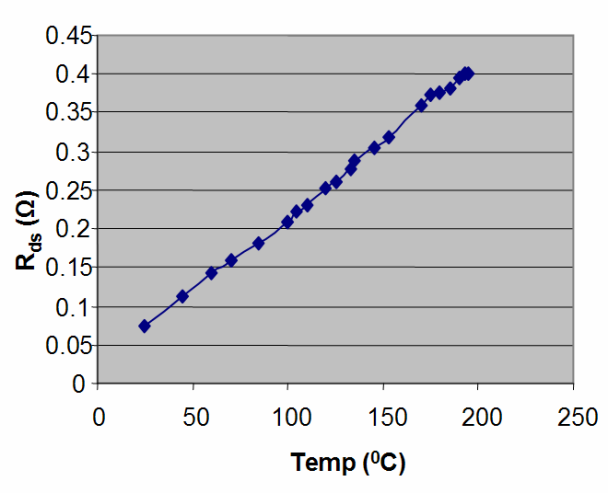


Fig. 4-5 Conduction resistance R_{ds} as a function of junction temperature

The unbalance current can be plotted as a function of the power MOSFET conduction resistance mismatch in Fig. 4-6. The current i_B is the balanced current and i_{D1} is the drain current of the first MOSFET whose conduction resistance is different from the others. R_{1-25} and R_{2-25} are the conduction resistances of the first and the other power MOSFETs respectively at room temperature (25^0C). The solid and dotted lines are for the conditions with and without considering the temperature effect. Generally, for large conduction resistance mismatch, the current unbalance increases. Also, a substantial reduction in the current unbalance is predicted when temperature effects are considered for a large number of power MOSFETs in parallel. This is because a smaller resistance conducts a higher current. Thus more heat generates and results in resistance increase. So the current is balanced to some extant. However the temperature cannot completely compensate for

the current unbalance caused by the conduction resistance mismatch. For a small number of power MOSFETs in parallel, the temperature compensation has a reduced effect. That is because when more power MOSFETs are in parallel, current decrease in one MOSFET causes a minor current increase for the others.

The conduction power loss also changes with the conduction resistance mismatch. Referring to the equivalent circuit during the conduction state in Fig. 4-4, the power losses can be derived for the current balance and unbalance conditions. The power loss for unbalance condition P_{uB} over that for balance condition P_B can be expressed as in equation (4-1).

$$\frac{P_{uB}}{P_B} = \frac{N}{[1+(N-1)k]^2}k + \frac{(N-1)N}{[(N-1)+1/k]^2} \tag{4-1}$$

where, $k = \frac{R_{1-25}}{R_{2-25}}$.

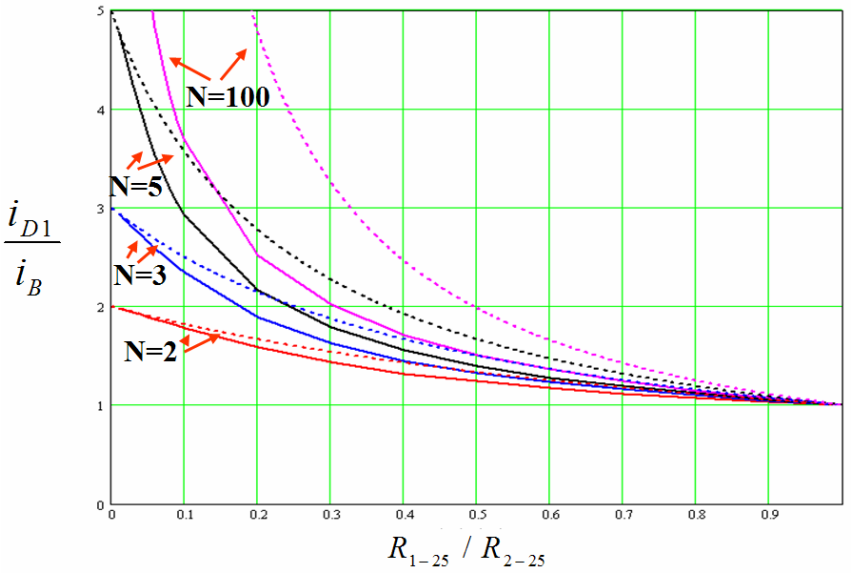


Fig. 4-6 Current unbalance as a function of conduction resistance mismatch (solid lines: with temperature effect; dotted lines: without temperature effect)

The conduction power loss change is plotted as a function of conduction resistance mismatch in Fig. 4-7. For the balance condition the conduction losses have no change.

When one power MOSFET has a different resistance $R_{1\text{-}25}$ from the others $R_{2\text{-}25}$, the total conduction losses may decrease or increase, depending on whether $R_{1\text{-}25}$ less or greater than $R_{2\text{-}25}$. When more power MOSFETs are paralleled, a substantial reduction in the conduction power loss unbalance is predicted due to the current unbalance compensation effect. When temperature effects are considered for the conduction resistance and current unbalance shown in Fig. 4-4, the conduction power loss change can be further reduced for a large number of power MOSFETs in parallel, which is not shown in Fig. 4-7. This is because the smaller resistance conducts higher current, thus more heat generates and results in resistance increase. So the conduction power loss change can be achieved to some extant.

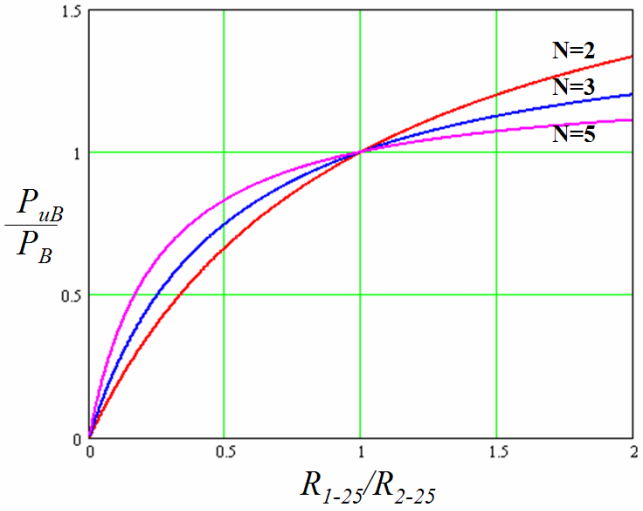


Fig. 4-7 Conduction power loss change as a function of conduction resistance mismatch

4.3 Switching Transient Current Sharing

The switching transient current sharing is more complicated. Not only can the device parameters like gain factor, threshold voltage, and Miller capacitance cause transient current unbalance, but also the power circuit stage parasitic inductance can cause differential currents and transient energies. For the power MOSFETs parallel switching transient, assuming the first device has different parameters from others, an equivalent

circuit can be drawn in Fig. 4-8. During the switching period, the power MOSFET operates at active region, which can be modeled as a voltage controlled current source. The drain and source parasitic inductance also have some effects, which will be explained and considered in the next section.

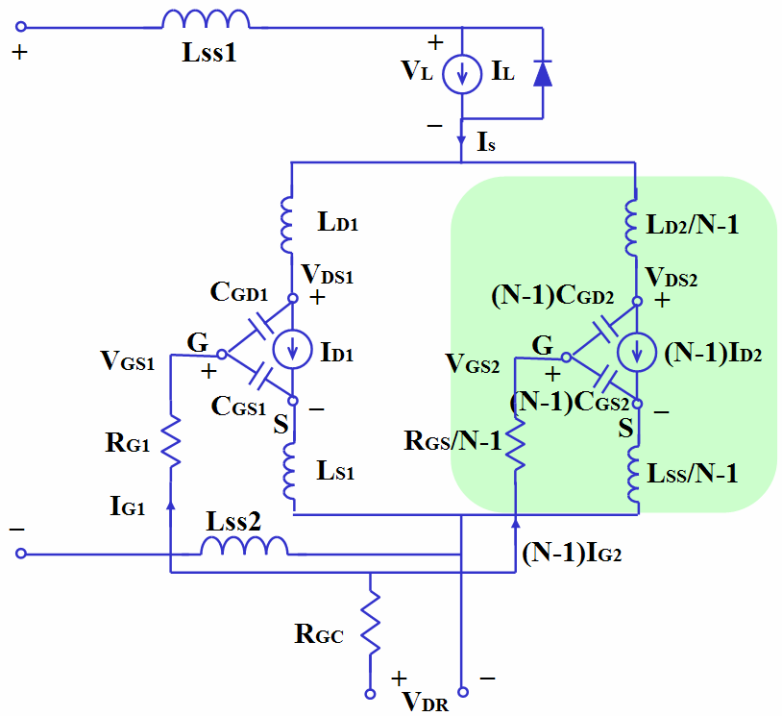


Fig. 4-8 Equivalent circuit during switching transient

Table 4-2 Normalized values for device parameters mismatch

Device	I_{DM} (A)	GF(A/V^2) (25C)	V_T (V) (25C)	I_{DM}/GF	(I_{DM}/GF) ^0.5	ΔV_{TN} (max.)	GF_{1N} (max.)	GF_{2N} (min)	GF_1/GF_2 (max.)
APT 60M75L 2FLL	292	14.4	4	20.3	4.5	0.44	1.4	0.6	2.33

To analyze the current unbalance, the first power MOSFET drain current over gain can be expressed as a function of the other MOSFETs drain current over gain under the different threshold voltages in equation (4-2) [4-8].

$$\frac{I_{D1N}}{GF_{1N}} = \{\frac{(N-1)}{\frac{GF_{1N}}{GF_{2N}} + N - 1}\Delta V_{TN} + \sqrt{\frac{N}{\frac{GF_{1N}}{GF_{2N}} + N - 1} \cdot \frac{I_{BN}}{GF_{2N}} - \frac{(N-1)\Delta V_{TN}^2}{[\sqrt{\frac{GF_{1N}}{GF_{2N}}} + (N-1)\sqrt{\frac{GF_{2N}}{GF_{1N}}}]^2}}\} \tag{4-2}$$

where, $I_{D1N} = \frac{I_{D1}}{I_{DM}}$, $I_{BN} = \frac{I_B}{I_{DM}}$, $GF_{1N} = \frac{GF_1}{GF}$, $GF_{2N} = \frac{GF_2}{GF}$, $\Delta V_{TN} = \Delta V_T / \sqrt{\frac{I_{DM}}{GF}}$, I_{D1} and GF_1 are the first power MOSFET drain current and transconductance. I_{DM} is the pulse drain current limited by the thermal constrain. I_B and GF are the average drain current and transconductance. GF_2 is transconductance for the rest of power MOSFET. ΔV_T is the threshold voltage difference between the power MOSFETs. These values are calculated according to the device datasheet and shown in Table 4-2.

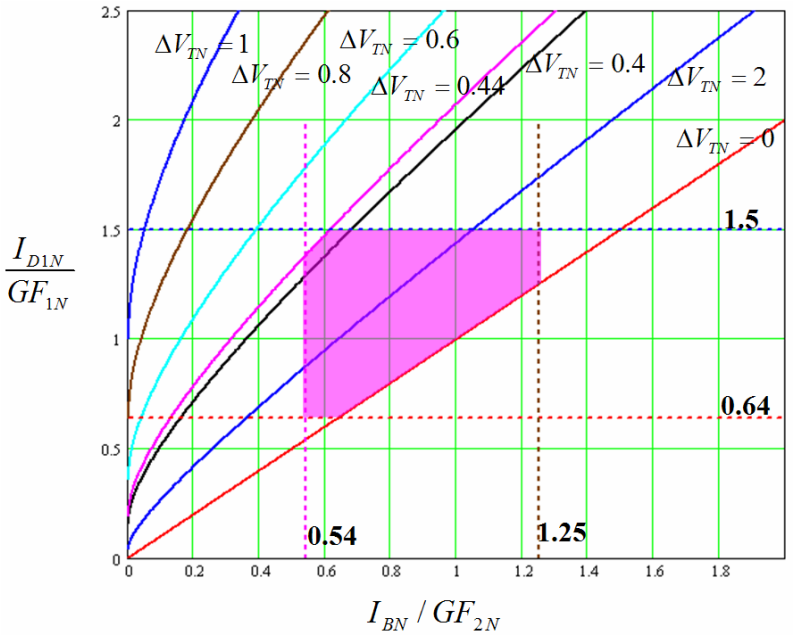


Fig. 4-9 Switching transient current unbalance map for power MOSFETs in parallel

The switching transient current unbalances for the simultaneous mismatch of gain and threshold voltage are illustrated in Fig. 4-9. For different threshold voltage mismatch, a group of curves can be plotted in the graph. If the maximum potential current unbalance

is limited to 20%, the calculated values for I_{D1N}/GF_{1N}, I_{BN}/GF_{2N}, ΔV_{TN} are given in equation (4-3). These limit boundaries form the shaded area in Fig. 4-9. If one chooses the power MOSFETs whose parameters fall into this area, the current sharing will meet the requirement. The corresponding current unbalance can be illustrated in Fig. 4-9.

$$0.64 \le \frac{I_{D1N}}{GF_{1N}} \le 1.5$$

$$0.54 \le \frac{I_{BN}}{GF_{2N}} \le 1.25$$

$$0 \le \Delta V_{TN} \le 0.44 \tag{4-3}$$

To balance the current between the parallel power MOSFETs, the gate driving effects on current sharing are studied below. Besides the device parameters mismatch, the gate driving performance also affects the device current sharing. During the switching transient, the power stage parasitic inductances need to be considered, especially the inductances within the gate driving loop. A simplified relationship during turn-off between the drain current and gate resistance can be found in equation (4-4).

$$\begin{aligned} i_D(R_g) = (V_{DS} - V_S)/[L_x(V_g - \frac{V_t - V_B}{2})/(R_g Q_{gd}) \\ - V_{DS}(L_x(V_g - \frac{V_t - V_B}{2})L_s L_g C_{oss}/(R_g Q_{gd}^2))] \end{aligned} \tag{4-4}$$

where, R_g is gate resistance, L_x is power stage parasitic inductance, L_g and L_s are gate and source parasitic inductance, V_g and V_s are gate and source voltage, V_t and V_B are threshold voltage and average threshold voltage, Q_{gd} is the miller capacitor charge, and C_{oss} is power MOSFET output capacitance.

The drain current is plotted as a function of drain-to-source voltage for different gate resistances shown in Fig. 4-10. Because the power MOSFETs are connected in parallel, they have the same drain-to-source voltage. From Fig. 4-10 one can see that the drain current becomes bigger when larger gate resistance is used during turn-off. By properly designing the gate driver, a reasonable current balance can meet the power converter

switching power loss requirements. There is a trade-off between the gate driver design and the switching losses [4-9].

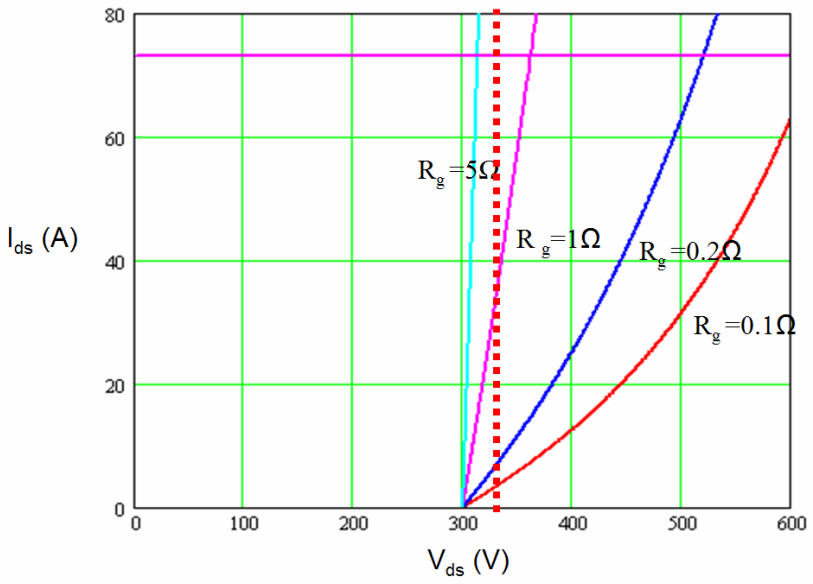


Fig. 4-10 Gate driving effects on current sharing

4.4 Current Sharing Techniques and Verification

To balance the currents for the power MOSFETs parallel operation, a gate voltage control method by controlling the gate current during the Miller period is developed for switching transient current sharing. The drain current is inherently related to the gate voltage during the device active region. The gate driver charges the power MOSFET gate capacitance through the gate resistance. The drain current slew rate is determined by the gate voltage change. The typical turn-on waveforms for two power MOSFETs in parallel are shown in Fig. 4-11. If the power MOSFETs parameters mismatch, the drain currents may have different slew rates under the same gate-to-source voltage during the turn-on/off transient. Its relationship with the gate driver circuit can be approximately expressed in equation (4-5). By properly designing the gate driving circuits the drain side currents can be balanced to some extent.

$$\frac{di_D}{dt} \approx g_m \frac{V_g}{\tau} e^{-t/\tau} \tag{4-5}$$

where, $\tau \approx R_g C_{gs}$, τ is the time constant, R_g is the gate resistance, and C_{gs} is gate capacitance.

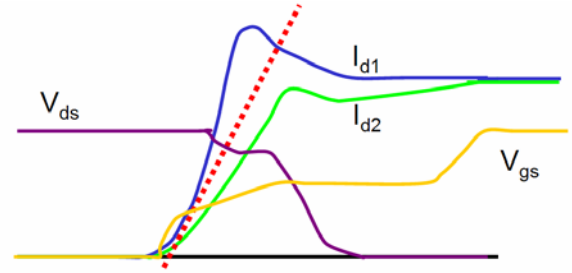
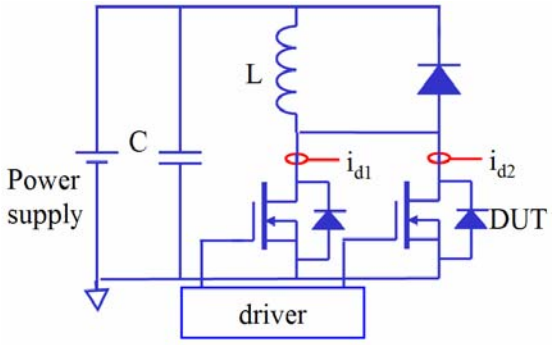
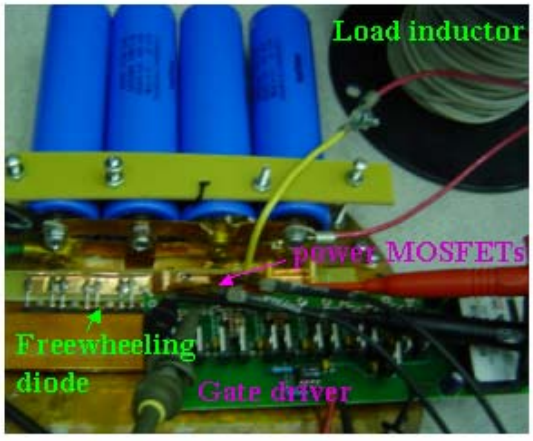


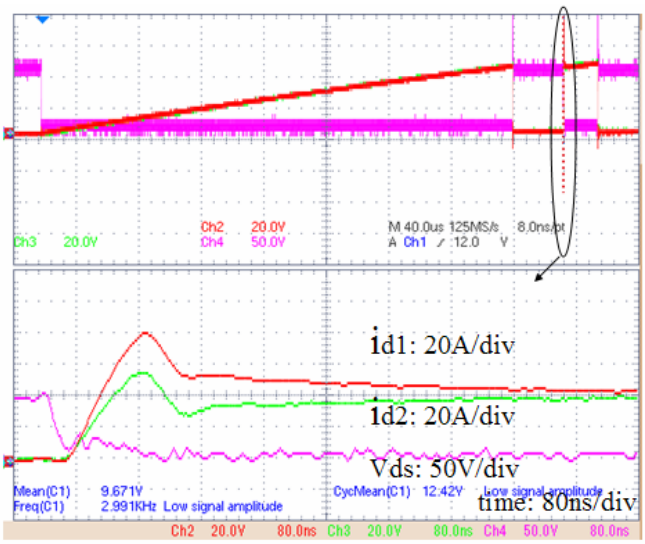
Fig. 4-11 Principle of current balancing approach



(a) test schematic



(b) test setup



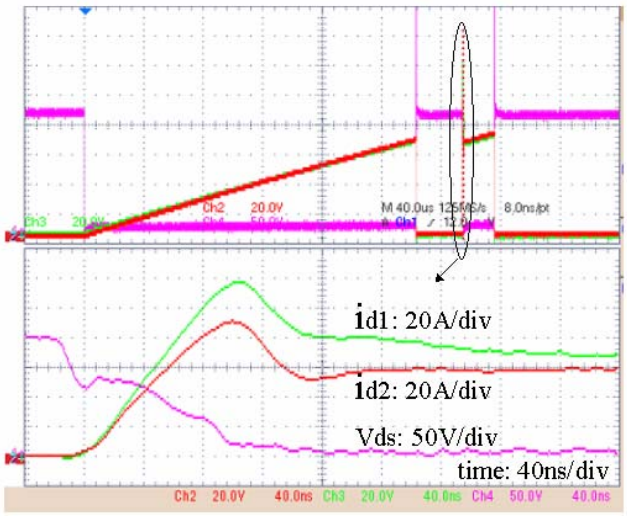
(c) Turn-on waveforms for the switching transient current sharing (200V/65A/3Ω & 3.2Ω)

Fig. 4-12 Experimental setup for two power MOSFETs in parallel

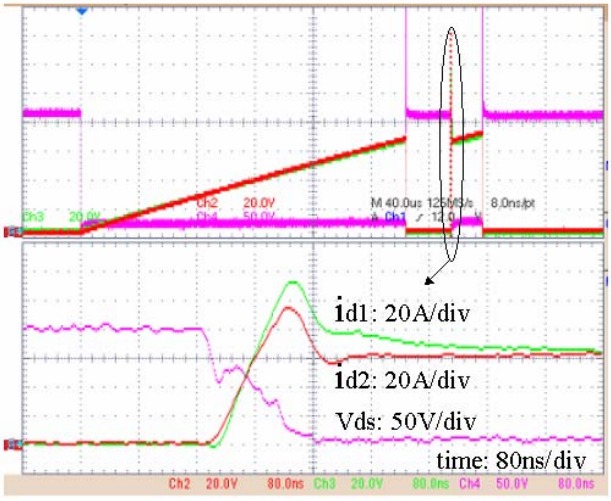
The experiments are conducted for two power MOSFETs in parallel in Fig. 4-12. The test switching waveforms are shown in Fig. 4-13 and Fig. 4-14 to verify the validity of above approach. Due to the fast switching that is intrinsic of the power MOSFET, the switching waveforms are affected by the gate resistance and power stage parasitic inductance. The smaller the gate resistance, the faster the turn-on/off speed is. During the turn-on transient, the voltage drop across the parasitic inductance may dominate, leading to the power MOSFET drain-to-source voltage lower. A tested turn-on example is shown in Fig. 4-12 (c) for gate resistance 3Ω and 3.2Ω for two power MOSFETs in parallel. The V_{ds} drops very quickly and the voltage across the device is low. This is similar to the soft-switching condition. The current unbalance is not as accurate as that of the hard switching condition. After many repeated experimental studies, the gate resistance (about 10 Ω) is chosen to study the current balance technique based on the above consideration.

During turn-on transients, the switching drain currents have a great difference between the two parallel power MOSFETs without current balance approach. The drain currents reach different peak values due to some parameter mismatch during the transconductance period. The power MOSFETs gate channel resistances are variable during the current rise transient. After a certain time the drain currents come together because the gate voltages and conductance resistance approach equal for the parallel power MOSFETs. After

implementing the current balance approach, the transient currents difference can be minimized to some extent. The drain currents close together during rise time and the peak value difference is smaller. Accordingly the current unbalance time decreases due to the gate driving effects. The switching process and turn-on loss is also associated with the freewheeling diode reverse recovery. For comparison, integrations of the voltages and currents indicate that the turn-on loss decreases for the balance condition, which is 14% lower than the unbalance condition shown in Fig. 4-13.



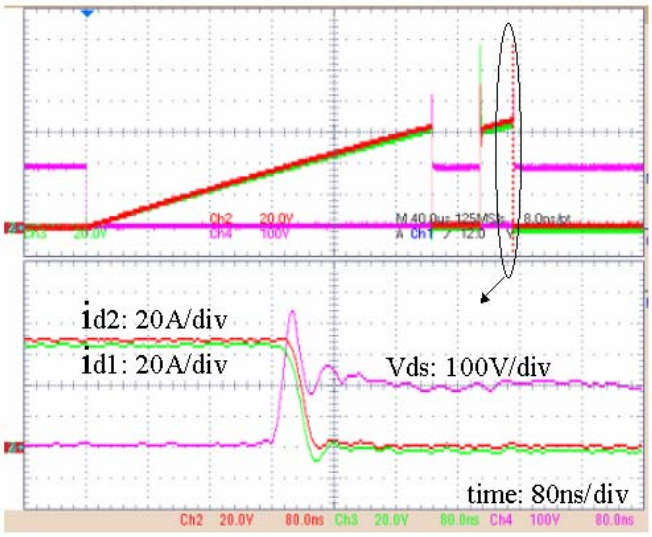
(a) Without the current balance approach



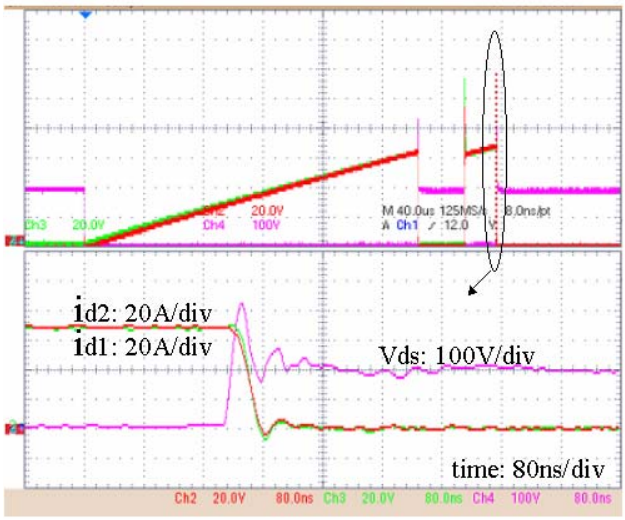
(b) With the current balance approach

Fig. 4-13 Turn-on waveforms for the switching transient current sharing (200V/65A/10Ω & 10.6Ω)

During the turn-off transients, the situation is similar and is shown in Fig. 4-14. First, the faster MOSFET drain current drops, leading to other MOSFET carrying more current, which is the opposite of the turn-on condition. The steady state current differences may contribute to the current probe issue with the floating ground and conduction resistance discrepancy. After implementing the current sharing approach, the two power MOSFET currents come together and, thus the transient time decreases. Accordingly, the calculated turn-off loss is 11% smaller compared to the unbalance conditions shown in Fig. 4-15.



(a) Without the current balance approach



(b) With the current balance approach

Fig. 4-14 Turn-off waveforms for the switching transient current sharing (200V/70A/10Ω & 10.6Ω)

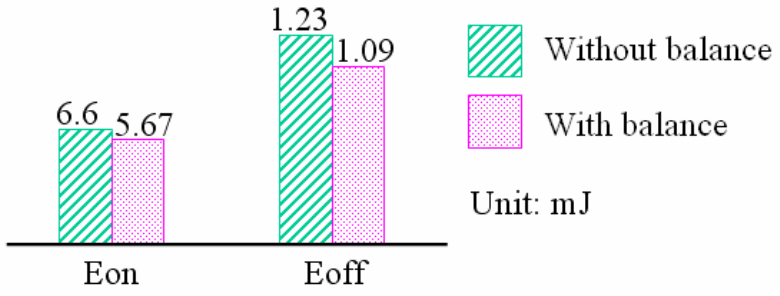
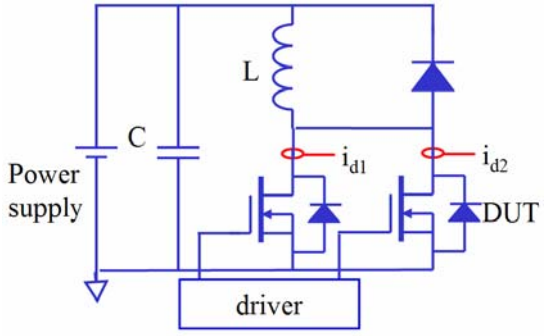


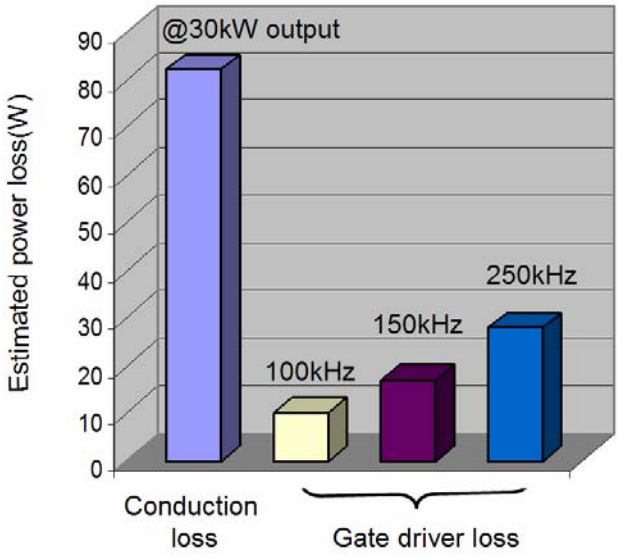
Fig. 4-15 Switching loss comparisons without and with current sharing control approach

4.5 Gate Driving for Power MOSFET Module

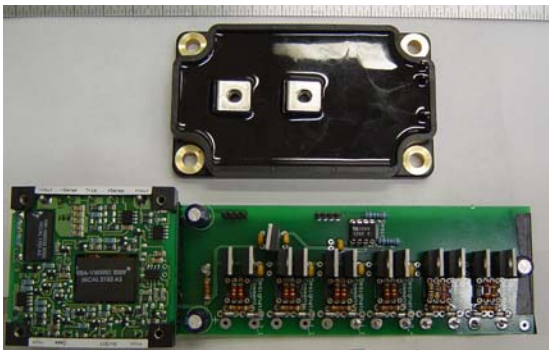
The future power converter must process energy with high efficiency and high power density. In order to achieve high power density, one common practice is to operate the converter at a high switching frequency in order to reduce passive component size. The power MOSFETs are desirable for these applications due to their high input impedance, fast inherent switching speed and ruggedness. The power MOSFET parallel module normally has to be used to meet the high power requirement. However, one issue related to high frequency applications is the significant gate driving losses, especially for the parallel power MOSFET chips with increased input capacitance. When the power MOSFET modules are used in the parallel resonant converter (PRC) for pulse power application, as an example, the gate driver loss is shown to compare with the conduction loss. For a conventional gate driving circuit with gate resistor, shown in Fig. 4-16, the gate driving loss is relatively high comparable to the conduction loss at more than 200 kHz. The gate-driving loss is almost proportional to the switching frequency. This loss can be significant when the switching frequency is high [4-12]. The power dissipation caused by charging and discharging of the gate capacitance becomes remarkably high, which may lead to the destruction of the gate driver. The increased gate driver loss needs a corresponding high power isolated DC/DC converter to supply the power. The hardware implementation shows the bulky volume of conventional gate driver in Fig. 4-16.



(a) Conventional resistive gate driver schematic



(b) Gate driver loss for a PRC pulse power converter



(c) Hardware implementation showing bulky volume

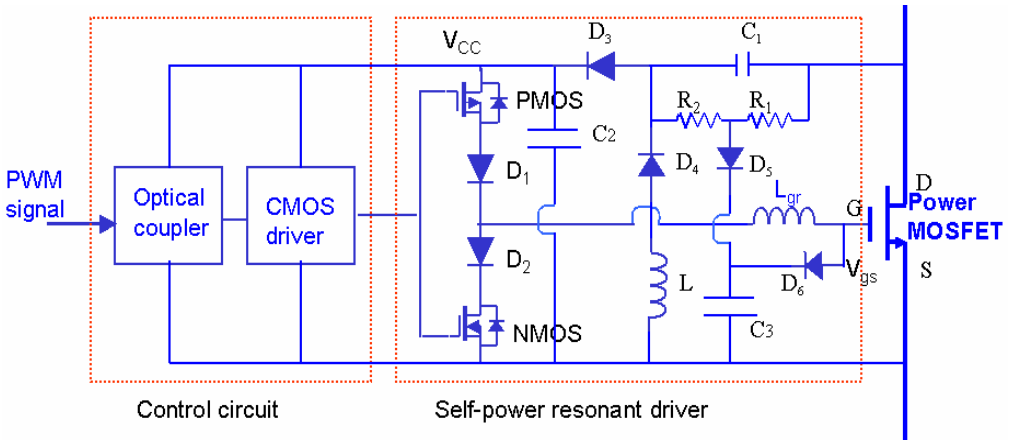
Fig. 4-16 Conventional gate driver for power MOSFET module

For a conventional gate driver, the most important power losses include the gate resistor power loss and the switching loss associated with the common drain drive MOSFETs [4-13]-[4-16]. The gate resistor loss accounts for more than two-third of the total gate driver loss. The drive MOSFET switching loss is determined by the drive MOSFET input and output capacitance. The conventional square-wave driving scheme to drive the MOSFET suffers from large gate drive loss. The main advantage is that the gate drive circuit is universal.

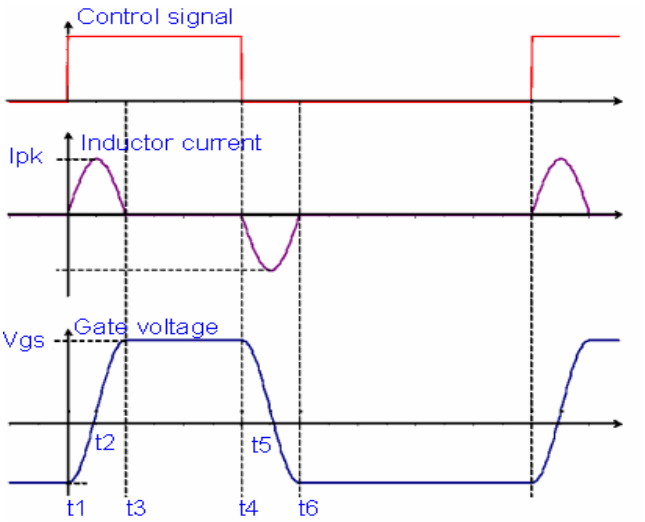
As a result, a resonant gate driving technique is applied to reduce the gate driving losses [4-13]. It is natural to use a resonant circuit to accomplish this task. Energy is circulating between the gate resonant inductor and capacitor. To improve the gate drive efficiency, energy stored in the input gate capacitance has to be recovered. Therefore, energy in the resonant tank is circulated every switching cycle, instead of being dissipated by the gate driver itself as in the conventional square-wave drive scheme. This promising feature makes the resonant gate driver operate very efficiently. Several resonant gate driver circuits have been reported [4-17]-[4-22], which, to some extent saves the power or the requirement for special applications. The proposed gate driver in this chapter features further reduced power loss, self-power function, thus achieve smaller gate driver size and high power device drive application.

4.5.1 Principle and Operation of the Self-power Resonant Gate Driver

The designed new high frequency self-power resonant gate driver schematic is shown in Fig. 4-17 (a). The control part has an optocoupler for high voltage isolation and integrated power MOSFET gate driver for the complementary power MOSFETs. The power stage is a self-power resonant circuit, consisting of the complementary P-channel and N-channel power MOSFETs, resonant gate inductor, and self-power unit. The operation of the circuit can be better explained through two parts, the resonant gate driver and the self-power unit.



(a) Circuit schematic



(b)

Fig. 4-17 High frequency self-power resonant gate driver schematic and resonant gate voltage ideal waveforms

4.5.2 Analysis of the Resonant Gate Driver

The ideal waveforms of the resonant gate driver are shown in Fig. 4-17 (b). During turn-on, the gate inductor and the input equivalent capacitor of the power MOSFET are series resonant under the gate driver bus voltage V_{cc}. At the beginning, both the P-MOSFET and N-MOSFET are off. Then at time t_1, PMOS is turned on and a voltage step appears at the conjunction node of PMOS and D_1. Responding to this step stimulus, the inductor current and the capacitor voltage both start to rise, until at time t_2 the inductor

current rises up to I_{pk}. Then the inductor current freewheels and continues to charge the input capacitor until the current goes down to zero and the capacitor voltage goes up to the maximum value. At this time t_3, the diode D_1 blocks the voltage and current reverses direction. If the diode D_1 forward voltage drop is neglected and the quality factor Q of the series resonant circuit is high enough, then the rise time t_r and positive peak current I_{pk_p} can be estimated as,

$$t_r = t_3 - t_1 = \frac{\pi}{\omega_o} = \pi\sqrt{L_{gr}C_i} \tag{4-6}$$

$$I_{pk\_p} = \frac{V_{cc}}{Z_o} = V_{cc}\sqrt{\frac{C_i}{L_{gr}}} \tag{4-7}$$

where, C_i is the equivalent gate capacitance of the power MOSFET module, Z_o is the characteristic impedance of the series resonant circuit, and ω_o is the resonant frequency.

Similar circuit operation is designed for the turn-off transition. During turn-off, the gate inductor and the input equivalent capacitor of the power MOSFET are parallel resonant under the gate voltage V_{gs}, which is different from the turn-on transient. At time t_4, PMOS turns off and NMOS turns on, the resonant occurs and the capacitive energy is transferred to the inductor L_{gr}. The inductor current increases and the capacitor voltage drops until at time t_5 when V_{gs} reaches zero and inductor current rises up to negative peak value. Because of the linear capacitor assumption, the falling time and the negative valley current can be expressed in equation (4-8) and (4-9). Then the inductor current freewheels and continues to discharge the input capacitor until the current goes down to zero and the capacitor voltage reaches the negative maximum value. At this time t_6, the diode D_2 blocks the voltage and current reverses flow. Such symmetry resembles that of a conventional gate driver. Similarly, if neglect the diode D_2 forward voltage drops and the quality factor Q of the parallel resonant circuit is high enough, the fall time t_f, negative peak current I_{pk_n} and negative maximum voltage V_{gs_min} can be estimated as in equation (4-8) ~ (4-9),

$$t_f = t_6 - t_4 = \frac{\pi}{\omega_o} = \pi\sqrt{L_{gr}C_i} \tag{4-8}$$

$$I_{pk\_n} = V_{gs\_\max}\sqrt{\frac{C_i}{L_{gr}}} \tag{4-9a}$$

$$V_{gs\_\min} = -V_{gs\_\max} \tag{4-9b}$$

where, V_{gs_max} is the positive maximum value.

The basic principle of the resonant gate driver is explained above in terms of voltages and currents during one switching cycle. Further analysis should be conducted to better understand the power loss effects on the resonant inductor current and input capacitor voltage under the continuous switching cycles. From time t_1 to t_3 the energy is transferred from the voltage sink C_2 to the resonant inductor and the gate capacitor C_i. The subsequent stage freewheels the inductor energy, which is finally transferred to the gate capacitor. From time t_4 to t_6 energy is circulated between the gate capacitor and inductor. The gate capacitor voltage reverses by this process. Because there is no energy recovery during one switching cycle, the energy transferred from the voltage sink must balance the gate driver power loss to achieve the stable gate voltage waveform. Also because of the small power loss, the Fig. 4-17 circuit consumes less power than a conventional gate driver. This can be seen through the detailed calculations below.

According to the series resonant circuit theory, during turn-on transient the power MOSFET module gate voltage V_{gs} and resonant inductor current i_{Lgr} can be expressed as in equation (4-10) and (4-11).

$$V_{gs}(t) = \frac{[V_{gs\min} - (V_{cc} - V_F)]\omega_o}{\omega} e^{-\delta t}\sin(\omega t + \beta) + V_{cc} - V_F \tag{4-10}$$

$$i_{Lgr}(t) = \frac{(V_{cc} - V_F - V_{gs\min})}{\sqrt{\frac{L_{gr}}{C_i} - \frac{R_g^2}{4}}} e^{-\delta t}\sin(\omega t) \tag{4-11}$$

where, $\omega = \sqrt{\frac{1}{L_{gr}C_i} - (\frac{R_g}{2L_{gr}})^2}$, $\delta = \frac{R_g}{2L_{gr}}$, $\omega_o = \sqrt{\delta^2 + \omega^2}$, $\beta = tg^{-1}\frac{\omega}{\delta}$, R_g is the total gate resistance including PMOS on-resistance, L_{gr} parasitic resistance, power MOSFET module gate resistance and package/layout resistance.

Similarly, during the turn-off period, the input capacitance parallel resonates with the inductor. The gate voltage V_{gs} and resonant inductor current i_{Lgr} can be expressed as in equation (4-12) and (4-13). The calculated gate voltage V_{gs} and resonant current i_{Lgr} curves are shown in Fig. 4-18 in one switching cycle during steady state, which are consistent with the experimental results.

$$V_{gs}(t) = \frac{V_{gs\max}\omega_o}{\omega} e^{-\delta t} \sin(\omega t + \beta) \tag{4-12}$$

$$i_{Lgr}(t) = -\frac{V_{gs\max}}{\sqrt{\frac{L_{gr}}{C_i} - \frac{R_g^2}{4}}} e^{-\delta t} \sin(\omega t) \tag{4-13}$$

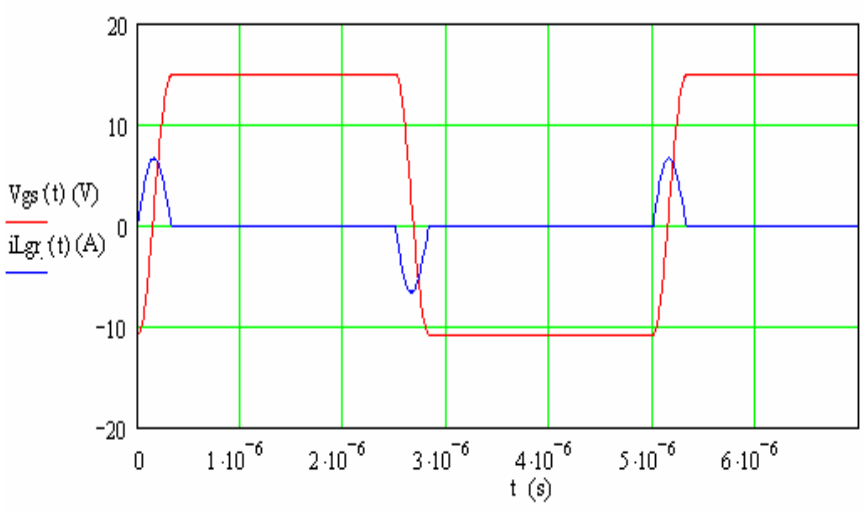


Fig. 4-18 Calculated gate voltage V_{gs} and resonant inductor current i_{Lgr} curves

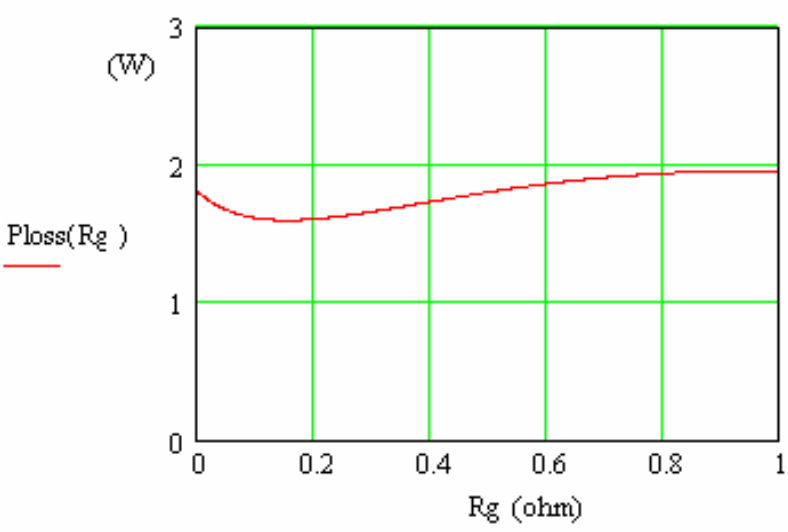


Fig. 4-19 Gate driver power loss as a function of gate resistance

4.5.3 Gate Driver Power Loss Analysis

The resonant gate driver charges and discharges the power MOSFET module gate capacitance. The power loss will be generated on the equivalent resistance and diode forward drop. During turn-on transient, the power loss is calculated in equation (4-14). During turn-off transient, the input capacitance energy is recovered through the resonant inductor. Overall, the power loss is a small portion of the total power needed to drive the power MOSFET module compared to the conventional gate driver.

$$P_{loss\_on} = \int_{t_1}^{t_3} (R_g i_{Lgr}^2 + V_F i_{Lgr}) dt \approx (\frac{R_g}{R_g + Z_o} + \frac{V_F}{V_{cc} + V_F}) \frac{1}{2} C_i (V_{gs\max} - V_{gs\min})^2 f_s \quad (4\text{-}14)$$

$$P_{loss\_off} = \frac{1}{2} C_i (V_{gs\max}^2 - V_{gs\min}^2) f_s \quad (4\text{-}15)$$

The total gate driver power loss is plotted as a function of gate resistance shown in Fig. 4-19. When the R_g is zero, the diode forward voltage drop causes the power loss. When the gate resistor value increases, the power loss decreases and then increases. This results in a minimum power loss for a certain gate resistor value. This is caused by the nonlinear

relationship between the gate bus voltage and the resistance to keep the driver output voltage at a constant value discussed below.

The driver output voltage has to be stable under different power losses caused by the equivalent gate resistance. The required driver bus voltage is calculated as a function of a gate resistance shown in Fig. 4-20. To keep the driver output voltage V_{gs_max} at 15V, a higher bus voltage V_{cc} is needed to compensate the increased gate driver power loss. Also, when the gate resistance increases, the minimum output voltage V_{gs_min} is reduced during the turn off transient.

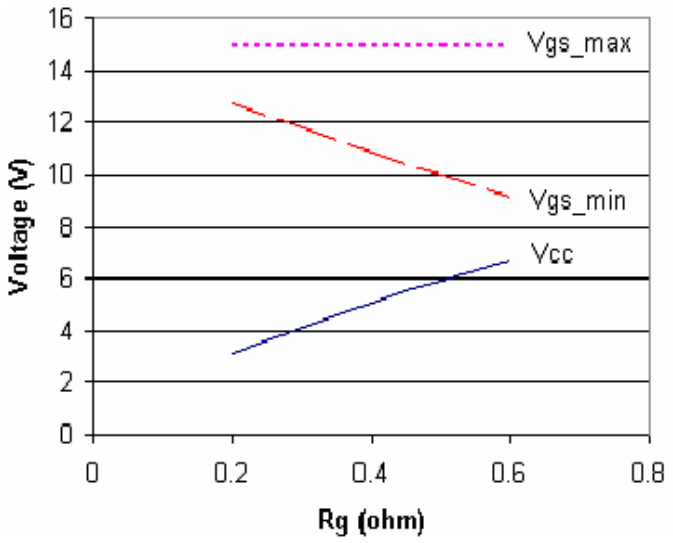


Fig. 4-20 Gate driver bus voltage V_{cc}, output voltage V_{gs} VS gate resistance R_g

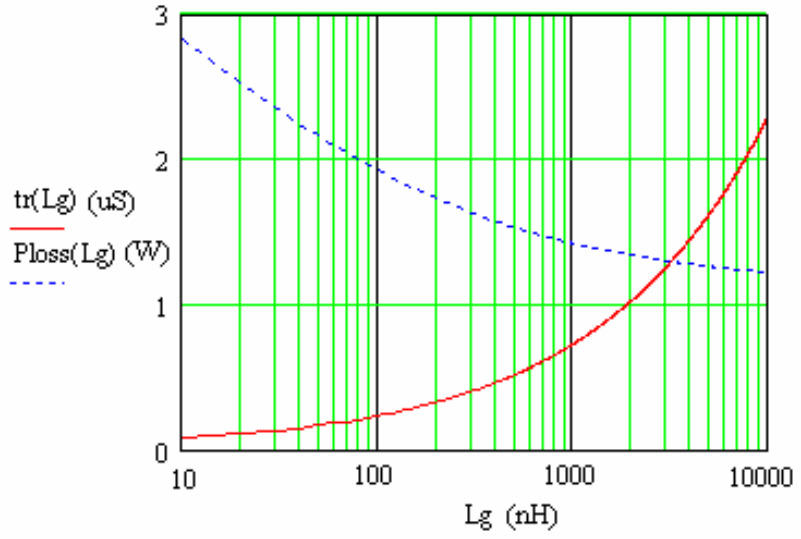


Fig. 4-21 Design tradeoff between switching transient and power dissipation based on resonant inductance value

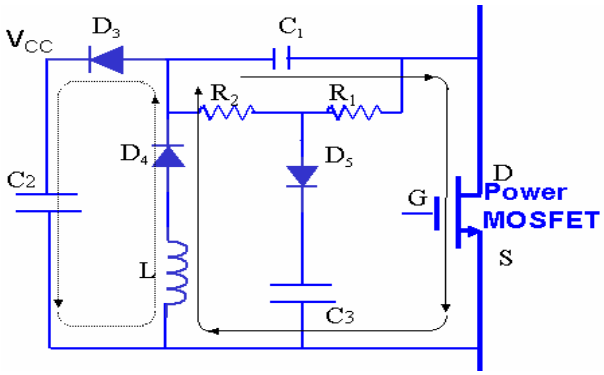
For a given power MOSFET, the gate drive speed is mainly determined by the resonant inductance. A smaller inductance produces a faster transition time shown in equation (4-6) and (4-9), but at the cost of a higher power loss in equation (4-14). A fundamental design tradeoff thus exists in determining the optimal value. For many high frequency applications, the MOSFET rise/fall time is often specified with a maximum value. Under such conditions, the selection of resonant inductance will have to be calculated according to equations (4-6) and (4-9). Fig. 4-21 depicts the conflicting relationship between the gate drive switching transient and the power loss under the conditions of R_g=0.4Ω, f_s=200 kHz and Q_g=900 nC for the power MOSFET module.

4.5.4 Analysis of the Self-power Unit

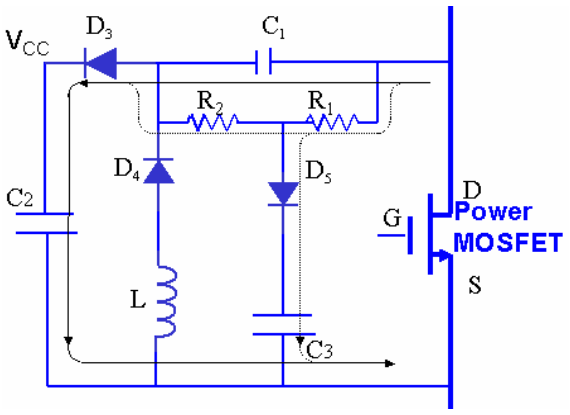
In order to shrink the power supply size for the gate driver, a self-power unit is developed which enables the gate drive power to be derived directly from the main DC bus. This does not need the additional driver power supply. The self-power approach has been reported thus far to application in high voltage power device series connection [4-23]. Further improved function with clamped gate voltage is developed and analyzed in this section.

The proposed self-power circuit in Fig. 4-17 (a) can be shown in **Fig. 4-22**. It consists of high voltage capacitor C_1, low voltage source bank C_2, clamp capacitor C_3, auxiliary

resistor R_1, R_2, and inductor L. During the normal off-state, capacitance C_1 withstands most of the bus voltage. Capacitance C_2 is like a voltage source bank. The bus voltage charges capacitor C_2 through the auxiliary resistor R_1 and R_2. The drive unit gets power from capacitor C_2. When the power MOSFET turns on, the high voltage of capacitor C_1 is applied across the inductor L. The inductor L current increases. The energy of C_1 is then transferred into inductor L. After the inductor current reaches its peak value, it then decreases, and charges capacitor C_2. The capacitor C_3 cannot be charged during this process due to the block diode D_5. This process can be better understood with detail theory analysis. The calculated self-power unit voltage, current curves during one switching cycle are shown in Fig. 4-23. When the power MOSFET turns off, the drain-to-source voltage increases and charges capacitor C_1 to the power MOSFET's bus voltage. The capacitor C_2 is also charged by the current of capacitor C_1. There is also little current flowing through the auxiliary resistor R_1 and R_2 to the capacitor C_2. The capacitor C_3 is also charged through R_1. C_3 is used to clamp the gate voltage, which may be high and caused by the unstable driver bus voltage V_{cc} , as discussed the previous section. So the power MOSFET's drive circuit can get continuous energy during the switching transients. The high voltage capacitor C_1 value is very small. The additional power loss of the power MOSFET caused by the capacitor C_1's energy transfer is negligible. The self-power unit's efficiency is high because no high power loss component is included during the energy transfer period.



(a) Turn-on transient



(b) Turn-off transient

Fig. 4-22 Self-power unit for the resonant gate driver

The self-power circuit has to transfer the energy to the gate driver to compensate the power loss. The gate driver power increases almost linearly with the switching frequency and the self-power unit has a similar situation for a certain bus voltage. The relationship between them needs to be analyzed to properly design the self-powered unit. Assuming the gate driver bus voltage is V_{c2}, the power loss P_{loss_p} and efficiency η of the self-power unit can be calculated in equation (4-16) - (4-18) with the switching frequency f_s. In the steady state operation, the self-power unit balances the gate driver power loss in equation (4-19). The P_{static} is static power to bias the gate driver chip. From equation (4-19) the relationship between self-power high voltage capacitor C_1 and device input capacitor C_i is plotted as an example for V_{ds}=100 V and f_s=200 kHz in **Fig. 4-24**. For the power MOSFET module with increased input capacitance, a larger high voltage capacitor C_1 is needed to transfer the energy for the gate driver.

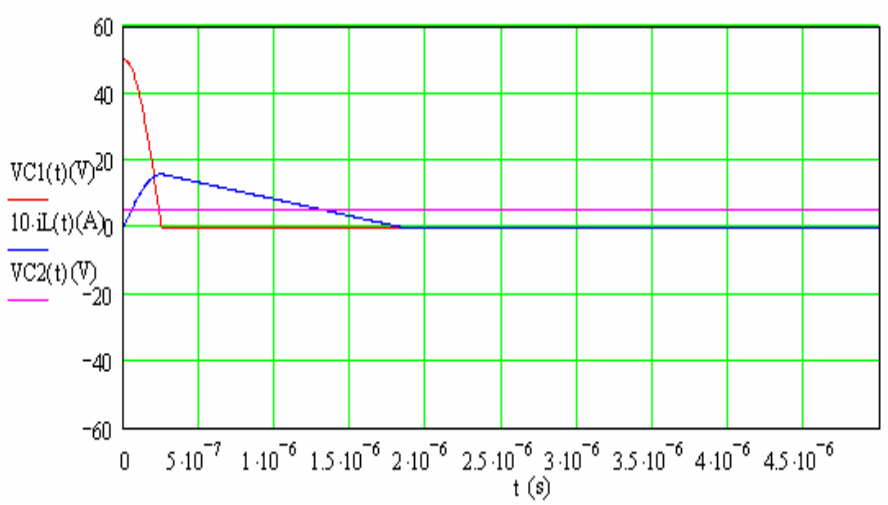


Fig. 4-23 Calculated self-power unit voltage V_{c1}, V_{c2}, current i_L waveforms during one switching cycle

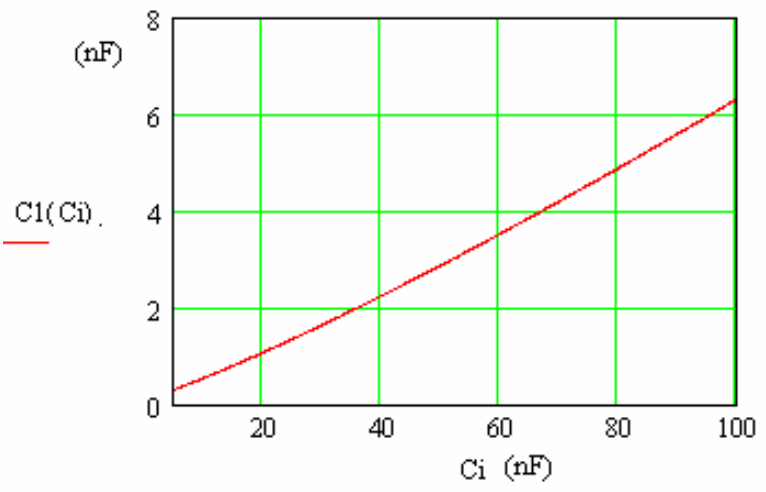


Fig. 4-24 Relationship between self-power high voltage capacitor C_1 and power MOSFET input capacitor C_i

$$P_{loss\_p} = \{[V_F \frac{i_L}{2} + R_L(\frac{i_L}{2})^2]t_c + [2V_F \frac{i_L}{2} + R_L(\frac{i_L}{2})^2]t_f + \frac{1}{2}C_1(V_{DS} - V_{c2})V_F\}f_s \quad (4\text{-}16)$$

$$P_t = [\frac{1}{2}C_1(V_{DS} - V_{c2})^2 + \frac{1}{2}C_1(V_{DS} - V_{c2})V_{c2}]f_s \tag{4-17}$$

$$\eta = 1 - P_{loss\_p} / P_t \tag{4-18}$$

$$P_t\eta = P_{loss\_on} + P_{loss\_off} + P_{static} \tag{4-19}$$

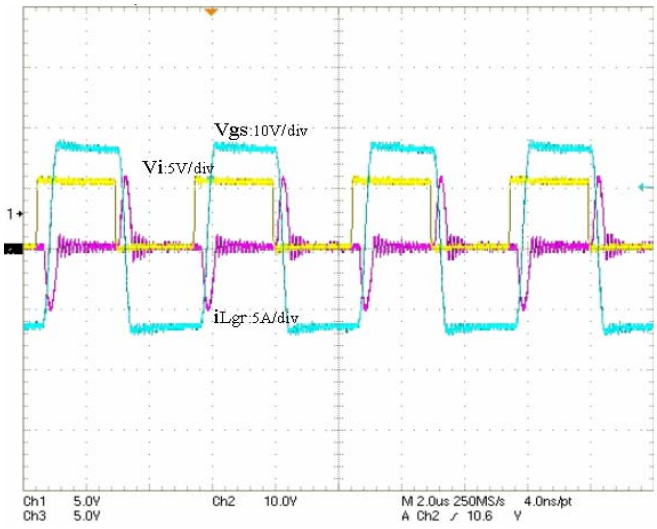
where, V_f is the diode forward voltage drop, R_L is equivalent resistance of the inductor L.

4.5.5 Experimental Verifications

In order to validate the proposed self-power resonant gate driving circuits, the hardware prototype is built and tested, as shown in Fig. 4-25. A small iron toroidal core is used for the resonant inductor with about 200 nH. The self-power inductor has an inductance of 5uH with equivalent resistance 160 mΩ. The power PMOS and NMOS with small gate charge and low R_{dson} are selected. Schottky diodes are used in the circuit for fast reverse recovery. The power MOSFET module gate capacitance is about 60 nF. To test the driver circuit and the self-power unit, a resistive load continuous mode operation is conducted under different bus voltages.

Fig. 4-25 shows the test waveforms in the 200 kHz switching frequency case. The curve V_i is the input signal to the gate driver. The output gate voltage varies from –12V to 15V while the driver bus voltage is 5V. During turn-on/off transient, the gate inductor resonates with the gate capacitance and transfers the energy to the power MOSFET gate side. The inductor peak current is about 5A, close to what can be calculated from equation (4-11).

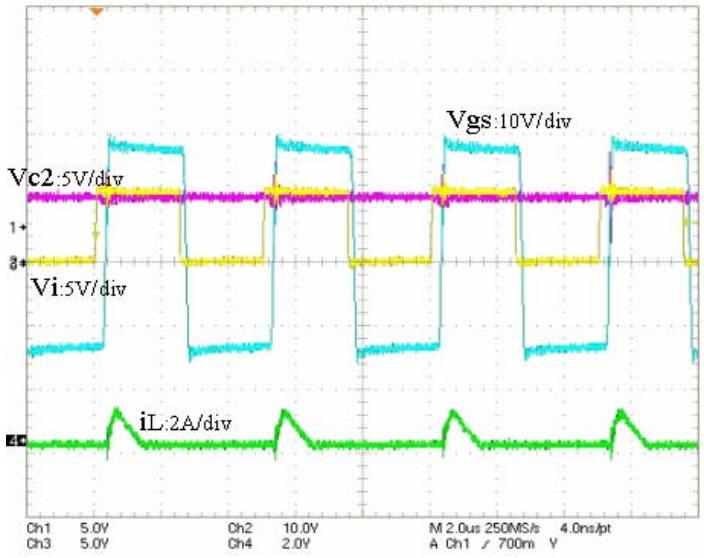
(a) Self-powered resonant gate driver prototype



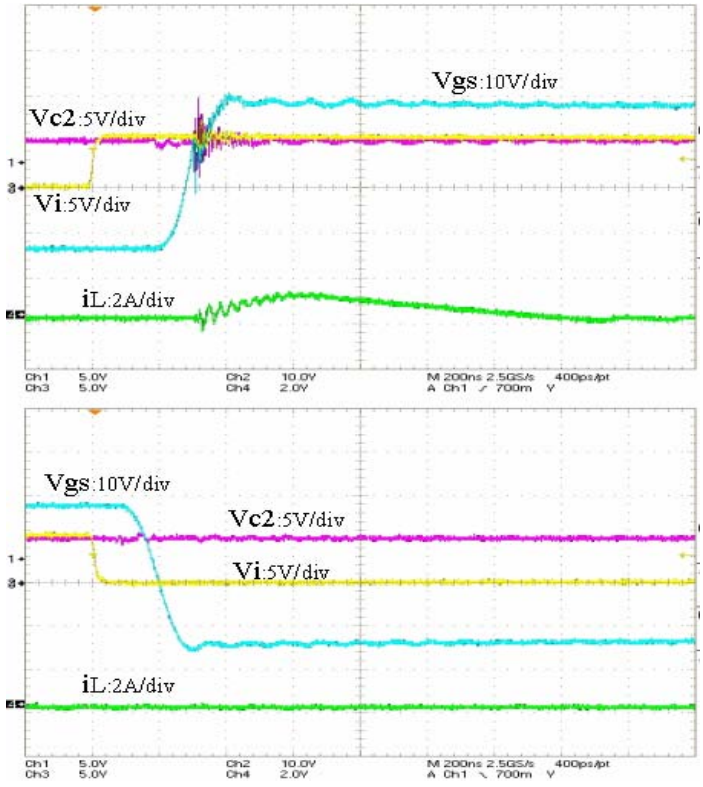
(b) Gate driver output voltage V_{gs} and resonant inductor current i_{Lgr} at 200 kHz

Fig. 4-25 Self-power resonant gate driver prototype and tested waveforms

The test waveforms for the self-power unit show a constant driver bus voltage V_{c2} requirement for the resonant gate driver operation in **Fig. 4-26** (a). The self-power inductor resonates with the high voltage capacitor C_1. The inductor current decreases linearly by the applied driver bus voltage V_{c2}. Through this mechanism the gate driver can get continuous energy from the self-power unit. **Fig. 4-26** (b) shows the detailed switching transients. During turn-on some noises occur caused by the parasitic inductance. The turn-off waveforms are clean because the gate capacitor discharges only through the resonant inductor to achieve the negative voltage.



(a) Self-power unit inductor current i_L and gate driver bus voltage V_{c2}



(b) Turn-on/off transient in (a)

Fig. 4-26 Self-power unit inductor current i_L and gate driver bus voltage V_{c2} at 200 kHz

To compare the efficiency of the proposed self-power resonant gate driver, three different gate driver hardware prototypes are built and tested to drive the same power

MOSFET module. Fig. 4-27 shows the efficiencies comparison for the three gate drivers between the proposed self-power resonant gate driver, and the conventional gate drivers under 200 kHz switching frequency. In the conducted experiments, a total loss of 24W was measured for the conventional resistive gate driver and gate driver power supply. The second resonant gate driver consumes an 11W power loss, because during turn-on the resonant inductor current freewheels through the diode D_1 thus causing a larger portion of power to dissipate. The self-power resonant gate driver consumes about 2W; where more power is saved due to the low driver bus voltage and energy recovery. This low power loss enables the self-power unit to function in driving the high power MOSFET modules and further reduces the power unit size.

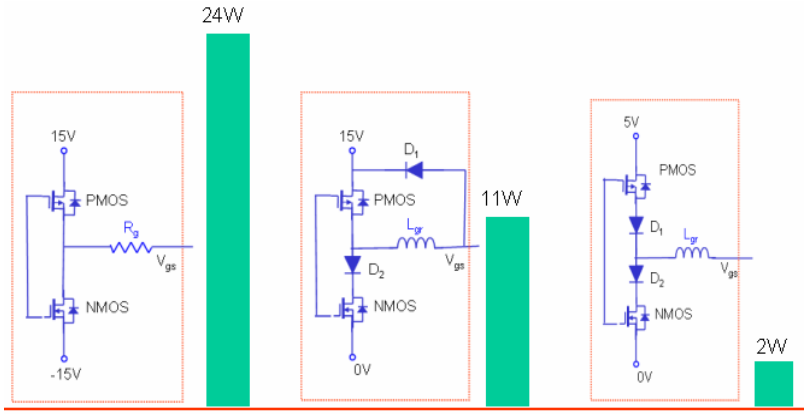


Fig. 4-27 Gate driver power loss comparisons for power MOSFET module

4.6 Power MOSFETs Parallel Operation Effects on Power Density

To improve the power density, the high frequency operation is desirable to reduce the passive components size. The power MOSFET parallel operation is selected as the main switch to meet the switching current requirement. To see the benefits of the power MOSFET parallel operation, the power densities for the designed three-level parallel resonant converter are compared to that of IGBT as the main switch. The IGBT (CM300DY-12NF) is selected according to the power density figure of merit in chapter

2. This single IGBT module has the same voltage rating as the power MOSFETs in parallel and can meet the current requirement.

The power loss of the selected IGBT is measured and calculated at different junction temperatures. The thermal stability graph is shown in Fig. 4-28. It can be derived that the maximum switching frequency is about 60 kHz and the maximum junction temperature is about 150^0C, both of them are below those of three power MOSFETs parallel operation. The thermal stability of the three power MOSFET in parallel has been developed in chapter 3, which is also shown in Fig. 4-30. It can be inferred that the maximum switching frequency is about 800 kHz and the maximum junction temperature is about 200^0C, which are much higher than those of IGBT. Therefore the power density improvement is expected. Compared to that of IGBT as the main switch, the benefits for power MOSFET in parallel to the power converter are,

- Switching frequency increase from 60kHz to 800kHz
- Device volume reduction by 88%
- Passive value (L, C) decrease by about 13 times
- Heat sink area decrease by 30%

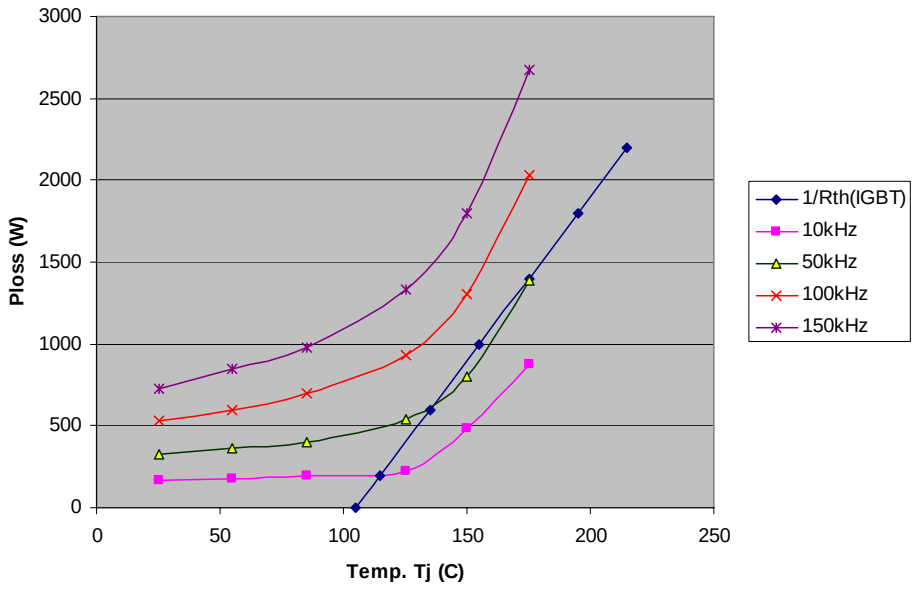


Fig. 4-28 A high power density IGBT (CM300DY-12NF) thermal stability graph

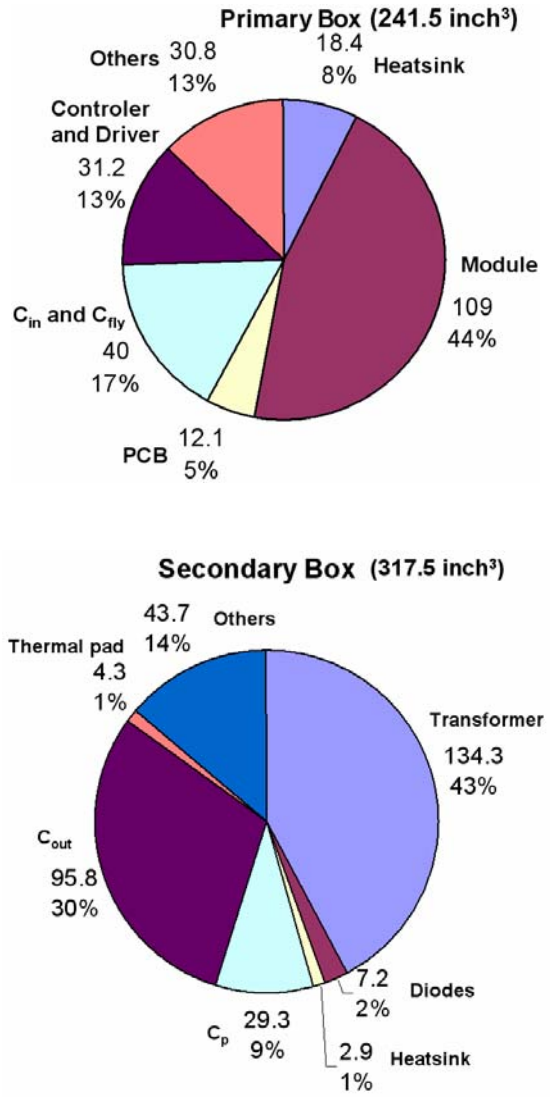


Fig. 4-29 Power density graph with IGBT as the main switch for pulse power high temperature operation (Power density: primary side: 124 W/inch^3, secondary side: 95 W/inch^3, whole converter: 54 W/inch^3)

The power density is calculated for the selected IGBT as the main switch and shown in Fig. 4-29. The components volume breakdown and according percentage of the total volume are also in the pie graph. Due to the big dimension and low frequency operation of the selected IGBT, the passive components occupy higher percent volume compared to that of power MOSFET in parallel as the main switch. The power densities comparisons are conducted and shown in Table 2-7 for power MOSFET and IGBT as the main switch. The number of power devices in parallel and their junction temperature are also shown in

Table 2-7, which are determined by the power converter system requirement. Their switching frequencies are limited by the device high temperature operation thermal stability. From the estimated power densities, it is concluded that the power density has two times improvement for the power MOSFET. The power MOSFET in parallel as the main switch has the potential to improve the system power density due to the low loss, high switching frequency operation.

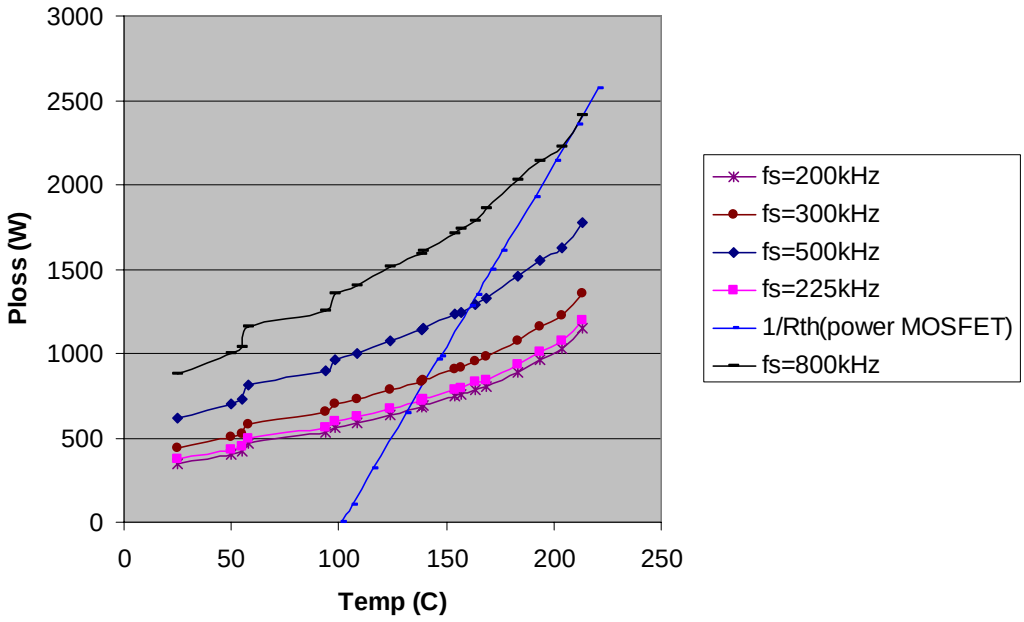


Fig. 4-30 Three power MOSFETs in parallel thermal stabilities for pulse power operation

Table 4-3 Comparisons of the three-level PRC power converter performance with different switching power devices

	Power MOSFET #1 APT60M75L2LL	IGBT CM300DY-12NF
Number of device in parallel / current (A)	3 / 219	1 / 300
Junction temperature (^{0}C)	200	150
Switching frequency (kHz)	800	60
Primary side (W/inch^3)	321	124
Whole converter (W/inch^3)	175	54

4.7 Summary

In high power high density converters, power MOSFETs need to be used in parallel as the main switch to meet the current rating requirement, increase the switching frequency, and minimize the power loss. This chapter analyzed the current sharing issues during conduction states and switching transients. Differential conduction resistance can cause current unbalance and are limited due to the positive temperature coefficient of the MOSFET resistance. The conduction power losses change with the resistance unbalance and are limited by the temperature effects and the number of MOSFETs in parallel.

During the switching transients, the transconductance differentials and threshold voltages result in limited current unbalance. Miller capacitances will affect the time required for the drain-to-source voltage to collapse across other parallel devices. The drain and source parasitic inductance has effects on the turn-on/off current sharing. A current sharing control approach from the gate driving side is developed. The experimental results indicate that the power MOSFETs can be paralleled with the proper gate driving design even if the device parameters are mismatched, and consequently the switching losses are significantly reduced. This is very useful for the switching loss dominated high power, high density converter design.

A novel self-power resonant gate driver for high power MOSFET modules is proposed and developed in this chapter. Compared with existing gate drivers, the new topology has several characteristics including reduced gate drive loss, self-power from the bus, high frequency application and easy implementation with a wide range of power MOSFET/IGBT modules. A conventional gate driver dissipates all the driving energy, while the proposed circuit has the low driver bus voltage and high energy recovery. Further power savings can be achieved by using low voltage drop diodes and low equivalent gate resistance, thus reducing the driver and self-power unit size. Its power consumption, self-power function and very high operating frequency will make it an attractive solution for many demanding high power gate drive applications.

To identify the benefits of power MOSFET parallel operation on the power density, it is compared to the same voltage rating IGBT device as the main switch. The power MOSFET has lower power loss and better thermal handling capability, thus can switch at

higher frequency. The comparison results show that the power density has two times improvement for the power MOSFET in the three-level parallel resonant converter. The power MOSFET in parallel as the main switch has the potential to improve the system power density due to the low loss, high switching frequency operation.

Chapter 5 Development of a Scalable Power Semiconductor Switch

5.1 Introduction

The advancement of power semiconductor switches is the main driving force behind the rapid development of power electronics technology. High switching frequency and high voltage are often desirable for the performance, cost, and size benefit of a system. For example, a high switching frequency can lead to smaller passives components – inductors, capacitors, and transformers; a high voltage can lead to lower current for a given power converter, thus allowing for lower copper losses or smaller wires. In addition, the dynamic performance can be improved with increased control bandwidth, which is directly related to the switching frequency. In industrial medium- and high-power (hundreds of kWs to MWs), and medium- and high-voltage (>2kV) converter applications, state-of-the-art semiconductor switching devices are high-voltage Insulated Gate Bipolar Transistors (IGBT) and hard-driven Gate-Turn-off (GTO) thyristors such as Integrated Gate Commutated Thyristors (IGCT) and Emitter Turn-off Thyristors (ETO). High voltage IGBT, IGCT and ETO have significantly improved switching performance over the conventional GTO, but their switching frequency is still limited to 1-2 kHz [5-2]-[5-9].

Fig. 5-1 compares several types of state-of-the-art high power high voltage semiconductor device technologies. All these power semiconductor switches are silicon based devices with limited switching capabilities. Among them, high voltage IGBTs have the best switching characteristics but their maximum switching frequency is still below 2kHz. Further improvement on their switching capability is fundamentally limited by the high switching loss of a bipolar device with a thick voltage supporting layer.

A more drastic future solution to this problem is to develop power switches based on a unipolar current conduction mechanism with sufficient voltage and power handling capability. A promising future solution would be a Silicon Carbide (SiC) power MOSFET. At present, the SiC power MOSFET, even with very low current rating (less

than a few amperes), is still in a developmental stage. Many technical and other barriers must be overcome before SiC MOSFETs can become available. These barriers include device materials, processing, packaging, reliability, and cost.

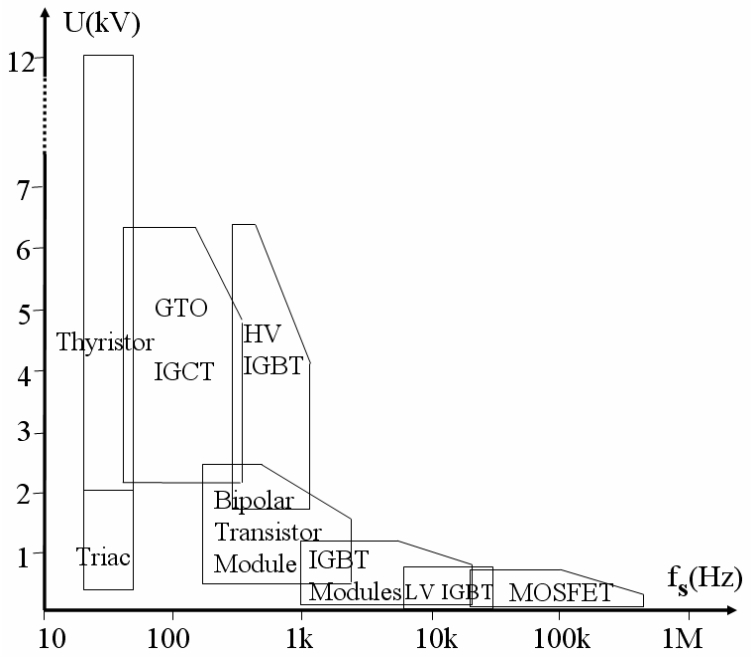


Fig. 5-1 State-of-the-art high power semiconductor device technologies

Another viable solution to achieve better switching performance in high voltage and high power applications is to use lower voltage silicon devices as building blocks for higher voltages [5-10]-[5-16]. The low voltage silicon devices have an excellent thermal handling capability and low switching losses, and therefore, better switching capability. For example, low voltage (<2kV) high current IGBTs can operate at a switching frequency of tens of kHz, much higher than that of a high voltage IGBT. The voltage ratings of the low voltage IGBTs cannot meet the requirement for many high voltage applications, while several of them could be series-connected for higher voltages. This concept is the basis of the Scalable Power Semiconductor Switch (SPSS) proposed in this chapter. The Scalable Power Semiconductor Switch (SPSS) uses a number of series-connected lower voltage IGBTs as the basic element. This allows scalability of the voltage rating. The current capability can remain the same as the IGBT used. The switching frequency capability is determined by the IGBT class used in the SPSS. The

scalability of the switching frequency and current is achieved by using IGBTs with different frequency and current capabilities.

There are other desired features for the proposed SPSS. It should be more than just a simple device series connection. In addition to the scalability, from a user's standpoint, SPSS should behave as a single switching device module with three terminals, and the internal device series connection should be of no concern to users.

This chapter presents the development of a SPSS based on series-connected low voltage high frequency IGBTs to achieve higher voltage ratings while preserving high switching frequency capability. The voltage balancing and IGBT tail current control techniques developed and used are discussed first. Then, the schemes on gate driving, communication, power supply, and packaging are described. Finally, SPSS prototyping and experimental results are presented. The results show that all design specs for SPSS are fully met and the SPSS is a viable concept to achieving high voltage, high power, and high frequency switching capability.

5.2 IGBT Series Connection Voltage Balancing Techniques Review

One key issue in the development of the proposed SPSS is to ensure static and dynamic voltage sharing across the series-connected IGBTs. Static balancing can be achieved relatively easily by connecting of resistors with a high resistance in parallel with each switch. Dynamic voltage sharing is more difficult to achieve. The methods reported thus far for dynamic voltage balancing can be divided into two groups: one concentrates on the power device side (collector to emitter), and the other on the gate side [5-17]-[5-29].

On the power device side, a passive snubber network across each IGBT device, a voltage clamping circuit, or a resonant tank over each device, etc., was often used in previous investigations. Usually a traditional RCD snubber circuit is parallel to the main device to clamp the over voltage shown in Fig. 5-2. The passive snubber components are exposed to high voltages and currents, resulting in high rating, large size, and high cost [5-17]. Sometimes a Zener voltage clamp circuit is added between the high voltage drain side and gate side in Fig. 5-3 [5-18]. The benefit of this approach is to have a small current feedback into the gate side when an overvoltage across the main switch exceeds

the Zener diode voltage. This approach is, to some extent, similar to the active gate control. However the Zener diode can only clamp the overvoltage at a certain level. When the overvoltage is lower than the Zener diode clamp voltage, the active gate control is not in effect. Also the high voltage Zener is not easily available.

To further improve the snubber circuit function, the active voltage clamp circuit is developed for a series-IGBT voltage balance in Fig. 5-4 [5-19]. A two voltage level clamp circuit is built with the small power rating IGBT in series. Each IGBT works like a voltage control current source. The Zener diode senses the overvoltage across the main switch. When a low over voltage occurs, the bottom Zener diode breakdowns first and the bottom IGBT conducts to clamp the voltage at the Zener diode rating voltage level. When an even higher over voltage occurs, both Zener diodes breakdown and clamp the voltage at the total rating voltage. The capacitor in parallel works like a RCD snubber. The Zener and IGBT, which are paralleling with the capacitor, clamp the capacitor voltage to a certain level. The voltage clamping circuit needs additional devices to clamp the main IGBT terminal voltage, which makes the circuit bulky [5-17]-[5-18]. This kind of clamp circuit has decreased power loss. However a high voltage Zener diode is not easily available and can clamp the voltage to a certain level.

Resonant techniques such as series or auxiliary clamping were also employed and generally are complex to build and control. In [5-15], it shows that the voltage falling can be controlled by a central auxiliary circuit, which guarantees a uniform turn-off transient for all on devices. However, different device characteristics during the off-state will cause an unbalanced steady state voltage distribution. Thus, an additional device side snubber or gate side control is still required. This certainly adds to circuit complexity and requires control over the medium voltage range [5-17].

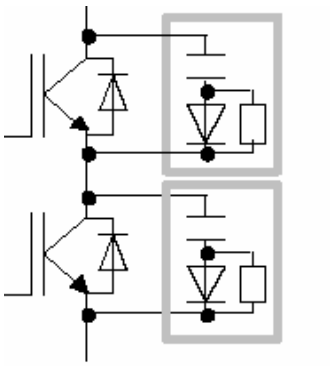


Fig. 5-2 Passive snubber circuit for series-IGBTs voltage balance [5-17]

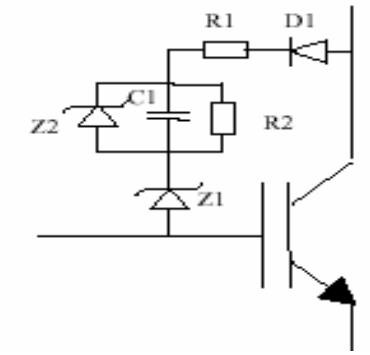


Fig. 5-3 Zener voltage clamp circuit for series-IGBTs voltage balance [5-18]

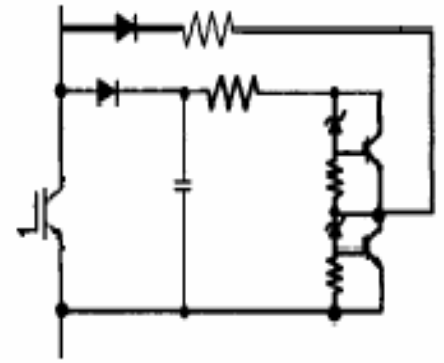


Fig. 5-4 Active voltage clamp circuit for series-IGBTs voltage balance [5-19]

The basis for gate-side control relies on the fact that an IGBT's switching transition rate can be manipulated by the amount of injected gate current during its voltage rise or fall phase due to the existence of a large Miller capacitance in the IGBT. This approach is used by some researchers and gate driver manufacturers [5-20]-[5-27]. A number of

papers discuss how to utilize current pulses for multiple control functions, such as slope manipulation, di/dt control during turn-on, and dv/dt control during turn-off [5-28]-[5-32]. By adjusting the gate current magnitude and direction, it is possible to control the transient slopes within the Miller period. This can be accomplished by control feedback circuitry where multiple stages, such as operational amplifiers and driving transistors, are employed. Undoubtedly they all introduce delays. These delays will become worse for higher power IGBT device drivers, and could even be so long as to cause the entire control system to start oscillation as observed in some previous work.

One of the active gate control approaches is to feedback the over voltage generated current through a capacitor to the gate side when over voltage occurs. The corresponding circuit is drawn in Fig. 5-5 [5-21]. The RC network functions as a voltage divider. The overvoltage is monitored by the top high voltage small value capacitor. The bottom capacitor has a big value and keeps almost constant voltage, like a voltage source. When the overvoltage occurs across the main switch, the top capacitor senses the overvoltage and sends a current feedback to the gate side, which slows down the IGBT turn-on speed. The overvoltage can be reduced accordingly. However, when the bus voltage changes abruptly, the top capacitor may feedback a strong current to the gate side, which will turn on the IGBT, even if the gate driver is in the off-state. The abrupt increase of DC-link voltage can result in undesirable turn on. This is the main disadvantage of this over voltage control approach.

Another voltage balance technique is the reference ramp voltage approach shown in Fig. 5-6 [5-22]. Each IGBT's collector-to-emitter voltage rise slope is pre-designed to allow the voltage rise following the reference ramp during turn-off transient. To sense the high voltage across the IGBT the voltage divider circuit is still needed to feedback to the low voltage analog circuits input side. The high speed, high sensitivity and fast time response analog circuitry are required to sense the high overvoltage and compare to the ramp reference.

Gate-signal delay adjustment is another kind of approach used so that IGBT devices of different speeds within the series connection will have different slopes, which can be viewed as having different delay times [5-23]-[5-24]. This approach is attractive because the common difference among conventional gate drivers is also the gate delay time. Thus

turn-on and turn-off transients can be balanced by their respective delays, while the steady-state voltage balance can be controlled by adjusting the magnitude of the applied gate voltages. The delay controller can accumulate knowledge of terminal voltage for each device. By adjusting times to turn on and turn off each device, their terminal voltages can be balanced during both the switching and steady state. Those schemes using active principles, such as "smart" computation of delay or dv/dt control using feedback loops during switching phases, need very complicated circuitries and are not easy to implement in high-voltage and high-power applications.

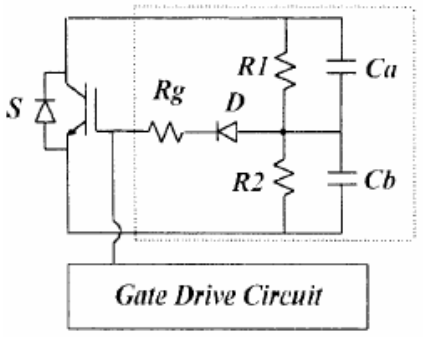


Fig. 5-5 dv/dt control approach during turn off for series-IGBTs [5-6]

The more precise and more complex approach is to combine many voltage unbalance information like the overvoltage across the IGBT, the over voltage change slope, gate current, gate current change and gate voltage. As shown in Fig. 5-7, all the signals above are feedback to the gate side and computed by the analog circuits. The fast response and smart computation circuitry is required to minimize the signal delay. These circuits are so complicated that it is not suitable for high voltage, high power application. Also the EMI noise may corrupt the useful signal and dysfunction the whole feedback loops.

Another gate-signal adjustment method is to balance the gate currents among the series-connected IGBTs. This method is to combine all the gate wires for the series-connected IGBTs magnetically with cores to synchronize the gate pulses [5-25]-[5-26]. So the magnetized inductance and leakage inductance of the core have to be carefully designed to prevent the gate current from oscillating.

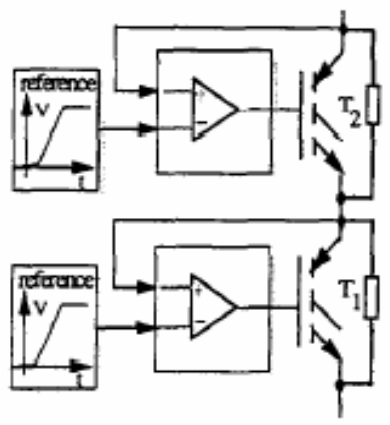


Fig. 5-6 Reference ramp voltage approach [5-21]

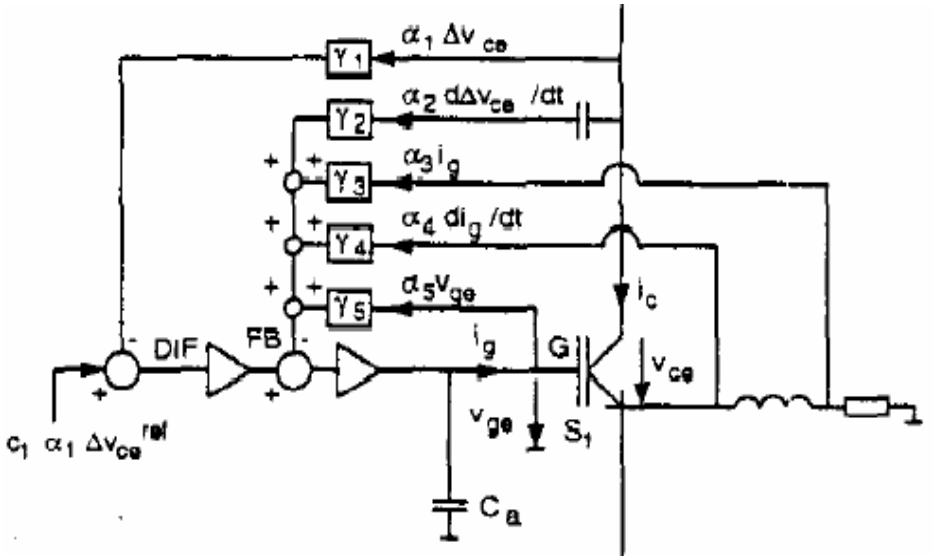


Fig. 5-7 Active gate control approach [5-28]

It should also be pointed out that balancing the voltage during an IGBT's tail current phase is very important [5-18] [5-27]. Simple analysis can show that the IGBT that supports the highest voltage will have to support even more voltages during this phase. Due to the bipolar current conduction mechanism, IGBT exhibits a significant amount of tail current, which is sensitive to device design and temperature. During the tail current phase, the IGBT can be approximately modeled as a current source, which can have different parameters, depending on variations of IGBTs and the switching conditions. When two IGBTs are connected in a series, because of the differences in the tail currents,

each IGBT will withstand a different voltage; hence the unbalanced voltage can occur during the tail current phase. Papers previously published [5-21]-[5-22] concentrated mostly on the switching transient voltage balancing using dv/dt, di/dt control. These dv/dt, di/dt control methods have little effect on the voltage difference due to the tail current.

Previously reported solutions to the voltage sharing problem due to a tail current phase include the use of a Zener diode to clamp the over-voltage caused by tail current. However, medium-voltage Zener diodes are not available; hence the series connection of Zener diodes is necessary. Furthermore, the series of Zener diodes can only clamp at a fixed value of over-voltage. If the bus voltage is lower than the Zener voltage, it cannot ensure the voltage balance between series IGBTs.

5.3 SPSS Voltage Balancing Principle

As discussed above, various existing techniques for voltage balancing all have some disadvantages when applying to high-frequency devices for a medium voltage application range. They may be either too complex or expensive to implement, can cause severe oscillation to damage the IGBT devices, or can incur too much energy loss. When developing voltage balancing technique for SPSS, the idea is to develop a practical approach that can combine both device-terminal voltage clamping and gate-signal delay control for a single-series connection. The active clamping circuit will handle the terminal voltage overshoot during start up and other drastic bus voltage change, while the gate delay control circuit enables voltage balancing during regular operation when the knowledge of device terminal voltage is available.

The proposed voltage-balancing circuit consists of two parts, static balancing and dynamic balancing, as shown in Fig. 5-8 [5-31]. To achieve proper voltage balancing in a series connection, it is important to ensure that the transient voltage for each switch is under a reasonable value and the balance can be achieved when the switch is in the steady off state. In addition, we have to be able to provide gate drive power. The steady-state voltage balancing can be achieved by using a parallel resistor R_1 as shown in Fig. 5-8. The resistor R_1 value can be determined according to the IGBT leakage current. The voltage across C_1 is constant because the Zener diode clamps the capacitor C_1 voltage to a

certain value. The resistor withstands most of the bus voltage and determines the static balancing condition.

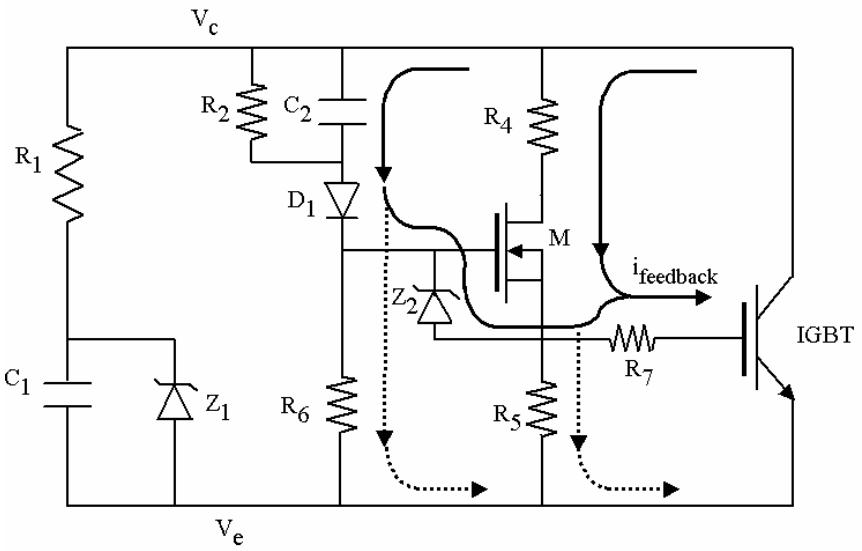


Fig. 5-8 Voltage balancing circuit for series connected IGBTs

Achieving dynamic voltage balance is more challenging. In a typical IGBT gate drive circuit component parameter differences can cause gate drive unit behaviors to be different such as different gate delays, which can cause dynamic voltage imbalance. In some cases a dangerous overvoltage can develop on a particular IGBT in the series chain. The voltage imbalance can also be generated by the variation of IGBT characteristics such as a difference in the IGBT's gate capacitances, and a difference in turn-off times and turn-off tail currents.

The above problems can be solved if the IGBT's gate-emitter voltage can be controlled so it is inversely proportional to the overvoltage on the IGBT in question. In the proposed circuit, shown in Fig. 5-8, the capacitor C_2 "remembers" the steady state voltage value of the individual IGBT. When an overvoltage occurs from the collector–to- emitter of the IGBT, capacitor C_2's voltage increases, the MOSFET M's gate voltage increases, and the MOSFET is turned on. A current flowing through the resistor R_7 is fed to the IGBT gate. This will make the IGBT turn on slightly (not fully saturated). The IGBT overvoltage can be reduced accordingly. The MOSFET cannot be turned on completely due to the feedback resistor R_5.

The design of the voltage balancing circuit in Fig. 5-8 must consider both the static and dynamic balancing need under various bus voltage conditions. The circuit must also be reliable and not to cause false turn-on under fluctuating voltages. In addition, the circuit itself should be as low loss, compact, and low cost as possible. As mentioned already, the static balancing is determined by the branch of R_1, C_1, and Z_1. C_1 functions as the voltage source for the gate driver (not shown in Fig. 5-8) and works complementarily with the dynamic self-power unit to be described. The capacitance of C_1 should be sufficiently large to meet the gate driver need, and its voltage is clamped by Z_1 (15V for the SPSS prototype) so it is not afftected by different bus voltage levels. R_1 and Z_1 current ratings should be significantly higher than IGBT leakage currents for good static balance and a rating of about ten times that of the leakage current is selected in the SPSS design. The impact of R_1 on the bus voltage range should also be considered, which will be described in the following section.

The dynamic balancing circuit acts through current $i_{feedback}$ on R_7. The current ratings of D_1, Z_2, M, R_4, R_5 and R_7 can all be related to and lower than $i_{feedback}$, which is less than 10A in similar range to the IGBT dynamic gate driving need. When the MOSFET *M* supposes to be off, the resistor R_6 helps to maintain it in the off-state, and therefore can be low voltage with high resistance (<1kΩ). On the other hand, C_2 bears the DC bus voltage and needs to maintain a relatively constant voltage during the switching transient so a high voltage capacitor with sufficient capacitance is needed (hundreds of nF capacitor used in the prototype). Zener diode Z_2 (15V) clamps the MOSFET *M* gate voltage and provides the path for C_2 current. *M* has to block the same bus voltage as the IGBT so a 1200V MOSFET is used. The function of R_5 is to generate a negative feedback when *M* is turned on, so its resistance is determined by the feedback voltage requirement and is relatively low (tens of Ω for the prototype). Therefore R_4 determines the conduction current of *M*. For the prototype, R_4 is in the range of hundreds of Ω. R_7 is a small resistance similar to the IGBT gate drive resistance and is about 10Ω. Resistor R_2 has high resitance (hundreds of kΩ) and provides a charge balancing path for C_2. High voltage diode D_1 prevents C_2 from discharging through IGBT when it turns on.

The dynamic voltage balancing circuit design has to consider the bus voltage fluctuation to avoid a false IGBT turn-on and excessive switching loss. The series resistor

R_5 has a intrinsicly strong negative feedback effect when the MOSFET *M* turns on, such that it limits the MOSFET and thus the IGBT conduction. In other words, the feedback current $i_{feedback}$ flowing to the IGBT gate side is very weak. Also during the off-state, the IGBT gate driver, which is connected to the IGBT gate side and not shown in Fig. 5-8, outputs a negative voltage (–15V) to further pull down the gate potential. This can keep the IGBT safely in the off-state. During the turn-off switching transient, the capacitor C_2 is activated when its voltage exceeds the steady state value. The feedback current will slow down the turn-off speed and cause the overvoltage to decrease. During the IGBT on-state, the capacitor C_2 voltage drops. If it drops too much in the subsequent switching, a longer turn-off time may result, leading to a high switching loss. A sufficiently large capacitor C_2 with large R_2 will result in a large discharge time constant (about 10ms for the SPSS prototype), which will keep the C_2 voltage practically constant to maintain fast switching.

From the above analysis one can see that the feedback current flowing into the IGBT gate drive is composed of two parts – one part flowing through C_2, Z_2, and the other through the MOSFET. The capacitor C_2 current mainly flows through Zener diode Z_2, because the value of resistor R_6 is much larger than that of R_7. So the total feedback current to the IGBT gate can be expressed as the following:

$$i_{feedback} = C_2 \frac{dV_{ce}}{dt} + \frac{V_{ce}}{R_4} \tag{5-1}$$

The proposed voltage balancing scheme is also effective during the IGBT current tailing phase. The experimental verification for the voltage balancing control will be presented after the discussion on how it works for the tail current control.

5.3.1 Tail Current Control

During turn-off, the IGBT behavior is very similar to a MOSFET except for the tail current. First the collector-to-emitter voltage reaches DC bus voltage, and then the current begins to fall, simultaneously for each of the series IGBTs. When the collector current reaches a threshold value that may vary for different IGBTs, an IGBT behaves

like a current source depending on the IGBT's doping profiles and switching conditions. A simplified model, shown in Fig. 5-9 can be used to analyze the voltage unbalance between the two series IGBTs during current tailing. R_{tail1} and R_{tail2} are the equivalent collector to emitter resistances during the period. The values of the resistances depend on the drift layer doping density and diffusion coefficient etc that are determined by the processing technology. Assuming R_{tail1} and R_{tail2} are equal for the series-IGBTs during turn-off transient, the current difference between the tail currents i_{tail1} and i_{tail2} will cause different currents flowing through the resistances, which results in the voltage imbalance. In general, neither tail currents nor equivalent resistances are equal, the voltage imbalance is likely to occur during the tail current phase without proper control.

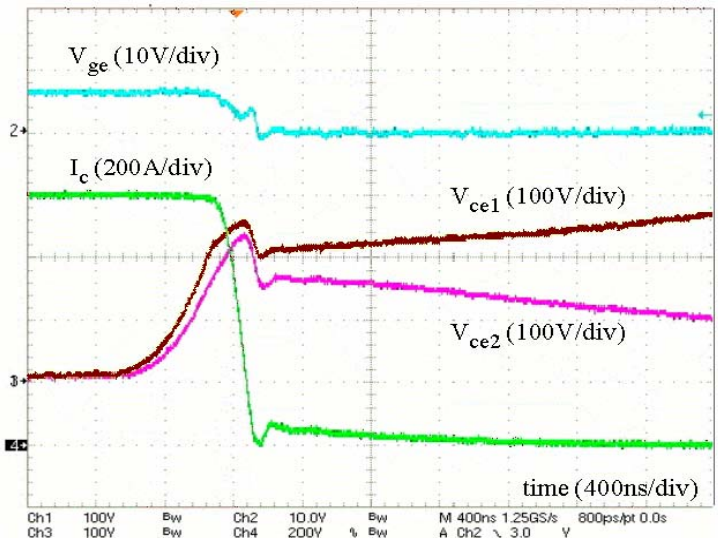


Fig. 5-9 The IGBT that handles the highest voltage after switching has increasing voltage due to tail current differences

The importance of voltage balancing during the IGBT tail-current phase and the limitations with previous solutions have been discussed and identified. The Fig. 5-9 shows an experimental waveform of two IGBTs in a series, with one of the IGBT faster than the other. It can be seen that the faster IGBTs has a higher voltage (Vce1) at the end immediately after turn-off. This IGBT voltage grows even higher during the tail current phase. After the turn-off transient the collector-to-emitter appears to have a high

resistance (about 200Ω). The tail current difference (about 1A) flows through these resistances, which results in an voltage unbalance across the IGBTs (about 200V). The simplified circuit model, shown in Fig. 5-10 can be used to quantitatively analyze or simulate voltage increases in the $IGBT_1$.

The paralleling circuit to the IGBT in Fig. 5-8 behaves like a voltage-controlled current source, which is also effective in controlling the voltage imbalance during the tail current phase. Its principle can be explained as follows. This circuit uses capacitor C_2 to keep the static state balance voltage in order to memorize the initial balance voltage achieved by parallel resistor R_1. During the tail current period, when the IGBT bus withstands an over-voltage, the capacitor C_2 is charged through R_6, so the voltage across R_6 increases. When the voltage increases to the threshold gate voltage of MOSFET M, the MOSFET will turn on, and start to carry the collector current difference between the series IGBTs during the tail current period. Therefore, the over-voltage across the IGBT can be decreased. The MOSFET only turns on slightly and is not fully saturated, so there is not much current flowing through the MOSFET. The overall power loss can be small due to the very short time.

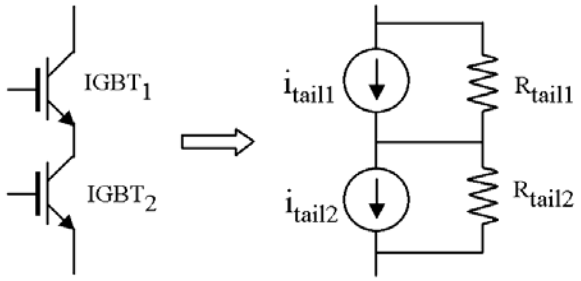


Fig. 5-10 The simplified analytical model for two series IGBTs during tail current period

The performance of this voltage control circuit was tested using two series IGBTs of 1200V and 2400A. The IGBT voltage waveforms are shown in Fig. 5-11. Without the tail current control, we can see that the two IGBT voltages differ significantly. Immediately after the turn-off transient, each IGBT voltage increases to half of the bus voltage. Then one IGBT voltage increases to nearly the full bus voltage while the other's voltage decreases to nearly zero. After about 400us, each IGBT voltage returns back to half of the bus voltage, and resumes the balanced voltage sharing state. When more IGBTs are in a

series connection, additional test results show that one IGBT may bear most of the bus voltage, which can lead to the destruction of the device. After implementing the proposed voltage control circuit, the voltage imbalance can be significantly reduced to a safe operating condition, as shown in Fig. 5-11. It also takes a much shorter time to achieve the balanced state.

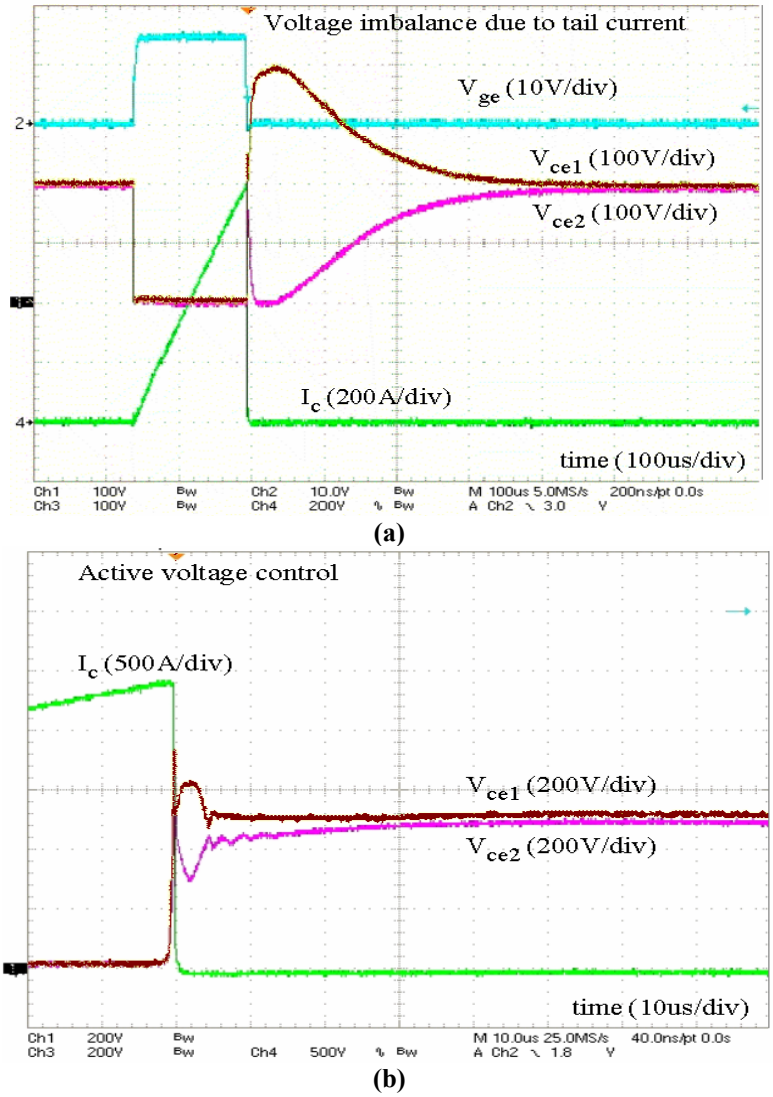


Fig. 5-11 Voltage balance with and without tail current control

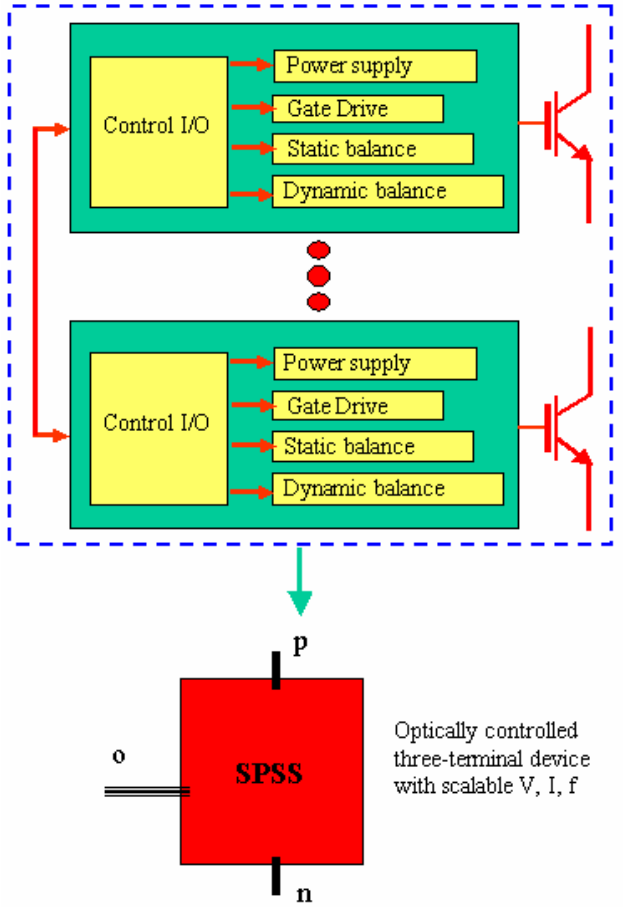


Fig. 5-12 Schematic of optically controlled three-terminal power semiconductor switch

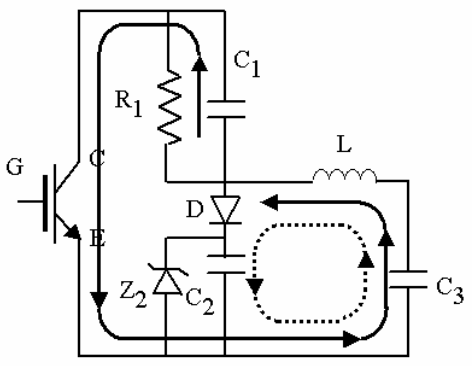
5.4 SPSS Development and Operation

In addition to the key issue of voltage balancing, there are other important aspects to the development of the SPSS. Fig. 5-12 shows the main functional block diagram of the SPSS, including not only the gate driving and voltage balancing functions, but also the self-sufficient power supply for the gate drive circuitry and control circuit for PWM signal communications among the IGBTs. Thermal management and packaging are also very important for the SPSS to function as a single device. The objective is that for a user, the SPSS should behave as an optically controlled three-terminal device.

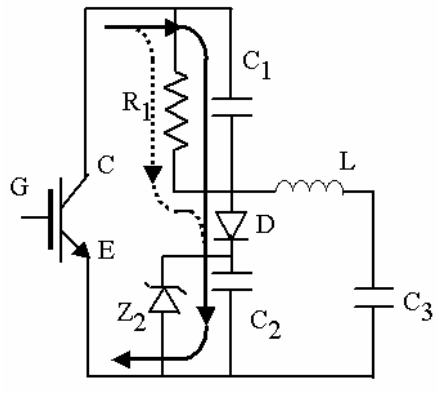
5.4.1 Power Supply for Gate Drive

In order for the SPSS to have a simple interface, its IGBT gate drive power is designed to draw directly from the main DC bus. As a result, the developed SPSS is limited to the voltage source converter applications, which are generally the converter of choice for IGBTs.

The proposed self-power supply circuit is shown in Fig. 5-13. It consists of high-voltage capacitor C_1, low voltage capacitor C_2, auxiliary resistor R_1, oscillation loop capacitor C_3 and inductor L. During the normal off state, capacitance C_1 withstands most of the bus voltage. Capacitance C_2 acts as a voltage source bank. The bus voltage charges capacitor C_2 through the auxiliary resistor R_1. The drive unit gets power from capacitor C_2. When the IGBT turns on, the high voltage of capacitor C_1 is applied across capacitor C_3 and inductor L. The current on inductor L increases. The energy of C_1 is then transferred into C_3 and inductor L. After the inductor current reaches its peak value, it then decreases and charges capacitor C_2. When the IGBT turns off, the collector-to-emitter voltage increases and charges capacitor C_1 to the individual IGBT's bus voltage. The capacitor C_2 is also charged by the current of capacitor C_1. There is also little current (about 10mA for the prototype SPSS, equal to the driver bias current) flowing through the auxiliary resistor R_1 to the capacitor C_2, so the IGBT's drive circuit can get continuous energy during the switching transients. The high-voltage capacitor C_1 value is very small (on the order 10nF for the prototype SPSS). The additional power loss of the IGBT caused by the capacitor C_1's energy transfer is negligible (about 0.01mJ, corresponding to a 100mW loss for a 10kHz switching). During the switching transient, this power supply can also generate a negative gate voltage from capacitor C_3, which is critical for the safe operation of the IGBT. During the switching transient, the power supply efficiency is high for the given bus voltage and frequency because no high power loss component is used. When the bus voltage changes, the Zener function circuit can stabilize the capacitor C_2 voltage. The capacitor C_2, resistor R_1, and the Zener circuit together will determine the operating voltage range that can stabilize gate power supply voltage. For the prototype SPSS, the voltage range is 600V~3000V.



(a) Turn-on period



(b) Turn-off period

Fig. 5-13 Built-in power supply for gate driver

5.4.2 Gate Signal Commutation

To further simplify the user interface, there should be only one PWM control port for the proposed SPSS. A master-slave signal communication bus is employed to control the individual gate drive of the series-connected IGBTs. The master IGBT receives the PWM control signal optically from the control board, and then transfers the command signal to the slave IGBTs. This communication architecture is shown in Fig. 5-14. Since there is a potentially high voltage difference between the IGBT's gate drive circuits, optical buses are adopted for isolation. Test results show that the time delay difference due to the optical fiber is virtually undetectable as a result of the short fiber length (<20cm).

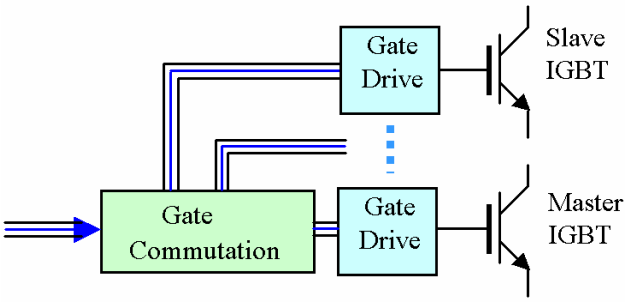


Fig. 5-14 Gate signal communication

5.4.3 SPSS Packaging

The proposed SPSS can be integrated into a standard module package. The main issues in designing the packaging are 1) high voltage isolation among IGBTs; 2) the thermal handling capability of the SPSS; 3) mechanical integrity, and 4) scalability for other current and voltage ratings. The key is to balance the electrical and thermal requirement. When more than two IGBTs are in series, the collector-to-baseplate insulation voltage has to be high enough to satisfy the requirement of high operational voltages while not greatly increasing the thermal resistance.

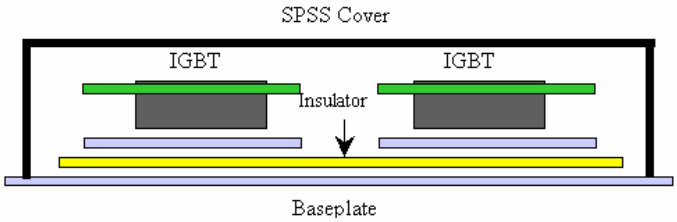


Fig. 5-15 SPSS structure showing the integration of IGBTs into single module housing

To meet these electrical and thermal requirements, the packaged SPSS structure is shown in Fig. 5-15. One can view this as a giant IGBT module. The large baseplate supports all the IGBTs inside. Between the IGBTs and the baseplate, an insulation structure is added to increase the isolation voltage between the IGBTs and the baseplate. The individual IGBT's junction-to-case (baseplate) thermal resistance increases by the additional insulation layer (0.009^0C/W for the prototype). The contact thermal resistance between the insulator and the baseplate is negligible because of the well-processed

contact. The designed structure can therefore satisfy the high voltage and low thermal resistance requirement.

The thermal system of the integrated SPSS is shown in Fig. 5-16. The main difference between this and a single IGBT is that the junction-to-case thermal resistance $R_{j\text{-}c(spss)}$ for the SPSS consists of N parts where the N is the number of IGBTs in series. The equivalent device thermal model is the parallel of thermal models of the N IGBTs. The baseplate thermal model is the parallel of N small baseplate thermal models. The power loss is the total of N IGBTs' switching and conduction losses. As an example, for four IGBTs in series, the steady-state junction-to-case thermal resistance $R_{j\text{-}c(spss)}$ can be simply expressed as:

$$R_{j-c(spss)} = R_{j-c,IGBT}/4 + R_{c-sb,IGBT}/4 + R_{sbase}/4 + R_{insulator} + R_{base} \tag{5-2}$$

where $R_{j-c,IGBT}$, $R_{c-sb,IGBT}$, R_{sbase}, $R_{insulator}$, and R_{base} are the thermal resistances of IGBT junction-to-case, IGBT case-to-small baseplate, the small baseplate, insulator, and large baseplate, respectively.

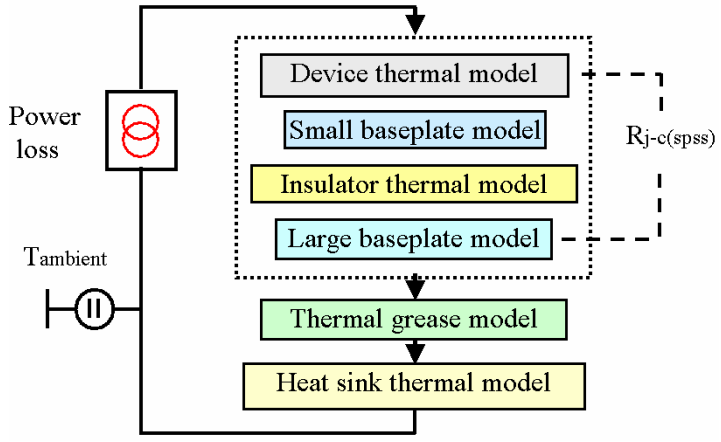


Fig. 5-16 Thermal system for the integrated SPSS

5.4.4 Switching Frequency Range

The built-in gate power supply of the SPSS gets energy from the power DC bus. The precondition is that the bus voltage should be above a certain value. In our current design, the SPSS will turn off automatically once a gate drive under-voltage is detected. The

under-voltage limit means that the SPSS has a maximum 'on' time, which also means that the switching frequency of the SPSS has a minimum value. This limit can be estimated as follows.

The total gate drive power requirement is the sum of the power to supply the IGBT gate charge and other power dissipation in the gate drive circuit. From this we can determine the maximum turn-on time. Assuming that the energy the gate drive receives is E_{supply}, and the average power dissipation for independent gate drive circuits during IGBT switching is P_{bias}. The maximum turn-on time $t_{on,\max}$ and corresponding minimum switching frequency $f_{s\min}$ can then be determined from the following equation (5-3).

$$E_{supply} = P_{bias} t_{on,\max} + Q_g V_g f_{s\min} \approx P_{bias} t_{on,\max} \tag{5-3}$$

where Q_g and V_g are gate charge and voltage. From equation (5-3) one can obtain minimum switching frequency $f_{s\min} = 1/t_{on,\max}$ if neglecting the second term because it's very small. To increase the maximum 'on' time, reducing the gate drive circuit's power consumption is important. Low power dissipation driver chips are preferable. When the SPSS is in the constant "on" mode, no energy can be transferred to the gate side. While the SPSS with self-power gate drive cannot operate for continuous on-state operation (such as in DC breakers or transfer switch), for general converter applications such as PMW mode operation, the gate driver can get the continuous power from the power stage side. For the prototype SPSS, the designed minimum switching frequency is 10Hz, posing no practical limits for most applications.

The maximum switching frequency of the SPSS is mainly determined by IGBT losses and the thermal handling capability of the SPSS package and cooling system. Due to the use of a low-voltage IGBT in the SPSS, the IGBT loss is lower than that of high-voltage IGBTs. In addition, the proposed SPSS package structure maintains an unchanged thermal path for each individual IGBT. Hence the upper switching frequency of the SPSS is close to each individual IGBT's upper switching-frequency limit. This is the key concept of the SPSS, because we can expand the SPSS's switching frequency limit to a

10 to 20kHz range that is currently unachievable for high-voltage IGBTs and other high-voltage bipolar devices such as the IGCT and ETO.

Assuming that $R_{j-c(SPSS)}$ is the individual IGBT's junction-to-case thermal resistance, E_{on}, E_{off} are IGBT turn-on and turn-off energies, P_{on} is conduction loss, and T_{jc} is the junction-to-case temperature difference. The upper switching frequency f_1 determined by the thermal management system is

$$(E_{on} + E_{off}) f_1 + P_{on} = T_{jc} / R_{j-c(SPSS)} \tag{5-4}$$

As discussed above, based on the SPSS package, f_1 should be in the same range as in the case of a single IGBT, provided that the thermal management system is comparable.

Since the SPSS's gate drive obtains power from the DC bus during the off state, as well as during the SPSS turn-on and turn-off, the transferred energy increases linearly when the switching frequency increases. The power consumed by the IGBT gate capacitance also increases linearly, though it is normally much less than the transferred energy from the power supply. The difference between the consumed and transferred energy accumulates and flows through a Zener clamp circuitry in parallel to C_2 in Fig. 5-13. To some extent the maximum allowed power dissipation of Zener circuitry limits the SPSS's upper switching frequency. The maximum switching frequency f_2 from this limitation can be found from equation (5-5).

$$P_T = (E_{transfer} - Q_g V_g) f_2 - P_{bias} \tag{5-5}$$

where P_T is Zener circuitry maximum power dissipation, $E_{transfer}$ is transferred energy for one switching period, $Q_g V_g$ is the energy needed to charge and discharge the IGBT gate capacitor, and P_{bias} is the gate drive circuitry bias power dissipation. Hence the maximum operation switching frequency $f_{s\max}$ can be determined considering the above factors.

$$f_{s\max} = \min(f_1, f_2) \tag{5-6}$$

For given applications one can design the proper switching frequency to meet the requirements. Normally, f_{smax} is limited by thermal resistance.

5.4.5 Voltage Range

The proposed SPSS can only operate for a certain range of DC bus voltage. The upper range is determined by the number of series IGBTs and the isolation voltage of the SPSS baseplate design. The lower limit is determined by the gate drive circuit power requirement during the off state. When the SPSS is 'off', the drive supply gets energy from the DC bus through the balance resistor R_1 in Fig. 5-8. The resistor is selected according to the gate drive power requirement P_{bias} and the IGBT's off-state leakage current. The leakage current is much smaller than the gate driver bias current.

The minimum working voltage should meet the requirement to provide sufficient energy through the resistor to the drive supply. Assuming the gate driver's bias current requirement is i_{bias}, the minimum working bus voltage $V_{bus\min}$ is

$$V_{bus\min} = R_1 i_{bias} = R_1 \frac{P_{bias}}{V_g} \tag{5-7}$$

One can select the balance resistor according to gate driver requirement. The higher R_1, the higher the minimum bus voltage at which the SPSS can operate. Again, for the prototype SPSS, the minimum voltage is 600V.

5.4.6 SPSS Prototype

Employing all functions discussed above, a prototype SPSS utilizing four 1200V, 300A IGBTs is developed. The SPSS prototype has a nominal rating of 4800V, 300A and 10kHz. As described previously, the SPSS does not need an additional external power supply. It appears and functions as a three-terminal device with only one optical control terminal and two power bus terminals. Table 5-1 lists the main parameters of the prototype SPSS. The recommended DC bus voltage and switching frequency are determined by the design based on the discussions above. The conduction voltage drop $V_{ce(sat)}$ is the total on-state voltage across the series-IGBTs, which is higher than that of a

single high voltage IGBT rated at comparable voltage and current. Of course, the high voltage IGBT has much worse switching loss characteristics. The developed prototype SPSS is shown in Fig. 5-17, with the three terminals clearly marked, positive p, negative n and optical gate o. The large baseplate is on the bottom and can be directly placed on a heat sink.

Table 5-1 Main parameters of the prototype SPSS

Collector-Emitter Voltage	V_{ce}	4800V
Collector Current	I_c	300A
Recommended DC Bus Voltage	V_{DC}	600 to 3000V
Collector-Emitter Saturation Voltage (typical)	$V_{ce(sat)}$	2.5x4V@300A
Recommended Switching Frequency	f_s	10Hz to 10kHz
Thermal Resistance, Junction to Case (per IGBT, Max.)	$R_{th(j-c)}$	0.073 °C/W
Base Plate to IGBT Isolation Voltage		>5000V

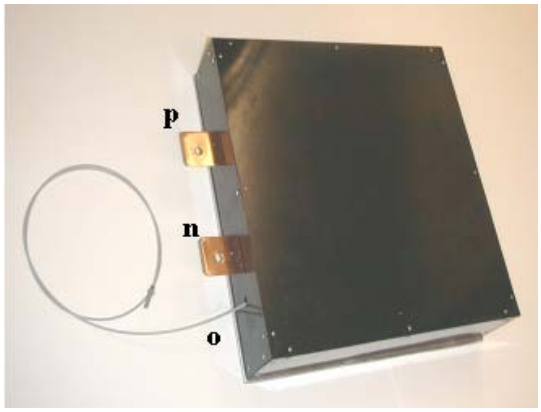
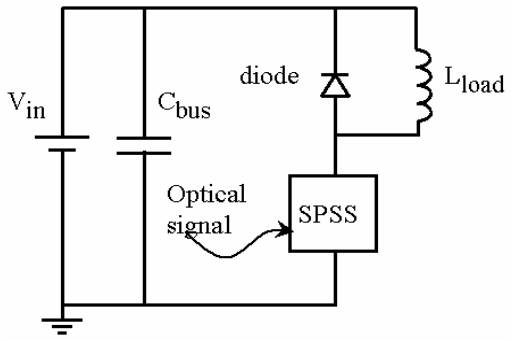


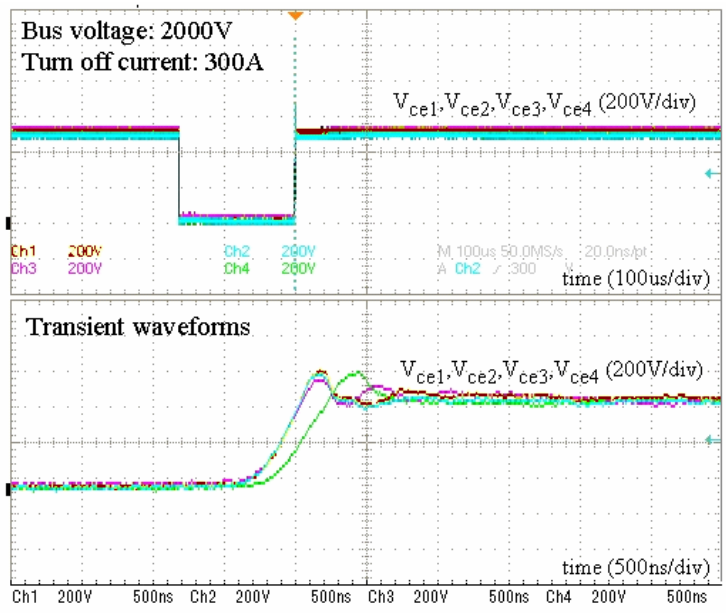
Fig. 5-17 Prototype of a 4800V, 300 A, 10 kHz SPSS

5.5 Experimental Verifications

Experimental measurements of the developed SPSS were conducted at a bus voltage of 2kV and a load current of 300A. All designed features have been tested and verified. Key test results and measurements are presented and discussed below.



(a) Test circuit



(b) Turn-off waveforms

Fig. 5-18 Voltage balance during the Scalable Power Semiconductor Switch turn-off

5.5.1 Switching Characteristics

The SPSS switching is controlled by an optical control signal via the device's control terminal. Fig. 5-18 shows the experimental circuit and results during the turn-off of an inductive load current. Three IGBTs' collector-to-emitter voltages are almost identical, while the fourth one is turned off a little later (100ns). Even so, all IGBT collector-to-emitter voltages reach about the same value as a result of the feedback gate control circuits in Fig. 5-8. The voltage balancing during the tail current phase is also excellent.

5.5.2 Gate Driver Power Supply

To verify that a constant gate voltage is maintained for all IGBTs under various switching conditions, a special test with resistive load at low bus voltage was conducted. First the maximum 'on' time or the minimum switching frequency is measured for the SPSS prototype, which corresponds to 10Hz. Then a higher frequency 20kHz is selected to verify the gate drive power supply function. Fig. 5-9 shows the test results and the bus voltage for each IGBT is 150V. From the waveforms one can see that the gate voltage remains constant at 15V and works normally. When the SPSS turns on, the voltage across each IGBT drops to nearly zero, and the dynamic power supply capacitor transfers the energy to the voltage source capacitor C_2 in Fig. 5-13. When the SPSS turns off, the voltage V_{ce} increases from 0 to 150V. Thus the drive can get continuous energy from the bus during the continuous switching period.

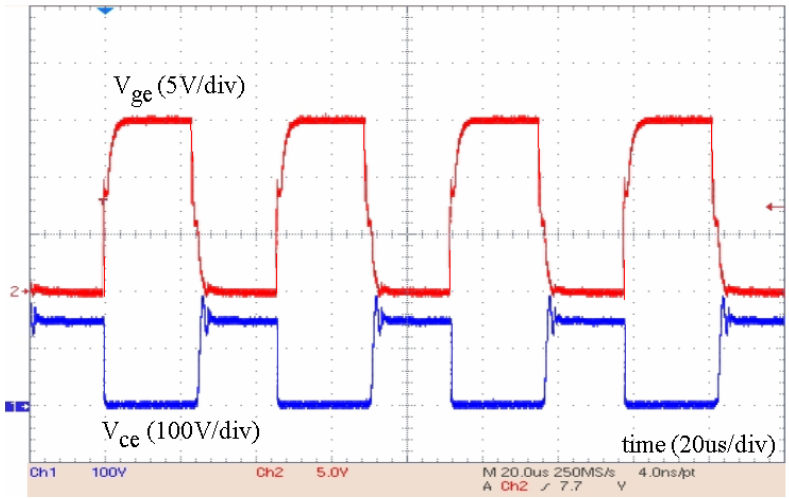


Fig. 5-19 20kHz switching test showing that constant drive voltage can be maintained (Scale: upper trace: 5V/div, lower trace, 100V/div)

5.5.3 Burst Mode Operation

A high-power burst mode operation was tested for the prototype SPSS with a bus voltage of 1200V. A multi-pulse generator was used to control the SPSS in a boost converter circuit. When the first pulse comes, the SPSS turns on and the load inductor current increases from zero; when the SPSS turns off, the current flows through the freewheeling diode. A number of pulses at 15 kHz were applied to the SPSS in such a manner that the final collector peak current i_c reached 150A. Fig. 5-20 shows the switching waveforms with two IGBTs voltage V_{ce}. During this test, the gate drive power supply remains constant, which is maintained by the voltage source capacitor C_2 in Fig. 5-13.

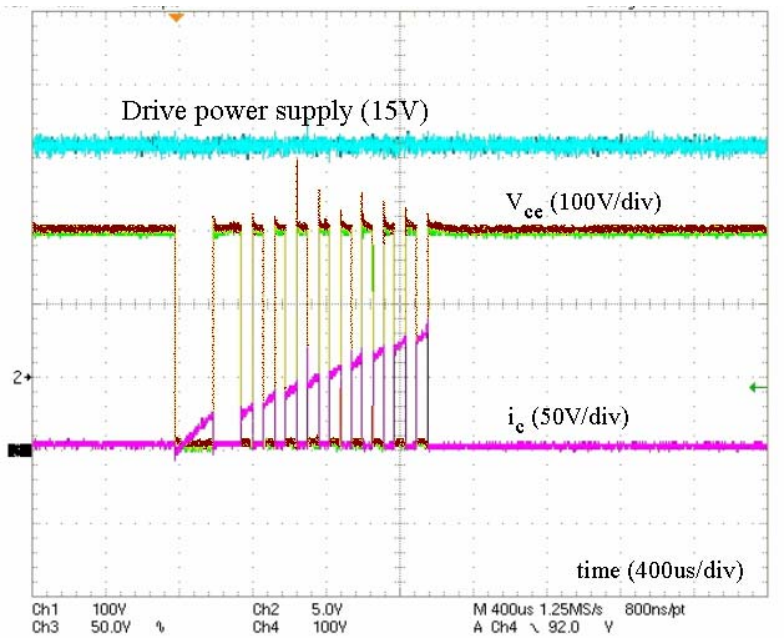


Fig. 5-20 10 pulses, 15 kHz burst mode operation of the SPSS

5.5.4 Bus Voltage Fluctuation

A test was also conducted to verify SPSS under fluctuating voltage. A 800V DC bus voltage was applied on the SPSS with four series-IGBTs. Fig. 5-21 shows that when the top two IGBTs are turned on suddenly, the bottom two IGBTs are still kept at their off-state with their collector-to-emitter voltages V_{ce3} and V_{ce4} jump from 200V to 400V.

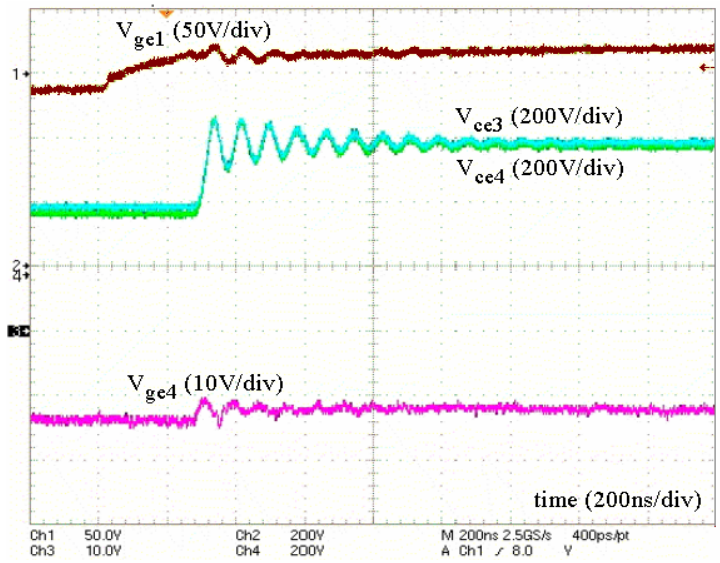


Fig. 5-21 SPSS under sudden change of bus voltage (V_{ge1}: gate-to-emitter voltages for the top two IGBTs; V_{ge4}: gate-to-emitter voltages for the bottom two IGBTs; V_{ce3} and V_{ce4}: collector-to-emitter voltages for the bottom two IGBTs)

5.6 Summary

This chapter presents the design and development of a Scalable Power Semiconductor Switch (SPSS). A 4800V, 300A, 10kHz SPSS was developed using four 1200V, 300A series-connected high frequency IGBTs. The static and dynamic voltage balancing between series-connected IGBTs is achieved using a hybrid approach of an active clamp circuit and an active gate control, which also works effectively during the tail-current phase. The developed SPSS also has a built-in power supply drawing the power directly from the DC bus, and a single optical control terminal that connects to all IGBT gate drives in a master/slave manner. An integrated package with a common base plate was used to achieve a thermal characteristic compatible with that of a single device. These design features allow the SPSS unit to function as a single optically controlled three-terminal switching device for users. The SPSS voltage rating is determined by the total ratings of the connected IGBTs with properly designed package insulation. While there is a theoretical minimum voltage limit due to the self-power drive circuit requirement, it poses little practical limitations for practical converter applications. Its current rating is practically identical with that of individual IGBTs given their compatible thermal

characteristics. The SPSS switching frequency capability is close to that of the individual IGBTs. Experimental evaluation of the prototype SPSS shows it fully achieves the design objectives. The SPSS is a useful power switch concept for building high voltage, high power and high frequency switching functions that are beyond the capability of individual power devices.

Chapter 6 Conclusions and Future Work

In this dissertation, the power semiconductor devices for high power density converter applications are investigated. The methodology is developed to evaluate the power semiconductor devices for high power density applications first. The power density figure of merit (PDFOM) for power MOSFET and IGBT are derived from the power loss, junction temperature rise and package points of view. The devices matrixes are generated for device comparison and selection to show how to use the PDFOM. A calculation example is given to verify the validity of the PDFOM. Several semiconductor material figures of merit are developed. The wide bandgap materials based power devices benefits for power density are explored compared to the silicon material power devices.

Secondly, the high temperature operation characteristics of power semiconductor devices including power MOSFET and IGBT have been presented. The device breakdown voltage, leakage current and thermal stability are tested and analyzed. The avalanche breakdown voltage change with junction temperature rise is verified by the experiments. The leakage current nearly increases exponentially with junction temperature rise, which contributes to the thermal instability at high junction temperature operation. To study the thermal stability of power device, the closed loop thermal system and stability criteria are developed and analyzed. At low junction temperature and high switching frequency operation, the switching loss determines the thermal stability. At high junction temperature, the high leakage current power loss causes the thermal instability. From the developed thermal stability system, the maximum switching frequency can be derived for the converter system design. The developed thermal system analysis approach can be extended to other Si devices including IGBT or wide bandgap material devices such as SiC device. For SiC power MOSFET, the predicted thermal stable point can be pushed much higher to operate the device at higher switching frequency and higher junction temperature.

The high power density converter operation requires the power devices switching at high case temperature for increased switching frequency and smaller heatsink size, thus results in the increased high junction temperature. To fully and safely utilize the power

devices the junction temperature prediction becomes necessary. The junction temperature prediction approach is developed and implemented in the system test, which considers the parasitic components inside the power MOSFET module when the power MOSFET module switches at hundreds kHz. Also the thermal stability for pulse power application characteristics is studied further to predict how the high junction temperature operation affects the power density improvement.

Thirdly, to develop the high power density converter, power MOSFETs are often used in parallel as the main switch to meet the high current rating requirement. However the current sharing issues during conduction and switching transient states may generate higher power losses, which need to be analyzed further. Differential conduction resistance can cause current unbalance and are limited due to the positive temperature coefficient of the MOSFET resistance. However it can not be completely compensated. On the other hand, the transconductance and threshold voltage differences result in limited current unbalance. The miller capacitances will affect the time required for the drain-to-source voltage to collapse across other parallel devices. The drain and source parasitic inductance has effects on the turn-on/off current sharing. A current sharing control approach from the gate side is proposed. The experimental results indicate that the power MOSFETs can be paralleled with proper gate driver design even if the device parameters are mismatched, and accordingly the switching losses are reduced to some extent. This is very useful for the switching loss dominated high power density converter design.

The gate driving design is also important for the power MOSFET module. The power MOSFET module with parallel dice inside has an intrinsic parasitic inductive gate loop. Not careful gate driver design may cause the gate voltage oscillation during switching transient, with results in the module failure. On the other hand, the power MOSFET module has an increased input capacitance. This results in the higher gate driver power loss when the traditional resistive gate driver is implemented. The additional bulky gate driver power supply is needed due to the power loss. Therefore the advanced self-power resonant gate driver is investigated and implemented. The low gate driver loss results in the development of the self-power unit that takes the power from the power bus. Thus the

additional gate driver power supply can be removed. The overall volume of the gate driver can be minimized thus improve the power density.

Next, power semiconductor device series-connection operation is often used in the high power density converter to meet the high voltage output. The static and dynamic voltage balancing between series-connected IGBTs is achieved using a hybrid approach of an active clamp circuit and an active gate control, which also works effectively during the tail-current phase. This research presents the design and development of a Scalable Power Semiconductor Switch (SPSS) based on series-IGBTs. A prototype of 4800V, 300A, 10kHz SPSS was developed using four 1200V, 300A series-connected high frequency IGBTs. The developed SPSS also has a built-in power supply drawing the power directly from the DC bus, and a single optical control terminal that connects to all IGBT gate drives in a master/slave manner. An integrated package with a common baseplate was used to achieve a thermal characteristic compatible with that of a single device. These design features allow the SPSS unit to function as a single optically controlled three-terminal switching device for users. Its current rating is practically identical with that of individual IGBTs given the compatible thermal characteristics. The SPSS switching frequency capability is close to that of the individual IGBTs. Experimental evaluation of the prototype SPSS shows it fully achieved the design objectives. The SPSS is a useful power switch concept for building high voltage, high power and high frequency switching functions that are beyond the capability of individual power devices.

Finally, the power semiconductor devices effects on power density of power converter are investigated from the power device figure of merit, high frequency high temperature operation and device parallel operation points of view. Due to the power loss, thermal performance and package area differences for power devices, the high PDFOM power devices have the potential to improve the converter power density for same junction temperature rise. The thermal stability of power semiconductor devices limits their continuous mode operation for high frequency high temperature operation. It is also shown that the power devices can operate much higher switching frequency for the pulse power than that for continuous power. So the passive components volume and heatsink size can be minimized thus the power density are improved to some extent for power

devices high temperature operation. To identify the benefits of power MOSFET parallel operation on the power density, it is compared to the same voltage rating IGBT device as the main switch. The power MOSFET has lower power loss and better thermal handling capability, thus can switch at higher frequency. The comparison results show that the power density has two times improvement for the power MOSFET in the designed three-level parallel resonant converter. The power MOSFET in parallel as the main switch has the potential to improve the system power density due to the low loss, high switching frequency operation compared to other same voltage rating power devices like IGBT.

The future work will focus on several research points.

- The power density figure of merit is proposed first. Its practical significance should be verified in the real converter design. However, to implement a converter it involves not only the power devices also the passive components, heatsink and cooling system etc. How to evaluate the power devices effects on the real converter power density needs to study further.
- Secondly, the power device thermal stability criteria and graph are developed. The junction temperature prediction approach is proposed and implemented. The future interesting research topic is to combine them together and develop a closed loop system for the high junction temperature high frequency operation to push the power devices switching at their thermal limit. Thus the highest power density can be achieved for a certain converter.
- Thirdly, for the power MOSFETs parallel operation, the current balance control from the gate sides is investigated. Due to the fast switching transient, it is very difficult to control the current using the discrete circuits. The promising solution is to develop the integrated circuit chip to control the gate currents during the transconductance period by sensing the conduction currents.

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