USE OF IGT/COMFET IN ZERO CURRENT QUASI RESONANT CONVERTERS

by

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(ABSTRACT)

The problems associated with IGT/COMFET devices in PWM converters, such as turn off current tailing and latching are largely avoided in a resonant converter. Dynamic saturation loss is identified as the predominant power loss in IGT/COMFET devices for very high frequency resonant operation. Device design change is suggested for very high frequency resonant operation applications.

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CHAPTER I: INTRODUCTION

Quasi-resonant converters have recently received considerable attention for high-frequency, switching power supply applications. [1] EMI reduction, fast response and high power density are among the advantages in using such converters.

In a conventional pulse width modulated (PWM) converter, the current of the power switch is interrupted by gate signal of the device. Power loss due to the device switching becomes predominant design consideration especially at high switching frequency. In a zero current quasi-resonant converter operation the switching loss of the power switch is much alleviated because of resonant operation. As a result, zero current quasi-resonant converter can be operated at frequency much higher than that of a conventional PWM converter and still retains high overall power efficiency. It has been reported high efficiently (>80 percent) power conversion can be accomplished at megahertz conversion frequency using power MOS Field Effect Transistors (MOSFETs). [13]

Power MOSFETs are capable of very fast switching but are relatively high in conduction resistance compared to a recent power semiconductor switch IGTs/COMFETs (Insulated Gate Transistor or conductivity Modulated FET).

Conduction resistance of a switch becomes a much more important consideration in a zero current quasi-resonant converters compared to the PWM counterpart. This is because the power switch in a resonant

converter conducts a much higher current pulse than in its PWM counterpart. For processing the same amount of power, it is often designed that the peak current of a resonant converter switch is several times of the PWM converter switch. IGT/COMFET becomes a good candidate for the power switch in a resonant converter because of its low conduction resistance.

The objective of the research leading to this thesis is to investigate the suitability of IGT/COMFET devices for high frequency zero current switching converters. Specifically, questions such as the following will be addressed.

(1) Which characteristics of IGT/COMFET fit the resonant operation and which characteristics do not?

(2) What parameters of the device becomes dominant considerations at very high frequency (> 200 KHz) resonant operation?

(3) What is the practical upper operation frequency of IGT/COMFET in a zero current quasi-resonant converter?

(4) Is there anyway to improve the IGT device characteristics for very high frequency resonant operation?

It has been reported that a family of converter configurations operate under the same principle of zero current switching [1]. However,

the electrical stresses on the power semiconductor switch in the family of converters are identical. The discussion and the verification of the results presented in this thesis are usually focused on Buck type of converters but those are applicable to other type of converters in the Zero Current switching family.

In chapter II a review of basic device characteristic of IGT is given. Several key characteristics related to conventional forced turn-off of device were pointed out. In chapter III, IGT/COMFET is examined from the point current resonant operation. Many device problems associated with PWM operation pointed out in Chap. II become much less severe under resonant operation discussed in this chapter. In Chapter IV, the high frequency characteristics of IGT under resonant operation is examined in detailed. Power loss estimation of high frequency resonant operation is compared to a comparable MOSFET for frequency between 50 KHz and 500 KHz. The major limitations of the IGT for very high frequency resonant operation are pointed out. Suggestions for device design change to alleviate the limitations are presented in Chap. V. Chapter VI concludes the thesis and recommends future research. The appendix gives detailed descriptions of the equations for estimation of various power losses components in an IGT/COMFET resonant converter.

CHAPTER II: IGT DEVICE CHARACTERISTICS

In this chapter a review of basic characteristics of IGT are discussed. These characteristics are intermittently related to certain circuit behavior to be presented in later chapters.

In Section 2.1 the basic device structure of IGT is described. Section 2.2 describes the device operation. Section 2.3 describes the conduction resistance of IGT. In Section 2.4 forced turn-off process in IGT is described. Device latching characteristics are described in Section 2.5.

2.1 DEVICE STRUCTURE OF IGT

The cross Section of an IGT is given in Figure 2.1. In comparison with that of a conventional power MOSFET the substrate is p^+ instead of n^+. Junction J_1 provides the forward voltage blocking capability. In the reverse blocking mode J_2 provides the blocking capability.

The two-transistor equivalent of IGT is shown in Figure 2.2. The similarity to the structure of an SCR is very striking. However, both the p-n-p and n-p-n are designed with low gain to suppress the SCR action. The p-n-p is a wide base transistor with Low gain and the gain of the npn transistor is also reduced by resistance shunt R_{sh}. The resistance shunt is achieved by overlapping source metalization which introduces the bulk distributed resistance R in the emitter [2]. This

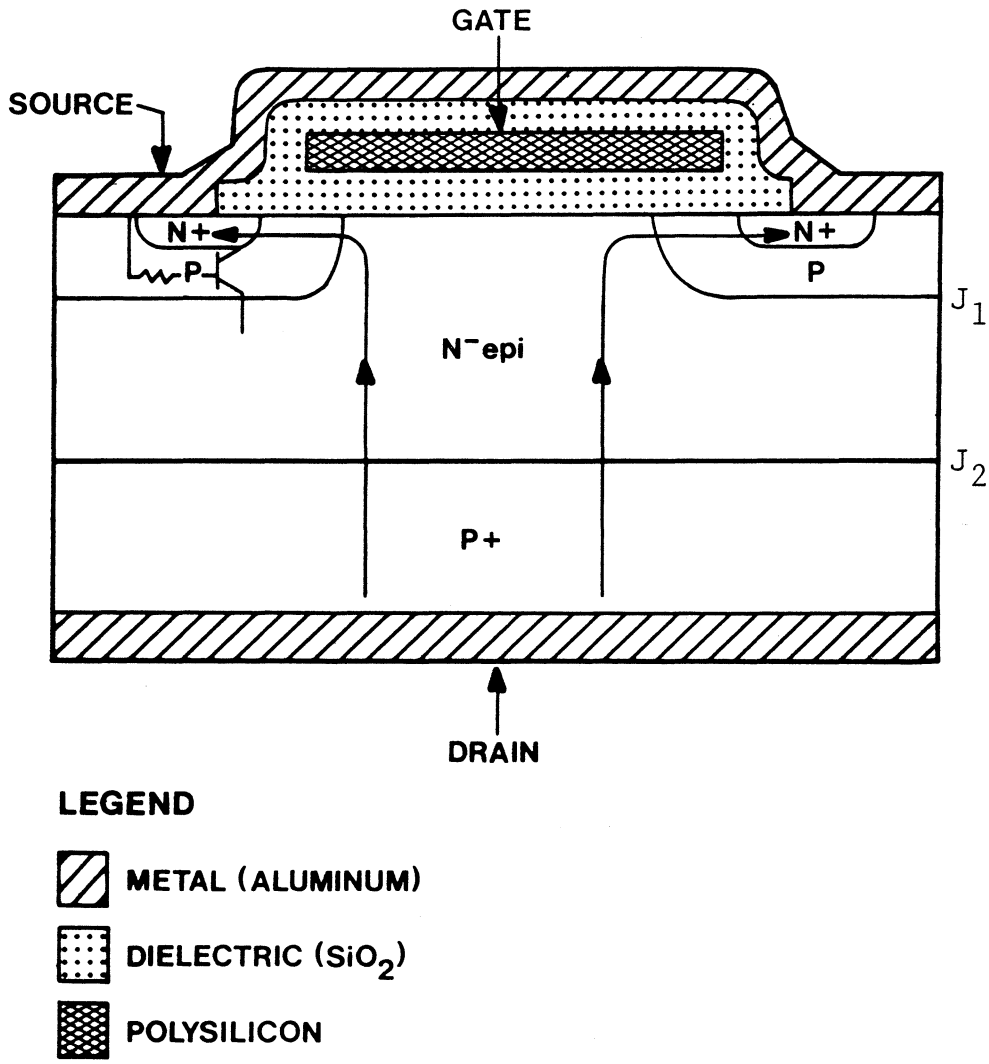


Figure 2-1. Device Structure of IGT

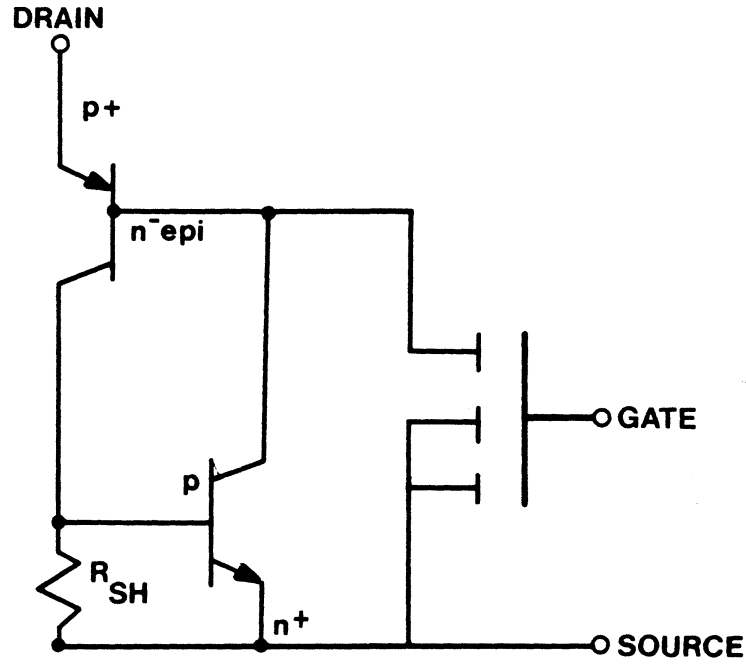


Figure 2-2. Two Transistor Equivalent of IGT

device design ensures that the alpha of the n-p-n transistor is kept deliberately low under all operating conditions and the SCR action never occur during normal operation of the device.

2.2 DEVICE TURN-ON PROCESS

The device is turned on when the MOS gate is given a positive bias with respect to the source and the drain is positive to the source. The forward gate source voltage inverts the p-doped base region immediately below the oxide, and J_2 junction is forward biased and the device conducts with n^- region conductivity modulated. A turn-on delay time exists due to a combination of the delay to charge the input capacitance and the forward recovery time of a p-i-n diode. The rise time is due to the rise time of a p-i-n diode. The p-i-n diode is a structure with highly doped p, n regions on the end and undoped intrinsic region in the middle [2].

2.3 CONDUCTION RESISTANCE

The conduction voltage of IGT mainly comprises the forward bias voltage of junction J_2 and the voltage drop due to the ohmic resistance of epitaxial n^- layer, the channel resistance and the metallization resistance. The highly resistive n^- epitaxial layer contributes little to the total drop because of conductivity modulation. It is this effect that makes IGT low conduction resistance device. This is especially significant

for high voltage devices. For a comparable chip area, the on-resistance of IGT is much smaller than an equivalent MOSFET. However a minimum conduction drop of 0.7 volts across the junction J_1 is necessary to maintain the conduction state. As a comparison, in a MOSFET device, current conduction starts at origin in the I-V characteristics. Figure 2.3 shows the I-V characteristics of an IGT and the characteristics of a MOSFET. Both devices are rated at 400 V, 10 A and the IGT/COMFET is only 1/3 of the MOSFET in terms of chip size. As can be seen from the figure, at 8A level, MOSFET has 4 conduction drop and IGT has only 2.2V.

It is this low conduction resistance characteristic which makes IGT an attractive device for zero-current switching resonant converter application. This is because resonant converters have inherently higher peak device currents than PWM converters. Hence lower conduction drop in IGT translates into lower power loss in the switching device and better overall efficiency for the converter.

2.4 TURN-OFF PROCESS OF IGT

The turn-off process in IGT could be divided into two phases. The first and the shorter phase is called the injection phase. This begins with the removal of the inversion layer in the p-base. Since the electron concentration in the n^- epitaxial layer region is high, electrons are injected into the substrate region while a corresponding hole current flows into the p-base region between n- source and the p-base.

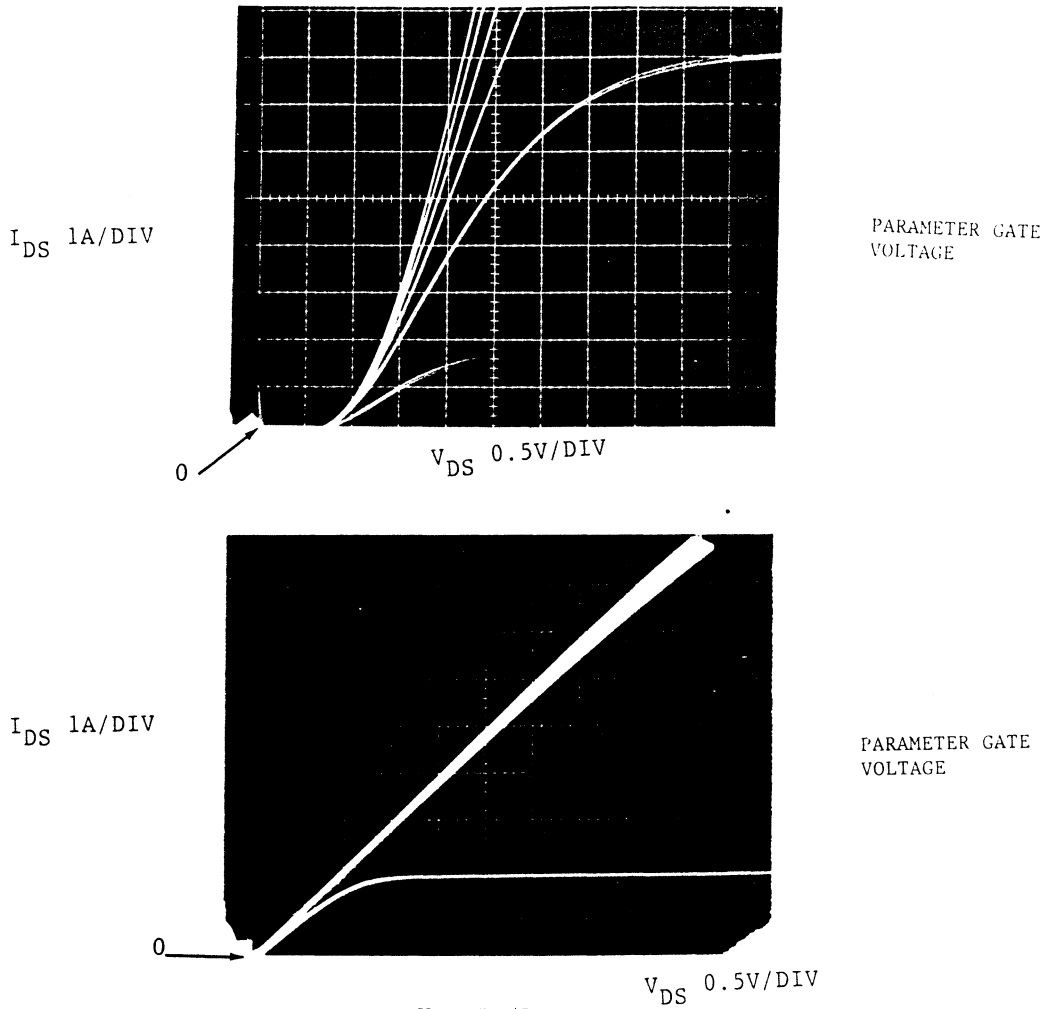


Figure 2-3. IV Characteristics of A) IGT/COMFET (GE IGT 4D10) B) MOSFET (IRF 450). Both devices are rated at 10 A, 40C V IGT/COMFET chip area is only 1/3 of the MOSFET.

The second and the longer phase of turn off is the current tailing. During this phase the plasma of electrons and holes left in the n^- epitaxial layer decays due to recombination. This time interval is independent of the gate source resistance and depends only on the device minority carrier life time in the n^- region.

One of the main obstacles in using IGT for high frequencies has been the long tailing time of the device. Excessive turn off power loss occur due to long tailing time.

The current tailing time for commercially available devices varies from 1μS to 10μS depending on the intended application of the devices. Faster device turn off could be achieved by electron or neutron irradiation. This process reduces the lifetime of minority carriers in the n^- region and speeds up the turn off process. But the trade-off involved here is the increased conduction drop [2].

2.5 DEVICE LATCHING CHARACTERISTICS

Latching in IGT is the tendency of the device to remain in its low impedance state and thus lose gate control. From previous studies done on IGT latching the following factors have been established as the conditions leading to device latching: [2]

1. excessively high current magnitudes,
2. excessively high temperatures,
3. high rate of rise of drain source voltage, and

4. high rate of fall of gate source voltage.

All four factors lead to in increased sum of the current gain α_{pnp} and α_{npn} of two transistors which eventually leads to latching. $(\alpha_{pnp} + \alpha_{npn} \rightarrow 1)$.

Efforts were made by device manufacturers in recent years to enhance this capability of IGT.

A typical application in which latching might occur is the forced turn off in a conventional PWM converter. However, as described in the next chapter, the tendency of the device to latch is removed in a zero current switching quasi resonant converter application. Hence the problems associated with device latching in a quasi resonant converter are minimized.

2.6 PARASITIC CAPACITANCES

Both in IGT and MOSFET the various parasitic capacitances are collected and identified under the following three quantities [3].

C_{iss} : Input capacitance with drain and source shorted.

C_{oss} : Common source output capacitance usually specified at V_{DS} = 25 V.

C_{rss} : Reverse transfer capacitance or gate to drain capacitance.

The typical values of these are given below. Both devices are rated at 450 V, 10 A.

	MOSFET	IGT/COMFET
	IRF-450	RCA IGT
C_{iss}	2000 pf	650 pf
C_{oss}	400 pf	230 pf
C_{rss}	100 pf	60 pf

As can be seen from the table. Input capacitance of IGT is significantly less than a comparable MOSFET. This is mainly due to smaller chip size of IGT.

Smaller parasitic capacitances places less demand on the gate drive circuit design. Also the lower output capacitance of IGT implies that at very high frequency high voltage switching circuits the loss due to this parasitic capacitance is lower thus reducing the overall device dissipation.

CHAPTER 3. RESONANT OPERATION OF IGT/COMFET

In the last chapter the IGT characteristics were briefly discussed from the point of view of its operation in pulse width modulated (PWM) circuits. Two characteristics, namely turn off current tailing and latching, have limited the operation of currently available IGT's to less than 50 KHz.

In this chapter IGT will be investigated from the point of view of resonant operation. The investigation will be focused on zero current resonant switching only. There are many power circuit topologies that utilize the concept of zero current switching. [5,6] Even though the circuit topology may be different, the stress on the switching device is the same. The discussion in this chapter will be focused on the stress of the device under resonant operation.

3.1 RESONANT CONVERTERS

At higher frequencies the physical weight and size of the over all size of the power converter is reduced. The upper limit for converter operating frequencies is set by heat generated by the individual switch [1]. In the resonant converters the switching takes place at zero current hence the switching losses are greatly reduced thus enabling higher operating frequencies [7]. There are basically two types of zero-current switching converters. One type is the parallel resonant converter (PRC)

and the series resonant converter (SRC) as shown in Fig. 3.1. The second type is the quasi-resonant resonant converters reported in [4]. A few of the circuits are listed in Fig 3.2. The switch current and the voltage waveforms for all of these converters, in full wave mode. If operated in a zero current switching mode, is as shown in Fig. 3.4. In the figure, I_m is the resonant current which is determined by the choice of resonant inductor L_r resonant capacitor C_r, and depending on circuit topology, by the source voltage or output voltage involve I_0 is the average current through the switch. One of the disadvantages of resonant operation is that the resonant current I_m is usually much larger than I_0. Therefore, the current peak of the device is usually much larger than the pulse-width modulated converter counterpart.

3.1.1 Conduction Losses

As mentioned earlier one of the disadvantages in the use of resonant converters, compared to PWM converters, is higher peak current and hence higher conduction losses. Referring to Fig. 3.4, I_m must be at least equal to I_0, to achieve zero current switching. In reality, however, I_m is three or four times of I_0. This results in a larger conduction loss, especially for majority carrier device such as MOSFET.

Two intrinsic characteristics of IGT make it possible to overcome these disadvantages when it is used in resonant converters. Due to the phenomenon of conductivity modulation, IGT can handle high peak currents for a given chip size and still maintain a low conduction voltage. This makes it ideal for handling high peak currents encountered in

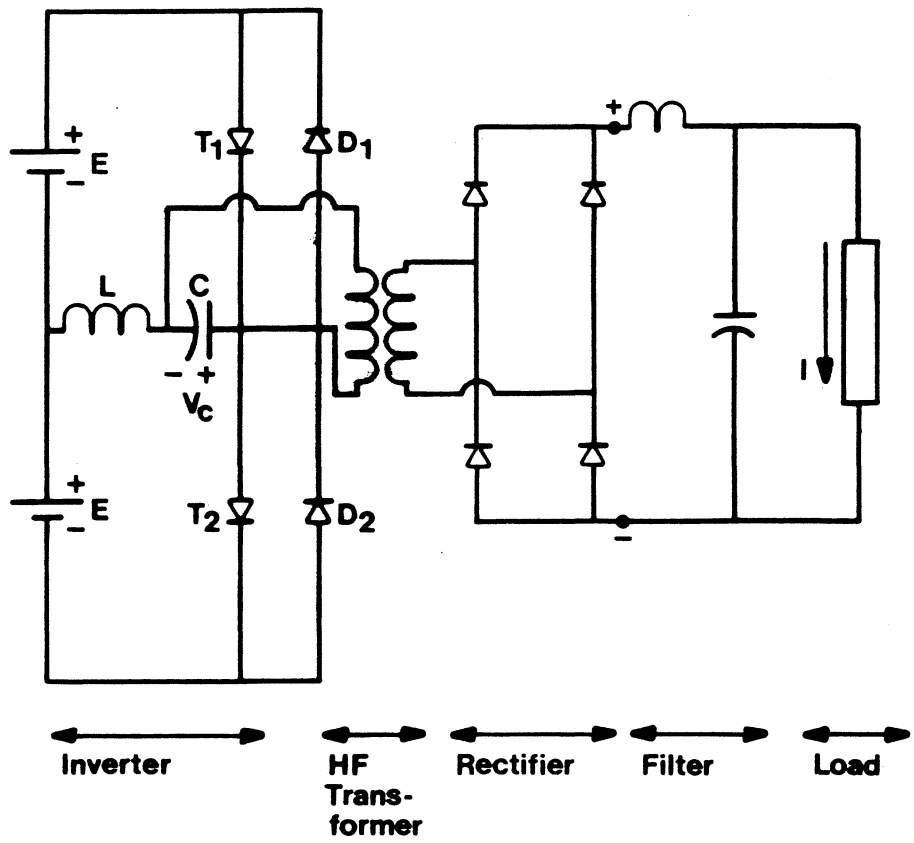


Figure 3-1. a) Parallel Resonant Converter

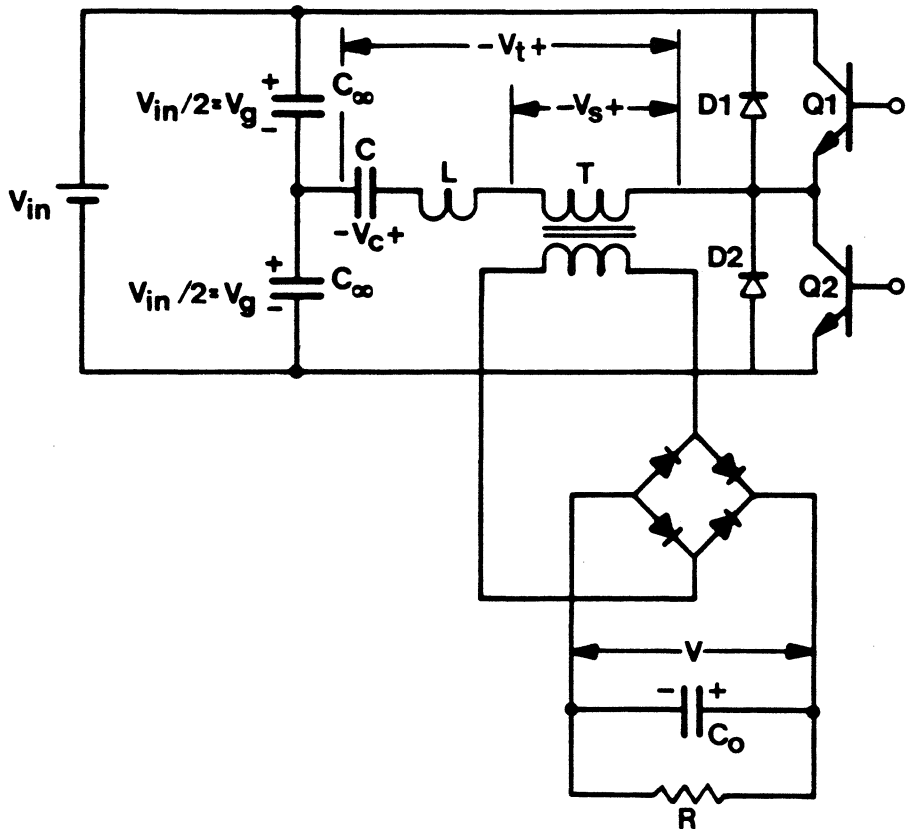


Figure 3-1. b) Series Resonant Converter.

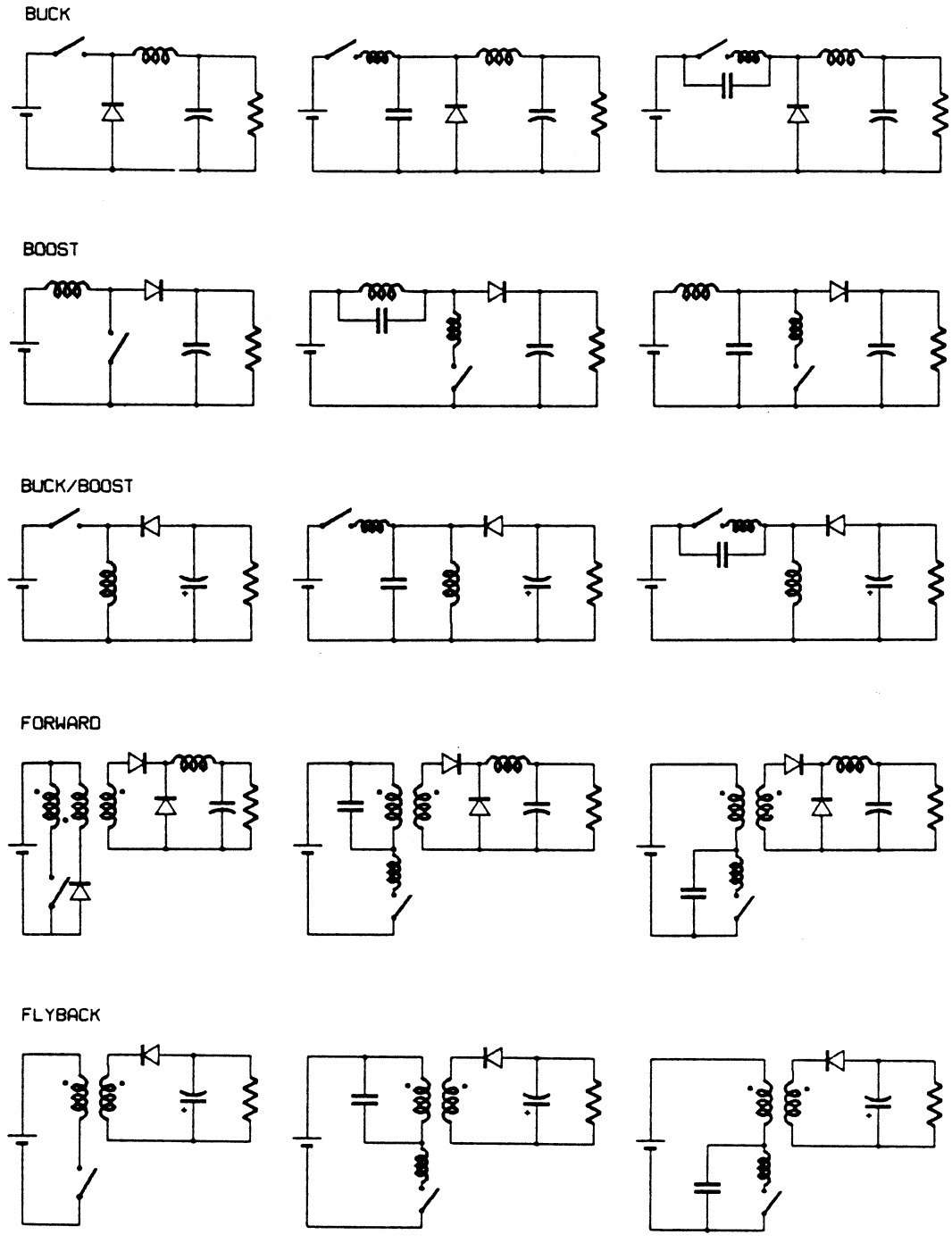


Figure 3-2. A Family of Resonant Switch Converters.

[See K. H. Liu et al. (7)]

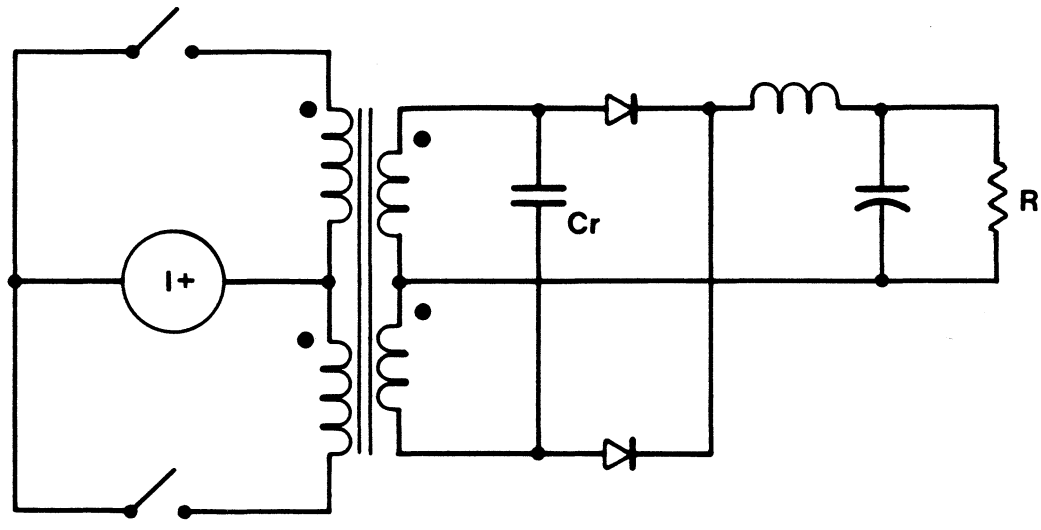


Figure 3-3. Push-Pull Quasi-Resonant Configuration.

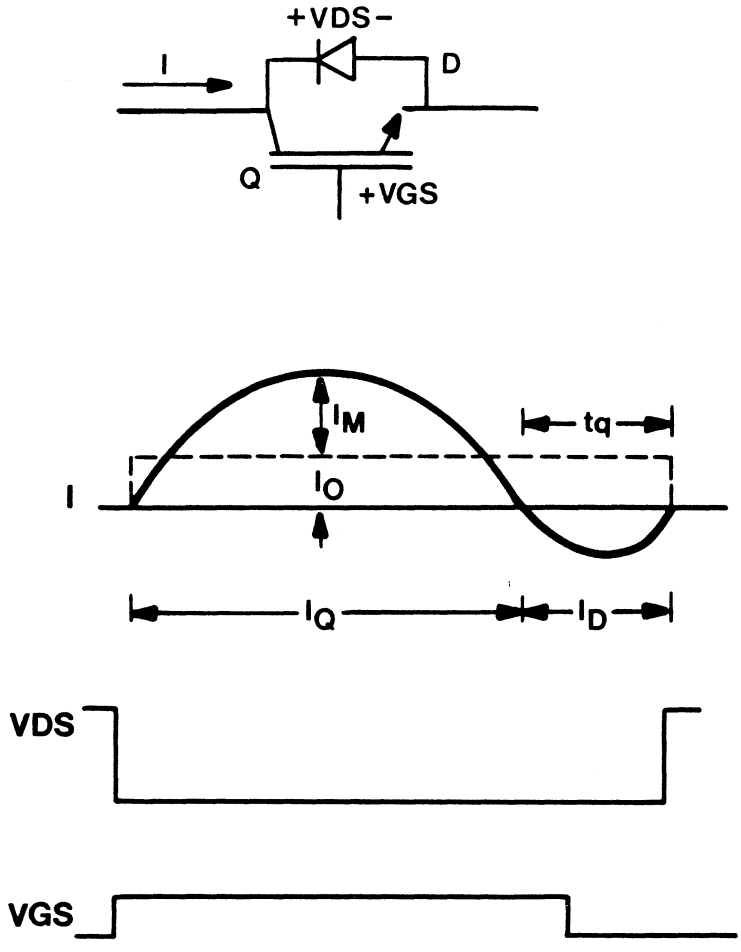


Figure 3-4. Transistor Current and Voltage Waveforms in a Resonant Operation.

resonant converters. As can be seen from Figure 2.3, for 400V, 10A devices, MOSFET has a conduction drop of 4.5V at 9A and IGT has 2.2V at 9A and the chip area of this particular IGT is only $\frac{1}{3}$' of the MOSFET.

3.1.2 Current Tailing

One of the major drawbacks in the use of IGT in high frequency (>50kHz) PWM circuits is its long current tailing time. This gives rise to considerable turn-off losses in a forced turn-off circuit waveforms operation shown in Figure 3-5. This is the main reason IGT cannot be used in high frequency PWM converter. In a resonant operation, however, the current is forced to be zero through circuit L-C resonance and the device turn off is accomplished at zero current.

This property of zero current turn off eliminates turn off losses when IGT is used as a switch. Hence the upper limit of switching frequency set by the device turn off losses due to current tailing is eliminated in a resonant operation.

3.2. DEVICE LATCHING

In the previous chapter the conditions under which an IGT latches were described. As mentioned, one of the circuit applications in which the occurrence of latching is common is the forced current turn off in a PWM. This in fact limits the frequency of operation of IGT in PWM application [5]. In a resonant type of operation the waveshape of the

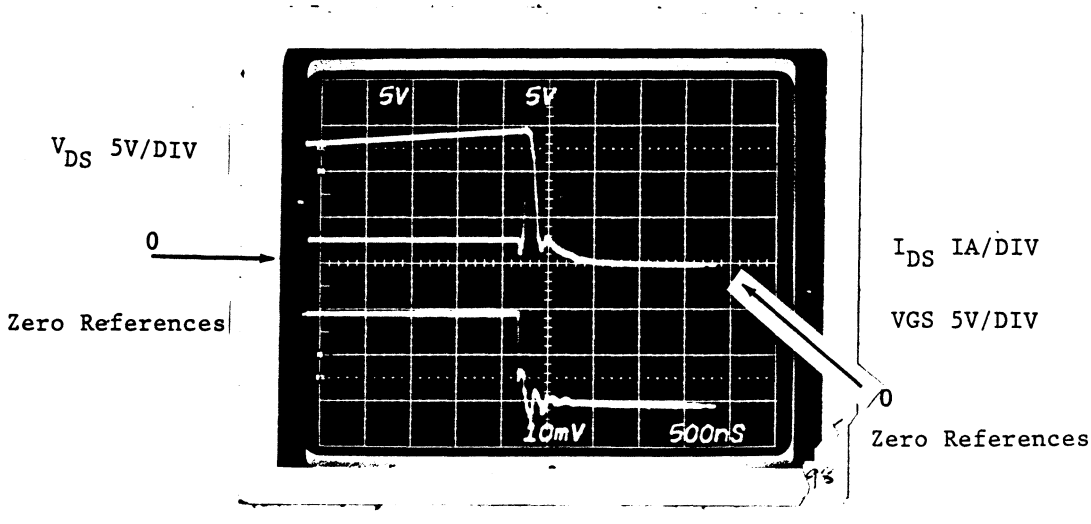


Figure 3-5. Forced Turn-Off Operation of IGT GE 4D10.

drain-source current of IGT is reduced to zero through LC resonance and will not constitute a condition for latching.

Another factor that might lead to the latching of IGT is high current magnitudes. Although high current magnitudes are common in resonant operation, it would not be a problem because if the device latches due to resonant high currents it would unlatch as the current is reduced back to the latching level. In fact, latching improved the conduction resistance because the SCR portion of the device contributes to conduction area.

3.3. RELATIVE IMPORTANCE OF DIFFERENT IGT CHARACTERISTICS IN RESONANT CIRCUITS

IGT has so far been used only in the frequency range of 50 KHz or below. Two main characteristics of IGT have been placed heavy restriction on PWM operation. These are the long tailing time and the tendency of IGT to latch under certain circuit conditions. The tailing is important because it contributes greatly to increased power dissipation in the device during turn off. Latching in many circuit application is very dangerous and could lead to catastrophic short circuit. But from the experimental results obtaining in resonant converters, it was observed that neither of these device characteristics limits the operation. Instead the two phenomena dv/dt effect and dynamic saturation played a major role in the operation of IGT at high frequency. This will be discussed in Chapter IV.

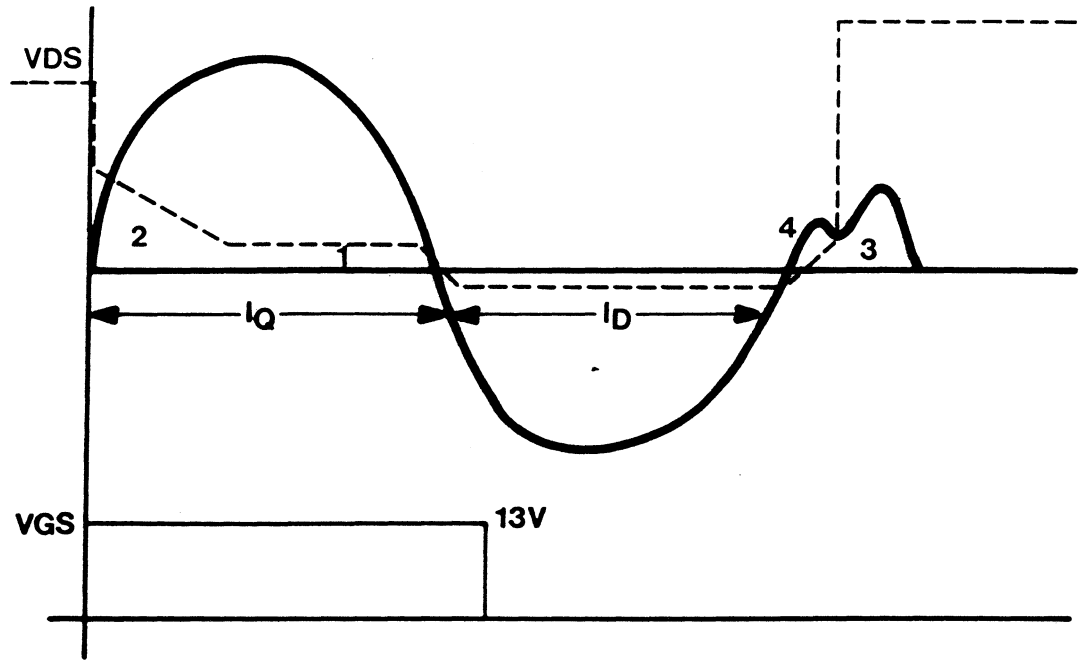
CHAPTER 4: VERY HIGH FREQUENCY OPERATION OF IGT

It was pointed out in Chapter III that resonant operation of IGT devices alleviate problems associated with the device, such as turn-off current tailing and the possibility of latching. Therefore, IGT can be operated to very high operating frequency (>100 KHz). However, as frequency goes up to hundred kilohertz range, many secondary characteristics of the device surface, and become on predominant consideration. It is the purpose of this chapter to point out such high frequency characteristics of the device.

An estimation of various power losses under different frequencies will be summarized. Comparison with MOSFET power losses will also be included. Four loss characteristics will be discussed:

1. Turn-on "dynamic" saturation loss
2. dv/dt loss
3. Reverse conduction characteristics
4. Parasitic Capacities Losses.

These are shown in Figure 4-1.



SOURCES OF POWER LOSSES

1. **Conduction Loss**
2. **"Dynamic Saturation" Loss**
3. **dv/dt Loss**
4. **Anti-parallel diode Reverse Recovery Losses**
5. **parasitic Capacitive Losses**

Figure 4-1. Sources of Power Losses

4.1. TURN ON DYNAMIC SATURATION IN IGT

Dynamic saturation is a phenomenon associated with the turn-on process in a high-voltage bipolar transistor. This term is used here to describe a similar phenomenon in an IGT even though the causing mechanism is different. Figures 4.2 and 4.3 show such phenomenon for different circuit conditions and devices. As can be seen from these oscillograms, it takes the drain-to-source voltage a significant amount of time to drop to a normal conduction voltage at turn-on. This is due to the forward recovery time of the P-I-N diode in the IGT structure. The duration and magnitude of the dynamic saturation depends on device design and circuit operating conditions. The larger the di/dt at turn-on, the larger is the dynamic saturation voltage drop.

4.1.1. di/dt Effect On Dynamic Saturation

Experiments show that there is a strong relationship between the duration of dynamic saturation and initial rate of rise of current through IGT. The smaller the di/dt, smaller the value of $V_{saturation}$, the initial drain-source voltage at turn on and consequently smaller the loss due to dynamic saturation. Figure No. 4.4, 4.5, 4.6 show the relationship between di/dt and the dynamic saturation voltage.

In a resonant converter, as the operating frequency goes higher, di/dt also becomes larger, (for the same device peak current). The dynamic saturation loss therefore increases rapidly with frequency.

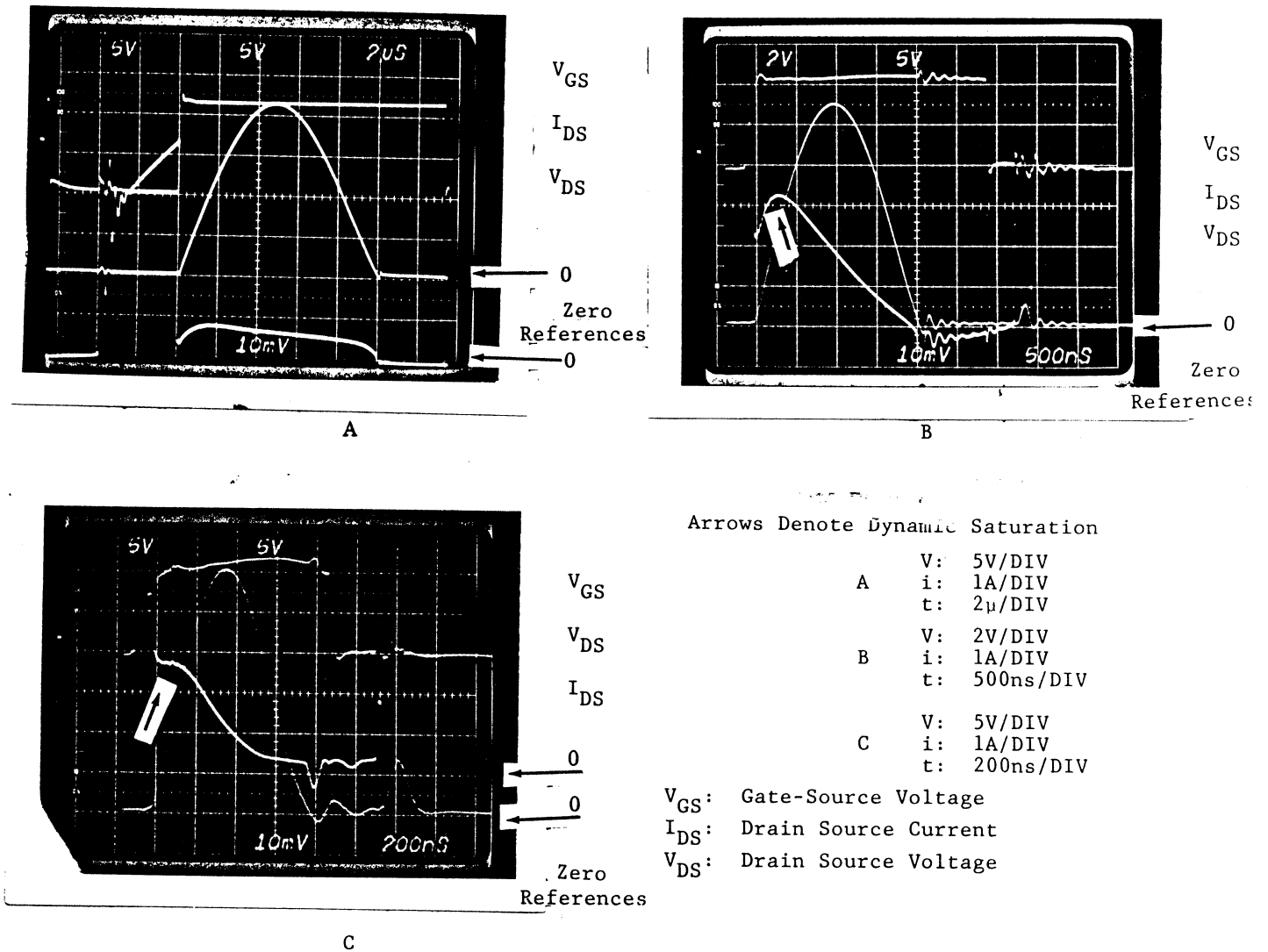
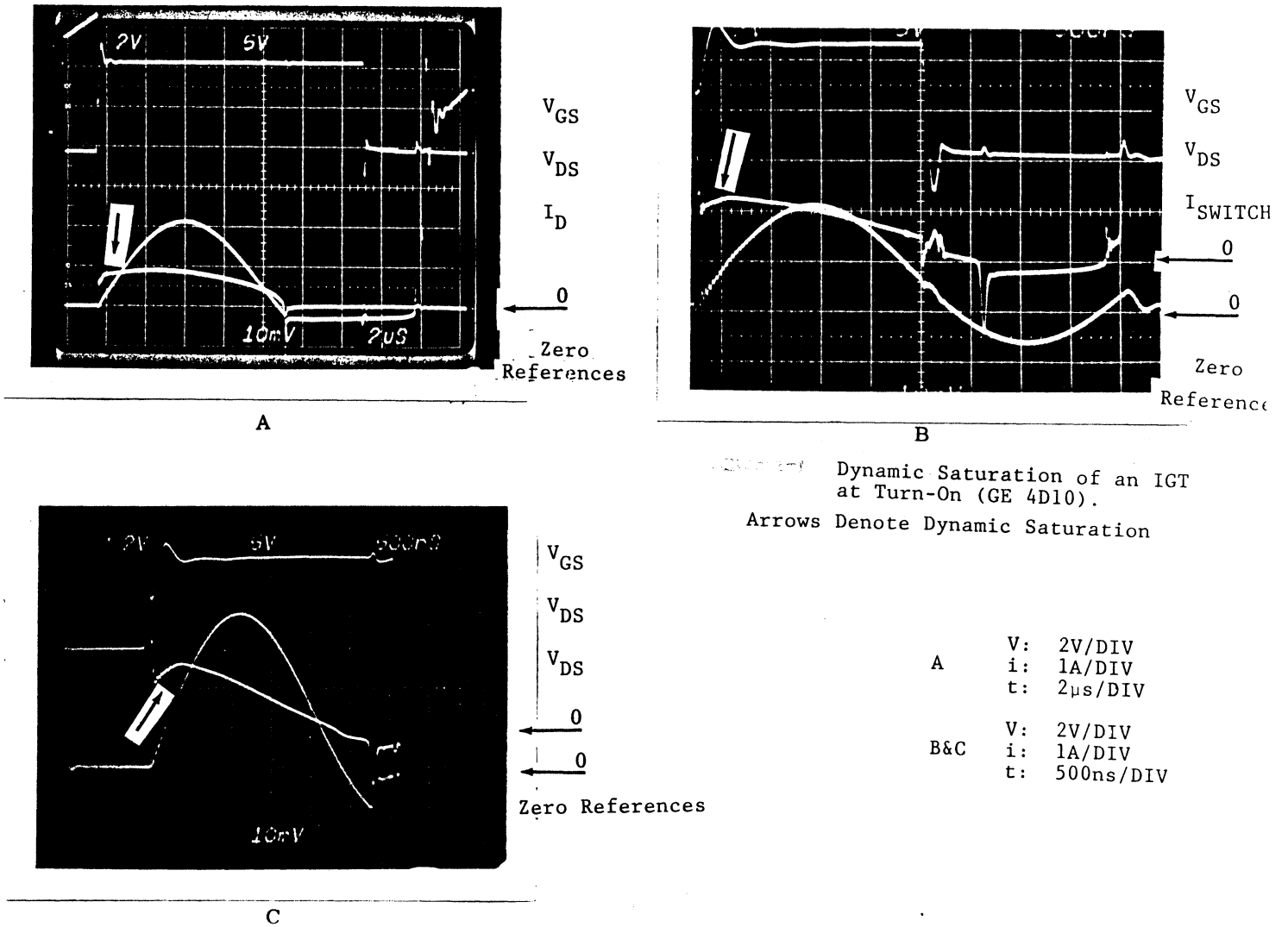


Figure 4-2. Dynamic Saturation of a COMFET at Turn-On (RCA Device).

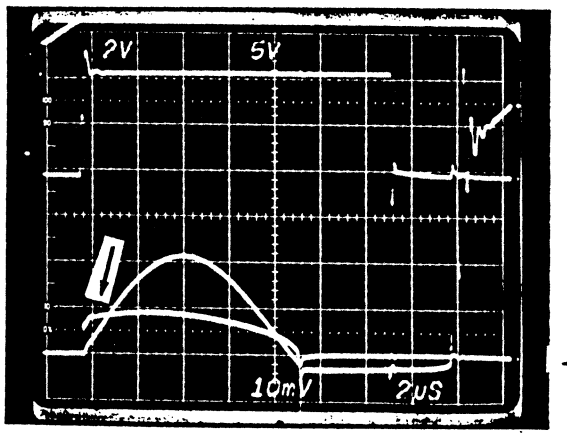


Dynamic Saturation of an IGT at Turn-On (GE 4D10).

Arrows Denote Dynamic Saturation

A	V:	2V/DIV
	i:	1A/DIV
	t:	2μs/DIV
B&C	V:	2V/DIV
	i:	1A/DIV
	t:	500ns/DIV

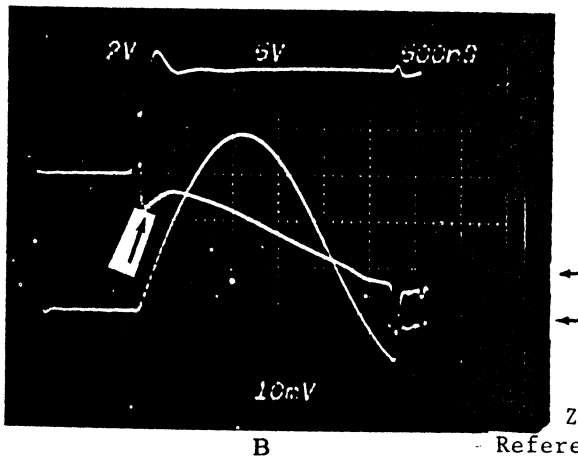
Figure 4-3. Dynamic Saturation of an IGT at Turn-On (GE 4D10).



V_{GS}
V_{DS}
I_D

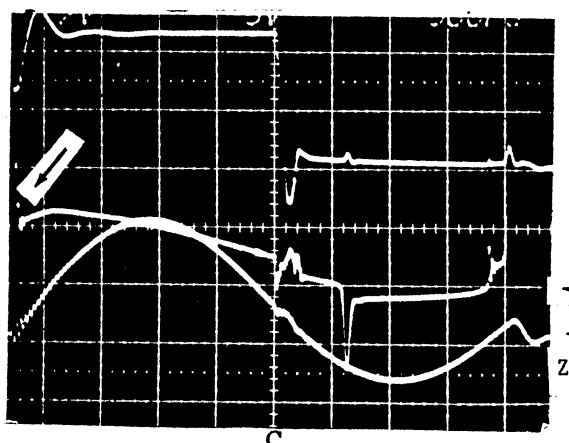
0 Zero References

Figure 4-4. Dynamic Saturation at Low Frequency (50 KHz)



V_{GS}
V_{DS}
I_{DS}
0
0
Zero References

Figure 4-5. Dynamic Saturation at Medium Frequency (150 KHz)



V_{GS}
V_{DS}
I_{SWITCH}
0
0
Zero References

Figure 4-6. Dynamic Saturation at High Frequency (500 KHz) (IGT 4D10)

A	V:	2V/DIV
	i:	1A/DIV
	t:	2μ/DIV
B&C	V:	2V/DIV
	i:	1A/DIV
	t:	500ns/DIV

Arrows Denote Dynamic Saturation

4.1.2. Gate Voltage Effect

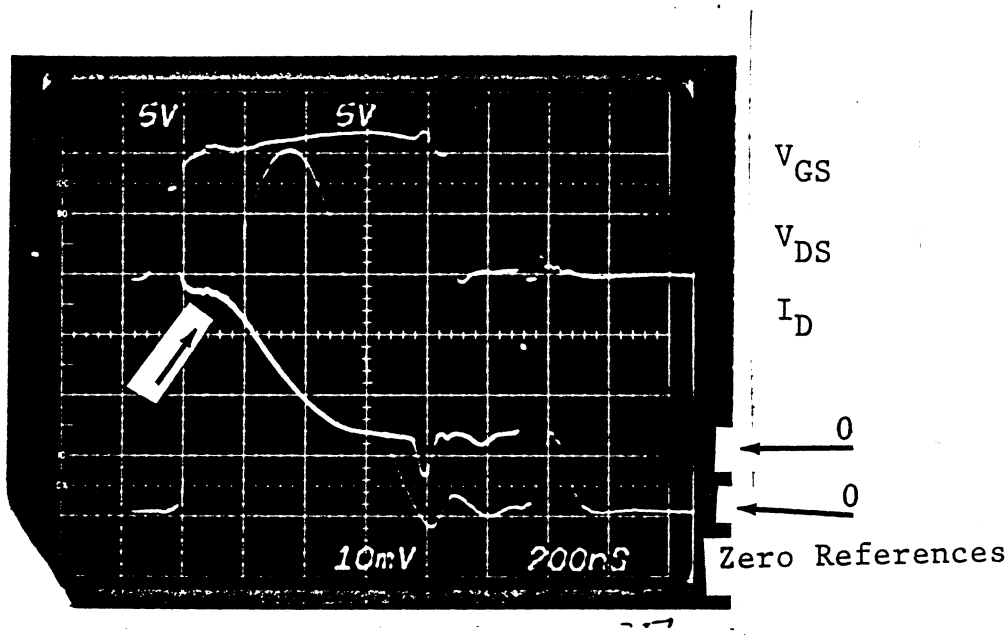
The dynamic saturation voltage drop is made even more pronounced if the turn-on of the gate is slow relative to current rise. However, even if the gate turn-on is fast, the phenomenon is still very pronounced at high frequency. It can be seen from Figure 4.6 that, the drain-source voltage is still around 8 volts even after gate-source voltage has already reached around 15V.

4.1.3. Effects of Device Turn-Off Speed on Dynamic Saturation

The dynamic saturation effect was common to both slow and fast IGT's. Fig. 4.6, 4.7 show the behavior of both slow and fast IGT's respectively. This phenomenon is common to both fast and slow IGT's.

4.2 DIODE RECOVERY LOSS

In a full-wave resonant switch, the current in the switch flows in both directions. At the end of diode conduction, however, the transistor is cut off due to the gate signal and the resonant current flows through the diode in reverse direction which forces the reverse recovery of the diode. This loss can becomes significant at very high frequencies. More importantly, the diode reverse characteristics affect the dv/dt loss of IGT to be discussed in the following section.



i: 1A/DIV

t: 200ns/DIV

Figure 4-7. Dynamic Saturation in Fast IGT (RCA DEVICE)

Arrows Denote Dynamic Saturation

4.3 dv/dt LOSS

In resonant operation, at the end of the reverse-recovery phase of the diode, the device voltage starts to rise. The dv/dt, caused by diode recovery, induces a current spike in the IGT device which leads to a power loss. The magnitude of the current spike depends on the amount of charge still stored in the IGT at this instant.

The slower the device and/or the higher the resonant frequency, the worse the current spike will be. In fact, the time duration between when the current starts conducting in the anti-parallel diode and the instant the diode reverse recovery ends is similar to t_q of an SCR. The "reapplied dv/dt" capability of an SCR is intermittently related to t_q. In the case of a IGT, three factors are involved in determining the dv/dt current spike. On factor is the dv/dt caused by the "softness" of the diode and the di/dt of the resonant current at zero crossing. The other factor is the device recombination rate and the third factor is the time t_q determined by circuit operating conductions. The diode shown in Figure 4.8 shows that reverse recovery generates a large dv/dt and Figure 4.9 shows dv/dt causes a large current spike in the IGT.

4.3.1. dv/dt-Induced Turn-on in Slow Device

When a slow IGT is used in a high-frequency resonant circuit, the device could be never really turned off even though it goes through zero-current reversal. This is because of the current spike generated by dv/dt generates certain amounts of charge in the device which can only be reduced to zero by recombination, much like forced turn-off.

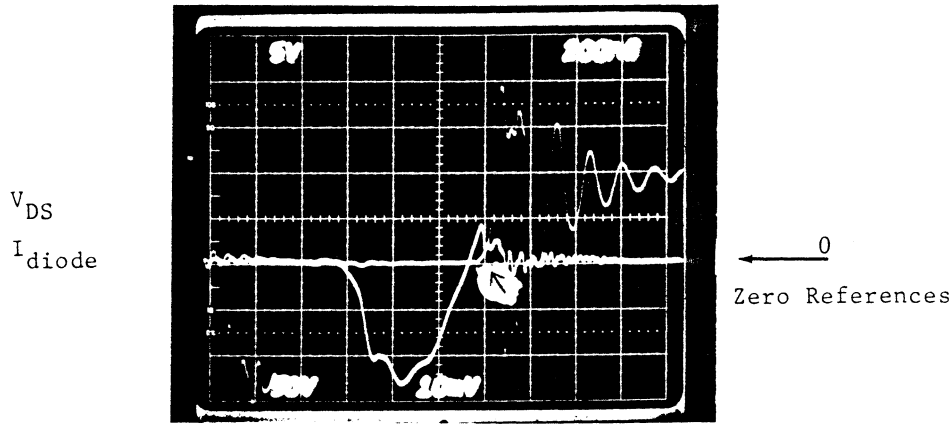


Figure 4-8. Diode Reverse Recovery and Generated dv/dt (RCA COMFET)

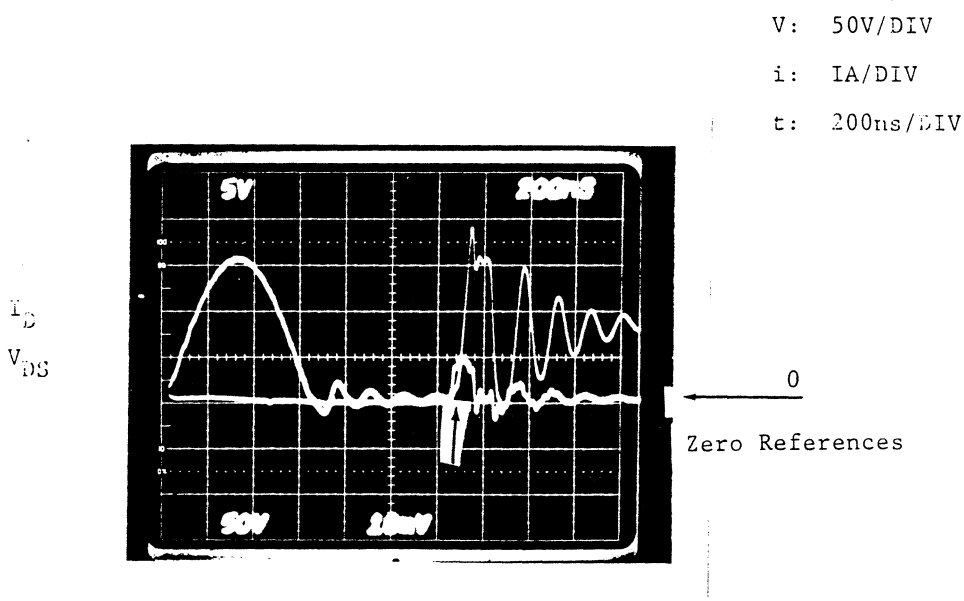


Figure 4-9. dv/dt Generated Current Spike in COMFET (RCA).

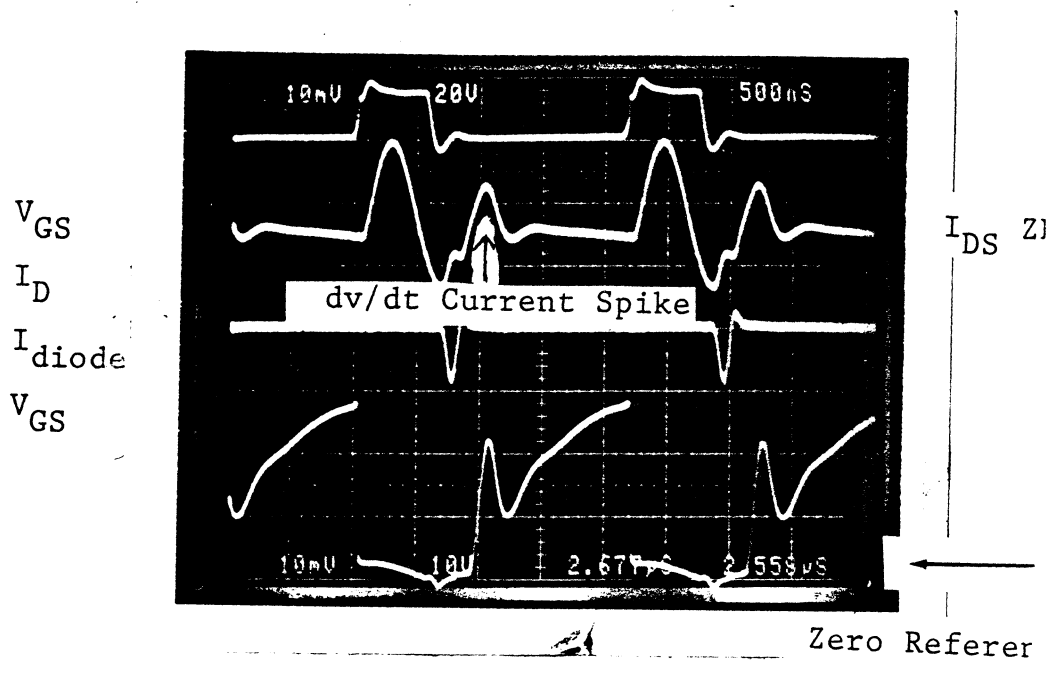
Since the frequency is so high the charge never reduces to zero before the device is turned-on again. Figure 4.10 show waveforms under such a condition. This condition sets another limit on the high frequency operating capability of IGT.

4.4. REVERSE CONDUCTION OF IGT

IGTs do not conduct reverse current in a static condition because of the junction J_2 in Fig. 2.1 is reverse biased. In a resonant operation, however, at the current reversal of the IGT, charge is still stored in the device and therefore device conducts reverse current. This is mostly pronounced in a slow IGT because of large stored charge and relatively show recombination rate. Fig. 4.9 shows such effect. From the figure, it can be seen that the reverse current flows through IGT in the beginning until the stored charge is depleted. The anti-parallel diode starts conducting afterword.

4.5. CAPACITIVE LOSSES

Charging and discharging the device parasitic capacitance are necessary to switch the IGT. The parasitic capacitances of an IGT is inherently smaller than an similarly rated MOSFET because a smaller chip area required. The typical capacitance values of 400 V, 10 A devices are given below:



V_{GS}: 20V/DIV

V_{DS}: 100V/DIV

i: 0.5A/DIV

t: 500ns/DIV

Note: IGT DOES NOT TURN OFF IN THIS FIGURE

Figure 4-10. Waveforms for Slow IGT.

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Table 4-1A. Summary of Device Power Losses at 50 KHz (Switching)

	GE IGT (4D10)	MOSFET (IRF450)
1. Conduction Loss	6.0 W	10.9 W
2. Dynamic Sat. Loss	2.4 W	-
3. Schottky Loss	-	1.8 W
4. Anti Parallel Diode Conduction Loss	0.3W	0.3W
5. Anti-Parallel Diode Reverse Rec. Loss	0.2W	0.2W
6. dv/dt Loss	Negligible	
7. Capacitive Loss	Negligible	
TOTAL	8.7 W	13.0 W

Operation Conditions

$t_{on}=45\%$ $f_r=60KHz$ $f_i=50KHz$
$V_{DS}=200V$ $I_n=7.5A$ $I_p=2.2A$

Table 4-1B. Summary of Device Power Losses at 150 KHz (Switching)

		GE IGT (4D10)	MOSFET (IRF450)
1. Conduction Loss		6.1W	10.9W
2. Dynamic Sat. Loss		6.0W	-
3. Schottky Loss		-	1.81W
4. Anti Parallel Diode Conduction Loss		0.11W	0.11W
5. Anti-Parallel Diode Reverse Rec. Loss		0.5	0.5
6. Capacitive Loss	C_{gs}	0.01	0.02
	C_{gd}	0.2	0.40
	C_{ds}	0.3	0.9
7. dv/dt Loss		1W	1.25W
	TOTAL	13.6	15.4 W

Operation Conditions

$I_m = 45\%$ $f_r = 180KHz$, $f_s = 150KHz$

$V_{DS} = 200V$, $I_m = 7.5A$, $I_o = 2.2A$

Table 4-1C. Summary of Device Power Losses at 250 KHz (Switching)

		RCA FAST IGT	MOSFET IRF450
1. Conduction Loss		4	6
2. Dynamic Sat. Loss		10.3	-
3. Schottky Conduction Loss		-	1.14W
4. Anti Parallel Diode Conduction Loss		0.2W	0.2W
5. Anti Parallel Diode Rev. Rec. Loss		0.65W	0.65
6. dv/dt Loss		3.12W	-
7. Capacitive Loss	C_{gs}	0.01	0.03
	C_{gd}	0.34	0.68
	C_{ds}	0.53	1.5
	TOTAL	19.0 W	9 Watts

Operation Conditions

$t_{on} = 30\%$, $f_r = 500KHz$, $f_s = 250KHz$

$V_{DS} = 200V$, $I_m = 10A$, $I_o = 3.3A$

Table 4-1D. Summary of Device Power Losses at 500 KHz (Switching)

		RCA FAST IGT	MOSFET IRF 450
1. Conduction Loss		4.W	6.W
2. Dynamic Sat. Loss		17.0W	-
3. Schottky Conduction Loss		-	1.0W
4. Anti Parallel Diode Conduction Loss		0.2W	0.2W
5. Anti Parallel Diode Reverse Rec. Loss.		2.5W	2.5W
6. dv/dt Loss		7.28W	
7. Capacitive Loss	C_{gs}	0.01475W	0.0475W
	C_{gd}	0.68W	1.33W
	C_{ds}	1.06	3.0
	TOTAL	32.6W	14.5W

Operation Conditions

$I_m = 30\%$, $F_R = 1MHz$, $F_s = 500KHz$

$V_{in} = 200V$, $I = 6.6A$, $I_o = 3.3A$

given in the Appendix. A G.E. IGT and a RCA COMFET were used. Both are fast switching devices with turn off time approximately 500 n.s.

Among the loss components, the dynamic saturation loss, the dv/dt loss and the diode reverse recovery loss have been discussed in Sections 4.2, through 4.5. These are the losses closely related to high frequency operation. The rest of loss components are not directly related to frequency and will be described in the following.

4.6.1. Conduction Loss

Figure 2.3 shows the I-V characteristics of a IGT/COMFET and a MOSFET. Both are 400V, 10A devices. It is noted that there is a forward threshold voltage (V_{DS}) of approximately 0.7V to keep IGT in conduction, which is not needed in a MOSFET. However, at high current levels, the conduction drop of a IGT is much smaller than that of a comparable MOSFET. The relative magnitude of the conduction loss and total losses depend on switching frequency, conduction duty cycle and the current level involved. As shown in Table 1A, B and C, the total losses is conduction loss at 50kHz. At 150kHz, the percentage of conduction loss drops to 50 and, at 500kHz, the percentage drops much further to about 15 .

4.6.2. Schottky Diode Loss

A series-connected Schottky diode is used to bypass the integral diode of the MOSFET. This is necessary to avoid a large diode reverse-recovery loss due to the slow recovery of the integral diode. Schottky diode conduction loss should then be included in a MOSFET converter. Since an integral diode does not exist in an IGT, there is no need to add a Schottky diode in IGT circuit.

4.6.3. Anti-Parallel Diode Conduction Loss

Diode conduction loss depends on diode current, diode conduction voltage drop and the diode conduction duty cycle. The diode duty cycle increases with a decreasing load. Even under open-load in which reverse current is as much as forward current condition diode conduction loss is still considerably less than transistor conduction loss because of small conduction voltage drop.

4.7. LIMITATION OF IGTS IN HIGH-FREQUENCY OPERATION

In a conventional PWM converter operation, turn-off loss of an IGT is the major portion of the total losses. This prevents the devices from being operated beyond the 50kHz range. Resonant operation enables the existing devices to be used beyond the 50kHz range. For very high-frequency applications, however, two limiting factors are identified. One severe limitation is the turn-on "dynamic saturation" loss. As can be seen from Table 4-B, this loss accounts for more than 50% of the total

device loss even at 150kHz. The other factor is related to the dv/dt current tailing indicated in Figs. 4.8 and 4.9. For a fast device, the loss associated with the phenomenon is not very significant as can be seen from Table 4-D even at 500 kHz operation. However, if the recombination time is too long relative to the operation period, the device may never turn off as shown in Figure 4.9. For this reason, even though resonant operation eliminates the turn-off loss of a slow IGT, a slow device is still not suitable for high frequency resonant operation. In the next chapter, suggestions will be made for device design changes for high frequency resonant operation.

4.8. CONCLUSION

It can be observed that both slow and fast IGTs exhibit turn on dynamic saturation when operated in zero current switching operation. Also two high frequency characteristic namely dv/dt induced current and Chynami saturation become of predominate consideration. Different losses which take place in the switch are tabulated for different frequencies comparison with MOSFET power losses are given IGTs are susceptible to latching under high dv/dt. When a slow IGT is operated at very high frequency it exhibits reverse conduction.

CHAPTER 5: SUGGESTIONS FOR DEVICE DESIGN MODIFICATIONS

In this chapter, IGT characteristics will be reviewed in view of the results obtained in Chapter IV. The device design practice of IGT is normally optimized for PWM operation. It is the intention of this chapter to point out some design trade-off of IGT for high frequency resonant operation.

5.1. DEVICE CONSIDERATIONS FOR RESONANT OPERATION

As mentioned in earlier chapters the problems associated with IGT device namely current tailing and latching etc. are alleviated when the device is used in resonant converter operation. There are new problems in high frequency resonant operation. They are dynamic saturation loss and stored charge or turn off time.

5.1.1. Dynamic Saturation

As it can be seen from the Tables 4-1A, 4-1B, 4-1C and 4-1D the loss in IGT due to dynamic saturation increases with frequency. Also at switching frequencies above 200 KHz, the dynamic saturation loss accounts for more than 50% of the total device loss. Hence any device design modifications must be aimed at reducing this loss.

5.1.2. Device Turn-on Process in IGT

The device structure of IGT is given again in Figure 5-1. The device is turned on when the MOS gate is given a positive bias with respect to the source and the drain is positive to the source. The forward gate source voltage inverts the p-doped base region immediately below the oxide and J_2 junction is forward biased and the device conducts with the n^- region conductivity modulated. A turn on delay time exists due to a combination of the delay to charge input capacitance and the forward recovery time of a P-i-n diode. The rise time is due to the rise time of the p-i-n diode. Dynamic saturation is believed to be caused by the minority carrier transit time t_b in the n^- epitaxial layer of the device. [9]

$$t_b = \frac{W_n^2}{4\,Dp} .$$

where W_n is the thickness of the n^- region and Dp is the diffusion constant of holes in the n^- region.

5.1.3. Methods to Improve Transit time

Reduction of W_n

As can be seen from the equation for transit time reduction of thickness of n^- epitaxial region would reduce the transit time and hence would reduce the dynamic saturation loss. But the thickness of n^- region is directly related to the voltage blocking capability of IGT. However

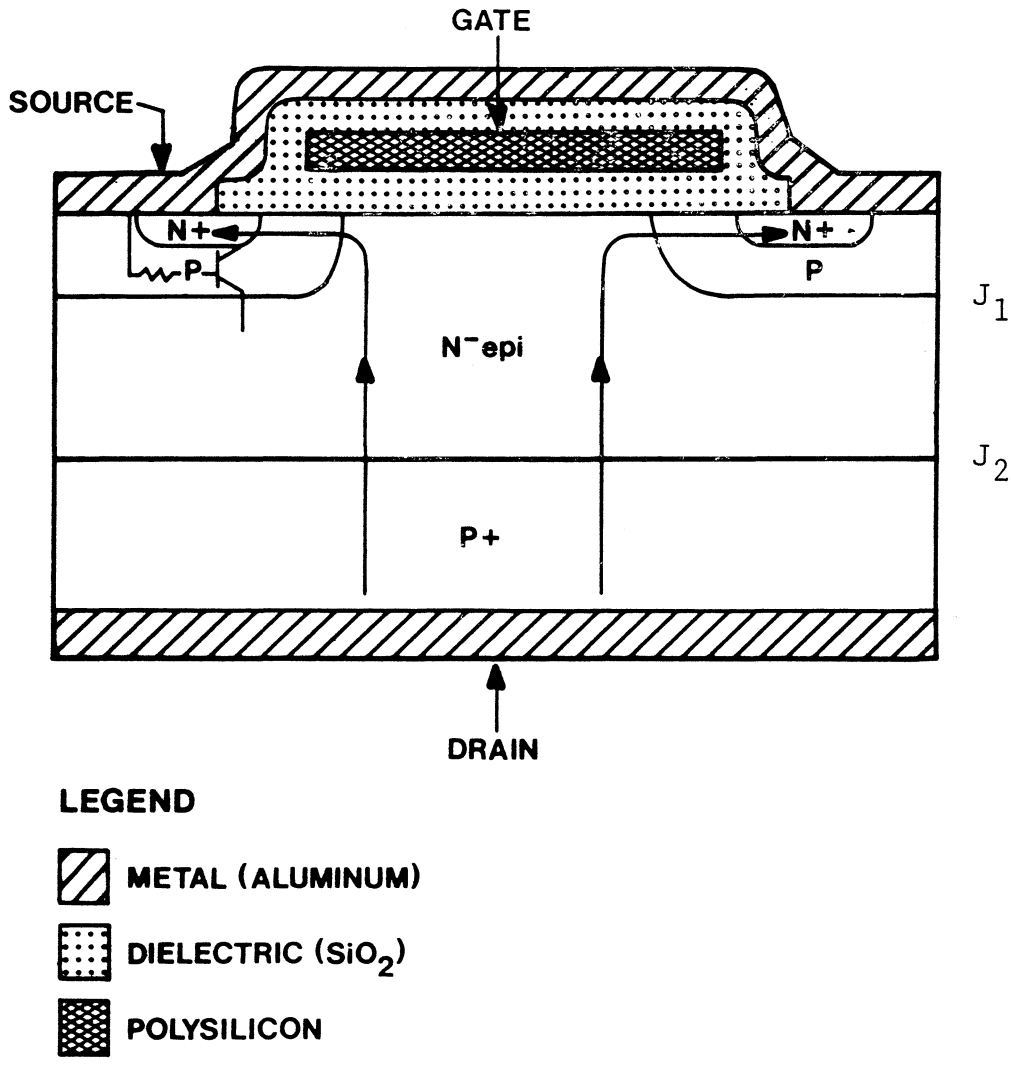

Figure 5-1. Device Structure of IGT.

in a normal device design, the thickness of n^- epitaxial region is over designed to obtain a good Reverse Bias Safe Operating Area (RBSOA). As an example for a IGT rated at 400 V, W_n of approximately 10 μm is adequate. But in order to improve their RBSOA IGT is designed to have 50 μm of W_n.

In a resonant operation the switch current is naturally commutated to zero. Hence RBSOA is not a concern. Therefore the thickness of n^- layer can be drastically reduced to improve dynamic Saturation loss without affecting any major operating characteristics.

Also the reduction of n^- region thickness would improve the conduction resistance and the current tailing at turn-off.

Use of P channel IGT

Since the electron mobility is three times higher than the hole mobility election diffusion constant D_n is approximately three times the hole diffusion constant Dp.

$$t_b = \frac{W_p^2}{4 D_n}$$

Therefore the transit time of a P-channel device is smaller compared to that of an N-channel IGT.

But in a P-channel IGT the conduction resistance is slightly higher than that of a N-channel device. However as can be seen from the results of operation of IGT in high frequencies (over 200 KHz) the reduction in

dynamic saturation loss would more than offset the increase in conduction loss due to the use of a P-channel IGT.

5.1.4. Dynamic Saturation in PWM Converters

It has been shown that when an IGT is used in PWM converts during the turn on process dynamic saturation is exhibited.

Figures 5-2, 5-3 and 5-4 show the turn on wave forms of three different IGT's when used in PWM converters. It can be seen that there exists a time during which the V_{DS} remains quite high compared to the normal conduction voltage level.

It is to be noted that these dynamic saturation voltage levels correspond to the resonant operation when di/dt of the initial currents are the same.

This again emphasis the strong relationship between initial di/dt and the dynamic saturation voltage level.

Hence to improve the high frequency performance of an IGT in resonant operation the dynamic saturation loss must be reduced two possibilities are suggested. One is to reduce the thickness of an n^- epitaxial layer and the other is rise of a P-channel IGT. Both would lead to a shorter minority carrier transit time and a smaller dynamic saturation loss.

5.1.5. Turn-off time

To reduce the turn off time through irradiation, the conduction drop is increase. It is true that in the resonant operation turn off time is

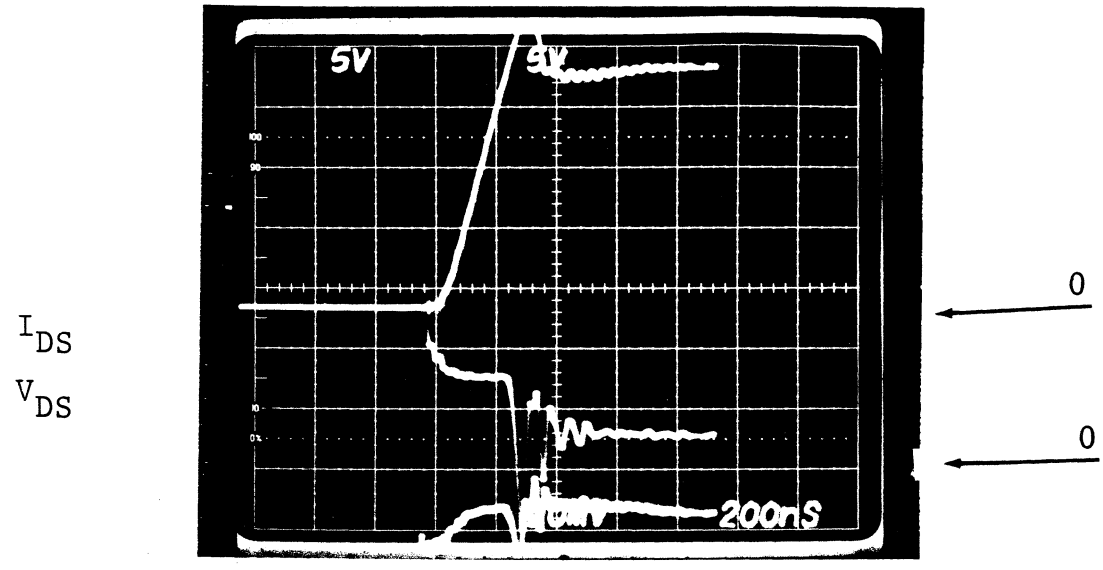

Figure 5-2. Dynamic Saturation in PWM Operation Turn-On GE Fast IGT.

Vertical: Voltage 5V/DIV
Current 1A/DIV

Horizontal: 200ns/DIV

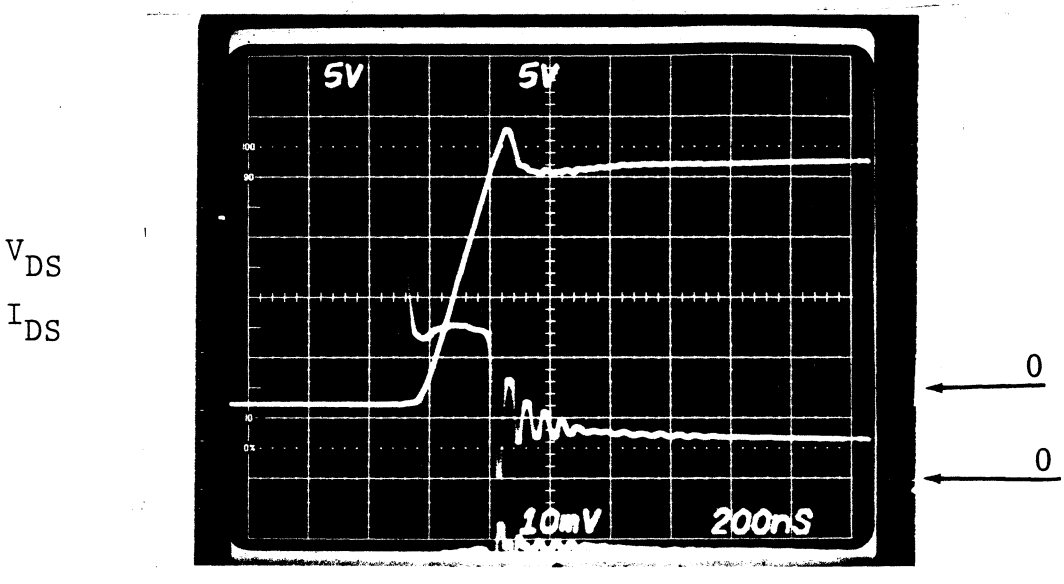

Figure 5-3. Dynamic Saturation in PWM Operation Turn-On RCA Slow IGT (4D10).

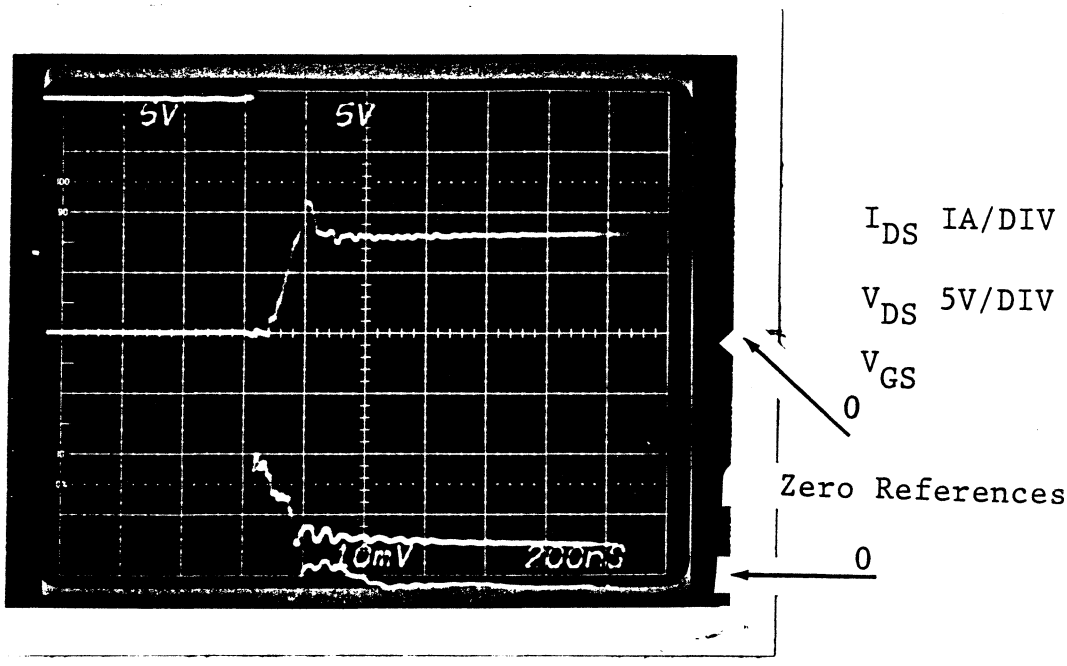

Figure 5-4. Dynamic Saturation in PWM Operation Turn-On GE Slow IGT (4D10).

not too critical. But it should be still short enough that the device will turn off after the resonant current has gone to zero.

It is shown as in Figure 4.10 that when a slower IGT is operated in a fast circuit it never turns off. After the resonant current has gone to zero it reverses and normally flows through the anti-parallel diode. But since IGT did not turn off it carries the major portion of the anti-parallel diode current.

Hence this is the other major limitation for use of IGT in resonant circuits.

CHAPTER 6. CONCLUSION

The following conclusions are reached from the present research.

1. Resonant operation does alleviate the problems associated with IGT/COMFET device used in conventional PWM converters. The problem associated with forced turn-off current tailing and the possibility of device latching do not exist in a quasi-resonant zero current switching operation. For these reasons the device can be operated at very high frequency if a zero current quasi-resonant converter circuit is used.
2. In the present research effort, the devices have been operated from 100 KHz to 500 KHz in a zero-current quasi-resonant converter. Loss comparison was made between an IGT/COMFET and a MOSFET for the frequency mentioned above. The comparison depends on the conduction current level, the switching frequency, and the source voltage level. AT 7A peak conduction current, 200 KHz switching frequency and 200 V source voltage, the power losses of IGT/COMFET is about the same as that of a comparable MOSFET. It should be noted that both the IGT and the MOSFET used in this comparison are rated at about 400 V, 10 A. The chip area of the MOSFET is about three times larger than the IGT. This particular IGT is a fast device with turn-off time of 0.5 μ.s..

In general, as conduction current level rises or as operating frequency reduces or as the voltage level increases, the balance will be tilted in favor of IGT/COMFET.

3. With the existing device design, there are several limiting factors for the use of IGT above 200 KHz quasi-resonant operation.

   a. Turn-on dynamic saturation loss is too high.

   b. Dv/dt induced loss at the end of reverse recovery of anti-parallel diode in the full-wave zero current resonant switch is too high. Dv/dt induces significant device current which tails off through recombination. If the operating frequency is high enough, the IGT may never turn off completely.

4. A device design change of IGT is necessary to reduce the dynamic saturation loss. One way is to reduce the thickness of n^- region of the device. A reduction in n^- region reduces the voltage rating. However, since the device is operated in zero current switching mode, the design consideration given to n^- region to increase RBSOA in a conventional practice is no longer needed. In other words, dynamic saturation loss becomes predominant consideration in very high frequency resonant operation and the RBSOA is no longer meaningful that n^- region thickness can be reduced.

   The other way of reducing dynamic saturation is to use p-channel IGT. The transit time can be reduced 2 to 3 times because

of the increase of carrier mobility in p-channel device in the epitaxial layer.

Both of the means to reduce dynamic saturation loss mentioned above are based on the assumptions that the transit time in the device n^- region is the cause of dynamic saturation. No experimental proof has been accomplished yet.

Suggestions for future research

1. Extend the research to other types of resonant switches including half-wave zero current switching and both full and half-wave zero voltage switching.
2. Dynamic saturation mechanism in IGT/COMFET device is not well understood. The period of the transit time of n^- region is believed to be the cause. However, the degree of dynamic saturation seems to be more severe in the resonant operation mode compared to the PWM mode. The drain-source voltage takes longer to reach full conduction voltage level in a resonant operation mode. This is not well understood and further research is needed in this area.

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APPENDIX

Equations for Estimating Power Losses in IGT in High-Frequency Resonant Operation [10]

CONTENTS

1. Formula for calculation of conduction loss in IGT in resonant operation.
2. Formula for calculation of dynamic saturation loss in IGT for resonant operation.
3. $\frac{dv}{dt}$ loss in IGT derivation of formula.
4. Diode reverse recovery power loss formula.
5. RMS & average value of resonant current for MOSFET power loss calculations.
6. Complete calculations with details for Table III.

I. Conduction Loss In IGT For Resonant Operation

Figure 1 gives the current through IGT in resonant operation

Value of $t_{on} \cong \frac{\theta}{\omega}$

where $\theta = \frac{-z_s I_o}{V_s}$

$$\omega = \frac{1}{\sqrt{L_1 C_1}}$$

L_1 = Resonant Inductance

C_1 = Resonant Capacitance

$z_s = \sqrt{\frac{L}{C}}$.

I_o = Output Load Current

V_s = Input DC Voltage

f_s = Switching Frequency

The equation for current during this interval is given by

$$I(t) = I_o + (\frac{V}{z_s}) \sin \omega t$$

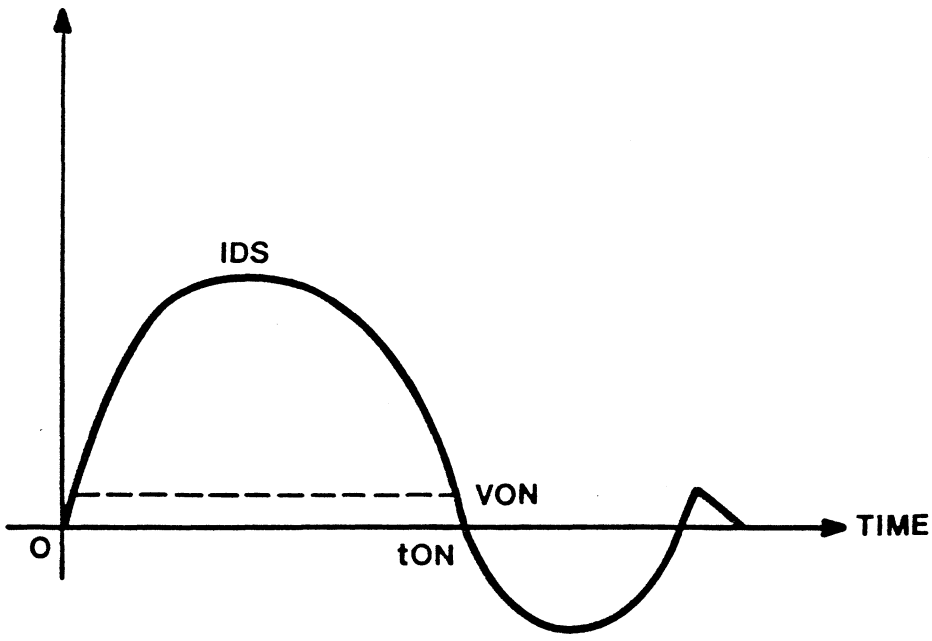


FIG. A-1

LEGEND

IDS: DRAIN-SOURCE CURRENT OF IGT

VON: CONDUCTION VOLTAGE OF IGT

tON: CONDUCTION PERIOD OF IGT

A-1. Conduction Loss in IGT.

(Note: The initial linear portion of current is ignored since its contribution to over all loss can be neglected.)

Let conduction loss = P_c

$$P_c = \{ \int_0^{t_{on}} V_{on}\left[I_o + \left(\frac{v}{z_s}\right) \sin \omega t\right]\}dt.f_s$$

$$= V_{on}\left[\int_0^{t_{on}} I_o dt + \int_0^{t_{on}} \left(\frac{v}{z_s}\right) \sin \omega t.dt\right] . f_s$$

$$= V_{on}.f_s\left[I_o t_{on} + \left(\frac{v}{z_s}\right)\left[- \frac{\cos \omega t}{\omega}\right]_0^{t_{on}}\right]$$

$$P_c = V_{on}.f_s\{I_o t_{on} + \left(\frac{V}{z_s}\right)\left[- \frac{\cos \omega t_{on} t}{\omega}\right]\}$$

where V_{on}, t_{on} are as shown in figure A-1.

II. Calculation of "Dynamic Saturation" Loss In IGT [11]

At typical $V_{DS(ON)}$ Voltage of IGT is shown in figure A-2. For the purpose of deriving equations straight line approximate are used

Some observation could be made about variables in figure A-2.

V_{sat} : As shown in Chapter IV two main factors determine value of V_{sat}.

1. The initial rate of rise of resonant current.
2. It is also determined by the method of manufacturing. (i.e) Different manufacturers' devices would have differnt V_{sat} for the same di/dt.

t_{fr} , t_{f2}: The duration of these vary with frequency. The trend being t_{fr} becomes longer with lower frequency and at low frequencies (around 50 KHz) these two points (t_{fr}, t_{f2}) coincide.

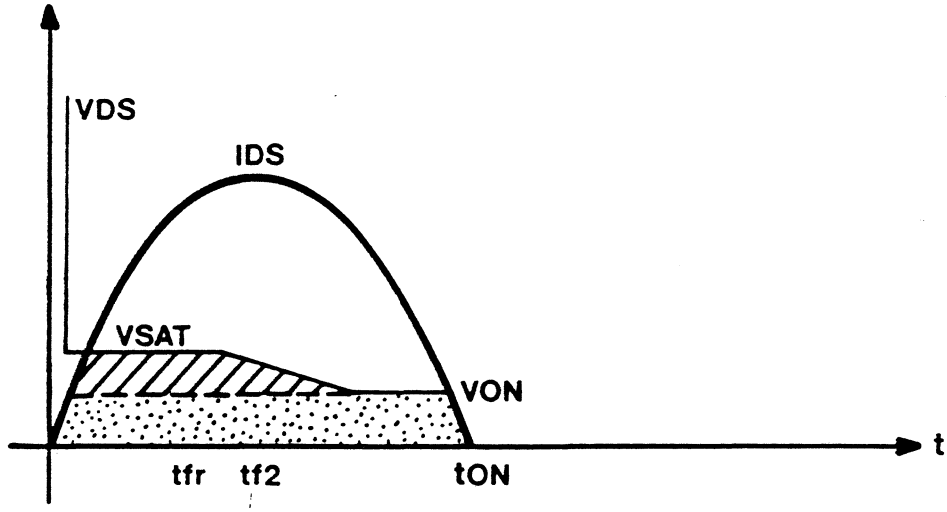


FIG. A-2

LEGEND

VDS: DRAIN SOURCE VOLTAGE OF IGT

VSAT: DYNAMIC SATURATION VOLTAGE LEVEL

A-2. Dynamic Saturation Loss in IGT.

Calculating Dynamic Saturation Loss

1. Loss due to constant voltage (approximately) portion of voltage.
2. Calculating loss due to the falling voltage portion of dynamic saturation loss.
3. To get dynamic saturation loss results from steps 1 and 2 are added and conduction loss is subtracted from it.

(i) Loss due to constant voltage portion of dynamic saturation loss

During this time we assume that $V_{DS(ON)}$ remains at V_{sat}. Recognizing that loss due to this voltage could be calculated in a manner similar to the conduction loss but with a different time duration.

If we use V_{sat} instead of V_{on} and t_{fr} instead of t_{on} in the formula for conduction loss we get

$$P_{D_1} = V_{sat} \cdot f_s \left[I_o t_{fr} + \left(\frac{V}{z_s}\right) \left[\frac{-\cos\omega t_{fr} + 1}{\omega} \right] \right]$$

(ii) Loss due to the falling voltage portion of Dynamic Saturation

Let P_{D_2} be the power loss during this duration

$$P_{D_2} = \int_{t_{fr}}^{t_{f2}} v.I.f.dt$$

$$= f \int_{t_{fr}}^{t_{f2}} \left[I_o + (\frac{V}{z_s}) \sin \omega t\right]\left[V_{sat} - (\frac{v_{sat} - v_{on}}{t_{f2} - t_{fr}})(t_{f2} - t_{fr})\right]$$

But for a given voltage and current waveform

$$\frac{V_{sat} - V_{on}}{t_{f2} - t_{fr}} \text{ is a constant.}$$

Let is be "K".

$$P_{D_2} = f \int_{t_{fr}}^{t_{f2}} \left[I_o + (\frac{V}{z_s}) \sin \omega t\right][V_{sat} - K(t_{f2} - t_{fr})]$$

$$= \int_{t_{fr}}^{t_{f2}} \left[I_o V_{sat} - I_o K(t - t_{fr}) + V_{sat}(\frac{V}{z_s}) \sin \omega t\right]$$

$$- K(\frac{V}{z_s}) \sin \omega t.(t_{f2} - t_{fr}).d$$

$$= \int_{t_{fr}}^{t_{f2}} I_o V_{sat} - I_o K t + I_o K t_{fr} + V_{sat}(\frac{V}{z_s}) \sin \omega t$$

$$+ K t_{fr}(\frac{V}{z_s}) \sin \omega t - K(\frac{V}{z_s}) \sin \omega t .$$

Integrating the above equation,

$$= I_o V_{sat}(t_{f2} - t_{fr}) - \frac{I_o K}{2}[t_{f_2}^2 - t_{f_r}^2]$$

$$+ I_o K\, t_{fr}(t_{f2} - t_{fr}) - V_{sat}\left(\frac{V}{z_s}\right)\frac{\cos \omega t_{f2} - \cos \omega t_{fr}}{\omega}$$

$$- K\, t_{fr}\left(\frac{V}{z_s}\right)\left[\frac{\cos \omega t_{f2} - \cos \omega t_{fr}}{\omega}\right]$$

$$- K\left(\frac{V}{z_s}\right)\left[\frac{1}{\omega^2}[\sin \omega t_{f2} - \sin \omega t_{fr}]\right]$$

$$+ \frac{1}{\omega}[t_{fr} \cos \omega t_{fr} - t_{f2} \cos \omega t_{f2}]$$

Note that when the above expression is multipled by the frequency of switching f_s we get P_{D_2}

Dynamic Saturation loss = $P_{D_1} + P_{D_2} - P_C$.

Since the formula is lengthy a HP 15C calculator program was used to evaluate it repeatedly.

III. Formula For Calculating dv/dt Loss In IGT

Equation of current in IGT for t=0 to t=tq/2 $= \left(\frac{IP}{tq/2}\right)t.$

Voltage across IGT during this period $= \left(\frac{V_{in}}{tq/2}\right)t$

Power loss during this period $= f_s \int_0^{tq/2} \left(\frac{IP}{tq/2}\right) t \left(\frac{V_{in}}{tq/2}\right) t$

$$= f_s \frac{4 V_{in} Ip}{tq^2} \frac{tq^3}{24} = f_s \frac{V_{in} I_p t_q}{6}$$

Equation for current from t = tq/2 to $t=t_q$ $= Ip - \left(\frac{Ip}{tq/2}\right)t$

Voltage across IGT during this period $= V_{in}$

Power Loss $= f_s \int_0^{tq/2} V_{in}\, Ip - \int_0^{tq/2} V_{in} \frac{Ip}{tq/2} t.dt$

$$= f_s \left[\frac{V_{in}\, Ip\, tq}{2} - \frac{V_{in}\, Ip\, tq}{4}\right]$$

$$\text{Total } \frac{dV}{dt} \text{ Loss} = \left[\frac{5\, V_{in}\, Iptq}{12}\right] f_s \quad \text{watts}$$

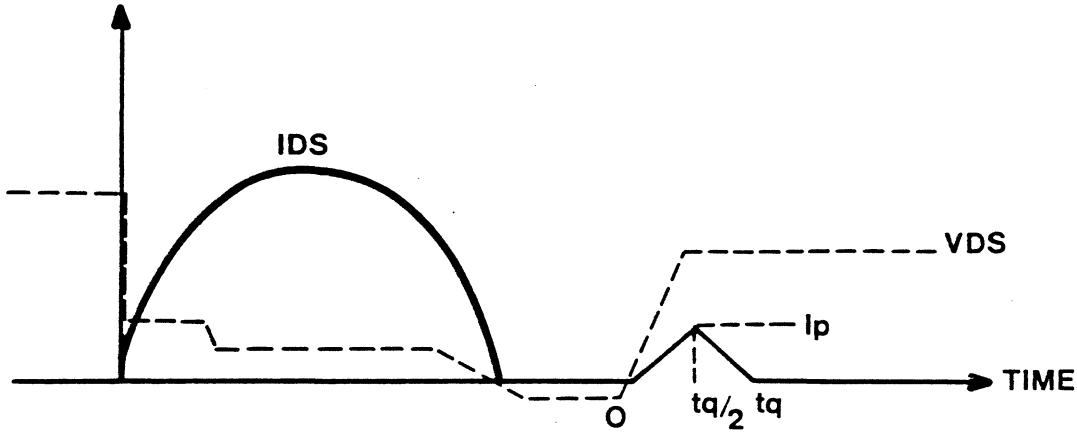


FIG. A-3

LEGEND

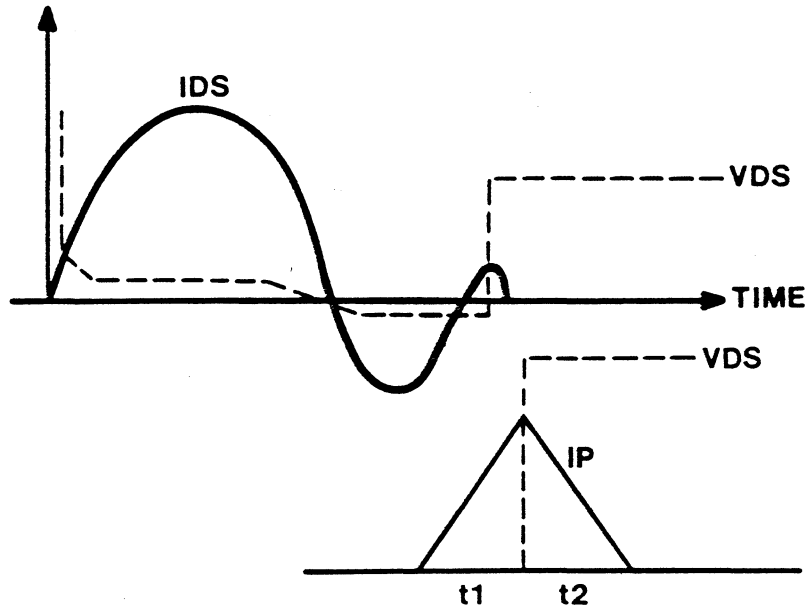
Ip: PEAK dv/dt CURRENT IN IGT

A-3. dv/dt Loss in IGT.

IV. Diode Reverse Recovery Loss [12]

From Figure A-4 the antiparallel diode reverse recovery loss

$$= \left[\frac{1}{2} \times t_2 \times Ip\, V_{in}\right] f_s \text{ watts}$$



A-4. Diode Reverse Recovery Loss.

V. RMS & Average Values of Resonant Current

The RMS value of the resonant current is used in calculating power loss in MOSFET's. The average value of current is used in calculating power loss in diode.

$$I = I_o + (\frac{V}{z_s}) \sin\theta .$$

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^{\theta} I_0^2 + (\frac{V}{z_s})^2 \sin^2\theta + 2(\frac{V}{z_s}) I_o \sin\theta - dt}$$

$$I_{RMS} = \sqrt{\frac{1}{T}\left[I_0^2\theta + \frac{1}{2}(\frac{V}{z_s})^2(\theta - \frac{\sin 2\theta}{2}) + 2 I_p I_o(1 - \cos\theta).\right]}$$

Here T is the total period with a given θ, the conduction angle and T, I_{RMS} could be calculated.

The average value of the current waveform is

$$I_{av} = \frac{1}{T}\int_0^{\theta} (I_o + (\frac{V}{z_s}) \sin\theta) d\theta.$$

$$I_{av} = \frac{1}{T}\left[I_o\theta + (\frac{V}{z_s})(1 - \cos\theta)\right].$$

VI. Detailed Calculation for Table III

Conductions for calculation

Resonant Frequency	=	200 KHz
Switching Frequency	=	100 KHz
Input Voltage	=	200 Volts
Peak Resonant Current	=	10 A
Output Current	=	3.3 A
t_{on}	=	30 percent

Conduction Losses

For IGT

We have the formula for conduction:

$$P_c = V_{on} f_s \left[I_o t_{on} + \left(\frac{V}{z_s}\right) \left[\frac{-\cos \omega t_{on} + 1}{\omega} \right] \right]$$

$$= 2 \times 100 \times 10^3 \left[3.3 \times 3 \times 10^{-6} + 6.6 \left[\frac{1.81}{2 \times \pi \times 200 \times 10^3} \right] \right]$$

$$= 4.0 \text{watts}$$

For MOSFET:

For I_p = 10A with a duty cycle = 0.3 we get I_{RMS} = 3.81A:

$$I_{RMS} = \sqrt{\frac{1}{T}\left[I_0{}^2\theta + \frac{1}{2}\left(\frac{V}{z_s}\right)^2\left(\theta - \frac{\sin 2\theta}{2}\right) + 2I_pI_o\,(1 - \cos\theta).\right]}$$

Here I_o = 3.3A

T = 2π

θ = 1.8 radians

I_p = 6.6A

Power Loss in MOSFET = $I^2_{RMS} \cdot R_{DS(ON)}$

= $(3.82)^2$ x 0.4

= 6 watts

Dynamic Saturation Loss For IGT:

The following are the variable values for dynamic saturation loss

t_{on} = 3 μsec

t_{fr} = 1 μsec

t_{f2} = 1.8 μsec

V_{on} = 2 Volts

V_{sat} = 6.5 Volts

f_s = 100 KHz

f_r = 200 KHz

Total Dynamic Saturation Loss = 8.61 watts
Conduction Loss = 4.01 watts

Dynamic Saturation Loss = 4.6 watts

Schottky Conduction loss:

Since $V_{(ON)}$ across schottky is -0.5 volts about $\frac{1}{4}$ across IGT

Schottky Conduction loss = $\frac{1}{4} \times 4.01 = 1$

Anti-Parallel Diode Conduction Loss:

Diode Conduction Loss = $V_{av} . I_{av}$

$$I_{av} = \frac{1}{4\pi}[I_p(1 - \cos\theta)]$$

I_p = 1A: θ = 160

I_{av} = 0.154 A

V_{on} = 0.7V

Power Loss = 0.11 watts

Anti Parallel Diode Reverse Recovery Loss

$$\text{Loss} = \frac{1}{2} \times t_2 \times I_p \times V_{in} \times f_s$$

$t_2 = 100 \times 10^{-9}$ sec

I_p = 0.1A

V_{in}= 200 V

f_s = 100×10^3 Hz

Loss = 0.1 watts

Capacitive Loss Calculations:

The different device capacitance are as follow:

	IRF 450	RCA IGT
Cgs	1900 pf	590 pf
Cgd	100 pf	60 pf
Cds	300 pf	170 pf

all values at 25V

Cgs Loss

$$\text{Cgs Loss} = \frac{1}{2} \text{ Cgs } Vgs^2 \ f_s:$$

For MOSFET

$$\frac{1}{2} \times 1900 \times 10^{-12} \times (100) \times 100 \times 10^3 = 0.0095 \text{ watts}$$

For IGT

$$\frac{1}{2} \times 590 \times 10^{-12} \times (10^2) \times 100 \times 10^3 = 0.00295 \text{ watts}$$

Note: Value of Cgs remains fairly constant over wide voltage range

Cgd Loss

$$C_{gd(LOSS)} = \left[\frac{1}{2} C_{gd(off)}\left[V_{DS(off)} - V_{GS(off)}\right]^2 + \frac{1}{2} C_{gd(on)} V_{gson}^2\right] f_s$$

For MOSFET

Given $C_{gd(25V)} = 100$ pf.

To get $C_{gd(200V)}$ we use C $\frac{1}{\sqrt{V}}$ approximation

$$(200V) = C_{25} \sqrt{\frac{25}{200}}$$

$$= 100 \sqrt{\frac{25}{200}} = 35.35 \text{ pf}$$

$$C_{gd(on)} = 3 C_{gd(off)} \qquad (13)$$

$$C_{gd(on)} = 300 \text{ pf}$$

V_{gson} = 10V

$$C_{gd(LOSS)} = (\frac{1}{2} \times 35 \times 10^{-12} \times 200^2) + \frac{1}{2} \times 300 \times 10^{-12} \times 10^2 \times 100 \times 10^3$$

= 0.071 watts

For IGT

Cgd(off 25V) = 60pf

$$Cgd(200\ V) = 60\sqrt{\frac{25}{200}} = 21\ pf$$

Cgd(on) = 180 pf

Cgd(LOSS) = 0.043 watts

Cds Loss:

$$Cds(Loss) = (\frac{1}{2} Cds(off) V_{DS(off)}^2 - \frac{1}{2} Cds(on)\ V_{DS(on)}{}^2) \cdot f_s$$

Since $V_{D(on)}^2 << V_{DS(off)}^2 \cdot f_s$ the second term can be neglected

$$Cds(LOSS) = \frac{1}{2} Cds(off)\ V_{DS(off)}^2\ f_s$$

For MOSFET

$$\text{Cds (200V)} = 300\sqrt{\frac{25}{200}} = 106 \text{ pf}$$

$$\text{Cds(Loss)} = \frac{1}{2} \times 106 \times 10^{-12} \times (200)^2 \times 100 \times 10^3$$

$$= 0.212 \text{ watts}$$

For IGT

$$\text{Cds(200V)} = 170\sqrt{\frac{25}{200}} = 60 \text{ pf}$$

$$\text{Cds(Loss)} = 0.12 \text{ watts}$$

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