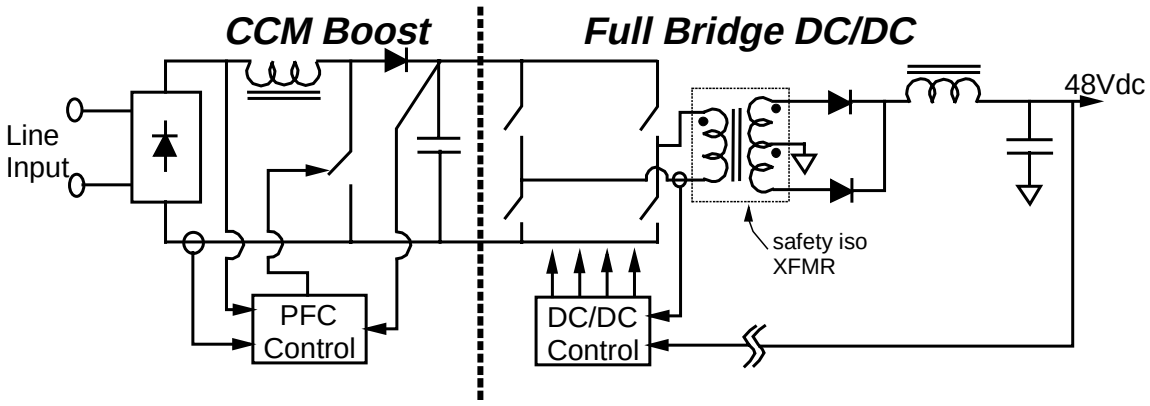
4. ACTIVE-CLAMP BOOST AS AN ISOLATED PFC FRONT-END CONVERTER

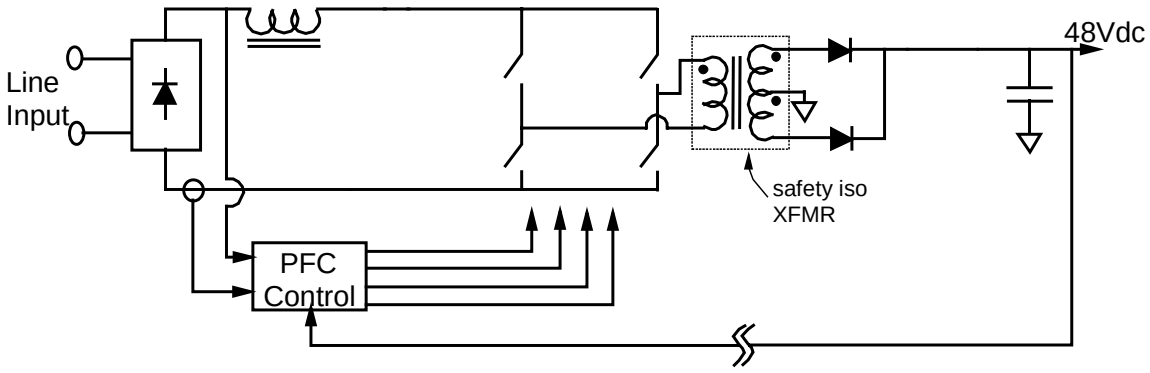
4.1 Introduction

This chapter continues the theme set by Chapter 3 - simplifying the standard two-stage front-end implementation to one that consists of just an isolated PFC converter. However, this chapter addresses this issue for higher power level system requirements.

As a starting point, shown in Fig. 4.1(a) is a typical, higher power output, two-stage front-end design topology. In Chapter 2, this design was simplified by incorporating secondary-side switching in the DC/DC converter. However, just as in Chapter 3, the "bulk" capacitor can be moved to the secondary, as shown in Fig. 4.1(b). Because kilowatt applications are being targeted, the full-bridge structure is maintained, and essentially replaces the PFC boost converter switch. Therefore, whatever the preferred PFC control method that is used in the two-stage approach is preserved in the implementation of Fig. 4.1(b). As with the front-end PFC flyback converter described in Chapter 3, the input line current's second harmonic is processed by the isolation transformer in the full-bridge boost converter shown in Fig. 4.1(b) and appears as voltage ripple on the output DC bus. However, the overall power stage design is much simpler, and, as will be experimentally demonstrated later in this chapter, this PFC implementation is more efficient than the two-stage circuit shown in Fig. 4.1(b).



(a) Topological concept of a traditional two-stage front-end design.



(b) Front-end consisting of an isolated boost PFC converter only.

Fig. 4.1 Two-stage and isolated boost PFC front-end conceptual designs.

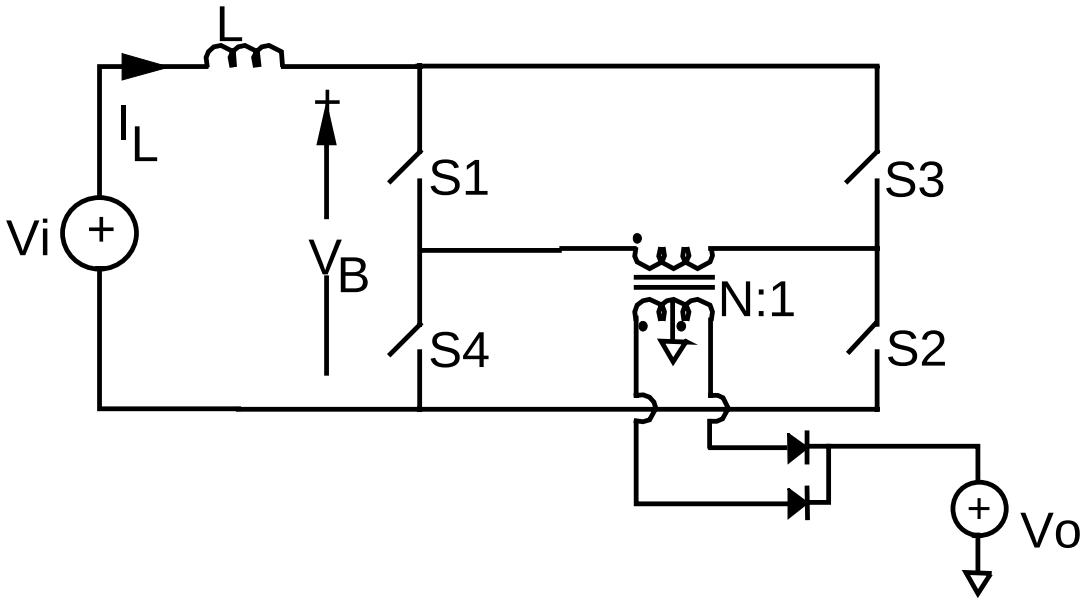
The full-bridge structure of the PFC boost converter's "switch" introduces the possibility of phase-shift control, in an analogous fashion to the phase-shift control used in voltage fed full-bridge converters. As will be discussed in the next section, phase-shifted control for the design shown in Fig. 4.1(b) can realize zero-current-switching (ZCS) for two of the four bridge switches, and a solution to the "voltage-spike" problem - so apparent in transformer isolated current fed designs, leads to ZVS for all four of the bridge switches [51].

4.2 Theory of Operation

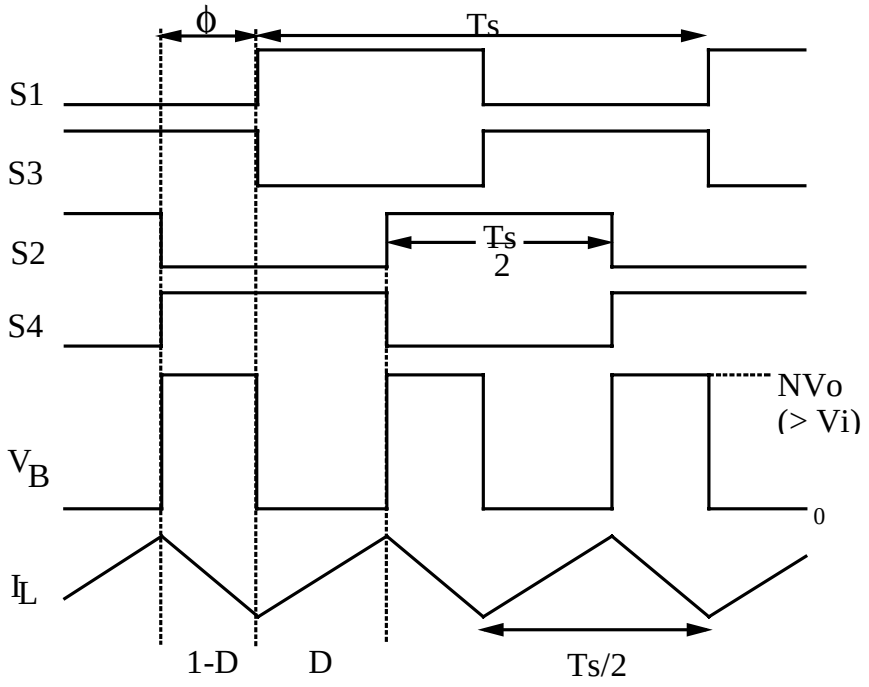
Figure 4.2 shows a simplified schematic of the active-clamp full-bridge boost topology. CCM operation for the boost inductor is assumed. Phase-shifting of the bridge switching sequence is utilized to control the boost function. The full-bridge topology, coupled with phase-shift control, offers a couple of advantages: 1) the boost inductor ripple frequency is twice the switching frequency, reducing its size, and, 2) with a slight modification to the phase-shift control ZCS becomes possible for the two of the four bridge switches [52]. Figures 4.2 and 4.3 illustrate these two concepts. For ZCS it is necessary to utilize the leakage inductance in the transformer (or possibly an external resonant inductor). Referring to Fig. 4.3, turning on S4 before S2 is turned off forces the current in L_{lk} to decrease linearly at a rate determined by:

$$\frac{di_{L_{LK}}}{dt} = \frac{NV_O}{L_{LK}}. \tag{4.1}$$

Current is increasing in S4 at the same rate (it's assumed the boost inductor can be

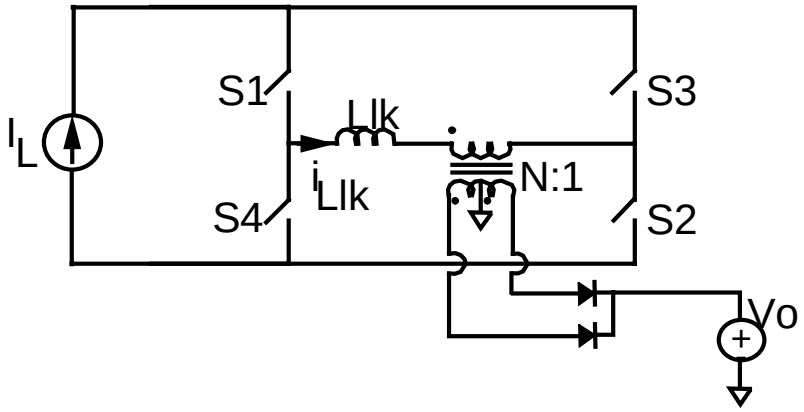


(a) Simplified circuit.

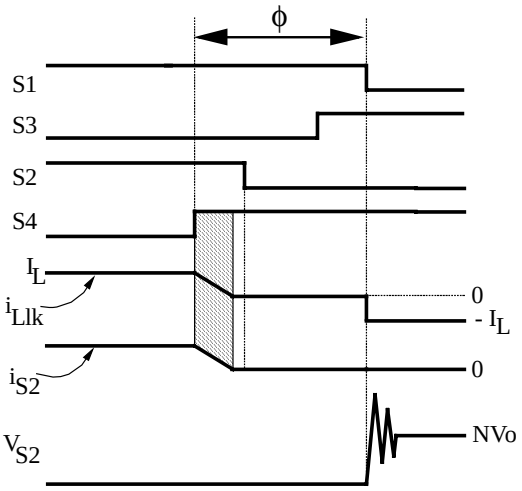


(b) Idealized waveforms.

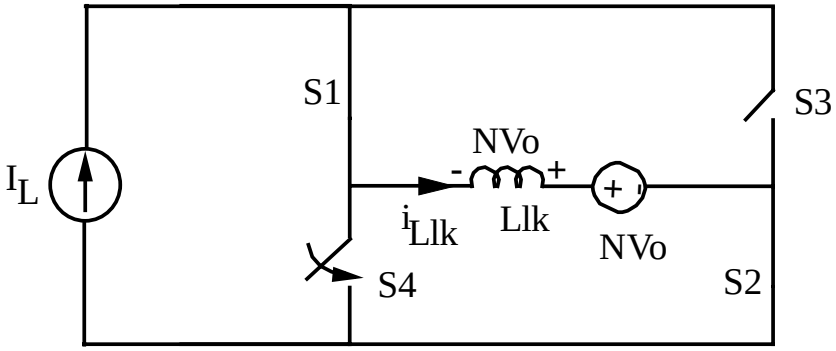
Fig. 4.2 Simplified ϕ-shifted active-clamp full-bridge boost converter operation.



(a) Simplified circuit with leakage inductance.



(b) Circuit waveforms.



(c) Converter topology for ZCS.

Fig. 4.3 Basic concept of boost full-bridge phase-shift operation [52].

idealized as a current source). When i_{S2} reaches zero the switch can be turned off with zero current.

As a practical matter, the isolated boost converter suffers from a problem at switch turn-off due to the dissimilarity of the values of the current source feeding the bridge (assuming the boost inductor can be idealized as a current source) and the current in the isolation transformer's leakage inductance. Unless an alternative path for the boost inductor current is temporarily provided, a large voltage spike, capable of destroying devices, will appear across the opened bridge switches. Some form of snubbing or clamping is necessary. For high-power applications RC snubbers are not very efficient. Therefore, an active-clamp circuit [51] (as shown in Fig. 4.4) is proposed for this application. In addition to the clamping function, the active-clamp circuit enables the isolation transformer's leakage energy to be used for zero-voltage switching (ZVS) of the bridge switches. Zero-voltage-switching is particularly important for S1 and S3, since snubber capacitors are used to reduce their turn-off losses. The ZVS mechanism recovers this turn-off energy before it is dissipated by switch turn-on. However, it should be pointed out that the circuit proposed here differs from that discussed in [51] in three fundamental ways: 1) ϕ-shift operation of the bridge switches enables zero-current switching (ZCS), 2) individual switches in the bridge operate with a fixed 50 % duty cycle, and 3) the operation of the boost inductor is in continuous conduction mode - necessary for single-phase high power operation.

Figure 4.4 shows the basic waveforms of operation with the active-clamp circuit. These waveforms are for a switching cycle and assume sufficient energy is stored in the leakage inductance to discharge C_{snub} completely. Also, it's assumed the clamp capacitor is infinite in value and the boost inductor can be replaced by a current source. The sequence of topological states is shown in Fig. 4.5, and is described below:

T_0-T_1: At T_0, S3 is turned off and the boost inductor current charges the switch capacitance. In order to control the switch turn-off losses, an external capacitor may be

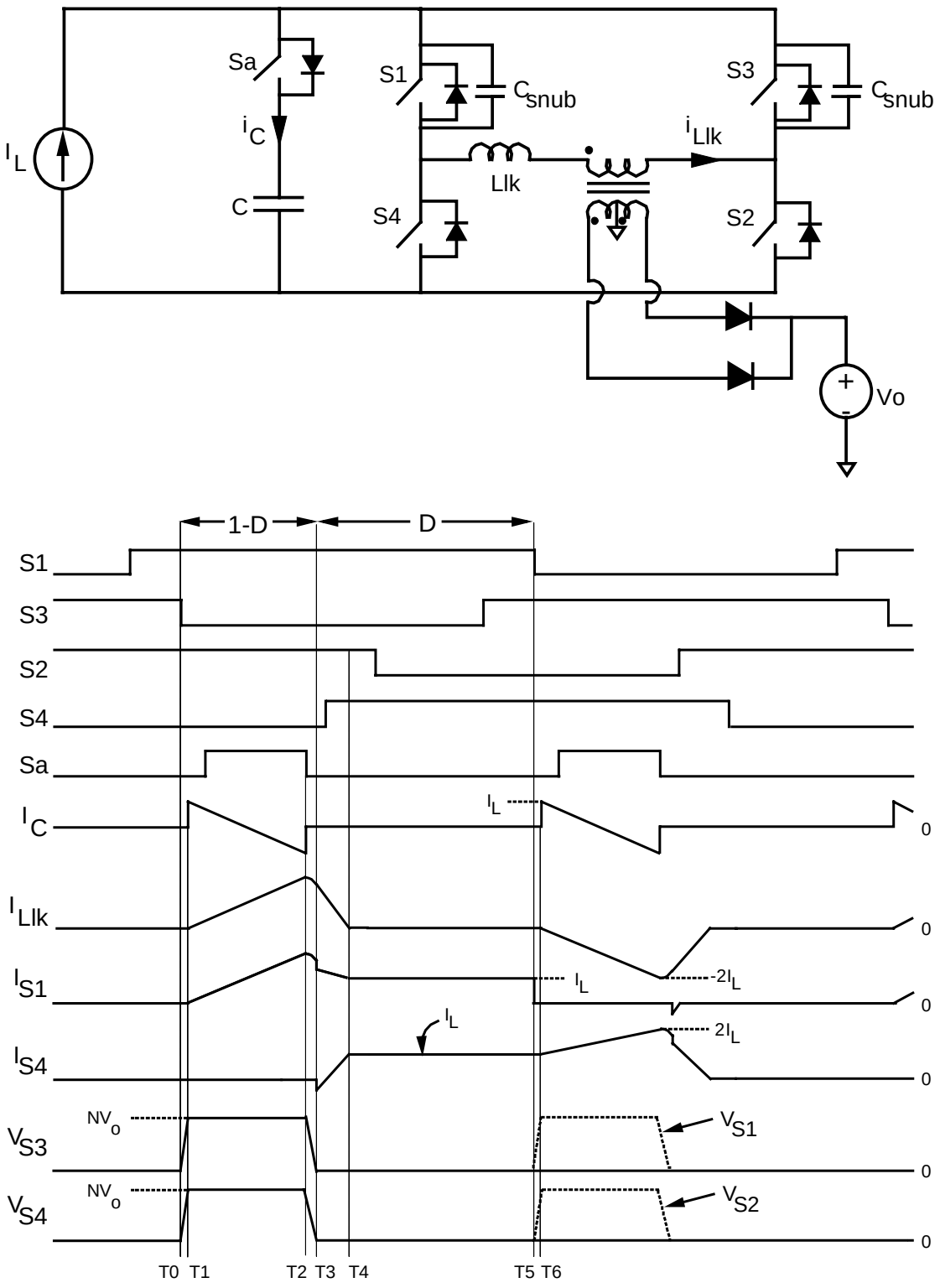


Fig. 4.4 Active-clamp FB boost converter ideal waveforms.

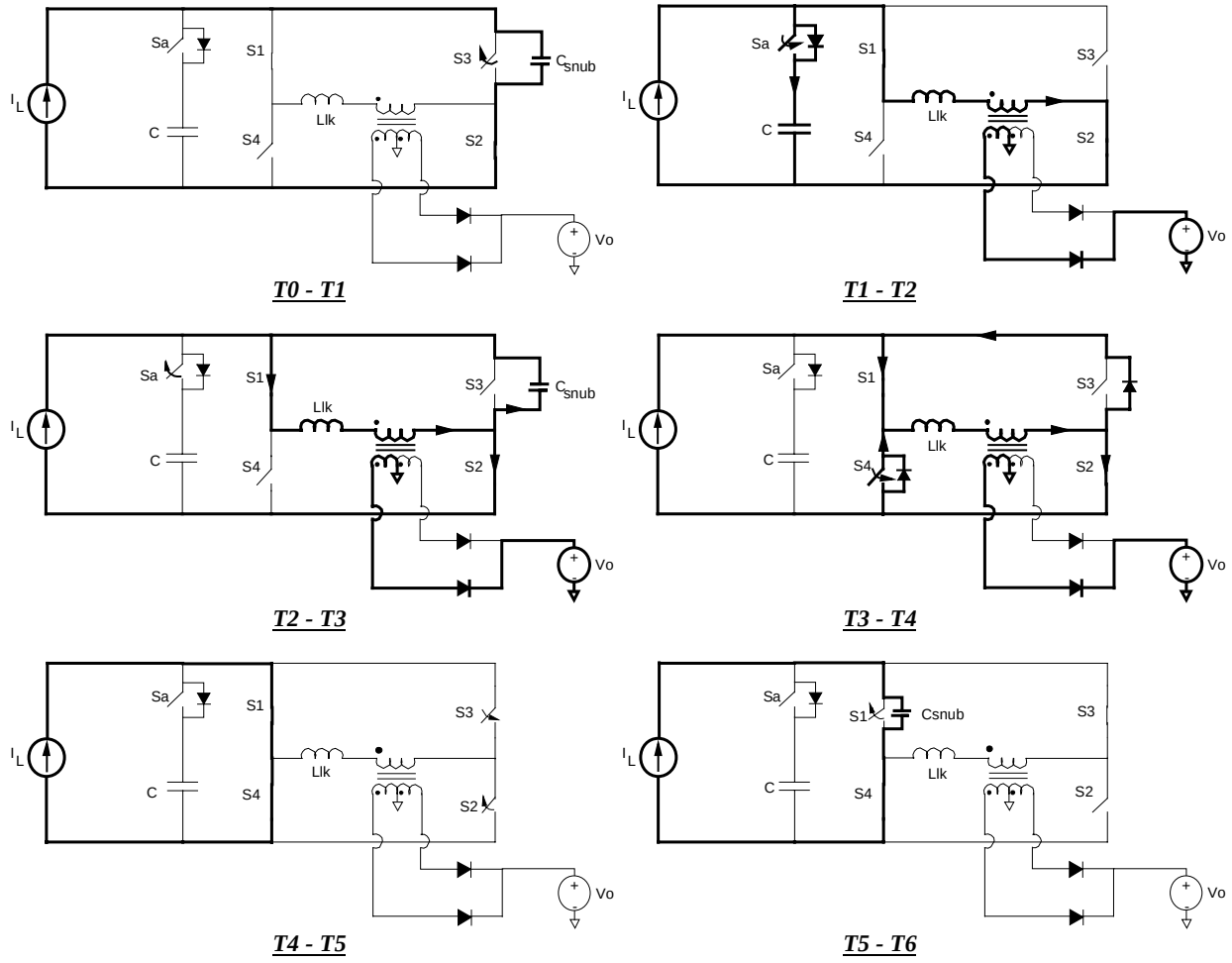


Fig. 4.5 Active-clamp full-bridge boost converter topological states.

added across the switch to form a turn-off snubber. This would be done, however, at the expense of decreasing the ZVS range.

T_1-T_2: At T_1, V_{S3} reaches the clamp capacitor voltage ($\approx NV_o$), and the clamp diode conducts the boost inductor current. The current through the leakage inductance increases as L_{LK} and C start to resonate. Current starts flowing to the output. To facilitate ZVS for Sa, the switch is turned on before the clamp current reverses.

T_2-T_3: At T_2 the active-clamp switch is turned off. Under the assumption of an infinite value of clamp capacitance, the turn-off current is equal to the boost inductor current (which implies $i_{Llk} = 2I_L$ at T_2). The difference between i_{Llk} and I_L discharges Csnub (Csnub and L_{LK} resonate). The voltage across S3 and S4 starts decreasing.

T_3-T_4: Assuming sufficient energy has been stored in L_{LK} to discharge Csnub, at T_3 the body diodes of S3 and S4 begin to conduct. S4 can then be turned on with zero voltage. I_{Llk} (and the current through S2) now decrease at a linear rate determined by the reflected output voltage and the value of L_{LK}. When i_{Llk} decreases to the value of the boost inductor current, S4 begins conducting the difference between the two currents.

T_4-T_5: When i_{Llk} decreases to zero, S2 can be turned off with zero current. Sometime during this interval S3 can be turned on with zero voltage, enabling Csnub to perform a lossless snubber action for turn-off of S3.

T_5-T_6: At T_5, S1 is turned off, ending the inductor charging interval. The sequence of topologies is then repeated for the other half of the bridge.

4.3 Design Considerations and Calculations

4.3.1 Switch timing

Other than the timing required to modulate the duty cycle through phase-shift control, it is necessary to derive the timing constraints to realize ZVS and ZCS. For ZVS, the timing between the turn off of Sa and the turn-on of S2 or S4 must allow the snubber capacitor voltage to reach its minimum. This is simply given by one-quarter of the L_{LK}-C_{snub} resonant period (during the T_2 - T_3 interval):

$$t_{Sa-S2} = t_{Sa-S4} = \frac{\pi}{2}\sqrt{C_{snub}L_{Lk}}\ . \tag{4.2}$$

For ZCS, sufficient time must be given between the turn-on of S2 or S4 and the turn-off of the switch on the opposite side of bridge (S4 or S2, respectively). The required time is determined by the value of transformer leakage inductance (referred to either the primary or the secondary), the output voltage (or reflected output voltage if leakage is considered from the primary), and the initial leakage inductance current. The worst case maximum time occurs with maximum leakage current (during the T_3 - T_4 interval):

$$t_{S2-S4} = t_{S4-S2} = \frac{2I_L^{peak}L_{Lk}}{\frac{Np}{Ns}V_o}\ . \tag{4.3}$$

I_L^{peak} is the peak boost inductor current.

4.3.2 Circulating energy

Due to the action of the active-clamp circuit, circulating energy is increased in the power stage components. To some degree this is beneficial, since it is desirable to operate under zero-voltage switching conditions. However, for ZVS it is not necessary for the clamp switch to conduct for almost the entire (1-D)Ts time period. As long as the leakage inductance current is larger than I_L at the instant the clamp switch is turned off, ZVS may be possible. Therefore, the timing for Sa can be modified, as shown in Fig. 4.6, to reduce conduction losses. The drawback to this modified timing scheme is that ZVS is lost for Sa and some ringing will be introduced across the bridge when neither Sa nor its diode is conducting.

4.3.3 Design calculations

The design calculations developed in this section primarily revolve around determining various component losses. It is assumed insulated gate bipolar transistors (IGBTs) are used for the bridge switches. In fact, the experimental results reported in Section 4.4 are based on the use of IGBT bridge switches.

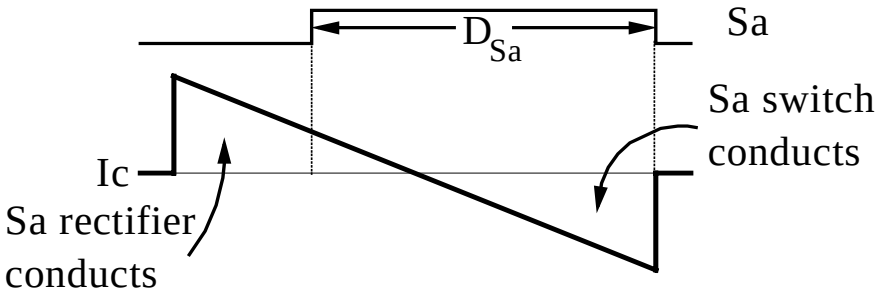
4.3.3.1 Full-bridge switch calculations

4.3.3.1.1 Conduction loss

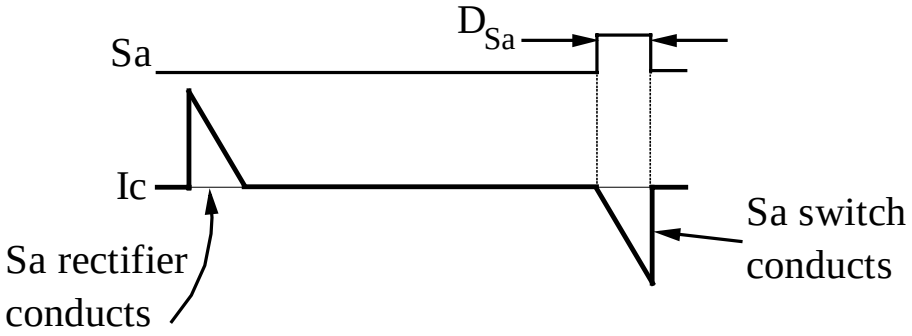
As a function of the 120 Hz line cycle, the average (switching cycle) current seen by individual switches in the bridge is given by:

$$\langle I_S \rangle(\phi) = \frac{\sqrt{2}P_o}{\eta 2V_{RMS}} \sin\phi, \tag{4.4}$$

where ϕ is the instantaneous operating point on the input line (normalized over the interval $[0,\pi]$) and η is the conversion efficiency. Due to the phase-shifted control of the



(a) Original timing.



b) Modified timing.

Fig. 4.6 Active-clamp switch timing to reduce conduction loss

full bridge, the duty cycle of each switch is approximately 50 % regardless of the operating point. Assuming V_{CE}(sat) for IGBTs is constant as a function of collector current, the conduction loss averaged over a line cycle is:

$$P_{cond,bridge} = \frac{4}{\pi}\int_0^{\pi} \langle I_S \rangle(\phi) V_{CE}(sat)\, d\phi \tag{4.5a}$$

$$= \frac{4\sqrt{2}P_o}{\eta\pi V_{RMS}} V_{CE}(sat)\,. \tag{4.5b}$$

4.3.3.1.2 Switching loss

Calculating the switching loss is more involved than calculating the conduction loss. Assuming unity power factor, ZVS is a function of the input voltage as it changes over the line cycle. This dependence greatly complicates matters, so in order to simplify the arithmetic, it will be assumed that Csnub is so small as to have no effect on reducing the turn-off loss for S1 and S3. As a consequence, however, ZVS will be available over the entire line cycle. The result of these assumptions is probably an overestimation of the S1, S3 turn-off loss and an underestimation of the S2, S4 turn-on loss. For ZVS operation, all four switches are turned on losslessly, and the bottom two switches are turned off with zero current. An important aspect for the zero-current turn-off of S2 and S4 is that their collector voltages remain at approximately V_{CE}(sat) for the duration of the boost inductor charge interval (see Fig. 4.10(a)). The top two switches suffer from hard turn-off, which is the reason for installing the snubber capacitors. The use of empirical methods is probably best to determine an optimum value for these capacitors.

For S1, S3 turn-off:

$$P_{off}(\phi)\Big|_{S1\,or\,S3} = F_S E_{off}(\phi)\frac{V_{CE,off}}{V_{CE,baseline}}, \tag{4.6}$$

where $V_{CE,baseline}$ is the test voltage used for device turn-off measurements and

$$E_{off}(\phi) = f(I_{CE,off}(\phi)). \tag{4.7}$$

$I_{CE,off}(\phi)$ is the boost inductor current at device turn-off. Its value is twice that given by Eq. (4.4). The turn-off voltage is constant and equal to the reflected output voltage. A curve fit based on device turn-off loss data can then be used to develop a relationship between turn-off energy and collector current.

4.3.3.2 Output rectifier calculations

For the output rectifiers, assume that individual rectifier forward drops (V_{fw}) are independent of forward current, and that the forward drops in each rectifier are equal. In an average sense, each rectifier sees the one-half of the output current. Therefore:

$$P_{output\ rectifier} = \frac{P_o}{2V_o}V_{fw}. \tag{4.8}$$

For rectifier switching losses, the stored charge can be used to determine the reverse recovery energy:

$$E_{sw}\Big|_{output\ rectifier} = V_R Q_{rr}. \tag{4.9}$$

Q_{rr} is a function of the peak rectifier forward current (just before turn-off) and the turn-off di_F/dt. The rate of turn-off current is fixed by the reflected value of the leakage (or resonant) inductance and the output voltage:

$$\frac{di_F}{dt} = \frac{V_O}{L_{LK} / \left(N_P / N_S \right)^2}. \tag{4.10}$$

The peak rectifier forward current is given by:

$$I_F^{peak}(\phi) = 2 \frac{N_P}{N_S} \frac{\sqrt{2} P_O}{\eta V_{RMS}} \frac{N_P}{N_S} sin(\phi). \tag{4.11}$$

The factor of 2 appearing in Eq. (4.11) is due to the action of active-clamp and is worst-case conservative. The reverse voltage (V_R) is equal to the output voltage. Assuming all the reverse recovery energy is dissipated, the switching losses are given by:

$$P_{SW}\big|_{output\ rectifier} = \frac{1}{\pi} \int_0^{\pi} F_s \frac{V_o}{2} Q_{rr}\left(I_F^{peak}(\phi), V_o \right) d\phi. \tag{4.12}$$

Because of the nonlinear dependence of Q_{rr} on I_F and V_R, the integration called for in Eq. (4.12) is a math phobic's worst nightmare. Things can be simplified by using the average value (over a line cycle) of the peak rectifier current (Eq. (4.11)) as a "steady-

state" operating point. This (along with V_O) can be used to select a value for Q_{rr}. Therefore:

$$P_{SW}\Big|_{output\ rectifier} \approx \frac{1}{2} F_S V_o Q_{rr}\Big|_{\left\langle I_F^{peak}(\phi)\right\rangle, V_o}. \tag{4.13}$$

4.3.3.3 Active-clamp circuit calculations

Active-clamp circuit losses consist of conduction losses for both the auxiliary diode and MOSFET and switching (turn-off) losses of the MOSFET. For the rectifier, or MOSFET body diode, conduction losses are given by:

$$P_{Sa,Rect} = \left\langle I_{Sa}\right\rangle\Big|_{\substack{line\\cycle}} V_F = \frac{V_F}{\pi}\int_0^{\pi} \left\langle I_{Sa}\right\rangle\Big|_{\substack{switching\\cycle}} d\phi\,, \tag{4.14}$$

where:

$$\left\langle I_{Sa}\right\rangle\Big|_{\substack{switching\\cycle}} \cong I_L(\phi) D_{Sa}\,, \tag{4.15}$$

and D_{sa} is the switch's duty cycle. $I_L(\phi)$ is the boost inductor (and line) current. Carrying out the integration called for in Eq. (4.14) yields:

$$P_{Sa,\mathrm{Rect}} = \frac{D_{Sa}\sqrt{2}P_O}{\eta\pi V_{RMS}} V_F\,. \tag{4.16}$$

Calculating conduction losses for the MOSFETs requires knowledge of the RMS current through the devices:

$$P_{Sa,MOSFET}(\phi) = \left(I_{Sa,RMS}(\phi)\right)^2 R_{DS,on}. \tag{4.17}$$

Therefore:

$$\left\langle P_{Sa,MOSFET} \right\rangle_{\substack{line \\ cycle}} = \frac{1}{\pi}\int_0^{\pi} P_{Sa,MOSFET}(\phi)d\phi. \tag{4.18}$$

Turn-off losses are given by:

$$P_{off,MOSFET} = \frac{1}{\pi}\int_0^{\pi} P_{off}(\phi)d\phi \tag{4.19a}$$

$$= \frac{1}{\pi}\int_0^{\pi} F_S \frac{N_P}{N_S}\frac{V_o}{3}\frac{t_f}{2} I_L(\phi)d\phi. \tag{4.19b}$$

The turn-off fall time, t_f, is assumed to be 75 ns. Turn-on losses are calculated in a similar fashion (t_r = 50 ns):

$$P_{on} = \frac{1}{\pi}\int_0^{\pi} P_{on}(\phi)d\phi = \frac{1}{\pi}\int_0^{\pi} F_S \frac{N_P}{N_S}\frac{V_o}{3}\frac{t_r}{2} I_L(\phi)d\phi. \tag{4.20}$$

4.4 Experimental Results

To provide experimental verification of the operating concepts incorporated into the phase-shift controlled, active-clamp FB boost converter, a breadboard was constructed to provide a 48 Vdc, 1 kW output DC bus voltage from a universal AC line input. The efficiency of this design is then compared to the efficiency obtained from two-stage front-end design consisting of a zero-voltage transition (ZVT) PFC boost converter cascaded with a ZVS FB second stage DC/DC converter.

4.4.1 Power stage design

The power stage design for the active-clamp boost converter is shown in Fig. 4.7. The bridge switches operate at 75 kHz, and are each 600 V ultra-fast IGBTs. The turn-off snubber capacitors are each 1500 pF, a value that was arrived at empirically. The clamp network consists of 600 V, 2 μF, polypropylene capacitor. The clamp capacitor should be of high quality in order to process the HF ripple currents introduced by the action of the active clamp network with as little loss as possible. The output diodes are 100 V Schottky rectifiers. Here the single-stage boost converter has a distinct advantage over the second stage DC/DC converter in the two-stage approach, where the use of Schottky rectifiers would be prohibited due to too high of a reverse voltage. Three 4700 μF Aluminum electrolytic capacitors form the output bulk capacitor. Peak 120 Hz voltage ripple was measured at about 2.5 V peak (± 5.2 %). In practice, the amount of output capacitance is determined by ripple current capability.

Also shown in Fig. 4.7 is the design of the boost inductor and the isolation transformer. Because of the high output current required and the additional circulating current introduced by the active clamp circuit, the design of T1's secondary required the use of Cu foil, as shown.

A block diagram of the average current mode control scheme is shown in Fig. 4.8. In order to obtain good power factor at the input, the full-bridge phase-shift is modulated.

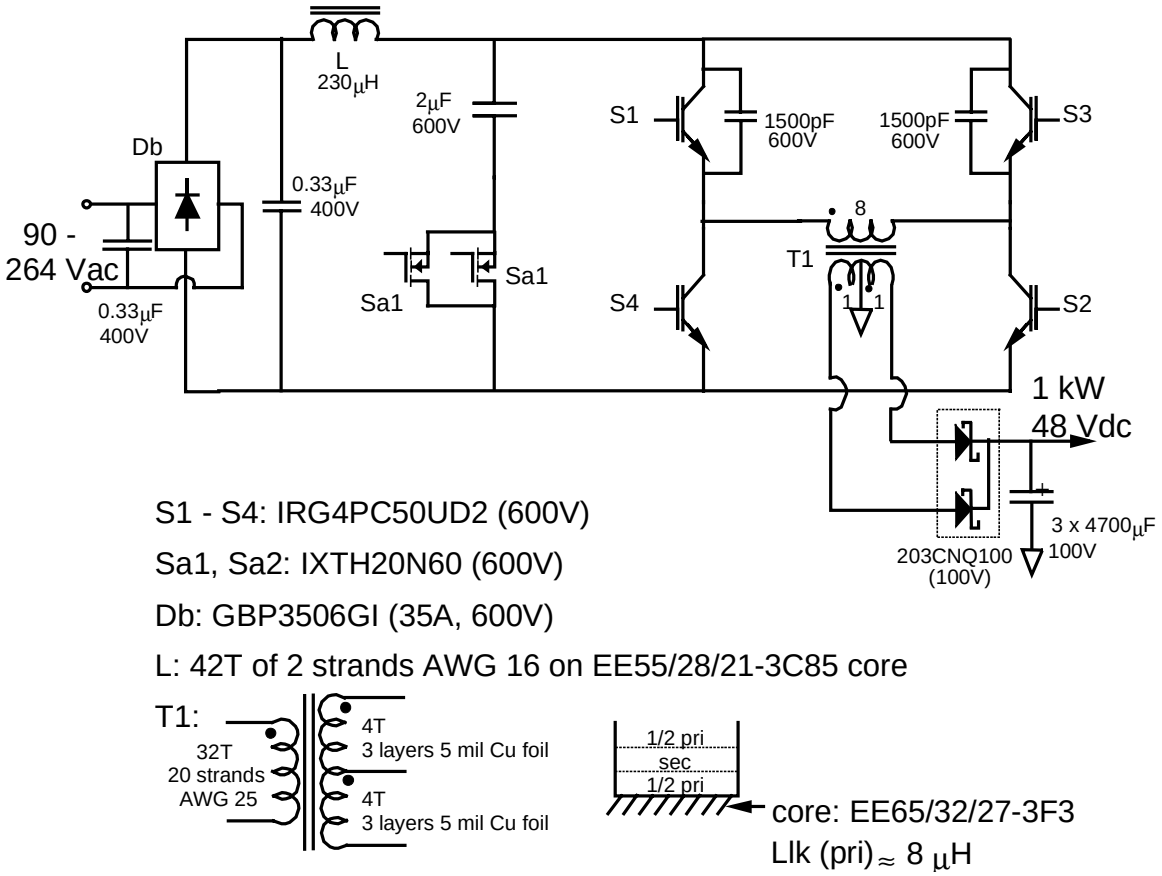


Fig. 4.7 Power stage component selection.

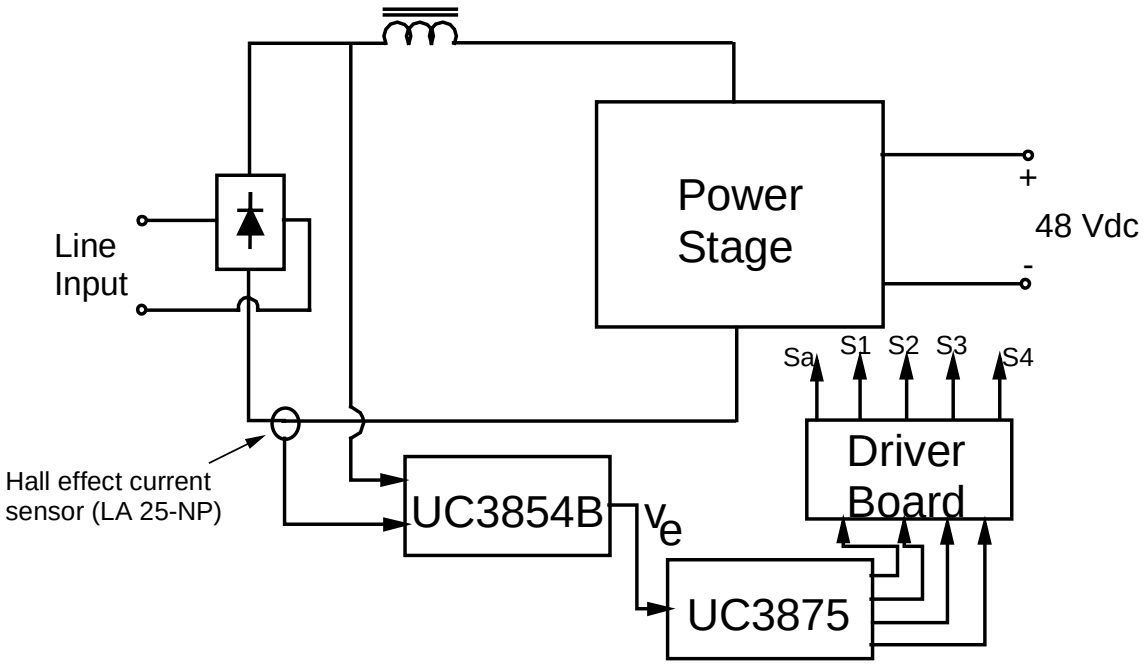


Fig. 4.8 Block diagram of FB control for PFC.

However, since there are no commercially available full-bridge ϕ-shift control integrated circuits for PFC, the method shown in Fig. 4.8 was adopted. A single-ended PFC controller IC, the UC3854B, was used to generate a control voltage, Ve, as part of the standard application of this IC [48]. This control voltage was then used as the error amplifier input for a ϕ-shift control IC, the UC3875. The UC3875 then generates the four ϕ-shifted drive signals for the bridge switches. The driver board is then responsible for developing the active-clamp switch drive based on the ϕ-shifting of the bridge switches.

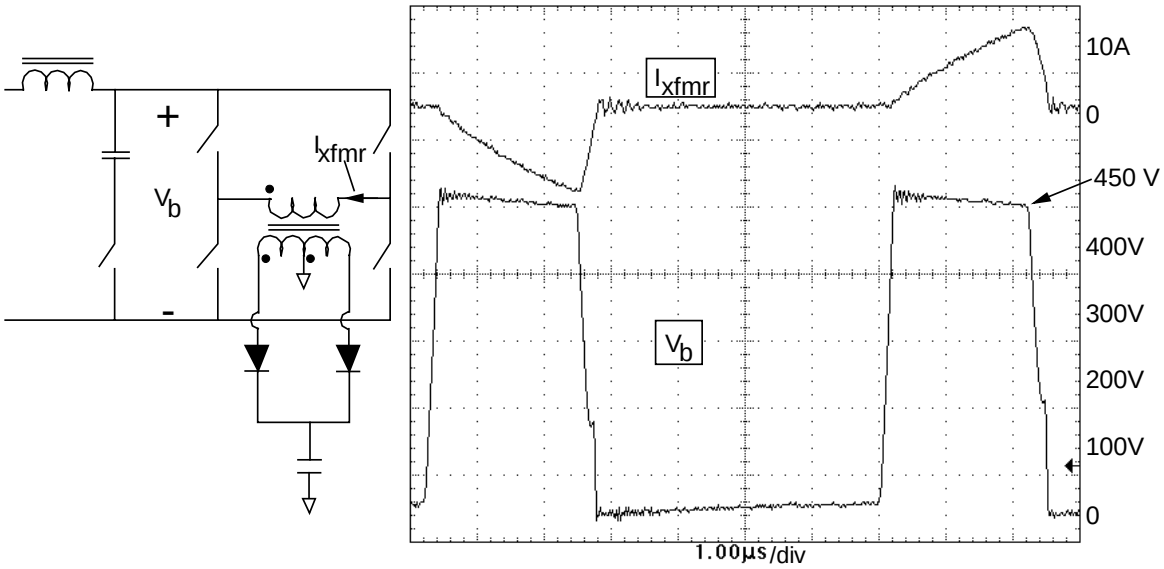
4.4.2 Experimental waveforms and efficiency measurements

Figures 4.9 through 4.11 summarize the fundamental experimental waveforms of the converter. Figures 4.9 and 4.10 were obtained with the converter operating from a DC input voltage in order to more clearly show these waveforms over a switching cycle. Figure 4.9 summarizes the operating waveforms associated with the active-clamp network. The fundamental characteristics of these waveforms is identical to those of the active-clamp flyback converter presented in Chapter 3. The waveforms illustrating the soft-switching characteristics are shown in Fig. 4.10. The line input waveforms are shown in Fig. 4.11 for Vin = 120 Vac and Po = 1 kW. As can be seen, the power factor is very high and has minimal harmonic distortion, both typical of average current mode control PFC and CCM operation of the boost inductor.

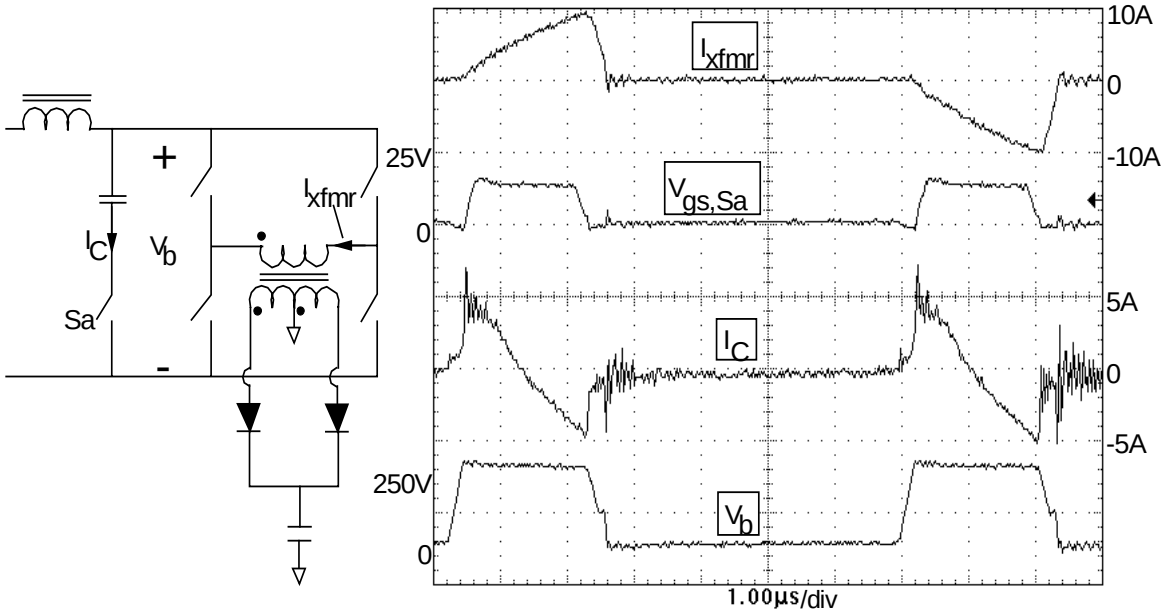
The experimental efficiencies, as a function of line and load are presented in Fig. 4.12. High-line/maximum load efficiencies are above 90 %.

4.4.3 Experimental comparison with the two-stage approach

In order to provide a relative efficiency comparison with the two-stage front-end approach, data was taken from the two-stage power train design shown in Fig. 4.13. This design cascades a ZVT PFC boost converter, switching at 140 kHz, with a standard ZVS ϕ-shifted full-bridge DC/DC converter switching at 100 kHz, using the components

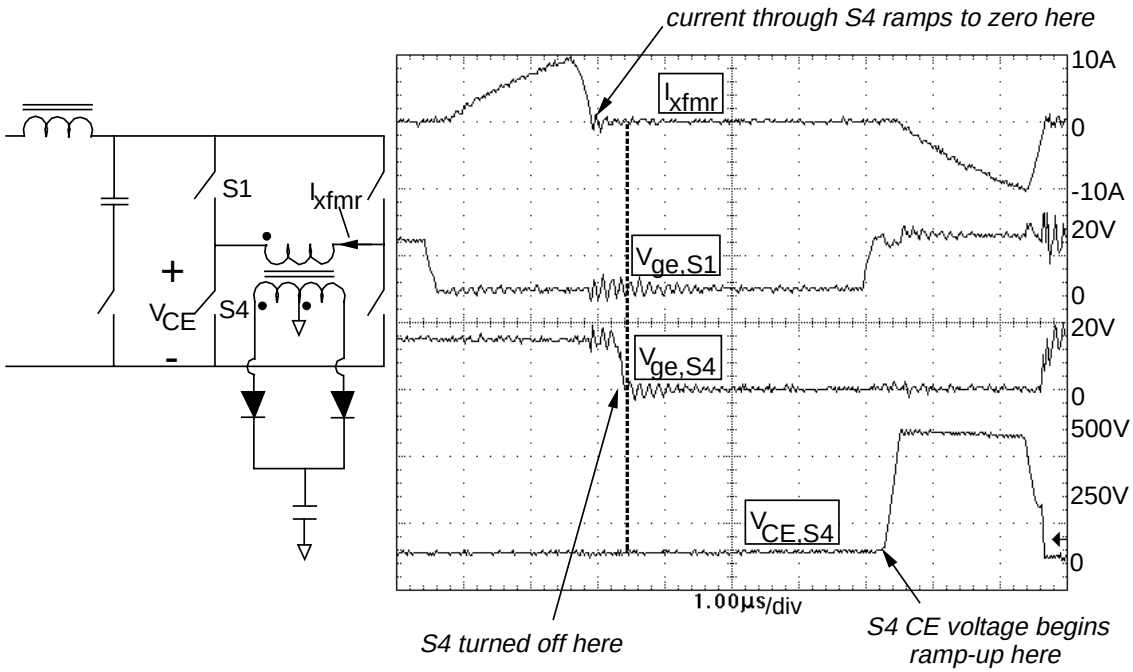


(a) Bridge-voltage clamping, Vin = 150 Vdc, Po = 960 W.

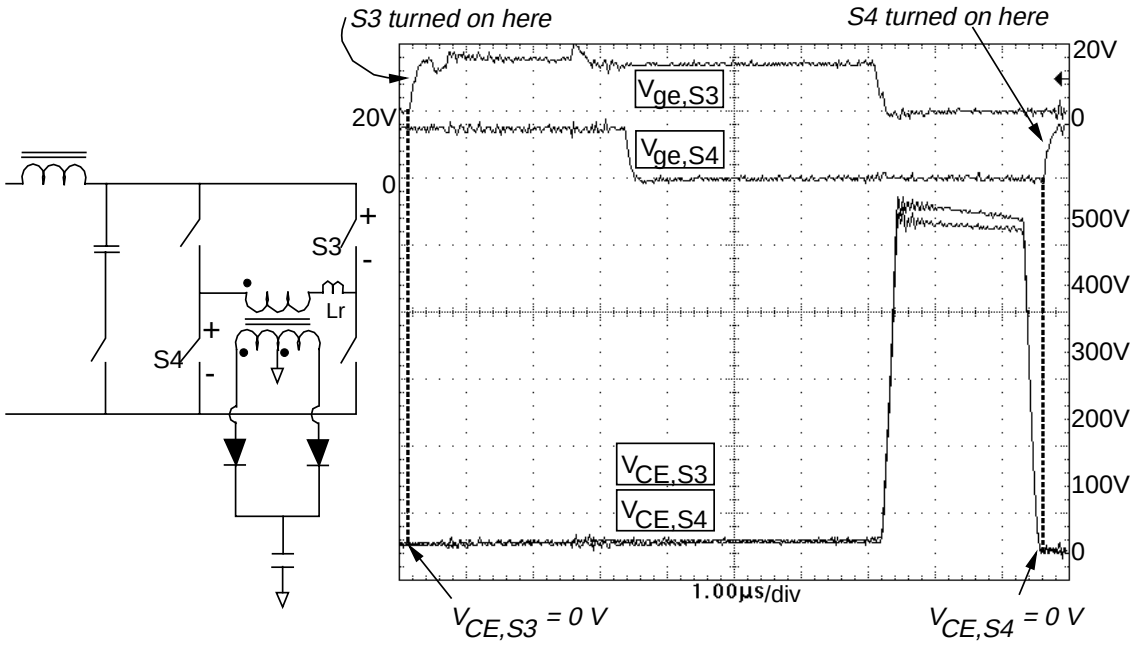


(b) Clamp circuit waveforms, Vin = 140 Vdc, Po= 700 W.

Fig. 4.9 Experimental waveforms - clamp operation.



(a) ZCS for S4, Vin = 140 Vdc, Po = 700 W.



(b) ZVS for S3/S4 (Lr = 5 µH), Vin = 140 Vdc, Po = 958 W.

Fig. 4.10 Experimental waveforms - soft-switching.

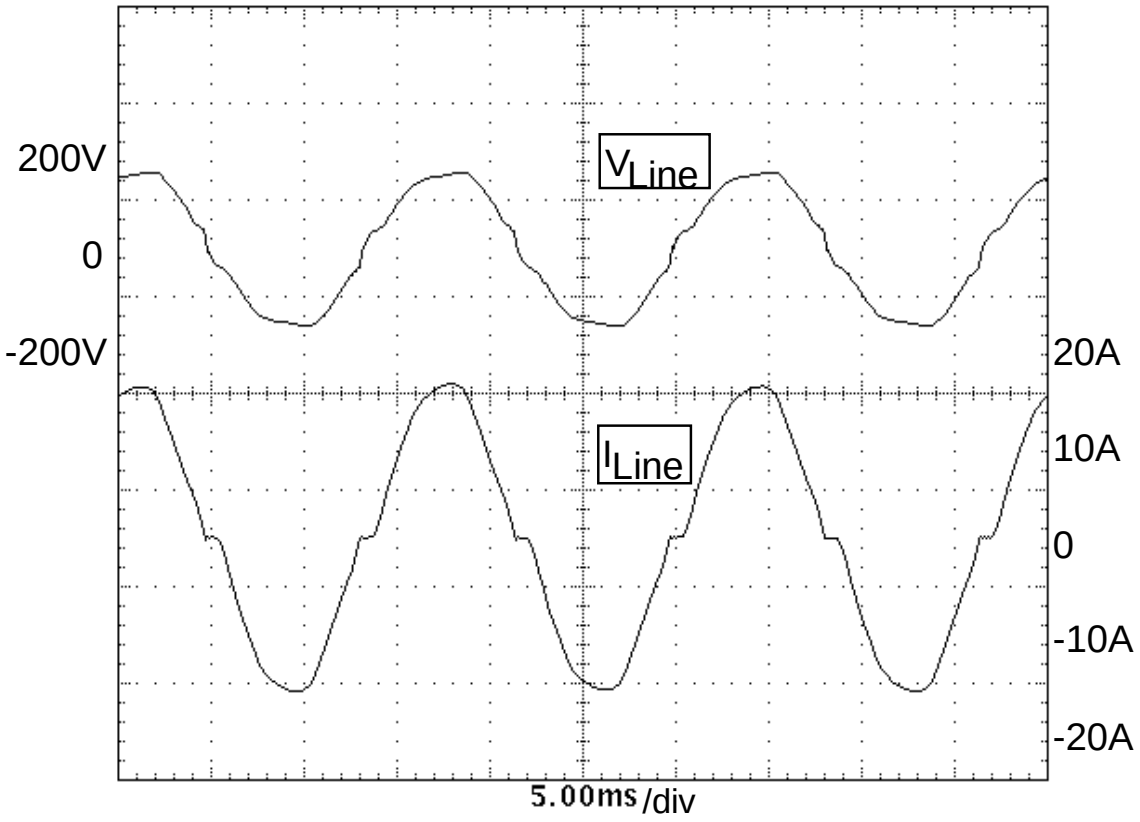


Fig. 4.11 Experimental waveforms - line voltage and current, Vin = 120 Vac, Po = 1 kW.

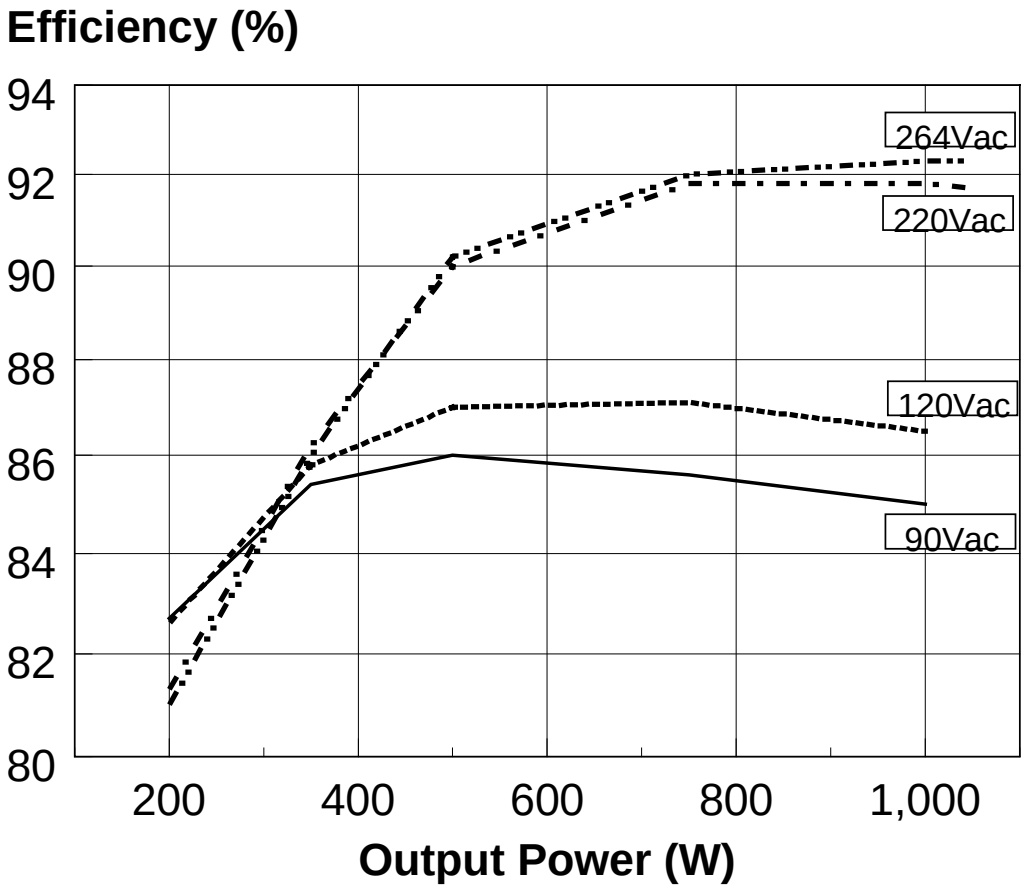


Fig. 4.12 Experimental efficiency as a function of line and load (includes control circuit losses).

indicated. The large value of bulk capacitance (close to 900 μF) used in this design is to provide for a significant hold-up function.

The efficiency data, as a function of line voltage with a constant output power of 1 kW, is given in Fig. 4.14. At low line voltages the efficiencies are very comparable, but as the line voltage is increased past about 150 Vac the two curves diverge. At Vin = 220 Vac the active-clamp boost is nearly 3 % more efficient. This makes sense as at high line the circulating energy losses introduced by the active-clamp network are reduced (boost inductor current is at a minimum) and maximum advantage can be taken of the fact that the power is processed in one conversion stage. From the efficiency data it would seem the active-clamp boost converter is best suited for applications requiring PFC and equipment operation from a single-phase 220 Vac input.

4.5 Summary

In this chapter, the phase-shift controlled, active-clamp full-bridge PFC boost converter has been shown to be an attractive solution for higher power front-end converters utilized in DC distributed power systems. The introduction of the active-clamp circuit introduces minimum complexity in the implementation of the overall converter and provides a mechanism to recover the transformer leakage energy and achieve zero-voltage switching. This approach reduces device voltage and switching stress at the expense of increasing circulating energy. It was also demonstrated how phase-shift operation of the bridge switches results in zero-current switching for two of the four bridge switches [52]. The control concept is straightforward, with constant frequency, PWM phase-shift control being utilized. Experimental results indicate a 3 % efficiency improvement (at high input line and with a 1 kW, 48 Vdc output) over a boost PFC/ZVS FB DC/DC two-stage design.

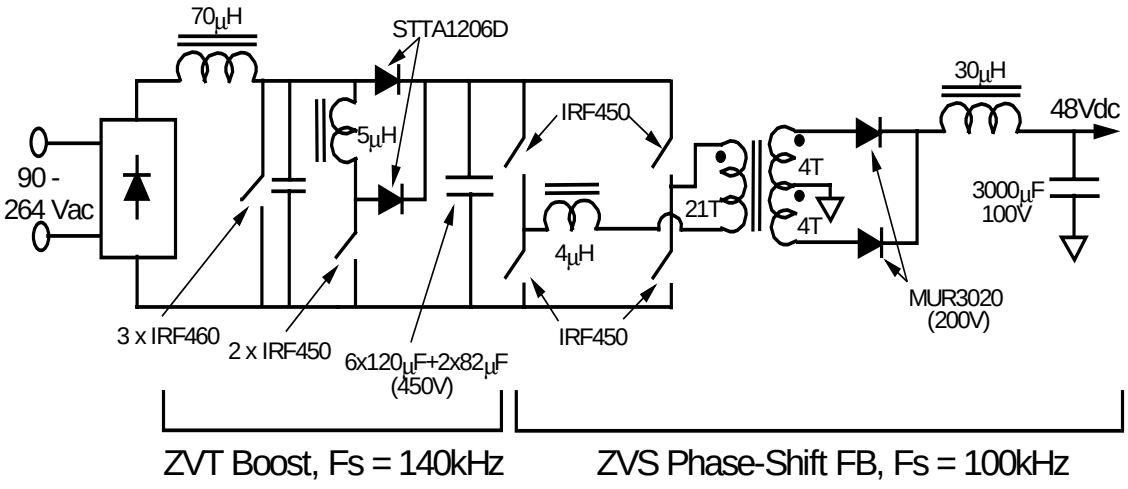


Fig. 4.13 Experimental two-stage power train design.

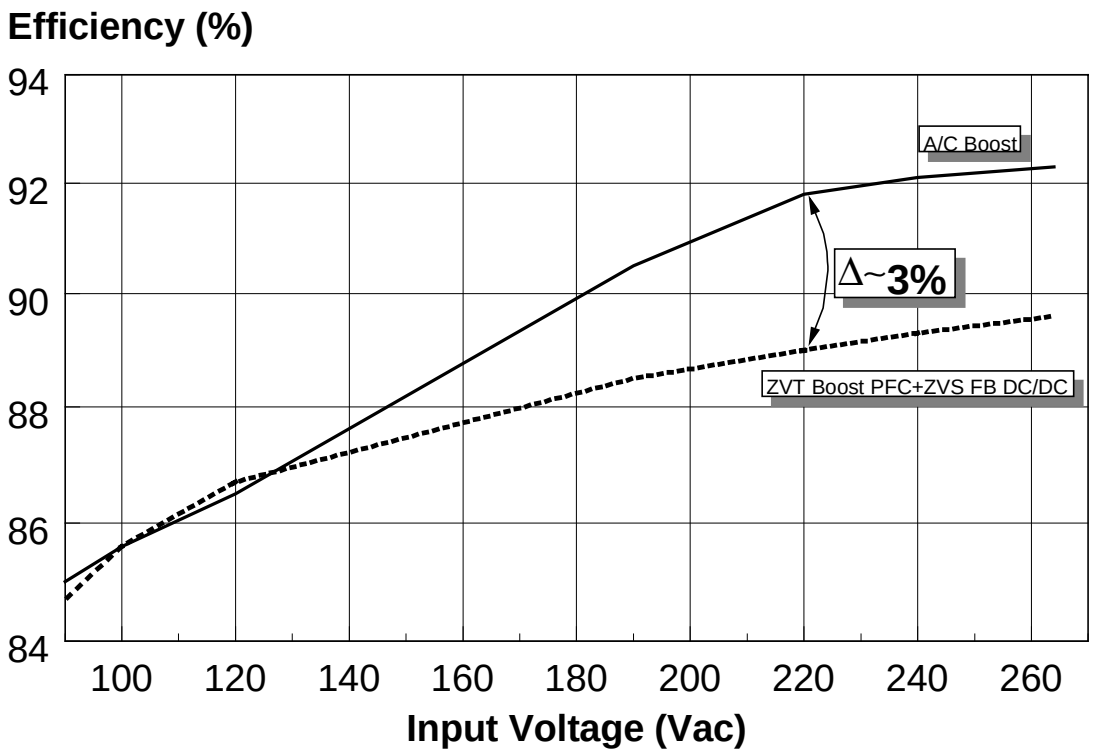


Fig. 4.14 Experimental efficiency comparison between 2 stage and single stage implementations. Po = 1 kW.