Analysis of Nonlinearities in a Voltage - Controlled Oscillator

by

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(ABSTRACT)

A voltage-controlled oscillator is investigated to determine the source of nonlinearities in the frequency-to-voltage characteristic. A computer model for the voltage-controlled oscillator is developed which emphasizes the nonlinear behavior of the current gain in its transistors. Additionally, a comprehensive model of the current mirror circuit is derived. The current mirror circuit plays an important role in determining the output frequency of the VCO. Included in the current mirror model are the effects of the unequal transistor power dissipation on the VCO performance.

An inexpensive and practical solution is proposed that allows the voltage-controlled oscillator to operate in a more linear fashion. The experimental measurements of the implementation of the proposed solution on a sample voltage-controlled oscillator yield favorable results. Additionally, a computer simulation incorporating the proposed solution compares favorably with the experimental data.

ACKNOWLEDGEMENTS

There are many people I would like to thank. I would like to thank my wife Linda McKearney for her support and help in preparing this report, and Barry Witherspoon and Lisa Underwood of Litton Industries for their enduring patience and help. I also thank my committee members, especially Dr. Donald M. Keller, for their time and guidance. A special thank you goes to my sponsors for the Raytheon Company scholarship, Mr. Pietro Ventresca and Mr. William Puzella.

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CHAPTER 1

INTRODUCTION

INTENT OF PROJECT

The intent of this project is to investigate and correct a nonlinear frequency-to-voltage characteristic in a voltage-controlled oscillator (VCO). The VCO is a currently manufactured analog integrated circuit that is used to tune a local oscillator in the Guidance Section of a missile defense system. The VCO must be tuned over several octaves of frequency (10 to 300 kHz range) and must maintain a specified frequency linearity with input tuning voltage. As currently produced however, the VCO has a frequency-to-voltage characteristic that compromises its production rate and yield, requiring excessive adjustment and tailoring during production test.

PROBLEM STATEMENT

The VCO is essentially a tunable multivibrator that transforms an input tuning voltage to a current, which charges a timing capacitor. The output frequency of the VCO is directly proportional to the timing capacitor charge current. As the input tuning voltage is varied, so is the timing cap-

pacitor charge current and thus the output frequency is varied. It was discovered that the timing capacitor charge current is a nonlinear function of the input tuning voltage. This nonlinearity is due to the inherently nonlinear current gain of the VCO transistors as the applied current to these transistors is varied. It is shown, both in the literature and through measurements, that at low to moderate levels of applied current, on the order of a few milliamperes, as the current is increased the current gain increases and then levels off. As the applied current is further increased to a range of approximately 10 to 13 mA the current gain then rapidly decreases, resulting in two distinct regions of the output frequency versus tuning voltage characteristic.

Figure 1.1, on the next page, is a plot of the measured frequency deviation of a sample VCO. The ideal condition would occur if the output frequency exhibited no deviation and were plotted as a zero Hertz deviation as a function of tuning voltage. In the first region, at low to moderate tuning voltage levels, the characteristic exhibits a slightly steeper than nominal slope which then levels off and becomes flatter. In this region the output frequency is within the specified frequency tolerance limits. In the second region, at higher tuning voltage levels, the characteristic exhibits a much less than nominal slope that tends to decrease further as the tuning voltage is increased.

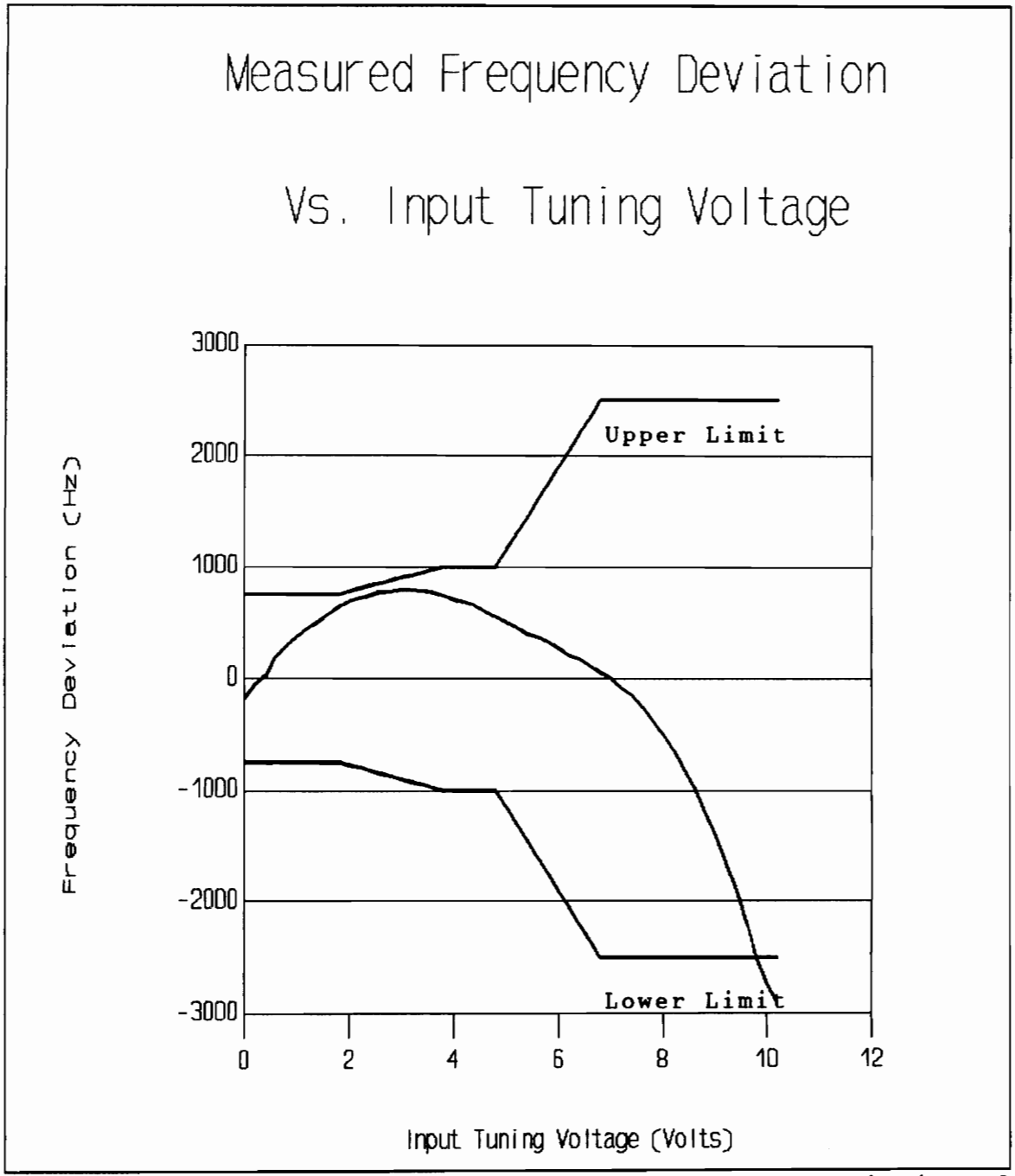

Figure 1.1. **Plot of measured output frequency deviation of the VCO.**

In this region the output frequency falls below the frequency tolerance limits.

PROPOSED SOLUTION

The most straightforward solution is to limit the applied current to the transistors in the VCO to a region where the transistor current gain is fairly linear, while still maintaining the required input tuning voltage range and output frequency range. The improved linearity can be accomplished by increasing the value of the resistor that controls the current in the VCO such that it limits the maximum applied current to a region where the transistor current gain is more linear. However, since the applied current is reduced, the output frequency range is also reduced. Therefore, to maintain the specified output frequency range, the value of the timing capacitor must be reduced. The resulting frequency-to-voltage characteristic is one that is more nearly linear.

RESULTS

A sample VCO was modified to implement the proposed changes. This particular VCO exhibited an extremely nonlinear frequency versus input tuning voltage characteristic. At the upper end of the tuning range of the VCO the specified frequency tolerance is ± 2500 Hz from the nominal output fre-

quency. The output frequency of this particular VCO was approximately 4500 Hz below the nominal frequency, which exceeds the specified tolerance. The typical production VCO when tuned to the upper end of its range exhibits an output frequency that is 2000 Hz below the nominal frequency, which just barely meets the specified tolerance. The particular VCO that was modified may exhibit a worst case condition. However, with the proposed solution installed, the VCO output frequency deviated only 300 Hz at its worst point from the nominal specification.

ORGANIZATION OF REPORT

The remainder of this report is divided into four chapters. Chapter 2 discusses the basic operation of the frequency control loop in the missile guidance section with emphasis on how the VCO is used with the missile's local oscillator. Chapter 3 provides a discussion of the VCO at its circuit card level leading to a detailed description of the operation of the VCO. In chapter 3 the VCO circuit is analyzed by combining empirical and analytical methods, which lead to the possible sources of the circuit nonlinearities. Also in Chapter 3 a computer model of the VCO is developed. Chapter 4 discusses the proposed solution and results. Chapter 5 is the concluding chapter that summarizes the results.

CHAPTER 2

SYSTEM OVERVIEW

As mentioned in Chapter 1, the VCO is used in a frequency control loop in the guidance section of a missile defense system. The system is of the semi-active type in which the target is illuminated by a radar beam from a stationary position other than the missile, while the missile receives, tracks and homes in on the target echo. The missile homes in on the target by determining the angular location and velocity of the target relative to the missile. The illuminator transmits a continuous wave (cw) signal and is positioned either at a ground base for land engagements, or shipboard for sea engagements. Figure 2.1, on the next page, shows the relationship between the illuminator, target and missile.

The guidance section is a receiver that determines both the angular location and velocity of the target. To determine the target angular location, the guidance section uses the principles of an amplitude comparison monopulse radar [Skolnik, 1980].

To determine the relative velocity of the target, the guidance section must measure the relative doppler fre-

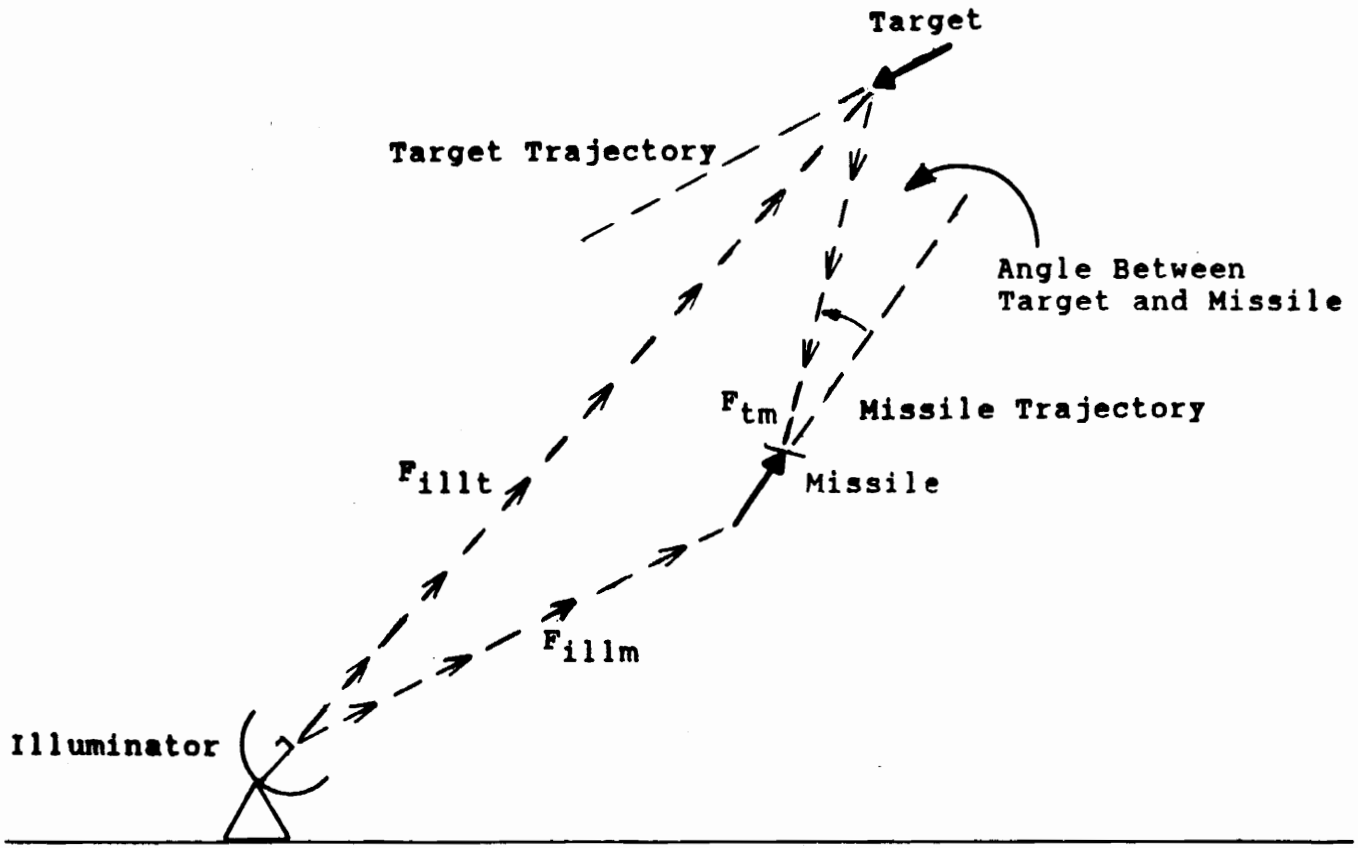

Figure 2.1 Relationship of illuminator, target and missile.

quency shift between the target and missile given by [Skolnik, 1980]

$$f_{tm} = \frac{f_{ill} \cdot 2 \cdot v_{tm}}{c} \qquad (2.1)$$

where f_{tm} is the doppler shift between the missile and the target, f_{ill} is the illuminator frequency, v_{tm} is the velocity of the target relative to the missile and c is the speed of light. Note that when the missile and target are traveling toward each other the resulting doppler frequency shift increases. Rearranging Equation (2.1) yields an expression for v_{tm} as

$$v_{tm} = \frac{f_{tm} \cdot c}{2 \cdot f_{ill}} \qquad (2.2)$$

A basic block diagram of the missile guidance section is shown, on the next page, in Figure 2.2. The VCO is essentially used to offset the frequency at the output of the 3 MHz VCO, which is point 3 in Figure 2.2. The target echo frequency received by the front antenna and processed in the front channel of the guidance section is given by

$$\text{f of Target Echo} = f_{ill} + (f_{tm} + f_{illt}) \qquad (2.3)$$

where f_{ill} is the illuminator frequency, f_{tm} is the doppler fre-

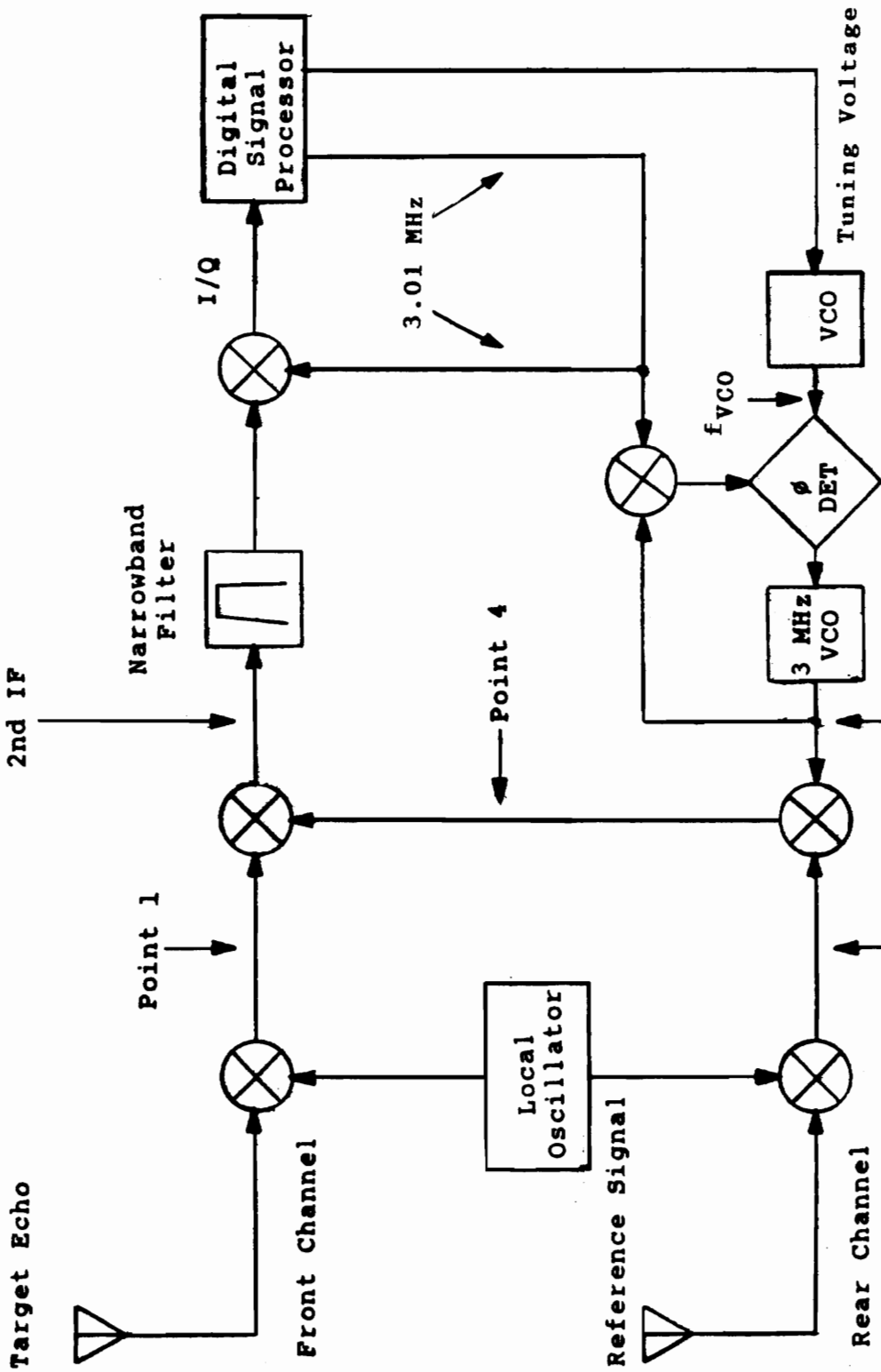

Figure 2.2 Block diagram of the missile guidance section.

quency shift from the target to missile and f_{illt} is the doppler frequency shift from the illuminator to the target. Similarly, the reference signal frequency from the illuminator, received by the rear antenna and processed in the rear channel, is given by

$$f \text{ of Reference Signal} = f_{ill} - f_{illm} \qquad (2.4)$$

where f_{illm} is the illuminator to missile doppler which decreases at the rate of separation.

To maintain signal coherency, the same fixed local oscillator is used to downconvert the front and rear signals to the system first intermediate frequency (IF). The resulting front and rear signals at points 1 and 2 of Figure 2.2 have frequencies given by

$$f \text{ at Point 1} = 1\text{st IF} - (f_{tm} + f_{illt}) \qquad (2.5)$$

$$f \text{ at Point 2} = 1\text{st IF} + f_{illm} \qquad (2.6)$$

The rear signal is then up-converted by mixing with the signal at point 3. The signal frequency at point 3 is the system second IF minus the VCO output frequency. The resulting frequency at point 4 is the sum of frequencies at points 2 and 3 :

$$f \text{ at Point } 4 = (1st\ IF + f_{illm}) + (2nd\ IF - f_{vco}) \qquad (2.7)$$

The second IF frequency is created by taking the difference between the signal frequencies at points 4 and 1 :

$$2nd\ IF = \text{frequency at Point } 4 - \text{frequency at Point } 1 \qquad (2.8a)$$

Substituting Equation (2.5) and Equation (2.7) into Equation (2.8a) yields the expression for the second IF:

$$2nd\ IF = [1st\ IF + f_{illm} + 2nd\ IF - f_{vco}] - [1st\ IF - (f_{tm} + f_{illt})] \qquad (2.8b)$$

Cancelling like terms and rearranging Equation (2.8b) yields an expression for the VCO output frequency in terms of the doppler frequencies:

$$f_{vco} = f_{tm} + f_{illt} + f_{illm} \qquad (2.9)$$

Therefore, the output frequency of the VCO represents the sum of the doppler frequency shifts from the target to missile, from the illuminator to target, and from the illuminator to missile.

The second IF signal is then passed through the

noise limiting, narrowband doppler filter and is further downconverted to a baseband. To maintain signal coherency in the frequency control loop, the local oscillator signal used to create the baseband is also used as a reference signal for the VCO. The baseband signal is broken into its in - phase (I) and quadrature (Q) components. The I and Q components of the signal are sampled, digitized, and sent to the digital signal processor. In the digital signal processor the amplitude and phase of the I and Q components are used to determine the angular location of the target with respect to the missile. Also, a Fast Fourier Transform is performed to measure the signal frequency. The digital signal processor uses the frequency information to send a tuning voltage to the VCO such that the second IF signal is centered in the doppler filter. During missile flight the relative target position and velocity constantly change, and the VCO must be continuously tuned to maintain target lock.

The target to missile doppler shift can be determined by rearranging Equation (2.9) as

$$f_{tm} = f_{vco} - f_{illt} - f_{illm} \qquad (2.10)$$

where f_{illt} and f_{illm} are determined by the illuminator radar.

The doppler information is then transmitted to the missile. The frequency of the VCO is computed in the missile's on board computer by

$$f_{VCO} = (K \cdot V_t) + 10.0 \text{ kHz} \qquad (2.11)$$

where K is the nominal frequency to tuning voltage slope of the VCO, V_t is the tuning voltage sent from the digital signal processor, and the last term in Equation (2.11) is a fixed offset frequency. Both the slope K of the VCO and the frequency offset are precisely adjusted during production test. In computing f_{vco} the computer assumes the slope of the VCO is linear over the entire tuning range of the VCO. Any nonlinearity in the frequency to tuning voltage characteristic of the VCO compromises the accuracy of the f_{vco} computation. The nonlinearity directly compromises the accuracy of the determination of the target to missile doppler shift f_{tm}, and thus the compromises the accuracy of the target to missile velocity v_{tm} computation.

CHAPTER 3

VCO ANALYSIS

INTRODUCTION

In this chapter the VCO theory of operation is discussed by providing circuit descriptions at both the circuit card level and at the VCO chip level. In the Circuit Investigation subsection a detailed circuit analysis is performed on the input circuit, the CA3096 transistor array and the current mirror which culminates in a computer model of the VCO.

CIRCUIT CARD OPERATION

The VCO is mounted on a circuit card assembly in the Guidance Section. Figure 3.1, on the next page, shows a basic block diagram of the VCO with its associated circuitry on the circuit card assembly. As shown, the output signal of the VCO provides an input to the phase locked loop. The phase locked loop stabilizes and offsets the output frequency of the 3 MHz VCO. As the VCO is tuned the phased locked loop output frequency f_{out} is offset from 3 MHz by the frequency f_{VCO}. The 3 MHz VCO is coarse tuned from the tuning voltage provided from the digital signal processor, and then fine tuned by the phase locked loop. The tuning voltage from the digital signal

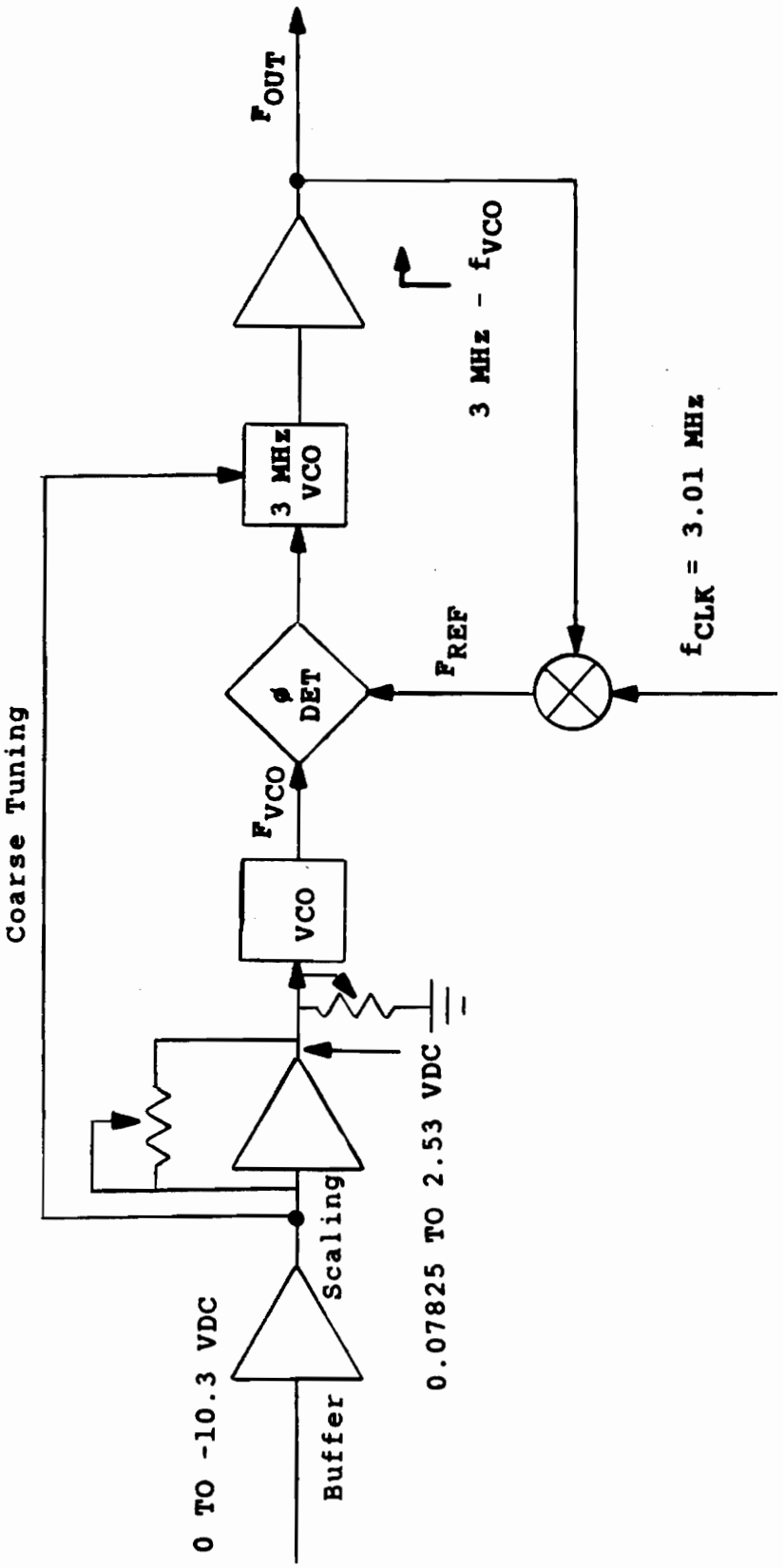

Figure 3.1 Block diagram of VCO on circuit card assembly.

processor varies from 0 Vdc to -10.3 Vdc . The tuning voltage is buffered and used to coarse tune the 3 MHz VCO and is also scaled down in the scaling amplifier to tune the VCO. Two potentiometers are used to adjust the frequency-to-tuning voltage characteristic of the VCO. One potentiometer controls the slope, while another potentiometer controls the absolute frequency offset of the VCO. Both potentiometers are adjusted during production test for the specified output frequency f_{VCO} versus input tuning voltage. The output frequency of the VCO is given by

$$f_{VCO} = |K \cdot V_t| + 10.0 \text{ kHz} \qquad (3.1)$$

where K is the slope, V_t is the input tuning voltage, and the 10.0 KHz term is the specified frequency offset when the tuning voltage is set to zero volts. Note that the absolute value of the product of K and V_t is considered since the tuning voltage V_t is negative. As mentioned earlier, the output of the VCO is phase - compared to the reference signal f_{ref} of the phase locked loop as shown in Figure 3.1. When the loop is locked the signal frequency f_{ref} is equal to the output frequency of the VCO f_{vco}, and therefore f_{ref} can be expressed as

$$f_{ref} = |K \cdot V_t| + 10.0 \text{ kHz} \qquad (3.2)$$

The signal f_{clk} is a crystal - controlled clock signal derived from the Digital Signal Processor and is set to 3.010 MHz. As shown, the reference signal f_{ref} for the loop represents the difference between f_{clk} and f_{out} and Equation (3.2) then becomes

$$f_{ref} = f_{clk} - f_{out} = |K \cdot V_t| + 10.0 \text{ kHz} \quad (3.3)$$

and since $f_{clk} = 3.010$ MHz Equation (3.3) becomes

$$3.010 \text{ MHz} - f_{out} = |K \cdot V_t| + 10.0 \text{ kHz} \quad (3.4)$$

Subtracting 10.0 kHz from both sides of Equation (3.4) yields

$$f_{out} = 3.0 \text{ MHz} - |K \cdot V_t| \quad (3.5)$$

Therefore, the frequency of the output signal f_{out} is offset from 3 MHz as the VCO is tuned.

VCO CIRCUIT OPERATION

The schematic diagram of the VCO is shown in Figure 3.2. Additionally, the voltage waveforms at various points around the circuit are shown in Figure 3.3.

The VCO is basically a tunable astable multivibrator. As shown in Figure 3.2 the tuning voltage is ap-

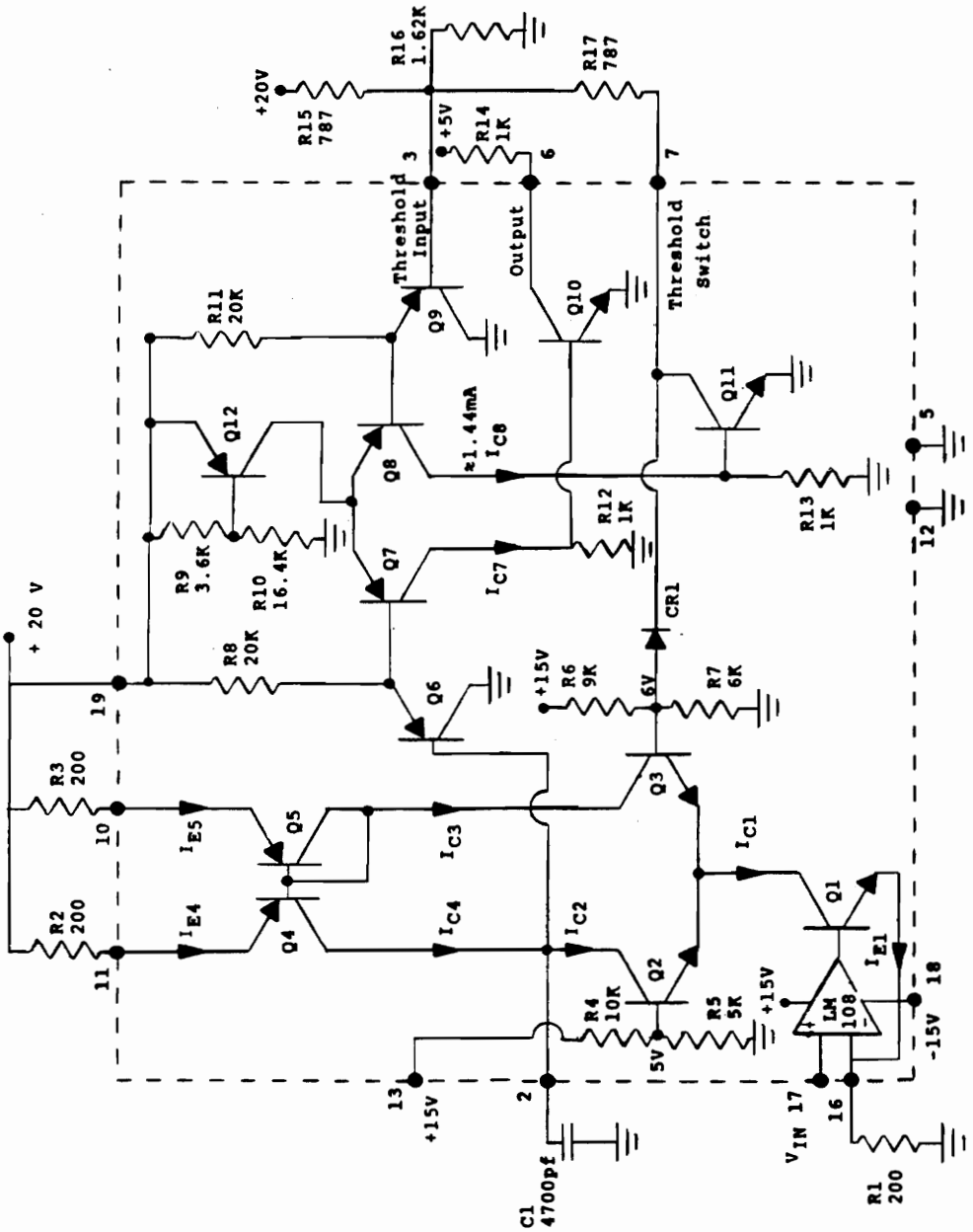

Figure 3.2 Schematic diagram of the VCO

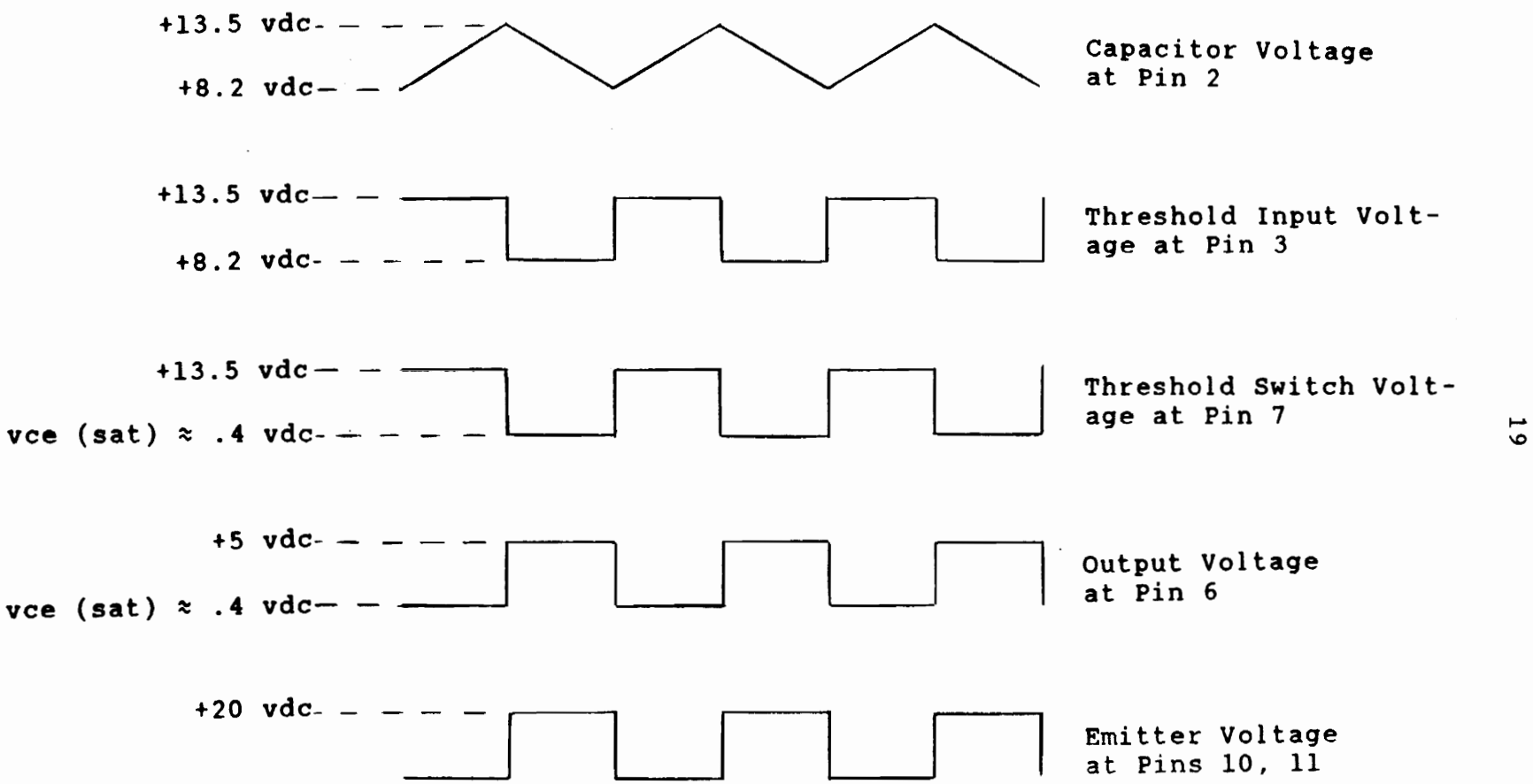

Figure 3.3 Voltage waveforms at various points in the VCO.

plied to the VCO at pin 17, the noninverting input of the LM 108 operational amplifier (OP AMP). The OP AMP is configured as a constant current amplifier with transistor Q1 in the feedback path. Because of negative feedback, both inputs of the OP AMP are essentially at the same potential; it follows that the tuning voltage is applied across the 200 Ω external resistor R1, which is called the current sense resistor. The emitter current I_{E1} for Q1 is equal to the current through R1 and the collector current I_{C1} for Q1 is $\alpha \cdot I_{E1}$. The current I_{C1} flows through the differential pair Q2-Q3 and through the current mirror Q4-Q5 in order to charge the timing capacitor C1. The time required to charge the timing capacitor is a function only of the current at the output of the current mirror I_{C4}. Similarly, the time required to discharge the timing capacitor is a function of the collector current I_{C2}. Collector currents I_{C4} and I_{C2} are not necessarily equal, therefore the charge and discharge times of the timing capacitor are unequal.

The bases of Q2 and Q3 are biased by resistor networks to 5 vdc and 6 vdc respectively. Therefore, when power is initially applied to the circuit, transistor Q3 is turned on while transistor Q2 is turned off. The collector current I_{C3} flows through Q3 providing the reference current for the current mirror Q4-Q5 . Since transistor Q2 is turned off, the output current of the current mirror I_{C4} charges the timing

capacitor C1. The voltage across the timing capacitor starts to rise as shown by the first waveform in Figure 3.3.

The voltage across the timing capacitor is applied to the base of transistor Q6. The base of Q6 provides one input of the Darlington differential pair formed by transistors Q6, Q7, Q8, and Q9 shown in Figure 3.2. The other input of the differential pair is referred to as the threshold input formed by the resistor network R15, R16 and R17. When the timing capacitor is charging the threshold input is set to its high voltage limit by

$$V_{high} = 20\ Vdc \cdot \frac{R16}{R16 + R15} \qquad (3.6)$$

and is approximately equal to 13.5 Vdc. When the rising voltage across the timing capacitor is less than 13.5 Vdc, transistors Q8 and Q9 are turned off while Q6 and Q7 are turned on. Collector current I_{C7} flows, which biases transistor Q10 on and sets the output of the oscillator to about 0.4 Vdc.

When the rising capacitor voltage just exceeds the 13.5 Vdc high threshold limit, transistors Q6 and Q7 are turned off and Q8, Q9 are turned on. Consequently, collector current I_{C7} ceases to flow, and transistor Q10 is turned off pulling the output of the oscillator to about 5 Vdc. Since Q8

is on, collector current I_{C8} turns transistor Q11 on thus pulling the collector potential down to approximately 0.4 Vdc (vce sat).

The low voltage potential at the collector of Q11 has two effects on the circuit operation. First, it changes the state of the threshold input voltage at pin 3 by now providing a current path through resistor R17. The low voltage limit of the threshold input voltage is determined by

$$V \text{ low} = \frac{20 \text{ Vdc/R15} + 0.4 \text{ Vdc/R17}}{1/R15 + 1/R16 + 1/R17} \qquad (3.7)$$

which is approximately equal to 8.2 Vdc. Secondly, it causes diode CR1 to conduct, forcing the base of transistor Q3 to about 1.1 Vdc, which turns off Q3 allowing Q2 to turn on. Transistor Q2 now provides a path for the timing capacitor to discharge. When the capacitor voltage decreases to about 8.2 Vdc, transistors Q6 and Q7 turn on and Q8 and Q9 turn off and the cycle repeats. The threshold input voltage returns to 13.5 Vdc and the output of the oscillator returns to a low state once again.

The output frequency of the VCO can be derived from

$$i = C \cdot \frac{dv}{dt} \qquad (3.8)$$

which states that the current through a capacitor is equal to the value of the capacitance multiplied by the rate of change of the voltage across the capacitor with time. Because i and dv/dt are constant while the capacitor is charging, Equation (3.8) may be integrated over the charging interval and rearranged to find the charge time given by

$$T\ charge = \frac{C1 \cdot \Delta v}{I_{C4}} \qquad (3.9a)$$

where I_{C4} is the collect current of transistor Q4, C1 is the timing capacitance equal to 4700 pf, and Δv is the difference between the threshold high and threshold low voltage levels which is approximately equal to 5.2 Vdc. Similarly, the time required to discharge the timing capacitor is

$$T\ discharge = \frac{C1 \cdot \Delta v}{I_{C2}} \qquad (3.9b)$$

where C1 and Δv are the same as before and I_{C2} is the collector current of transistor Q2. The charge and discharge times are not equal since I_{C4} is not equal to I_{C2}. Actually, as will be shown later, I_{C4} is greater than I_{C2}, therefore the discharge time exceeds the charge time. The output frequency of the VCO is equal to the reciprocal of the sum of the charge

and discharge times:

$$f_{VCO} = \frac{1}{T\ charge + T\ discharge} \qquad (3.10)$$

Substituting Equation (3.9a) and Equation (3.9b) into Equation (3.10) yields the equation for the output frequency of the VCO

$$f_{VCO} = \frac{I_{C4} + I_{C2}}{C1 \cdot \Delta v} \qquad (3.11)$$

The currents I_{C4} and I_{C2} are functions of the input tuning voltage. Any nonlinearity in the current-to-tuning voltage characteristic results in a nonlinearity in the frequency-to-tuning voltage characteristic. The parameters C1 and Δv are invariant to changes in the tuning voltage, therefore the following circuit investigation is limited to sources of the current nonlinearities.

CIRCUIT INVESTIGATION

This section discusses a detailed circuit analysis combining empirical and numerical methods to determine the source of the nonlinearities. The circuit analysis leads to a computer model that expresses the output currents and thus the output frequency, as a function of the input tuning

voltage.

INPUT CIRCUIT ANALYSIS

The obvious place to start any investigation is at the beginning, or in this case at the input of the circuit. As shown in Figure 3.1, the tuning voltage from the Digital Signal Processor is modified and scaled through a buffer/ scaling amplifier before being applied to the VCO. The buffer/scaling amplifier is a hybrid device, consisting of three operational amplifiers and a few scaling resistors, which is mounted on the same circuit card assembly as the VCO. A plot of the measured output voltage versus input voltage of the buffer/scaling amplifier is shown in Figure 3.4. Moreover, a difference plot from the best fit straight line is shown in Figure 3.5 indicating no real nonlinearity. The rolloff in Figure 3.5 is compensated when the initial adjustments are made to both offset and gain and is therefore not a source of the frequency nonlinearity.

The equivalent circuit diagram of the OP AMP and its associated circuitry is shown in Figure 3.6. As shown, the OP AMP is configured as a constant current amplifier [Irvine, 1981]. The nonlinear load resistor R_L represents the base - emitter junction of transistor Q1. Resistor R1 is the current sense resistor. The linearity of the circuit can be determined simply by measuring the difference between the

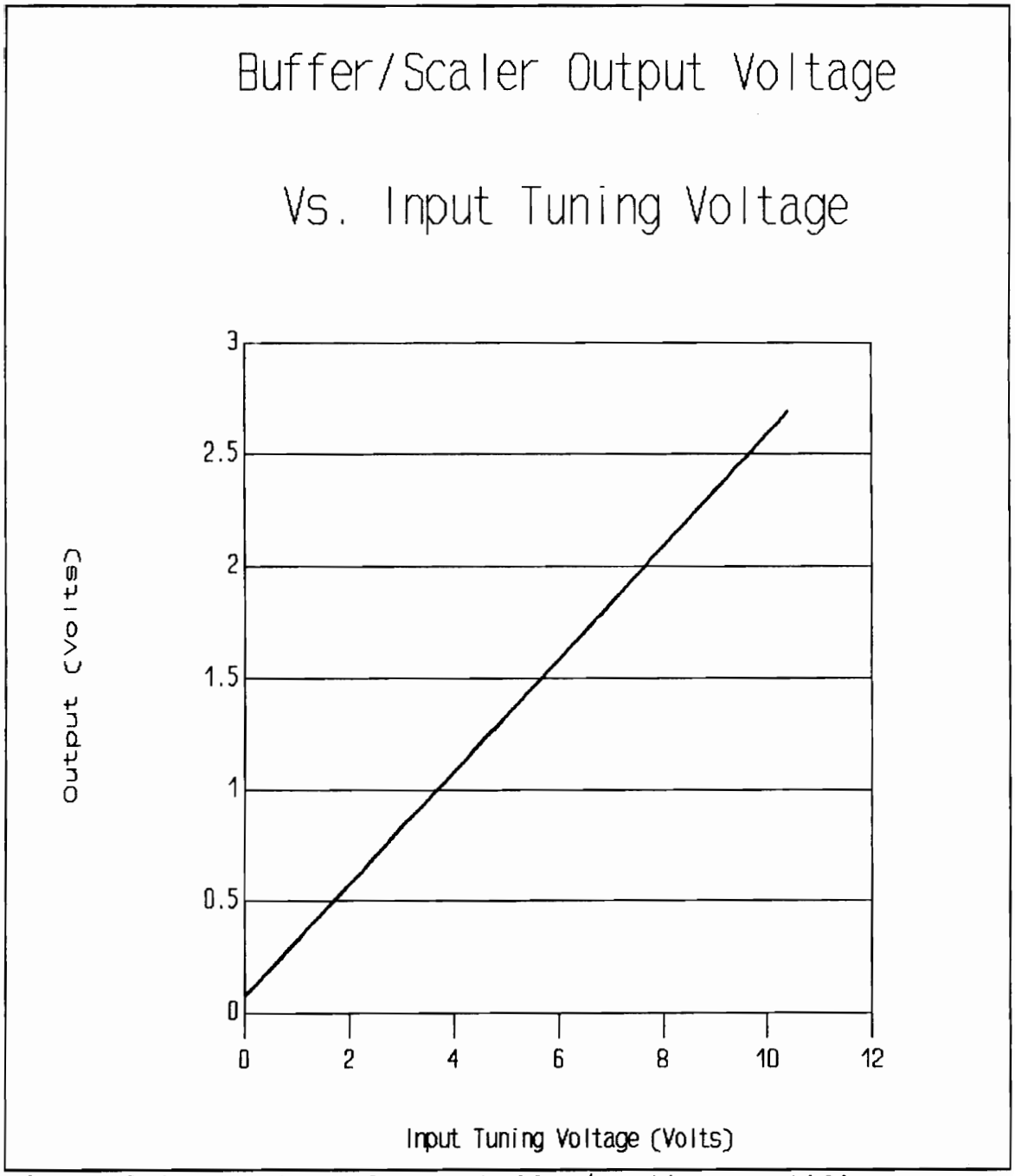

Figure 3.4 Plot of the buffer/scaling amplifier output voltage versus the input tuning voltage.

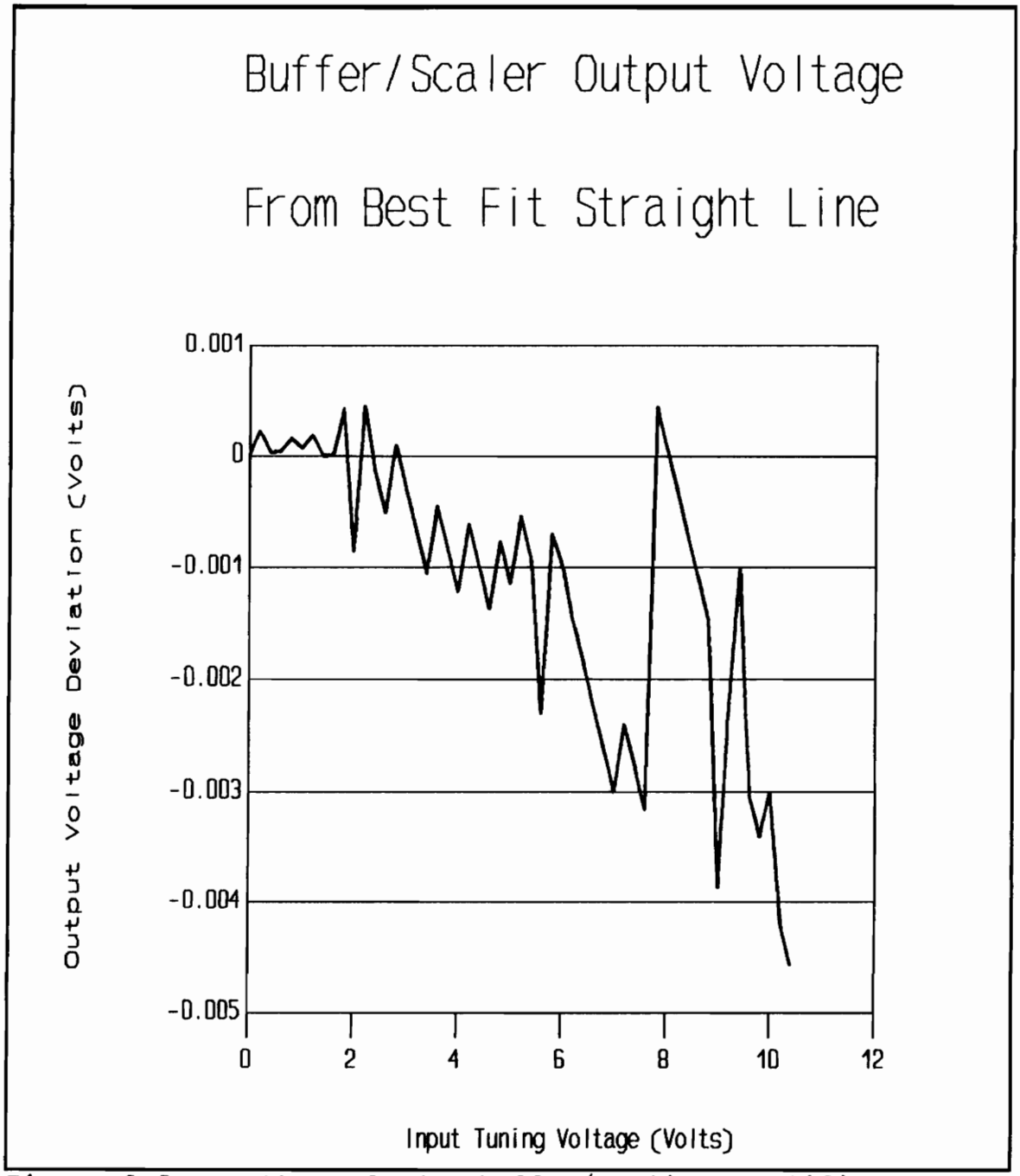

Figure 3.5 Plot of the buffer/scaling amplifier output voltage subtracted from a best fit straight line versus the input tuning voltage.

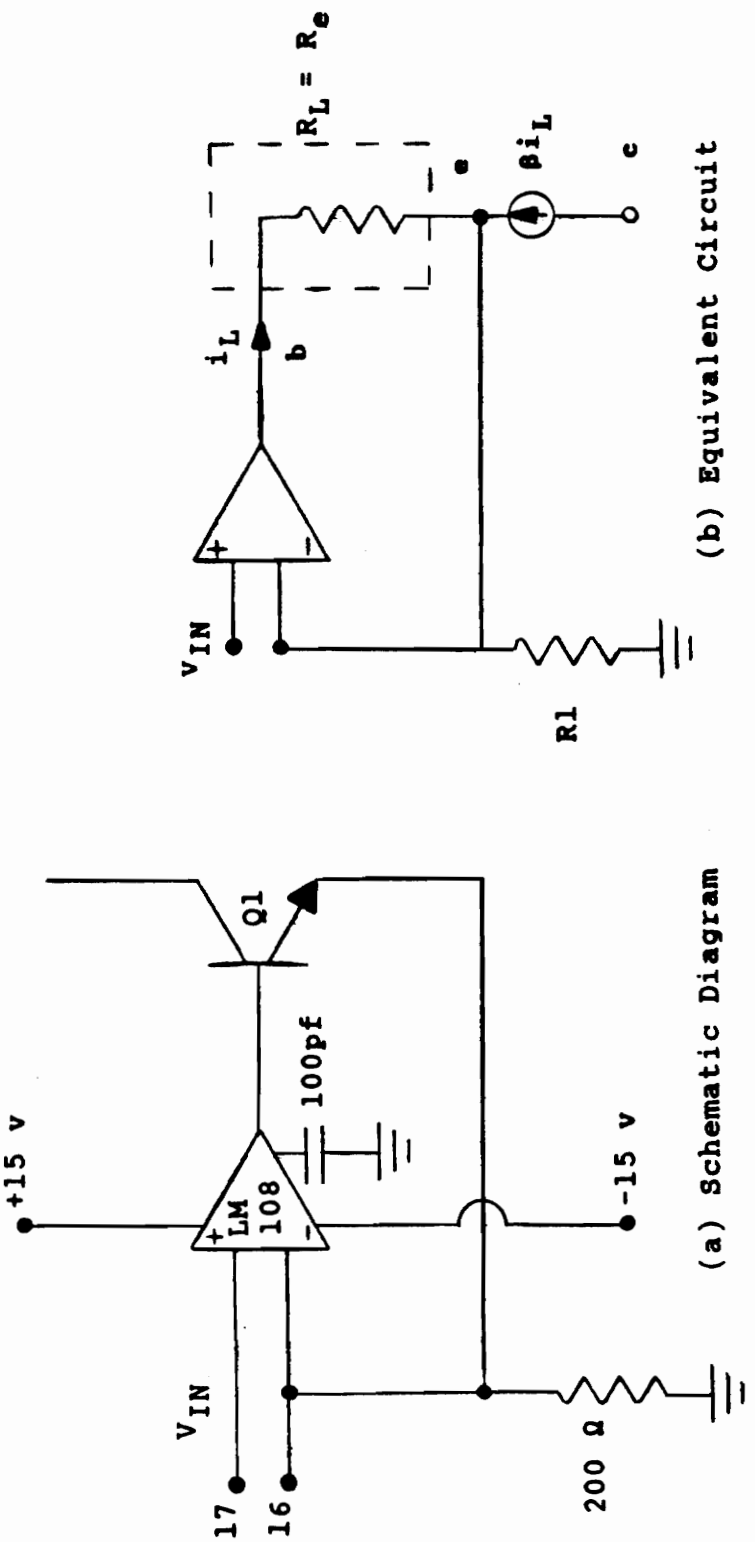

Figure 3.6 Schematic diagram and equivalent circuit of the constant current amplifier.

input voltages at pin 17 and pin 16. As shown in Figure 3.7 the measured difference between pins 16 and 17 is quite small which is sufficient proof that the OP AMP/transistor feedback path is operating linearly.

The output voltage of the OP AMP is the sum of the base - emitter voltage Q1, which is typically 0.7 Vdc and the voltage across R1, which is V_{IN}. The maximum input voltage V_{IN} is approximately 2.6 Vdc. Consequently, the maximum output voltage of the OP AMP is approximately 3.3 Vdc which is well below the rated output saturation voltage of 13 Vdc [National Semiconductor, 1982]. Since the buffer/scaling amplifier provides a linear input voltage to the VCO and the constant current amplifier is operating linearly, the next step is to investigate the CA3096 transistor array and the current mirror for any nonlinearities.

COMPUTER MODEL

The remainder of the circuit analysis is better approached through numerical methods than through hand computations. In order to determine the sources of nonlinearities a computer program was written in Fortran using double precision. A flow diagram of the computer model is provided in Figure 3.8, and a program listing is provided in the Appendix.

The computer model increments the input tuning voltage in 0.2 Vdc steps over its dynamic range. The buf-

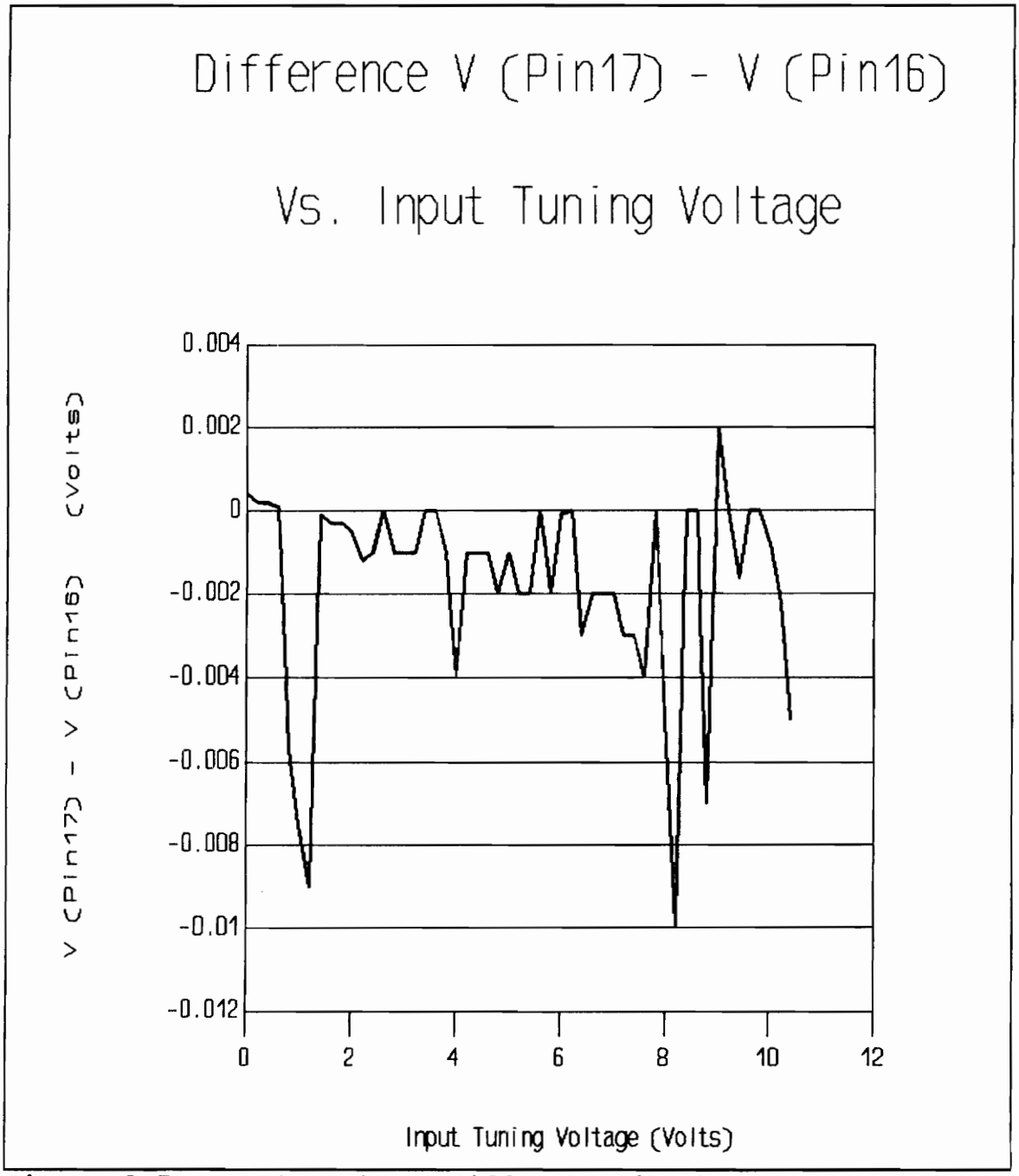

Figure 3.7 Plot of the difference in the measured voltage at pin 17 and pin 16 of the VCO.

fer/scaling amplifier is modeled by adjusting the offset and gain of the input tuning voltage via the keyboard entry when prompted. The emitter current of Q1 is computed by dividing the scaled input voltage by R1, the 200 Ω current sense resistor. A model for the CA3096 transistors Q1, Q2 and Q3 is developed using a piecewise linear approximation to the variation of current gain versus applied current. The current I_{E1} is modified by the current gain of transistors Q1 and Q2 to give I_{C2}, which is used to compute the discharge time of the timing capacitor by using Equation (3.9b). Current I_{C3} is then set equal to I_{C2}. A model for the current mirror circuit is developed which further modifies the current I_{C3} to give I_{C4} which is used to compute the charge time of the timing capacitor using Equation (3.9a). The output frequency is computed using Equation (3.11). The simulated frequency deviation is then plotted versus the input tuning voltage.

CA3096 TRANSISTOR ANALYSIS

Transistors Q1, Q2, Q3 and Q12 as shown in the schematic diagram of Figure 3.2 are contained in the CA3096 transistor array. The CA3096 is a general purpose high voltage silicon transistor array. Each array consists of five independent transistors (two p-n-p and three n-p-n) on a common substrate. In particular, critical to circuit operation is the dynamic behavior of the current gain β of Q1, Q2 and

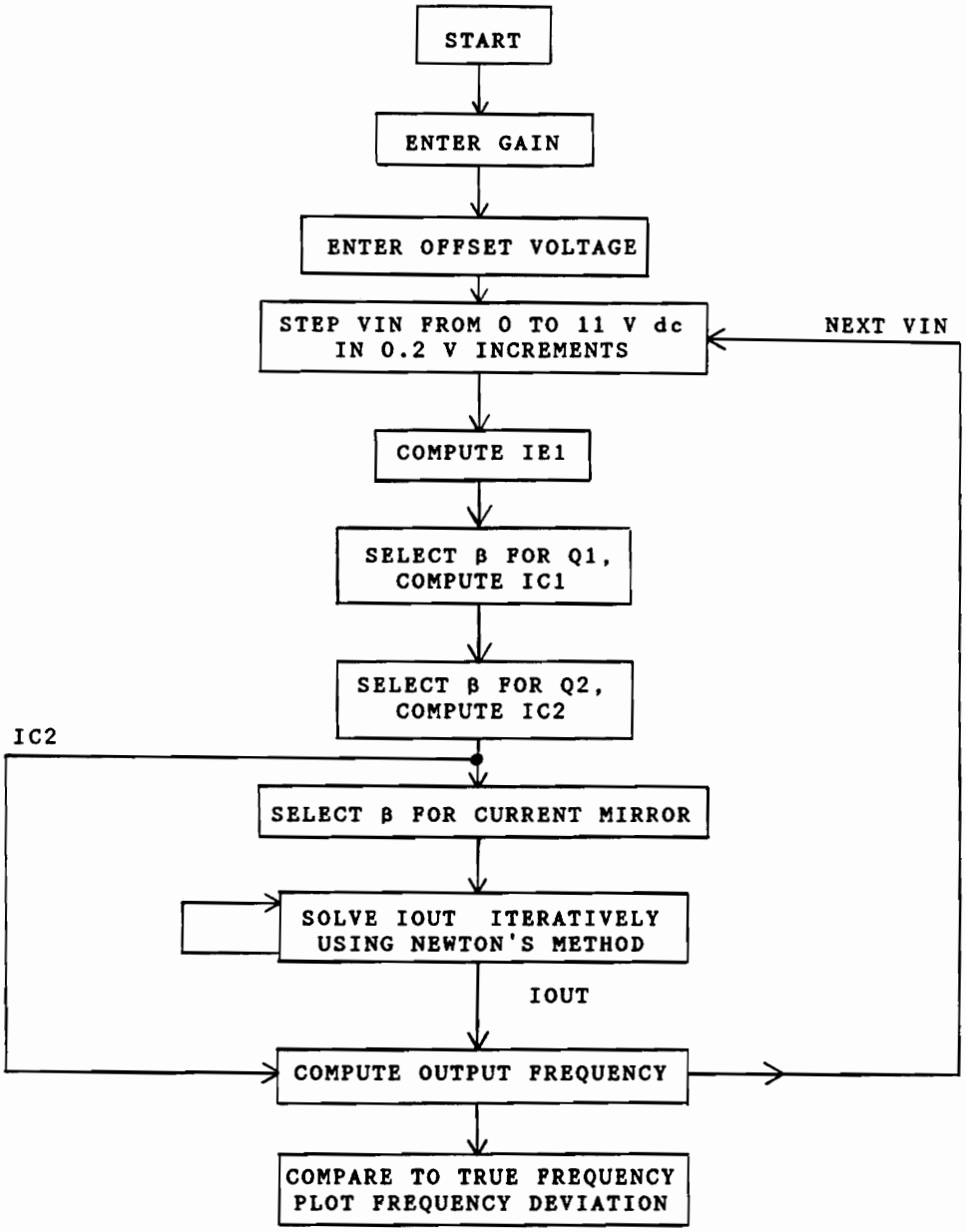

Figure 3.8 Flow diagram of the computer model for the VCO.

Q3. Although transistor Q12 is contained in the CA3096, its performance is not as critical as that of the other three transistor since it operates statically.

It is well documented [Gray-Meyer, 1977] that the current gain β is not a constant function of current drive level. Shown in Figure 3.9 [RCA, 1974] is a plot of transistor current gain β as a function of collector current for the CA3096 transistor array. The shape of the plot in Figure 3.9 is typical for n-p-n integrated-circuit transistors. As shown, there are three regions of operation. At low current levels in region I, β increases with increased current and is proportional to the square root of the collector current. At mid-level currents, in region II, β is considered to be fairly constant as a function of collector current. At higher current levels, in region III, β decreases rapidly with increasing collector current, and is approximately proportional to 1/Ic.

The reasons for the variations of β with current can be better appreciated by plotting base and collector currents on a log scale as functions of V_{be}. This plot is shown in Figure 3.10 [Gray-Meyer, 1977] and, because of the log scale on the vertical axis, the value of (ln β) can be obtained directly as the distance between the two curves. At moderate current levels in region II both the collector and base cur-

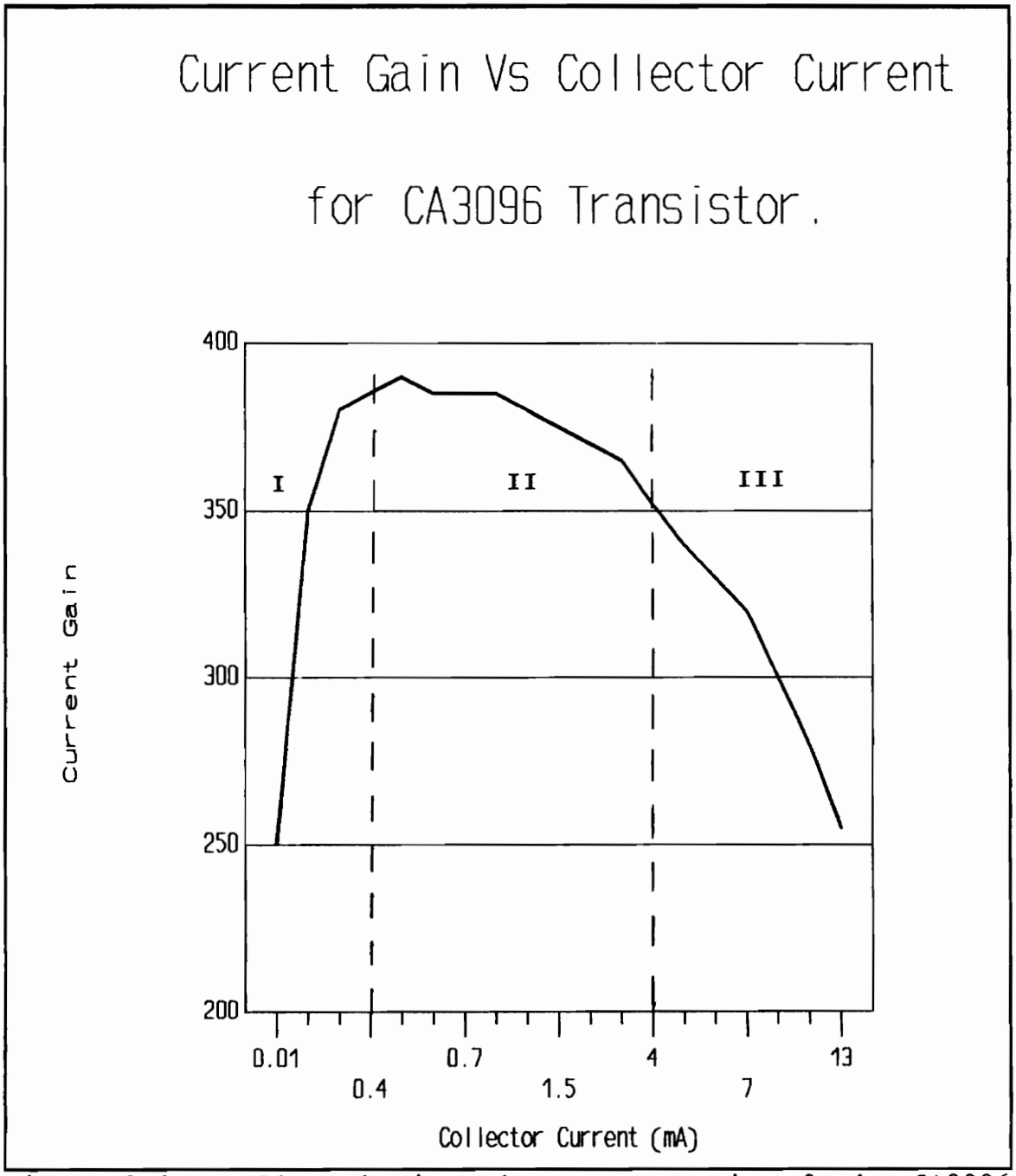

Figure 3.9 Plot showing the current gain of the CA3096 versus the applied collector current. Also shown are the three region of the current gain.

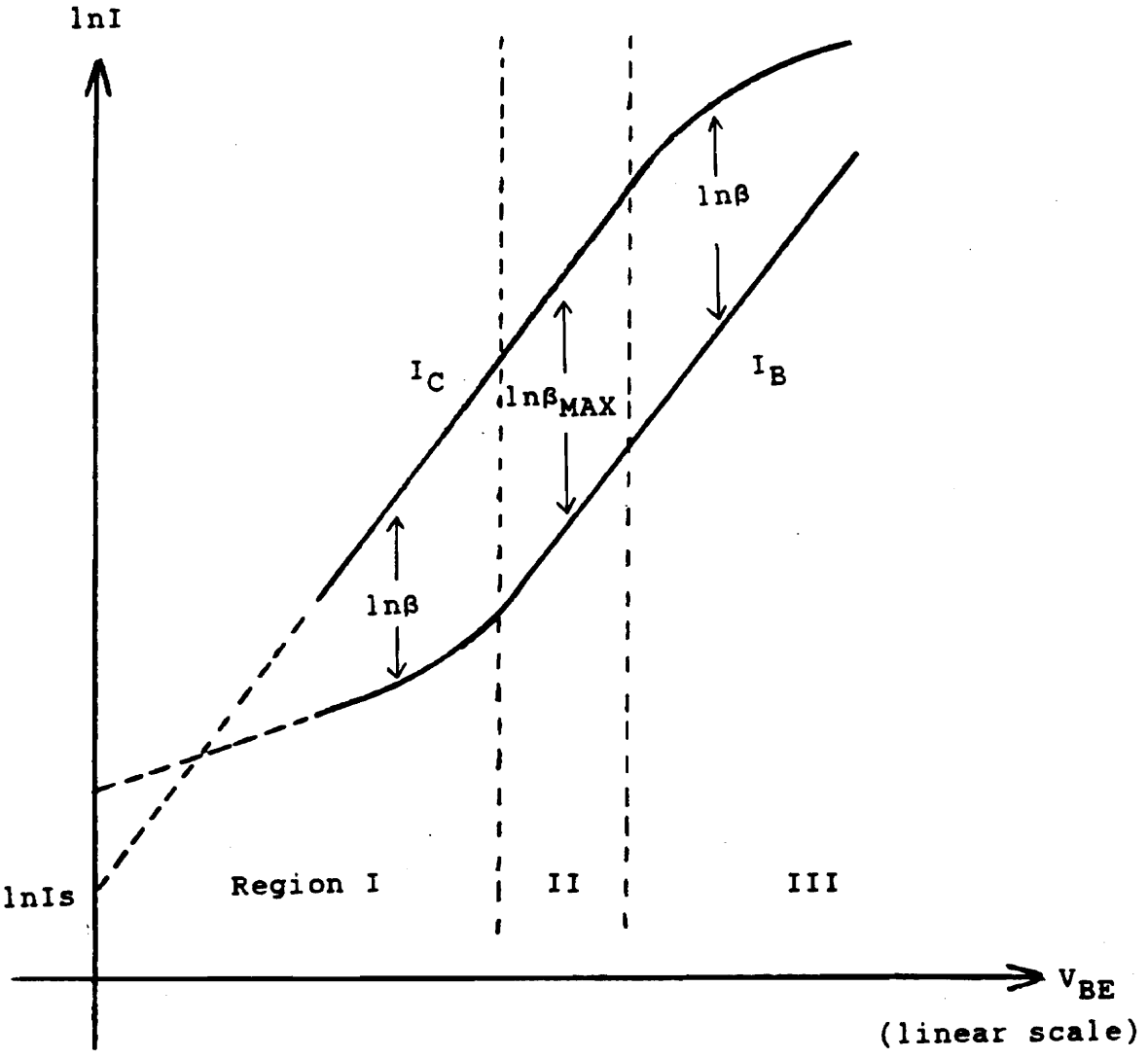

Figure 3.10 Collector current and base current plotted on a log scale versus Vbe on a linear scale. The distance between the curves is a direct measurement of ln β

rents follow the ideal behavior

$$I_C = I_S \cdot \exp \frac{V_{be}}{V_t} \tag{3.12}$$

$$I_B \approx \frac{I_S}{\beta_{max}} \exp \frac{V_{be}}{V_t} \tag{3.13}$$

where β_{max} is the maximum value of β, I_S is the emitter saturation current and $V_t = kT/q$ where

$$k = \text{Boltzmann constant} = 1.38 \times 10^{-23} \text{ J/K}$$

$$q = \text{electronic charge} = 1.602 \times 10^{-19} \text{ C}$$

and

$$T = \text{Kelvin Temperature.}$$

A typical value for V_t is to 25 mV at room temperature.

At low current levels, the collector current still follows the ideal relationship of Equation (3.12); however, the decrease in β is due to an additional component in the base current which is due to recombination of carriers in the base-emitter depletion region that is present at all current levels. The base current resulting from recombination in the

depletion region is

$$I_{BX} \approx I_{SX} \cdot \exp \frac{V_{be}}{mV_t} \qquad (3.14)$$

where $m \approx 2$ and I_{SX} is the emitter saturation current in the depletion region. At low current levels this additional current dominates the base current, and the current gain can be computed from Equation (3.12) and Equation (3.14) as

$$\beta \approx \frac{I_C}{I_{BX}} = \frac{I_S}{I_{SX}} \exp\left[\frac{V_{be}}{V_t} \left(1 - \frac{1}{m} \right) \right] \qquad (3.15)$$

Substitution of Equation (3.12) into Equation (3.15) yields

$$\beta \approx \frac{I_S}{I_{SX}} \cdot \frac{I_C}{I_S}^{[1-(1/m)]} \qquad (3.16)$$

Since $m \approx 2$, Equation (3.16) indicates that β is proportional to the square root of the collector current.

At higher current levels, the base current tends to follow the relationship of Equation (3.13) and the decrease in β is due mainly to a decrease in the collector current below the value given by Equation (3.12). The decrease in the

collector is due to the effect of high level injection and at high current levels the collector current approaches

$$I_C \approx I_{SH} \cdot \exp \frac{V_{be}}{2V_t} \tag{3.17}$$

where I_{SH} is the emitter saturation current at higher current levels. The current gain in this region can be computed from Equation (3.17) and Equation (3.13) as

$$\beta \approx \frac{I_{SH}}{I_S} \beta_{MAX} \exp \left[-\frac{V_{be}}{2V_t} \right] \tag{3.18}$$

Substitution of Equation (3.17) into Equation (3.18) yields

$$\beta \approx \frac{I_{SH}^2}{I_S} \beta_{MAX} \frac{1}{I_C} \tag{3.19}$$

From Equation (3.19) the current gain at high current levels decreases as a function of the reciprocal of the collector current. The VCO operates with current levels in region II and III.

To confirm these theoretical results, measurements were made on the CA3096 transistor array from an actual VCO. The lid was removed from the VCO hybrid assembly. The connection from the collector of transistor Q1 to the emitters

of Q2 and Q3 was broken and a pair of bond wires were attached to unused pins 1 and 8 for monitoring. A measurement of the collector current versus emitter current was performed to ascertain the current gain β of Q1. A DC ammeter was connected across pins 1 and 8 to measure the collector current of Q1 while the emitter current was varied. The ratio of the measured emitter and collector currents can be computed to yield

$$\alpha = \frac{I_C}{I_E} \tag{3.20}$$

and since

$$\alpha = \frac{\beta}{\beta + 1} \tag{3.21}$$

then

$$\beta = \frac{\alpha}{1 - \alpha} \tag{3.22}$$

and therefore

$$\beta = \frac{I_C}{(I_E - I_C)} \tag{3.23}$$

The current gain β was computed from Equation (3.23) using the measured emitter and collector currents and is plotted in

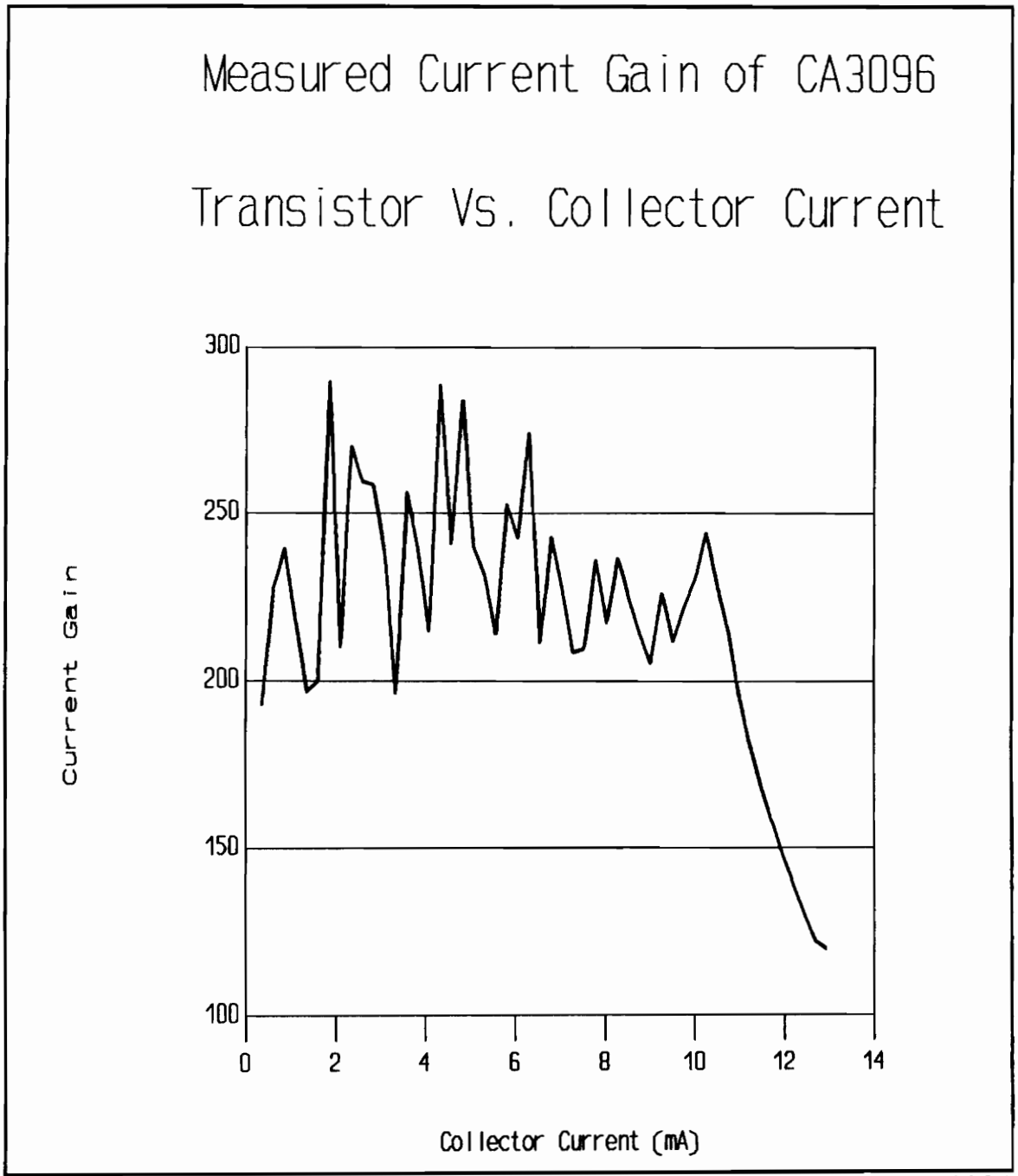

Figure 3.11 Plot of measured current gain of CA3096 transistor versus collector current.

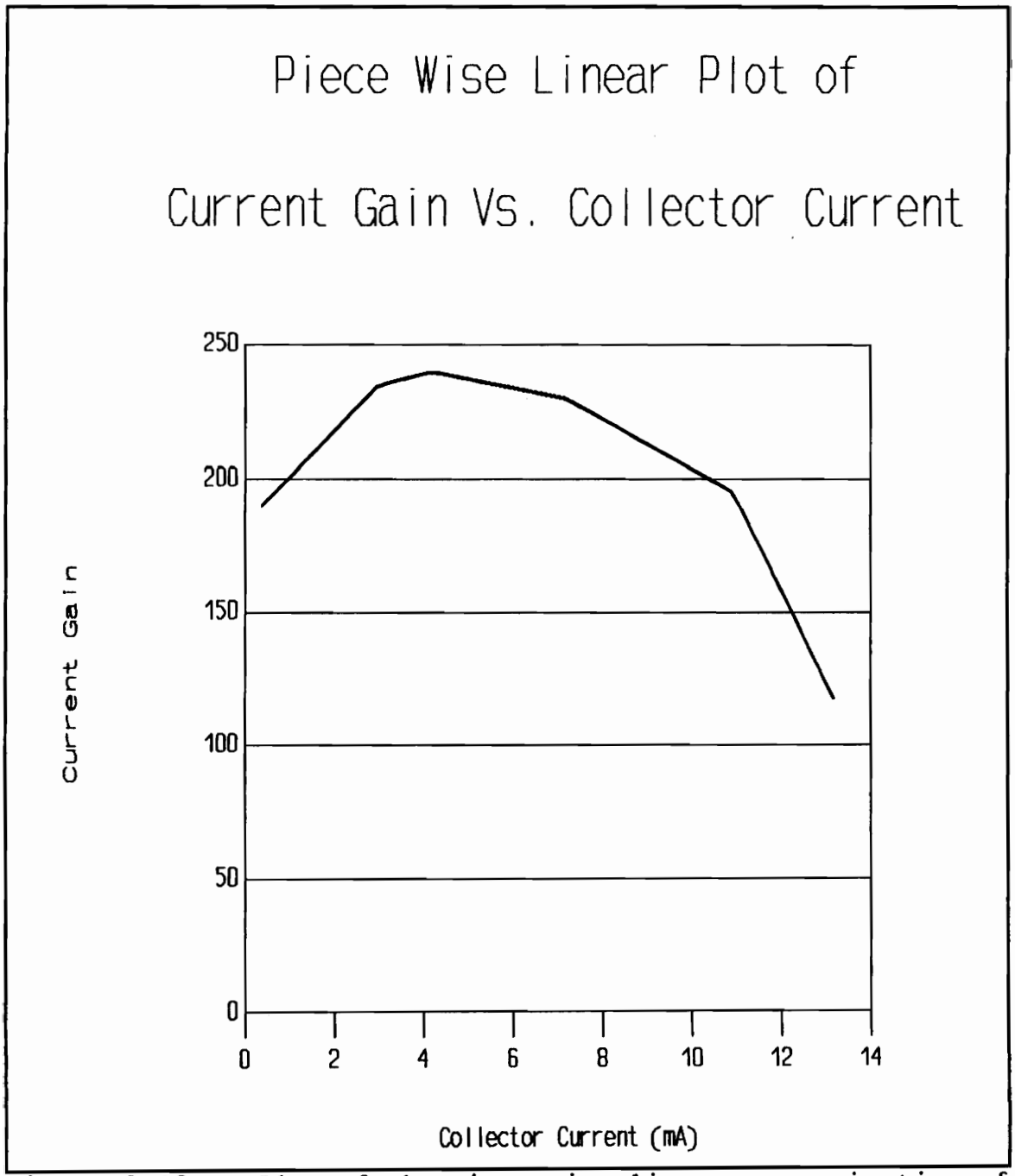

Figure 3.12 Plot of the piece wise linear approximation of measured current gain versus collector current used by the computer model.

Figure 3.11 on page 40. However, for simplicity the computer model uses a piecewise linear curve to approximate the measured current gain, as shown in Figure 3.12 on page 41. As mentioned before, the scaled input voltage is incremented in 0.2 Vdc steps. The emitter current I_{E1} of transistor Q1 is computed by dividing each input voltage by 200 Ω. The collector current I_{C1} of Q1 is equal to $\alpha \cdot I_{E1}$ where α is computed from the appropriate value of β using Equation (3.21). The collector current I_{C3} for Q3 is computed and is equal to $\alpha \cdot I_{C1}$. In the computer program collector current I_{C2} for transistor Q2 is set equal to I_{C3}. Current I_{C2} is used to compute the discharge time of the timing capacitor by using Equation (3.9b). Current I_{C3} is then used as the reference current for the current mirror, which will now be analyzed.

CURRENT MIRROR ANALYSIS

The current mirror circuit shown in Figure 3.13 is a common circuit that is fairly well documented in textbooks [Holt, 1978],[Gray-Meyer, 1977]. However, most textbooks tend to simplify their analysis resulting in a model that does not reflect the actual operation of the circuit. The simplified analysis asserts that the output current I_{OUT} is less than or equal to the reference current I_{REF} with equality for very large values of β. The model developed in this section as well as actual measurements show that the output current is

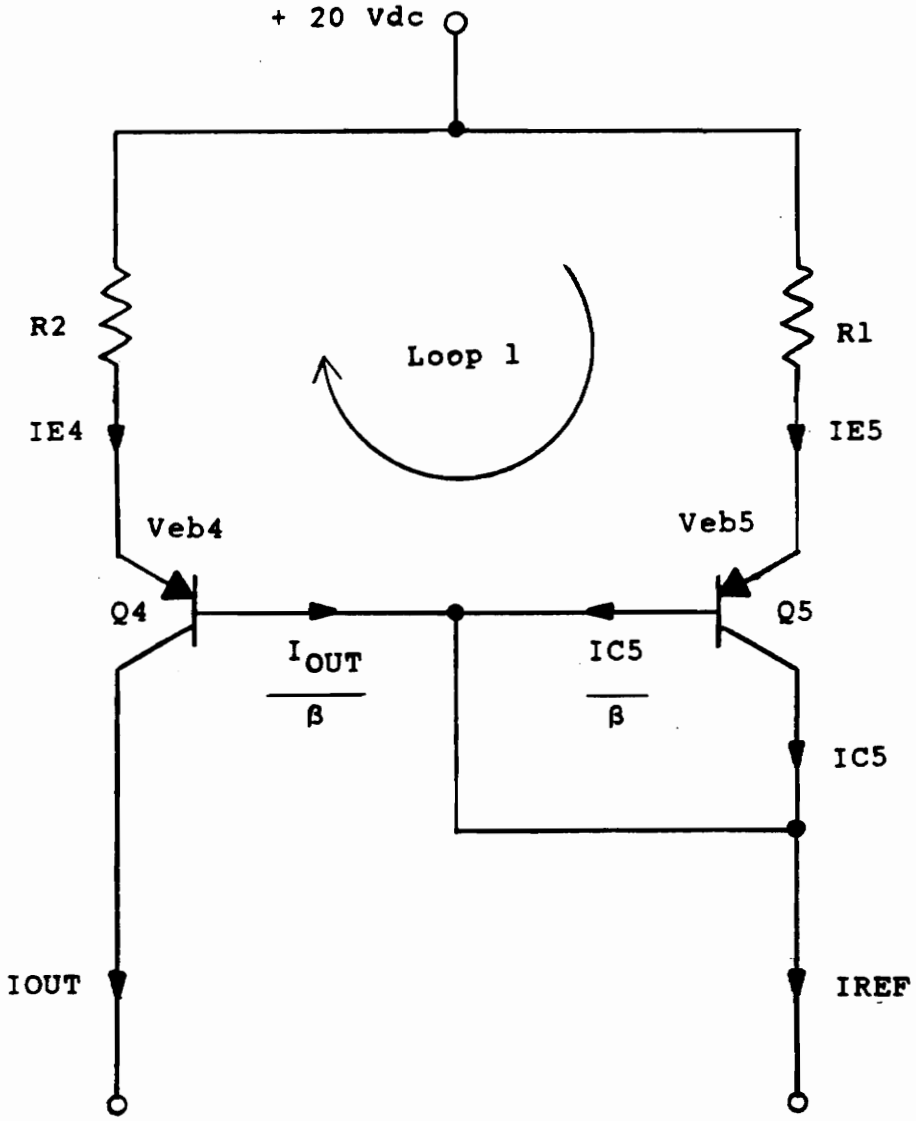

Figure 3.13 Schematic diagram of the current mirror.

in fact always greater than the reference current. Also, the model and actual measurements show that the output current is not a linear function of the reference current as the reference current is varied. The nonlinearity is partly attributed to the nonlinear variation in the current gain of transistors Q5 and Q4 as the reference current is varied. This is similar to the current gain behavior of the CA3096 transistor array. Another reason for the nonlinear behavior in the output current is that transistor Q5 dissipates more power than transistor Q4 solely due to its position in the circuit. As the reference current is incremented, the power dissipation in Q4 increases more rapidly than the power dissipation in Q5. Consequently, the emitter-base voltage of Q4 decreases more rapidly than does the emitter base voltage of Q5 due to thermal affects. As the reference current increases, the difference in the emitter-base voltage of the two transistors increases, but in a nonlinear fashion. This phenomenon was observed in the laboratory while monitoring the emitter-base voltages of the current mirror in the VCO. The empirical data was then integrated into the computer model to simulate the effects of the unequal power dissipation. As will be shown, the output current is a function of the difference in the emitter-base voltages, thus resulting in the nonlinear output current.

The transistors used in the current mirror of the

VCO are 2N3811's. The 2N3811 transistors are a pair of p-n-p transistors that are fabricated on the same substrate with nearly identical parameters. The computer model developed in this section will assume the transistors are matched for current gain, saturation current, Early voltage and temperature dependence.

In the schematic diagram in Figure 3.13, the reference current I_{REF} is the same as collector current I_{C3}, which is supplied to the current mirror from the CA3096 transistor array. The output current I_{OUT} is used to compute the timing capacitor charge time. With reference to the schematic diagram of the current mirror in Figure 3.13, the reference current can be expressed as

$$I_{REF} = I_{C5} + I_{OUT}/\beta + I_{C5}/\beta \qquad (3.24)$$

where $I_{C5} + I_{C5}/\beta = I_{E5}$. Rearranging Equation (3.24) yields

$$I_{E5} = I_{REF} - I_{OUT}/\beta \qquad (3.25)$$

Similarly, the emitter current of Q4 can be expressed as

$$I_{E4} = I_{OUT} + I_{OUT}/\beta \qquad (3.26)$$

Using Kirchoff's Voltage Law and summing the voltages around loop 1 of Figure 3.13 yields

$$I_{E5} \cdot R1 + V_{eb5} - V_{eb4} - I_{E4} \cdot R2 = 0 \qquad (3.27)$$

The difference between V_{eb5} and V_{eb4} can be expressed as

$$V_{eb5} - V_{eb4} = I_{E4} \cdot R2 - I_{E5} \cdot R1 \qquad (3.28)$$

Substituting Equation (3.25) and Equation (3.26) for I_{E5} and I_{E4} respectively into Equation (3.28) yields

$$V_{eb5} - V_{eb4} = R2 \cdot (I_{OUT} + I_{OUT}/\beta) - R1 \cdot (I_{REF} - I_{OUT}/\beta) \qquad (3.29)$$

Combining similar terms simplifies Equation (3.29) to

$$V_{eb5} - V_{eb4} = I_{OUT} \cdot (R2 + R2/\beta + R1/\beta) - R1 \cdot I_{REF} \qquad (3.30)$$

Recalling that $1/\alpha = (1 + 1/\beta)$ simplifies Equation (3.30) to

$$V_{eb5} - V_{eb4} = I_{OUT} \cdot (R2/\alpha + R1/\beta) - R1 \cdot I_{REF} \qquad (3.31)$$

By rearranging Equation (3.31) the output current can now be expressed as

$$I_{OUT} = \frac{V_{eb5} - V_{eb4} + R1 \cdot I_{REF}}{R2/\alpha + R1/\beta} \qquad (3.32)$$

Expressions for V_{eb5} and V_{eb4} can be derived from the standard Ebers - Moll equation [Streetman, 1980] for the emitter current I_E

$$I_E = I_{ES} (e^{Veb/Vt} - 1) - \alpha I_{ES} (e^{Vcb/Vt} - 1) \qquad (3.33)$$

where V_t is approximately 25 mV and I_{ES} is the magnitude of the emitter saturation current.

The second term in Equation (3.33) can be neglected since V_{cb} is zero volts for transistor Q5 and less than approximately -3.3 Vdc for transistor Q4. Therefore the simplified Ebers - Moll expression for the emitter current I_E is

$$I_E = I_{ES} (e^{Veb/Vt} - 1) \qquad (3.34)$$

An additional factor must be included in Equation (3.34) since variations in collector current are dependent on variations in collector to emitter voltage V_{CE}, which results in the typical transistor output characteristics as shown in

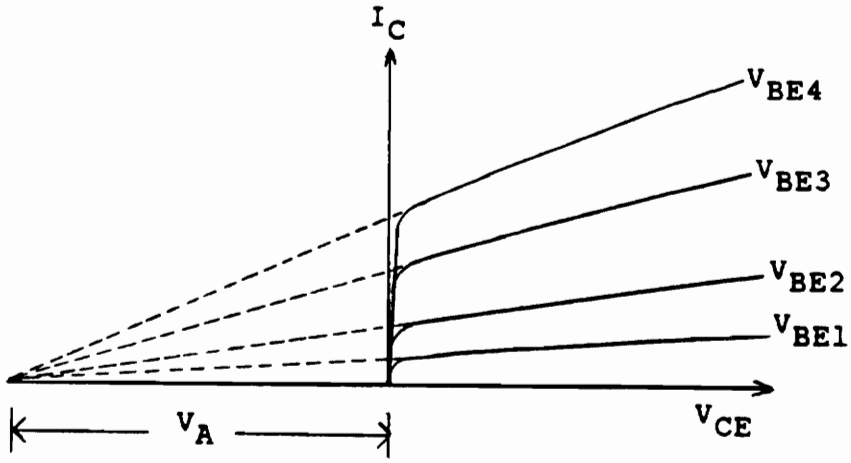

Figure 3.14 Plot showing variations in the collector current as a function of variations in the collector to emitter voltage for constnat values of base - emitter voltage.

Figure 3.14 [Gray-Meyer, 1977]. These characteristics are shown for constant values of V_{BE} and when extrapolated back to the V_{CE} axis give an intercept V_A called the Early voltage where

$$V_A = \frac{I_C}{dI_C \; / \; dV_{CE}} \tag{3.35}$$

The variation of I_C with V_{CE} is called the Early Effect. Typical values of V_A for integrated transistors are 50 to 100 Vdc. The value set for both transistors in the computer model is 100 Vdc. The influence of the Early Effect on the transistor large signal characteristics in the forward active region can be represented approximately by modifying Equation (3.34) to

$$I_E = I_{ES} \left(1 + \frac{V_{CE}}{V_A}\right) \cdot \left(e^{Veb/Vt} - 1\right) \tag{3.36}$$

The emitter current of transistor Q5 can be expressed as

$$I_{E5} = I_{ES5} \left(1 + \frac{V_{CE5}}{V_{A5}}\right) \cdot \left(e^{Veb5/Vt} - 1\right) \tag{3.37}$$

Since the collector is connected to the base of Q5, the

collector-emitter voltage is equal to the emitter-base voltage. Rearranging Equation (3.37) and solving for V_{eb5} yields

$$V_{eb5} = V_t \cdot \ln \left[\frac{I_{E5}}{I_{ES5} \left(1 + V_{eb5}/V_{A5}\right)} + 1 \right] \qquad (3.38)$$

Substituting Equation (3.25) for I_{E5} in Equation (3.38) yields the complete expression for V_{eb5}:

$$V_{eb5} = V_t \cdot \ln \left[\frac{I_{REF} - I_{OUT}/\beta}{I_{ES5} \left(1 + V_{eb5}/V_{A5}\right)} + 1 \right] \qquad (3.39)$$

A similar expression can be derived for V_{eb4}:

$$V_{eb4} = V_t \cdot \ln \left[\frac{I_{OUT} + I_{OUT}/\beta}{I_{ES4} \left(1 + V_{CE4}/V_{A4}\right)} + 1 \right] \qquad (3.40)$$

When the expressions for V_{eb5}, Equation (3.39) and V_{be4}, Equation (3.40) are substituted into Equation (3.32) the current I_{OUT} appears on both sides of the equation. To solve for I_{OUT} the Newton's Method is used [Johnson-Riess, 1982]. The Newton's Method is an iterative root finding technique.

The general expression for the Newton's Method is

$$x(n+1) = x(n) - \frac{f(x(n))}{f'(x(n))} \qquad (3.41)$$

where x(n + 1) is the current value of x, x(n) is the value of x at the previous iteration, f (x(n)) is the function evaluated at x(n) and f'(x(n)) is the first derivative of the function evaluated at x(n). Substituting I_{OUT} into Equation (3.41) yields

$$I_{OUT}(n+1) = I_{OUT}(n) - \frac{f(I_{OUT}(n))}{f'(I_{OUT}(n))} \qquad (3.42)$$

where $f(I_{OUT})$ is found from Equation (3.32) to be

$$f(I_{OUT}) = I_{OUT} - \left[\frac{V_{eb5} - V_{eb4} + R1 \cdot I_{REF}}{R2/\alpha + R1/\beta} \right] \qquad (3.43)$$

The first derivative of $f(I_{OUT})$ is taken with respect to I_{OUT}, giving [CRC Standard Math Tables, 1990]

$$f'(I_{OUT}) = 1 + \frac{V_t \left[1/(\beta \cdot I_{REF} - I_{OUT}) + 1/I_{OUT} \right]}{R1/\beta + R2/\alpha} \qquad (3.44)$$

In the computer model Equation (3.43) and Equation (3.44) were

substituted into Equation (3.42) and solved iteratively to a convergence accuracy of 1×10^{-10} .

A piecewise linear approximation obtained from Motorola data books [Motorola Incorporated, 1974] was used for the current gain of the 2N3811 transistor. This approximation is shown in Figure 3.15. As the reference current I_{REF} is incremented in the computer model the appropriate value of the current gain β is selected from the curve in Figure 3.15. This value of β is used when computing I_{OUT} using Equation (3.32).

As evidenced by Equation (3.32) the output current is a function of the difference in the emitter-base voltages of Q5 and Q4 and of the reference current. The difference in the emitter-base voltages of Q5 and Q4 is greater than zero resulting in the output current being greater than the reference current. The difference between V_{eb5} and V_{eb4} was measured on the current mirror of the VCO; it increased approximately from 6 mV to 67 mV as the reference current was incremented and is plotted in Figure 3.16. As the plot in Figure 3.16 indicates, the difference between the emitter-base voltages increased as the reference current increased, indicating that V_{eb4} is decreasing more rapidly than V_{eb5}. The difference in the emitter-base voltages was computed using Equation (3.39) and Equation (3.40). The difference between the computed emitter-base voltages increases to about 2 mV and

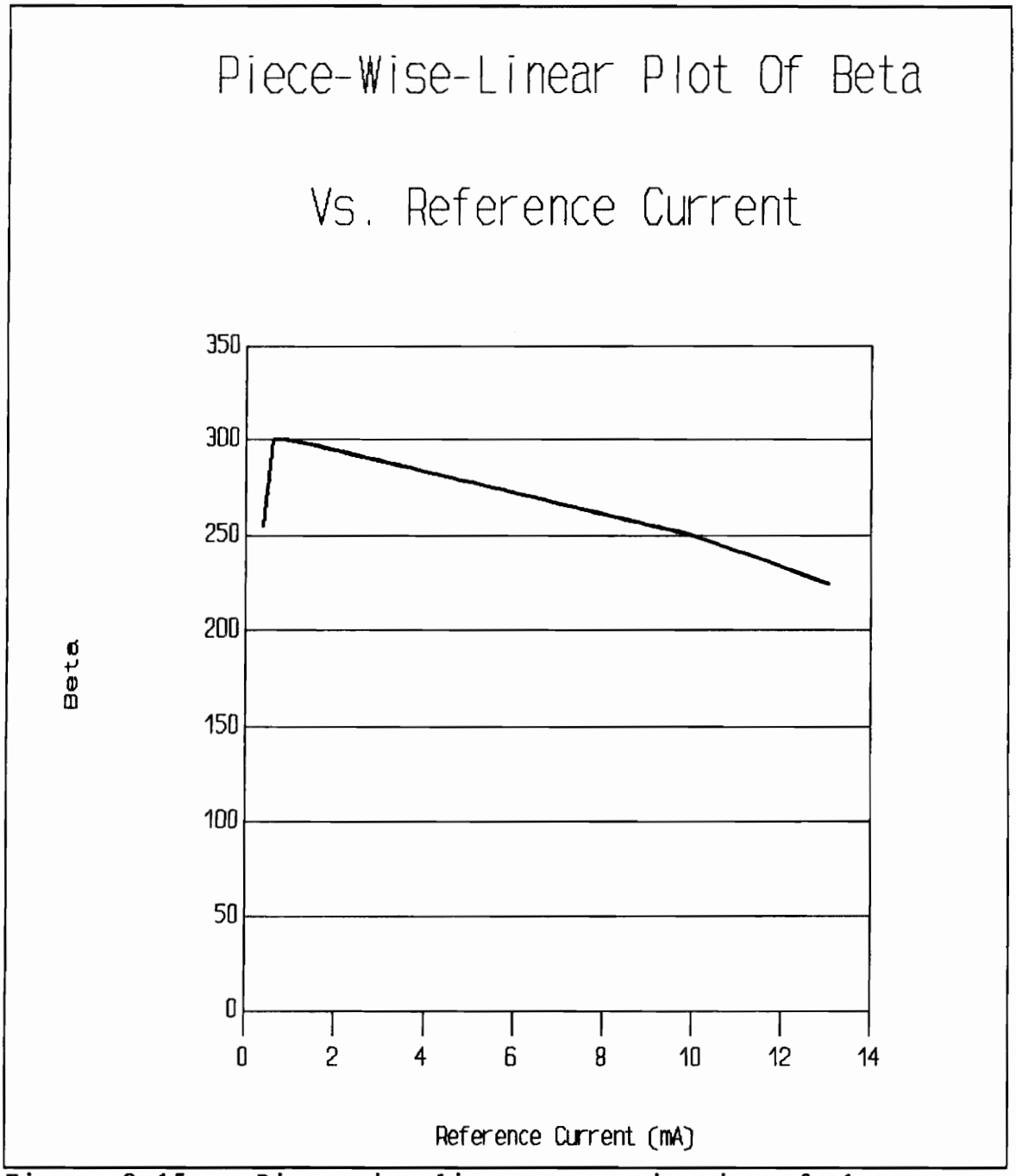

Figure 3.15 Piece wise linear approximation of the current gain for the 2N3811 transistor for use in computer model.

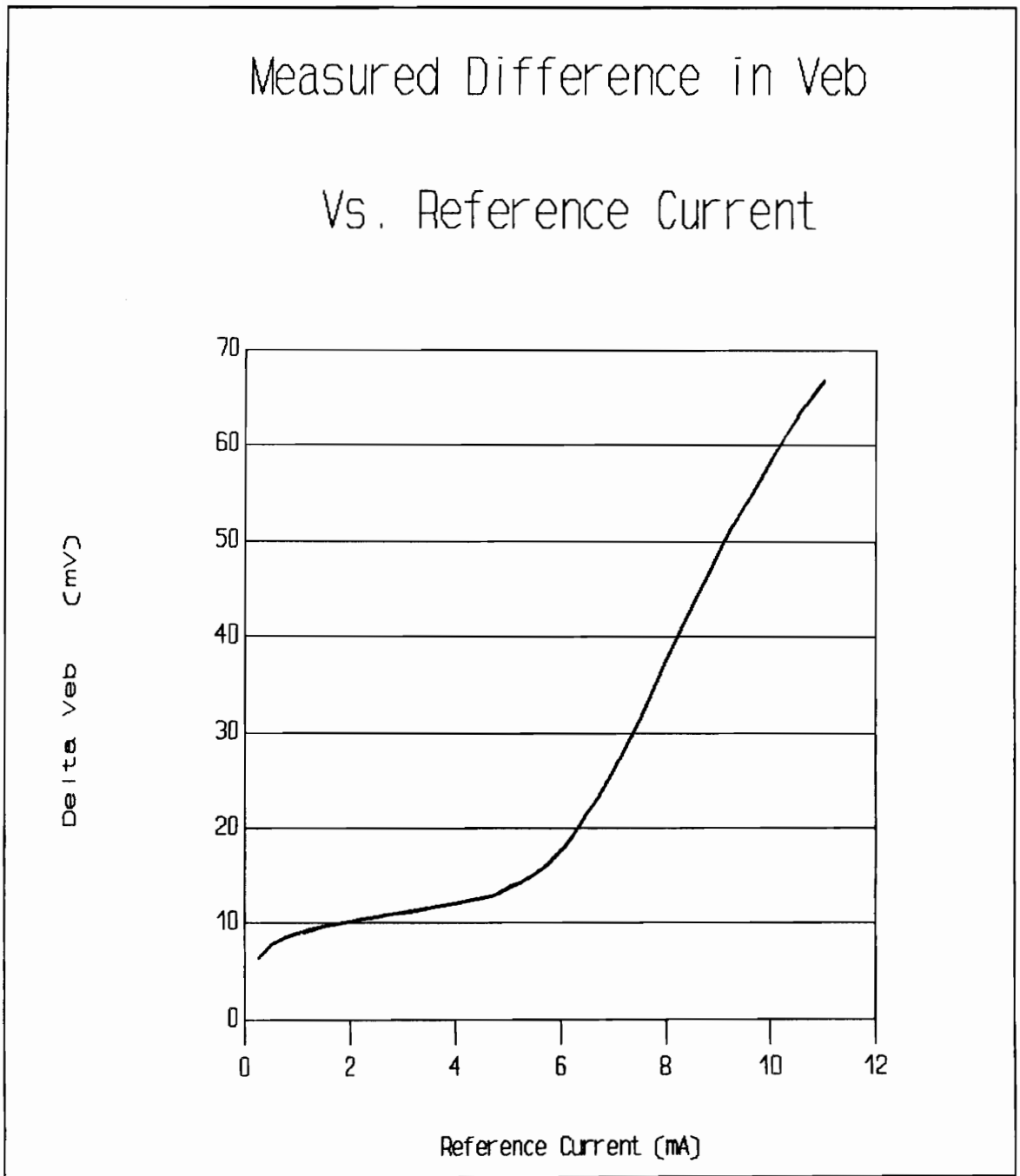

Figure 3.16 Plot of the measured difference in the emitter-base voltages of Q5 and Q4 of the current mirror circuit.

then slowly decreases.

The discrepancy between the measured and computed emitter-base voltages can be accounted for in the computer model by considering the power dissipation of the transistors Q5 and Q4. The power dissipation of the transistor raises the emitter-base junction temperature. The rise in temperature causes the emitter saturation current I_{ES} to increase and the exponential term in Equation (3.34) to decrease, however, the change in I_{ES} is dominant [Holt, 1978]. Both effects are combined as a net decrease in the emitter-base voltage by 2 mV per degree Celsius, for a given emitter current. As will be shown transistor Q4 dissipates more power than transistor Q5 at an increasing rate as the reference current is increased. The power dissipation in transistor Q5 can be computed from

$$P_{D5} = V_{CE5} \cdot I_{C5} \tag{3.45}$$

and the power dissipation of transistor Q4 is

$$P_{D4} = V_{CE4} \cdot I_{OUT} \tag{3.46}$$

In Equation (3.45) the collector-emitter voltage of transistor Q5 is equal to the emitter-base voltage; as determined by Equation (3.39), it varies from about 0.63 Vdc to about 0.72

Vdc. In Equation (3.46) the collector-emitter voltage can be determined by

$$V_{CE4} = 10 \text{ Vdc} - I_{E4} \cdot R2 \qquad (3.47)$$

where I_{E4} is the sum of I_{OUT} and I_{OUT}/β. The 10 V dc level used in Equation (3.47) is used to simplify the analysis and represents approximately the average collector voltage. From Equation (3.47) as I_{E4} is varied over its dynamic range, the computed collector-emitter voltage varies from about to 9.9 Vdc to about 7.3 Vdc.

Figure 3.17 plots the power dissipation of Q5 and Q4 using Equations (3.45) and (3.46). The junction temperature of Q4 and Q5 is a linear function of the dissipated power, and the voltage change as mentioned earlier, is a linear function of temperature. Therefore, the change in the emitter-base voltage of Q4 and Q5 is a linear function of the change in the power dissipated in each transistor. As shown in Figure 3.16, on page 54, the measured change in the emitter-base voltage is approximately 62 mV. Similarly, as shown in Figure 3.17, on the next page, the computed change in the difference in the power dissipation of Q4 and Q5 is approximately 85 mW. The ratio of the difference in the measured emitter base voltage to the difference in the power dissipation can be considered the temperature gradient of the

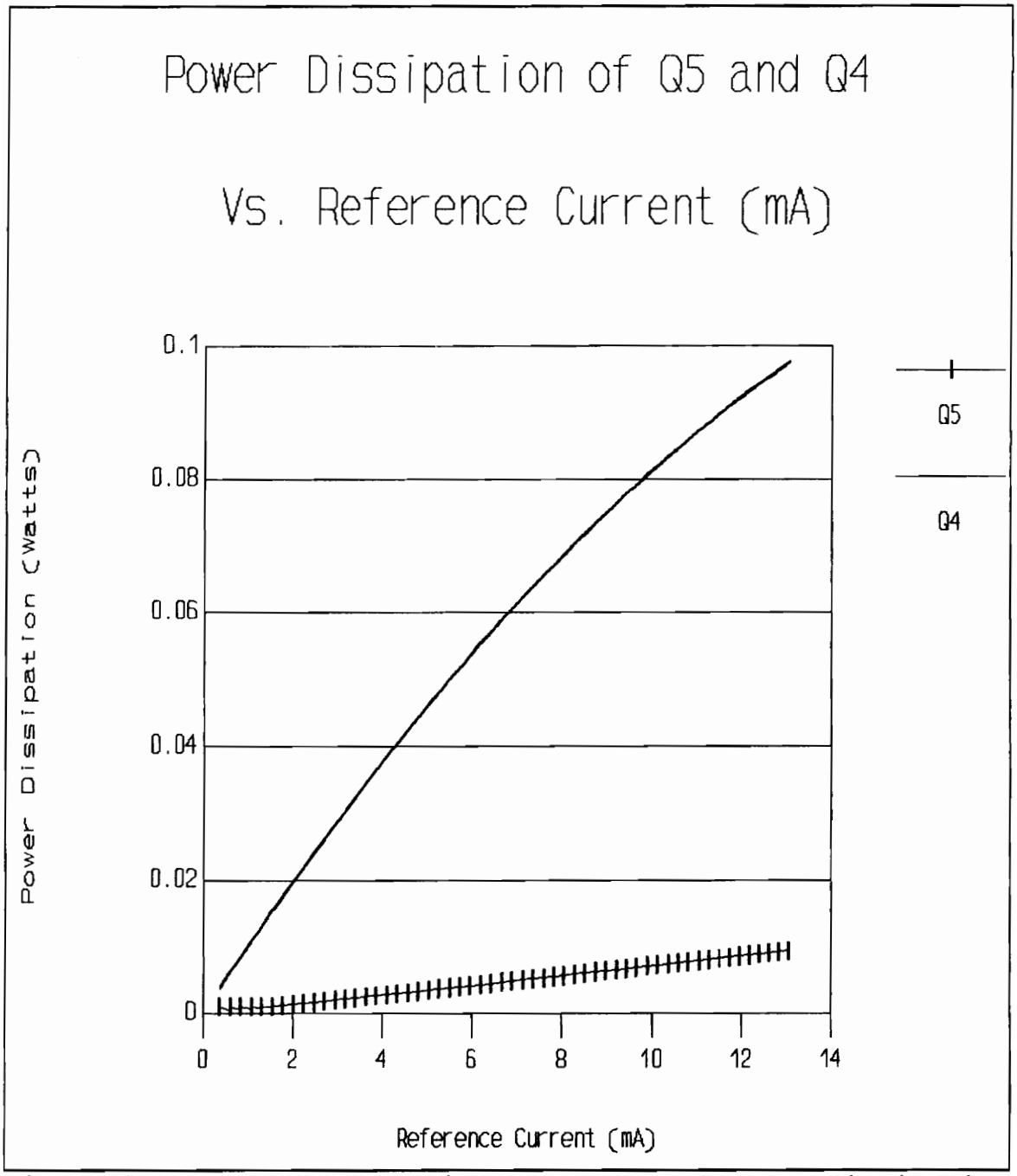

Figure 3.17 Plot comparing the computed power dissipation of transistors Q5 and Q4 in the current mirror circuit.

transistors, and when computed is approximately equal to 0.73. The so called temperature gradient factor has units of A^{-1} and can be used to simulate the effect of a temperature rise in the transistors due to the power dissipation. The modified values of emitter-base voltage for either Q4 or Q5 can be computed by

$$V_{ebM} = V_{eb} - (TG \cdot PD) \tag{3.48}$$

where V_{ebM} is the modified value of the emitter-base voltage, V_{eb} is the emitter-base voltage computed from Equation (3.39 or 3.40), TG is the temperature gradient of the transistors and PD is the power dissipation computed from Equation (3.45 or 3.46). A value of 0.80 for the temperature gradient was chosen for the computer model to fit the measured data of the difference of the emitter-base voltages. The computed difference of the emitter-base voltages of Q5 and Q4 is plotted in Figure 3.18.

Table 3.1, on page 60, lists the computed reference and output currents of the current mirror and emitter-base voltages for transistors Q5 and Q4. As shown in Table 3.1, the output current is greater than the reference current, but is not a linear function of the reference current. Plotted in Figure 3.19, on page 61, is the difference between the output and reference currents of the current mirror subtracted

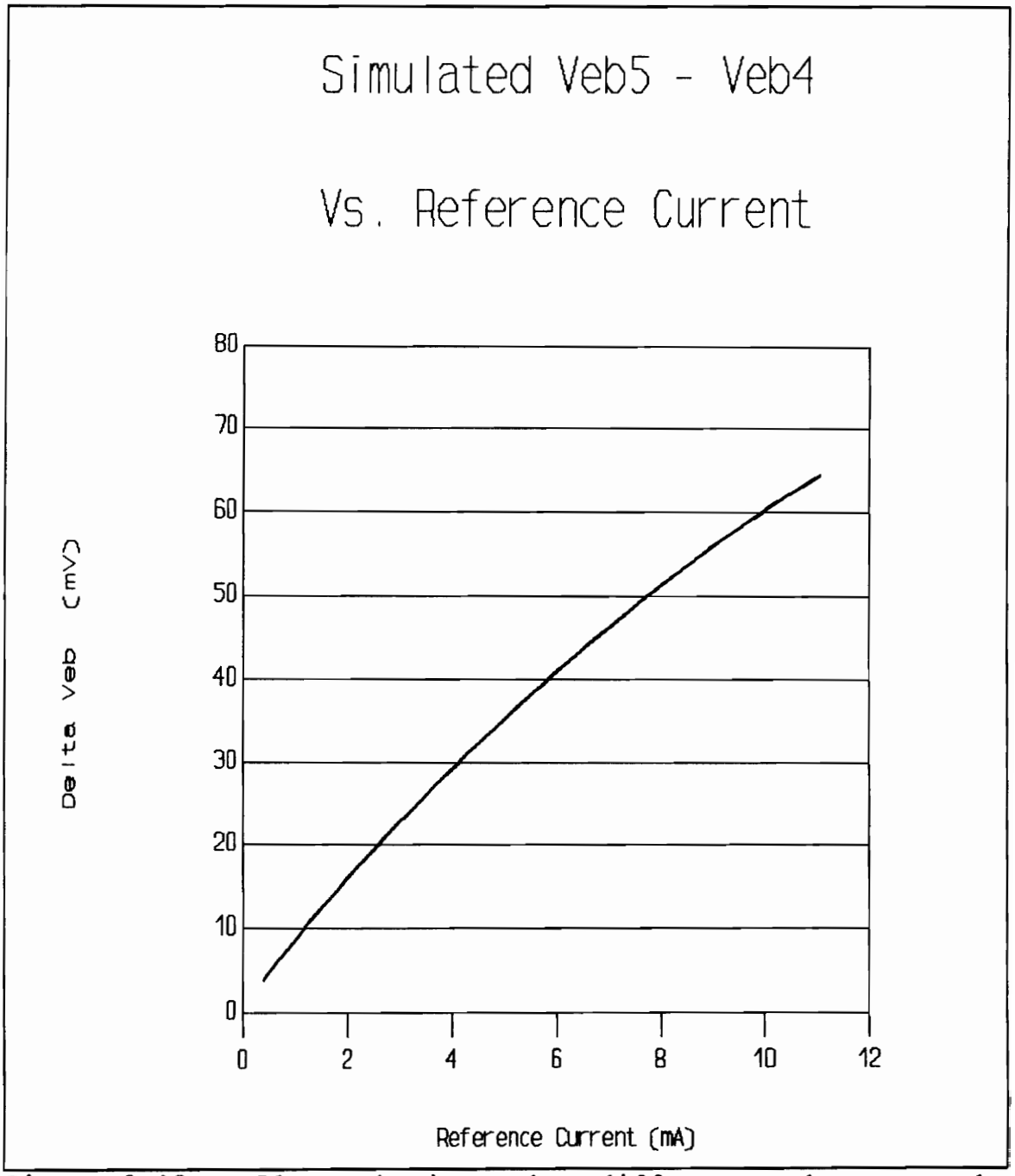

Figure 3.18 Plot showing the difference between the computed emitter-base voltages of transistors Q5 and Q4 of the current mirror circuit.

Table 3.1 Computed values of the reference current, output current, and emitter - base voltages for the current mirror circuit.

IREF (mA)	IOUT (mA)	Veb5 (Volts)	Veb4 (Volts)
0.378	0.394	0.632	0.628
0.843	0.874	0.653	0.645
1.308	1.354	0.665	0.653
1.773	1.832	0.672	0.657
2.239	2.311	0.678	0.660
2.704	2.789	0.682	0.661
3.171	3.267	0.686	0.662
3.636	3.744	0.689	0.662
4.102	4.221	0.692	0.663
4.567	4.697	0.695	0.663
5.032	5.171	0.697	0.662
5.497	5.647	0.699	0.661
5.961	6.120	0.701	0.660
6.426	6.594	0.703	0.659
6.891	7.067	0.704	0.658
7.356	7.539	0.705	0.657
7.819	8.011	0.707	0.656
8.283	8.481	0.708	0.655
8.746	8.951	0.709	0.654
9.209	9.420	0.711	0.653
9.673	9.889	0.711	0.652
10.13	10.35	0.712	0.651
10.59	10.82	0.713	0.650
11.05	11.28	0.714	0.649
11.51	11.74	0.715	0.648
11.96	12.19	0.715	0.648
12.41	12.64	0.716	0.647
12.84	13.08	0.717	0.646

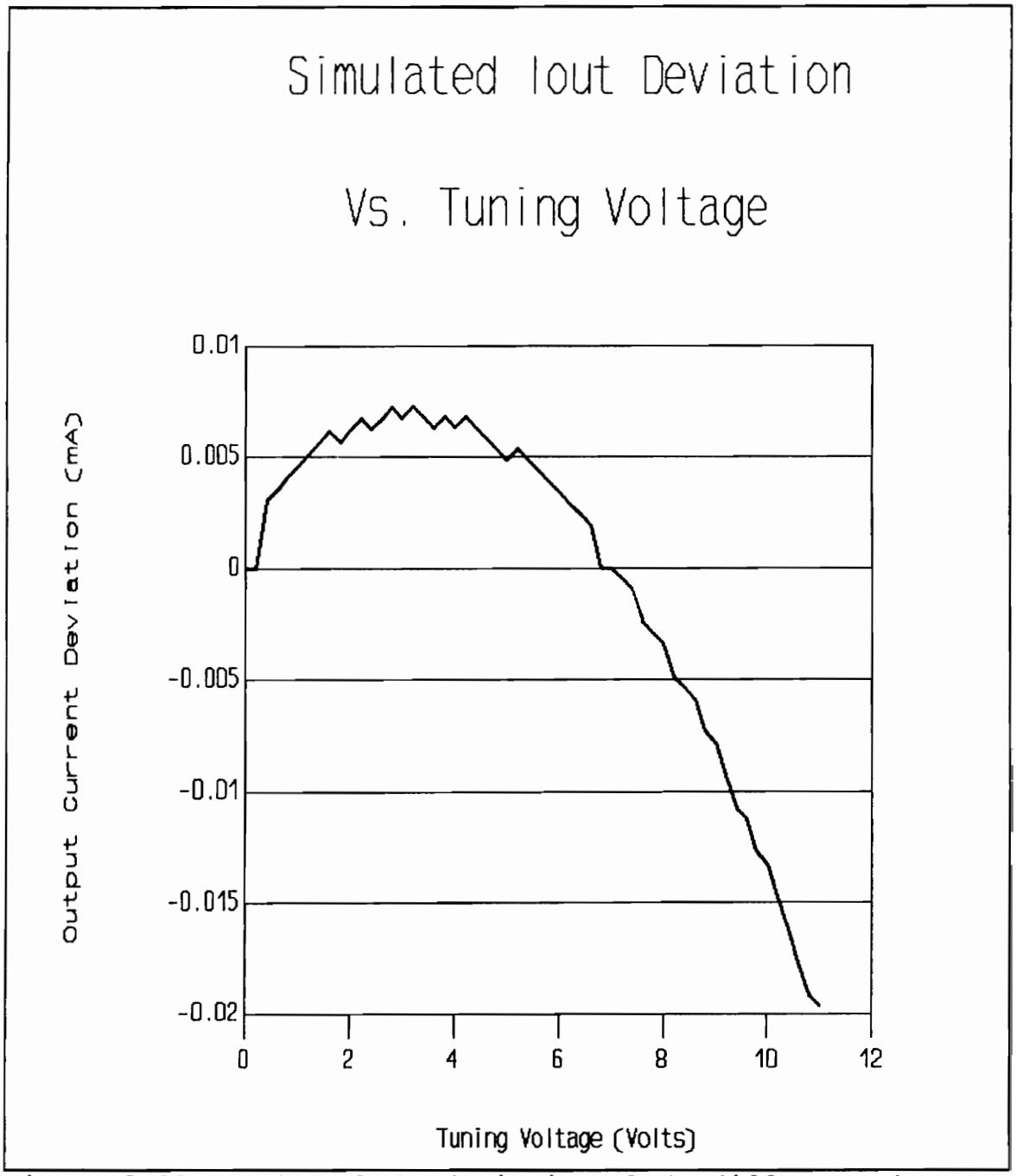

Figure 3.19 Plot of the deviation of the difference between IOUT and IREF of the current mirror from a best fit straight line versus the input tuning voltage.

from a best fit straight line. Notice the plot has the same general shape as the measured frequency deviation plot of Figure 1.1. In the computer model the output current I_{OUT} is used to compute the charge time of the timing capacitor by Equation (3.9a). From the discharge time Equation (3.9b) and the charge time Equation (3.9a), the output frequency is computed using Equation (3.11). The computed output frequency deviation from the nominal specified frequency is plotted in Figure 3.20, on the next page. This plot has the same general shape as the measured frequency deviation plot in Figure 1.1 and the output current deviation plot in Figure 3.19.

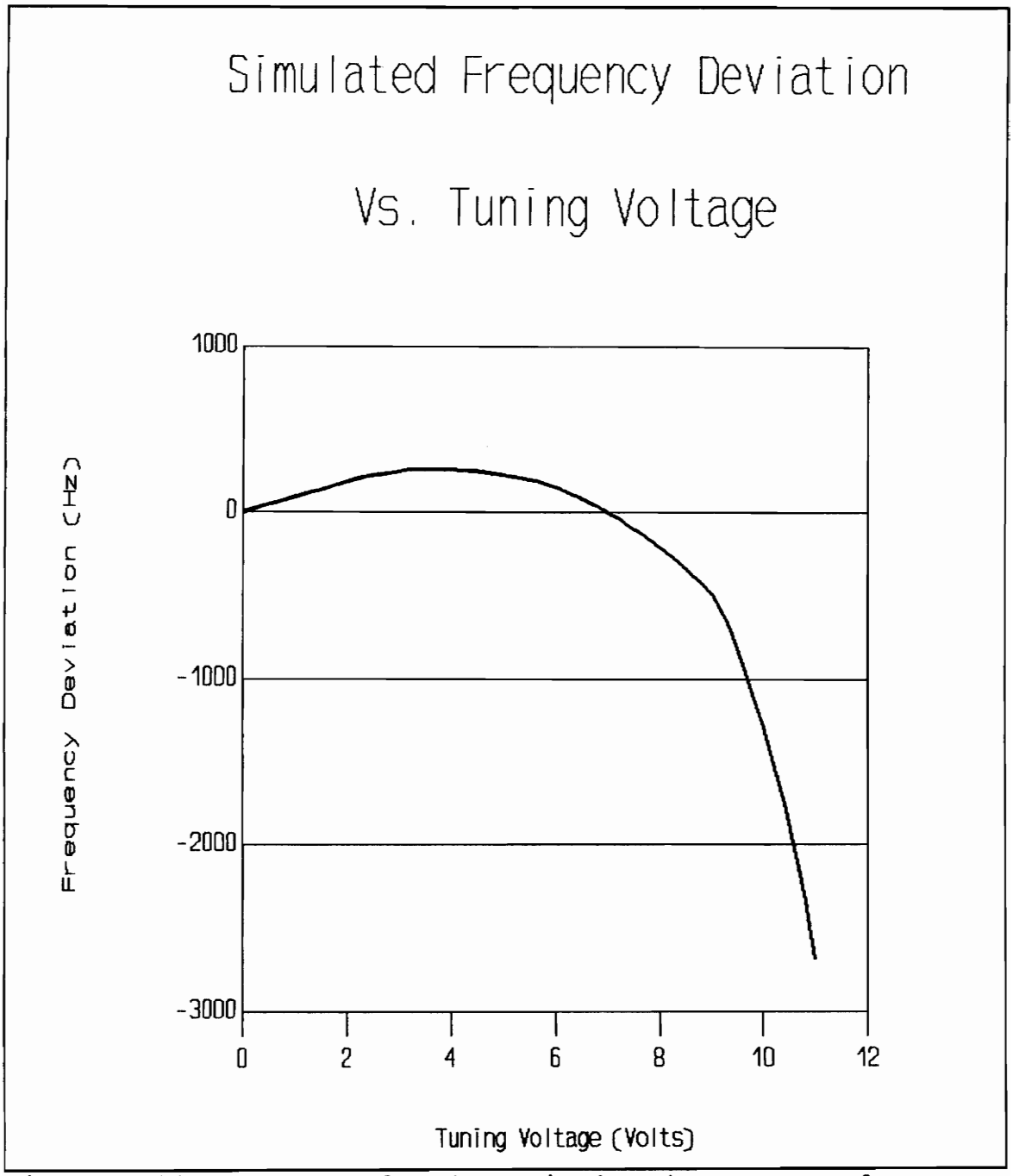

Figure 3.20 Plot of the simulated output frequency deviation of the VCO versus the input tuning voltage.

CHAPTER 4

PROPOSED SOLUTION AND RESULTS

The computer model developed for the VCO was used as an aid to propose a solution to the nonlinearity of the frequency-to-voltage characteristic as evidenced in Figure 3.20. As mentioned in the introduction of this report, the most straightforward solution is to limit the current to the VCO transistors to a region where their current gain is more nearly linear. However, the VCO must still be tuned over the same range of input voltage while yielding the same output frequency as specified.

As shown in the schematic diagram of the VCO in Figure 3.2 on page 18 of this report, the input current is controlled by R1, the 200 Ω external current sense resistor. Maintaining the input voltage at pin 17 of the VCO, and increasing the value of R1 would then decrease the operating current of the VCO. As shown in the frequency deviation plot of Figure 3.20 the output frequency starts to roll off severely at an input tuning voltage of about 8 Vdc. Once the input voltage is scaled down this translates into an operating current of about 9.9 mA. To limit the operating current to 9.9 mA requires the value of R1 to increase to about 255 Ω.

As a starting point in the computer model, resistor R1 was increased to 255 Ω. As shown by Equation (3.11) on page 24 of this report, the output frequency of the VCO is directly proportional to the current and inversely proportional to the capacitance value C1 and Δv. Since the operating current is decreased, the output frequency is decreased. To increase the output frequency either the capacitance value or Δv can be decreased. With the increased value of R1 the computer simulation was run. The resulting computed output frequency had decreased to a point where a change in Δv would not be practical since it would affect the operating point of transistor Q4 of the current mirror. The only practical solution would be to decrease the value of capacitor C1 to sufficiently increase the output frequency. The computer simulation was run several times using standard component values for capacitor C1 and resistor R1. The optimum performance was obtained with a capacitor value of 2700 pf and a resistor value of 360 Ω.

Figure 4.1 compares the simulated output frequency deviation with and without the proposed solution. In the computer simulation, the maximum operating current had to be decreased further than originally thought, from 9.9 mA to 7 mA. The explanation for the further decrease in current is due partly to the shape of the frequency deviation plot and partly to the manner in which the VCO is tuned. As shown in

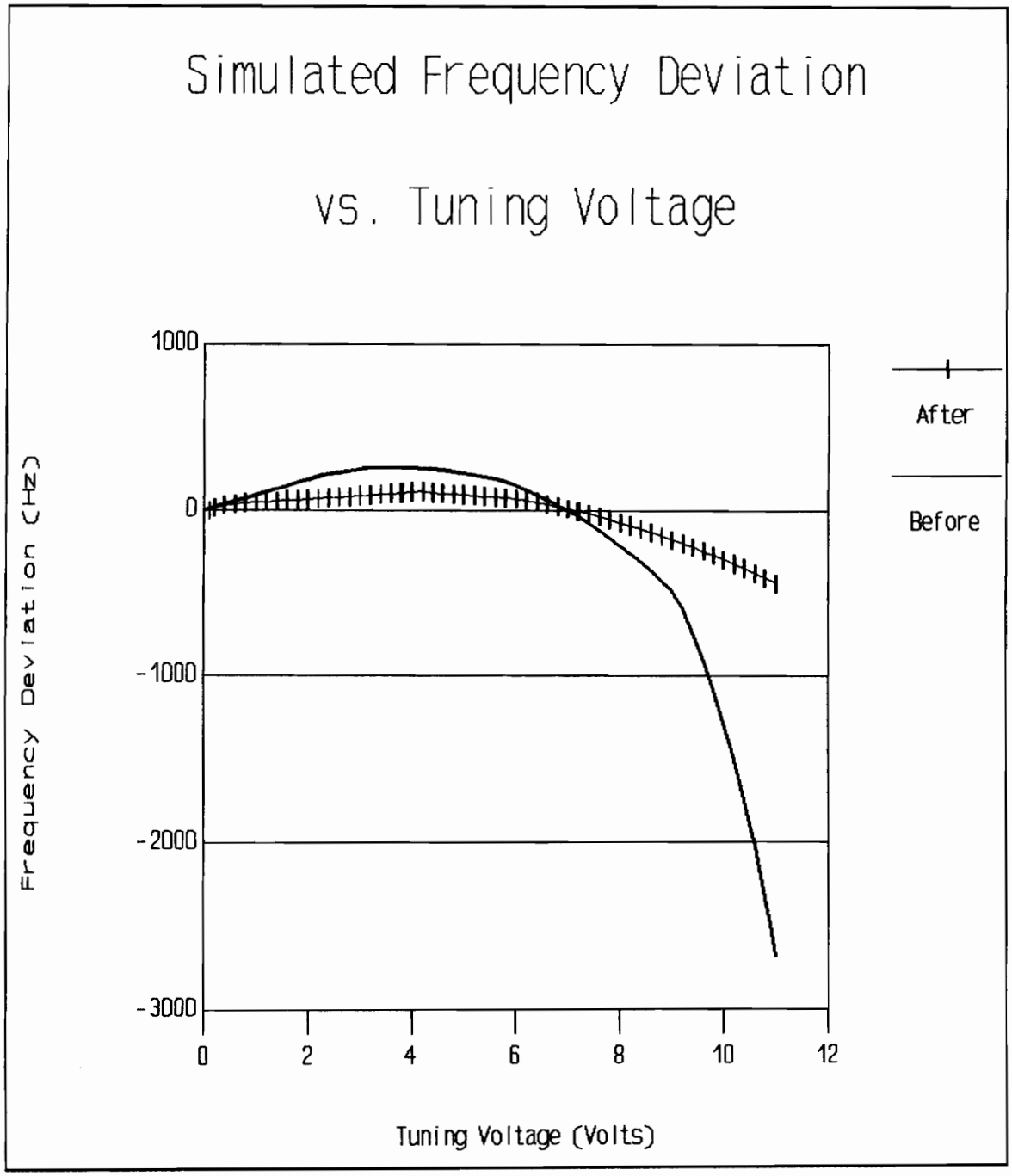

Figure 4.1 Plot of the simulated output frequency deviation of the VCO before and after the proposed fix.

Figure 4.1 the plot with the proposed solution labeled "after" is actually a stretched-out version of the original plot in the region from 0 to 8 V. During production test, the VCO slope and offset are adjusted for zero Hertz frequency deviation at about 0 Vdc and 7 Vdc of input tuning voltage. The frequency deviation of the VCO is then computed from a straight line passing through 0 Vdc and 7 Vdc. The input tuning voltage at 7 Vdc on the proposed stretched-out scale is equivalent to the 5 Vdc point on the original plot, which is nearly at the peak of its frequency deviation curve. The resulting frequency deviation at the upper end of the tuning range is greater than originally thought since this frequency is relative to the frequency at 5 Vdc on the original scale. Consequently, the proposed solution came about from a series of computer simulations where the resistor R1 was increased, capacitor C1 was decreased, followed by a retuning of the VCO to yield optimum results. Additionally, the peak to peak voltage Δv across the capacitor had to be decreased slightly from its nominal value of 5.25 Vdc to about 5.1 Vdc. The reduction in Δv was accomplished by reducing resistor R16 used in the threshold circuit from 1.62 kΩ to 1.5 kΩ. The reduction in Δv was required to maintain the nominal setting of the gain and offset potentiometers, used to tune the VCO, close to the center of their tuning range.

The proposed solution was demonstrated on a sample

VCO. This particular VCO exhibited a frequency deviation that far exceeded the specified output frequency tolerance by as much as 2000 Hz at the extreme upper end of its tuning range. The proposed component values for C1, R1 and R15 obtained from the computer simulation were demonstrated on the VCO. To yield similar results as the computer simulation, resistor R1 was decreased to 330 Ω and capacitor C1 was increased to 3300 pf; resistor R15 remained the same at 1.5 kΩ. The maximum operating current is limited to 7.7 mA which is fairly close to the current limit of 7 mA obtained from the computer simulation. The resulting output frequency deviation was one that was far more linear and which deviated by only 300 Hz from the specified frequency at its worst point. Figure 4.2 shows the measured output frequency deviation with and without the proposed solution implemented. The difference between the values obtained from the computer simulation and the experimental data is a result primarily of the shape of the frequency deviation curves and the manner in which the VCO is tuned as discussed earlier. The VCO in which the proposed solution was demonstrated may exhibit a worst case scenario which justly supports the proposed solution.

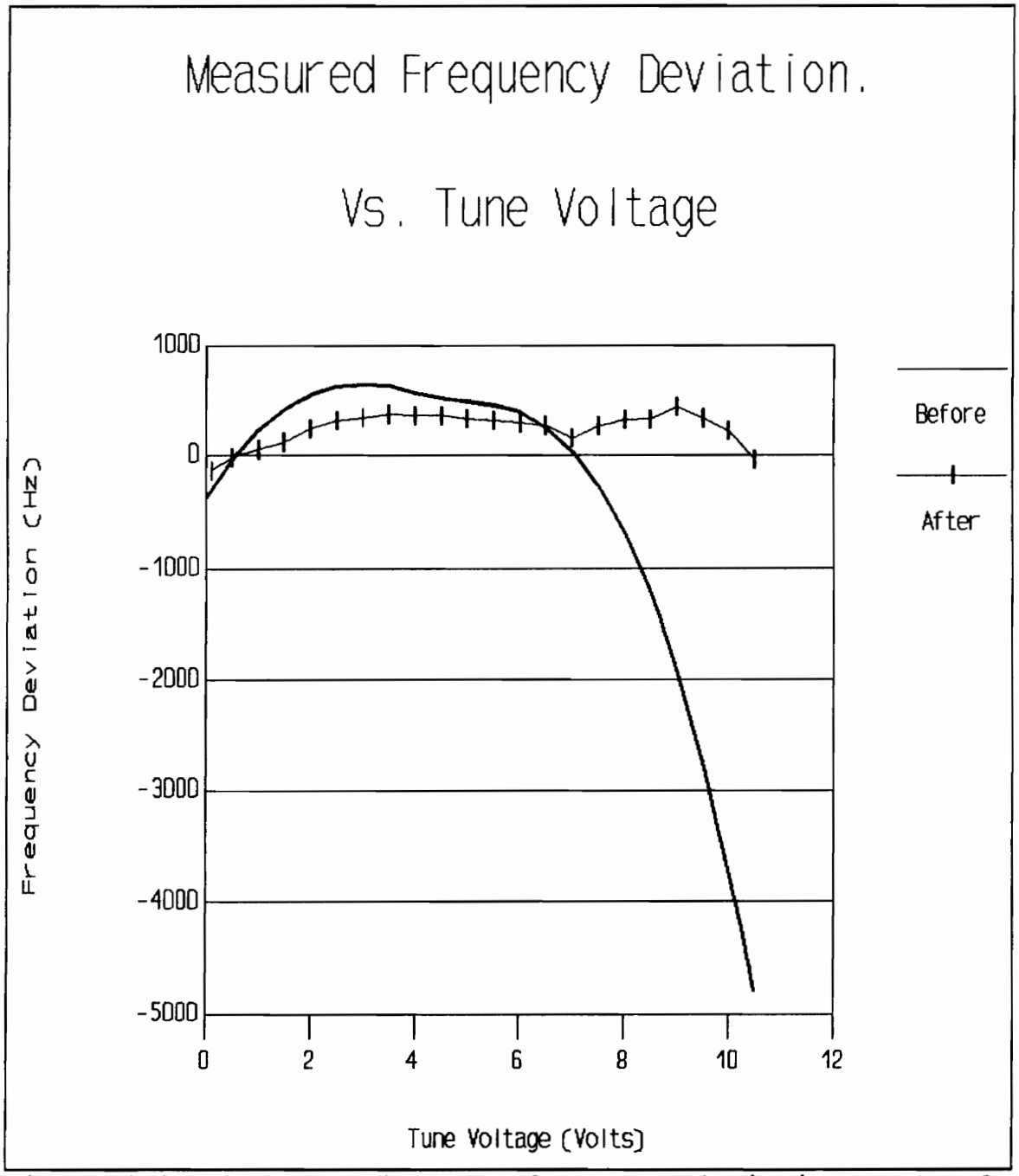

Figure 4.2 **Measured output frequency deviation on sample VCO before and after the proposed fix.**

CHAPTER 5

CONCLUSION

The sources of the nonlinearities in the frequency-to-voltage characteristic of the voltage-controlled oscillator have been successfully diagnosed and corrected. The cause of the nonlinear performance was isolated to the nonlinear current gain in the VCO transistors. Additionally, the imbalance in the power dissipation in the transistor pair used in the current mirror circuit exacerbated the nonlinearity.

A solution has been proposed that requires the change of three component values: R1 to 330 Ω, C1 to 3300 pf and R16 to 1.5 kΩ. These components are standard values that are external to the VCO chip, thus avoiding costly design and artwork changes. Laboratory measurements of the implemented solution on a VCO yielded a frequency-to-voltage characteristic that was more nearly linear. The computer model developed in this report confirms the laboratory data.

Additionally, a comprehensive model for the current mirror circuit was developed whose level of detail goes beyond most textbooks. The model accurately simulates the circuit in practice.

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APPENDIX

A computer model of the VCO, written in Fortran code is provided in this Appendix.

```
James F. Mckearney
May 20,1991


 IMPLICIT NONE
 DOUBLE PRECISION B,IES1,VT,ACC,I2(100),DEL,R1,R2,X,B1,V(100),T
1,IC(100),BI(100),VA,A,BB,S,DV,CAP,VI,I1(100),IR,G,F,VH,VL,R3,R4
1,TRUE(100),FR(100),DELF(100),VG,VOF,IE1(100),IE2(100),BA,BC,RS
1,IES2,VBE1,VBE2,IEA,DEN,delv,VCE2,IEB,PD1,PD2,VA1,VA2,CT,DT,R5
 INTEGER I,J

 OPEN(UNIT=1,FILE='E:\QUATTRO\PROJECT\BET.FOR')

 ****************************************************************
 THIS PROGRAM SIMULATES THE OUTPUT FREQUENCY OF THE OFFSET
 VCO.  THE OPERATOR ENTERS IN THE OFFSET AND GAIN VALUES TO SET
 UP THE VCO TRANSFER FUNCTION.  THE OUTER LOOP ITERATES THE TUN-
 ING VOLTAGE IN 0.2 V STEPS FROM 0 V TO 11 V.  THE INPUT CURRENT
 IS COMPUTED WHICH IS MODIFIED AS IT FLOWS THROUGH TWO TRANSIS-
 TORS.  EACH TRANSISTOR'S CURRENT GAIN VARIES WITH APPLIED
 CURRENT.  THE INNER LOOP SIMULATES THE CURRENT MIRROR BY SOLVING
 FOR THE OUTPUT CURRENT BY USING A NEWTON ROOT FINDING TECHNIQUE.
 THE OUTPUT FREQUENCY IS COMPUTED FROM THIS CURRENT AND COMPARED
 TO THE NOMINAL SPECIFIED FREQUENCY.
 ****************************************************************

 WRITE(6,*) 'ENTER VOLTAGE GAIN'
 READ *,VG

 WRITE(6,*) 'ENTER VOLTAGE OFFSET'
 READ *,VOF


 R3=7.87D+2
 R4=7.87D+2
 R5=1.62D+3

 VH=(20D+0*R5)/(R5+R4)
 VL=(20.4D+0/R3)/((1/R3)+(1/R4)+(1/R5))
 DV=VH-VL
 CAP=4.7D-9

 EMITTER RESISTORS R1 AND R2
 R1=2.0D+2
 R2=2.0D+2

 SET SATURATION CURRENTS
 IES1=1D-14
 IES2=1D-14

 q/KT EQUAL TO 26 Mv
 VT=2.6D-2
```

```
SET EARLY VOLTAGES
VA1=100.0D+0
VA2=100.0D+0

SET LOOP ACCURACY
ACC= 1.0D-10

RS=200
INCREMENT INPUT VOLTAGE
DO 100 J=1,56
V(J)=(J-1)*.2D+0
VI=(V(J)*VG)+VOF

COMPUTE INPUT CURRENT
I1(J)=VI/RS

COMPUTE SPECIFIED FREQUENCY
TRUE(J)=

MODIFY INPUT CURRENT BY BETA OF 1ST TRANSISTOR
IF(I1(J).LE.3D-3) BA=1.7199D+4*(I1(J)-I1(1))+190
IF(I1(J).GE.3D-3) THEN
IF(I1(J).LE.4.2D-3) BA=4.166D+3*(I1(J)-3.0D-3)+235D+0
END IF
IF(I1(J).GE.4.2D-3) THEN
IF(I1(J).LE.7.2D-3) BA=-3.333D+3*(I1(J)-4.2D-3)+240D+0
END IF
IF(I1(J).GE.7.2D-3) THEN
IF(I1(J).LE.11D-3) BA=-9.2D+3*(I1(J)-7.2D-3)+230D+0
END IF
IF(I1(J).GE.11D-3) BA=-3.4D+4*(I1(J)-11D-3)+195D+0
B1=BA+1.0D+0
X=B1/BA

IE1(J)=I1(J)/X

MODIFY CURRENT AGAIN BY BETA OF 2ND TRANSISTOR
IF(IE1(J).LE.3D-3) BC=1.7199D+4*(IE1(J)-IE1(1))+190
IF(IE1(J).GE.3D-3) THEN
IF(IE1(J).LE.4.2D-3) BC=4.166D+3*(IE1(J)-3.0D-3)+235D+0
END IF
IF(IE1(J).GE.4.2D-3) THEN
IF(IE1(J).LE.7.2D-3) BC=-3.333D+3*(IE1(J)-4.2D-3)+240D+0
END IF
IF(IE1(J).GE.7.2D-3) THEN
IF(IE1(J).LE.11D-3) BC=-9.2D+3*(IE1(J)-7.2D-3)+230D+0
END IF
IF(IE1(J).GE.11D-3) BC=-3.4D+4*(IE1(J)-11D-3)+195D+0
B1=BC+1.0D+0
X=B1/BC
IE2(J)=IE1(J)/X

INTIAL VALUE FOR OUTPUT CURRENT I2.  IR IS REFERENCE CURRENT
```

```
      I2(1)=IE2(J)*.9D+0
      IR=IE2(J)

      SET UP BETA OF CURRENT MIRROR
      IF(IE2(J).LE.5D-4) B=3.75D+5*(IE2(J)-1D-4)+150
      IF(IE2(J).GE.5D-4) THEN
      IF(IE2(J).LE.1D-3) B=300
      END IF
      IF(IE2(J).GE.1D-3) THEN
      IF(IE2(J).LE.10D-3) B=-5.555D+3*(IE2(J)-1D-3)+300
      END IF
      IF(IE2(J).GE.10D-3) B=-8.333D+3*(IE2(J)-10D-3)+250
      B1=B+1.0D+0
      X=B1/B
      VBE1=.7


      VCE2 IS VCE FOR OUTPUT TRANSISTOR.
      PD1 AND PD2 ARE POWER DISSIPATION OF TRANSISTORS 1 AND 2.
      IEA IS EMITTER CURRENT OF REFERENCE TRANSISTOR.

      DO 50 I=1,50
      VCE2=10-(X*I2(I)*R2)
      PD2=VCE2*I2(I)
      PD1=VBE1*IR
      A=1+(VCE2/VA2)
      IEA=IR-(I2(I)/B)
      VBE1=VT*DLOG(IEA/(IES1*(1+(VBE1/VA1)))+1)
      VBE2=VT*DLOG((I2(I)*X)/(IES2*A)+1)
      VBE1=VBE1-PD1*.8D+0
      VBE2=VBE2-PD2*.8D+0
      DELV=VBE1-VBE2
      DEN=R1/B+R2*X

      NEWTON ROOT FINDER.
      F=I2(I)-((DELV+(R1*IR))/DEN)
      G=1+(VT*(1/I2(I)+ 1/((B*IR)-I2(I)))/DEN)
      I2(I+1)=I2(I)-F/G

      DEL=DABS(I2(I)-I2(I+1))
      IF (DEL.LT.ACC) GO TO 90
   50 CONTINUE
   90 IC(J)=I2(I+1)
      WRITE(1,333)IE1(J),BA
  333 FORMAT(2X,F13.6,2X,F13.6,2X,F13.6,2X,F13.6)

      COMPUTE THE OUTPUT FREQUENCY
      CT=(CAP*DV)/IC(J)
      DT=(CAP*DV)/IR
      FR(J)=1/(CT+DT)
      DELF(J)=FR(J)-TRUE(J)
      DELV=IC(J)-IR
      WRITE(6,222)V(J),IR,IC(J),DELV
```

```
222 FORMAT(2X,F13.6,2X,F13.6,2X,F13.6,2X,F13.6)
100 CONTINUE

    DO 200 I=1,56
    DEL=IC(I)-IE2(I)
    WRITE (6,30) V(I),FR(I),TRUE(I),DELF(I)
 30 FORMAT(2X,F13.6,2X,F13.6,2X,F13.6,2X,F13.6)
200 CONTINUE
    WRITE(6,500) VG,VOF,DV,CAP,RS
500 FORMAT(2X,F13.6,2X,F13.6,2X,F13.6,2X,1E9.4,2X,F13.6)
    CLOSE(UNIT=1)
    END
```

VITA

James F. McKearney was born in New York City, New York on April 24, 1955. He received an Applied Associates in Science degree in Electrical Technology from the State University of New York at Farmingdale in 1975. He received a Bachelor of Engineering degree in Electrical Engineering from the State University of New York at Stony Brook in 1982 where he was a member of Eta Kappa Nu.

From 1975 to 1980 he worked as an electronic development technician at Eaton Corporation, AIL Division. He worked on satellite receivers, microwave antenna systems, and the development of commercial frequency synthesizers.

From 1982 to 1987 he held the position of RF design engineer at Eaton Corporation, where he was responsible for the design and production of a microwave channelized receiver on the B1-B system.

He is presently working for Raytheon Company, Missile Systems Division as an RF design engineer. He is responsible for the design and production of the receiver unit of a missile defense system. He is currently on a scholarship funded by Raytheon to complete his Master's degree in Electrical Engineering.


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