

High Temperature Characterization and Analysis of Silicon Carbide (SiC) Power
Semiconductor Transistors

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ABSTRACT

This thesis provides insight into state-of-the-art 1.2 kV silicon carbide (SiC) power semiconductor transistors, including the MOSFET, BJT, SJT, and normally-on and normally-off JFETs. Both commercial and sample devices from the semiconductor industry's well-known manufacturers were evaluated in this study. These manufacturers include: Cree Inc., ROHM Semiconductor, General Electric, Fairchild Semiconductor, GeneSiC Semiconductor, Infineon Technologies, and SemiSouth Laboratories. To carry out this work, static characterization of each device was performed from 25 °C to 200 °C. Dynamic characterization was also conducted through double-pulse tests. Accordingly, this thesis describes the experimental setup used and the different measurements conducted, which comprise: threshold voltage, transconductance, current gain, specific on-resistance, parasitic capacitances, internal gate resistance, and the turn on and turn off switching times and energies. For the latter, the driving method used for each device is described in detail. Furthermore, for the devices that require on-state dc currents, driving losses are taken into consideration. While all of the SiC transistors characterized in this thesis demonstrated low specific on-resistances, the SiC BJT showed the lowest, with Fairchild's FSICBH057A120 SiC BJT having $3.6 \text{ m}\Omega\cdot\text{cm}^2$ (using die area) at 25 °C. However, the on-resistance of GE's SiC MOSFET proved to have the smallest

temperature dependency, increasing by only 59 % from 25 °C to 200 °C. From the dynamic characterization, it was shown that Cree's C2M0080120D second generation SiC MOSFET achieved dv/dt rates of 57 V/ns. The SiC MOSFETs also featured low turn off switching energy losses, which were typically less than 70 μ J at 600 V bus voltage and 20 A load current.

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Chapter 1 Introduction

1.1 Motivation and Application Background

Power electronics are fundamental components in consumer electronics and clean energy technologies [1], [2]. For several decades, silicon (Si) has been the primary semiconductor choice for power electronic devices. Due to the many decades dedicated to the development and fabrication optimization of Si devices, as well as the large abundance of material [3], the manufacturing capability is high, and the costs are extremely low. However, Si is quickly approaching its limits in power conversion [3], [4]. Wide bandgap (WBG) semiconductors offer promise of improved efficiency, reduced size, and lower overall system cost [3].

Of the various types of WBG semiconductors, silicon carbide (SiC) and gallium nitride (GaN) have proven to be the most promising technologies [3], [4], with several devices already being sold commercially. GaN is favored for its high frequency switching capability, though its high costs and driving intricacies currently limit its commercial viability [5]. In particular, the lack of quality substrates hinders the development of the economically advantageous vertical structure [4], [5]. Vertical devices are desirable as the lateral arrangement limits the current density, and voltage capabilities of the GaN technology [5]. Alternatively, SiC has shown tremendous high temperature capability, as well as aptitude for high voltage applications [3], [4]. Furthermore, the cost of SiC

devices has decreased within the last decade, and the performance has proven superior to that of conventional Si devices.

Some of the potential application areas for these WBG devices include: transportation electrification, downhole drilling, and renewable energy [3]. Transportation electrification is a major trend today, especially in the aerospace and automotive industries. Further success of electric cars and more-electric aircrafts hinges on advances in power electronics. Within the oil and gas industry, high temperature electronics are in demand for downhole drilling in the exploration of petroleum. These deep oil wells can reach temperatures greater than 200 °C, which is far beyond the limit of traditional Si devices. Regarding renewable energy, in particular, WBG devices have been explored for replacement of Si insulated gate bipolar transistors (IGBTs) in photovoltaic inverters in order to improve efficiency. WBG semiconductors are well suited for these applications due to their high temperature capabilities, fast switching speeds, and low losses. The high temperature capability of these devices allow them to better withstand the harsh environmental conditions, and have relaxed cooling system requirements [3], [4]. In addition to this high temperature capability, the fast switching speed of these devices allows for higher frequency operation thereby resulting in the reduction of the passive components, which decreases the total size, weight, and cost of the system [3].

1.2 *Silicon Carbide Power Devices*

These benefits of WBG semiconductors such as SiC arise from their greater thermal conductivity, higher critical electric field for breakdown and saturation electron drift velocity, and lower intrinsic carrier concentration compared to Si [6]-[8]. The higher

thermal conductivity of SiC makes it superior to Si in terms of heat transfer to the environment, which allows for increased power densities [4]-[7]. SiC has a breakdown electric field that is more than eight times higher than that of Si [6]. This means that, for a given blocking voltage, SiC can be more heavily doped than Si, thereby reducing the on-state resistance [6]. The higher saturation drift velocity makes SiC more suitable for high frequency applications [7]. Also, due to the wider bandgap of SiC, it has a lower intrinsic carrier concentration, which allows these devices to operate at higher temperatures without suffering from excessive leakage [6], [7].

Infineon Technologies and Cree Inc. introduced the first commercial SiC power devices in 2001 and 2002, which were SiC Schottky diodes [9], [10]. The wild success of the SiC Schottky diodes led to the further development, and eventual commercialization, of the vertical trench SiC junction field-effect transistor (JFET) by SemiSouth Laboratories in 2008. Although SemiSouth has dissolved, other companies such as Infineon and United Silicon Carbide, Inc. (USCi) have taken over the production of SiC JFETs, though choosing to focus on the depletion mode (normally-on) SiC JFET [11], [12].

Just three years after the release of the SiC JFET, Cree commercialized the first SiC metal-oxide-semiconductor field-effect transistor (MOSFET) [9]. Though the gate-oxide reliability proved to be a challenge, improved manufacturing has resulted in new generation SiC MOSFETs with superior oxide quality [13]. Today, more manufacturers are producing SiC MOSFETs, including General Electric (GE) [14], ROHM Semiconductor [15], Mitsubishi Electric [16], and Sumitomo Electric Industries [17].

Bipolar devices are also becoming available. In 2013, GeneSiC Semiconductor released its SiC super junction transistor (SJT) [18], and Fairchild Semiconductor is developing its SiC bipolar junction transistor (BJT) [19]. These SiC devices experience quite different characteristics as compared to their Si counterparts, such as high current gains and fast switching speeds, as will be seen in a later chapter. Figure 1 summarizes this progression of the commercialization of SiC power semiconductors.

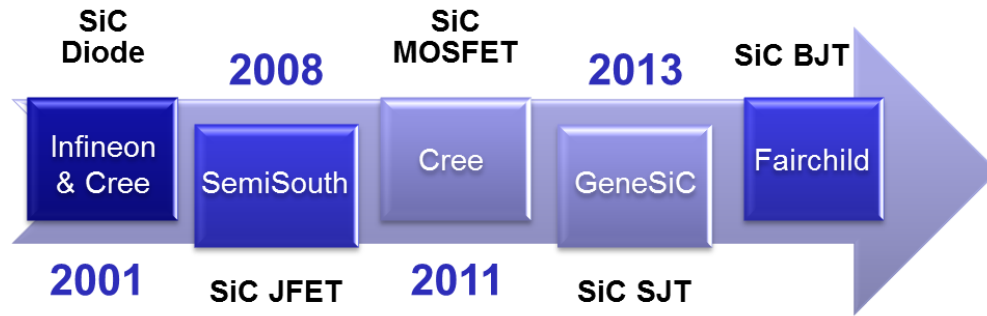


Figure 1: History of the commercialization of SiC power semiconductor devices.

1.3 Research Objectives

Due to the continuous emergence of new SiC transistors, many questions about their performance arise. Consequently, a significant effort has been devoted to characterizing the numerous SiC power semiconductor devices, some of which are commercially available, in order to thoroughly evaluate their functionality. Of these devices, the SiC MOSFET has received significant attention up to now. SiC MOSFETs were fully characterized in [18]-[21], and compared to Si IGBTs in [14], [22]-[29], and Si MOSFETs in [14], [30], [31]. Additionally, recent studies have shown that the gate-oxide of SiC MOSFETs is reliable beyond 200 °C [13], [15], [32], which remained one of the major barriers of this device until now.

Since the benefits of SiC transistors over conventional Si devices has been demonstrated in the above listed studies, the remaining question is how the various types of SiC devices compare to one another. This evaluation was carried out in [33]-[37], though there was still room for further research. [33] compared six different SiC devices: one of Cree's first generation SiC MOSFETs, a SiC MOSFET from ROHM, an early version of Fairchild's SiC BJT, a SemiSouth enhancement mode JFET, and two depletion mode JFETs (one from SemiSouth and another from Infineon). While [33] evaluated a great variety of SiC devices, more characterization could be performed in order to better compare the device performances. The temperature at which this testing was carried out could also be increased beyond 150 °C in order to take advantage of the full high temperature capability of SiC.

In [34], three SiC devices were tested to higher temperatures (from 50 °C to 175 °C for the static characterization). These devices were depletion mode and enhancement mode JFETs from SemiSouth, and Cree's first generation SiC MOSFET. Although [34] tested the devices to higher temperatures than [33], and provided better comparison of the on-state characteristics of the devices, the switching energy loss information presented in the paper was taken from the datasheet for the Cree MOSFET and obtained from SemiSouth for the JFETs. By using the information from the different manufacturers, the benefit of performing the comparison is lost, as the variability between the testing conditions is unknown, and only conservative temperatures are tested (125 °C in this case).

In [35], on the other hand, the driving conditions used for each of the three SiC devices under test, which included a SiC MOSFET, BJT, and enhancement mode JFET

(the manufacturers of which were not specified) were provided. However, the temperature was only increased up to 125 °C, and the switching waveforms showed substantial ringing. Limited results were also presented on the static characteristics of the devices, though the influence of the die area on the on-resistance was taken into consideration by using the specific on-resistance to compare the on-state performances of the transistors.

As in [34], [36] again characterized depletion mode and enhancement mode JFETs from SemiSouth, and Cree's first generation SiC MOSFET. Although explanations on the methods used for the temperature setup are provided, the static operation of the devices was only tested up to 100 °C, and the dynamic characterization was evaluated at even lower temperatures of a mere 80 °C. Moreover, the study again did not specify the driving conditions that were used in the characterization.

High temperature operation was evaluated in [37]. The paper showed the I-V curves, specific on-resistances, and blocking characteristics of a SiC depletion mode JFET and a SiC MOSFET (manufacturers not specified) up to 300 °C. However, no dynamic characterization was reported.

Additionally, new generations of SiC devices have become available since these studies. Accordingly, this thesis offers insight into the high temperature performances of state-of-the-art SiC power semiconductors by characterizing and comparing the latest generation of 1.2 kV SiC MOSFET, BJT, SGT, and normally-on (depletion mode) and normally-off (enhancement mode) JFET devices from well-known manufacturers; namely Cree Inc., ROHM Semiconductor, General Electric (GE), Fairchild Semiconductor, GeneSiC Semiconductor, Infineon Technologies, and SemiSouth

Laboratories. To carry out this study, full static and dynamic characterizations were performed from 25 °C to 200 °C on each transistor. Some of this characterization was previously reported in [38]-[40].

Moreover, the characterization of the 1.2 kV SiC MOSFETs conducted in this work revealed behaviors not experienced in standard Si MOSFETs. These unique characteristics include an extended transition region between the linear and saturation regimes of the output characteristic curves, a non-flat Miller Plateau, and a decrease in channel resistance with increased temperature [41]-[44]. These phenomenon can be attributed to the modest transconductance [44], short-channel effects, and traps at the SiC/SiO₂ interface [43], [44], [53].

Due to these unorthodoxies, models developed for Si MOSFETs are not well-suited for SiC. Consequently, significant effort has been made to adjust previous, or develop entirely new, models to accommodate the abnormalities seen by SiC MOSFETs. However, many of these new models for SiC MOSFETs involve knowledge of the physical parameters of the device, or require extensive parameter extraction from the electrical characteristic curves. This work instead seeks to realize a simple method for users to predict the dynamic performance of these SiC devices using their readily available static characteristics. In this way, the dynamic characterization of these devices can be significantly reduced or eliminated entirely. This is of interest because this dynamic testing can be time-consuming and expensive. To accomplish this goal, a simplified analytical model, which utilizes the MOSFET switching waveforms and equivalent circuit to calculate the turn on and turn off switching times, will be proposed.

Similar models were developed in the past for the ideal Si MOSFET, and proved useful in the early design stages.

1.4 Thesis Organization

To satisfy the above objectives, this thesis is organized as follows. Chapter 2 introduces the SiC MOSFET, and provides the results of the complete static and dynamic characterization performed up to 200 °C. Analysis on the differences observed between Si and SiC MOSFETs will then be detailed, followed by a survey on the types of models that have been developed for SiC MOSFETs. A new analytical model will then be proposed. Chapter 3 explores the performances of SiC BJT and SGT devices. Particular attention is paid to the driving of these transistors, as they require dc current in the on-state. Chapter 4 evaluates the characteristics of SiC normally-on and normally-off JFETs. Again, the driving of these devices is taken into consideration. Chapter 5 presents a summary of the key characterization results for all of the 1.2 kV SiC devices studied in this thesis. Conclusions will then be drawn in Chapter 6, followed by a discussion of the future work.

Chapter 2 Characterization of 1.2 kV SiC MOSFETs

2.1 *Introduction*

With the push to higher power, ordinary Si MOSFETs become less favorable due to increased on-state losses. Consequently, the Si IGBT was typically the preferred choice for voltages greater than approximately 200 V. The emergence of the superjunction MOSFET (SJ-MOSFET) and CoolMOS technologies allowed Si unipolar transistors to contend with 600 V devices. However, above this voltage, Si IGBTs are again favored. Although the Si IGBT has lower on-state losses than high voltage Si MOSFETs, it experiences slow switching speeds and thus high dynamic losses.

Alternatively, the larger critical electric field for breakdown of SiC allows it to have a greatly reduced drift region resistance for the same breakdown voltage [6]. Furthermore, SiC MOSFETs have the benefit of being unipolar devices, and thus typically experience faster switching than an IGBT. As a result, extensive work on the characterization of SiC MOSFETs, and comparison of their dynamic performance to Si IGBTs, has been carried out [14], [22]-[29].

In this chapter, the background of SiC MOSFETs will first be discussed, followed by detailed descriptions of the complete high temperature static and dynamic characterization methods and results. This chapter will then explore the unique characteristics observed for SiC MOSFETs that are unseen in conventional Si MOSFETs.

A survey of models for SiC MOSFETs will then be provided, followed by a new proposed analytical model for predicting the switching times of these 1.2 kV devices.

2.2 Background of SiC MOSFETs

The initial fabrication of SiC MOSFETs was stifled by two main issues: (1) the quality of the SiC/SiO₂ interface [4], and (2) the high electric field generation [6]. The poor quality of the boundary between the SiC surface and oxide resulted in low mobility in the inversion layer, while the high electric field generated within the SiC caused degradation of the gate oxide [6]. Significant improvement has been made to the manufacturing of SiC MOSFETs, and thus it has been demonstrated that these issues have been resolved [13], [15].

A common structure for SiC MOSFETs is the double-diffused or DMOSFET (Figure 2), which allows for fast switching speed and high durability. In this structure, when no voltage is applied to the gate, a high voltage can be supported within the thick, lightly doped n- drift region. Upon application of a positive gate bias, an inversion layer is produced at the surface of the p- well region underneath the gate electrode. This inversion layer provides a path for the flow of current from the drain to the source [6]. This structure includes an intrinsic body diode, and allows operation in both the first and third quadrants. Current flows through the body diode when the MOSFET gate is off, and a positive drain bias exceeding approximately 0.7 V is applied. If instead a positive gate voltage is applied, and the drain is negatively biased, then the channel will conduct with current flowing from the source to the drain, resulting in third quadrant operation.

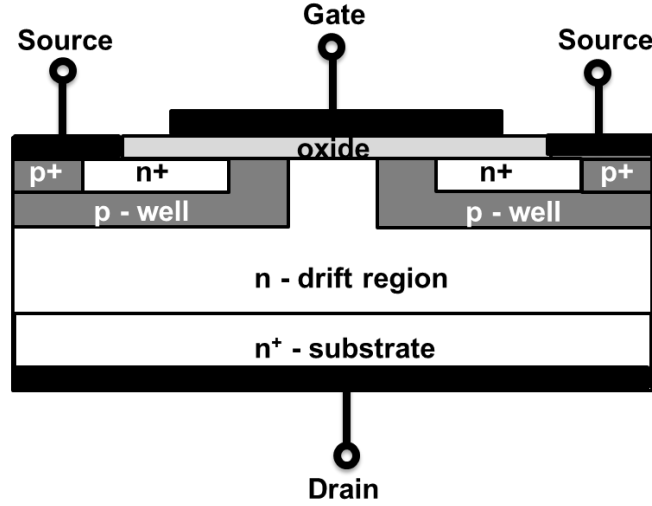


Figure 2: SiC DMOSFET structure.

The SiC power MOSFET is also capable of supporting high positive drain voltages. Furthermore, due to its greater critical electric field for breakdown, the doping concentrations in the drift region of SiC MOSFETs can be increased, thereby resulting in a lower drift resistance for a given blocking voltage. This relationship is shown by the following equation for the ideal on-state resistance $R_{on-ideal}$

$$R_{on-ideal} = \frac{4BV^2}{\epsilon_s \mu_n E_c^3} \quad (1)$$

where BV is the breakdown voltage, ϵ_s is the dielectric constant of the semiconductor, μ_n is the mobility of the drift region, and E_c is the critical electric field for breakdown [6]. Moreover, SiC also features a higher saturation drift velocity, allowing for faster switching, and thus is suitable for high frequency applications.

Given these benefits of SiC, many companies have invested extensively in research and development of SiC transistors. The SiC MOSFETs that will be assessed in this work are shown in Table I, where all of the devices are rated at 1.2 kV and are in TO-247 package. This table lists the device manufacturer, part number, continuous current

and operation temperature ratings as listed in their respective datasheets [45]-[49], and their die areas normalized to that of Cree's C2M0080120D 2nd Generation Z-FET.

Normalizing the die areas shows the sizes of the devices relative to one another, which is significant because the size of the device directly relates to the on-state resistance and junction capacitance. As the device size is reduced, the on-state resistance increases, thereby resulting in higher conduction losses. On the contrary, smaller devices feature lower junction capacitances, which results in faster switching and thus reduced dynamic losses.

Table I: 1.2 kV SiC MOSFETs under study.

<i>Mfg.</i>	<i>Device</i>	<i>I_{D,Cont}</i>	<i>T_{Max}</i>	<i>A_{Norm}</i>
Cree	CMF20120D (1 st Gen. Z-FET)	42 A (25 °C); 24 A (100 °C)	135 °C	1.59
	C2M0080120D (2 nd Gen. Z-FET)	31.6 A (25 °C); 20 A (100 °C)	150 °C	1.00
GE	GE12N20L	30 A (25 °C); 22.5 A (100 °C) 20 A (125 °C)	200 °C	0.97
ROHM	SCT2080KE	40 A (25 °C); 28 A (100 °C)	175 °C	1.21
	SCT2160KE	22 A (25 °C); 16 A (100 °C)	175 °C	0.75

2.3 Static Characterization of the 1.2 kV SiC MOSFETs

In the following subsections, the methods and measurement results for the static characterization of the SiC MOSFETs listed in Table I will be presented. The parameters include: blocking capability, threshold voltage, transfer characteristics and transconductance, output characteristics and on-resistance, body diode I-V

characteristics, internal gate resistance, and junction capacitances. Each parameter, with the exception of the internal gate resistance and junction capacitances, was measured from 25 °C to 200 °C in order to assess the high temperature capabilities of the devices under study. Much of the results presented in the following sections were previously reported in [38]-[40].

2.3.1 Static Characterization Methods

The static characterization was performed using a Tektronix 371b curve tracer, and Agilent 4294A impedance analyzer. For the Tektronix 371b curve tracer, four-terminal (also known as Kelvin) sensing was employed to ensure measurement accuracy. The curve tracer was connected via GPIB to a computer such that the data from the curves could be quickly and easily retrieved. An oscilloscope was also utilized for the threshold voltage measurements to obtain improved resolution. A hotplate and thermocouple were used for heating and temperature sensing. Measurements were taken in 25 °C increments from 25 °C to 200 °C. Once the desired steady-state temperature was reached, measurements were taken quickly in order to avoid the self-heating of the devices. Figure 3 depicts the static characterization setup.

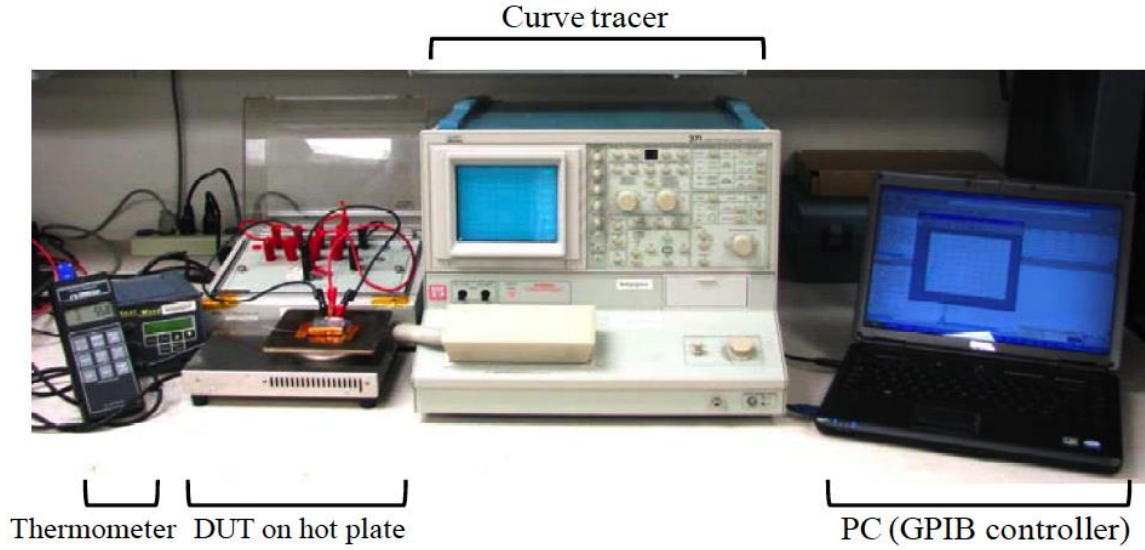


Figure 3: Static characterization setup, showing the hotplate and thermocouple used for heating and temperature sensing, curve tracer with four-terminal measurements for obtaining the curves, and PC with GPIB controller for retrieving the data. Image from [Z. Chen, “Characterization and modeling of high-switching-speed behavior of SiC active devices,” M.S. thesis, Dept. Elect. Comput. Eng., Virginia Tech, Blacksburg, VA, 2009], with permission from Zheng Chen.

2.3.2 Blocking Capability

The curve tracer was used to measure the leakage current of the SiC MOSFETs at increasing temperature. This was done by first shorting the gate and source terminals of the device under test such that the gate-source voltage remained at 0 V, and thus the device was off. Next, the drain current of the device was measured as the drain-source voltage was increased. This measured drain current is known as leakage current since it is current that flows through the device when it is in the off state. The applied drain-source bias is known as the blocking voltage as it is the voltage that the device is supporting. At a blocking voltage of 1200 V, all of the SiC MOSFETs listed in Table I showed leakage

currents well below 10 μA . Since the resolution of the 371b curve tracer is 10 $\mu\text{A}/\text{div}$ at this power level, a specific leakage current value could not be accurately determined.

Typically, as the temperature of transistors rises, the leakage currents increase. This is due to the intrinsic carrier concentration increasing exponentially with temperature [8]. However, even at 200 $^{\circ}\text{C}$, the SiC MOSFETs under study revealed leakage currents of much less than 10 μA at a blocking voltage of 1200 V. This is a significant improvement when compared to similarly-rate Si transistors, and is due to the lower intrinsic carrier concentration and wide bandgap of SiC. This result demonstrates the high temperature capabilities of the SiC MOSFETs.

2.3.3 Threshold Voltage

The threshold voltage is the gate-source voltage needed for current to start flowing through the channel of the device. In this study, the threshold voltage was taken to be the gate-source voltage at which the drain current reached 1 mA. For the measurement, the gate and drain terminals of the device were shorted such that the gate-source and drain-source voltages were equal, which is a standard practice. The curve tracer was then put into high voltage mode such that fine current resolution could be achieved. However, in this mode, the minimum voltage resolution is 50 V/div, which is more than an order of magnitude higher than the threshold voltages of these devices. Consequently, an oscilloscope was used to measure the gate-source (or equivalently the drain-source) voltage at which 1 mA of drain current was reached.

Figure 4 shows a plot of threshold voltage versus temperature for the SiC MOSFETs in question. The threshold voltages of these SiC MOSFETs are low compared to those of Si MOSFETs. Furthermore, the threshold voltages show a negative

temperature coefficient, decreasing by nearly 40 % at 200 °C when compared to their room temperature values. This negative temperature coefficient of the threshold voltage is also experienced in Si MOSFETs, and is due to the increase in intrinsic carrier concentration with increased temperature [6]. Due to the combination of a low threshold voltage at room temperature and this negative temperature coefficient, when utilizing these SiC MOSFETs, a negative gate-source voltage should be applied during the off-state to ensure that the devices do not experience false turn on.

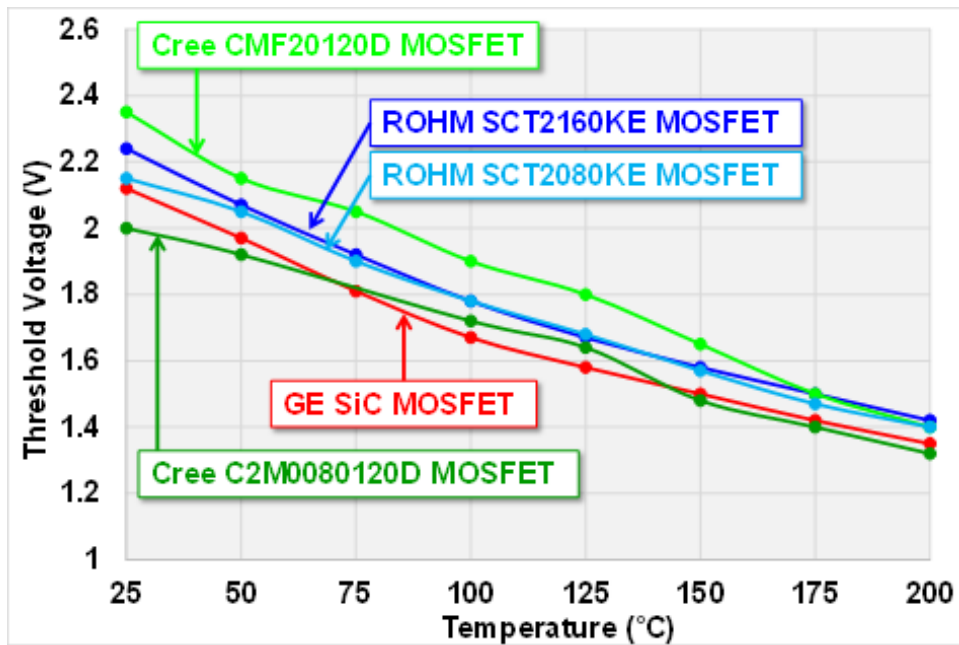


Figure 4: Plot of threshold voltage versus temperature for all five SiC MOSFETs with a drain current of 1 mA and the gate-drain terminals shorted [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, “High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs,” IEEE ECCE, pp. 3235-3242, Sept. 2013].

2.3.4 Transfer Characteristics/Transconductance

The transfer characteristics of the MOSFETs were obtained by measuring the drain current as the gate-source voltage was swept for a fixed drain-source voltage.

Figure 5 shows the transfer (drain current versus gate-source voltage) curves of each of the SiC MOSFETs taken at a drain-source voltage of 20 V for temperatures of 25 °C and 200 °C. It can be observed that the majority of the SiC MOSFETs have similar transfer curves at room temperature. The transfer curves of Cree's C2M0080120D MOSFET, however, showed a noticeably steeper gradient, especially at lower current densities. It can also be observed from this figure that the slopes of the transfer curves for these MOSFETs increase with temperature at low current densities, but decrease with temperature at higher currents. Although the transfer curves presented in the datasheets [45]-[49] for these devices were obtained under different drain-source voltage conditions, in general, the measured results presented in this work are in good agreement with the manufacturer data.

The slope of the transfer curve is known as the transconductance g_{fs} of the MOSFET. The transconductance can therefore be expressed as

$$g_{fs} = \frac{\Delta I_d}{\Delta V_{gs}} \quad (2)$$

This is the gain of the MOSFET as it gives the change in drain current (the output) obtained for a given change in gate-source voltage (the input). Figure 6 shows the transfer curves for Cree's C2M0080120D SiC MOSFET at a drain-source voltage of 20 V for temperatures from 25 °C to 200 °C. From this figure, it can be observed that the slope of the transfer curve, and thus the transconductance, of the SiC MOSFET does not change much as the temperature is increased from 25 °C to 200 °C, until currents of approximately 30 A. At drain currents larger than this value, a noticeable decrease in the slope is observed as the temperature is increased. Compared to similarly rated Si power MOSFETs, these SiC MOSFETs experience lower transconductances, but feature smaller

negative temperature coefficients. The impact of this modest transconductance will also be discussed in a subsequent section.

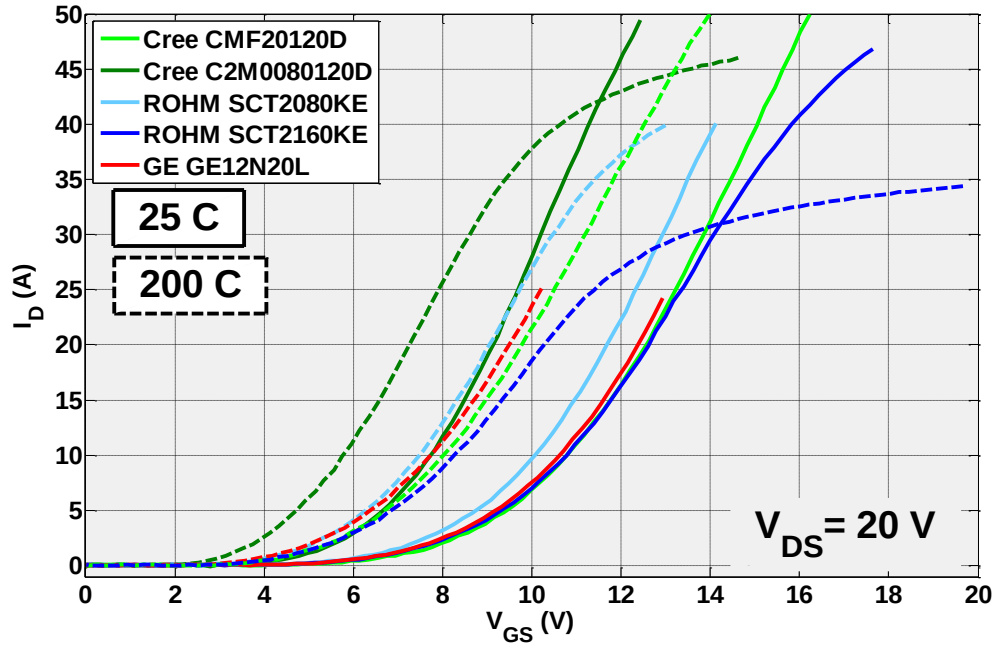


Figure 5: Transfer curves of each of the SiC MOSFETs taken at a drain-source voltage of 20 V for temperatures of 25 °C (solid curves) and 200 °C (dashed curves).

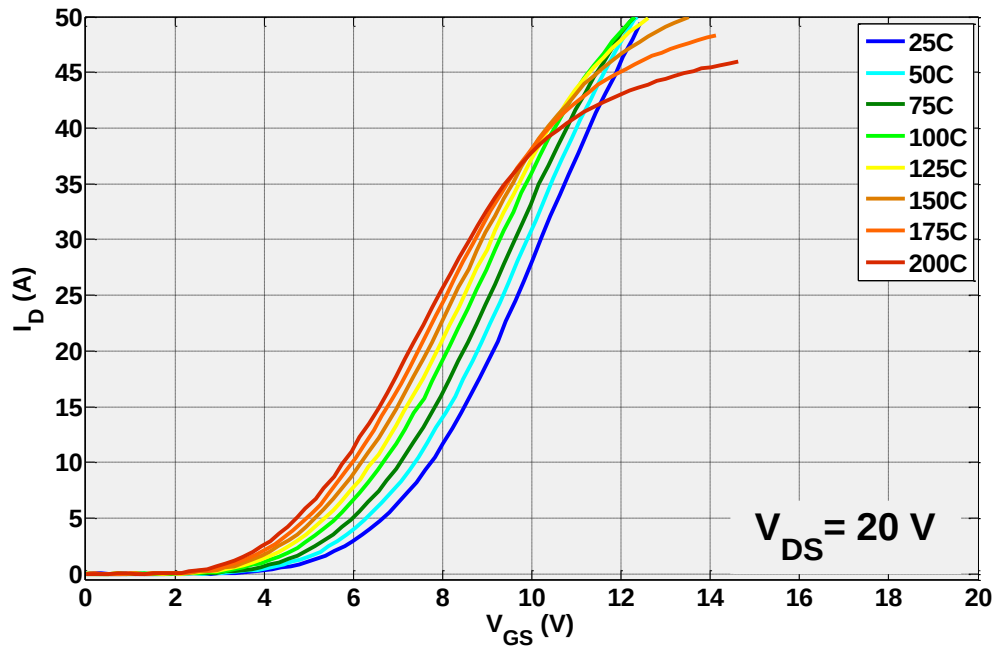


Figure 6: Transfer curves for Cree's C2M0080120D SiC MOSFET at a drain-source voltage of 20 V for temperatures from 25 °C (blue) to 200 °C (red).

2.3.5 Output Characteristics/On-Resistance

The I-V curves, or output characteristics, of each MOSFET were measured using a curve tracer and four-terminal (or Kelvin) sensing for temperatures from 25 °C to 200 °C. Figure 7 shows the I-V curve comparison of one of the SiC MOSFETs for temperatures of 25 °C and 200 °C, and gate-source voltages of 10 V to 20 V. This comparison demonstrates the low temperature dependency of the on-state characteristics of the SiC MOSFETs. It can also be observed that for gate-source voltages of 16 V or less, the linear region of the I-V curves become steeper with increased temperature. This indicates that if this MOSFET is driven at gate-source voltages of 16 V or less, then the on-resistance will feature a negative temperature coefficient. At 18 V gate-source voltage, almost no change is seen between the curves taken at 25 °C and 200 °C,

suggesting near constant conduction losses with increased temperature. However, for optimal performance, a gate-source voltage of 20 V is recommended for the SiC MOSFETs. As shown by figure, the slope of the linear region of the I-V curves at this gate-source voltage decreases with increased temperature, resulting in a positive temperature coefficient of the on-resistance under this input condition.

From the I-V curve, the on-resistance of each SiC MOSFET was calculated. Figure 8 shows the on-resistance versus temperature curves for each of the SiC MOSFETs. The on-resistances were measured at a gate-source voltage of 20 V, and at the drain current values listed in parenthesis in the figure. As shown by the figure, ROHM's SCT2160KE MOSFET has a higher on-resistance than the other SiC MOSFETs in this study. This can be partly attributed to its smaller size.

As mentioned previously, a smaller device will result in a higher on-resistance for a given blocking voltage. Consequently, it is important to look at the specific on-resistances of the devices. In this case, this figure was obtained by multiplying the measured on-resistance values by the die area of the device. Typically, the active area is used for this calculation, however, this dimension could not be obtained for all of the devices in this study, and so the die area was used instead.

Figure 9 shows the measured specific on-resistance versus temperature. The drain currents used for the measurements are shown in parentheses. The gate-source voltage used for the on-resistance measurement was 20 V since this is the voltage at which the MOSFETs will be driven. As seen in the figure, the GE MOSFET is the least temperature dependent, increasing by approximately 59 % at 200 °C with respect to its room temperature resistance. When compared to Si power MOSFETs, these SiC MOSFETs

feature significantly lower, and less temperature-sensitive, on-resistances. This lesser temperature coefficient can be partially attributed to the decrease in the channel resistance of 4H-SiC MOSFETs with increasing temperature due to an increase in MOS channel mobility [37] caused by the de-trapping of charges in the gate oxide. This decrease in the channel resistance counteracts the increase of the drift region resistance, resulting in a lower positive temperature coefficient in the total on-state resistance [37], [41]-[44].

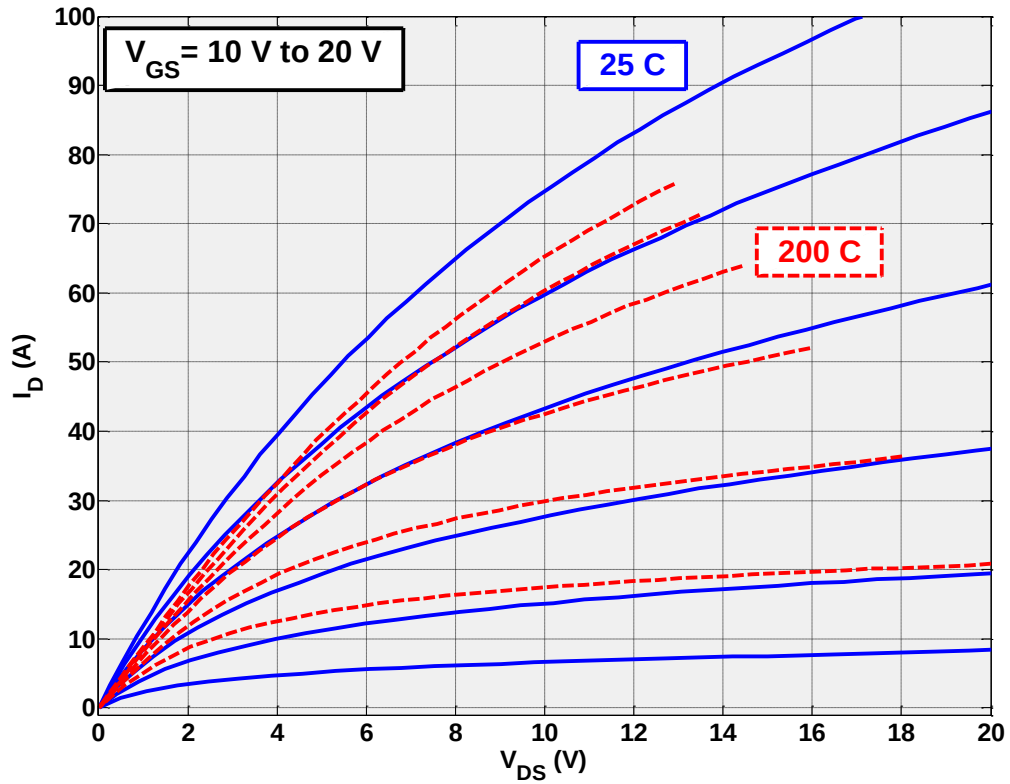


Figure 7: I-V curves of a SiC MOSFET for temperatures from 25 °C (blue solid curves) to 200 °C (red dashed curves), and gate-source voltages of 10 V to 20 V with 2 V steps.

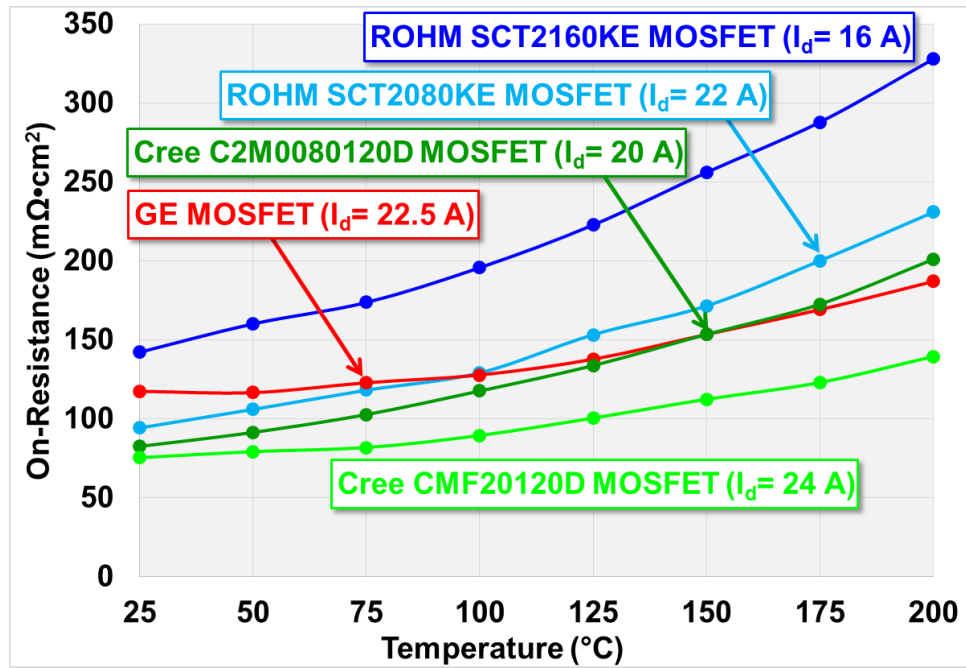


Figure 8: On-resistance versus temperature curves for each of the SiC MOSFETs at a gate-source voltage of 20 V and the drain currents specified in parentheses.

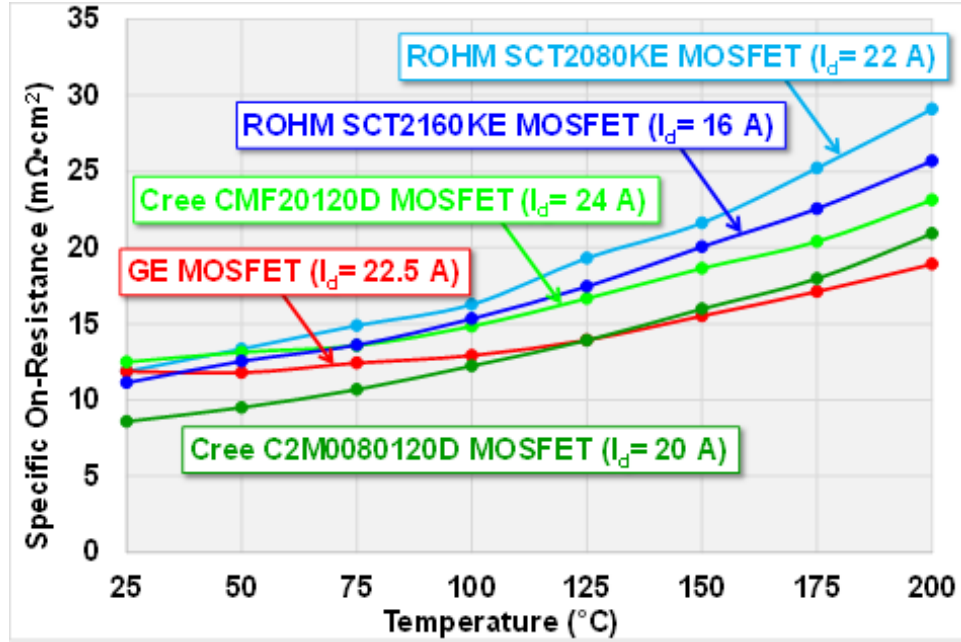
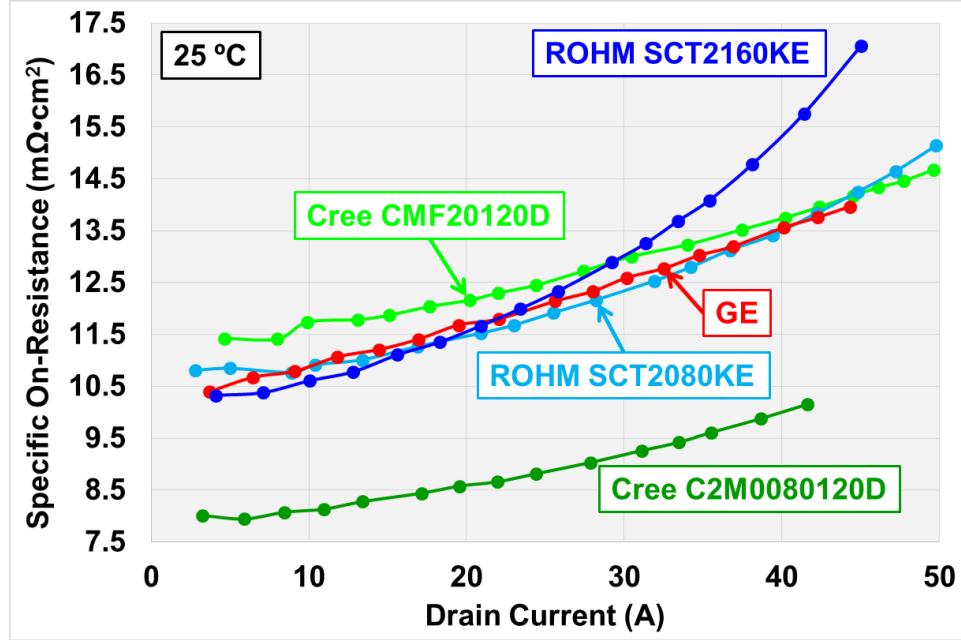


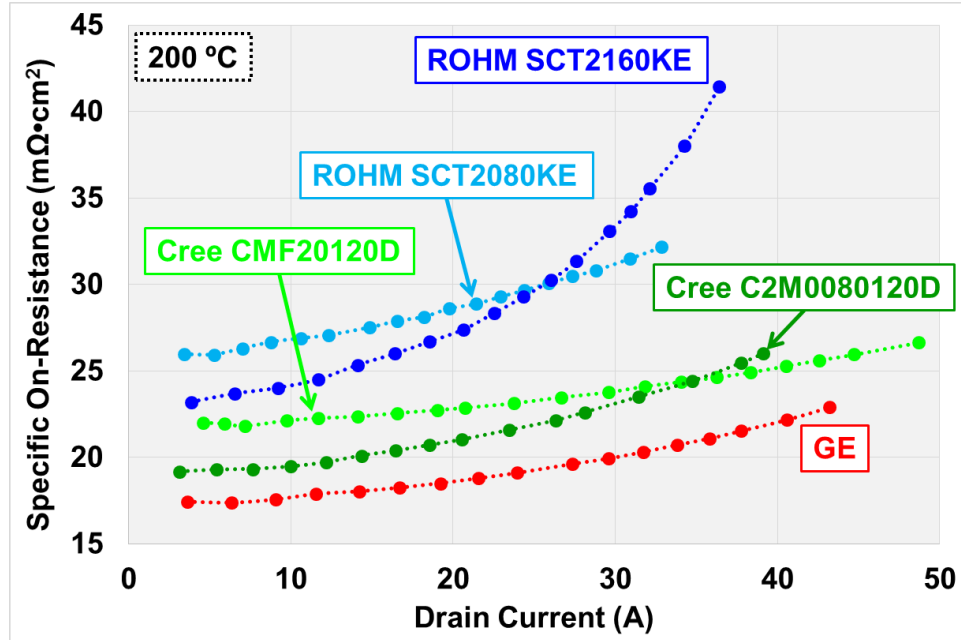
Figure 9: Specific on-resistance (using die area) versus temperature curves for each of the SiC MOSFETs at a gate-source voltage of 20 V and the drain currents specified in parentheses [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, “High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs,” IEEE ECCE, pp. 3235-3242, Sept. 2013].

Figure 10a and Figure 10b show the specific on-resistance versus drain current curves at 25 °C and 200 °C, respectively, for each of the SiC MOSFETs. As shown, while most of the MOSFETs have similar specific on-resistances at 25 °C, Cree’s C2M0080120D experiences a lower specific resistance by approximately 3 mΩ·cm² at all drain currents. However, at 200 °C, GE’s MOSFET proves to have the lowest specific on-resistance. Furthermore, ROHM’s SCT2160KE MOSFET is shown to be the most sensitive to higher load currents. This can be attributed to the fact that it has the smallest die area, and thus the highest resistance and lowest current rating. As listed in Table I, the SCT2160KE has a continuous current rating of 16 A at 100 °C, so an increase in on-resistance at larger drain currents is expected, especially at elevated temperatures. The

on-resistance curves presented in this work are in good agreement with those given in the datasheets [45]-[49] of these SiC MOSFETs.



(a)



(b)

Figure 10: Specific on-resistance (using die area) versus drain current curves for each of the SiC MOSFETs at a gate-source voltage of 20 V, and (a) 25 °C, and (b) 200 °C.

2.3.6 Body Diode I-V Characteristics

The body diode I-V curves were determined using a curve tracer and four-terminal measurement. With the gate and source terminals shorted, a bias was applied across the source and drain of the device, and the current flowing from the source to the drain through the body diode could be sensed. The resulting body diode I-V curves for the SiC MOSFETs at 25 °C and 200 °C are shown in Figure 11. As can be seen from the figure, all of the SiC MOSFETs experience a reduction in the body diode forward turn on voltage as the temperature is increased. However, it can also be observed that each of the SiC MOSFETs feature different slopes in their body diode I-V curves, with the Cree C2M0080120D MOSFET having the steepest slope, and the ROHM SCT2080KE MOSFET having the most gradual. A steeper slope corresponds to a lower resistance in series with the body diode, and thus allows for reduced on-state losses when the body diode is conducting [50].

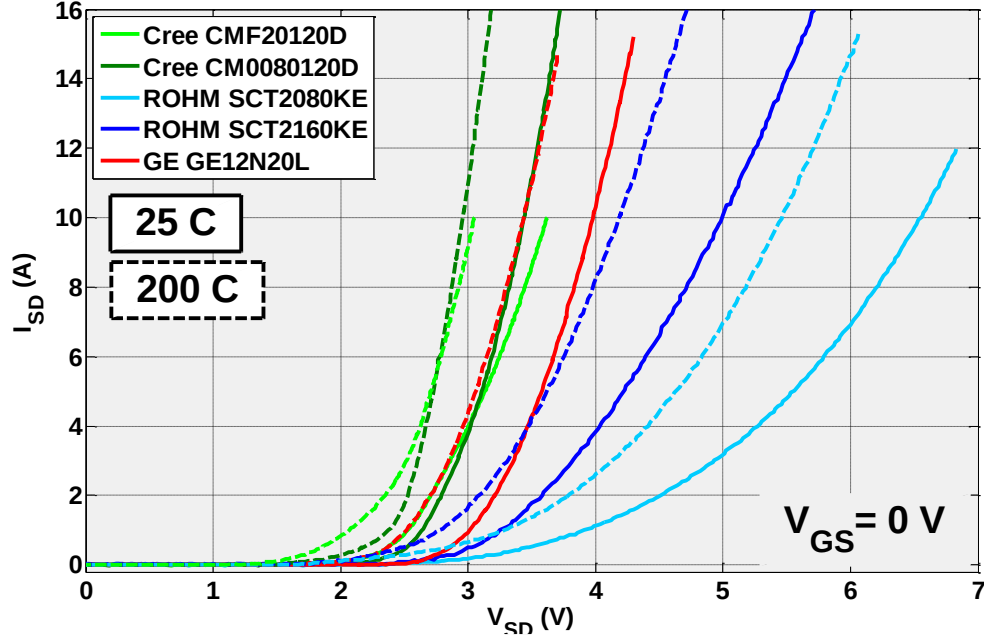


Figure 11: Body diode I-V curves for the SiC MOSFETs at 25 °C (solid curves) and 200 °C (dashed curves) for a gate-source voltage of 0 V.

2.3.7 Internal Gate Resistance

The internal gate resistance of a MOSFET will greatly influence its dynamic performance. Figure 12 depicts the measurement setup and equivalent circuit for the determination of the internal gate resistances. The internal gate resistance of each SiC MOSFET was determined using the impedance analyzer to measure across the gate and source terminals with the drain floating. Measurements were taken at a frequency of 1 MHz. The resulting values are presented in Table II, and are in good agreement with those listed in the datasheets [45]-[49]. It can be seen that ROHM's SCT2160KE has the highest internal gate resistance, while GE's MOSFET has the lowest. This large variation in internal gate resistances among the different MOSFETs in this study makes it essential to test various external gate resistances when evaluating their dynamic performance.

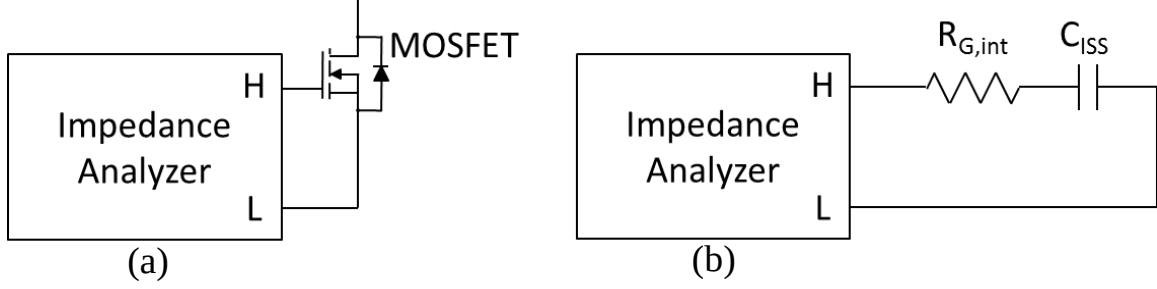


Figure 12: (a) Measurement setup, and (b) equivalent circuit, for the measuring the internal gate resistance of the devices.

Table II: Internal gate resistances of the SiC MOSFETs [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, “High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs,” IEEE ECCE, pp. 3235-3242, Sept. 2013].

<i>Mfg.</i>	<i>Device</i>	<i>Internal Gate Resistance</i>
Cree	CMF20120D	4.98 Ω
	C2M0080120D	4.85 Ω
GE	GE12N20L	2.41 Ω
ROHM	SCT2080KE	7.25 Ω
	SCT2160KE	13.7 Ω

2.3.8 Junction Capacitances

The junction capacitances of each SiC MOSFET were measured under increasing drain-source voltage. The measurements were only conducted at room temperature since it has been shown that the junction capacitances are independent of temperature [50].

Schematics of the test circuits used for the measurement of the input capacitance C_{ISS}

($C_{GS} + C_{GD}$), output capacitance C_{OSS} ($C_{DS} + C_{GD}$), and Miller capacitance C_{RSS} (C_{GD}), are shown in Figure 13a, Figure 13b, and Figure 13c, respectively. These circuits, presented in [50], were used to extend the voltage bias (represented by V_{DS} in the schematics) since the Agilent 4294A can only supply up to 40 V. The 1 μ F capacitor connected to the “High” terminal of the impedance analyzer serves to protect the instrument from the high voltage bias V_{DS} . The capacitances were all measured at a frequency of 1 MHz.

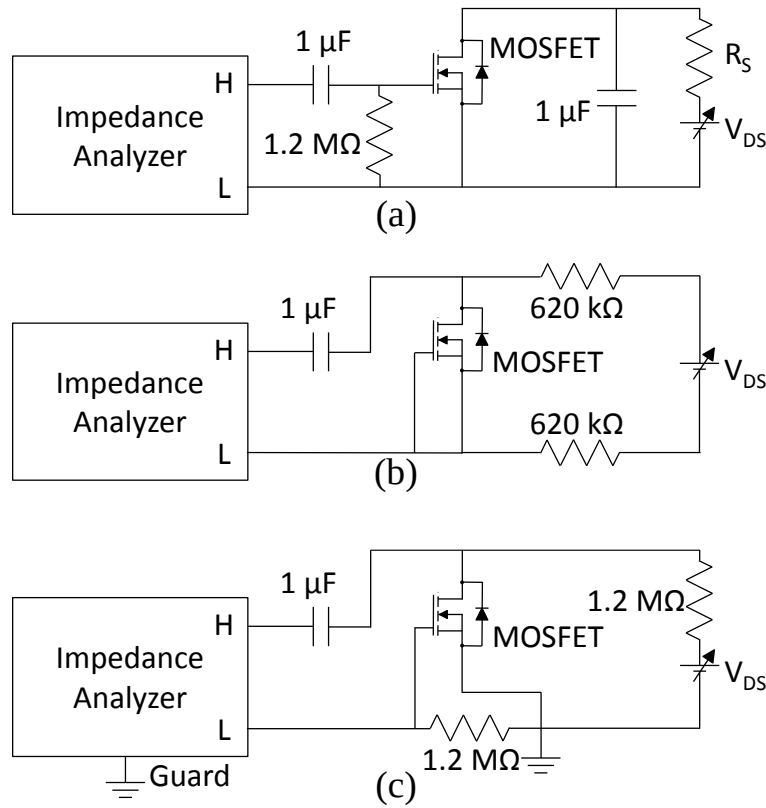


Figure 13: Measurement setup for determination of the (a) input capacitance, (b) output capacitance, and (c) Miller capacitance of the devices as was presented in [Z. Chen, “Characterization and modeling of high-switching-speed behavior of SiC active devices,” M.S. thesis, Dept. Elect. Comput. Eng., Virginia Tech, Blacksburg, VA, 2009], and used in [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, “High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs,” IEEE ECCE, pp. 3235-3242, Sept. 2013].

The resulting capacitance versus voltage curves at room temperature are shown in Figure 14, Figure 15, and Figure 16, and are in good agreement with those given in the datasheets [45]-[49] of these SiC MOSFETs. As shown in Figure 14, Cree's C2M0080120D has the lowest input capacitance, followed by the GE and ROHM SCT2160KE MOSFETs, which have nearly identical values. A smaller input capacitance will reduce the time constant of the gate loop, resulting in shorter switching delays and faster drain current slew rates.

Figure 15 shows that ROHM's SCT2160KE has the lowest output capacitance, while Cree's CMF20120D has the highest. The other MOSFETs all had similar output capacitances at all measured biases. The output capacitance is the primary contributor to the parasitic ringing during the turn off transient. This is because during turn off the current sees the drain-source parasitic inductance in series with the output capacitance. During turn on, however, the junction capacitance of the freewheeling diode is also in the current path, and, since this capacitance is typically much smaller than the MOSFET's output capacitance, it is the main contributor of the parasitic ringing [50]. The output capacitance is also responsible for a slower drain-source voltage slew rate. This is due to a longer charging time of the drain-source capacitance.

Finally, Figure 16 shows that the ROHM SCT2160KE and Cree C2M0080120D MOSFETs have the smallest Miller capacitances, while the ROHM SCT2080KE MOSFET has the largest. The Miller capacitances of the GE and Cree CMF20120D MOSFETs are similar at biases greater than 40 V. The Miller capacitance has a more pronounced impact on the drain-source voltage slew rate, and thereby has a greater influence on the switching losses. The impact of these capacitances on the switching

performance of these SiC MOSFETs will be appreciated when evaluating the switching behaviors of the devices in the subsequent section.

These capacitance curves also show that, in general, the MOSFETs with the larger die sizes tend to have higher capacitances. If these measured capacitances are divided by the die area, then the specific capacitances of the devices can be plotted to verify this postulation. As shown by Figure 17, Figure 18, and Figure 19, the distribution in specific capacitances is much narrower than that of the regular capacitance measurements. Figure 17 shows that the specific input capacitances of the ROHM SiC MOSFETs are identical. Figure 18 reveals that all of the SiC MOSFETs have nearly overlapping specific output capacitances. No substantial changes were seen for the specific Miller capacitance curve (Figure 19) though.

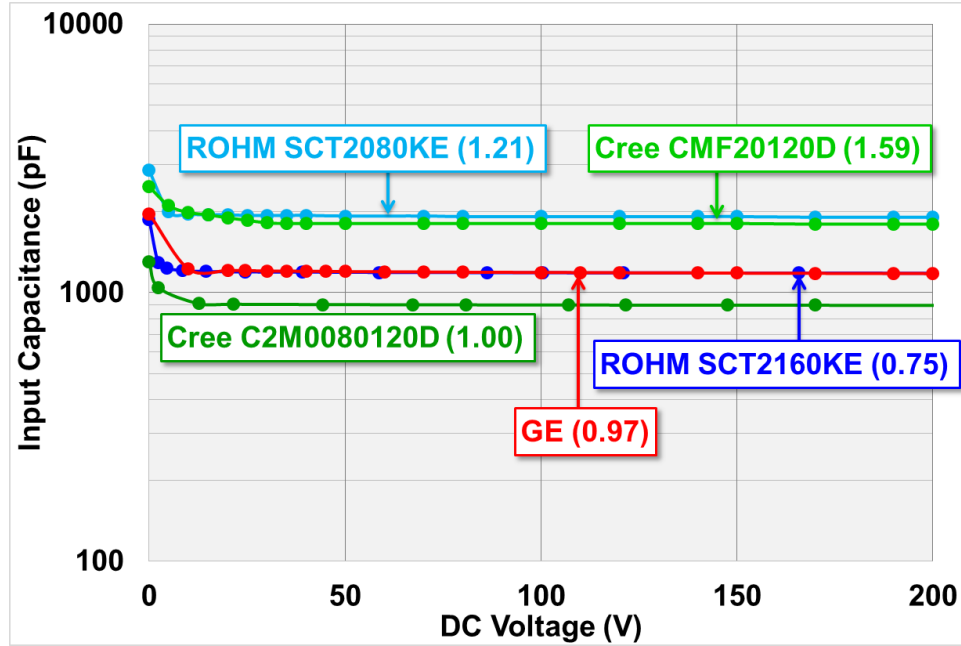


Figure 14: Input capacitance versus voltage curves for the SiC MOSFETs measured at 1 MHz and room temperature. The die areas of the devices normalized to that of Cree's C2M0080120D SiC MOSFET are shown in parentheses [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, "High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs," IEEE ECCE, pp. 3235-3242, Sept. 2013].

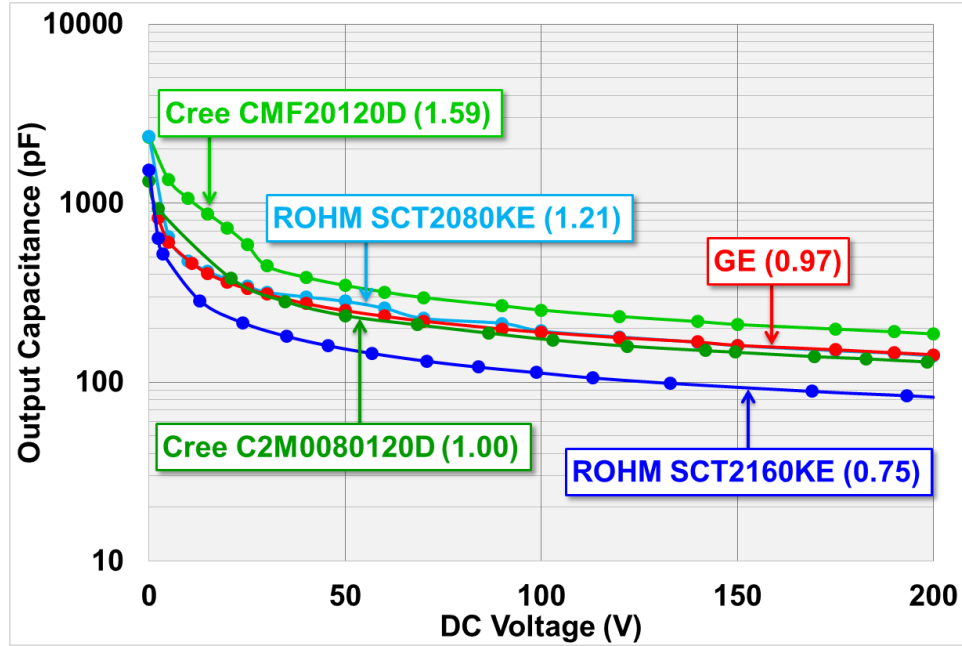


Figure 15: Output capacitance versus voltage curves for the SiC MOSFETs measured at 1 MHz and room temperature. The die areas of the devices normalized to that of Cree's C2M0080120D SiC MOSFET are shown in parentheses [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, "High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs," IEEE ECCE, pp. 3235-3242, Sept. 2013].

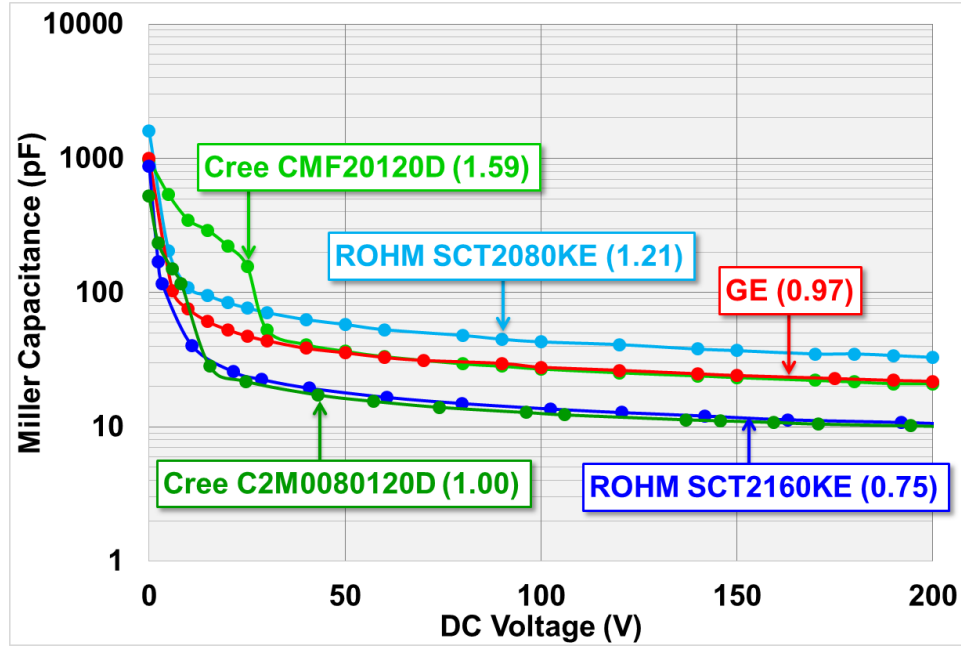


Figure 16: Miller capacitance versus voltage curves for the SiC MOSFETs measured at 1 MHz and room temperature. The die areas of the devices normalized to that of Cree's C2M0080120D SiC MOSFET are shown in parentheses [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, "High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs," IEEE ECCE, pp. 3235-3242, Sept. 2013].

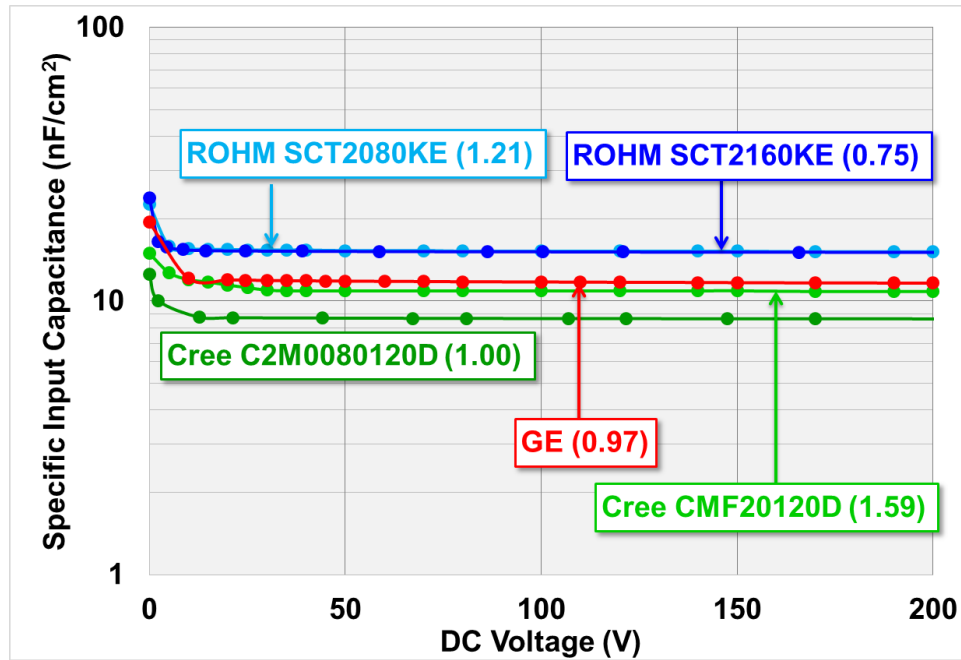


Figure 17: Specific input capacitance versus voltage curves for the SiC MOSFETs measured at 1 MHz and room temperature. The die areas of the devices normalized to that of Cree's C2M0080120D SiC MOSFET are shown in parentheses.

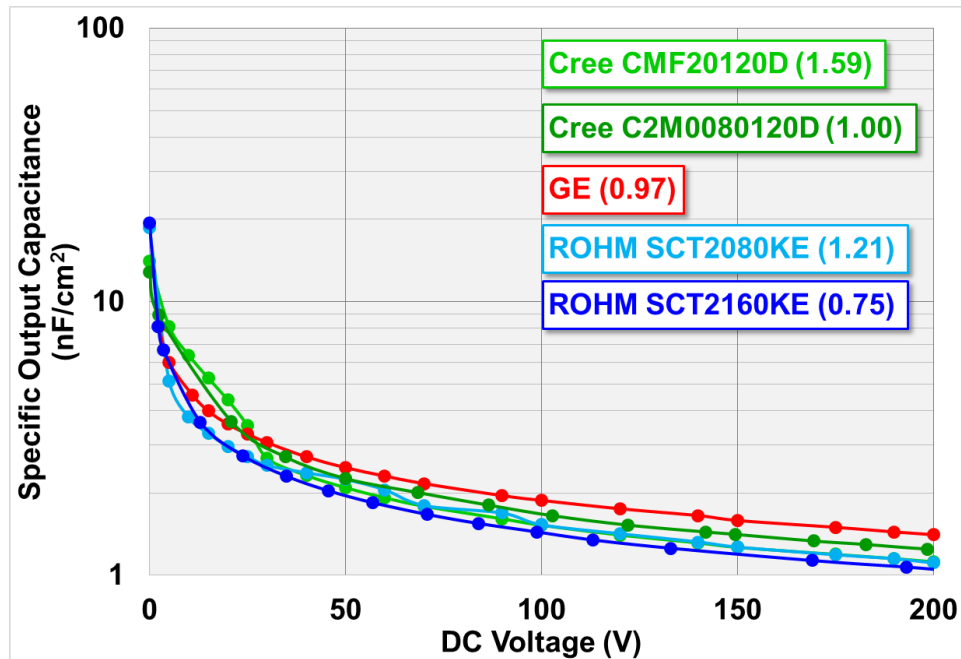


Figure 18: Specific output capacitance versus voltage curves for the SiC MOSFETs measured at 1 MHz and room temperature. The die areas of the devices normalized to that of Cree's C2M0080120D SiC MOSFET are shown in parentheses.

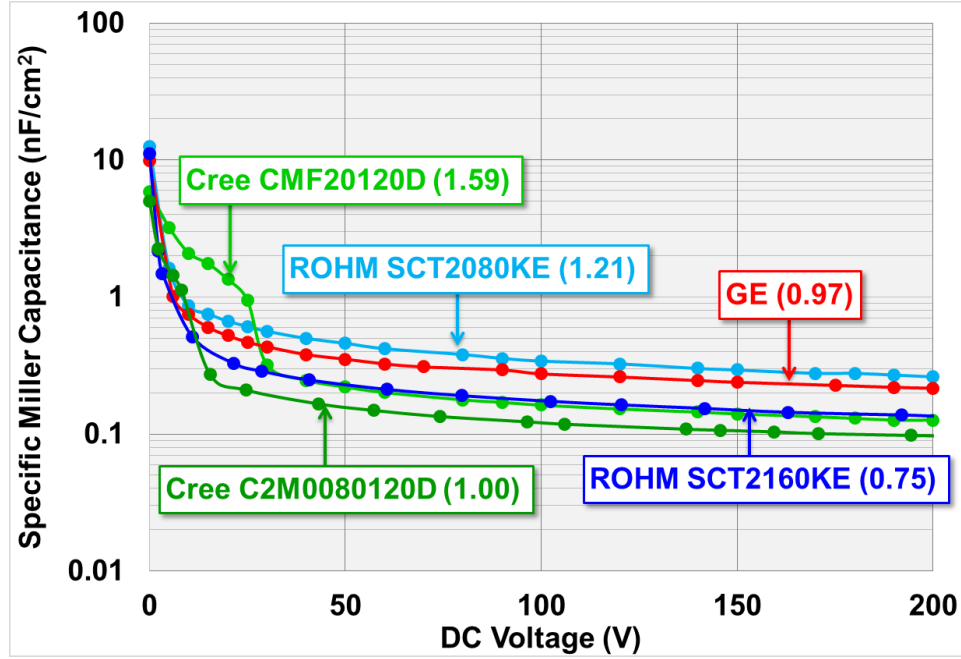


Figure 19: Specific Miller capacitance versus voltage curves for the SiC MOSFETs measured at 1 MHz and room temperature. The die areas of the devices normalized to that of Cree's C2M0080120D SiC MOSFET are shown in parentheses.

2.4 Dynamic Characterization of the 1.2 kV SiC MOSFETs

In the following subsections, the driving and measurement methods used for the dynamic characterization of the SiC MOSFETs will be presented. The switching energy losses of each device for different load currents and temperatures will also be shown. A comparison of the dynamic performance of the devices will then be provided.

2.4.1 Dynamic Characterization Methods

Double-Pulse Tests (DPTs) were performed on each SiC MOSFET with a DPT setup specifically designed to reduce the parasitic components that inhibit switching performance. The layout is based on the DPT board described in [51], and is similar to the tester used in [50]. A simplified schematic of the DPT setup is shown in Figure 20.

Cree's C2D10120A SiC Schottky diode was used as the freewheeling diode (FWD), and the same IXDD614 low-side MOSFET gate driver (which has an output resistance of $0.3\ \Omega$) was used for all of the devices in this study.

To conduct the measurements, a BNC and high voltage probe were used to measure the drain-source voltage, a probe-tip-adaptor and low-voltage passive probe were used to measure the gate-source voltage, and a $0.1\ \Omega$ coaxial shunt from T&M and BNC cable was used to measure the drain current of the different devices. The source ground was isolated to reduce noise. All of the DPTs reported in this paper were conducted for a dc bus voltage of 600 V. Figure 21 shows an image of the DPT hardware with the key components labeled.

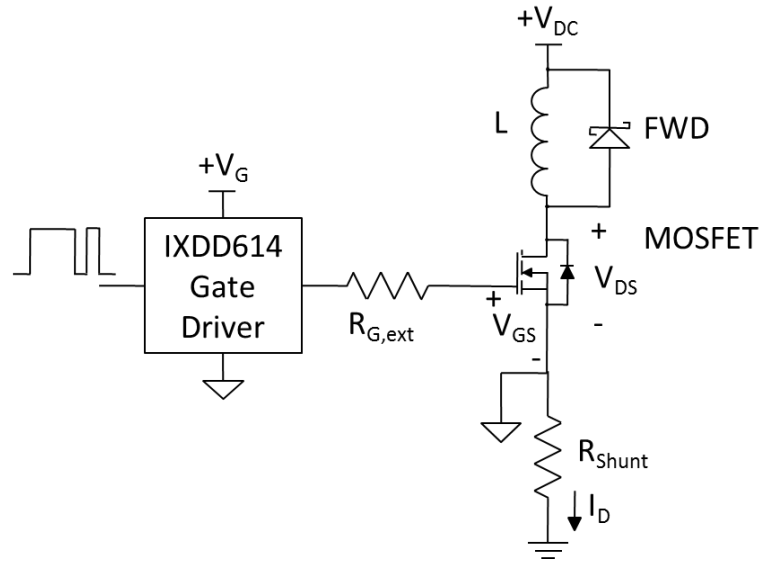


Figure 20: Schematic of the double-pulse test setup used for the dynamic characterization of the SiC MOSFETs [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, “High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs,” *IEEE ECCE*, pp. 3235-3242, Sept. 2013], [C. DiMarino, Z. Chen, D. Boroyevich, R. Burgos, P. Mattavelli, “Characterization and comparison of 1.2 kV SiC power semiconductor devices,” *IEEE EPE*, pp. 1-10, Sept. 2013], and [C. DiMarino, Z. Chen, D. Boroyevich, R. Burgos, P. Mattavelli, “High-temperature characterization and comparison of 1.2 kV SiC power semiconductor devices,” *J. Microelectron. Electron. Packaging*, vol. 10, no. 4, pp. 138, 2013].

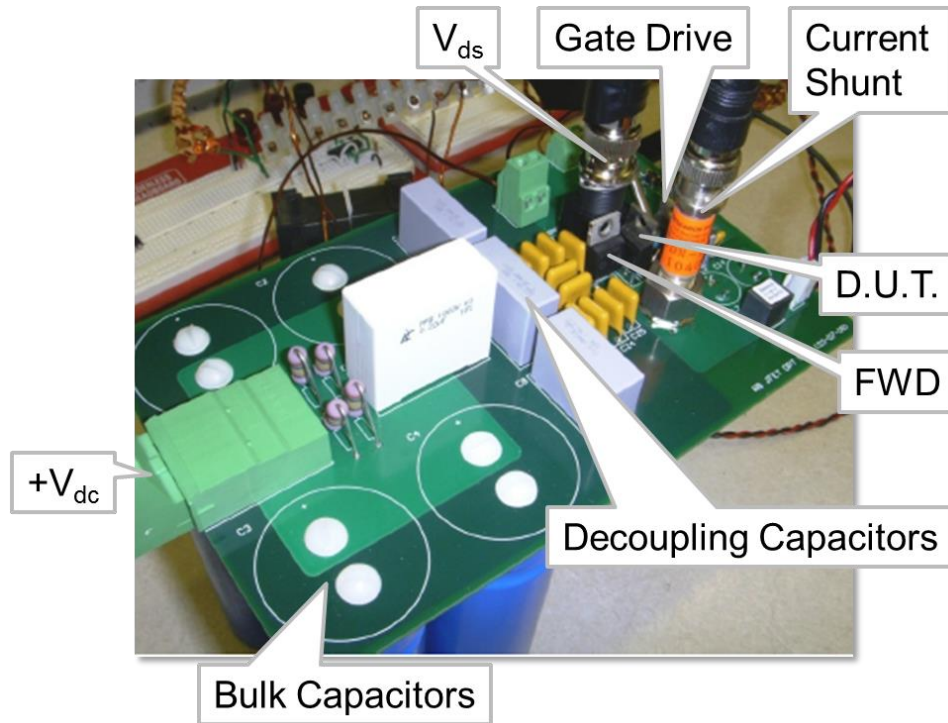


Figure 21: DPT hardware with the key components labeled.

A block diagram was created in LabVIEW that could interface with the function generator. In this way, many double-pulse signals (corresponding to different load current, dc voltage, and inductance combinations) could be easily programmed and stored. This method speeds up the testing of the devices since the signals can be quickly loaded and sent to the function generator. The function generator is then triggered, sending the pulses to the hardware. The oscilloscope then captures the falling and rising edges of the gate-source voltage waveform for the turn off and turn on transitions, respectively. MATLAB is then used to retrieve the data from the oscilloscope, and to compute the turn on and turn off switching energies. The switching losses are calculated by multiplying the drain current and drain-source voltage waveforms in order to get a plot of the instantaneous power. This plot is then integrated 10 % above the peak power value

for both the turn on and turn off transients. The total switching loss is the sum of the turn on and turn off energies. Figure 22 depicts this process.

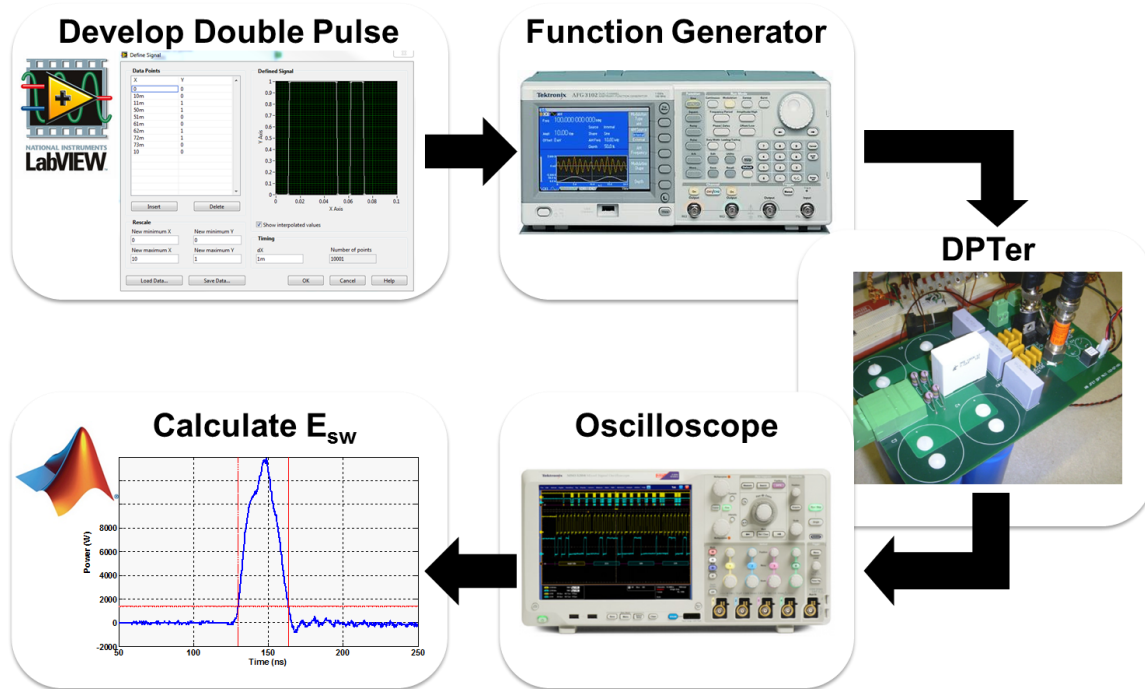


Figure 22: Process used for the double-pulse testing.

2.4.2 Switching Characteristics

In this section, the process used for selecting the optimal external gate resistance for the SiC MOSFETs will be shown. The external gate resistance that yielded the lowest switching energy loss without causing significant ringing was selected. Although details will only be provided for the Cree CMF20120D, ROHM SCT2080KE, and GE GE12N20L MOSFETs, similar testing was performed on the other SiC MOSFETs as well. Once justification has been given on the selection of the external gate resistances, the room temperature switching performance of all of the SiC MOSFETs will be compared. The high temperature switching behavior of the SiC MOSFETs will then be presented.

2.4.2.1 Cree CMF20120D SiC MOSFET

The turn on and turn off waveforms for Cree's CMF20120D SiC MOSFET are shown in Figure 23 and Figure 24, respectively, for a DPT conducted at 600 V, 20 A, and 25 °C with external gate resistances of 0 Ω , 2.5 Ω , 5 Ω , and 10 Ω . Gate voltages of 0 V for the off-state, and 20 V for the on-state were used for the DPTs. Note that the gate-source voltage waveforms have been aligned (bottom subplots) for ease of viewing. As shown by these waveforms, while there was a drastic increase in delay times and slew rates when an external gate resistance of 10 Ω was used, there was little change when the resistance was reduced beyond 2.5 Ω .

When no external gate resistor was added, the Cree CMF20120D MOSFET experienced noticeable ringing in the turn off waveforms (Figure 24). As a result of this ringing, the total switching energy loss was nearly the same for the cases of 0 Ω and 2.5 Ω external gate resistances, with values of 432 μJ and 430 μJ , respectively, for DPTs at 600 V, 20 A, and 25 °C. Since no reduction in the switching loss was achieved when using 0 Ω as the external gate resistance, 2.5 Ω was determined to be the optimal value as it demonstrated less ringing in the waveforms.

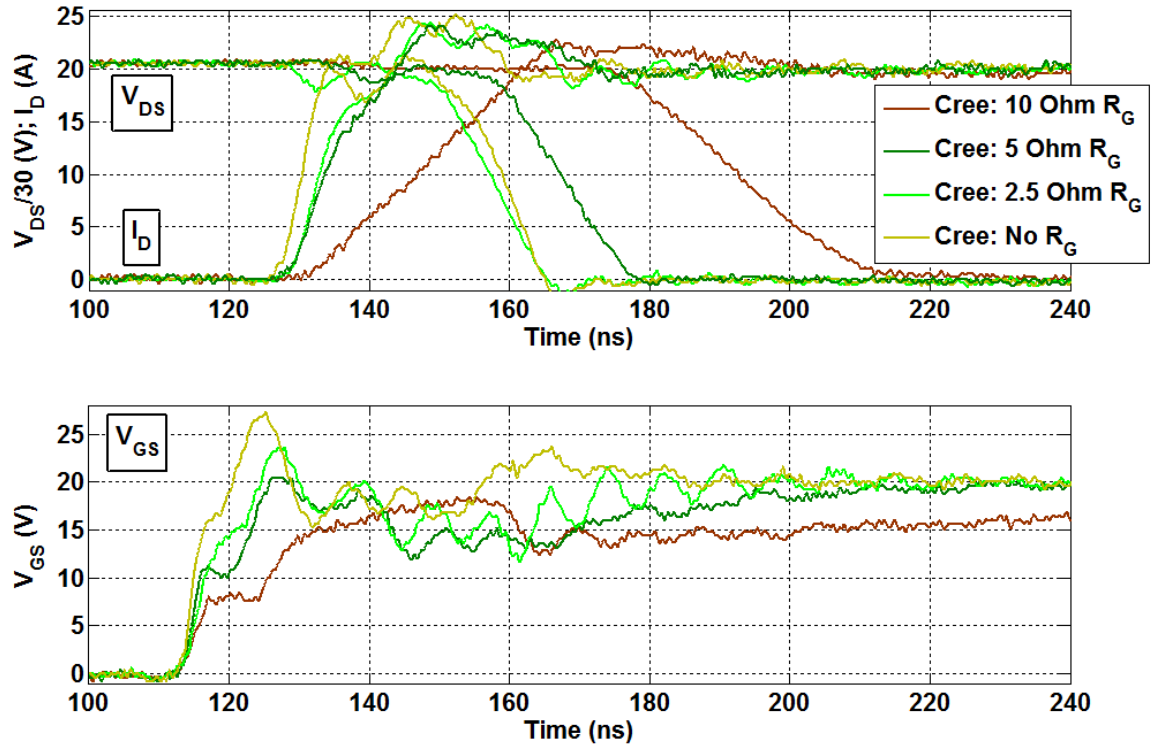


Figure 23: Turn on waveforms for the Cree CMF20120D MOSFET at 600 V, 20 A, and 25 °C for external gate resistances R_G of 0 Ω (gold), 2.5 Ω (green), 5 Ω (dark green), and 10 Ω (brown).

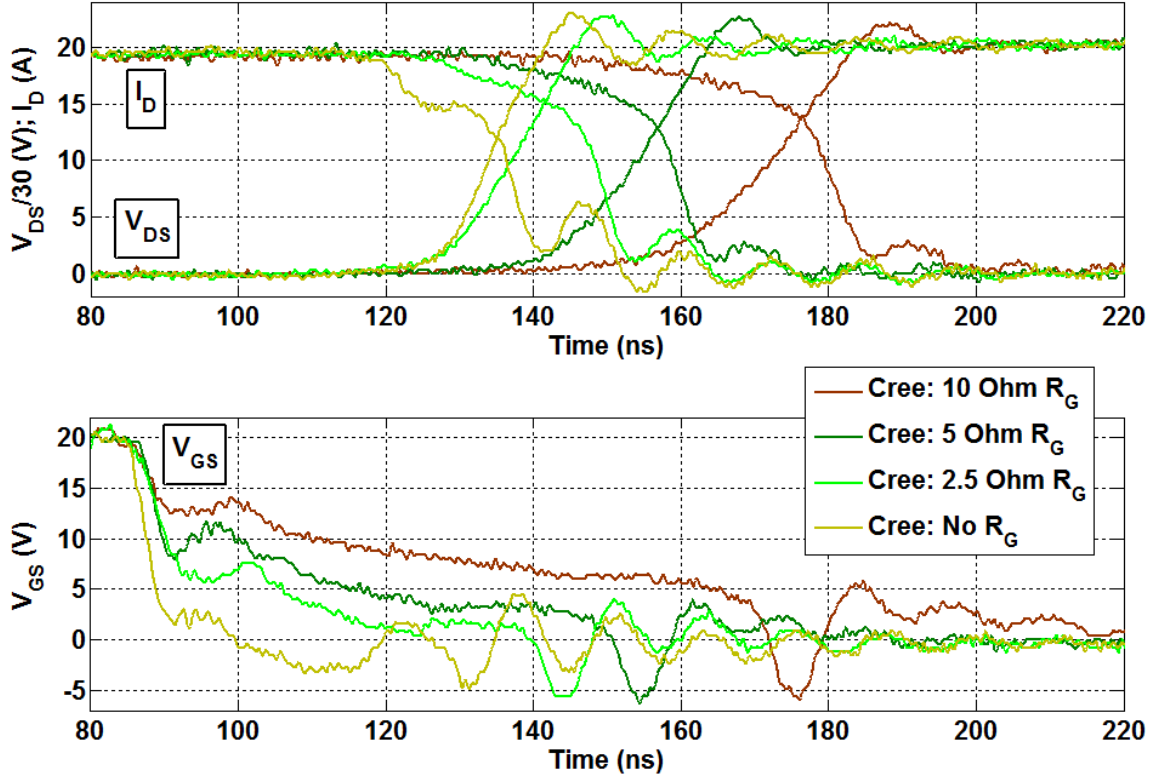


Figure 24: Turn off waveforms for the Cree CMF20120D MOSFET at 600 V, 20 A, and 25 °C for external gate resistances R_G of 0 Ω (gold), 2.5 Ω (green), 5 Ω (dark green), and 10 Ω (brown).

2.4.2.2 ROHM SCT2080KE SiC MOSFET

The turn on and turn off waveforms for ROHM's SCT2080KE SiC MOSFET are shown in Figure 25 and Figure 26, respectively, for a DPT conducted at 600 V, 20 A, and 25 °C with external gate resistances of 0 Ω , 2.5 Ω , 5 Ω , and 10 Ω . Gate voltages of 0 V for the off-state, and 20 V for the on-state were used for the DPTs. As shown by these waveforms, unlike the case for the Cree CMF20120D MOSFET, using no external gate resistor continued to improve the device's switching performance. The switching energy loss reduced from 576 μ J with a 2.5 Ω external gate resistance to 502 μ J with no external gate resistor for DPTs conducted at 600 V, 20 A, and 25 °C. This decrease can be attributed to the slightly larger internal gate resistance of the ROHM SCT2080KE MOSFET (Table

II). This higher internal gate resistance also prevented ringing when no external gate resistor was used. Consequently, a $0\ \Omega$ external gate resistor was determined to be the optimal choice.

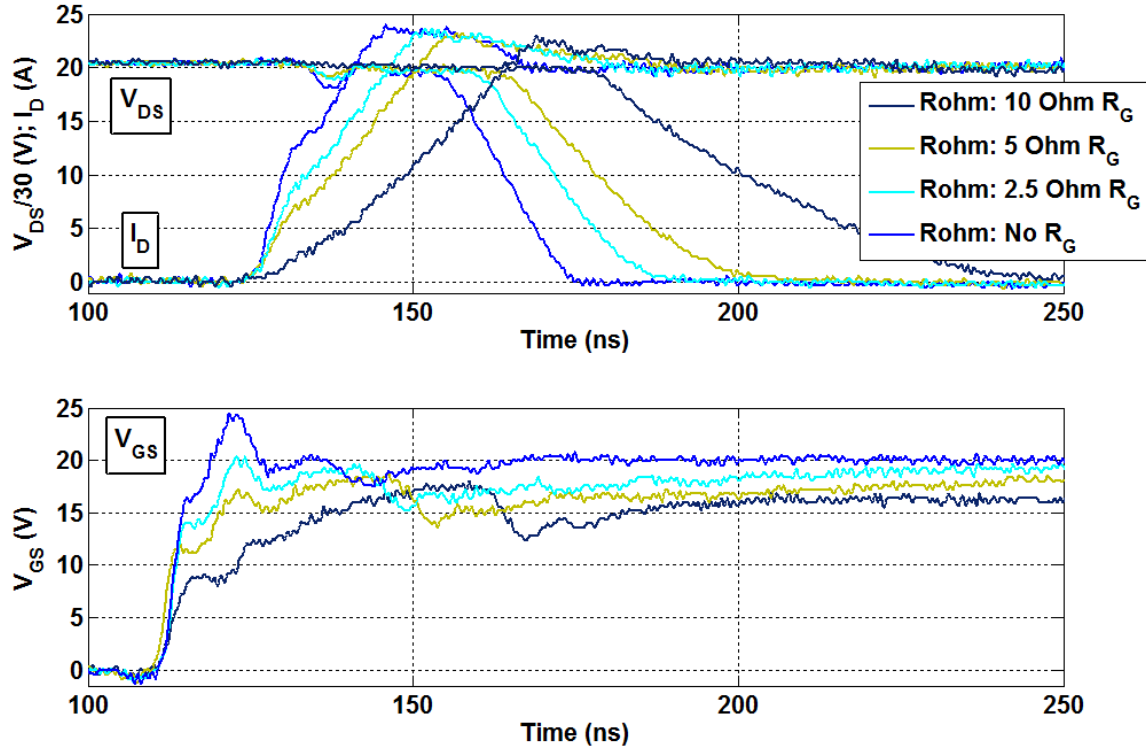


Figure 25: Turn on waveforms for the ROHM SCT2080KE MOSFET at 600 V, 20 A, and 25 °C for external gate resistances R_G of $0\ \Omega$ (blue), $2.5\ \Omega$ (light blue), $5\ \Omega$ (gold), and $10\ \Omega$ (dark blue).

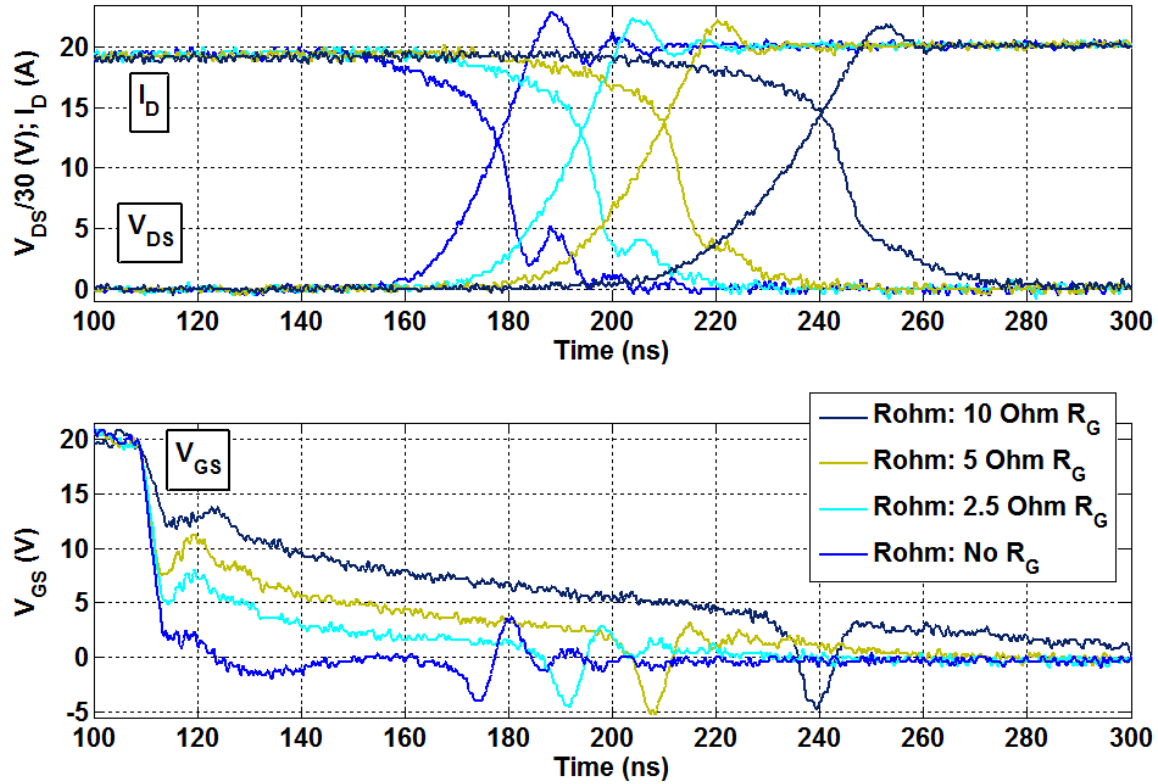


Figure 26: Turn off waveforms for the ROHM SCT2080KE MOSFET at 600 V, 20 A, and 25 °C for external gate resistances R_G of 0 Ω (blue), 2.5 Ω (light blue), 5 Ω (gold), and 10 Ω (dark blue).

2.4.2.3 GE GE12N20L SiC MOSFET

The turn on and turn off waveforms for GE's SiC MOSFET are shown in Figure 27 and Figure 28, respectively, for a DPT conducted at 600 V, 15 A, and 25 °C with external gate resistances of 0 Ω , 5 Ω , and 10 Ω . Gate voltages of 0 V for the off-state, and 20 V for the on-state were used for the DPTs. As shown by these waveforms, reducing the external gate resistance beyond 5 Ω resulted in considerable ringing. However, unlike in the case of the Cree CMF20120D MOSFET, using no external gate resistor further reduced the switching energy loss from 254 μJ with a 5- Ω external gate resistor to 227 μJ (for DPTs carried out at 600 V, 15 A, and 25 °C). Nevertheless, it may be preferable to accept this

extra loss in order to diminish the ringing. For this work, the external gate resistance value of $5\ \Omega$ was determined to be optimal.

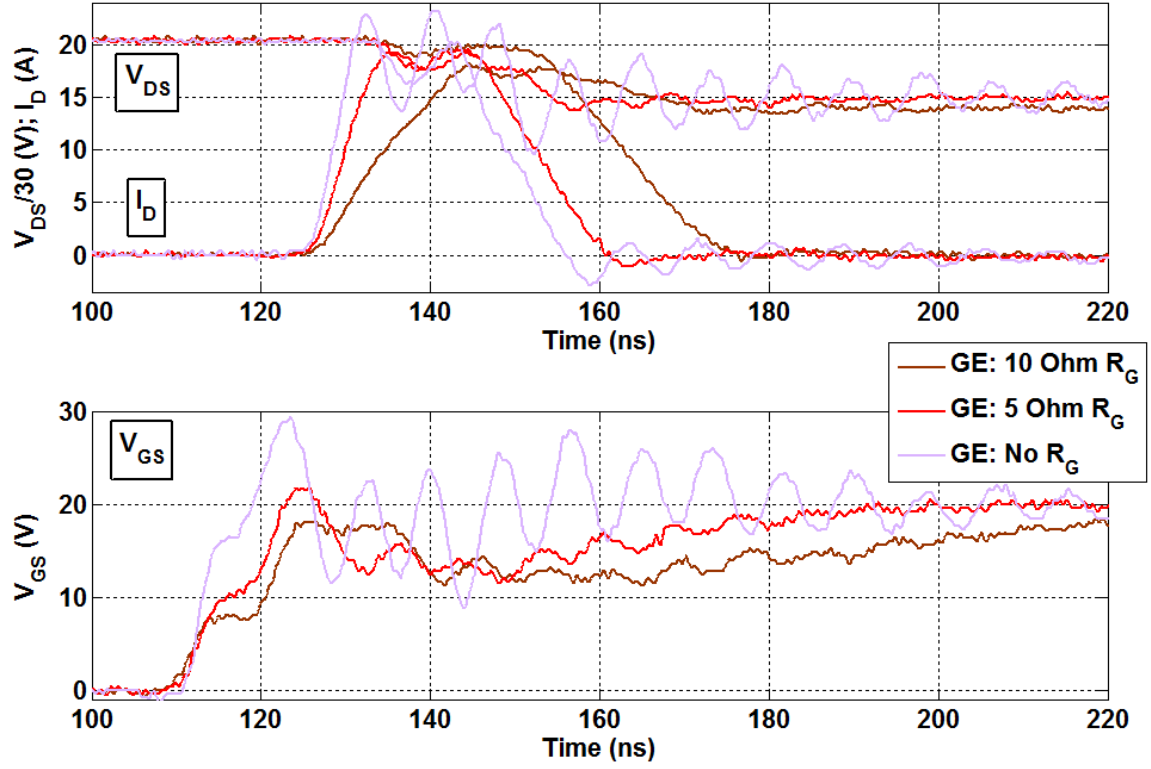


Figure 27: Turn on waveforms for the GE GE12N20L MOSFET at 600 V, 20 A, and 25 °C for external gate resistances R_G of 0 Ω (pink), 5 Ω (red), and 10 Ω (dark red).

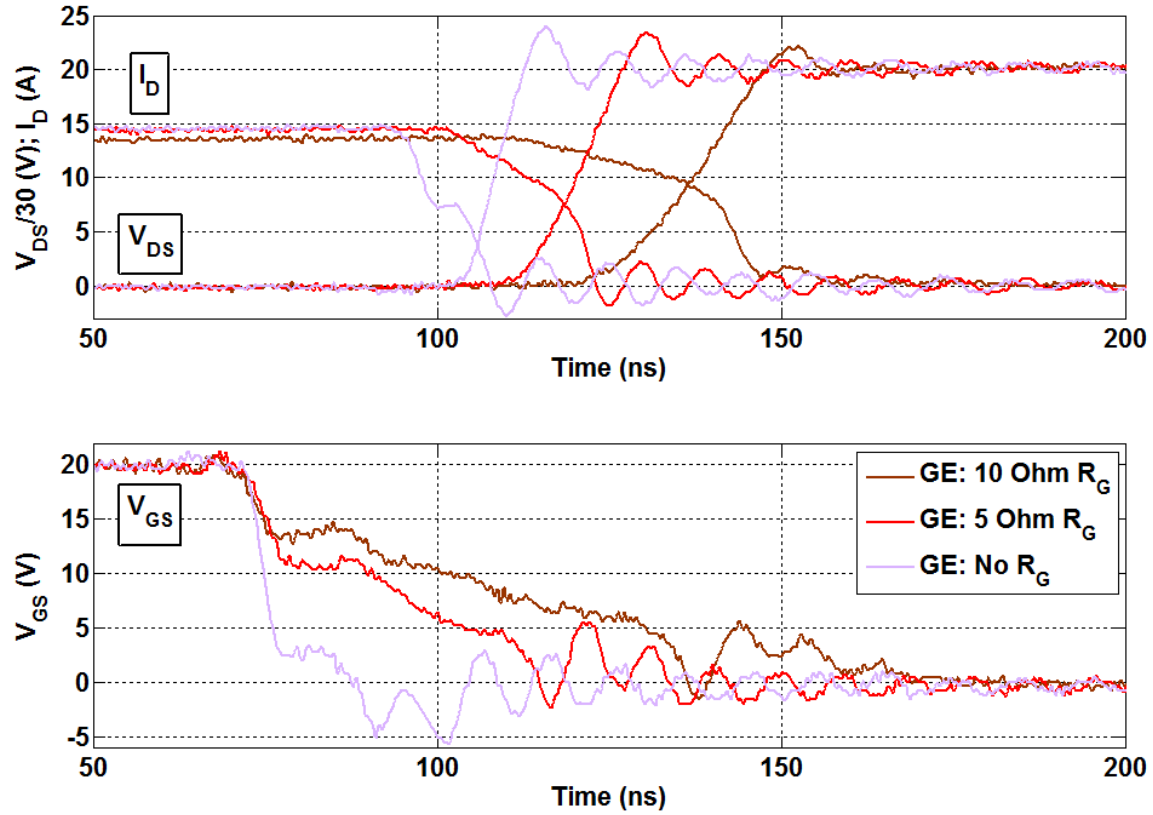


Figure 28: Turn off waveforms for the GE GE12N20L MOSFET at 600 V, 20 A, and 25 °C for external gate resistances R_G of 0 Ω (pink), 5 Ω (red), and 10 Ω (dark red).

2.4.2.4 Comparison of the SiC MOSFET Switching Behaviors

The determined optimal external gate resistance for each SiC MOSFET are listed in Table III. The internal gate resistance measured for each device is repeated in the table for reference. As can be seen, the sum of the internal and external gate resistances for the majority of the MOSFETs is about 7.4 Ω . However, due to the large internal gate resistance of the ROHM SCT2160KE MOSFET, even when no external gate resistance is used the total gate resistance is still nearly double that of the other devices. Consequently, although the ROHM SCT2160KE MOSFET proved to have low junction capacitances, the device can be expected to experience higher losses. Although the external gate

resistances of the other MOSFETs could have been increased to match that of the internal gate resistance of the ROHM SCT2160KE MOSFET, this was not done because it was desired to obtain the best possible switching performance for each device.

Table III: Internal, external, and total (sum of the internal and external) gate resistances of the SiC MOSFETs [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, “High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs,” IEEE ECCE, pp. 3235-3242, Sept. 2013].

<i>Mfg.</i>	<i>Device</i>	<i>Internal Gate Resistance</i>	<i>External Gate Resistance</i>	<i>Total Gate Resistance</i>
Cree	CMF20120D	4.98 Ω	2.5 Ω	7.48 Ω
	C2M0080120D	4.85 Ω	2.5 Ω	7.35 Ω
GE	GE12N20L	2.41 Ω	5 Ω	7.41 Ω
ROHM	SCT2080KE	7.25 Ω	0 Ω	7.25 Ω
	SCT2160KE	13.7 Ω	0 Ω	13.7 Ω

The turn on and turn off switching waveforms for all of the SiC MOSFETs under study are shown in Figure 29 and Figure 30, respectively, for tests conducted at room temperature using a 600 V dc bus voltage, 20 A load current, and the corresponding external gate resistance listed in Table III. Gate voltages of 0 V for the off-state, and 20 V for the on-state were used for the DPTs. As shown in Figure 29, for the turn on transient, Cree’s C2M0080120D MOSFET has the fastest drain current slew rate. This could be accredited to the fact that it possesses the smallest input capacitance. This MOSFET,

however, also experiences the most ringing due to a combination of a small Miller capacitance, which increases the drain-source voltage slew rate, and a low internal gate resistance. It can also be seen from the figure that the ROHM SCT2160KE MOSFET has the longest di/dt rate, which can be attributed to the combination of a larger internal gate resistance and input capacitance.

For the turn off transient (Figure 30), both of the ROHM MOSFETs experience a slow drain-source voltage slew rate. While for the ROHM SCT2160KE MOSFET this can again be a result of the larger internal gate resistance, for the SCT2080KE this could be a result of the larger Miller capacitance.

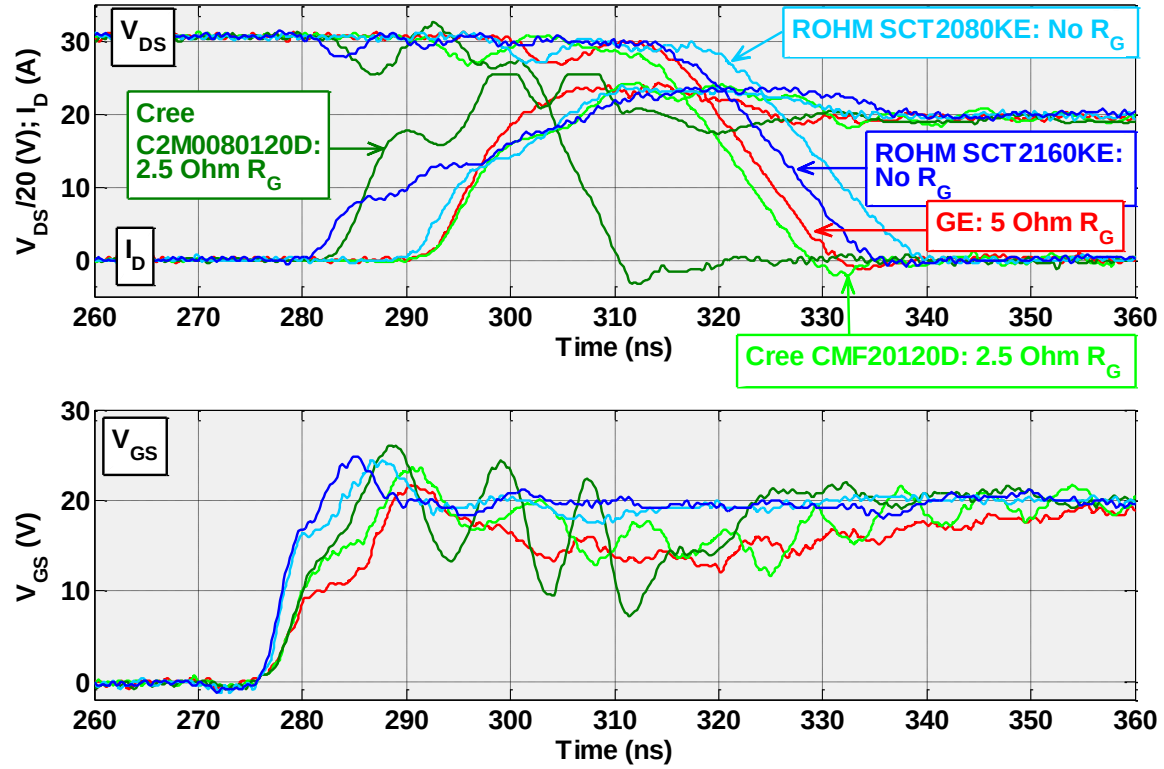


Figure 29: Turn on switching waveforms of all five SiC MOSFETs at room temperature, with a dc bus voltage of 600 V, load current of 20 A, and using the external gate resistances listed in Table III [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, “High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs,” IEEE ECCE, pp. 3235-3242, Sept. 2013].

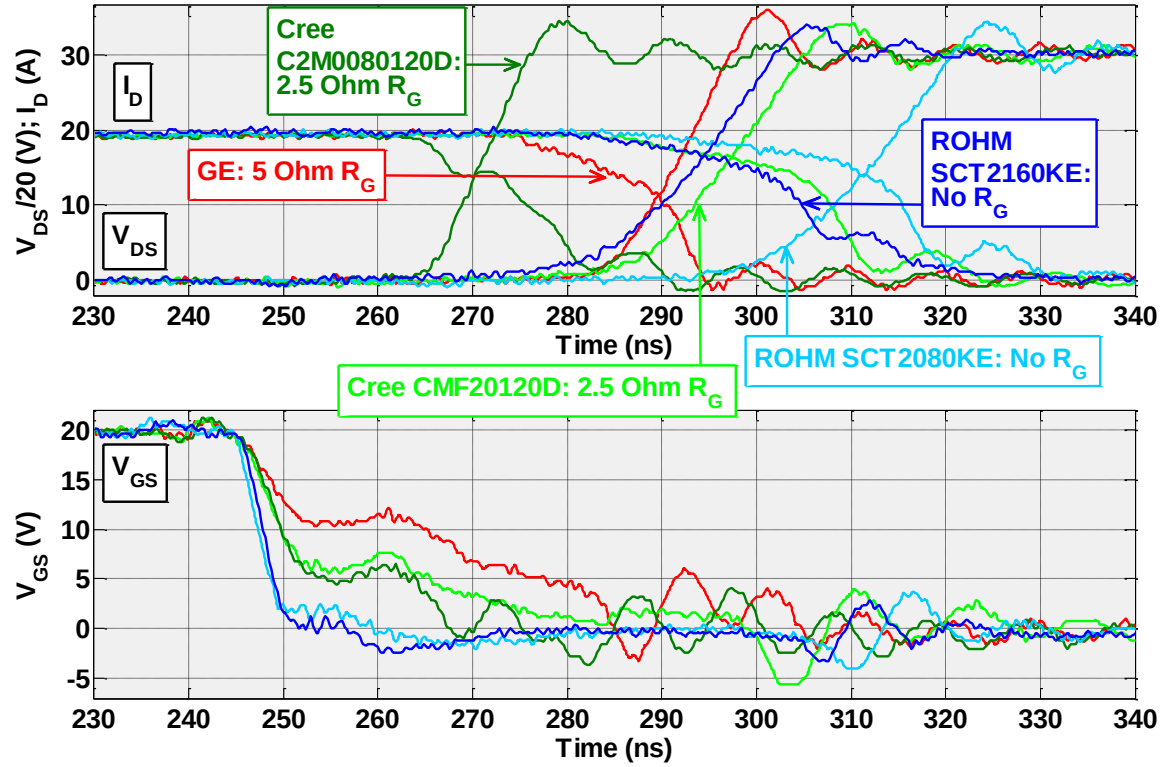


Figure 30: Turn off switching waveforms of all five SiC MOSFETs at room temperature, with a dc bus voltage of 600 V, load current of 20 A, and using the external gate resistances listed in Table III [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, “High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs,” IEEE ECCE, pp. 3235-3242, Sept. 2013].

Plots of the turn on, turn off, and total switching energies versus load current for all of the SiC MOSFETs under study are shown in Figure 31, Figure 32, and Figure 33, respectively, for tests conducted at room temperature using a 600 V dc bus voltage, and the corresponding external gate resistance listed in Table III. Gate voltages of 0 V for the off-state, and 20-V for the on state were used for the DPTs. The on-resistances of the MOSFETs are shown in parentheses in these figures as a reference. As expected, the Cree C2M0080120D MOSFET shows the lowest turn on switching energy losses. However, for the turn off process, GE’s MOSFET proves to have the smallest losses. When

summing these turn on and turn off switching energies, the total value can be found (Figure 33). The Cree C2M0080120D MOSFET shows the lowest total switching loss, while the ROHM SCT2160KE MOSFET demonstrates the largest. The higher switching loss of the ROHM SCT2160KE device can again be attributed to its higher internal gate resistance (Table III) and slower switching speeds (Figure 29 and Figure 30).

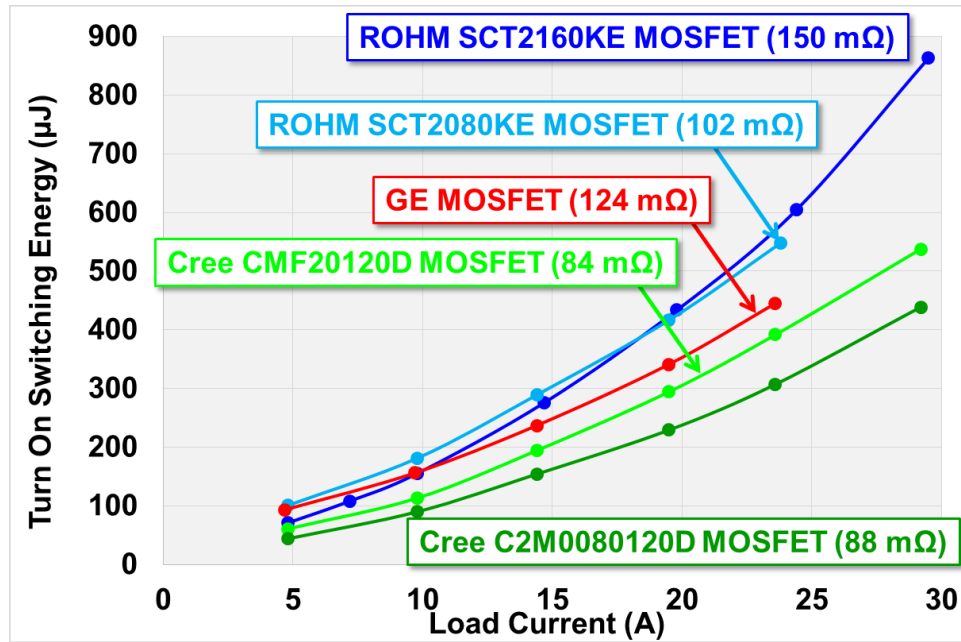


Figure 31: Turn on switching energy loss versus load current for all five SiC MOSFETs at room temperature, with a dc bus voltage of 600 V, and using the external gate resistances listed in Table III. The on-resistance of each device is shown in parentheses as a reference [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, “High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs,” IEEE ECCE, pp. 3235-3242, Sept. 2013].

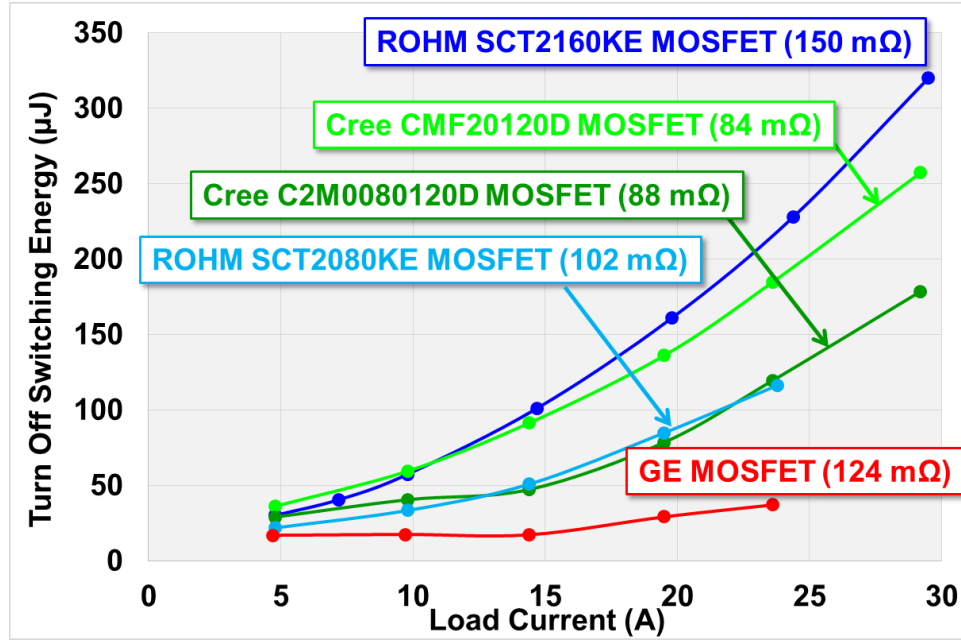


Figure 32: Turn off switching energy loss versus load current for all five SiC MOSFETs at room temperature, with a dc bus voltage of 600 V, and using the external gate resistances listed in Table III. The on-resistance of each device is shown in parentheses as a reference [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, “High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs,” IEEE ECCE, pp. 3235-3242, Sept. 2013].

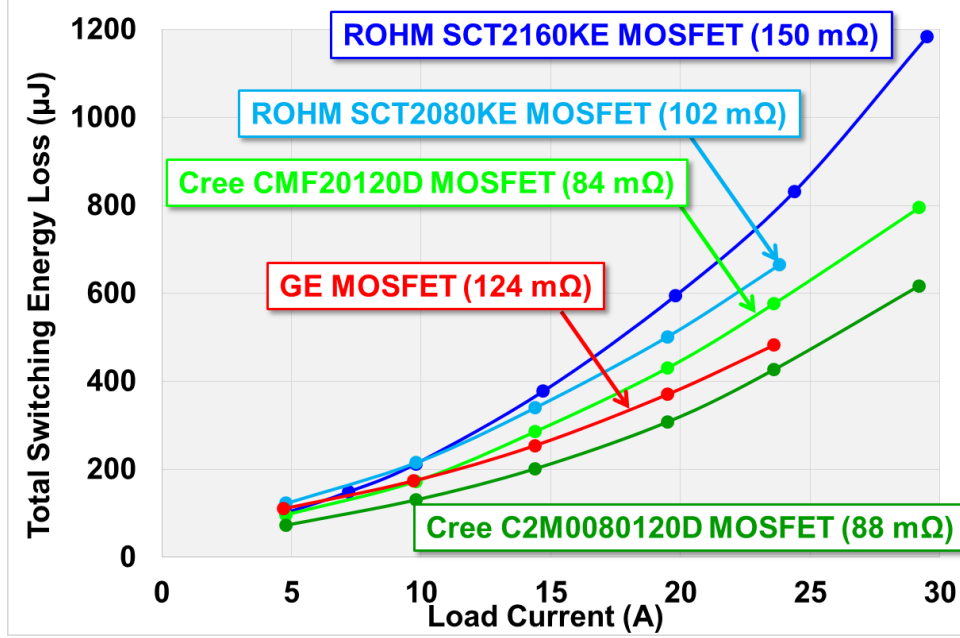


Figure 33: Total switching energy loss versus load current for all five SiC MOSFETs at room temperature, with a dc bus voltage of 600 V, and using the external gate resistances listed in Table III. The on-resistance of each device is shown in parentheses as a reference [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, “High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs,” IEEE ECCE, pp. 3235-3242, Sept. 2013].

However, the drain-source capacitance of the MOSFET discharges its stored energy through the device channel during the turn on process, and draws some current from the load during the turn off process [50]. This results in an underestimation of the turn on switching loss measurements, and an overestimation of the turn off loss measurements [50]. Though the total switching energy loss remains the same [50]. To account for this behavior, the energy stored in the capacitance was calculated, and added to the turn on switching energies, and subtracted from the turn off switching energies. The adjusted turn on and turn off switching energy loss plots are shown in Figure 34 and Figure 35, respectively. As shown by the figures, when comparing the switching losses of the MOSFETs to one another, no noticeable changes can be observed.

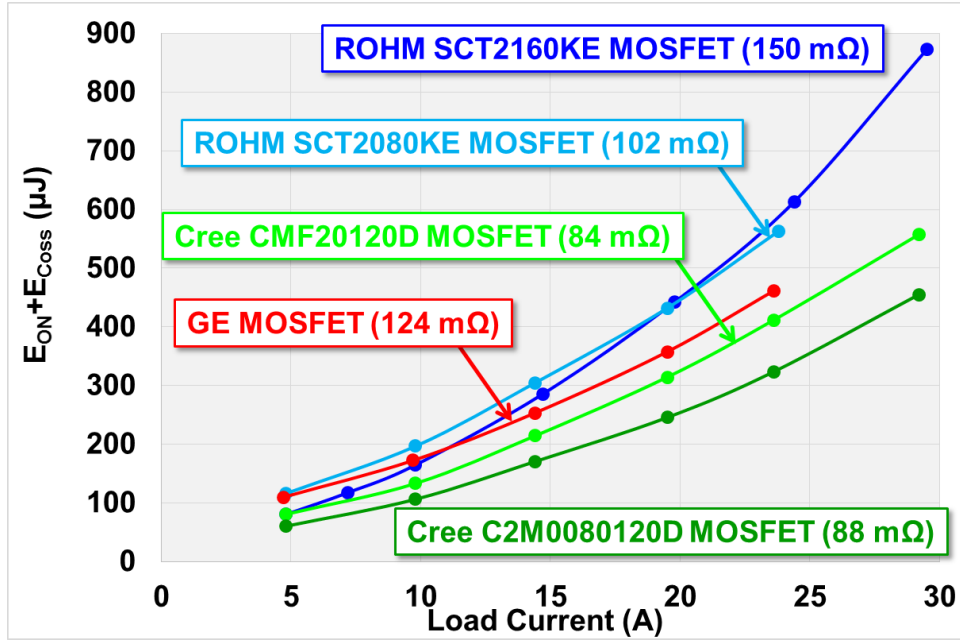


Figure 34: Turn on switching energy loss E_{ON} versus load current for the SiC MOSFETs with the energy stored in the output capacitance E_{Coss} added.

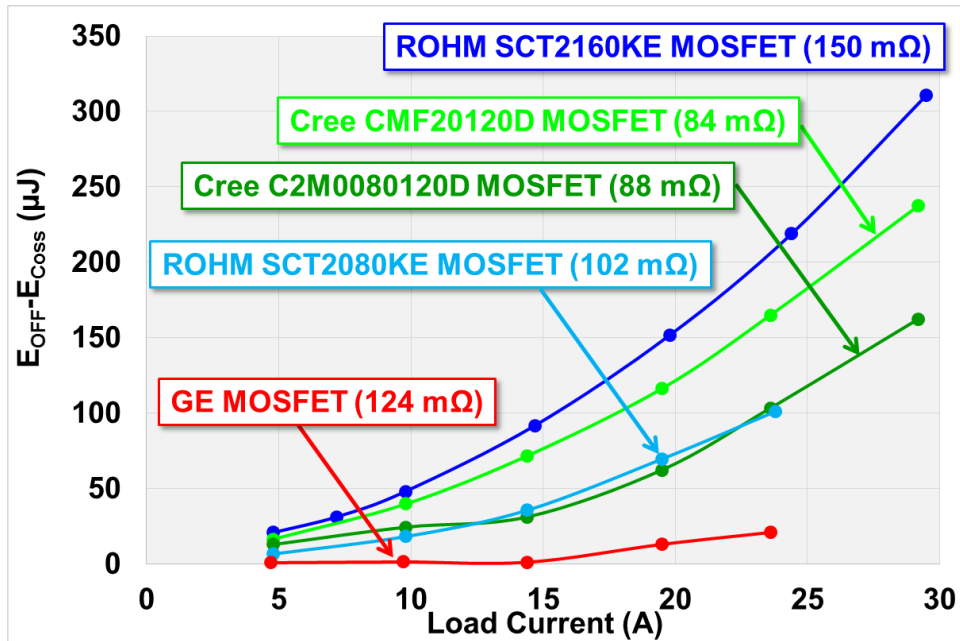


Figure 35: Turn off switching energy loss E_{OFF} versus load current for the SiC MOSFETs with the energy stored in the output capacitance E_{Coss} subtracted.

Table IV lists the turn on and turn off times, and slew rates for the SiC MOSFETs. For the turn on process, the drain current rise time t_{ir} , and slew rate di/dt were measured from 10 % to 90 % of the steady-state load current, which was 20 A in this case. The drain-source voltage fall time t_{vf} , and slew rate dv/dt were measured from 90 % to 10 % of the steady-state dc bus voltage, which was 600 V for the listed values. The turn off drain-source voltage rise t_{vr} and drain current fall t_{if} times, and corresponding slew rates were measured similarly. As shown by the table, for the current rise and fall stages, the GE and Cree C2M0080120D MOSFETs had similarly fast transition times and di/dt rates. The Cree CMF20120D and ROHM SCT2080KE devices also had comparable current rise and fall times and di/dt rates. However, Cree's C2M0080120D MOSFET proved to have the fastest voltage fall and rise times, as well as the highest dv/dt rates.

Table IV: Turn on and turn off times and slew rates for the SiC MOSFETs at room temperature, 600 V, 20 A, and the external gate resistances listed in Table III.

	<i>Turn On</i>				<i>Turn Off</i>			
<i>Device</i>	t_{ir} (ns)	di/dt (A/ns)	t_{vf} (ns)	dv/dt (V/ns)	t_{vr} (ns)	dv/dt (V/ns)	t_{if} (ns)	di/dt (A/ns)
Cree CMF20120D	11.3	1.4	13.5	35.5	15.6	30.7	21.9	0.72
Cree C2M0080120D	6.2	2.5	8.5	56.6	8.5	56.6	16.2	0.98
GE GE12N20L	6.6	2.4	12.9	37.7	11.0	43.8	16.8	0.94
ROHM SCT2080KE	12.2	1.3	15.8	30.5	18.1	26.5	20.3	0.78
ROHM SCT2160KE	21.4	0.73	15.2	31.6	18.4	26.1	26.6	0.60

2.4.3 High Temperature Switching Behavior

Figure 36 shows the high temperature DPT setup. For this testing, only the device under test was heated; the MOSFET was soldered to the underside of the DPT PCB and mounted to a hotplate. The temperature of the device was measured using a thermocouple, and a fan was used to keep the DPT PCB components at a reasonable temperature. Thermal camera images verified that the PCB components remained at temperatures below 50 °C. An overcurrent protection circuit was also utilized to protect the device from possible faults. The purpose for only heating the SiC transistor is to allow for insight into the high temperature operation of the device alone. In this way, the results

can be applied to a wide range of applications. If instead the other components were also heated, then the results would not be applicable to systems that utilize, for instance, different gate drives or FWDs, as these parts may feature unique high temperature performance characteristics.

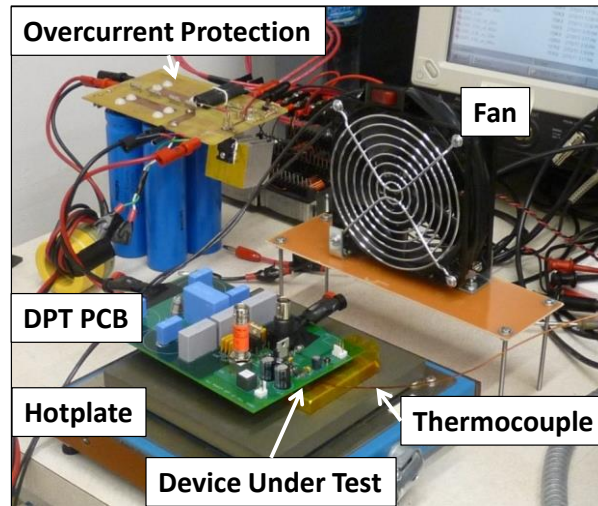


Figure 36: High temperature DPT setup with key components identified [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, “High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs,” IEEE ECCE, pp. 3235-3242, Sept. 2013], [C. DiMarino, Z. Chen, D. Boroyevich, R. Burgos, P. Mattavelli, “High-temperature characterization and comparison of 1.2 kV SiC power semiconductor devices,” *J. Microelectron. Electron. Packaging*, vol. 10, no. 4, pp. 138, 2013].

The turn on and turn off switching waveforms for the Cree CMF20120D SiC MOSFET for temperatures of 25 °C to 200 °C, and DPTs at 600 V and 20 A, using a 10 Ω external gate resistance are shown in Figure 37 and Figure 38, respectively. As shown, while the di/dt and dv/dt rates increased during turn on, they decreased during turn off. It can also be seen that the turn on delay times decreased, whereas the turn off delays increased. These phenomena are primarily due to the decrease in threshold and plateau

voltages experienced with increasing temperatures [50]. Consequently, the turn on energy loss decreased with temperature, while the turn off energy loss increased, as shown in Figure 39. This trend was verified by the device datasheet [45], as well as [50]. The DPTs for the ROHM and GE MOSFETs showed similar waveforms and trends. The results of these high temperature DPTs are summarized in Table V.

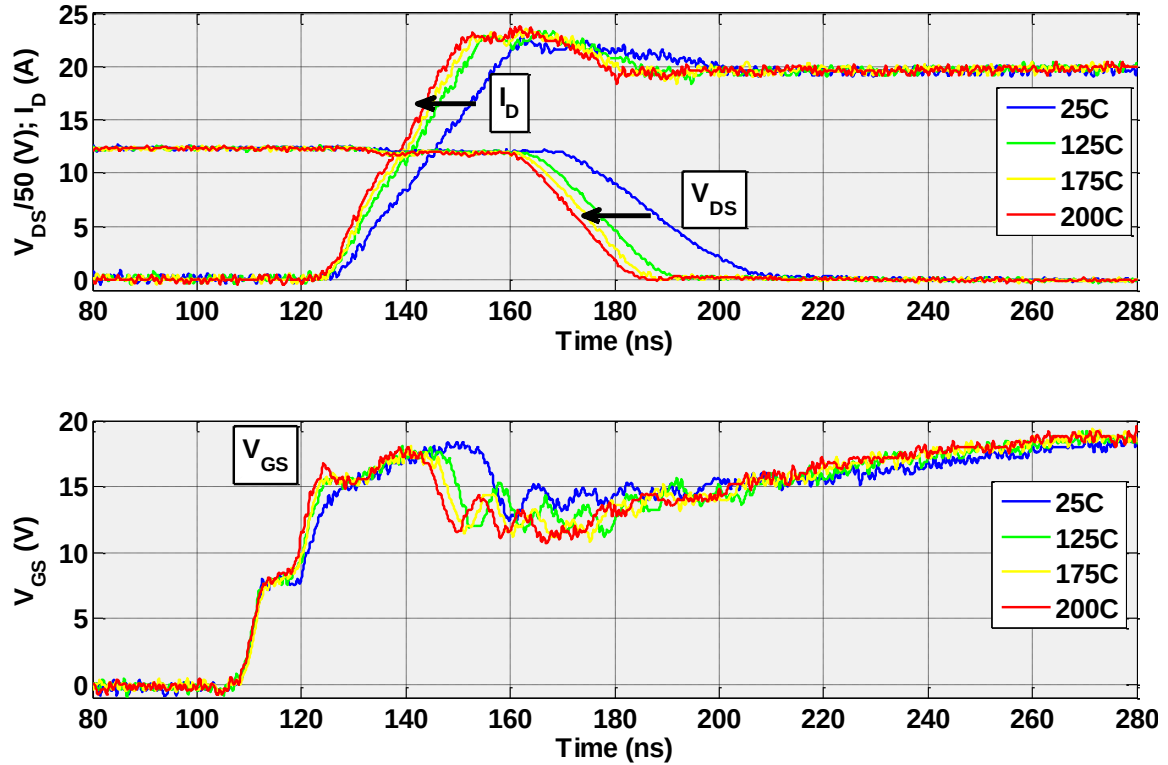


Figure 37: Turn on switching waveforms for Cree's CMF20120D SiC MOSFET with a dc bus voltage of 600 V, a load current of 20 A, and using an external gate resistance of 10 Ω for 25 $^{\circ}\text{C}$ (blue) to 200 $^{\circ}\text{C}$ (red) [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, "High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs," IEEE ECCE, pp. 3235-3242, Sept. 2013], [C. DiMarino, Z. Chen, D. Boroyevich, R. Burgos, P. Mattavelli, "High-temperature characterization and comparison of 1.2 kV SiC power semiconductor devices," *J. Microelectron. Electron. Packaging*, vol. 10, no. 4, pp. 138, 2013].

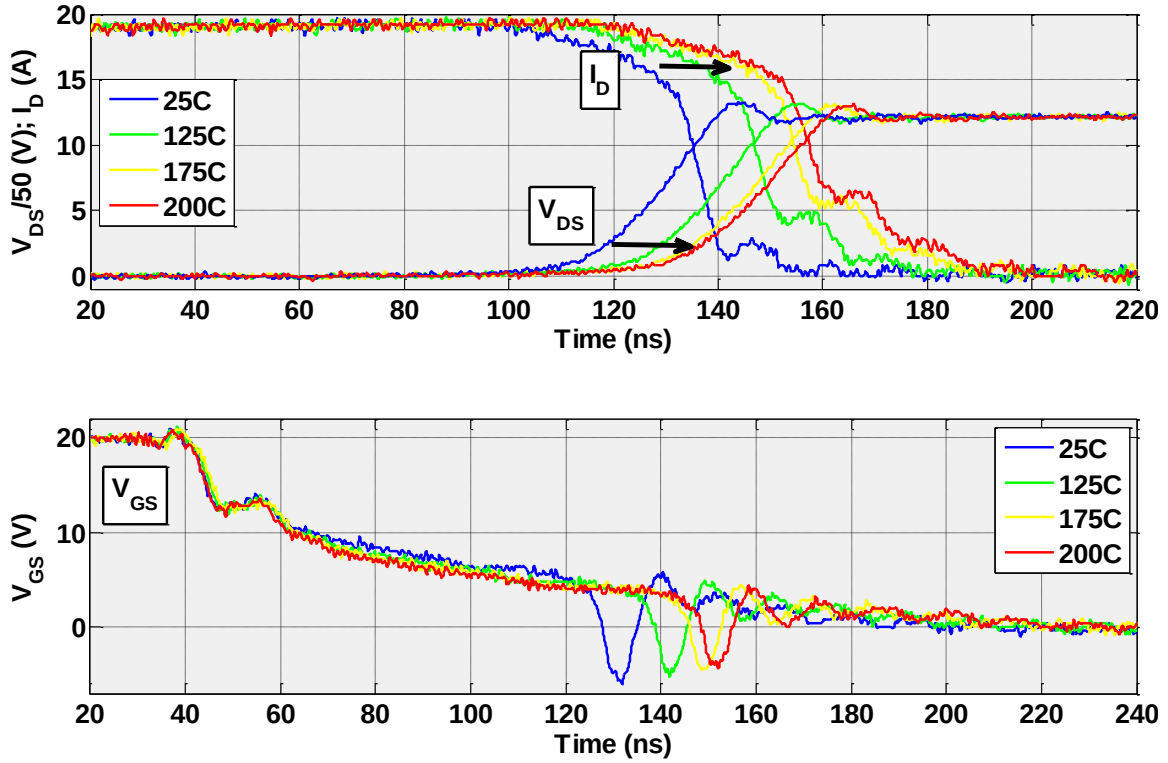


Figure 38: Turn off switching waveforms for Cree's CMF20120D SiC MOSFET with a dc bus voltage of 600 V, a load current of 20 A, and using an external gate resistance of 10 Ω for 25 °C (blue) to 200 °C (red) [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, "High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs," IEEE ECCE, pp. 3235-3242, Sept. 2013], [C. DiMarino, Z. Chen, D. Boroyevich, R. Burgos, P. Mattavelli, "High-temperature characterization and comparison of 1.2 kV SiC power semiconductor devices," *J. Microelectron. Electron. Packaging*, vol. 10, no. 4, pp. 138, 2013].

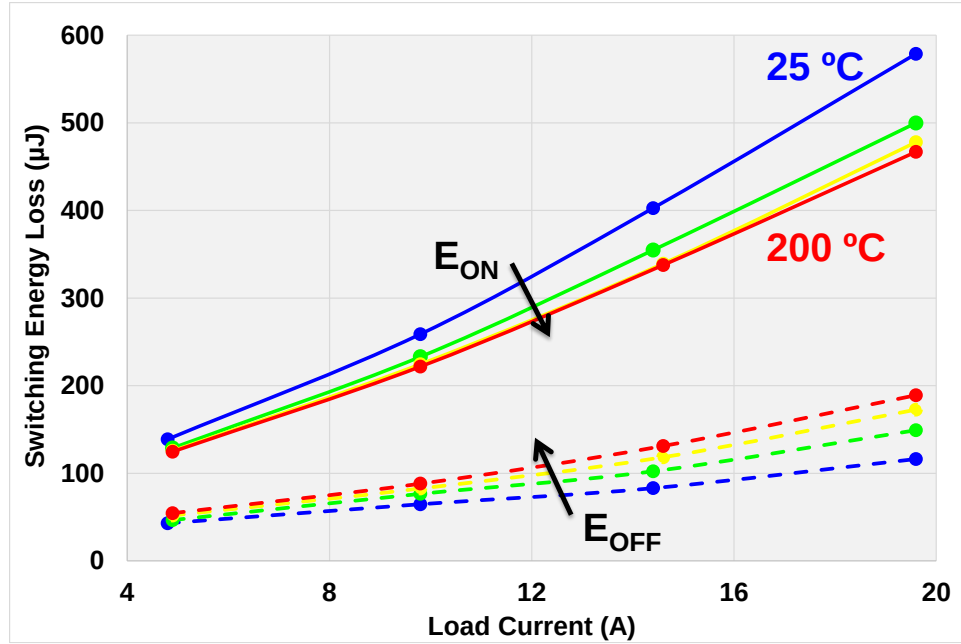


Figure 39: Turn on (solid line) and turn off (dashed line) switching energy loss versus load current for Cree's CMF20120D SiC MOSFET with a dc bus voltage of 600 V, and using an external gate resistance of 10 Ω for $^{\circ}\text{C}$ (blue) to 200 $^{\circ}\text{C}$ (red) [C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, P. Mattavelli, "High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs," IEEE ECCE, pp. 3235-3242, Sept. 2013], [C. DiMarino, Z. Chen, D. Boroyevich, R. Burgos, P. Mattavelli, "High-temperature characterization and comparison of 1.2 kV SiC power semiconductor devices," *J. Microelectron. Electron. Packaging*, vol. 10, no. 4, pp. 138, 2013].

Table V: Change in the turn on ΔE_{ON} , turn off ΔE_{OFF} , and total ΔE_{TOT} switching energies of the SiC MOSFETs for temperatures from 25 °C to 200 °C, 600 V, 20 A, and 10 Ω external gate resistance.

<i>Device</i>	ΔE_{ON}	ΔE_{OFF}	ΔE_{TOT}
Cree CMF2012D	↓	↑	↓ 6 %
GE GE12N20L	↓	↑	constant
ROHM SCT2080KE	↓	↑	↓ 8 %

2.5 Modeling of 1.2 kV SiC MOSFETs

This section will begin with a discussion on the distinctive features of the SiC MOSFET that were not observed in their typical Si counterparts. A survey of the various types of models will then be presented, which will include the advantages and disadvantages of each. Finally, a new analytical model will be proposed for the 1.2 kV SiC MOSFETs.

2.5.1 Unique Characteristics of 1.2 kV SiC MOSFETs

In carrying out the characterization of these five different 1.2 kV SiC MOSFETs, behaviors not experienced in conventional Si MOSFETs were revealed. These unique characteristics include an extended transition region between the linear and saturation regimes of the output characteristic curves, a non-flat Miller Plateau, and a decrease in channel resistance with increased temperature. This stretched transition region of the SiC MOSFET was seen in Figure 7. Figure 40 shows a comparison of the gate charge curves

of the Cree CMF20120D SiC MOSFET and a 1000 V, 10 A Si MOSFET (IXFH10N100), where the data was extracted from the device datasheets [45], [52]. As shown by the figure, while the IXFH10N100 Si MOSFET has a flat plateau voltage, the SiC MOSFET does not. In other words, the gate-source voltage of the SiC MOSFET changes during the drain-source voltage fall and rise transitions instead of remaining constant.

The on-resistance of a MOSFET can be approximated as the sum of the drift and channel resistances. While, as expected, the drift region resistance features a positive temperature coefficient, the channel resistance decreases with increased temperature. This decrease in the channel resistance with increased temperature causes the on-resistance of SiC MOSFETs to have a negative temperature coefficient at low gate-source voltages since the channel resistance is dominant when the device channel is in weak inversion. This phenomenon was clearly shown in [43]. These unique features of the SiC MOSFET can be attributed to the modest transconductance [44], short-channel effects, and traps at the SiC/SiO₂ interface [43], [44], [53].

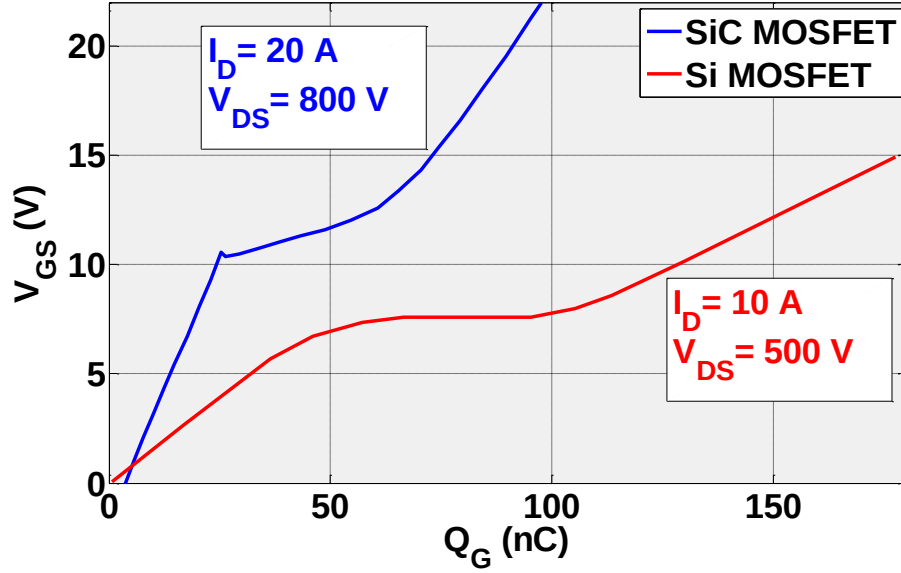


Figure 40: Gate charge curves for Cree's CMF20120D SiC MOSFET (blue) and IXYS's IXFH10N100 Si MOSFET (red). This data was extracted from their respective datasheets [45], [52].

2.5.2 Survey of Models

Due to these unorthodoxies, models developed for Si MOSFETs are not well-suited for SiC. Consequently, significant effort has been made to adjust these models to accommodate the abnormalities seen by SiC MOSFETs. The types of models can be grouped into two major categories: (1) physics-based, and (2) analytical. The physics-based models utilize physical parameters and equations to predict the device behavior. Unfortunately, although this type of model is highly accurate, much of the required information, such as doping concentration and channel length and width [53], is often unknown to users, and thus these models cannot be properly utilized.

The analytical models, on the other hand, rely on electrical characteristics and extraction techniques to determine and/or find other ways to express these physical parameters. Regrettably, the number of parameters that need to be extracted for this type of model can be extensive. For instance, [43] proposed a model that requires parameters

to be extracted from common curves found in the datasheet. However, more than twenty parameters needed to be extracted. This extraction involved finding the slopes of numerous curves, and then substituting these values into various different equations.

Alternatively, [44] presents a model and parameter extraction sequence for SiC MOSFETs, which utilizes software packages (IMPACT and SATSMR) to find the necessary parameters. However, some of these parameters require extraction from saturation current versus gate-source voltage, and on-state voltage versus gate-source voltage curves, which are not normally found in the datasheets of SiC MOSFETs. It should also be noted that this model requires knowledge of the device active area and drift region width, which is typically unknown to consumers. In [54], a tool was proposed for easy extraction of these static, thermal, and dynamic parameters without the need of active area or drift region width. Nevertheless, the extraction procedure is still more time-consuming, and requires a more adequate knowledge of device characteristics, than what is preferred by most users.

Instead, it is desirable to have a fast and simple modeling process that can allow for direct evaluation and comparison of the dynamic performance of SiC MOSFETs for use in preliminary designs. For Si power MOSFETs, [55]-[57] provide simple equations that could be used to determine the turn on and turn off durations by calculating the turn on delay, current rise, and voltage fall times, and the turn off delay, voltage rise, and current fall times, respectively. The aim of these models is to allow designers to choose suitable devices for their applications using minimal information found in the device datasheets. These models utilize the MOSFET equivalent circuit and switching waveforms to derive simple equations that can be used to calculate the transition times

mentioned. This model therefore utilizes a minimum number of parameters, all of which can be taken directly from the datasheet, and a few equations that provide the switching times in order to determine the dynamic performance of the device. A similar model was shown in [50] and [58], which discussed its application for SiC MOSFETs. However, it will be shown in this work that this model is not appropriate for SiC MOSFETs. There are two primary reasons for this: (1) the model requires ambiguous determination of the transconductance parameter, and (2) even if the proper transconductance values could be found, poor matching with experimental results was observed for some of the transition times.

Moreover, some manufacturers, such as Cree, ROHM, GeneSiC, and Infineon, provide SPICE models for their devices on their websites [59]-[62]. However, these models are often not able to keep up with the release of new generation devices. For instance, although Cree is now planning to release a third generation SiC MOSFET, the SPICE models available on the company's website [59] are currently for their first generation CMF10120D and CMF20120D devices only. Figure 41 shows a comparison of the measured, datasheet [45], and SPICE model I-V curves for Cree's CMF20120D. While this particular model shows adequate matching in the output characteristics, the complexity and accuracy of these models will vary based on the manufacturer. Consequently, experimental results need to be conducted to verify the precision of the model. As such, these models are generally more useful later in the converter design stage when one or a select few devices have been chosen for further evaluation. As the goal of this thesis is to provide a method for preliminary device assessment, in other

words prior to acquiring these transistors and measuring their characteristics, a general model that can be applied to all of these SiC MOSFETs is desired.

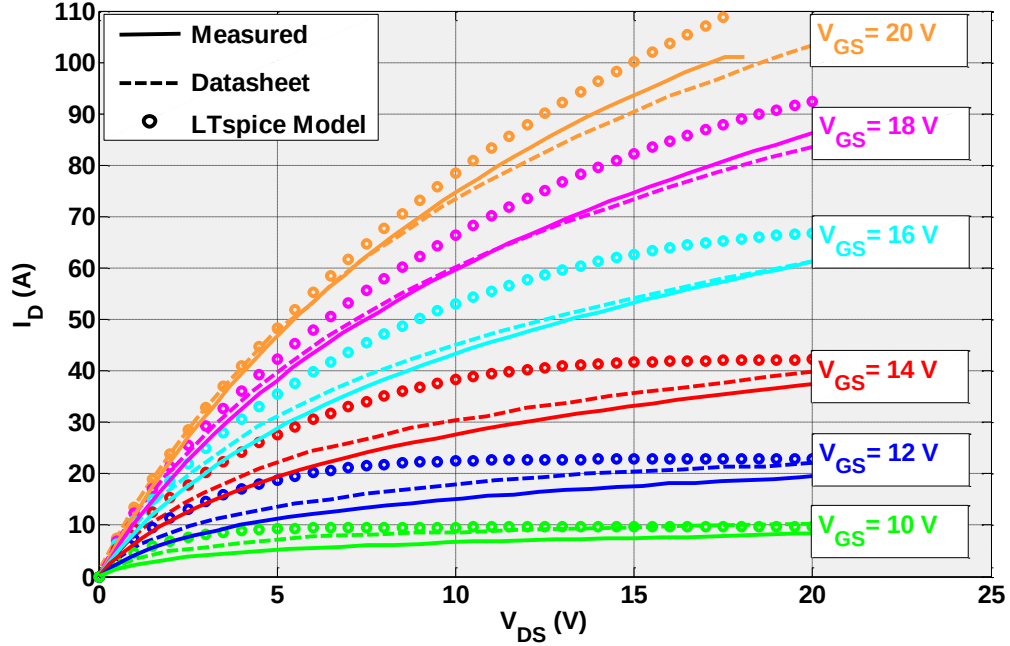


Figure 41: Comparison of the measured, datasheet [45], and SPICE model I-V curves.

2.5.3 Evaluation of Previous Analytical Model

In this section, the equations presented in [50] and [58] will be evaluated. This is achieved by utilizing the device parameters provided in the datasheets to calculate the current rise t_{ir} and voltage fall t_{vf} times during the turn on transition, and the voltage rise t_{vr} and current fall t_{if} times for the turn off transition. These calculated switching times can then be compared to the measured values for the five different 1.2 kV SiC MOSFETs that have been characterized in this work. From [50] and [58], the ideal turn on and turn off waveforms for a typical Si power MOSFET (Figure 42 and Figure 43, respectively), along with the MOSFET equivalent circuit, are used to derive the following transition time equations.

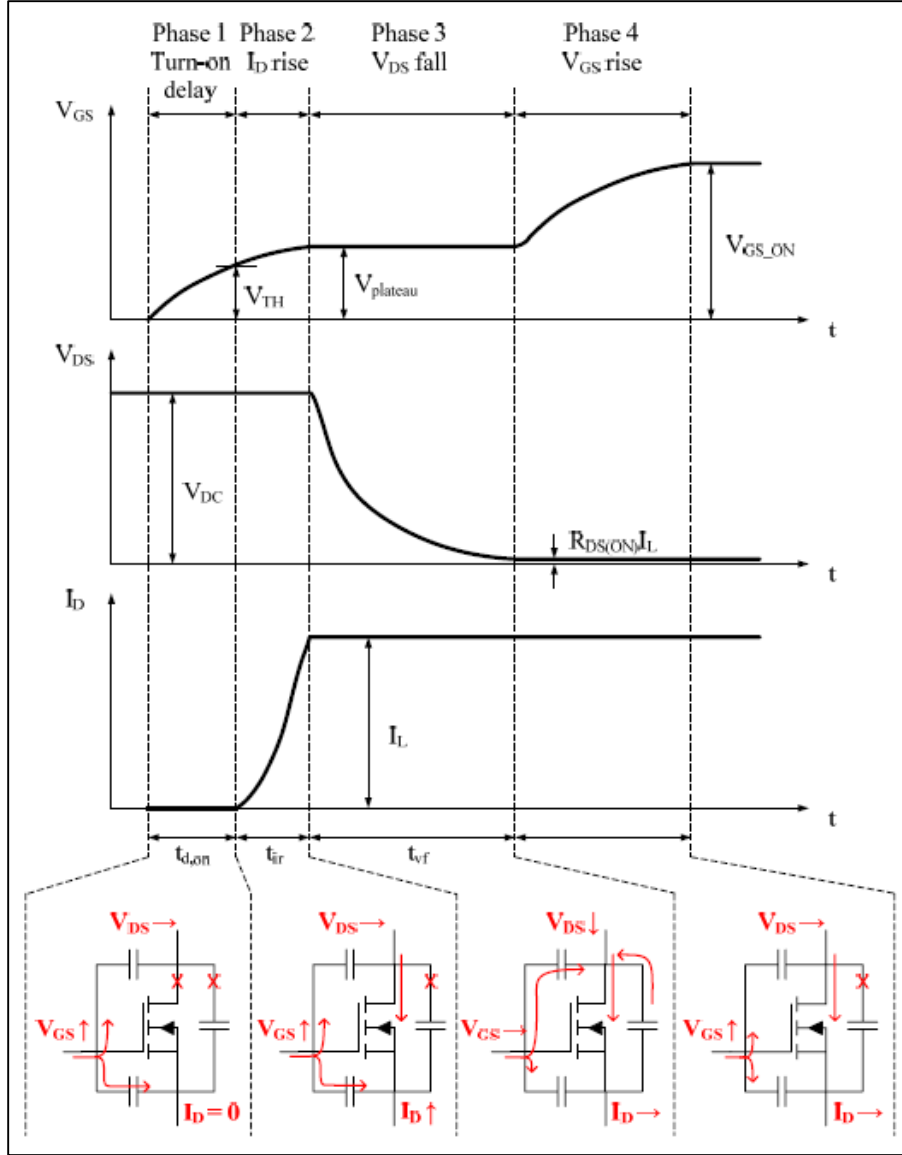


Figure 42: Ideal Si MOSFET turn on process. Image from [Z. Chen, “Characterization and modeling of high-switching-speed behavior of SiC active devices,” M.S. thesis, Dept. Elect. Comput. Eng., Virginia Tech, Blacksburg, VA, 2009], with permission from Zheng Chen.

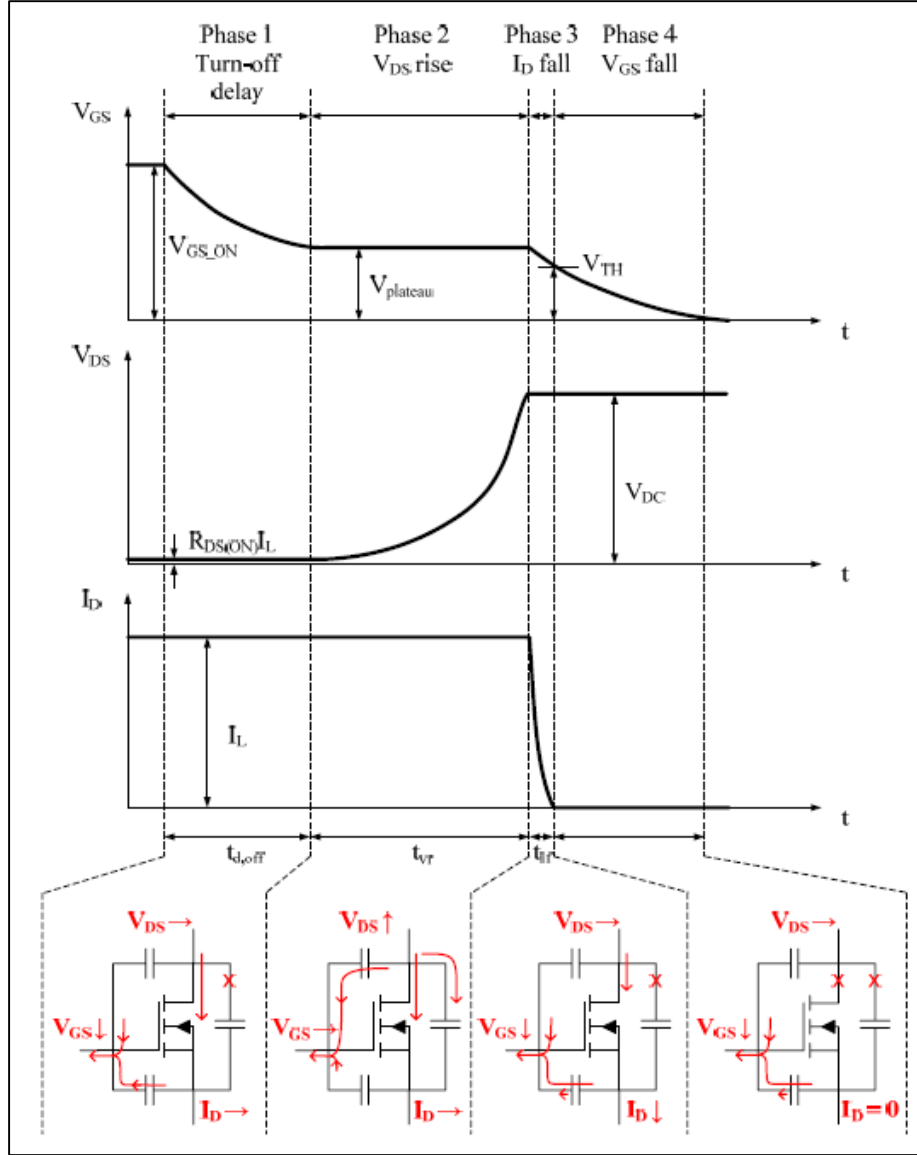


Figure 43: Ideal Si MOSFET turn off process. Image from [Z. Chen, “Characterization and modeling of high-switching-speed behavior of SiC active devices,” M.S. thesis, Dept. Elect. Comput. Eng., Virginia Tech, Blacksburg, VA, 2009], with permission from Zheng Chen.

From [50] and [58], the current rise and voltage fall times during the turn on process are given by

$$t_{ir} = R_G C_{ISS} \ln \left(\frac{V_{Drive} - V_{GS(th)}}{V_{Drive} - V_{Plateau,tir}} \right); \text{ where } V_{Plateau,tir} = \frac{I_{Load}}{g_{fs}} + V_{GS(th)} \quad (3)$$

$$t_{vf} = \frac{Q_{GD} R_G}{V_{Drive} - V_{Plateau,tvf}}; \text{ where } V_{Plateau,tvf} = \frac{I_{Load}}{g_{fs}} \quad (4)$$

For the turn off process, [50] and [58] gives the voltage rise and current fall times to be

$$t_{vr} = \frac{Q_{GD} R_G}{V_{Plateau,tvr}}; \text{ where } V_{Plateau,tvr} = \frac{I_{Load}}{g_{fs}} \quad (5)$$

$$t_{if} = R_G C_{ISS} \ln \left(\frac{V_{Plateau,tif}}{V_{GS(th)}} \right); \text{ where } V_{Plateau,tif} = \frac{I_{Load}}{g_{fs}} + V_{GS(th)} \quad (6)$$

where

R_G = total gate resistance

C_{ISS} = input capacitance

V_{Drive} = on-state gate driving voltage

$V_{GS(th)}$ = device threshold voltage

$V_{Plateau}$ = plateau voltage

I_{Load} = load current

g_{fs} = device transconductance

Q_{GD} = gate-drain charge

The total gate resistance is taken to be the sum of the internal and external gate resistances, where the internal gate resistance of the device is provided by the datasheet. The input capacitance is taken at high drain-source bias, as it can be seen from the switching waveforms in Figure 42 and Figure 43 that during the current transitions the drain-source voltage of the device is equal to the applied dc bias. As shown by the above equations, the plateau voltages are represented by linear expressions related to the device transconductance and threshold voltage (for the current transition phases), and the load current. [50] states that the gate-drain charge was used due to the strong non-linearity of the Miller capacitance as a function of the drain-source voltage, which is changing during

the voltage fall and voltage rise stages. However, the gate-drain charge also changes with drain-source bias, where a larger charge is associated with a higher voltage.

To evaluate these equations, the current rise, voltage fall, voltage rise, and current fall times were calculated for each of the five SiC MOSFETs in this study for various load currents and external gate resistance values. The standard definition for the current rise time is the time it takes for the drain current of the device to rise from 10 % to 90 % of the steady-state load current. It is common practice to measure the voltage fall time from the time at which the drain-source voltage falls from 90 % to 10 % of the steady-state dc voltage. Similar definitions are used for the voltage rise and current fall time measurements.

Figure 44 - Figure 51 show the measured and calculated current rise, voltage fall, voltage rise, and current fall times versus load current for various external gate resistance values and a dc bus voltage of 600 V for the Cree CMF20120D and ROHM SCT2080KE SiC MOSFETs. The values used for the model parameters were taken from the device datasheets [45], [48], and are listed in Table VI. Note that the gate-drain charge is adjusted to correspond to a drain-source voltage of 600 V. It should also be noted that this model was applied to all of the SiC MOSFETs presented in this work, but for brevity the comparison between the measured and model data is only shown for two of the five MOSFETs.

As can be seen by the figures, the model does not match well with the measured switching times. This is partly due to the transconductance value used in the plateau voltage calculation. The value provided by the datasheets is typically given at the continuous current rating of the device. However, this value is not appropriate for all of

the transition times. For instance, when the current is rising, a smaller transconductance, which corresponds to a lower current level, should be utilized. During the voltage fall transition, however, the current has risen to the load current, and thus the current gain specified in the datasheet is appropriate. By adjusting these transconductance values, the model can be semi-curve fitted to better match with the measured results. Two examples are shown for Cree's CMF20120D MOSFET in Figure 52 and Figure 53 for the current rise and fall times using a transconductance of 2.5 S and 1 S, respectively, instead of the 7.9 S specified in the datasheet [45]. Although the current rise time calculations with this transconductance match fairly well with the measured data, the calculated current fall times do not. In fact, the model suggests that the current fall time should increase with increasing load current, whereas the measured data shows the opposite trend. It was shown in [63] that an increase in the load current will result in a decrease in the current fall time, which is in agreement with the measured data. Consequently, even if these optimized transconductance values could be determined, the equations still do not provide good matching with the measured switching times. Accordingly, revisions of this model are necessary, and will be proposed in the subsequent section.

Table VI: Parameters from the device datasheets [45], [48] that were used to evaluate the switching time equations (3)-(6).

<i>Parameter</i>	<i>Cree CMF20120D</i>	<i>ROHM SCT2080KE</i>
$R_{G,int}$	5 Ω	6.3 Ω
C_{ISS}	1.8 nF	2.08 nF
V_{Drive}	20 V	20 V
$V_{GS(th)}$	2.65 V	2 V
g_{fs}	7.9 S	3.7 S
Q_{GD}	34 nC*	40 nC*

*Adjusted for $V_{ds} = 600$ V.

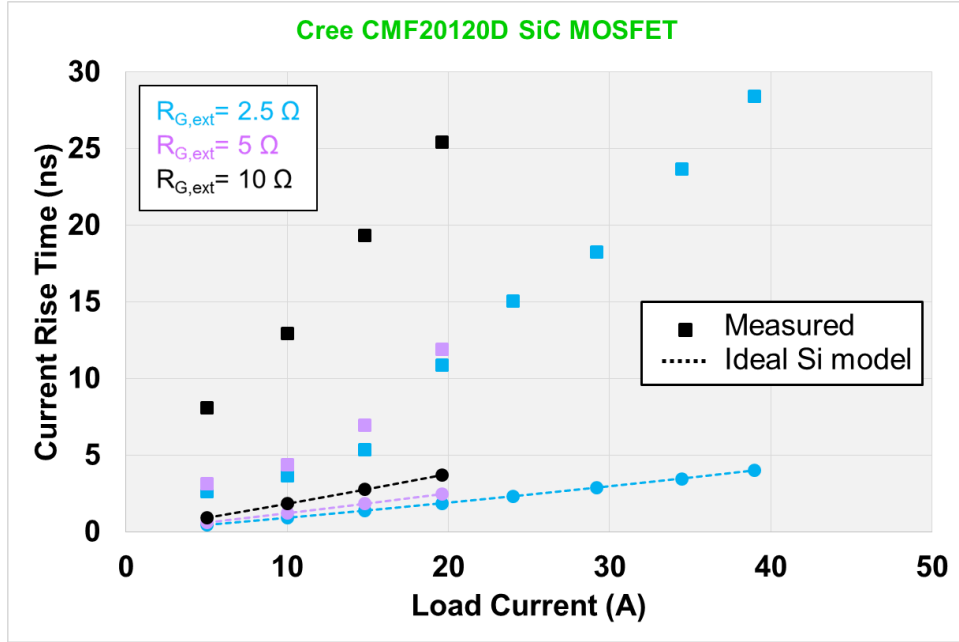


Figure 44: Comparison of the measured (squares) and calculated (dotted curves) current rise times of the Cree CMF20120D SiC MOSFET versus load current for external gate resistances of 2.5 Ω (blue), 5 Ω (purple), and 10 Ω (black).

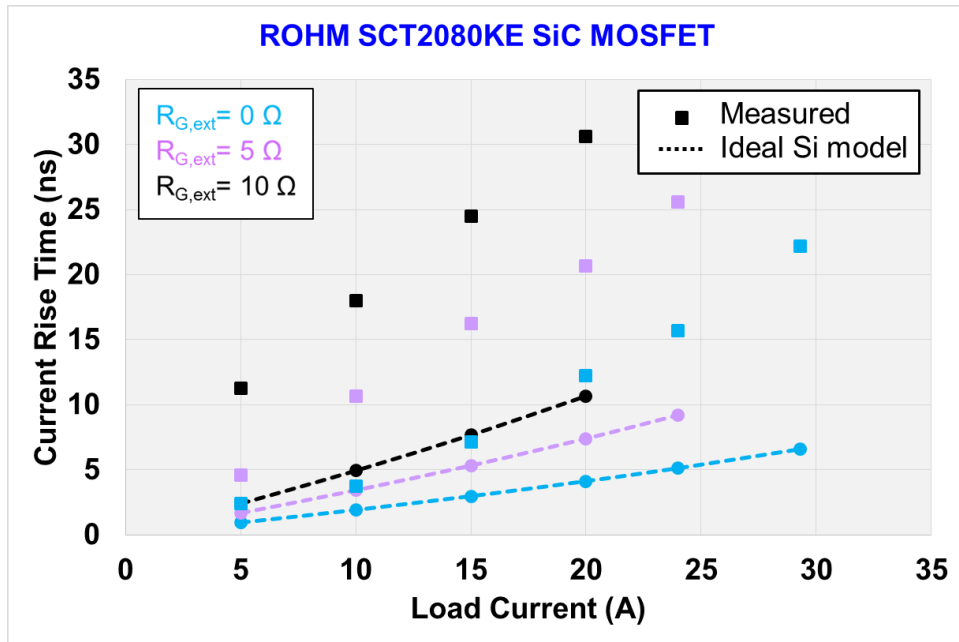


Figure 45: Comparison of the measured (squares) and calculated (dotted curves) current rise times of the ROHM SCT2080KE SiC MOSFET versus load current for external gate resistances of 0 Ω (blue), 5 Ω (purple), and 10 Ω (black).

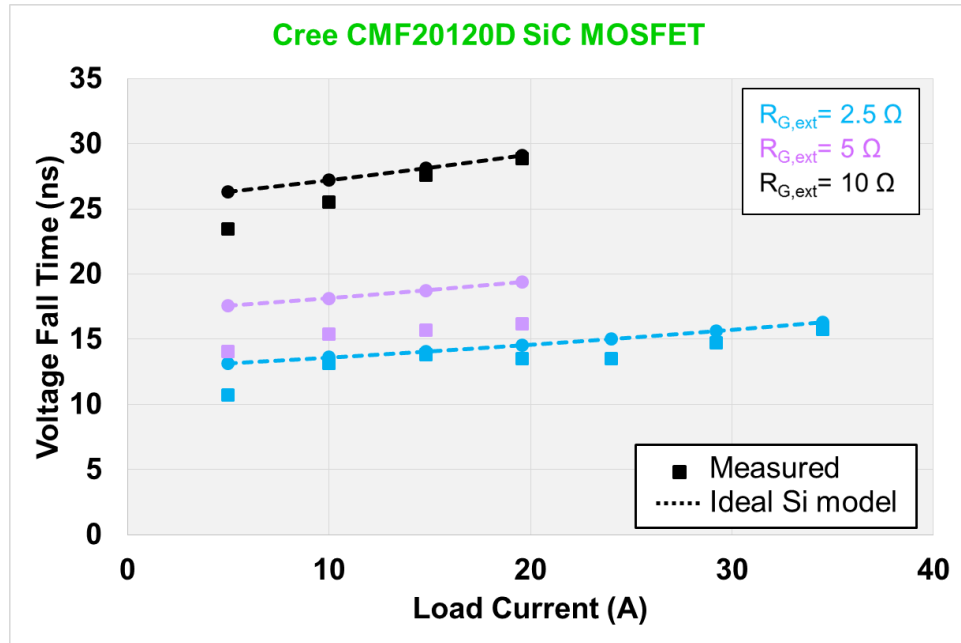


Figure 46: Comparison of the measured (squares) and calculated (dotted curves) voltage fall times of the Cree CMF20120D SiC MOSFET versus load current for external gate resistances of 2.5Ω (blue), 5Ω (purple), and 10Ω (black).

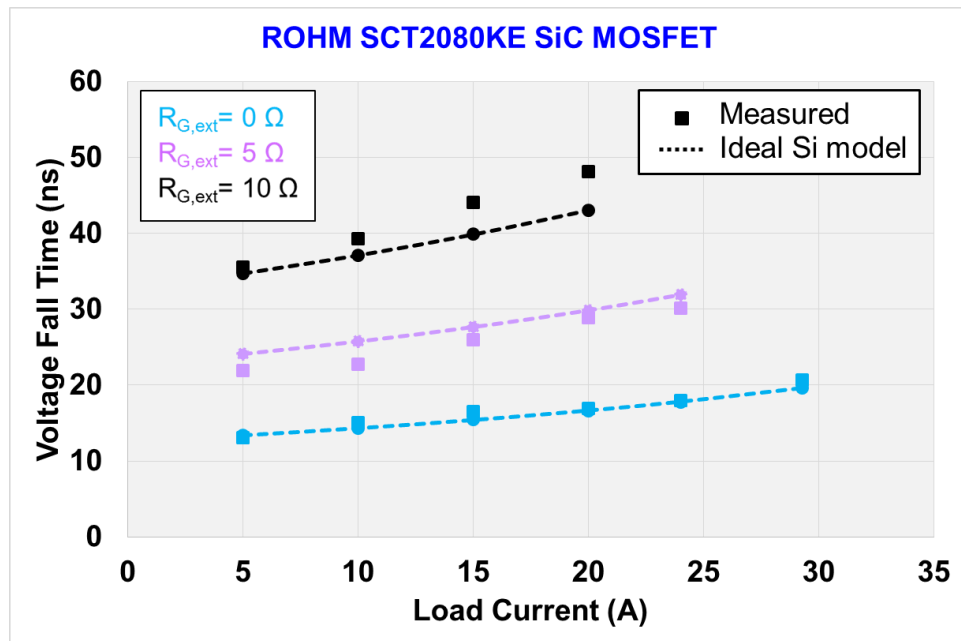


Figure 47: Comparison of the measured (squares) and calculated (dotted curves) voltage fall times of the ROHM SCT2080KE SiC MOSFET versus load current for external gate resistances of 0Ω (blue), 5Ω (purple), and 10Ω (black).

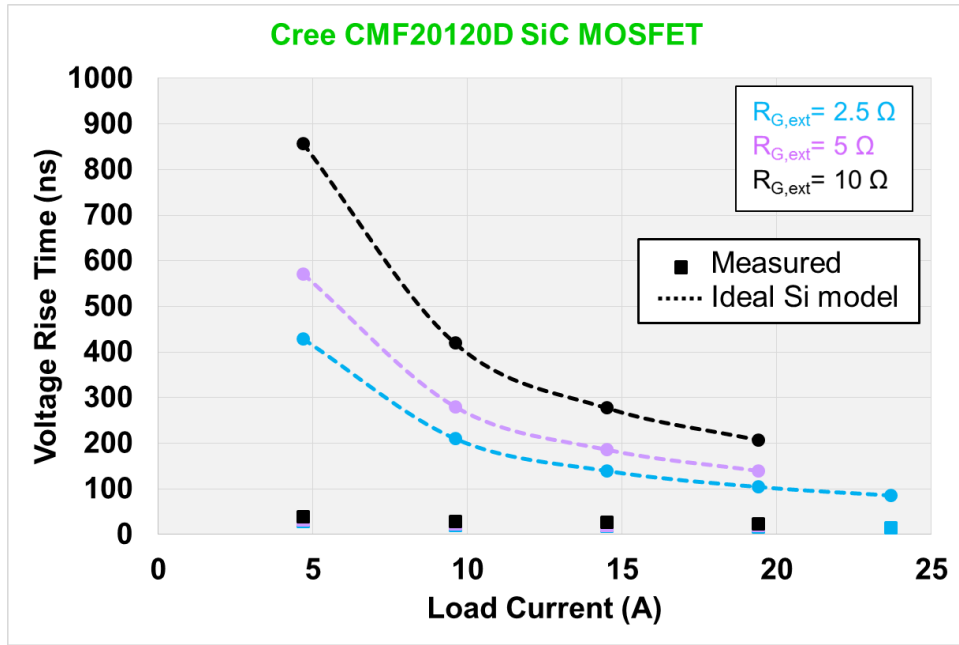


Figure 48: Comparison of the measured (squares) and calculated (dotted curves) voltage rise times of the Cree CMF20120D SiC MOSFET versus load current for external gate resistances of 2.5 Ω (blue), 5 Ω (purple), and 10 Ω (black).

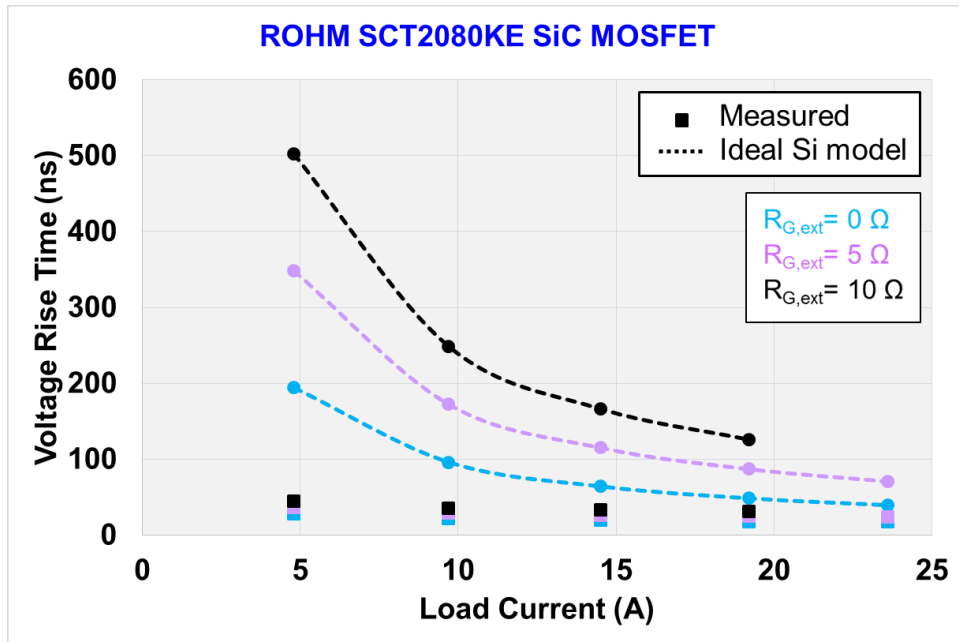


Figure 49: Comparison of the measured (squares) and calculated (dotted curves) voltage rise times of the ROHM SCT2080KE SiC MOSFET versus load current for external gate resistances of 0 Ω (blue), 5 Ω (purple), and 10 Ω (black).

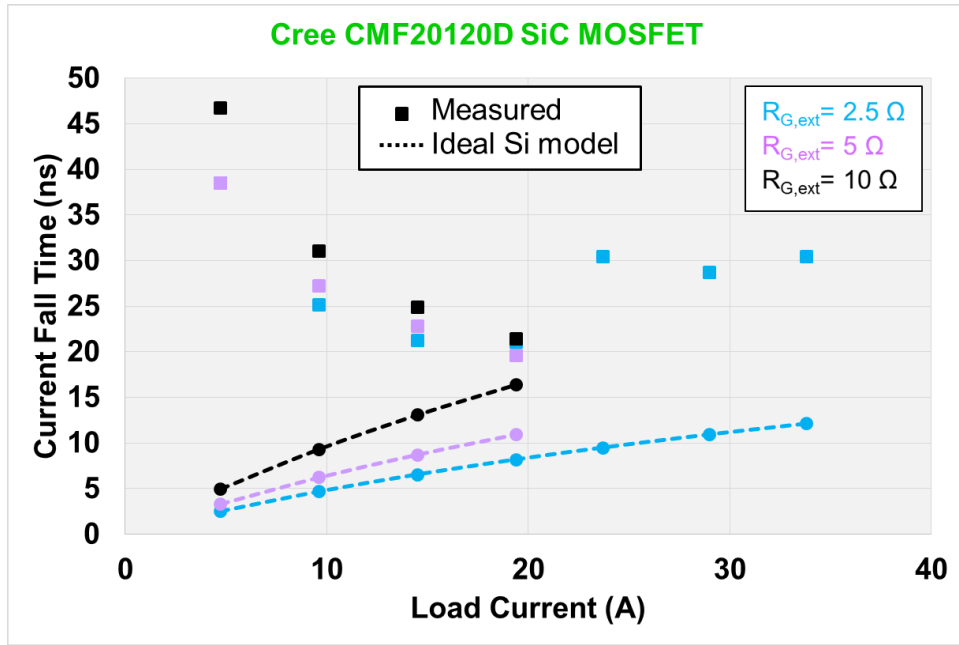


Figure 50: Comparison of the measured (squares) and calculated (dotted curves) current fall times of the Cree CMF20120D SiC MOSFET versus load current for external gate resistances of 2.5Ω (blue), 5Ω (purple), and 10Ω (black).

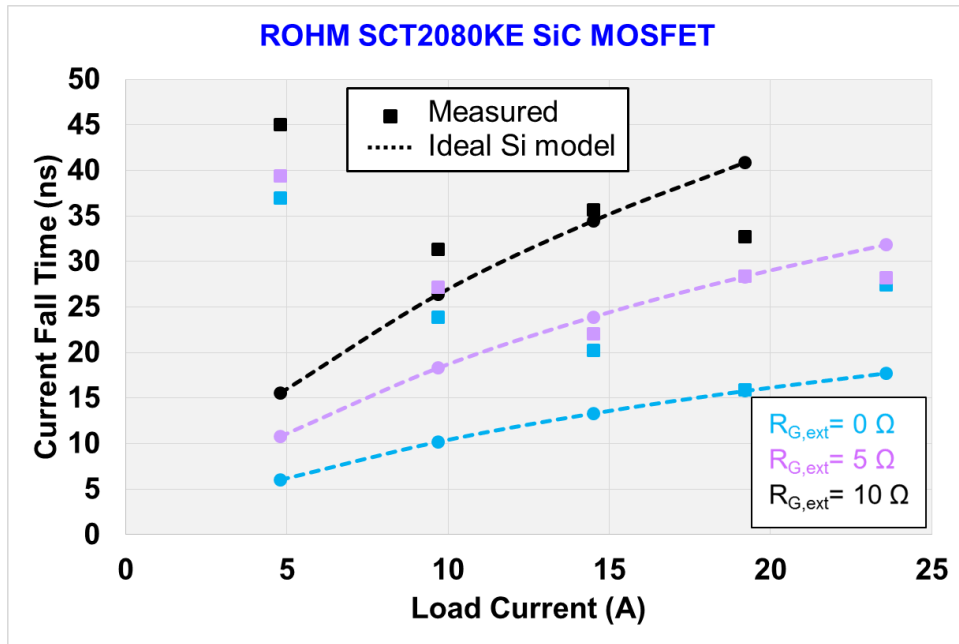


Figure 51: Comparison of the measured (squares) and calculated (dotted curves) current fall times of the ROHM SCT2080KE SiC MOSFET versus load current for external gate resistances of 0Ω (blue), 5Ω (purple), and 10Ω (black).

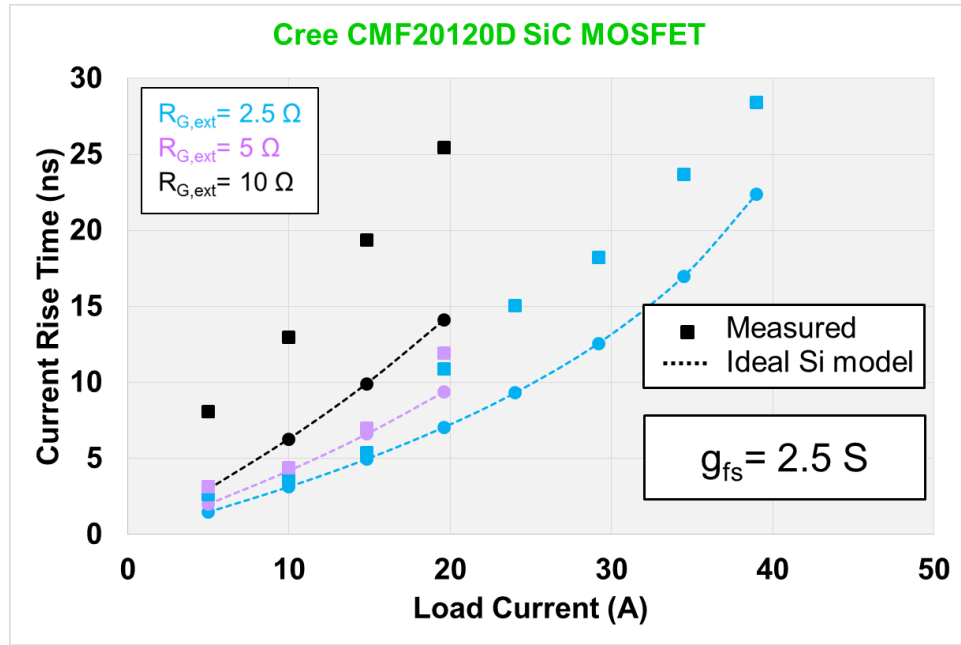


Figure 52: Comparison of the measured (squares) and calculated (dotted curves) current rise times of the Cree CMF20120D SiC MOSFET versus load current for external gate resistances of 2.5Ω (blue), 5Ω (purple), and 10Ω (black) with an optimized transconductance determined by curve-fitting.

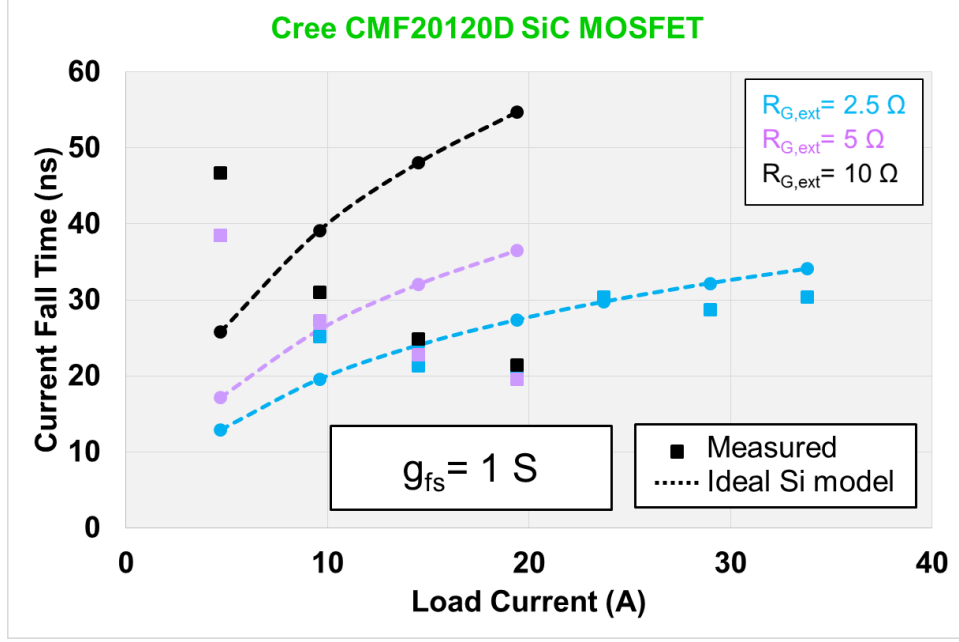


Figure 53: Comparison of the measured (squares) and calculated (dotted curves) current fall times of the Cree CMF20120D SiC MOSFET versus load current for external gate resistances of 2.5 Ω (blue), 5 Ω (purple), and 10 Ω (black) with an optimized transconductance determined by curve-fitting.

2.5.4 Proposed New Analytical Model for 1.2 kV SiC MOSFETs

The objective of this work is to develop a way for users to quickly and easily predict and compare the performance of SiC devices. To accomplish this, the simple model presented in the previous section, which utilizes the switching waveforms and MOSFET equivalent circuit to calculate the turn on and turn off switching times, will be revised to better fit with the measured data.

Since the current rise stage for SiC MOSFETs is similar to that of Si MOSFETs, the current rise time expression shown in equation (1) can still be utilized. However, another method for determining the plateau voltage is required. As five different SiC MOSFETs have been extensively characterized in this work, a curve fitting approach is taken to find a common relationship for the plateau voltage. First, the current rise times

of each of the SiC MOSFETs for varying load currents and external gate resistances were measured. Next, the current rise time equation was set equal to these measured values such that the corresponding plateau voltage could be found, where the other parameters in the equation were taken from the device datasheets [45], [47], [48] and are listed in Table VII. These determined plateau voltages were then plotted versus load current for each of the SiC MOSFETs with different external gate resistances (Figure 54).

As shown by Figure 54, the plateau voltage is linearly related to the load current, as was seen in the plateau voltage expression of equation (3) from [50]. A general linear expression can be used to now determine approximate plateau voltages for each of the SiC MOSFETs for the current rise time stage. With this approximate plateau voltage, the current rise time can then be calculated using equation (3). Figure 55, Figure 56, and Figure 57 show the current rise time results for this revised analytical model compared to the measured data for the Cree CMF20120D, ROHM SCT2080KE, and GE GE12N20L SiC MOSFETs, respectively. As shown by the figures, the revised model is in better agreement with the measured results. Alternatively, instead of finding a general expression relating the plateau voltage to the load current for all of the SiC MOSFETs, a specific relationship can be found for each device. This would allow for improved accuracy.

Table VII: Parameters from the device datasheets [45], [47], [48] that were used to evaluate the switching time equations (3) and (7).

<i>Parameter</i>	<i>Cree CMF20120D</i>	<i>ROHM SCT2080KE</i>	<i>GE GE12N20L</i>
$R_{G,int}$	5 Ω	6.3 Ω	2.5 Ω
C_{ISS}	1.8 nF	2.08 nF	1.28 nF
V_{Drive}	20 V	20 V	20 V
$V_{GS(th)}$	2.65 V	2 V	2.12 V
C_{GD}	25 nC*	35 nC*	25 nC*

*Taken at approximately 100 V.

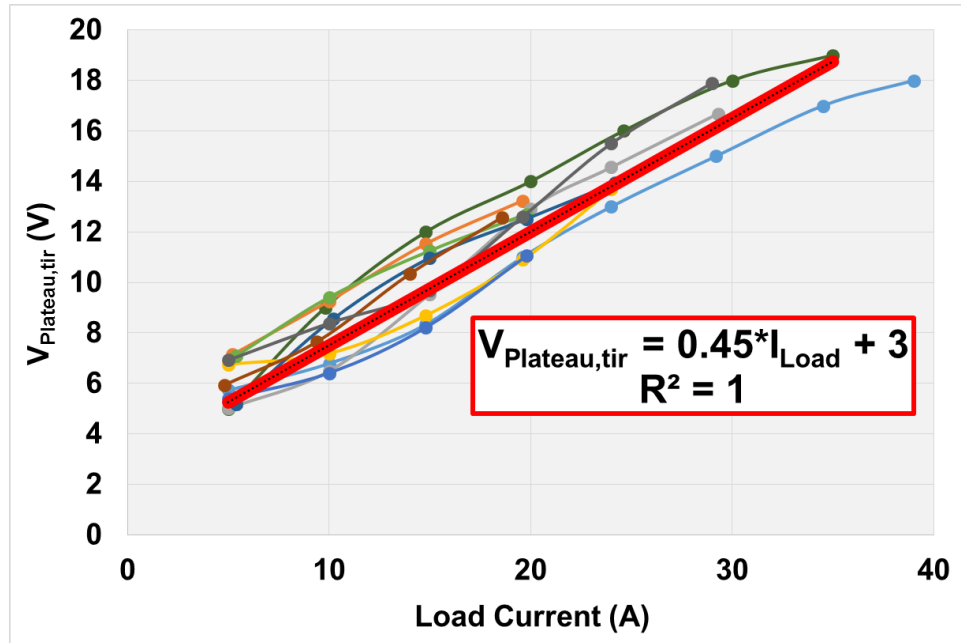


Figure 54: Plot of plateau voltage versus load current for all of the SiC MOSFETs with different external gate resistances for the current rise transition. The red curve is the general linear relationship to be used to determine the plateau voltage during this stage for each MOSFET and a given load current.

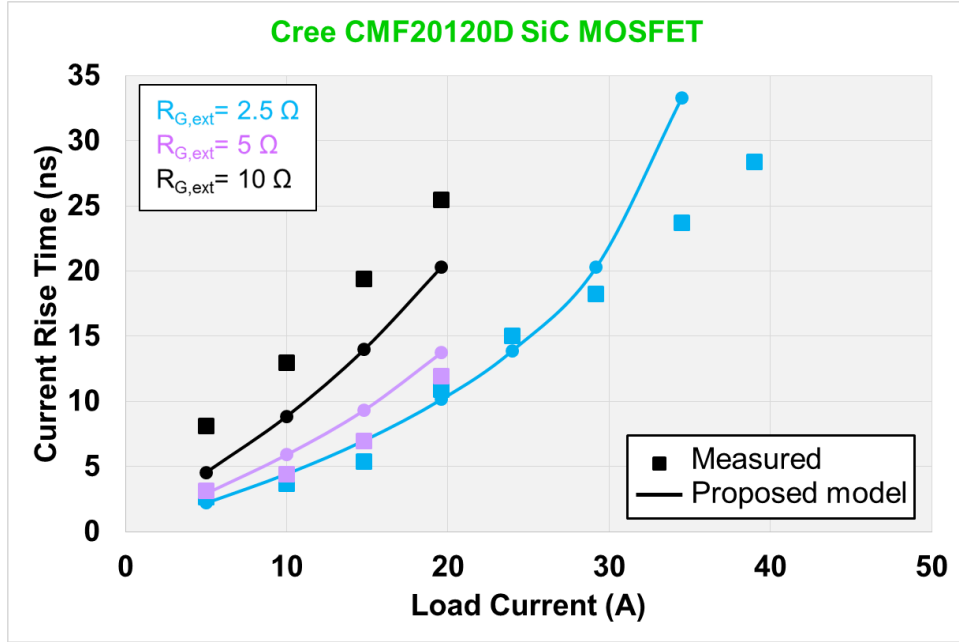


Figure 55: Comparison of the measured (squares) and proposed model (solid curves) current rise times of the Cree CMF20120D SiC MOSFET versus load current for external gate resistances of 2.5 Ω (blue), 5 Ω (purple), and 10 Ω (black).

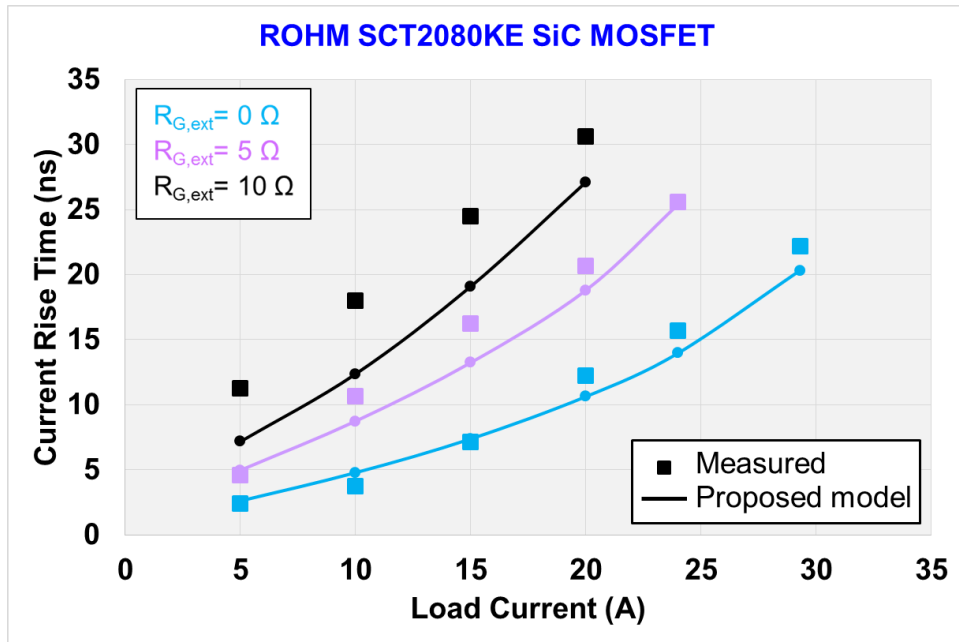


Figure 56: Comparison of the measured (squares) and proposed model (solid curves) current rise times of the ROHM SCT2080KE SiC MOSFET versus load current for external gate resistances of 0 Ω (blue), 5 Ω (purple), and 10 Ω (black).

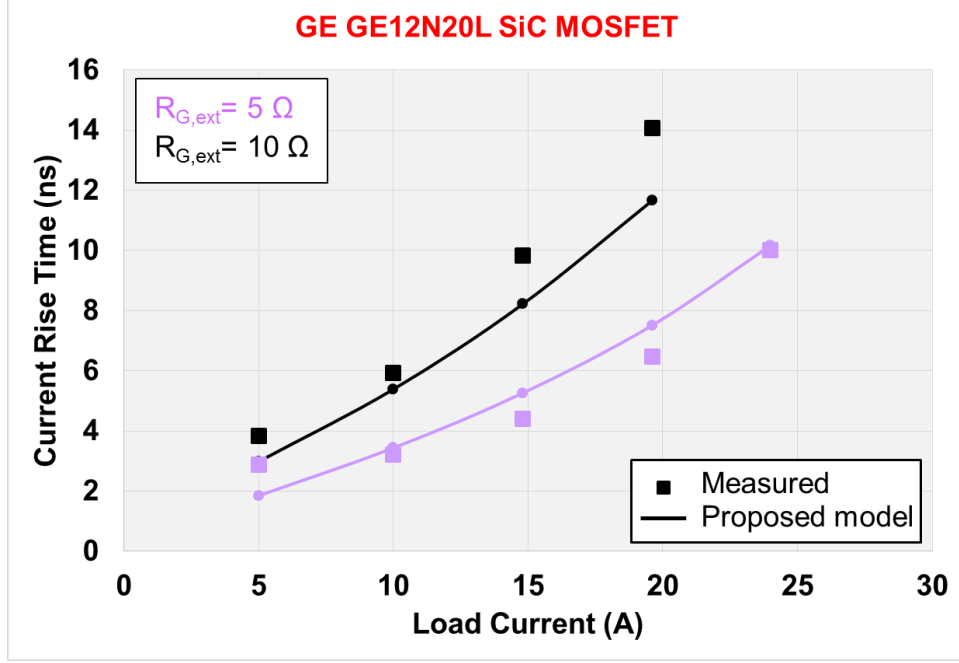


Figure 57: Comparison of the measured (squares) and proposed model (solid curves) current rise times of the GE GE12N20L SiC MOSFET versus load current for external gate resistances of 5 Ω (purple), and 10 Ω (black).

For the voltage fall transition period, equation (4) was adjusted as shown in equation (7), below.

$$t_{vf} = R_G C_{GD} \frac{(V_{dc}(0.1) - V_{dc}(0.9))}{V_{drive} - V_{Plateau,tvf}} \quad (7)$$

Instead of using the gate-drain charge, the gate-drain capacitance and change in the drain-source voltage were utilized. There are two reasons for this. First, the capacitance curves in the datasheets can be used to find the gate-drain capacitance over a wide range of voltages, whereas typically the gate-drain charge is only specified at a single voltage. Second, this allows the user to take into consideration the fact that the voltage fall time is commonly measured from 90 % to 10 % of the dc voltage, and thus the calculated results will be in line with these measurements. For instance, for a dc

voltage of 600 V, the voltage fall time would then be taken over the drain-source voltage range of 540 V to 60 V. As shown in Figure 16, the Miller capacitance of these SiC MOSFETs does not change as dramatically at voltages greater than approximately 50 V, therefore an average capacitance value for this drain-source voltage range will result in sufficient accuracy. In this work, the Miller capacitance corresponding to a drain-source voltage of approximately 100 V was used.

With this revised expression, the voltage fall time equation was set equal to the measured values such that the corresponding plateau voltage could be found, where the other parameters in the equation were taken from the device datasheets [45], [47], [48] and are listed in Table VII. These ascertained plateau voltages were then plotted versus load current for each of the SiC MOSFETs with different external gate resistances (Figure 58).

As shown by Figure 58, the plateau voltage is linearly related to the load current, as was seen for the current rise transition phase. However, it can be noticed that the plateau voltage during the voltage fall period is less dependent on load current than for the current rise transition. A general linear expression can again be used to now determine approximate plateau voltages for each of the SiC MOSFETs for the voltage fall time stage. With this approximate plateau voltage, the voltage rise time can then be calculated using equation (7). Figure 59, Figure 60, and Figure 61 show the voltage fall time results for this revised analytical model compared to the measured data for the Cree CMF20120D, ROHM SCT2080KE, and GE GE12N20L SiC MOSFETs, respectively. As shown by the figures, the revised model is in better agreement with the measured results. Also, instead of finding a general expression relating the plateau voltage to the load

current for all of the SiC MOSFETs, a specific relationship can be found for each device. This would allow for improved accuracy.

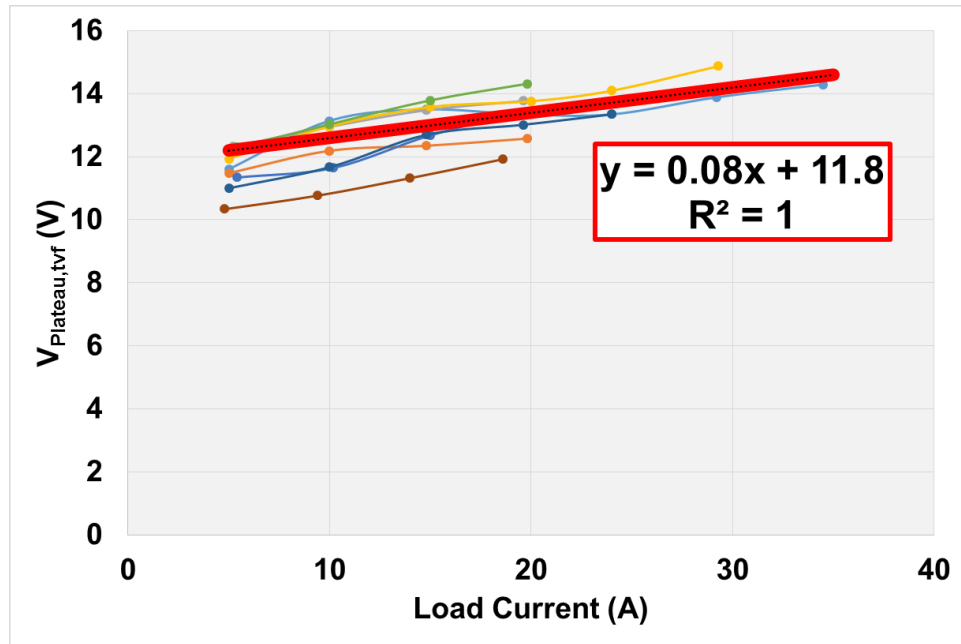


Figure 58: Plot of plateau voltage versus load current for all of the SiC MOSFETs with different external gate resistances for the voltage fall transition. The red curve is the general linear relationship to be used to determine the plateau voltage during this stage for each MOSFET and a given load current.

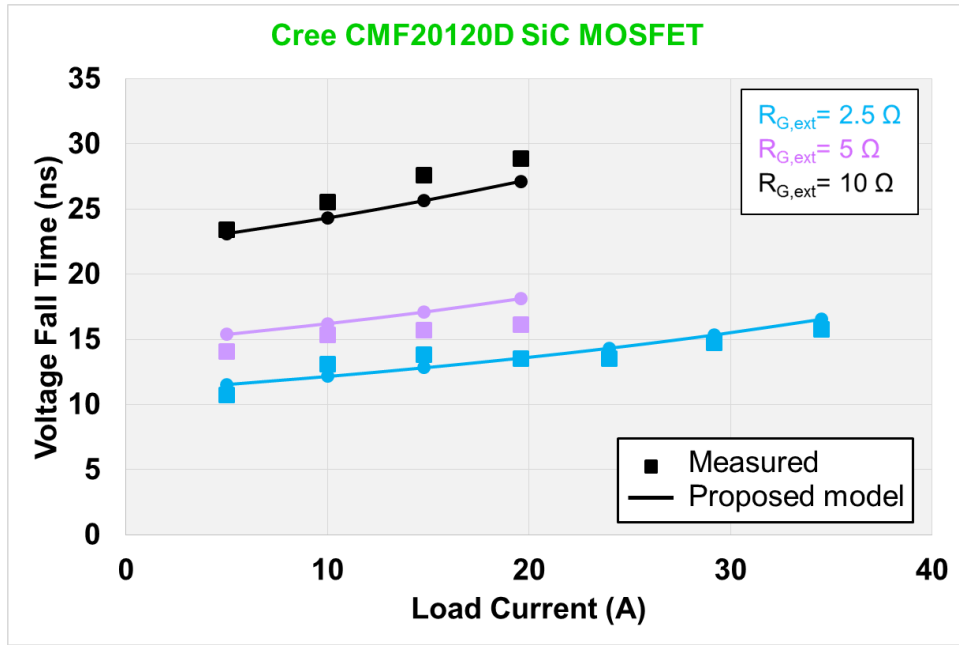


Figure 59: Comparison of the measured (squares) and proposed model (solid curves) voltage fall times of the Cree CMF20120D SiC MOSFET versus load current for external gate resistances of 2.5 Ω (blue), 5 Ω (purple), and 10 Ω (black).

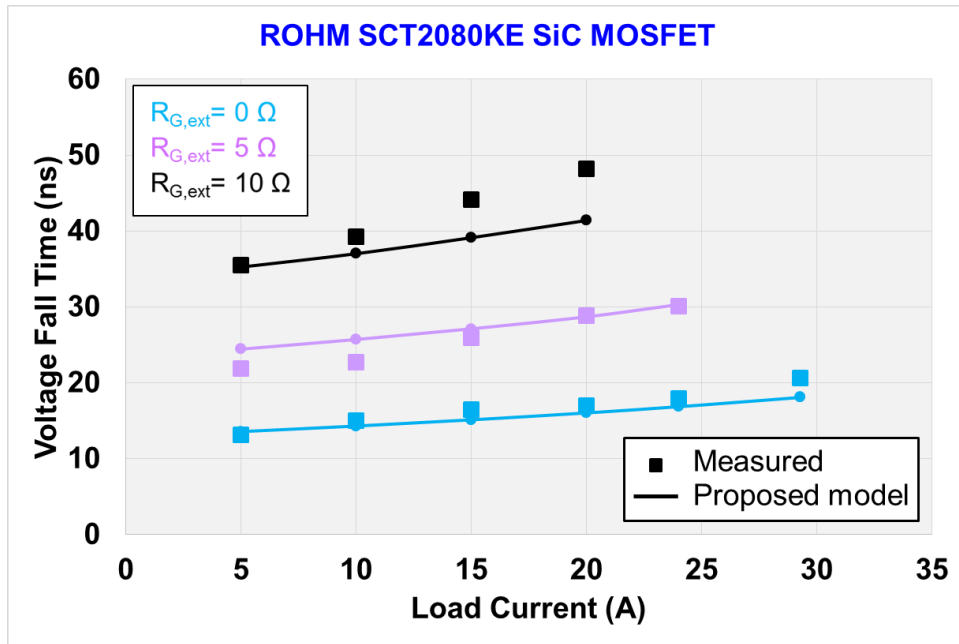


Figure 60: Comparison of the measured (squares) and proposed model (solid curves) voltage fall times of the ROHM SCT2080KE SiC MOSFET versus load current for external gate resistances of 0 Ω (blue), 5 Ω (purple), and 10 Ω (black).

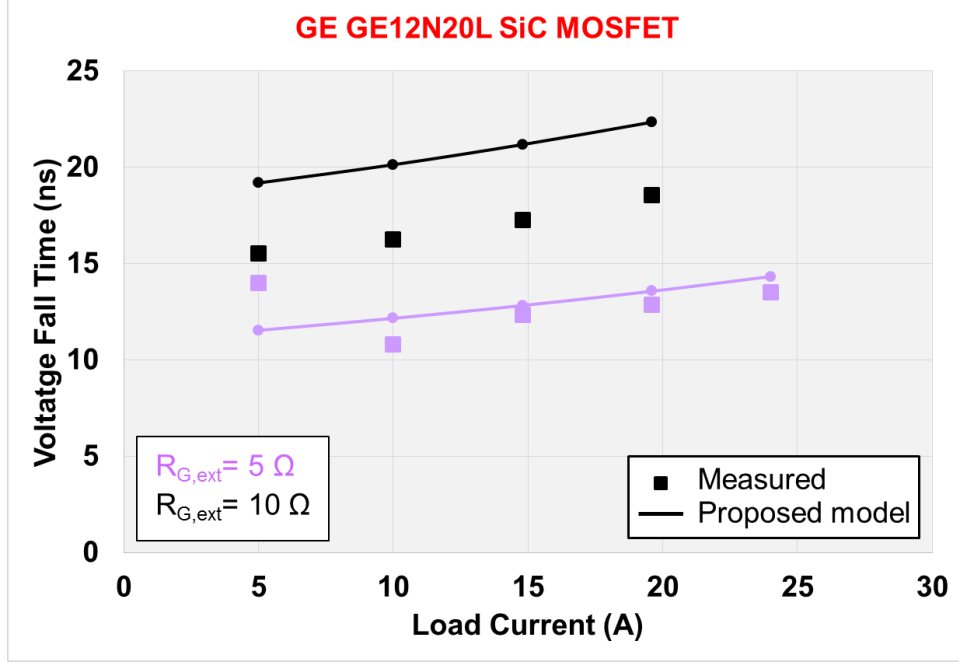


Figure 61: Comparison of the measured (squares) and proposed model (solid curves) voltage fall times of the GE GE12N20L SiC MOSFET versus load current for external gate resistances of 5 Ω (purple), and 10 Ω (black).

For the turn off process, the plateau voltages can be found by setting the following expressions for the voltage rise and current fall times equal to the measured results.

$$t_{vr} = R_G C_{GD} \frac{(V_{dc}(0.1) - V_{dc}(0.9))}{V_{Plateau,tvr}} \quad (8)$$

$$t_{if} = R_G C_{ISS} \ln \left(\frac{V_{Plateau,tif}}{V_{GS(th)}} \right) \quad (9)$$

Figure 62 shows the plot of the plateau voltage versus load current for the voltage rise transition. As shown by the figure, it can be seen that the plateau voltage determined using equation (8) is not linearly related to the load current. Instead, there is a logarithmic relationship. Figure 63 shows the plot of the plateau voltage versus load

current for the current fall transition. As shown by the figure, it can be seen that the plateau voltage determined using equation (9) is also not linearly related to the load current.

More work needs to be done to determine the reason for this nonlinear relationship between the plateau voltages and load current for the turn off process. The proposed model, however, showed good prediction of the current rise and voltage fall times. This information is useful in the early design stages of converters. For example, knowledge of these transition times would allow for sufficient estimation of the switching losses of different devices under a variety of operating conditions (such as load current and external gate resistance values). This gives the designers more flexibility than the dynamic characteristics presented in the device datasheets, which are typically shown for a small number of operating conditions.

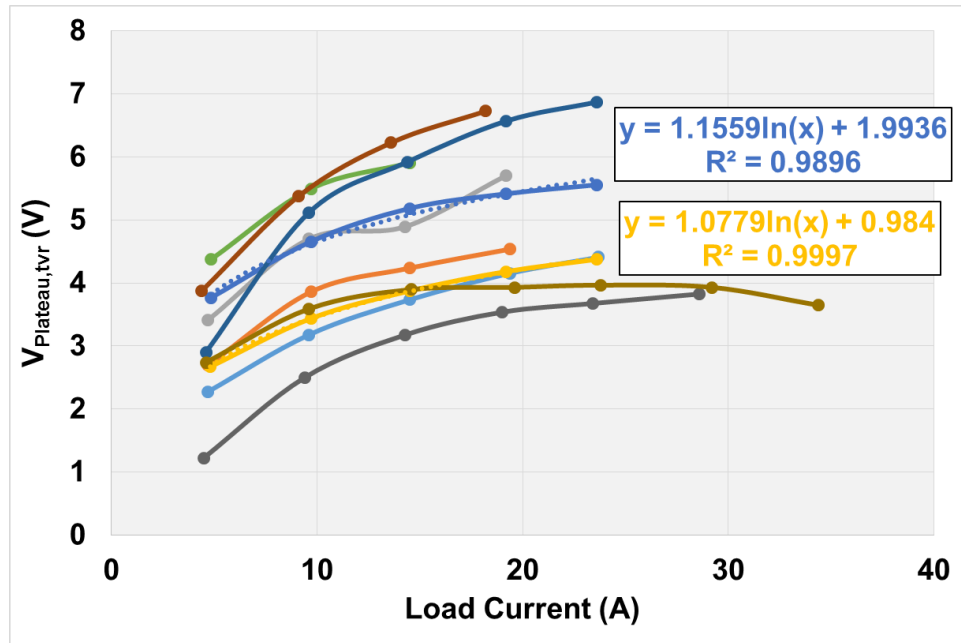


Figure 62: Plot of plateau voltage versus load current for all of the SiC MOSFETs with different external gate resistances for the voltage rise transition.

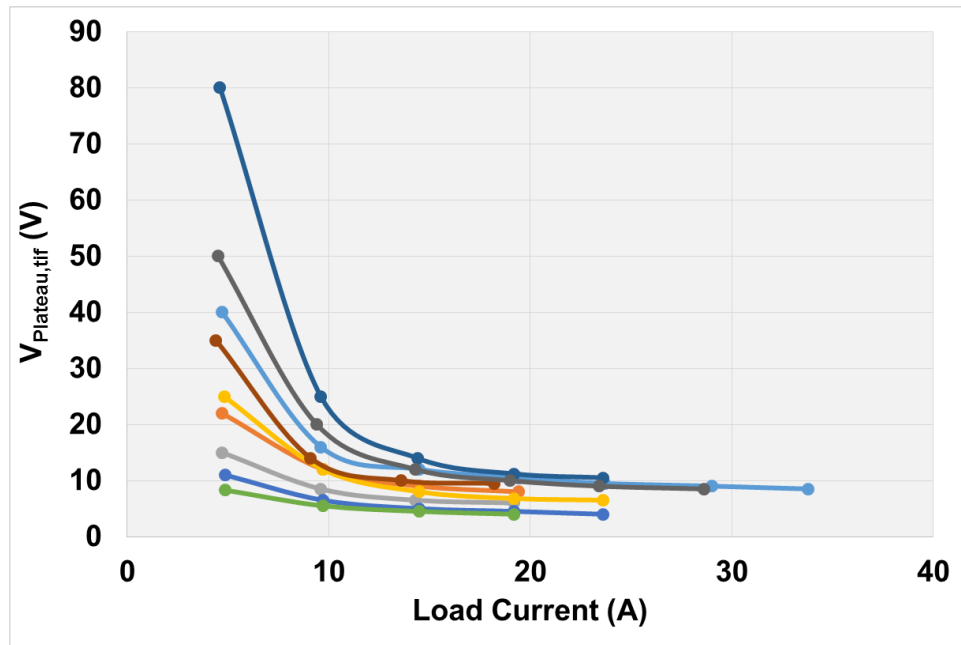


Figure 63: Plot of plateau voltage versus load current for all of the SiC MOSFETs with different external gate resistances for the current fall transition.

Chapter 3 Characterization of 1.2 kV SiC BJT and SJT

3.1 *Introduction*

The Bipolar Junction Transistor (BJT) was invented by William Schokley, John Bardeen, and Walter Brattain in 1949 at Bell Laboratories [64]. The BJT requires a junction of n-type and p-type doped semiconductor, which results in the bidirectional flow of two types of charge carriers: electrons and holes. This is contrary to unipolar devices, such as FETs, which only have one kind of charge carrier.

The BJT was eventually replaced by CMOS technology for a number of reasons. First, the Si BJT featured low current gain; that is, the ratio of supplied base current (input) to the resulting collector current (output). The current gain would also reduce as the current rating of these Si BJTs was increased [65]. Second, the large dynamic resistance within the device resulted in high switching losses [65]. Third, the BJTs experienced numerous reliability issues. In forward-biased mode, high temperature filaments could arise with current crowding, thereby leading to device failure [65]. Reverse-biased breakdown could also occur due to voltage and current stress present during inductive load switching, which cause the electric field stress to extend beyond the drift region [65]. Consequently, strict limits were placed on the Reverse Safe Operation Area (RSOA) of the Si BJTs, and thus they had no short-circuit capability [65].

It is thought that the implementation of BJTs in SiC would revive this technology. The wider band gap of SiC allows for a higher current gain [65] and therefore lower

driver losses and improved efficiency. The higher breakdown field of SiC also makes the BJT less susceptible to thermal runaway and thus increases the reliability [65]. In this chapter, the background of SiC BJTs will be discussed, and then the results of the high temperature static and dynamic characterization will be presented.

3.2 *Background of SiC BJTs*

As mentioned in the previous section, SiC BJTs feature many improvements over their Si counterparts. SiC BJTs also possess qualities that make them good contenders to Si IGBTs. These benefits include wider RBSOA, lower stored charge allowing for faster switching, more modest reduction of the current gain at high current densities, smaller collector-emitter saturation voltage, and high temperature operation [66]. Of course, unlike Si IGBTs, the SiC BJT requires a continuous base driving current, which can complicate driving in some applications. However, as will be shown in this chapter, SiC BJTs have large current gains, thereby reducing the needed base current. A typical structure for the SiC BJT is shown in Figure 64.

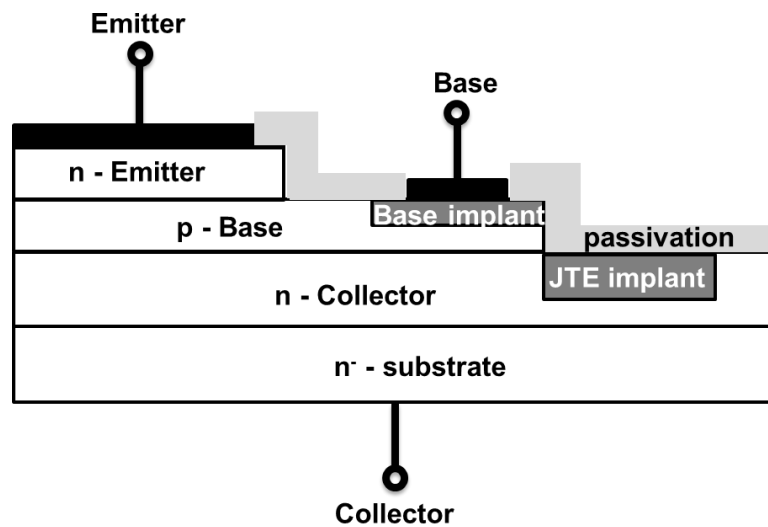


Figure 64: SiC BJT structure.

The SiC BJTs and SJT that will be assessed in this work are listed in Table VIII, where all of the devices are rated at 1.2 kV and are in TO-247 package. This table lists the device manufacturer, part number, continuous current and operation temperature ratings as listed in their respective datasheets [67]-[69], and their die areas normalized to that of Cree's C2M0080120D 2nd Generation Z-FET. Normalizing the die areas shows the sizes of the devices relative to one another, which is significant because the size of the device directly relates to the on-state resistance and parasitic capacitance. As the device size is reduced, the on-state resistance increases, thereby resulting in higher conduction losses. On the contrary, smaller devices feature lower capacitances, which results in faster switching and thus reduced dynamic losses.

Table VIII: 1.2 kV SiC BJTs and SJT under study.

<i>Mfg.</i>	<i>Device</i>	<i>$I_{D,Cont}$</i>	<i>T_{JMax}</i>	<i>$A_{Norm\ to\ Cree}$ C2M0080120D</i>
Fairchild Semiconductor	FSICBH057A120	20 A (100 °C)	175 °C	0.64
	FSICBH017A120	50 A (100 °C)	175 °C	1.88
GeneSiC Semiconductor	GA06JT12-247	6 A (90 °C)	175 °C	0.33

3.3 Static Characterization of the 1.2 kV SiC BJTs and SJT

In the following subsections, the methods and measurement results for the static characterization of the SiC BJTs and SJT listed in Table VIII will be presented. The parameters include: blocking capability, collector-emitter saturation voltage, base-emitter saturation voltage, current gain, output characteristics and on-resistance, internal base

resistance, and parasitic capacitances. Each parameter, with the exception of the internal base resistance and parasitic capacitances, was measured from 25 °C to 200 °C in order to assess the high temperature capabilities of the devices under study.

3.3.1 Static Characterization Methods

The static characterization was performed using a Tektronix 371b curve tracer, and Agilent 4294A impedance analyzer. For the Tektronix 371b curve tracer, four-terminal (also known as Kelvin) sensing was employed to ensure measurement accuracy. A hotplate and thermocouple were used for heating and temperature sensing. Measurements were taken in 25 °C increments from 25 °C to 200 °C. Once the desired steady-state temperature was reached, measurements were taken quickly in order to avoid the self-heating of the devices.

3.3.2 Blocking Capability

For Si BJTs, the breakdown voltage of the device when the base is left open BV_{CEO} , is lower than the breakdown voltage when the base is shorted and the emitter is open BV_{CBO} [6], [70]. This is because, when the base of the Si BJT is open and a positive bias is applied to the collector terminal, the base-emitter junction is forward biased and the base-collector junction is reverse biased [6]. Therefore, the majority of the voltage is supported by the base-collector junction [6]. Since the leakage current also flows through the base-emitter junction, the gain of the transistor amplifies the current, reducing the maximum blocking capability of the Si BJT [6]. Consequently, the breakdown voltage of Si BJTs is limited by BV_{CEO} [6].

It has been shown in [70], however, that SiC BJTs do not experience an obvious difference between BV_{CEO} and BV_{CBO} . This can be attributed to the low current gain of the SiC BJTs at low current densities [70]-[73]. This change in current gain with collector current will be discussed in more detail in a later section.

In this work, the leakage current of the SiC BJTs was measured at a collector-emitter bias of 1200 V for increasing temperatures under two different conditions: (1) shorted base, and (2) opened base. When the base was shorted to the emitter, Fairchild's SiC BJTs showed leakage currents well below 10 μ A up to 200 °C, as was the case for the SiC MOSFETs. Since the resolution of the 371b curve tracer is 10 μ A/div at this power level, a specific leakage current value for these SiC BJTs could not be accurately determined. For GeneSiC's SiC SGT, when the gate and source terminals were shorted, a leakage current of 20 μ A was observed at both 25 °C and 200 °C.

If instead the base terminal is left open, the leakage currents for the SiC BJTs and SGT devices typically increased, as is also the case for Si BJTs. However, this parameter is not specified in the datasheets of these devices [67]-[69].

Table IX lists the open-base leakage currents of the SiC BJTs and SGT that were measured in this work for a blocking voltage of 1200 V at 25 °C and 200 °C. It can be seen from this table that, while the FSICBH057A120 BJT maintained low leakage currents under the open base condition, the leakage currents of the FSICBH017A120 BJT and SGT increased, especially at high temperature. For the SGT, at 200 °C, the leakage current increased abruptly after approximately 1100 V.

Table IX: Open-base leakage currents of the SiC BJTs and SJT for a blocking voltage of 1200 V at 25 °C and 200 °C

<i>Mfg.</i>	<i>Device</i>	<i>T</i>	<i>I_{c,leak}</i>
Farichild Semiconductor	FSICBH057A120	25 °C	<10 μ A
		200 °C	<10 μ A
	FSICBH017A120	25 °C	30 μ A
		200 °C	70 μ A
GeneSiC Semiconductor	GA06JT12-247	25 °C	200 μ A
		200 °C	>500 μ A at 1150 V

3.3.3 Collector-Emitter Saturation Voltage

The low collector-emitter saturation voltage of SiC BJTs makes these devices good competitors to Si IGBTs. The two primary reasons for this reduced collector-emitter saturation voltage are: (1) the opposite polarities of the base-emitter and collector-base voltages, and (2) the high critical field strength of SiC. In the saturation mode of operation, the base-emitter and collector-base junction voltages experience opposite polarities such that they virtually cancel each other [66]. This near cancellation results in a low contribution to the collector-emitter voltage [66]. The high critical electric field strength of SiC, as mentioned previously, allows for a thinner collector region and higher doping concentrations, which result in a lower resistance of the collector region when

compared to Si [66]. Furthermore, this eliminates the need for conductivity modulation of the collector region [66].

The collector-emitter saturation voltages of the Fairchild SiC BJTs and GeneSiC SGT versus temperature are shown in Figure 65, below. As shown by the figure, the SiC BJTs experience low collector-emitter saturation voltages, which increase with increasing temperature. These measured values are in good agreement with those listed in the datasheets [67]-[69]. For comparison, the collector-emitter saturation voltage of a 1.2 kV, 15 A Si IGBT from Infineon (IHW15N120R3) is also plotted. Si IGBTs with collector currents similar to that of GeneSiC's SiC SGT (rated at 6 A at 90 °C) showed similar collector-emitter voltages to that of the IHW15N120R3, so this data was not included. However, Si IGBTs with current ratings comparable to that of Fairchild's FSICBH017A120 SiC BJT (rated at 50 A at 100 °C) showed much higher collector-emitter voltages of greater than 2 V at room temperature.

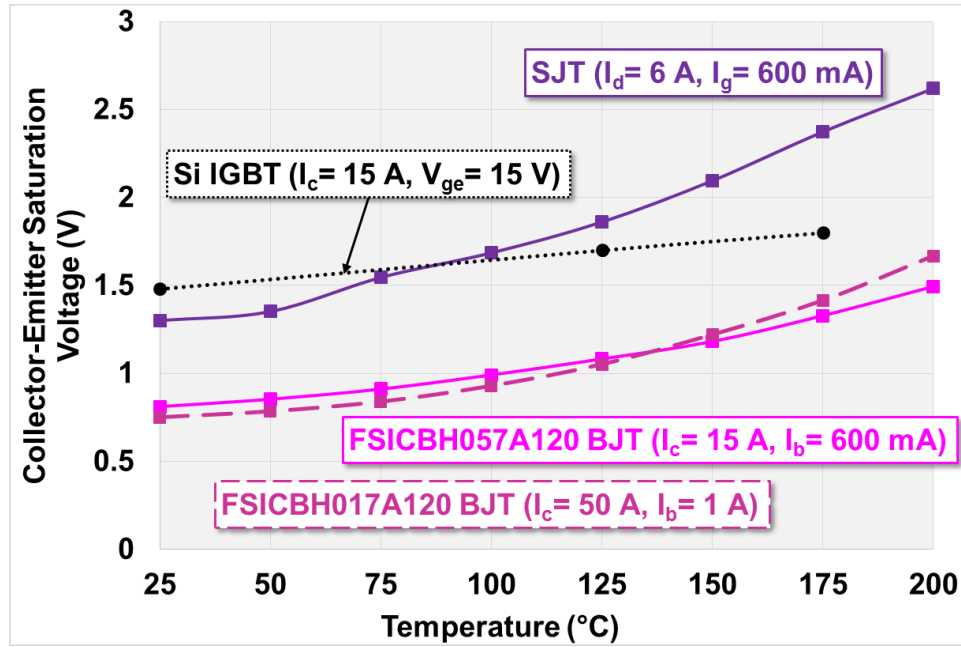


Figure 65: Collector-emitter saturation voltage versus temperature curves for the SiC BJTs and SJT. A Si IGBT (IHW15N120R3) is included for comparison. The collector and base currents used for the measurements are shown in parentheses.

3.3.4 Base-Emitter Saturation Voltage

The base-emitter junction must be forward biased in order for the BJTs or SJT to start conducting. The base-emitter saturation voltages of the SiC BJTs and SiC SJT are shown in Figure 66. For the FSICBH057A120 BJT and GA06JT12-247 SJT a base current of 600 mA was applied, and the collector-emitter voltage was increased until the desired collector current was reached. This base current was selected because it is the value that will be utilized when measuring the on-resistance of the devices (up to 200 °C), and when driving the devices for the dynamic characterization testing. For the FSICBH017A120 BJT, a base current of 1 A was used. The reason for this selection is due to the high temperature output characteristics, which will be presented in a later section. As shown by the figure, the devices experience approximately a 0.5 V reduction

in their base-emitter saturation voltages from 25 °C to 200 °C. It can also be seen that the slope of the base-emitter voltage versus collector current curve is higher for the devices with greater current ratings.

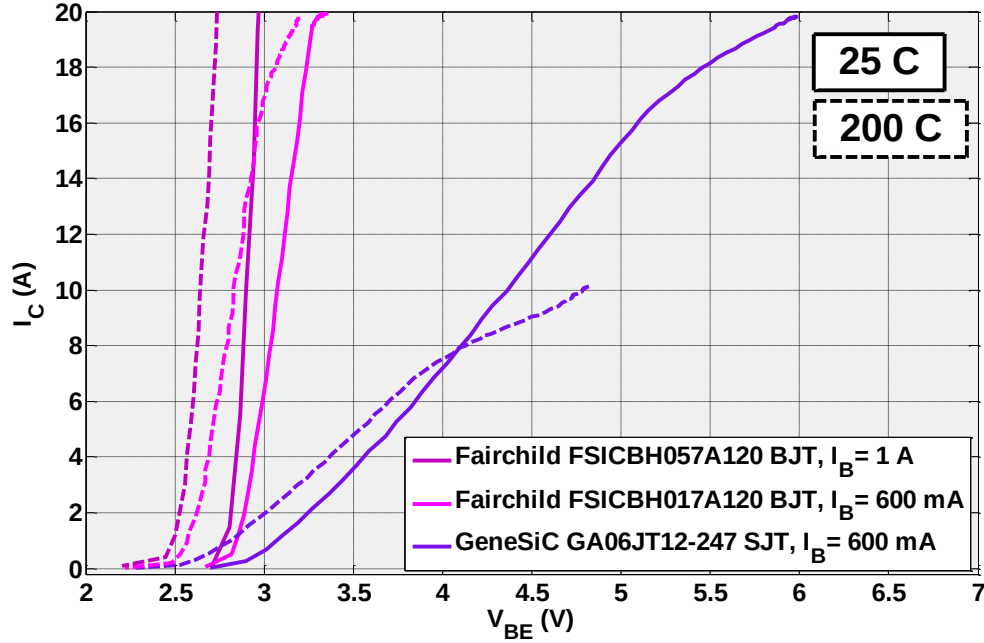


Figure 66: Base-emitter saturation voltage curves for the SiC BJTs and SiC SGT at 25 °C (solid curves), and 200 °C (dashed curves). The base current used for each device is given in the legend.

3.3.5 Current Gain

As was mentioned previously, the current gain of SiC BJTs is low at small current densities [70]-[73]. As the current increases, the gain increases due to less influence from the space charge recombination current in the base [70]. However, at high currents, the current gain falls off [72], [73]. Figure 67 shows a plot of current gain versus temperature for the SiC BJTs and SiC SGT. The current gains were taken at a collector-emitter voltage of 5 V, and at the respective continuous current rating of the device listed in Table VIII.

These measured current gains are in good agreement with those listed in the datasheets [67]-[69].

As shown in this figure, these devices have significantly higher current gains than those of conventional Si BJTs, indicating an improved driving capability. However, the current gains of both devices also have a strong negative temperature coefficient, decreasing by nearly 50 % at 200 °C relative to their respective room temperature values. This negative temperature coefficient of the SiC BJT is unlike that of the Si BJT, and is a result of the incomplete ionization of acceptor dopants at room temperature [73]-[75]. At elevated temperatures, the dopant ionization increases, resulting in a larger hole concentration in the base region, which reduces the emitter injection efficiency [73]-[75]. This phenomenon effectively cancels the positive temperature coefficient caused by the increase in minority carrier lifetime in the base [73]-[75]. The decrease in current gain with temperature is a positive attribute of the SiC BJT because it prevents thermal runaway, which leads to forward-biased second breakdown [73], [75].

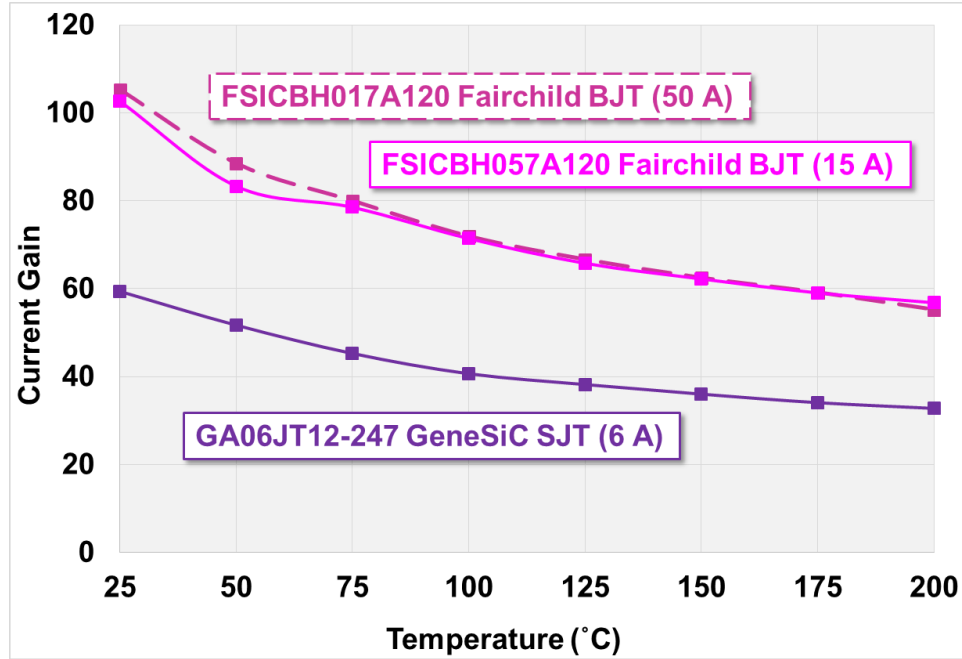


Figure 67: Current gain versus temperature curves for the SiC BJTs and SJT. The current gains were taken at a collector-emitter voltage of 5 V, and the collector currents listed in parentheses in the plot.

3.3.6 Output Characteristics/On-Resistance

The I-V curves of the SiC BJTs and SJT were measured using a curve tracer and four-terminal sensing for temperatures from 25 °C to 200 °C. Figure 68 shows the I-V curve comparison of one of the SiC BJTs for temperatures of 25 °C and 200 °C, and base currents of 100 mA to 1 A with 100 mA steps. This comparison demonstrates the temperature dependency of the on-state characteristics of the SiC BJTs. The decreased slope in the saturation region (called the linear region when referring to FETs) of the I-V curves indicates an increase in the on-resistance with an increase in temperature. Looking at the active region (known as the saturation region for FETs), it can be seen that the current gain of the SiC BJTs and SJT decreases as the temperature is increased, as was shown in the previous section.

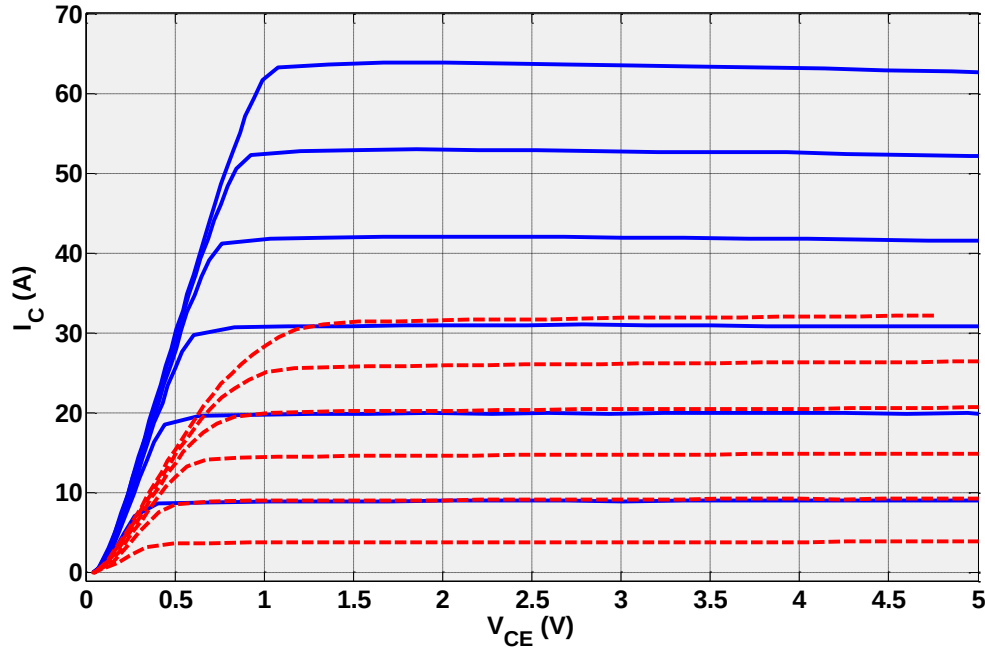


Figure 68: I-V curves of the SiC BJT for temperatures of 25 °C (blue solid curves) and 200 °C (red dashed curves) and base currents of 100 mA to 1 A with 100 mA steps.

From the I-V curves, the on-resistances of the SiC BJTs and SJT were calculated. Figure 69 shows the on-resistance versus temperature curves for these devices, with the on-resistance curve of Cree's C2M0080120D MOSFET shown as a reference. The on-resistances were measured at the collector currents listed in parentheses in the figure, and at a base current of 600 mA for the FSICBH057A120D BJT and GA06JT12 SJT, which is the approximate base current at which these devices will be driven for the dynamic characterization as will be shown in a later section. These measured on-resistances are in good agreement with those listed in the datasheets [67]-[69].

The on-resistance of the FSICBH017A120 BJT, on the other hand, was determined using a base current of 1 A. This is because the curves for the lower base currents would go into saturation prior to reaching a collector current of 50 A, which is the rated continuous current of the device [68]. This phenomenon can be seen in Figure

68, where it is evident that at 200 °C a base current of 600 mA is not sufficient to produce a collector current of 50 A, as it saturates at approximately 30 A.

As shown by Figure 69, the SJT experiences the highest on-resistance. This is largely due to its smaller size. As mentioned previously, a smaller device will have a higher on-resistance for a given blocking voltage. Consequently, it is important to look at the specific on-resistances of the devices. In this case, this figure was obtained by multiplying the measured on-resistance values by the die area of the device. Although the active area is typically used for this calculation, this dimension could not be obtained for all of the devices in this study, and so the die area was used instead.

Figure 70 shows the measured specific on-resistances versus temperature. The collector currents used for the measurements are shown in parentheses, and Cree's C2M0080120D SiC MOSFET is included for comparison. Figure 70 shows that the Fairchild BJTs feature low specific on-resistances. The low on-resistance of the BJT is due to junction voltage cancellation between the base-emitter and base-collector junctions [66], [72], [73].

Figure 71a and Figure 71b show the measured specific on-resistance versus collector current at 25 °C and 200 °C, respectively, for the SiC BJTs and SJT. Cree's C2M0080120D MOSFET is also included as a reference. As shown, while the SiC MOSFET experiences an increase in on-resistance at higher current densities, at room temperature the SiC BJTs and SJT demonstrate the opposite trend (Figure 71a). At high temperature, however, the SJT shows an increase in on-resistance with increased drain current (Figure 71b).

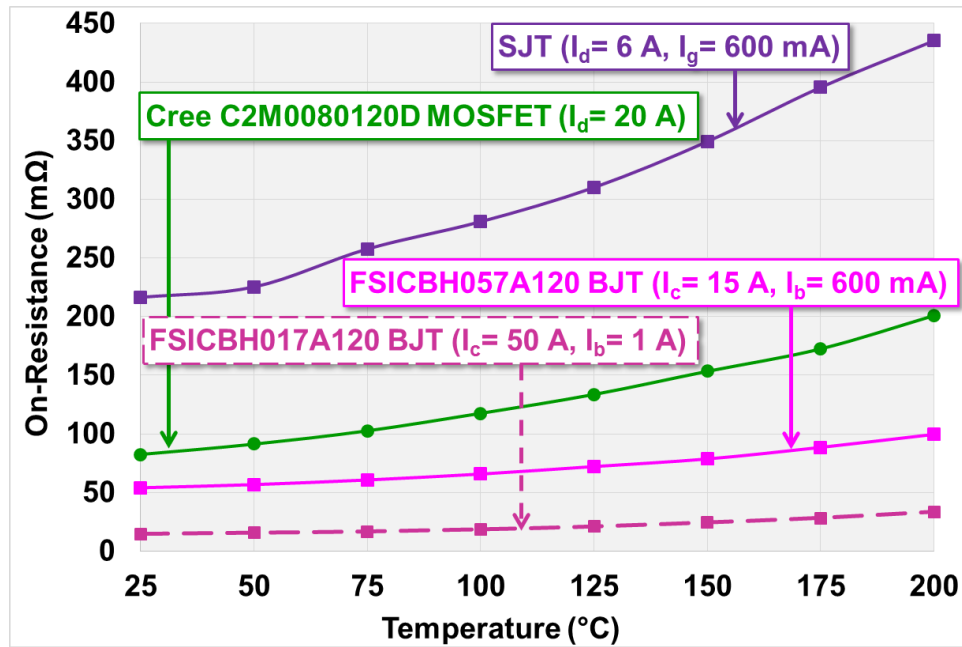


Figure 69: On-resistance versus temperature curves for the SiC BJT and SJT at the base and collector currents specified in parentheses. The on-resistance of Cree's C2M0080120D SiC MOSFET is included for comparison.

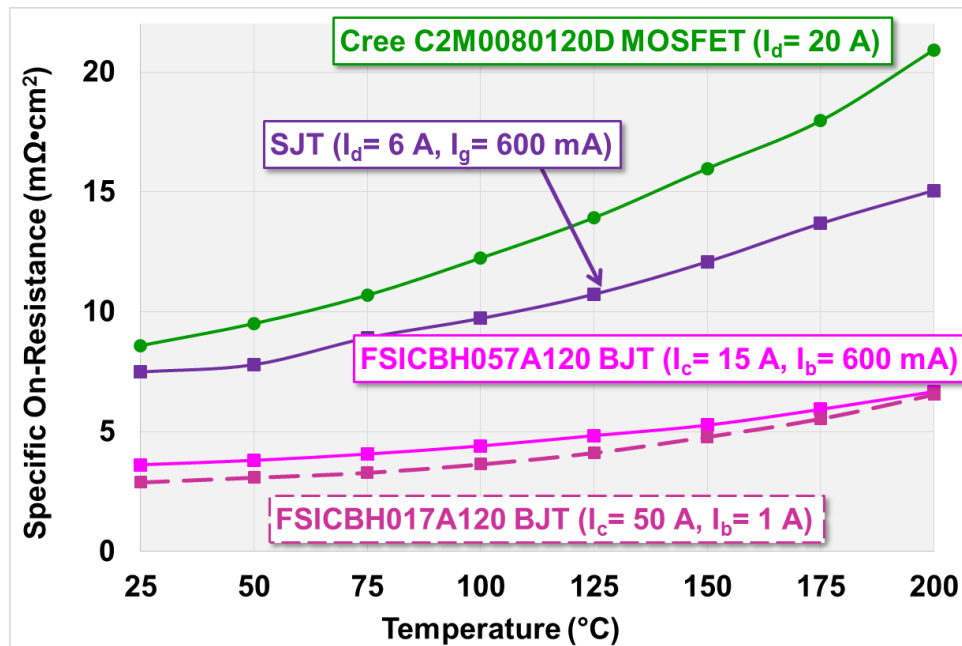
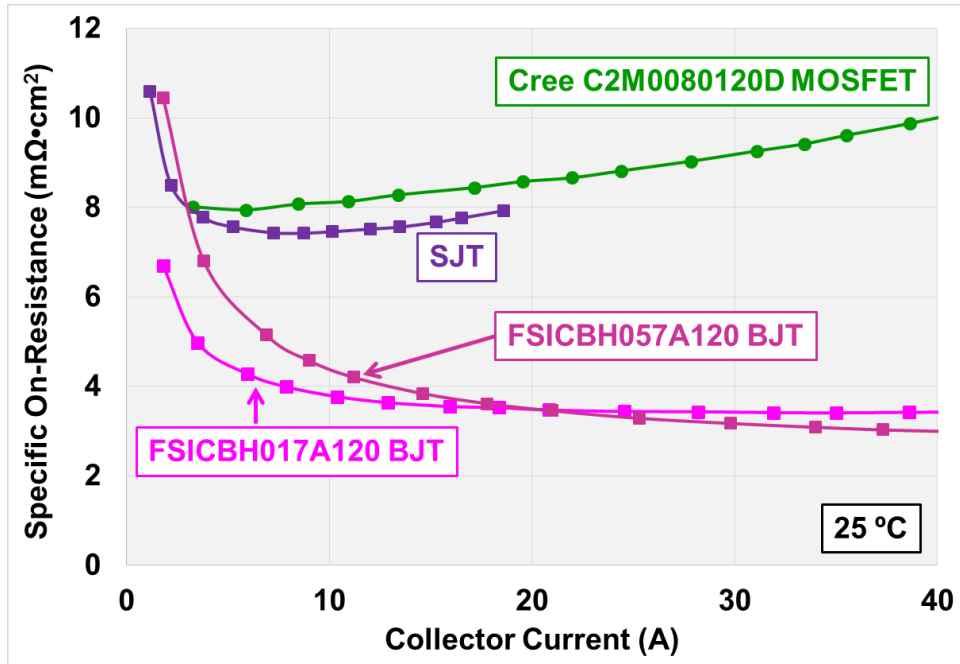
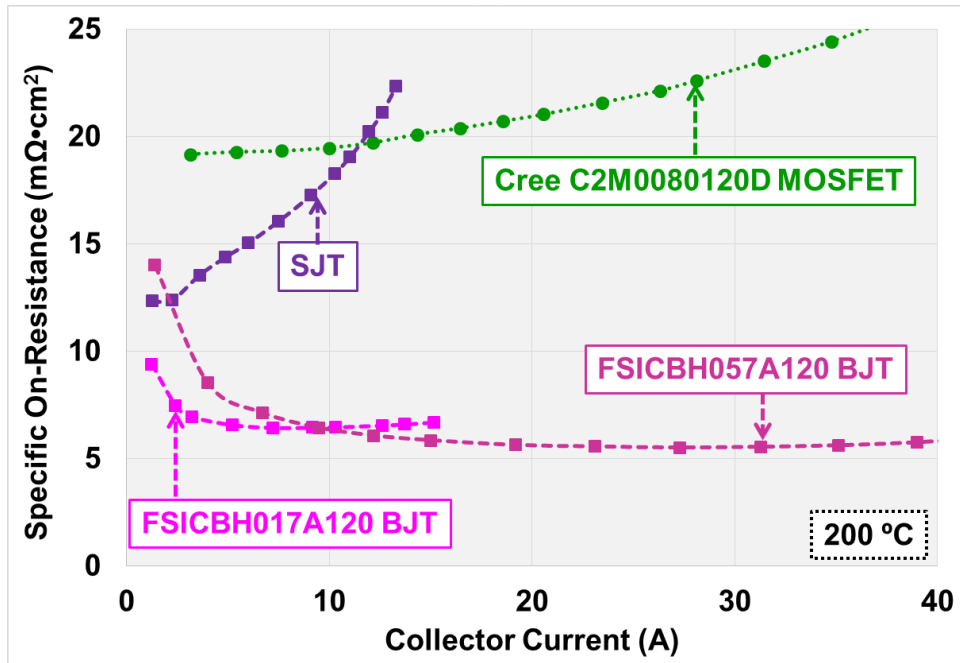


Figure 70: Specific on-resistance (using die area) versus temperature curves for the SiC BJT and SJT at the base and collector currents specified in parentheses. The specific on-resistance of Cree's C2M0080120D SiC MOSFET is included for comparison.



(a)



(b)

Figure 71: Specific on-resistance (using die area) versus drain current curves for each of the SiC BJTs and SJT at (a) 25 °C, and (b) 200 °C. The specific on-resistance of Cree's C2M0080120D is shown for comparison.

3.3.7 Internal Base Resistance

The internal base resistances of the FSICBH057A120 SiC BJT and GA06JT12-247 SiC SGT were determined using the impedance analyzer to measure across the base and emitter terminals with the collector floating (Figure 12). Measurements were taken at a frequency of 1 MHz. The resulting values are presented in Table X. It can be seen that Fairchild's FSICBH057A120 BJT has a low internal base resistance, which is more than six times less than that of GeneSiC's SGT.

Table X: Internal base resistances of the SiC BJT and SGT.

<i>Device</i>	<i>R_{G,int}</i>
Fairchild SiC BJT (FSICBH057A120)	2.4 Ω
GeneSiC SiC SGT (GA06JT12-247)	15.7 Ω

3.3.8 Parasitic Capacitances

The parasitic capacitances of the BJTs and SGT were measured in the same manner as was done for the SiC MOSFETs (Figure 13). However, only the input capacitances (sum of the base-collector and base-emitter capacitances) and the Miller capacitances (base-collector capacitances) were measured. The resulting capacitance versus voltage curves at room temperature are shown in Figure 72 and Figure 73, where Cree's C2M0080120D is included as a reference. As shown in Figure 72 and Figure 73, the FSICB017A120 BJT has the largest capacitances. When comparing the BJTs and

SJT, it can be seen that the devices with the smaller die areas (where the normalized die areas are shown in parentheses in the plots) have lower capacitances.

If the measured capacitances are divided by the die area, then the specific capacitances of the devices can be plotted to verify this assumption. As shown by Figure 74 and Figure 75, the distribution in specific capacitances is much narrower than that of the regular capacitance measurements. However, even when dividing by the die area, it can still be seen that the devices with the larger die sizes have slightly higher specific capacitances. This could be attributed to the fact that die area is utilized instead of active area. Upon receiving the die size information of the SiC BJTs from Fairchild, the company mentioned that the die areas have not yet been optimized and thus the active areas would give more accurate results. However, again since the active areas could not be obtained for the other devices, it was determined that only die area would be used.

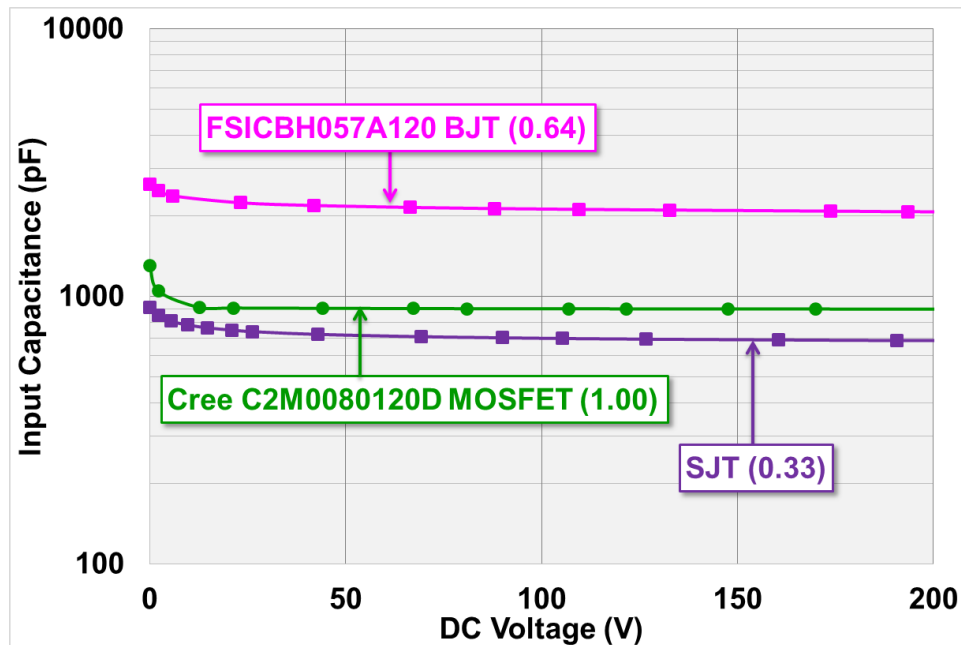


Figure 72: Input capacitance versus voltage curves for the SiC BJTs and SJT measured at 1 MHz and room temperature. The die areas of the devices normalized to that of Cree's C2M0080120D SiC

MOSFET are shown in parentheses. The capacitance curve of Cree's C2M0080120D MOSFET is also included for comparison.

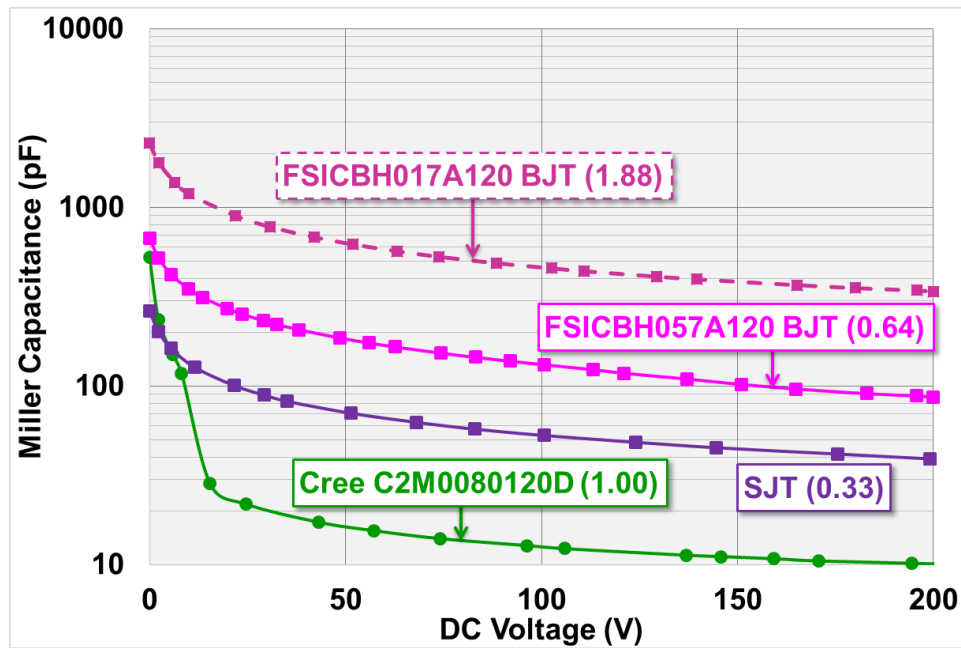


Figure 73: Miller capacitance versus voltage curves for the SiC BJTs and SJT measured at 1 MHz and room temperature. The die areas of the devices normalized to that of Cree's C2M0080120D SiC MOSFET are shown in parentheses. The capacitance curve of Cree's C2M0080120D MOSFET is also included for comparison.

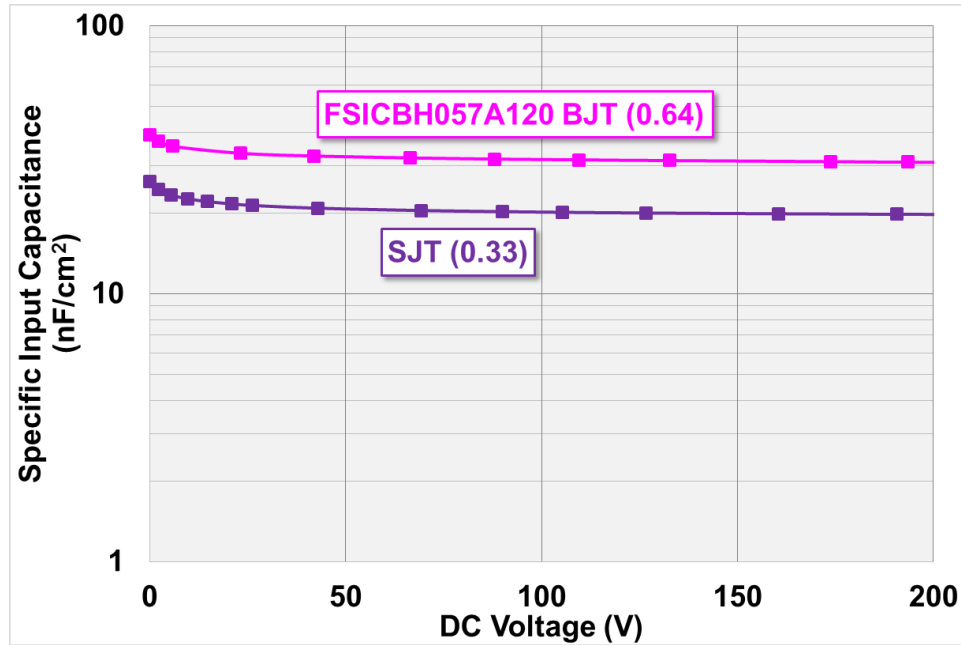


Figure 74: Specific input capacitance versus voltage curves for the SiC BJTs and SGT measured at 1 MHz and room temperature. The die areas of the devices normalized to that of Cree's C2M0080120D SiC MOSFET are shown in parentheses.

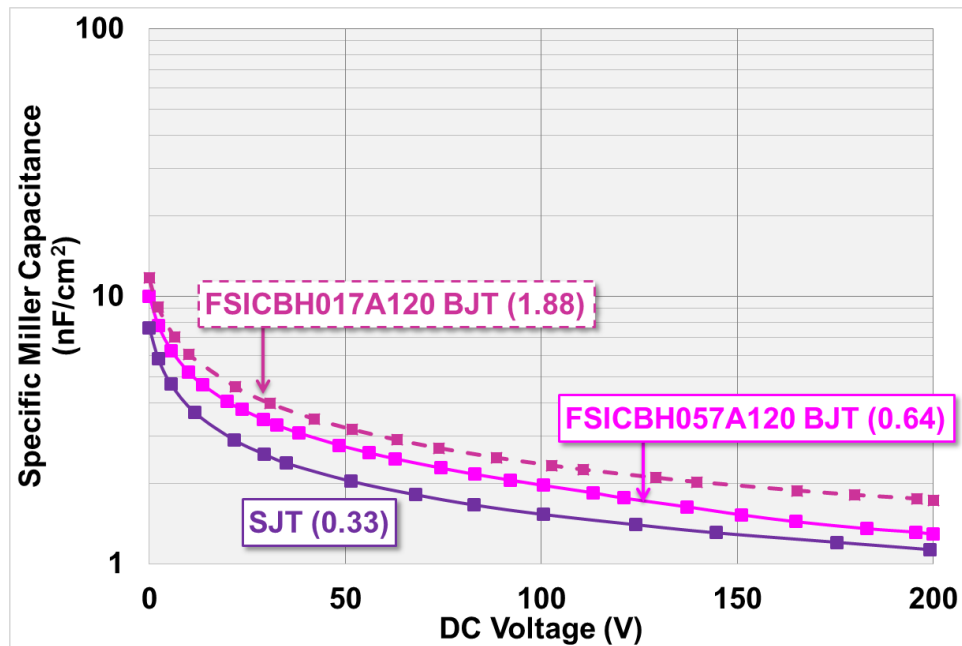


Figure 75: Specific Miller capacitance versus voltage curves for the SiC BJTs and SGT measured at 1 MHz and room temperature. The die areas of the devices normalized to that of Cree's C2M0080120D SiC MOSFET are shown in parentheses.

3.4 *Dynamic Characterization of the 1.2 kV SiC BJT and SJT*

In the following subsections, the driving and measurement methods used for the dynamic characterization of the SiC BJT and SJT will be presented. The switching energy losses of each device for different load currents and temperatures will also be shown. A comparison of the dynamic performance of the devices will then be provided.

3.4.1 **Dynamic Characterization Methods**

The same DPT circuit as was described for the SiC MOSFETs was utilized for the SiC BJT and SJT, except that now a ceramic capacitor was placed in parallel to the external base resistance (Figure 76). This driving technique for bipolar transistors was also shown in [19], [33] and [35]. This parallel capacitor allows current to be quickly sourced and removed to and from the base of the device, thereby resulting in faster switching and thus reduced dynamic losses.

However, it is also important to take the driving losses associated with this simple driving scheme into consideration. Since these devices require a dc current in the on-state, power will be dissipated across the external base resistor. Considering this to be the primary contributor to the driving losses, the following approximation can be made

$$P_{drive} = I_{ON} \times V_R = \frac{(V_{drive} - V_{BE(sat)})^2}{R_{G,ext}} \quad (10)$$

where V_{drive} is the supplied voltage to the base, $V_{BE(sat)}$ is the base-emitter saturation voltage of the BJT or SJT, and $R_{G,ext}$ is the external base resistance. As shown by this equation, a smaller external base resistance will result in increased driving losses.

Increasing the driving voltage would also result in greater power dissipation across the

external base resistance. On the other hand, a larger driving voltage also increases the switching speed of the transistor and thus reduces the transient losses.

A series of DPTs were performed for various combinations of external base resistance and base supply voltage in order to evaluate the impact of these parameters on the driving and switching losses. The external base resistance was varied from 5 Ω to 30 Ω , and the supply voltage was changed from 10 V to 20 V. Figure 77 shows the dynamic power loss breakdown for some of the tested resistor-voltage combinations. As shown by the figure, increasing the driving voltage reduced the switching losses, but increased the driver losses, as expected. While increasing the external base resistance from 5 Ω to 30 Ω for a constant driving voltage reduced the driver losses significantly, it did not have a pronounced impact on the switching losses. This is because the current path during the switching transients is through the parallel capacitance, thus the external gate resistance only impacts the amount of current flowing to the device in the steady-state.

It was determined from this analysis that the combination of a 20 V driving voltage and 30 Ω external resistance would be utilized for driving the SiC BJTs and SJT in the remaining dynamic characterization testing. Accordingly, the on-state current for these devices with this driving voltage and resistor combination was approximately 600 mA, which was the current value used for the on-resistance measurements of the FSICBH057A120 BJT and SJT devices. This consistency allows for a more appropriate evaluation of the static and dynamic performance of these devices.

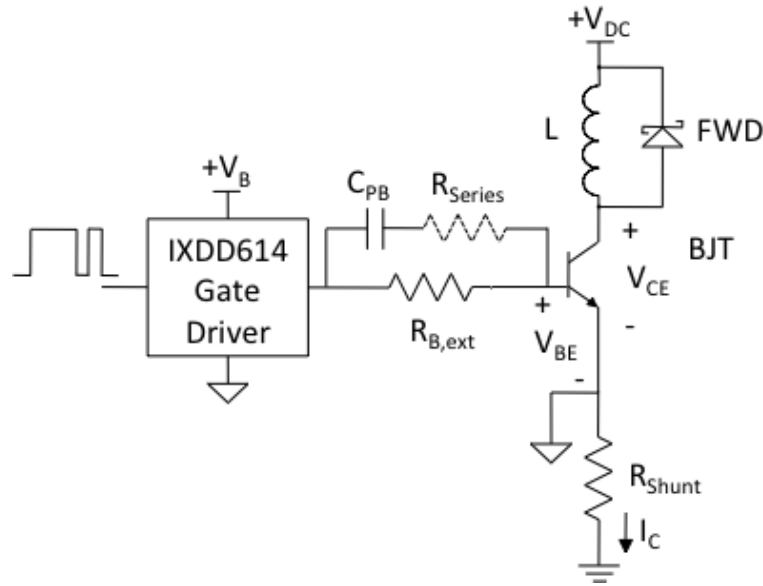


Figure 76: Schematic of the double-pulse test setup used for the dynamic characterization of the SiC BJT and SJT [C. DiMarino, Z. Chen, D. Boroyevich, R. Burgos, P. Mattavelli, “Characterization and comparison of 1.2 kV SiC power semiconductor devices,” *IEEE EPE*, pp. 1-10, Sept. 2013].

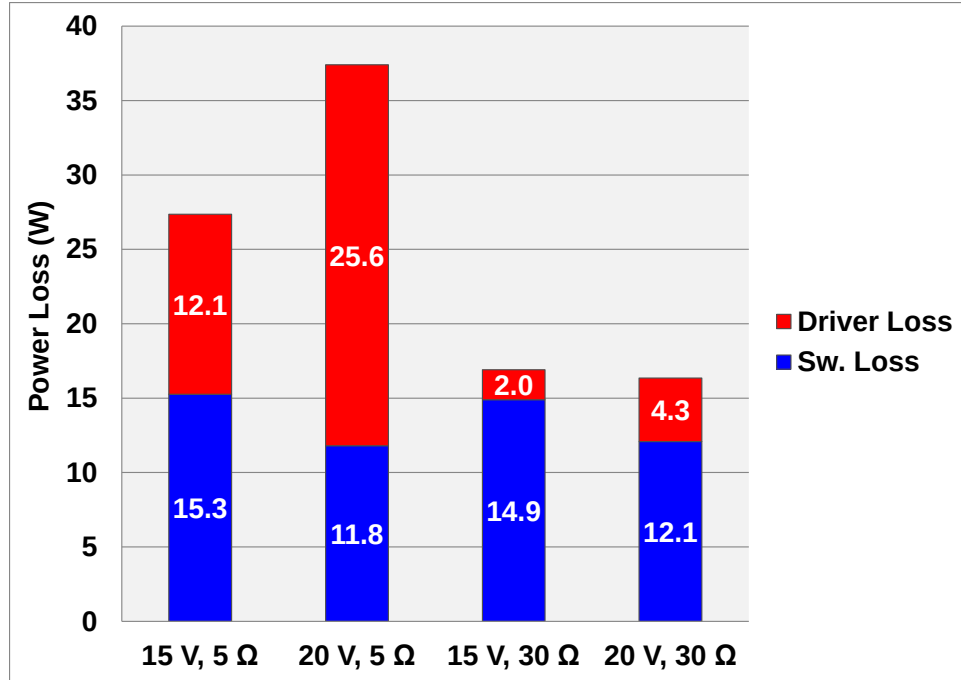


Figure 77: Switching (blue) and driving (red) power losses for different supply voltage and external gate resistance combinations from the SiC SBT DPTs conducted at 600 V, 10 A, and room temperature, assuming a switching frequency of 70 kHz and duty cycle of 50 % [C. DiMarino, Z. Chen, D. Boroyevich, R. Burgos, P. Mattavelli, “Characterization and comparison of 1.2 kV SiC power semiconductor devices,” *IEEE EPE*, pp. 1-10, Sept. 2013].

3.4.2 Switching Characteristics

The turn on and turn off waveforms for the FSICBH057A120 BJT and SBT at room temperature are shown in Figure 78, and Figure 79, respectively. For each device, the tests were conducted using a 600 V dc bus, a driving voltage of 20 V, an external base resistance of 30 Ω , and a parallel capacitance of 47 nF. A 3 Ω resistance was also put in series with the parallel capacitance for the FSICBH057A120 BJT to dampen the ringing. The switching waveforms of Cree’s C2M0080120D MOSFET are also included as a reference. The load currents for these waveforms are 20 A for the FSICBH057A120 BJT and the Cree C2M0080120D MOSFET, and 10 A for the SBT. For ease of viewing, the base-emitter

voltage waveforms for each device have been aligned. Also, the dynamic performance of Fairchild's FSICBH017A120 BJT has not been evaluated in this work. Instead, the dynamic testing results of the FSICBH057A120 BJT will be presented, as it has a current rating similar to that of the other SiC transistors being evaluated in this study.

As shown in Figure 78, for the turn on transient, GeneSiC's SJT experiences the shortest turn on delay. Also, Cree's C2M0080120D MOSFET has a shorter delay time than that of the FSICBH057A120 BJT, as well as greater di/dt and dv/dt rates. For the turn off transient, as seen by Figure 79, GeneSiC's SJT again shows the shortest delay time, and Cree's MOSFET experiences the fastest di/dt and dv/dt rates.

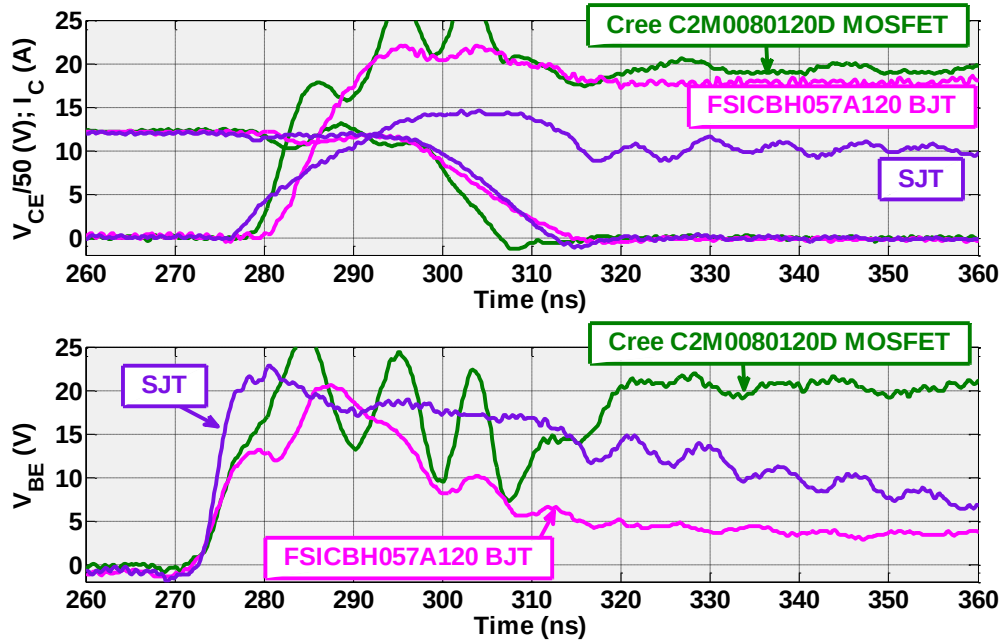


Figure 78: Turn on switching waveforms of the SiC BJT and SJT at room temperature, with a dc bus voltage of 600 V, load current of 20 A, and 10 A, respectively, using a 30 Ω external base resistance and 20 V driving voltage. The switching waveform of Cree's C2M0080120D MOSFET is included for comparison.

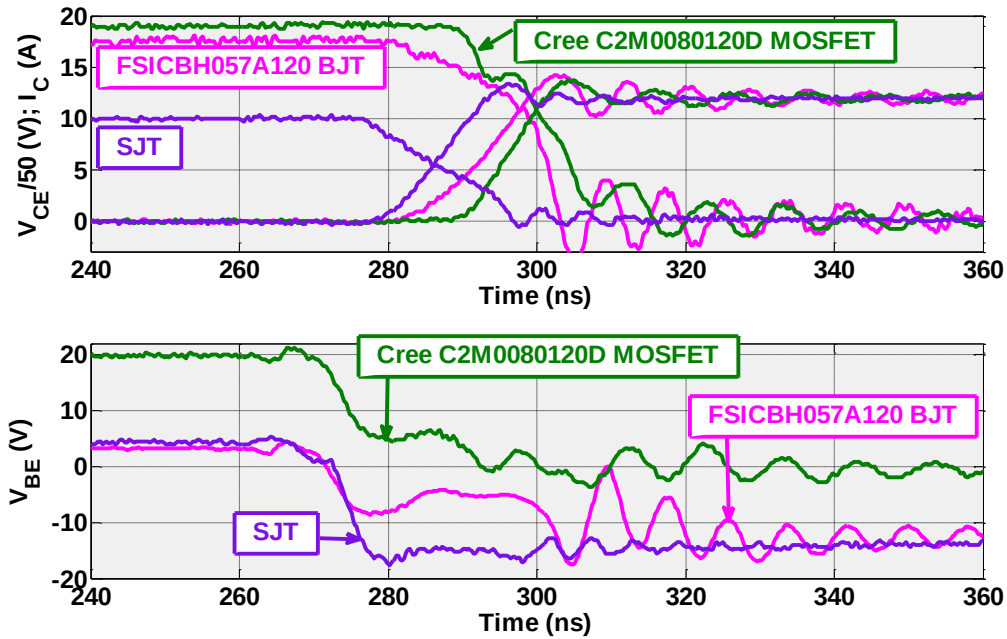


Figure 79: Turn off switching waveforms of the SiC BJT and SGT at room temperature, with a dc bus voltage of 600 V, load current of 20 A, and 10 A, respectively, using a 30 Ω external base resistance and 20 V driving voltage. The switching waveform of Cree’s C2M0080120D MOSFET is included for comparison.

The turn on, turn off, and total switching energy losses for the FSICBH057A120 BJT and SGT at room temperature are shown in Figure 80, Figure 81, and Figure 82, respectively. The switching losses of Cree’s C2M0080120D MOSFET are included as a reference. Note that the energy stored in the output capacitance of the C2M0080120D MOSFET has been added to the turn on energy, and subtracted from the turn off energy; the total switching energy, however, remains the same. As shown by the figures, these devices all experience similarly low switching losses. The SGT features higher turn on losses, but low turn off losses, which is alike to the behavior seen by MOSFETs. It should be noted that the driving losses were not taken into consideration in these plots.

Depending on the application and the driving method employed, the losses due to the driving of the SiC BJT and SJT devices may become significant.

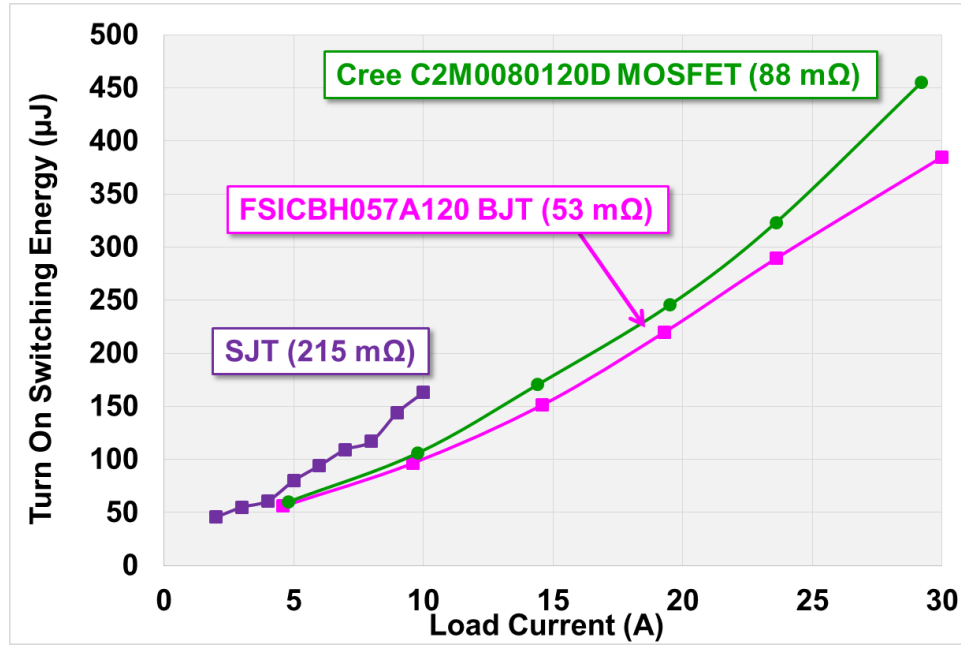


Figure 80: Turn on switching energy loss versus load current for the SiC BJT and SJT at room temperature, with a dc bus voltage of 600 V. The switching loss for Cree's C2M0080120D MOSFET is shown for comparison. The on-resistance of each device is shown in parentheses as a reference.

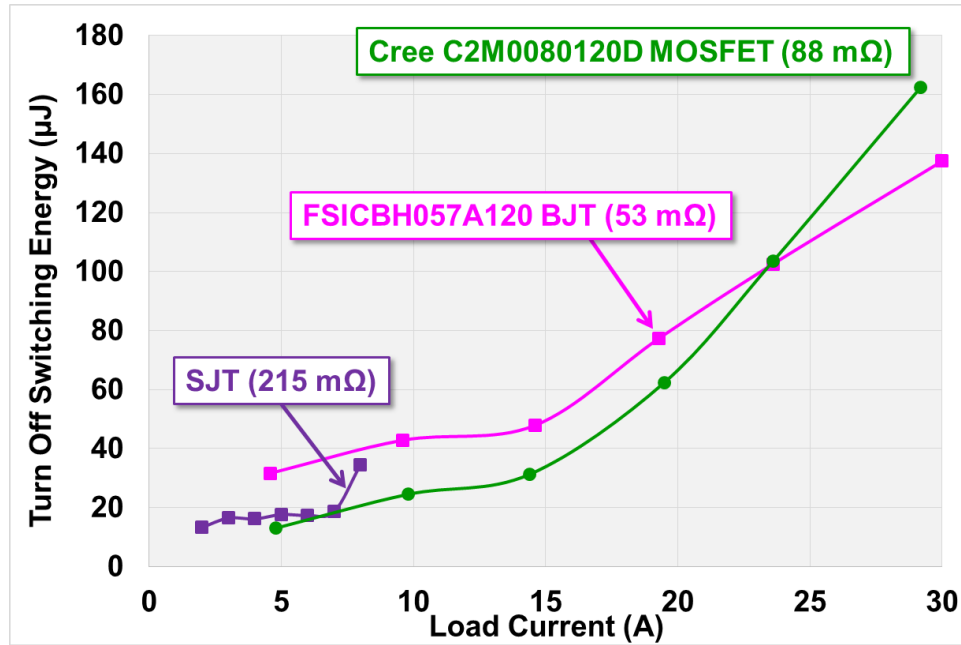


Figure 81: Turn off switching energy loss versus load current for the SiC BJT and SGT at room temperature, with a dc bus voltage of 600 V. The switching loss for Cree's C2M0080120D MOSFET is shown for comparison. The on-resistance of each device is shown in parentheses as a reference.

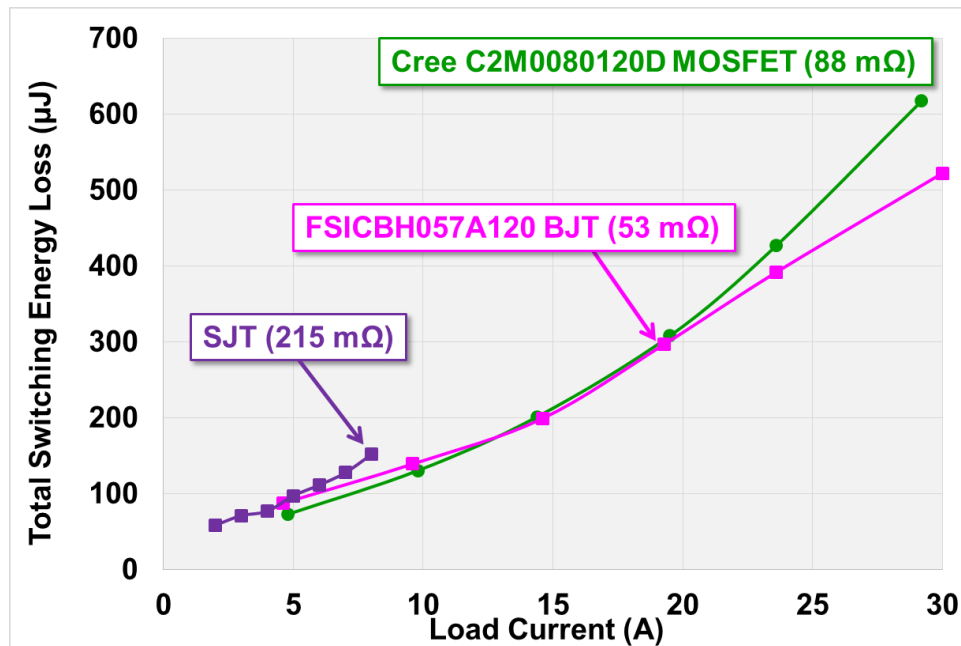


Figure 82: Total switching energy loss versus load current for the SiC BJT and SGT at room temperature, with a dc bus voltage of 600 V. The switching loss for Cree's C2M0080120D MOSFET is shown for comparison. The on-resistance of each device is shown in parentheses as a reference.

Table XI lists the turn on and turn off times, and slew rates for the SiC FSICBH057A120 BJT and GA06JT12-247 SGT. These results were measured from DPTs conducted at room temperature, 600 V dc voltage, and for load currents of 20 A for the SiC BJT and 10 A for the SiC SGT. The switching results for Cree's C2M0080120D MOSFET are repeated for comparison. As shown by the table, the SiC BJT and SGT experience faster switching than a traditional Si BJT, with results comparable to that of Cree's C2M0080120D SiC MOSFET.

Table XI: Turn on and turn off times and slew rates for the SiC BJT and SGT at room temperature, 600 V, and 20 A and 10 A, respectively, with 30 Ω external base resistance and 20 V driving voltage.

The results for Cree's C2M0080120D MOSFET are shown for comparison.

	<i>Turn On</i>				<i>Turn Off</i>			
<i>Device</i>	<i>t_{ir}</i> (ns)	<i>di/dt</i> (A/ns)	<i>t_{vf}</i> (ns)	<i>dv/dt</i> (V/ns)	<i>t_{vr}</i> (ns)	<i>dv/dt</i> (V/ns)	<i>t_{if}</i> (ns)	<i>di/dt</i> (A/ns)
Fairchild FSICBH057A120 BJT	8.8	1.8	15.4	31.3	12.5	38.5	26.1	0.61
GeneSiC GA06JT12-247 SGT	9.92	0.79	12.96	37.0	10.9	44.1	17.0	0.46
Cree C2M0080120D MOSFET	6.2	2.5	8.5	56.6	8.5	56.6	16.2	0.98

3.4.3 High Temperature Switching Behavior

The same method employed for testing the high temperature dynamic performance of the SiC MOSFETs is utilized for the SiC BJT and SJT. The switching waveforms for the SiC BJT with increasing temperature for DPTs at 600 V and 15 A are shown in Figure 83 and Figure 84, where the base-emitter voltage waveforms for various temperatures have been aligned so that the influence of temperature on the collector current and collector-emitter voltage waveforms could be clearly observed. As shown, there was a slight increase in the di/dt rate during the turn on process, which caused a minor decrease in the turn on switching energy with increased temperature. For the turn off process, Figure 84 shows an increase in the delay time as the temperature was increased, as was also seen for the SiC MOSFETs. However, as in the case of the turn on process, there was a small increase in the slew rate, resulting in a minor decrease in the turn off energy with increased temperature. The DPTs for the SJT reveal similar trends. Upon computing the switching losses, the BJT and SJT DPTs revealed a decrease in total switching energy loss from 25 °C to 200 °C of less than approximately 25 μ J at all load current values. The results of these high temperature DPTs are summarized in Table XII.

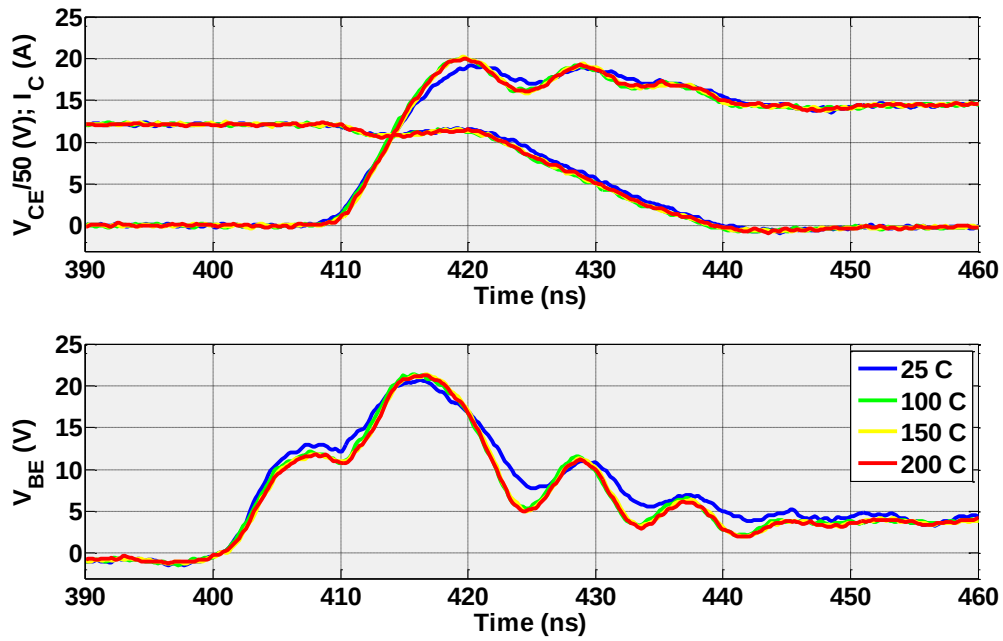


Figure 83: Turn on switching waveforms for the SiC BJT with a dc bus voltage of 600 V, a load current of 15 A, for 25 °C (blue) to 200 °C (red).

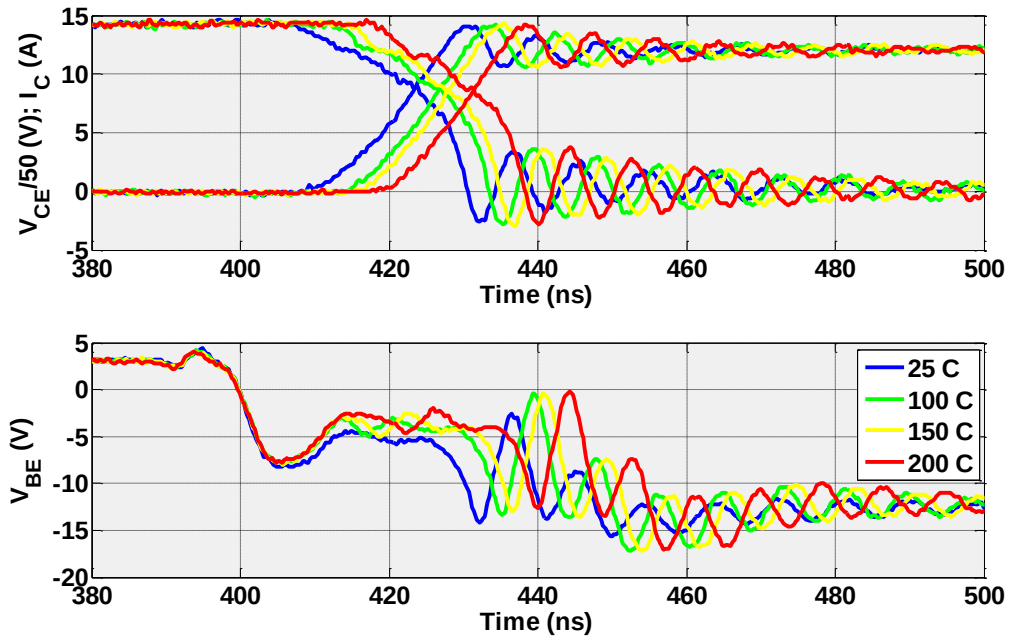


Figure 84: Turn off switching waveforms for the SiC BJT with a dc bus voltage of 600 V, a load current of 15 A, for 25 °C (blue) to 200 °C (red).

Table XII: Change in the turn on ΔE_{ON} , turn off ΔE_{OFF} , and total ΔE_{TOT} switching energies of the SiC BJT and SGT for temperatures from 25 °C to 200 °C, and a dc bus voltage of 600 V.

<i>Device</i>	ΔE_{ON}	ΔE_{OFF}	ΔE_{TOT}
Fairchild SiC BJT	↓	↓	↓ 6 %
GeneSiC SGT	↓	↓	↓ 14 %

Chapter 4 Characterization of 1.2 kV SiC Normally-On and Normally-Off JFETs

4.1 *Introduction*

In the early stages of the SiC technology, issues with the gate oxide of the SiC MOSFET hindered its progression. Consequently, many companies focused their attention on the SiC JFET, and thus the technology quickly matured. Utilizing SiC instead of Si allows for practical enhancement and depletion mode JFETs. As in the case for SiC MOSFETs, SiC JFETs allow for fast unipolar switching that is seen by devices such as the Si SJ-MOSFETs, but at higher voltage ratings of 1.2 kV or more. Moreover, unlike MOSFETs, JFETs do not have a gate oxide [76] , [77]. Thus, although advancements have been demonstrated in the gate-oxide reliability and threshold voltage instability of the SiC MOSFETs, the SiC JFETs still feature lower failure risks due to the lack of oxide processing [76] , [77].

The enhancement mode JFETs are normally-off devices, but require some dc current in the on-state, similar to a BJT [80]. These devices also have low threshold voltages, which are determined by the built-in potential of the gate-source pn junction diode [78], [79]. Therefore, a negative off-state gate voltage is typically recommended [80]. Furthermore, enhancement mode JFETs also experience manufacturing complexity due to strict dimension requirements needed to achieve normally-off behavior [78]. As a

result, precise lithography and patterning techniques are needed [77]. Due to the vertical structure, these devices also do not possess internal body diodes [80].

Alternatively, the depletion mode JFETs, which conduct current when no bias is applied to the gate, are a mature technology that has comparably relaxed processing requirements. Of course, since these devices are normally-on, added attention must be paid to the driving of these JFETs. Significant research has been done on the driving of these types of devices, with particular attention paid to the cascode configuration, where a low voltage Si MOSFET is connected in series with the JFET, and is always conducting [81]. This MOSFET allows the device to be driven as if it is normally-off [81]. The addition of this Si MOSFET adds additional voltage drop, which contributes to the on-state losses [81]. However, [76] proposed a “direct-driven JFET” concept where a separate drive is used for the Si MOSFET. This method eliminates the switching losses due to the Si MOSFET, and reduces its contribution to the conduction losses [76]. Additionally, depending on the layout of the cascode structure, the MOSFET may limit the high temperature operation of the normally-on JFET. For instance, if the JFET is mounted to the heat sink, while the MOSFET is soldered to the PCB, then there is minimal thermal coupling between the devices. In this chapter, the background of SiC JFETs will be discussed, and then the results of the high temperature static and dynamic characterization will be presented.

4.2 Background of SiC JFETs

A common structure for the SiC normally-on JFET is shown in Figure 85. This quasi-vertical structure has a lateral channel, which can conduct bidirectional current, as well as an inherent body diode. The current flow is controlled by the p-type gate and n-

type source pn junction. The lateral channel thus narrows when a negative bias is applied across the gate-source junction. Once the bias has surpassed the pinch-off voltage, the channel is pinched-off and thus no current flows and the device is off.

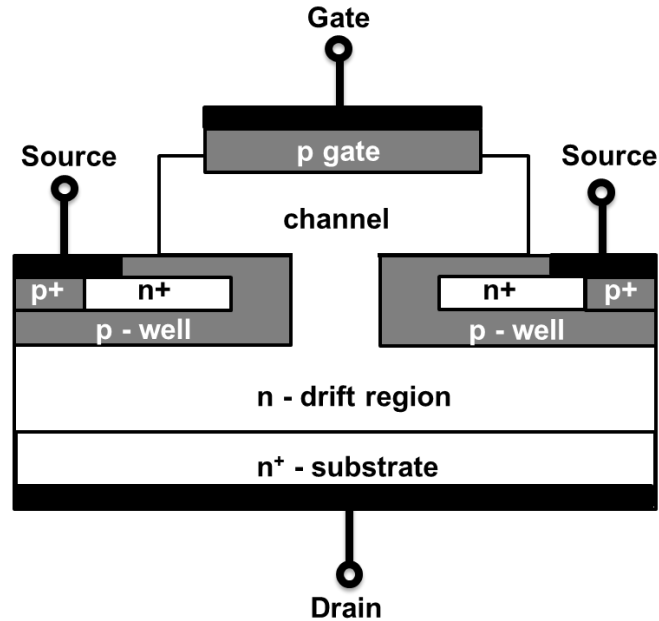


Figure 85: Quasi-vertical SiC normally-on JFET structure.

Figure 86 illustrates the structure of a common vertical SiC normally-off JFET. For this normally-off JFET, the channel is fully pinched off when zero bias is applied to the gate-source junction [79]. This is due to overlapping of the depletion regions formed by the two adjacent gate junctions [79]. Consequently, negligible current flows between the drain and source terminals when no voltage is applied to the gate and thus the device is normally-off.

Upon applying a positive gate voltage, the gate-source junction becomes forward biased, causing the depletion regions to shrink, and thus allowing for a conduction path between the drain and source [79]. Unlike the case for the SiC MOSFETs, when higher drain voltages are applied, the electric field reaches a critical value, which causes the

carriers to reach their saturated drift velocity and thus the current goes into saturation [79]. As the gate voltage is increased, the vertical conductive channel widens, allowing for a higher saturation current [79].

However, due to the pn diode at the gate-source junction (similar to that of a BJT), a gate-source bias greater than the built-in potential of the diode will not result in an increase in the current saturation value [79], as will be shown in a later section. For SiC at 25 °C, this built-in potential is approximately 3 V [79]. This high potential allows for improved enhancement mode JFETs as compared with those made of Si, which have a built-in potential of the gate-source pn junction that is around 0.6 V [80]. This low built-in potential of enhancement mode Si JFETs complicates the control design, and makes these devices impracticable [80]. The larger built-in potential of the pn junction of SiC as compared to Si is due to the wider bandgap [80]. As mentioned previously, SemiSouth was the first company to commercialize the SiC JFET, and provided both enhancement and depletion mode devices rated at 1.2 kV for a variety of current levels. Although SemiSouth is no longer in existence, its SJEP120R100 SiC normally-off JFET will be evaluated in this work to represent the enhancement mode SiC JFET technology.

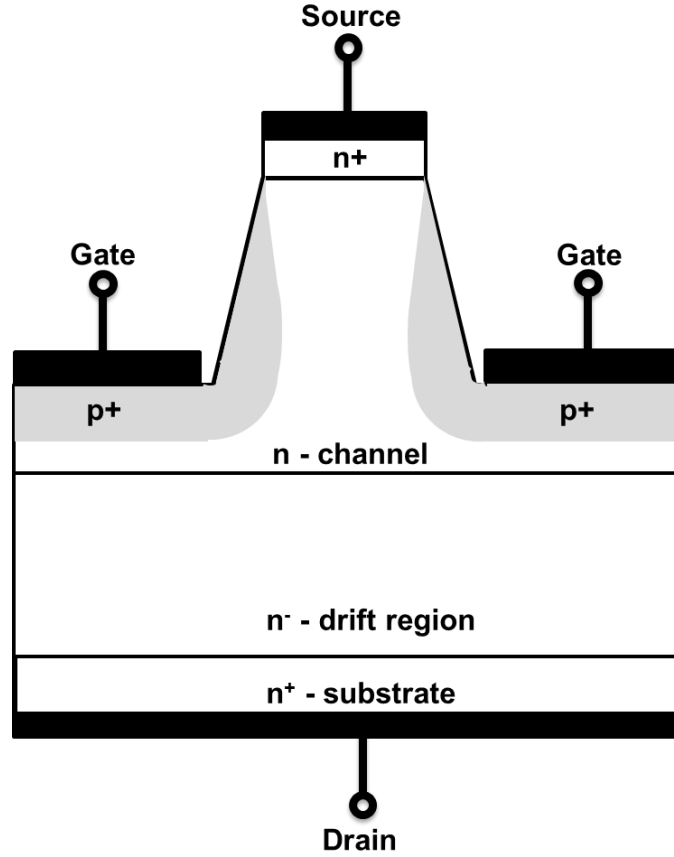


Figure 86: SiC normally-off JFET structure.

The SiC normally-on and normally-off JFETs that will be assessed in this work are shown in Table XIII, where all of the devices are rated at 1.2 kV and are in TO-247 package. This table lists the device manufacturer, part number, continuous current and operation temperature ratings as listed in their respective datasheets [83]-[85], and their die areas normalized to that of Cree's C2M0080120D 2nd Generation Z-FET.

Normalizing the die areas shows the sizes of the devices relative to one another, which is significant because the size of the device directly relates to the on-state resistance and parasitic capacitance. As the device size is reduced, the on-state resistance increases, thereby resulting in higher conduction losses. On the contrary, smaller devices feature lower capacitances, which results in faster switching and thus reduced dynamic losses.

Table XIII: 1.2 kV SiC normally-on and normally-off JFETs under study.

<i>Mfg.</i>	<i>Device</i>	<i>I_{D,Cont}</i>	<i>T_{JMax}</i>	<i>A_{Norm to Cree}</i> <i>C2M0080120D</i>
Infineon Technologies	IJW120R100T1	26 A (25 °C); 18 A (100 °C); 10 A (150 °C)	175 °C	0.97
	IJW120R070T1	36 A (25 °C); 26 A (100 °C); 15 A (150 °C)	175 °C	1.29
SemiSouth Laboratories	SJEP120R100	17 A (100 °C); 10 A (150 °C)	150 °C	0.43

4.3 Static Characterization of the 1.2 kV SiC JFETs

In the following subsections, the methods and measurement results for the static characterization of the SiC normally-on and normally-off JFETs listed in Table XIII will be presented. The parameters include: blocking capability, threshold voltage, transfer characteristics and transconductance, output characteristics and on-resistance, body diode I-V characteristics, internal gate resistance, and junction capacitances. Each parameter, with the exception of the internal gate resistance and parasitic capacitances, was measured from 25 °C to 200 °C in order to assess the high temperature capabilities of the devices under study.

4.3.1 Static Characterization Methods

The static characterization was performed using a Tektronix 371b curve tracer, and Agilent 4294A impedance analyzer. For the Tektronix 371b curve tracer, four-terminal (also known as Kelvin) sensing was employed to ensure measurement accuracy. An oscilloscope was also utilized for the threshold voltage measurements to obtain improved resolution. A hotplate and thermocouple were used for heating and temperature

sensing. Measurements were taken in 25 °C increments from 25 °C to 200 °C. Once the desired steady-state temperature was reached, measurements were taken quickly in order to avoid the self-heating of the devices.

4.3.2 Blocking Capability

The curve tracer was used to measure the leakage current of the normally-on and normally-off JFETs at increasing temperature. For the SemiSouth normally-off JFET, this was done in the same manner as in the case of the SiC MOSFETs, where the gate and source terminals of the device under test were shorted such that the gate-source voltage remained at 0 V and thus the device was off. Next, the drain current of the device was measured as the drain-source voltage of the device was increased. At a blocking voltage of 1200 V, the normally-off JFET showed a leakage current below 10 μ A at 25 °C. Since the resolution of the 371b curve tracer is 10 μ A/div at this power level, a specific leakage current value could not be accurately determined. However, as the temperature increased, so did the leakage current. At 200 °C, the leakage current for a blocking voltage of 1200 V increased to 550 μ A. Similar leakage currents for the SiC normally-off JFET were reported in [86], and were accredited to the reduction in the threshold voltage, which enhanced the drain induced barrier lowering effect.

For the normally-on JFET, since it conducts current when no bias is applied to the gate, a negative potential needed to be utilized. A gate-source voltage of -19 V was applied to the JFET since this is the recommended off-state driving voltage [83], [84]. With this bias, a blocking voltage of 1200 V could be applied, and the corresponding leakage current could be measured. Under these conditions, the normally-on JFETs showed leakage currents well below 10 μ A, even at high temperature.

4.3.3 Threshold Voltage

The threshold voltage is the gate-source voltage needed for current to start flowing through the channel of the device. In this study, the threshold voltage was taken to be the gate-source voltage at which the drain current reaches 40 mA for the SemiSouth normally-off JFET (same condition used in the device datasheet [85]), and 1 mA for the Infineon normally-on JFET. For the normally-off JFET, the gate and drain terminals of the device were shorted such that the gate-source and drain-source voltages are equal, as was done for the SiC MOSFETs. The curve tracer was then put into high voltage mode such that fine current resolution could be achieved. However, in this mode, the minimum voltage resolution is 50 V/div, which is more than an order of magnitude higher than the threshold voltages of these devices. Consequently, an oscilloscope was used to measure the gate-source (or equivalently the drain-source) voltage at which 40 mA of drain current was reached. For the normally-on JFET, 600 V was applied across the drain-source terminals, and then the gate-source voltage was adjusted such that a drain current was approximately 1 mA. This corresponding gate-source voltage was taken to be the pinch-off voltage of the device.

Figure 87 and Figure 88 show the threshold voltage for the normally-off JFET, and the pinch-off voltage for the IJW120R100T1 normally-on JFET, respectively. The threshold voltage of Cree's C2M0080120D MOSFET is included in Figure 87 for comparison. As shown in Figure 87, the threshold voltage of the normally-off JFET is much lower than that of the SiC MOSFET, even for a larger drain current of 40 mA as opposed to 1 mA. This is due to the device structure and material properties. It can also be seen from this figure that the threshold voltage of the normally-off JFET has a small

negative temperature coefficient. These threshold voltage measurements are consistent with those reported in [85] and [86]. Consequently, when using the SiC normally-off JFET in applications, a negative off-state gate-source voltage is recommended [80]. As shown in Figure 88, the pinch-off voltage of the SiC normally-on JFET has a small negative temperature coefficient, decreasing by less than 6 % at 200 °C. Since this pinch-off voltage has sufficient margin to the recommended applied off-state gate driving voltage of -19 V, the device features good noise immunity. The pinch-off voltage results are only shown for the IJW120R100T1 JFET since, according to their datasheets [83] and [84], both of the normally-on JFETs have similar pinch-off voltages.

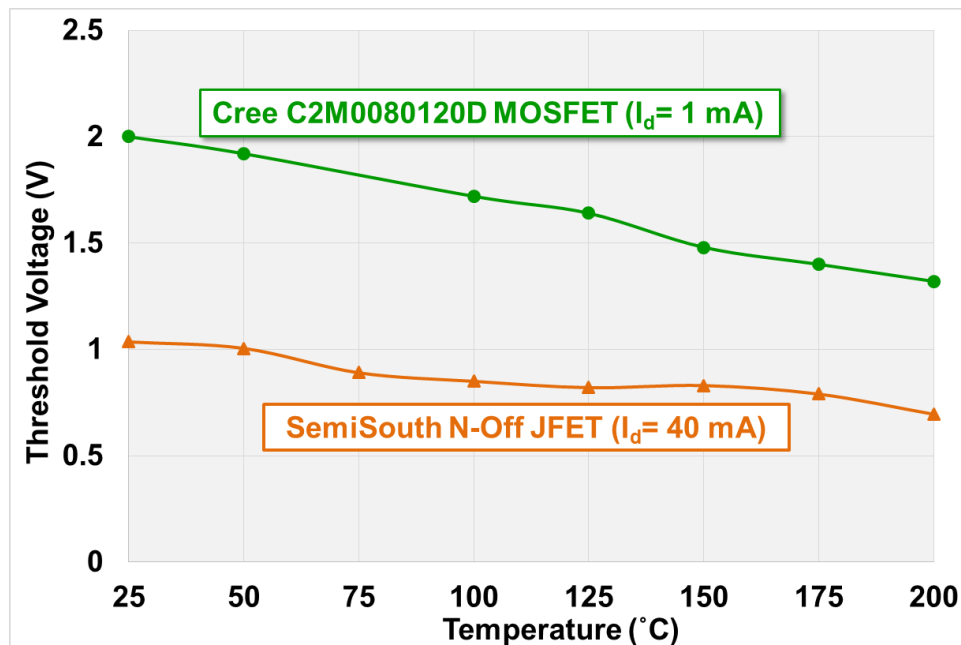


Figure 87: Plot of threshold voltage versus temperature for SemiSouth's SiC normally-off JFET with a drain current of 40 mA and the gate-drain terminals shorted. The threshold voltage curve of Cree's C2M0800120D is shown for comparison.

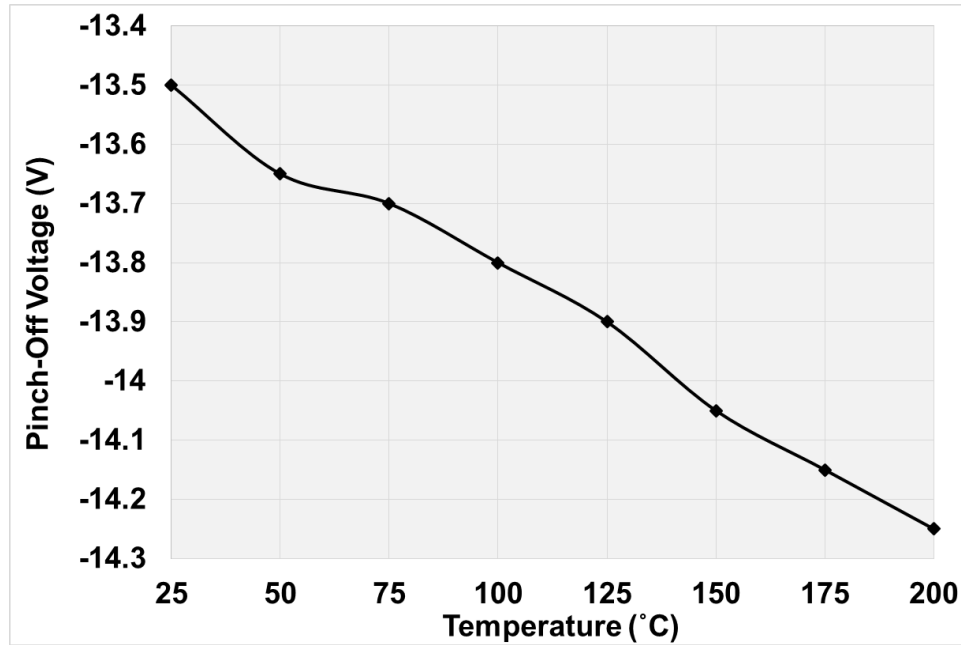


Figure 88: Pinch-off voltage versus temperature for Infineon's IJW120R100T1 normally-on JFET with a drain-source voltage of 600 V.

4.3.4 Transfer Characteristics/Transconductance

Figure 89 and Figure 90 show the transfer curves of Infineon's normally-on JFETs and SemiSouth's normally-off JFET, respectively, for temperatures from 25 °C to 200 °C. For SemiSouth's normally-off JFET, it can be seen from Figure 90 that, while it experiences high gain at room temperature, it has a large negative temperature coefficient. In effect, from 25 °C to 200 °C, the transconductance (taken at a drain-source voltage of 5 V) of the normally-off JFET decreases by more than half. Although Infineon's normally-on JFET has a lower transconductance than the normally-off JFET at room temperature, its decrease with temperature is more modest. At 200 °C, the transconductance (taken at a drain-source voltage of 30 V) decreases by less than thirty percent. Similar temperature dependencies of the transconductances for the normally-off and normally-on JFETs were seen in [87] and [88], respectively.

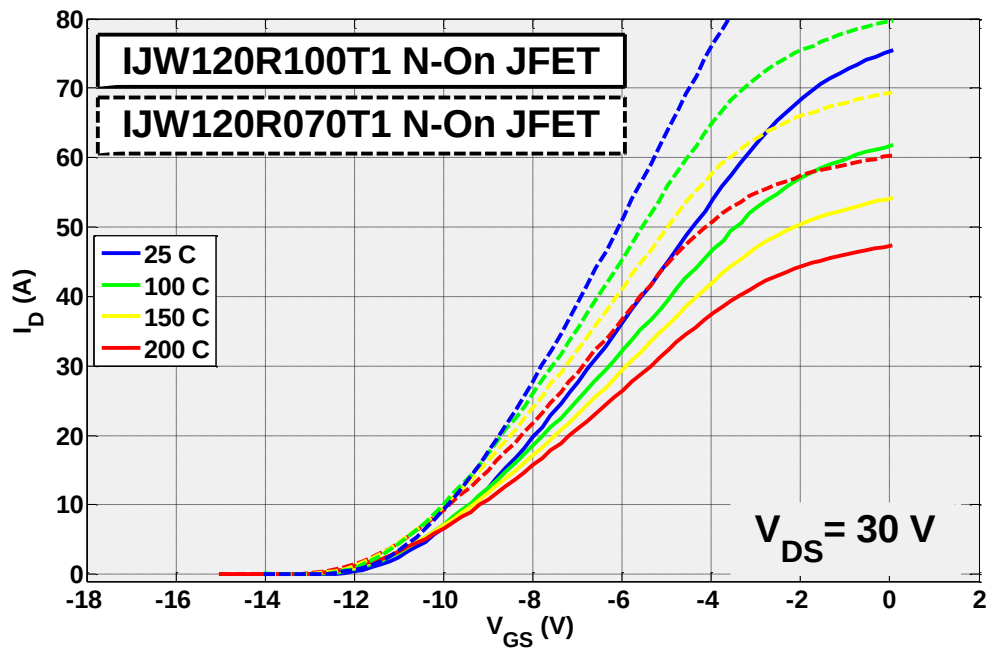


Figure 89: Transfer curves for Infineon's SiC normally-on JFET at a drain-source voltage of 30 V for temperatures from 25 °C (blue) to 200 °C (red).

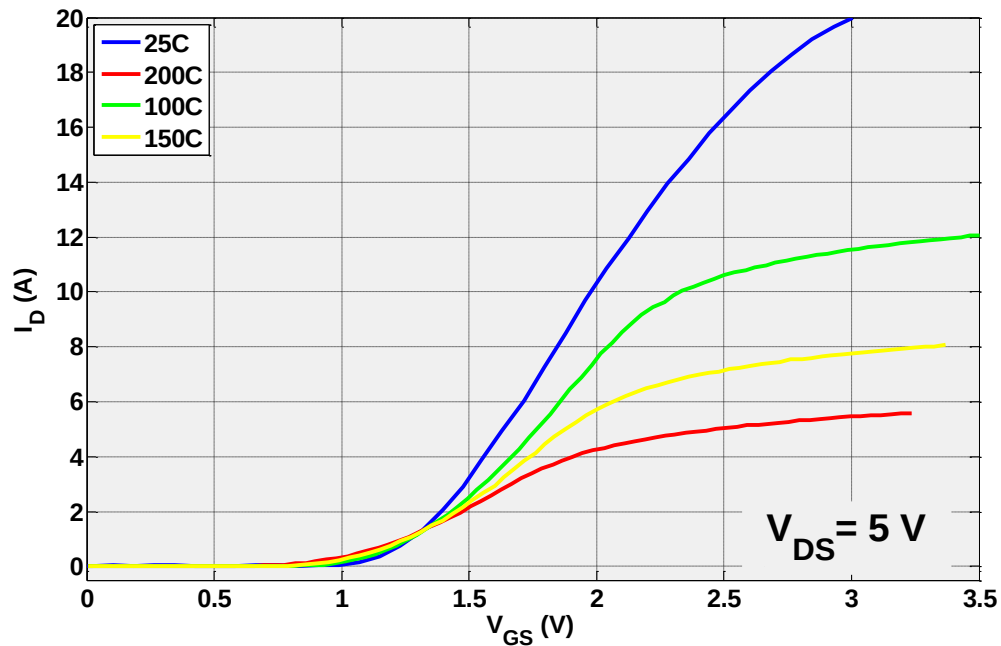


Figure 90: Transfer curves for SemiSouth's SiC normally-off JFET at a drain-source voltage of 5 V for temperatures from 25 °C (blue) to 200 °C (red).

4.3.5 Output Characteristics/On-Resistance

The I-V curves of the normally-on and normally-off JFETs were measured using a curve tracer and four-terminal sensing for temperatures from 25 °C to 200 °C. Figure 91 shows the I-V curves of the IJW120R100T1 normally-on JFET for temperatures of 25 °C and 200 °C and gate-source voltages of -8 V to 0 V with 2 V steps. This comparison demonstrates the temperature dependency of the on-state characteristics of the SiC normally-on JFET. As can be seen from the figure, the SiC normally-on JFET, just like the SiC MOSFET, does not experience a clear saturation region. However, unlike that of the SiC MOSFET, there is a significant change in the I-V curve as the temperature is increased.

Figure 92 shows the I-V curves for SemiSouth's normally-off JFET for temperatures of 25 °C and 200 °C and gate-source voltages of 1.3 V to 3.5 V with 500 mV steps. As was mentioned previously, when the gate bias surpasses the built-in potential of the pn diode at the gate-source junction, which is approximately 3 V for SiC at room temperature, no further increase in the saturation current is experienced [79]. Thus, as expected, there is almost no difference between the 3 V and 3.5 V gate-source voltage curves in Figure 92. Moreover, it can be observed that, unlike the SiC normally-on JFETs and SiC MOSFETs, the normally-off JFET has a clear saturation region. Additionally, this Figure 92 shows the large temperature dependency of the static characteristics of the normally-off JFET.

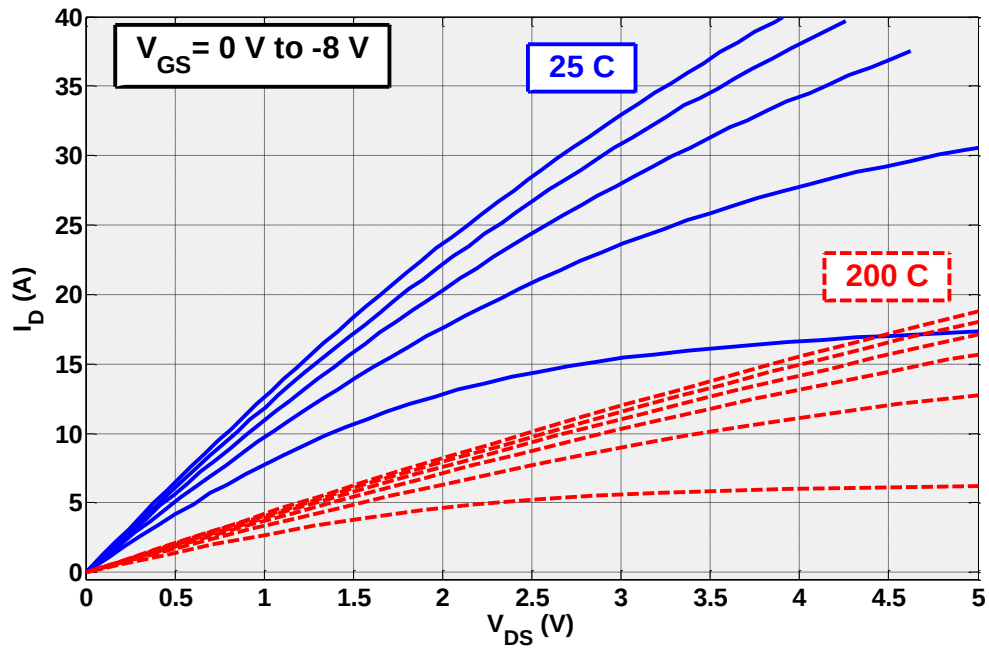


Figure 91: I-V curves of Infineon's SiC normally-on JFET for temperatures from 25 °C (blue solid curves) to 200 °C (red dashed curves), and gate-source voltages of -8 V to 0 V with 2 V steps.

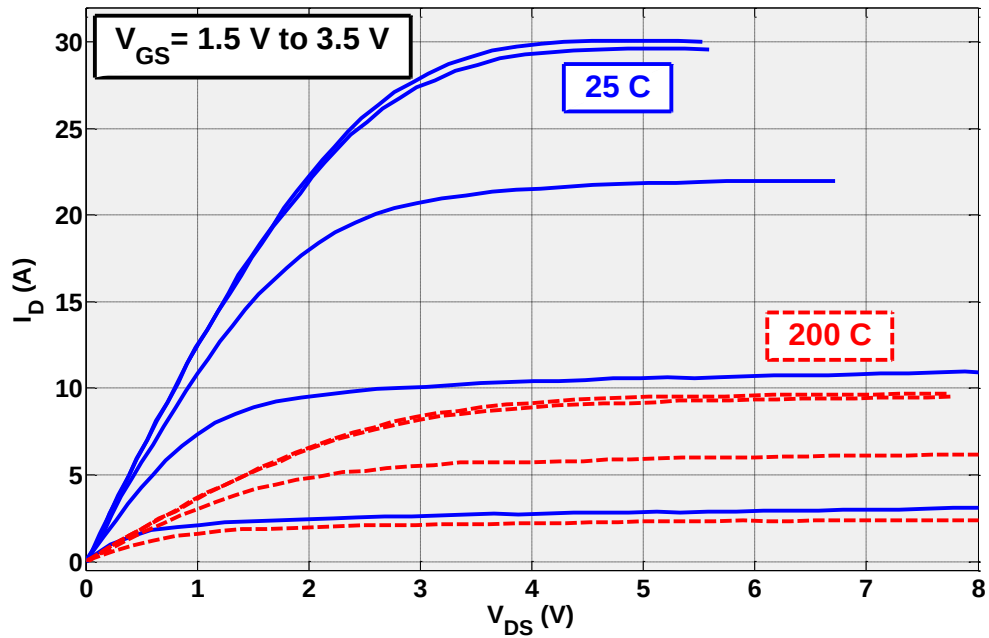


Figure 92: I-V curves of SemiSouth's SiC normally-off JFET for temperatures from 25 °C (blue solid curves) to 200 °C (red dashed curves), and gate-source voltages of 1.5 V to 3.5 V with 500 mV steps.

From the I-V curves, the on-resistances of the SiC normally-on and normally-off JFETs were calculated. Figure 93 shows the on-resistance versus temperature curves for these devices, with the on-resistance curve of Cree's C2M0080120D MOSFET shown as a reference. The on-resistances were measured at the drain currents listed in parentheses in the figure, and at gate-source voltages of 0 V for the normally-on JFETs, and 3 V for the normally-off JFET. This gate-source voltage value was selected for the normally-off JFET because, as was shown in the I-V curve of the device (Figure 92), gate voltages greater than 3 V do not result in a noticeable increase in the slope in the linear region and thus will not produce a reduction in the on-resistance.

As shown by Figure 93, while at low temperatures the majority of the devices experience nearly identical losses, as the temperature is increased, the normally-off JFET displays a noticeable increase in on-resistance. It can also be observed from this figure that the IJW120R070T1 normally-on JFET has the lowest on-resistance. However, this is due to its larger size. As mentioned previously, a smaller device will result in a higher on-resistance for a given blocking voltage. Consequently, it is important to look at the specific on-resistances of the devices. In this case, this figure was obtained by multiplying the measured on-resistance values by the die area of the device.

Figure 94 shows the measured specific on-resistance versus temperature. The drain current used for the measurements is shown in parentheses, and Cree's C2M0080120D SiC MOSFET is included for comparison. Figure 94 shows that the two normally-on JFETs have similar specific on-resistances, as would be expected. It can also be seen that their values are comparable to that of Cree's C2M0080120D SiC MOSFET, though these normally-on JFETs experience a larger increase in resistance as the

temperature is increased beyond approximately 100 °C. Figure 94 also reveals that SemiSouth's normally-off JFET possesses the lowest specific on-resistance of these devices, though it is the most temperature-sensitive, increasing by 340 % from 25 °C to 200 °C. This can be attributed to strong phonon scattering, which reduces the carrier mobility as the temperature is increased, which is due to channel saturation effects imposed by the maximum width requirement necessary to achieve a reliable normally-off behavior [89].

Figure 95a and Figure 95b show the measured specific on-resistance versus drain current at 25 °C and 200 °C, respectively, for the normally-on and normally-off JFETs. Cree's C2M0080120D MOSFET is also included as a reference. As shown by Figure 95a, the normally-on JFETs and Cree C2M0080120D MOSFET experience nearly identical specific on-resistances at all measured drain current values at room temperature. However, the normally-on JFETs feature a greater increase in specific-on resistance as the temperature is increased from 25 °C to 200 °C than the Cree MOSFET. Figure 95a also shows that, at room temperature, the changes in on-resistance with increasing drain current are comparable for these devices. At 200 °C, however, the on-resistance of the normally-off JFET shows a notable increase for drain currents greater than approximately 8 A (Figure 95b). This is due to the decrease in the saturation current that the normally-off JFET experiences. These measured on-resistances are in good agreement with those listed in the datasheets [83]-[85].

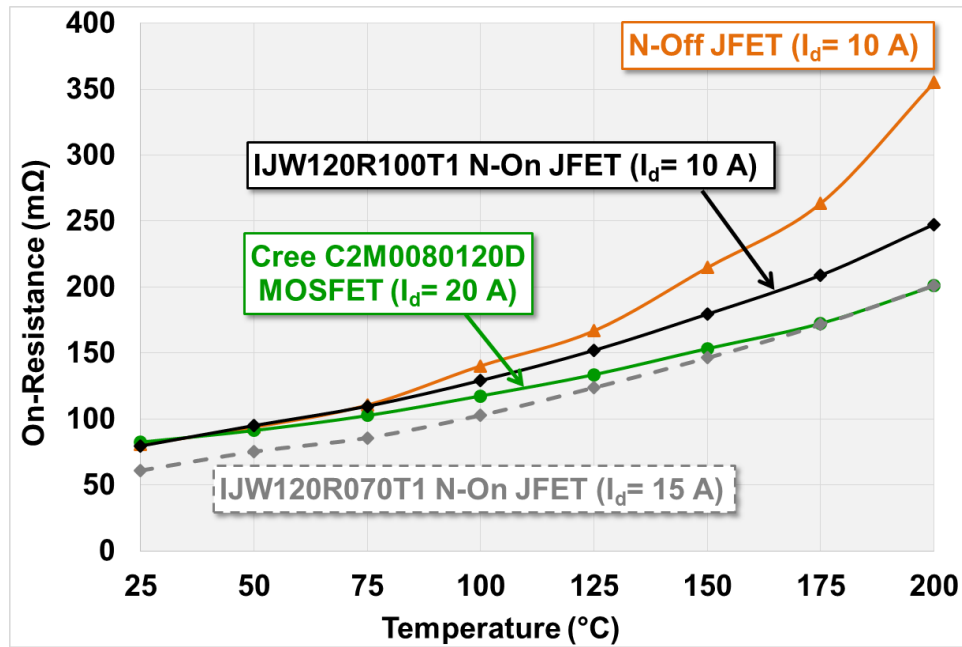


Figure 93: On-resistance versus temperature curves for the SiC normally-on and normally-off JFETs at gate-source voltages of 0 V and 3 V, respectively, and the drain currents specified in parentheses.

The on-resistance curve of Cree's C2M0080120D MOSFET is shown for comparison.

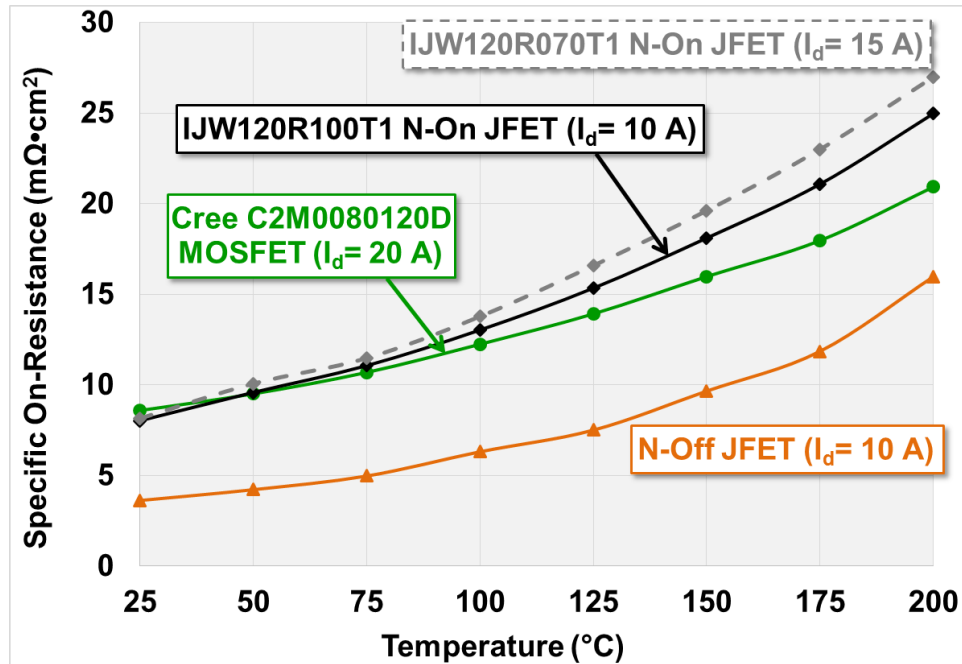
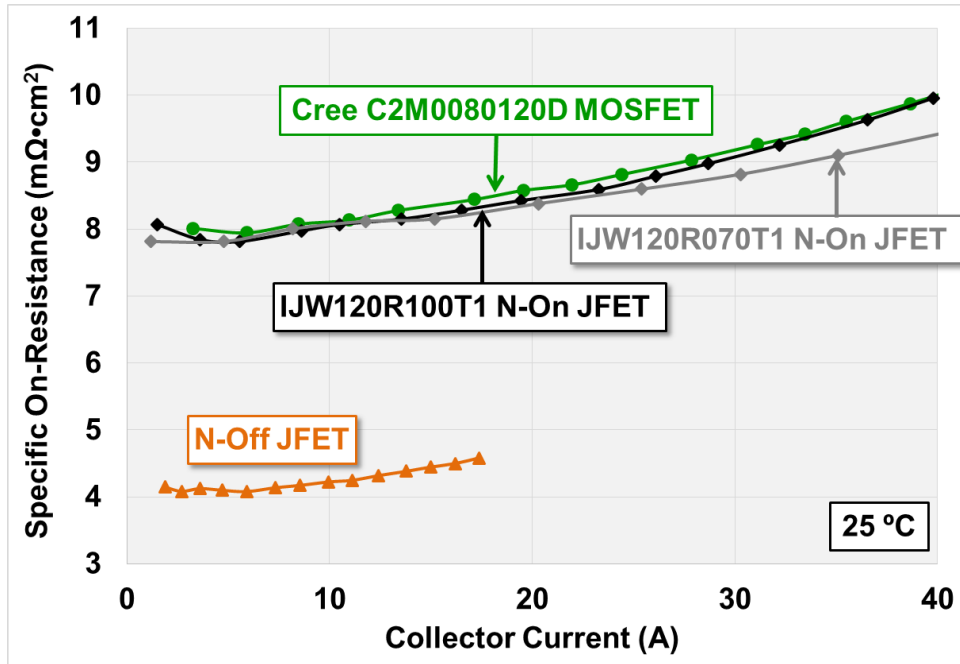
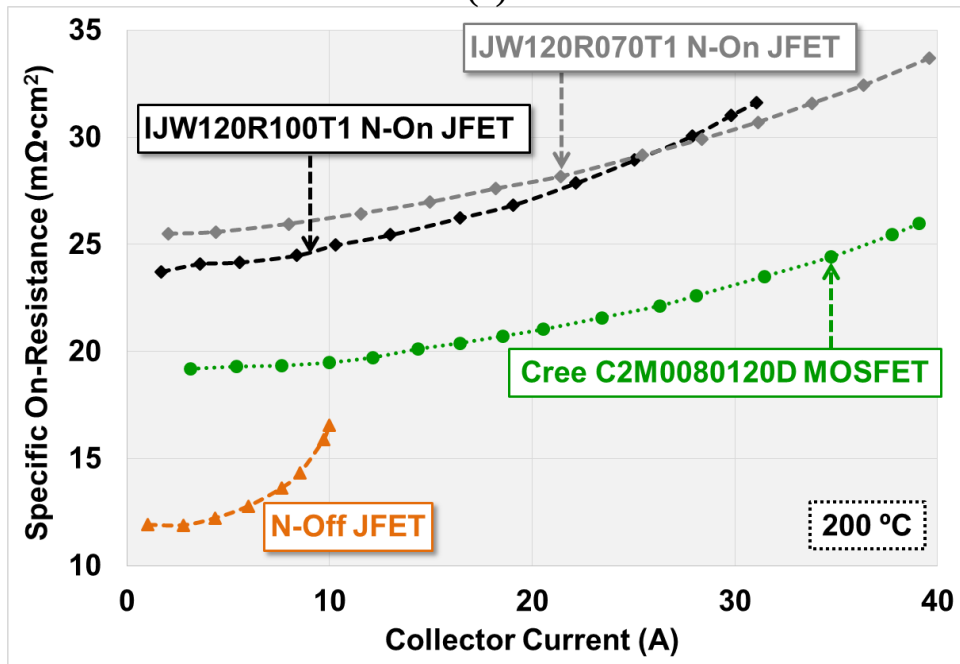


Figure 94: Specific on-resistance (using die area) versus temperature curves for the SiC normally-on and normally-off JFETs at gate-source voltages of 0 V and 3 V, respectively, and the drain currents specified in parentheses. The specific on-resistance curve of Cree's C2M0080120D MOSFET is shown for comparison.



(a)



(b)

Figure 95: Specific on-resistance (using die area) versus drain current curves for the SiC normally-on and normally-off JFETs at (a) 25 °C, and (b) 200 °C. The specific on-resistance of Cree's C2M0080120D is shown for comparison.

4.3.6 Body Diode I-V Characteristics

While the normally-on JFETs have an intrinsic body diode, the normally-off enhancement mode JFETs do not [80]. Consequently, this section will focus on the normally-on JFETs. The body diode I-V curves were determined using a curve tracer and four-terminal measurement. A negative gate-source voltage that is sufficient to ensure that the JFET is off was first applied. Then the voltage across the source and drain of the device was increased, and the current flowing from the source to the drain through the body diode was sensed. The body diode I-V curves for the IJW120R070T1 and IJW120R100T1 SiC normally-on JFETs at 25 °C and 200 °C are shown in Figure 96 for gate-source voltages of -19 V and -25 V. These two gate-source voltages were selected because the dynamic performance of the device will be evaluated for these two off-state voltages.

As can be seen from the figure, the SiC normally-on JFETs experience a reduction in the body diode forward turn on voltage as the temperature is increased, as was also seen for the body diodes of the SiC MOSFETs. It can also be observed that the body diode of the IJW120R070T1 JFET features a steeper slope than that of the IJW120R100T1 JFET.

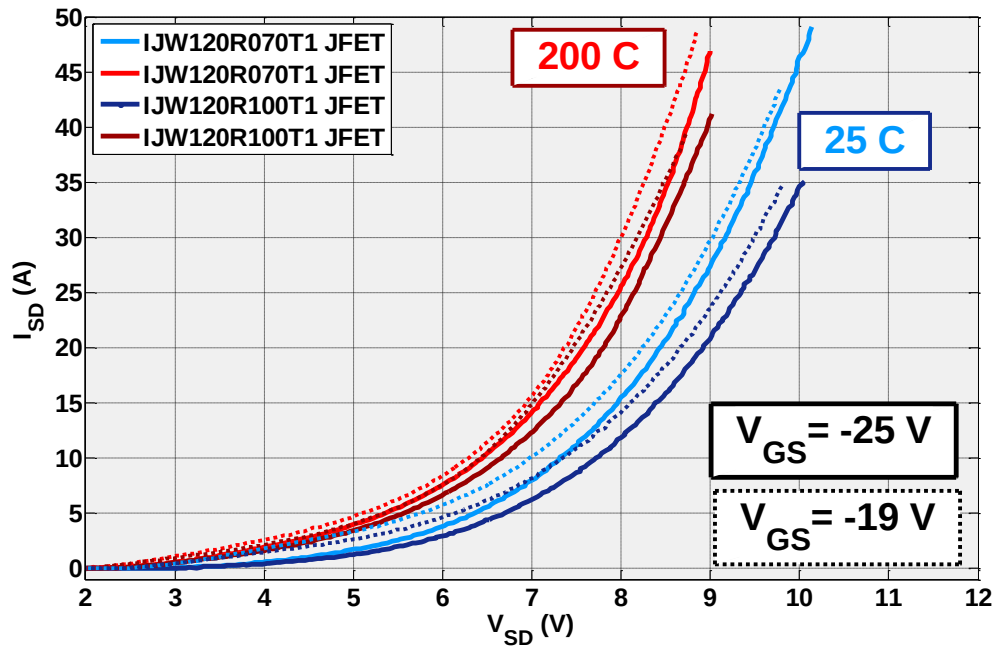


Figure 96: Body diode I-V curves for Infineon's SiC normally-on JFETs at 25 °C (red) and 200 °C (blue) for gate-source voltages of -19 V (dashed curves) and -25 V (solid curves).

4.3.7 Internal Gate Resistance

The internal gate resistances of the IJW120R100T1 SiC normally-on JFET and SJEP120R100 SiC normally-off JFET were determined using the impedance analyzer measuring across the gate and source terminals with the drain floating (Figure 12). Measurements were taken at a frequency of 1 MHz. The resulting values are presented in Table XIV. It can be seen that Infineon's IJW120R100T1 normally-on JFET has a low internal gate resistance, which is comparable to that of GE's SiC MOSFET, and is eight times less than that of SemiSouth's normally-off JFET. Note that the datasheet of the SJEP120R100 normally-off JFET reports a lower intrinsic gate resistance, though this is for the case when the drain and source terminals are shorted [85]. With the drain-source

shorted, the impedance analyzer measured a lower gate resistance for the normally-off JFET of approximately 8 Ω .

Table XIV: Internal gate resistances of the SiC JFETs.

<i>Device</i>	<i>R_{G,int}</i>
Infineon Normally-On JFET (IJW120R100T1)	2.6 Ω
SemiSouth Normally-Off JFET (SJEP120R100)	21.0 Ω

4.3.8 Junction Capacitances

The parasitic capacitances of the normally-off JFET were measured in the same manner as was done for the SiC MOSFETs (Figure 13). The capacitances for the normally-on JFETs were extracted from their respective datasheets [83] and [84]. The resulting capacitance versus voltage curves at room temperature are shown in Figure 97, Figure 98, and Figure 99, where Cree's C2M0080120D is included as a reference. As shown in these figures, the normally-off JFET features the lowest input and output capacitances, but the largest Miller capacitance. This larger Miller capacitance of the normally-off JFET is due to increased coupling between the gate and drain regions [76], [77]. When comparing the JFETs, it can be seen that, in general, the devices with the smaller die areas have lower capacitances.

If the measured capacitances are divided by the die area, then the specific capacitances of the devices can be plotted to verify this assumption. As shown by Figure 100, Figure 101, and Figure 102, the distribution in specific capacitances is much

narrower than that of the regular capacitance measurements. In fact, the specific capacitance curves for the two normally-on JFETs are almost completely overlapped. It can also be observed that the normally-off JFET possess slightly larger specific capacitances than the normally-on JFETs.

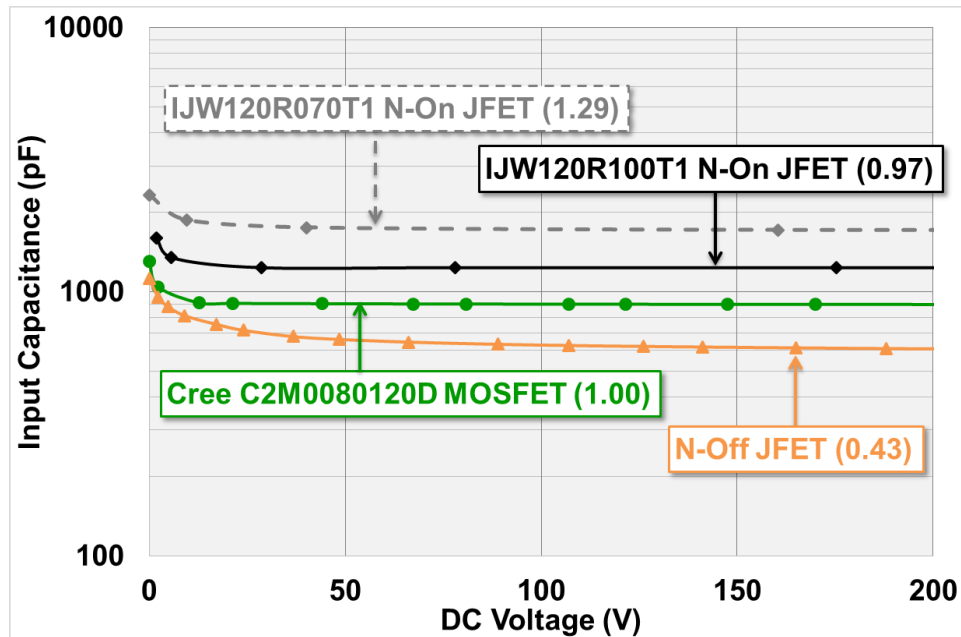


Figure 97: Input capacitance versus voltage curves for the SiC normally-on and normally-off JFETs measured at 1 MHz and room temperature. The capacitance curve of Cree’s C2M0080120D is included for comparison.

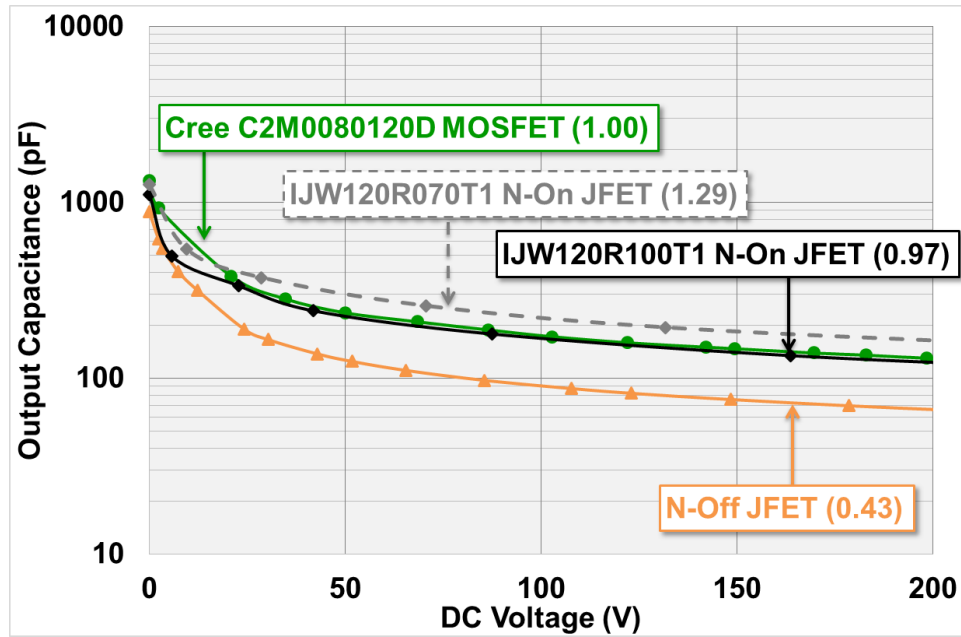


Figure 98: Output capacitance versus voltage curves for the SiC normally-on and normally-off JFETs measured at 1 MHz and room temperature. The capacitance curve of Cree's C2M0080120D is included for comparison.

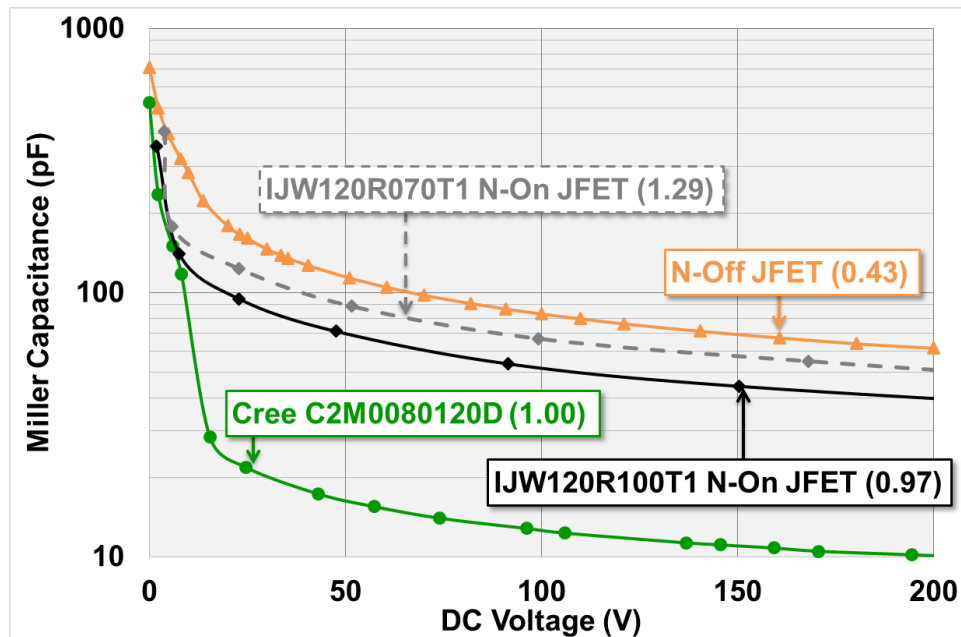


Figure 99: Miller capacitance versus voltage curves for the SiC normally-on and normally-off JFETs measured at 1 MHz and room temperature. The capacitance curve of Cree's C2M0080120D is included for comparison.

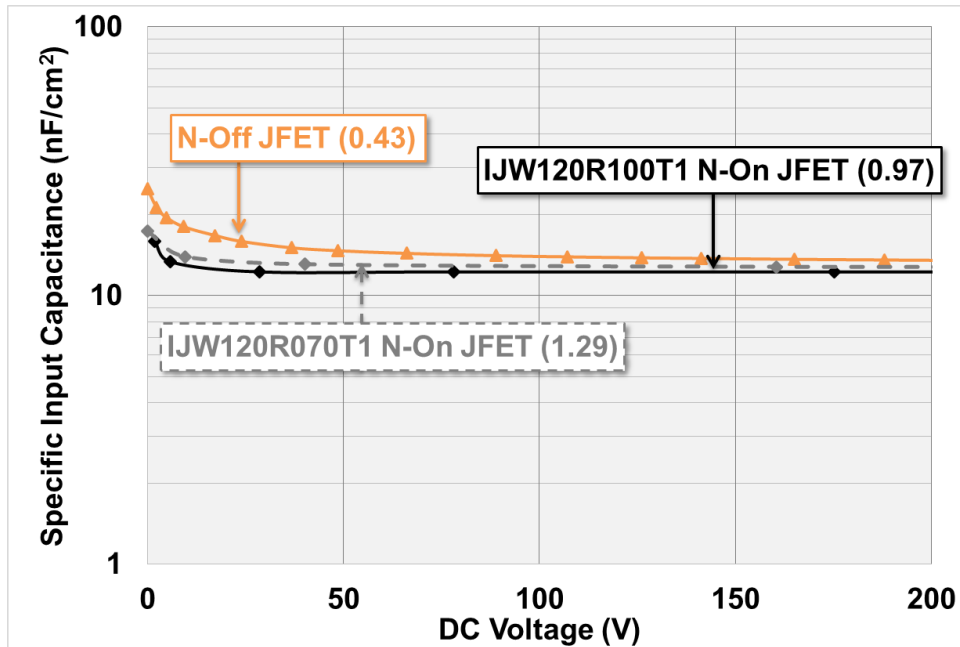


Figure 100: Specific input capacitance versus voltage curves for the SiC normally-on and normally-off JFETs measured at 1 MHz and room temperature.

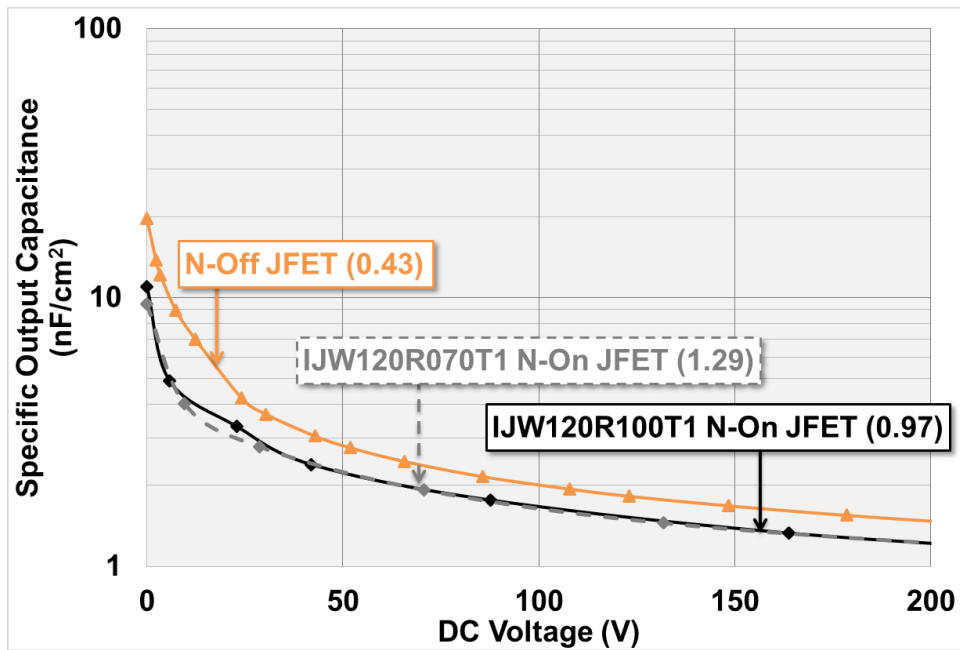


Figure 101: Specific output capacitance versus voltage curves for the SiC normally-on and normally-off JFETs measured at 1 MHz and room temperature.

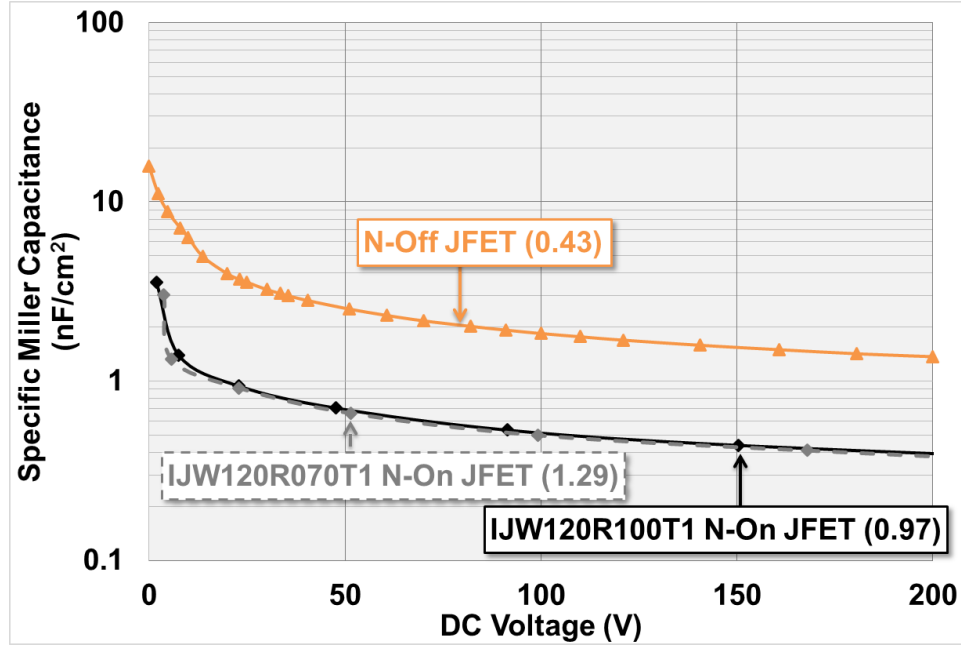


Figure 102: Specific Miller capacitance versus voltage curves for the SiC normally-on and normally-off JFETs measured at 1 MHz and room temperature.

4.4 Dynamic Characterization of the 1.2 kV SiC JFETs

In the following subsections, the driving and measurement methods used for the dynamic characterization of the SiC normally-on and normally-off JFETs will be presented. The switching energy losses of each device for different load currents and temperatures will also be shown. A comparison of the dynamic performance of the devices will then be provided.

4.4.1 Dynamic Characterization Methods

The driving scheme used for the SiC normally-on JFET DPTs is depicted in Figure 103, which was based on that employed in [51] and [90]. The notable changes compared to the driving of the SiC MOSFETs are that the $+V_G$ is now grounded while the ground pin of the IXDD614 gate driver is held at a negative potential $-V_G$, and a

parallel resistor-capacitor-diode (R-C-D) network has been added. Other than these differences, the DPT PCB layout for the normally-on JFET was identical to that used for the other devices in this study.

The R-C-D network allows the normally-on JFET to be driven at gate-source voltages that are more negative than the reverse breakdown voltage of the gate diode. This is due to the large value of the resistor R, which prevents sizeable avalanche currents from flowing to the gate when the JFET is in the off state. The capacitor absorbs the potential difference between the gate drive supply voltage and the gate-source terminal voltage. It also forward biases the gate-source junction of the device, thereby increasing the switching speed. In this study, a 5 k Ω resistor, 10 nF capacitor, and three paralleled 60 V, 1 A Schottky diodes (PMEG6010) with low forward voltages were used for the R-C-D network [51], along with a 3.3 Ω external gate resistance. A 3.3 Ω external gate resistance was experimentally determined to be optimal, as it resulted in the lowest switching losses while not experiencing substantial ringing.

The benefit of driving the device beyond its breakdown voltage is a decrease in switching energy. Figure 104 compares the switching energy losses of the device, with and without the R-C-D network, against load current for 600 V and an external gate resistance of 3.3 Ω . Without the R-C-D network, the gate source voltage must be kept more positive than the breakdown voltage. Consequently, for this comparison, -19 V was chosen as supply voltage for the gate drive circuit. It can be seen that using the R-C-D network to drive the normally-on JFET with -25 V yielded a great reduction in switching loss when compared to the case without the R-C-D network. For instance, at 20 A, the

total switching energy loss decreased by 104 μJ . This was primarily due to a significant decline in the turn on switching energy.

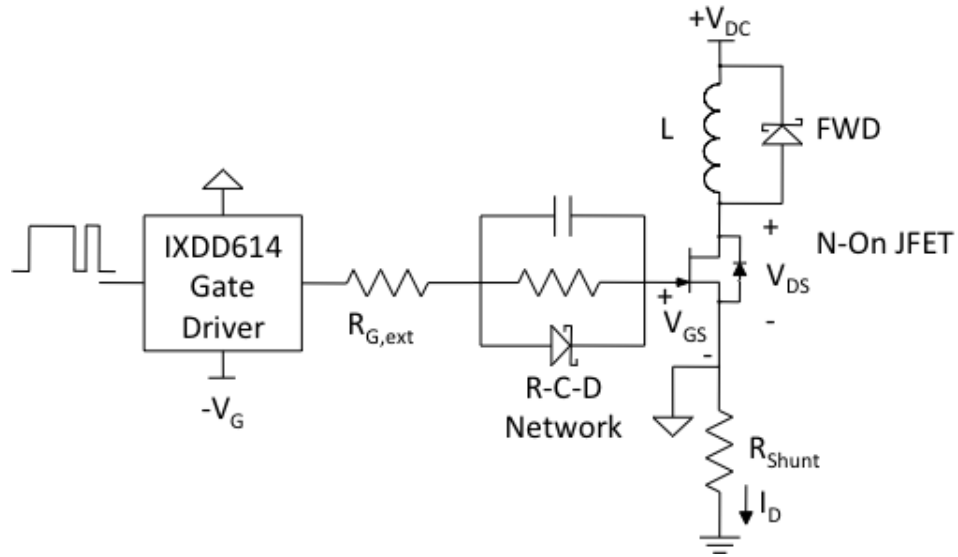


Figure 103: Schematic of the double-pulse test setup used for the dynamic characterization of the SiC normally-on JFET [C. DiMarino, Z. Chen, D. Boroyevich, R. Burgos, P. Mattavelli, “Characterization and comparison of 1.2 kV SiC power semiconductor devices,” *IEEE EPE*, pp. 1-10, Sept. 2013].

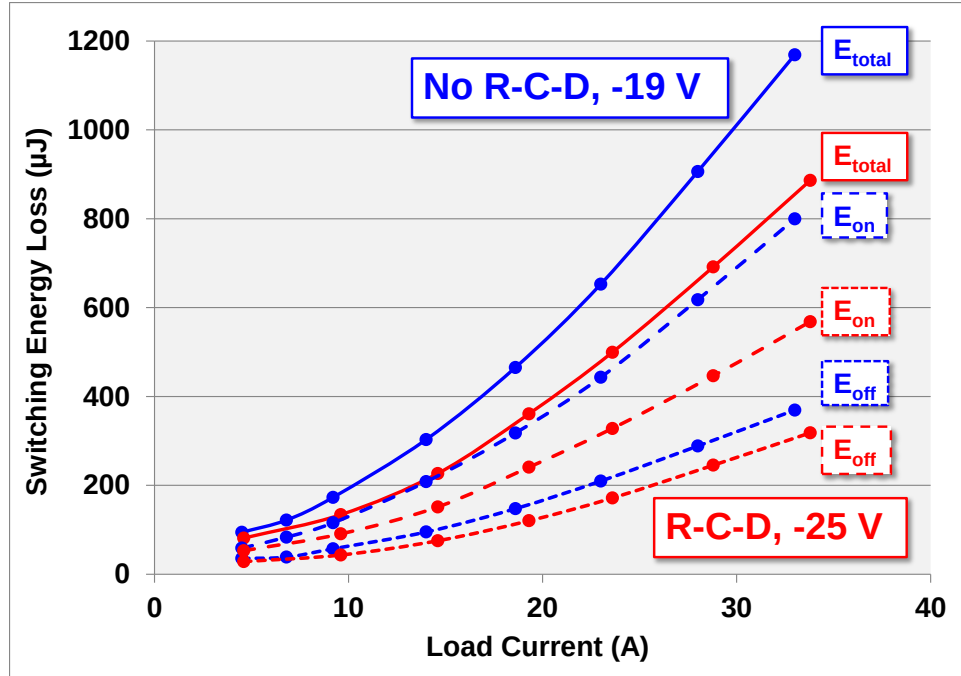


Figure 104: Comparison of the turn on (dashed curves), turn off (dotted curves), and total (solid curves) switching energies versus load current for the IJW120R100T1 normally-on JFET with (red curves) and without (blue curves) the R-C-D network for 600 V and an external gate resistance of 3.3 Ω [C. DiMarino, Z. Chen, D. Boroyevich, R. Burgos, P. Mattavelli, “Characterization and comparison of 1.2 kV SiC power semiconductor devices,” *IEEE EPE*, pp. 1-10, Sept. 2013].

The driving method used for SemiSouth’s normally-off JFET is the same as that utilized for the SiC BJT and SJT (Figure 76), which was reported in the preceding chapter. As mentioned previously, the normally-off enhancement mode JFET structure has a pn diode across the gate-source junction, just as a BJT. Consequently, when the gate-source bias exceeds the built-in potential of this junction, which is 3 V for SiC at 25 °C, current will flow from the gate to the source. As a result, although the normally-off JFET is still considered to be a voltage-controlled device, it has a gate current in the on-state [80]. For this reason, a capacitor was put in parallel to the external gate resistance. In this way, a larger external gate resistance could be used to limit the gate current and

thus the driving losses during the on-state operation, while also allowing for fast turn on and turn off speeds.

4.4.2 Switching Characteristics

The turn on and turn off waveforms for the IJW120R100T1 normally-on JFET and SJEP120R100 normally-off JFET at room temperature are shown in Figure 105 and Figure 106, respectively. For each device, the tests were conducted using a 600 V dc bus and 20 A load current. For the normally-on JFET, the R-C-D network was utilized such that a gate voltage of -25 V could be applied during the off-state without damaging the device. An external gate resistance of 3.3 Ω was also used. For the normally-off JFET, a driving voltage of 20 V, an external base resistance of 30 Ω , and a parallel capacitance of 47 nF (same as for the BJT and SJT). A 3 Ω resistance was also put in series with the parallel capacitance for the normally-off JFET to dampen the ringing. The switching waveforms of Cree's C2M0080120D MOSFET are also included as a reference. For ease of viewing, the gate-source voltage waveforms were aligned. The dynamic performance of Infineon's IJW120R070T1 normally-on JFET has not been evaluated in this work. Instead, the dynamic testing results of the IJW120R100T1 normally-on JFET will be presented, as it has a current rating and die size that are more similar to that of the other SiC transistors being evaluated in this study.

As shown in Figure 105, for the turn on transient, the normally-off JFET has the shortest delay time. Also, the IJW120R100T1 normally-on JFET and C2M0080120D MOSFET have virtually identical delay times, and di/dt and dv/dt rates. For the turn off transient, as seen by Figure 106, it can again be observed that the normally-off JFET has

the shortest delay time, and the normally-on JFET and C2M0080120D MOSFET again have very similar switching waveforms.

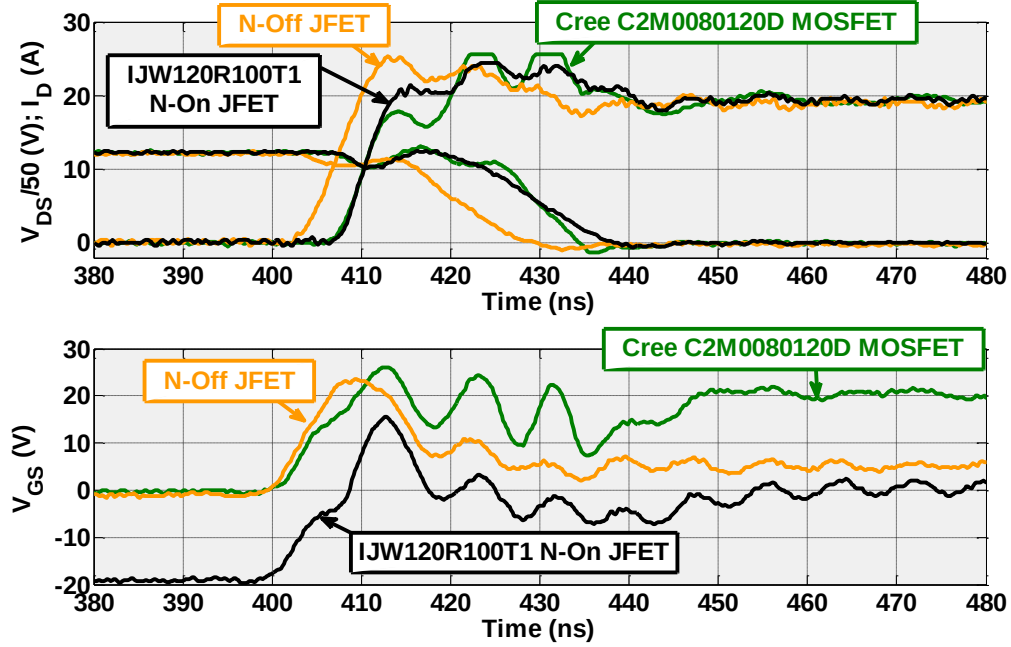


Figure 105: Turn on switching waveforms of the SiC normally-on and normally-off JFETs at room temperature, with a dc bus voltage of 600 V, load current of 20 A. The switching waveform of Cree's C2M0080120D MOSFET is included for comparison.

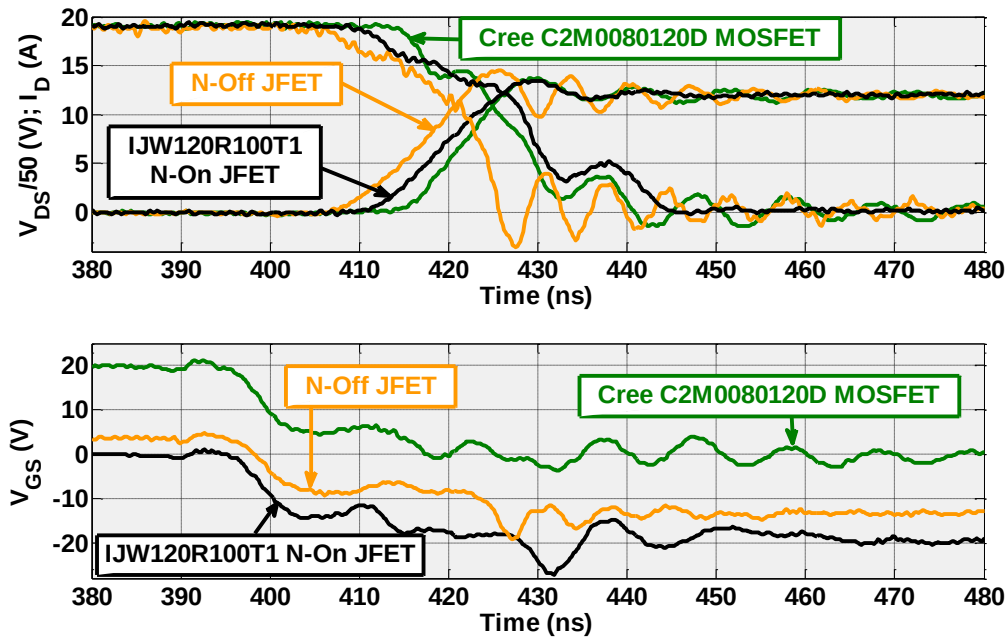


Figure 106: Turn off switching waveforms of the SiC normally-on and normally-off JFETs at room temperature, with a dc bus voltage of 600 V, load current of 20 A. The switching waveform of Cree’s C2M0080120D MOSFET is included for comparison.

Figure 107, Figure 108, and Figure 109 show the turn on, turn off, and total switching energies, respectively, for the IJW120R100T1 normally-on and SemiSouth normally-off JFETs. The losses for the C2M0080120D MOSFET are also shown for comparison. The energy stored in the output capacitances of these devices has been subtracted from their respective turn off energies, and added to their turn on energies. As shown in Figure 107, when the R-C-D network was used for the driving of the normally-on JFET such that an off-state driving voltage of -25 V could be utilized, the turn on switching energy losses were comparable to that of Cree’s C2M0080120D MOSFET. This figure also shows that the normally-off JFET has the lowest turn on switching energy losses. Figure 108 shows that the JFETs experience higher turn off losses than that of the C2M0080120D MOSFET.

Figure 109 reveals that, while these devices all experience similar losses at drain currents of approximately 15 A and below at room temperature, at higher load currents the normally-off JFET demonstrates the lowest switching energy losses. However, with the driving method utilized in this study, the normally-off JFET experienced greater driving losses than the MOSFET or normally-on JFET, which may become significant depending on the application.

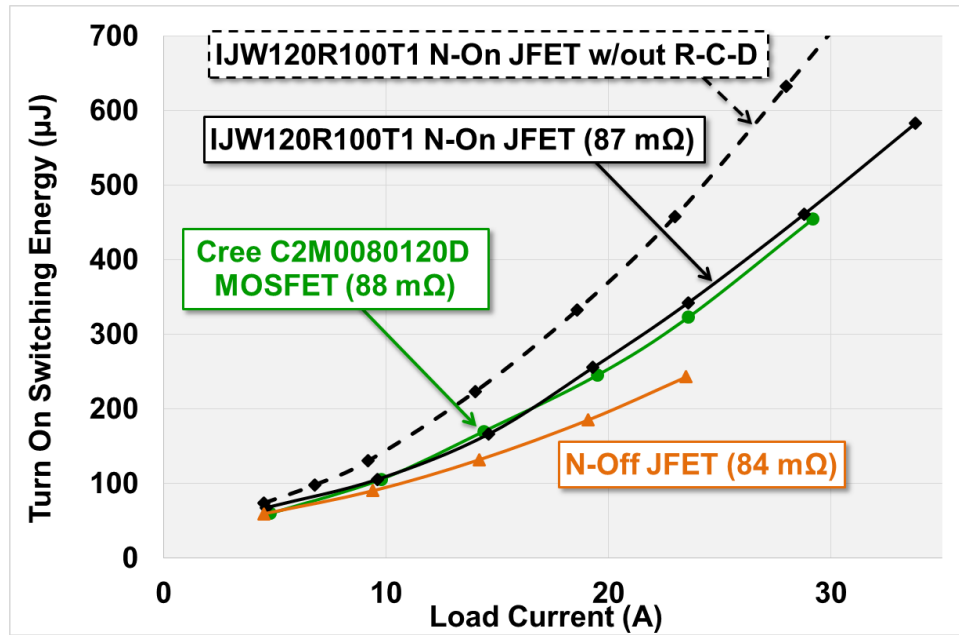


Figure 107: Turn on switching energy loss versus load current for the SiC normally-on and normally-off JFETs at room temperature, with a dc bus voltage of 600 V. The switching loss for Cree's C2M0080120D MOSFET is shown for comparison. The on-resistance of each device is shown in parentheses as a reference.

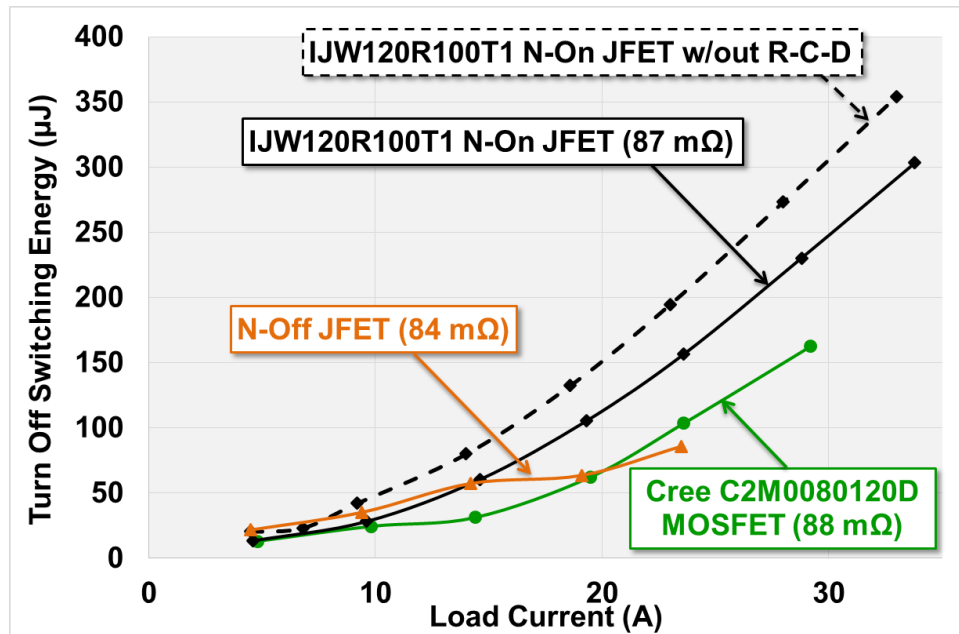


Figure 108: Turn off switching energy loss versus load current for the SiC normally-on and normally-off JFETs at room temperature, with a dc bus voltage of 600 V. The switching loss for Cree's C2M0080120D MOSFET is shown for comparison. The on-resistance of each device is shown in parentheses as a reference.

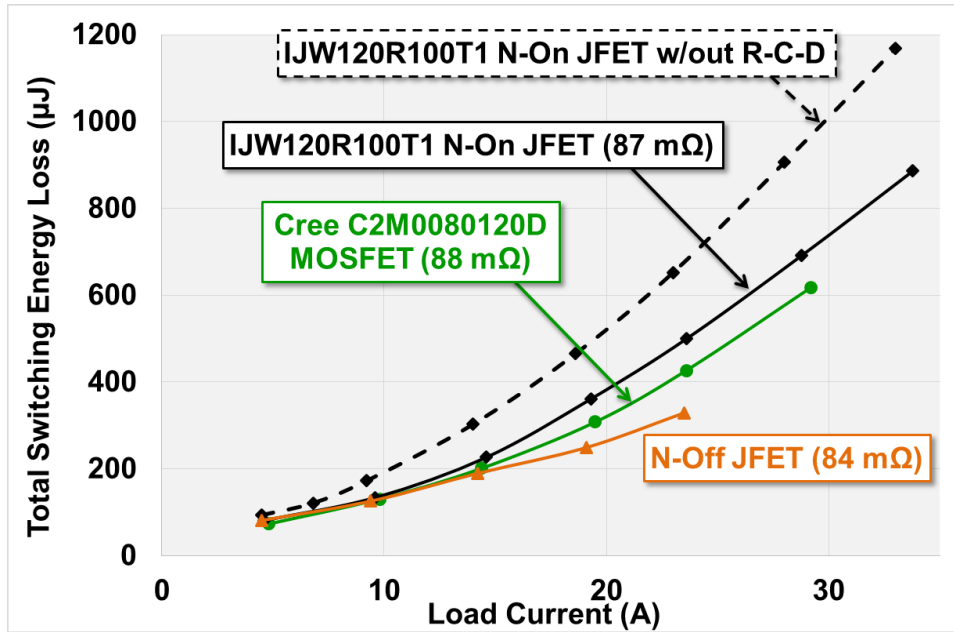


Figure 109: Total switching energy loss versus load current for the SiC normally-on and normally-off JFETs at room temperature, with a dc bus voltage of 600 V. The switching loss for Cree’s C2M0080120D MOSFET is shown for comparison. The on-resistance of each device is shown in parentheses as a reference.

Table XV lists the turn on and turn off times, and slew rates for the SiC IJW120R100T1 normally-on and SJEP120R100 normally-off JFETs. These results were measured from DPTs conducted at room temperature, 600 V dc voltage, and for load currents of 20 A, with the R-C-D network used for driving the normally-on JFET. The switching results for Cree’s C2M0080120D MOSFET are shown for comparison. As shown by the table, the SiC normally-on and normally-off JFETs feature similarly fast switching speeds, which are comparable to that of Cree’s C2M0080120D SiC MOSFET.

Table XV: Turn on and turn off times and slew rates for the SiC normally-on and normally-off JFETs at room temperature, 600 V, and 20 A. The results for Cree’s C2M0080120D MOSFET are shown for comparison.

	<i>Turn On</i>				<i>Turn Off</i>			
<i>Device</i>	t_{ir} (ns)	di/dt (A/ns)	t_{vf} (ns)	dv/dt (V/ns)	t_{vr} (ns)	dv/dt (V/ns)	t_{if} (ns)	di/dt (A/ns)
Infineon IJW120R100T1 normally-on JFET	4.5	3.5	14.2	33.7	11.2	42.9	21.0	0.75
SemiSouth SJEP120R100 normally-off JFET	5.6	2.8	11.7	41.1	11.0	43.5	17.9	0.88
Cree C2M0080120D MOSFET	6.2	2.5	8.5	56.6	8.5	56.6	16.2	0.98

4.4.3 High Temperature Switching Behavior

The same method employed for testing the high temperature dynamic performance of the SiC MOSFETs is utilized for the normally-on and normally-off JFETs. The switching waveforms for the IJW120R100T1 normally-on JFET with increasing temperature for DPTs at 600 V and 10 A are shown in Figure 110 and Figure 111, where the gate-source voltage waveforms for various temperatures have been aligned so that the influence of temperature on the drain current and drain-source voltage waveforms could be clearly observed. As shown, there was essentially no change in the turn on switching waveform of the normally-on JFET as the temperature was increased.

For the turn off process, however, Figure 111 shows that there was an increase in the di/dt and dv/dt rates as the temperature was increased. This resulted in a decrease in the turn off energy with increased temperature, and thus a net decrease in the total switching energy loss as the temperature was increased from 25 °C to 200 °C.

The switching waveforms for SemiSouth's normally-off JFET with increasing temperature for DPTs at 600 V and 10 A are shown in Figure 112 and Figure 113, where the gate-source voltage waveforms for various temperatures have been aligned so that the influence of temperature on the drain current and drain-source voltage waveforms could be clearly observed. Unlike the normally-on JFET, the total switching energy loss of the normally-off JFET, was found to increase by approximately 15 μ J from 25 °C to 200 °C for a load current of 10 A. As shown by Figure 112 and Figure 113, this increase was due entirely to the turn on switching energy, as the turn off switching loss remained constant with temperature. This trend was verified by the device datasheet [85] and [33]-[35], [86]. The DPT waveforms (Figure 112) revealed that the increase in turn on switching energy loss was a result of a significant decrease in the dv/dt rate. The results of these high temperature DPTs for the SiC normally-on and normally-off JFETs are summarized in Table XVI.

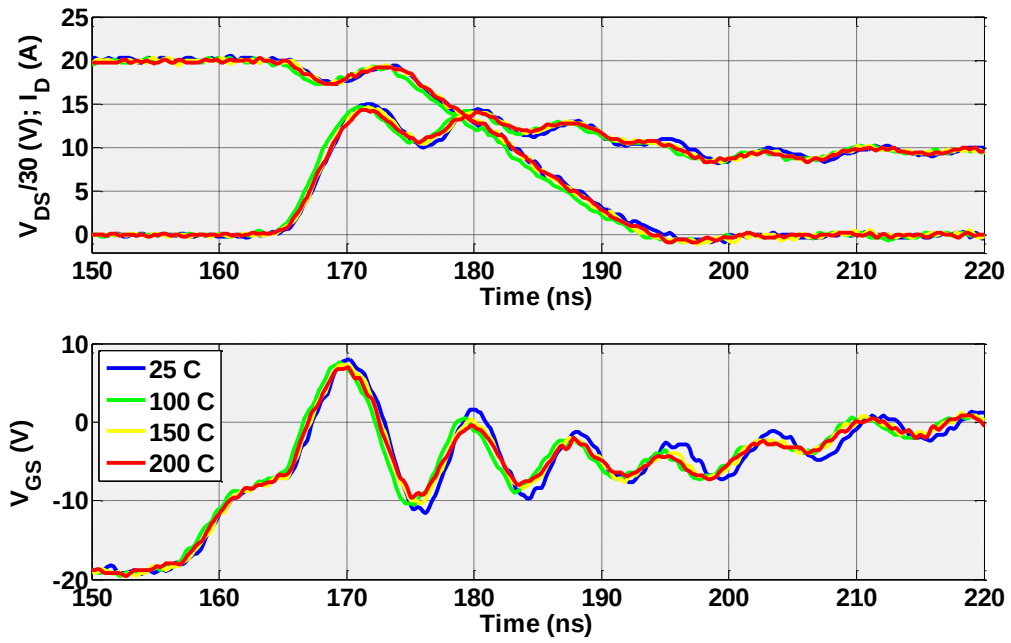


Figure 110: Turn on switching waveforms for Infineon's SiC normally-on JFET with a dc bus voltage of 600 V, a load current of 10 A, and without the R-C-D network (thus $V_{gs} = -19$ V in the off-state) for 25 °C (blue) to 200 °C (red).

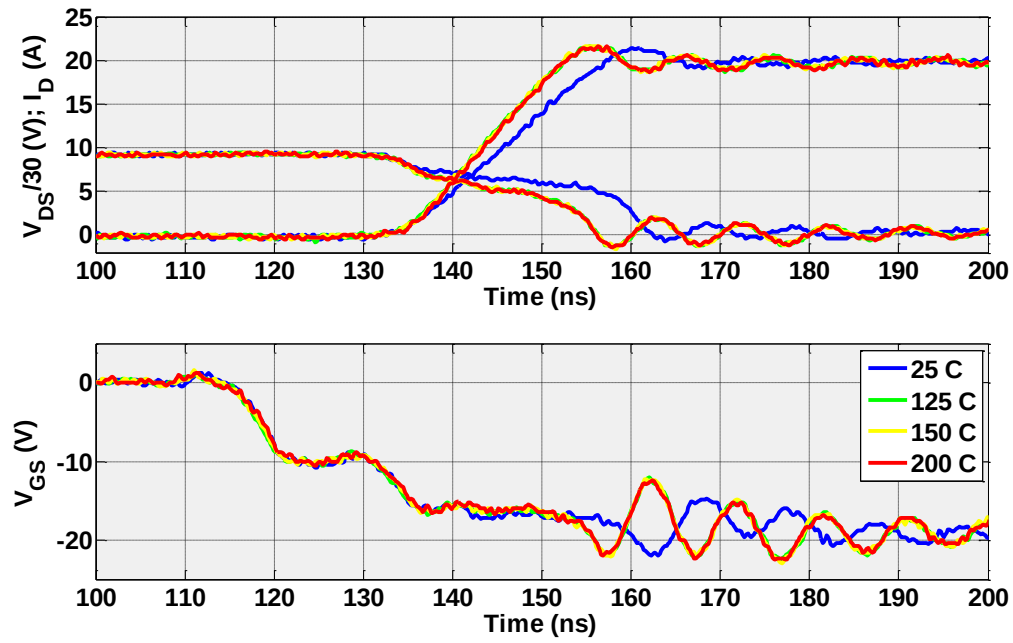


Figure 111: Turn off switching waveforms for Infineon's SiC normally-on JFET with a dc bus voltage of 600 V, a load current of 10 A, and without the R-C-D network (thus $V_{gs} = -19$ V in the off-state) for 25 °C (blue) to 200 °C (red).

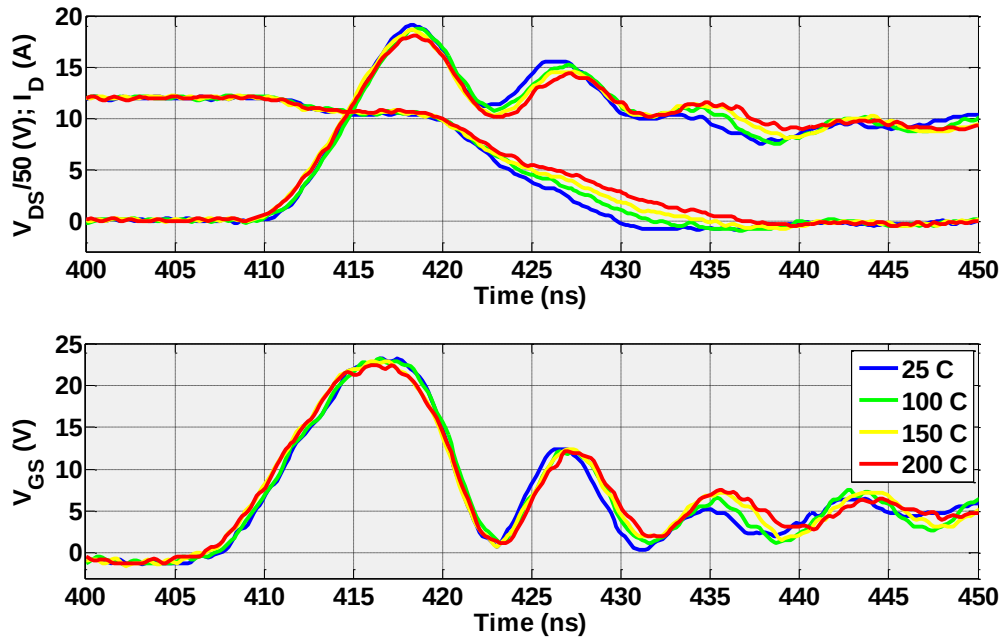


Figure 112: Turn on switching waveforms for SemiSouth's SiC normally-off JFET with a dc bus voltage of 600 V, a load current of 10 A, for 25 °C (blue) to 200 °C (red).

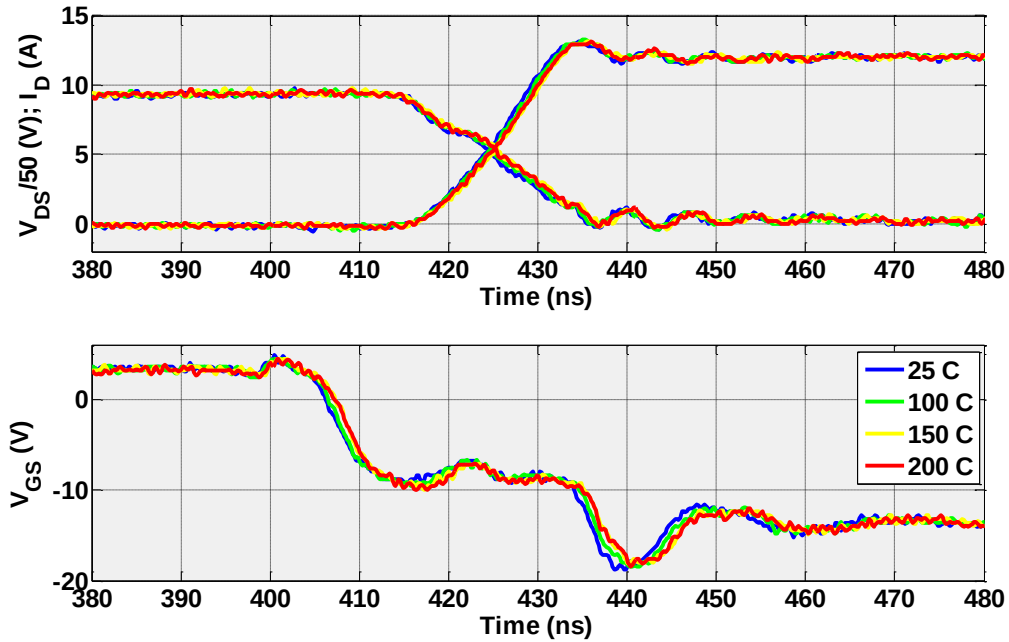


Figure 113: Turn off switching waveforms for SemiSouth's SiC normally-off JFET with a dc bus voltage of 600 V, a load current of 10 A, for 25 °C (blue) to 200 °C (red).

Table XVI: Change in the turn on ΔE_{ON} , turn off ΔE_{OFF} , and total ΔE_{TOT} switching energies of the SiC normally-on and normally-off JFETs for temperatures from 25 °C to 200 °C, and a dc bus voltage of 600 V.

<i>Device</i>	ΔE_{ON}	ΔE_{OFF}	ΔE_{TOT}
Infineon Normally-On JFET	constant	↓	↓ 11 %
SemiSouth Normally-Off JFET	↑	constant	↑ 11 %

Chapter 5 Summary

5.1 *Summary*

In this thesis, complete high temperature characterization was performed on 1.2 kV SiC MOSFET, BJT, SJT, normally-on and normally-off JFET devices. Table XVII summarizes the foremost characterization results for all of the studied 1.2 kV SiC transistors. The categories are: gain (transconductance for the MOSFETs and current gain for the BJTs), on-resistance R_{ON} (including specific on-resistance $R_{ON,sp}$), room temperature (RT) switching energy loss (E_{sw}), driving requirements, and high temperature (HT) performance (with percent change in on-resistance and switching energy loss from 25 °C to 200 °C).

Table XVII: Summary of SiC device characterization.

<i>Device</i>	<i>Gain</i>	<i>R_{ON}</i>	<i>RT E_{SW}</i>	<i>Driving</i>	<i>HT</i>
Cree SiC MOSFET (CMF20120D)	Low NTC (at I _d = 20 A)	Lowest R _{ON} of the MOSFETs	Low E _{SW}	Simple, low losses, but -V _{GS} for safe turn off	85 % R _{ON} rise, 6 % drop in E _{SW,total}
Cree SiC MOSFET (C2M0080120D)	Highest g _{fs} (at I _d = 20 A)	Low R _{ON} and R _{ON,sp}	Lowest E _{SW} of the MOSFETs	Simple, low losses, but -V _{GS} for safe turn off	144 % R _{ON} rise with temperature
ROHM SiC MOSFET (SCT2080KE)	Low NTC (at I _d = 20 A)	Highest R _{ON,sp}	Low E _{SW}	Simple, low losses, but -V _{GS} for safe turn off	145 % R _{ON} rise, 8 % drop in E _{SW,total}
ROHM SiC MOSFET (SCH2160KE)	Lowest g _{fs} (at I _d = 20 A)	Highest R _{ON} of the MOSFETs	Highest E _{SW} , but sensitive to I _{Load}	Simple, low losses, but -V _{GS} for safe turn off	130 % R _{ON} rise with temperature
GE SiC MOSFET (GE12N20L)	Low NTC (at I _d = 20 A)	Low R _{ON} and R _{ON,sp}	Low E _{SW} with lowest E _{Off}	Simple, and low losses, but -V _{GS} for safe turn off	59 % R _{ON} rise, and constant E _{SW,total}
Fairchild SiC BJT (FSICBH057A120)	High h _{FE} (at I _c = 15 A) with NTC	Lowest R _{ON} and R _{ON,sp}	Low E _{SW} , not sensitive to I _{Load}	R _{B,ext} chosen to minimize losses	84 % R _{ON} rise, 6 % drop in E _{SW,total}
GeneSiC SJT (GA06JT12-247)	High h _{FE} (at I _c = 6 A) with NTC	Highest R _{ON} , but low R _{ON,sp}	Low E _{SW} with low E _{Off}	R _{B,ext} chosen to minimize losses	101 % R _{ON} rise, 14 % drop in E _{SW,total}
SemiSouth Normally-Off JFET (SJEP120R100)	High NTC	Low R _{ON} at RT, and low R _{ON,sp}	Lowest E _{SW} , and low sensitivity to I _{Load}	R _{B,ext} chosen to minimize losses, and -V _{GS} for safe turn off	340 % R _{ON} rise, 11 % rise in E _{SW,total}
Infineon Normally-On JFET (IJW120R100T1)	Moderate NTC	Good R _{ON} and R _{ON,sp}	Low E _{SW} with R-C-D, but sensitive to I _{Load}	-V _{GS} chosen for faster switching	219 % R _{ON} rise, 11 % drop in E _{SW,total}

NTC= negative temperature coefficient.

Chapter 6 Conclusions and Future Work

6.1 *Conclusions*

In general, all of the SiC transistors characterized in this thesis showed superior high temperature static and dynamic performance compared to Si devices. In particular, these SiC devices all feature low on-resistances, even at 200 °C, which is due to the higher critical field for breakdown of SiC. As a result, these SiC transistors will have small on-state losses. In particular, the SiC BJT showed the lowest specific on-resistances ($3.6 \text{ m}\Omega\cdot\text{cm}^2$ for Fairchild's FSICBH057A120 SiC BJT at room temperature using die area). However, GE's SiC MOSFET had the lowest change in on-resistance of only 59 % for a temperature increase of 25 °C to 200 °C. The SiC devices also showed low leakage currents ($< 10 \text{ }\mu\text{A}$ for most of the devices) at 1200 V and up to 200 °C, further demonstrating their ability to operate at high temperature.

For the dynamic characterization, it was shown that the SiC devices all experience fast switching speeds, and low dynamic losses. In particular, the SiC BJT is faster than its Si counterpart, and resembles unipolar-like performance during switching. Cree's second generation C2M0080120D SiC MOSFET demonstrated very fast switching capabilities, with dv/dt rates of approximately 57 V/ns (for 600 V bus voltage and 20 A load current). The SiC MOSFETs also showed low turn off energy losses (typically less than 70 μJ at 600 V bus voltage and 20 A load current); therefore, utilizing these devices in soft-switching applications could result in nearly negligible switching losses.

The high temperature dynamic characterization showed that the SiC MOSFETs all experienced decreases in their turn on energies and increases in their turn off energies with increased temperature. The BJT and SJT, on the other hand, featured decreases in both their turn on and turn off losses. The normally-on JFET showed no change in its turn on switching energy, but a decrease in its turn off. Still yet, the normally-off JFET experienced no change in its turn off switching energy, but an increase in its turn on. The normally-off JFET, consequently, was the only device tested in this work that experienced an increase (of 11 % for a load current of 10 A) in its total switching energy loss as the temperature was increased from 25 °C to 200 °C. These results suggest that the temperature dependencies of the switching performance are related to the device structure.

6.2 *Future Work*

With this enhanced performance of SiC devices over conventional Si, a growing number of companies are interested in utilizing the technology to improve the efficiency, power density, and overall cost of their systems. This has led to an increasing number of semiconductor manufacturers producing SiC devices. Since the start of this work, many other manufacturers have joined the SiC market, such as United Silicon Carbide, Inc. with SiC normally-on JFETs (also offered in cascode packages), and STMicroelectronics with SiC MOSFETs. Additionally, Cree, ROHM, and GE are all continuously working on newer generations of their SiC MOSFETs. Cree intends to introduce a third generation SiC MOSFET with a voltage rating of 900 V in the near future. ROHM also released a new SCT2080KE MOSFET in late 2013, and GE has a second generation of its 1.2 kV SiC MOSFET, as well as 1.7 kV SiC MOSFETs. To uphold the objective of evaluating

the latest generation of SiC devices, this future work involves continuing to characterize these newly released SiC transistors. This assessment of the progression of the SiC technology is invaluable information for many industries and other consumers that are considering incorporating these devices into their products.

These SiC device manufacturers are also fabricating power modules with current ratings ranging from 50 A to 100 A. ROHM is also introducing a single SiC trench MOSFET chip rated at 300 A for HEV and electric car applications. Moreover, Cree, GE, and GeneSiC also have 1.7 kV SiC transistors. Cree's C2M1000170D 1.7 kV, 4.9 A SiC MOSFET is currently listed as only \$5.25 on DigiKey, which is cheaper than similarly rated Si MOSFETs and IGBTs. GeneSiC has 1.7 kV SiC SJTs with various current ratings that are commercially available as well. Consequently, this future work also includes evaluating these SiC power modules, and higher voltage SiC devices.

Finally, it is of interest to further verify and extend the proposed analytical model for the 1.2 kV SiC MOSFETs that was presented in this thesis. In particular, the turn off process requires additional analysis and evaluation. This model also needs to be verified under different operating conditions, such as changing temperature and dc bus voltage. Additionally, this model could be extended to higher voltage SiC MOSFETs.

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