Design of an Arbitrary Waveform Generator for Power System Perturbation

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ABSTRACT

In this thesis, the design of a voltage-source inverter (VSI)-based three-phase impedance analyzer's perturbation injection unit (PIU) is described including all relevant power stage and control design. Both series and shunt injection are examined from .1 Hz to 1000Hz. Both types of injection are performed using only energy from the system under test stored in a DC link capacitor. Sinusoidal, square (pulse), and chirp perturbation waveforms are explored. Results from a constructed realization of the design are presented, and the limits of the device characterized. The maximum achievable perturbation power is 10 kW in shunt and 8 kW in series on a 460 V, 100 kW bus. Using the same conditions, maximum power is achievable from 10Hz to 100Hz, at .1Hz, .72 kW is achievable, and at 1000Hz, 6.0 kW is achievable.

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Thanks much to the sponsors of the impedance analyzer project for giving me the opportunity to work and play (and eat.)

No acknowledgement section of a thesis would be complete without thanking the members of the student's advisory committee, but I believe that these individuals have imparted more knowledge to me than is generally the case; without their help, I would still be floundering with basic concepts. Thank you to Dr. Steve Southward, who makes it seem like advanced control concepts are fun and easy, and that anyone can learn them and everyone should. Thank you to Dr. Paolo Mattavelli, who is responsible for the majority of my tutelage in both electrical engineering and power electronics, and who has patiently endured countless undergraduate-level (and a few graduate-level) questions, often of no bearing to the matter at hand ("Why-a you want-a to make-a your life difficult? Your thesis- it's done already?"). Thank you to Dr. Dushan Boroyevich, my advisor, who, perhaps despite his better judgment, let a man with no prior electrical engineering instruction into his lab. I hope that you're happy with your decision.

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1. Introduction

1.a Overview

While there may be many other uses for a 10kW arbitrary waveform generator, this one was destined to be part of a three-phase power system stability measurement device. There are several commercially available frequency response analyzers that perform this task for DC systems, such as the Venable Model 350, the Ray Ridley Engineering AP300, and the myriad of HP impedance analyzers. However, there are no commercial devices at the time of the writing of this thesis that perform this task for three-phase systems.

The role that an arbitrary waveform generator plays in a stability measurement device as well as the applicable theory that is required for the development of such a device is presented in the Literature Review later in this section. At the end of this section, goals will be presented for the development of the waveform generator. With the goals outlined, the salient features of the real-world generation of d-q signals will be discussed. After the abc realizations of d-q signals are outlined, the power stage design methodology will be presented. This involves the AC side construction for both shunt and series injection, as well as the selection of the DC link energy storage capacitor. Once the topology and component values are known, the control strategy and implementation can be discussed. Both the series and shunt control schemes are discussed, as well as the methods for maintaining DC link capacitor charge. With the power stage and control design complete, the fault protection and power routing of the device will be explained. With the complete device design discussion complete, the simulation and experimentation results can be discussed. Finally, conclusions are made and possible future work is discussed.

1.b Literature Review

Understanding the reasons that a stability measurement device requires an arbitrary waveform generator (or why such a stability measurement device should be built in the first place) requires some background knowledge.

Historically, power utilities have done a very good job of maintaining stability of the 3 phase systems that lead to the end user. However, with the advent of research in the realm of distributed power generation, many future 3 phase power systems may be disconnected entirely from the grid, and will not benefit from the work done by the utilities. In addition, modern power electronics systems involve more complex and higher performance control systems than ever before. This leads to a level of interaction between power subsystems never seen previously. Therefore, it's of use to not only make use of existing methods to predict stability of a system to be built, but also to develop a method to measure an existing system and to produce a numerical indication of the likeliness of instability.

The determination of stability of systems involving controlled power converters is nothing new; in 1976, Dr. R. David Middlebrook first published work on the stability analysis of a controlled converter attached to an input filter comprised of reactive elements [4]. In 1978, he refined this method [5]. Being that a converter can also be considered to be a reactive element, it's easy to extend this method beyond input filters to cascaded converters, and even to multiple converters tied to a common bus. The method that Middlebrook developed has come to be known as "The Middlebrook Stability Criterion." The basis of this method is the study of the interaction of the output impedance of one system with the input impedance of the system that it's attached to.

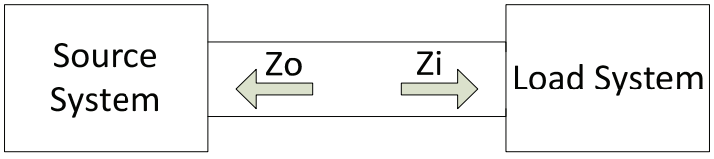

Figure 1.1: Generalized Impedance Diagram

If the system can be broken and the impedances determined, the model of the system can be reduced to:

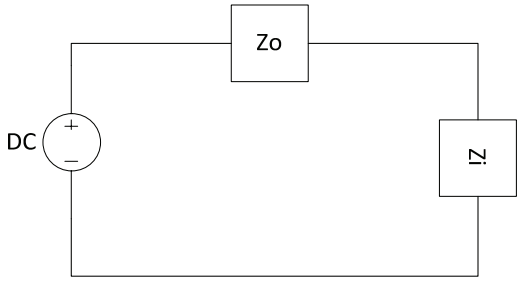

Figure 1.2: Equivalent Electrical Circuit to 1.1

To find the output voltage (the voltage across the impedance "Zi"), the voltage divider equation can be used.

(1.1) $$\frac{V_{Z_i}}{V_{DC}} = \frac{Z_i}{Z_i + Z_o}$$

Or, equivalently,

(1.2) $$\frac{V_{Z_i}}{V_{DC}} = \frac{1}{1 + \frac{Z_o}{Z_i}}$$

The open loop gain on the return path of this closed-loop system can then be expressed as:

(1.3) $$T = \frac{Z_o}{Z_i}$$

$Z_o =$ Output Impedance of the Source system

$Z_i =$ Input Impedance of the Load System

In this thesis, this loop gain will be referred to as the "Interface Impedance" or "Return Ratio" to reduce confusion with other loop gains.

The Middlebrook Stability Criterion's salient feature is that the above loop gain can be used exactly as the open loop transfer function of a system in classical control design. The closed loop properties of the system can be determined by studying the frequency response of the open loop system. Because of this, classical control tools, such as the Nyquist Stability Criterion, can be applied. The easiest way to explain the mechanics of the application of the classical control theory in the way that Middlebrook did is graphically. First, the impedances must be found. The manner of finding these

impedances will be discussed later, and is the majority of the basis for this undertaking. After the impedances are found, their frequency responses can be plotted.

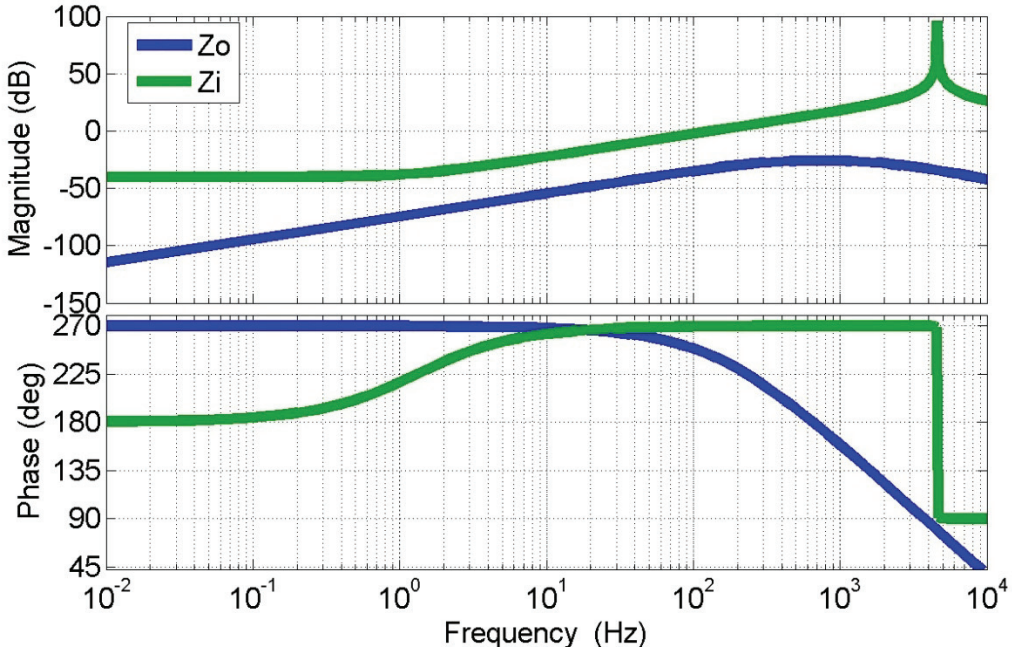

Figure 1.3: Bode Plots of Input and Output Impedances of a Stable System

If the output impedance magnitude rises above the input impedance magnitude, a potential instability exists. In this case, Zo never rises above Zi. If it did, the minimum of the phase difference between the two must be studied to determine stability.

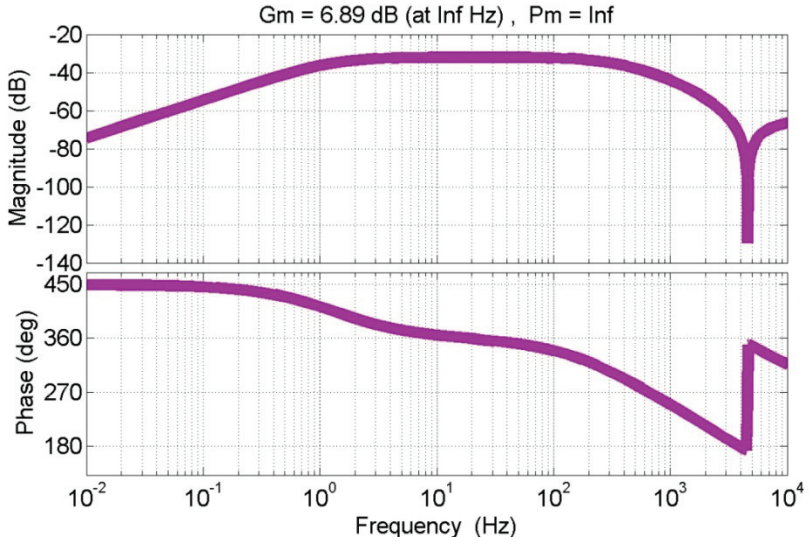

Figure 1.4: Bode Plot of the "Interface Impedance" of a Stable System

An easier manner to view this interaction (or lack thereof) is to plot the "Interface Impedance". As alluded to before, this transfer function can be treated much like the open loop transfer function of a plant when studying stability using classical control methods. The interface impedance transfer function has a gain margin and a phase margin, and they can not only predict instability, but also represent the aforementioned numerical measures of system instability likeliness. In this case, the gain margin and the phase margin are both sufficient to ensure stability.

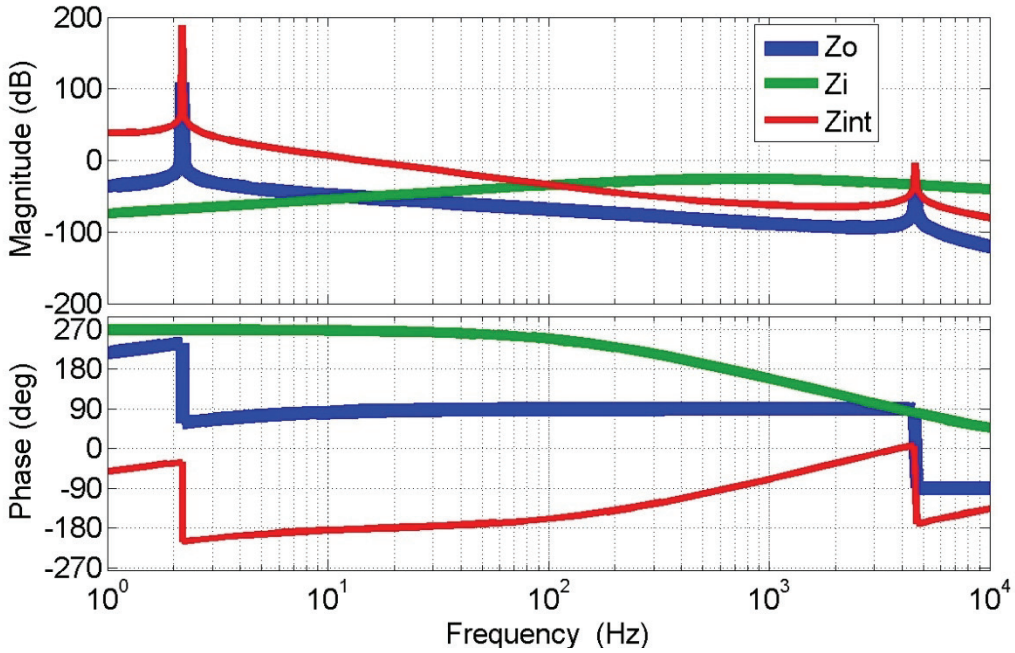

Figure 1.5: Impedances of an Unstable System

Here, a resonance at approximately 2Hz in the output impedance results in a -180° crossing in the phase response. At this frequency, the interface impedance gain is clearly above 0dB; this system is unstable. Another way to view these properties is with the Nyquist plot. The Nyquist Stability Criterion requires that:

(1.4) $$Z = P + N$$

Where Z is the number of right half plane zeros in a transfer function, P is the number of right half plane poles in the transfer function, and N is the number of times that the Nyquist plot encircles the -1 point on the real axis. The Nyquist plots of the above stable and unstable transfer functions are shown below.

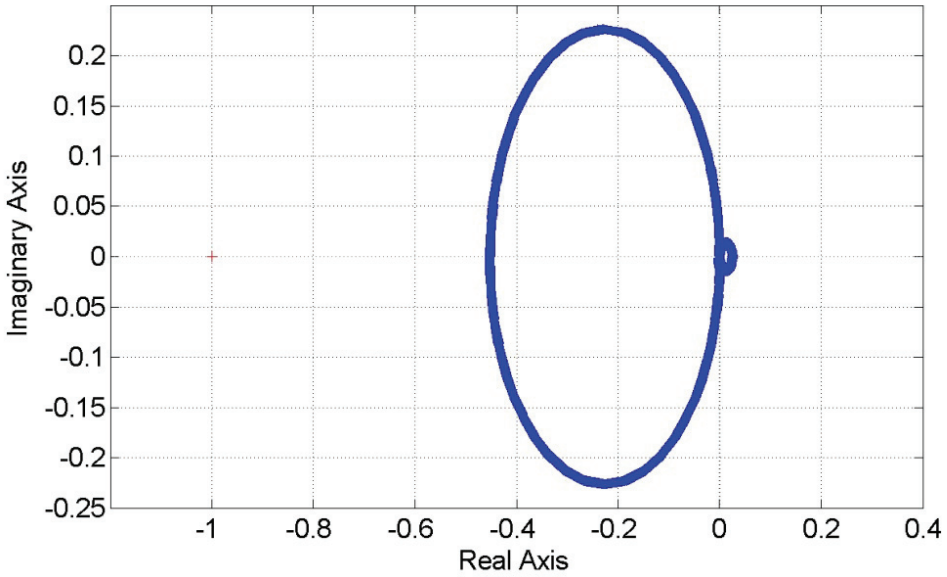

Figure 1.6: Nyquist Plot of a Stable System

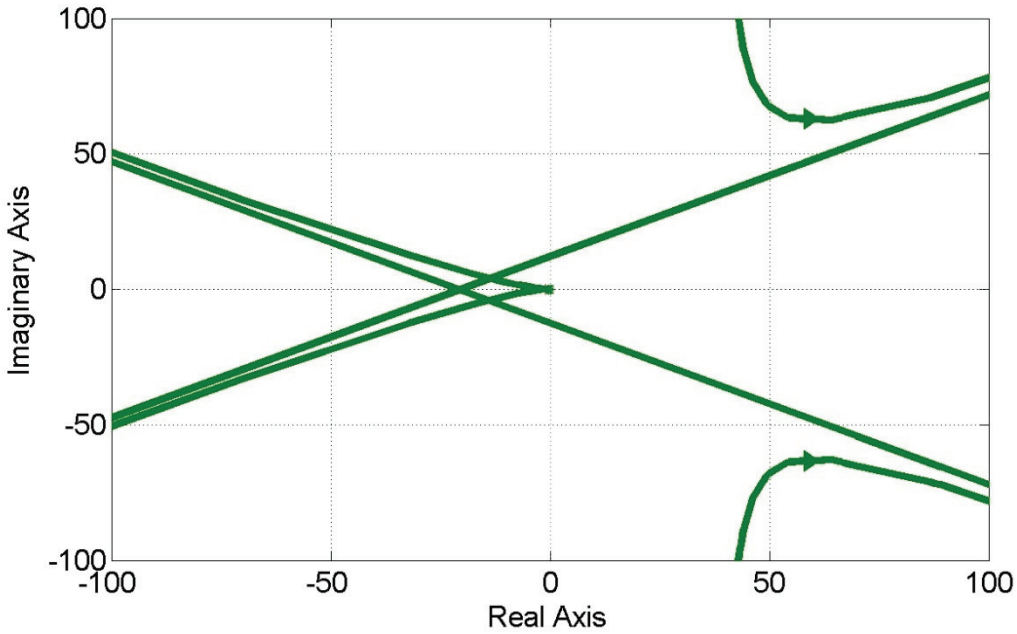

Figure 1.7: Nyquist Plot of an Unstable System

The arrows in Figure VII indicate the direction of the Nyquist plot as frequency increases. Neither of these transfer functions have any right half plane poles nor any right half plane zeros, so both require zero encirclements of the -1 point for stability. The stable system meets this criterion, and the unstable system does not. The Bode plot and Nyquist plot methods of stability analysis are equivalent; whichever one makes analysis easier for a given situation may be used.

This type of stability analysis for power systems works very well when the impedances of the subsystems can be treated as single-in, single-out systems, with the current being the input and the voltage being the output. This is the case with such systems as those with multiple DC/DC only converters. However, standard Nyquist analysis falls short when the impedances must be treated as multiple-in, multiple-out systems such as those found in three-phase AC Systems. The literature review section of this report contains the methods of extending the Middlebrook Criterion to make it applicable to be used in three-phase AC systems.

The methods for impedance measurement implemented in the system that utilizes this arbitrary function generator rely heavily on frequency response estimation techniques, which are usually presented in literature as a precursor to system identification [8]. These methods involve perturbing the system under test with signals of known frequency, and measuring the resulting response of the system. Therefore, an impedance measuring device requires two major subsystems; the first perturbs the system under test, and the second measures the response.

Herein lies the use of an arbitrary waveform generator to a stability measurement system; the waveform generator plays the role of the first major subsystem, and is responsible for the perturbation of the system under test. Mechanical controls engineers sometimes call this type of device “the hammer”, as in “hit it with a hammer and see what happens.”

If the system under test is a 100kW micro-grid, production of a “hammer” large enough to produce a measurable response is no insignificant task. One issue with regard to this is the signal-to-noise ratio. If the perturbation response signal strength is small when compared to the normal level of noise on the system under test, measurement of an output becomes difficult. Time and frequency averaging techniques exist that allow

lower signal-to-noise ratios to be accommodated in system identification [8], but all of them require perturbing and measuring for longer periods of time for smaller signal-to-noise ratios. Therefore, a higher signal to noise ratio is desirable. Another issue is the digital nature of modern controls for 3 phase power systems.

The sensors in modern three-phase power systems that inform the controller of the voltage and current in the system are tied to analog-to-digital converters. These converters discretize the analog voltages and currents to a number. For example, a voltage sensor and ADC might have 255 discrete levels that all voltages must fall into. If the voltage of the system swings from -678V to 678V (as it does in a 480V commercial three-phase system), this means that each discrete level corresponds to a voltage range of 5V. If a perturbation is made that doesn't change the system voltage by at least 5V, then the controller may not register a change in the system that it controls. If this happens, no reaction will be made. While most modern ADCs have a much better resolution than 255 levels, system identification usually requires a change of several levels, with more levels producing better results. For the design of this waveform generator, a perturbation power level of 1.5% of the total system under test power was specified.

There are many ways of designing a device capable of this level of perturbation power. In the past, linear amplifiers have been used to generate the signal [6]. In this case, a three-phase voltage-source inverter is implemented. The use of such an inverter for this purpose presents several benefits. First, one system can perturb the all three phases of the system under test at once, resulting in arbitrary perturbation of the d and q voltage and/or current channels; 3 linear amplifiers would be necessary to do this. Also, if the VSI is controlled properly, it can be used bi-directionally. Also, being a switched-mode power device, the VSI will be more efficient and produce less heat. Third, if the converter is used bi-directionally, an energy storage element, such as a capacitor or battery, can be placed on the DC link and charged/discharged in a controlled manner. This means that all power for the waveform generator can be taken from the device under test, and a separate power supply is not required. This is not the case with linear amplifiers. In addition to being an inconvenience, the necessity of an external power supply can cause errors in measurement. If the system under test is also used to feed the perturbation device during perturbation, the system under test will be changed during the

measurement period. The measurements will be accurate as a measure of impedances for the system with the tester attached, but not as a measure of impedances for the system without the tester attached. An energy storage device in the perturbation generator results in the only effect of the perturbation generator on the system being the perturbation itself.

In 1994, Dr. Silva Hiti first extended the Middlebrook method to three-phase systems through the use of the d-q, or "park" coordinate transform [10]. In 1997, Dr. Mohamed Belkhayat published a paper [9] further increasing the sophistication of the analysis by incorporating the "Generalized Nyquist Criterion". Since the d-q transform effectively transforms the 3 phase system into a multiple-in, multiple-out system with two inputs and two outputs [1], the GNC, which was designed for MIMO systems, is applicable.

Since the d and q channels (both in current and in voltage) are coupled, instead of having a single output impedance and a single input impedance, there are now 4 input impedances and 4 output impedances. This results in a set of 4 interface impedances that must be analyzed for stability. Dr. Belkhayat represented these 4 interface impedances as a matrix, and called the matrix the "Return-Ratio Matrix"

(1.5) $$Y_L = \frac{1}{Z_L}$$

(1.6) $$\boldsymbol{Y}_L = \begin{bmatrix} Y_{Ldd} & Y_{Ldq} \\ Y_{Lqd} & Y_{Lqq} \end{bmatrix}$$

(1.7) $$\boldsymbol{Z}_S = \begin{bmatrix} Z_{Sdd} & Z_{Sdq} \\ Z_{Sqd} & Z_{Sqq} \end{bmatrix}$$

(1.8) $$\boldsymbol{Z}_S\boldsymbol{Y}_L = \begin{bmatrix} Z_{Sdd} & Z_{Sdq} \\ Z_{Sqd} & Z_{Sqq} \end{bmatrix}\begin{bmatrix} Y_{Ldd} & Y_{Ldq} \\ Y_{Lqd} & Y_{Lqq} \end{bmatrix} =$$
$$\begin{bmatrix} Z_{Sdd}Y_{Ldd} + Z_{Sdq}Y_{Lqd} & Z_{Sdd}Y_{Ldq} + Z_{Sdq}Y_{Lqq} \\ Z_{Sqd}Y_{Ldd} + Z_{Sqq}Y_{Lqd} & Z_{Sqd}Y_{Ldq} + Z_{Sqq}Y_{Lqq} \end{bmatrix}$$

To utilize generalized Nyquist stability determination methods, the eigenvalues of this matrix of transfer functions must be found. These eigenvalues are themselves transfer functions, which must then be analyzed using the Nyquist stability methods outlined above.

This obviously complicates the original simple Nyquist stability analysis by quite a bit. It was the work of Dr. Rolando Burgos to simplify this method [7]. Dr. Burgos

found that for high power factor systems, only Z_{dd} has an effect on stability. While he doesn't specify a lower limit to the power factor, his work is very applicable to most modern 3 phase AC systems with power factor correction. The 2010 work of Dr. Burgos represents the state-of-the-art theory in the realm of three-phase power system stability analysis.

In order for both the Belkhayat method and the Burgos method to work, the input and output impedances must first be known. As alluded to in the introduction of this thesis, the estimation of these impedances comprises the goal of the work presented in this thesis.

The selection of a perturbation signal is paramount to successful system identification. Controls engineers sometimes call this signal the "excitation signal". Every system reacts differently to different excitation signals, and what works well for one system doesn't work well for another. Common excitation signals include white noise, band limited white noise, sinusoids, chirps, and step or pulse signals. If a system is to be built to identify multiple unknown systems, availability of multiple excitation signals will more than likely prove beneficial. For this endeavor, the sine, chirp, and pulse signals were selected to comprise the impedance measurement device's perturbation arsenal for reasons explained below.

In the end, this stability analysis system will produce frequency response functions that represent the frequency domain behavior of the system impedances. As mentioned in the introduction, frequency response estimation techniques do a good job of providing these types of functions given that a clear input and a clear output can be determined. This is the case for impedance; the input is current, and the output is voltage. There are 8 impedances in total required to determine stability, but all of them can be represented in the same way.

$$\tilde{Z} = \frac{\tilde{v}}{\tilde{\imath}} \tag{1.9}$$

Here, the tildes simply indicate "small signal", which is the information of interest when finding frequency responses.

Unfortunately, it's very difficult to simply measure the frequency response of the current and the frequency response of the voltage, and then to directly calculate impedance. The reasons for this involve noise, and will be explained later. For now the method of impedance calculation will simply be presented.

(1.10) $$\tilde{G}_{id} = \frac{\tilde{\imath}}{\tilde{c}_p}\ ,\ \tilde{G}_{vd} = \frac{\tilde{v}}{\tilde{c}_p},\ \tilde{Z} = \frac{\tilde{G}_{vd}}{\tilde{G}_{id}} = \frac{\frac{\tilde{v}}{\tilde{c}_p}}{\frac{\tilde{\imath}}{\tilde{c}_p}} = \frac{\tilde{v}}{\tilde{\imath}}$$

Here, $\tilde{c}_p$ is the perturbation command, or the command to the arbitrary waveform generator. Thus, there is a method to determine impedance from a known waveform command. This method simply requires determining two frequency response functions to this known input. All that's left to do from here (in theory) is to select the perturbation command.

The easiest method of frequency response estimation requires a sinusoidal perturbation. A sinusoid of one frequency is used as the input, and the response of the system to that frequency only is measured. This is done numerous times until a frequency response like the one below is produced.

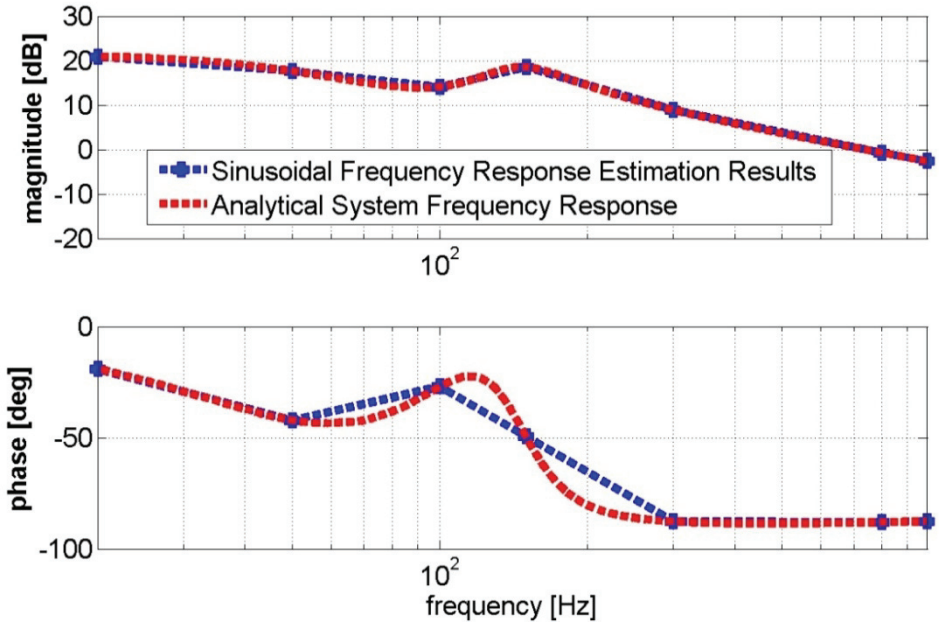

Figure 1.8: Sinusoidal Frequency Response Function Estimation*

* All FRF bode plots shown in this section were produced by an internal CPES MATLAB ".m" file written by Marko Jaksic

This method is the most accurate when a system is highly non-linear like many three-phase power systems. In these power systems, one excitation will likely cause a response at many different frequencies such as the 3rd, 5th, and 7th harmonic to the excitation frequency. When this method is used, only the response of the system at the excitation frequency is considered, and all other responses are thrown away. However, as can be seen in figure 1.8, this method must be repeated at many frequencies to get an accurate representation of the real frequency response. This can be very, very time consuming. The sinusoidal perturbation must be made, then enough time must pass for the system to reach steady-state, then the response must be measured, and then whole process must be repeated for the next frequency point of interest. In addition to making for unhappy engineers, this process can result in inaccurate results if the system changes during the long response estimation process.

The next easiest method for frequency response estimation involves exciting the system with a signal containing many frequencies, sampling both the excitation and the response, taking the Fourier transform of both the excitation data set and the response data set, and simply dividing the results.

(1.11)
$$\frac{\widetilde{output}}{\widetilde{input}} = \frac{\tilde{y}}{\tilde{u}} = \frac{FFT(y(t))}{FFT(u(t))}$$

If the system is linear and has no noise, the results of this method are very attractive.

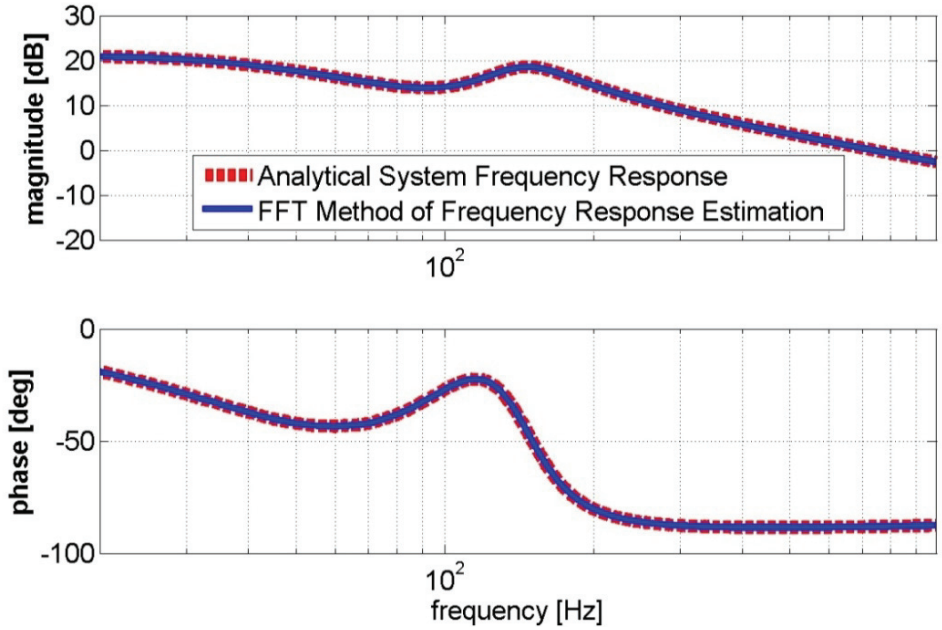

Figure 1.9: FFT Frequency Response Function Estimation, No Noise

Unfortunately, a linear system with no noise doesn't exist in the real world. When noise is added to the system under test, the FFT method often results in a frequency response function like the one shown below.

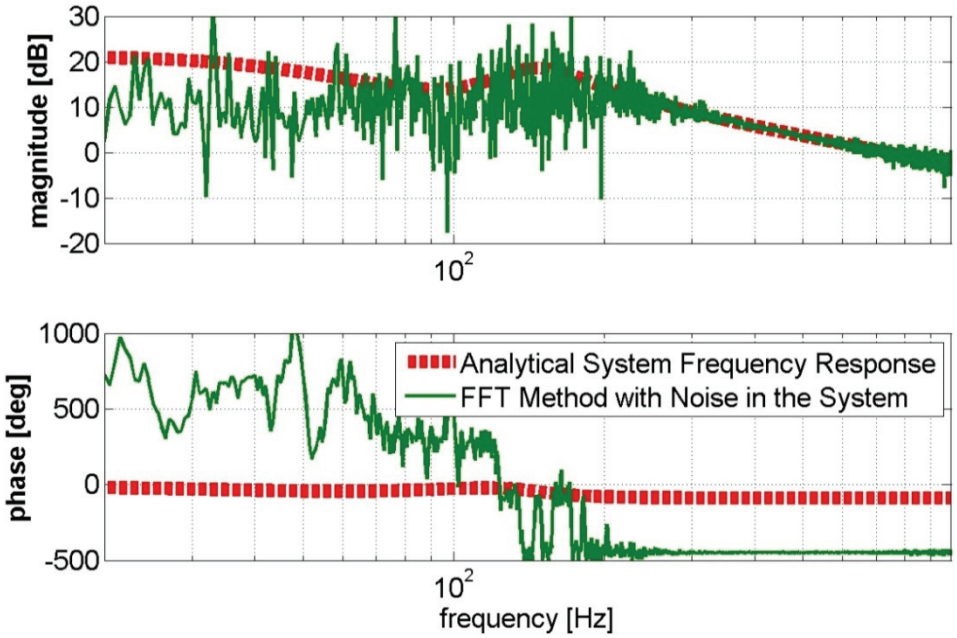

Figure 1.10: FFT Frequency Response Function Estimation with Noise

In order to fix this problem, time and frequency averaging techniques have been developed to reject noise. Techniques among the most common involve using the cross-power spectral density of the same sampled data used in the FFT method.

(1.12) $$H_1\left(\frac{\tilde{y}}{\tilde{u}}\right) = \frac{S_{uy}}{S_{uu}},\ H_2\left(\frac{\tilde{y}}{\tilde{u}}\right) = \frac{S_{yy}}{S_{yu}}$$

Here, S_{uu} is the auto-power spectral density of the input (excitation) data, S_{yy} is the auto-power spectral density of the output data, S_{uy} is the cross-power spectral density from the input to the output, and S_{yu} is the cross-power spectral density from the output to the input [12]. All CPSD methods work best when using time-averaged data. Among the most famous of these is the Welsh method [11]. These methods are very good at removing noise during a system identification process, but they both have limits. H_1 assumes no noise on the input, and requires that any noise on the output is uncorrelated to the input. H_2 assumes the inverse; there is no noise on the output, and noise on the input is uncorrelated to the input [12]. These assumptions and requirements are the reasons that the impedance can't easily be found from voltage and current data alone. Both of these signals will have some noise, so neither the H_1 nor the H_2 method can be expected to be effective. However, the command signal is unlikely to contain any noise; it will be generated within the waveform generator controller, and can be easily passed to the measurement computer without ever having to be involved with the system under test or any other source of noise. Because of this, the frequency response functions in (5) can be found with the H_1 estimate with a reasonable expectation for accuracy.

When these methods are properly implemented, results like those shown below can be achieved.

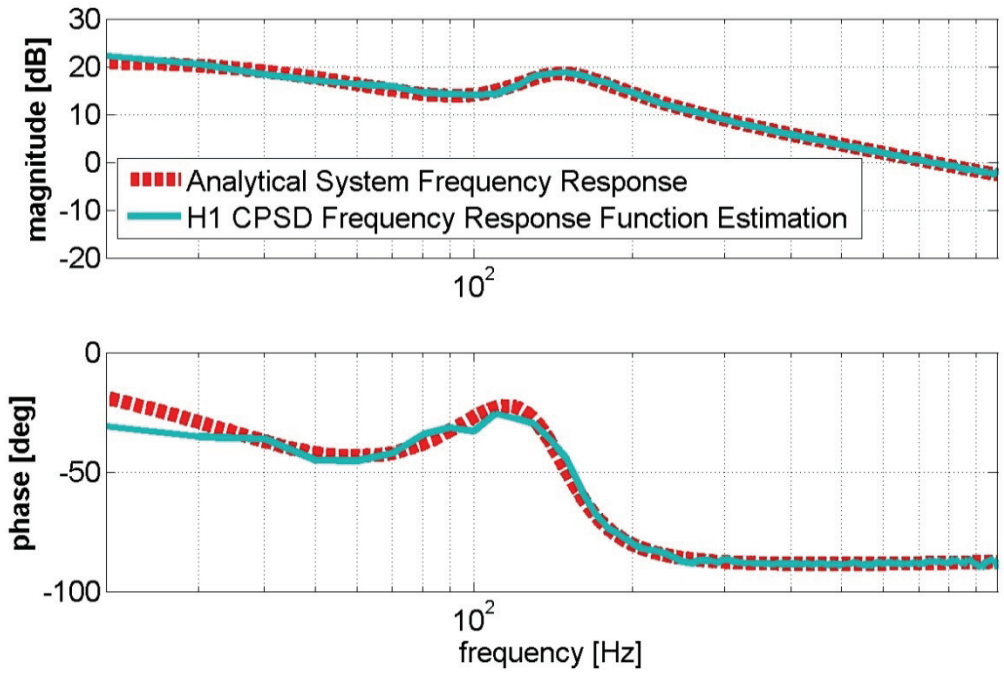

Figure 1.11: H_1 Frequency Response Function Estimation with Noise

Notice that there is still some distortion between the analytical solution and the H_1 estimate. Such a slight deviance may have no effect on stability analysis, but this deviance is shown here to illustrate a point. Both methods have an additional requirement- they require that enough samples have been taken to average out the effects of the noise [12]. If more data is taken, this distortion will eventually be averaged out. However, the same time-dependent problem associated with sinusoidal frequency response estimation is also applicable here. As the sampling time increases, the risk that the system under test will change mid-test also increases.

It is currently unknown whether or not these time and frequency averaging techniques will produce accurate (albeit linearized) results when applied to the identification of a non-linear three-phase power system. This is one of the goals of the greater research project that this arbitrary waveform generator is part of.

One thing that is common to the FFT and CPSD methods is that they require a perturbation signal that is rich in spectral content in the frequency range of interest. Since an infinite frequency signal cannot be achieved, a range of frequencies must be

chosen when trying to identify a system. For this attempt at stability analysis, the impedance measurement range has been specified to be .1Hz to 1kHz.

1.c Goals

The goals of this thesis are most easily explained in tabular form.

Performance Mark/ Device Specified	Specification Value
Bus Power, Nominal	100kW
Bus Voltage, line-to-line, Nominal	460VAC RMS
Injection Power, min	1% of nominal Bus Power (1.0kW)
Injection Power, max	10% of nominal Bus Power (10kW)
Power Source	120VAC RMS and Bus Only
Frequency Range of Interest	.1-1000Hz
EMI Filter	Differential and Common Mode
Switching Equipment	American Superconductor PM 1000
Control Board	Dr. Herbert Ginn's Control Board for the PM1000
Injection Modes	Shunt and Series

Table 1.1: Performance and Hardware Specifications

Table 1.1 outlines the boundaries of specification and therefore the goal parameters. This waveform generator will be able to perform injections of sinusoidal, pulse, and chirp forms in both series and shunt injection orientations with a power of at least 1kW and at most 10kW on a 100kW 460V line-to-line three-phase bus. Figure 4.1 illustrates what is meant by "series" and "shunt" with regard to injection orientation.

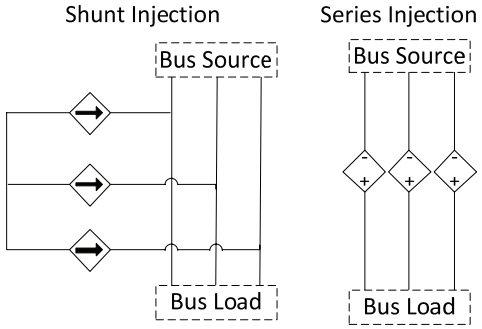

Figure 1.12 Shunt and Series Modes of Injection

2. Arbitrary Waveforms for Power System Perturbation

What makes this arbitrary waveform generator special is that the perturbation signals required of it aren't measured in the "real" domain. Being that the system to be identified resides in the d-q reference frame, the perturbation signals must also be in this rotating reference frame. When these signals are translated back to the "real" domain, they bear little resemblance to the original perturbation signals in d-q. In addition, they have properties of concern to multiple calculations related to both the construction and use of the complete device. Examples of the aforementioned pulse, chirp, and sinusoidal perturbation signals in this reference frame are presented below. For all examples presented here, the fundamental d-q frequency will be 60Hz.

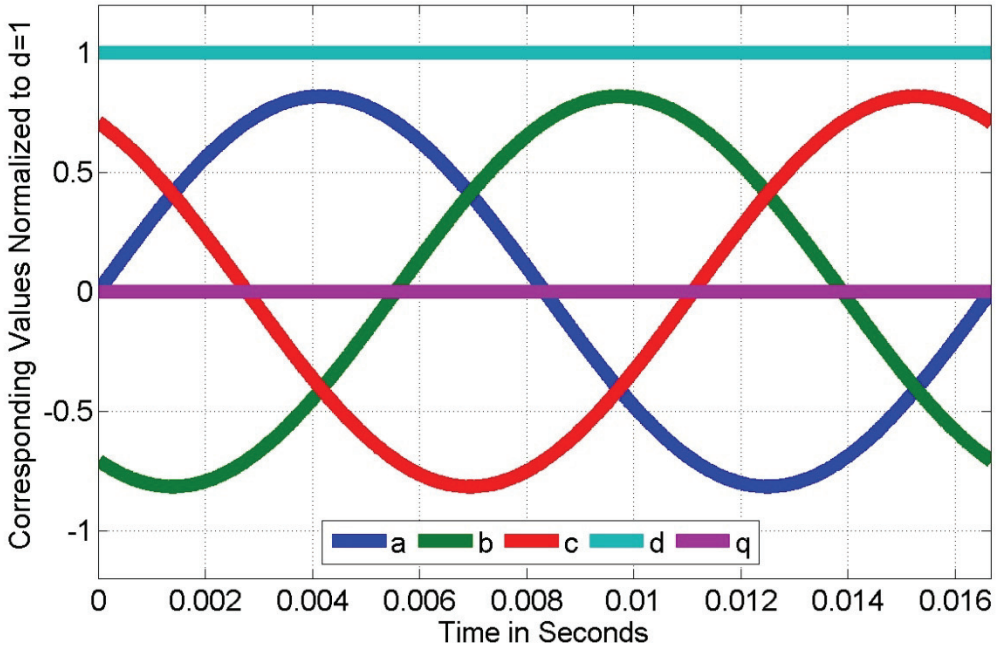

Figure 2.1: abc Waveforms Translated from d=1, q=0

Before delving into these perturbation waveforms, having a short refresher on translating from dq to abc (or "real world") reference frames and the resulting effect on signal power will make further discussion of the perturbation signals easier. Translating

from abc to dq requires two steps. First, the "Clarke" or "alpha-beta" transform takes the three abc waveforms and turns them into two waveforms with a 90° separation [2].

$$\begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} X_a \\ X_b \\ X_c \end{bmatrix} \tag{2.1}$$

Then, the "Park" transform takes the 2 alpha-beta waveforms and turns them into 2 waveforms that are DC at the rotational frequency [2].

$$\begin{bmatrix} X_d \\ X_q \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} X_\alpha \\ X_\beta \end{bmatrix} \tag{2.2}$$

In these transformations, the "gamma" component of the "Clarke" transform and the "zero" component of the "Park" transform are ignored. If the 3 waveforms are unbalanced, these components cannot be ignored. However, it is common practice to assume balanced waveforms and to ignore "gamma" and "zero". Also, the conversion matrices back from "alpha-beta" and "d-q" are simply the transposes of the transformation matrices presented above; they are constructed such that their inverses are their transposes.

Notice the scaling factor of $\sqrt{2/3}$ in the "Clarke" transform. This is part of a greater scaling factor built into the transformation matrix. Although this is unnecessary for transformation from balanced 3 phase waveforms to 2 orthogonal waveforms, it allows for easier power calculations. The waveforms shown above use the transform as shown here, with the scaling factor. The RMS value of the each of the 3 abc components is $\sqrt{3}/3$ when d = 1. When d=1 produces these RMS values in abc, the sum of the power in the d channel and the q channel is equal to the sum of the power in a, b, and c. To illustrate this, the values in the figure above can be used. If these values represent both the voltage and the current, the power calculations become:

$$P_{tot\_abc} = \begin{bmatrix} V_a & V_b & V_c \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} \frac{\sqrt{3}}{3} & \frac{\sqrt{3}}{3} & \frac{\sqrt{3}}{3} \end{bmatrix} \begin{bmatrix} \frac{\sqrt{3}}{3} \\ \frac{\sqrt{3}}{3} \\ \frac{\sqrt{3}}{3} \end{bmatrix} = 1 \tag{2.3}$$

$$P_{tot\_dq} = \begin{bmatrix} V_d & V_q \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} 1 \\ 0 \end{bmatrix} = 1 \tag{2.4}$$

(2.5) $$P_{tot\_abc} = P_{tot\_dq}$$

Just to show that this works in the q channel as well, the waveforms resulting from q=1 and d=0 are shown below.

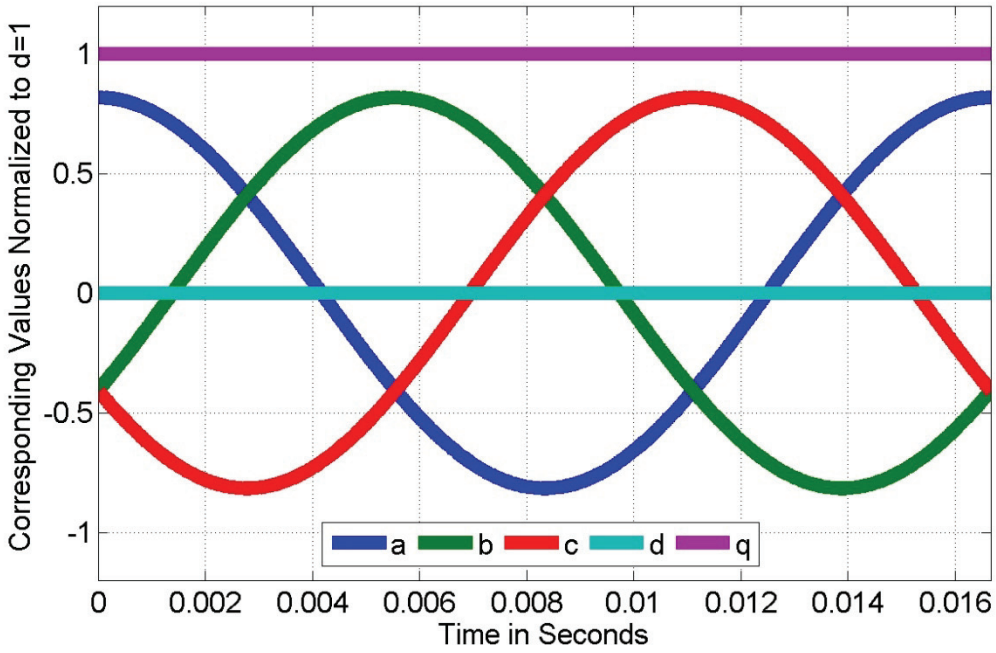

Figure 2.2: abc Waveforms Translated from d=0, q=1

The arbitrary waveform generator designed here will be able to perturb either the voltage or the current of the system under test. To find the current or voltage necessary to perturb the system by a desired power level, the system under test voltage or current must be known. Luckily, the other half of the system identification device, the measurement half, can easily produce these values. For current perturbation, the calculation of the d or q channel current necessary for a desired power level is simply:

(2.6) $$i_{drms} = \frac{P_{d\_desired}}{V_{drms\_SUT}},\ i_{qrms} = \frac{P_{q\_desired}}{V_{qrms\_SUT}}$$

For voltage perturbation, the calculations are very similar.

(2.7) $$V_{drms} = \frac{P_{desired}}{i_{drms\_SUT}},\ V_{qrms} = \frac{P_{q\_desired}}{i_{qrms\_SUT}}$$

Notice that the values presented here are root mean square values. This is important to generality; for the DC d and q examples presented above, the RMS values are identical to the DC values. DC perturbations, however, are of almost no use when trying to identify a system.

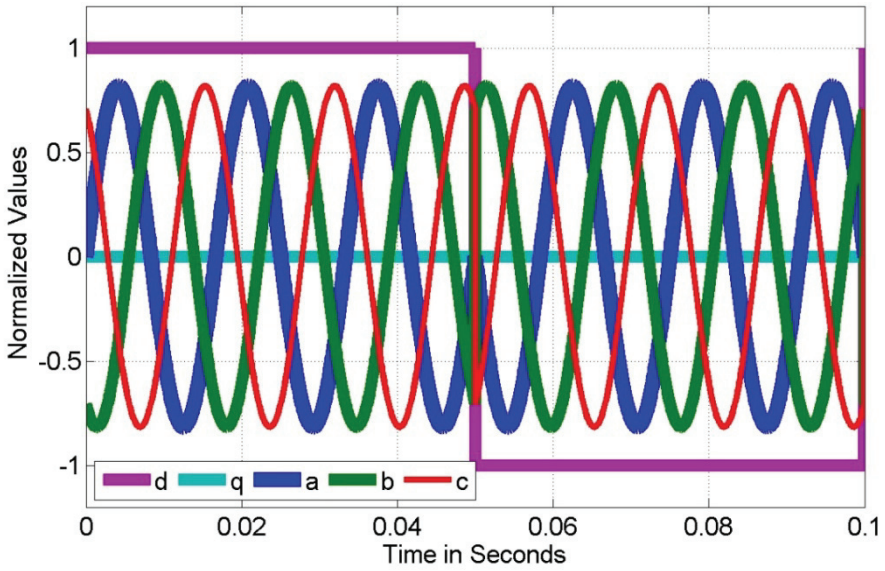

Figure 2.3: abc Waveforms Translated from a 10 Hz 50% Duty Cycle Pulse Signal in d of Amplitude 1

The easiest d-q perturbation signal to understand is the "pulse" or "step" signal. If the pulse signal goes from a positive value to the negative of that value, the RMS value of the waveforms in abc are $\sqrt{3}/3$ times the positive value of the pulse, identical to the DC case. The only difference is that the abc values invert, as shown in Figure 2.3.

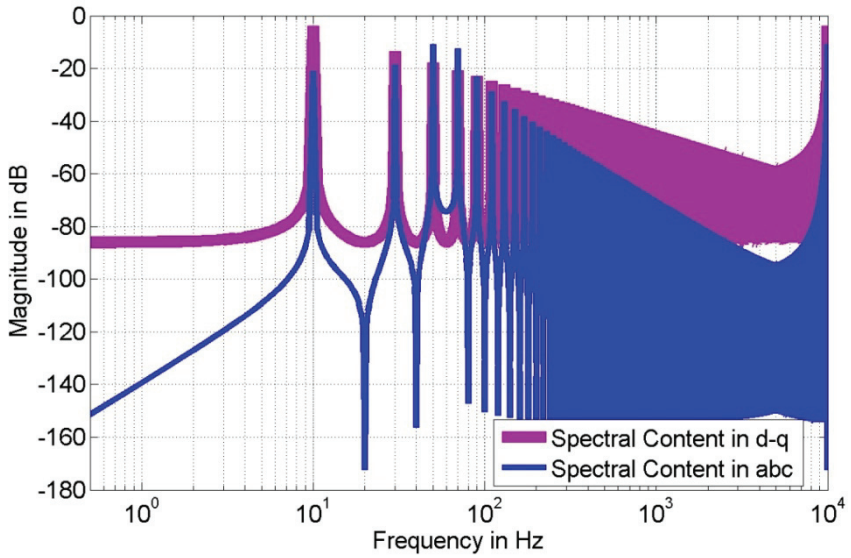

Figure 2.4: Spectral Content of the d-q Pulse Signal in d-q and abc Reference Frames

The specific pulse signal analyzed here is the same as in Figure 2.3- it has a 50% duty cycle at 10Hz. The spectral content of this signal illustrates several important points. First, the pulse signal has high content at its nominal frequency. Second, it also has quite a bit of content at the 3rd, 5th, 7th, etc. harmonics, albeit a lower level of content than at the nominal frequency. This signal can be expected to produce good response data at these frequencies, although the space between them may produce a somewhat diminished response between these frequencies. As part of a set of perturbation signals, this type of signal can help to measure a frequency response function at lower frequencies.

There's also some interesting information in the abc translation of this signal. The d-q transform takes the d-q rotational frequency (60Hz in this thesis) and makes that frequency DC. Therefore, it stands to reason that when a signal in d-q is translated to abc, the frequency spectrum of that translated signal will appear as if the original d-q signal's spectrum has had its DC results shifted to the d-q rotational frequency. This can be seen in the abc spectrum above. At 10Hz above the nominal frequency, the same spike can be seen as at 10Hz in the d-q spectrum. Also, in signal processing theory, it is known that 0Hz acts as a "folding point"; the negative frequency range is a mirror of the positive frequency range. Since 0Hz has been shifted to 60Hz through the d-q to abc transform, 60Hz now acts as that "folding point". As seen in figure 2.4, this is indeed the

case; the same spike seen at 70 Hz is also seen at 50Hz in the abc spectrum. The reason that this is important is that it can then be expected that one frequency in the d-q perturbation signal will result in two frequencies in the "real" world- one at the nominal frequency plus the d-q signal frequency, and one at the nominal frequency minus the d-q signal frequency. This fact can be seen in the spectral content of the rest of the perturbation signals, as well.

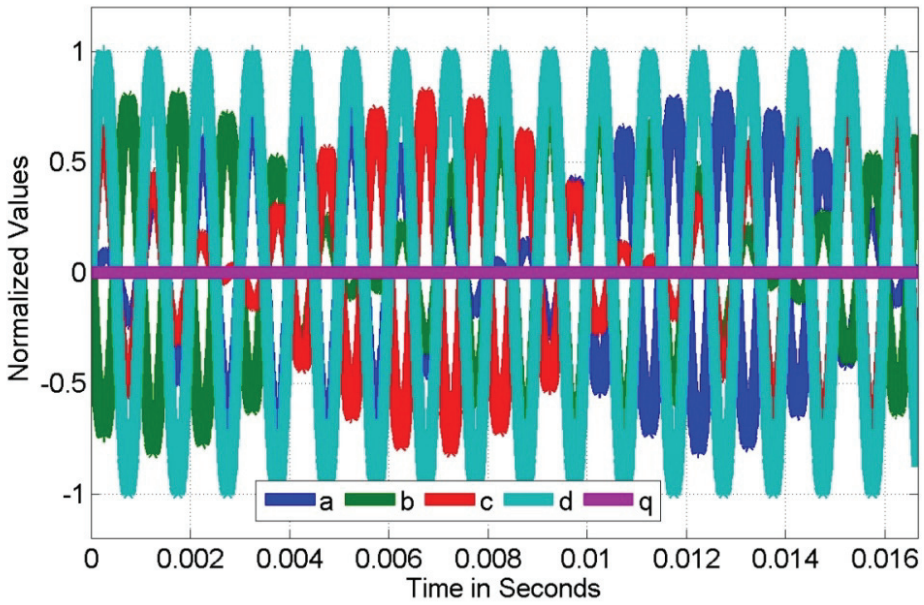

Figure 2.5: abc Waveforms Translated from a 1000 Hz Sine in d of Amplitude 1

The second easiest perturbation signal to understand is the sinusoidal signal, although the jump in complexity from the pulse signal is significant. Truth be told, Figure 2.5 looks like an incomprehensible mess. Viewing just the "a" channel, which is the same as the "b" and "c" channels translated by 120° and 240° degrees, respectively, makes this perturbation signal much easier to understand.

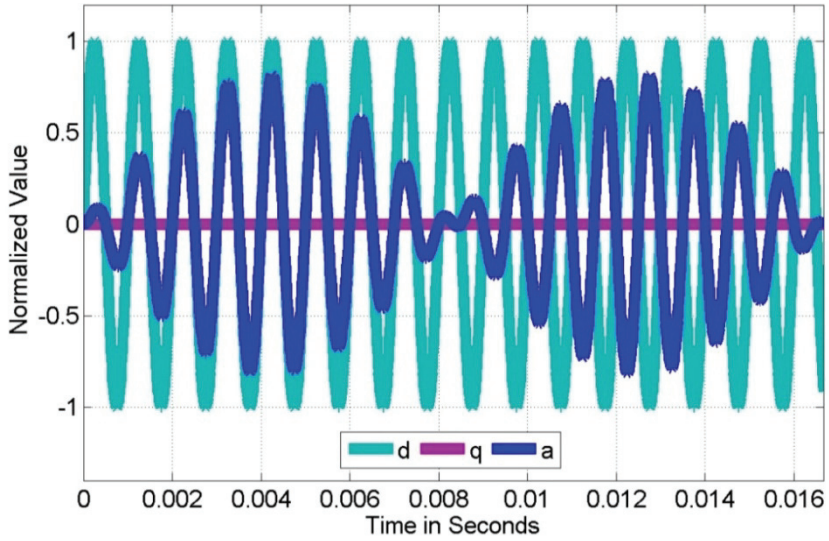

Figure 2.6: "a" Waveform Translated from a 1000 Hz Sine in d of Amplitude 1

When a d or q sinusoid is translated into the abc domain, the resulting waveform contains both the d-q rotational frequency and the d or q sinusoid frequency, resulting in the "beat" waveform seen in figure 2.6. As can be seen, the RMS value of the "a" waveform is less than in the pulse waveform; it is the RMS value of the d-q sinusoid multiplied by $\sqrt{3}/3$, or the amplitude of the d-q sinusoid multiplied by $1/3$.

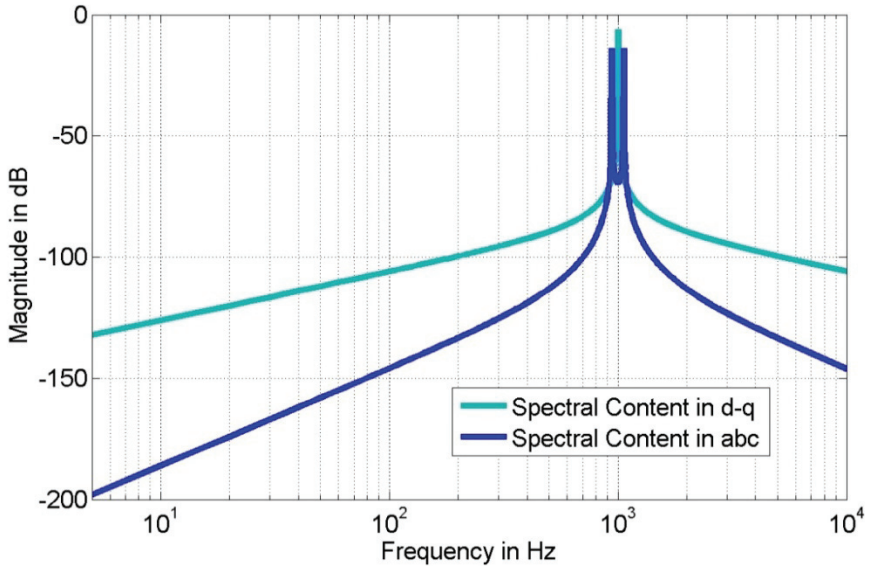

Figure 2.7: Spectral Content of the d-q Sinusoidal Signal in d-q and abc Reference Frames

The specific sinusoid studied here is the same as the one shown in figure 2.6. As expected, the d-q spectral content of this waveform has one peak at 1000Hz. The peaks in abc also appear as before at the d-q rotational frequency plus or minus the nominal frequency. In this case, there is indeed a peak at -940Hz, and being that the negative frequency range must be a perfect mirror of the positive frequency range, this peak also appears at 940Hz. This waveform is basically only good for the sinusoidal frequency response estimation method described in the previous section; the spectral content is very weak at all locations except the sine's frequency.

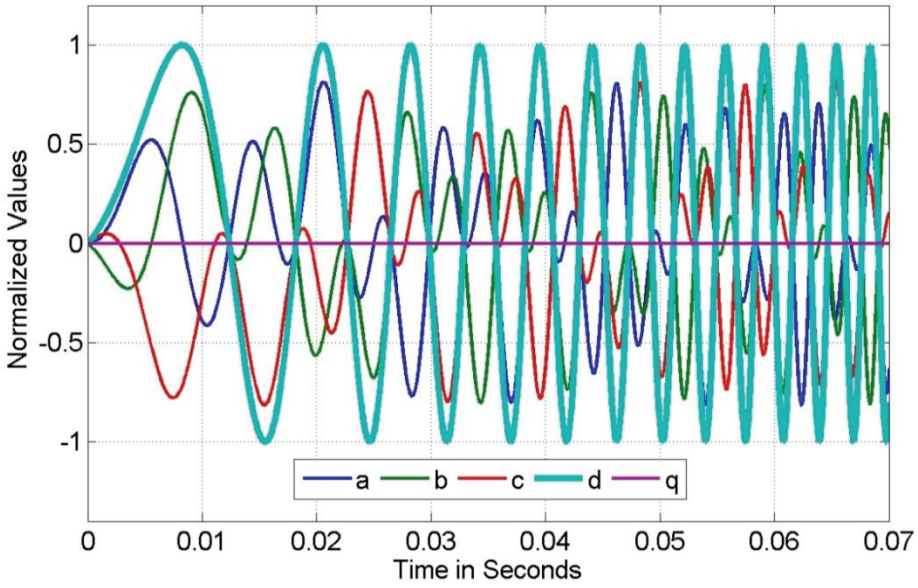

Figure 2.8: abc Waveforms Translated from a 10Hz-1000Hz in .2s d-q Chirp Signal of Amplitude 1

If the time-domain waveforms of the chirp signal look a lot like the sinusoidal time-domain waveforms, it's because that's exactly what they are. The chirp is a variable frequency sinusoidal signal that usually starts at a low frequency and sweeps to a high frequency. At frequencies lower than the d-q rotational frequency, the waveform looks slightly different than at frequencies higher than the d-q rotational frequency, but the power analysis is the same, provided the sampling time is longer than the lowest chirp frequency. Because the RMS value of a sine wave is the same regardless of frequency, a

chirp will constant magnitude will once again result in a RMS value for each phase of $1/3$ times the chirp magnitude.

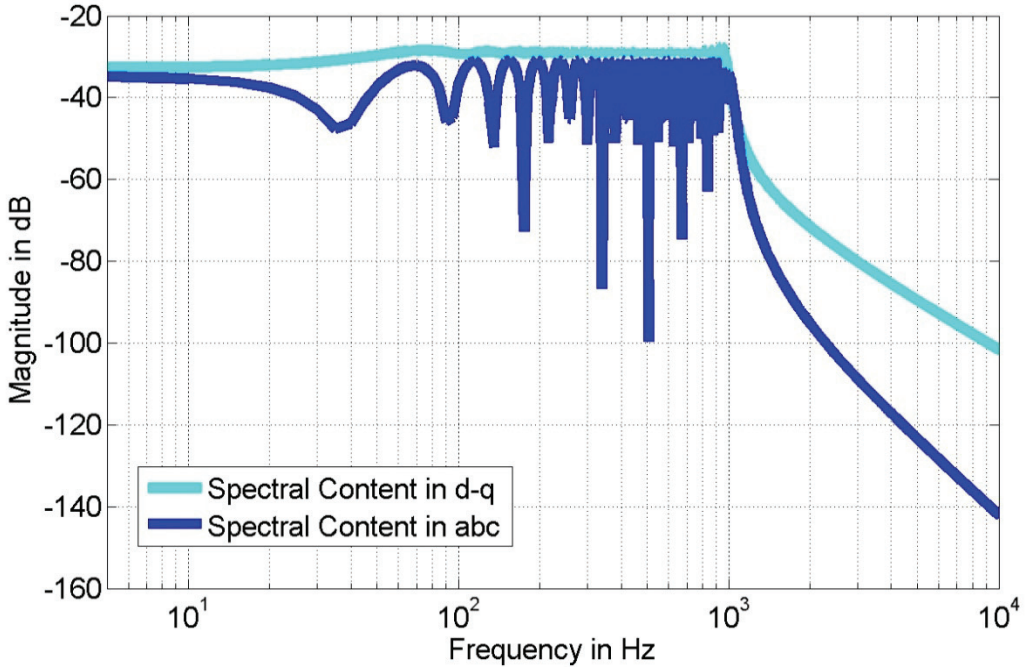

Figure 2.9: Spectral Content of the d-q Chirp Signal in the d-q and abc Reference Frames

Figure 2.9 illustrates the usefulness of the chirp signal to system identification; it has a wide rich spectral content band. This signal is expected to be of the most use in the stability analysis device.

It is worth noting here that given enough time, all of these perturbation signals are of reactive power if a long enough time scale is used, with the exception of the chirp. This is not to say that they are all in the q channel, but rather that since they are symmetric about 0, they result in 0 net power transfer. They all require instantaneous power, but after a long enough time, that power will be returned to its source. The chirp signal is mostly reactive, but since it spends a different amount of time being positive and being negative, there is a slight amount of net active power. These facts will be especially important in the "DC Link Capacitor Selection" portion of the next section.

3. Power Stage Design

3.a Power Stage Specifications

The design of the power stage warrants some discussion, if only to impart the reader with some of the special limitations and considerations inherent in the use of a traditional three-phase inverter for this particular application. The topologies discussed in this section have been used for a time period in excess of 30 years, and are discussed in detail in reference [2]. In the practical realization of them presented here, off-the-shelf parts were used wherever possible.

Being that this waveform generator is to be used as part of a greater overall project, there are not only performance specifications to adhere to in the design, but in some cases there are also hardware specifications. The table below is presented again because it sums up all of the specifications provided at the beginning of the design.

Performance Mark/ Device Specified	Specification Value
Bus Power, Nominal	100kW
Bus Voltage, line-to-line, Nominal	460VAC RMS
Injection Power, min	1% of nominal Bus Power (1.0kW)
Injection Power, max	10% of nominal Bus Power (10kW)
Power Source	120VAC RMS and Bus Only
Frequency Range of Interest	.1-1000Hz
EMI Filter	Differential and Common Mode
Switching Equipment	American Superconductor PM 1000
Control Board	Dr. Herbert Ginn's Control Board for the PM1000
Injection Modes	Shunt and Series

Table 3.1: Performance and Hardware Specifications

Notice that some specifications are numerical, while others are far vaguer. For example, there was no specification for EMI performance made, but rather simply that there should be a filter that acts both in the common and differential modes. This is due to the fact that it's currently somewhat unknown what's required of a perturbation device for this

type of power system in order for successful system identification to be achieved. Therefore, much of this design uses components of common structure, architecture, and packaging with other components of slightly different values. For example, the EMI filter chosen for this injector is the MTE RF3-0018-4. Most of the reasons for this selection will be outlined later in this thesis. One reason for this, however, is that this unit shares a mounting footprint with the MTE RF3-0025-4. If more injection power or greater common mode attenuation proves necessary, the move to the higher-power EMI filter would be a trivial undertaking. There are several examples of this that will be fully explained later in this section.

"Shunt" and "Series" modes of injection refer to the manner in which the perturbation signal is introduced to the bus, as stated in the "Goals" section of the introduction. The "shunt" mode introduces an extra (more or less) controlled current to the bus without controlling the entirety of the current already on that bus. The "series" mode introduces an extra (more or less) controlled voltage to the bus without controlling the entirety of the voltage already on the bus. Both methods are useful in different situations. When using shunt injection, the current introduced to the bus will split between the source and load directions in amounts proportional to the ratio between the source and load impedances. If one of these two impedances is exceedingly low, almost all of the current will go towards that impedance, making measurement of the other, larger, impedance exceedingly difficult. In series injection, the current through the source impedance and load impedance is equal; only the voltage is changed. There are also disadvantages to series injection, but they become more visible once the practical implementation of each mode is shown, which is done in figure 3.1.

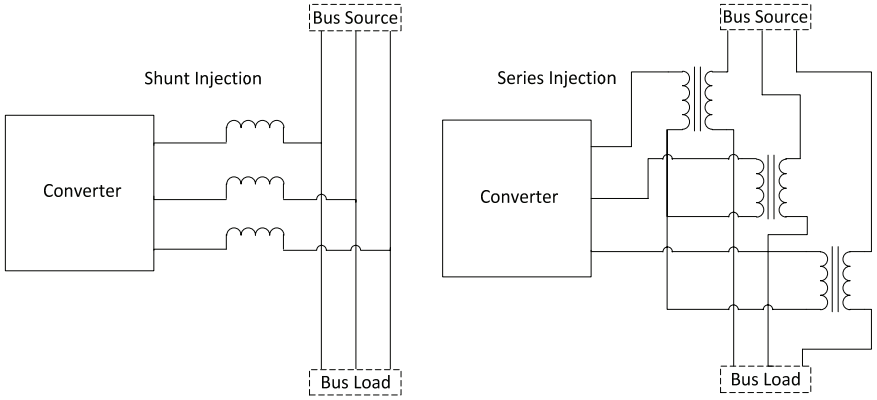

Figure 3.1: Shunt and Series Modes of Injection, Practical Implementation

Series injection requires adding a controllable voltage source in series with the bus, much like connecting batteries in series to increase voltage. Practically at this power level, the easiest way to do this is with transformers. Unfortunately, this introduces a lower limit to the frequency of perturbation. As shown in the section "Arbitrary Waveforms in d-q", frequencies close to 60Hz in d-q have peaks in the abc domain at low frequencies. Every transformer has a lower frequency limit at which the core will saturate, and the transformer will cease to work. Therefore, there's a finite band of frequency in which the series injection method will be unable to measure d-q realm impedances. The shunt method, having no transformers, is able to identify across the entire frequency band.

Extensive analysis can be performed in the selection of output filter components for a 3 phase inverter. This analysis can greatly benefit noise performance, efficiency, and cost. However, in this application, the level of noise that the identification side of the analyzer can handle is unknown, and being that this is a measurement device rather than a power converter to be used for power delivery, efficiency is not the highest priority in design. However, there are hard limits that will be explained later that limit the values of the output filter components. Up to the point where the low pass filters of the output filter start to attenuate the highest frequency of interest (1060Hz in this case), larger output components result in better noise performance. Therefore, the largest components that still satisfy the hard limits inherent in the hardware specifications will be used for output filter construction. If the noise present with these filters proves too great for the system identification apparatus, there must be a way built into the system to allow for greater attenuation, albeit at the price of lower injection power.

3.b Shunt Injection Power Stage

The American Superconductor PM1000 model provided for this waveform generator is the 820V DC link, air-cooled, 175kVA capable model. The schematic for this device is as follows:

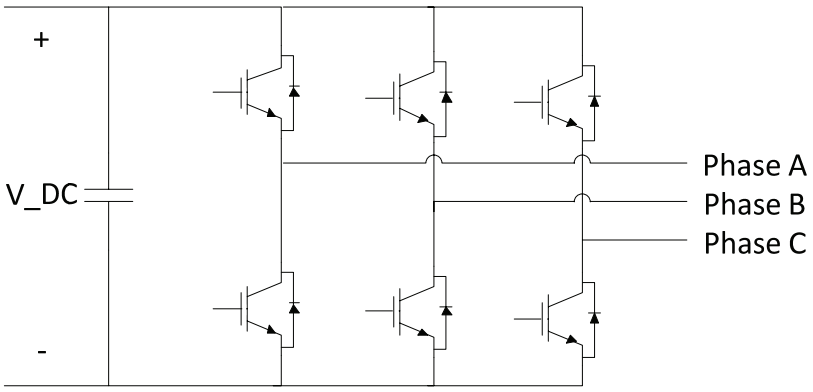

Figure 3.2: PM1000 Simplified Internal Schematic

The PM1000 also contains gate drivers, voltage and current sensors, and communications capabilities, but these are omitted for clarity's sake in this section, and only the power-stage relevant portions are shown.

Given the integral capacitor on the DC link, the Current Source Inverter topology cannot be implemented without modification of the PM1000 internals. The far easier option among 6 switch three-phase inverters is the Voltage Source Inverter. A simplified schematic of this topology is presented below.

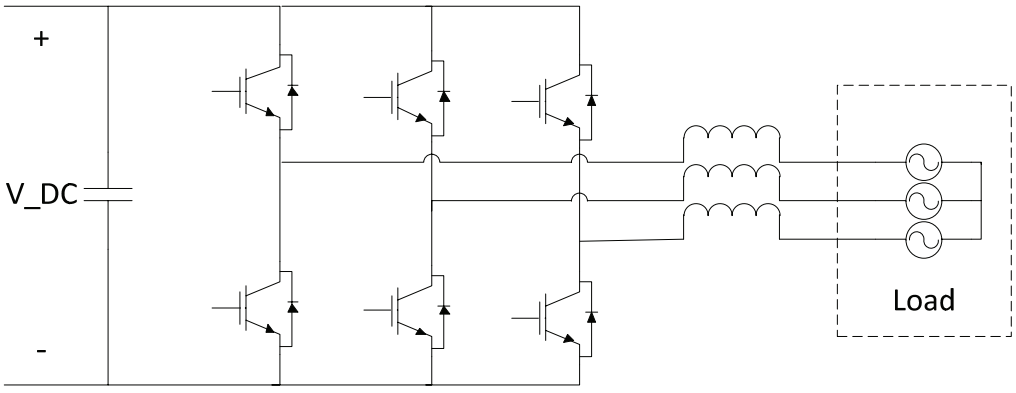

Figure 3.3: Simplified VSI Schematic for Current Injection

Note the "Load" cell. The load isn't really part of the converter, but it must be considered when designing the converter. In this case, the converter will be used to inject a perturbation onto a 3 phase bus. The voltage will indeed change, as if it didn't, the impedance would be 0. However, the perturbation is being designed here to be of a strength that is 1% of the nominal bus power. Therefore, a simplification of the load from a bus of unknown composition to a constant voltage load will greatly simplify the power stage and the closed loop control design.

Given that 10kW is the maximum injection specified, the current handling capability of this device is more than capable to handle anything that it may see during use in this application. However, the nominal DC link voltage leaves something to be desired. In this application, 1.5kW of perturbation must be possible at all frequencies of interest. Being that the impedance of an inductor increases as frequency increases, this is a problem of greatest concern at 1000Hz, the maximum perturbation frequency. As shown in figure 3.11, the 1000Hz d-q perturbation shows up in abc as 940Hz and 1060Hz. Therefore, the maximum frequency used in these calculations will be 1060Hz. Also, the load in this case is a bus operating at 460V RMS. Therefore, the maximum inductance allowable in the power stage while still satisfying the minimum power injection specification for the channel in phase with the bus voltage (the d channel) can be calculated as:

(3.1) $$Z_{max\_powerstage} = \frac{V_{available}}{I_{min}}$$

(3.2) $$V_{ph} = \frac{V_{ll}}{\sqrt{3}} = \frac{460V}{\sqrt{3}} = 266V\ RMS,\ 376V\ Peak$$

(3.3) $$I_{min} = \frac{1500W}{3*266V} = 1.88A\ RMS,\ 2.65A\ Peak$$

(3.4) $$V_{available} = 1.15\left(1 - \frac{T_{dead}}{T_s}\right)\frac{V_{DC}}{2} - V_{bus_{peak}} = 1.15\left(1 - \frac{.000002}{.00005}\right)\frac{865}{2} - 376V = 101.48V$$

(3.5) $$Z_{max\_powerstage} = \frac{101.48V}{2.65A} = 38.29\Omega$$

(3.6) $$Z_{max\_powerstage} = 2\pi * f_{max} * L_{max} = 38.29\Omega = 2\pi 1060 * L_{max}$$

(3.7) $$L_{max} = 5.75mH$$

These calculations have been done with phase-to-neutral voltages because these voltages make inductance calculations slightly easier than line-to-line voltages; the calculations could also be done in with line-to-line voltages.

There are several requirements that these numbers put on the remainder of the design. Notice that the DC link voltage has been raised from the nominal of 820V to a voltage of 865V. Being that the available voltage is so low when the nominal operational voltage is used, the 80V margin of safety between the 820V nominal and 900V maximum has been cut into. In between perturbations, the DC link voltage will be much lower than the 820V nominal; only right before perturbation will the voltage be raised to 865V. This is safe, but requires very good overvoltage protection and very slow DC voltage regulation. This will be further discussed in the protection and control sections of this thesis.

Another requirement that these calculations put on later design is the now mandatory use of Space Vector Modulation or similar 3rd harmonic injection PWM scheme. The DC voltage used for phase-to-neutral based voltage calculation is half of the DC link voltage times 1.15. Unless 3rd harmonic injection is used, this voltage is not available.

The last requirement is the requirement that these calculations were designed to produce in the first place; the maximum inductance. Figure 4.2 is a simplification of the final circuit used only for preliminary calculations. The final circuit will include more than one inductor per phase, and these inductances must add up to less than the maximum inductance calculated above.

A common method of incorporating a differential mode EMI filter into the power stage of a VSI intended for current control only (as is the case with “shunt” injection) is to add a capacitor and an extra inductor to each phase leg in figure 4.2, realizing what is known as an “LCL” filter.

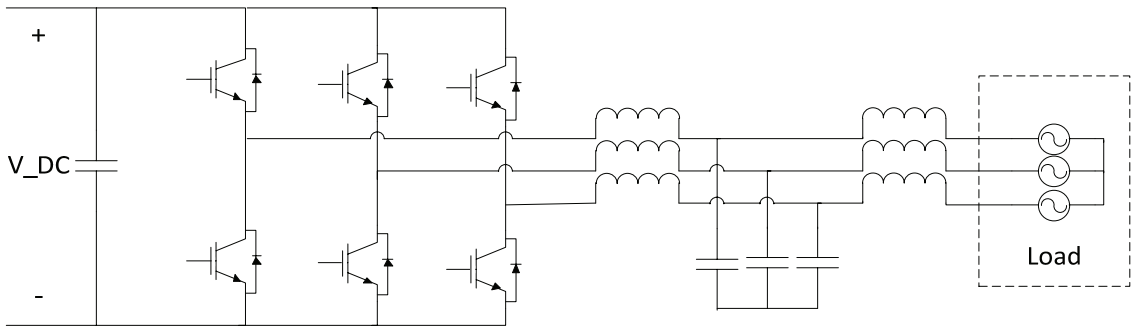

Figure 3.4: LCL Output Filter Topology as Realized with a VSI

The sum of these two inductances must be less than 5.74mH, they both must be able to withstand constant operation at 460V RMS between lines and 266V RMS to ground, and they both must be able to handle the amperage associated with the maximum injection power of 10kW.

(3.8) $$I_{maxrms} = \frac{P_{max}/3}{V_{rms}} = \frac{10000W/3}{3*266V} = 12.5A$$

While the impedance of the inductors limits the active power injection to 1.5kW, the reactive power injection can reach much higher values, as will be seen in the PLL section of the "Closed Loop Control Design" chapter.

Lastly, the first inductor will be fed a square wave voltage of a range equal to the DC voltage, so it must be "PWM friendly." Two off-the-shelf parts that fit all of these requirements nicely are the MTE RL-01803 three-phase inductor and the Vishay-Dale IHV-15-500.

Device	Current Rating, A RMS	Voltage Rating, V RMS Nominal	Dielectric Voltage Strength, V RMS	Inductance
MTE RL-01803	18	690	3000	2.5mH/Phase
Vishay IHV-15-500	15	unrated	707 minimum	.5mH

Table 3.2: Inductor Selection

If it's determined that too much switching noise or not enough power is present in the perturbation to achieve successful impedance measurement, the MTE device shares most of a mounting footprint with 13 other MTE three-phase inductor models with current ratings of power ratings from 18A RMS to 55A RMS and inductances from .3mH to 1.3mH. A 4.2mH device is also available at 12A RMS of current capability, but this one would require some mounting hardware modification. The compact nature of the Vishay device (2.45"x1.45") allows provisions for multiple inductor mounting easy to accommodate, and similar package inductors are available down to 24uH should fine-tuning of output inductance prove necessary.

The upper limit of the capacitance portion of the LCL filter can be determined by setting an upper limit to the circulating energy at the nominal frequency of operation.

(3.9) $$I_{circ} = \frac{V_{ph_{rms}}}{Z_{cap}} = \frac{266}{\frac{1}{2\pi 60 C_{max}}}$$

For an upper limit of 5% circulating energy,

(3.10) $$.05 * 12.5 = \frac{266}{\frac{1}{2\pi 60 C_{max}}}$$

(3.11) $$C_{max} = 6.23\mu F$$

Given that there's also a binary requirement for a common-mode EMI filter, it makes sense to include this capacitance as part of an EMI filter structure known as a "Pi Filter"

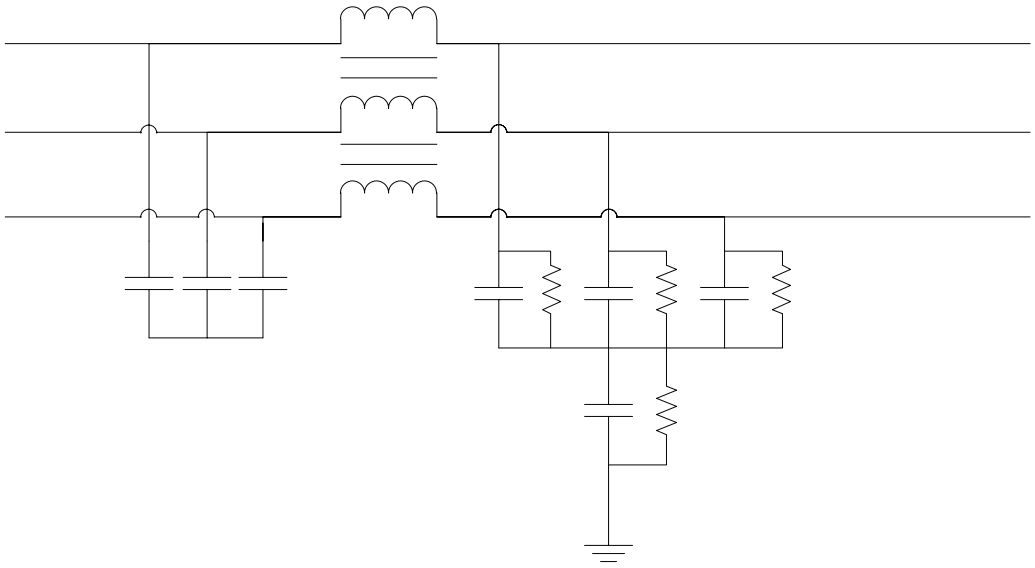

Figure 3.5: Generic “Pi Filter” Structure

The beauty of the “Pi Filter” lies in that when it is viewed from the common mode perspective, there’s an LC filter to ground comprised of the mutual inductance and only the capacitance that goes to ground, but when viewed from the differential mode perspective, only two capacitances per leg in parallel, or, equivalently, one capacitance per leg, is visible. This makes it a very easy way to incorporate a common mode EMI filter to a three-phase inverter power stage while simultaneously adding the necessary capacitance for the differential mode filter. The MTE RF3-0018-4 contains a total capacitance of 4uF per phase, which falls under the maximum capacitance specified by the circulating current requirement. In addition, it’s designed for continuous operation on a 480V bus at 18A RMS. Lastly, as stated previously in this section, it shares a common package with the RF3-0025-4, which is an extended version of the “Pi Filter” that has a 4^{th} order common mode EMI filter as opposed to the 2^{nd} order shown here, as well as a 25A RMS continuous rating. If greater common-mode noise attenuation or greater injection power proves necessary, this upgraded version of the filter chosen could easily be swapped in.

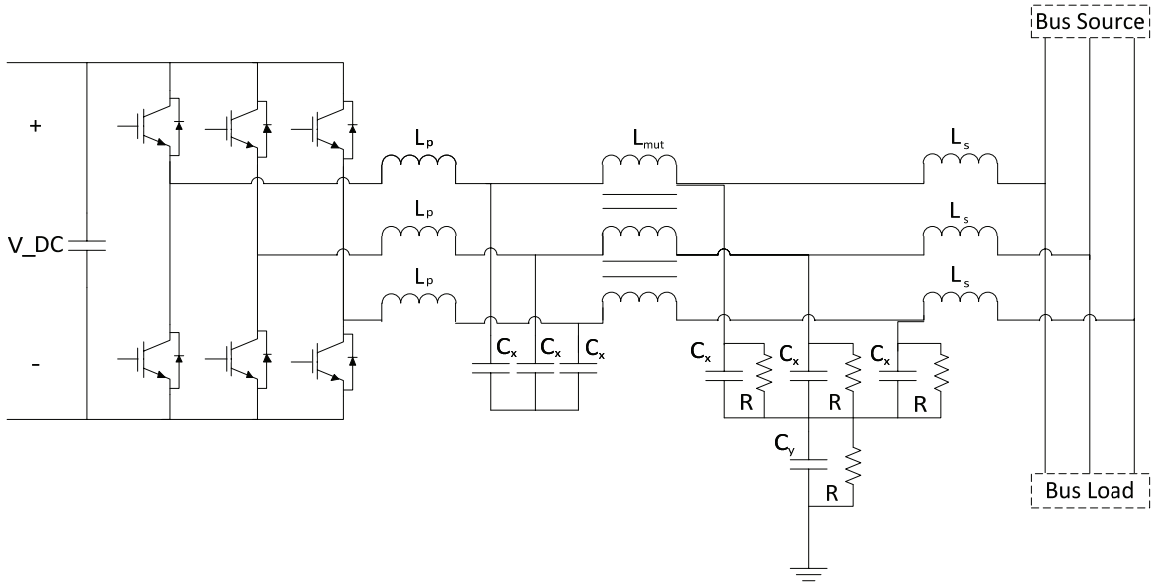

Figure 3.6: Complete Shunt Injection Power Stage

Component	Value
L_p	2.5mH
L_s	.5mH
L_m	3.5mH
C_x	2µF
C_y	1µF
R	1MΩ

Table 3.3: Shunt Injection Power Stage Schematic Component Values

For all of the apparent complexity of this circuit, it is entirely contained in 6 individual commercial products and 4 individual orderable part numbers.

Part	Manufacturer	Part Number
3 Phase Inductor	MTE	RL-01803
EMI Filter	MTE	RF3-0018-4
Shunt Output Inductor	Vishay/Dale	IHV-15-500
Switching Equipment	American Superconductor	PM1000

Table 3.4: Shunt Injection Power Stage Commercial Components

With these components, the maximum output power in the d channel is:

(3.12) $$Z_{ind\_powerstage} = 2\pi * f_{max} * L_{tot} = 2\pi * 1060 * .003 = 19.98\Omega$$

(3.13) $$Z_{ind\_powerstage} = \frac{V_{available}}{I_{abc-max}} = \frac{101.48V}{I_{abc-max}} = 19.98\Omega$$

(3.14) $$I_{abc-max} = 5.079A = 3.591A\ RMS$$

(3.15) $$3.591A * 266V * 3 = P_d = 2865.98kW$$

3.c Series Injection Power Stage

The most important parts of the series injection power stage are the transformers. All other components must merely comprise a circuit that feed these devices voltage and current waveforms that the transformers find acceptable. Ideally, at the end of each phase leg there would be a transformer with an infinitely large core that can transform DC power from its primary to its secondary. Practically, this is difficult. As stated in the "Power Stage Specifications" section and illustrated in the "Arbitrary Waveforms in d-q" section, frequencies close to d-q rotational frequency (60Hz here) in d-q produce frequency content close to 0Hz when translated into abc, which is the world that the transformers must operate in. Therefore, when a lower frequency limit is specified for the transformers, this results in a frequency band across which no measurements can be made in d-q that is equal in range to twice the lower frequency limit of the transformers and centered about the d-q rotational frequency. In addition, the relationship between lowest frequency of operation of a transformer and the size (and therefore the cost) of the transformer is logarithmic. A transformer designed to operate at 20Hz can be expected to be twice the size of a transformer designed to operate at 40Hz, and a 10Hz transformer to be twice the size of the 20Hz transformer. Begrudgingly, the lower frequency limit of the transformers was specified to be 40Hz by the team responsible for the measurement and calculation portion side of the impedance measurement device.

This is where the bad news ends, however. The design of the rest of the series injection stage is much more forgiving than the design of the shunt injection stage. The most versatile aspect of designing a circuit with a transformer is that a turns ratio can be

specified that makes the design of the rest of the circuit easier. Being that the series injection is the dual of the shunt injection in that it purposely varies voltage instead of current, the power calculations will be done in terms of voltage instead of current here.

(3.16) $$V_{inj-max} = 10\% * 266V = 26.6V\ RMS$$

(3.17) $$V_{inj-min} = 1\% * 266V = 2.6V\ RMS$$

Being that the existing shunt power stage was designed for 266V RMS and a voltage of 26.6V is necessary for 10% perturbation, it makes sense to specify that the transformers have a turns ratio of 10:1. Now that the voltage, turns ratio, and frequency of operation specifications have been made, and in the knowledge that the primary side of the transformers and the associated circuits have requirements that have been made to match the requirements of shunt injection, the shunt injection calculations can be re-used to determine the current specifications of the transformers.

(3.18) $$I_{max-primary} = 12.5A\ RMS$$

(3.19) $$I_{min-primary} = 1.25A\ RMS$$

With a 10:1 turns ratio, this results in a secondary maximum current of 125A RMS. Sadly, these calculations were performed incorrectly at the time of transformer construction. The result was 3 transformers over-rated for current and under-rated for voltage. The final transformer specifications are:

Specification	Value
Turns Ratio, Primary: Secondary	10:1
Primary Windings Maximum RMS Voltage	200V
Secondary Windings Maximum RMS Voltage	20V
Primary Windings Maximum RMS Operating Current	20A
Secondary Windings Maximum RMS Operating Current	200A
Overall Dielectric Strength to Ground	650.5V min
Lowest Frequency of Continuous Operation	40Hz

Table 3.5: Series Injection Transformer Specifications

The dielectric strength to ground value of 650.5V represents the peak value of 460V line-to-line RMS. It has been untested, and is probably far greater than this value, but has been guaranteed to be at least this value.

The 20V secondary side rating reduces the maximum output power to 7.5% of the nominal bus power, or 7.5kW. Were this device to be reconstructed, this upper voltage value should be changed.

A transformer should not be connected to an inductor directly. If this is done, in the best case the connected inductor is in series with the leakage inductance of the transformer, and is simply effectively absorbed. However, if there is a switch between these two inductances, the worst case may happen. If there are different currents moving through the two inductances when they are connected by the switch, they "fight", usually resulting in a discharge across a parasitic element or the air and damage of some component. Therefore, in this design, a capacitor will be connected to the input of the transformer.

Because of the design of the transformer, the portions of the power stage leading up to the transformer now have the same requirements placed on them as the shunt injection power stage. If the output inductor is removed from the shunt power stage, then it can be re-used for the portion of the series power stage necessary for feeding the primary side of the transformer. The resulting circuit is shown below.

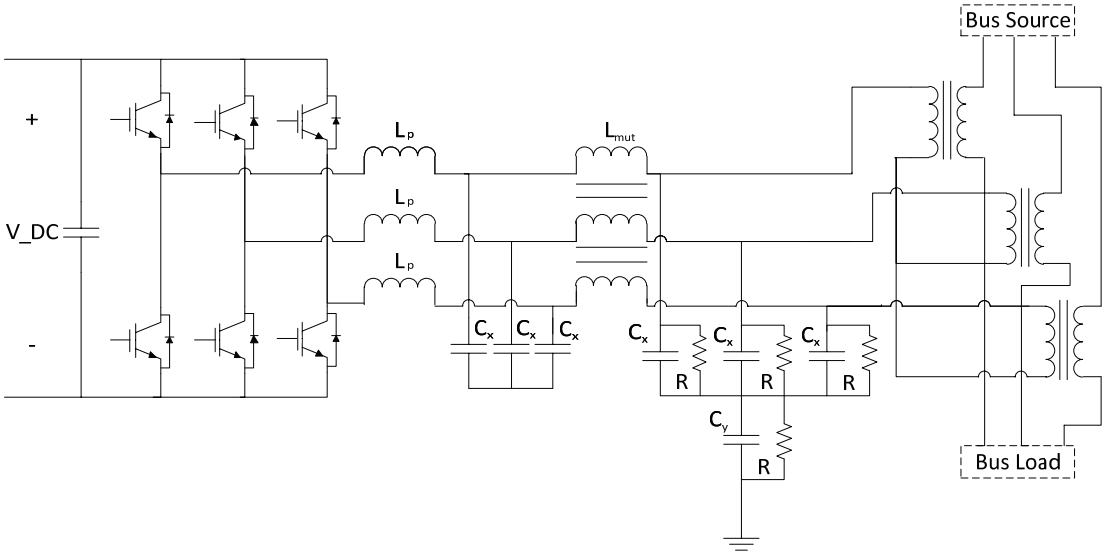

Figure 3.7: Series Injection Power Stage

Magnetics design is a complex enough subject that many people specialize in and are employed entirely for the purpose of designing inductors and transformers. While the design and construction of the actual device is possible for an amateur such as those working on this particular project, the time constraints placed on this project make this unfeasible, and the result would be an inferior product to one designed and built by a professional. Therefore, these specifications were provided to a professional magnetics designer, and the design/construction work outsourced.

The transformer can be modeled as an ideal transformer with a magnetizing inductance in parallel with the primary windings and a leakage inductance in series with the primary windings.

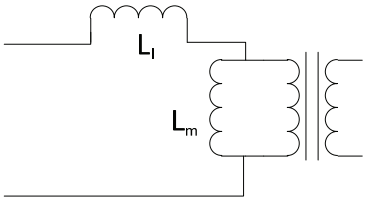

Figure 3.8: Model of a Transformer with Parasitic Inductances

Being that the leakage inductance is in series with the ideal transformer windings, it can play the same role as the output inductor in the shunt injection system and decrease the

maximum possible output power. However, this value is typically much, much less than the .5mH of the output inductor. If there were no leakage inductance, the maximum output power in the d channel would be

(3.20) $$Z_{ind\_powerstage} = 2\pi * f_{max} * L_{tot} = 2\pi * 1060 * .0025 = 16.65\Omega$$

(3.21) $$Z_{ind\_powerstage} = \frac{V_{available}}{I_d} = \frac{101.48V}{I_d} = 16.65\Omega$$

(3.22) $$I_d = 6.09A\ max, 4.30A\ RMS$$

(3.23) $$4.30A * 266V * 3 = P_d = 3431.4kW$$

The limit that the voltage rating on the transformer induces on the system is:

(3.24) $$\frac{V_{pert}}{V_{nom}} * P_{nom} = \frac{20V}{266V} * 100kW = 7518.8kW$$

This result shows that the error in transformer specification calculation doesn't affect the maximum injection power at high frequency at all, but limits the lower frequency injections by 25%.

3.d DC Link Capacitor Specification

One of the things that makes this perturbation device special is that it requires no external power source except standard household 120V AC. One of the ways to accomplish this is to place a large enough capacitor on the DC link of the VSI to hold all the energy necessary for a perturbation of sufficient energy to result in successful impedance measurement. The question then becomes "How much energy is required in these perturbations?"

As shown in the section "Arbitrary Waveforms in d-q", the d-q power is equal to the abc power given that a scaling factor is used in the Clarke transform. Therefore, all calculations done here will be done with the d-q values. As also shown in this section, the abc RMS power per phase of the d-q pulse signal is equal to the magnitude of the pulse multiplied by $\sqrt{3}/3$, provided that the pulse is symmetrically bi-directional. The RMS powers of the chirp and sine perturbation signals are equal to $\sqrt{6}/6$ times the peak

of the chirp or sine signal. Finally, it was also discussed in that section that all of these signals except for the chirp are reactive in power given a long enough time scale due to the fact that they are equally positive and negative. Therefore, they all only require enough energy to produce the signal for the longest strictly positive or strictly negative portion of the signal.

One amp for one second is one coulomb, so the easiest way to determine the maximum energy drain on the DC link capacitor is to take the integral of each perturbation signal with regard to time. The pulse signal is a piecewise linear signal. For the positive portion of the pulse, the time integral is a positive ramp with slope equal to the pulse magnitude, and for the negative portion of the pulse, the time integral is a negative ramp with slope equal to the pulse magnitude. The result is a "triangle" waveform.

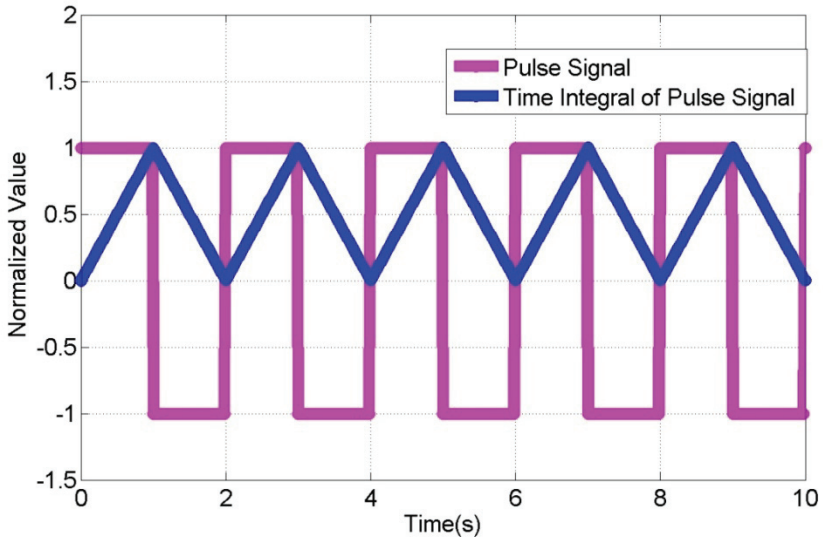

Figure 3.9: Pulse Signal of Magnitude 1, Period 2s, Duty Cycle of .5, and its Time Integral

The longest pulse signal to be used will be of 10 seconds (.1Hz) at 50% duty cycle, and if the maximum power is used, the largest energy expenditure will be

(3.25) $Q_{max-pulse} = (duty\ cycle)(1/f_{min})(I_{max-rms}) = .5 * 10s * 12.5A = 62.5C$

For the same waveform at the minimum injection power, the energy expenditure is:

(3.26) $Q_{min-pulse} = (duty\ cycle)(1/f_{min})(I_{min-rms}) = .5 * 10s * 1.88A = 9.39C$

The sinusoidal signal has the simplest integral; it's simply the sine magnitude multiplied by negative cosine multiplied by the period of the sine.

(3.27) $$\int x \sin(2\pi f t) = -\frac{x}{2\pi f}\cos(2\pi f t)$$

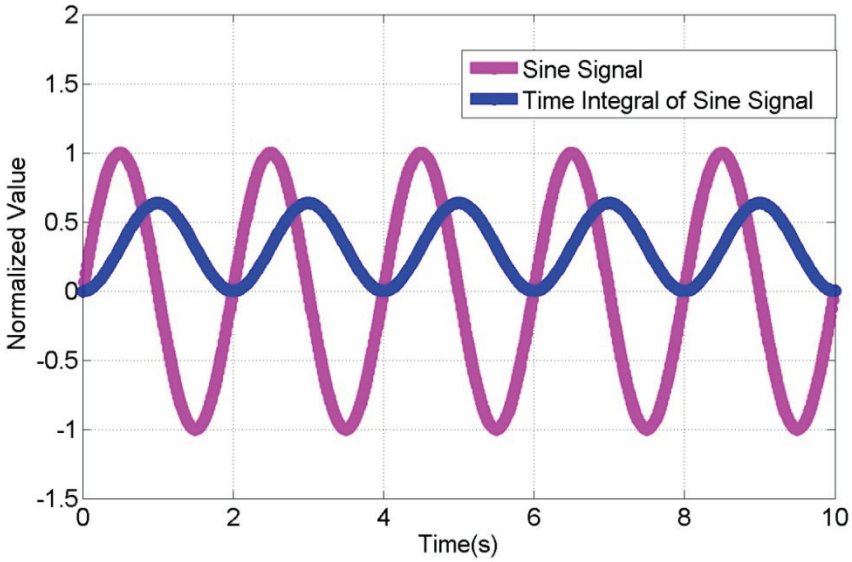

Figure 3.10: Sine of Magnitude 1, Period of 2s, and its Time Integral

As the period gets larger, the integral gets larger. Therefore, the largest energy expenditure while using the sine wave signal will come at .1Hz. Using maximum and minimum injection currents:

(3.28) $$Q_{max-sine} = -\frac{I_{maxpeak}}{2\pi f_{min}}\max(\cos(2\pi f_{min} t)) = -\frac{12.5\sqrt{2}}{2\pi(.1)}1 = 28.13\text{C}$$

(3.29) $$Q_{min-sine} = -\frac{I_{minpeak}}{2\pi f_{min}}\max(\cos(2\pi f_{min} t)) = -\frac{1.88\sqrt{2}}{2\pi(.1)}1 = 4.23\text{C}$$

The chirp signal has the most interesting integral. The chirp signal itself can be represented in the time domain as:

$$(3.30) \quad y = x\sin\left(2\pi f_{min}t * f_{max}t * T_{chirp}\right) = x\sin\left(2\pi f_{min}f_{max}T_{chirp}t^2\right)$$

Here, f_{min} is the minimum frequency of the chirp, f_{max} is the maximum frequency of the chirp, and T_{chirp} is the time that the chirp should take to sweep from minimum to maximum frequency.

There is no exact numerical solution for the integral of this function currently available in mathematics. The series of the Fresnel integral is commonly used to approximate the numerical values, however [13].

$$(3.31) \quad S(z) = \int_0^z x\sin\left(2\pi f_{min}f_{max}T_{chirp}t^2\right) \approx \sum_{n=0}^{\infty} \frac{(-1)^n\left(2\pi f_{min}f_{max}T_{chirp}\right)^{2n+1}z^{4n+3}}{(2n+1)!(4n+3)}$$

Were one so inclined, one could approximate an infinite series for many time steps in order to get a curve that shows the maximum energy expenditure of a given chirp signal. However, this process has a habit of crashing even advanced mathematical software packages run on powerful engineering workstations. A much simpler solution, in this case, is simply to use Simulink's capability to approximate integrals by simulating in the time domain.

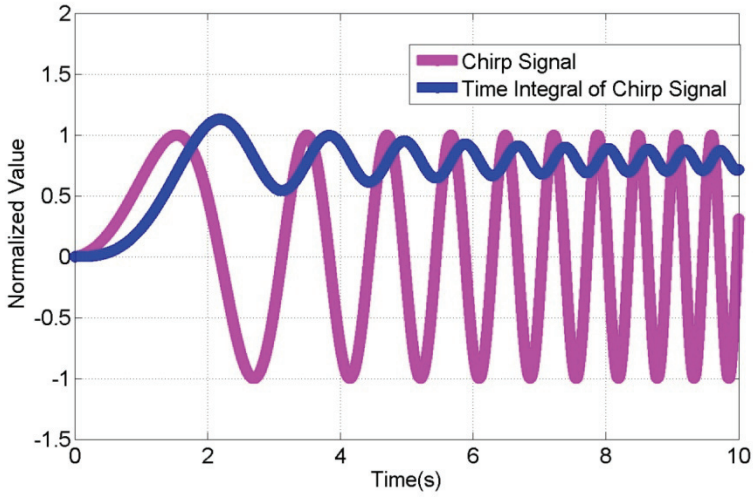

Figure 3.11: Chirp of Magnitude 1, Frequency Range of .01Hz-2Hz over 10s, and its Time Integral

Chirp functions have integrals that have an offset from zero due to the extra time spent in the beginning of the chirp above zero, but quickly arrive at that offset and then behave similarly to the sine integral. Therefore, the largest energy expenditure will happen at the beginning of the chirp, and will be greater for chirps that spend more time at lower frequencies. The measurement and analysis team on this project specified a 30s chirp from .1Hz to 1000Hz as the chirp signal that will spend the most time at low frequencies.

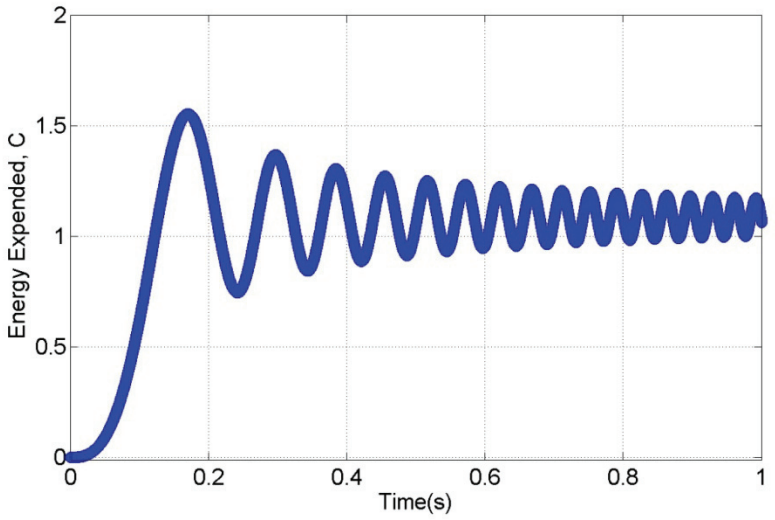

Figure 3.12: Chirp of Magnitude 17.76A, Frequency Range of .1Hz-10Hz over 30s, and its Time Integral

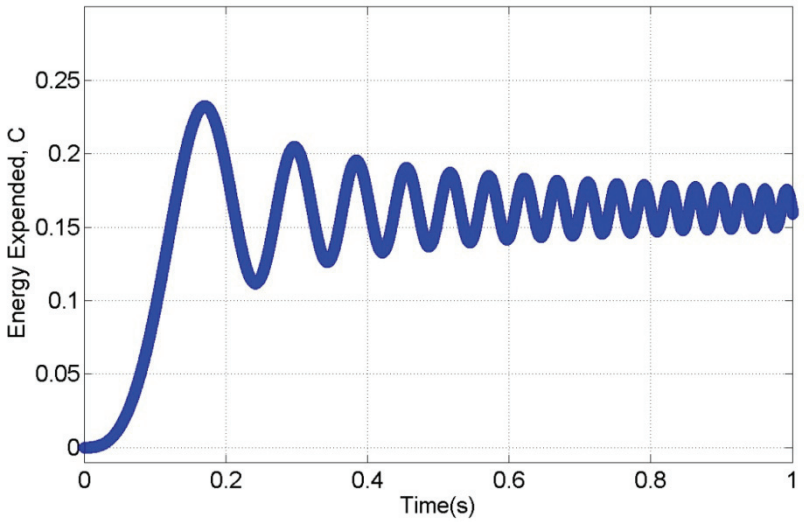

Figure 3.13: Integral of Chirp, Magnitude 2.66A, Frequency Range of .1-1000Hz over 30s

The manner in which energy expended can be related to voltage across the DC link capacitor is represented as:

(3.32) $$Q = CV$$

If an absolute maximum DC link starting voltage of 875V is used, the perturbation waveforms shown above result in the following necessary DC Link capacitances:

Signal	Energy Expenditure(C), max	Energy Expenditure(C), final	Necessary DC Link Capacitance (mF), 0.1Hz	Necessary DC Link Capacitance (mF), 1000Hz
Pulse, max power	62.5	0	516.528	n/a
Pulse, min power	9.39	0	77.603	n/a
Sine, max power	28.13	0	232.479	n/a
Sine, min power	4.23	0	34.958	n/a
Chirp, max power	1.65	1.25	5.136	83.33333333
Chirp, min power	0.23	0.17	.4136	11.33333333

Table 3.6: Necessary DC Link Capacitances for Various Perturbation Signals

The minimum DC link voltages necessary for .1Hz injection and 1000Hz injection are 650V and 860V as calculated from equations 4.1-4.7, and the associated maximum voltage drops from 875V are 15V and 220V, respectively.

As can be seen in table 4.6, some of the necessary capacitance values for these worst case waveforms are astronomical. However, not every waveform has to be used all the way down to .1Hz, and the chirp signal has multiple parameters that can be "tweaked" to produce different waveforms with different maximum energy expenditures. For example, a chirp that starts at 10Hz instead of .1Hz will require less capacitance to reach 1000Hz at a given power level. Inversely, since a very low DC link capacitance is necessary at low frequency for a .1Hz to 1000Hz chirp at minimum power, if the chirp is stopped short of 1000Hz, the power can be raised or the time to high frequency made longer, both of which increase low frequency content. In short, this table serves as a

guide when selecting a DC link capacitance and shows the worst cases at lowest frequency.

In the end, the overall team decided to work with a 13mF DC link capacitance. This results in a maximum charge expenditure of:

$$Q_{.1Hz} = 2.86C$$

$$Q_{1000Hz} = .195C$$

Furthermore, after this decision was made, the decision to incorporate a DC link controller during perturbation was made. This makes the 1000Hz charge expenditure value moot- a slow DC link controller will bring the voltage back to nominal during high frequency perturbation without much effect on the perturbation waveform. With a slow DC link controller enabled, the system must only be able to handle the lower frequency charge expenditures. This will be further discussed in the control design section.

4. Closed-Loop Control Design and Simulation

4.a General Comments about Three-Phase Control Using Fixed Point DSPs

The Ginn Control Board contains two DSPs and one CPLD. One of the DSPs remains largely unused; it is an advanced floating point DSP. The CPLD contains logic that handles protection tasks. The other DSP is fixed point, and is used for all of the sensing and control of the PM1000, as well as the communication with outside devices. In addition, the Ginn board uses a custom auxiliary board that contains all of the current sensors that the PM1000 needs for control and protection.

Communication with outside devices is done through a fiber optic link that uses TCP/IP Ethernet protocols. Communication between the fixed point DSP and the CPLD is done through analog signals. The majority of these signals are analog values formed using an on-board digital-to-analog converter and used by the CPLD as references for comparators that trip over-voltage and over-current faults. The CPLD is also connected to the PM1000's existing fiber optic transmitters and receivers, of which there are two each. Being fed by analog circuits, these have very fast response time. Here, one transmitter is used for signal synchronization with the measurement computer, the other transmitter is used to act on AC overvoltage protection signals, and one receiver is used to receive AC overvoltage signals. More on this can be found in the section "Fault Protection and Power Routing Design."

Being that the fixed-point DSP on the Ginn board is from Texas Instruments, the plethora of software tools that TI makes available for use on its fixed-point DSPs becomes available for use in this design. The two TI tools used extensively here are the "IQ Math" library and the "Motor Control" Library.

IQ Math makes use of non-integer numbers much easier on fixed-point DSPs, especially those with 32 bit computational ability. The library is incorporated into the project as a header, and allows for the definition of "_IQ" type 32 bit variables. The type of IQ variable, settable from "_iq0" to "_iq31", determines how many of the 32 bits are used for the whole number portion of the variable, and how many are used for the fractional part. A global IQ type may be set, but variables of IQ type differing from the global type may be declared and used. IQ math isn't exactly like floating-point math;

each IQ type has a different range and resolution and must be used accordingly [15]. For this waveform generator, it was found that IQ variables of type 20 worked best; these variables have a range from -2048 to 2047.999999046 in .000000954 increments.

The Motor Control Library is part of Texas Instruments' ControlSUITE software package, and is available for free download at the link in [16]. This library contains header files that define structures that contain all of the necessary variables for a function, and the functions themselves as optimized callable macros. The current version, v2.1, utilizes IQ math. Among the functions from the Motor Control Library used in the control of this waveform generator are the Park transform, the Clarke transform, Space Vector Modulation, and the PID controller. This package makes control of 3 phase systems much easier, with few exceptions.

One possible exception is the implementation of the PID controller. The TI PID scheme is fantastic for trial-and-error PI control, and includes smart anti-windup, but requires a short derivation to be used with the canonical form of the digital difference equation. This derivation is presented in appendix A.

It is also of note that the PM1000 is capable of switching at up to 20kHz, and that the Ginn board is capable of double-update sampling. Both of these facts were taken advantage of in this design, and thus the sampling frequency for all of the digital controllers in the following sections is 40 kHz.

4.b The Phase-Locked Loop

In all applications that use d-q transform-based control methods to feed into an already energized three phase bus, some method of determination of the angle of the sinusoids on the bus must be utilized. The most common of these methods is the Phase Locked Loop. Effectively, this loop senses all three voltages, transforms them to d-q, and uses a controller to change the phase angle and force the q value to zero. When this happens, the angle that the PLL produces is aligned with the active power rotating channel, the d channel [18]. A block diagram of the PLL is shown below.

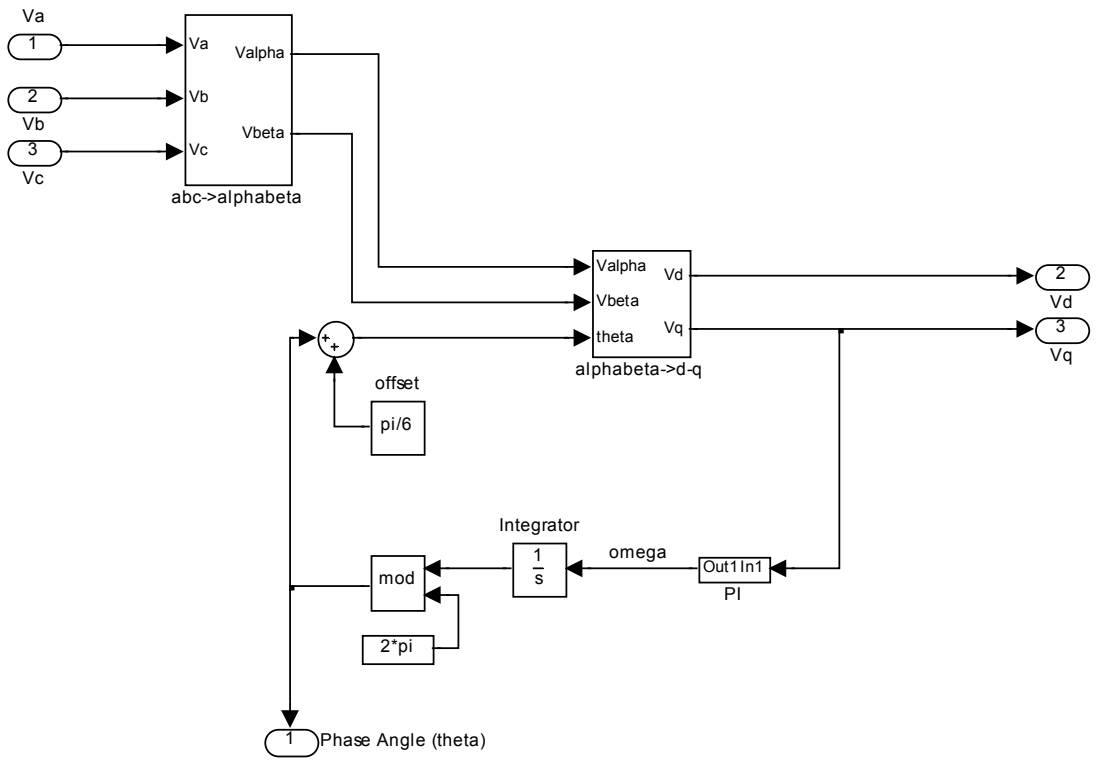

Figure 4.1: General Form of the PLL

Generally, this generalized diagram is not presented with the offset; as q is expected to go to zero, there is a reference of zero to the system. However, having an offset present is useful, especially when control is performed in phase-to-neutral values and the voltage sensors measure line-to-line voltages. The value of $\pi/6$ as an offset is shown here to remedy this situation. There are other benefits to having an offset as well, as will be shown later in this section.

The linearized open loop transfer function from θ to q is derived in Appendix B and is presented below.

$$\frac{V_q}{\theta} = \frac{\sqrt{V_\alpha^2 + V_\beta^2}}{s} \tag{4.1}$$

It can be surmised from equation 5.1 that unless there is some sort of voltage normalization in place, the bandwidth of the closed loop PLL will change as voltage changes. This is a bad thing with a PLL. For most control systems, a high bandwidth is desired; this is not the case with a PLL. The effect of a high bandwidth combined with

noise or distortion in the input waveforms can cause distortion of the phase angle. A lower bandwidth tends to reject these disturbances, although not always completely [18]. One normalization scheme is presented below.

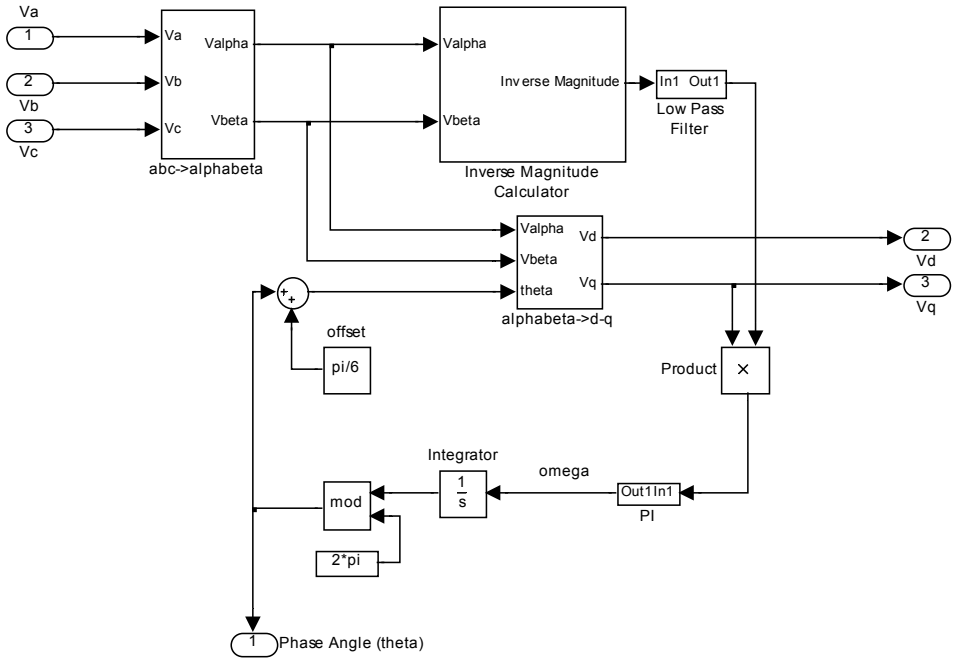

Figure 4.2: PLL with Magnitude Normalization

By multiplying the value of V_q by the inverse magnitude of the alpha-beta voltage waveforms, the open-loop transfer function can be made to be no longer dependent on voltage magnitude.

(4.2) $$\frac{V_q}{\theta} = \frac{1}{s}$$

This makes effectively controlling the bandwidth of the PLL across all voltages much easier.

The low pass filter is a simple first order Butterworth filter transformed into the discrete domain by Tustin approximation and implemented as a direct form II IIR [19], the form of which can be seen in Appendix A. The bandwidth of this filter is 5Hz. The PI filter is realized in the form that TI uses, which is also visible in Appendix A.

Given an open-loop transfer function, the PI controller can be designed. For this application, a bandwidth of 5Hz and a phase margin of approximately 90° will be the design criteria. First, an integrator must be implemented to ensure zero steady state error. Next, given that the phase will be -180° when two integrators are multiplied together, a zero must be placed at less than 1 decade below the desired crossover frequency. .5 Hz will work for this purpose. The open loop transfer function is then

(4.3) $$T_{pll} = \frac{s+3.14}{s^2}$$

The magnitude and phase at 5Hz are now:

(4.4) $$\frac{j\omega+3.14}{(j\omega)^2} = \frac{j31.45+3.14}{(j31.54)^2} = \frac{j31.54+3.14}{-994.77} = -\frac{3.14}{994.77} - \frac{31.45}{994.77}j = -.003157 -$$

(4.5) $$.031615j = .03177\angle -95.7°$$

If the desired gain is 1 at 5Hz, then the proportional gain must be:

$$K_p = \frac{1}{.03177} = 31.47$$

The PI transfer function becomes the following in both the analog and digital domains, with the continuous-to-discrete transformation being the bilinear Tustin performed at the sampling frequency of 40 kHz.

(4.6) $$C_{plls} = \frac{31.47s+98.81}{s}$$

(4.7) $$C_{pll} = \frac{31.4712-31.4712z^{-1}}{1-z^{-1}},\ sampling\ time\ 2.5 * 10^{-5}s$$

As this is destined to be implemented on a DSP, the following plot shows the analog behavior of the digital loop when connected to an analog-to-digital converter that samples at 40 kHz and includes a one sampling period delay.

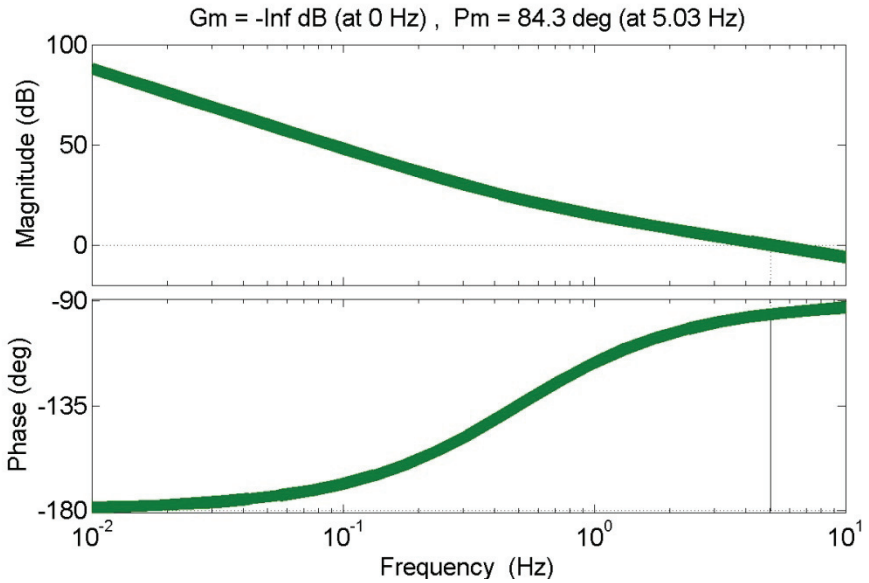

Figure 4.3: Gain and Phase Margin of Digital PLL at 40 kHz Sampling and 1 Sampling Period Calculation Delay

The linearization performed in Appendix B breaks down at large errors. Therefore, it is imperative that the output of the PI controller be set to the expected line frequency before the controller is turned on. If this precondition isn't met, or if the line frequency is too different from the expected frequency, the PLL can be expected to fail.

As alluded to previously in this section, there can be benefits for aligning the PLL d-q at an angle to the d-q of the bus voltage. In the "Power Stage Design" section, it was shown that with the power stage design being used for this waveform generator, the maximum current at 1000Hz that can be injected in the d (active power) channel of the bus voltage is 3.8A RMS per phase as a result of the difference between the DC bus voltage and the maximum phase voltage. This phenomenon is represented graphically below.

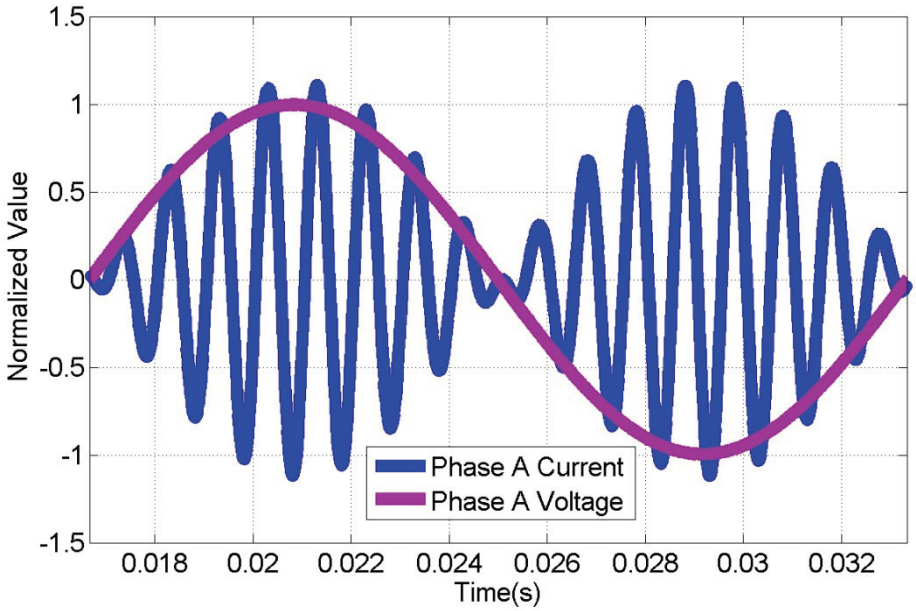

Figure 4.4: Normalized 60Hz Phase A Voltage and Current as a Result of a d Channel Sinusoidal Command at 1000Hz

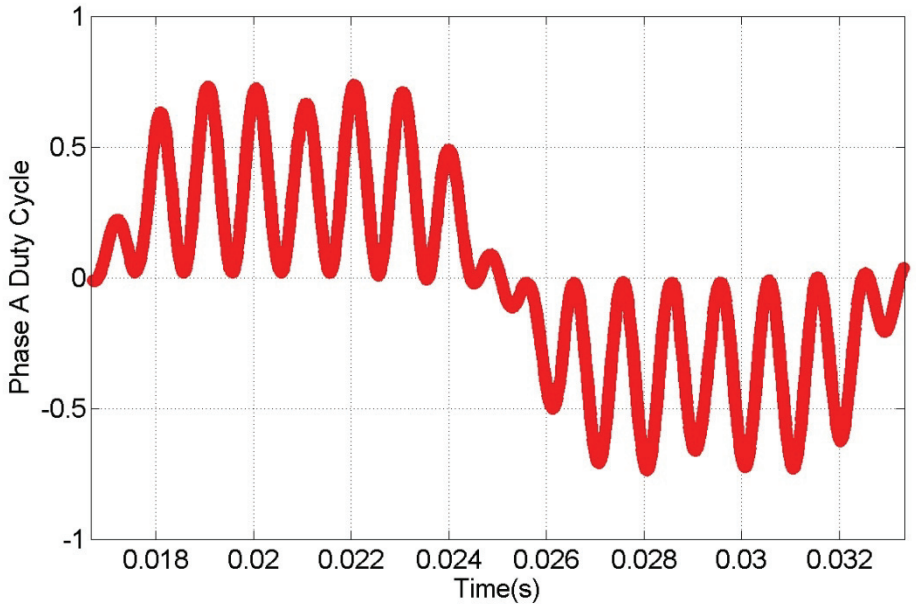

Figure 4.5: Duty Cycle of Phase A, Bi-Directional and Zero Centered, that Caused the Current Profile in 4.4

When a current perturbation signal is commanded in the d-channel, the 60Hz portion of that signal in abc resulting from the inverse Park transformation is aligned with the phase voltages, and the difference between the DC link voltage and the phase voltage is

least. This is apparent in figure 5.5; when the current must be greatest (and therefore the duty cycle must be greatest), the duty cycle is already at the point where it is greatest during the rotational frequency period. In other words, when the most available voltage is needed, the least is present.

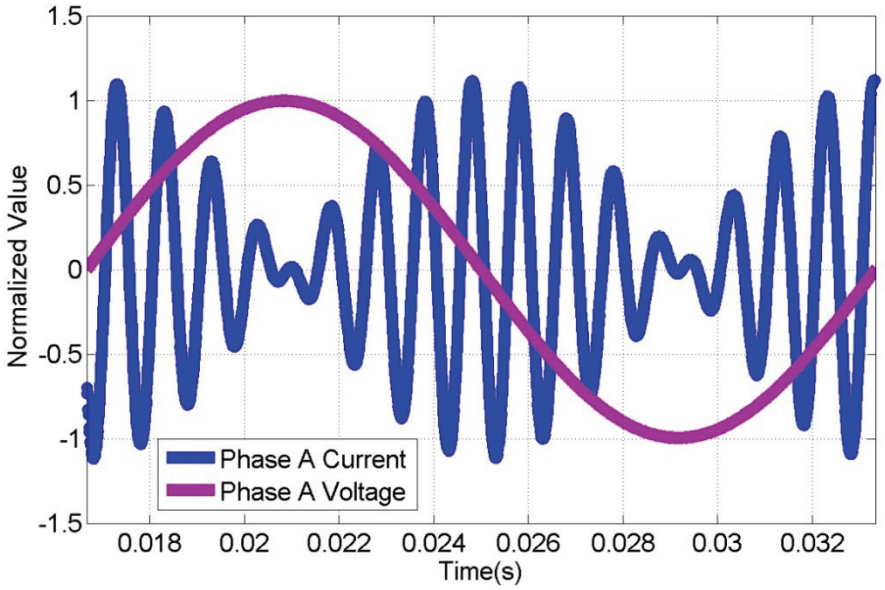

Figure 4.6: Normalized 60Hz Phase A Voltage and Current as a Result of a q Channel Sinusoidal Command at 1000Hz

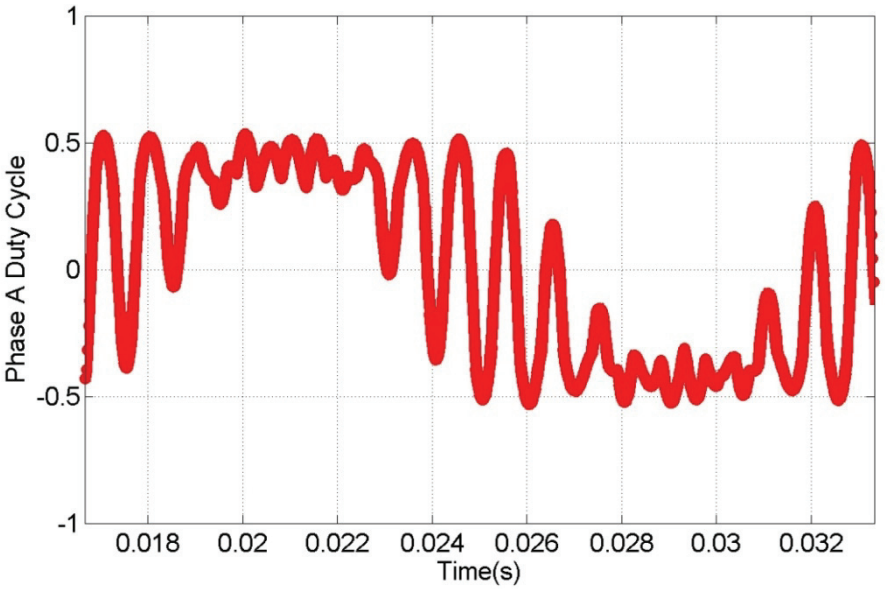

Figure 4.7: Duty Cycle of Phase A, Bi-Directional and Zero Centered, that Caused the Current Profile in 4.6

In the q or reactive channel, the opposite is true. The most current is required as the phase voltage swings to zero, providing the most available voltage.

This effect cannot be cheated; only an amount of power dictated by the phase leg inductance and minimum available voltage may be injected into the active power channel. However, a favor may be done for the measurement team in the form of a greater overall perturbation power, even if all of it isn't in the active channel.

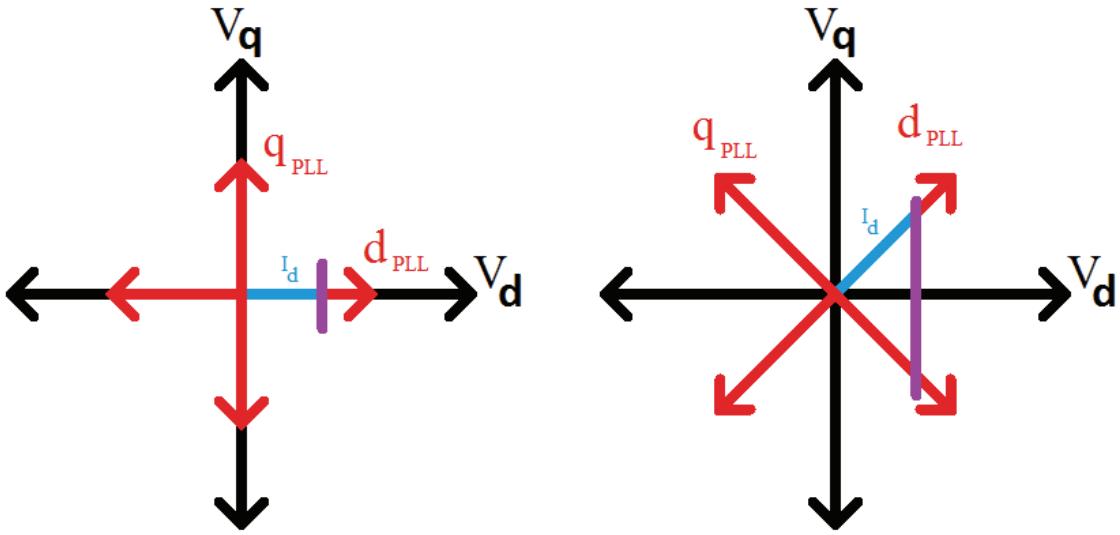

Figure 4.8: Comparison of V_q=0 Alignment and 45° Alignment Schemes

If the PLL is set to a different alignment than q=0 with respect to the bus voltage, even though the overall injection power in the active channel of the bus isn't increased, the overall power of injection can be increased. This is helpful for the measurement team because a greater perturbation results in more level changes when the voltage and current signals are converted from analog to digital signals, and therefore quantization effects are diminished. If the alignment is set to 45°, then both the d and q channels are capable of injecting the maximum q=0 alignment d current multiplied by the square root of two. If the alignment is further skewed, even greater perturbation currents could be realized. If the measurement computer is aligned to the bus voltage and the PM1000 is aligned to whatever angle produces the maximum d and q current, the measurement computer should be able to calculate both of the d and q channel impedances from a single, strong perturbation. However, this isn't feasible for this impedance measuring device. In the section "The Role of Perturbation Signals in System Identification", it is shown that the

PM1000 control-to-current and control-to-voltage signals are used in the determination of the impedances. Therefore, the PM1000 must inform the measurement computer what these perturbation signals are. If they are sent in d-q form, then the PM1000 PLL and the measurement computer PLL must be aligned identically. If the perturbation signals are sent in abc, then the measurement computer could determine the d-q perturbations based on its own alignment, but this work is left to be done in the future. For now, both PLLs are aligned 45° from bus voltage; this works because Dr. Belkhayat's generalized Nyquist method works regardless of alignment, as it captures all of the active and reactive power information. However, Dr. Burgos's method will obviously no longer work, because the d channel is no longer the only channel that contains active power information.

The effect of this type of alignment is shown below.

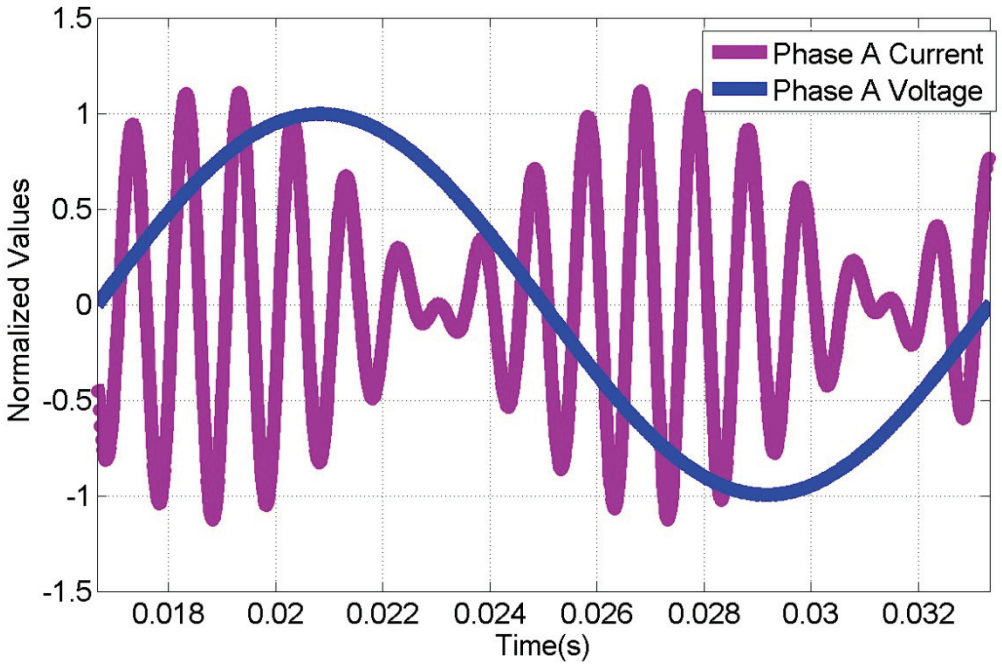

Figure 4.9: Normalized 60Hz Phase A Voltage and Current as a Result of a 45° Aligned d- or q- Channel Sinusoidal Command at 1000Hz

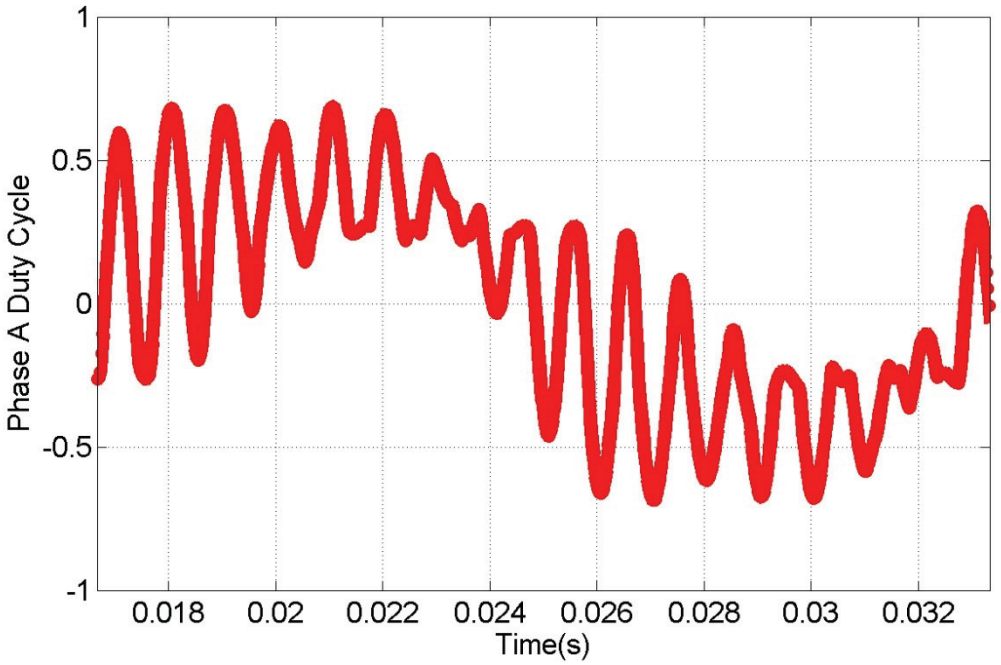

Figure 4.10: Duty Cycle of Phase A, Bi-Directional and Zero Centered, that Caused the Current Profile in 4.9

As expected, the 45° alignment shifts the portion of the current with highest magnitude to 45° from the maximum phase voltage. Although it is not readily apparent from the duty cycle graphs, this does allow for a 41% increase in injection power, or in this case, 5.38A RMS, or 4293kW total injection.

Another benefit that this 45 degree alignment provides is that now both the d and the q channel are 45 degrees from being aligned with the load voltage. This gives both channels the capability to make use of active power; at 0 degrees of alignment, the d channel contains only active power and the q channel contains only reactive power. Now, both channels measure both. This will be important when the DC link voltage controller is implemented; either d or q can be used to charge the capacitor, because a command in either can result in active power.

4.c Control Logistics

In order to understand this section, two points of design that hasn't been discussed thus far must be explained. As previously discussed, there are two parts to the impedance measuring device; the first is this machine, the arbitrary waveform generator, and the second is the measuring equipment. As also previously discussed, the manner in which this measurement device works to calculate impedance involves knowing the perturbation signal as the PM1000 sees it (see equation 3.2). The measuring equipment in this impedance measuring device has its own computer. In addition to knowing the perturbation signal, the measurement computer must know as close to exactly as possible when the perturbation signal starts. The best way to do this is through a fiber-optic link that allows the PM1000 to directly send a synchronization signal to the measurement computer. This is the only direct link between these two computers; all other communication is done through a third host computer with a user interface.

The second point of design that must be discussed involves the actuation of the relays to select the various topologies needed for various functions. The PM1000 doesn't have enough accessible outputs to toggle all of these relays, so the host computer must perform the task. The overall schematic including actuators is presented in the "Fault Protection and Power Routing Design" section, but studying it is unnecessary to understand the operations described here.

There are 4 main operations that the waveform generator must perform. It must inject in shunt, inject in series, charge the DC link capacitor, and stand by. These operations are mutually exclusive; no two tasks may be performed at the same time. Therefore, one architectural method of separating tasks is to create a simple discrete state machine. The PLL operates outside of the state architecture; PLL functions occur regardless of state. Each of the 4 main operations above represent a state, and the flow chart of operations to be performed during each sampling period (and main interrupt service routine) is shown below.

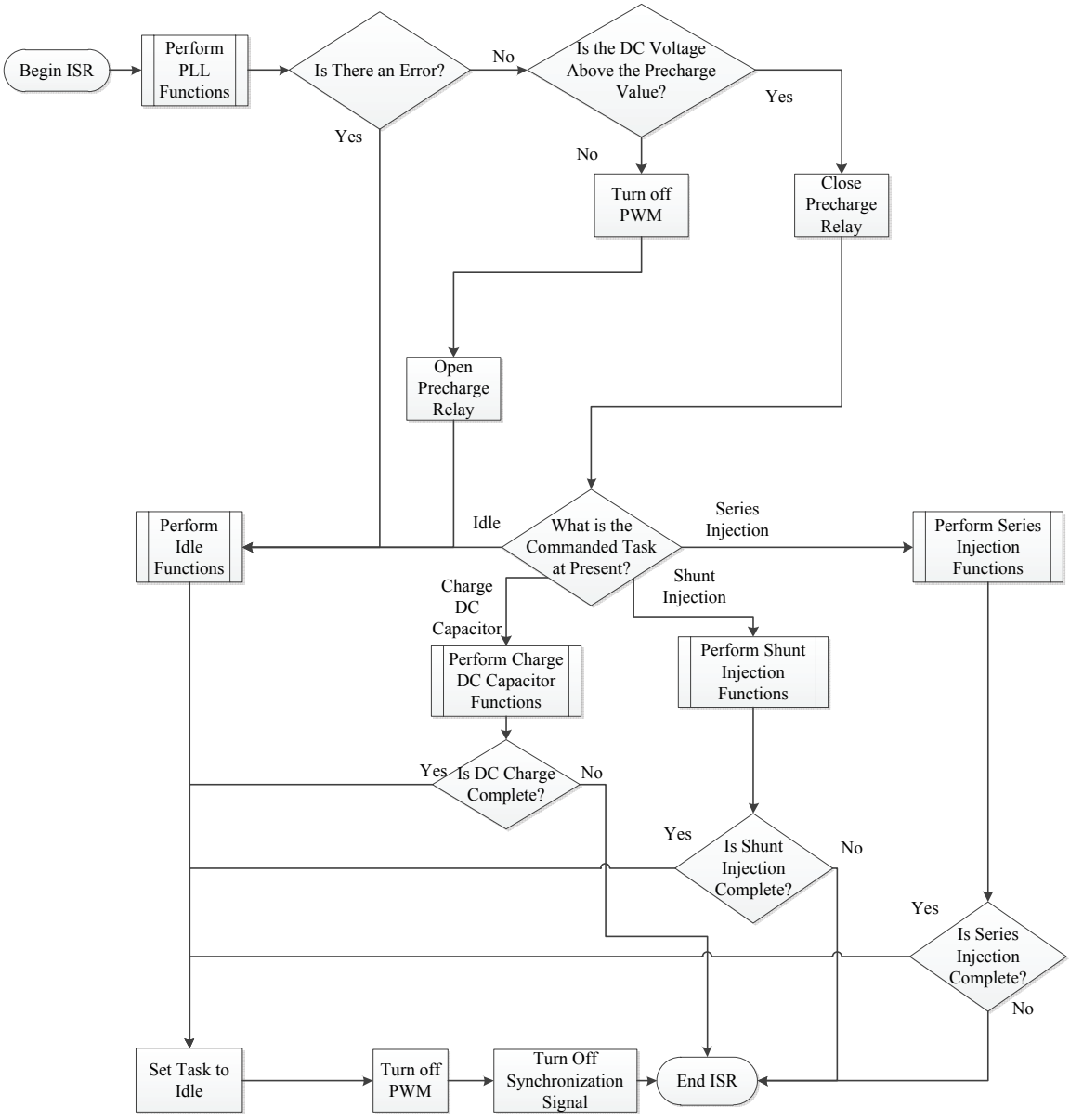

Figure 4.11: Main Interrupt Service Routine Flowchart

There are 5 subroutines in this flowchart- “Perform PLL Functions”, “Perform Idle Functions”, “Perform Charge DC Capacitor Functions”, and “Perform Shunt Injection Functions”, and “Perform Series Injection Functions”. The flow charts of these subroutines are presented below.

The state command and associated parameters are passed into global variables by a separate communications interrupt that receives information from the user interface on

the host computer regarding type of perturbation requested, associated power level, and associated perturbation duration.

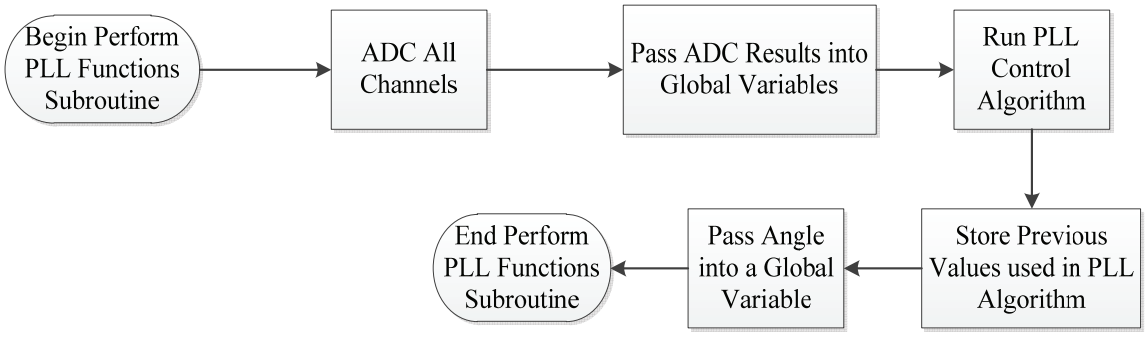

Figure 4.12: Perform PLL Functions Subroutine

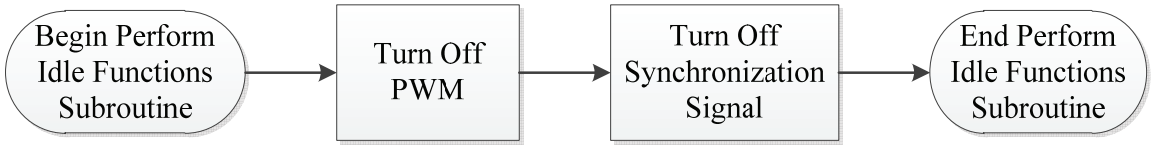

Figure 4.13: Perform Idle Functions Subroutine

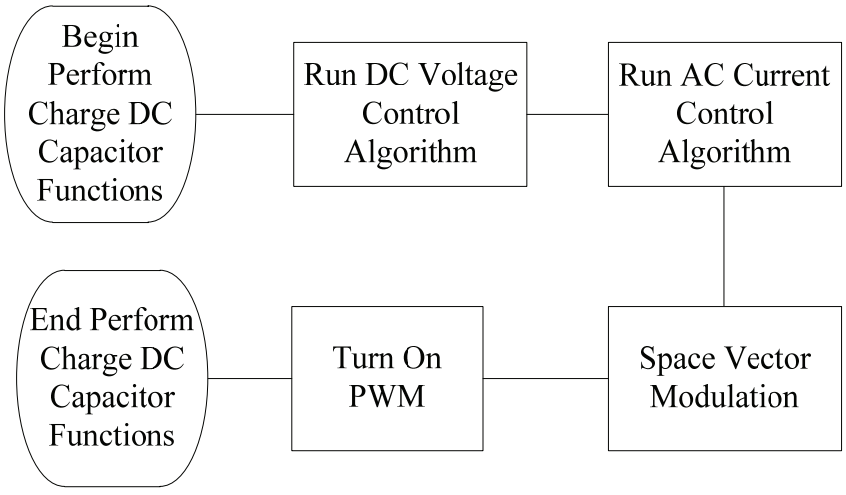

Figure 4.14: Perform Charge DC Capacitor Functions Subroutine

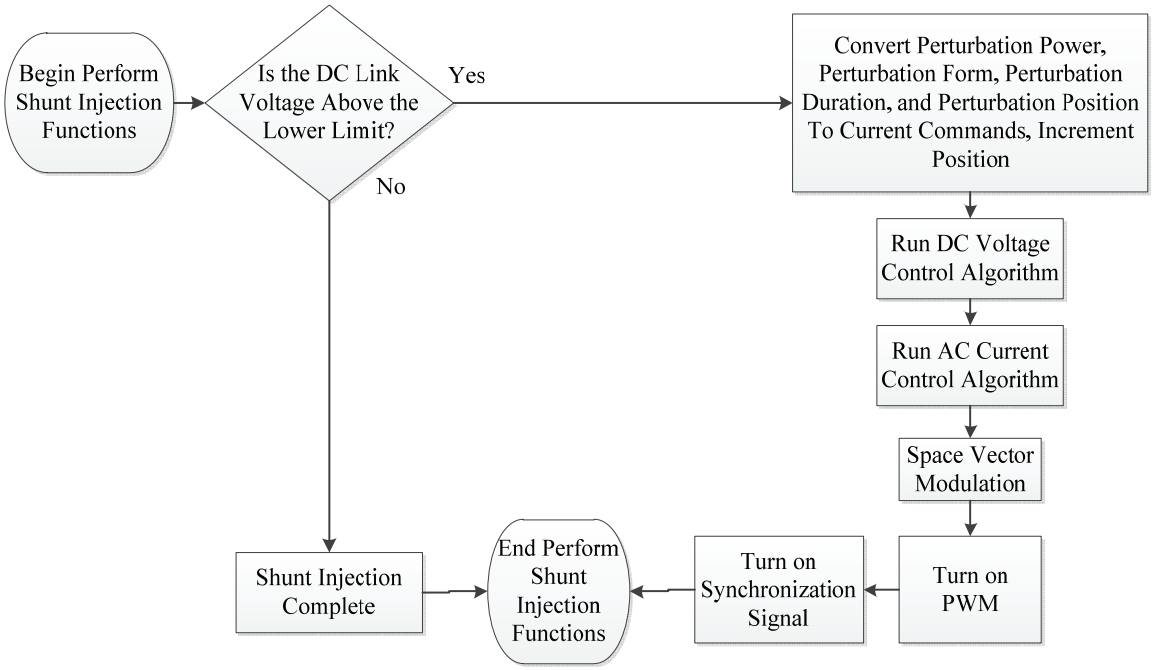

Figure 4.15: Perform Shunt Injection Functions Subroutine

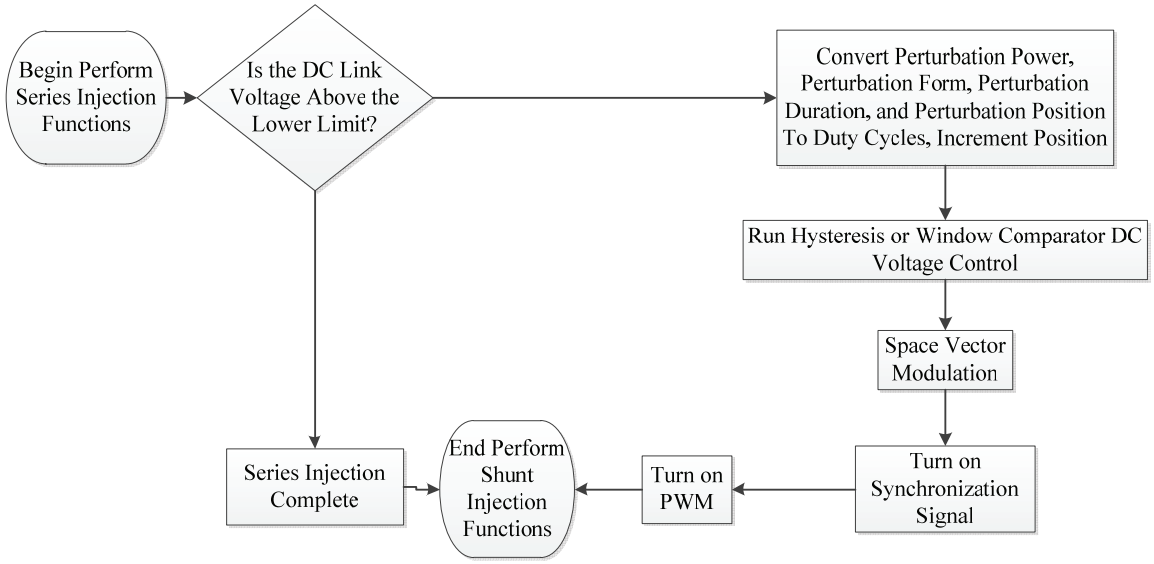

Figure 4.16: Perform Series Injection Functions Subroutine

The host computer passes to and can receive from the PM1000 a set of variables including “commanded task”, “perturbation power”, “perturbation form”, “perturbation duration”, and “error”. The host computer only receives the “last task”, “precharge complete”, and “last task complete” variables.

There are two events outside of errors that can interrupt injection. First, the perturbation position becomes equal to the perturbation duration. Second, the DC link voltage falls below a pre-set minimum value. The minimum values of the DC link voltage are discussed in the "DC Link Capacitor Specification" section. The effect of both of these is the same: the "last task complete" variable is set to 1, and the current task is set to "idle". The host computer will attempt to generate impedances. If the user is unhappy with the results, a new perturbation and measurement cycle can begin.

4.d Shunt Injection Closed Loop Current Control

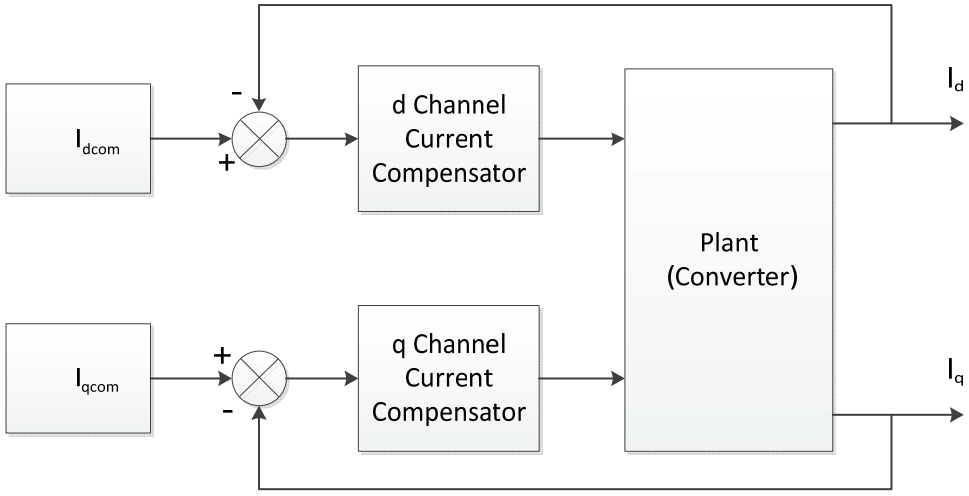

Figure 4.17: Shunt Current Control Implementation

Figure 4.17 shows the implementation of shunt current control in the PM1000. The hardest part of closed loop control in three phase converters is the derivation of the open loop transfer function of the plant. This task is performed in Appendix C. Once this is complete, the manner of control design explained in the PLL section can be used to design a compensator. Here, this was done in the analog domain, and transferred into the digital domain by MATLAB. A bandwidth of greater than 1 kHz is desirable so that the controller can follow the highest frequency sine wave to be used for perturbation. The EMI filter and output inductor will be outside of the control loop and will therefore have

some uncontrolled attenuation, however. This is one of the reasons for the ratio of main inductance to output inductance.

The shunt injection compensator transfer functions are shown below.

[4.8] $$C_i(s) = \frac{.033702(s+620.8)}{s}$$

[4.9] $$C_i(z) = \frac{.033964(z-.9846)}{z-1}$$

The compensator was designed to have a phase margin of 60 degrees at 1100Hz. However, when the uncontrolled portion of the power stage is taken into account, there will be a slightly lower bandwidth and phase margin. The exact transfer function can be found by simulation, and will be shown in the simulation portion of this report.

4.e Charge and Shunt DC Link Voltage Control

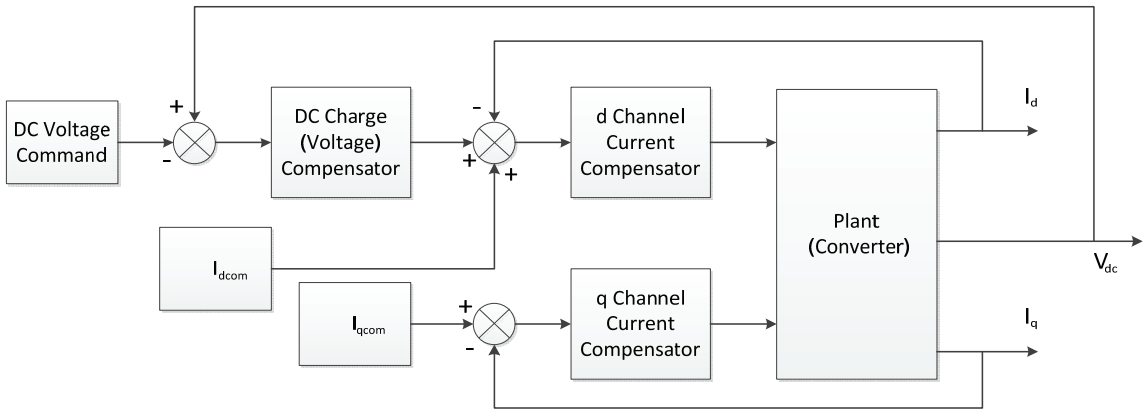

Figure 4.18: Shunt DC Link Voltage Control Implementation

As a result of the lack of available voltage between the maximum AC voltage and the DC link voltage at maximum frequency, there's almost no margin of safety between operating voltage and the PM1000's "Do not cross" voltage of 900V. Therefore, the DC link voltage controller must have near zero overshoot. In addition, a low bandwidth is desired during perturbation in order to maintain DC voltage without corrupting the perturbation signal with the action of the DC voltage compensator.

The DC link voltage controller will make use of the current controller shown in section 4.d. The open loop transfer function from the d channel current command to the DC voltage is again derived in Appendix C. The compensator transfer functions are:

[4.10] $$C_v(s) = \frac{3.06(s+5.386*10^4)}{s}$$

[4.11] $$C_v(z) = \frac{5.12(z-.1953)}{z-1}$$

4.f Shunt Simulation

For this thesis, simulation was used only for control design and verification. A detailed model is not necessary for this, but a simplified model can help greatly. Here, MATLAB and Simulink were used with the PLECS power electronics add-on.

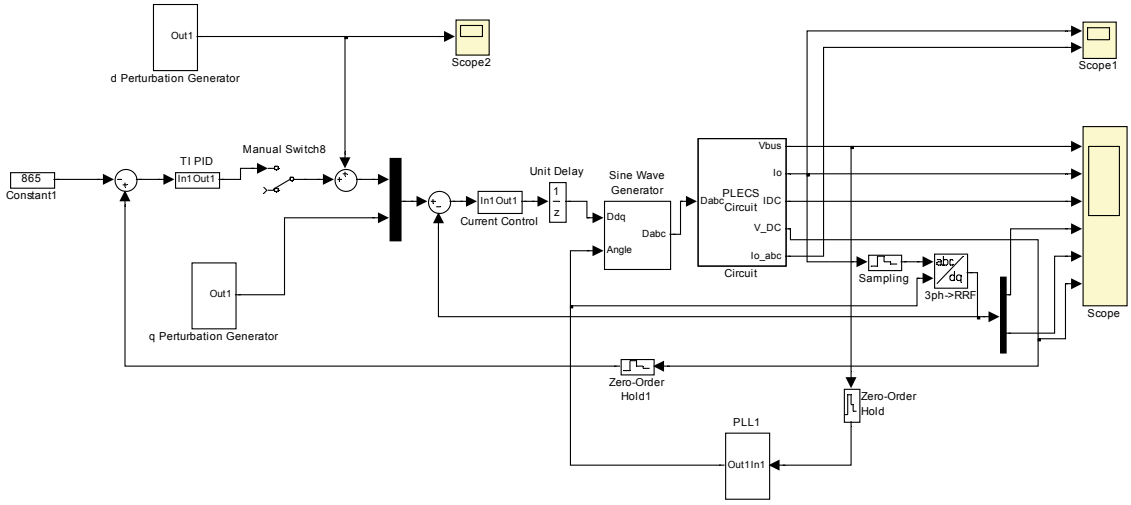

Figure 4.19 Shunt Injection SIMULINK Model

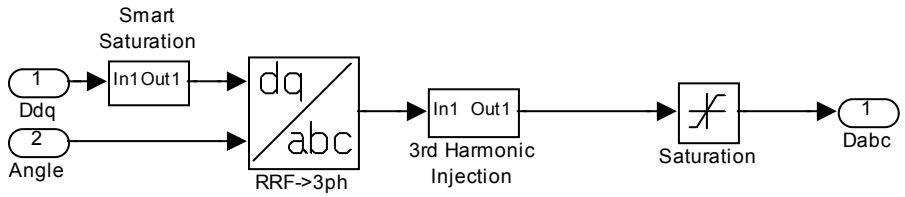

Figure 4.20: Averaged Model Shunt Injection Sine Wave Generator Block

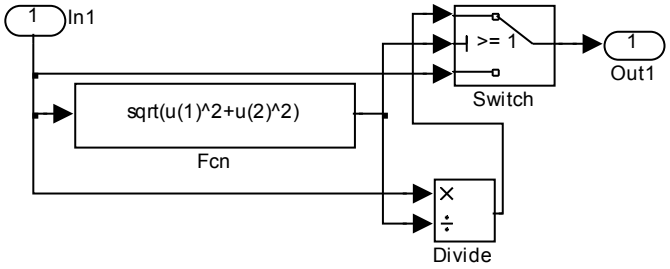

Figure 4.21: Smart Saturation

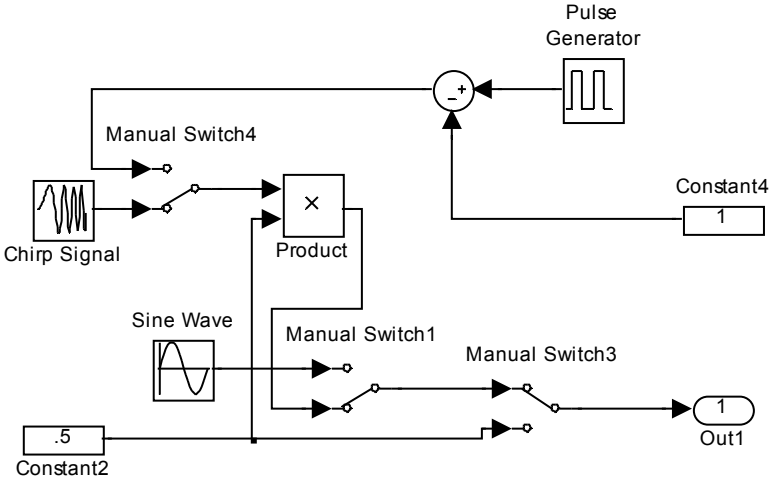

Figure 4.22: Perturbation Signal Generator

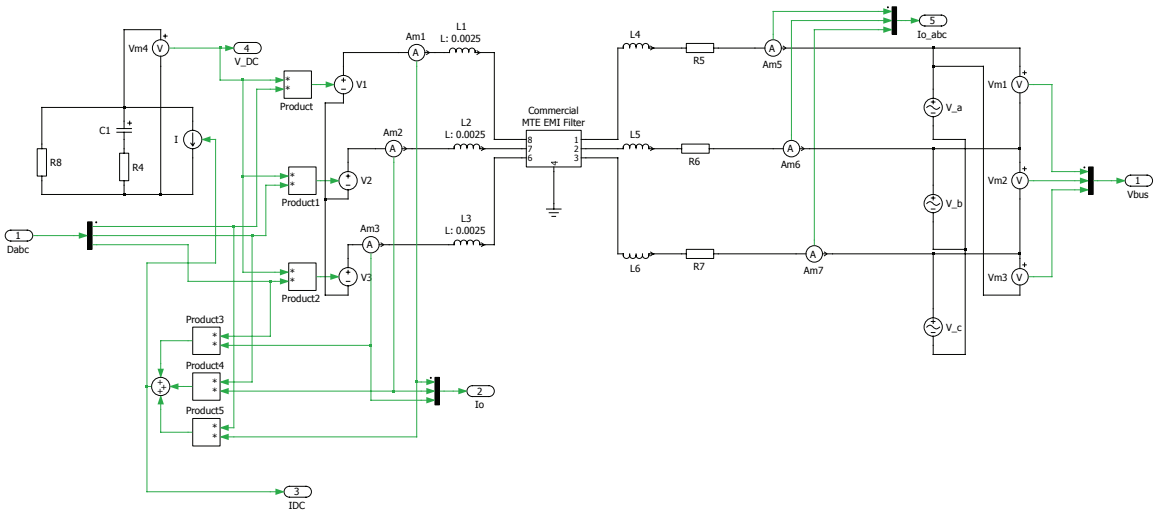

Figure 4.23: Averaged Shunt Injection Model PLECS Circuit

The linearization of these models with MATLAB's linearization tool produces the following transfer functions for current and voltage control.

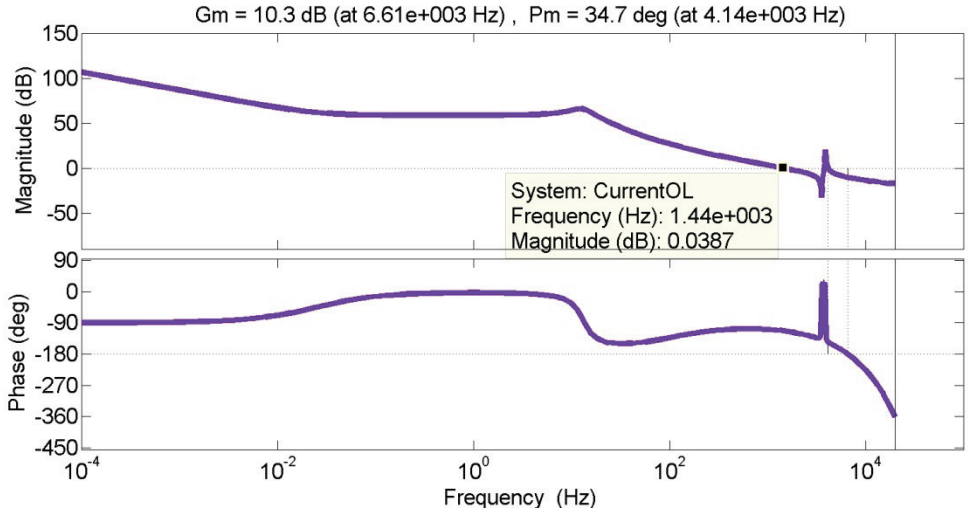

Figure 4.24: Open Loop Compensated Control-to-Current Transfer Function

The controller implemented in figure 4.20 was actually determined through several iterations. The phase margin of 34.7 degrees is obviously less than ideal, but if a bandwidth of 1 kHz is desired, this is the best that can be done. If the bandwidth is lowered, the shape of the bode plot near the crossover frequency doesn't allow for much phase margin improvement unless a drastically lower crossover frequency is chosen. In addition, this configuration is relatively safe; the resonances near 4 kHz can be incorrectly modeled by as much as a 50% frequency discrepancy without creating an unstable loop.

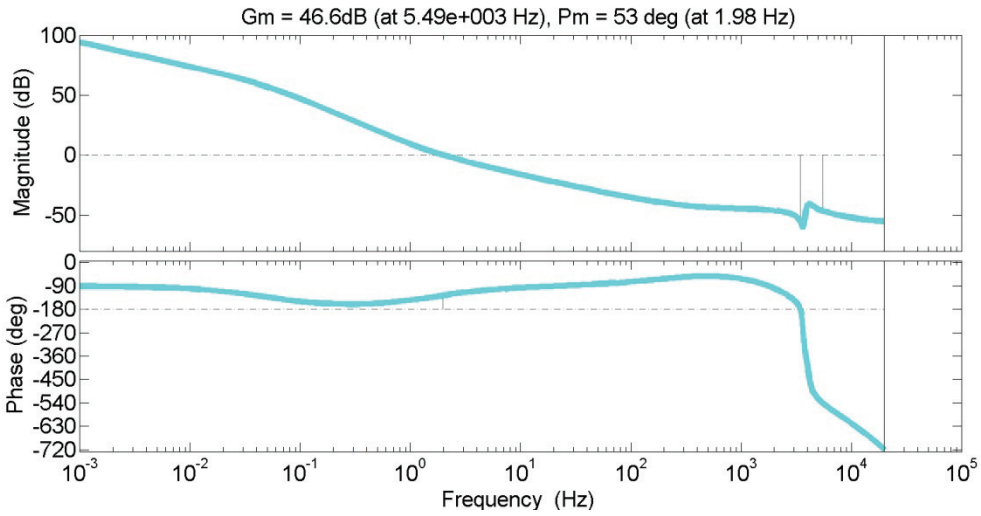

Figure 4.25: Open Loop Compensated Control-to-DC Voltage Transfer Function

While a 60 degree phase margin is generally desirable, this compensator was chosen for a very simple and overriding reason- it works best in hardware.

4.g Series Open Loop Injection and DC Voltage Control

The small signal behavior of control-to-voltage for the shunt injection scheme is very hard to determine; being that there are voltages on the bus that are determined by unknown dynamics (the measuring of which is the purpose of this entire project), closed loop voltage control becomes very difficult. However, the VSI has linear duty-cycle-to-output voltage behavior.

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \frac{V_{dc}}{2} \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix}$$

If the VSI is operated open-loop, a reasonably well controlled voltage can be obtained. The two factors fighting against this are the frequency-related attenuation of signals by the power stage and the variability of the DC link voltage. This is the main reason that a method of stopping and re-starting a perturbation after a DC link recharge session is necessary. In shunt injection, the maximum energy drain can be estimated with some accuracy. This is not the case for open-loop series injection operation. A duty cycle will output a known time-averaged voltage to the main inductor, but depending on the

impedances on the bus, the current drain will vary to maintain that voltage. This variation of DC voltage will also change the transfer function of control-to-output in the VSI, which may change the results of impedance measurement. There are two ways to combat this. First, a narrow DC voltage range can be specified. Second, the perturbation signal command communicated from the PM1000 to the host computer can be normalized real-time with the known DC voltage. In this implementation, both methods are employed.

Without a linear current controller, design of a DC Voltage linear controller becomes nearly impossible. Therefore, for this implementation, hysteresis control was chosen to maintain the DC voltage during series injection. Hysteresis control (sometimes called "bang-bang" or "cop-out" control) involves setting an upper and lower limit to the controlled signal, and using a fixed force to drive the controlled signal to a value somewhere between the upper and lower limit. Further explanation of this scheme is done most easily with the graphics in the "Series Simulation" portion of this thesis.

4.h Series Simulation

A switching simulation was chosen for the simulation of series injection because it was found to more accurately model the action of the anti-parallel diodes in the converter.

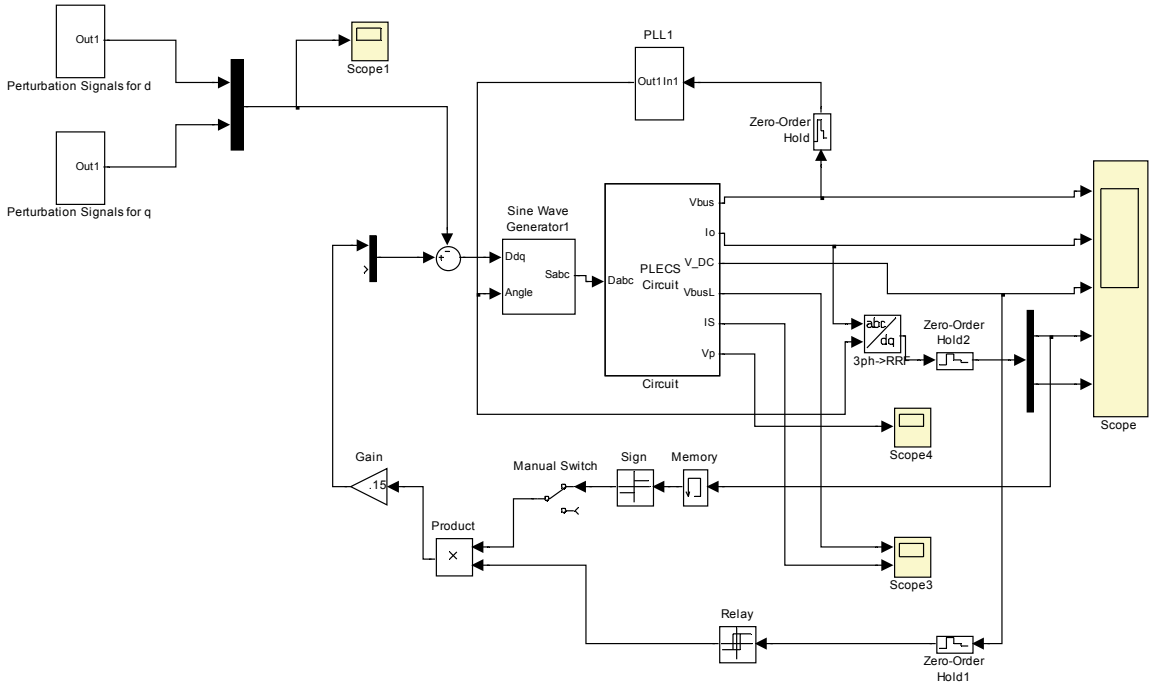

Figure 4.26: Series Injection SIMULINK Model

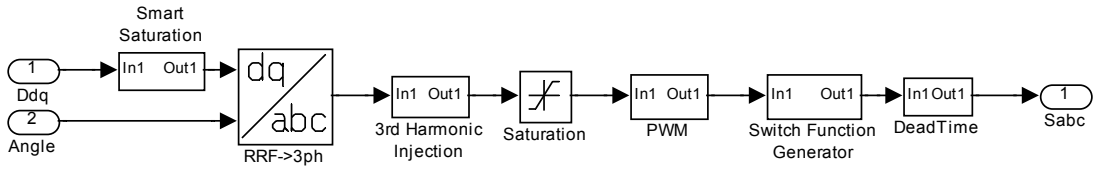

Figure 4.27: Switching Sine Wave Generator Block

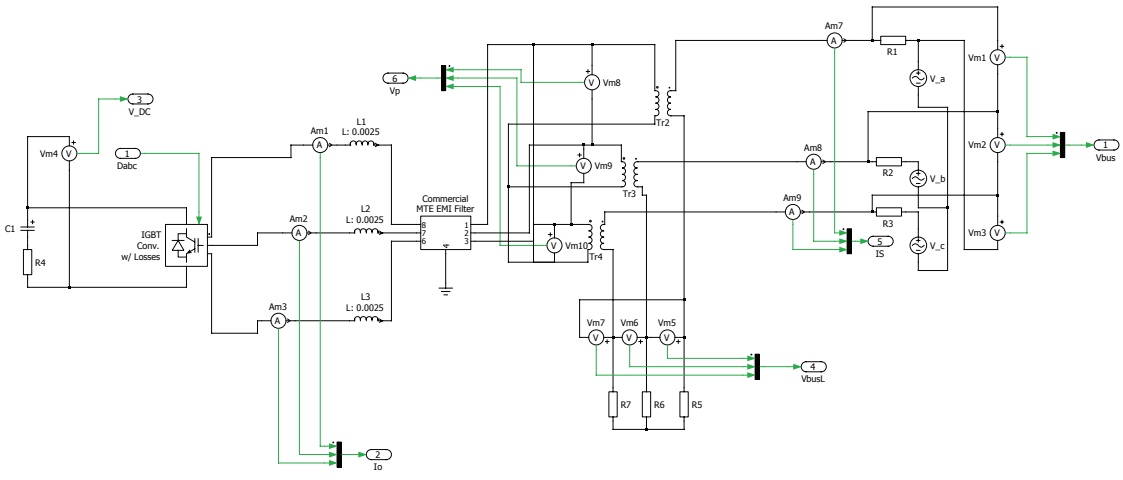

Figure 4.28: Series Injection PLECS Model

The lower portion of Figure 4.24 shows the implementation of hysteresis control. The "Relay" block outputs 1 when the DC voltage falls below a specified value, and -1 when the DC voltage goes above a different specified value. If the DC voltage is between the two values, the "Relay" block continues to output whatever it was last outputting. There's a slight variation of hysteresis control known as "Window Comparator" control. The only difference between traditional hysteresis control and "Window Comparator" control is what the "Relay" block outputs when the DC voltage is between the upper and lower limit; hysteresis control behaves as previously described, whereas in "Window Comparator" control, the "Relay" block outputs zero between the two limits. Both types of control are implemented in hardware, and either can be chosen by the host computer.

The twist involved here is that the direction of force required to move the DC voltage low or high is not necessarily always the same. As can be seen in figure 4.26, if the active-power oriented component of the bus current is flowing into the tops of the transformer secondary windings, the direction of active-power oriented voltage on the primary windings will be different than if the active-power oriented component of the bus current is flowing out of the tops of the secondary windings. Therefore, to pull power from the bus and use it to charge the DC link capacitor, the direction of the active-power oriented current on the secondary side must be known. This sounds complicated, but has a very simple solution. Using the d-q transform that is exploited pervasively throughout this thesis, the direction of the active-power oriented current on the primary windings, and therefore on the secondary windings, can be known. In hardware, there are current sensors in series with the transformer primary windings, so this is easily done. Figure 4.24 shows the simulation implementation of this. It is of note that for this particular bus, the load is resistive, so active power can only flow from the voltage sources to the load. However, this impedance analyzer will be used on a bus of unknown orientation and construction, so power in the opposite direction is entirely possible.

Once the structure is determined, 3 values must be found by trial and error. These three values are the upper hysteresis window limit, the lower hysteresis window limit, and the magnitude of the constant force. Through simulation, the most effective values for these variables were found to be 870V, 860V, and .05, respectively.

5. Fault Protection and Power Routing Design

After the power stage has been designed, steps can be taken to ensure that it doesn't tear itself to pieces. The types of faults that can damage the equipment fall into two categories: overvoltage faults and overcurrent faults. Overcurrent faults usually take longer than overvoltage faults to damage equipment, as the damage associated with overcurrent faults is usually thermal. Overvoltage faults, however, cause damage associated with dielectric breakdown. Most components have overcurrent ratings that allow for a measure of overcurrent for a short period of time, but have a hard "do not pass" voltage limit; overvoltage damage is often considered to be instantaneous. The voltages and currents for all parts of the system are already known, but are reiterated here for the sake of convenience:

Location	V_{max} to Ground (DC or Peak)	V_{max}, line-to-line (Peak)	I_{max} (DC or RMS)
DC Link	900	n/a	13.26
AC side Before Main Inductor	900	900	12.5
AC side After Main Inductor (Primary only in Series)	376	651	12.5
Series Secondary (Bus Power)	376	20	132.6

Table 5.1: Maximum Voltages and Currents at Various Points in the Waveform Generator

It is of note that with the exception of the EMI filter, the entire power stage is isolated from ground. However, for protection purposes, an upper limit to the voltage between any of these parts and ground must be estimated. In all cases, there will be stray capacitances between each point in the system and ground. The ratio of stray capacitances of two points to ground determines where the potential between each point and ground lies with respect to the potential between the two points. In all cases, the voltage from one point to ground will fall somewhere between 0 and the absolute value of the maximum voltage between that point and any other point. For example, the

maximum voltage between the positive terminal of the DC link and any other point is between the positive terminal of the DC link and the negative terminal of the DC link. The maximum value of the voltage between the positive terminal and ground is then the voltage between the two DC link terminals. Although the ratio of stray capacitances is rarely so one-sided, it's safest to assume that the maximum voltage to ground is possible. Therefore, the maximum voltage to ground of all components in the DC link is the maximum voltage across the DC link terminals.

First, the easy part will be explained- the wiring. Proper wiring is necessary to prevent short circuit faults through the wiring insulation and can set the level of overcurrent faults if not sized in compliance with the current rating of the other components. Wiring is rated in RMS, both for voltage and for amperage, so the peak value of the acceptable voltage is the rating multiplied by the square root of 2.

For all locations except the DC link and AC side before the main inductor, standard 600V wire works well. On the DC link, 1000V wire is necessary. On the AC side before the main inductor, 600V wire is used for easy phase identification, but precautions are taken as if the wire was bare; the three phase wires are individually suspended by isolated, rigid components and run a maximum of 4 inches each.

According to [14], 90°C 12AWG wire can handle up to 23A in confined spaces (as opposed to in free air), and 90°C 00AWG wire can handle up to 175A under the same conditions. 12AWG works for all cases except the secondary side of the transformer, which will operate well with 00AWG. This design decision is very conservative; these are continuous duty values, and the waveform generator will only operate very intermittently. Also, much of the wiring in the waveform generator can be considered to be operating in free air conditions, especially the 00AWG wire. The free air rating of the wires is significantly more by this reference. For example, the free air rating of 00AWG is 283A.

The best way to explain the protection and routing schemes is to first show the whole schematic, then to explain each part of it. The schematic was produced in the Educational Version of Autodesk Electrical because translation mechanisms are in place between Autodesk Inventor and Autodesk Electrical that makes wiring harness design for manufacture very easy.

It should be mentioned that that the communications computer controls all relays that switch the power stage between different modes of operation. The PM1000 control board doesn't have enough output ports to operate these. However, for time-critical operations, the PM1000's fiber optic ports are used to directly control separate protection relays through analog hardware based signal paths. All relays and controls triggered by the host computer are done so through opto-isolators on a set of custom output control boards. All relays and controls also have an extra set of contactors with which the host computer can sense whether or not the commanded task was actually performed. This sensing is also done through opto-isolators on a set of custom input boards.

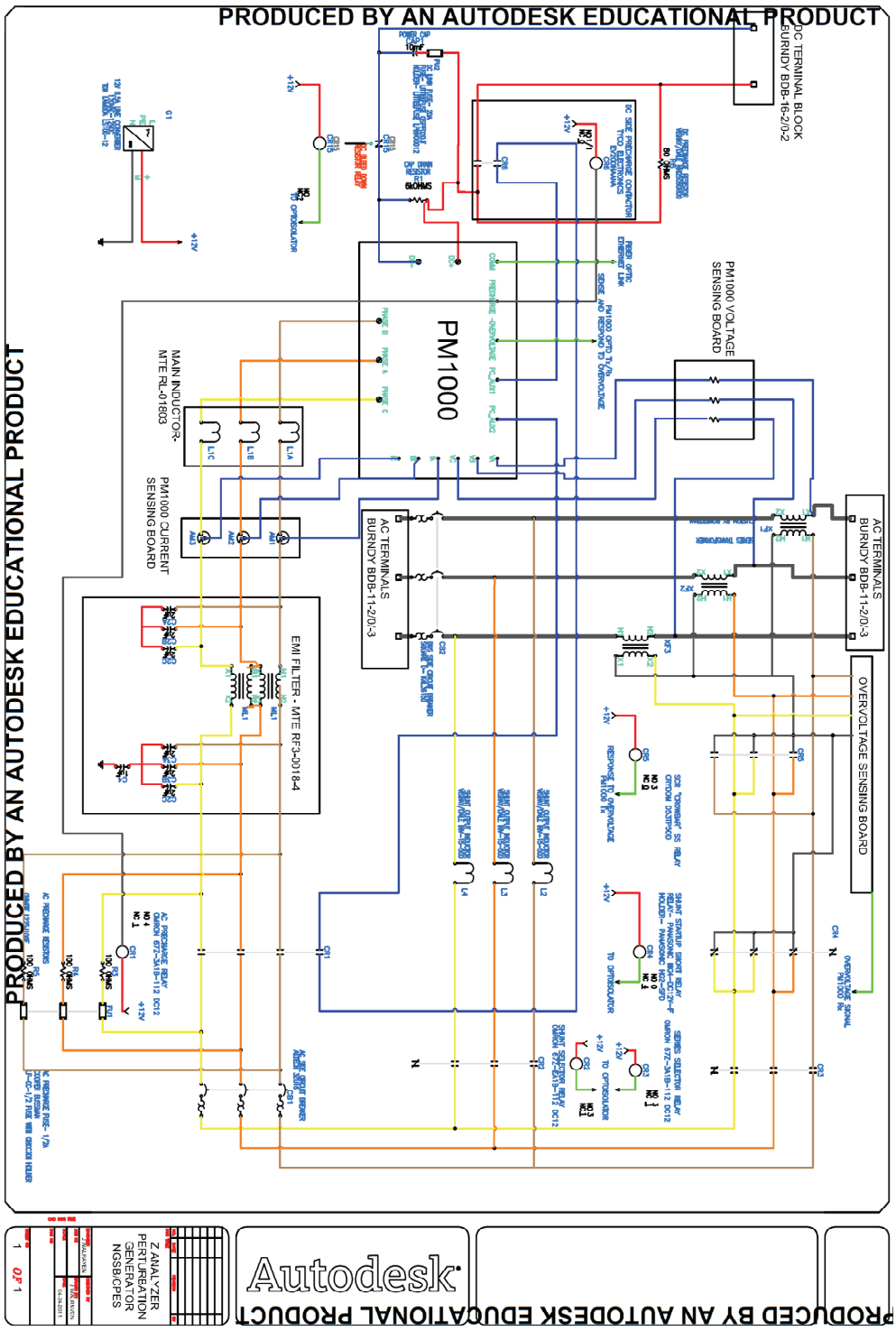

Figure 5.1: Overall Power Stage and Protection Schematic

This is large enough that it is difficult to read on one size A page. This diagram is only presented to provide reference for the location of each of the detail diagrams shown below.

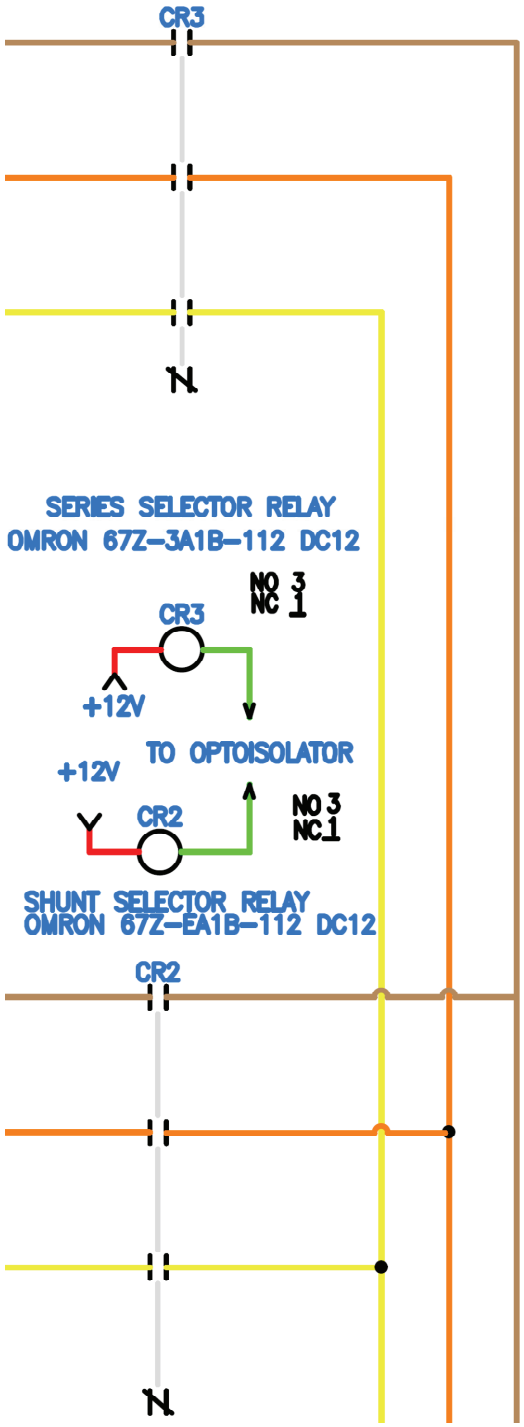

Figure 5.2: Detail of Series/Shunt Selection Relays

The main inductor, current sensors, and EMI filter are shared by the shunt and series injection power stages. In order to choose between them, two three-phase relays with auxilliary contactors are used. These relays are controlled by the host computer, and the auxilliary contators fulfill the role of feedback sensors to tell the host computer that the relays are actually closed.

Overcurrent protection on the AC side of the PM1000 is provided through the CPLD on the control board. For closed-loop control, the PM1000 requires current sensors on the AC side, and these are placed within the shared portion of the power stage. In addition to being used for control, these sensors send signals to comparators in the CPLD that stop PWM if overcurrent is sensed on the AC side of the PM1000, effectively breaking the loop for all components in the waveform generator. In addition, this error causes the primary side of the transformers to be shorted, again making the entire impedance analyzer invisible to the bus.

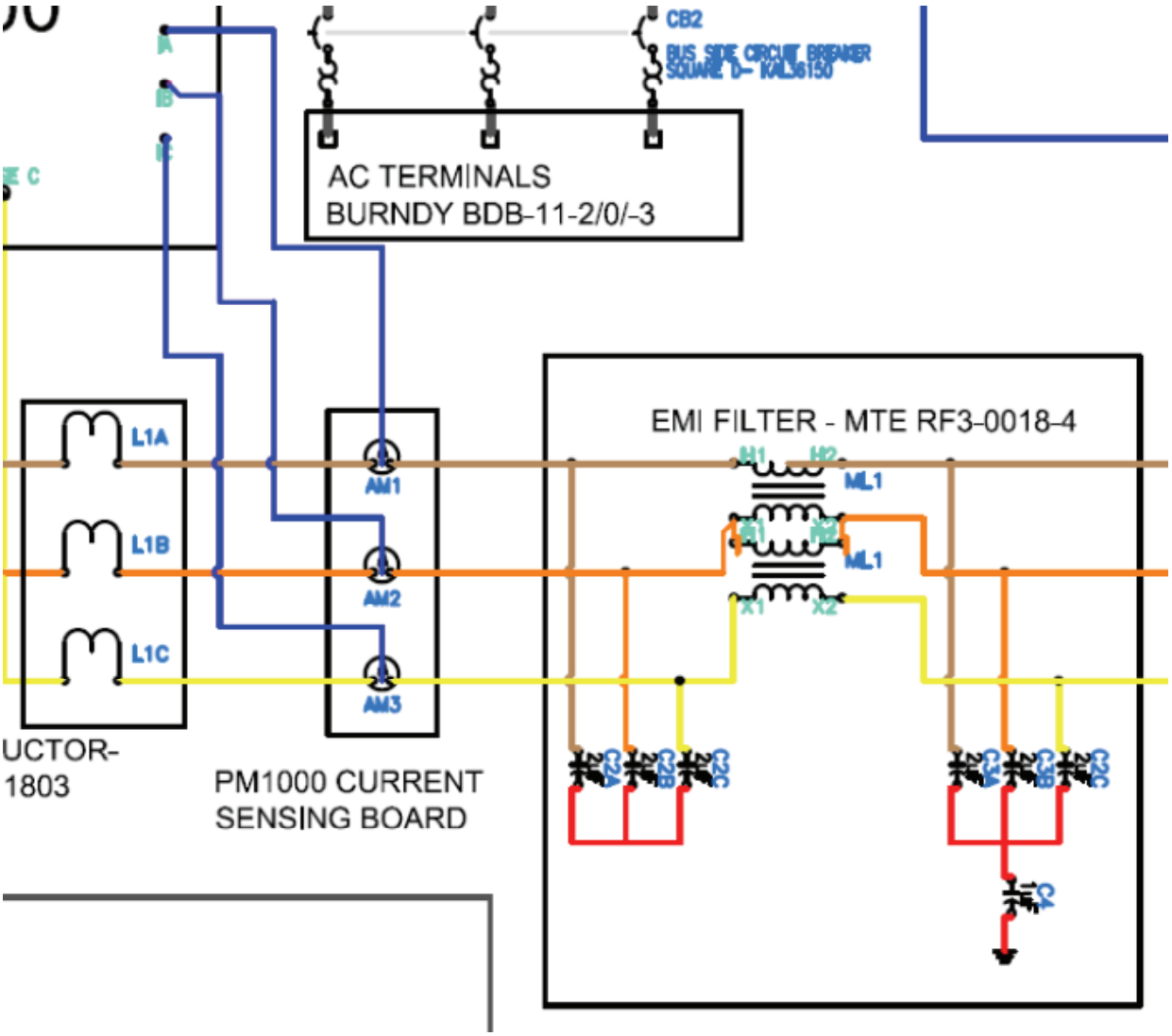

Figure 5.3: Detail of Shared Portion of Power Stage and PM1000 AC side Overcurrent Protection

The PM1000 is powered by the DC capacitor voltage, and in this case, this voltage is initially fed by the AC side bus voltage and the non-PWMing IGBT modules acting as a diode 6-pulse bridge. Normally, the AC bus voltage won't ramp up to its nominal value over a long period of time; a switch will be thrown, and nominal voltage will be applied to the lines. If the DC link capacitor has no charge in it, this will result in an inrush of current than can damage the DC link capacitor. In order to prevent this, a "Precharge" circuit must be implemented. Resistors are connected in series on the AC lines leading to the IGBTs, and current is limited until the voltage reaches a pre-set level. At this point,

the PM1000 will close a relay placed in parallel with the resistor, and normal operation can commence. However, if for whatever reason this relay opens during normal operation, currents producing power losses in the resistors far beyond their rating will flow through the resistors. This can cause resistor damage and dangerous temperatures in the impedance analyzer cabinet. Therefore, a fuse must be placed in series with the resistor.

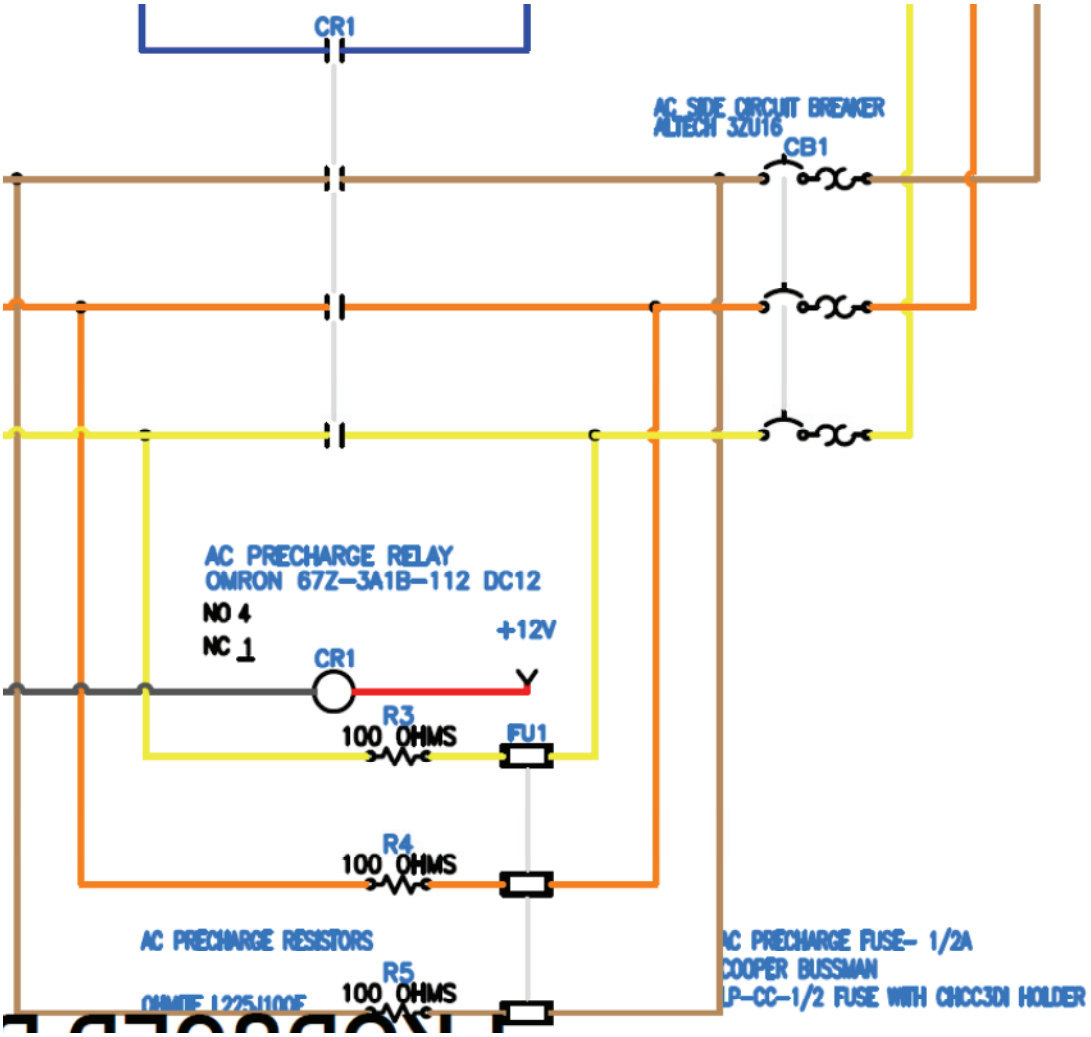

Figure 5.4: AC Precharge Circuit Detail

This circuit also shows the AC side circuit breaker. This breaker serves two purposes; one, it provides an extra measure of AC side overcurrent protection, and in a completely hardware implementation to boot. Two, it serves as a main switch for the AC side of the PM1000.

Given that the turns ratio of the primary to secondary side is 10:1, a short on the bus that causes a voltage drop of full bus voltage across the transformer secondary can cause a voltage of 10 times full bus voltage or 3760V across the primary side; in the time that it takes to break the secondary side with the circuit breaker, the entire waveform generator power stage may be damaged. Two measures are in place to ensure that this doesn't happen; first, the primary side is normally shorted with a normally closed relay. A short of the primary side (0V) ensures a zero voltage drop across the secondary side, effectively making the entire impedance analyzer invisible to the bus. This relay only opens during series injection, so all modes of operation except for series injection, a short on the bus would result in no effect except the eventual opening of the secondary side circuit breaker. The second protection against this event is much faster; voltage dividers sensing the primary side voltages are connected to analog comparators that send a signal through a fiber-optic transmitter and receiver pair to the PM1000 control board. The PM1000 control board sends this signal through the on-board CPLD directly to another set of fiber-optic communicators to a board that closes an SCR-based solid state relay. Both of these boards were custom made and populated, and ensure reaction to an overvoltage at the primary side of the transformers in less than 1µs.

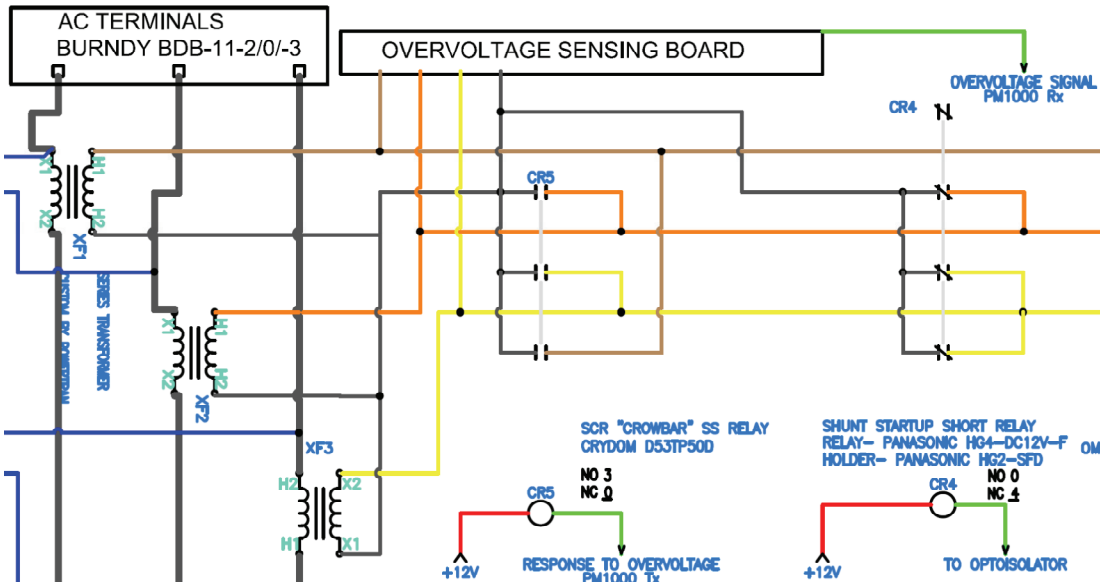

Figure 5.5: Transformer Primary Side Overvoltage Protection Detail

On the secondary side of the transformers, protection measures must be taken to ensure that the transformers are protected should an overcurrent occur on the system under test. This takes the form of a three-phase circuit breaker rated at 150A with a breakage curve that ensures breakage at 200A, the maximum operating current of the secondary side of the transformers. If the current goes to 250, or 125% of the rated secondary current, the breakage will occur within 10 minutes. In the case of a short on the bus, the breakage will occur in less than 1s.

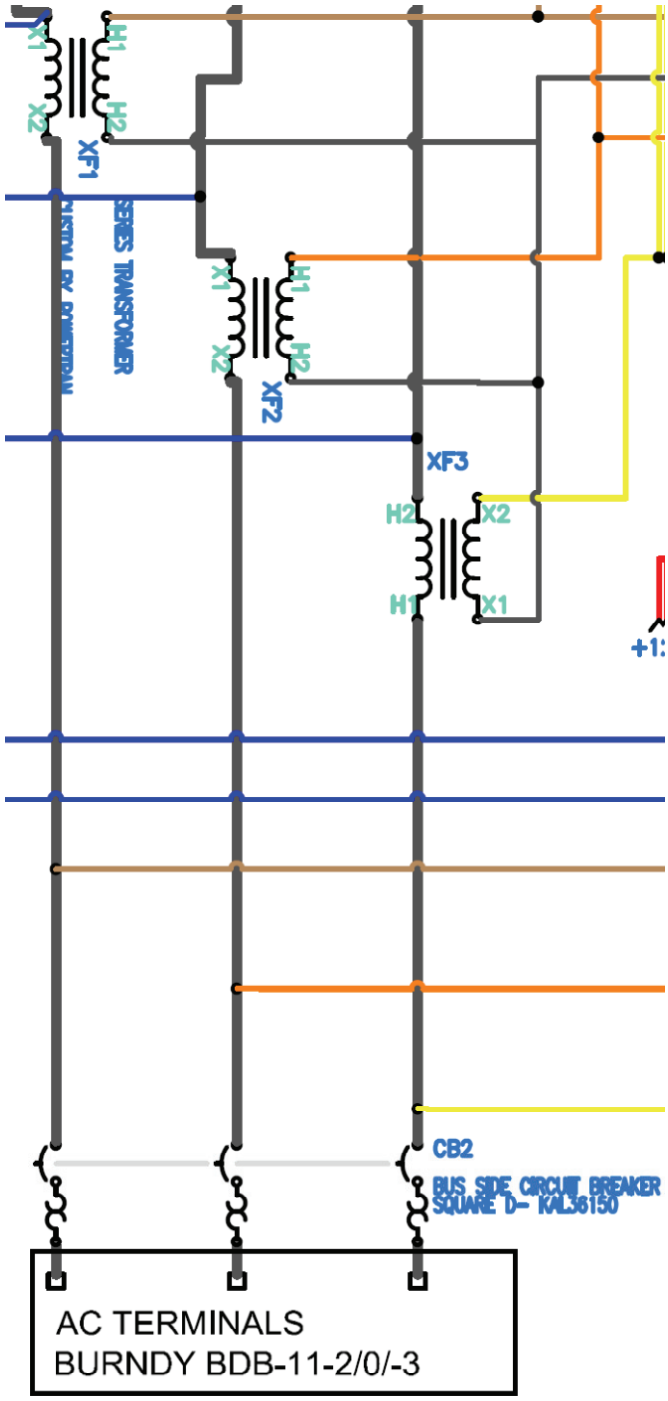

Figure 5.6: Transformer Secondary Side Overcurrent Protection Detail

The next possible problem is again on the secondary side of the transformers. If the overall bus voltage exceeds a maximum, the circuit must prevent the overvoltage from reaching the IGBTs. The PM1000 has a set of 3 voltage sensors attached to the source

side of the bus which are normally used for the phase locked loop, as described in the "Closed Loop Control Design" section. If these voltages exceed a specified maximum, comparators within the CPLD on the control board provide a hardware signal to stop PWM and a software signal to the measurement computer to open all relays attached to the bus, effectively isolating the PM1000 and its IGBTs from the overvoltage.

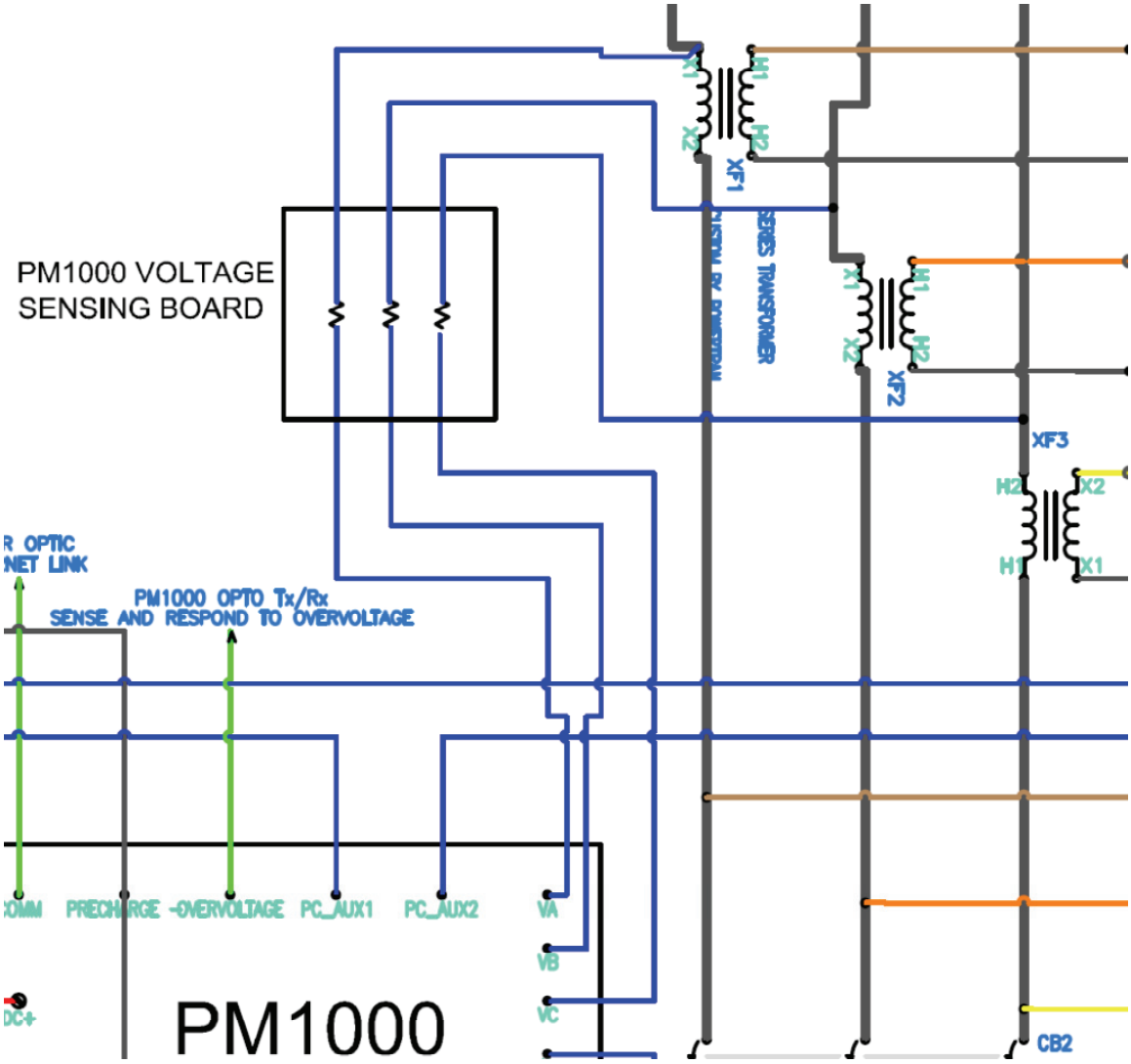

Figure 5.7: Secondary Side Overvoltage Protection Detail

The DC link capacitance is comprised of 3 parallel film capacitors in the PM1000 and 4 series/parallel electrolytic capacitors. The electrolytic capacitors are very large, and electrolytic capacitors have a reputation for exploding under overcurrent conditions. The

first protection against this is a fuse connected directly in series with the capacitors. The second is a 14 gauge steel box.

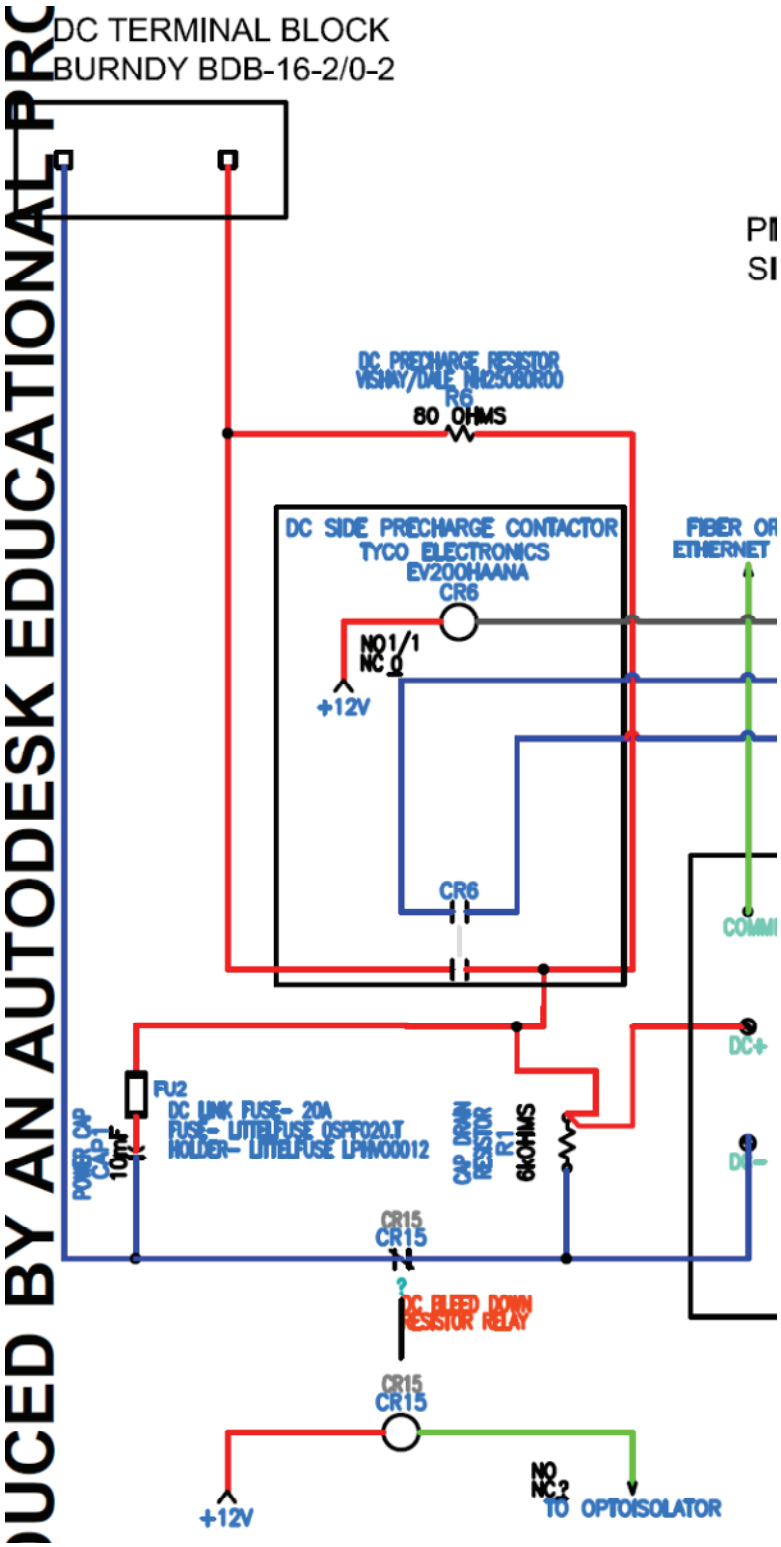

Figure 5.8: DC Link Detail

Note that the DC side also has a precharge circuit like the AC side. This converter may be fed power from the DC side, but this is not the case during normal operation. The DC terminal block normally remains unconnected, and the AC side brings the DC capacitor to the voltage and energy necessary for perturbation. However, precharge is required should the DC power terminals be used. There is no fuse in the DC precharge circuit; should the user choose to power the unit from the DC side, he or she is responsible for overcurrent protection.

Another safety mechanism in place is the DC link bleed down resistor. If left to its own devices, the DC link capacitor will take at least 3.75 minutes to reach safe voltage levels. A normally closed relay and resistor in series are placed in parallel with the DC capacitors to make this situation safer. Under normal operating conditions, this "bleed-down resistor" is disconnected from the DC link, as the host computer opens the "bleed-down relay". However, should an error, loss of bus voltage, loss of 120V power, or anything else that interrupts control occur, the normally closed relay will place the resistor in series with the DC Link, and within 30 seconds the DC voltage will reach safe levels.

The last and perhaps most important measure of safety is the DC overvoltage protection. This is done in hardware within the PM1000. Being that there is almost no margin of safety between the operating voltage of 875V and the 900V "DO NOT CROSS" value of the PM1000, the sensor associated with this safety mechanism must be extremely well calibrated.

6. Experimental Validation and Hardware Characterization

6.a Shunt Chirp

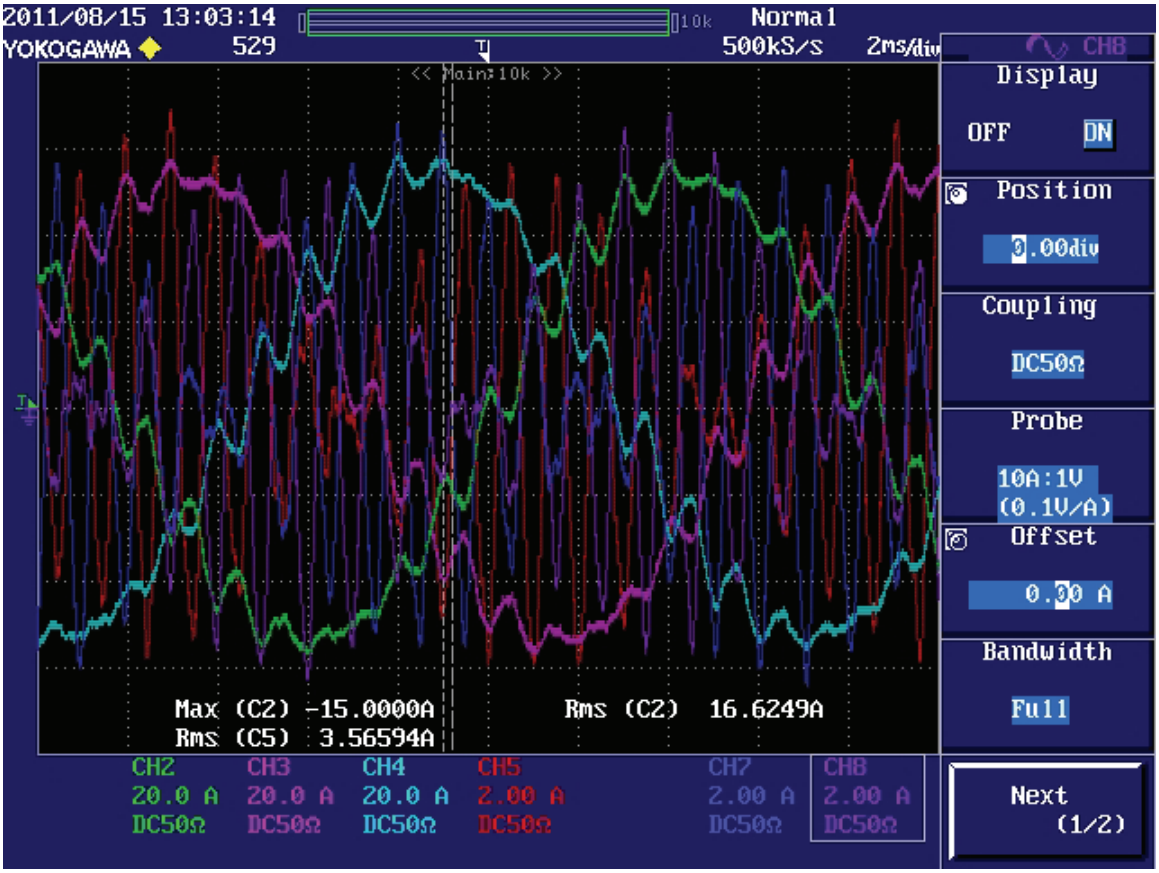

Figure 6.1: A Very Perturbed 30kW Bus

In most frequency ranges, the perturbation generation device can be used to generate a 12.5A RMS or 20V RMS perturbation. This can be dangerous if the system isn't designed to handle such a perturbation; figure 6.1 illustrates a 10% perturbation, which may be too much for some systems. While it's currently unknown what level of power is necessary to accurately the measure bus impedance, care should be taken to use the minimum amount for each situation.

For all experiments, a California Instruments MX-45-3pi-SNK and a 7 ohm/phase resistor bank comprised the test "bus". The system was operated at the nominal 460V RMS line-to-line voltage, but CPES does not currently have the capability to operate a 360V bus at the 100kW used in the design specifications. Here, the bus was operated at 30kW. Figure 6.2 shows the equipment used.

Figure 6.2: Test "Bus"

Throughout the sections of the "Experimental Validation" portion of this thesis that involve shunt injection, "Perturbation" and "Bus" currents are described. Figure 6.3 shows the exact location of current measurements for each of these signals.

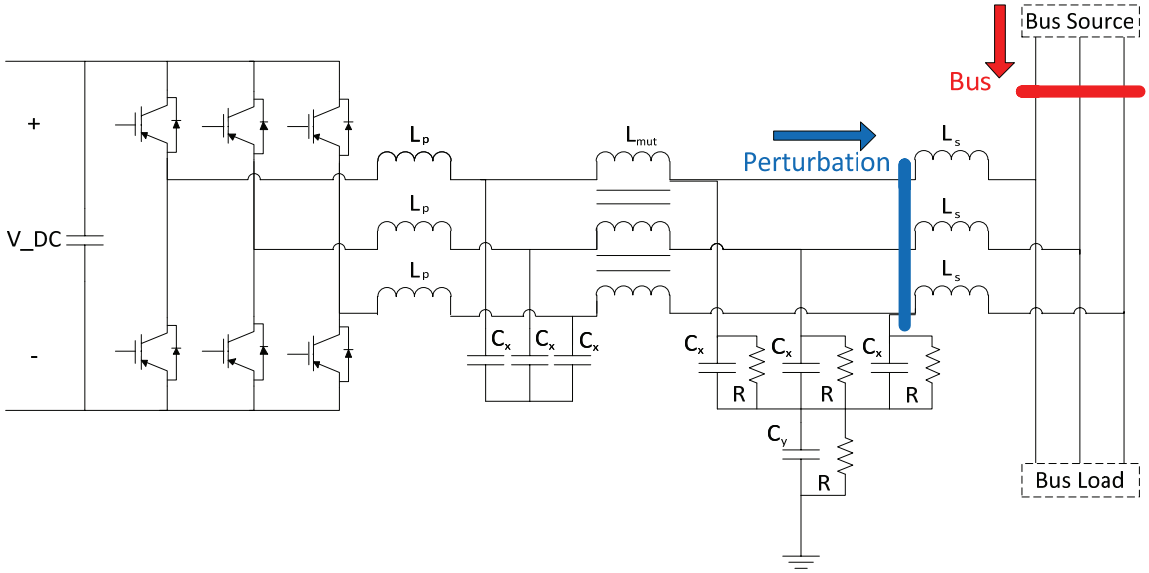

Figure 6.3: Shunt Current Measurement Locations

The following plots are the result of a 10 second chirp from 0Hz-1000Hz repeated 6 times.

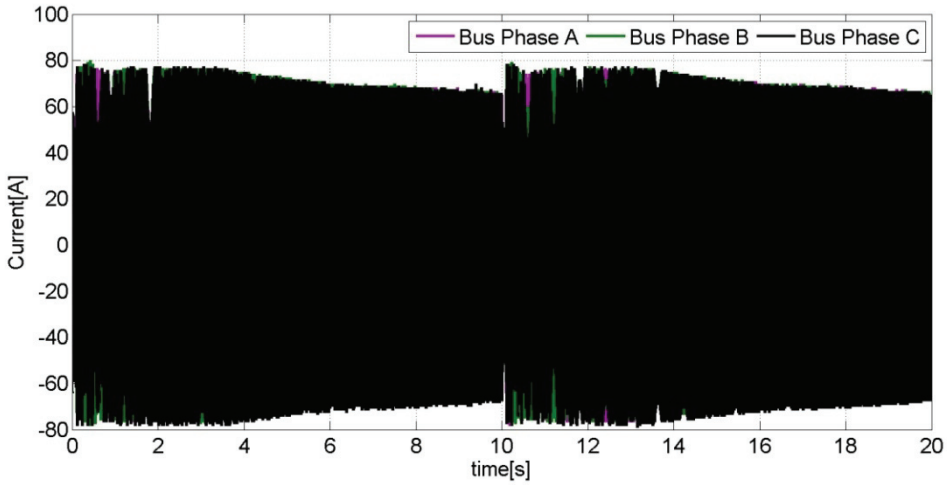

Figure 6.4: Two 10 second Shunt Chirps from 0-1000Hz in d, Bus Currents

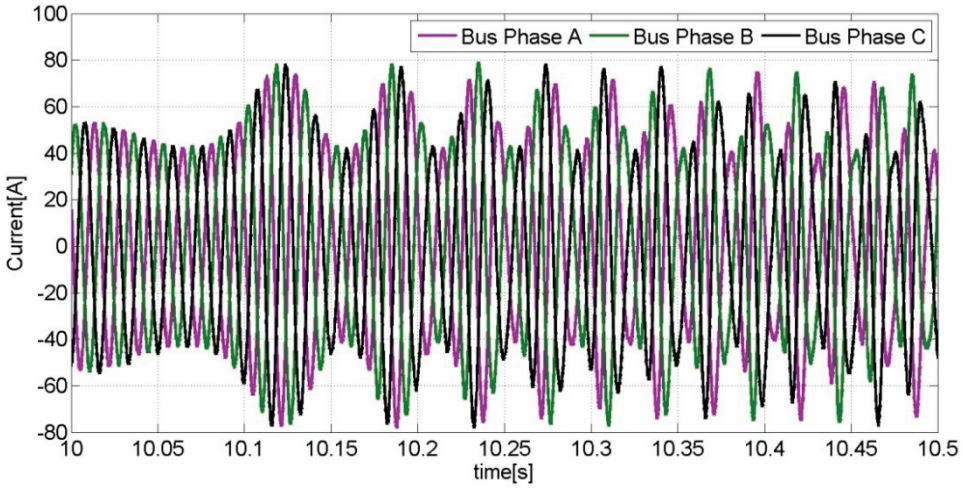

Figure 6.5: Low Frequency d Channel Shunt Chirp Detail, Bus Currents

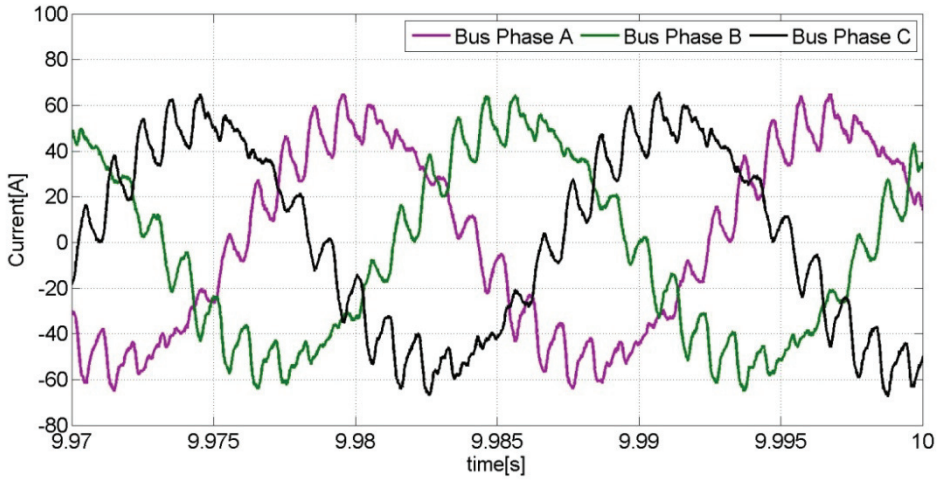

Figure 6.6: High Frequency d Channel Shunt Chirp Detail, Bus Currents

Figures 6.4, 6.5, and 6.6 show the effects on the bus of a 10s, 0-1kHz chirp in shunt. For this experiment (and all shunt experiments), a DC link voltage controller is implemented as well as the current controllers. This allows for infinite length perturbations, but produces a small amount of distortion in the signal most apparent at the beginning of each chirp; this shows up as a slight "spike" in the current as each chirp starts. It is also of note that at a certain frequency, the current level begins to decrease. This is a result of the shunt output stage inductance increasing in impedance as the chirp frequency increases. The perturbation signals that cause these bus currents are shown below.

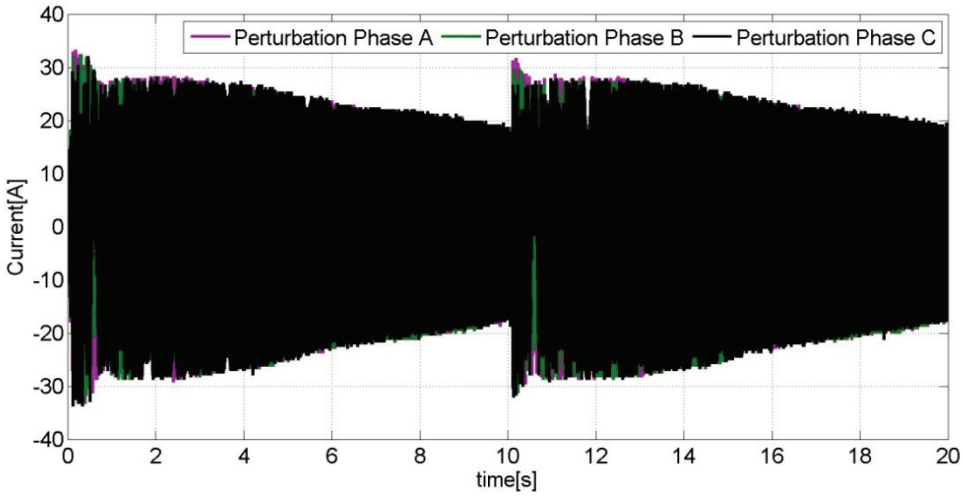

Figure 6.7: Two 10 second Shunt Chirps from 0-1000Hz in d, Perturbation Currents

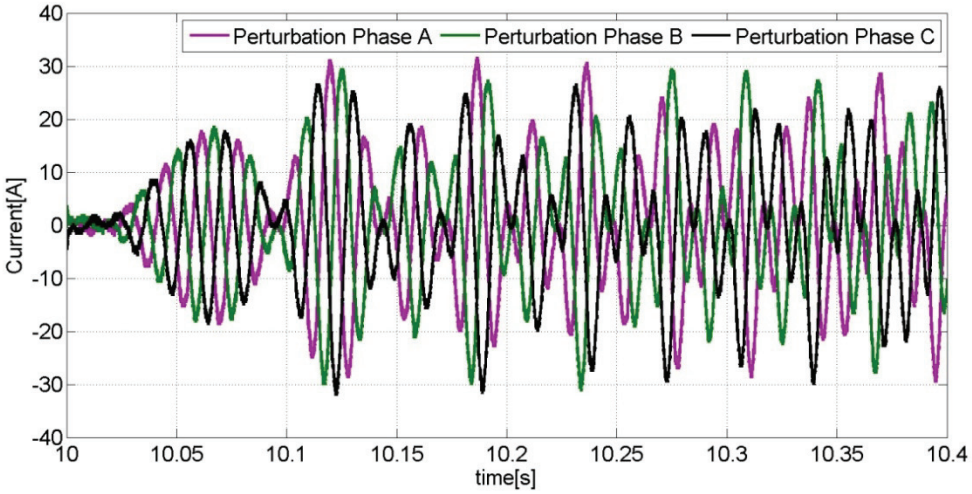

Figure 6.8: Low Frequency d Channel Shunt Chirp Detail, Perturbation Currents

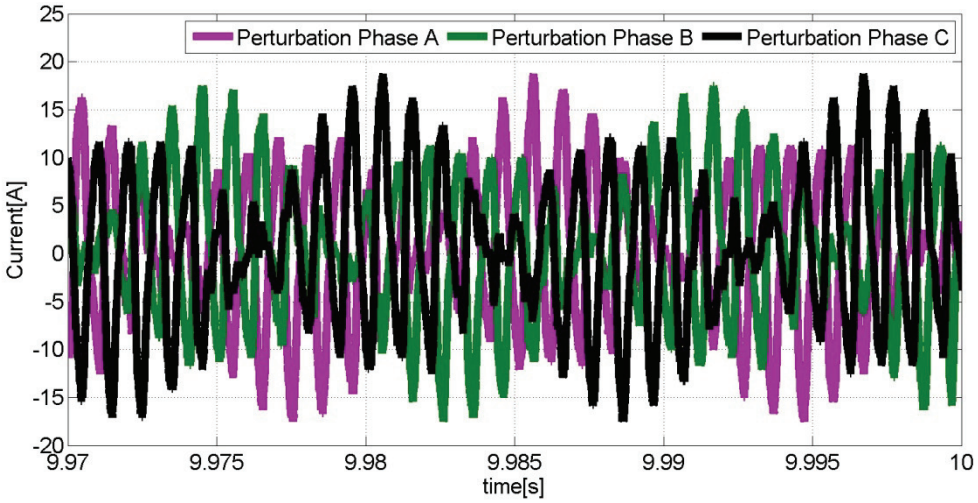

Figure 6.9: High Frequency d Channel Shunt Chirp Detail, Phase Currents

Figures 6.7-6.9 show the perturbation currents during the same intervals as Figures 6.4-6.6. The DC controller "spike" is more pronounced here, as there's no nominal bus current to mask it. Also notice the 60Hz component in the high frequency detail; this is also caused by the DC controller, and is in 180 degrees out of phase with the bus voltages, resulting in active power from the bus to the DC link capacitor to keep it charged.

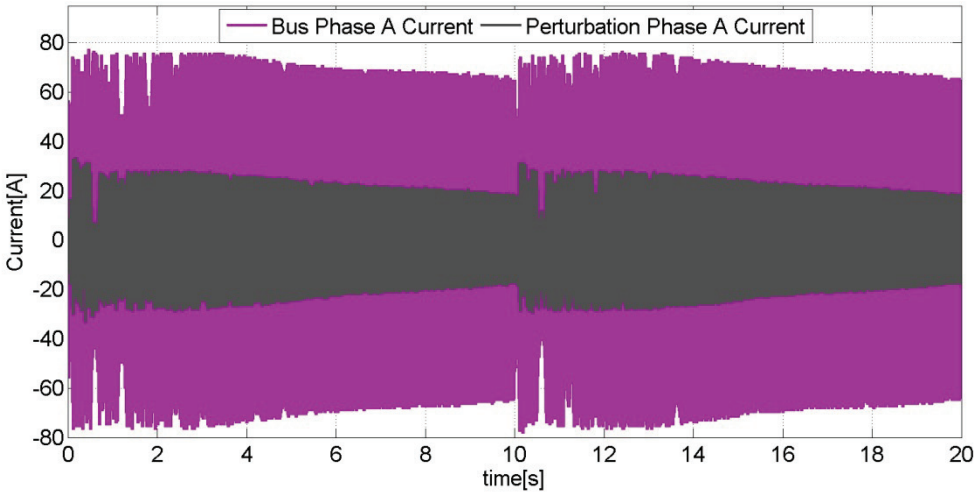

Figure 6.10: Two 10 second Shunt Chirps from 0-1000Hz in d, Perturbation and Bus Phase A Currents

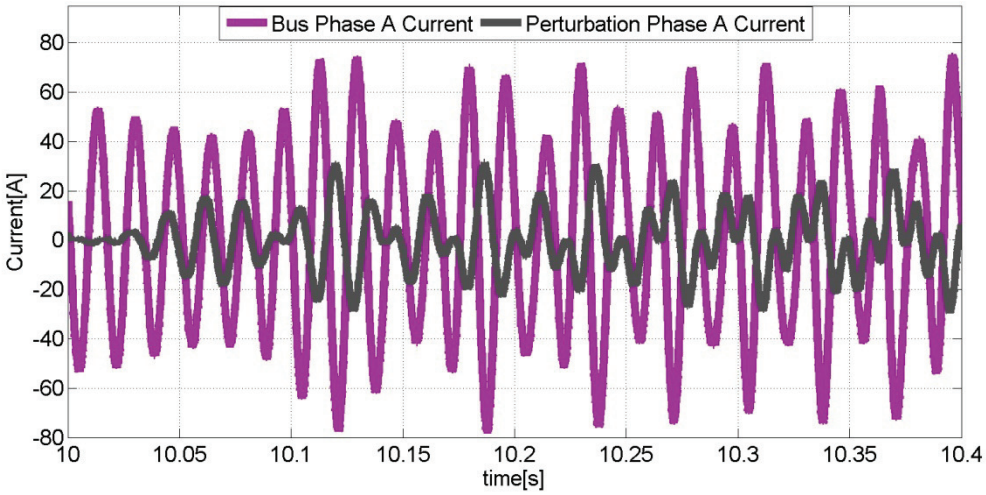

Figure 6.11: Low Frequency d Channel Shunt Chirp Detail, Perturbation and Bus Phase A Currents

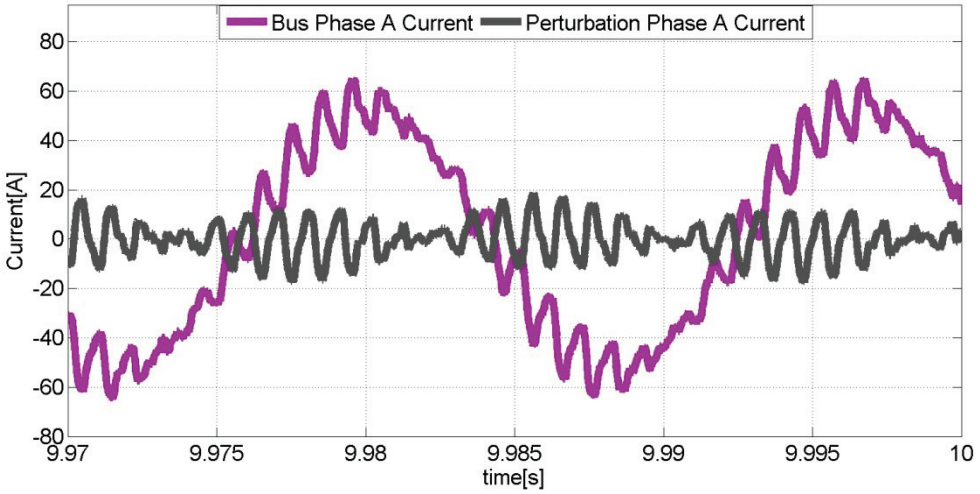

Figure 6.12: High Frequency d Channel Shunt Chirp Detail, Perturbation and Bus Phase A Currents

Figures 6.10-6.12 show a single phase bus and perturbation current set to better illustrate the previously described effect that the perturbation has on the bus current.

The d and q perturbations are nearly identical in nature when using the 45 degree PLL alignment, but have a few small differences. The chirp signal illustrates these differences well.

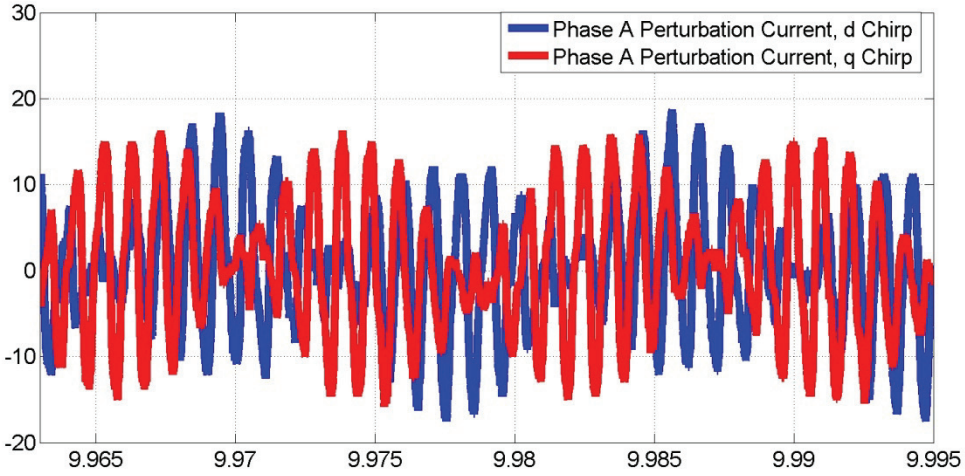

Figure 6.13: Phase A Perturbation Currents as a Result of a d Channel Shunt Perturbation and a q Channel Shunt Perturbation

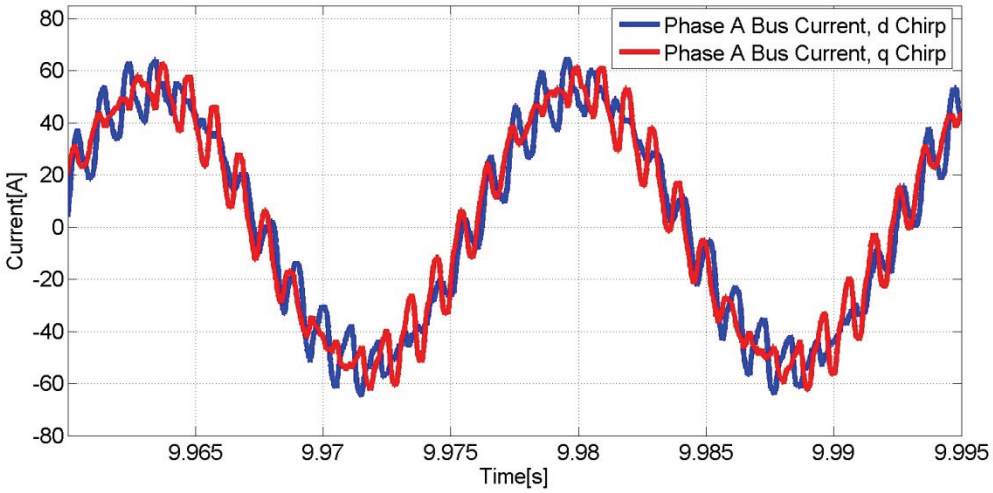

Figure 6.14: Phase A Bus Currents as a Result of a d Channel Shunt Perturbation and a q Channel Shunt Perturbation

The overall and low frequency comparisons between a d chirp and a q chirp are not shown here because they look almost identical at those scales. Only when the high frequency behavior of the two perturbations is studied can the differences be ascertained. In figure 6.13, it can be clearly seen that the perturbations are 90 degrees apart on the time scale of the 60Hz bus frequency. In figure 6.14, the greatest portions of the

perturbation effects on the bus for each perturbation can be seen to be at 90 degrees from one another with respect to the bus frequency.

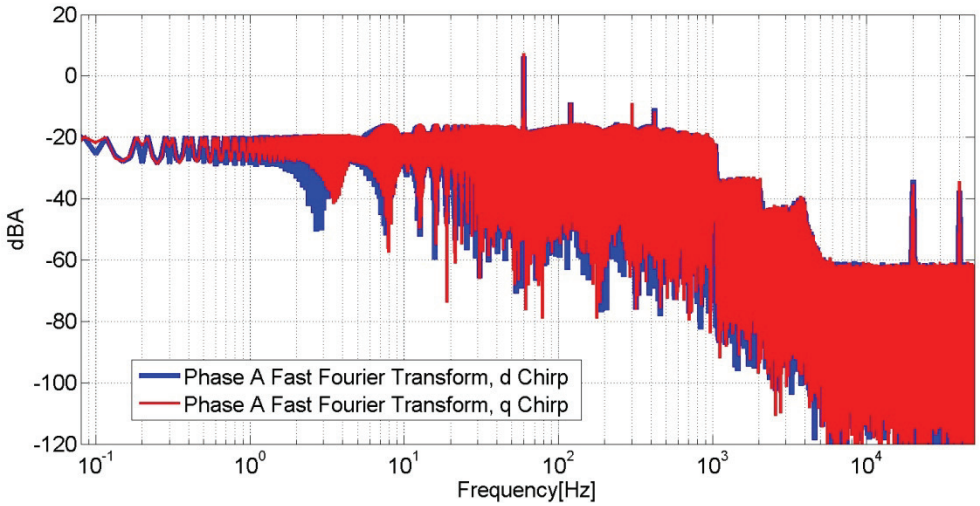

Figure 6.15: Phase A Perturbation FFT as a Result of a Shunt Chirp in d and in q

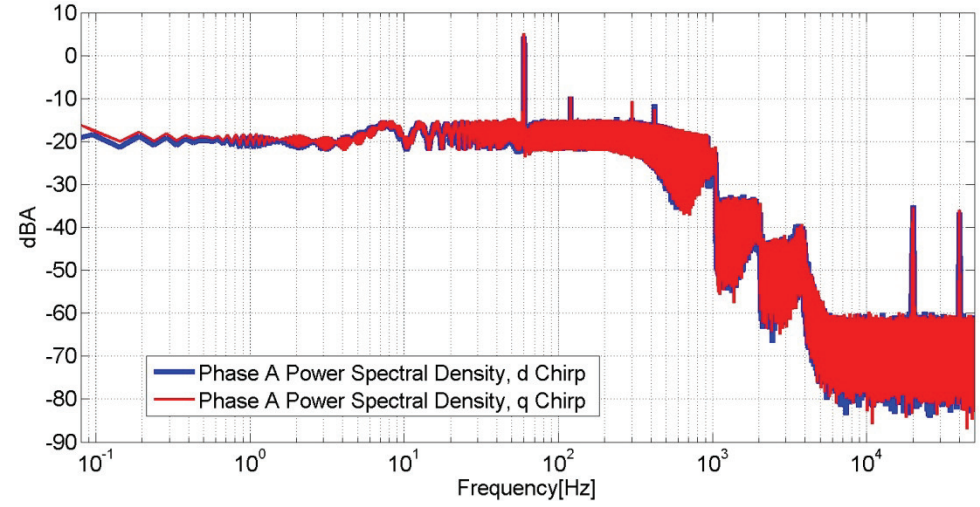

Figure 6.16: Phase A Perturbation PSD as a Result of a Shunt Chirp in d and in q

As shown in figures 6.15 and 6.16, very little difference can be seen in the abc domain frequency analysis of the perturbation signals as a result of the d and q chirps. It's not until the d-q-tranformed signals are studied that the majority of the difference between the two can be seen. This difference can be be seen when studying the d channel

current as a result of a perturbation in d and comparing it to the q channel current as a result of a q perturbation.

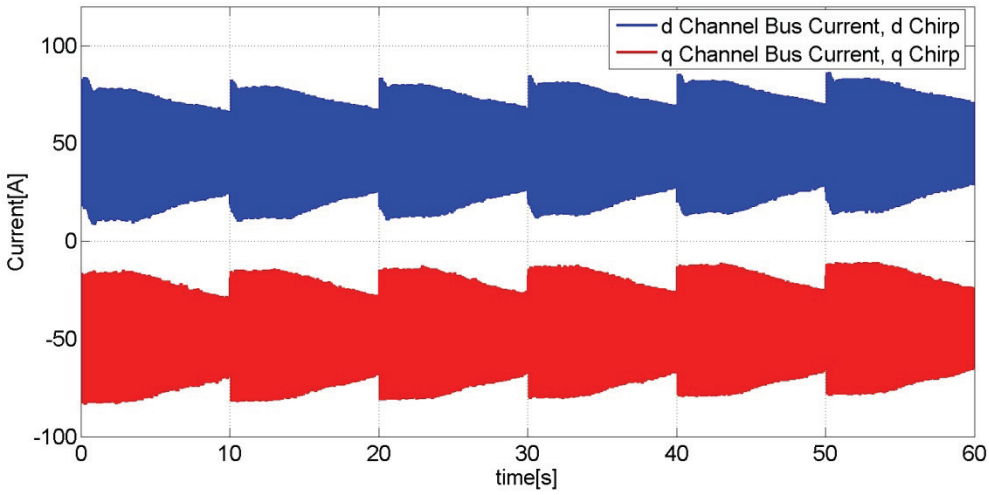

Figure 6.17: Comparison of Perturbed Channel Bus Currents in d and q, 45 Degree d-q-to-Bus Voltage Alignment

Here, the d-q alignment is set to 45 degrees from the bus voltage, as it was when the perturbations were generated. The fact that the d perturbation results in a positive bus current and the q perturbation results in a negative bus current speaks only to the alignment with respect to the bus nominal frequency, and shouldn't be considered a difference; if the d-q alignment was at 135 degrees to the bus voltage instead of 45 degrees, the d channel would be negative and the q positive.

The aforementioned effects of the DC link controller are seen here, and are indeed the only difference between the d and q channel perturbations. For both perturbations, the DC link controller makes use of the d channel. Therefore, the DC controller-caused "spike" can be seen in the d perturbation, but not in the q perturbation. Other than this, the two signals are almost identical in effect, only 90 degrees apart with respect to the phase of the nominal bus frequency. An interesting comparison to make is between the two perturbations when the d-q angle is set to be in phase with the oscillation of the nominal bus frequency.

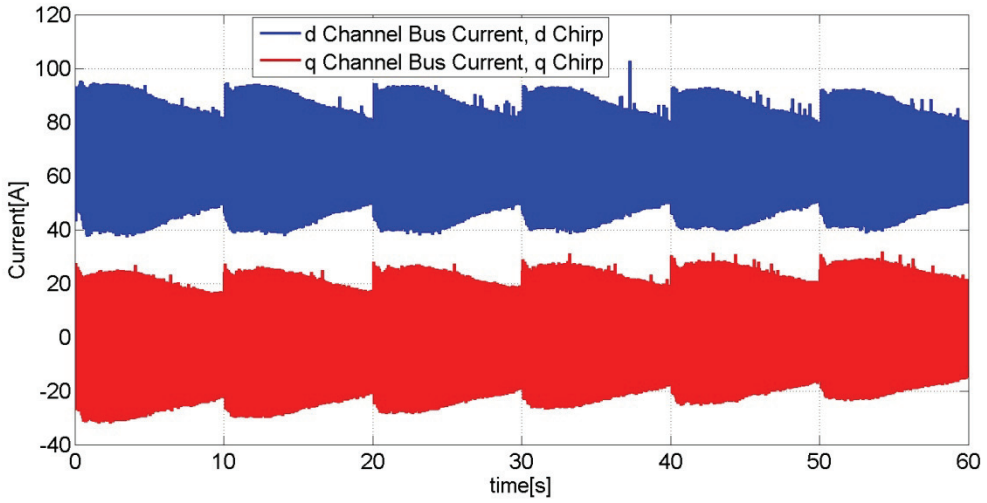

Figure 6.18: Comparison of Perturbed Channel Bus Currents in d and q, 0 Degree d-q-to-Bus Voltage Alignment

Figure 6.18 shows that when aligned to bus voltage, the perturbations are identical, but the q perturbation is now centered about zero. This is as would be expected when the PLL aligns d to be the active power channel.

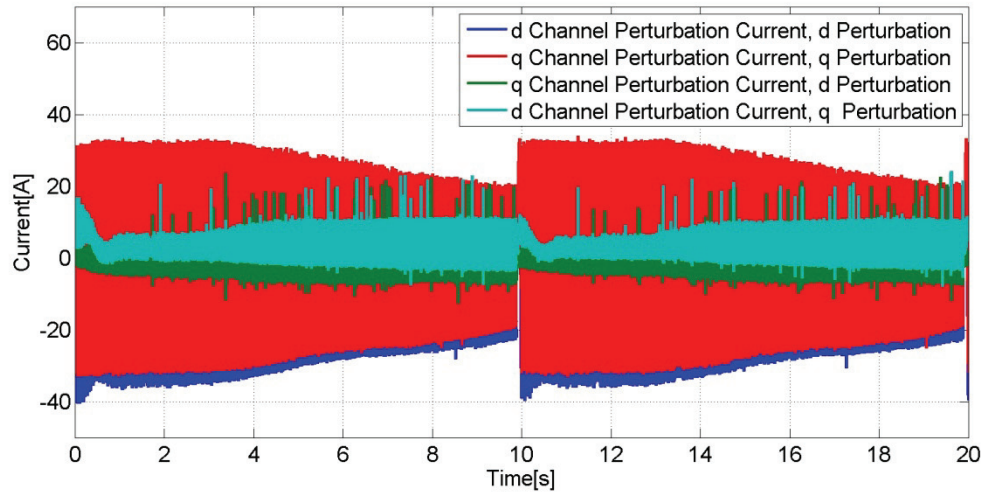

Figure 6.19: Comparison of d and q Channel Perturbation Currents in d and q, 45 Degree d-q-to-Bus Voltage Alignment

A comparison of both d and q c perturbation currents as a result of both d and q channel perturbations illustrates the differences best. No matter which perturbation is underway, the d channel always sees the effects of the DC link controller, which include an initial spike and a DC offset of the rotating reference frame current.

At 45 degrees of alignment to the nominal bus phase, both the d and the q channel have the same magnitude of effect on active power. For safety reasons, the q channel chirp was commanded to be negative in the d-q reference frame. This results in the initial DC link voltage transient always starting negative, which in turn results in a lower probability for DC link overvoltage. When the q-channel d-q command is negative, both chirps have an identical effect on active power, and therefore an identical effect on the DC link voltage.

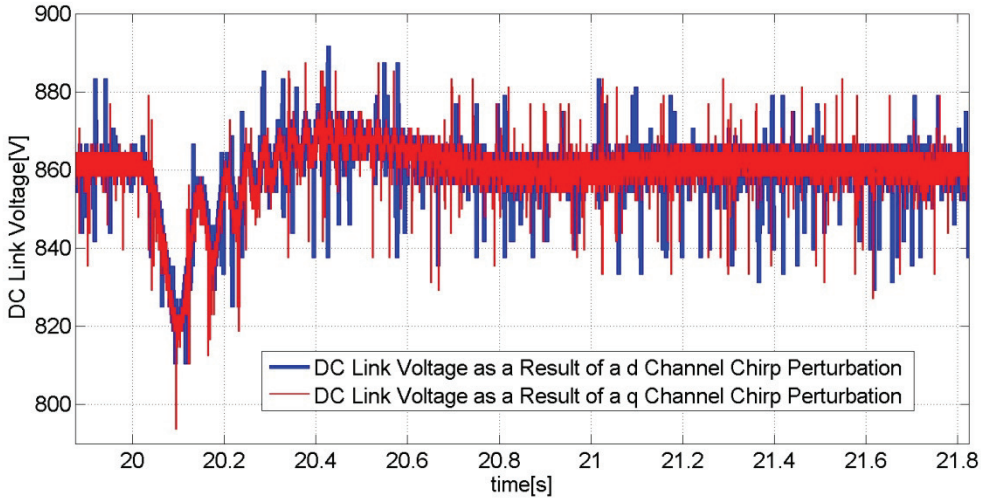

Figure 6.20: DC Link Voltage as a Result of the d and q Channel Perturbations

Figure 6.20 bears quite a resemblance to Figure 4.12, the Fresnel function, although it is inverted. It should; the DC link voltage mirrors the energy expenditure that a perturbation signal requires. Here, the Fresnel function is "bent"- the DC link voltage controller is slow enough to not interfere much with the lower frequency signal generation, but brings the voltage back up to the voltage level necessary for higher frequency perturbation.

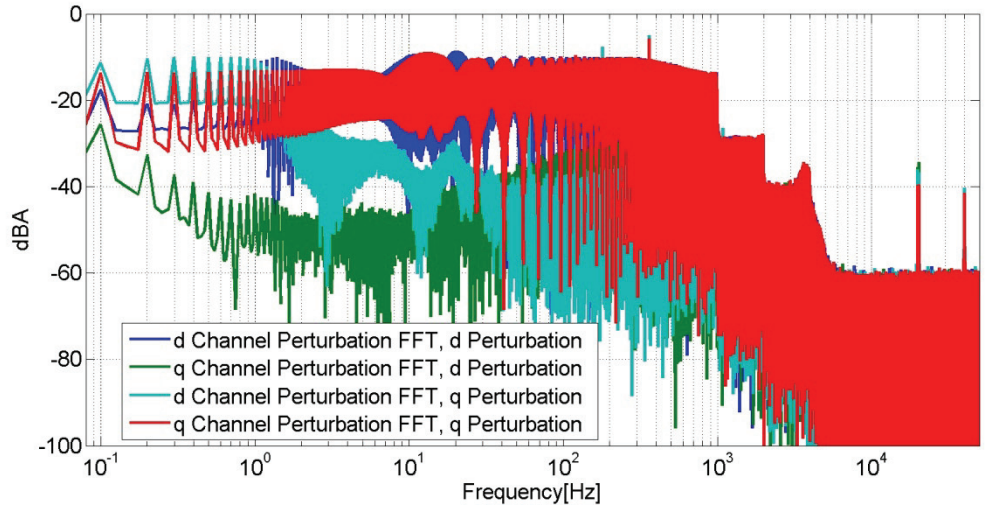

Figure 6.21 d and q Perturbation Current Fast Fourier Transforms as a Result of a d and q Perturbation

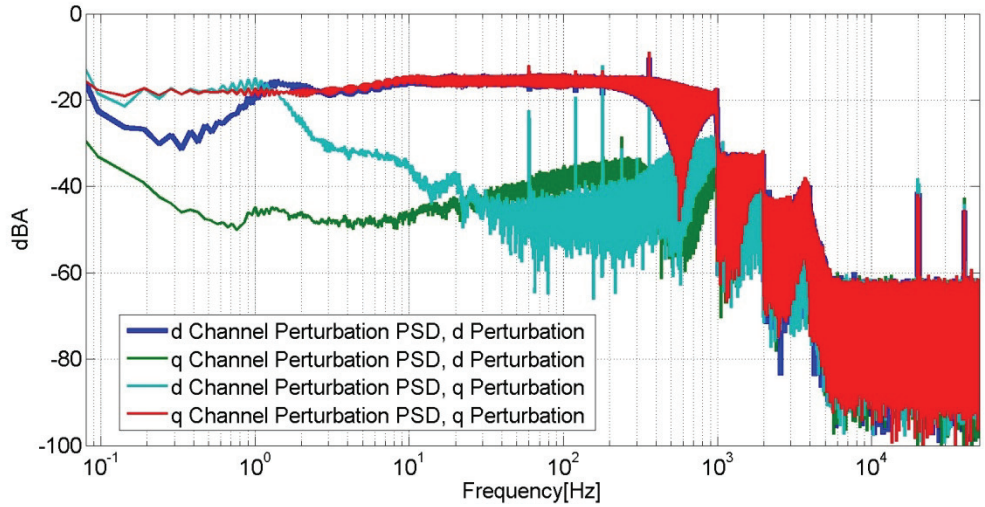

Figure 6.22 d and q Perturbation Current Power Spectral Densities as a Result of a d and q Perturbation

Judging from the spectral analysis of the perturbation waveforms, it seems to be easier to get a higher low frequency response with the channel not tied to the DC link controller (the d channel in this case). This feature accurately sums up the difference between the d and q perturbations when the two are set at 45 degrees to the phase of the

bus voltage active direction and one is used in conjunction with a DC link controller. The two perturbations are identical with regard to active power with the exception of the effect of the DC link controller. Being that both channels have an active power direction component, the DC link controller could be tied to whichever channel is not currently in use for perturbation, resulting in identical effects for both channels. However, this is outside the scope of this thesis. For now, it can be seen that it's more difficult to get a desirable frequency spectrum with the channel tied to the DC link controller, albeit minimally. Therefore, for the remainder of the signals studied in this thesis, only the d (DC controller-tied) channel will be studied.

The same figures used to describe the differences between d and q perturbation here can also be used to describe the results of the shunt chirp tests. As can be seen from the figures in this section, a full 10kW chirp (12.5A RMS) can be made from 0 to approximately 350Hz, at which point the power stage inductance reaches an impedance that begins to limit the injectable power. The overall chirp power for the d and q channels are shown below.

	d Perturbation	q Perturbation
Current (A RMS) per Phase	10.619	10.768
% of 125.3A (nominal 460V, 100kW Bus Phase Current)	8.475	8.594
Power on a 460V, 100kW Bus (kW)	8.475	8.594

Table 6.1: Achieved Perturbation Power, Chirp in Shunt

6.b Shunt Sine

Tests were performed to inject a single sinusoidal frequency into the bus at .1Hz, 1 Hz, 10Hz, 100Hz, and 1000Hz. Figures 6.22 to 6.24 show the spectral content of the perturbations resulting from these tests.

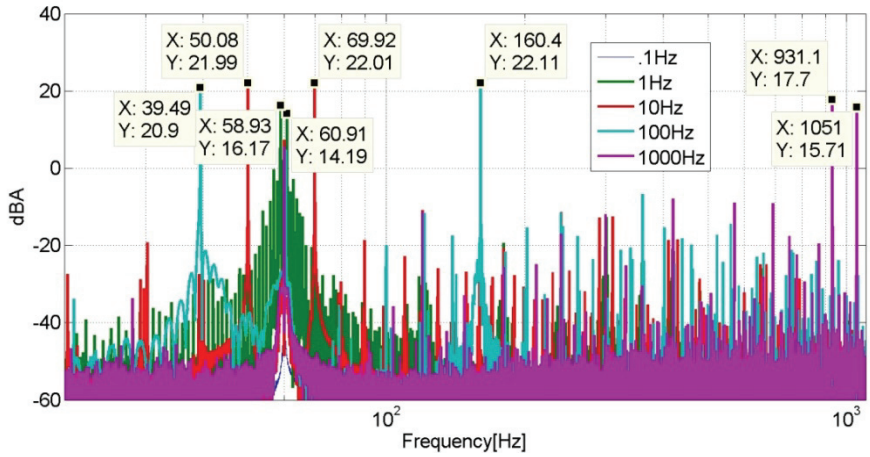

Figure 6.23: FFT of Phase A 1Hz, 10Hz, 100Hz, and 1000Hz Sinusoidal Shunt Perturbations

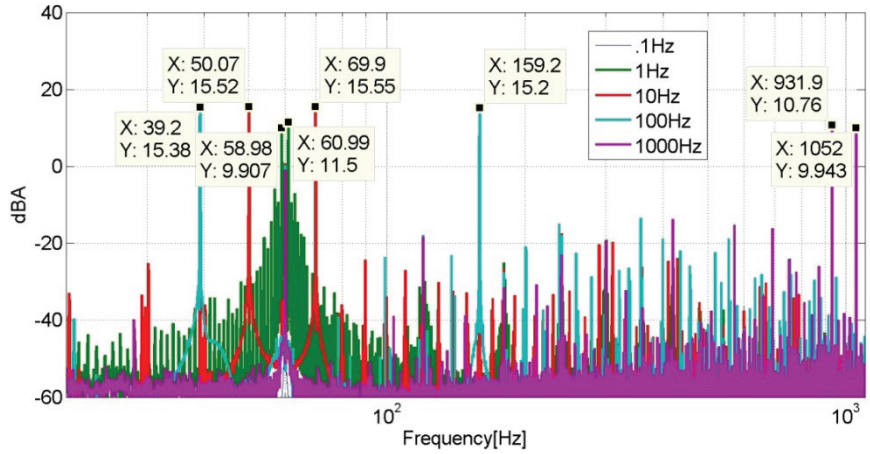

Figure 6.24: PSD of Phase A 1Hz, 10Hz, 100Hz, and 1000Hz Sinusoidal Shunt Perturbations

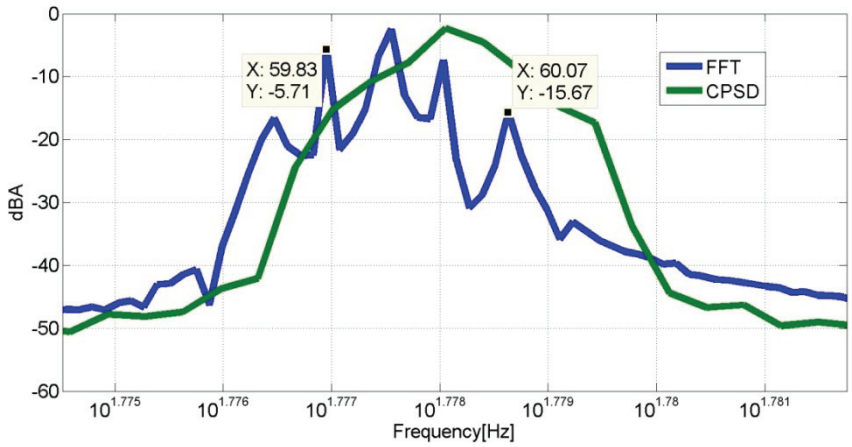

Figure 6.25: FFT and PSD of .1Hz Sinusoidal Shunt Perturbation

Note that in the abc domain, the .1Hz d-q perturbation is very difficult to see, as shown in figure 6.24. This is due to the fact that a .1 Hz d-q perturbation shows up in the abc domain as 59.9Hz and 60.1Hz, which requires a very, very high FFT/PSD resolution to see. Such a perturbation is much easier to see in the d-q domain, as will be shown below.

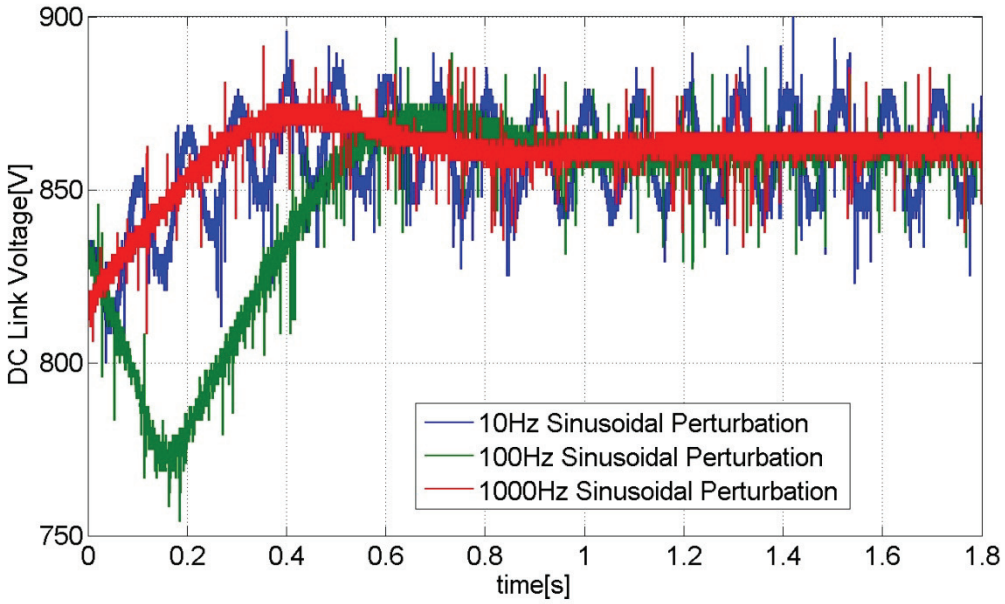

Figure 6.26: DC Link Behavior under 10Hz, 100Hz, and 1000Hz Sinusoidal Shunt Perturbations

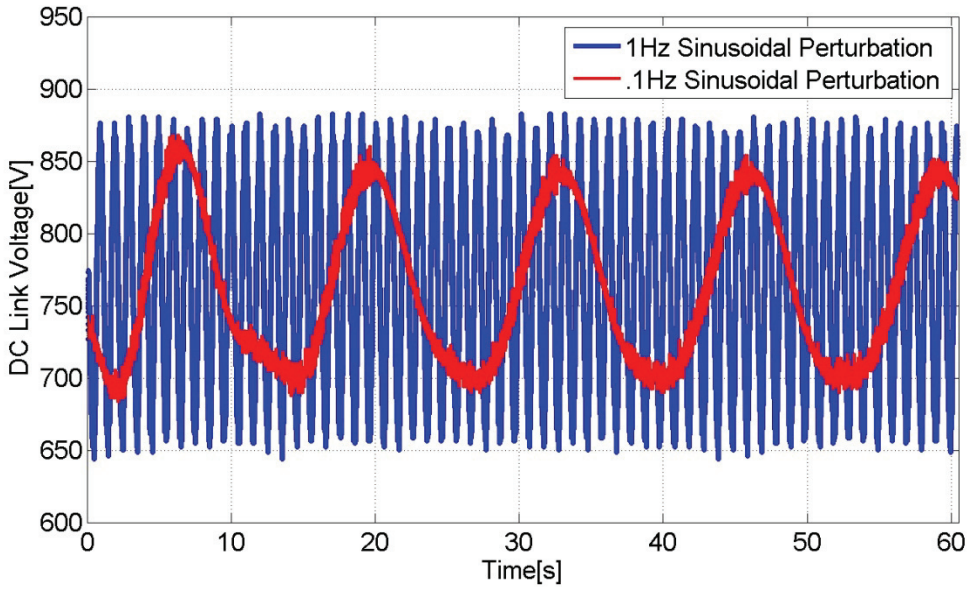

Figure 6.27: DC Link Behavior under .1Hz and a 1Hz Sinusoidal Shunt Perturbations

In order to perturb the system, the DC voltage must be at least 650V. The DC overvoltage value is 885V. This envelope must be adhered to during all perturbations. This limitation is of little consequence when injecting signals above 10 Hz, as seen in figure 6.25, but results in quite a challenge when injecting lower frequencies, as seen in figure 6.26. The DC link controller parameters had to be changed to allow for the 1 Hz and .1Hz perturbations: the DC controller proportional gain was changed from .2 to .003 for both the .1 and 1Hz tests.

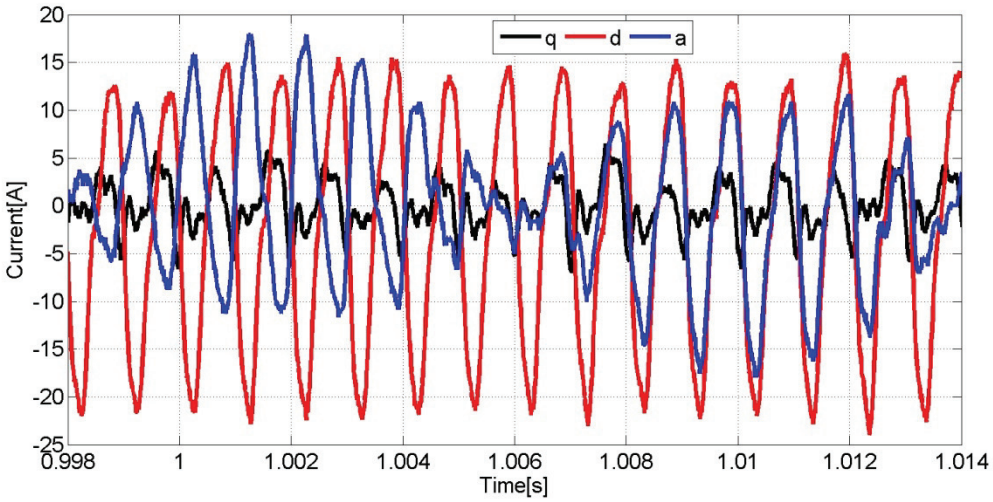

Figure 6.28: 1000Hz Sinusoidal Shunt Perturbation Phase A, d, and q Currents

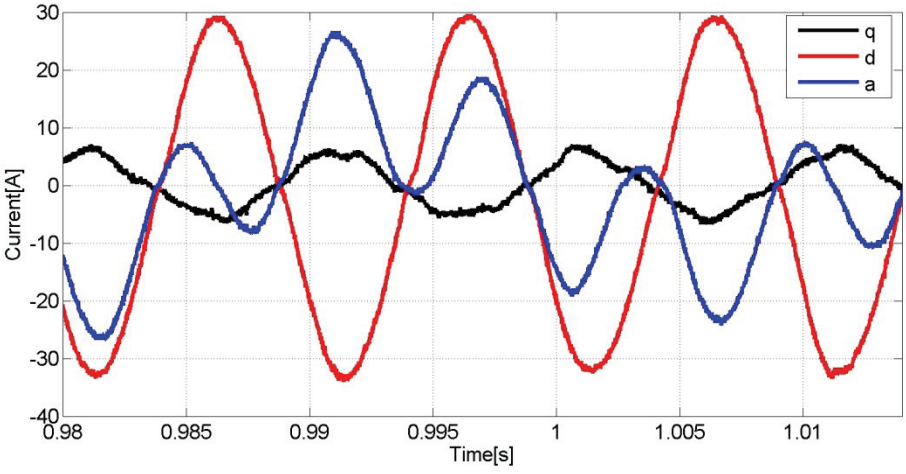

Figure 6.29: 100Hz Sinusoidal Shunt Perturbation Phase A, d, and q Currents

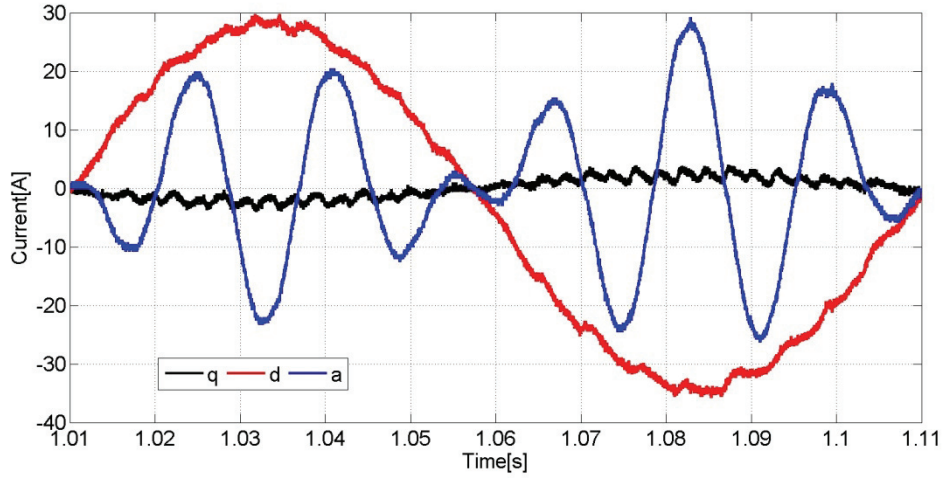

Figure 6.30: 10Hz Sinusoidal Shunt Perturbation Phase A, d, and q Currents

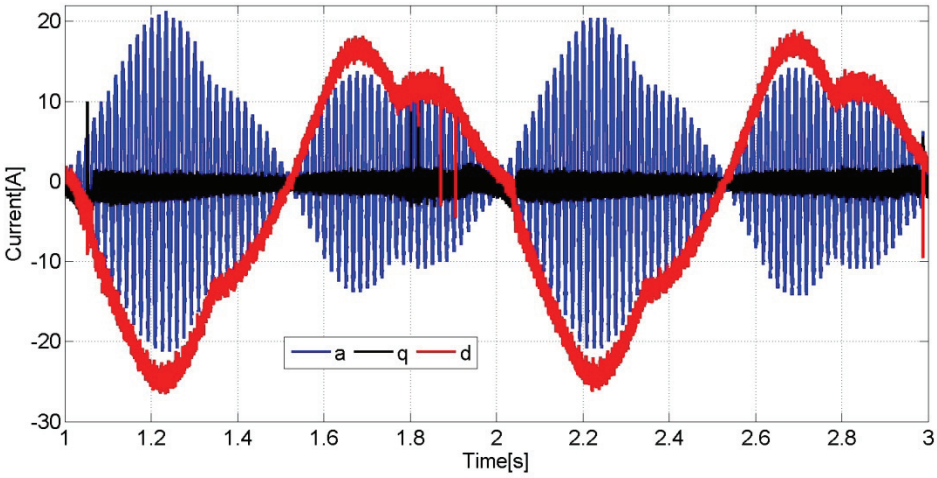

Figure 6.31: 1Hz Sinusoidal Shunt Perturbation Phase A, d, and q Currents

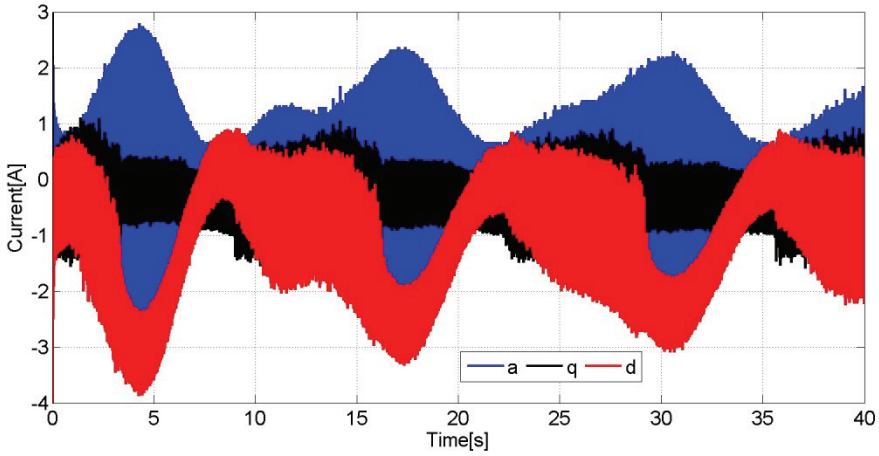

Figure 6.32: .1Hz Sinusoidal Shunt Perturbation Phase A, d, and q Currents

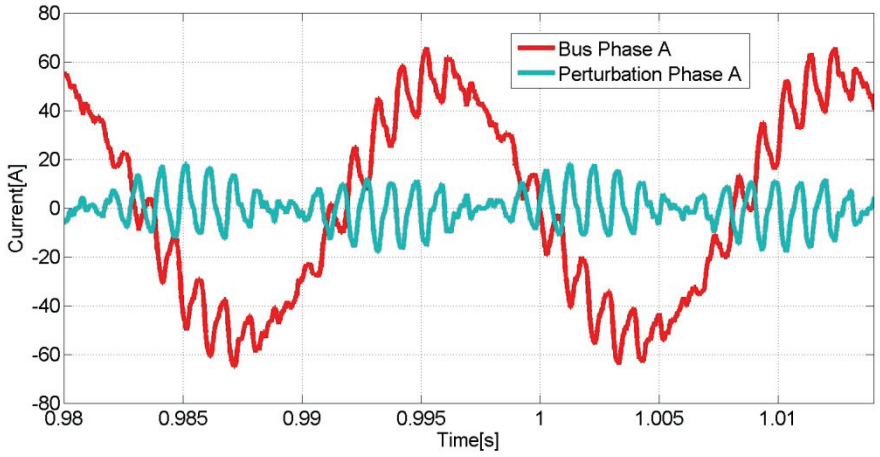

Figure 6.33: 1000Hz Sinusoidal Shunt Perturbation Phase A and Bus Phase A Currents

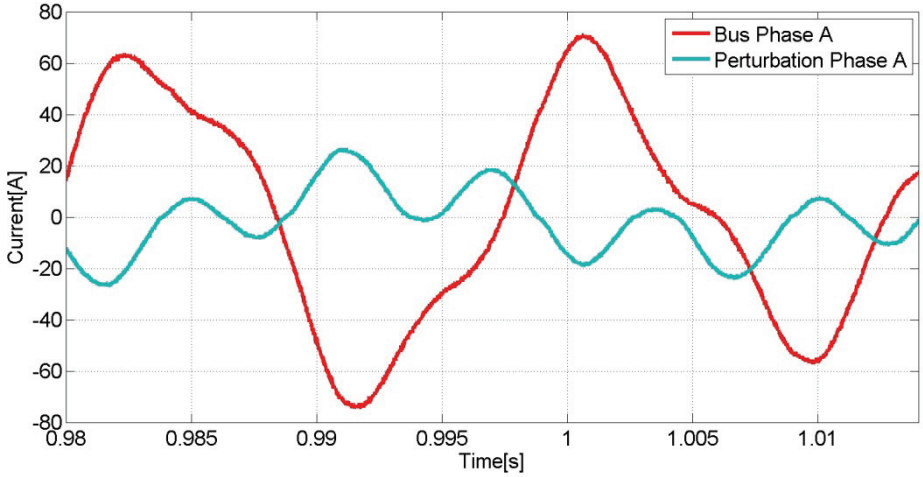

Figure 6.34: 100Hz Sinusoidal Shunt Perturbation Phase A and Bus Phase A Currents

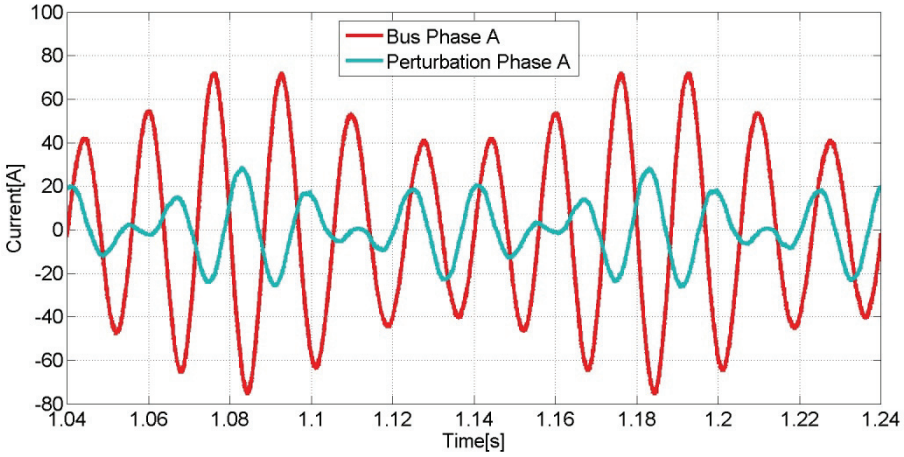

Figure 6.35: 10Hz Sinusoidal Shunt Perturbation Phase A and Bus Phase A Currents

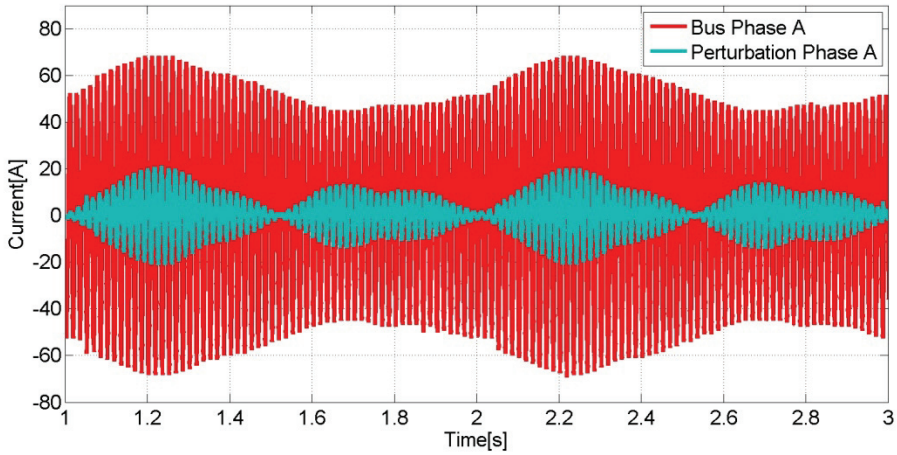

Figure 6.36: 1Hz Sinusoidal Shunt Perturbation Phase A and Bus Phase A Currents

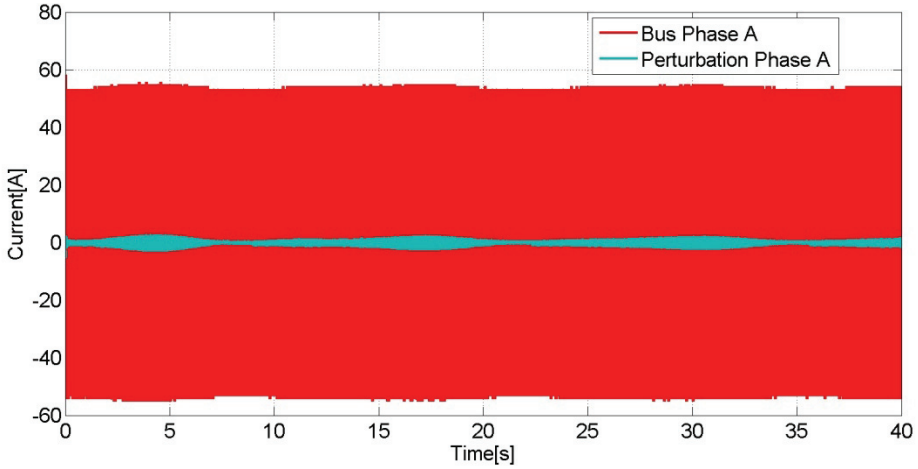

Figure 6.37: .1Hz Sinusoidal Shunt Perturbation Phase A and Bus Phase A Currents

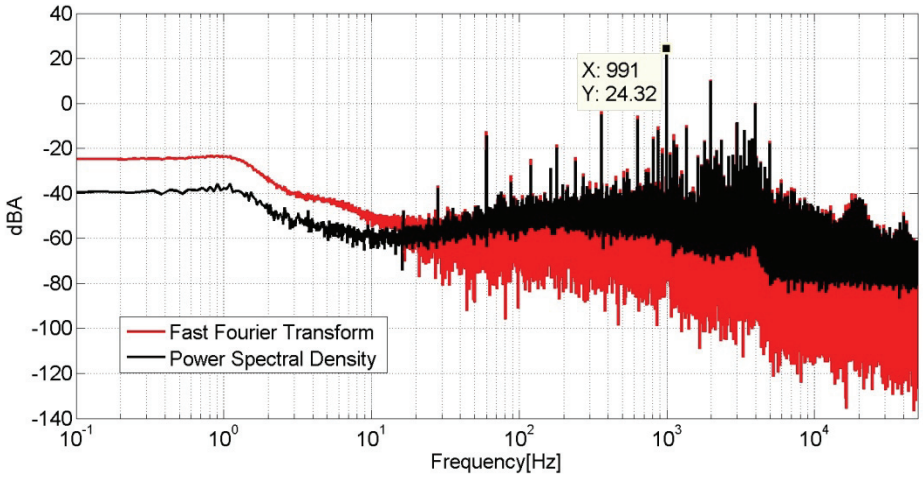

Figure 6.38: 1000Hz Sinusoidal Shunt Perturbation d-q Domain FFT and PSD

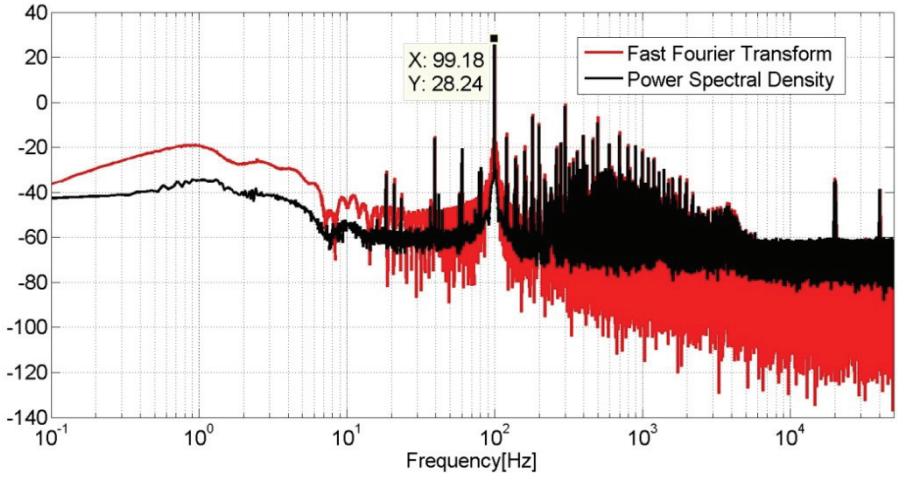

Figure 6.39: 100Hz Sinusoidal Shunt Perturbation d-q Domain FFT and PSD

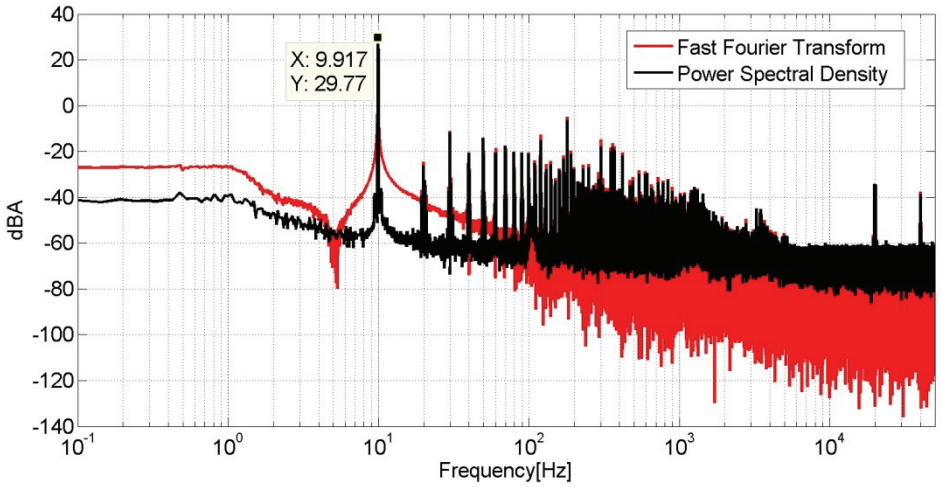

Figure 6.40: 10Hz Sinusoidal Shunt Perturbation d-q Domain FFT and PSD

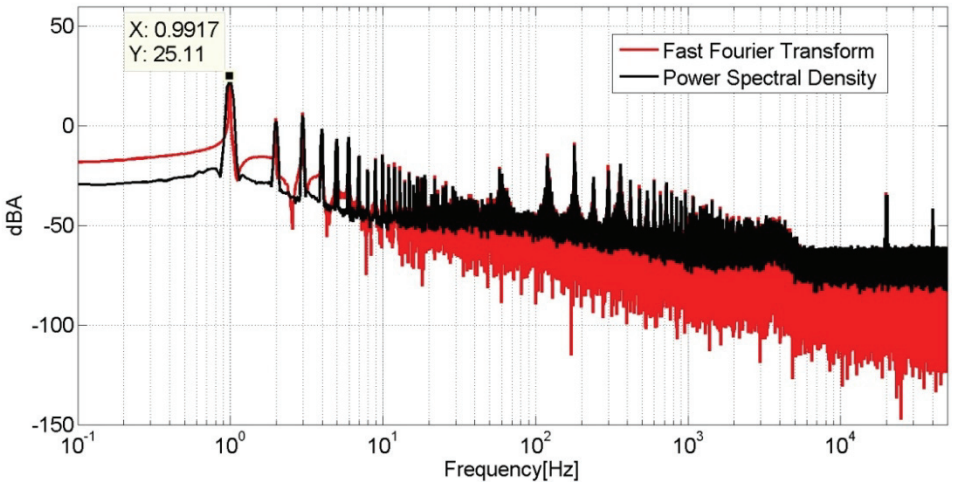

Figure 6.41: 1Hz Sinusoidal Shunt Perturbation d-q Domain FFT and PSD

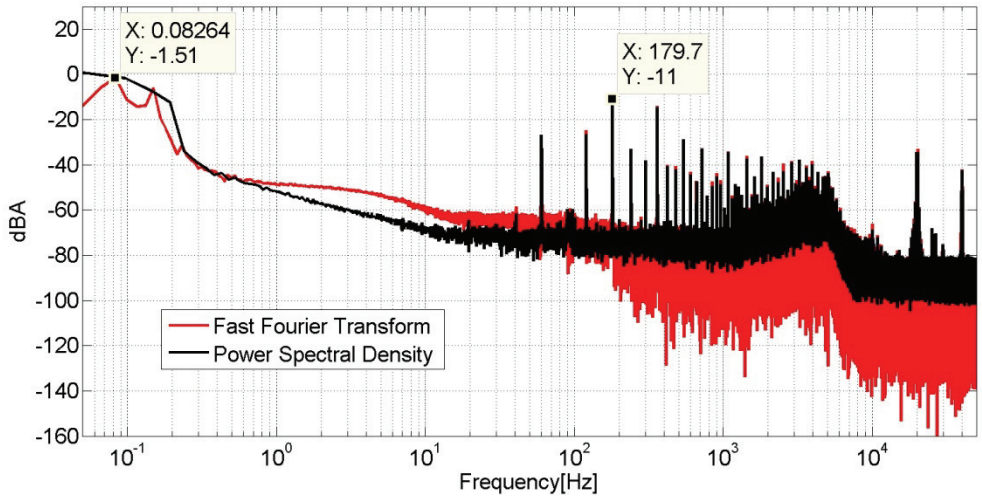

Figure 6.42: .1Hz Sinusoidal Shunt Perturbation d-q Domain FFT and PSD

Figures 6.27 to 6.41 show the results of the shunt sinusoidal perturbation tests at .1, 1, 10, 100, and 1000Hz, which are summed up in the tables below.

	.1Hz	1Hz	10Hz	100Hz	1000Hz
Current (A RMS) per Phase	0.900	7.720	12.840	12.590	7.580
% of nominal 460V, 100kW Bus Phase Current	0.718	6.161	10.246	10.047	6.049
Power on a 460V, 100kW Bus (kW)	0.718	6.161	10.246	10.047	6.049

Table 6.2: Power Injection for Sinusoidal Shunt Perturbation, Total Signal

	.1Hz	1Hz	10Hz	100Hz	1000Hz
Current (A RMS) per Phase	0.343	7.35	12.57	10.542	6.713
% of nominal 460V, 100kW Bus Phase Current	0.273	5.865	10.030	8.412	5.356
Power on a 460V, 100kW Bus (kW)	0.273	5.865	10.030	8.412	5.356

Table 6.3: Power Injection for Sinusoidal Shunt Perturbation, Specified Signal

Notice that in all cases, there's a slight frequency distortion. At higher frequencies, this is less than 1% in all cases, and can be attributed to rounding error in the digital signal processor. At .1Hz, however, the error is much greater, on the order of 20%. At this low frequency, the IQ math parameters would need to be changed to more accurately inject a specified frequency. The present error doesn't prevent sinusoidal FRF, however.

As long as the actual frequency injected is known, the output can be tracked properly, and a point determined on the FRF plot. This point won't be exactly at the desired frequency, but will be close; in this case, instead of at .1Hz, identification at .0826Hz can be performed.

6.c Shunt Pulse

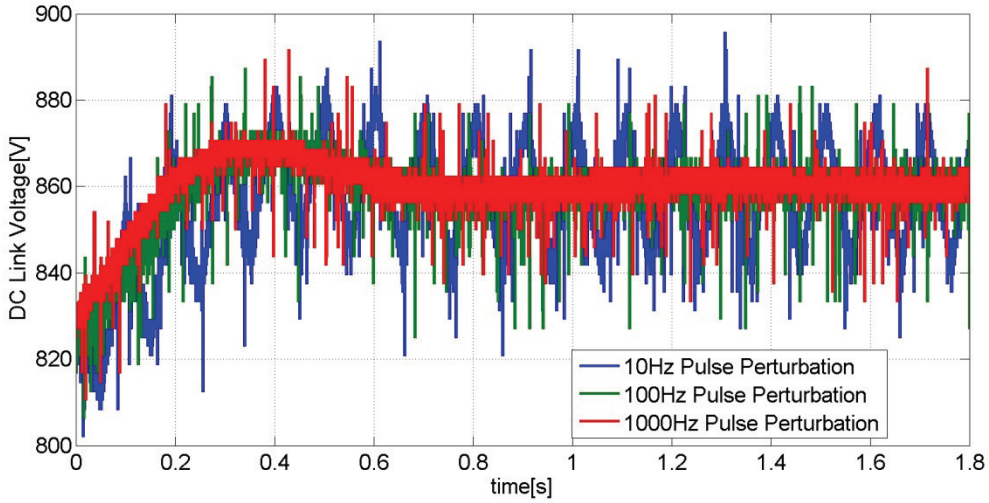

Figure 6.43: DC Link Behavior under 1Hz, 10 and 1kHz Shunt Pulse Perturbations

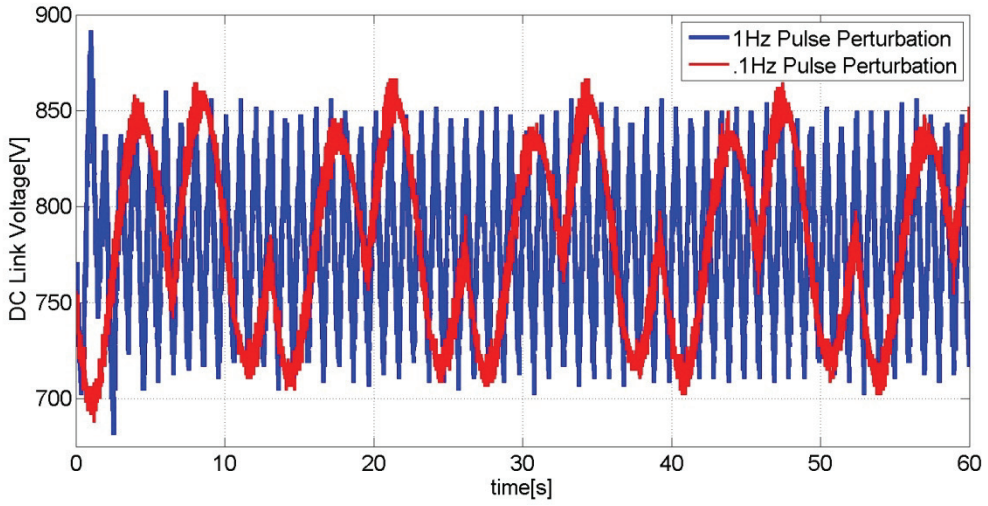

Figure 6.44: DC Link Behavior under .1Hz and 1Hz Shunt Pulse Perturbations

Figures 6.41 and 6.42 show DC link behaviors similar to those shown in figures 6.25 and 6.26, the DC link behavior of the system under sinusoidal perturbations. For all except .1Hz, the only difference is that the waveform here is triangular, while the waveform for sinusoidal perturbation is sinusoidal. This is to be expected given the integrals of the perturbation waveforms. At .1 Hz, the waveform is significantly different; the system is struggling to maintain a DC voltage given the extremely slow speed of perturbation. However, a .1Hz (or near .1Hz) square wave can be seen to be a portion of the DC link waveform. Once again, the DC link controller proportional gain had to be decreased to maintain this signal. This time, it was decreased to .02.

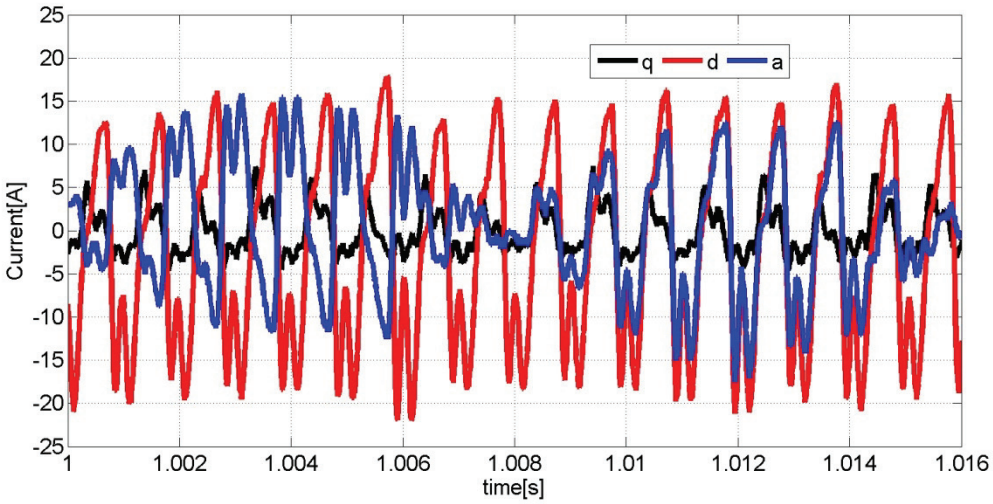

Figure 6.45: 1000Hz Shunt Pulse Perturbation Phase A, d, and q Currents

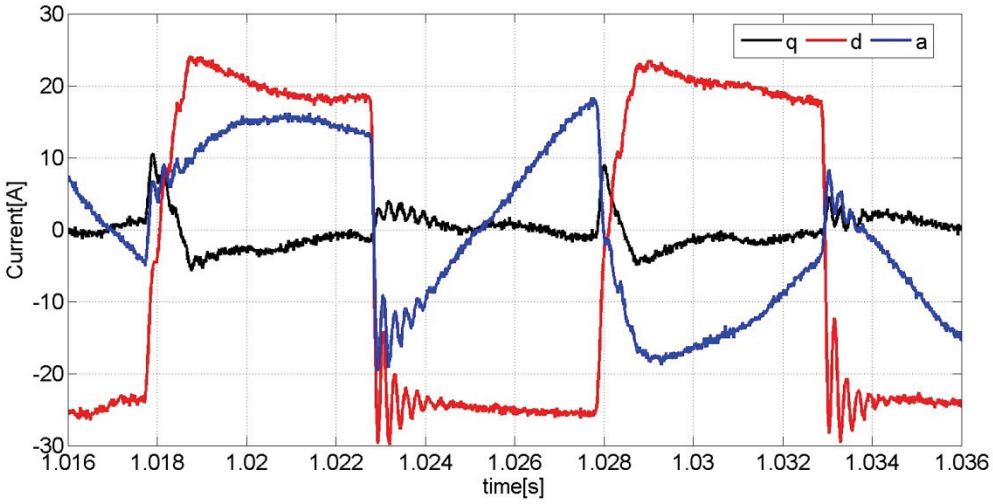

Figure 6.46: 100Hz Shunt Pulse Perturbation Phase A, d, and q Currents

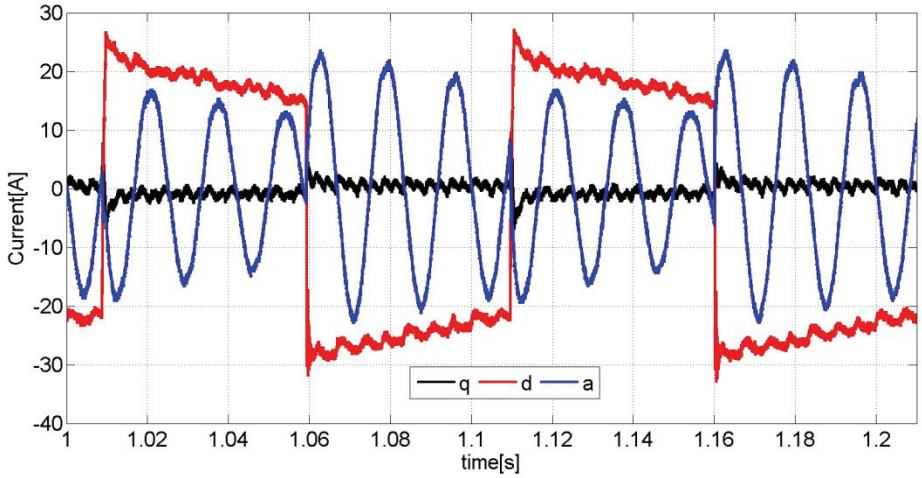

Figure 6.47: 10Hz Shunt Pulse Perturbation Phase A, d, and q Currents

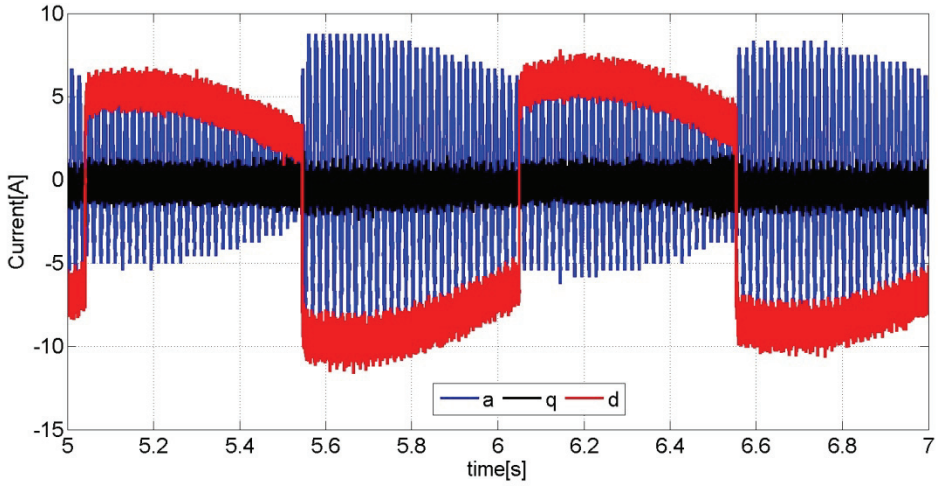

Figure 6.48: 1Hz Shunt Pulse Perturbation Phase A, d, and q Currents

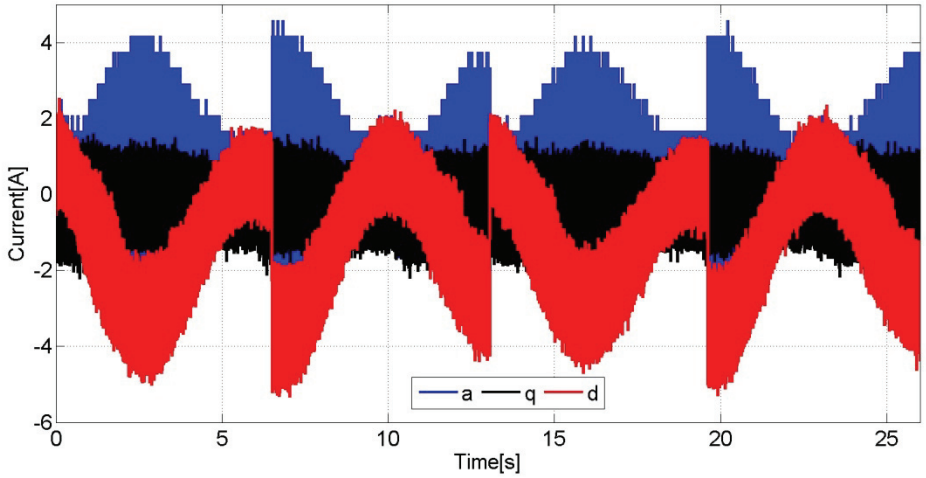

Figure 6.49: .1Hz Shunt Pulse Perturbation Phase A, d, and q Currents

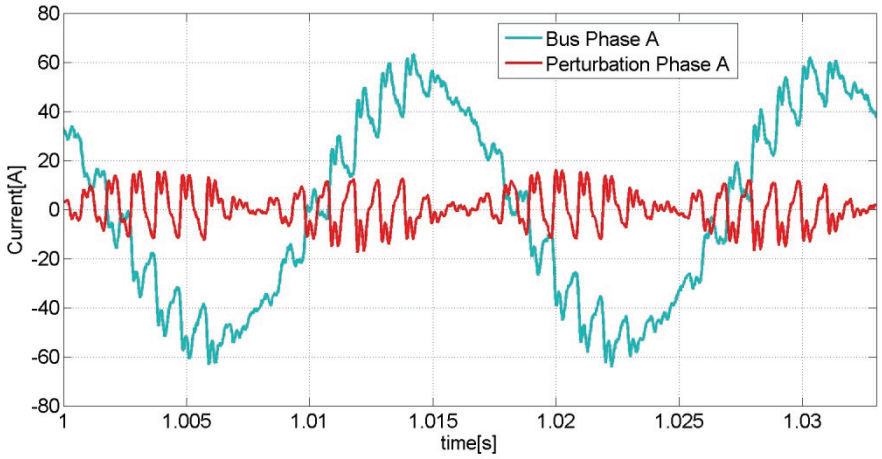

Figure 6.50: 1000Hz Shunt Pulse Perturbation Phase A and Bus Phase A Currents

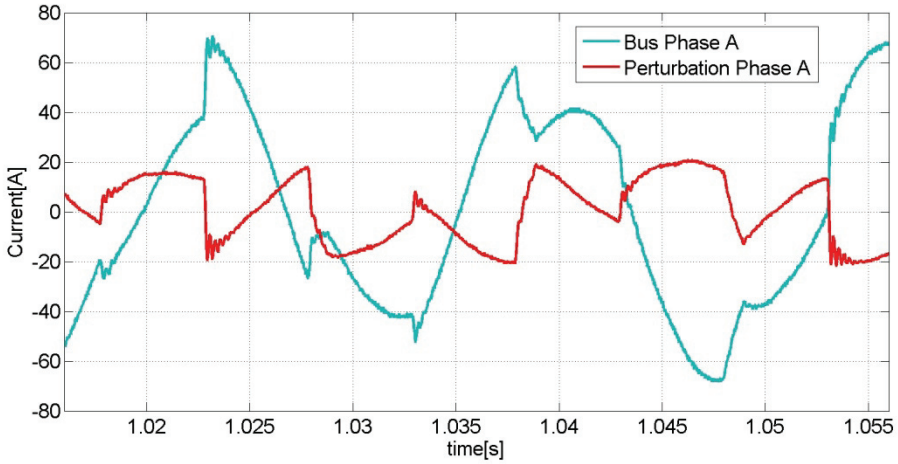

Figure 6.51: 100Hz Shunt Pulse Perturbation Phase A and Bus Phase A Currents

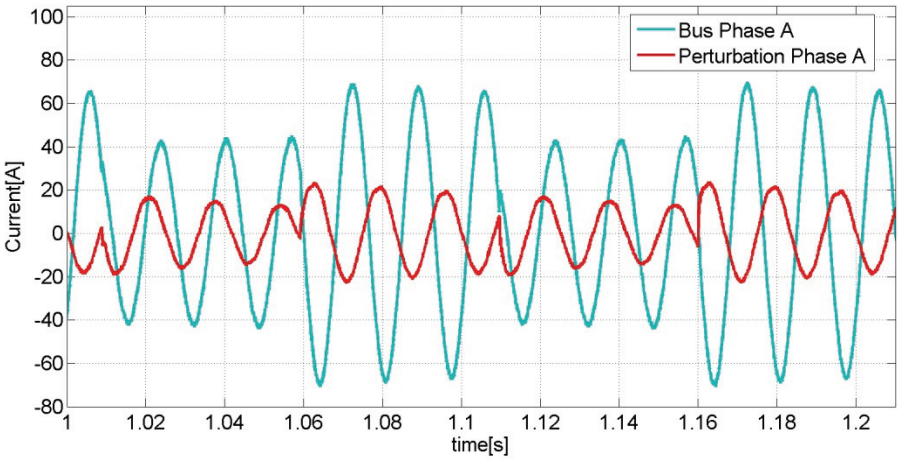

Figure 6.52: 10Hz Shunt Pulse Perturbation Phase A and Bus Phase A Currents

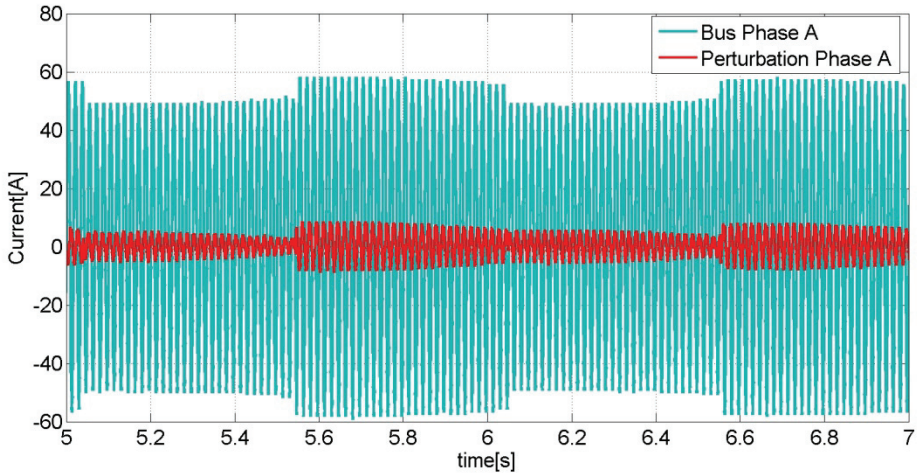

Figure 6.53: 1Hz Shunt Pulse Perturbation Phase A and Bus Phase A Currents

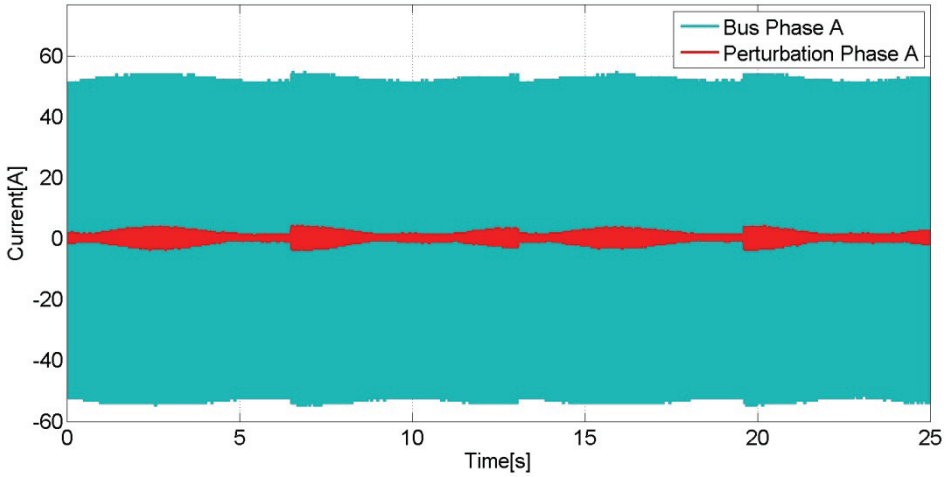

Figure 6.54: .1Hz Shunt Pulse Perturbation Phase A and Bus Phase A Currents

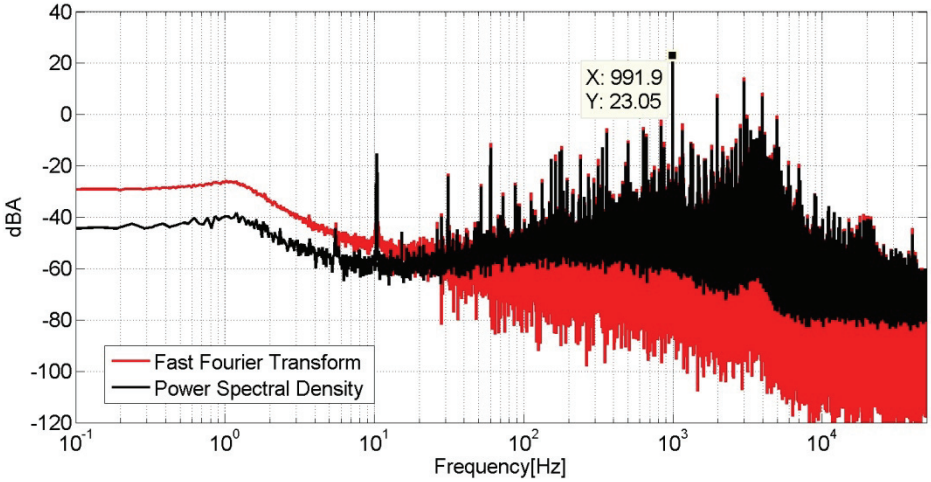

Figure 6.55: 1000Hz Shunt Pulse Perturbation d-q Domain FFT and PSD

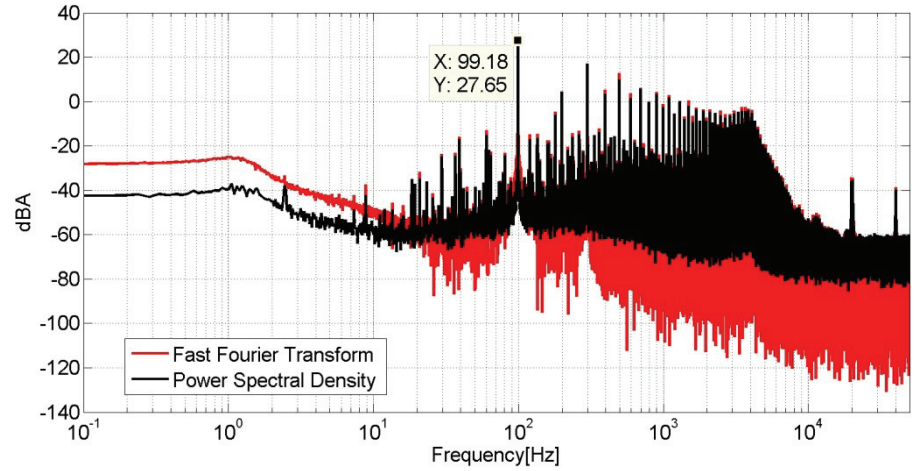

Figure 6.56: 100Hz Shunt Pulse Perturbation d-q Domain FFT and PSD

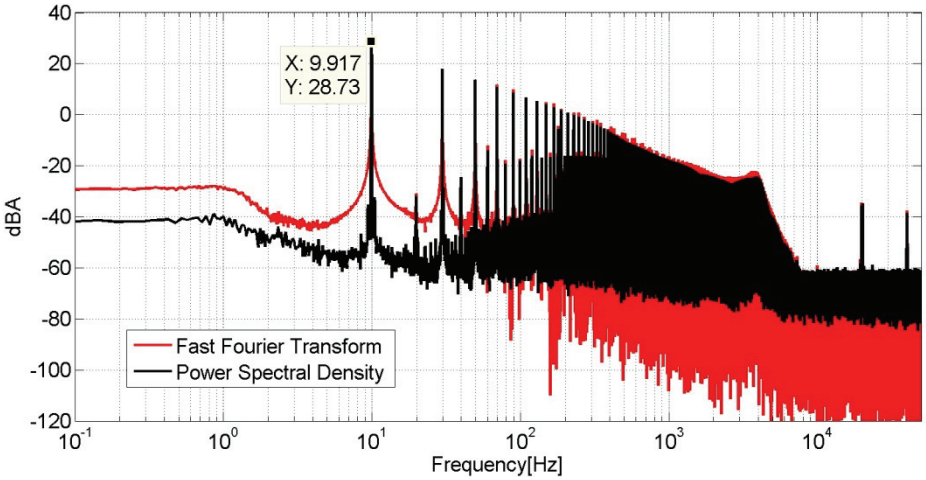

Figure 6.57: 10Hz Shunt Pulse Perturbation d-q Domain FFT and PSD

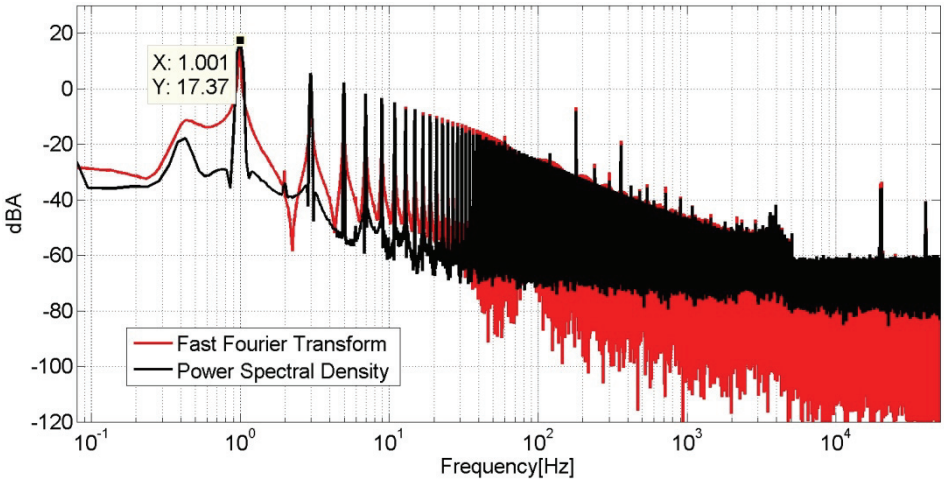

Figure 6.58: 1Hz Shunt Pulse Perturbation d-q Domain FFT and PSD

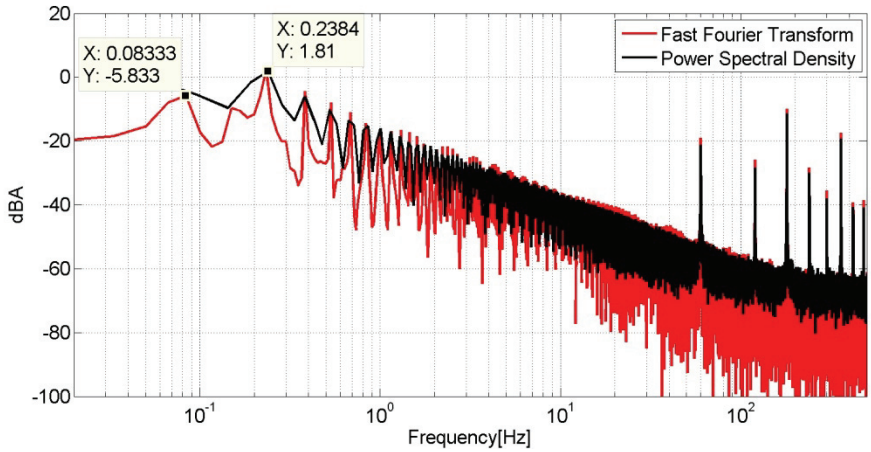

Figure 6.59: .1Hz Shunt Pulse Perturbation d-q Domain FFT and PSD

Figures 6.44-6.58 show the results of the shunt pulse perturbations at .1, 1, 10, 100, and 1000Hz. Although the time domain waveforms are drastically different from those of the sinusoidal perturbations, the frequency domain behavior is similar, although the harmonics are more pronounced. The resulting perturbation currents and relative powers from these experiments are shown below.

	.1Hz	1Hz	10Hz	100Hz	1000Hz
Current (A RMS) per Phase	1.115	4.063	12.727	12.737	7.012
% of nominal 460V, 100kW Bus Phase Current	0.890	3.242	10.156	10.164	5.596
Power on a 460V, 100kW Bus (kW)	0.890	3.242	10.156	10.164	5.596

Table 6.4: Power Injection for Shunt Pulse Perturbation, Total Signal

	.1Hz	1Hz	10Hz	100Hz	1000Hz
Current (A RMS) per Phase	0.209	3.016	11.15	9.84	5.57
% of nominal 460V, 100kW Bus Phase Current	0.167	2.407	8.898	7.852	4.445
Power on a 460V, 100kW Bus (kW)	0.167	2.407	8.898	7.852	4.445

Table 6.5: Power Injection for Shunt Pulse Perturbation, Specified Signal

6.d Bonus Signal- Shunt Square Chirp

While not required by the design specifications, an easily made and interesting signal is the varying frequency square wave signal. This signal is essentially a combination of the pulse and chirp signals. Figures 6.58 to 6.70 show the results of implementing a square chirp perturbation in shunt and compare the effects to those of a shunt sinusoidal chirp perturbation.

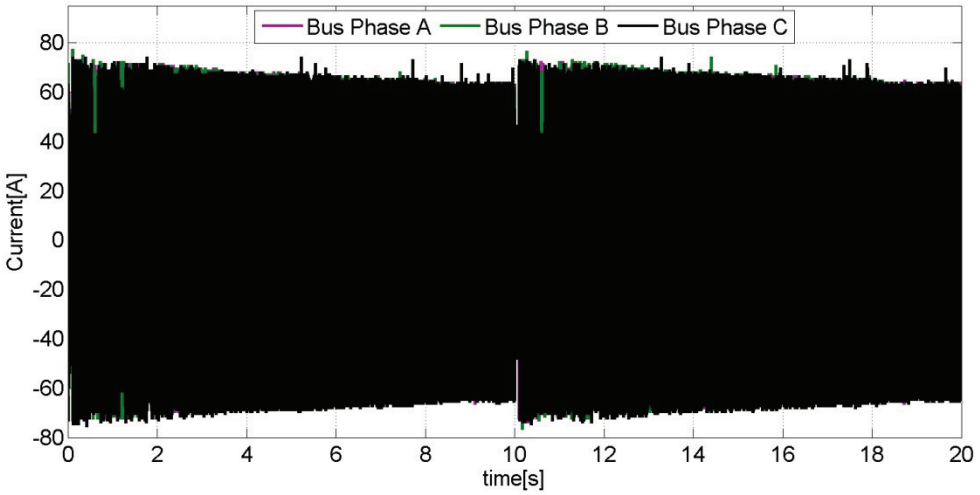

Figure 6.60: Two 10 second Shunt Square Chirps from 0-1000Hz, Bus Currents

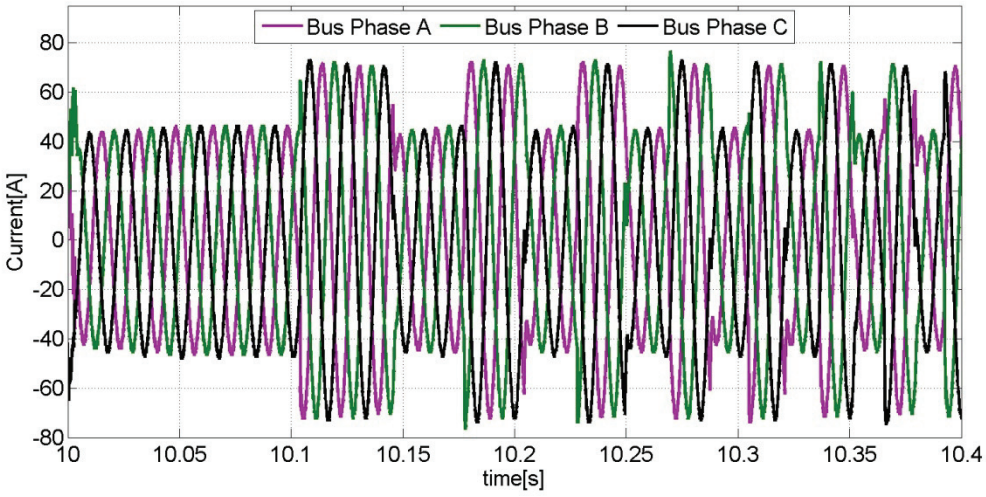

Figure 6.61: Low Frequency Shunt Square Chirp Detail, Bus Currents

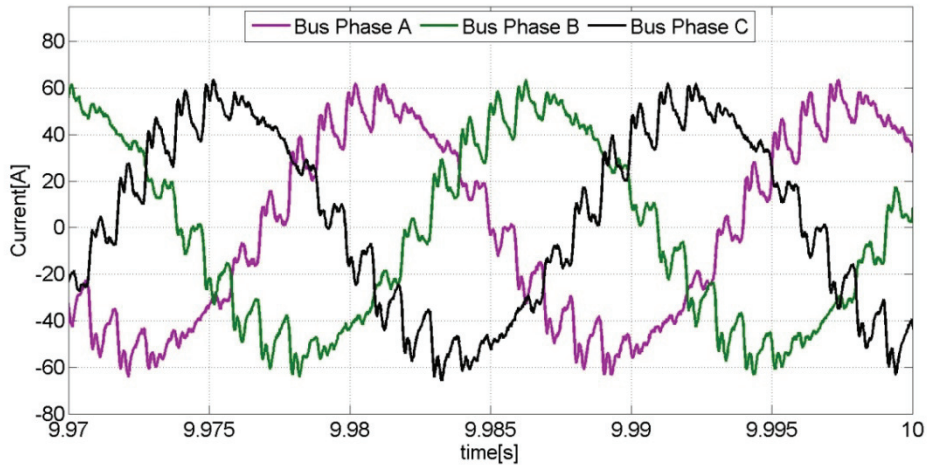

Figure 6.62: High Frequency Shunt Square Chirp Detail, Bus Currents

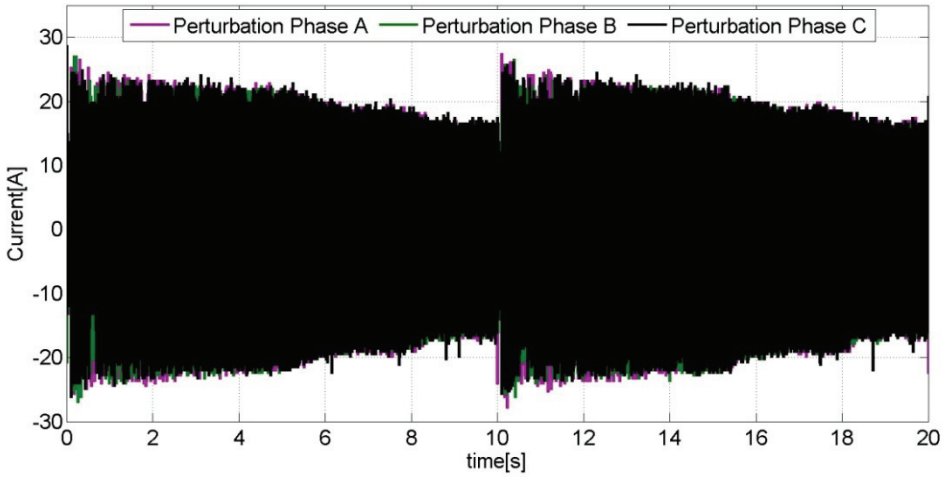

Figure 6.63: Two 10 second Shunt Square Chirps, Perturbation Currents

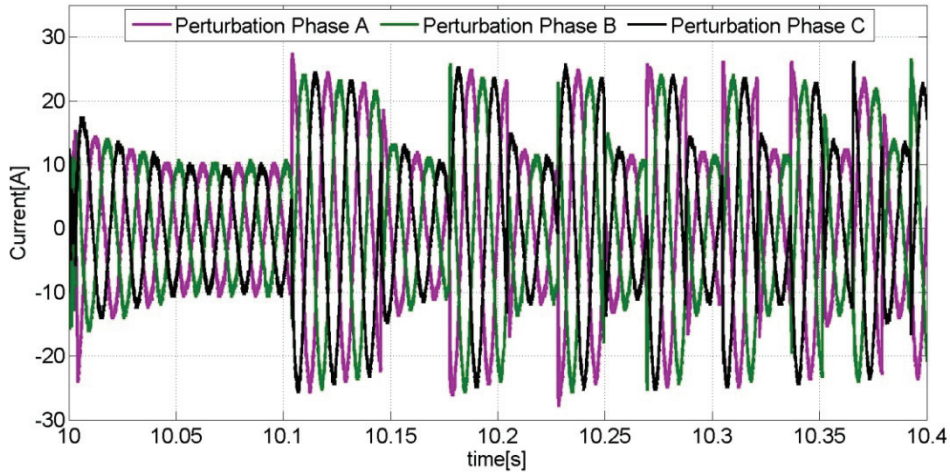

Figure 6.64: Low Frequency Shunt Square Chirp Detail, Perturbation Currents

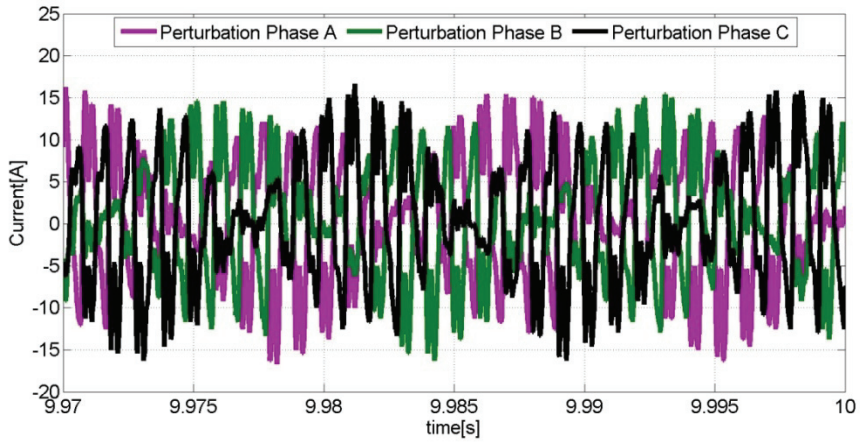

Figure 6.65: High Frequency Shunt Square Chirp Detail, Phase Currents

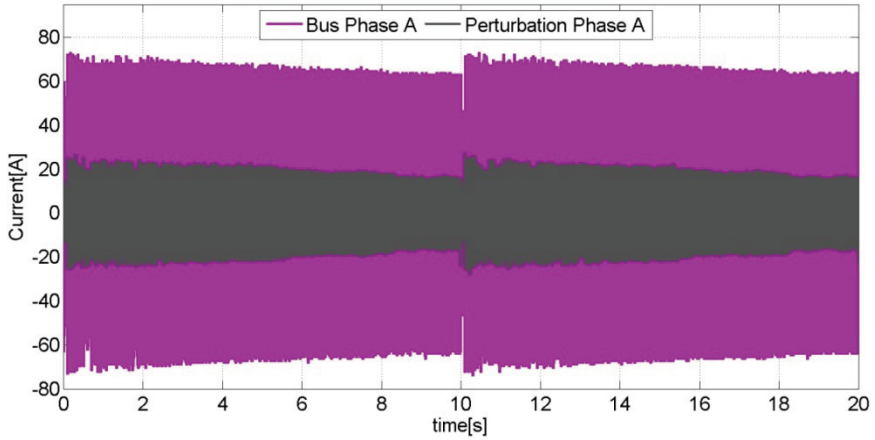

Figure 6.66: Two 10 second Shunt Square Chirps from 0-1000Hz, Perturbation and Bus Phase A Currents

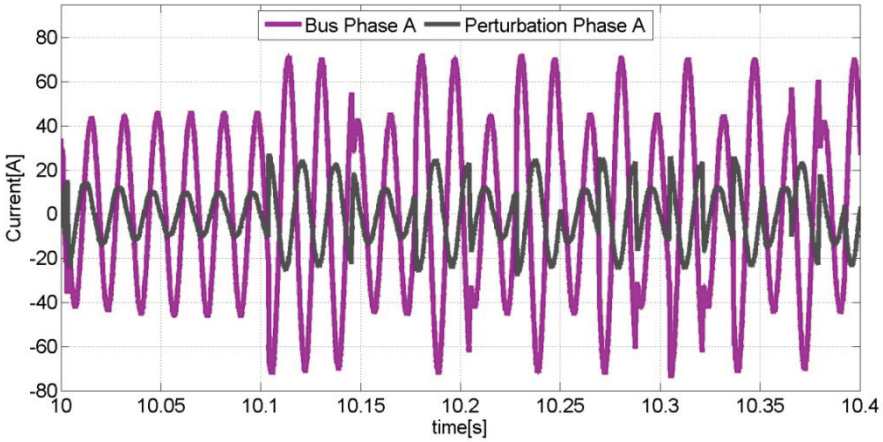

Figure 6.67: Low Frequency d Shunt Square Chirp Detail, Perturbation and Bus Phase A Currents

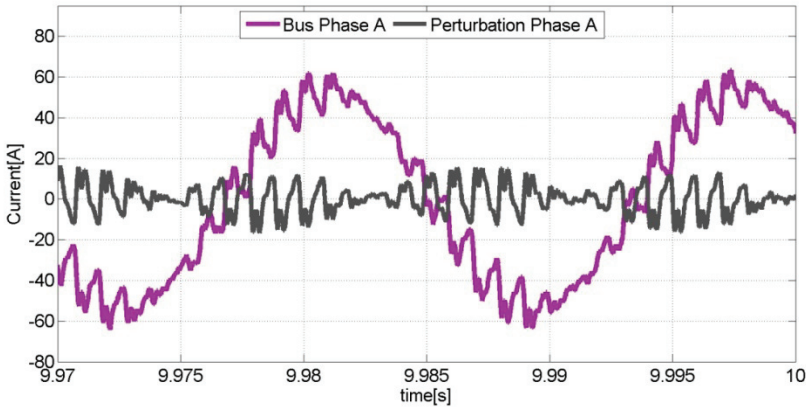

Figure 6.68: High Frequency Shunt Square Chirp Detail, Perturbation and Bus Phase A Currents

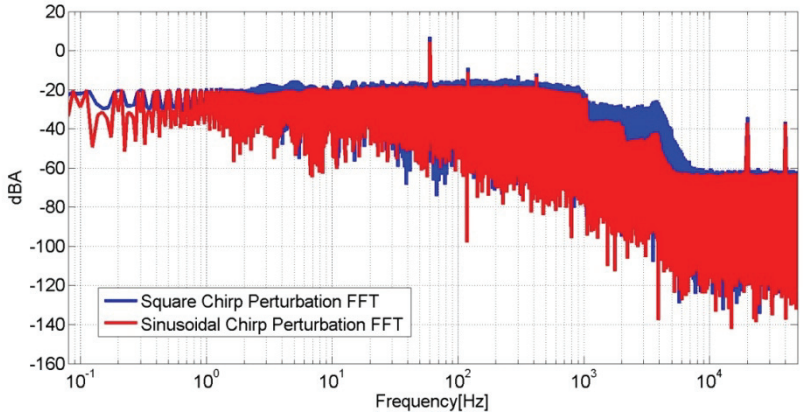

Figure 6.69: Phase A Perturbation FFT as a Result of a Shunt Chirp and a Shunt Square Chirp

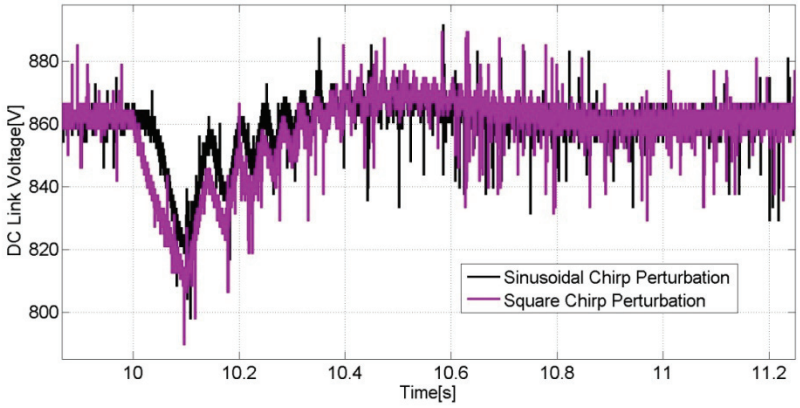

Figure 6.70: DC Link Voltage as a Result of the Shunt Chirp and Shunt Square Chirp Perturbations

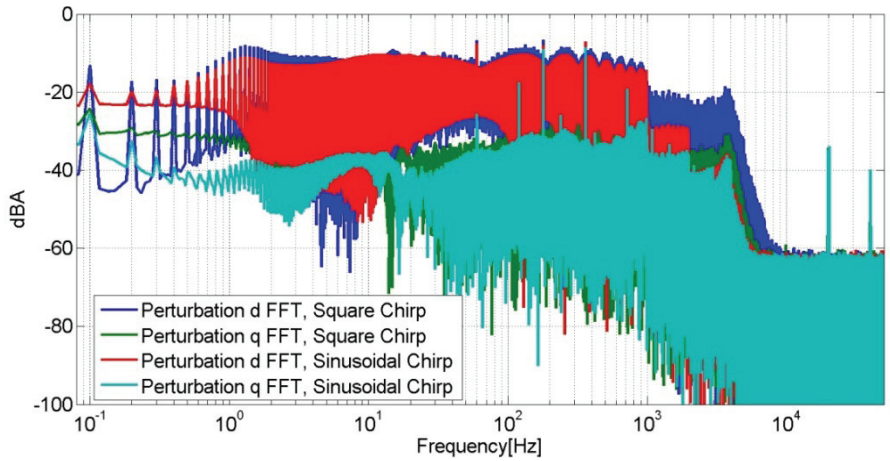

Figure 6.71 d and q Perturbation Current Fast Fourier Transforms as a Result of Shunt Chirp and Shunt Square Chirp Perturbations

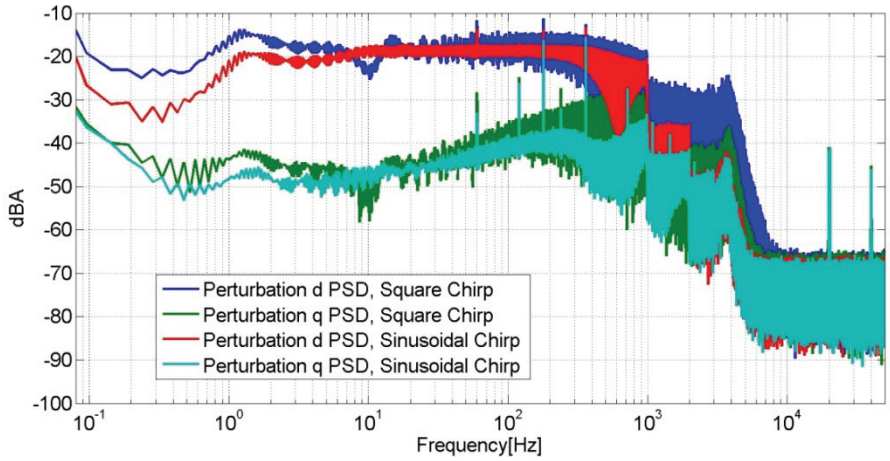

Figure 6.72 d and q Perturbation Current Power Spectral Densities as a Result of Shunt Chirp and Shunt Square Chirp Perturbations

	Square Chirp	Sine Chirp
Current (A RMS) per Phase	10.293	10.619
% of 125.3A (nominal 460V, 100kW Bus Phase Current)	8.234	8.495
Power on a 460V, 100kW Bus (kW)	8.234	8.495

Table 6.6: Achieved Perturbation Power, Square and Sinusoidal Chirp in Shunt

Although the overall power of injection is nearly the same for both signals, it seems that the square chirp signal will produce a greater portion of that power at lower frequencies than will the sinusoidal chirp signal.

6.e Series

The vast majority of what is true for shunt injection is also true for series injection; the lower frequencies will be limited in the exact same way by the DC link capacitance, and the higher frequencies will be limited by the power stage inductance. In fact, series injection will perform slightly better at higher frequencies, as the inductance of the power stage in series is slightly less. There are only two complications that series injection adds; the first involves voltage limitation across the transformer primary windings, and the second involves saturation of the transformers at low frequencies.

The EMI filter is rated at 480 V line-to-line. This translates to 391 V peak line-to-neutral voltage. The bus under test maximum voltage is 460 V line-to-line, which translates to 376 V peak line-to-neutral. To perturb the system to 10%, 37.6 V peak must be present on the secondary side of the transformers, and 376 V on the primary side. This is within the specifications of the EMI filter, and the system can indeed inject 10kW on a 460V, 100kW bus. However, such a perturbation is very short lived; without a DC link charging scheme such as that described in the control section, the losses in the circuit cause the DC link voltage to drop quickly. To charge the DC link, approximately 70V is required. The overvoltage protection must be set at 391V, so this only leaves 321V for perturbation. Practically, some margin for noise and variation must be left, and 300V of perturbation is the greatest achievable. Applying 300V on the transformer primary (producing 30V on the secondary) results in a 7.9% perturbation, or 7.9kW on a 100kW bus. This is still within the original specification, although less than is achievable in shunt.

To fully characterize the system, the only limitation left to explore is that of the transformer saturation. As described in the "Arbitrary Waveforms in d-q" section, a single frequency in d-q translates to two frequencies in the abc domain, one at the perturbation frequency plus the rotational frequency and one at the perturbation frequency minus the rotational frequency. In the case here, the rotation frequency is 60Hz. Therefore, perturbation frequencies near 60Hz in d-q will result in a component near zero in abc. Figure 6.73 illustrates this phenomenon.

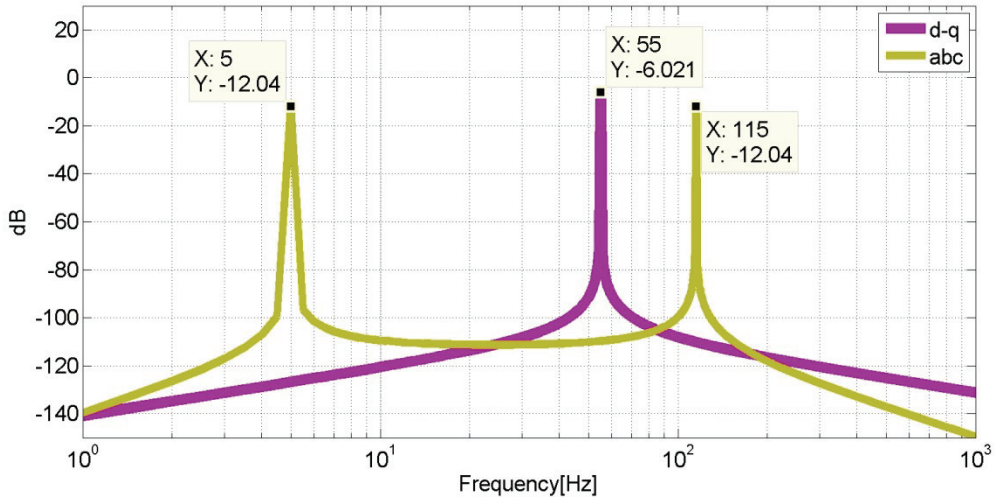

Figure 6.73: Low Frequency abc Component of d-q Frequencies Close to Rotational Frequency

Being that transformers operate in the abc domain, this can result in saturation of the transformers when a frequency near 60Hz is injected. Therefore, a frequency band centered around 60Hz in the d-q domain will be unavailable to identification by series injection.

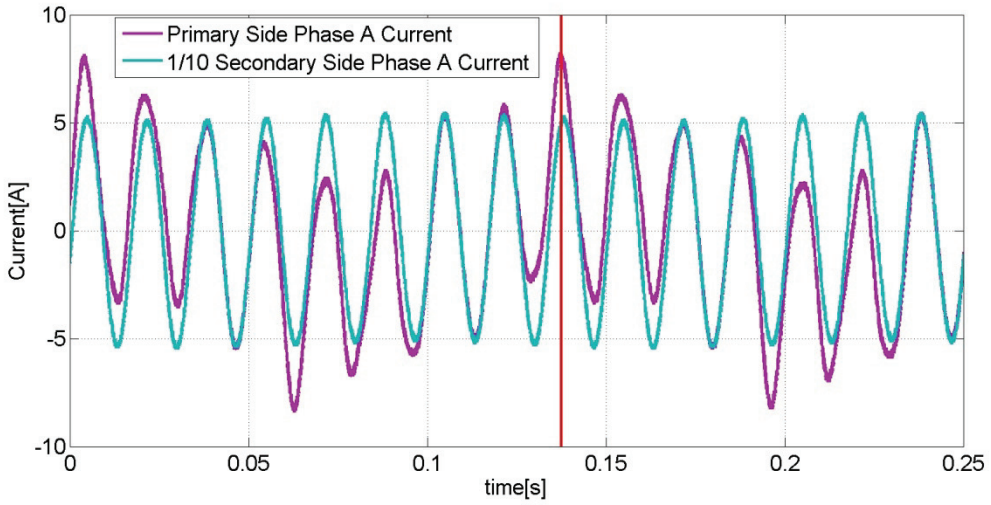

Figure 6.74: 300V Series Injection at 68Hz in the d-q Domain, Primary Phase A and 1/n Times Secondary Phase A Currents

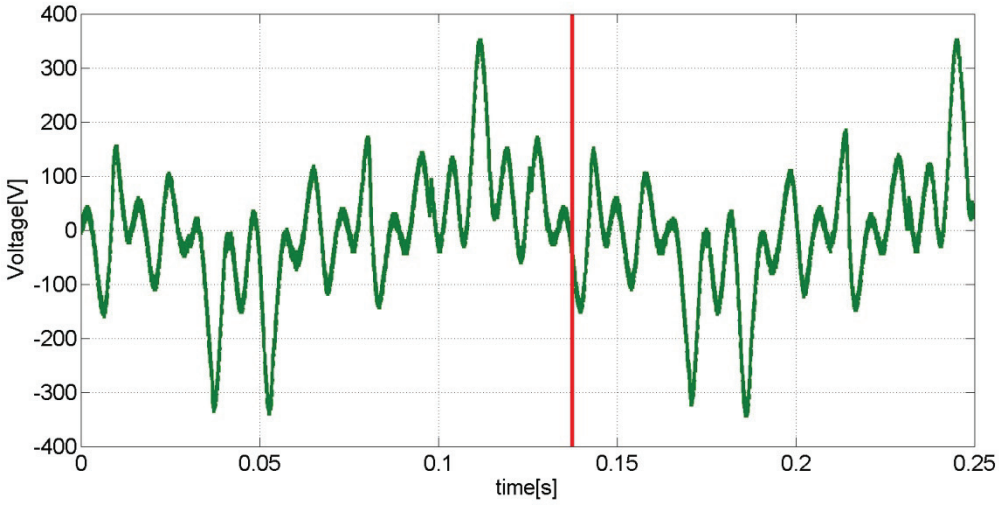

Figure 6.75: Primary Side Voltage Resulting in the Currents in Figure 6.74

Figures 6.74 and 6.75 show pronounced saturation. The two currents in figure 6.75 should be identical, but the primary side current shows significant deviation from what it should be. At the peak of this deviation (shown by the red line), it can be seen in figure 6.75 that the low frequency component of the primary side voltage is approximately zero. When the low frequency component of the primary side voltage is zero, the integral of the primary side voltage (the "volt-seconds") is greatest. The greatest saturation effect is expected to occur when the "volt-seconds" applied to the primary side is greatest, verifying that the phenomenon captured in figure 6.76 is indeed saturation. By lowering the voltage applied to the primary side of the transformers or increasing the frequency of that voltage, the transformer can be brought back out of saturation.

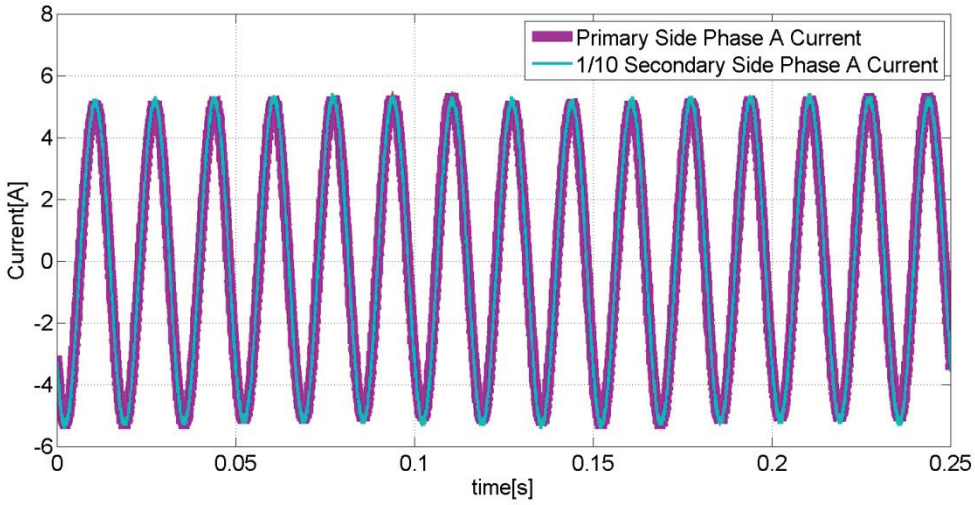

Figure 6.76: 160V Series Injection at 68Hz in the d-q Domain, Primary Phase A and 1/n Times Secondary Phase A Currents

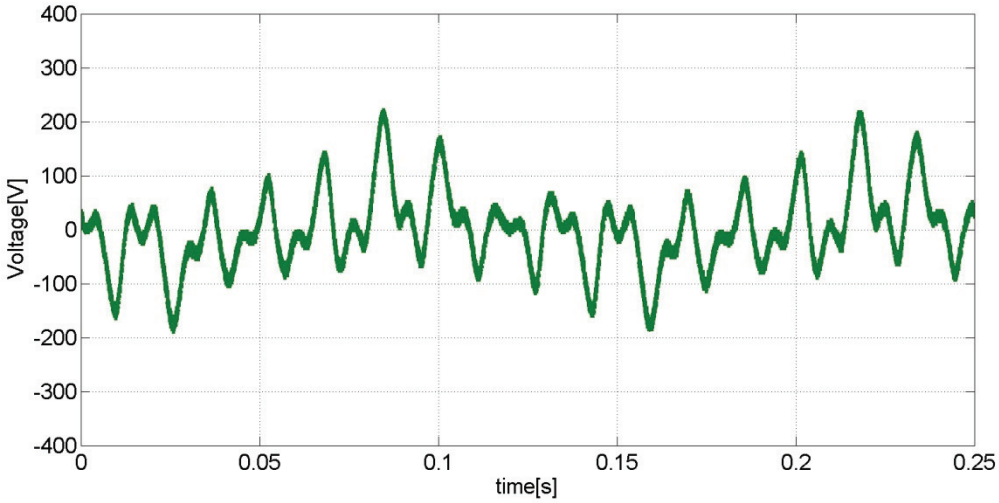

Figure 6.77: Primary Side Voltage Resulting in the Currents in Figure 6.76

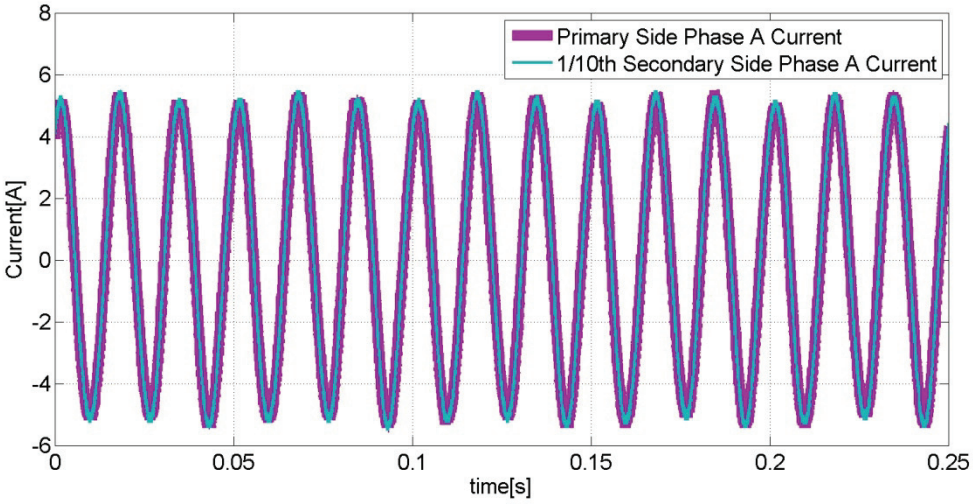

Figure 6.78: 300V Series Injection at 80Hz in the d-q Domain, Primary Phase A and 1/n Times Secondary Phase A Currents

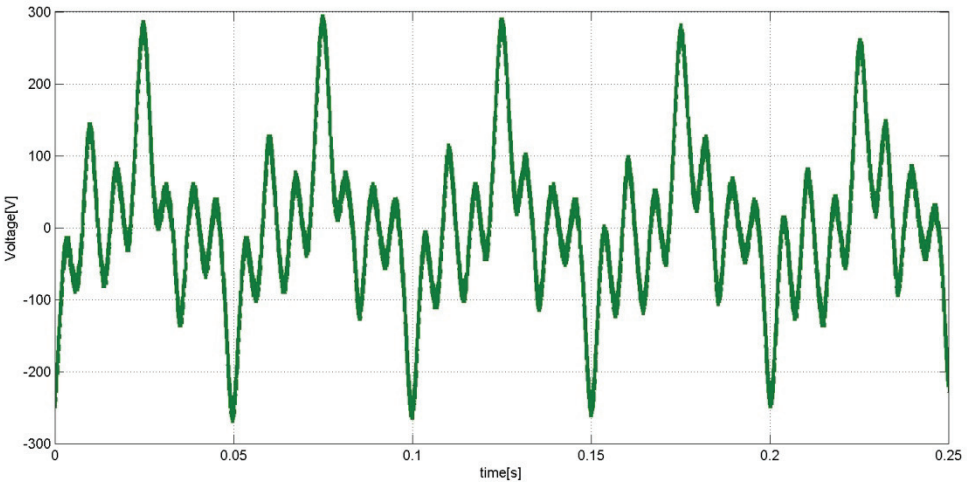

Figure 6.79: Primary Side Voltage Resulting in the Currents in Figure 6.78

Figures 6.76 and 6.77 show the results of decreasing the applied voltage until saturation stops, and figures 6.78 and 6.79 show the results of increasing the frequency until saturation stops. If the frequency is lowered below 80Hz, less pronounced, but still visible, saturation occurs.

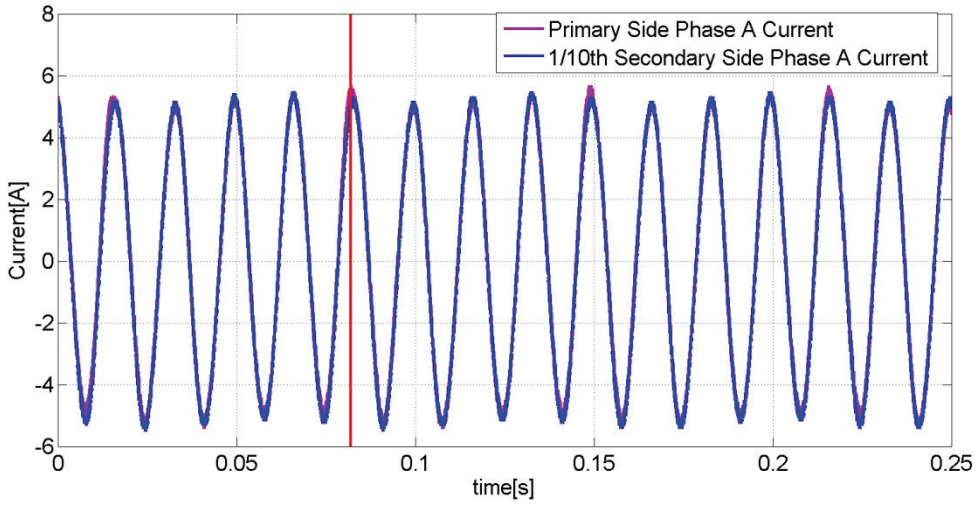

Figure 6.80: 300V Series Injection at 78Hz in the d-q Domain, Primary Phase A and 1/n Times Secondary Phase A Currents

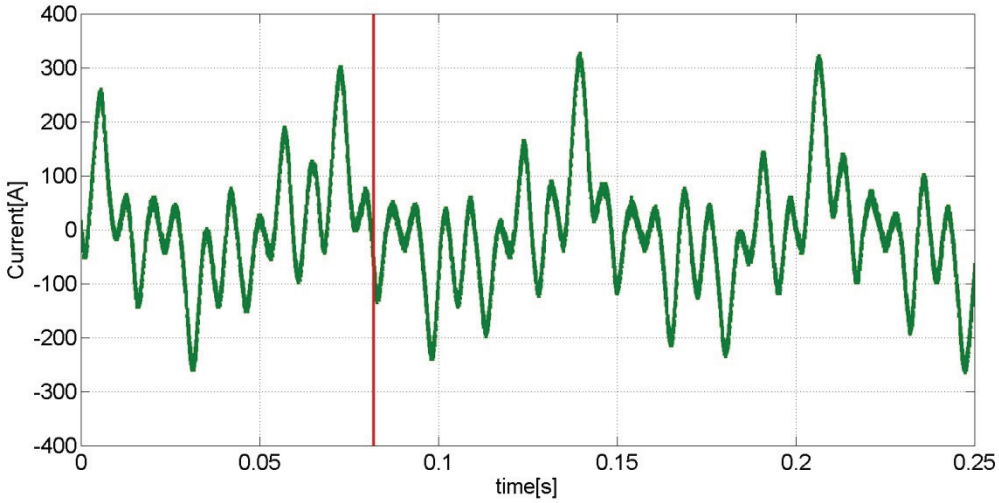

Figure 6.81: Primary Side Voltage Resulting in the Currents in Figure 6.80

Being that any d-q frequency near 60Hz will result in a low frequency component in abc and that only frequencies above 60Hz have been shown so far, the results of testing the frequencies symmetric from those shown above across 60Hz are shown below.

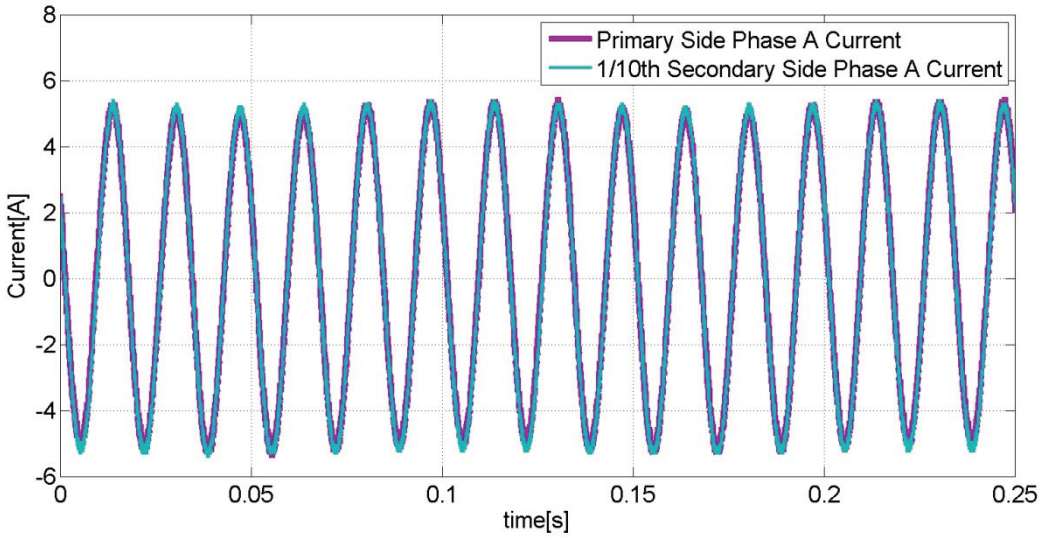

Figure 6.82: 160V Series Injection at 52Hz in the d-q Domain, Primary Phase A and 1/n Times Secondary Phase A Currents

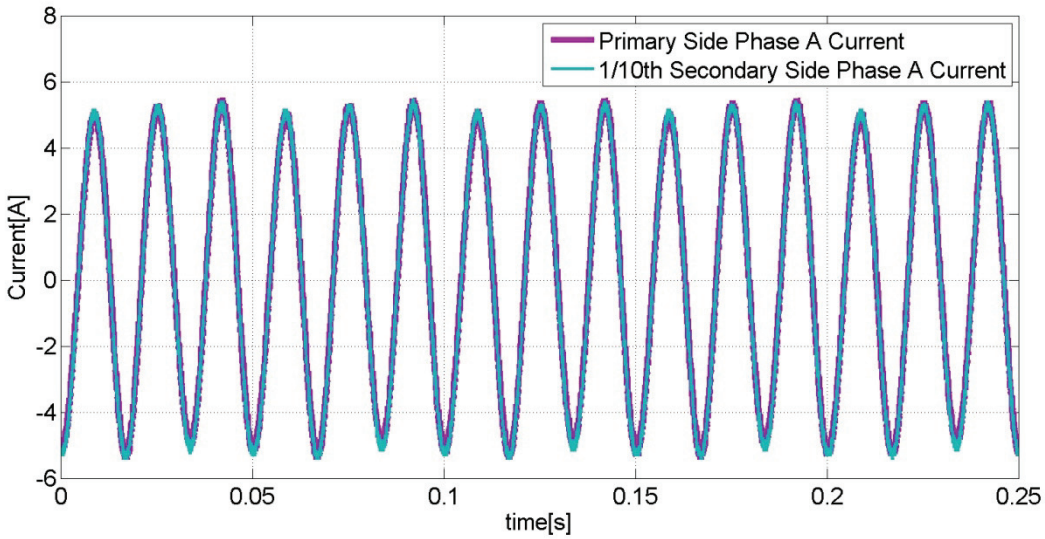

Figure 6.83: 300V Series Injection at 40Hz in the d-q Domain, Primary Phase A and 1/n Times Secondary Phase A Currents

These results can be easily evaluated by plotting perturbation voltage possible as a function of frequency.

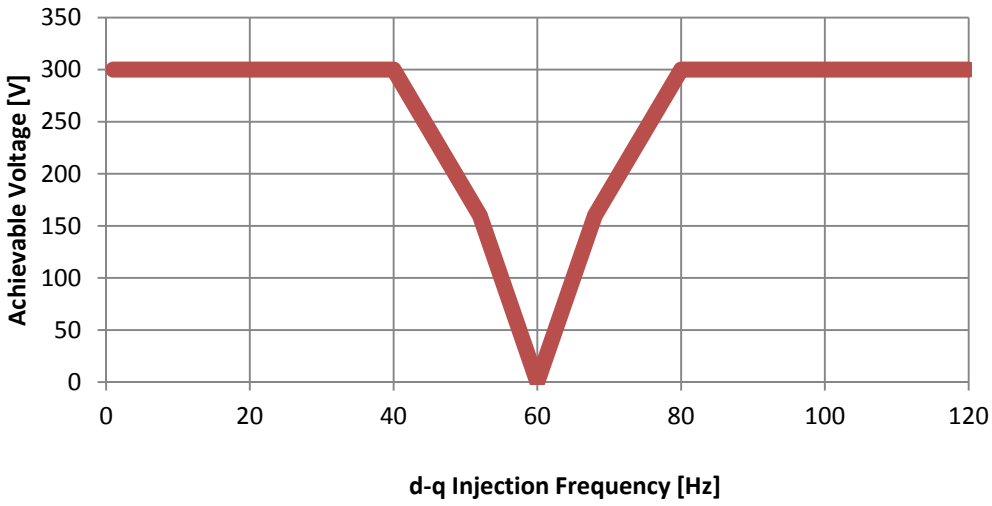

Figure 8.84: Perturbation Voltage Possible as a Function of Frequency

Given this information, the last of the limits on perturbation power, both in series and in shunt, is known. Figure 8.85 graphically describes these limits.

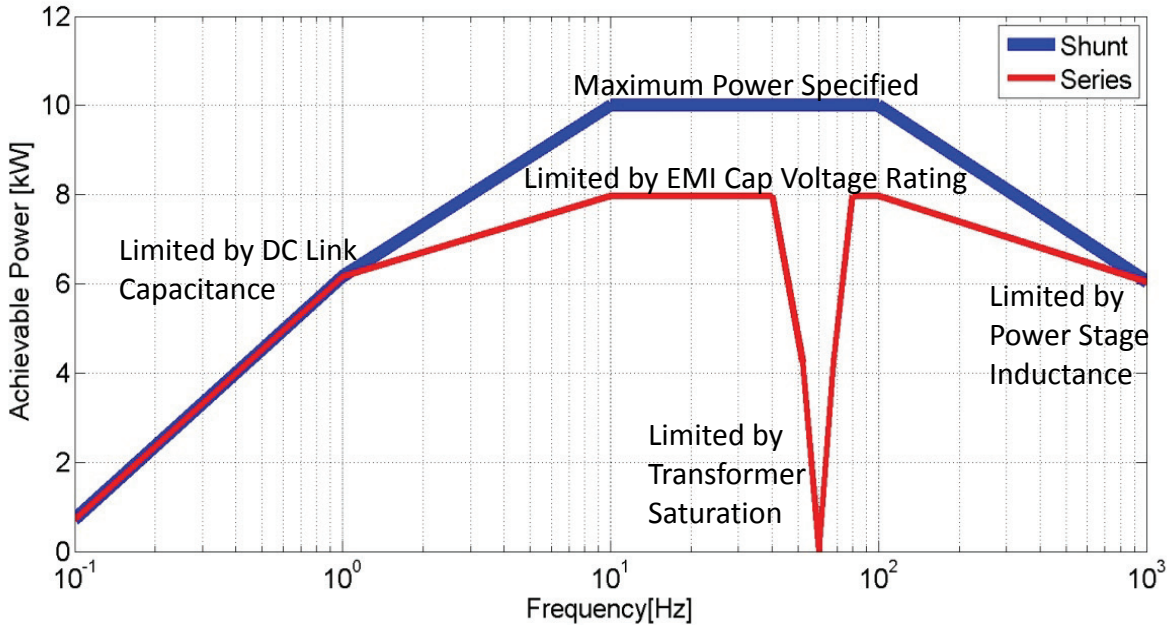

Figure 8.85: Achievable Perturbation Power as a Function of Frequency

7. Conclusions and Future Work

Given the rapidly advancing sophistication of controls in three-phase power systems, as well as the desire to disconnect such power systems from utility grid power and all associated stability-related benefits, measurement of stability margins of three-phase power becomes desirable. To date, there are no commercially available devices that can do this. There are two portions to a device capable of measuring the impedances necessary to calculate stability margins. One portion injects a perturbation into the system under test, and the other portion measures the system's response. In this thesis, the design and test of the perturbation injection unit (PIU) is explored. Both series and shunt injection orientations are explored.

For different systems, a different level of power is necessary to measure the impedances necessary for stability margin calculation, although to date, it is unknown what levels of power yield good results. The PIU described here is designed for a 460V, 100kW bus, and is capable of a maximum injection power of 10kW on such a bus. At various frequencies, there are various limitations on injection power, and the achievable power for the frequency range between .1 Hz and 1000Hz is shown in figure 8.85 of this thesis.

Table 1.1 describes the goals of this thesis. As shown in the results section, all goals were met with the exception of perturbation at .1Hz and 1kW; only .72kW was achievable, and of that only .27kW was at the desired frequency. This is due to the DC link capacitance; without much more capacitance, the 1kW mark will not be achievable. However, with a DC supply, this value is easily achieved; 10kW is possible with such a supply. Again however, this may not be necessary; there are signals presented and examined in this thesis with spectral content at .1Hz that may be used to determine impedances at this frequency through batch processing by FFT or CPSD.

Several lessons about construction of a PIU for stability analysis can be learned from the design presented in this thesis. First, a low DC link voltage can limit maximum injection power at higher frequencies. Second, aligning the PLL to be at a 45 degree angle from the bus voltage active power direction produces d and q channels that both have the same effect with regard to active power and both have an injectable power equal to 1.41 times the maximum power injectable in the active power direction across the

power stage impedance. Third, injection can be performed using only power from the system under test, but doing so limits the injectable power at lower frequencies.

The most obvious next step is to integrate this system with one capable of measuring bus currents and voltages and then calculating impedances. In fact, this is already completed, but the results of such a marriage are outside the scope of this thesis. Many uncompleted next steps involve the algorithms used to determine impedances from the measurements. Cross-power spectral density methods of frequency response function (FRF) estimation are mentioned here but not fully explained, and have many parameters that can be modified to obtain better results given a batch set of voltage and current data. After an FRF is estimated, a numerical transfer function can be stochastically fit, allowing for much easier further analysis. An entire branch of signal processing theory is dedicated to this called "System Identification."

Another possibility involving only the PIU portion is to perform perturbations inductively, negating the necessity to turn off the bus, break the bus, connect the bus wires to the impedance analyzer, and then turn the bus back on. Such a device would involve only magnetic couplers that clamp onto the bus wires. Lastly to be mentioned here, a PIU could theoretically be used to impose a controllable impedance on the system under test. If this is possible, then an impedance measurement device could theoretically become a stability maintenance device that adaptively changes the bus characteristics to maintain specified stability margins. In other words, the Impedance Obtaining Equipment would become Adaptive and Inductive Impedance Correction Equipment.

Appendix A. Derivation of Integral and Proportional Gains for Use in Texas Instruments' PID Control Algorithm from the Canonical Digital Domain Difference Equation

TI's PID implementation is shown below for comparison to the canonical digital domain difference equation

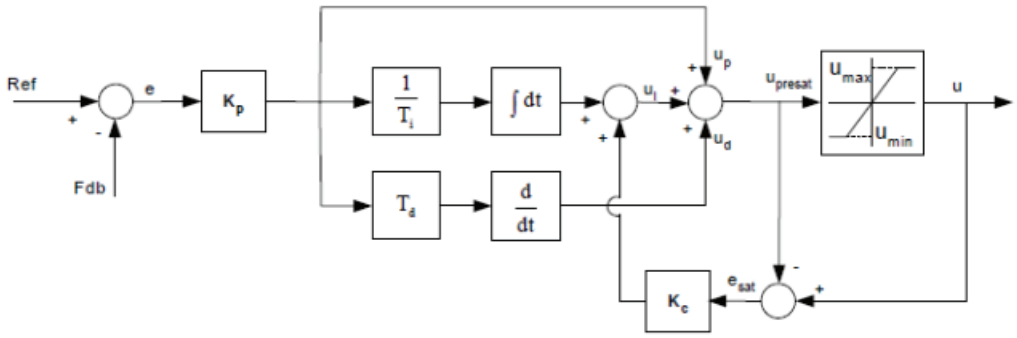

Figure 1: Block diagram of PID controller with anti-windup

The differential equation for PID controller with anti-windup before saturation is described in the following equation [1].

$$u_{presat}(t) = u_p(t) + u_i(t) + u_d(t) \quad (1)$$

Each term can be expressed as follows:

Proportional term: $$u_p(t) = K_p e(t) \quad (2)$$

Integral term with saturation correction:

$$u_i(t) = \frac{K_p}{T_i}\int_0^t e(\varsigma)d\varsigma + K_c\left(u(t) - u_{presat}(t)\right) \quad (3)$$

Derivative term: $$u_d(t) = K_p T_d \frac{de(t)}{dt} \quad (4)$$

where

- u(t) is the output of PID controller
- $u_{presat}(t)$ is the output before saturation
- e(t) is the error between the reference and feedback variables
- K_p is the proportional gain of PID controller
- T_i is the integral time (or reset time) of PID controller
- T_d is the derivative time of PID controller
- K_c is the integral correction gain of PID controller

Equations (1)-(4) can be discretized using backward approximation as follows:

Pre-saturated output:

$$u_{presat}(k) = u_p(k) + u_i(k) + u_d(k) \quad (5)$$

Proportional term:

$$u_p(k) = K_p e(k) \quad (6)$$

Integral term with saturation correction:

$$u_i(k) = u_i(k-1) + K_p \frac{T}{T_i} e(k) + K_c \left(u(k) - u_{presat}(k)\right) \quad (7)$$

Derivative term:

$$u_d(k) = K_p \frac{T_d}{T} \left(e(k) - e(k-1)\right) \quad (8)$$

Defining $K_i = \frac{T}{T_i}$, and $K_d = \frac{T_d}{T}$, then integral with saturation correction and derivative terms finally become

$$u_i(k) = u_i(k-1) + K_i u_p(k) + K_c \left(u(k) - u_{presat}(k)\right) \quad (9)$$

$$u_d(k) = K_d \left(u_p(k) - u_p(k-1)\right) \quad (10)$$

where T is sampling period (sec).

Figure A.1: TI's PID Controller Architecture and Equations as Copied Directly from Reference [16]

This diagram and set of equations bear little resemblance to the canonical form of the difference equation and the widely used Direct Form 2 Realization of the IIR [19]

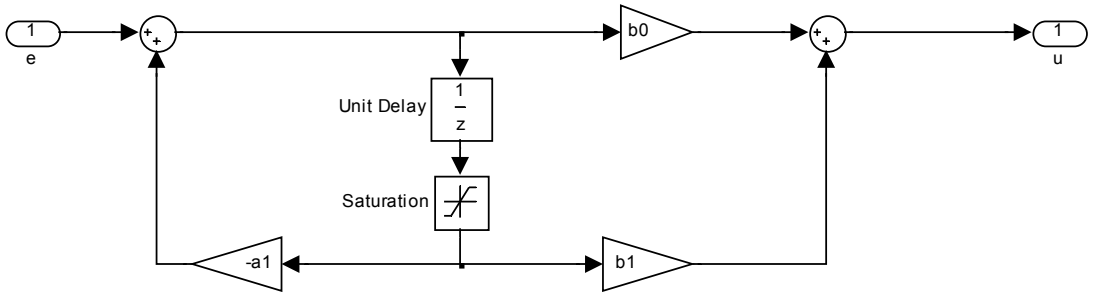

Figure A.2: Direct Form 2 IIR Realization of a PI Controller with Saturation

(A.1) $$\frac{u(z)}{e(z)} = \frac{b_0 z + b_1}{z + a_1} = \frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1}}$$

In this waveform generator, only PI controllers are used. Also, [16] states that TI uses the Euler form of the digital integrator rather than the bilinear form [17]. Lastly, for the initial analysis the smart anti-windup will be removed from the TI diagram to produce:

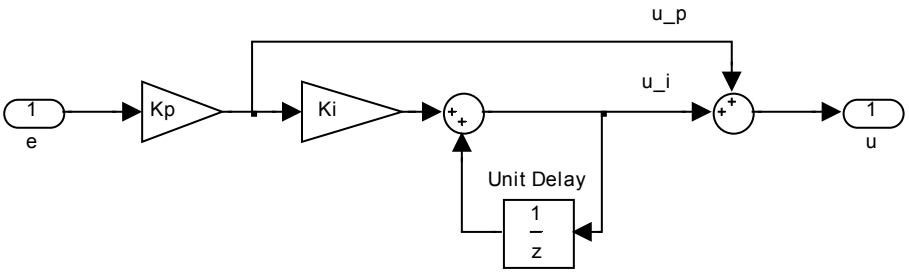

Figure A.3: Simplified Block Diagram of TI's PI Algorithm

This can be reduced to produce the canonical form of the digital difference equation.

(A.2) $$\frac{u(z)}{e(z)} = K_p + K_p K_i \left(\frac{1}{1 - z^{-1}}\right) = \frac{K_p - K_p z^{-1}}{1 - z^{-1}} + \left(\frac{K_p K_i}{1 - z^{-1}}\right) = \frac{K_p(1 + K_i) - K_p z^{-1}}{1 - z^{-1}}$$

(A.3,4,5) $$b_1 = -K_p,\ b_0 = K_p(1 + K_i),\ a_1 = -1$$

The more useful calculations for implementation of the TI PID macro with a calculated transfer function are the inverses of A.3, and 4, which are presented below.

(A.6,7) $$K_p = -b_1,\ K_i = \frac{b_0}{K_p} - 1$$

If a_1 is anything but -1, the digital difference equation is not the realization of an Euler PI controller.

The value of the gain in TI's non-linear smart anti-windup can be determined by trial and error, as is usually the case with anti-windup values.

Appendix B. Derivation of PLL Open Loop Transfer Function

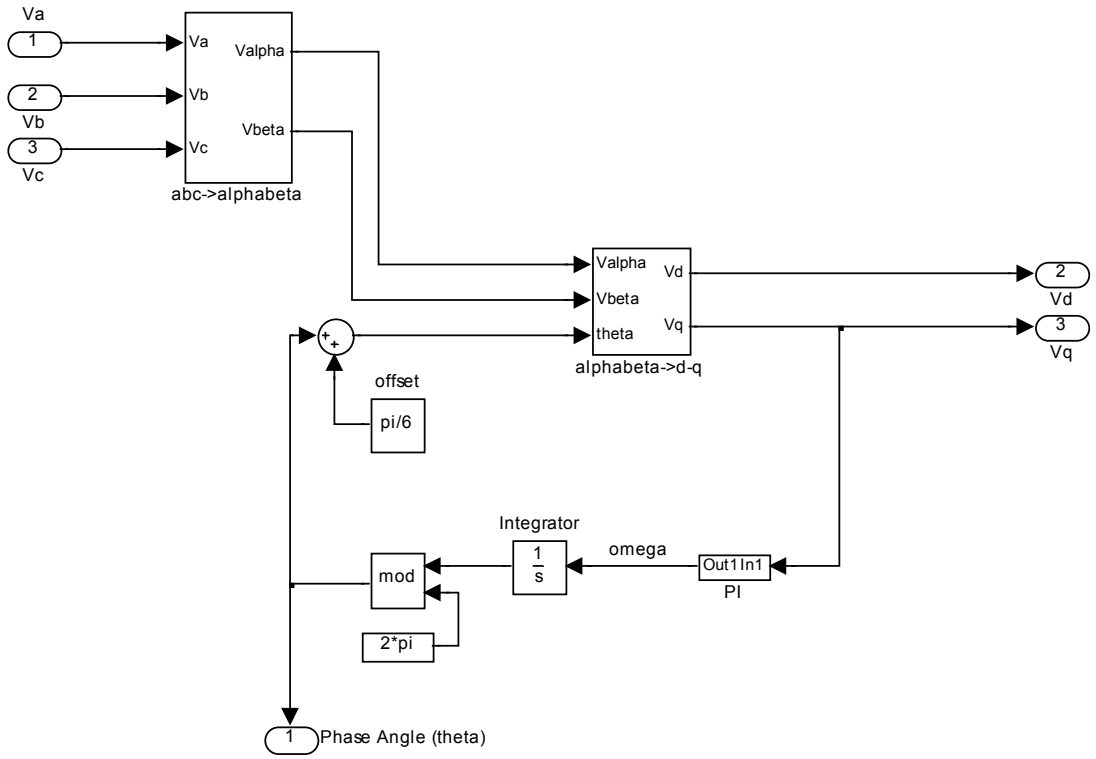

Figure B.1: General Form of the PLL

In order to find the transfer function between theta and q, a diagram of the vectors in d-q space is useful.

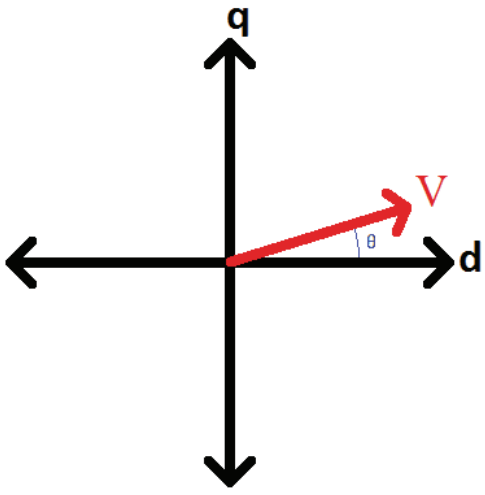

Figure B.2: Voltage Vector in d-q Space

As can be seen in figure B.2, in addition to the standard d-q transform from alpha-beta, the q component can also simply be represented as:

(B.1) $$V_q = V sin\theta$$

The magnitude of vector V is the same in d-q space as it is in alpha-beta; there are no scaling factors between the Clarke and Park transformations, but only trigonometric functions that force the vector to rotate. Therefore, the expression can also be represented as:

(B.2) $$V_q = \sqrt{V_\alpha^2 + V_\beta^2} sin\theta$$

The only other dynamic component to the loop is the integrator that changes rotational speed, ω, to rotational angle, θ.

(B.3) $$V_q = \frac{\sqrt{V_\alpha^2 + V_\beta^2} sin\theta}{s}$$

This equation is nonlinear, and must be linearized. The PLL is expected to drive V_q to zero, so theta will be near zero during normal operation. Under these conditions, it is reasonable to expect that the value of the sine of theta can be approximated by the value of theta itself.

(B.3) $$V_q = \frac{\sqrt{V_\alpha^2 + V_\beta^2}\theta}{s}$$

(B.4) $$\frac{V_q}{\theta} = \frac{\sqrt{V_\alpha^2 + V_\beta^2}}{s}$$

Appendix C. Derivation of Bi-Directional VSI Open Loop Transfer Functions

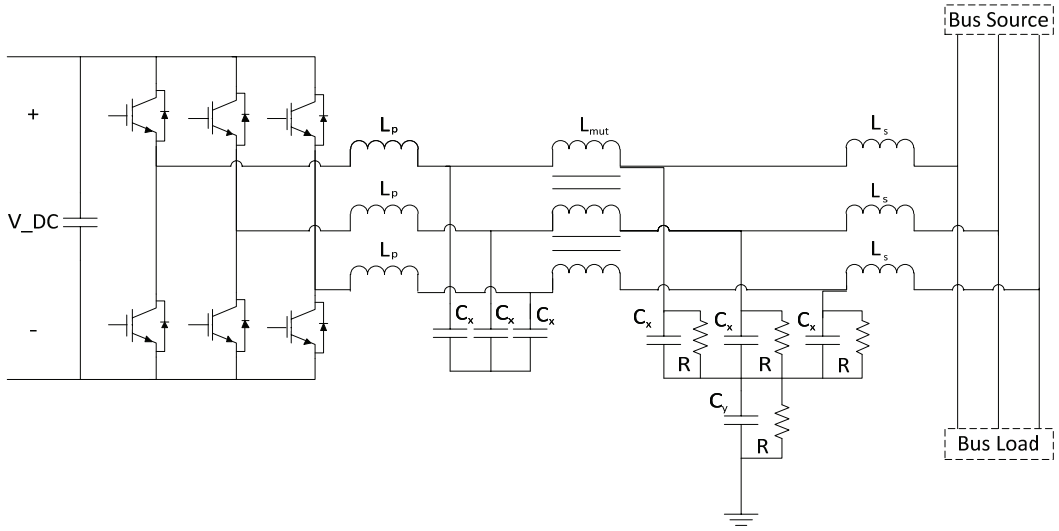

Figure C.1(Figure 4.7): Complete Shunt Injection Power Stage

In this arbitrary waveform generator, only the current through the primary inductors is controlled; the EMI filter and output inductor portions are uncontrolled, but similar impedance comparison techniques to those that are the focus of this entire project are used in section 5.d to ensure stability. The controlled portion of the converter looks like this:

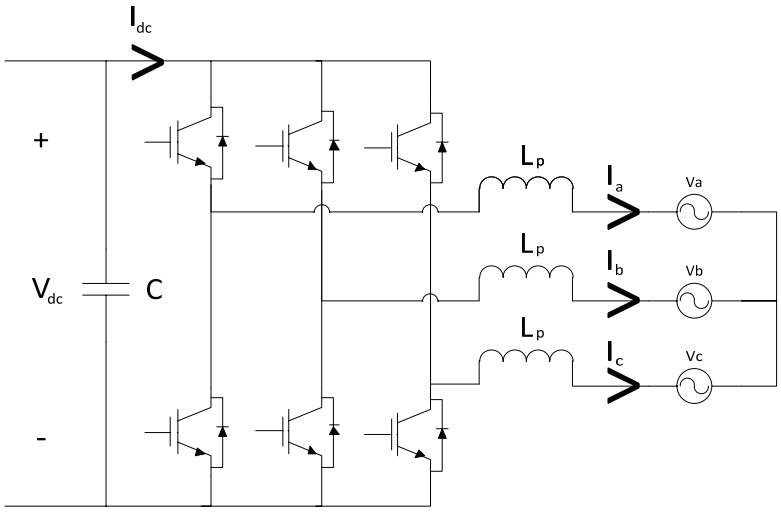

Figure C.2 (Figure 4.4): Annotated VSI for Current Control

The phases will be ordered such that the top one is phase A and the bottom is phase C. All calculations will be performed with phase-to-neutral voltages and currents. In order to operate with a voltage load, the time-averaged output voltage of the 3 switching legs must be equal to the voltages at the load.

[C.1] $$i_{dc} = [s_a \quad s_b \quad s_c] \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

[C.2] $$V_{dc} \begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

[C.3] $$[s_a \quad s_b \quad s_c] =$$

The non-continuous switching waveforms of phase leg a, b, and c

The time-averaged (switching frequency removed) waveforms of the switching waveforms are the duty cycles that are fed into the PWM waveform generator. To find an averaged model, then, the switching matrices will be replaced with duty cycle matrices.

[C.4] $$i_{dc} = [d_a \quad d_b \quad d_c] \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

[C.5] $$\frac{V_{dc}}{2} \begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

[C.6] $$[s_a \quad s_b \quad s_c] =$$

The continuous duty cycle waveforms of phase leg a, b, and c

From these equations, the schematic of an averaged model may be drawn.

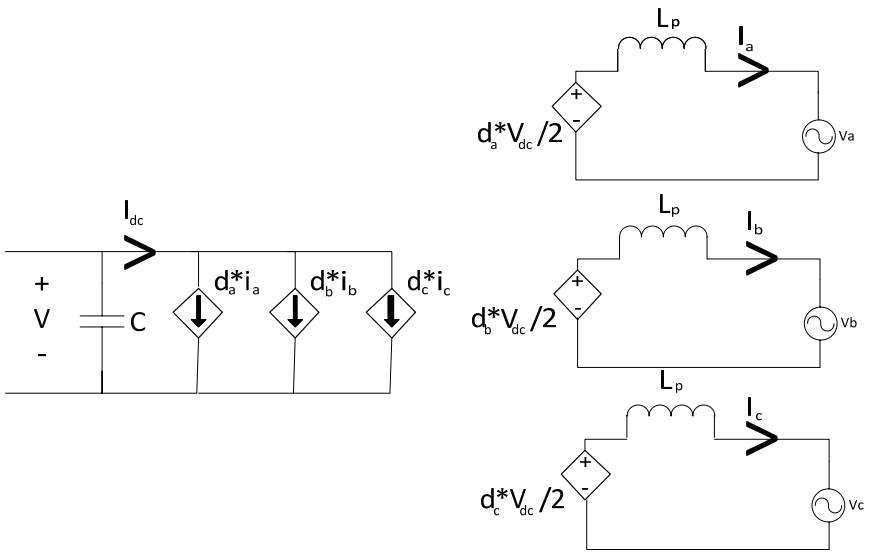

Figure C.3: abc Domain Averaged Model of Figure C.2

The large signal dynamic equations of this model can be written as:

[C.7] $$L\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \frac{V_{dc}}{2}\begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix} - \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

[C.8] $$C\frac{dV_{dc}}{dt} = -[d_a \quad d_b \quad d_c]\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

These equations can be transformed using the Clarke and Park transformations, or the combined direct abc->d-q transform [2].

[C.9] $$T_{abc\to dq0} = \sqrt{\frac{2}{3}}\begin{bmatrix} \cos(\omega t) & \cos\left(\omega t - \frac{2\pi}{3}\right) & \cos\left(\omega t + \frac{2\pi}{3}\right) \\ -\sin(\omega t) & -\sin\left(\omega t - \frac{2\pi}{3}\right) & -\sin\left(\omega t + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} = T_{dq}$$

[C.10, 11] $$X_{dq0} = T_{dq} * X_{abc}, \qquad X_{abc} = {T_{dq}}^{-1} * X_{abc} = {T_{dq}}^{T} * X_{dq0}$$

Assuming balanced three phase operation and ignoring the 0 channel,

[C.12] $$L\frac{d}{dt}\left({T_{dq}}^{T}\begin{bmatrix}i_d\\ i_q\end{bmatrix}\right)=\frac{V_{dc}}{2}\,{T_{dq}}^{T}\begin{bmatrix}d_d\\ d_q\end{bmatrix}-{T_{dq}}^{T}\begin{bmatrix}V_d\\ V_q\end{bmatrix}$$

[C.13] $$L\frac{d}{dt}\left({T_{dq}}^{T}\begin{bmatrix}i_d\\ i_q\end{bmatrix}\right)=L\left(\frac{d}{dt}{T_{dq}}^{T}*\begin{bmatrix}i_d\\ i_q\end{bmatrix}+{T_{dq}}^{T}*\frac{d}{dt}\begin{bmatrix}i_d\\ i_q\end{bmatrix}\right)$$

[C.14] $$L\left(\frac{d}{dt}{T_{dq}}^{T}*\begin{bmatrix}i_d\\ i_q\end{bmatrix}+{T_{dq}}^{T}*\frac{d}{dt}\begin{bmatrix}i_d\\ i_q\end{bmatrix}\right)=\frac{V_{dc}}{2}{T_{dq}}^{T}\begin{bmatrix}d_d\\ d_q\end{bmatrix}-{T_{dq}}^{T}\begin{bmatrix}V_d\\ V_q\end{bmatrix}$$

Multiplying through by the transformation matrix on both sides of the equation:

[C.15] $$L\left(T_{dq}\frac{d}{dt}{T_{dq}}^{T}*\begin{bmatrix}i_d\\ i_q\end{bmatrix}+T_{dq}{T_{dq}}^{T}*\frac{d}{dt}\begin{bmatrix}i_d\\ i_q\end{bmatrix}\right)=\frac{V_{dc}}{2}T_{dq}{T_{dq}}^{T}\begin{bmatrix}d_d\\ d_q\end{bmatrix}-T_{dq}{T_{dq}}^{T}\begin{bmatrix}V_d\\ V_q\end{bmatrix}$$

[C.16] $$L\left(T_{dq}\frac{d}{dt}{T_{dq}}^{T}*\begin{bmatrix}i_d\\ i_q\end{bmatrix}+\frac{d}{dt}\begin{bmatrix}i_d\\ i_q\end{bmatrix}\right)=V_{dc}\begin{bmatrix}d_d\\ d_q\end{bmatrix}-\begin{bmatrix}V_d\\ V_q\end{bmatrix}$$

[C.17] $$T_{dq}\frac{d}{dt}{T_{dq}}^{T}=\sqrt{\frac{2}{3}}\begin{bmatrix}\cos(\omega t) & \cos\left(\omega t-\frac{2\pi}{3}\right) & \cos\left(\omega t+\frac{2\pi}{3}\right)\\ -\sin(\omega t) & -\sin\left(\omega t-\frac{2\pi}{3}\right) & -\sin\left(\omega t+\frac{2\pi}{3}\right)\\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}}\end{bmatrix}$$

$$*\sqrt{\frac{2}{3}}\begin{bmatrix}-\omega\sin(\omega t) & -\omega\cos(\omega t) & 0\\ -\omega\sin\left(\omega t-\frac{2\pi}{3}\right) & -\omega\cos\left(\omega t-\frac{2\pi}{3}\right) & 0\\ -\omega\sin\left(\omega t+\frac{2\pi}{3}\right) & -\omega\cos\left(\omega t+\frac{2\pi}{3}\right) & 0\end{bmatrix}=\frac{2}{3}\begin{bmatrix}A & B & C\\ D & E & F\\ G & H & I\end{bmatrix}$$

[C.18] $$A=\omega\left(-\sin(\omega t)\cos(\omega t)-\sin\left(\omega t-\frac{2\pi}{3}\right)\cos\left(\omega t-\frac{2\pi}{3}\right)-\sin\left(\omega t+\frac{2\pi}{3}\right)\cos\left(\omega t+\frac{2\pi}{3}\right)\right)=0$$

[C.19] $$B = \omega\left(-\cos^2(\omega t) - \cos^2\left(\omega t - \frac{2\pi}{3}\right) - \cos^2\left(\omega t + \frac{2\pi}{3}\right)\right) = -\frac{3\omega}{2}$$

[C.20] $$C = 0 + 0 + 0 = 0$$

[C.21] $$D = \omega\left(\sin^2(\omega t) + \sin^2\left(\omega t - \frac{2\pi}{3}\right) + \sin^2\left(\omega t + \frac{2\pi}{3}\right)\right) = \frac{3\omega}{2}$$

[C.22] $$E = \omega\left(\sin(\omega t)\cos(\omega t) + \sin\left(\omega t - \frac{2\pi}{3}\right)\cos\left(\omega t - \frac{2\pi}{3}\right) + \sin\left(\omega t + \frac{2\pi}{3}\right)\cos\left(\omega t + \frac{2\pi}{3}\right)\right) = 0$$

[C.23] $$F = 0 + 0 + 0 = 0$$

[C.24] $$G = -\frac{\omega}{\sqrt{2}}\left(\sin(\omega t) + \sin\left(\omega t - \frac{2\pi}{3}\right) + \sin\left(\omega t + \frac{2\pi}{3}\right)\right) = 0$$

[C.25] $$H = -\frac{\omega}{\sqrt{2}}\left(\cos(\omega t) + \cos\left(\omega t - \frac{2\pi}{3}\right) + \cos\left(\omega t + \frac{2\pi}{3}\right)\right) = 0$$

[C.26] $$I = 0 + 0 + 0 = 0$$

[C.27] $$T_{dq}\frac{d}{dt}{T_{dq}}^T = \frac{2}{3}\begin{bmatrix} 0 & -\frac{3\omega}{2} & 0 \\ \frac{3\omega}{2} & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} = \begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

Ignoring the 0 component,

[C.28] $$\begin{bmatrix} 0 & -\omega & 0 \\ \omega & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}$$

[C.29] $$L\left(\begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix}\right) = V_{dc}\begin{bmatrix} d_d \\ d_q \end{bmatrix} - \begin{bmatrix} V_d \\ V_q \end{bmatrix}$$

[C.30] $$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{V_{dc}}{2L}\begin{bmatrix} d_d \\ d_q \end{bmatrix} - \frac{1}{L}\begin{bmatrix} V_d \\ V_q \end{bmatrix} - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix}$$

Now, for the DC voltage equation:

[C.31] $$C\frac{dV_{dc}}{dt} = -[d_a \quad d_b \quad d_c]\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

[C.32] $$C\frac{dV_{dc}}{dt} = -[d_a \quad d_b \quad d_c][I]\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = -[d_a \quad d_b \quad d_c]{T_{dq}}^T T_{dq}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$$

[C.33] $$[d_a \quad d_b \quad d_c]{T_{dq}}^T = \left(T_{dq}\begin{bmatrix} d_a \\ d_b \\ d_c \end{bmatrix}\right)^T$$

[C.34] $$\frac{dV_{dc}}{dt} = -\frac{1}{C}[d_d \quad d_q]\begin{bmatrix} i_d \\ i_q \end{bmatrix}$$

Both the inductor current and DC voltage equations have non-linear components, and must be linearized.

[C.35] $$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \frac{V_{dc}}{2L}\begin{bmatrix} d_d \\ d_q \end{bmatrix} - \frac{1}{L}\begin{bmatrix} V_d \\ V_q \end{bmatrix} - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix}$$

[C.36] $$\frac{d}{dt}\begin{bmatrix} \tilde{\imath}_d \\ \tilde{\imath}_q \end{bmatrix} = \frac{V_{dc}}{2L}\begin{bmatrix} \tilde{d}_d \\ \tilde{d}_q \end{bmatrix} + \frac{\tilde{v}_{dc}}{2L}\begin{bmatrix} d_d \\ d_q \end{bmatrix} - \frac{1}{L}\begin{bmatrix} \tilde{v}_d \\ \tilde{v}_q \end{bmatrix} - \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}\begin{bmatrix} \tilde{\imath}_d \\ \tilde{\imath}_q \end{bmatrix}$$

[C.37] $$\frac{dV_{dc}}{dt} = -\frac{1}{C}[d_d \quad d_q]\begin{bmatrix} i_d \\ i_q \end{bmatrix}$$

[C.38] $$\frac{d\tilde{v}_{dc}}{dt} = -\frac{1}{C}\begin{bmatrix} \tilde{d}_d & \tilde{d}_q \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} - \frac{1}{C}[d_d \quad d_q]\begin{bmatrix} \tilde{\imath}_d \\ \tilde{\imath}_q \end{bmatrix}$$

Putting all of this into one big state space representation:

[C.39] $$\frac{d}{dt}\begin{bmatrix} \tilde{\imath}_d \\ \tilde{\imath}_q \\ \tilde{v}_{dc} \end{bmatrix} = \begin{bmatrix} 0 & -\omega & \frac{d_d}{L} \\ \omega & 0 & \frac{d_q}{L} \\ -\frac{d_d}{C} & -\frac{d_q}{C} & 0 \end{bmatrix}\begin{bmatrix} \tilde{\imath}_d \\ \tilde{\imath}_q \\ \tilde{v}_{dc} \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}}{2L} & 0 \\ 0 & \frac{V_{dc}}{2L} \\ -\frac{i_d}{C} & -\frac{i_q}{C} \end{bmatrix}\begin{bmatrix} \tilde{d}_d \\ \tilde{d}_q \end{bmatrix} + \begin{bmatrix} -\frac{1}{L} & 0 \\ 0 & -\frac{1}{L} \\ 0 & 0 \end{bmatrix}\begin{bmatrix} \tilde{v}_d \\ \tilde{v}_q \end{bmatrix}$$

[C.40] $$\begin{bmatrix} 0 & -\omega & \frac{d_d}{L} \\ \omega & 0 & \frac{d_q}{L} \\ -\frac{d_d}{C} & -\frac{d_q}{C} & 0 \end{bmatrix} = \boldsymbol{A}$$

[C.41] $$\begin{bmatrix} \frac{V_{dc}}{2L} & 0 \\ 0 & \frac{V_{dc}}{2L} \\ \frac{i_d}{C} & \frac{i_q}{C} \end{bmatrix} = \boldsymbol{B}$$

[C.42] $$\begin{bmatrix} \frac{1}{L} & 0 \\ 0 & \frac{1}{L} \\ 0 & 0 \end{bmatrix} = \boldsymbol{F}$$

In the world of power electronics, the output voltages are often considered to be process disturbances in state space representations. When finding individual transfer functions and setting all small signal values except the ones of interest to zero, the F matrix can be used instead of B to easily find output impedances.

Using the standard method of converting a state space representation to a matrix of continuous domain transfer functions,

[C.43] $$\frac{y(s)}{u(s)} = (s\boldsymbol{I} - A)^{-1}\boldsymbol{B}$$

Using Mathematica to perform the matrix inverse and simplify the expressions:

In[1]:=
```
A = {{0, -w, dd / L}, {w, 0, dq / L}, {-dd / C, -dq / C, 0}}
```

Out[1]=
$$\begin{pmatrix} 0 & -w & \frac{dd}{L} \\ w & 0 & \frac{dq}{L} \\ -\frac{dd}{C} & -\frac{dq}{C} & 0 \end{pmatrix}$$

In[2]:=
```
B = {{Vdc / L / 2, 0}, {0, Vdc / L / 2}, {-id / C, -iq / C}}
```

Out[2]=
$$\begin{pmatrix} \frac{Vdc}{2L} & 0 \\ 0 & \frac{Vdc}{2L} \\ -\frac{id}{C} & -\frac{iq}{C} \end{pmatrix}$$

In[3]:=
```
Gid = Collect[FullSimplify[Dot[Collect[Inverse[(s * IdentityMatrix[3] - A)], s], B]], s]
```

Out[3]=
$$\begin{pmatrix} \frac{Vdc\ dq^2+2\ id\ L\ w\ dq-2\ dd\ id\ L\ s+C\ L\ s^2\ Vdc}{2\ L\ s\left(dd^2+dq^2+C\ L\left(s^2+w^2\right)\right)} & -\frac{2\ dd\ iq\ L\ s+C\ L\ Vdc\ w\ s+dd\ dq\ Vdc-2\ dq\ iq\ L\ w}{2\ L\ s\left(dd^2+dq^2+C\ L\left(s^2+w^2\right)\right)} \\ \frac{L\ (C\ s\ Vdc-2\ dd\ id)\ w-dq\ (2\ id\ L\ s+dd\ Vdc)}{2\ L\ s\left(dd^2+dq^2+C\ L\left(s^2+w^2\right)\right)} & \frac{Vdc\ dd^2-2\ iq\ L\ w\ dd-2\ dq\ iq\ L\ s+C\ L\ s^2\ Vdc}{2\ L\ s\left(dd^2+dq^2+C\ L\left(s^2+w^2\right)\right)} \\ -\frac{Vdc\ (dd\ s+dq\ w)+2\ id\ L\left(s^2+w^2\right)}{2\ s\left(dd^2+dq^2+C\ L\left(s^2+w^2\right)\right)} & \frac{-dq\ s\ Vdc+dd\ w\ Vdc-2\ iq\ L\left(s^2+w^2\right)}{2\ s\left(dd^2+dq^2+C\ L\left(s^2+w^2\right)\right)} \end{pmatrix}$$

In[4]:=
```
G_iddd = Collect[Numerator[Gid[[1, 1]]], s] / Collect[Denominator[Gid[[1, 1]]], s]
```

Out[4]=
$$\frac{C\ L\ s^2\ Vdc - 2\ dd\ id\ L\ s + dq^2\ Vdc + 2\ dq\ id\ L\ w}{2\ L\ s\left(C\ L\ w^2 + dd^2 + dq^2\right) + 2\ C\ L^2\ s^3}$$

In[5]:=
```
G_idqd = Collect[Numerator[Gid[[1, 2]]], s] / Collect[Denominator[Gid[[1, 2]]], s]
```

Out[5]=
$$\frac{s\ (-C\ L\ Vdc\ w - 2\ dd\ iq\ L) - dd\ dq\ Vdc + 2\ dq\ iq\ L\ w}{2\ L\ s\left(C\ L\ w^2 + dd^2 + dq^2\right) + 2\ C\ L^2\ s^3}$$

In[7]:=
```
G_iddq = Collect[Numerator[Gid[[2, 1]]], s] / Collect[Denominator[Gid[[2, 1]]], s]
```

Out[7]=
$$\frac{s\ (C\ L\ Vdc\ w - 2\ dq\ id\ L) - dd\ dq\ Vdc - 2\ dd\ id\ L\ w}{2\ L\ s\left(C\ L\ w^2 + dd^2 + dq^2\right) + 2\ C\ L^2\ s^3}$$

In[8]:=
```
G_idqq = Collect[Numerator[Gid[[2, 2]]], s] / Collect[Denominator[Gid[[2, 2]]], s]
```

Out[8]=
$$\frac{C\ L\ s^2\ Vdc + dd^2\ Vdc - 2\ dd\ iq\ L\ w - 2\ dq\ iq\ L\ s}{2\ L\ s\left(C\ L\ w^2 + dd^2 + dq^2\right) + 2\ C\ L^2\ s^3}$$

In[9]:=
```
G_vdd = Collect[Numerator[Gid[[3, 1]]], s] / Collect[Denominator[Gid[[3, 1]]], s]
```

Out[9]=
$$\frac{-dd\ s\ Vdc - dq\ Vdc\ w - 2\ id\ L\ s^2 - 2\ id\ L\ w^2}{2\ s\left(C\ L\ w^2 + dd^2 + dq^2\right) + 2\ C\ L\ s^3}$$

In[10]:=
```
G_vdq = Collect[Numerator[Gid[[3, 2]]], s] / Collect[Denominator[Gid[[3, 2]]], s]
```

Out[10]=
$$\frac{dd\ Vdc\ w - dq\ s\ Vdc - 2\ iq\ L\ s^2 - 2\ iq\ L\ w^2}{2\ s\left(C\ L\ w^2 + dd^2 + dq^2\right) + 2\ C\ L\ s^3}$$

The values of the duty cycles and the currents will vary, but as long as one channel is used at a time, the variance in the transfer functions isn't very much. For the values of L, C, ω, V_{dc} in the waveform generator power stage design, and exciting each of the channels independently to maximum power and duty cycle:

[C.41] $$G_{iddd} = G_{idqq} = \frac{172000s - 4.18462}{s^2 + 339045}$$

When the loop is closed about a compensator such as that designed in the "Closed Loop Design" section, this transfer function can be compared to a simulation of the averaged model circuit. Using identical compensators, the closed-loop transfer function gained from simulation and the closed-loop transfer function gained from the analytical solution are presented below.

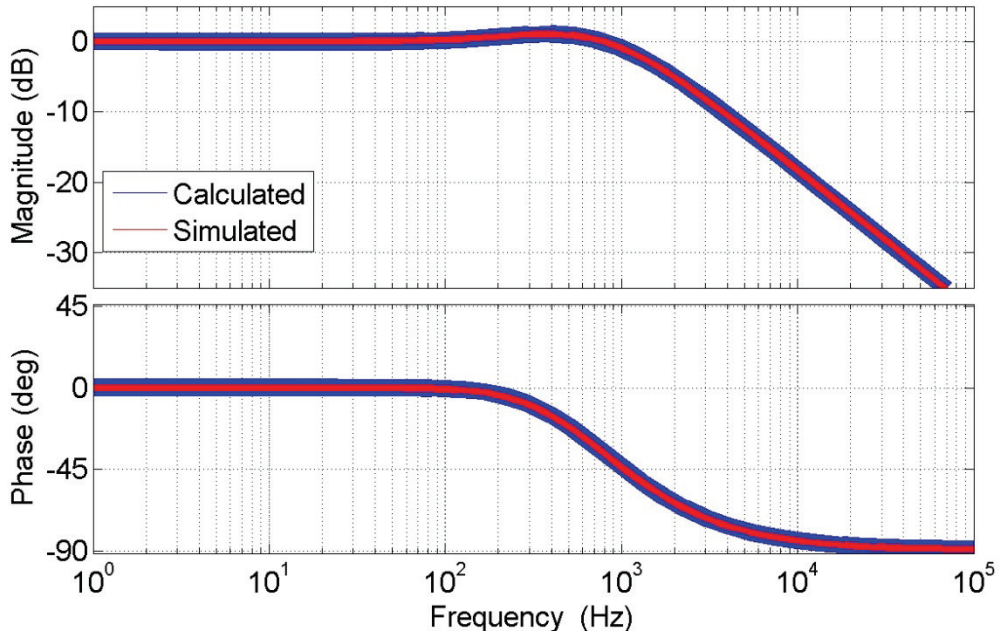

Figure C.4: Calculated and Simulated Closed Loop Control-to-Current Transfer Functions

It is of note that a slight resonance can occur if both channels are excited at the same time. The plot below illustrates this.

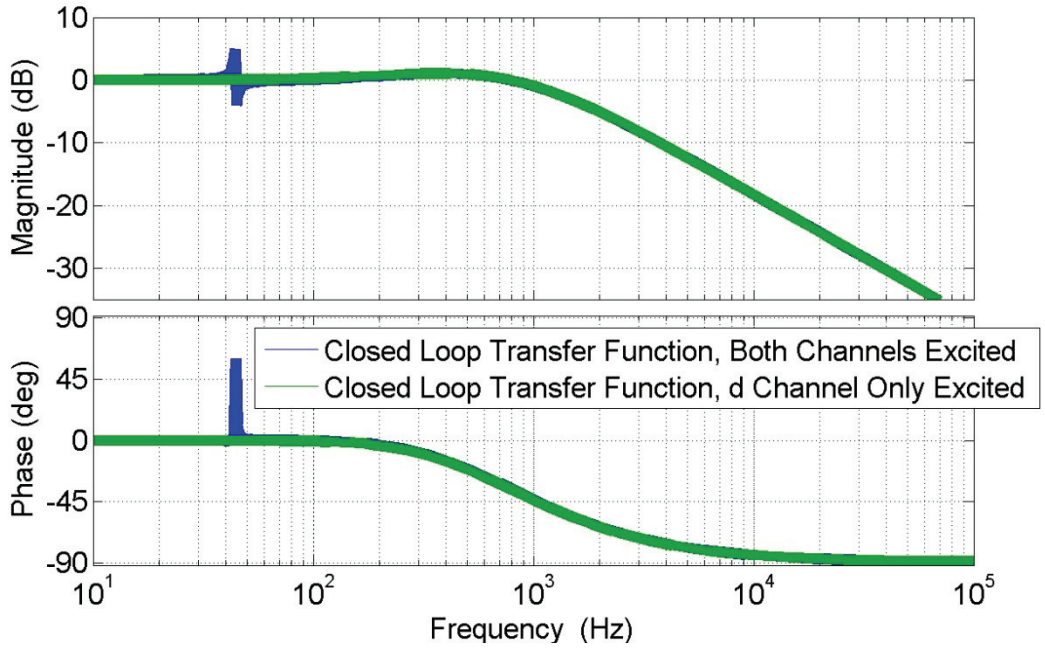

Figure C.5: Closed Loop Control-to-Output Transfer Functions with One and Both d-q Channels Excited

This is the effect of the coupling. This derivation was simplified; there is no damping whatsoever in the model. Practically, it can be expected that the resonance shown will further damped.

The compensator used in Figures C.4 and C.5 is the one designed in the section "Closed Loop Control Design." The transfer function of closed-loop control to current is:

[C.42] $$\frac{\tilde{\imath}_{com}}{\tilde{\imath}_d} = \frac{8038s^2+1.249*10^7-3.087*10^8}{s^3+8038s^2+1.283*10^7 s-3.083*10^8}$$

The i_d-to-V_{dc} transfer function can be found from equation C.39.

[C.43] $$\frac{\tilde{v}_{dc}}{\tilde{\imath}_d} = -\frac{d_d}{sC} = -\frac{.8}{.0013s}$$

Knowing control-to-current and current-to-V_{dc}, the open loop transfer function of control-to-V_{dc} can be found as:

[C.44] $$\frac{\frac{\tilde{v}_{dc}}{\tilde{\imath}_d}}{\frac{\tilde{\imath}_{com}}{\tilde{\imath}_d}} = \frac{\tilde{v}_{dc}}{\tilde{\imath}_{com}} = -\frac{.07656\, s^3 + 615.4s^2 - 2.363*10^7\, s}{s^3 + 1554\, s^2 - 3.84*10^4\, s}$$

Notice that this whole transfer function is negative. This simply means that an increase in current command results in a decrease in DC link voltage. This is to be expected; positive current has been defined here as active current flowing away from the DC link. All that this means is that in order for a compensator to work normally, the negative of the error must be fed to the compensator.

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