Electric Field Grading and Electrical Insulation Design for High Voltage, High Power Density Wide Bandgap Power Modules

Maryam Mesgarpour Tousi

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Mona Ghassemi, Chair
Virgilio A. Centeno
Vassilis Kekatos
Ahmad Safaai-Jazi
Weijun Xie

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ABSTRACT

The trend towards more and all-electric apparatuses and more electrification will lead to higher electrical demand. Increases in electrical power demand can be provided by either higher currents or higher voltages. Due to “weight” and “voltage” drop, a raise in the current is not preferred; so, “higher voltages” are being considered. Another trend is to reduce the size and weight of apparatuses. Combined, these two trends result in the high voltage, high power density concept. It is expected that by 2030, 80% of all electric power will flow through “power electronics systems”. In regards to the high voltage, high power density concept described above, “wide bandgap (WBG) power modules” made from materials such as “SiC and GaN (and, soon, Ga_2O_3 and diamond)”, which can endure “higher voltages” and “currents” rather than “Si-based modules”, are considered to be the most promising solution to reducing the size and weight of “power conversion systems”. In addition to the trend towards higher “blocking voltage”, volume reduction has been targeted for WBG devices. The blocking voltage is the breakdown voltage capability of the device, and volume reduction translates into power density increase. This leads to extremely high electric field stress, E, of extremely nonuniform type within the module, leading to a higher possibility of “partial discharge (PD)” and, in turn, insulation degradation and, eventually, breakdown of the module. Unless the discussed high E issue is satisfactorily addressed and solved, realizing next-generation high power density WBG power modules that can properly operate will not be possible. Contributions and innovations of this Ph.D. work are as follows. i) Novel electric field grading techniques

including (a) various geometrical techniques, (b) applying “nonlinear field-dependent conductivity (FDC) materials” to high E regions, and (c) combination of (a) and (b), are developed; ii) A criterion for the electric stress intensity based upon accurate dimensions of a power device package and its “PD measurement” is presented; iii) Guidelines for the electrical insulation design of next-generation high voltage (up to 30 kV), high power density “WBG power modules” as both the “one-minute insulation” and PD tests according to the standard IEC 61287-1 are introduced; iv) Influence of temperature up to 250°C and frequency up to 1 MHz on E distribution and electric field grading methods mentioned in i) is studied; and v) A coupled thermal and electrical (electrothermal) model is developed to obtain thermal distribution within the module precisely. All models and simulations are developed and carried out in COMSOL Multiphysics.

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GENERAL AUDIENCE ABSTRACT

In power engineering, power conversion term means converting electric energy from one form to another such as converting between AC and DC, changing the magnitude or frequency of AC or DC voltage or current, or some combination of these. The main components of a power electronic conversion system are power semiconductor devices acted as switches. A power module provides the physical containment and package for several power semiconductor devices. There is a trend towards the manufacturing of electrification apparatuses with higher power density, which means handling higher power per unit volume, leading to less weight and size of apparatuses for a given power. This is the case for power modules as well. Conventional "silicon (Si)-based semiconductor technology" cannot handle the power levels and switching frequencies required by "next-generation" utility applications. In this regard, "wide bandgap (WBG) semiconductor materials", such as "silicon carbide (SiC)"," gallium nitride (GaN)", and, soon, "gallium oxide" and "diamond" are capable of higher switching frequencies and higher voltages, while providing for lower switching losses, better thermal conductivities, and the ability to withstand higher operating temperatures. Regarding the high power density concept mentioned above, the challenge here, now and in the future, is to design compact WBG-based modules. To this end, the extremely nonuniform high electric field stress within the power module caused by the aforementioned trend and emerging WBG semiconductor switches should be graded and mitigated to prevent partial discharges that can eventually lead to breakdown of the module. In this Ph.D. work, new electric field grading methods

including various geometrical techniques combined with applying nonlinear field-dependent conductivity (FDC) materials to high field regions are introduced and developed through simulation results obtained from the models developed in this thesis.

To my beloved husband, Ebrahim, and my little angel, Bahar

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these years, who was the source of peace, energy, and life for me. I am also truly appreciative for having an amazing and artistic mother, Sheyda, and perceptive and compassionate father, Abolghassem, who were always believed in me, and with their unconditional love have supported me in my whole life.

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Chapter 1

Introduction

1.1 Motivation and Significance: WBG Module Packaging in Light of High Voltage, High Power Density Concept

Owing to the increased demand for displacing heavy mechanical, pneumatic, and hydraulic systems with low-weight, compact, and high-efficient electrical alternatives, the higher electrical requirement is needed. Advancing toward higher voltages or higher currents is required to well-address the demand for increased electrical power. Typically, higher voltages rather than higher currents are more desirable due to the weight considerations and voltage drop. Another tendency, particularly in the aerospace and military applications, is decreasing the volume and weight of devices. To illustrate, a 4.7% yearly growth in the global air traffic passengers is anticipated by 2028 [1], with a duplicated number of passengers expected in the following 20 years to about 2040 [2]. Nonetheless, the “aerospace industry” will need to deal simultaneously with “economic” and “environmental” challenges. As preserving one-kilogram mass per flight could lead to saving approximately 1700 t and 5400 t of fuel and CO_2 per year for all air travels, respectively.[3]. As another instance, most of the electrical system functionality

requirements of the next-generation all-electric warships can be met by the existing power electronics technology but does so at the cost of “high weight” and a “large footprint”.

In power engineering, power conversion term means converting electric energy from one form to another such as converting between AC and DC, changing the magnitude or frequency of AC or DC voltage or current, or some combination of these. By 2030, power conversion systems are expected to receive almost 80% of all electric power [4]. Military, commercial, and industrial applications of “high voltage, high power-density conversion electronics systems” include “high-speed motor” drives [5], “down-hole drilling” [6], “hybrid-electric” and “all-electric vehicle chargers” [7], “solar/wind inverters” [8], “high-voltage circuit breakers” [9], “power conversion for naval ships” [10], “solid-state transformers” [11], “smart grid-tie systems” [12], “energy storage systems” [13], and “rail transport” [14], to name a few.

The main components of a power electronic conversion system are power semiconductor devices acted as switches. A power module provides the physical containment and package for several power semiconductor devices. The trend towards the high voltage, high power density concept is the case for power modules as well. Conventional “silicon (Si)-based semiconductor technology” cannot handle the power levels and switching frequencies required by next-generation utility applications. In this regard, “WBG semiconductor materials”, such as silicon carbide (SiC), gallium nitride (GaN) (and soon gallium oxide (Ga_2O_3) and diamond) are capable of higher switching frequencies and higher voltages while providing for lower switching losses, better thermal conductivities, and the ability to withstand higher operating temperatures.

Regarding the high voltage, high power density concept mentioned above, the challenge here, now and in the future, is to design compact WBG-based modules. For instance, while the highest record of the blocking voltage of Si-based IGBT is 6.5 kV to date, the high blocking voltages of 15 kV for 80 A and 24 kV for 30 A for SiC IGBT have been reported [15]. In addition to 2.3 times higher blocking voltage, the 15-kV SiC IGBT has a volume three times smaller than its Si-based counterpart. [15]. The combination of a higher blocking voltage and a more compact design results in a higher electric field within the power device packaging. Consequently, an extremely undesirable environment for the insulation system created by the presence of high electric stress and exposure of the power device to high slew rates voltage pulses causes a detrimental impact on the insulation materials aging and degradation due to increased unacceptable PD events. [16-29].

To this end, the extremely nonuniform high electric field stress within next-generation high voltage, high power density WBG power modules should be graded and mitigated to prevent unacceptable PD activity that can eventually lead to breakdown of the module. Unless the discussed high electric field issue is satisfactorily addressed and solved, realizing next generation high voltage, high power density WBG power modules that can properly operate will not be possible.

1.2 Research Objectives and Results

The aim of this Ph.D. work is the grading and mitigation of extremely nonuniform "high electric field stress" within "envisaged high voltage, high power density WBG power modules". Also, an electrothermal model is developed to predict precisely temperature in power modules.

The electric field grading techniques introduced and developed in this work are combinations of various geometrical techniques and utilizing composites with “nonlinear field dependent conductivity (FDC)” characteristics as layers applied to high-stressed regions within the power module, where nonlinear FDC layers are characterized in terms of required nonlinearity properties and dimensions. To this end, accurate finite element method (FEM) electric field calculation models are developed in COMSOL Multiphysics.

There is a challenge here: how much we have to lessen the electric field intensity in the module? In other words, a criterion as allowable electric field stress in the module should be defined. This criterion is developed in this thesis.

Besides the challenge between trend towards minimum dimension (maximum compactness) of future high voltage WBG power modules and allowable electric field stress, the electrical insulation design should meet both the present standard tests recommended in IEC 61287-1 (PD and one-minute insulation test), that is addressed in this thesis.

1.3 Research Outline

This thesis is outlined in six chapters as follows.

Since one of the main contributions of this thesis is to introduce combinations of nonlinear FDC composites with various geometrical techniques as efficient techniques for electric field grading, it is needed to explain the characteristics of nonlinear FDC composites. In this regard, **CHAPTER 2** provides a literature review of nonlinear FDC composites. Mainly the focus will be on “Microvaristors” having superior properties than other

nonlinear FDC materials, and their parameters, such as shape, size, and the percolation level of the filler particles that affect nonlinear properties are discussed in detail.

In **CHAPTER 3**, an electric field "criterion" based upon exact dimensions and PD test measurements of a "power module" is proposed. Our studies show that the enhanced electric field issue within "high voltage high power-density WBG power modules" cannot be addressed by either individually or combined geometrical modifications such as (1) "metal layer offset", (2) "stacked substrate design", and (3) "protruding substrate". Subsequently, for the first time, we demonstrate that by combining the above-mentioned "geometrical techniques" and utilization of a "nonlinear FDC composite layer", the high electric field issue can be addressed effectively. In this chapter, several electric field mitigation techniques developed, and through simulations performed via COMSOL Multiphysics, their effectiveness was verified. These Mitigation techniques can be further utilized as a guideline for designing the "next-generation WBG power modules". These guidelines assure that the insulation design of the "envisaged high voltage WBG power module" meets all the requirements regarding the standard insulation tests based on IEC 61287-1.

CHAPTER 4 presents the assessment of the proposed field grading technique using a combination of geometrical techniques and applying nonlinear FDC composites under a wide range of temperatures and frequencies up to 250°C and 1 MHz. In this chapter, using the experimental data reported in the literature on the dielectric behavior of silicone gel and Aluminum Nitride (AlN), two dielectrics usually used in power modules, the effect of both temperature and frequency on the efficacy of the developed mitigation technique is investigated.

CHAPTER 5 develops a coupled electrical and thermal (electrothermal) model using a circuit simulator to obtain accurate thermal distribution within a proposed 10 kV power module consisting of 9 WBG PiN diodes. The influence of the temperature-dependency behavior of the electrical characteristics of the chips under different loads is studied, and the maximum current load that the power module can withstand is estimated.

CHAPTER 6 provides a general conclusion of the research findings discussed in this work and outlines some recommendations for further improvements.

Chapter 2

Nonlinear Dielectric Composite Characteristics

2.1 Introduction

Localized electric field enhancement at high stressed regions of the compact power modules operating at high blocking voltages can induce unacceptable PD activities within dielectrics embedded in the module. Sustaining undesirable PD activities over time within dielectric materials leading to material aging and shortening the life-time of the whole power device.

One of the most effective approaches to mitigate the enhanced electric field in high voltage apparatus is using nonlinear FDC dielectric composites. This method has been successfully utilized in stress grading systems in form-wound machines and cable terminations in [30, 31].

Nonlinear FDC composites, having $J(E)$ characteristics e.g. shown in Figure 2.1 where J is the current density composed of "conductive" or "semiconductive" filler particles (e.g., "zinc oxide microvaristors") blended with a "polymer matrix" (e.g., "silicone rubber" or "epoxy resin"). Nonlinear FDC materials can influence the electric field distribution based upon their two inherent characteristics: switching field (E_b) and

nonlinearity coefficient (α). Filler shape, size, and percolation level in the polymer matrix are the most critical parameters that greatly impact the nonlinearity characteristics of FDC materials. Typically, in most of the applications, the field grading influence of nonlinear FDC materials with $\alpha > 10$ is independent of frequency and thus is more efficient. Resistive currents generated through nonlinear FDC composite resulting from phase change from capacitive to resistive at $E > E_b$, improve the uniformity of electric field lines in particular in high-stressed zones. Since E_b and α can be tailored and engineered by modifying the filler physical characteristics, and concentration of filler particles as well as the type of host polymer matrix, the influence of each of these parameters on E_b and α is discussed in the following. We discuss further Figure 2-1 in Section 2-5.

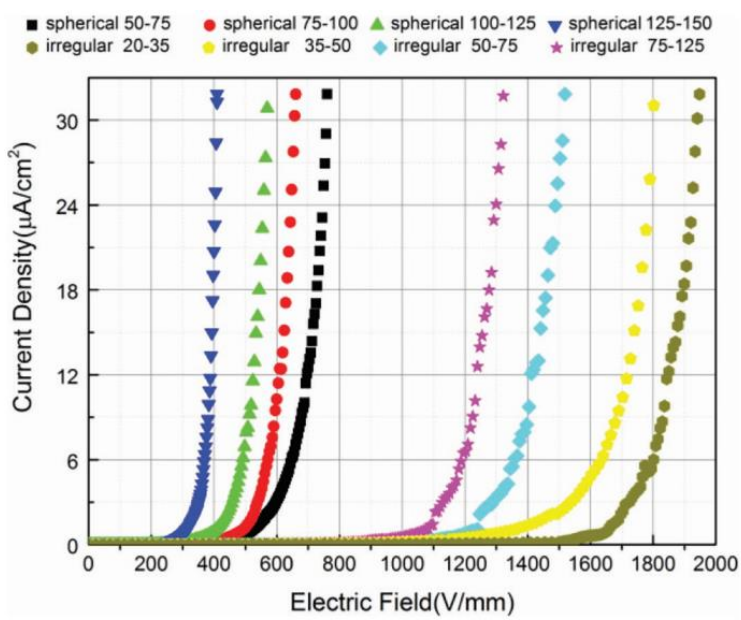

Figure 2-1: $J(E)$ characteristics of silicone rubber/ZnO composites containing 46.5 vol % of ZnO particles of various shapes and sizes [32].

2.2 The Percolation Level of Filler Particles within the Composite

The concentration level of filers has a decisive role in the onset of nonlinearity features of the FDC composite. Thus, to display nonlinear electrical characteristics, the

filler percolation level must exceed a threshold value. The process by which the concentration of filler in the insulation is controlled is called the “percolation process”. Accordingly, a practical way to manipulate the nonlinearity characteristics of FDC composites is to monitor the fillers' percolation level in the insulation matrix meticulously. At sufficiently low percolation levels, the FDC materials act similar to perfect insulators. At percolation levels higher than the threshold value, which is thoroughly dependent on the filler and insulator’s chemical and physical properties, the composite shows field-dependent conductivity features.

Composites such as ZnO/Polyethylene or SiC/EPDM where ZnO and SiC are fillers and polyethylene and EPDM are host polymers, with spherical and round fillers, it was found that the percolation threshold value must be between 30-50 %vol for obtaining the nonlinearity characteristics like those shown in Figure 2-1 [33-35]. Percolation level is greatly influenced by the filler-filler contact that is dependent on the shape of fillers. In this regard, two types of contact as “face-contact” as shown in Figure 2-2b and “edge-contact” as shown in Figure 2-2c exist between irregular-shaped fillers, while a spherical filler can be in contact with adjacent particles with one type of contact as shown in Figure 2-2a. We will discuss this further in Section 2-5.

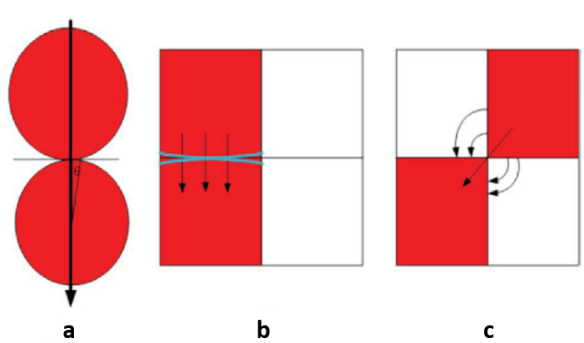

Figure 2-2: Different types of filler contacts, (a) filler contact between spherical particles (b) irregular-shaped face-contact, (c) irregular-shaped edge-contact [32].

Different types of contacts between fillers lead to different percolation thresholds. In [36] three phases for percolation level including 1) fully, 2) nearly, and 3) further lower percolated cases were considered and studied.

Figure 2-3 shows $J(E)$ characteristics of the ZnO-microvaristors samples with filler concentrations of 35%, 39%, 43%, 47% vol. According to Figure 2-3, the higher the filler concentration, the smaller the value of the switching field.

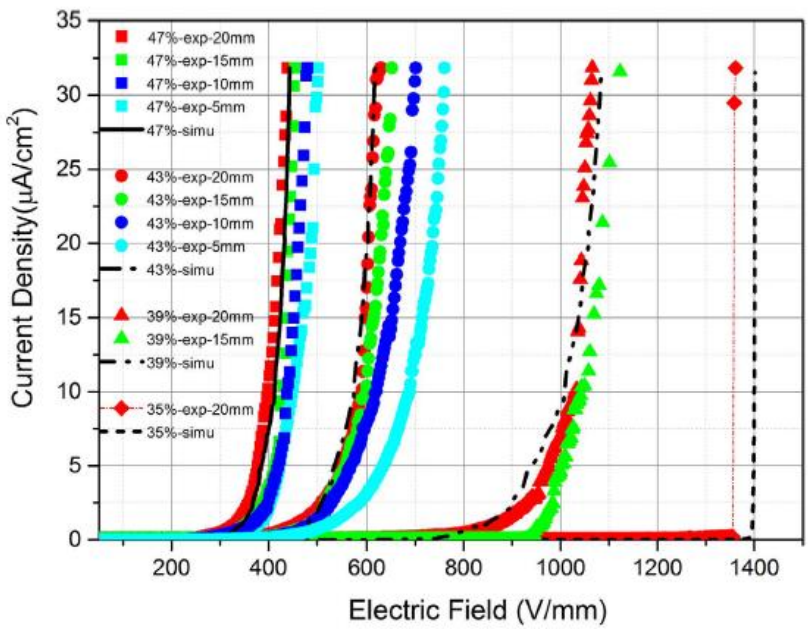

Figure 2-3: Nonlinear $J(E)$ Characteristics of ZnO-microvaristors samples with different filler concentrations [36].

To explain this, note that the conduction current flows in the composite through the filler particles already aligned and contacted fully or partially with their adjacent particles. These aligned particles form a path called "conduction path" in the composite, which can be straight or curved. The more straight ahead of the path, the larger current flowing through the material. Figures 2-4a and 2-4b show an image of ZnO microvaristor samples

with 47% vol taken by scanning electron microscope (SEM) imaging and its simulated picture obtained by the Voronoi Network simulation [36], respectively. The red line in Figures 2-4a exhibits the conduction path in the composite generated by aligning the filler particles. As seen from the picture, the conduction path is pretty straight, so the current through this path would be substantial.

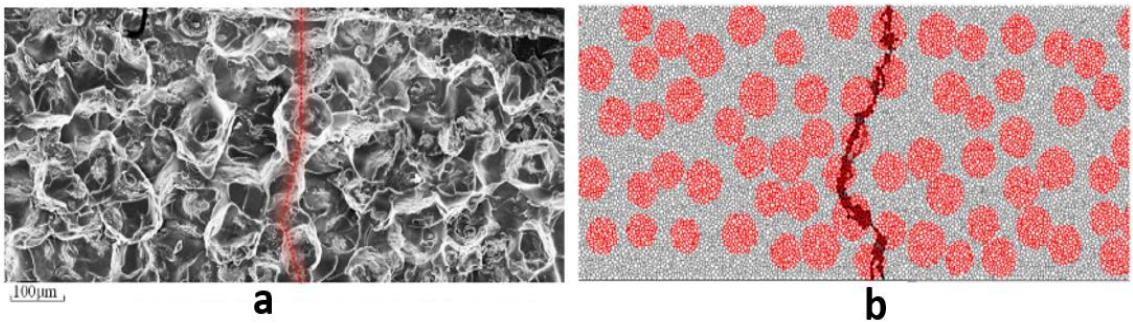

Figure 2-4: (a) SEM image, (b) the conduction path obtained by Voronoi network simulation of a ZnO-Microvaristor composite with the 47% vol filler concentration [36].

2.2.1 Fully Percolated Cases

In a fully percolated case, due to the high concentration level of fillers, the distance between filler particles becomes very low since most of the particles are almost in direct contact with each other. Therefore, several conduction paths are formed in the composite, and the probability of forming short paths becomes high. In other words, the conduction current has many choices of short paths to flow, and this results in the low switching field of the sample. So by increasing the filler concentration in the composite, the switching field decreases accordingly. Moreover, it has been shown that by raising the percolation level, the conduction path becomes more straight ahead. Figure 2-5 presents the SEM images of possible conduction paths in samples with different filler concentrations of 47%, 43%, and 39% vol all categorized as fully percolated cases [36]. The conduction path of the samples with a lower level of percolation is more curved. The reason is that for a low concentration

of fillers, the average distance between particles is large, and the filler particles are blocked more by the insulator matrix. Therefore, the conduction path may be formed after much curving, making it very lengthy.

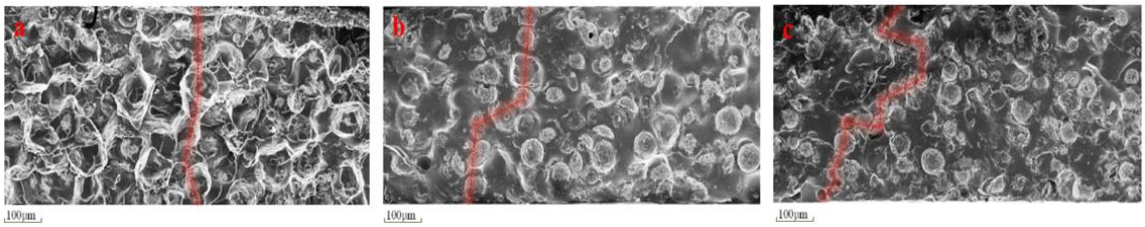

Figure 2-5: The SEM images and possible conduction paths for the samples with filler concentration of (a) 47%, (b) 43%, and (c) 39% [36].

2.2.2 Near Percolated Cases

Seen from Figure 2-3, the behavior of the $J(E)$ curve for the 35% vol, considered as a near percolated case, is different from others. While its switching field value is the largest among all the others, its $J(E)$ reaches the maximum current density very fast. This $J(E)$ characteristic indicates that a partial breakdown has occurred in the composite. When the filler concentration in the composite is not high enough, a thin layer of silicon rubber fills out the free spaces between the filler particles. So the conduction path in the composite is clogged by the silicon rubber at some locations. Based on the voltage division rule for two resistors in series, since the resistivity of the filler particles in the composite at sufficiently high electric fields owing to the nonlinear nature of the filler particles is much lower than that of silicon rubber, a higher voltage allocates to the silicon rubber layer, leading to breakdown and puncture of it. Consequently, due to the short circuit of that insulation layer, the current flowing through the composite increases, and the $J(E)$ reaches its maximum very quickly.

However, this is not the end of the story. The $J(E)$ characteristics of the 35% sample right after the first partial breakdown mentioned above presents the same nonlinearity as the samples with the lowest switching fields. It can be explained through the fact that the silicon rubber layer has been short-circuited, shortening the conduction path and, in turn resulting in a lower switching field value of the composite. Figure 2-6 shows the SEM image of the 35% vol sample right after the first partial breakdown, where the line in yellow is the short-circuited part.

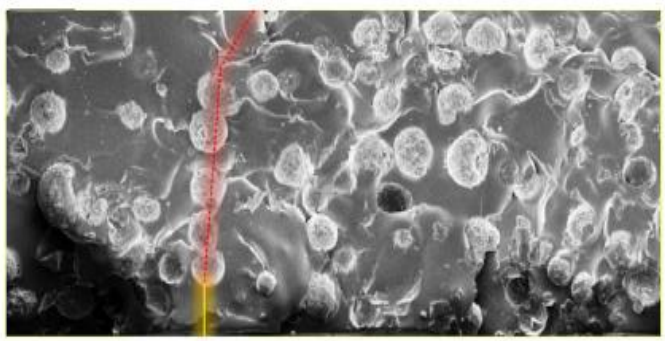

Figure 2-6: The SEM image and conduction path for the sample with 35% filler concentration after the first partial breakdown [36].

2.2.3 Further Lower Filler Concentration Below Percolation

For a composite with a shallow concentration of filler, e.g., 30% vol, the partial breakdown in the silicon rubber is much severe than that in the near percolated cases. The silicon rubber layer is much thicker between the filler particles, and the conduction path formation is very hard in the composite. Because of the thick layer of the insulation matrix between the filler particles, the electric field sufficient to puncture the layer must be very high. For these cases, the $J(E)$ characteristic of the composite right after the first partial breakdown is almost linear, and no nonlinearity feature is observed. It means that the partial

breakdown of the silicon rubber has been severe so that many conduction paths have been generated and the composite has been converted to a conductive material.

2.3 The Influence of the Electrode Area on the Switching Field

The influence of the electrode cross-section on $J(E)$ characteristics of the samples with different filler concentrations have also been investigated in [36]. Generally, by increasing the cross-section of the electrodes e.g., plane-plane electrodes compared to needle-plane electrodes in contact with a sample, the number of conduction paths increases significantly. Apart from generating more conduction paths in the sample with electrodes with a larger area, the shape of conduction paths becomes more straight ahead. As a result, the conduction current can find the shortest path among plenty of the short path choices in the sample to flow, and the switching field decreases accordingly.

However for a sample with high percolation level, e.g., 47% vol, the electrode area effect on the switching field value is minor, because of many conduction paths already formed in the sample owing to the high level of filler particles, and the number of conduction paths is sufficient under even small electrode areas. In contrast, the situation is different for the samples with a lower level of filler concentration, e.g., 39%, where due to not being enough conduction paths in the composite, the electrode area plays a critical role in increasing the probability of shorter conduction paths formation. Therefore, at a low-level filler concentration in the composite, larger electrodes lead to shorter conduction paths and lower switching field.

2.4 The Influence of the Filler Size on the Switching Field

To study the effect of filler sizes on the switching field of the composite, four groups of different sizes of spherical and irregular-shaped microvaristors with a certain

percolation level of 46.5% vol were examined in [32]. The results show that the switching field value decreases significantly by increasing the filler sizes for both filler shapes. The reason is that for a given concentration, although the larger fillers lead to a fewer number of the filler particles, the formation probability of shorter and more conduction paths is higher, as shown in Figures 2-7c-f, leading to a smaller switching field as shown in Figure 2-7g.

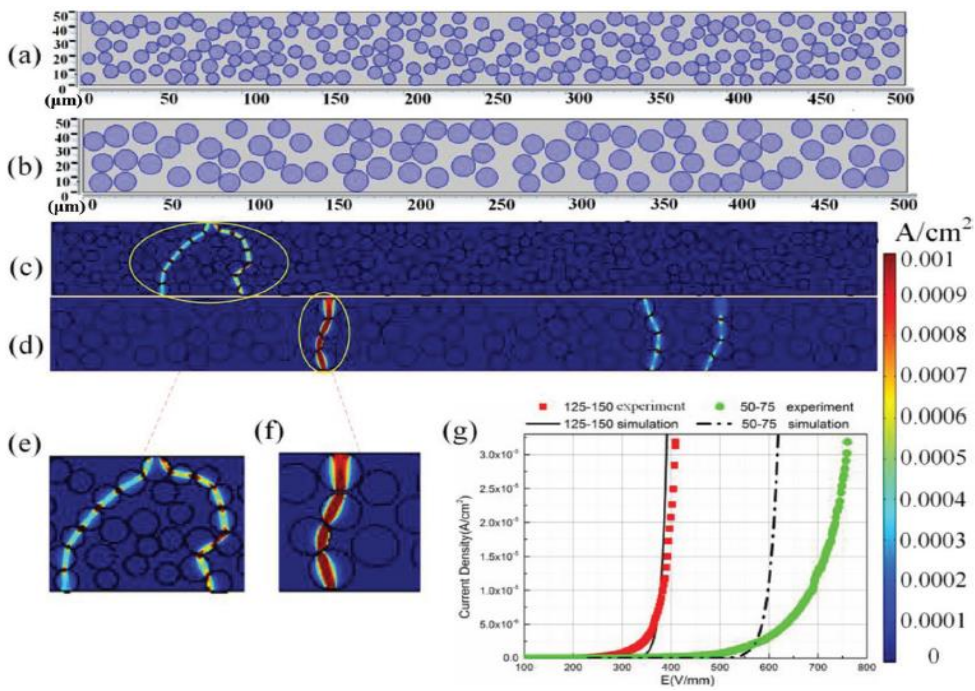

Figure 2-7: Sample with (a) small-size fillers, (b) large-size fillers; (c) and (d) calculated current density for (a) and b cases, respectively; (g) simulated and experimental results of $J(E)$ for two different diameters of fillers [32].

Seen from Figure 2-7g, there is not a good agreement between simulated and measured results of the $J(E)$ curve for the composite with fillers having a diameter in 50-75 μm range. As justified in [32], the reason is that the effect of the shape of particles was only considered in simulations, and the effect of contact resistance between particles, discussed in detail in Section 2.5, was ignored.

2.5 The Influence of the Contact Resistance on the Switching Field

Figure 2-2 illustrates the different contact types for irregular, estimated by square, -shaped particles and spherical-shaped particles. The contact resistance for spherical-shaped particles can be formulated by Hertzian contact stress. In 1882, Heinrich Hertz analyzed and formulated the localized stresses that develop as two curved surfaces come in contact and deform slightly under the imposed loads. When two spherical bodies come in contact, they initially are in touch with each other at a single point. By exerting a very small force on the bodies, due to the elastic deformation, the bodies are squeezed into each other and a contact area with radius "a" is formed as shown in Figure 2-8a. To apply Hertz analysis, the following assumptions must be considered:

1- The body surfaces must be perfectly smooth, frictionless, and continuous.

2- The size of the bodies has to be much larger than that of the contact area.

3- Each body can be modeled as an elastic half-space at the contact area.

Suppose that spheres 1 and 2 in Figure 2-8a are perfectly smooth and in contact with each other. Then the contact moduli of two materials contacting each other, E^*, is given by

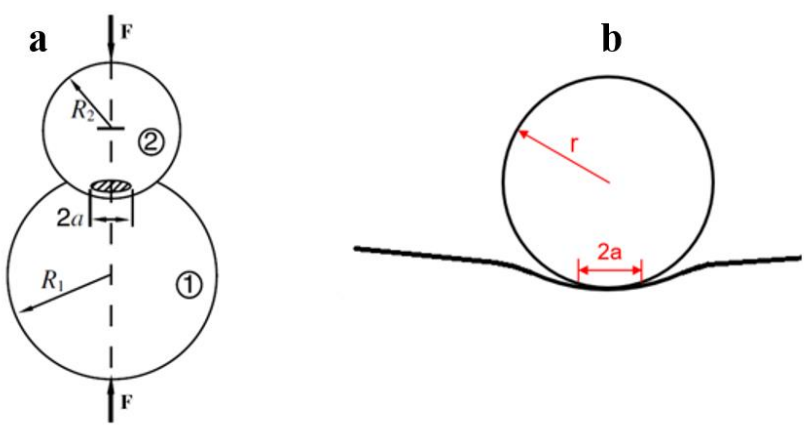

Figure 2-8: (a) Sketch of two adjacent filler particles [37], (b) A protrusion of one filler particle in contact with a flat surface of another [38].

$$\frac{1}{E^*} = \frac{1-\vartheta_1^2}{E_1} + \frac{1-\vartheta_2^2}{E_2} \qquad (2-1)$$

where E_1 and E_2 are the elastic moduli and ϑ_1 and ϑ_2 are Poisson's ratios associated with each body.

In the case of particles with the same material, both elastic moduli and Poisson's ratios are equal ($E_1 = E_2 = E$ and $\vartheta_1 = \vartheta_2 = \vartheta$). Thus, (2-1) becomes:

$$\frac{1}{E^*} = 2\left(\frac{1-\vartheta^2}{E}\right) \rightarrow E^* = \frac{E}{2(1-\vartheta^2)} \qquad (2-2)$$

The equivalent radius of two spheres with radiuses of R_1 and R_2 is

$$\frac{1}{R_e} = \frac{1}{R_1} + \frac{1}{R_2} \rightarrow R_e = \frac{R_1 R_2}{R_1 + R_2} \qquad (2-3)$$

If the contact between particles arises as a protrusion of a particle and the flat surface of the adjacent particle (Figure 2-8b), then $R_2 \rightarrow \infty$ and by setting $R_1 = r$, we have

$$R_e \cong R_1 = r \qquad (2-4)$$

The pressure distribution formulated by Hertz for this contact situation (Figure 2-8b) is:

$$P(r) = P_0\left(1 - \frac{r^2}{a^2}\right)^{\frac{1}{2}} \qquad (2-5)$$

where P_0 is the maximum pressure at the contact point of the two bodies. The load and pressure are related to each other through $F = P/A$, where A is the cross-section area where the load is applied to it. Therefore, the total load on the circular cross-section would be:

$$F = \int_A P(r)\, ds = \int_0^a P_0\left(1 - \frac{r^2}{a^2}\right)^{\frac{1}{2}} (2\pi r) dr = \frac{2}{3} P_0 \pi a^2 \qquad (2-6)$$

Thus, the maximum pressure can be derived by

$$P_0 = \frac{3F}{2\pi a^2} \qquad (2-7)$$

The radius of the contact area can be determined by [39]:

$$a = \frac{\pi P_0 r}{2E^*} \qquad (2-8)$$

By inserting P_0 from (2-7) to (2-8) and solving for a, we have

$$a = \frac{\pi r}{2E^*} \cdot \frac{3F}{2\pi a^2} \rightarrow a = \left(\frac{3Fr}{4E^*}\right)^{\frac{1}{3}} \qquad (2-9)$$

By replacing E^* from (2-2), the radius of the contact area will be

$$a = \left(\frac{3Fr(1-\vartheta^2)}{2E}\right)^{\frac{1}{3}} \qquad (2-10)$$

The elastic force between particles can also be determined by

$$F = \frac{2}{3} \cdot \frac{E}{(1-\vartheta^2)} \cdot \frac{a^3}{r} \qquad (2-11)$$

The contact resistance at the area with radius a between two particles, R_c, is given by [40]:

$$R_c = \frac{\rho_T}{2a} \qquad (2-12)$$

where ρ_T is the bulk resistivity of filler grains. By solving (2-10) and (2-12) for a, the contact resistance becomes:

$$R_c = \frac{\rho_T}{2a} = \frac{1}{2}\rho_T \cdot \left(\frac{2E}{3Fr(1-\vartheta^2)}\right)^{\frac{1}{3}} \qquad (2-13)$$

According to (2-13), the contact resistance increases by decreasing the protrusion radius, r, i.e. for smaller particles. As shown in Figure 2-9, for a given conduction path, the path formed by more and smaller particles will have more contact interferences compared to the one with less and larger particles, leading to higher total resistivity and consequently higher switching field of the composite, see Figure 2.1.

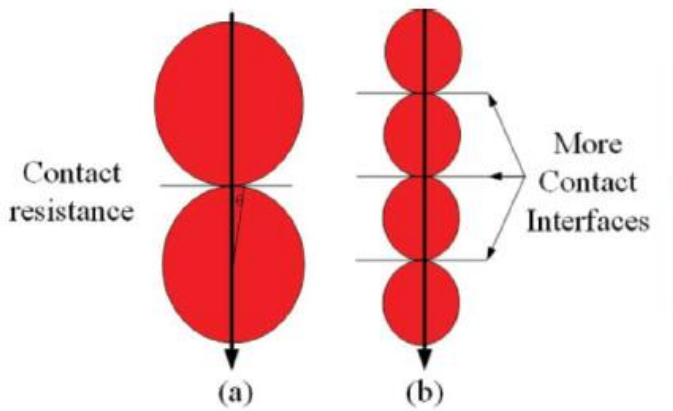

Figure 2-9: Contacts among spherical filler particles with (a) large diameter, (b) small diameter, for the given conduction path [32].

Besides filler size, filler concentration affects the contact resistance as well. An increment percolation level of filler in the composite leads to the lower contact resistance and the switching field value of the composite. The reason is due to the shorter and more straight ahead conduction paths at higher percolation levels. A shorter path involves fewer particles; thus there are fewer contact interfaces in the path, and in turn, total resistivity and switching field will be smaller, as seen in Figure 2-3.

For irregular-shaped filler particles, since the surface of the particles is not perfectly flat, the contact resistance between particles with the face-contact type can be described by (2-13). However, this is not the case for the edge-contact type. Seen from Figure 2-2c, in the edge-contact case, some parts of current flowing in the conduction path will pass through the insulator to reach from a filler to another. Therefore, the insulator conductivity must also be taken into account as given by (2-14) [41]:

$$\sigma_{eff} = \sqrt{\sigma_c \sigma_i} \qquad (2-14)$$

where σ_{eff} is the effective conductivity of the composite, and σ_c and σ_i are the conductivity of the filler particles and insulation matrix, respectively. Since $\sigma_c \gg \sigma_i$, the resistivity of a

composite with irregular-shaped filler particles having an edge-contact type is much higher than that of spherical-shaped particles, leading to a higher switching field as seen in Figure 2-1.

Chapter 3

Electric Field Grading in High Voltage High-Density Wide Bandgap Power Modules via Combined Geometrical Techniques and Applying Nonlinear Field Dependent Conductivity Layers

3.1 Introduction: Structure of A Power Module, Explaining the Problem, and Background

Figure 3-1a displays a side-view representation of an IGBT or diode with active metal brazing (AMB). Encapsulating materials and ceramic substrate are the primary constituents of a conventional power device packaging. The key role of the ceramic substrate in the insulation system is electrically isolating the area in between the HV electrode (semiconductor chip) and the ground electrode (e.g. base plate made of copper or AlSiC) attached to the heat sink. To facilitate heat transmission to the heat sink from HV components, the ceramic substrate which can be usually AlN, Al_2O_3, or Si_3N_4 is metalized by copper at both sides. semiconductor devices and base plates are attached to the metalized ceramic substrate where the blocking voltage is applied across. To reduce the risk of electrical discharges in air and preserving the embedded component against environmental impacts, the power module's final arrangement is immersed in silicone gel.

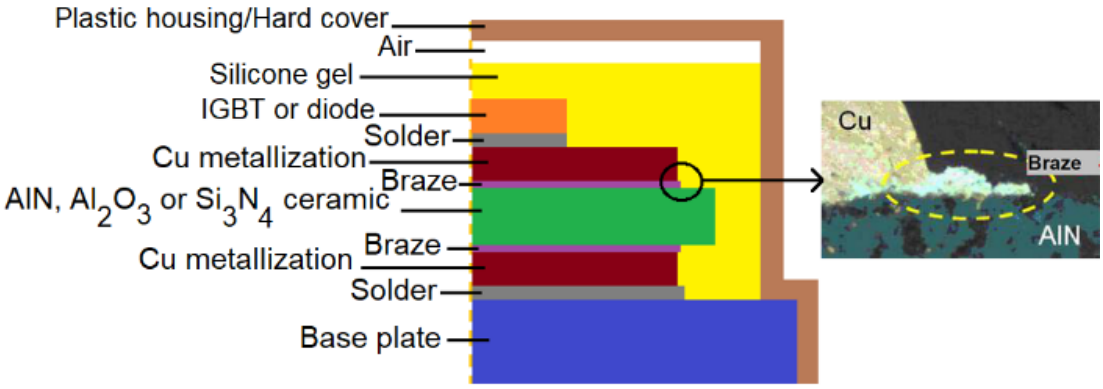

Figure 3-1: (a) Schematic of an IGBT or diode substrate; (b) Protrusions with extremely sharp edges of brazing below the metallization layer.

Owing to the high electric fields in particular at the edges of the copper metallization known as triple points where the ceramic substrate, copper electrode, and encapsulation material meet together, PDs can be initiated from these regions. The worst situation is protrusions with extremely sharp edges of some braze below the metallization in AMB as shown in Figure 3-1b.

To date, several field grading techniques have been proposed which can be classified as four main categories: 1) geometrical methods [42-46], 2) Coating the high-stress zones with nonlinear field-dependent conductivity (FDC) materials [47] or "field-dependent permittivity (FDP) fillers in silicone gel" [48], 3) utilizing high-temperature (up to 350°C) insulating liquids alternatives to conventional silicone gels [49-51], and 4) accompanying geometrical techniques and implementing nonlinear field-dependent conductivity composites [52-58]. The fourth solution has been developed in this Ph.D. work.

Typically, FDP composites are formed through the inclusion of a ferroelectric filler,

barium titanate, to a polymer base (silicone gel) [48]. Nevertheless, the field grading merit of this method is restricted by its two inherent limitations, in particular, in WBG power modules. First, at temperatures exceeding a threshold known as the “Curie point” (∼130°C for pure “barium titanate”), the stress-relieving advantage of this technique vanishes [48]. Despite the higher Curie point in composite with FDP fillers than the “maximum junction temperature” of “Si-based semiconductor devices” (~150°C in Si-IGBT, and ~ 125°C in diodes) [48], efficacity of this technique for stress grading in WBG power devices with far higher operating temperature- So far is 200°C owing to the silicone gel limiting operating temperature- drops noticeably. Another weak point of this technique is an extreme increase in the viscosity of the composite with a rise in the filler rate- about five times increase in a filled composite with 15% barium titanate by volume [48]. Although this 15% barium titanate filled composite can still be well-poured in the power module [48], due to the challenges associated with high viscosity, the rates above 15% by volume of “barium titanate” cannot be utilized in the power modules. It is crystal clear that this method has a critical thermal limitation for use in WBG-based power modules where the temperatures may increase up to 200°C.

Despite the greater dielectric strength of the non-polar dibenzyltoluene (DBT) liquid, Jarytherm® DBT encapsulant, proposed in [49-51] for being utilized in "high-temperature power electronics modules" in comparison with other “liquid dielectrics” such as " mineral oil” or “esters" at 20°C, at elevated temperatures, say 350°C, its dielectric strengths drop by 58% of its value at 20°C.

However, PD measurements in [51] show promising results for these high temperature liquids as an alternative for silicone gel. To the best of our knowledge, there

are only three papers [49-51] (all are conference papers) proposing DBT as an alternative for silicone gel for high-temperature WBG power modules. The low number of papers on this topic and their publication year (2018, 2019) indicates that this topic is very immature.

Despite many years of using "nonlinear FDC materials" also known as nonlinear resistive stress-relieving materials in "form-wound machines" and in "cable terminations" [30, 31, to cite a few], the implementing feasibility of these materials as electric field grading in power modules were first introduced in [47]. Nevertheless, they have not been put into effect in power modules up to now.

The geometrical approaches for electric field mitigation in power modules include “1) metal layer offset [42, 43], 2) protruding substrate [42, 44], 3) stacked substrate [45], and 4) 3D module layers [46]”. However, the “3D module layer" technique results in an increment of 20% in "stray inductance" [46].

In this chapter, it is demonstrated that " the enhanced electric field issue within high voltage high power-density WBG power modules cannot be addressed by either individually or combined geometrical modifications such as 1) metal layer offset, 2) protruding substrate, and 3) stacked substrate design". Subsequently, for the first time, we demonstrate that a combination of the above-stated “geometrical” approaches and utilization of a “nonlinear FDC composite layer” can sort out the issue and fulfill both the "one-minute insulation” and “PD tests” based on “IEC 61287-1”.

3.2 A Criterion for Permissible Maximal Electric Field Intensity Within Power Modules

The silicone gel/substrate Interfaces [59, 60], voids within the silicone gel [61], and pores presenting in sintered ceramic "AlN" or "Al_2O_3 substrates" [62] are the most widespread postulations regarding the origin of PDs in the modules. We believe that PDs may arise from all aforesaid sites. Typically, the electric stress magnitude has a great impact on PD intensity. Our proposed criterion for insulation design has been carried out based on the calculated maximum electric field intensity within the ceramic substrate and silicone gel at a given (1) "partial discharge inception voltage (PDIV)" and (2) "the dimensions of a power module". The cross-sectional view of an "industrial metalized AlN substrate" incorporating the accurate shape and size of the "protrusion" and "metallization layer" is illustrated in Figure 3-2 [44]. Based on the given dimensions and scale presented in Figure 3-2, a "finite element method (FEM)" model was developed in "COMSOL Multiphysics".

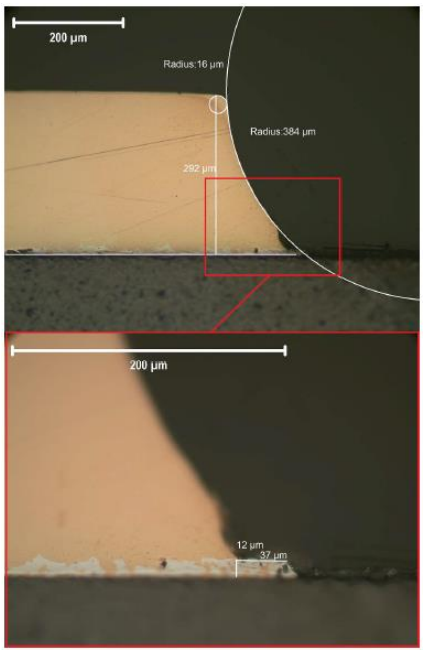

Figure 3-2: Cross-section of an industrial substrate with protrusion [44].

According to the PD test results provided by the researchers at the "LAPLACE laboratory

(Paul Sabatier University, Toulouse)" for an industrial substrate consisting of a 1 mm-thick "AlN substrate", the PDIV value was 4.7 kV at 10 pC under AC 50 Hz applied voltage [44]. According to "IEC 61287-1", the maximum allowed level for PD of a power module during the PD test is 10 pC. This signifies that the maximum acceptable value of E in both the ceramic substrate and encapsulation can be obtained and employed as a "design criterion" for electrical insulation. In other words, if the E_{max} in "AlN" and "silicone gel" for any "WBG module packaging" design is below the calculated maximum, in this case, the detected level of PD is less than "10 pC", for the same material characteristics and manufacturing process of "conventional modules" will be applied in "WBG modules".

Due to the remarkable advances in "WBG semiconductor industry", it is expected that the insulation materials of envisaged "WBG power modules" will be exposed to "high frequency (a switching frequency up to 500 kHz)", "fast (a dv/dt up to 100 kV/µs) square wave voltages" which may lead to a dissimilar "aging" state from when they subjected to a "50/60 Hz AC voltage". Nevertheless, as IEC 61287-1 is the only existing standard to assess PD activities level within power electronic modules under 50/60 Hz AC voltages, this chapter presents a benchmark for designing the next-generation WBG power modules insulation system based on this on hand criterion. Figure 3-3a illustrates the obtained electric field distribution by COMSOL Multiphysics at $t = 5\ ms$ (voltage peak) and under $V = 4.7\sin(100\pi t)$ kV. The thickness of the metallization layers at both sides of the substrate has set to 292 µm.

The "perfectly sharp edges" of metallization layers were properly arched to avoid theoretically infinite calculated values for electric stress at those areas. Another challenge while dealing with electric field calculations via the finite element method is the strong

dependency of E values on mesh size. To tackle this issue, two approaches were adopted in this manner: 1) Three meshing zones, as presented in Figure 3-3b were assigned to the whole model. While "zone 1" with an extremely high-resolution meshing with a maximum element size of "2 µm" is incorporated all sharp edges, the remaining regions are defined under "zones 2 and 3" with the maximal element size of "40 µm" and "400 µm", consecutively. 2) E measurements were performed on two cutlines (L1 and L2 in AlN and silicone gel, respectively) which have been illustrated in Figure 3-3a, and each has a 15 µm distance to the HV boundaries. A combination of mentioned strategies leads to an accurate E calculation at the desired points as the variation between the derived E values is less than 1% for the assigned mesh size and smaller. The maximum values of E (E_{max}) measured on line "L1" and "L2" are "15.98 and 17.48 kV/mm", respectively. The Calculated E_{max} values will be our "criterion" for the "electrical insulation design" of "envisaged WBG power modules" to fulfill the PD test requirement (<10 pC). The "relative permittivity" of the silicone gel and AlN substrate which were used in electric field simulations were set to 2.5 (Wacker Elastosil RT 754 mentioned in [44]) and 9 [44], respectively. Also, their "electrical conductivities" were considered as "10^{-11} and 10^{-13} S/m", respectively.

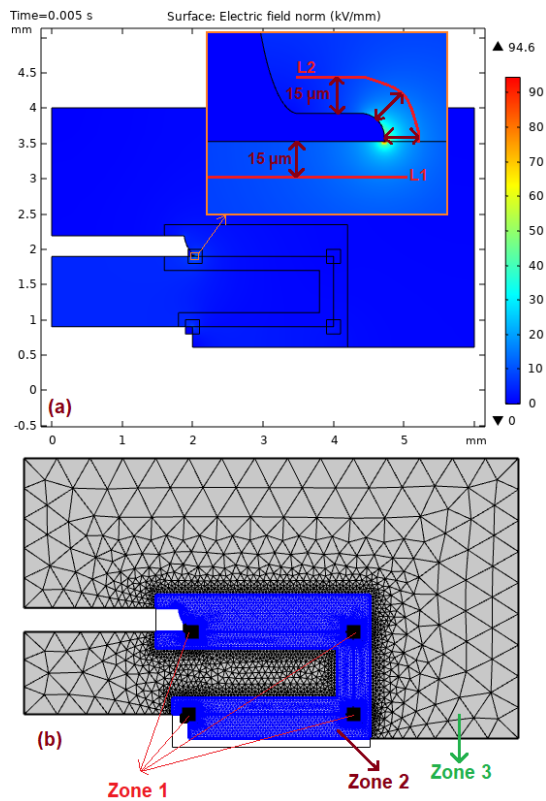

Figure 3-3: (a) Electric field distribution for the geometry considered according to Figure 3-2 under a 4.7 kV (peak) AC 60 Hz voltage, (b) meshing strategy.

3.3 Modeling and Simulation Results for a High Density 25 kV WBG Power Module

3.3.1 Base Case

In this section, we demonstrate that for a "high-density WBG power module" with a "blocking voltage" of 25 kV, the measured E values (on "L1 and L2") are greater than those evaluated as a "criterion" in Section 3.2. As such, to deal with the problem, several electric field mitigation methods are developed and elaborated in the following sections. As specified by "IEC 61287-1", the "power module" should satisfy the criteria for the "one-minute insulation test" where an AC voltage with an RMS value of $V_{rms} = \left(2U_b/\sqrt{2} + 1\right)$ kV (U_b(kV): blocking voltage) is applied to the substrate. Thus, for a 25 kV-power module,

an ac voltage with an amplitude of $V_{ac,max}$= 51.41 kV is applied to the module during the test. There is a mismatch between the information on the dielectric strength of the AlN substrate form the manufactures datasheet and through experimental measurements [63, 64]. The average dielectric strength of metalized AlN substrate supplied by different companies measured in [63] is roughly 20-30 kV/mm at 20°C under AC voltage. For instance, the "dielectric strength" of AlN1 and AlN2 provided by two manufacturers datasheets were "16 and 14 kV/mm", respectively [64]. Though, at 25°C and under AC voltage, the extracted values of dielectric strength for AlN1 and AlN2 samples were "31-41 kV/mm" and "33-36 kV/mm", respectively [64]. Another key point from the experimental results is that both AlN1 and AlN2 samples present a nearly stable dielectric strength within the temperature range of "room temperature" to "200°C". However, at temperatures above 200C, dielectric characteristics of the samples are not following the same pattern. While dielectric strength magnitude of AlN1 remained constant, that of AlN2 dramatically increased with temperature. All in all, based on the discussion above, a value of 25 kV/mm seems a reasonable choice for the dielectric strength of AlN covering all the test results in both references. Considering the above-stated value for AlN dielectric strength, we can calculate the minimum required thickness for AlN to endure the "one-minute insulation test" as 51.41/25=2.06 mm.

Based on IEC 61287-1 criterion for PD evaluations, the module should be biased with a "50/60 Hz AC voltage" with a maximum of "$1.5U_b$" for "one-minute (t_1)", that is followed by "an AC voltage" with a maximum of "$1.1U_b$" for "30 seconds (t_2)" duration. To pass the PD test, the maximum intensity of PD level must be less than 10 pC in the last 5 seconds of the cycle. To comply with the associated condition of PD measurement test

for simulations, while the bottom metallization layer is grounded, the top-metallization of the "ceramic substrate" is biased with a voltage of "1.1U_b=27.5 kV".

The new simulations have been carried base on the parameters and dimensions used in Section 3.2, excluding the AlN thickness and voltage applied across the module. E_{max} on "L1 and L2" are "63.36 and 69.8 kV/mm", respectively, that is far above the "criterion values" stated in Section 3.2. Here, multiple "geometrical techniques" as well as the implementation of "nonlinear FDC layer" have inspected to take E down to the "criterion values".

3.3.2 Geometrical Approaches

3.3.2.1 Metal Layer Offset

The "offset" of two "metallization layers" is described as $r_{off} = r_u - r_l$ where r_u and r_l presented in Figure 3-4a. Figure 3-4b depicts E_{max} upon "L1 and L2" illustrated in Figure 3-3a for a range of r_{off}. In Sections 3.2 and 3.3.1: $r_{off} = 0$, and in Figure 3-4a: "$r_{off} = 0.5$ mm". To generate various values of r_{off}: r_u is kept unchanging while r_l is varied. As represented in Figure 3-4b, descending r_{off} takes E_{max} down on either line as for r_{off}= –1.5 mm, E_{max} intensities on "L1 and L2" are "12% and 11%" less than that for "$r_{off} = 0$". Albeit, the measured E_{max} on both lines are yet much higher than the allowed levels defined in Section 3.2. Worth noting that increasing the length of the "top metallization layer" relative to the top one giving rise to negative amounts of r_{off}, which eventually has an adverse effect on the uniformity of the heat transfer in the module compared to $r_{off} = 0$ and may cause a "thermal issue". Accordingly, the maximum

admissible negative value of $r_{off} = -1.5$ mm is considered for the following investigations.

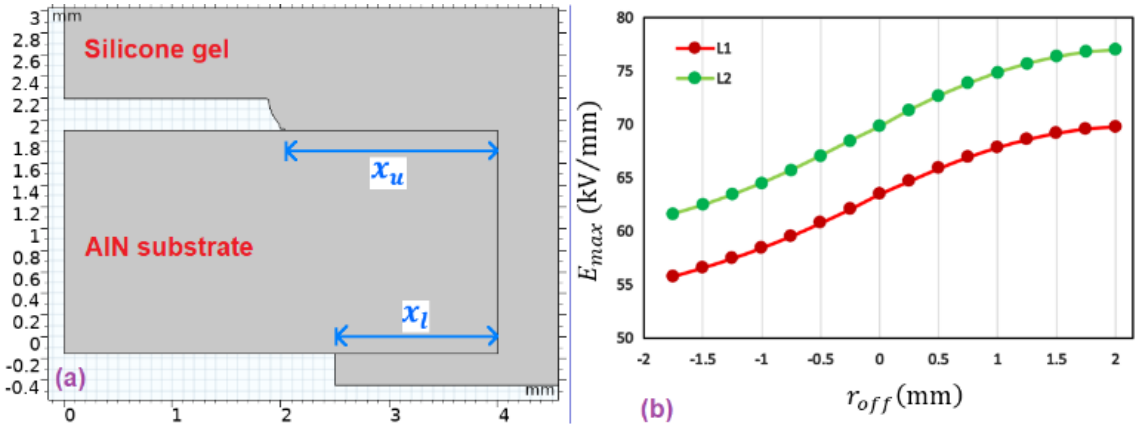

Figure 3-4: Influence of r_{off} on E_{max} for L1 and L2.

3.3.2.2 Protruding Substrate

The "protruding substrate design" illustrated in Figure 3-5a was developed in [44] where the "sharp edges" of 500 µm-thick metal layers were curved with a radius of R_c=250. Then, a "protrusion" with a height (h) and length (l) of 150 µm and 500 µm, respectively, were carved out of the AlN substrate. The metallization layers, afterward, were soldered on this "protruding substrate". Figure 3-5b represents the cross-sectional view of the "protruding substrate" fabricated by [44]. A picture of the "test vehicle" along with the substrate set for "dielectric testing" is depicted in Figure 3-5c.

Although the PDIV magnitude for the manufactured protruding substrate with no encapsulation incorporated within the module was greater than those for "industrial substrates" with "silicone encapsulation", the measured "PDIV" for "protruding substrates" by integrating silicone gel was turned lower than that of the "industrial substrate" [44]. This can be explained by either the low quality of the encapsulation material or of "encapsulant/substrate interface (e.g., trapped air bubbles or delamination of

the interface)" owing to inadequate "degassing", or presence of "contamination" at the surface of substrate. Consequently, as previously stated, as flawless and the most suitable manufacturing processing states and materials often cannot be attainable, experimental approaches for assessing and analyzing different electric field mitigation techniques often fail.

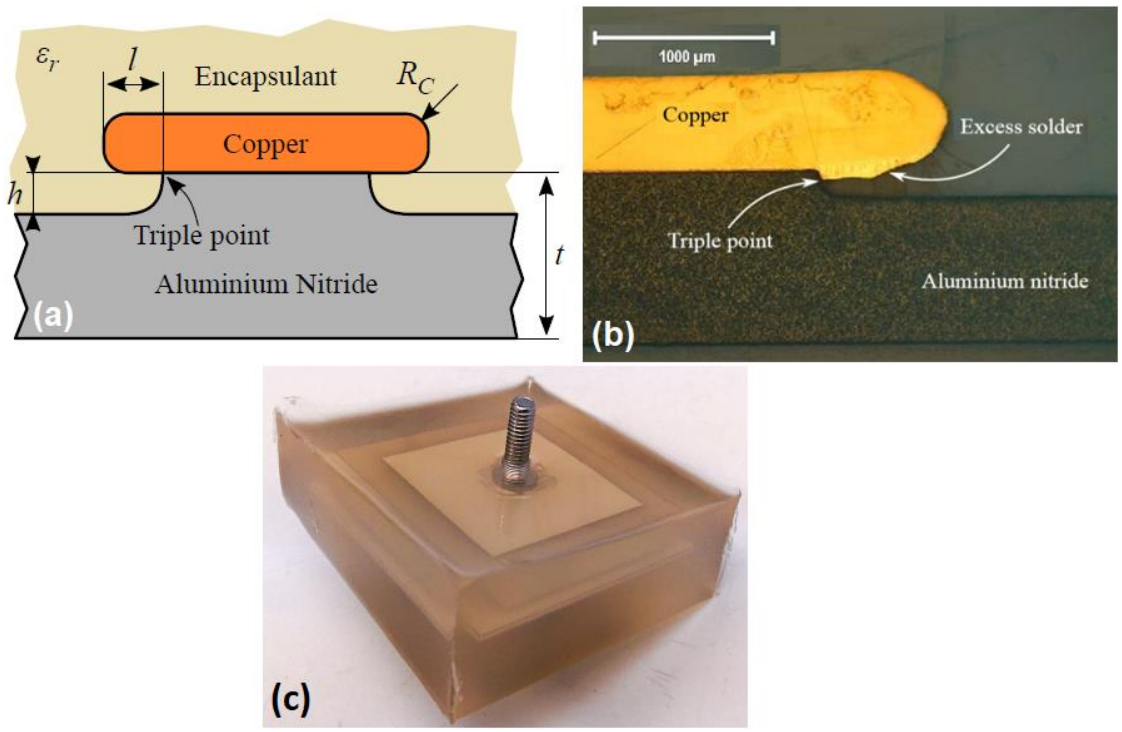

Figure 3-5: Protruding substrate [44].

Albeit E can be estimated for a wide range of the parameter values presented in Figure 3-5a, its manufacturing for all those parameters may not be feasible. Thus, we suppose that the "protruding substrate" fabricated in [44] can also be produced for our "base case" including a ceramic substrate made out of AlN with a thickness of 2.06 mm, displayed as t in Figure 3-5a. The geometry of the "protruding substrate" with the excess solder shown in Figure 3-5b is outlined in "COMSOL Multiphysics" and illustrated in

Figure 3-6a. The measured E_{max} on lines "M1 and M2" represented in Figure 3-6, are "30.32 and 67.71 kV/mm", respectively.

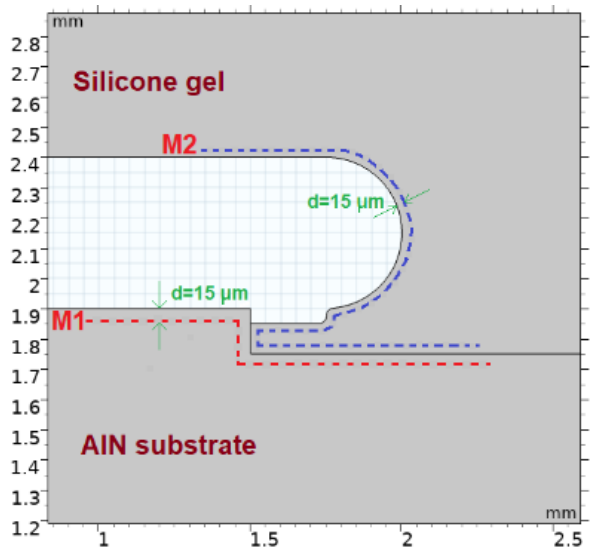

Figure 3-6: The geometry considered in COMSOL for protruding substrate.

All the points located on lines M1 (in AlN) and M2 (in silicone gel) to "HV electrode" or "AlN substrate/silicone gel interface" has a minimal distance of 15 µm. Remaining conditions e.g. applied voltage as well as the assigned mesh are kept in the same manner as those for the "base case" in Section 3.2. In contrary to the "base case", despite a 52% decrease in the value of E_{max} in the AlN substrate, a slight reduction of only 2% in the silicone gel was obtained. Accordingly, in both ceramic substrate and silicone gel, E_{max} are yet higher than the "criterion" values defined in Section 3.2.

3.3.2.3 Combined Metal Layer Offset and Protruding Substrate

By running "COMSOL Multiphysics" file in section 3.3.2.2 for $r_{off} = -1.5$ mm, the measured value of E_{max} on lines "M1 and M2" were "24.97 and 56.18 kV/mm", respectively, which are exceeding the criterion values, particularly in silicone gel. This was

the maximum decrease of E achievable by pure "geometrical techniques", and it is obvious that the enhanced electric field problem in the high power-density "WBG power modules" cannot be addressed by these approaches alone.

3.3.2.4 Applying Nonlinear FDC Coatings

In this section, a "nonlinear FDC" coating is applied to the high-stressed regions (protrusion and triple point) of the "base case" in section 3.3.1 as bridging the ground and HV electrodes. As mentioned before, "nonlinear FDC composites" can impact the electric field distribution based on their two key characteristics: the "switching field (E_b)" and "nonlinearity coefficient (α)", each of which can be controlled by regulating the "percolation level", size and shape of the fillers [32]. To obtain an efficient and "frequency-independent field-grade for a majority of applications, "$\alpha > 10$ and E_b should be equivalent to the ratio of the maximum applied voltage to the layer length" [47].

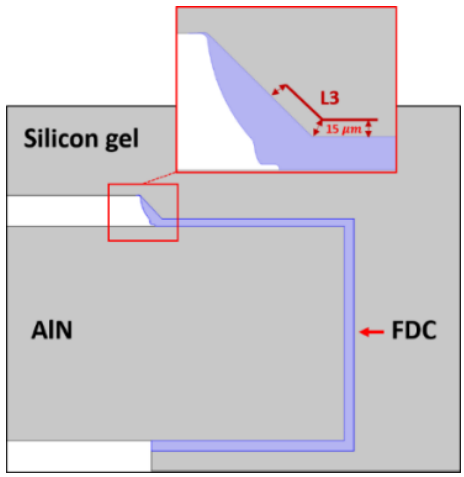

Figure 3-7: The geometry considered in COMSOL for the base case with applying a nonlinear FDC layer.

While the electric field intensity within "nonlinear FDC materials" exceeds a threshold value known as "switching field (Eb)", a significant amount of conduction

current flows through the layer which results in a notable electric-stress reduction in zones where the composite is applied on.

"The nonlinear FDC layer" can be applied to desired zones as "bridging" or "nonbridging". Since in the nonbridging case, the "top and bottom metallization" are not connected by the layer, the high field is shifted to the layer end. So, to settle this problem, a "bridging FDC layer" is recommended and used in this study. The conductivity (σ) of nonlinear FDC materials varies with E according to:

$$\sigma(E) = \sigma_0(1 + (E/E_b)^{\alpha-1}) \qquad (3-1)$$

"where σ_0 is the linear resistivity (σ_0=3.3×10^{-11} S/m), $E_b = V_{max}/L_{FDC} = 27.5\ \mathrm{kV}/6.07\ \mathrm{mm} \approx 4.5$ kV/mm, and $\alpha = 12$. The relative permittivity of the nonlinear FDC material is considered as $\varepsilon_r = 12$ [32, 47], and the nonlinear FDC layer thickness is set at 100 µm".

To compute E_{max} intensity in "AlN substrate", "nonlinear FDC layer", and "silicone gel", lines L1, L2, and L3 are defined. Lines L1 and L2 are located exactly at the places were described earlier in Section 3.2 and represented in Figure 3-3a while L3 placed in silicone gel and having a distance of 15 µm from the "FDC layer/silicone gel interface" is denoted in Figure 3-7. The calculated values of E_{max} on "L1, L2, and L3" are "22.57, 10.07, and 10.36 kV/mm", respectively. Relative to the "base case", a remarkable decrease in the value of E_{max} in the silicone gel were achieved as the acceptable level established in Section 3.2 was met. Nevertheless, in spite of a notable electric stress decline of "64.5% in the AlN substrate", it is yet slightly greater than the "criterion".

3.3.4 Combined Geometrical Techniques and Applying Nonlinear FDC Coatings

3.3.4.1 Considering Protrusions for Top Metallization Layers

As illustrated in Figure 3-8, in this section, a “nonlinear FDC layer” with a thickness of 100-µm is added as bridging to “HV metallization layer” and “triple point” of the “protruding substrate” investigated in Section 3.3.2.3. The electrical parameters of the “nonlinear FDC layer” (E_b, α, and ε_r) are kept just like those in Section 3.3.2.4. E_{max} is determined on the lines “M1, M2, and M3, where M1 and M2 are the same as those shown in Figure 3-6, and M3 shown in Figure 3-8, is at a distance of 15 µm from the interface of the silicone gel and the nonlinear FDC layer”. The calculated value of “E_{max} on M1, M2, and M3 are 14.65, 9.12, and 16.24 kV/mm, respectively”. In comparison with the results in Section 3.3.2.4, it can be seen that a combination of geometrical techniques ("protruding substrate and metal layer offset") and application of "a nonlinear FDC layer" can significantly mitigate the E_{max} in both substrate and silicone gel as the criterion described in Section 3.2 was fully met.

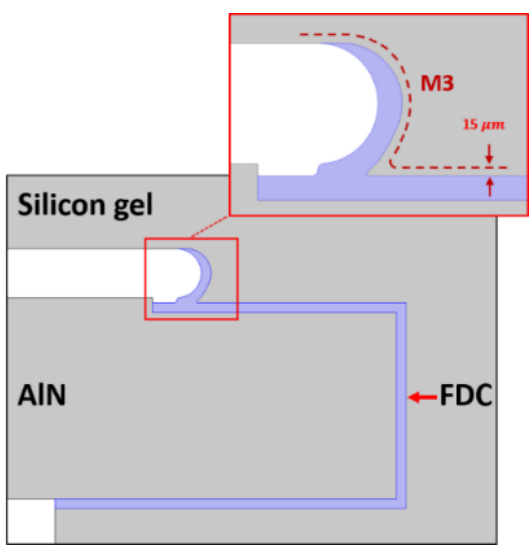

Figure 3-8: The geometry considered in COMSOL for a combination of a nonlinear FDC layer, protruding substrate design, and metal layer offset.

3.3.4.2 Considering Protrusions for Both Top and Bottom Metallization Layers: A More Realistic Situation

In the preceding sections, a "protrusion" was regarded for just the" top metallization layer" and it was demonstrated that by "combining geometrical techniques and applying a nonlinear FDC layer" as expressed in Section 3.3.4.1, the "criteria values" could be set out. In our simulations as yet, perfectly sharp edges were considered for the bottom metallization, and we were focused only on evaluating the E_{max} in the top-side areas of the substrate. However, the brazing of the metallization layer at the bottom side of the substrate could create a protrusion with remarkably sharp edges as well. In this section, a more factual situation is taking under consideration as a protrusion is assumed for both bottom and top metal layers, and then multiple field grading techniques are adopted to mitigate the high electric stress problem within the power module.

Thus, we need to update the "criterion values" developed in Section 3.2 for this new situation. The electric field distribution regarding the new geometry is illustrated in Figure 3-9 where the applied voltage, meshing strategy, and model dimension are kept the same as those in Figure 3-3 aside from taking a protrusion into account for the bottom metallization layer similar to that at the top-side layer. The E_{max} is evaluated on "L1 and L2" exhibited in Figure 3-3 and "L3 and L4" represented in Figure 3-9. The calculated E_{max} values for "the AlN substrate and silicone gel are 16.01 and 17.6 kV/mm", respectively. These obtained values are considered as our new "criterion values" for this section. Owing to existing a protrusion at the bottom side of the substrate, the determined E_{max} for this case is a bit greater than those calculated in Section 3.2.

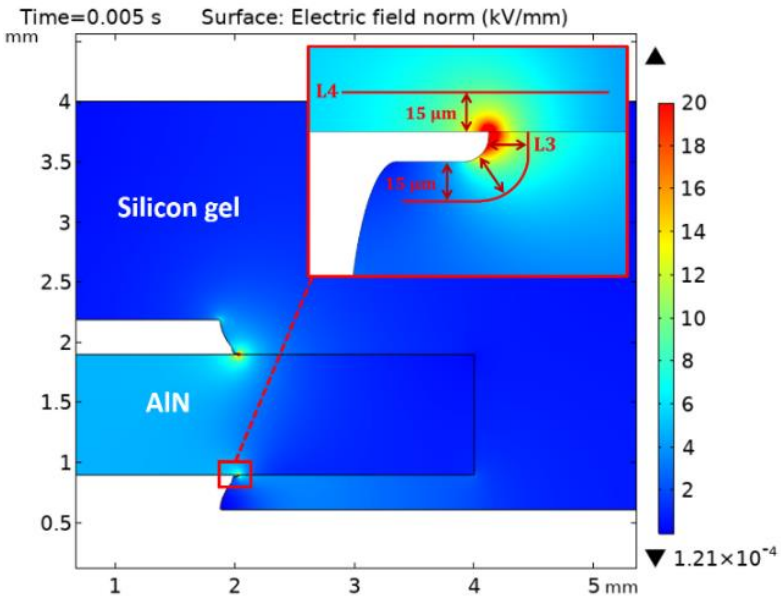

Figure 3-9: Electric field distribution for the geometry considered with a protrusion at both top and bottom metallization layers.

The base case condition in this section is exactly similar to that in Section 3.3.1 except for an extra protrusion at the bottom-side just like that for the top metallization layer. The obtained maximum electric stress value in this base case is 63.57 kV/mm in AlN substrate and 70.02 kV/mm in silicone gel. As mentioned earlier, the "protruding substrate" can decrease E_{max} in the "AlN substrate". Thus, the case examined in Section 3.3.2.4 is assessed by considering the geometry depicted in Figure 3-2 for the "bottom metallization layer". Figure 3-10a describes the electric field distribution in this case where "E_{max} in the AlN substrate and silicone gel is 34.31 and 67.91 kV/mm", respectively. In the "AlN substrate", E_{max} takes place on L3 illustrated in Figure 3-9.

Assuming the "protruding substrate design for both top and bottom metallization layers and r_{off}=-1 mm" as illustrated in Figure 3-10b, E_{max} in the "AlN substrate" and "silicone gel" drops off to "28.81 and 60.11 kV/mm", respectively. It is the maximum electric stress mitigation that could be attained via pure "geometrical techniques".

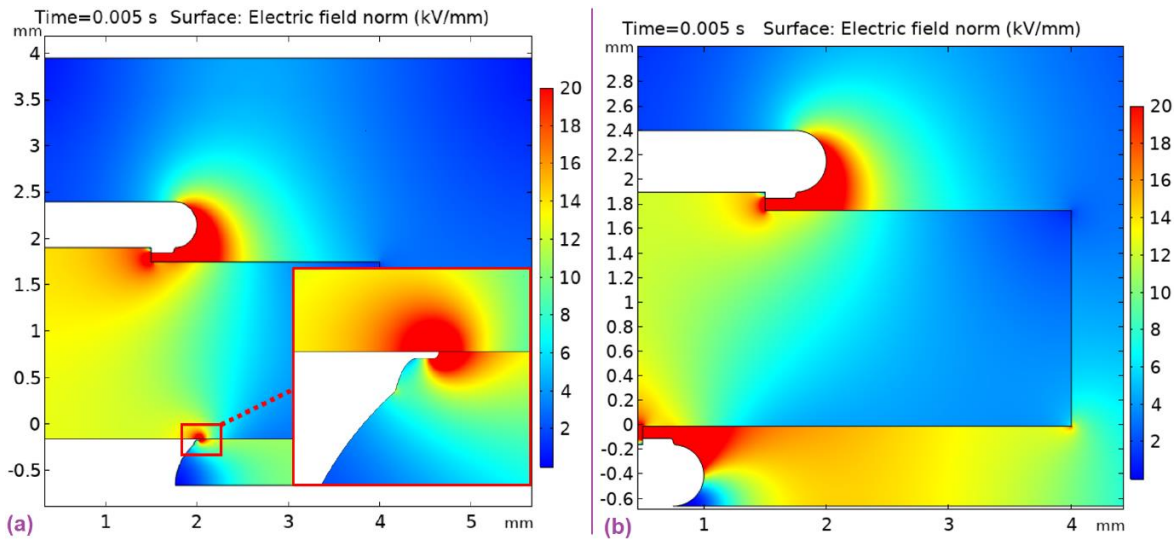

Figure 3-10: a) Electric field distribution for protruding substrate design for the top metallization layer and protrusion for the bottom metallization layer, b) Electric field distribution for protruding substrate design for both top and bottom metallization layers and r_{off}= –1 mm.

So as to comply with the "criterion values", the geometrical approaches are combined with a nonlinear FDC coating layer. Subsequently, as demonstrated in Figure 3-11a, a 100 µm-thick "bridging nonlinear FDC layer" and $E_b = 3.6$ kV/mm is inserted. In this regard, new measuring lines M4 - M6 are added to the former lines. The obtained E_{max} values for this configuration in the "AlN substrate", "nonlinear FDC layer", and "silicone gel" are 22.06, 7.44, and 20.46 kV/mm, respectively. In spite of the outstanding electric field mitigation, yet, it is greater than the "criterion values".

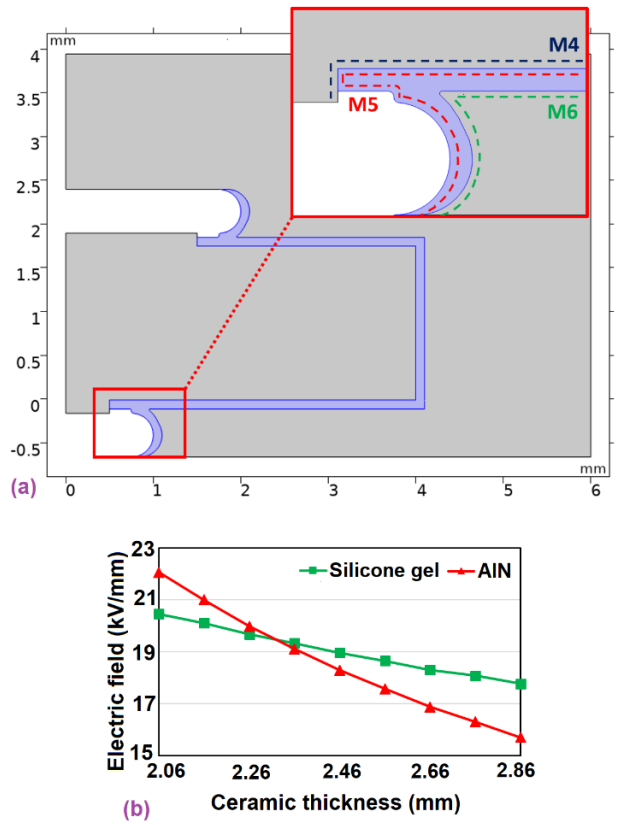

Figure 3-11: a) Geometry considered for a combination of applying a nonlinear FDC layer and both-sided protruding substrate design and r_{off}= -1 mm, b) E_{max} in AlN substrate and silicone gel vs. ceramic thickness.

In order to fulfill the "criterion values", the only way is to extend the thickness of the "AlN substrate". In order to do this for the case demonstrated in Figure 3-11a, the thickness of the "AlN substrate" was incremented in steps of 0.1 mm. The variation of E_{max} in the silicone gel and AlN substrate as a function of "ceramic substrate" thickness is represented in Figure 3-11b. Worth mentioning that, an increase in the thickness of the AlN leads to an extension in the "FDC layer length" as well and update the value of E_b. As presented in Figure 3-11b, for the "AlN substrate" with a thickness of 2.86 mm, E_{max} has met our criterion value. Nevertheless, E_{max} in the silicone gel (on M6) still need to be slightly graded as its value reaches to the determined criterion value.

In order to bring down the electric stress on M6, the gap between the "base plate" and "AlN substrate" has been fully covered by the "nonlinear FDC layer", according to Figure 3-12. By doing so, the evaluated E_{max} in the "AlN substrate" and "silicone gel" is 15.7 and 12.52 kV/mm, respectively, which fulfills the "criterion".

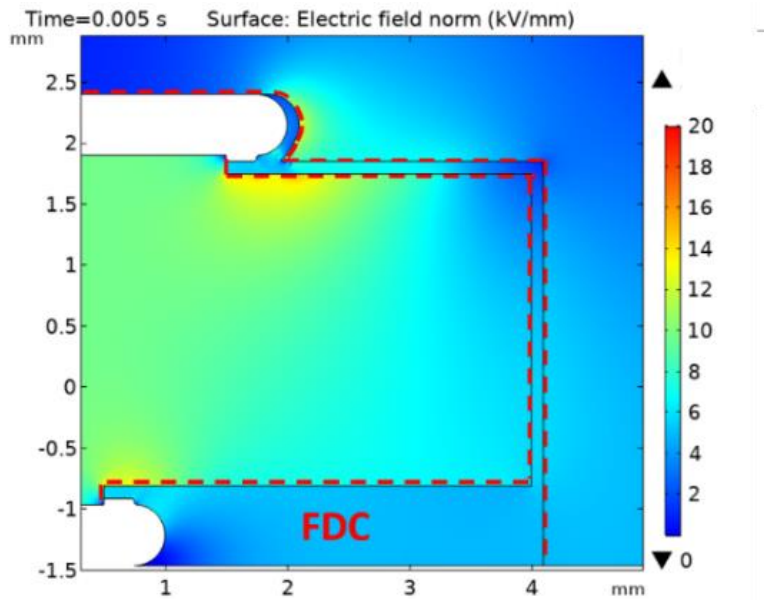

Figure 3-12: Electric field distribution for both-sided protruding substrate, r_{off}= -1 mm, AlN thickness=2.86 mm, and fully covered bottom region with nonlinear FDC layer.

3.3.4.3 Considering Stacked Ceramic Substrate

First introduced in [45], the "stacked substrate design" consisting of two or three "ceramic substrates" with a total thickness equivalent to one "ceramic substrate" are stacked. In Figure 3-12, to take E_{max} in "the silicone gel" down to the "criterion" value, the bottom-side zone of substrate was fully covered with "nonlinear FDC material". Rather than the method adopted in Figure 3-12, in this section, we investigate if the "stacked design" depicted in Figure 3-13a can resolve the issue. The only change applied to the structure illustrated in Figures 3-11a is a substitution of the single 2.86 mm-thick "AlN substrate" with two 1.43 mm "AlN substrates" and a 292 μm metallization layer in

the middle, Figure 3-13a. Furthermore, a voltage corresponding to the half of that across the "HV electrode" is applied on the middle metallization layer. Moreover, for the top- and bottom-side of the "middle metallization layer", two "protrusions", as demonstrated in Figure 3-13a, are considered with the dimensions described in Figure 3-2, and also new measuring lines M7-M9 were added.

In the "stacked substrate design", r_{off}^{*} is defined as the "offset between the middle metallization layer and the bottom layer". Thus, r_{off}^{*} = –3 mm shown in Figure 3-13a indicates that the width of the "middle metallization layer" and "AlN substrates" are equal. Thus, for the considered case, the evaluated E_{max} in the "AlN substrate" and "silicone gel" is "15.18 and 18.35 kV/mm", respectively. While in AlN substrate, E_{max} meets the "criterion", its value in the "silicone gel" is slightly higher. To deal with this issue, the E_{max} variation in silicone gel at different values of the r_{off}^{*} is illustrated in Figure 3-13b. Accordingly, as demonstrated in Figure 3-13b, E_{max} in both AlN and silicone gel meets the "criterion values" for r_{off}^{*} = -2.3 mm. As a result, There is no need for the "full coverage" of the bottom zone by "nonlinear FDC materials" anymore.

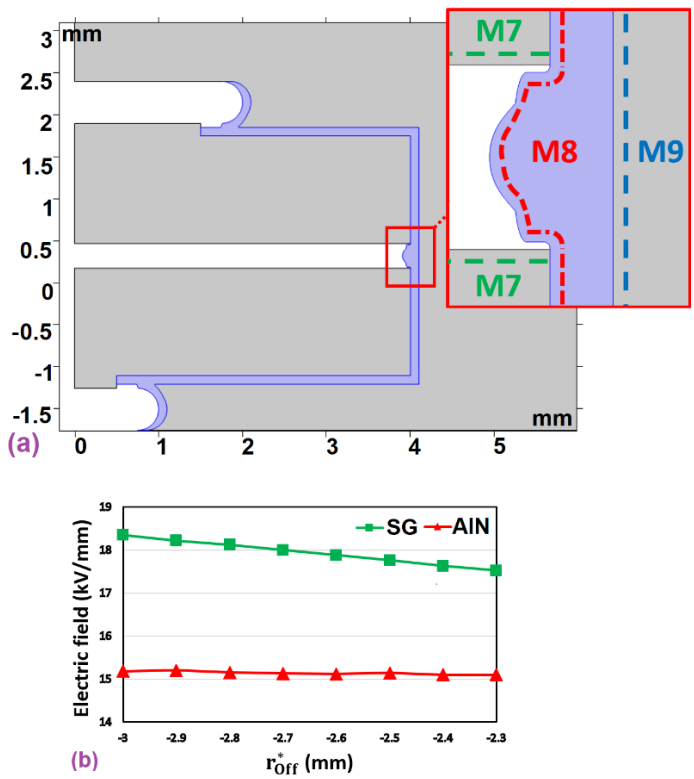

Figure 3-13: a) The geometry considered for a combination of applying a nonlinear FDC layer, both-sided protruding substrate, and stacked ceramic substrate design with r_{off}= -1 mm and r^*_{off} = −3 mm, b) E_{max} in AlN substrate and silicone gel vs. r^*_{off} .

3.4 Modeling and Simulation Results for a High-Power Density 30 kV WBG Power Module

The main difference between this section and section 3.3 is that instead of the measuring lines, e.g. L1 and L2 shown in Figure 3-3a, electric field intensity at some specific points is considered. It should be noted that E_{max}, considered in Section 3.3 to evaluate and compare various electric field grading techniques, may occur in different locations on a measuring line for different electric field grading methods. In this section, E values obtained by different electric field grading methods are compared at given points. In other words, measuring locations are fixed when comparing different mitigation methods. However, it should be noted that these E values may not be the maximum value

of electric fields at a given distance of interfaces. Using simulation results presented in Section 3.3 and this section, the effectiveness of the proposed mitigation method, combined geometrical techniques and applying nonlinear FDC layers, can be proved in both terms of E_{max} on measuring lines and E at given points. Also, modeling and simulation here are carried out for a blocking voltage of 30 kV, to examine our mitigation method for a higher voltage level. Moreover, the influence of other parameters not discussed in Section 3.3 is presented here.

According to IEC 61287-1, for a 30 kV-power module ($U_b = 30$ kV), "$V_{ac,max} = 61.42\ kV$". As discussed earlier, by assuming a value of 25 kV/mm for the "dielectric strength" of the "AlN substrate", the minimum thickness of the substrate should be $61.42/25 = 2.46$ mm to assure that the substrate would endure the one-minute insulation test. Also, to simulate the similar condition as the "PD measurement test", an AC voltage with the amplitude of "$1.1U_b$= 33 kV" should be applied across the "top metallization layer", whereas the "bottom metallization layer" is considered grounded.

Figures 3-14a and 3-14b show the geometry examined for simulations. The dimensions of the "base case" and "protruding substrate" except for the AlN thickness (2.46 mm) are set to be the same as those indicated in Figures 3-2 and 3-3.

Here again, to avoid theoretically infinite value for E at perfectly sharp edges, with a proper radius, all sharp edges were curved. Again, since mesh size has a decisive role in the measured values of E, two methods were adopted as follows: 1) Two distinguished meshing zones were defined. All sharp edges were included in zone 1 where an "extremely dense meshing" was applied. Also, a dense meshing was defined for the remaining zones. 2) Measuring points, instead of the measuring lines in Section 3.3, are considered as points

"M1-M4" denoted in Figures 3-14a and 3-14b as the minimal distance between a point placed in a medium and another medium is "15 µm". Employing these two approaches results in a disparity of less than 1% in the measured values of E by considering smaller meshing size. In order to examine the impact of different parameters on the "electric field intensity", the associated E values at the "measuring points" are determined.

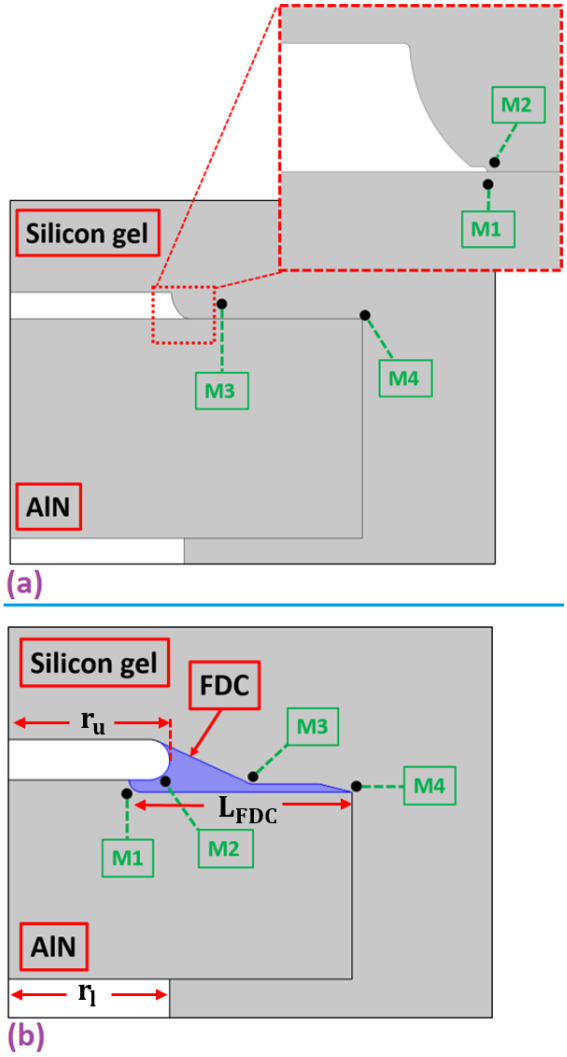

Figure 3-14: The geometry of (a) a conventional substrate, and (b) protruding substrate with a nonlinear FDC layer.

As mentioned above, electric field breakdown strength of AlN substrate is assumed to be 25 kV/mm. As a commercial case, "SYLGARD™ 527 Silicone Dielectric Gel"

manufactured by the "Dow Chemical Company" demonstrates a "dielectric strength of 17 kV/mm" [65]. Thus, the aforementioned two values of materials' dielectric strength have been considering as our criterion in this section for the "electrical insulation design" of the "envisaged 30 kV high power density WBG power module", which is also different from that defined in Section 3.3 that was based on PD.

The obtained values of E at "M1-M4" for the "base case (Figure 3-14a) under DC ($V_{DC} = 33$ kV) and AC ($V_{AC} = 33\sin(100\pi t)$ kV, $f = 50$ Hz)" are recorded in Table 3-1. These AC / DC voltages are also utilized for the following simulations. Worthwhile to note that E at measuring points under AC in Table 3-1 and the further tables, indeed, represents E_{max} at points of interest. The "relative permittivity (ε_r)" of "AlN substrate and silicone gel" was typically assumed to be "9 and 2.86", respectively. Accordingly, their "electrical conductivities" were considered as "10^{-11} and 10^{-13} S/m", respectively. The E values at every point of the module are computed by "FEM models developed in COMSOL Multiphysics". Based on Table 3-1, the obtained values of E in the "AlN substrate" (M1) and "silicone gel" (M2) are far above the determined "criterion values".

Another noteworthy point is that, while under DC applied voltages, only conduction currents are flowing within the dielectric, the situation is a bit different under AC voltages where both conduction and capacitive currents are contributing to the total current flowing through the material.

Table 3-1: E (kV/mm) Values at M1 − M4 for the Base Case under DC and AC

$Mode$	$M1$	$M2$	$M3$	$M4$
DC	81.24	82.2	22.19	2.11
AC	80.12	78.61	23	3.23

To meet the criterion, the impact of protruding substrate design on E is examined in the first place. The calculated values of E at "M1-M4" for the model described in Figure 3-14b with no nonlinear FDC coating and under DC voltage are reported in Table 3-2. It is obvious that the "protruding substrate design" cannot address the "high electric field" problem individually in the "envisaged 30 kV high-density WBG module".

Table 3-2: E ($\mathbf{kV/mm}$) Values at M1-M4 for the Protruding Substrate under DC

$Mode$	$M1$	$M2$	$M3$	$M4$
DC	39.22	80.33	9.45	4.03

Thus, allegedly, "a combination of the protruding substrate design and the application of a nonlinear FDC layer", as represented in Figure 3-14b can utterly solve the high electric stress issue.

As illustrated in Figure 3-14b, the "HV protruding" area is entirely covered by the "nonlinear FDC layer", and then the layer thickness reduces to "100 µm" from the vicinity of "M3 to M4". The high-stressed zone of the module is located nearby the "HV protruding electrode". Several structures of the "nonlinear FDC layer" adjacent to "the HV protruding electrode" were studied, and the geometry presented in Figure 3-14b is the best illustration that can level E down to the "criterion values". In the following subsections, the impact of various parameters of the proposed grading technique on E at the "measuring points" is examined.

3.4.1 The Influence of Switching Field

Table 3-3 represents E at the "measuring points M1-M4" depicted in Figure 3-14b for the developed grading technique "under DC and AC voltages" for various values of E_b.

As indicated for all examined values of E_b, the grading technique, "combined protruding substrate and applying a nonlinear FDC layer", can dramatically mitigate "high electric field issue" in "envisaged WBG power module". For instance, Table 3-3 demonstrates that "under DC and for E_b=8 kV/mm", the grading method can be leading to an electric field decrement of "66% at M1 and 91% at M2" relative to the "protruding substrate design" individually (Table 3-2).

Table 3-3: *E* (kV/mm) Values at M1-M4 for Different Values of E_b

Mode	E_b	M1	M2	M3	M4
DC	2	13.34	2.50	2.46	6.92
AC		14.32	4.59	5.35	7.40
DC	4	13.24	3.97	4.57	3.99
AC		14.17	8.89	9.40	2.90
DC	6	13.24	6.00	6.25	3.02
AC		14.39	13.01	11.37	2.60
DC	8	13.36	7.03	7.44	2.65
AC		14.94	16.18	10.53	2.52
DC	12	13.49	8.61	8.19	2.54
AC		15.70	21.66	10.20	2.49
DC	18	13.51	8.93	8.23	2.54
AC		15.81	22.09	10.16	2.48

It can be inferred from Table 3-3 that the lower values of E_b may results in the more electric field mitigation at the desired points ("M1 (AlN substrate) and M3 (silicone gel)"). It is worth noting that M4 is located 15 µm away from the "nonlinear FDC layer" ending. The "nonbridging nonlinear FDC layer" illustrated in Figure 3-14b, is implicitly transferring the "high electric stress" of HV region to the end of the layer and as seen in Table 3-3 this is the more case for smaller E_b.

To assure the effectiveness of the “nonlinear FDC layer” in field reduction particularly when operating under “high-frequency AC voltages”, for the AC simulations in the following subsections, a “smaller value of switching field (E_b=4 kV/mm)” is taking into account. The impact of the applied voltage frequency on the field mitigation will be studied in Section 3.4.4. However, regarding DC simulations, a “moderate value of the switching field (E_b=8 kV/mm)” is employed in the following subsections. In fact, a more efficient field grading can be achieved using a smaller “switching field” value but owing to the enhancement of the electric field at the end of the “nonbridging layer”, a “moderate” value of E_b is preferred for DC simulations.

The E distribution for the “protruding substrate” case with and without application of the “nonlinear FDC coating” is displayed in Figures 3-15a and 3-15b, respectively. The same meshing size was assigned to the model for either case stated above. The simulations were carried under DC for both case studies. For better visualization, the maximum range of the E plot is set to 0-50 kV/mm. The E distribution regarding the case with E_b=8 kV/mm is represented in Figure 3-15b. It can be concluded from Figures 3-15a and 3-15b that “applying a nonbridging nonlinear FDC layer” can effectively mitigate the high field issue in the vicinity of the top metallization zone. Nonetheless, it is leading to an increase in the E value adjacent to the “bottom metallization layer”. To deal with the problem, the “bridging design” discussed in Section 3.4.3. is recommended.

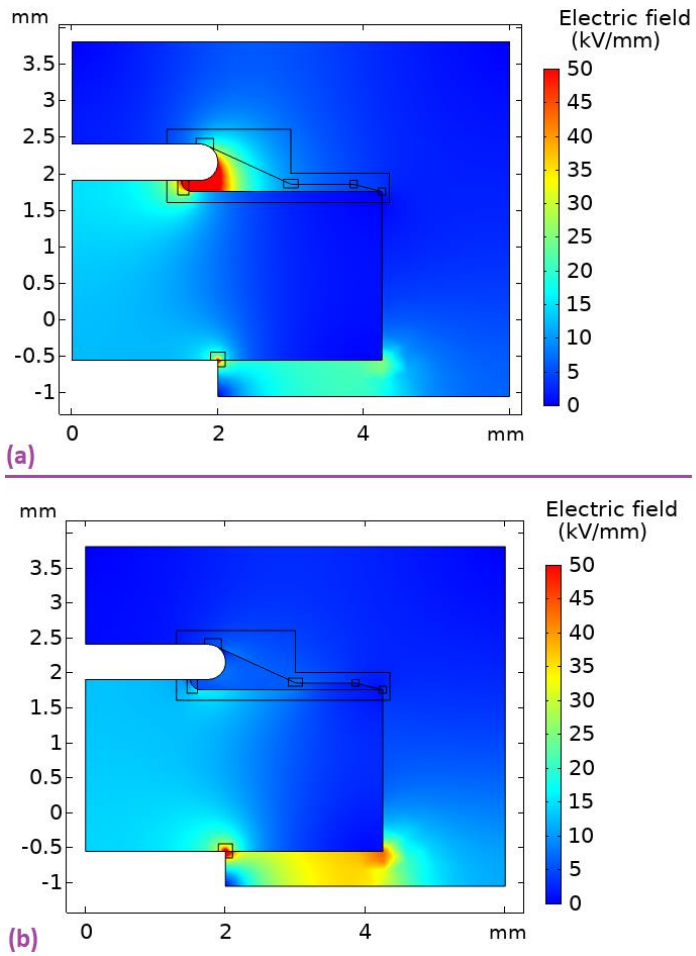

Figure 3-15: E distribution for the protruding substrate (a) without applying the nonlinear FDC layer and (b) by applying the nonlinear FDC layer.

3.4.2 The Influence of the Nonlinear FDC Layer Length

Here, the impact of "the nonlinear FDC layer length (L_{FDC})" depicted in Figure 3-14b on the field reduction is studied. For the sake of simulations, two values of L_{FDC} ("1.8 mm and 2.75 mm") are examined. The simulation results demonstrated in Table 3-4 present that "the length of the nonlinear FDC layer" has a minor influence on the field reduction. However, the electric field value at M4 is negatively impacted by selecting a smaller length. The result was expected as for a smaller "L_{FDC}", M4 relocated to a region closer to

the “HV electrode” and high-stressed area. All E values reported in Table 3-3 are for “L_{FDC}=2.75 mm”. For the following subsections, L_{FDC}=2.75 mm was considered.

Table 3-4: E (kV/mm) Values at M1-M4 for Different Values of L_{FDC} (mm)

	L_{FDC}	M1	M2	M3	M4
DC	1.8	13.39	7.13	6.86	13.9
AC		14.25	9.17	9.4	16.25
DC	2.75	13.36	7.03	7.44	2.65
AC		14.17	8.89	9.4	2.9

3.4.3 The Protruding Substrate with a Bridging Nonlinear FDC Layer

Despite using a “nonbridging layer” of “nonlinear FDC material” to the “top metallization layer” area as indicated in Figure 3-14b can well address the “high field issue” in that area as shown before, it will lead to E enhancement in “bottom metallization layer” area. The reason is that for $E > E_b$, “nonlinear FDC layer” acts as a “prolongation of the HV electrode” increasing E around the “ground electrode”. For addressing this issue, a “bridging nonlinear FDC layer” as depicted in Figures 3-16a and 3-16b is proposed. In the geometry demonstrated in Figure 3-16a, the thickness of the “nonlinear FDC layer” bridging the “top and bottom metallization layers” is 100 µm along the way. But, its thickness increases to 250 µm to fully cover the region between “AlN substrate” and “base plate” in the “field grading geometry proposed” in Figure 3-16b.

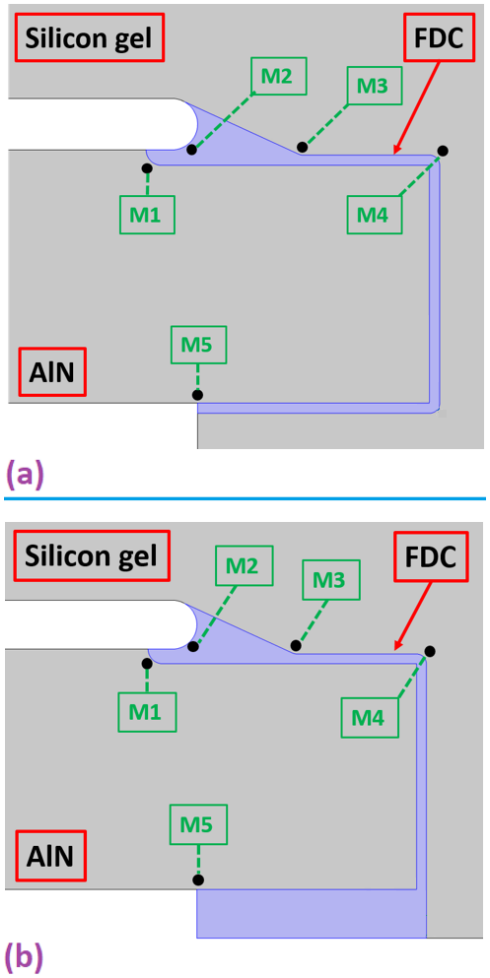

Figure 3-16: The geometry considered for simulations for a combination of the protruding substrate and a bridging nonlinear FDC layer with (a) a uniform thickness of 100 µm, (b) an increased thickness in the bottom metallization layer area.

A new "measuring point" represented by M5 (in the "AlN ceramic") in Figure 3-16 is considered. E values at "M1-M5" for the field mitigation techniques proposed in Figures 3-16a and 3-16b under "DC and AC" are presented in Table 3-5. E values presented in Table 3-5 are obtained for $r_{off} = 0$.

Table 3-5: *E* (kV/mm) Values at M1-M5 for the Field Grading Methods Shown in Figures 3-16a and 3-16b

Case	Mode	M1	M2	M3	M4	M5
Figure 3-16a	DC	14.5	4.81	8.48	1.49	44.54

	AC	14.53	8.73	9.54	2.50	14.86
Figure 3-16b	DC	15.33	7.62	9.19	2.85	3.87
	AC	14.83	8.73	9.75	2.86	6.20

As it is observable in Table 3-5, a “nonbridging FDC layer” cannot take E down to the “criterion value” at the “AlN substrate” (“25 kV/mm”) at “M5” under DC. Using the method shown in Figure 3-16b can well address this issue in the “bottom area”. Note that for the method proposed in Figure 3-16b, E at all desired points in both “silicone gel” and “AlN” meet the “criterion values”.

Figures 3-17a and 3-17b present the E distribution for the mitigation techniques illustrated in Figures 3-16a and 3-16b, respectively. Both cases are under “DC” and for “E_b=8 kV/mm”. The range of E plot is restricted to “0-50 kV/mm” for both cases to able to compare them visually. Seen in Figure 3-17a and mentioned above, there is a “high field issue” around the “bottom metallization layer”. This problem can be well-addressed by fully covering the bottom area with the “nonlinear FDC layer”, as illustrated in Figure 3-17b.

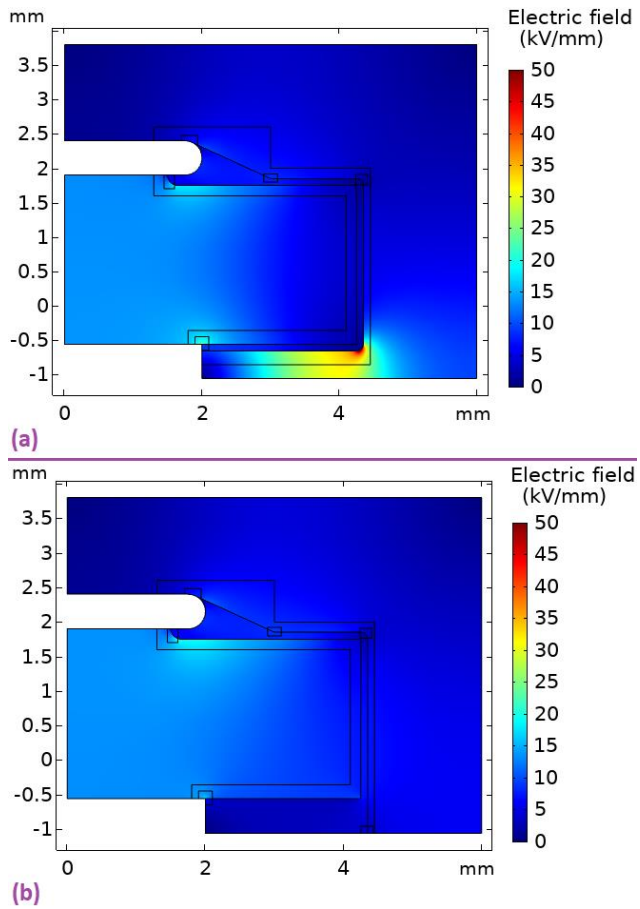

Figure 3-17: E distribution for the methods shown in (a) Figure 3-16a, (b) Figure 3-16b.

3.4.4 The Influence of the Frequency of Applied Voltages

In this section, the performance of the proposed method shown in Figure 3-16b under "sinusoidal AC voltages" with frequencies of "100 Hz, 1 kHz, 10 kHz, and 100 kHz" is investigated. For evaluation a severe condition, simulations are performed for "$r_{off} = -1$ mm".

The "relative permittivity" of "AlN substrates" was tested over the frequency range "500 Hz to 10 MHz" in [77], and it was found that it is frequency independent. According to the datasheet of "SYLGARD™ 527 silicone gel", its "relative permittivity" is also "frequency-independent" over the frequency range from "100 Hz to 100 kHz".

Furthermore, as mentioned above "nonlinear FDC materials" with "$\alpha > 10$" have "frequency-independent" "relative permittivity" and "electrical conductivity". The "electrical conductivity" of the "AlN substrate" and "silicone gel" is dependent on frequency and can be estimated by fitting the experimental data presented in [77, 78] as "$\sigma \approx 2.5 \times 10^{-13}(f - 50) + 10^{-11}\ \mathrm{S/m}$" and "$\sigma \approx 5.9 \times 10^{-14}(f - 50) + 10^{-13}\ \mathrm{S/m}$", respectively, where f is the frequency of the sinusoidal voltage in Hz.

Table 3-6 shows the values of E at M1-M5 for the "proposed method" indicated in Figure 3-16b under "sinusoidal AC voltage" with the above-mentioned frequencies. According to the results, the "proposed method" works well for frequencies up to 100 kHz.

To the best of our knowledge, all research on the "frequency dependence of insulation materials" like those above-mentioned has been performed under "sinusoidal AC voltages", not "square wave voltage". Note that the "relative permittivity" and "electrical conductivity" of "insulation material" are linked to its polarization caused by changing the polarity of the "external electric field" (or voltage). Therefore, a "sinusoidal AC voltage" and a "square wave voltage" with the same frequency will have the same effect. But, the measurement of the above-mentioned "frequency dependence of the materials" under "square wave voltage" can be considered as further research.

Table 3-6: E (kV/mm) Values at M1-M5 for Figure 3-16b Under Sinusoidal AC Voltage with Different Frequencies

$Frequency$	$M1$	$M2$	$M3$	$M4$	$M5$
100 Hz	15.07	9.35	10.63	2.85	5.49
1 kHz	15.14	11.20	11.42	2.59	5.15
10 kHz	15.24	13.23	12.45	2.42	4.86
100 kHz	15.67	15.70	12.58	2.33	4.67

It should be noted that a PD event in a “gas-filled void” located in the “silicone gel”, “AlN substrate”, or pores of “AlN ceramic” and “metallization layer” surfaces can be initiated right after the moment that the “electric field intensity” across the void is higher than a minimum “electric field” to initiate “electron avalanche” and “streamer formation” known as the “inception field”. The “electric field intensity” across the void is dependent on the magnitude of the applied voltage. This is the reason that the maximum amplitude of the applied voltages for DC, 50 Hz AC, and sinusoidal AC with different frequencies shown in Table 3-6 was considered to be an identical value of 33 kV to provide the same condition for PD initiation.

3.5 Conclusion

Efforts for producing testing samples to investigate novel methods to address “high electric fields” in “next-generation high voltage high-density WBG power modules” in universities’ Labs frequently fail due to 1) the “low thickness of the substrate” and “metallization layers” in the millimeter (mm) range and the so small dimensions of “protrusions of brazing” below the “metallization layers” in the micrometer (µm) range, 2) highly sharp edges in such structures which leads to highly “nonuniform electric fields”, and 3) the need for “high-quality materials and manufacturing/ factory” conditions and equipment. For addressing this issue, an “electrical field criterion” based on “accurate dimensions” and “PD measurement” of an actual “power module” was determined. For the first time, a systematic method for the “electrical insulation design of a high voltage high-density power module” was developed that met the requirements of the “one-minute insulation test” and the “PD test” according to IEC 61287-1. Simulation results from FEM

electric field calculations in “COMSOL Multiphysics” proved that geometrical techniques including 1) “metal layer offset”, 2) “protruding substrate”, and 3) “stacked substrate design”, either individually or combined, cannot meet the criterion values for a compact packaging. It was indicated that a combination of the above-mentioned “geometrical methods” and applying a “nonlinear FDC layer” could meet the “criterion values” for a “25-kV power module” considered for “modeling and simulations”. This work provides a comprehensive framework for the “electrical insulation design of high voltage, compact power electronics modules”. Following the method developed in this work can result in outstanding savings where the design obtained, e.g., Figures 13-2 or 3-13 for a “blocking voltage” of 25 kV, can be built and measured for the two above-mentioned tests in IEC 61287-1. Albeit requirements are not met, we are very close to a final solution.

Also, “FEM electric filed” models of the “electrical insulation system” envisaged for a “30 kV high-density WBG power module” were developed in “COMSOL Multiphysics”. Instead of E_{max} on the measuring lines considered for the 25-kV one, E values at given measuring points were considered for this 30-kV one. Again, it was shown that a combination of the “protruding substrate design” and applying “nonlinear FDC layer” to “high field areas” in the module could well bring E down to the “criterion values”, and for example, an electric field reduction of 66% and 91% in the “AlN substrate” and “silicone gel”, respectively can be acquired using the proposed method in comparison with using the “protruding substrate design” alone. Moreover, the influence of the switching field, the nonlinear FDC layer length, bridging nonlinear FDC layer compared to nonbridging one, and the frequency of applied voltages on E results was also studied.

Chapter 4

Effects of Frequency and Temperature on Electric Field Mitigation Method via Protruding Substrate Combined with Applying Nonlinear FDC Layer in Wide Bandgap Power Modules

4.1 Introduction

The insulation materials of "envisaged WBG power modules" will be under "square wave voltage pulses" with few-hundred-degree temperatures and few-MHz frequency. Considering the latter, while the silicon-based devices' temperature at junction is 175°C, the "WBG devices" possess the practicable capability at high temperatures of 200– 400°C [66, 67].

But, AC electrical conductivity, σ_{ac}, and the relative permittivity, ε_r, of nonlinear FDC materials, silicone gel, and aluminum nitride (AlN) ceramic were supposed to be independent of frequency and temperature in the modeling and simulations presented in Chapter 3 except for Section 3.4.4 where this topic was briefly studied. This is the case for other works presented by others focusing on electric field calculations inside power

electronics modules [68-75, to cite a few]. For electric field calculations, ε_r and σ_{ac} of materials are necessary and utilized.

Nevertheless, the records as reflected in the publication show that ε_r and σ_{ac} in a variety of insulators used in "power models" vary with frequency and temperature. It mounts major concerns about the validation of simulations of electric field—for previously mentioned parameters—that are measured under "DC or $50/60$ Hz AC sinusoidal voltages" at room temperature. This chapter deals with this concern as well as technical distance. Reflecting in the literature, Measurement data about the "frequency- and temperature-dependency" of the "relative permittivity" and "electrical conductivity" of "silicone gel", "nonlinear FDC material", and AlN are applied to investigate the effect of temperature and frequency on the "electric field reduction method" proposed in the previous chapter.

4.2 Frequency- and Temperature- Dependency of the Relative Permittivity and AC Electrical Conductivity

4.2.1 Silicone Gel

Rare experimental data are available in the literature related to the "thermal and frequency dependence" of ε_r and σ_{ac} of "silicone gel". Figures 4-1 and 4-2 respectively show the frequency dependence of ε_r and σ_{ac} for "silicone gel" at a variety of temperatures in the range of $20 - 160°\mathrm{C}$, reworked from [76], and applied in this chapter to simulate. In [76], the plate-to-plate electrodes with 1 mm gap distance, confirming a "uniform electric field" inside the sample, were dipped in a commercial "silicone gel" for under about one-hour vacuum for removing trapped gas bubbles just before the polymerization, and then was used for tests.

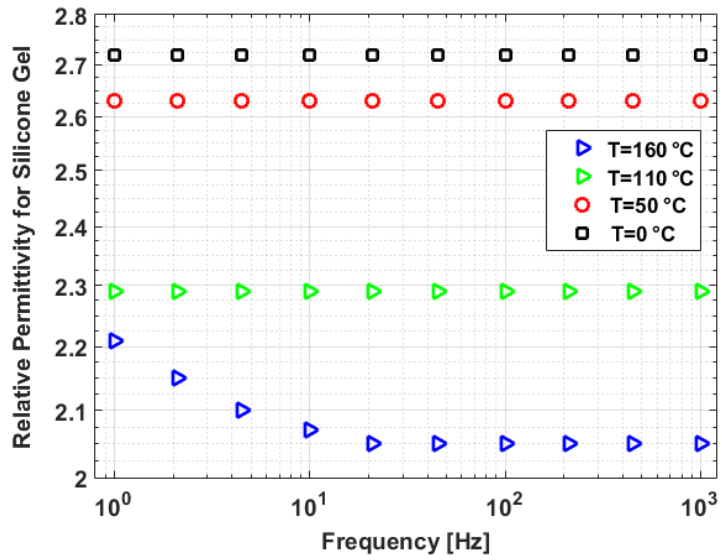

Figure 4-1: Frequency dependence of the relative permittivity of silicone gel at several temperatures between 20 and 160 °C, reproduced from [76].

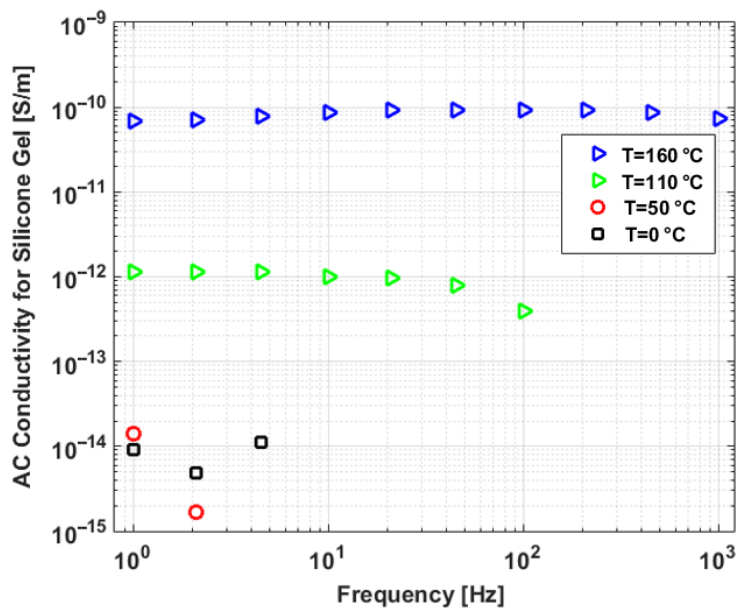

Figure 4-2: AC electrical conductivity of silicone gel versus frequency at several temperatures between 20 and 160 °C, reproduced from [76].

In [76], the ε_r and σ_{ac} measurements over a broad range of frequency—up to 1 kHz— at a number of temperature—up to 160ºC—was performed. In another measurement [77], however, ε_r and σ_{ac} was reported over frequencies ranged from 0.1 Hz to 1 MHz and just for the one temperature of 250°C.

Figures 4-3 and 4-4 show the measured records of ε_r (ε') and ε'' ("dielectric loss"), respectively, reflected in [89]. σ_{ac} of the sample is linked to the "dielectric loss" by

$$\sigma_{ac} = \omega\varepsilon_0\varepsilon'' \qquad (4-1)$$

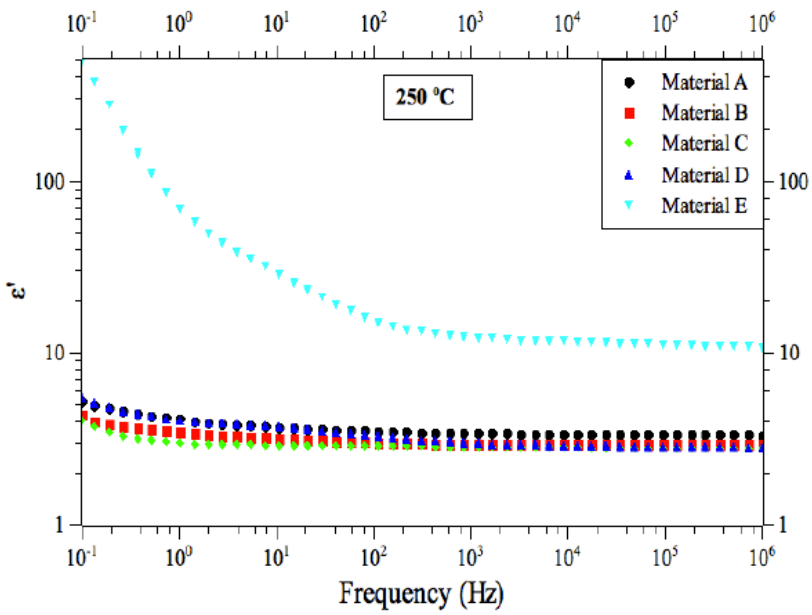

Figure 4-3: The relative permittivity (ε_r) of silicone gel versus frequency at 250°C [77].

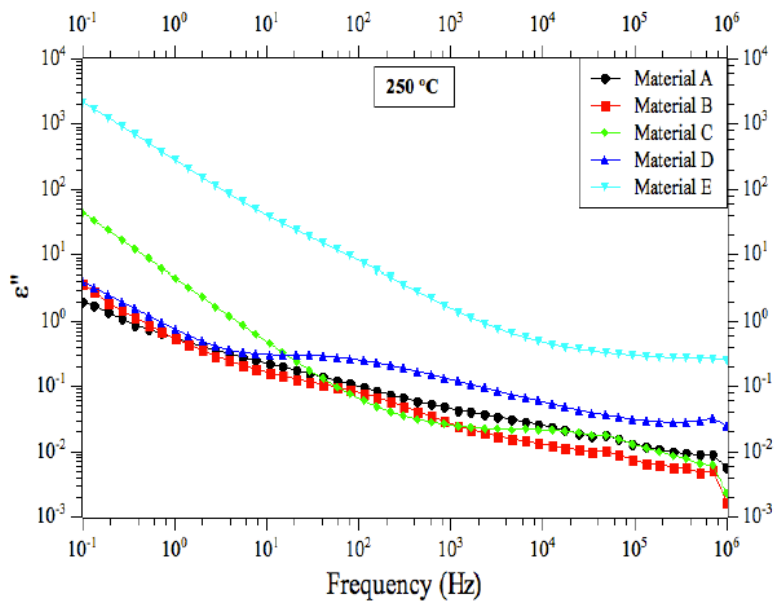

Figure 4-4: The dielectric loss (ε'') of silicone gel versus frequency at 250°C [77].

Simulations are accomplished for the base case of "$\{22\ °C, 50\ Hz\}$" and other seven case studies ("Case 1: $\{110\ °C, 450\ Hz\}$, Case 2: $\{110\ °C, 1000\ Hz\}$, Case 3: $\{160\ °C, 450\ Hz\}$ and Case 4: $\{160\ °C, 1000\ Hz\}$ Case 5: $\{250°C, 10\ kHz\}$, Case 6: $\{250°C, 100\ kHz\}$ and Case 7: $\{250°C, 1\ MHz\}$"). From Figure 4-1, ε_r for the "base case" and "Cases 1–4 is $2.72, 2.29, 2.29, 2.05$, and 2.05", respectively. It can be seen in Figure 4-1that ε_r is frequency-independent for the range of $50 - 1000$ Hz, while it declines with temperature. From Figure 4-2, σ_{ac} for the temperature of $110\ °C$, was recorded up to "100 Hz - $3.9 \times 10 - 13\ S/m$—in" [76]. The same value is assumed for 450 and 1000 Hz. The reported value for σ_{ac} at $22\ °C$ was up to 4.5 Hz in [88], assuming that almost there will be no change for $50, 450$ and 1000 Hz ("$1.1 \times 10 - 14\ S/m$"). From Figure 4-2, it is observable that σ_{ac} is rather "frequency-independent", and so the aforementioned assumptions are valid. The reproduced data for all cases is summarized in Table 4-1.

4.2.2 Aluminum Nitride Substrate

Few reports are available on the "high-temperature insulation properties of the ceramic insulating substrate" for "power modules". In this chapter, ε_r and σ_{ac} of AlN applied in "power modules" up to a "high temperature" of 450℃ and a "high frequency" of 10 MHz reported in [78] are utilized for simulations. In [78], ε_r and σ_{ac} are determined using measure of the complex impedance of a "metalized ceramic substrate" with 1 mm thickness under 10 V AC voltage and over a range of "$100\ mHz - 10\ MHz$" for frequency from the room temperature to $450°C$, can be seen in Figures 4-5 and 4-6.

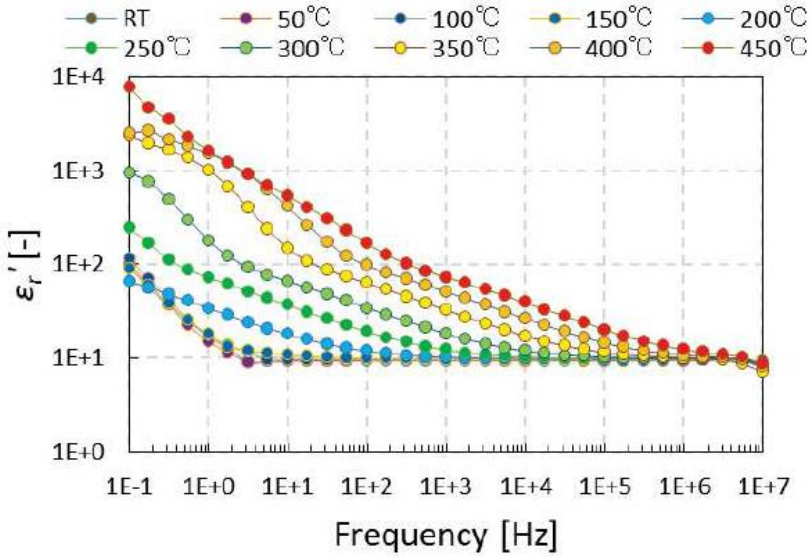

Figure 4-5: The relative permittivity (ε_r) of AlN for different frequencies and temperatures [78].

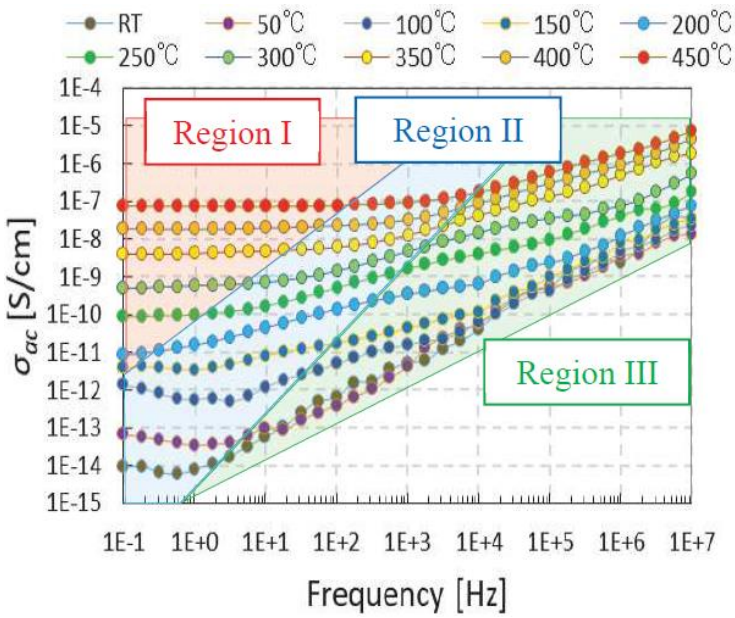

Figure 4-6: The ac electrical conductivity (σ_{ac}) of AlN for different frequencies and temperatures [78].

The reproduced data for the case studies from Figures 4-5 and 4-6 are brought in Table 4-1.

Table 4-1: Parameter Used for Simulations.

Case	AlN	AlN	Silicone gel	Silicone gel
	ε_r	$\sigma_{ac}\ (S/m)$	ε_r	$\sigma_{ac}\ (S/m)$
Base Case	9.43	5×10^{-11}	2.72	1.1×10^{-14}
Case 1	9.62	1.45×10^{-9}	2.29	3.9×10^{-13}
Case 2	9.42	2.06×10^{-9}	2.29	3.9×10^{-13}
Case 3	10.79	5.76×10^{-9}	2.05	8.8×10^{-11}
Case 4	10.02	1×10^{-8}	2.05	7.4×10^{-11}
Case 5	10.01	3.9×10^{-7}	2.88	1.11×10^{-8}
Case 6	9.8	8.9×10^{-7}	2.82	7.34×10^{-8}
Case 7	9.6	4×10^{-6}	2.87	1.31×10^{-7}

4.2.3 Nonlinear FDC Material

"Polymeric composites using fillers" such as "carbon black", SiC, or blends of various oxides, e.g., "$BaTiO_3$, TiO_2, SiO_2, Fe_3O_4, and mica", have been applied for both "end corona protection of motor stator bars" and "cable accessories" for a long time.

More recently, a new "nonlinear field grading material" based upon "ZnO microvaristors" has been made available. In [79], electrical and thermal data of "ZnO microvaristors" are provided, the reproduced measuring data of which (Figure 4-3) indicates the influence of temperature on the conductivity of a "silicone compound" with "35 vol% ZnO microvaristor filler" at temperatures of "22 and 90°C". As discussed in [79], the combined actions of the "thermally activated transport of ZnO microvaristor fillers" and the "thermal expansion of the silicon rubber matrix" lead to a somewhat "temperature-independent" conductivity.

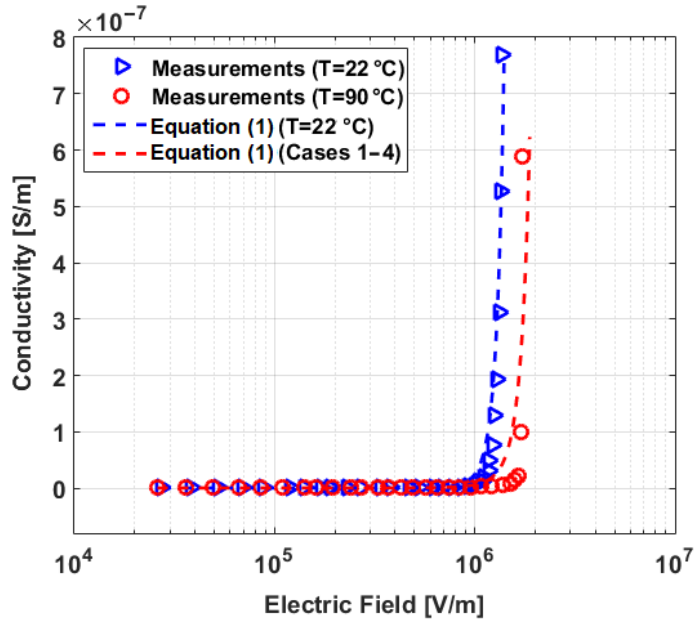

Figure 4-7: $\sigma(E)$ of a ZnO microvaristor-silicone compound for different temperatures, reproduced from [79].

In this chapter, the "ZnO microvaristor-silicone compound" (Figure 4-3) is regarded as "nonlinear FDC material" for simulations. The recorded data in Figure 4-3 is fitted by

$$\sigma(E) = ae^{bE} \qquad (4-2)$$

where (a,b) for the temperatures of 22 and 90°C are, respectively, $(4.83 \times 10^{-12}, 8.552 \times 10^{-6})$, and $(3.092 \times 10^{-11}, 5.272 \times 10^{-6})$. The recorded data for the temperature of 90°C (Figure 4-7) is utilized for the considered case studies of $110, 160$, and 250°C in this chapter, as the conductivity of the "ZnO microvaristor-silicone compound" is somewhat temperature-independent (can be seen in Figure 4-7 and argued in [91]). As already reported, ε_r only poorly depends on a frequency above 50 Hz [79]. The "frequency-dependency" of conductivity and "temperature-dependency" of ε_r for "microvaristor-silicone compounds" are not reflected in [79] and also such data couldn't be found in other

literature. Accordingly, the "AC electrical conductivity" and ε_r of the "microvaristor-silicone compound" examined for simulations are supposed to be "frequency-independent" and "temperature-independent", respectively. The summarized reproducing data from [79] for the "base case" and four other cases are available in Table 4-2.

Table 4-2: The FDC Materials' σ(E) Parameters and ε_r Used for Different Cases [79].

Case	a	b	ε_r
Base Case	4.83×10^{-12}	8.552×10^{-6}	11.47
Case 1	3.092×10^{-11}	5.272×10^{-6}	11.18
Case 2	3.092×10^{-11}	5.272×10^{-6}	11.11
Case 3	3.092×10^{-11}	5.272×10^{-6}	11.18
Case 4	3.092×10^{-11}	5.272×10^{-6}	11.11
Case 5	3.092×10^{-11}	5.272×10^{-6}	10.98
Case 6	3.092×10^{-11}	5.272×10^{-6}	10.9
Case 7	3.092×10^{-11}	5.272×10^{-6}	10.86

4.3 Modeling and Simulation Results

Studies are done for a 6.5-kV "power module" advantaging from a "protruding substrate" combined with the application of a "non-bridging nonlinear FDC layer" as presented in Figure 4-8.

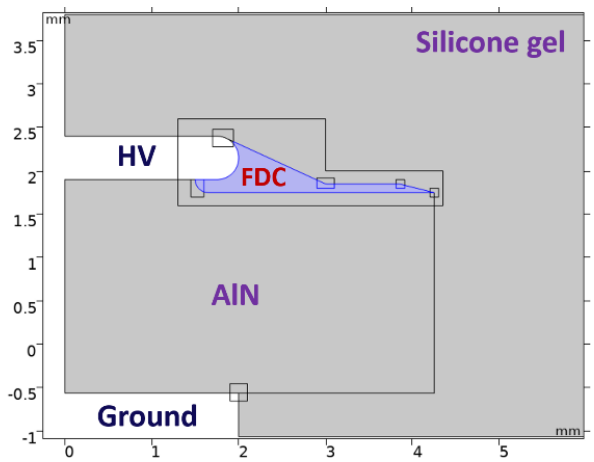

Figure 4-8: The geometry considered for simulations.

It can be seen in Figure 4-9a that three zones with different mesh sizes were considered. A highly dense meshing with a "maximum element size" of 4 µm has been used for the "zone 1", which included all "sharp edges". The maximum mesh element sizes of "10 and 400 µm" have also been used for "zones 2 and 3", respectively. The "electric field measurements" are performed at measuring lines "L1 (in AlN substrate)", "L2 (in nonlinear FDC layer)", and "L3 (in silicone gel)", as demonstrated in Figure 4-11b, where the lines have a minimum distance of 15 µm from materials' interfaces.

A "50 Hz AC voltage" with a "maximum amplitude of 7.15 kV" was applied to the "HV electrode". But, for Cases 1–7, in which the frequency is above 50 Hz, the same procedure as "IEC 61287-1" for PD was followed with the only change in the applied voltage frequency from 50 to 450 Hz in Cases 1 and 3, to 1 kHz in Cases 2 and 4, and to 10 kHz, 100 kHz, 1 MHz, in Case 5-7, respectively. The electrical parameters expressed in Section 4-2 were utilized for the simulations. E_{max} and L1–L3 for case studies is summarized in Table 4-3.

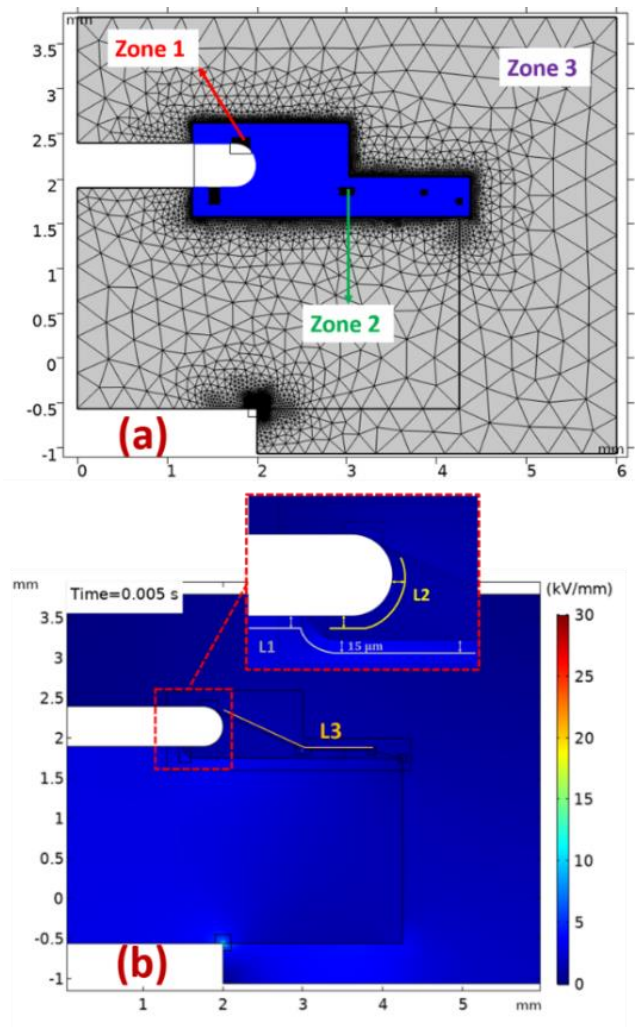

Figure 4-9: (a) Meshing strategy, (b) electric field distribution for the geometry considered according to Figure 4-6 under a 7.15 kV (peak) AC 50 Hz voltage.

Table 4-3: E_{max}(kV/mm) at L1-L3 for the geometry of Figure 4-10 for case studies.

Case	L1	L2	L3
Base case	3.91	1.17	3.49
Case 1	3.88	1.84	2.21
Case 2	3.90	1.72	2.26
Case 3	3.85	1.86	2.22
Case 4	3.90	1.98	2.34
Case 5	4.10	2.39	2.66
Case 6	4.24	2.74	2.93
Case 7	4.31	3.11	3.16
Case 8	8.48	10.54	4.82

Table 4-3 shows that the "electric field reduction method" as the "protruding substrate" design combined with the application of a "nonlinear FDC layer" is somewhat "temperature- and frequency-independent" in the temperature range of $22-160°C$ and frequency range of $50-1000$ Hz. The maximum value of electric field (E_{max}) for $250°C$ (Cases 5-7) along lines L1-L3 raises (by "5% in AlN, 30% in nonlinear FDC later, and 19% in silicone gel") frequency increases from 10 kHz to 1 MHz. As Table 4-3 shows, Case 8 is the same as Case 7 ($250°C$, 1 MHz) but without applying a "nonlinear FDC layer". It is obvious that, still, the "nonlinear FDC layer" works well at the high temperature of $250°C$ under 1 MHz, compared to Case 7, leading to an E decrease of 49% in AlN and 71% in "silicone gel". Comparing the base case ($22\ °C, 50$ Hz) with Case 7 ($250°C, 1$ MHz) shows that E values increase by 10% in AlN and 165% in the "nonlinear FDC layer", and reduces by 9% in "silicone gel". Regarding these results as well as the accessibility of measurement data for ε_r and σ_{ac} for "silicone gel" [76, 77], AlN [78], and other "ceramic substrate materials" noted in the literature, it is suggested using the values of the aforementioned parameters at working conditions, particularly for high temperatures and frequencies to acquire more precise and dependable values of E.

4.4 Conclusion

Practically, the "insulation materials" of "envisaged WBG power modules" are exposed to "square wave voltage pulses" with a "frequency up to a few MHz" and temperatures up to a few hundred degrees. "Temperature" and "frequency" are two significant factors that commonly influence the electrical characteristics ("relative

permittivity and AC electrical conductivity") of the "dielectric materials" and they may affect "electric field distribution". The "electric field simulations and calculations" reflected in the literature to date disregard the "frequency and "temperature dependency" of ε_r and σ_{ac} for the "insulating materials" used in the "power modules". Hence, there is a doubt about the results' validation for "high temperatures" and "high frequencies". This chapter addresses this technical gap through:

- Supplying the measurement data of ε_r and σ_{ac} reflected in diverse literature for "AlN", "silicone gel", and a "nonlinear FDC material" as a "base case$\{22\ °\mathrm{C}, 50\ \mathrm{Hz}\}$" and seven cases for "$\{110\ °\mathrm{C}, 450\ \mathrm{Hz}\}$, $\{110\ °\mathrm{C}, 1000\ \mathrm{Hz}\}$, $\{160\ °\mathrm{C}, 450\ \mathrm{Hz}\}$, Case 4: $\{160\ °\mathrm{C}, 1000\ \mathrm{Hz}\}$ Case 5: $\{250°\mathrm{C}, 10\ \mathrm{kHz}\}$, Case 6: $\{250°\mathrm{C}, 100\ \mathrm{kHz}\}$ and Case 7: $\{250°\mathrm{C}, 1\ \mathrm{MHz}\}$".
- Developing a "FEM model" for electric field evaluations in "COMSOL Multiphysics", where the successful "electric field reduction method" matured in our aforementioned investigations via "protruding substrate" combined with applying a "nonlinear FDC layer" was adopted for simulations,
- Simulations employing the model and aforementioned measurement data, where it was found that the success of our developed electric field mitigation approach as "protruding substrate" combined with the application of a "nonlinear FDC layer" is not influenced even at $250°\mathrm{C}$ and $1\ \mathrm{MHz}$.

The findings of this chapter were presented in [80, 81].

Chapter 5

Accurate Estimation of Temperature within a 10 kV SiC Power Module via an Electrothermal Model

5.1 Introduction

As mentioned before, there is a trend towards high voltage, high power density concept. As an example of its high power density part, the existing maximum heat flux of IGBT modules in hybrid electric vehicle power electronics of 100-150 W/cm^2 is expected to reach up to 500 W/cm^2 soon [82]. Heat losses are caused due to 1) conduction loss in the on-state situation and 2) switching losses. Although SiC and GaN-based devices can survive at temperatures much higher than Si-based ones that are limited up to 150°C for 6 kV [83], due to the limit on the operating temperature of packaging materials, especially silicone gel, their junction temperature is limited to 175°C [84]. Thus, in this chapter, this limit (175°C) is considered when determining the maximum load current of the SiC module. The thermal increase within the module also impacts the electrical characteristics

of different components in the power module. Double-sided cooling, jet impingement, spray cooling, and microchannel heatsink [85-87, to cite a few] are thermal mitigation solutions introduced to date.

The packaging components of a power module experience a combination of electrical, thermal, and mechanical stresses, which may affect each other as well. Thus, considering the impact of each stress without taking account of the effect of other stresses on it may result in inaccurate evaluation. On the other hand, experimental methods presented to measure the junction temperature of the chip are via thermocouple, infrared thermal scanner, and pressure drop method. In addition to the lack of sufficient accuracy, the mentioned experimental techniques cause permanent damage to the device as well as they are not cost-effective especially for designing a new prototype. To address these issues, Multiphysics models have been developed in either circuit simulators such as PSpice and Simulink based on RC network models or FEM-based tools such as COMSOL Multiphysics and ANSYS, or analytical approaches [88-90, to cite a few] to consider coupling effects of stresses and obtain an accurate estimation of temperature within a power module. Each of these methods has drawbacks such as insufficient accuracy, high computational time, or applicable for elementary geometries, respectively.

In this chapter, it is shown that with a combination of FEM simulations in COMSOL Multiphysics and RC network modeling developed in a circuit simulator, temperature distributions within the modules can be obtained in a fast and accurate way. The method is used to design the packaging for a 10-kV module consisting of 9 SiC PiN diodes. The Temperature-dependency of the electrical characteristics of the chip is considered and for considered dimensions, the maximum load current is determined.

5.2 Electrical Insulation Design and Thermal Analysis

The 3D schematic of the proposed 10 kV power module modeled in COMSOL Multiphysics is shown in Figure 5-1. In the power module, SiC PiN diodes (or often called as dies) are soldered in parallel on a DBC layer. The DBC layer, which consists of a ceramic substrate sandwiched between two copper layers, provides electrical insolation between the dies and the grounded base plates and heatsinks.

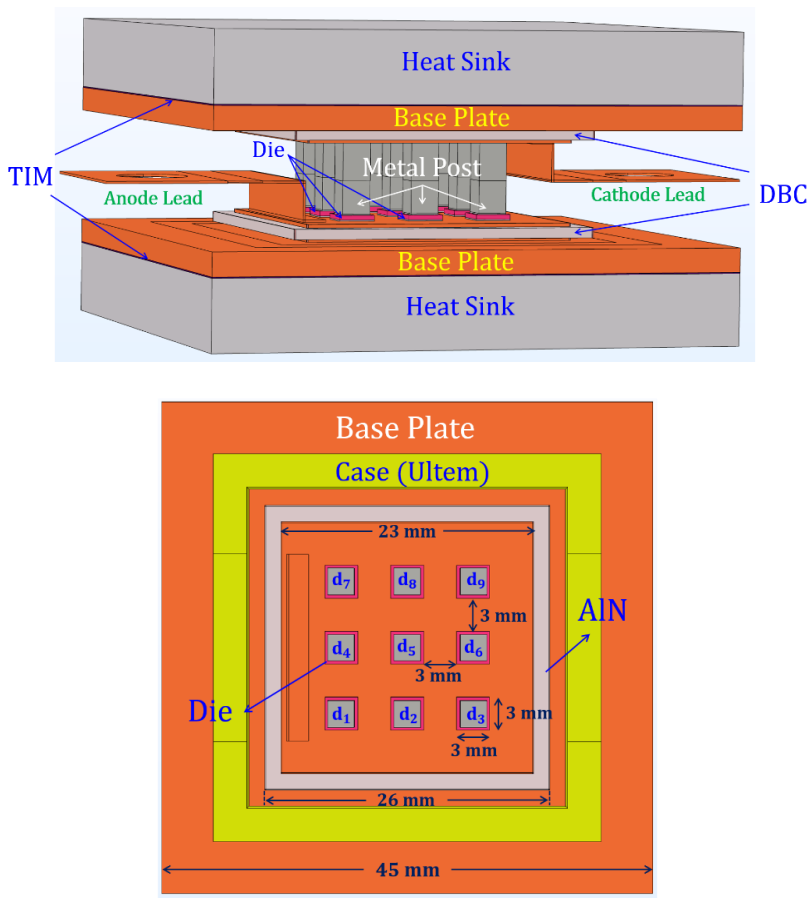

Figure 5-1: 3D schematic view of the 10-kV power module with its dimensions.

Although Al_2O_3 is the most economical choice, it has a thermal conductivity of 10-15 times smaller than AlN. Thus, AlN is considered as the substrate here, as shown in Figure 5-1. Using a double-sided heat sink provides two paths for the heat transfer to the

ambient and ensures better cooling. To reduce the parasitic inductance and eliminate the risk of wire-bond breakage in thermal cycling, metal posts introduced in [91] and made from Molybdenum (MO) are used for chips interconnection and circuit joints. The usual existing encapsulant, silicone gel, is used to avoid PD from occurrence with air and protect the module components against environmental impact.

5.2.1 Electrical Insulation Design

Considering the dielectric strength of the metalized AlN of 25 kV/mm, a minimum thickness of 0.86 mm is required to pass the "one-minute insulation test" according to IEC 61287-1 for a blocking voltage of 10 kV. This thickness of AlN is used for simulations of the PD test. To simulate the PD test recommended in IEC 61287-1, the maximum voltage applied to the chips should be $1.1U_b$ =11 kV. To reduce the electrical stress on the chips, this voltage is applied to the module symmetrically: $V = 5.5\sin(100\pi t)$ kV to the Anode lead and $V = -5.5\sin(100\pi t)$ kV to the Cathode lead. Because of the symmetry and for reducing the computational time, the electric field simulations were carried out for the 2D model. Guidelines for choosing proper meshing strategy and measuring lines (L1 in AlN and L2 in "silicone gel") are the same as those presented in chapter 3 and are not repeated here. Figures 5-2a and 5-2b show electric field distribution and measuring lines, and meshing strategy, respectively. The parameter used for the electrical and thermal simulations is summarized in Table 5-1. The maximum electric stresses on L1 and L2 are 18.02 kV/mm and 18.5 kV/mm, respectively. Using electric field grading techniques studied and developed in Chapter 3, high electric fields around triple points can be mitigated. We will not present those methods here, since for example, applying nonlinear

FDC layers with thicknesses of 100 µm has a negligible impact on temperature distribution in the module.

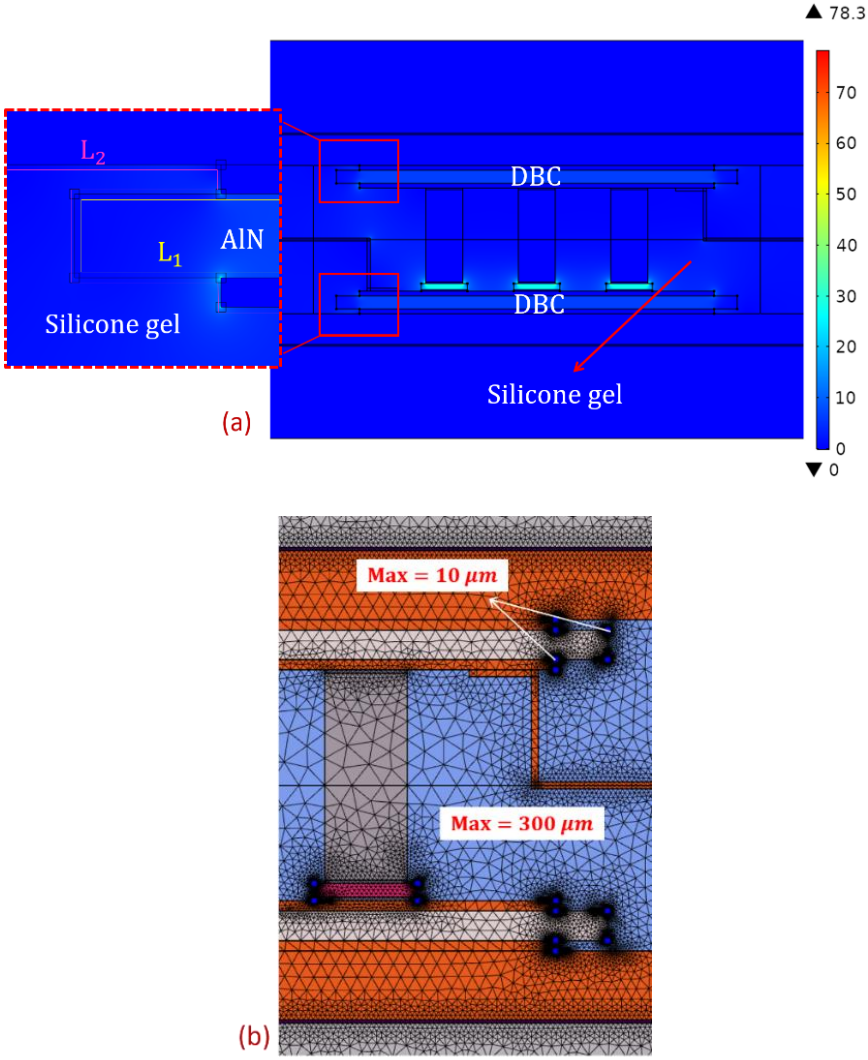

Figure 5-2: (a) Electric field distributions and measuring lines (L1 and L2), (b) meshing strategy.

Table 5-1: Material Characteristics

Component	**Material**	σ (S/m)	ε_r	κ $(W/m.K)$	C_p $(J/Kg.K)$
diode	SiC	1×10^3	10	450	1200
Metallization	Copper	5.99×10^7	1	393	385
Substrate	AlN	10^{-10}	8.6	160	690

Encapsulation	Silicone gel	1.43×10^{-16}	2.85	0.213	1510
Metal Post	Molybdenum	1.87×10^{7}	1	142	250
Solder	Sintered Ag	2.44×10^{7}	1	200	233
Heat sink	Al 6063-T83	3.03×10^{7}	1	201	900
Thermal Layer	TIM	5.6×10^{-10}	1	2	1200

5.2.2 Thermal Analysis

In a "power module", the heat generated in dies at the on-state is transferred through the beneath layers including solder and DBC to the base plate and heat sink, and then to the ambient. Typically, a thin layer of thermal grease, 100 µm, is added between the base plate and heat sink shown in Figure 5-1 as "Thermal Interface Material" (TIM) to reduce the contact thermal resistance [92]. The total thermal resistance of the module is determined by the sum of thermal resistance of all layers available within the conduction path. As mentioned in Section 5.1, the thermal management of the module aims to maintain the junction temperature below the maximum temperature of 175°C. Among all types of heat transfer in solids—conduction, convection, and radiation— the dominated one in power modules is conduction [92]. As in power modules, the source of heat flux is semiconductor dies, the factor of the position-dependent heat source can be eliminated from the heat conduction equation and it can be simplified to:

$$\kappa\left(\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}\right)=\rho c\frac{\partial T}{\partial t} \qquad (5-1)$$

where κ is the thermal conductivity, ρ is the mass density, and c is the specific heat capacity. Since the ratio of the thickness to the width for each layer within the power module is close to zero, the heat conduction process can be reduced to a one-dimensional

problem, from the top of the chip to the bottom of the heat sink. Thus considering z as the heat conduction direction, (19) is simplified to:

$$\kappa\left(\frac{\partial^2 T}{\partial z^2}\right) = \rho c \frac{\partial T}{\partial t} \qquad (5-2)$$

The boundary conditions for the thermal analysis can be defined as heat flux at the top surface of each chip, (5-3), and the convection heat transfer from the heat sink to air, (5-4).

$$\kappa_c \frac{\partial T_c(z)}{\partial z}\left[z = z_{\text{chip\_topside}}\right] = -Q_{in} = -\frac{P_{in}}{A} \qquad (5-3)$$

$$\kappa_H \frac{\partial T_H(z)}{\partial z}\left[z = z_{\text{Heatsink\_bottomside}}\right] = -h(T_H - T_{Amb}) \qquad (5-4)$$

where κ_c and κ_H are the thermal conductivity of chips and heat sink, respectively; Q_{in} is the input flux, P_{in} is the input power, A is the surface area perpendicular to the heat flux direction, and h is the convection flux coefficient. T_{Amb} is the ambient temperature which is set as 293.15 K (20°C) and T_H represents the heat sink temperature. The natural free heat convection to air at room temperature is 5-25 $W/m^2.K$ that is corresponding to the dissipated heat flow of 150-1500 W/cm^2 [92]. To increase the heat convection coefficient, cooling systems can be employed. A slab made from Aluminum 6063-T83 is considered for the heat sink that is cooled by a mix of water and ethylene glycol (50%/50%).

To obtain an accurate estimation of the junction temperature of the module, considering the cross heating of the chips is essential. In other words, the power loss on each chip will not only result in increasing the same chip temperature but also it leads to elevation of the neighbor chips temperature. To calculate the coupling effect of chips,

typically, equal to the number of chips available on the same DBC, FEA simulation must run, each time with only one die on.

From each simulation, the T of the on-chip and the other 8 off-chips, the solder, DBC, and base plate must be determined at the points of interest. The extracted values then are inserted in (5-5) and (5-6) to obtain the thermal resistance corresponding to each layer and the cross-heating of the chips [93]. The electrothermal modeling algorithm is illustrated in Figure 5-3.

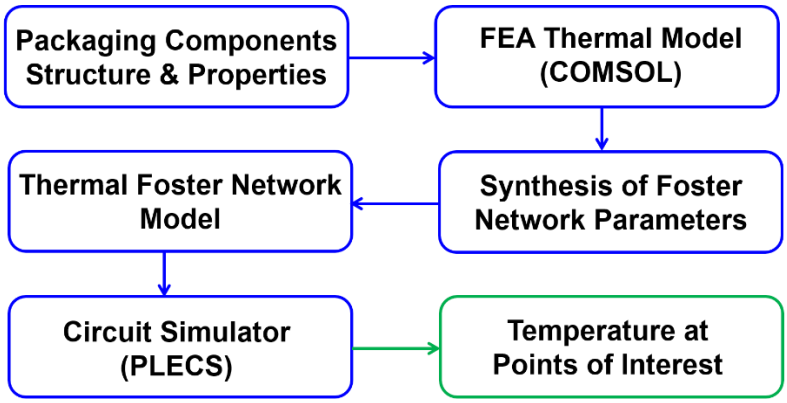

Figure 5-3: Electrothermal modeling algorithm.

Figure 5-4 shows different heat transfer layers for die #5 of the packaging design shown in Figure 5-1 where temperatures at nodes a, b, c, and d located on the active-chip top-surface, active-chip bottom-surface, bottom of the DBC copper layer, and bottom of the base plate, respectively, are obtained from an electrothermal model developed in COMSOL Multiphysics. Then temperature values are inserted in (5-5) and (5-6) to obtain the thermal resistance corresponding to each layer and the cross-heating of the chips.

$$R_{ill'} = \frac{T_m - T_{m-1}}{P_{loss-d_i}} \quad l, l' = J, S, D, B, A\,; \;\; m = a, b, c, d \qquad (5-5)$$

$$R_{i-jC} = \frac{T_{d_j} - T_A}{P_{loss-d_i}} \qquad i,j = 1 \dots 9 \qquad (5-6)$$

where $R_{ill'}$ is the thermal resistance between layers l and l', and R_{i-jC} represents the thermal resistance of the neighboring chips induced by the power loss in the active chip. P_{loss-d_i} is the power loss in the active chip. The letters $J, S, D, B,$ and A are assigned to the junction, solder, DBC, base plate, and ambient.

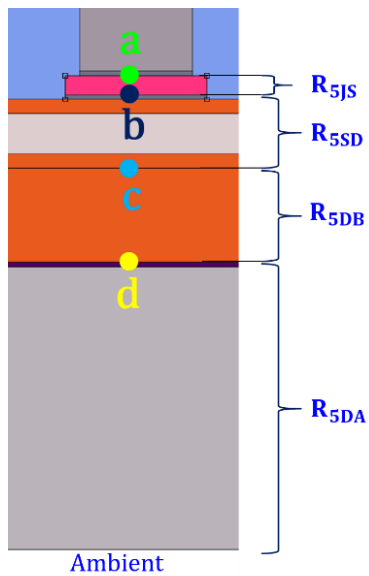

Figure 5-4: Thermal resistance of different heat transfer layers for die #5 in the proposed packaging design shown in Figure 5-1.

The self-thermal resistance of diode i (R_{iS}) is the sum of the thermal resistance of each layer placed within the conduction path given by

$$R_{iS} = R_{iJS} + R_{iSD} + R_{iDB} + R_{iBA} \qquad (5-7)$$

where R_{iJS}, R_{iSD}, R_{iDB}, and R_{iBA} are self-thermal resistance of junction to solder (node a-b), solder to DBC (node b-c), DBC to the base plate (node c-d), and the base plate to

ambient (node d to ambient). Then the junction temperature of each chip within the device, T_{Jd_i}, is calculated through the following thermal resistor matrix:

$$\begin{bmatrix} T_{Jd_1} \\ \vdots \\ T_{Jd_9} \end{bmatrix} = \begin{bmatrix} R_{1S} & \cdots & R_{1-9C} \\ \vdots & \ddots & \vdots \\ R_{9-1C} & \cdots & R_{9S} \end{bmatrix} \times \begin{bmatrix} P_{loss-d_1} \\ \vdots \\ P_{loss-d_9} \end{bmatrix} + \begin{bmatrix} T_A \\ \vdots \\ T_A \end{bmatrix} \qquad (5-8)$$

To obtain the junction temperature on each chip, we have to repeat the same process as we performed for the chip at the center (d_5), separately. The reasons that we have carried out the simulation steps only for the centered-chip are:

1- The thermal and electrical characteristics, as well as dimensions of all chips, are equal in the power module.
2- The temperature of the centered chip is highest among all other chips, as it is surrounded by other chips in four sides.

The thermal grease layer which is used usually between the base plate and heat sink imposes a nonlinearity on the heat diffusion process within the module. Thus, the calculated junction temperature without considering the nonlinearity characteristics of the thermal path parameters is not accurate. In this regard, the nonlinearity equation for R_{iBA} and the coupling thermal resistances (R_{i-jC}) should be considered.

The convection coefficient, h, can be determined by (5-9), that depends on the total power loss generated by the 9 chips ($9 \times P_{loss-d}$) and the area of the heat sink (S).

$$h = \frac{9 \times P_{loss-d_i}}{(T_{\text{base plate}} - T_{\text{amb}}) \times S} \qquad (5-9)$$

As seen from (5-9), for a given amount of S, different power losses in chips result in different values of h. Thus, to have an accurate electrothermal simulation, it is essential

to obtain the nonlinear equations corresponding to each thermal resistance which will be later used as the parameters of the Foster R- network. Thus, as the first step, the thermal resistance of each layer of the module is calculated at different h values. Considering $T_{\text{base plate}}$ and T_{amb} equal to 40°C and 20°C, respectively, and the heat sink area of $S = 45 \times 45\, mm^2$, for $h =$ 1000, 2000, 3000, 4000, 5000, 6000, and 7000 $W/m^2.K$, P_{loss-d_i} will be 4.5, 9, 13.5, 18, 22.5, 27, and 31.5 W, respectively.

The next step is to determine the thermal resistance of different layers of the module at each h and P_{loss-d}. To calculate the thermal parameters for the Foster R-network, seven steady-state FEM simulations using COMSOL Multiphysics are carried out for seven values of h and P_{loss-d} mentioned above and the calculated thermal resistances are fitted as a power equation of $F(x) = ax^b + c$, where $a, b,$ and c are constant and brought in Table 5-2 for each corresponding thermal resistance.

To build the electrothermal model, the Foster R-network with considering the coupling effect of the chips and the nonlinearity behavior of thermal resistances at different loads is modeled in PLECS which is a simulation platform for power electronic systems. The aim of the electrothermal analysis in this chapter is to estimate the maximum amount of current that can flow through each chip to meet the junction temperature limit of 175°C. In electrothermal simulations, power loss is provided by an electrical circuit that is coupled to the thermal circuit.

Before proceeding with electrothermal simulations, the junction temperature of d_5 as well as the solder, DBC, and base plate temperatures resulted from R-network in PLECS have been compared with those values estimated by FEA simulations from COMSOL where $P_{loss} = 31.5$ W is applied to the top-side of all chips. The results from FEA and R-

network demonstrate a good consistency, shown in Table 5-3 with a maximum disparity of 0.8 %.

Table 5-2: Parameters of the Fitted Curve for R_{ON} Vs. Temperature

R_{th} (K/W)	a	b	c
R_{5BA}	154.6	-0.9688	0.2187
R_{5-1C}	114	-0.845	0.0659
R_{5-2C}	203.9	-0.9379	0.1169
R_{5-3C}	116	-0.8526	0.0592
R_{5-4C}	203.9	-0.9379	0.1169
R_{5-6C}	203.9	-0.9379	0.1169
R_{5-7C}	183.7	-0.918	0.0665
R_{5-8C}	203.9	-0.9379	0.1169
R_{5-9C}	114	-0.845	0.0659

The on-resistance of the semiconductor die has a decisive role in the magnitude of power loss generated in the chip. However, the on-resistance (R_{On}) of semiconductor dies is temperature-dependent, which can significantly influence the magnitude of the power loss generated in the chips. The power loss in a chip is related to the R_{On} of semiconductor through $P_{lOss} = R_{On} I_{Cond}^2$, where I_{Cond} is generated via a current source. In other words, at a constant I_{Cond}, the smaller R_{On} leads to a decrease in P_{lOss} generated in the chip.
The on-resistance of the semiconductor die has a decisive role in the magnitude of power loss generated in the chip.

Figure 5-5 presents the R_{On} vs. T for a temperature range of 25-210°C for the SiC PiN diode (GA01PNS80-CAL), reproduced from the manufacturer's datasheet [94]. As seen from the R-T plot, the value of the R_{On} has been reduced from 1.24 Ω at T=25°C to 0.62 Ω at T=210°C. Accordingly, to improve the accuracy of the junction temperature

calculations, the R_{On} of the chips must be considered as a function of the temperature. Figure 5-6 describes the thermal R-network coupled with a simple electric circuit consists of a resistor and a DC source modeled in PLECS.

Table 5-3: The Predicted Temperatures for Different Layers via FEA and Foster Network Simulations.

Temperature (K)	FEA	Thermal R-network
Junction	350.76	353.68
Solder	349	351.65
DBC	338	339.7
Baseplate	335	337.8

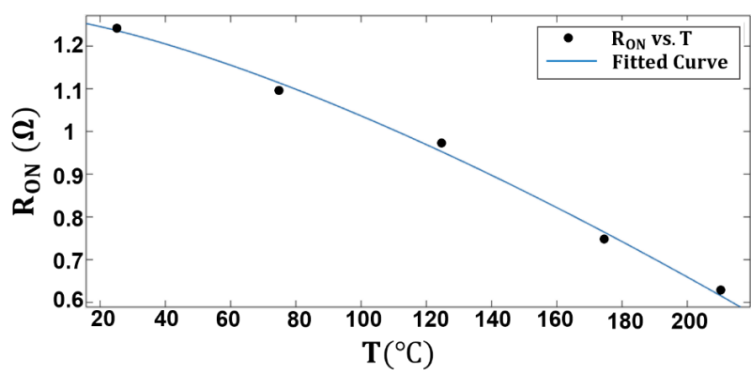

Figure 5-5: R_{on} of GA01PNS80-CAL vs. temperature [94].

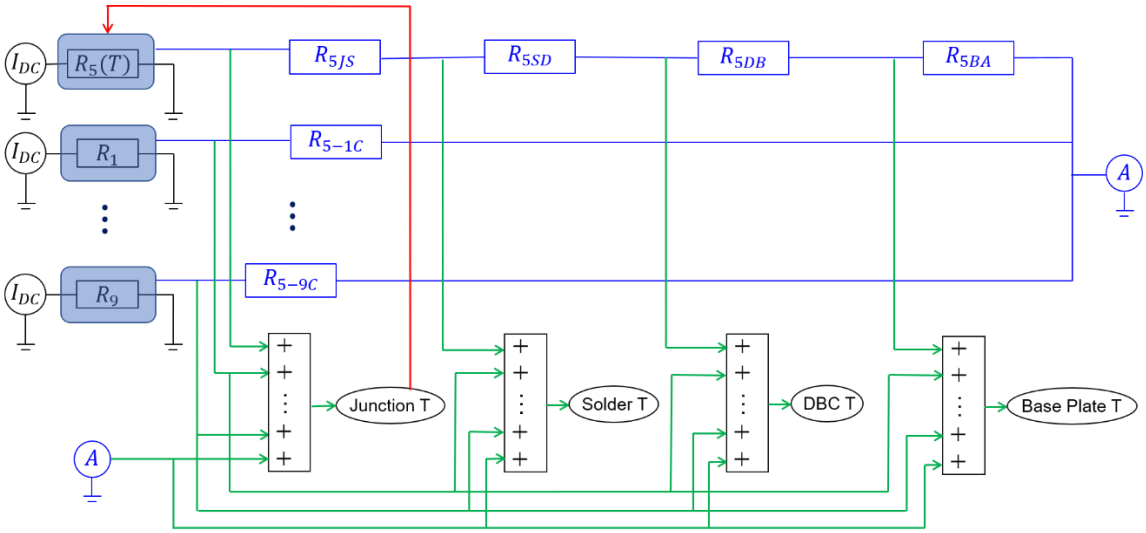

Figure 5-6: Thermal network for thermal simulation modeled in PLECS.

To compare the simulated value of the junction temperature for the cases with 1) constant, and 2) temperature-dependent R_{On}, electrothermal simulations have been carried out for the current source of 10 A. In the latter case, the R_{On} of die 5 was considered as $R_{On} = -0.0004\, T^{1.385} + 1.271$, while the resistivity of the other chips set constant similar to the former case with the value of 1.24 Ω equivalent to the magnitude of R_{On} at T=25℃. According to the simulation results, Table 5-4, by considering the temperature dependency of the R_{On} , the evaluated temperature at all layers has been reduced by roughly 16% in comparison with the constant R_{On} case.

To determine the maximum load current that the package can withstand regarding the junction temperature limit of 175°C, several simulations in PLECS were performed for different current sources in the 2-12 (A) range as shown in Figure 5-7. The simulation results indicate that at $I = 10\ A$ for each die, the junction temperature reaches 180.31°C, and the temperature at solder, DBC, and base plate are 175.5°C, 147.6°C, and 143.13°C, respectively. Since the SiC chip can survive at temperatures much higher than 200°C, and the estimated temperature at the other locations of the module is 175°C or less, the maximum load current of the module should not exceed 9×10=90 A.

Table 5-4: The Electrothermal Simulation Results for the Die with Constant Electric Resistivity vs. T and with Constant Resistivity.

Temperature (°C)	$\boldsymbol{R_{On} = 1.24\Omega}$	$\boldsymbol{R_{On} = -0.0004\, T^{1.385} + 1.271}$
Junction	216.6	180.3
Solder	208.7	175.5
DBC	161.6	147.55

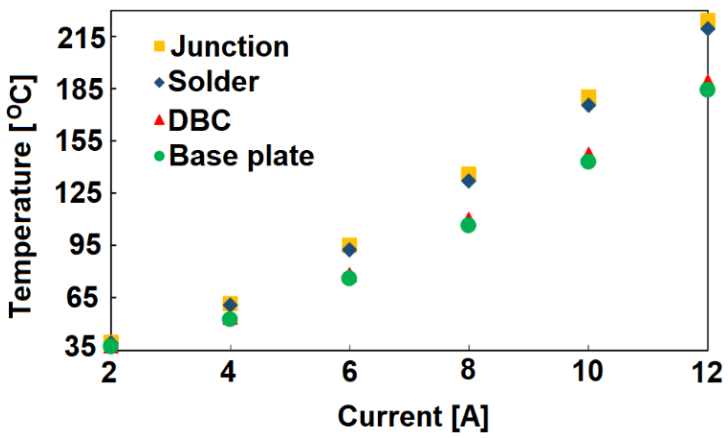

Figure 5-7: The calculated temperature at different locations of the power module vs. different load currents.

5.3 Conclusions

The compact packaging design of envisaged high voltage WBG power modules brings many challenges in terms of thermal management and electric field enhancement. The thermal issues within the power module originated from the heating of the chips in their on-state while electric stress occurs at the off-state of the chips and close to their breakdown voltage. To ensure reliable operation of WBG power modules in both states, accurate thermal and electric field analyses are essential. In this chapter, a packaging design with a double-sided cooling system and parallel metal posts to hold 10-kV SiC PiN diodes on a DBC made from AlN is presented. Through FEM electric field simulations in COMSOL Multiphysics, the thickness of AlN was determined. In the thermal side, through FEM simulations carried out in COMSOL Multiphysics combined with thermal network analysis developed in PLECS, the convectional coefficient of the cooling system and the junction temperatures for different loads were obtained and for the proposed packaging

design, a maximum load current of 90 A for the module has resulted. The findings of this chapter were presented in [95].

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The trend towards more and all electric apparatuses and more electrification will lead to higher electrical demand. Increases in electrical power demand can be provided by either higher currents or higher voltages. Thanks to weight and voltage drop, an increase in current is not preferred; therefore, higher voltages are being regarded. Another trend is to reduce the size and weight of apparatuses. Combined, these two trends result in the high-voltage, high-power-density concept.

It is expected that by 2030, 80% of all “electric power” will flow through “power electronics conversion systems”. In regards to the high-voltage, high-power-density concept described above, WBG power modules made are considered to be the most promising solution to reducing the size and weight of power electronics conversion systems. For WBG power modules, along with the trend towards “higher breakdown voltage capability”, known as the “blocking voltage”, “volume reduction” and, thus, “power density” increases have also been targeted. This leads to extremely “high electric

stress" of extremely nonuniform ones inside the module, resulting in unacceptable PD levels and, in turn, insulation degradation and, eventually, breakdown of the module. Thus, current and future challenges are to address this high electric stress within modules, which is the subject of this Ph.D. work.

For the first time, a systematic method for the "electrical insulation design" of a "high voltage high-density power module" and addressing "high electric stress" within power modules was developed that met the requirements of both the "one-minute insulation test" and the "PD test" according to IEC 61287-1. The models and simulations were developed and carried out in "COMSOL Multiphysics". Defining different zones for meshing where the zones including more sharp edge electrodes have a denser mesh and considering measuring lines and points and at a proper distance from interfaces and edges ensures precise results when comparing different electric field grading methods.

When electric field reduction and grading for design purposes, the key question is how much we should reduce the electric field stress in the module? In other words, a criterion as allowable electric field stress in the module should be defined. A method, for the first time, was developed in this thesis to define this criterion based upon precise dimensions of a "power module" and its PD measurement where the measured average PDIV value at continuous 10 pC discharges for "encapsulated industrial substrates" with a 1 mm-thick "AlN ceramic" from one manufacturer was 4.7 kV. Based on IEC 61287-1, the PD level for "power modules" must not exceed 10 pC. This indicates that the maximum permissible E in "silicone gel" and "AlN ceramic" can be determined and used as a design criterion for electrical insulation. In other words, if E_{Max} in "silicone gel" and "AlN ceramic" for any "WBG module packaging" design is less than the maximum determined,

then the PD level of that module is less than 10 pC, assuming that the same material quality and manufacturing process of existing modules will be used for "WBG modules". Then, by developing the model, the permissible maximum E values in AlN and silicone gel was determined to be 15.98 and 17.48 kV/mm, respectively. These two E values were used as criterion for the "electrical insulation design of envisaged WBG power modules" to pass the PD test (<10 pC).

Simulation results verified that "geometrical techniques" including 1) "metal layer offset", 2) "protruding substrate", and 3) "stacked substrate design", either individually or combined, cannot meet the criterion values for compact packaging. It was shown, for the first time, that a combination of the aforementioned geometrical methods and applying a "nonlinear FDC layer" could meet the criterion values for power modules with high blocking voltages up to 30-kV power module where for example, an electric field reduction of 66% and 91% in the AlN substrate and silicone gel, respectively was achieved through the proposed method in comparison with using the protruding substrate design alone.

The big question that remained unanswered is whether or not electric field simulations are valid for "high-temperature" and "high-frequency" conditions. The electric field simulations and calculations reported in the literature to date ignore the "frequency and temperature dependency" of ε_r and σ_{ac} for the "insulating materials" used in the "power modules". Therefore, there is doubt about the validation of results for high temperatures and high frequencies. In this Ph.D. work, this technical gap was also addressed where a "frequency- and temperature-dependent finite element" method (FEM) model up to 250°C and 1 MHz of the insulation system envisaged for high voltage, high-density WBG power module. The module modeled had a blocking voltage of 6.5 kV, where

a “protruding substrate” combined with the application of a “nonlinear FDC layer” was considered to address the high field issue. By making use of this model, the effect of frequency and temperature on the effectiveness of the proposed “electric field reduction” method was studied and it was found that the effectiveness of our proposed “electric field reduction” method is not affected.

Besides high electric issue, thermal management in next-generation WBG modules is a big challenge. For this, knowing the precise temperature at different points of a module is needed. Although the cause of this heat is electrical due to 1) conduction loss in the on-state situation and 2) switching losses, the thermal analysis reported in the literature has been done through an assumed power density, independent from electrical effect, and thus leading to inaccurate evaluation. To address this issue, a combination of FEM simulations in COMSOL Multiphysics and RC network modeling developed in a circuit simulator was developed to obtain temperature distributions within the modules. The method was used to design the packaging for a 10-kV module consisting of 9 SiC PiN diodes. The temperature-dependency of the electrical characteristics of the chip was considered and for considered dimensions, a maximum load current of 90 A was determined.

6.2 Future Work

Insulation materials and systems that are currently working well for Si-based power devices will be insufficient for the envisioned high voltage, high-density WBG power modules. Reasons are due to a combination of 1) a high electric field, 2) exposure to high slew rates (dv/dt) (ranging from tens to hundreds of kV/μs) and repetitive (frequencies ranging from hundreds of kHz to MHz) voltage pulses, and 3) operation at high temperatures up to 500°C. These working conditions create an extremely high electrical

and thermal stress working environment for dielectrics in next-generation WBG-based power devices that are not experienced in Si-based power devices. Thus, there is a vital need to develop new dielectrics and design novel insulation systems for WBG power devices. The technology today uses packaging elements such as ceramic substrates, brazing and wire bonding, and passivation, which may be operated at up to 600°C, 300°C and 250°C, respectively. In this regard, silicone gel that is commonly used as encapsulation materials has an even lower operating limit of 200°C or 175°C over long periods. Moreover, PDs in silicone gel tend to reduce its insulation capabilities and silicone gel has very limited self-healing properties compared to liquids. In this regard, high-temperature liquid dielectrics may be game-changing and enable us to address packaging WBG devices. Moreover, liquids can enhance cooling by convection, and/or electroconvection due to Electrohydrodynamics (EHD) motion. Combinations of nonlinear FDC layers, geometrical techniques, and high-temperature liquid dielectric to address both high electric field issue and high temperature issue within envisaged high voltage high-density WBG power modules can be envisaged and for that the electric field grading methods developed in this Ph.D. work can be used.

The insulation materials used in (next-generation) "WBG power modules" (will be) are exposed to high frequency (a switching frequency up to 500 kHz), fast (a dv/dt up to 100 kV/μs) square wave voltages that may result in a different aging status from that exposed to a 50/60 Hz AC voltage. However, the only existing standard and criterion to evaluate PD performance of "power electronics modules" is IEC 61287-1 that is based on applying a 50/60 AC voltage. Next research can be conducted to see whether or not IEC 61287-1 reflects actual aging condition under slew rate and frequencies mentioned above

and then whether the electric field grading methods developed in this thesis work for those conditions.

In the material science and engineering side, efficient processing techniques should be developed to deposit thin nonlinear FDC composites on high fields regions within the module.

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Publications

Journal Papers (3 papers):

1. M. M. Tousi and M. Ghassemi, "Combined geometrical techniques and applying nonlinear field dependent conductivity layers to address the high electric field stress issue in high voltage high-density wide bandgap power modules," *IEEE Trans. Dielectrics and Electrical Insulation*, vol. 27, no. 1, pp. 305-313, February 2020.

2. M. M. Tousi and M. Ghassemi, "Nonlinear field dependent conductivity for electric field grading in wide bandgap power electronic modules," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 343-350, March 2020.

3. M. M. Tousi and M. Ghassemi, "The effects of frequency and temperature on electric field mitigation method via producing substrate combined with applying nonlinear FDC layer in wide bandgap power modules," *Energies*, vol. 13, no. 8, p. 2022, April 2020.

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1. M. M. Tousi and M. Ghassemi, "Electric field control by nonlinear field dependent conductivity dielectrics characterization for high voltage power module packaging," *IEEE International Workshop on Integrated Power Packaging (IWIPP)*, Toulouse, France, pp. 54-58, April 24-26, 2019.

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