CHAPTER III

Solder Joint Reliability Assessment

3.1 Introduction 83

3.1.1 Current Approach for Studying Solder Joint Fatigue Failure 84
3.1.2 Solder Joint Fatigue Models 85

3.2 Experimental Procedures 88

3.2.1 Accelerated Temperature Cycling Test 89
3.2.2 Tensile and Shear Tests 93
3.2.3 Failure Analysis 96

3.3 Experimental Results 108

3.3.1 Results on Tensile and Shear Tests 108
3.3.2 Results on Temperature Cycling Test 119

3.4 Discussion 141

3.4.1 Solder Joint Fatigue Failure Physics 141
3.4.2 Effects of Solder Joint Shape and Height on Thermal Fatigue 148

3.5 Summary and Conclusions 160

3.6 References 162

3.1 Introduction

The reliability of a component or system is the probability that the component or system performs its intended function under stated conditions for a specified period of time [1]. Reliability is a function of time and it is estimated by observing the fraction of a population of components surviving at time t. There are three periods of failure rate-decreasing fail rate, constant failure rate, and increasing fail rate, which give rise to the so-called “bathtub” curve, as shown in Figure 3.1 [1].

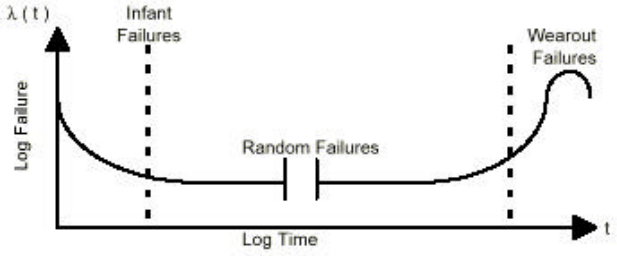


Figure 3.1. The “Bathtub” failure rate [1].

Thermal fatigue failure caused by the CTE mismatches among silicon chip, substrate, and solder joint is the dominant failure mechanism in solder joint interconnections. In this chapter, we evaluate the reliability of the produced solder joints for power chip interconnection. First, the current solder joint fatigue study approaches are introduced and the popular solder joint fatigue models of solder joint reliability assessment and life prediction are briefly reviewed. Accelerated temperature cycling test as well as tensile and shear tests on solder joint assembly with different solder joint configurations are described and the failure analysis methods were then elaborated. Finally, we present the experimental results and discuss the solder joint fatigue failure behaviors.

3.1.1 Current Approach for Studying Solder Joint Fatigue Failure

The fatigue failure of solder joints and their life prediction are one of the most important issues of solder joint reliability. In terms of fatigue failure of solder joints, current paradigm for assessing the in-service reliability of electronic packages is based on thermal/mechanical cycling and thermal shock tests with the humidity, which is a time-consuming practice. Therefore, the accelerated testing becomes more important and is the focus of intensive research area recently, driven by short-time-to-market and low-cost. Rapid reliability assessment is highly desirable for electronic manufacturing industries. It has long been known that solder fatigue life under the high homologous temperature cycling is difficult to predict due to the time/rate/temperature-dependent viscoplastic behaviors of solder alloys. The complicated geometry of solder joints makes the task more difficult. Moreover, thermal fatigue life of solder joints under accelerated test conditions also depends on extreme temperatures (maximum and minimum temperatures), temperature ramping rates, dwell time and dwell temperature, evolution of solder microstructures, presence of intermetallics, soldering defects, and residual strains due to processing.

The definition of fatigue failure of a solder joint plays a critical role in understanding the failure mechanisms and the fatigue models. There are, in fact, wide discrepancies on the failure definition in literature. For instance, expedient fatigue failure criteria include complete electrical circuit opens, a 50% reduction in the measured stress amplitude on the solder joint, and a 20% crack propagation across the solder joint.

Current engineering approaches for solder joint reliability assessment include the methodologies of the life prediction, computer modeling, and accelerated testing of solder joints

under various accelerated hygro-thermal-mechanical testing conditions. Early solder joint fatigue models were developed based on experimental thermal cycling tests. Most models that address fatigue require stress-strain data in order to predict service life. Early fatigue data was collected experimentally using strain gauges. However, with the decreasing size of the solder joint, experimental collection of stress-strain data is becoming increasing difficult, and finite element analysis (FEA) is becoming more and more important in obtaining stress-strain relationships. Therefore, fatigue modeling is becoming the dominant approach in solder fatigue evaluation. The general approach to fatigue modeling consists of four primary steps. First, a theoretical or constitutive equation, which forms the basis for modeling, is either defined or chosen. Appropriate assumptions need to be made in constructing the constitutive equation. Second, the constitutive equation is translated into a FEA program and a model created. The FEA program calculates the predicted stress-strain values for the system under study and returns stress values for the simulated conditions. Third, the FEA results are used to create a model predicting the number of cycles to failure, N_f. Fourth, the model or results be verified experimentally.

3.1.2 Solder Joint Fatigue Models

Solder joint fatigue models are developed based on experimental stress/strain/energy data from thermal/mechanical cycling tests. A number of life prediction approaches have been proposed for solder joint fatigue during the past few years. These approaches can be classified into four major categories: (i) plastic strain-based approach; (ii) creep strain-based approach; (iii) energy-based approach; and (iv) fracture mechanics-based approach, based on the fundamental mechanism viewed as being responsible for inducing damage. There could have a stress-based classification based on the application of a force or stress to a component, causing a resultant strain. Stress-based approach is less used in practice although it can be useful for vibration or physically shocked or stressed components. In literature, there is wide disagreement in these fatigue models. Some authors and their work favor this model, some favor other models. There is no single dominant model though plastic strain-based model (Coffin-Manson) is the most popular one.

3.1.2.1 Plastic Strain-Based Approach

The well-known Coffin-Manson equation is plastic strain based method for low cyclic fatigue [2-3]. The method has been widely used for fatigue life prediction of many solder alloys subjected to shear strain-dominated deformation [4]. This model predicts failure based on calculation or experimental determination of the applied plastic shear strain. Coffin-Manson (C-M) equation is:

$$N_f = q(\Delta g_p)^{-f} \qquad \text{Equation 1}$$

where N_f is the number of cycles to failure; $\Delta\gamma_p$ is plastic strain range and θ and ϕ are material constants. For solder joints, θ is about 1.3 and ϕ is about 1.9 [5-6].

In order to account for frequency effect, a frequency-modified version of the Coffin-Manson equation was also proposed [2]. Because C-M equation considers only plastic deformation, it is sometimes (e.g. Basquin's model) combined to account for elastic deformation as well, thus the resulting total strain replaces the plastic strain. Also Miner's model account for creep strain. However, each of the plastic strain-based models considers plastic deformation as the main driving force for fatigue failure. All of the plastic strain-based fatigue models require some form of geometry specific data to calculate the fatigue life. This information comes from FEA or from experimental work. The C-M formulation, not intended for deformation modes other than plastic distortion, can not adequately predict thermal fatigue of solder joint, the very nature of which has time depend creep deformation [7].

3.1.2.2 Creep Strain-Based Approach

Creep strain-based approach account strictly for the creep deformation phenomenon involved in solder joints. For solder joints, it is commonly accepted that creep may be due to grain boundary sliding and/or matrix creep (dislocation movement). Knecht and Fox have proposed a simple matrix creep fatigue model relating the solder microstructure and matrix creep shear strain range as [8]

$$N_f = \frac{C}{\Delta g_{mc}} \qquad \text{Equation 2}$$

The number of cycles to failure, N_f, is related to a constant C, which is dependent on failure criteria and solder joint microstructure. $\Delta\gamma_{mc}$ is the strain range due to matrix creep.

The second creep mechanism, grain boundary sliding, is incorporated with matrix creep into a fatigue model by Syed [9-10]. In this model, creep strain is partitioned into two parts as [9],

$$N_f = ([0.022 D_{gbs}] + [0.063 D_{mc}])^{-1} \quad \text{Equation 3}$$

where D_{gbs} and D_{mc} are the accumulated equivalent creep strain per cycle for grain boundary sliding and the matrix creep, respectively. It has been reported [10] that a complex number of parameters including dwell times, ramp rate, hold times, high temperature extremes, and low temperature extremes affects the fatigue lifetime of solder joint. One limitation in the creep-based models is the absence of plastic strain effects. Actually plastic strain effects can be neglected only of the strain rate is low enough to be neglected, thus resulting in a constant stress-situation and the strain is indeed time-dependent.

3.1.2.3 Energy-Based Approach

The energy models are used to predict fatigue failure based on a hysteresis energy term or type of volume-weight average stress-strain history. The energy absorbed by an interconnection in a thermal cycle is numerically equal to the non-recoverable work, expressed as the summed product of the various force components acting on the element and the resulting nonreversible displacement amplitudes. This energy, which may be considered a measure if damage accumulation, is dissipated non-uniformly throughout the interconnection, depending on the geometric stress distribution. The fundamental assumption of the energy theory of fatigue is that fracture will occur when the energy accumulated in the susceptible region-which dissipates the most energy per unit volume per cycle-reaches a critical value. Several strain energy-based methods have been applied to the fatigue life prediction of solder joints [11-12]. The general form of energy-based models can be expressed as

$$N_f = C(W)^{-d} \quad \text{Equation 4}$$

where δ and C are the material constants. W is inelastic strain energy density. Some authors use total strain energy density which consists of elastic, plastic and creep strain energy density in the above equation [13].

3.1.2.4 Fracture Mechanics-Based Approach

Fracture mechanics approach assumes a microscopic flaw or crack initiator exists in any solder joint and begins to grow from the beginning of thermal cycle. The fatigue life of crack

propagation from a tiny crack to final joint failure electrically and/or mechanically can be a significant portion of whole fatigue life. Therefore, fracture mechanics approaches may play an important role in characterizing the crack behavior and thus can lead to the formulation of life prediction method. Fracture mechanics describes the progression of a crack though a stressed material as a function of time, geometry, and environmental conditions. Crack growth velocity is given by the basic equation [14-15]

$$\frac{da}{dt} = B(Ys\sqrt{pa})^n \qquad \text{Equation 5}$$

Where a is the crack length, σ is the stress, Y is a geometry parameter, B and n are empirical constants which vary with ambient.

Paris-Erdogan equation gives the crack propagation per cycle [16]

$$\frac{da}{dN} = C\Delta K^q \qquad \text{Equation 6}$$

where a is the crack length, ΔK equaling $\Delta t\sqrt{pa}$ is the stress intensity factor.

3.2 Experimental Procedures

The reliability of fabricated solder joints in this study was evaluated by accelerated temperature cycling test and adhesion tests. During the temperature cycling, in-process electrical resistance measurement and nondestructive evaluations such as scanning acoustic microscopy and optical microscopy were conducted to monitor solder joint failure behaviors. Destructive tensile and shear tests were performed on as-processed solder joint assembly samples as well as temperature cycled samples to investigate the adhesion strength of different solder joint configurations and study the adhesion strength change and fracture behavior of these solder joint configurations as a result as temperature cycling. Before and after fatigue failure, the solder joints were characterized and failure modes were analyzed. Figure 3.2 is the experimental procedure flowchart for solder joint reliability assessment of this study.

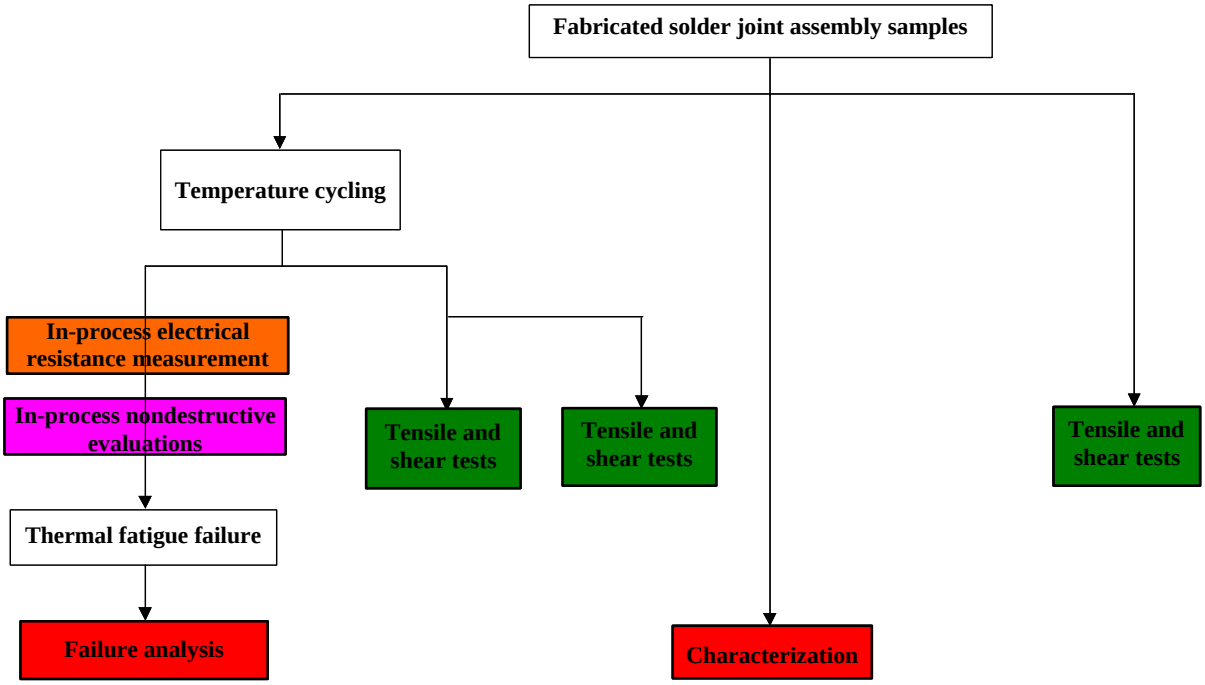


Figure 3.2. Experimental procedure flowchart for solder joint reliability assessment of this study.

3.2.1 Accelerated Temperature Cycling Test

Temperature cycling test is one of the most important tests used to assess the reliability of solder joint interconnection. The objective of temperature cycling test is to assess the resistance and robustness of the package structure to exposures at extremes of high and low temperatures and to the effect of alternate exposures to these extremes. Our temperature cycling test was conducted in Envirotronics thermal cycling chamber in which the environment temperature periodically changes from hot to cold. The test samples were removed from the chamber and were tested and characterized periodically for integrity.

3.2.1.1 Evaluation Method and Criterion

The electrical resistance of the solder joint interconnections was measured during the temperature cycling to tell if there is failure of the solder joints. Four-point probe method, which is described below, is used in measuring the solder joint resistance. When there is significant crack in the solder bump, the electrical resistance will increase. As introduced earlier, there is no standard failure criterion for flip chip solder joint interconnection. For our temperature cycling test, we set our own criterion as 20% electrical resistance increase, that is, when the resistance has 20% increases, we regard the solder bump interconnection fails.

Four-point method is a popular way in measuring solder bump resistance. The testing principle is indicated in Figure 3.3. The testing involves three solder bumps. For example, we want to measure the resistance of the middle solder bump. We can let current flows through trace A (T_a), through bump 1, over the trace of the chip, down bump 2 and out of trace B (T_b). There is no current flow through traces C (T_c) and D (T_d). Furthermore, bump 3 and Td are at the same potential as the top of bump 2. Also T_c is at the same potential as the bottom of bump 2. Therefore, any potential difference measured across T_c and T_d would represent the potential drop across bump 2. Given the current flowing through bump 2 and the measured potential difference across T_c and T_d, the bump resistance can be calculated.

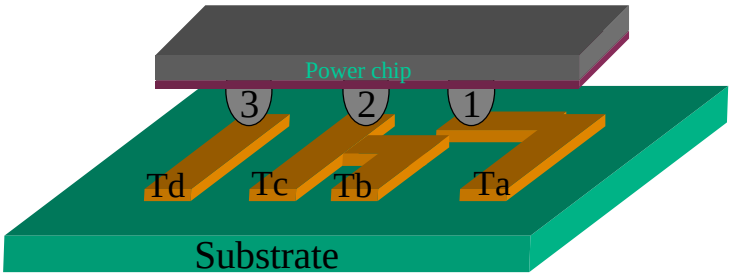
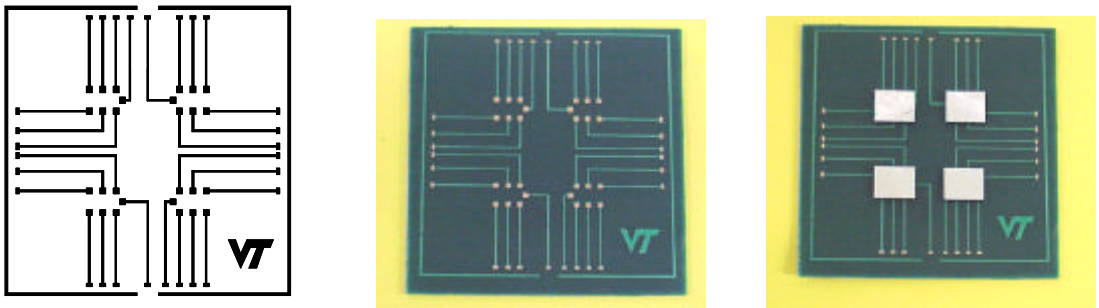


Figure 3.3. A schematic illustration showing the measurement of solder bump resistance.

Simple test vehicle has been designed and built in order to characterize solder bump interconnection of power devices and evaluate solder joint reliability. Figure 3.4 shows the test vehicle deign and hardware. We can see that this test vehicle can be used to measure solder joint resistance using four-point method.



(a) (b) (c)

Figure 3.4. (a) The test vehicle design; (b) picture of the test vehicle; and (c) flip chip under test in the test vehicle.

3.2.1.2 Test Samples

Two sets of samples were performed temperature cycling test. For both sets of samples, there are seven solder joints on each silicon chip. The chip dimensions and solder joint locations

are shown in Figure 3.5. All the test samples were flip chip attached to the test vehicle introduced above which is made of rigid printed circuit board. Figure 3.6 shows an example of the temperature cycling samples.

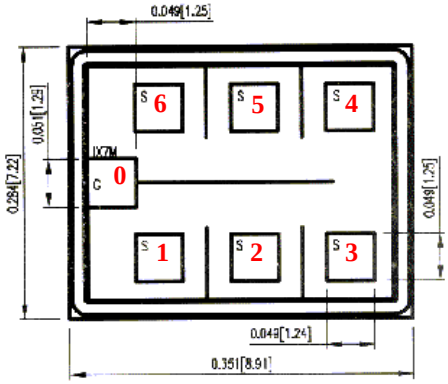


Figure 3.5. Dimensions and solder joint locations of temperature cycling test chips [17].

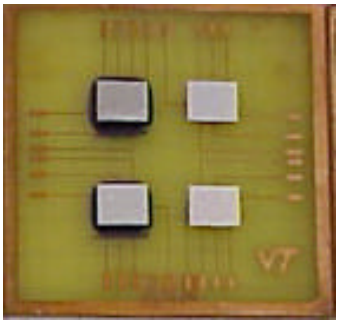


Figure 3.6. Example of the temperature cycling samples.

For the first set of samples, there are four different solder joint configurations, which is illustrated in Figure 3.7. They are single bump barrel-shaped solder joint without underfill, single bump barrel-shaped solder joint with underfill, triple stacked hourglass/column-shaped solder joint without underfill and triple stacked hourglass/column-shaped solder joint with underfill. For the former two configurations, only one sample was tested, that is, 7 solder joint were tested for each case. For latter two configurations, two samples were tested, that is, 14 solder joint were tested. The temperature cycling condition is set as: Temperature range: 0°C and 100°C; Temperature raise rate: 10°C/min; Dwell time at 100°C: 5 min; Temperature fall rate: 10°C/min; Dwell time at 0°C: 5 min. However, we monitored the temperature close to the sample and found that the real temperature is exactly same as what we set. The real temperature profile close to the sample is shown in Figure 3.8.

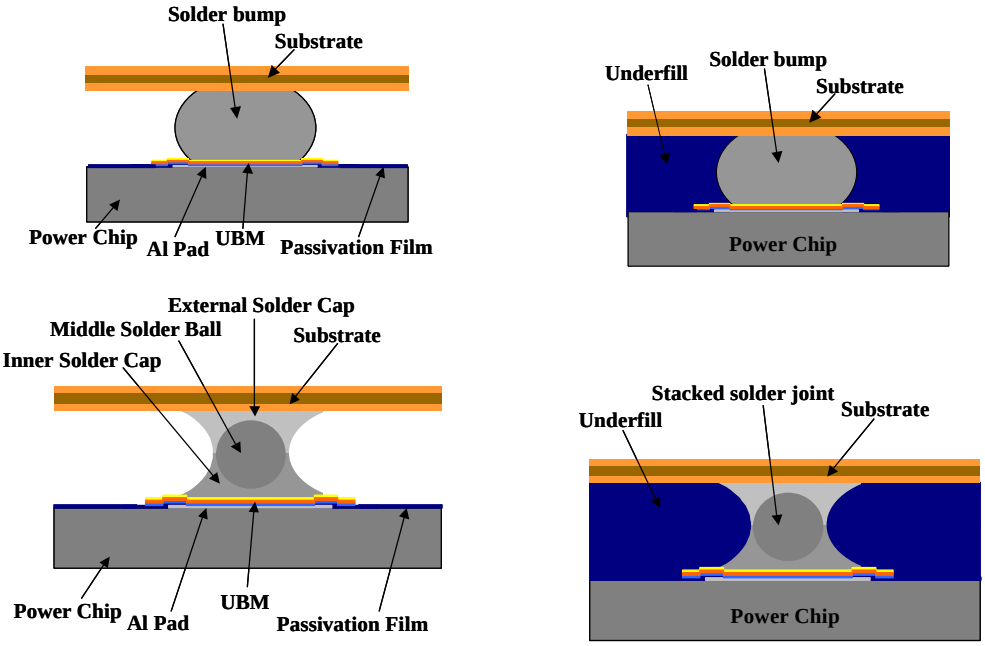


Figure 3.7. Solder joint configurations for the first set of temperature cycling samples.

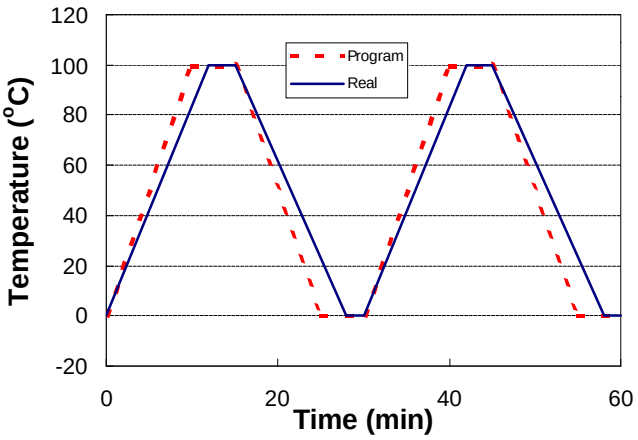


Figure 3.8. Programmed temperature cycling temperature profile and real temperature profile for the first set of samples.

For the second set of samples, there are three different solder joint configurations, which is illustrated in Figure 3.9. They are single bump barrel-shaped solder joint, triple stacked barrel-shaped solder joint, and triple stacked hourglass/column-shaped solder joint. All of them are not underfilled. For each configuration, three samples were tested, that is, 21 solder joint were tested. The temperature cycling condition is set as: Temperature range: -40°C and 125°C; Temperature raise rate: 6.6°C/min; Dwell time at 125°C: 5 min; Temperature fall rate: 6.6°C/min; Dwell time at -40°C: 5 min. However, we monitored the temperature close to the

sample and found that the real temperature is exactly same as what we set. The real temperature profile close to the sample is shown in Figure 3.10.

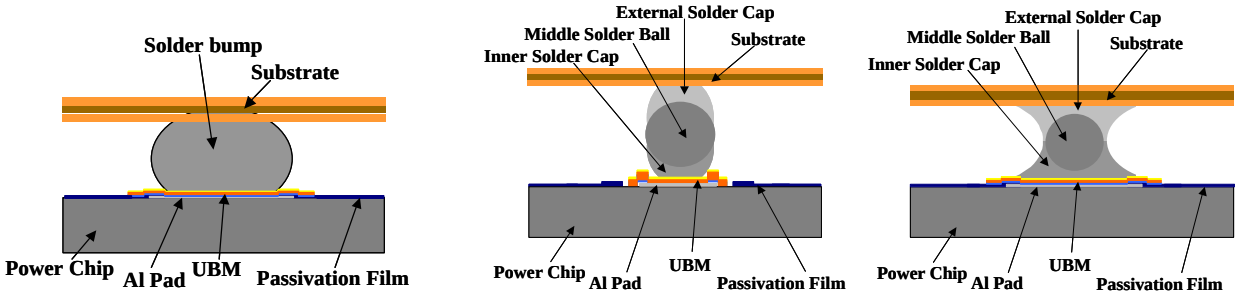


Figure 3.9. The solder joint configurations for the second set of temperature cycling samples.

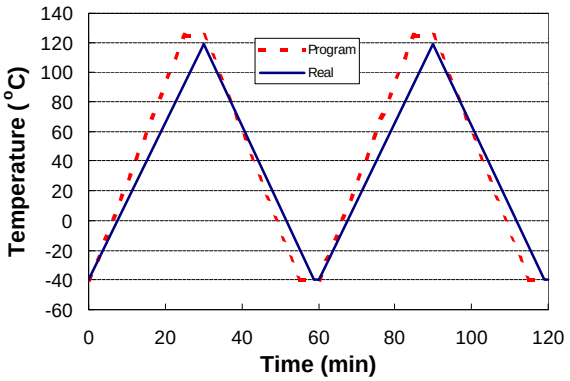


Figure 3.10. Programmed temperature cycling temperature profile and real temperature profile for the second set of samples.

3.2.2 Tensile and Shear Tests

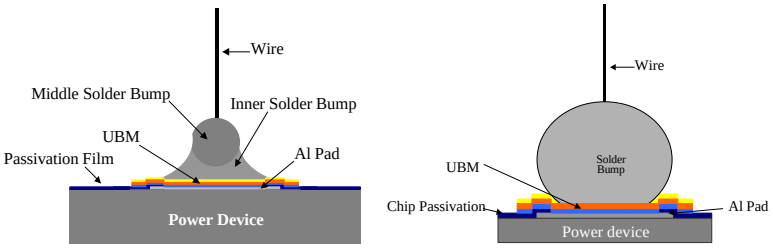
The adhesion between the interfaces of the Al pad and UBM film, the UBM film and solder joint, and solder joint and substrate pad is critical to flip chip and BGA assembly since these are the most vulnerable interfaces. It is very important to test the bonding strength of the solder joints.

Tensile and shear tests were conducted on both stacked solder bump and conventional single solder bump for comparison. Also both in-house sputtered UBM Cr/Cu and vendor-supplied solderable devices (Ti/Ni/Ag UBM) were used. For both stacked solder bump and conventional single solder bump, the chip and pad size is designed to be same. The testing was performed on a 4505 Instron machine controlled through its GPIB interface using LabVIEW software. Figure 3.11 shows the Instron machine. An appropriate load cell was selected for

different samples and the samples were loaded at a crosshead displacement rate of 1 mm/min. Utilizing LabVIEW software, the load at break was recorded. The load value is supposed to increase with the increasing displacement linearly within the elastic region. As the load versus displacement curve deviates from linearity, it comes to the plastic region. When the load reaches a maximum and begins to decrease rapidly, the solder joint has achieved a maximum loading level and begins to break.

Figure 3.11. Instron machine used for adhesion test.

After solder bumping process, we did tensile tests. In order to do the testing, thin wires were soldered on top of the solder bumps. Figure 3.12 illustrates the tensile test samples for bumped chips. For these samples, A 100 Newton load cell was selected.



(a) (b)

Figure 3.12. Tensile test samples after solder bumping. (a) Stacked solder bump; (b) conventional single solder bump.

The tensile tests on bumped chip actually test the adhesion strength of the interfaces between the Al pad and UBM, and UBM and solder joint. In order to investigate the tensile and shear loading behavior of the complete joint and study the tensile and shear loading behavior after the samples are exposed to a certain number of temperature cycling, the solder bumped chips were flip chip bonded a rigid printed circuit board. Tensile and shear tests were conducted

on both stacked hourglass-shaped solder joints and single barrel-shaped solder joints before and after 800, 1200 temperature cycles. The temperature cycling condition is: Temperature range: -40°C and 125°C; Temperature raise rate: ~6°C/min; Dwell time at 125°C: 2 min; Temperature fall rate: ~6°C/min; Dwell time at -40°C: 2 min. Figure 3.13 shows tensile and shear test chip configuration. For each test chip, there are seven pads. Solder mask is applied to define the solder bump contact area and seven solder joints were formed on the seven pads. Figure 3.14 illustrates the tensile test structures for both stacked hourglass-shaped solder joints and single barrel-shaped solder joints. A test fixture is attached to the backside of the chip using adhesive. During the tensile test, the PCB is clipped on a flat station of the Instron machine and the fixture is connected to load cell. For shear test, double lap joint configuration is chosen instead of single lap joint. In symmetrical double lap joints, our-of-plane normal stresses can be much reduced while in single lap joint, the bending moment which increases the principal tensile stress is very significant. Therefore, symmetrical double lap joints structure is closer to pure shear test. Figure 3.15 shows the double lap joints shear test structure we used in our experiment. For these samples, A 1000 Newton load cell was used since these samples have seven solder joints and higher load is needed to break these solder joints.

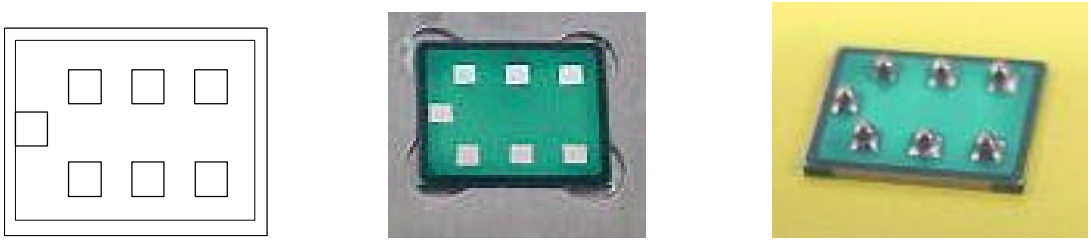


Figure 3.13. Tensile and shear test chip configuration.

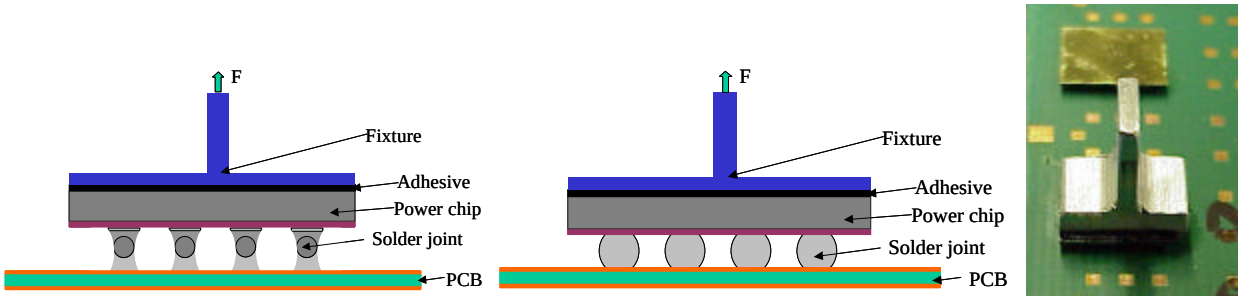


Figure 3.14. Schematic of tensile test structures and a photograph of test sample.

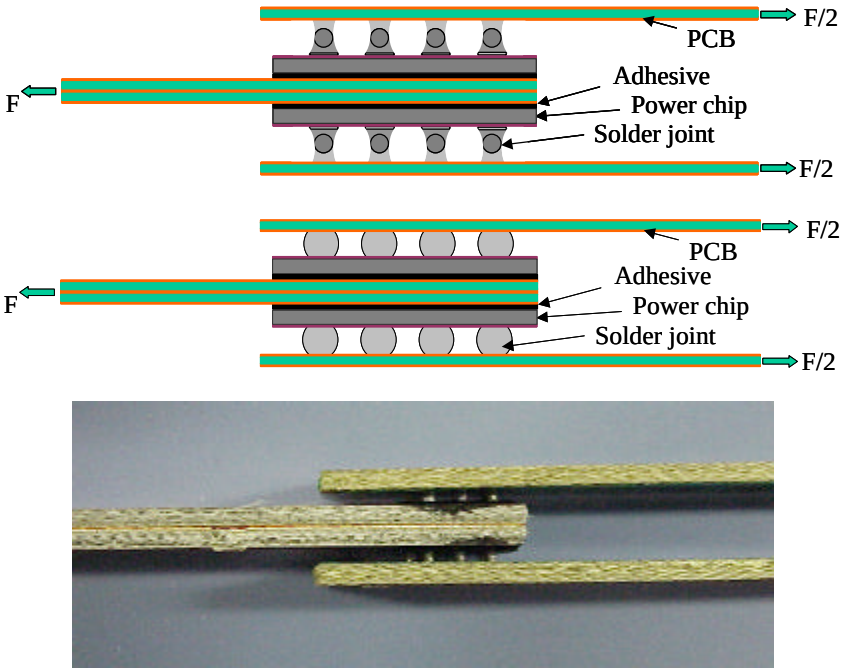


Figure 3.15. Schematic of double lap joints shear test structure and a photograph and test sample.

3.2.3 Failure Analysis

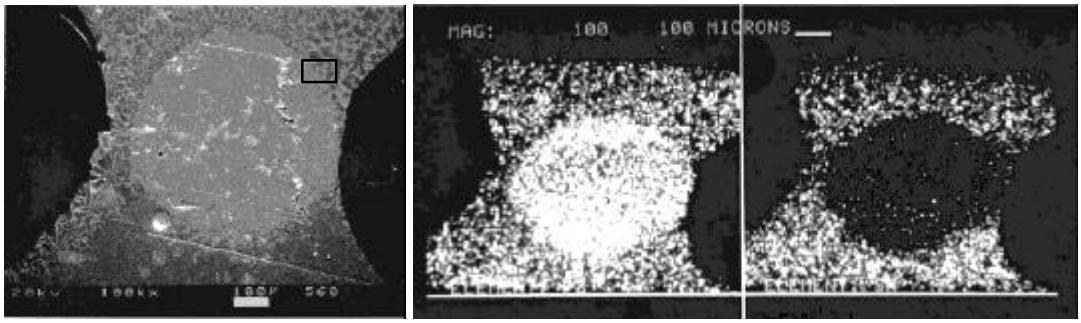
Generally, the weakest interface in flip chip assembly is the interface between solder bump and silicon chip. The triple-stacked high standoff solder joints are developed to improve reliability. However, for stacked solder joints, failure could come first inside triple-stack solder joint since it is composed of three layers and has two interfaces. The interfaces as well as the failed structures of the solder joint configurations were examined using scanning electron microscopy (SEM), energy dispersive X-ray analysis (EDX) and optical microscopy for the integrity of the joints and fatigue failure modes. Acoustic microscopy imaging (nondestructive evaluation) is utilized to examine the quality of the bonded interfaces and to detect cracks and other defects before and during accelerated fatigue tests.

3.2.3.1 Interface Characterization

Generally, the weakest interface in flip chip assembly is the interface between solder bump and silicon chip. The triple-stacked hourglass solder bump was developed to reduce the stress concentration at the interface. However, failure could come first from the triple-stack solder joint since it is composed of three bumps and has two interfaces. Figure 3.16 (a) shows

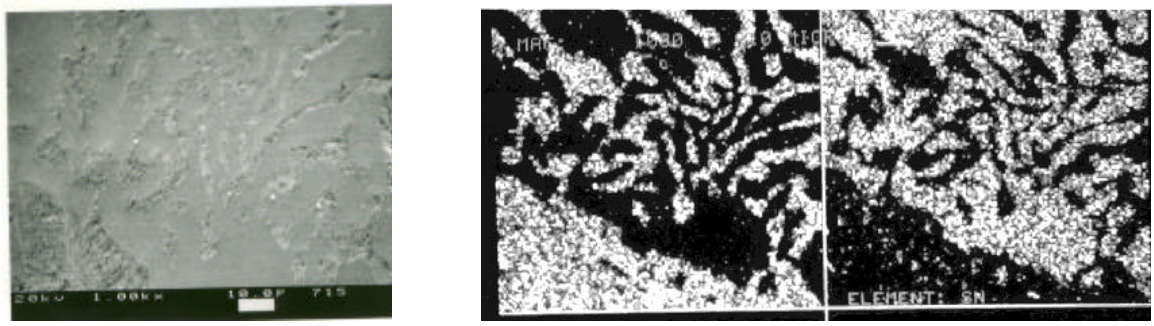
the SEM picture of the triple-stacked solder joint and Figure 3.16 (b) shows the corresponding EDX mapping.

Figure 3.17 shows the high-magnified interface (the box in Figure 3.16 (a)) between middle solder ball (Sn10/Pb90) and outer solder cap (Sn63/Pb37). The left EDX picture shows the Pb element EDX mapping, while the right one shows the Sn element mapping. SEM results reveal that the interfaces between the three solder bumps for as processed triple-stacked solder bump structure are consistent. EDX results show that the boundaries of different solder compositions are obvious and it shows that there is not much diffusion between the different solder compositions. This indicates that the interfaces should be strong.



(a) (b)

Figure 3.16. (a) SEM picture; (b) EDX mapping of the triple-stacked solder bump structure.



(a) (b)

Figure 3.17. (a) SEM picture; (b) EDX mapping of the interface between middle solder bump (Sn10/Pb90) and external solder bump (Sn63/Pb37).

3.2.3.2 Crack and Defects Detection using Scanning Acoustic Microscopy

In recent years, scanning acoustic microscopy (SAM) has being found to be a very successful technique to evaluation the reliability of electronic packages. SAM is a non-

destructive imaging technique, which can detect voids and defects in materials. We have used 75MHz C-SAM (Sonix system) to detect cracks and monitor crack propagation in flip chip solder joints during temperature cycling. In this section, we introduce the fundamentals of acoustic microscopy imaging and give an example of tomographic acoustic micro imaging, which we used in this research, on flip chip solder joints.

3.2.3.2.1 Introduction to Acoustic Microscopy Imaging [18]

When an ultrasonic wave is incident on an interface between two different materials, part of the wave is transmitted while the other part is reflected. The amplitude, time of flight and polarity of the reflected signal provide crucial information about the material, which reflected the acoustic signal. Reflection of an acoustic signal is governed by acoustic impedance of a material, which is the ratio of the acoustic pressure to the particle velocity per unit area; acoustic impedance is defined as the following,

$$\mathbf{Z_i = \rho_i . v_i}$$

where, Z_i = acoustic impedance of the material in the i_{th} layer, ρ_i = density of the material in the i_{th} layer, and v_i = velocity of sound in the i_{th} layer.

Figure 3.18 illustrates the phase inversion principle of acoustic imaging, where an ultrasonic wave is incident on an ideal interface. The amplitude of the incident, reflected and transmitted waves are P_I, P_R and P_T respectively. The materials are assumed to be ideal elastic solids with boundary conditions such that the acoustic pressure and velocity in both materials are equal at the interface and the frequency remains unchanged across the interface. The reflected and transmitted pressure amplitudes can be expressed as the following where Z_1 and Z_2 are the acoustic impedances of materials 1 and 2.

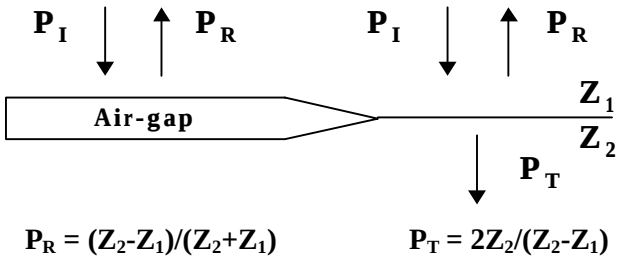


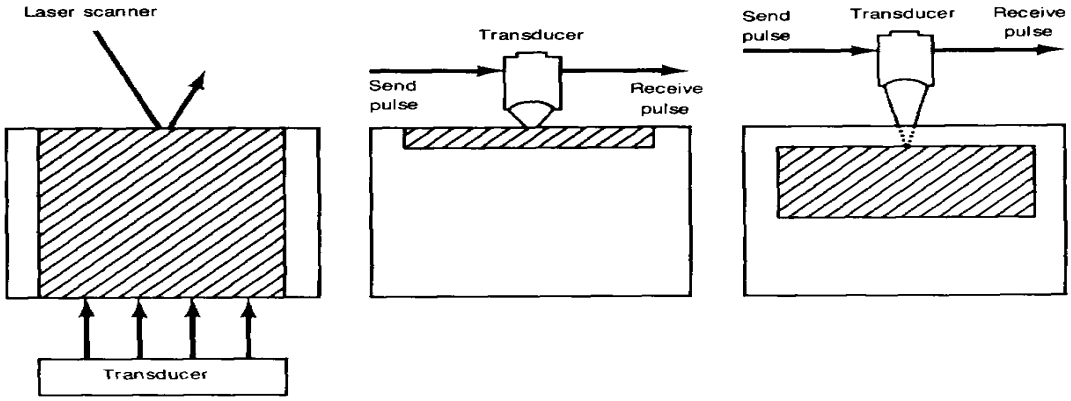
Figure 3.18. Reflection from an air-gap and at a bonded interface

In the following table, acoustic impedances of a few materials are listed.

Table 3.1. Acoustic Impedance of Common Packaging Materials [19]

Material	Density	Wavelength (mm) at 25 MHz	Acoustic Impedance (10^6 kg/sec-m^2)
Air (20°C)	0.00	0.014	0.00
Alumina	3.8	0.416	39.56
Aluminum	2.70	0.25	16.90
Copper	8.90	0.188	41.83
Epoxy Resin	1.20	0.104	3.12
Glass (Quartz)	2.70	0.223	15.04
Molding Compound	1.72	0.157	6.76
Silicon	2.33	0.344	20.04
Water (20°C)	1.00	0.059	1.48

There are three types of acoustic microscopes that are utilized in most common applications to study and evaluate interfaces -- the scanning laser acoustic microscope (SLAM); SAM; and the C-mode scanning acoustic microscope (C-SAM). All of the instruments use high frequency ultrasound to detect internal discontinuities in materials and components. The SLAM is a through transmission technique operating at frequencies between 10 and 500 MHz [20-22]. SLAM uses a scanning laser detector of the ultrasound images of the internal features of a material. The ultrasonic wave travels through the entire volume of the material and the scanning laser detects the variations in the transmitted ultrasound. On the other hand, SAM is primarily a reflection-based microscope that generates very high-resolution images of a sample surface or a near surface plane. Finally, the C-SAM method uses a pulse-echo microscope that employs a focused transducer to generate and receive the ultrasound beneath the surface of the sample. In the schematic below, the different acoustic microscopy imaging methods are shown.



(a) SLAM (b) SAM (c) C-SAM

Figure 3.19. A comparison of the available three acoustic microscopy techniques [21].

Based on the availability and applicability of the methods to our multilayered structure, we have selected the C-SAM technique to image the interface of the heat spreader attachment material. C-SAM is a pulse-echo microscope that employs a focused transducer to generate and receive the ultrasound beneath the surface of the sample. The transducer is scanned across the sample in several passes for image generation. Scan time varies from seconds to minutes depending on the desired resolution and the area of scan. At the tip of the transducer, a concave lens is attached. The reflective inspection acts on a pulse-echo mode; a reflection from the top of a package returns earlier than a reflection within the package. This time separation is employed to separate layers within a structure.

C-SAM has the ability to perform non-destructive package analysis while imaging the internal features of the package. Ultrasonic waves are very sensitive to the density variations (such as voids or delaminations similar to airgaps) of the surface. C-mode scanning acoustic microscopy uses high-frequency ultrasound to detect internal discontinuities in materials and components. The C-SAM emits acoustic waves in a reflection mode at a specific frequency, typically ranging from 15 to 180 MHz. The distance between the echoes relates to their depth in the device under test. A transducer that alternatively acts as a receiver and sender achieves the reflection. The transducer electronically switches between the transmit and the receive modes. An electronic gate is used to select a specific depth or interface. This microscope generates images by mechanically sweeping a sample while emitting ultrasonic waves from the transducer. The ultrasonic wave uses an inert fluid, such as de-ionized water, as a coupling medium.

Several different imaging modes of the C-SAM are discussed in the following paragraphs [21, 23-24].

A-Scan: The fundamental information using reflection mode acoustic systems is contained in the A-Scan, which displays the depth information in the sample. Echoes from different interfaces are displayed. The distance between the echoes is related to the depth of the interfaces in the device, and it is expressed as,

$$D = vt/2, \text{ where } D = \text{distance}, v = \text{velocity of sound}, t = \text{time}.$$

A-Scan is a graph of sound intensity against time. The horizontal scale defines the depth within a sample while the vertical scale defines amplitude of the reflected sound wave. In Figure 3.20, major peaks of the waveform are labeled to their corresponding interfaces within a package [25]. Once the section to be inspected is identified, the red gate is placed around the layer. Next,

the transducer distance is varied to focus the transducer at high sound amplitude. In a conventional imaging technique, a wide gate is placed on the waveform, and consequently, a single image of all layers is projected on to one plane. Also, the system may not be able to detect a defect if an adjacent layer has high intensity than the defect itself.

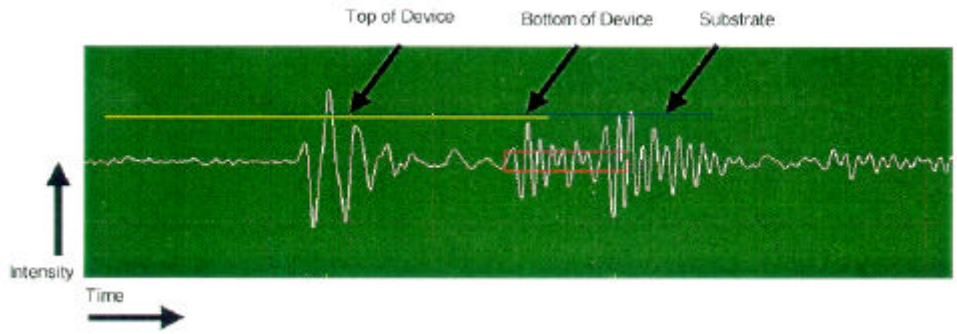


Figure 3.20. A typical A-Scan image (with the selected gates) of a device on a substrate [25]

Time of flight scan: In a time-of-flight (TOF) scan, the arrival time of the echo is converted to a gray scale for imaging. This mode provides a general overview of the feature depths and thickness information, which can be projected to a three-dimensional analysis to achieve a perspective of the contour of the interfaces. This specific mode is mostly used in profiling cracks in an IC plastic package, where an isomeric plot of the time-of-flight is acquired simultaneously with the amplitude image to get an enhanced image of the cracks.

B-scan: In this mode, the image displays one dimension of the scan plane on the x-axis and the depth position on the y-axis. The transducer is indexed in the depth direction of the sample to ensure uniform focus throughout the thickness. The time-of-flight data is converted to a depth data so that a cross-sectional image can be obtained. A cross-sectional view, such as a B-scan image can detect the location of a void at a certain thickness of the sample. However, a B-scan image may provide a distorted dimensional information of the device since the object may appear thicker than the actual size. This is due to the fact that B-scan is out of aspect and the horizontal scale is not equal to the vertical scale causing image distortion. Typically, B-scan involves the most complicated and time-consuming analysis of all the available modes.

Interface Scan: The interface scan is most commonly used for imaging delaminations and voids. This method involves gating the reflection specific to the interface under test. At the same time, the transducer is focused onto that specific interface. The acoustic image using an interface scan provides both amplitude and phase of the gated reflection.

Bulk Scan: This technique is employed to portray the acoustic appearance of the bulk specimen, as opposed to a specific interface. The gating of the acoustic signal within the material begins immediately after an interface echo, and includes all of the area up to the next interface reflection. In the case of a homogeneous material, there will be no significant signal on the image. However, if the material contains voids or other irregularities, they will cause signal reflections to be displayed on the image. The limitation of a bulk scan is that no depth information is supplied in the image. Any defects, between the front surface and the back surface, appear in the image. Obtaining depth information requires additional user interaction and time to view each A-scan or the generation of B-scan, which requires re-scanning the material.

C-SAM images of voids, cracks, disbonds and delaminations are of high contrast, which enables one to distinguish the irregularities from one another. The most important feature of this tool is that it is non-destructive, which gives the researcher more opportunities for further electrical or thermal testing. The commonly available scanning acoustic microscopes (such as Sonix systems) are capable of providing extraordinary resolution. Acoustic image resolution varies with the sample material as well as the frequency of the sound. The tradeoff between a low- and a high-frequency transducer is in the depth of penetration and resolution. The high-frequency transducer provides excellent resolution, while being limited in depth penetration. On the other hand, a low frequency transducer allows more transmission through materials. In the following table, typical resolution and penetration depths for available transducer frequencies are listed.

Table 3.2. Resolution and Penetration at Common Operating Frequencies

Frequency	**Wavelength**	**Resolution**		**Typical Depth**
(MHz)	in water (mils)	surface (mils)	interior (mils)	penetration (mils)
30	2	1.4	2.8-7.0	0-280
50	1.2	0.8	1.6-4.0	0-200
100	0.6	0.4	0.8-2.0	0-80
500	0.12	0.08	0.1-0.4	0-1.6
1000	0.06	0.04	0.08-0.2	0-0.8

Consequently, C-SAM as a low-frequency transducer would allow us to image a deep interface, such as flip chip solder joints. We can see from the table that a 100 MHz transducer will allow us to penetrate samples up to 80 mil thick and to detect voids as small as 1 mil in diameter.

3.2.3.2.2 Tomographic Acoustic Micrography Imaging (TAMI™) on Flip Chip Solder Joints

In recent years, Sonix has developed a new feature within C-SAM, called TAMI™ (Tomographic Acoustic Micro Imaging) scan, which can supply defect x, y, and z coordinate information without re-scanning for every single layer [23, 26-27]. This feature, as shown in Figure 3.21, has two advantages: it allows automatic focus adjustments to ensure all depths are in focus and it allows multiple gating to provide images or slices at many different levels (up to 33 slices) within the interlayer. The real advantage is that all 33 images are generated at the same time it takes to do a bulk scan. Therefore, TAMI™ can be easily integrated in the package fabrication process as a standard method of inspecting interface layers. We define the spacing between the TAMI™ images and it is measured in microseconds. This measurement is converted into a millimeter measurement by using the simple formula Distance = Velocity x Time. Therefore, by paging down through the TAMI™ images, we can look deeper within the interface by a given amount.

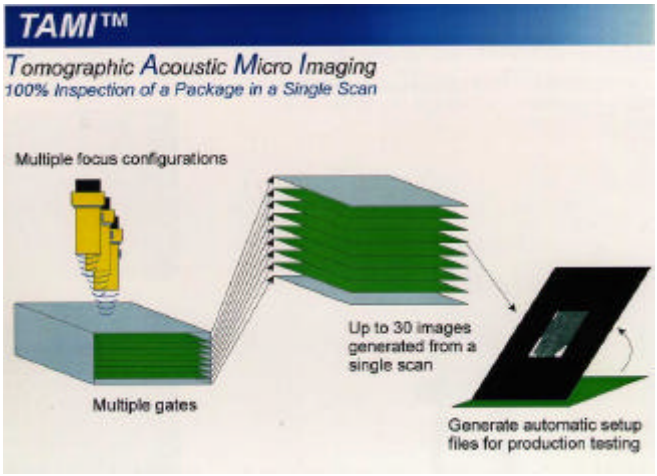


Figure 3.21. Schematic of the C-SAM TAMI™ technique [26]

Conventional acoustic imaging could be time consuming and requires a significant amount of expertise to analyze the complex waveforms to determine the layer at which a defect is detected. Ultrasonic parameters such as gate position and focusing need to be adjusted for accurate scanning. For example, in a multilayer structure (such as our test sample), in order to

isolate a thin interface, such as a solder layer, a very narrow gate is required, which makes the gate setup extremely crucial and challenging. The problem arises from determining the positive and negative cycles of the A-Scan waveform of the interface under inspection. In most cases, the identification process demands a trial and error method for precise positioning of the gate. As a result, to get an optimal setup, the transducer needs to be focused and the sample needs to be scanned repeatedly.

TAMI^{TM} eliminates all the above mentioned difficulties with the setup and the interpretation of a conventional imaging system. Focusing at an interface is attained by examining C-Scan features rather than maximizing an A-Scan. In a TAMI^{TM} scan, the user sets the start position for the scanning, and the additional gates are automatically set according to the user-defined gate width and spacing. Typically, these gates are set next to each other or in a slightly overlapping manner as shown in Figure 3.22. Consequently, the gate width and the frequency of the transducer determine the thickness of each layer.

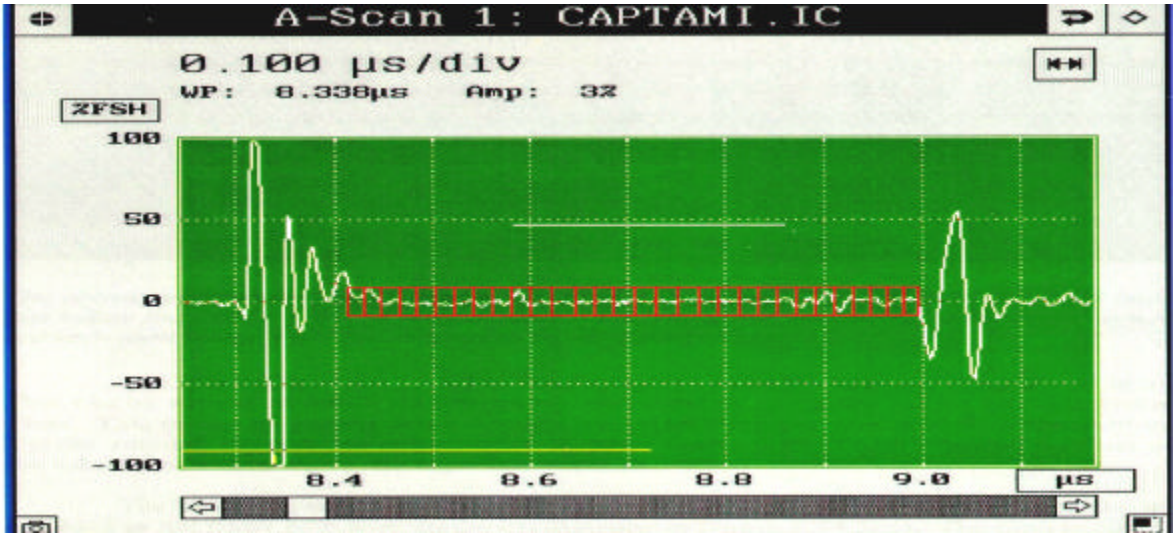


Figure 3.22. Gating scheme with TAMI feature [27]

In the following paragraphs, we describe how we use TAMI^{TM} to study our flip chip solder joints. First, it is necessary to select the right transducer for the sample material and set up the scan parameters, such as scan frequency, speed and resolution. We used 75 MHz transducer for flip chip assembly. After this setup, we can get A-scan signal when the transducer is focused to the right position. Figure 3.23 shows a typical A-scan image of a flip chip on board assembly with selected gates. The gate width is selected wide enough to cover the top silicon surface and down inside solder joints, which is normally preferred for the first scan because we can then

zoom in the position where we are interested in based on this wide scan. The spacing of gates also need to the wide, or else there would be more gates than the system allows. For this example, the gate spacing is selected in such a way that maximum gate number (33) is achieved for our system. Until now, we can change into scan interface and begin C-scan with the TAMI feature. Figure 3.24 shows the computer interface for TAMI scan of Sonix system. During the scan, we can page down to different gates and look at the layers corresponding to the gates. Figure 3.25 shows several representative gates and their corresponding images. We can see from Figure 3.25 (a) that the first several strong peaks in TAMI^{TM} signal are acoustic energy reflected by the top silicon surface layers. After the strong peaks, the signal is very week for a certain thickness, which is corresponding to the layers inside silicon, as shown in Figure 3.25 (b). Around gates 8, 9 and 10, there are high peaks again which is corresponding to the chip pad and solder joint interface, as we can see from Figure 3.25 (c). Then acoustic signal attenuates gradually which is down inside solder joint. Figure 3.25 (d) shows TAMI signal and image inside solder joint. The chip pad and solder joint interface is what we are interested in, thus we can specifically focus on that interface and zoom in those layers by reducing the gate width and space.

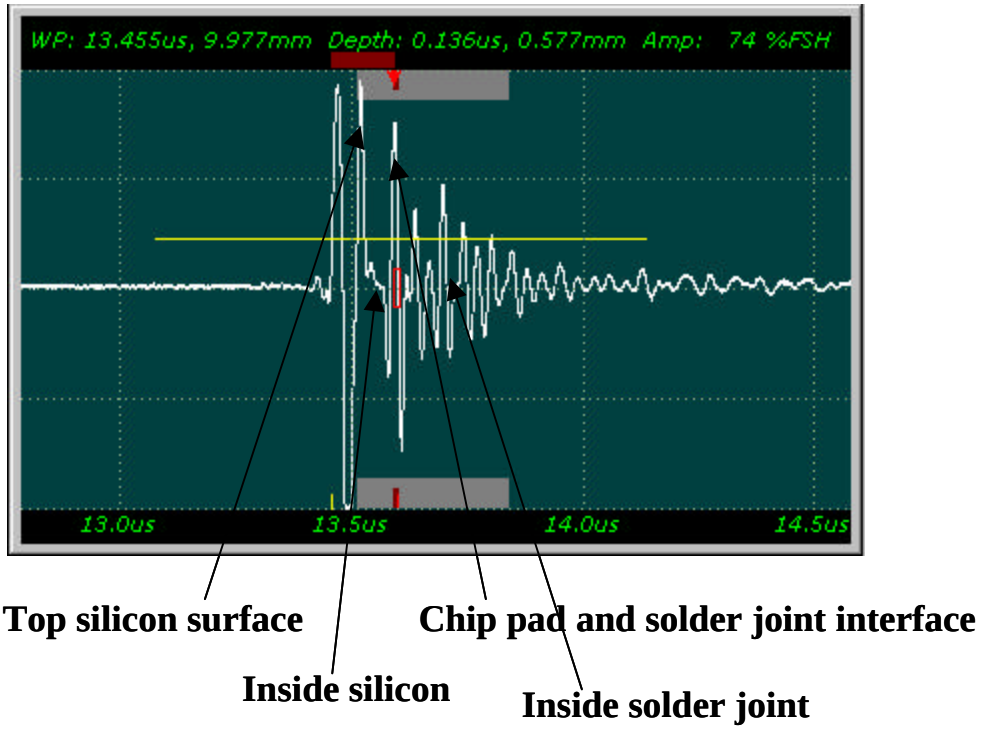


Figure 3.23. A typical A-Scan image (with the selected gates) of a flip chip on board assembly.

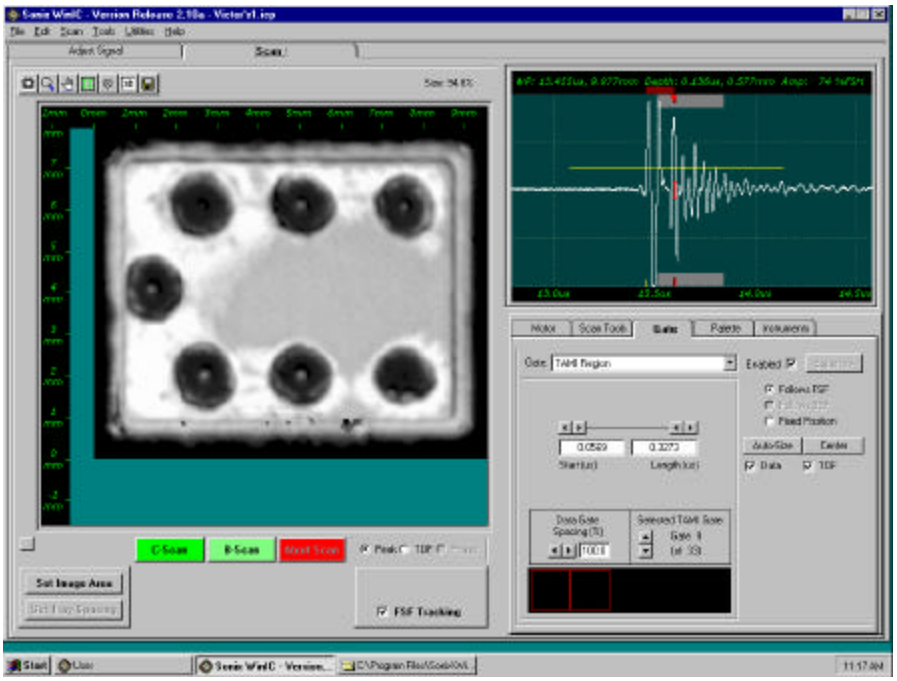
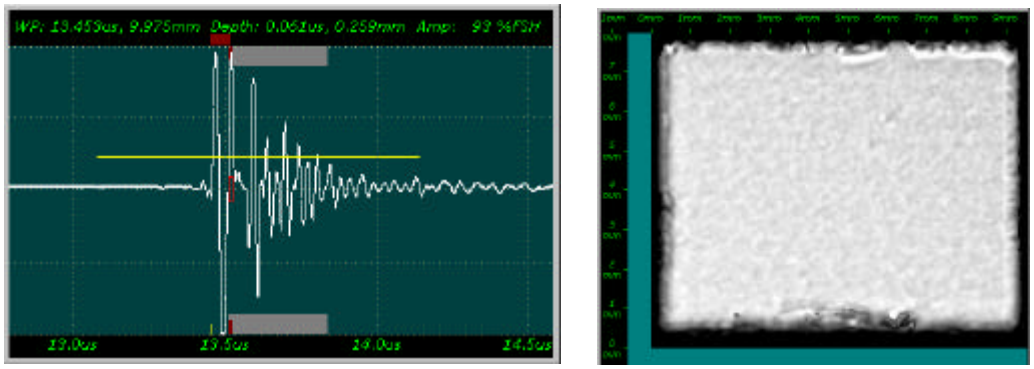
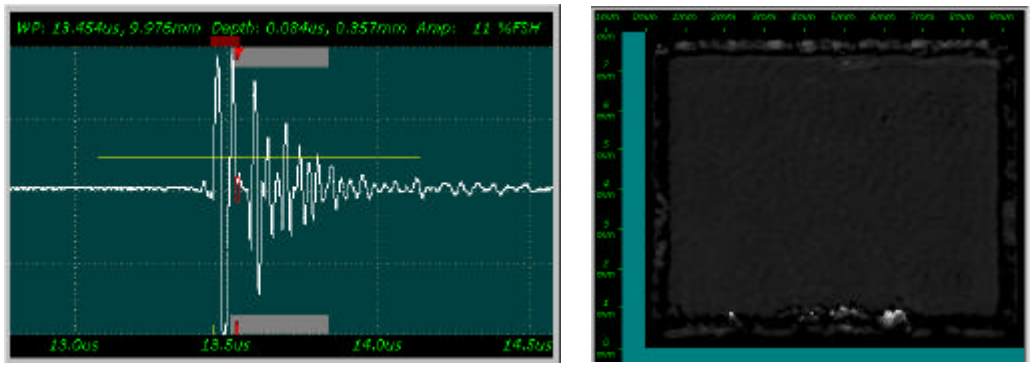


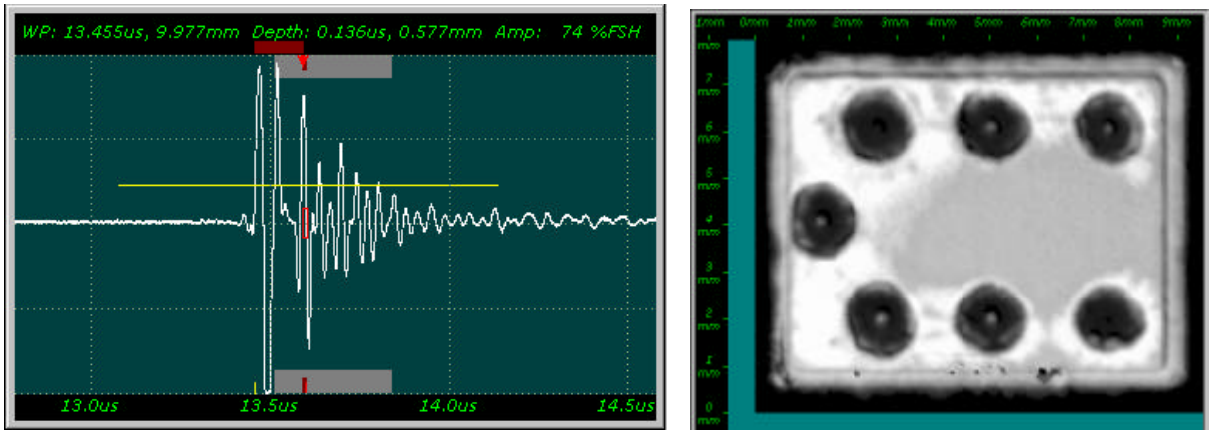
Figure 3.24. Computer interface of TAMI™ scan.



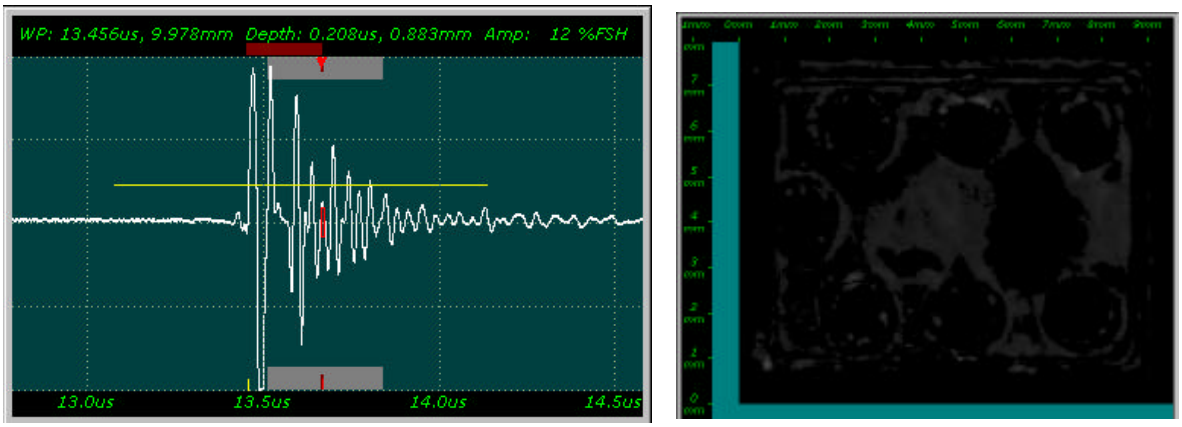
(a)



(b)



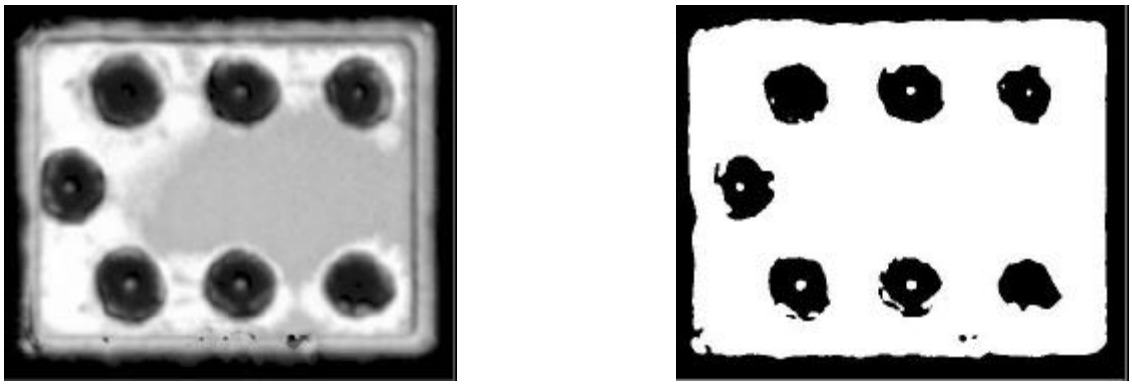
(c)



(d)

Figure 3.25. TAMI™ signal and images at selected gates corresponding to different layers in the scanned structure; (a) gate 1 corresponding to top silicon surface; (b) gate 3 corresponding to a layer inside silicon; (c) gate 9 corresponding to the interface between chip pad and solder joint; and (d) gate 16 corresponding to a layer inside solder joint.

Once the TAMI™ images are obtained, we can learn the crack initiation location, crack propagation rate and figure out failure modes of solder joint interconnection as cracks, defects are evident in the images. Crack areas or contact areas can be set to different colors and calculated. The National Instruments IMAQ Vision Builder software is used to measure the percent threshold values of different colored regions within the user-defined area of an image. Figure 3.26 shows an acoustic image of a flip chip assembly and processed picture of that image by IMAQ Vision Builder software. The soft ware can calculate crack or contact area of the processed picture.



(a) (b)

Figure 3.26. (a) TAMI™ image of a flip chip assembly; (b) processed picture of the TAMI™ image by IMAQ Vision Builder software which is used to calculate crack or contact area.

3.3 Experimental Results

In this section, we present the experimental results on tensile and shear tests, and temperature cycling tests of solder joint assemblies. For the tensile and shear tests, results on as-processed samples and samples after 800 and 1200 temperature cycles are presented. There are two sets of temperature cycling samples. For each set, there are different solder joint configurations. The results of each set of samples and solder joint configurations are reported.

3.3.1 Results on Tensile and Shear Tests

As we described before, tensile test were conducted on bumped chips and both tensile and shear tests were conducted on flip chip bonded assemblies. For each test configuration, four samples were tested. After tensile and shear testing, samples were observed and investigated using optical microscopy.

3.3.1.1 Tensile Test on Solder Bumps on Chip

Figure 3.12 showed the tensile test structure of solder bumps on chip. Tensile tests showed that the failure mode for all the solder bumped samples was interfacial fracture. However, the adhesion strength for different sample configurations was quite different, as shown in Figure 3.27. The stress values in Figure 3.27 are the average stresses, and the error bars are the standard deviation for four samples. Figure 3.28 and Figure 3.29 are typical stress vs. displacement curves for solder bumps on IGBT pads. The IGBT pad size is same for both

stacked solder bumps and conventional single solder bumps, which is 1.1×1.1 mm. We can see that the adhesion strength for solder bumps on in-house made UBM device pad are much lower than that on vendor supplied solderable device pad. Interestingly, the adhesion strength for conventional single solder bumps and stacked solder bumps is almost the same for in-house made solderable device. However, the adhesion strength for conventional single solder bumps and stacked solder bumps is quite different for vendor supplied solderable devices. This could be understood after we investigated the fracture interface. From optical microscope observations, we found that the fracture occurred at the UBM/Al pad interface for in-house made solder devices, while for vendor supplied solderable devices, the fracture happened at the interface between UBM and solder bump (or probably between the UBM layers). This indicated that the quality of the in-house made UBM was not as good as that of the vendor supplied. From the curves in Figure 3.29, we can see that the adhesion strength for stacked solder bump is about 60 MPa, while that of single solder bump is about 40 MPa for vendor supplied solderable devices. We believe the reason for this difference is that the stacked solder bump has lower stress concentration at the corners of the UBM/solder interface than single solder bump. There are stress singularities at the contact corners of the solder bumps. The stacked solder bump has smaller contact angle and thus less severe singularity, as illustrated in Figure 3.30. On the other hand, the adhesion strength difference verified that the stacked solder bump structure reduced the stress concentration at the corners of the solder bump.

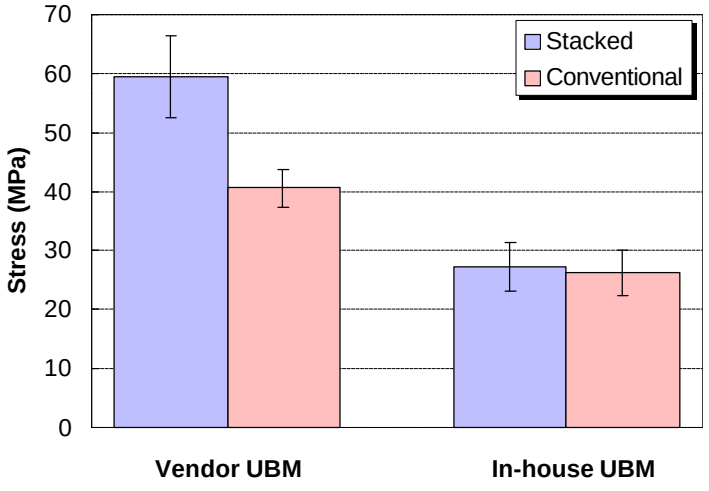


Figure 3.27. Adhesion strength for different solder joint configuration.

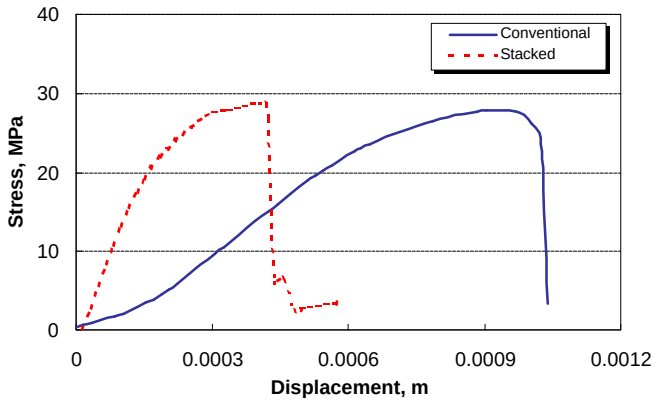


Figure 3.28. Typical stress-displacement curve under tensile test for conventional single solder bump and stacked solder bump on in-house sputtered Cr/Cu UBM device pad.

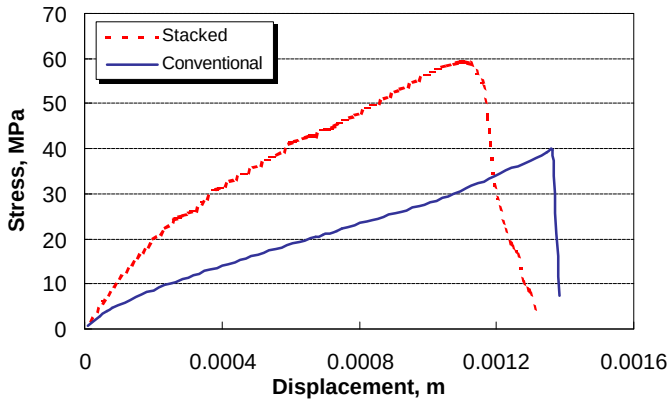


Figure 3.29. Typical stress-displacement curve under tensile test for conventional single solder bump and stacked solder bump on vendor supplied solderable device pad (Ti/Ni/Ag UBM).

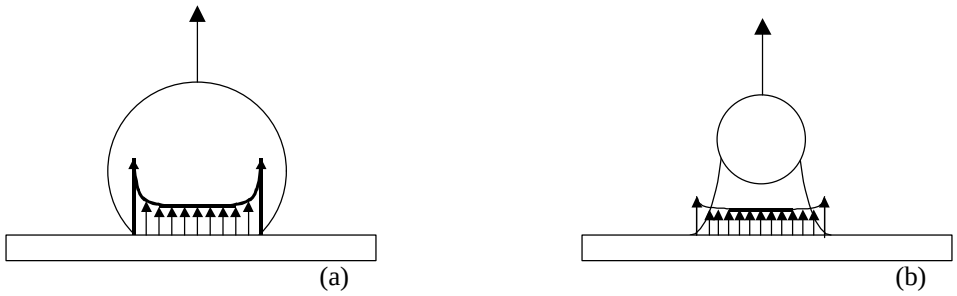


Figure 3.30. Pictorial representation of stress concentration for (a) conventional single solder bump; (b) stacked solder bump.

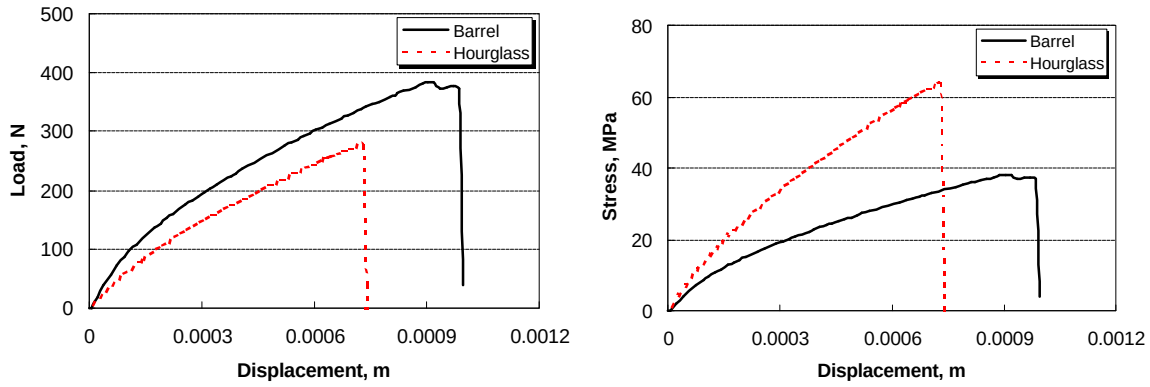
As indicated earlier, we soldered wires on top of the solder bump in order to do the tensile test, thus our test results also include wire's behaviors. However, we believe our

experiments at least show the maximal adhesion strength (or accurate enough to show the maximal adhesion strength) for different samples.

Since the quality of the in-house made UBM was not as good as that of the vendor supplied UBM, we only used those chips that have vender supplied UBM for the following tensile, shear tests and reliability evaluation.

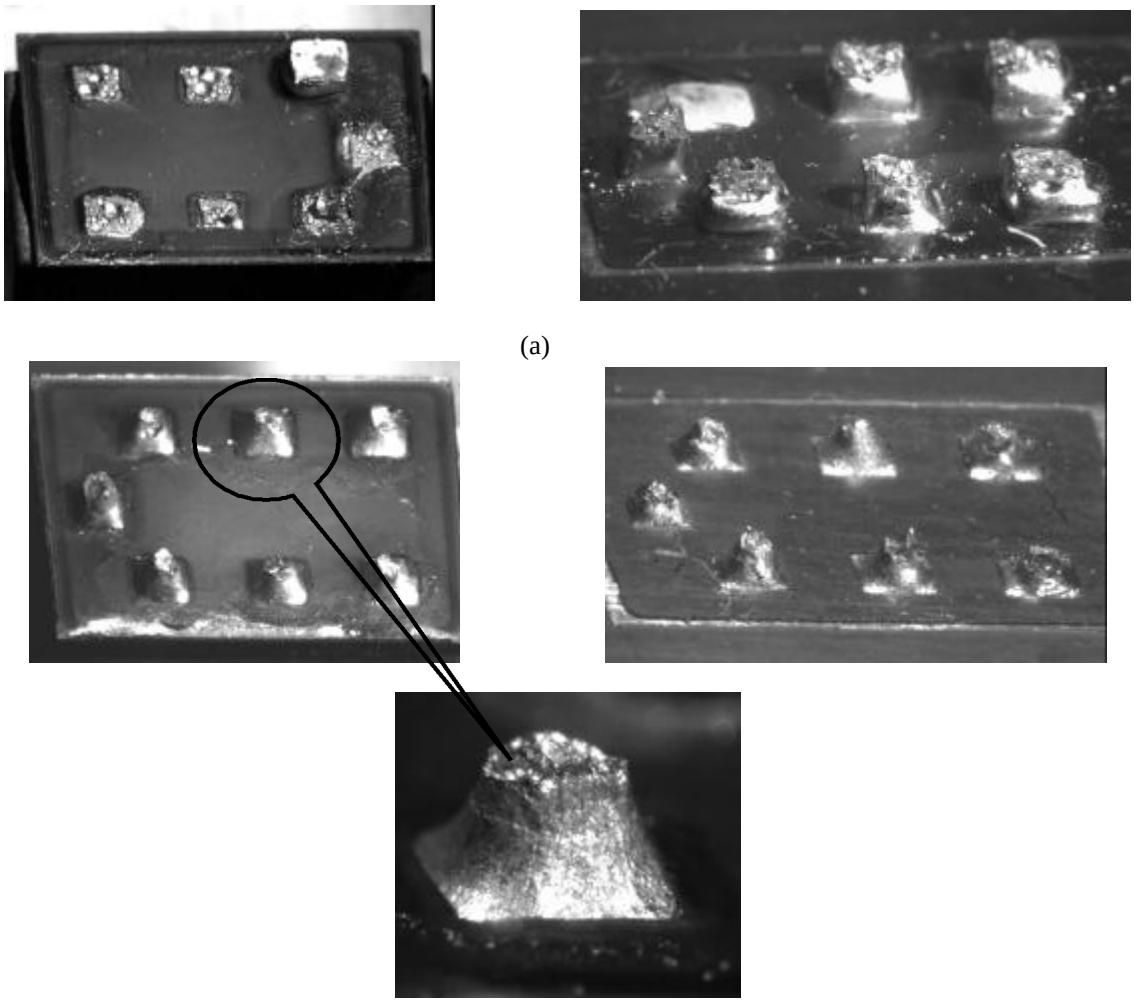
3.3.1.2 Tensile Test on Flip-Chip Attached Solder Joints

For flip chip attached solder joints, tensile tests were conducted on both stacked hourglass-shaped solder joints and single barrel-shaped solder joints at 0, 800, and 1200 temperature cycles. The test sample configurations were shown in Figure 3.14 and described in section 3.2.2. Figure 3.31 (a) and (b) show typical load-displacement and engineering stress-displacement curves under tensile test for as-processed single barrel-shaped solder joints and stacked hourglass-shaped solder joints. We can see from Figure 3.31 (a) that the failure load of single barrel-shaped solder joints is greater than that of stacked hourglass-shaped solder joints. However, the failure stress of single barrel-shaped solder joints is lower than that of stacked hourglass-shaped solder joints, as a typical stress-displace curve shown in Figure 3.31 (b). This is in agreement with the tensile tests on solder bumps on chip results we discussed in section 3.3.1.1. The reason why the failure stress of single barrel-shaped solder joints is lower than that of stacked hourglass-shaped solder joints while failure load is higher is that the failure locations for as-processed single barrel-shaped solder joints and stacked hourglass-shaped solder joints are quite different. For single barrel-shaped solder joints, the failure location is either solder joint and chip pad interface (about 80%) or solder joint and substrate pad interface (about 20%). On the other hand, stacked hourglass-shaped solder joints unanimously fail at the mid neck points of the joints. That is, the middle high-lead solder ball fractured. Figure 3.32 shows the typical failed samples of as-processed single bump barrel-shaped solder joints and stacked hourglass-shaped solder joints under tensile test. Figure 3.33 is a comparison of the average adhesion strength of as-processed single barrel-shaped solder joints and stacked hourglass-shaped solder joints. The load and stress values in Figure 3.33 are the average values, and the error bars are the standard deviation for four samples. We can see that stacked hourglass-shaped solder joints have greater adhesion strength than single barrel-shaped solder joints.



(a) (b)

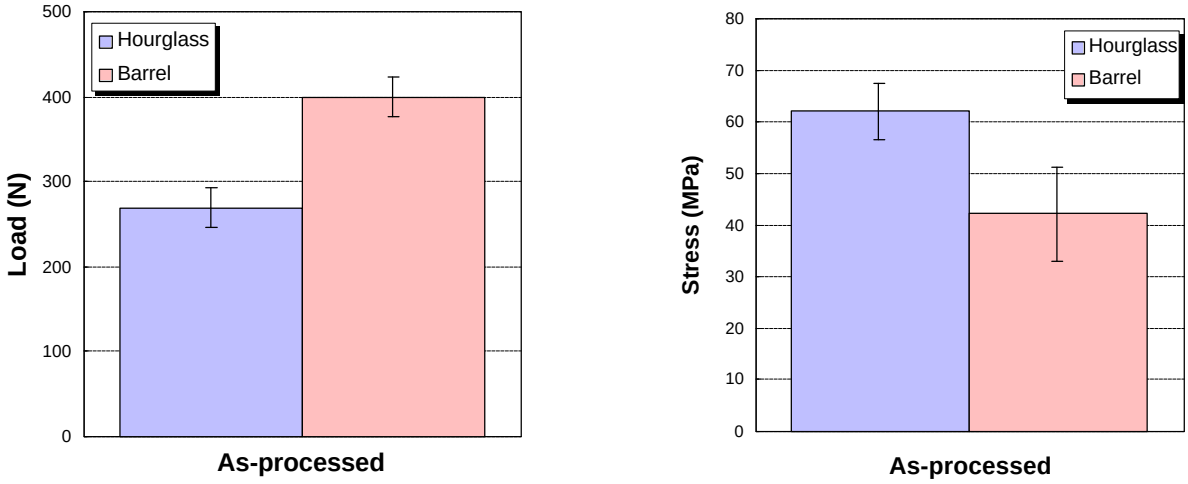
Figure 3.31. Typical (a) load-displacement curve; (b) engineering stress-displacement of as-processed single barrel-shaped solder joints and stacked hourglass-shaped solder joints under tensile test.



(a)

(b)

Figure 3.32. Typical failed samples of (a) single bump barrel-shaped solder joints and (b) stacked hourglass-shaped solder joints before temperature cycling under tensile test.



(a) (b)

Figure 3.33. Average adhesion strength of as-processed single barrel-shaped solder joints and stacked hourglass-shaped solder joints; (a) in load; (b) in stress.

Figure 3.34 and Figure 3.35 show the typical load-displacement curves of single barrel-shaped solder joints and stacked hourglass-shaped solder joints after 800 and 1200 temperature cycles respectively, under tensile test. After 800 temperature cycles, the failure load of single barrel-shaped solder joints is still greater than that of stacked hourglass-shaped solder joints. However, after 1200 cycles, the failure load of single barrel-shaped solder joints is lower than that of stacked hourglass-shaped solder joints. For both cases, we believe the failure stress of single barrel-shaped solder joints is lower than that of stacked hourglass-shaped solder joints. After 800 and 1200 temperature cycles, the failure location of single barrel-shaped solder joints is still either at the solder joint to chip pad interface or at the solder joint to substrate pad interface, while the failure location of stacked hourglass-shaped solder joints under tensile test is no longer unanimously at the mid neck point of the joints, nor unanimously at the solder joint to chip and substrate pad interfaces. The majority of the failure location of stacked hourglass-shaped solder joints shifted from the mid neck point of the joint to the locations closer to solder joint and pad interfaces and a small fraction completely shifted to solder joint to pad interfaces, especially after 1200 cycles. Figure 3.36 shows the typical failed samples for single bump barrel-shaped solder joints and stacked hourglass-shaped solder joints after 1200 temperature cycles under tensile test. Since the fracture locations of stacked hourglass-shaped solder joints vary and the fracture areas are not uniform, it is very difficult to calculate failure stresses after

temperature cycling. We can also see from Figure 3.36 (b) that some of the solder mask fractured after 1200 thermal cycles.

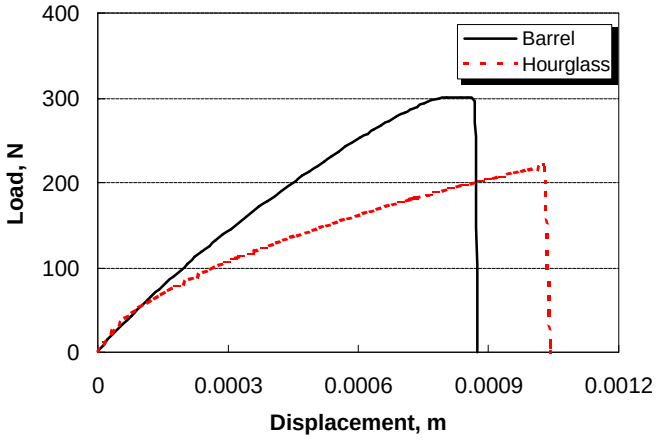


Figure 3.34. Typical load-displacement curves of single bump barrel-shaped solder joints and stacked hourglass-shaped solder joints under tensile test after 800 temperature cycles.

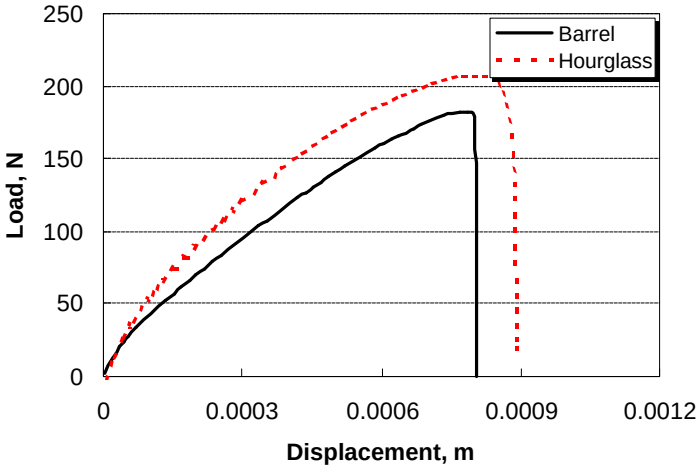
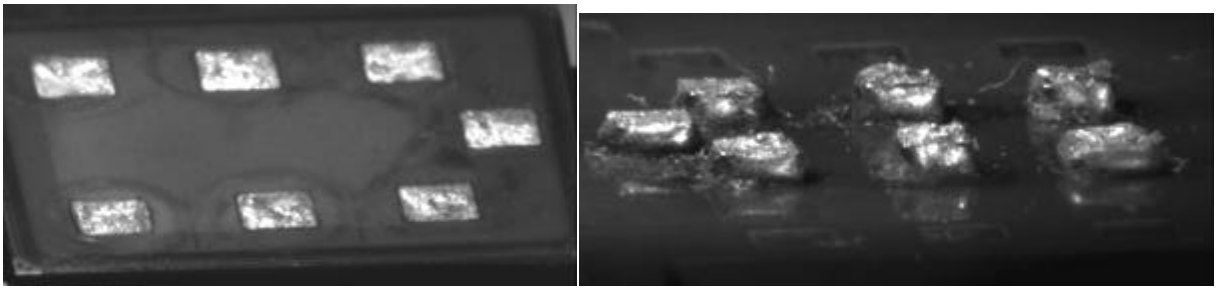
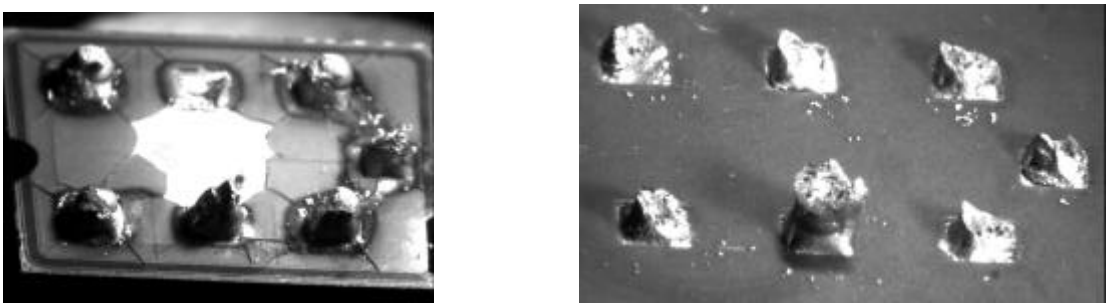


Figure 3.35. Typical load-displacement curve under tensile test for single bump barrel-shaped solder joints and stacked hourglass-shaped solder joints after 1200 temperature cycles.



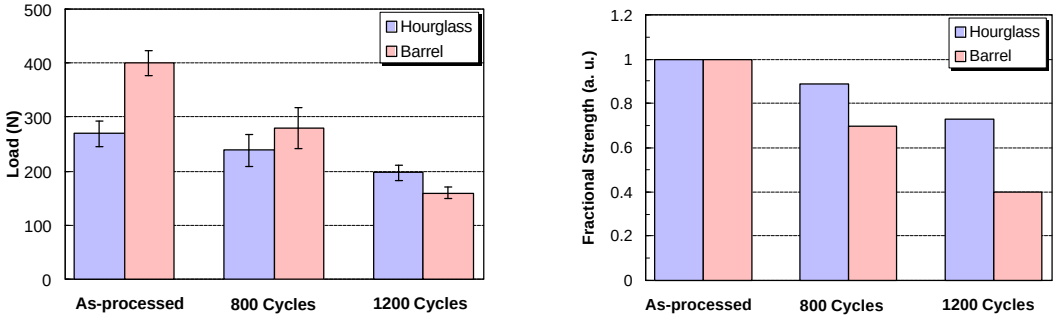
(a)



(b)

Figure 3.36. Typical failed samples of (a) single bump barrel-shaped solder joints and (b) stacked hourglass-shaped solder joints after 1200 temperature cycles under tensile test.

Figure 3.37 summarizes the tensile test results of stacked hourglass-shaped and single barrel-shaped solder joints for as-processed samples and samples after 800, 1200 temperature cycles. Again the load values in Figure 3.37 are the average values, and the error bars are the standard deviation for four samples. The adhesion strengths of both single barrel-shaped and stacked hourglass-shaped solder joints reduce with the increasing number of temperature cycling. The decrease of adhesion strength is regarded as a result of degradation of solder joints during temperature cycling. As we can see from Figure 3.37 (b) that the adhesion strength of single barrel-shaped solder joints reduces faster than that of stacked hourglass-shaped solder joints. This indicates that single barrel-shaped solder joint is less reliable than stacked hourglass-shaped solder joint.



(a) (b)

Figure 3.37. Tensile test results (a) failure load; (b) fractional strength of stacked hourglass-shaped and single barrel-shaped solder joints for as-processed samples and samples after 800, 1200 temperature cycles.

3.3.1.3 Shear Test on Flip-Chiped Solder Joints

For flip chip attached solder joints, shear tests were also conducted on both stacked hourglass-shaped solder joints and single barrel-shaped solder joints at 0, 800, and 1200

temperature cycles. The test sample configurations were shown in Figure 3.15 and described in section 3.2.2. Since the test structure is double lap joints, we divided the load by 2 for all the shear test results, thus making the results referring to one joint only. Figure 3.38, Figure 3.40 and Figure 3.41 are the typical load-displacement curves of single barrel-shaped solder joints and stacked hourglass-shaped solder joints for as-processed samples and samples after 800 and 1200 temperature cycles respectively, under shear test. For as-processed samples, the failure load of single barrel-shaped solder joints is greater than that of stacked hourglass-shaped solder joints. Figure 3.39 shows the typical failed samples of single bump barrel-shaped and stacked hourglass-shaped solder joints before temperature cycling under shear test. The failure location of single barrel-shaped solder joints is either solder joint and chip pad interface (about 90%) or solder joint and substrate pad interface (about 10%). For stacked hourglass-shaped solder joints, the majority of the failure locations are close or at the mid neck points of the joints and few failed at the solder joint and pad interfaces. After 800 temperature cycles, the failure load of single barrel-shaped solder joints is still greater than that of stacked hourglass-shaped solder joints, while after 1200 cycles, the failure load of stacked hourglass-shaped solder joints is almost same as that of single barrel-shaped solder joints. After 800 and 1200 temperature cycles, the failure locations of both single barrel-shaped solder joints and stacked hourglass-shaped solder joints are the same as the situation for as-processed samples. Figure 3.36 shows the typical failed samples for single bump barrel-shaped solder joints and stacked hourglass-shaped solder joints after 1200 temperature cycles. We can also see from load vs. displacement curves that stacked hourglass-shaped solder joints have higher displacement than single bump barrel-shaped solder joints. This indicates that stacked hourglass-shaped solder joint is more compliant.

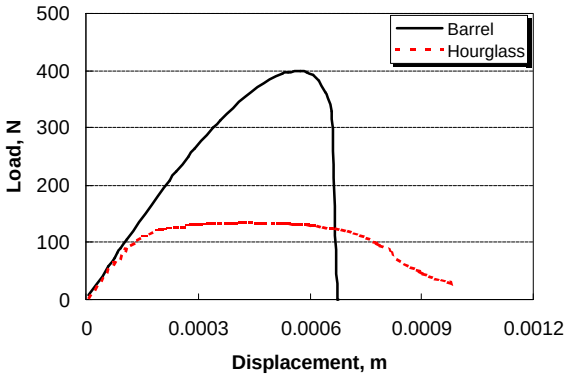
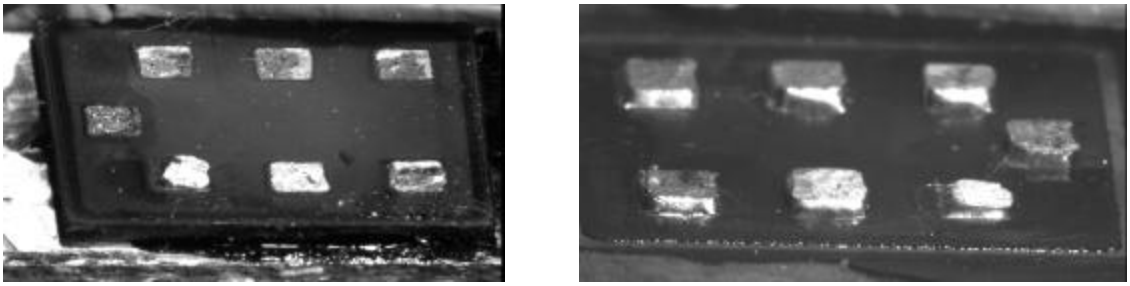
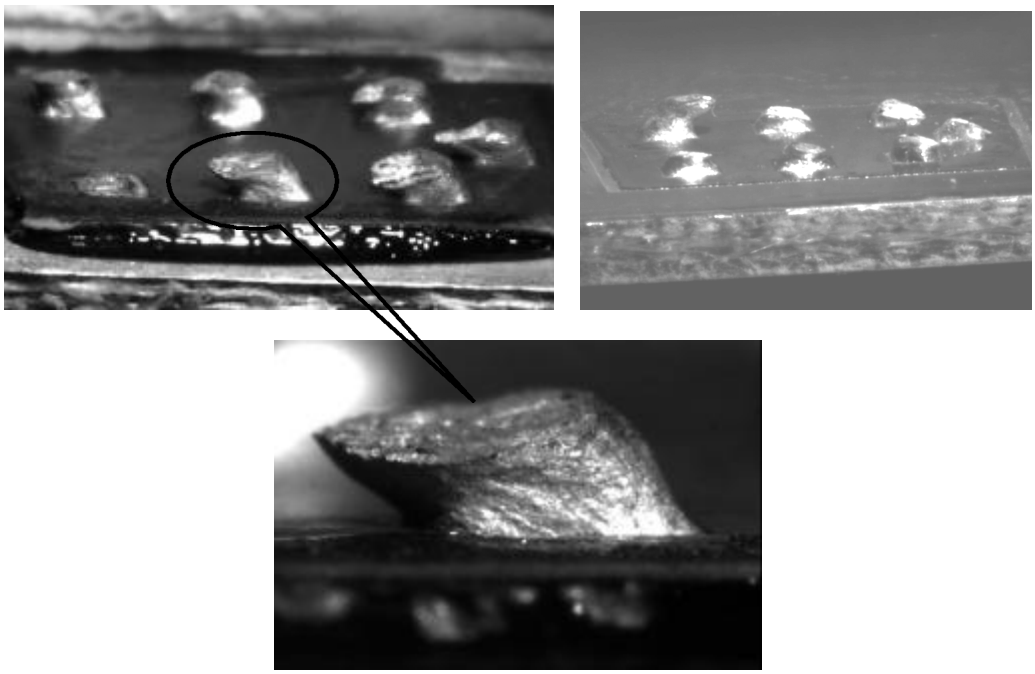


Figure 3.38. Typical load-displacement curve under shear test for as-processed single barrel-shaped solder joints and stacked hourglass-shaped solder joints.



(a)



(b)

Figure 3.39. Typical failed samples of (a) single bump barrel-shaped solder joints and (b) stacked hourglass-shaped solder joints before temperature cycling under shear test.

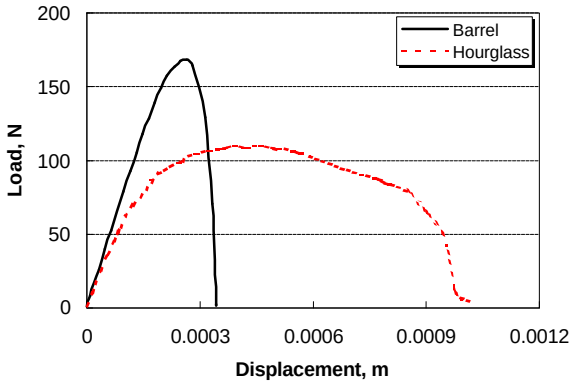


Figure 3.40. Typical load-displacement curve under shear test for single bump barrel-shaped solder joints and stacked hourglass-shaped solder joints after 800 temperature cycles.

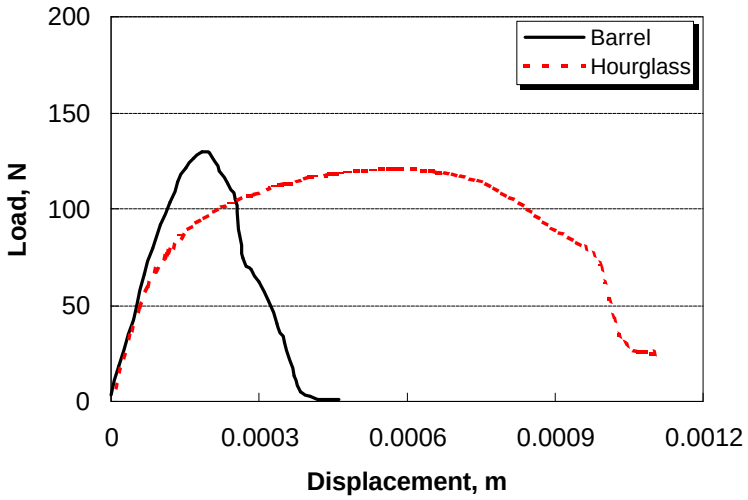
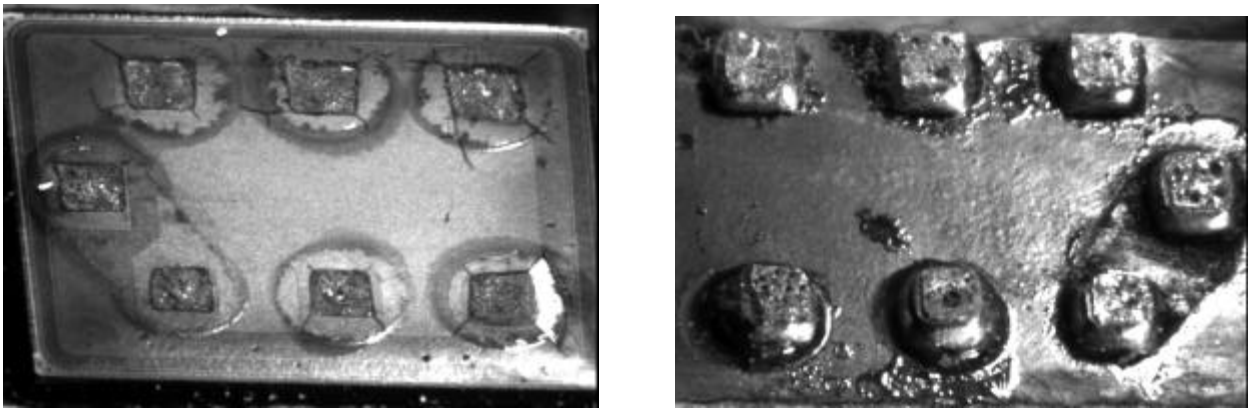
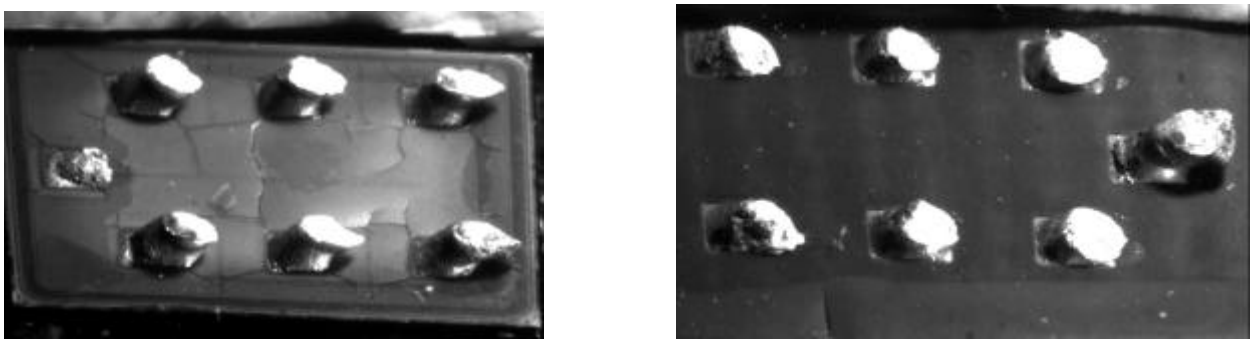


Figure 3.41. Typical load-displacement curve under shear test for single bump barrel-shaped solder joints and stacked hourglass-shaped solder joints after 1200 temperature cycles.



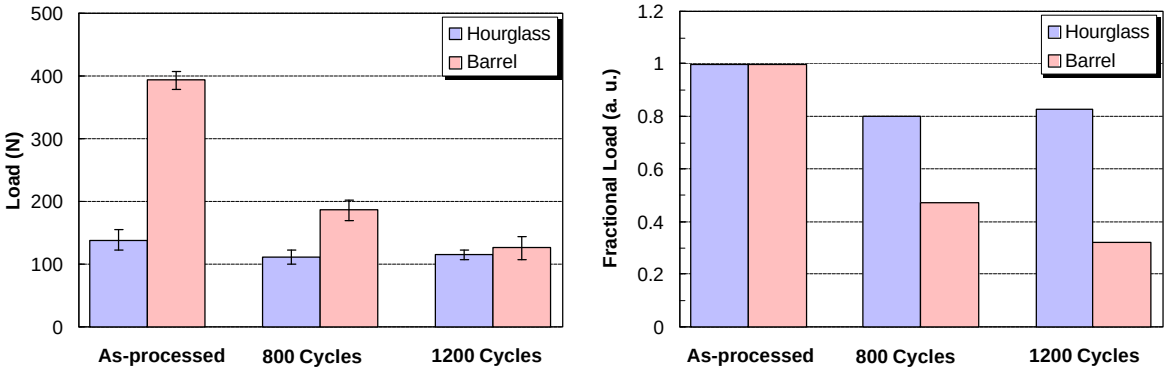
(a)



(b)

Figure 3.42. Typical failed samples of (a) single bump barrel-shaped solder joints and (b) stacked hourglass-shaped solder joints after 1200 temperature cycles under shear test.

Figure 3.43 summarizes the shear test results of stacked hourglass-shaped and single barrel-shaped solder joints for as-processed samples and samples after 800, 1200 temperature cycles. The load values in Figure 3.43 are the average values, and the error bars are the standard deviation for four samples. The failure load of single barrel-shaped reduces with the increasing number of temperature cycling while that of stacked hourglass-shaped solder joints decreases slightly if there any reduction. As we can see from Figure 3.43 (b) that the failure load of single barrel-shaped solder joints reduces much faster than that of stacked hourglass-shaped solder joints.



(a) (b)

Figure 3.43. Shear test results (a) failure load; (b) fractional load of stacked hourglass-shaped and single barrel-shaped solder joints for as-processed samples and samples after 800, 1200 temperature cycles.

3.3.2 Results on Temperature Cycling Test

In this section, temperature cycling results on both the first set and the second set of samples will be presented. As we introduced before, electrical resistance increase is used as a criterion to evaluate solder joint fatigue life. Scanning acoustic images of the samples taken during the temperature cycling is used to verify the fatigue degradation of the solder joints. After temperature cycling, the fatigue failure of the solder joints are analyzed by metallographic cross sectioning. The fatigue life of single bump barrel-shaped solder joint without underfill, single bump barrel-shaped solder joint with underfill, triple stacked barrel-shaped solder joint without underfill, triple stacked hourglass/column-shaped solder joint without and with underfill is compared and their failure modes are discussed.

3.3.2.1 Results on the First Set of Samples

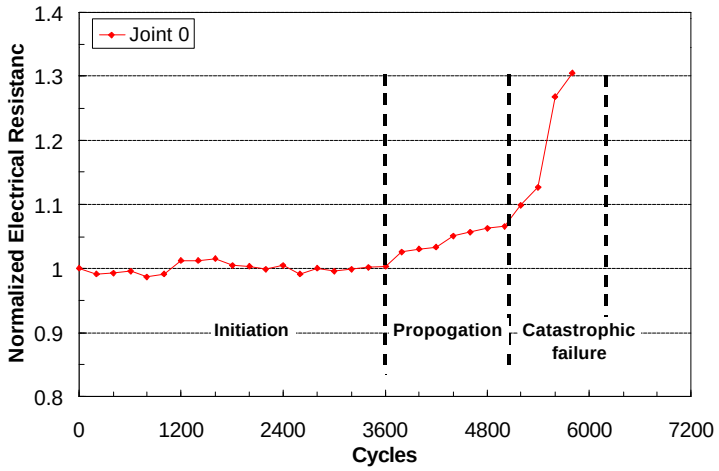
The first set of samples has four solder joint configurations: single bump barrel-shaped solder joint without underfill, single barrel-shaped solder joint with underfill, triple stacked hourglass/column-shaped solder joint without underfill and triple stacked hourglass/column-shaped solder joint with underfill. The underfilled solder joint systems are very complicated due to the effects of underfilling. The main objective of this study is to improve solder joint interconnection reliability through solder joint geometry optimization and understand the solder joint geometry effect on failure modes. Therefore, we will mainly discuss the two solder joint configurations that are not underfilled, with brief report of the results of the underfilled configurations.

As we know, there are seven solder joints on each of our chip samples. The solder joint are at different locations on the chip. Thermal strain on solder joint is related to the distance of the solder joint to neutral point, thus the solder joints at different locations on the chip may have different fatigue behavior and fatigue life. The neutral point is the location where the chip does not move relative to the substrate. At different temperatures, there are shear forces exerted on solder joints. Those shear forces on (and by) all solder joints must be in equilibrium along both chip horizontal axes, thus there exists the neutral point which is generally in a site near the center of the solder joint array. Considering the solder joint positions and their relationship to the neutral point, we divide the seven solder joints into three groups. Joint 0 itself is one group. Joints 2 and 5 are grouped together since they are symmetric to the neutral point. The third group includes joints 1, 3, 4 and 6 since they are almost symmetric to the neutral point and have very close distance to the neutral point.

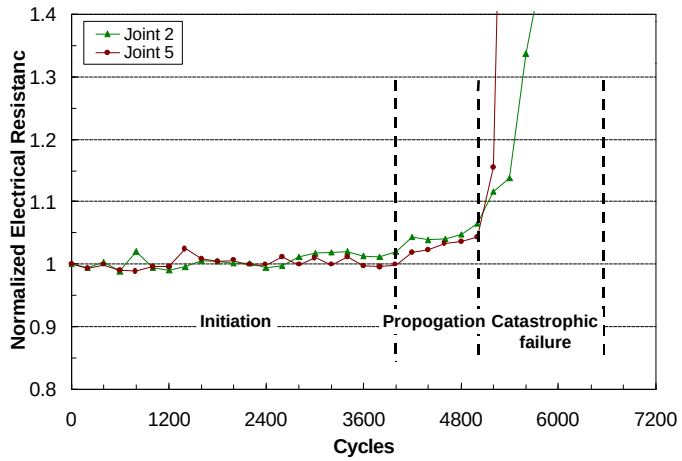
3.3.2.1.1 Single Barrel-Shaped Joints

Figure 3.44 shows the typical electrical resistance increases of single bump barrel-shaped non-underfilled solder joints during temperature cycling. We can see that all the normalized electrical resistance vs. temperature cycle curves have the same trend. From Figure 3.44, it can be clearly see that the curves can be divided into three periods, corresponding to three different fatigue degradation phases which are crack initiation, crack propagation and catastrophic failure. In the crack initiation phase, electrical resistance almost has no increase, while in crack propagation phase, resistance increases with the increasing number of temperature cycles since less and less contact area is left due to crack propagation. Once crack increases to a certain

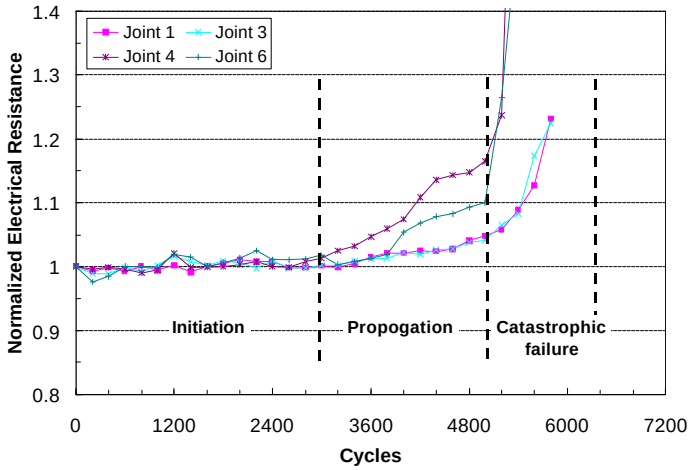
critical level, catastrophic damage occurs and the electrical resistance increases dramatically. Note that we set 20% resistance increase as failure criterion, we can estimate solder joint fatigue lives based on the normalized electrical resistance vs. temperature cycle curves such as those in Figure 3.44. Also we can estimate the crack initiation time, crack propagation time and catastrophic failure time of solder joints from the normalized electrical resistance vs. temperature cycle curves. Figure 3.45 summaries the average fatigue life (crack initiation, crack propagation and catastrophic failure) of single barrel-shaped non-underfilled solder joints at different locations. We can see that the total life of the solder joints at different locations is almost the same. This is probably because the size of the chips we used is small and the solder joints are large compared to the chip. The solder joint size we designed is even larger than the size of general board level interconnections industries commonly use, such as ball grid arrays. However, the size of the board or chip carriers industries use is generally several times larger than the size of our chip. The average total fatigue life of single bump barrel-shaped non-underfilled solder joints is about 5400 cycles. We can also see from Figure 3.45 that the crack initiation, crack propagation and catastrophic failure times for different group of solder joints are also almost the same considering that there is no clear criterion for crack initiation, crack propagation and catastrophic failure. However, it is clear that the crack initiation time is longer than that of crack propagation, with the catastrophic failure time being the shortest for all solder joints. The average crack initiation and propagation times of single bump barrel-shaped non-underfilled solder joints are about 61% and 29% of the average total fatigue lifetime, respectively.



(a)



(b)



(c)

Figure 3.44. Typical electrical resistance increases of single bump barrel-shaped non-underfilled solder joints (a) joint 0; (b) joints 2,5; and (c) joints 1, 3, 4, 6 during temperature cycling.

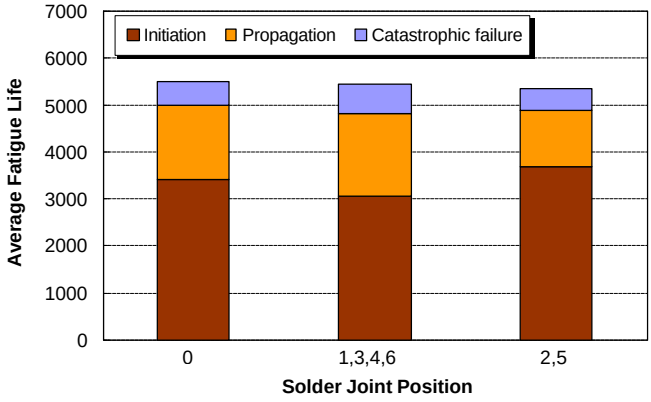
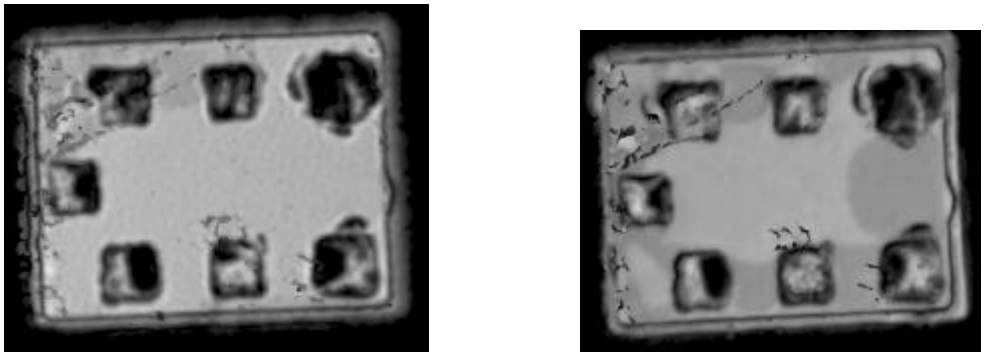


Figure 3.45. Average fatigue life (crack initiation, crack propagation and catastrophic failure) of single bump barrel-shaped non-underfilled solder joints at different locations.

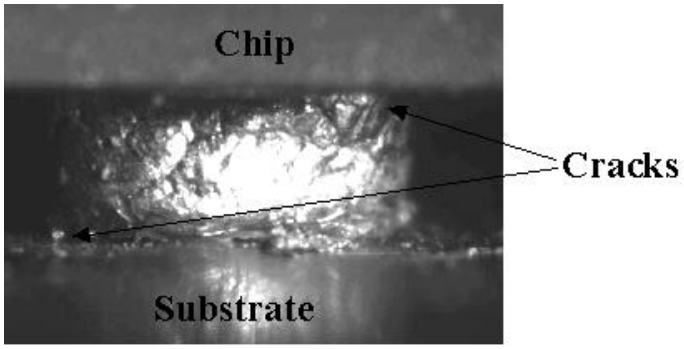
During the temperature cycling test, C mode scanning acoustic microscopy (C-SAM) was employed to examine the solder joint interfaces for cracking, delaminating and voiding. Figure 3.46 shows typical C-SAM images of the interface between solder joints and chip after 3400 and 5600 temperature cycles, respectively. The C-SAM images verified that the electrical resistance increase is due to solder joint cracking. We can see from Figure 3.46 that some parts of the solder joints had faded or were not present at all after 3400 temperature cycles. After 5600 cycles, more areas became faded or were disappeared. This clearly shows the crack propagation during the temperature cycling.



3400 cycles 5600 cycles

Figure 3.46. C-SAM images of the interface between barrel-shaped solder joints and chip during temperature cycling.

The temperature cycling samples were also investigated using optical microscopy during thermal cycling. Figure 3.47 shows side views of single barrel-shaped solder joints after temperature cycling. Cracks were generated at the interface between solder joint and silicon chip and/or at the interface between solder joint and PCB substrate. We found that cracks were more likely to be initiated at the locations that are along the line between the solder joint and the neutral point. Furthermore, cracks were more likely to appear in pairs at the diagonal corners, such as upper-right and lower-left corners, or upper-left and lower-right corners.



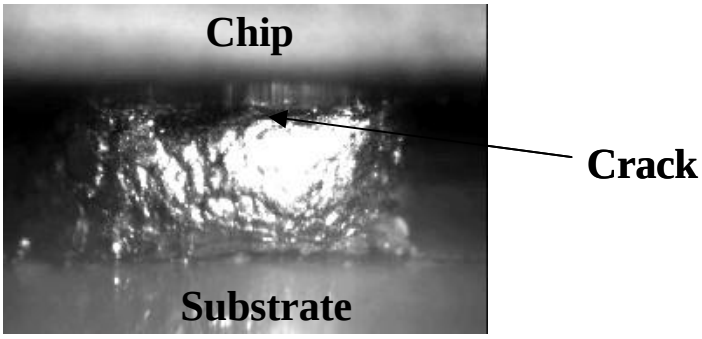
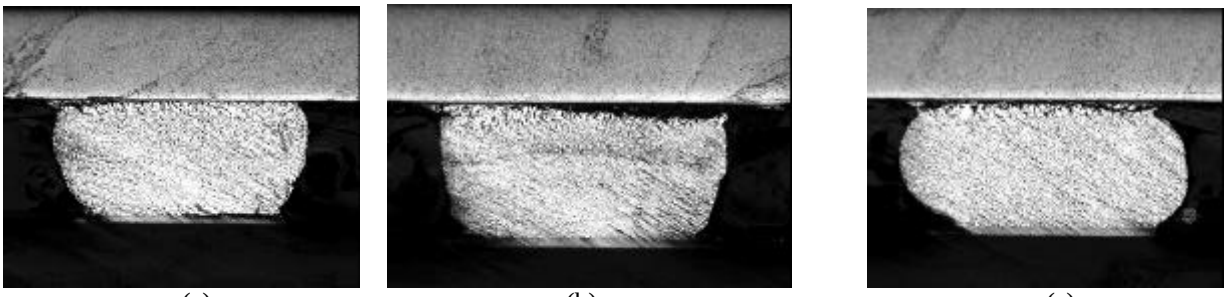


Figure 3.47. Side views of single bump barrel-shaped solder joints after temperature cycling.

Figure 3.48 shows typical cross sections of thermal fatigue failed single barrel-shaped solder joints. The cross sectional pictures show strong correlation between the faded or disappeared parts of the solder joints identified by C-SAM, with the missing information of C-SAM for the interface between solder joint and substrate because the acoustic signal can not penetrate through the whole solder joint thickness and reach the bottom interface. Figure 3.48 (a) and (b) are the dominant thermal fatigue failure modes in single barrel-shaped solder joints. In Figure 3.48 (a), there is a big crack close to or at the interface between solder joint and silicon chip at one corner, while there is one smaller crack at the diagonal corner. In Figure 3.48 (b), there is a bigger crack at one of the solder joint upper corners and a smaller one at the other upper corner, while there are two even smaller cracks at the lower solder joint corners. The other common fatigue failure mode in single barrel-shaped solder joints is illustrated in Figure 3.48 (c), which has two cracks at the upper solder joint corners and sometimes, the two cracks are connected. There are no obvious cracks at the lower corners.



(a) (b) (c)

Figure 3.48. Typical cross sections of thermal fatigue failed single barrel-shaped solder joints.

Figure 3.49 shows one electrical resistance vs. temperature cycling curve for the underfilled case. We can see that the fatigue lifetime of the solder joint for the underfilled case is much improved compared to that without underfill. The electrical resistance showed no

increase until 6000 cycles and there is only a little resistance increase before the whole structure fails. Figure 3.50 is the C-SAM images of the interface between single barrel-shaped underfilled solder joints and chip during temperature cycling. The acoustic images confirm that there is no obvious crack at the interface between solder joint and chip until 5600 cycles. However, at 7600 cycles, there begin to have cracks at the corners of the solder joints and there is severe chip cracking. Chip cracking is the major cause of the sudden increase of electrical resistance. The cross sectional pictures of failed single barrel-shaped underfilled solder joints, as shown in Figure 3.51, indicate that there is no big cracks in the solder joints, but have severe cracks in silicon chip. Furthermore, we can see that the upper parts of the solder joints closer to silicon chip are very rough compared to the lower part of the solder joints.

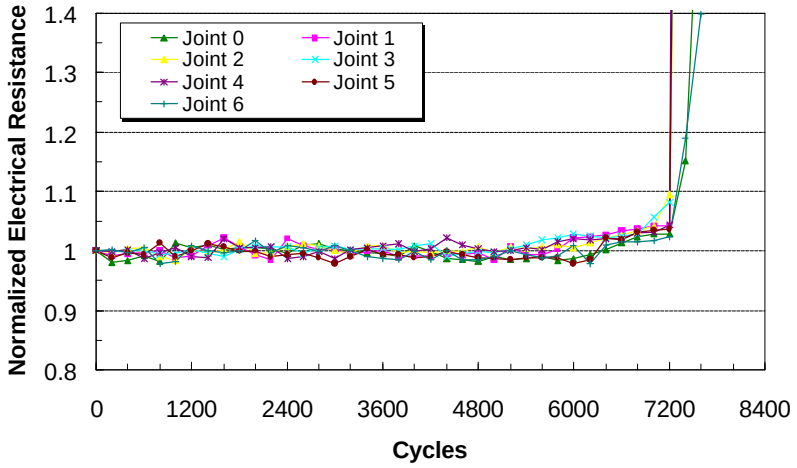


Figure 3.49. Electrical resistance increases of single barrel-shaped underfilled solder joints during temperature cycling.

3400 cycles 5600 cycles 7600 cycles

Figure 3.50. C-SAM images of the interface between single barrel-shaped underfilled solder joints and chip during temperature cycling.

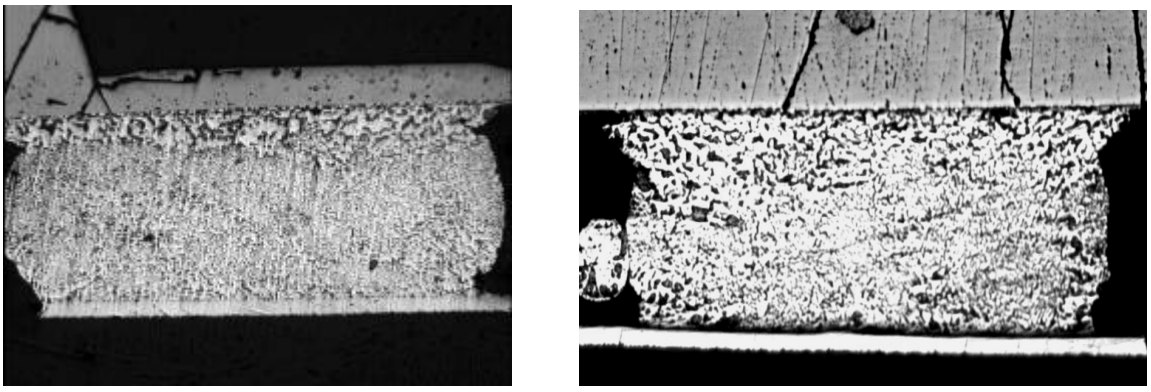
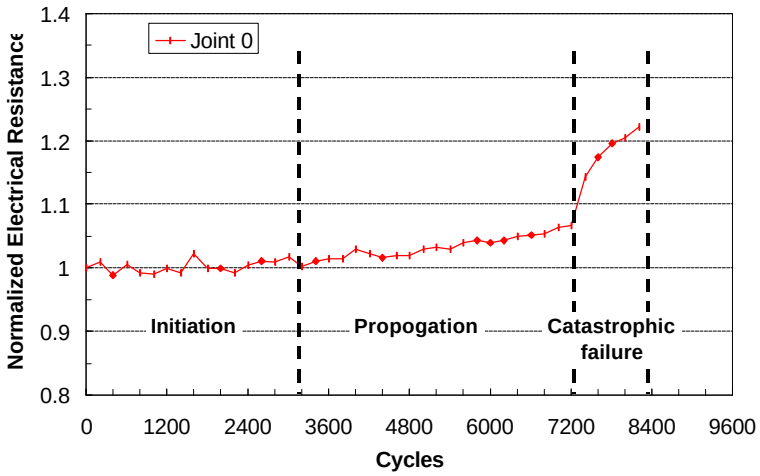


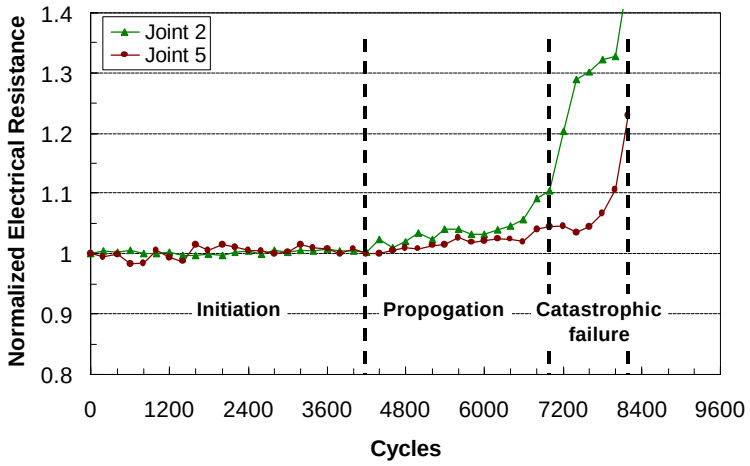
Figure 3.51. Cross sections of failed single barrel-shaped underfilled solder joints.

3.3.2.1.2 Stacked Hourglass/Column-Shaped Joints

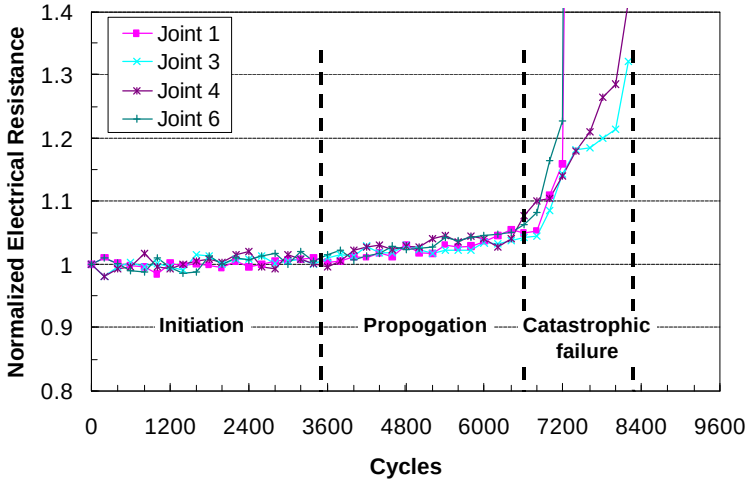
Figure 3.52 shows the typical electrical resistance increases of stacked hourglass/column-shaped non-underfilled solder joints during temperature cycling. Similar to the normalized electrical resistance vs. temperature cycle curves of single barrel-shaped solder joints, we can see that all the normalized electrical resistance vs. temperature cycle curves of stacked hourglass/column-shaped non-underfilled solder joints can also be divided into three periods, corresponding to three different fatigue degradation phases which are crack initiation, crack propagation and catastrophic failure. Figure 3.53 summaries the average fatigue life (crack initiation, crack propagation and catastrophic failure) of stacked hourglass/column-shaped non-underfilled solder joints at different locations. Again, we can see that the total life of the solder joints at different locations is almost the same. The average total fatigue life of stacked hourglass/column-shaped non-underfilled solder joints is about 7600 cycles. We can also see from Figure 3.53 that the crack initiation, crack propagation and catastrophic failure times for different group of solder joints are also almost the same considering that there is no clear criterion for crack initiation, crack propagation and catastrophic failure. However, there is one major difference between the fatigue behavior of stacked hourglass/column-shaped non-underfilled solder joints and single barrel-shaped non-underfilled solder joints which is the ratio of crack propagation life to the total fatigue life. The average crack initiation and propagation times of stacked hourglass-shaped non-underfilled solder joints are about 50% and 40% of the average total fatigue lifetime, respectively.



(a)



(b)



(c)

Figure 3.52. Typical electrical resistance increases of stacked hourglass/column-shaped non-underfilled solder joints (a) joint 0; (b) joints 2,5; and (c) joints 1, 3, 4, 6 during temperature cycling.

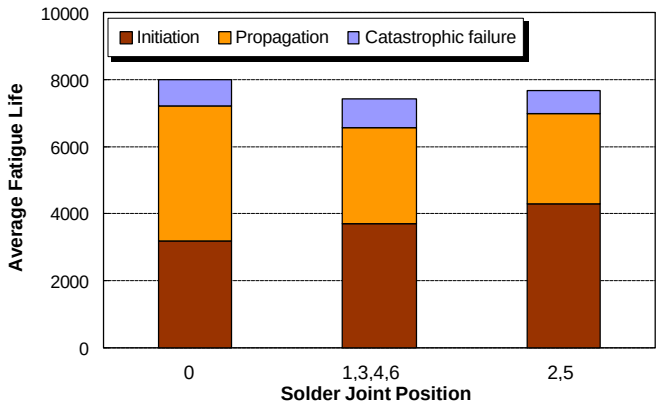
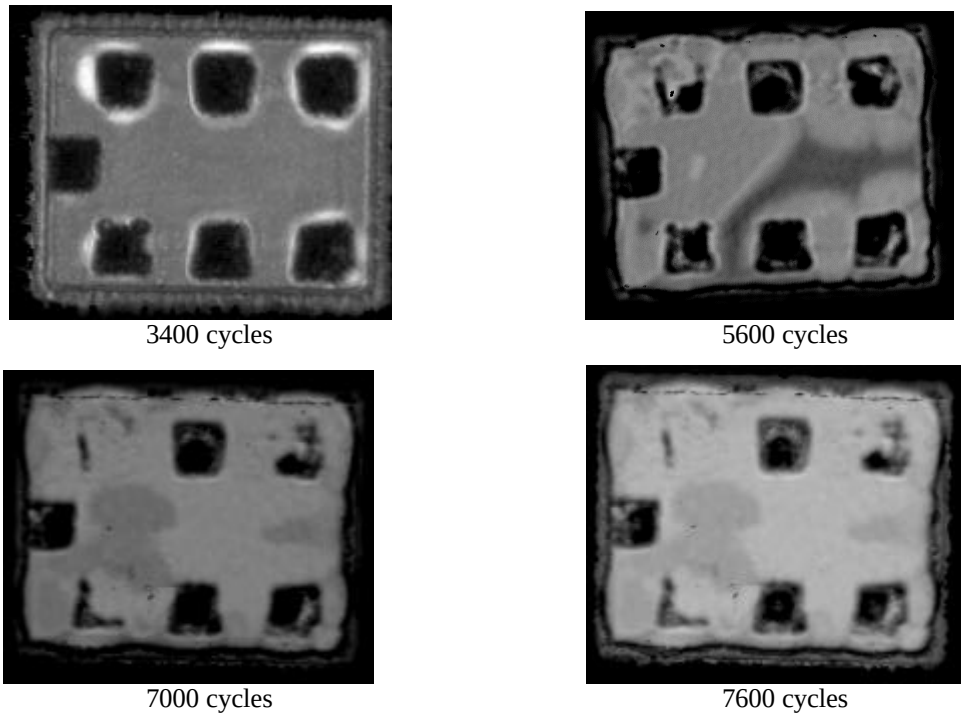


Figure 3.53. Average fatigue life (crack initiation, crack propagation and catastrophic failure) of stacked hourglass/column-shaped non-underfilled solder joints at different locations.

Figure 3.54 shows typical C-SAM images of the interface between stacked hourglass/column-shaped solder joints and chip after 3400, 5600, 7000 and 7600 temperature cycles, respectively. We can see from Figure 3.54 that the solder joints appeared quite homogeneous and pretty well defined after 3400 cycles. However, some parts of the solder joints had faded or were not present at all after 5600 temperature cycles. After 7000 and 7600 cycles, more areas became faded or were disappeared.



3400 cycles 5600 cycles

7000 cycles 7600 cycles

Figure 3.54. C-SAM images of the interface between stacked hourglass/column-shaped solder joints and chip during temperature cycling.

Figure 3.55 shows side views of stacked hourglass/column-shaped solder joints during temperature cycling. Different from the single barrel-shaped solder joints, cracks appeared not only at the interface between solder joint and silicon chip and/or at the interface between solder joint and PCB substrate, but also inside the solder joint. Like the single barrel-shaped solder joints, cracks were more likely to be initiated at the locations that are along the line between the solder joint and the neutral point. We can also see from Figure 3.55 that stacked hourglass/column-shaped solder joints are distorted during thermal cycling.

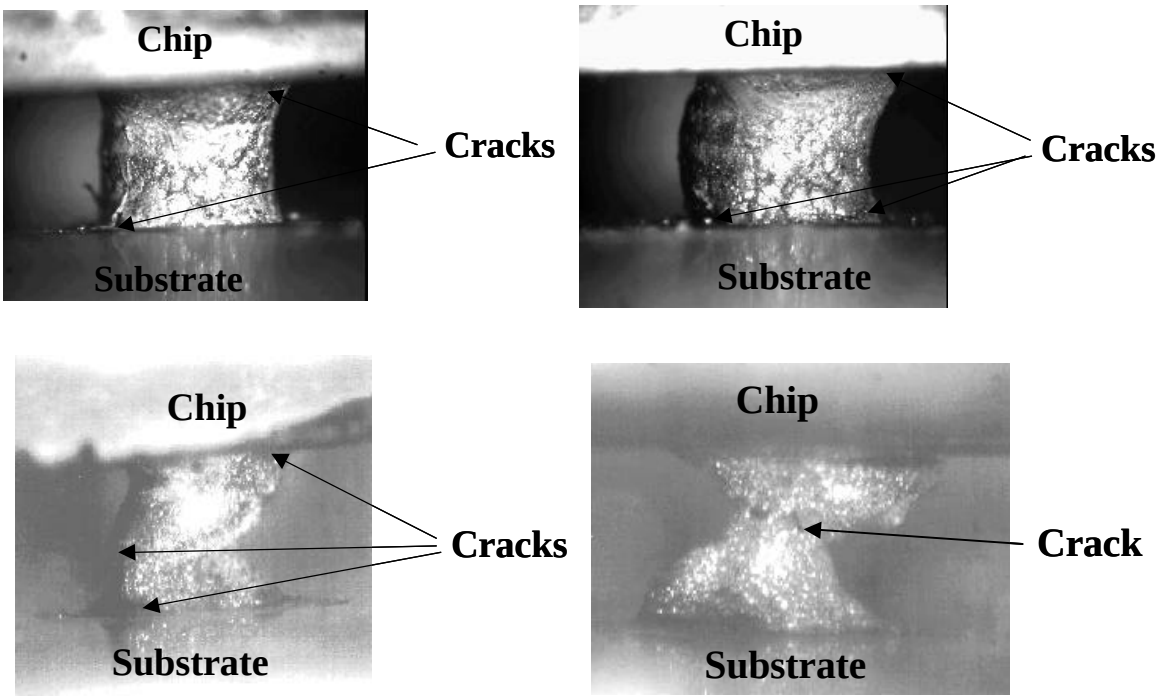


Figure 3.55. Side views of stacked hourglass/column-shaped solder joints after temperature cycling.

Figure 3.56 shows typical cross sections of thermal fatigue failed stacked hourglass/column-shaped solder joints. The cross sectional pictures show strong correlation between the faded or disappeared parts of the solder joints identified by C-SAM, with the missing information of C-SAM for the interface between solder joint and substrate because the acoustic signal can not penetrate through the whole solder joint thickness and reach the bottom interface. Figure 3.56 (a), (b) (c) are the dominant thermal fatigue failure modes in stacked solder joints which are more like column-shaped and have lower standoff. In Figure 3.56 (a), there is a big crack close to or at the interface between solder joint and silicon chip at one corner, while there is one smaller crack at the diagonal corner. In Figure 3.56 (b), there are cracks at each of the solder joint corners. For Figure 3.56 (c), which has two cracks at the upper solder

joint corners and sometimes, the two cracks are connected. There are no obvious cracks at the lower corners. Figure 3.56 (d), (e) and (f) are the dominant thermal fatigue failure modes in stacked solder joints which are more like hourglass-shaped and have higher standoff. In this case, failure is likely to occur inside of the solder joints as well as at the interfaces. We did not observe severe failures at the interfaces between the different solder layers.

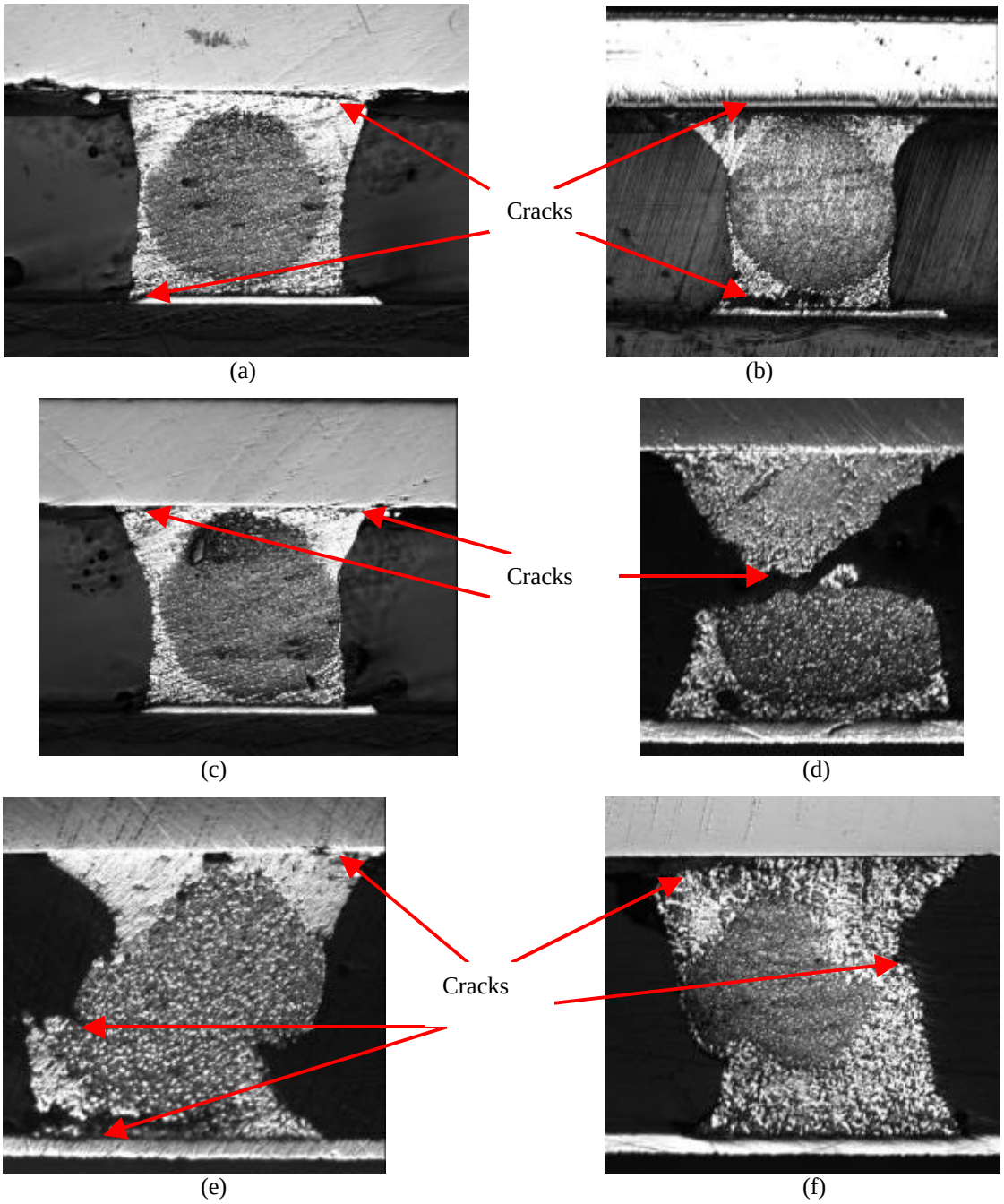


Figure 3.56. Typical cross sections of thermal fatigue failed stacked hourglass/column-shaped solder joints.

Figure 3.57 shows electrical resistance vs. temperature cycling curves for the underfilled case. We can see that the fatigue lifetime of the solder joint for the underfilled case is much improved compared to that without underfill. The electrical resistance showed no increase until 7200 cycles and resistance increases slowly until the structure fails. Figure 3.58 is the C-SAM images of the interface between stacked hourglass/column-shaped underfilled solder joints and chip during temperature cycling. The acoustic images confirm that there is no obvious crack at the interface between solder joint and chip until 7600 cycles. However, at 8600 cycles, there began to have cracks at the corners of the solder joints and the cracks gradually grow. The typical cross sectional pictures of failed stacked hourglass/column-shaped underfilled solder joints are shown in Figure 3.59. Again, Figure 3.59 (a), (b) (c) are the dominant thermal fatigue failure mode in stacked solder joints which are more like column-shaped and have lower standoff. We can also see that the solder material close to the interfaces, especially the solder joint and chip interface is very rough compared to the other part of the solder joints. Figure 3.56 (e), (d) (f) are the dominant thermal fatigue failure mode in stacked solder joints which are more like hourglass-shaped and have higher standoff. In this case, the solder joint are distorted and failure likely to occur inside of the solder joints as well as at the interfaces. However, there is no failure observed at the interfaces between the different solder layers.

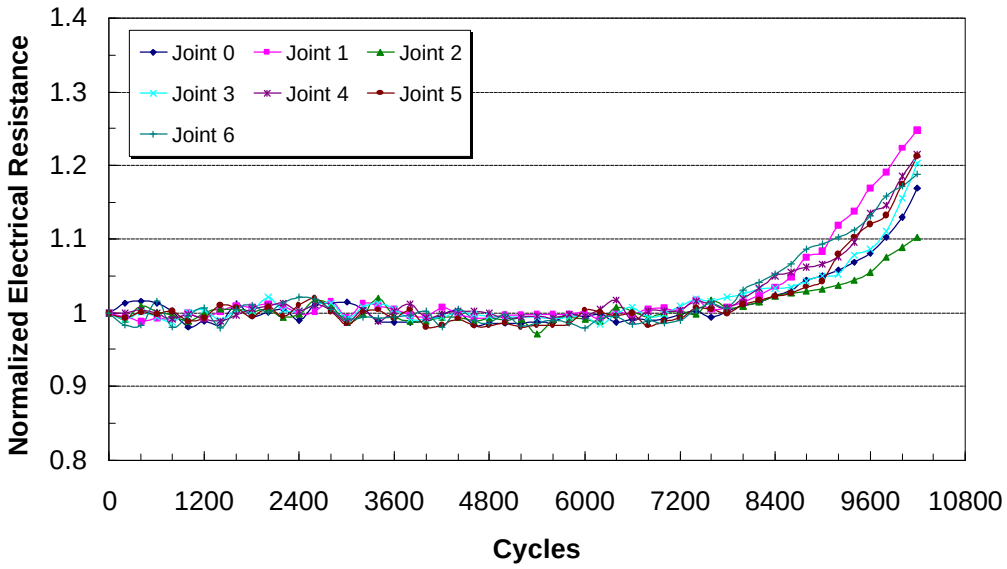


Figure 3.57. Electrical resistance increases of stacked hourglass/column-shaped underfilled solder joints during temperature cycling.

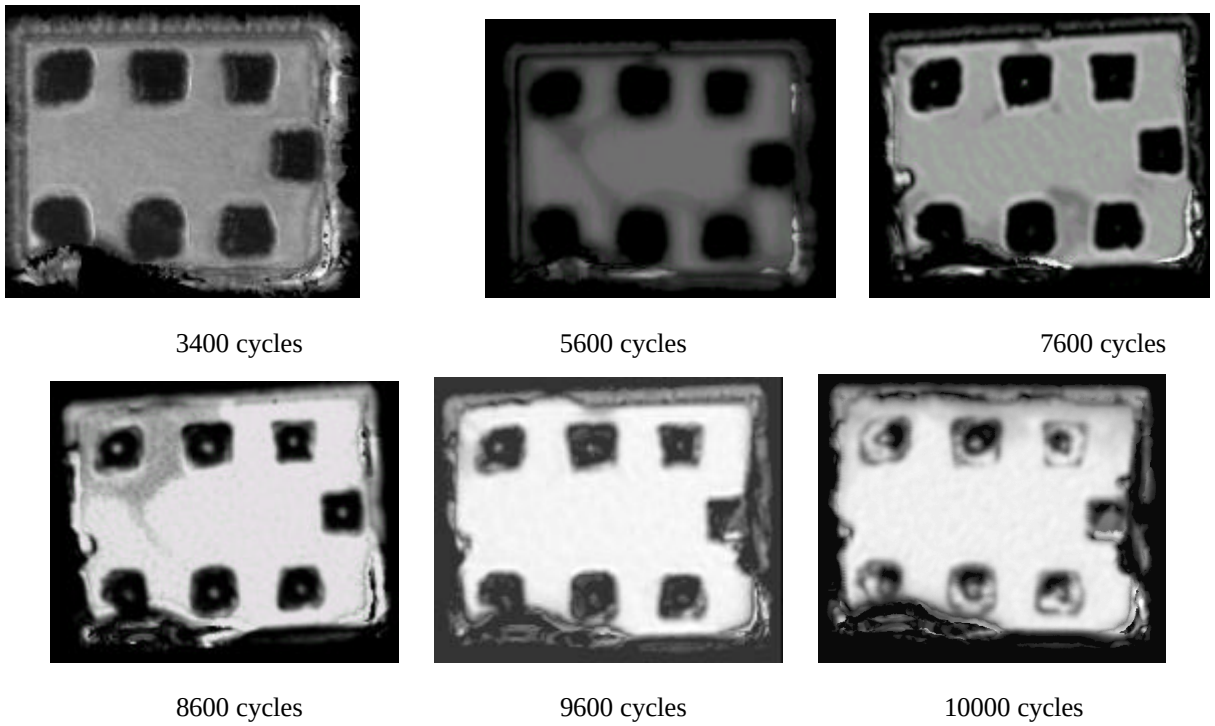


Figure 3.58. C-SAM images of the interface between stacked hourglass/column-shaped underfilled solder joints and chip during temperature cycling.

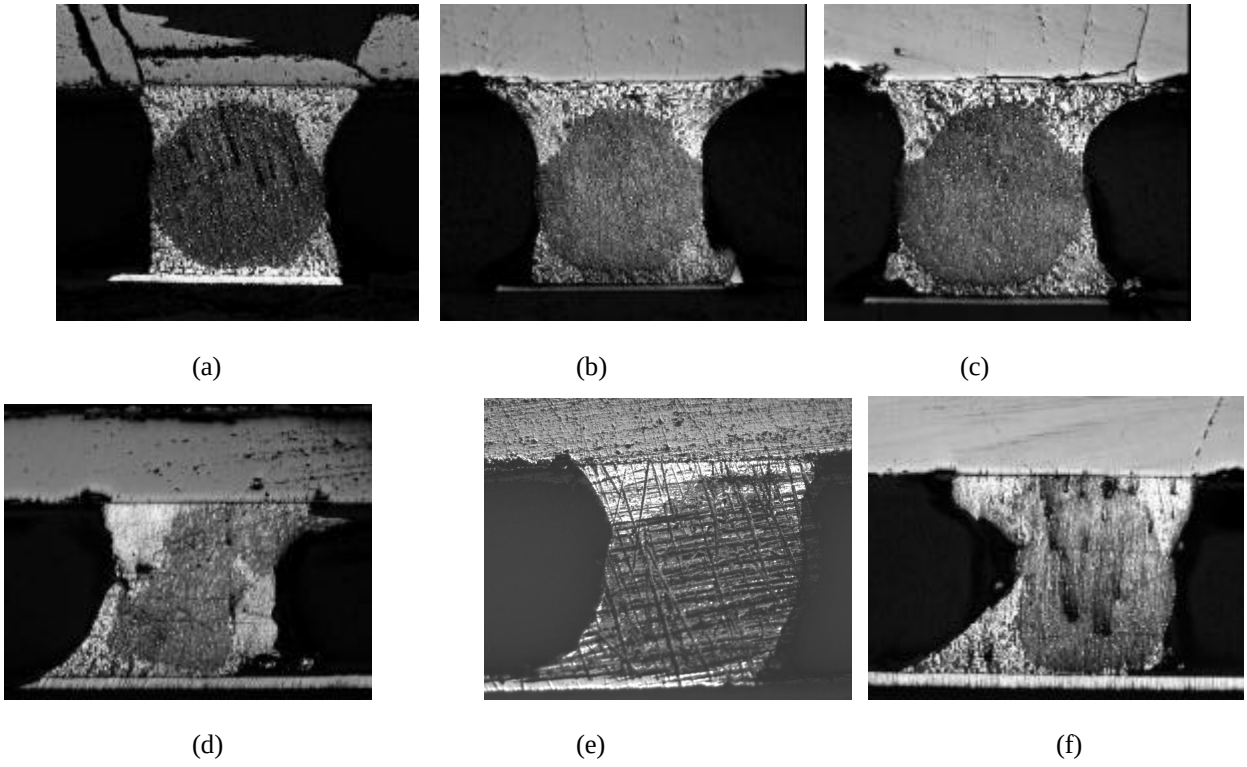


Figure 3.59. Typical cross sections of thermal fatigue failed stacked hourglass/column-shaped underfilled solder joints.

3.3.2.2 Results on the Second Set of Samples

The second set of samples has three solder joint configurations: single bump barrel-shaped solder joint, stacked barrel-shaped solder joint, and triple stacked hourglass/column-shaped solder joint. All of them are not underfilled. There are seven solder joints on each of our chip samples and the solder joints are at different locations on the chip. However, from the results of the first set of samples, we knew that there is no significant difference in thermal fatigue behaviors among the solder joints at different locations on chip because the chip we used is rather small and the solder joints are quite large. Therefore, for the second set of samples, we will no longer divide the seven solder joint into three groups and just treat them as one group. Note that, as we introduced before, the temperature cycling condition of the second set of samples is different from the first set of samples.

3.3.2.2.1 Single Bump Barrel-Shaped Joints

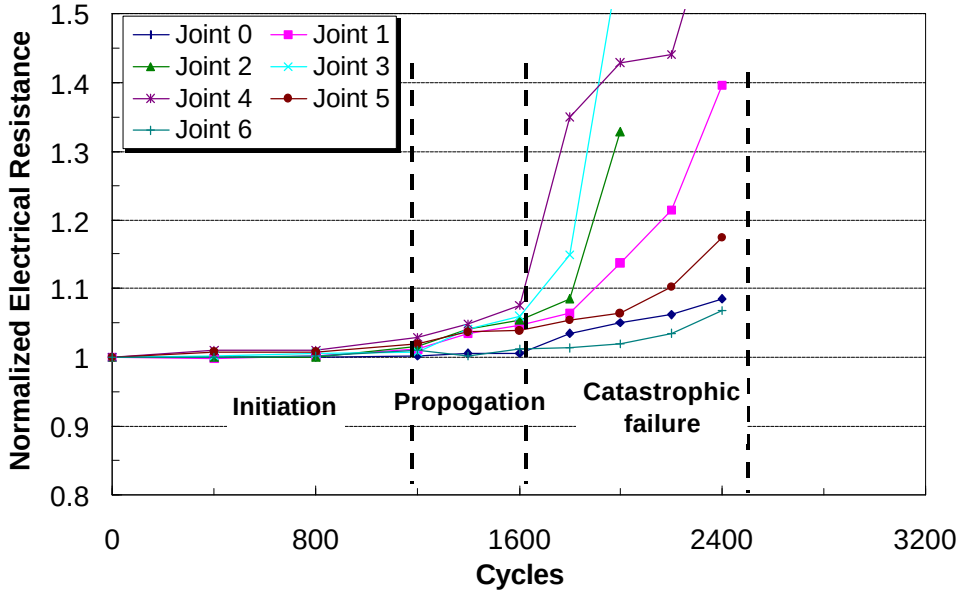
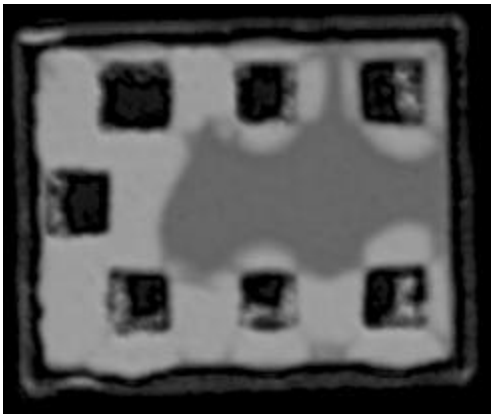


Figure 3.60. Typical electrical resistance increases of single bump barrel-shaped solder joints during temperature cycling.

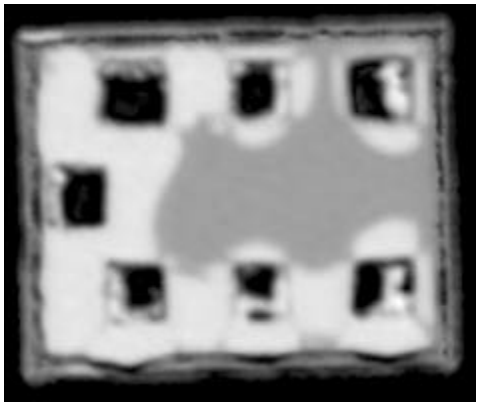
Figure 3.60 shows the typical electrical resistance increases of single bump barrel-shaped solder joints during temperature cycling. We can see that all the normalized electrical resistance vs. temperature cycle curves have the same trend. From Figure 3.60, it can be clearly seen that the curves can be divided into three periods just like the first set of samples, corresponding to

three different fatigue degradation phases which are crack initiation, crack propagation and catastrophic failure. Again, we set 20% resistance increase as failure criterion and solder joint fatigue lives can be estimated based on the normalized electrical resistance vs. temperature cycle curves such as those in Figure 3.60. The average fatigue lifetime of single bump barrel-shaped solder joints is about 2200 cycles. We can also estimate the crack initiation time, crack propagation time and catastrophic failure time of solder joints from the normalized electrical resistance vs. temperature cycle curves.

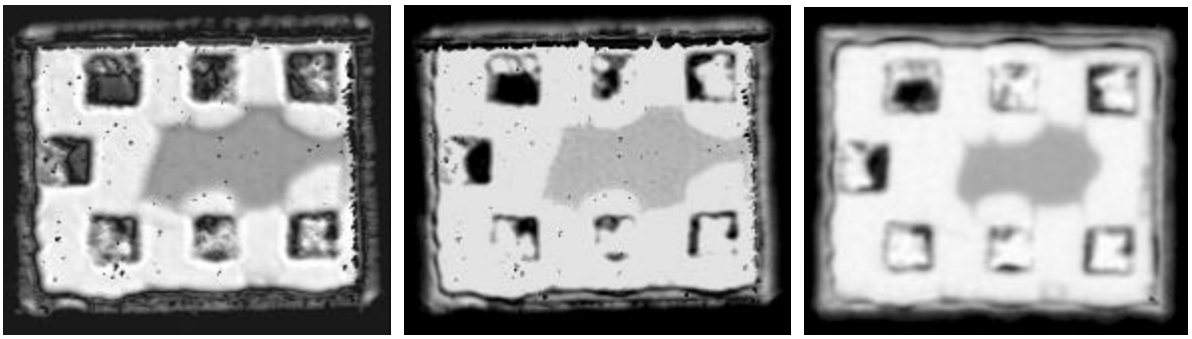
Figure 3.61 shows typical C-SAM images of the interface between single barrel-shaped solder joints and chip after 1400, 1700, 2000, 2200 and 2400 temperature cycles, respectively. The C-SAM images verified that the electrical resistance increase is due to solder joint cracking. We can see from Figure 3.61 that some parts of the solder joints had faded or were not present at all after 1400 temperature cycles. More and more areas became faded or were disappeared afterwards. This clearly shows the crack propagation during the temperature cycling. The other obvious phenomenon we can see from the C-SAM images is that cracks are initiated at the outer end of the solder joints and propagate centripetally towards the neutral point. As we introduced before, crack area can be set to different colors and calculated using the National Instruments IMAQ Vision Builder software. We calculated solder joint crack area at different temperature cycles and monitored the crack growth process. Figure 3.62 shows the fractional crack area of solder joint and chip pad interface for the seven solder joints on a test chip at 1400, 1700, 2000, 2200 and 2400 temperature cycles. We can see that the fractional crack area increases with the increasing of temperature cycles.



1400 cycles



1700 cycles



2000 cycles 2200 cycles 2400 cycles

Figure 3.61. C-SAM images of the interface between single barrel-shaped solder joints and chip during temperature cycling.

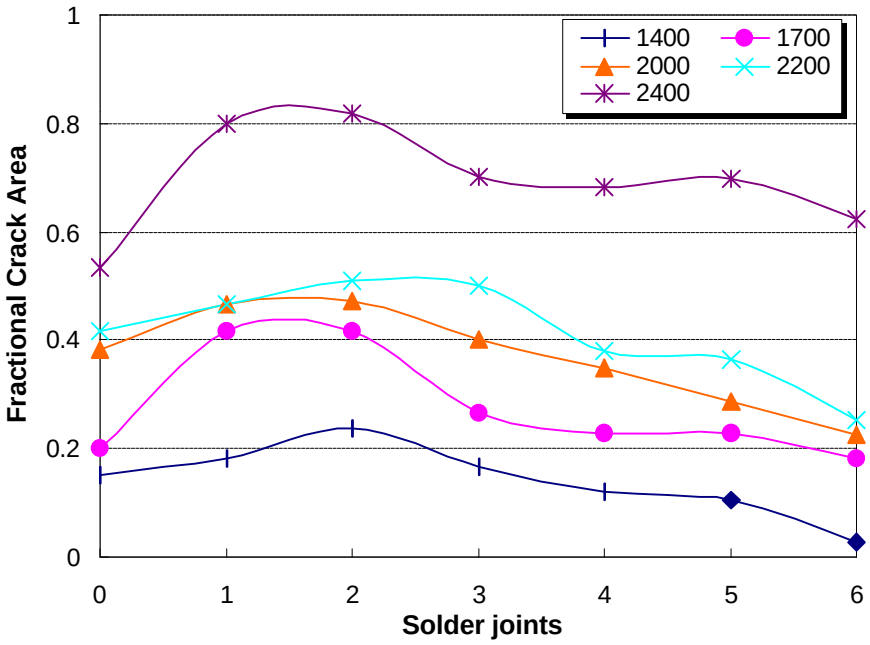
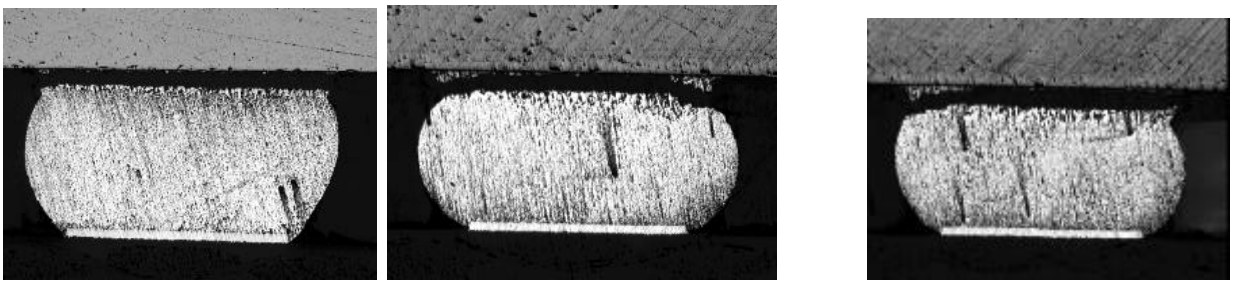


Figure 3.62. The fractional crack area of solder joint and chip pad interface for the seven solder joints on a test chip at different temperature cycles.

Figure 3.63 shows typical cross sections of thermal fatigue failed single barrel-shaped solder joints. The majority of the samples failed at the interface between solder joint and chip pad. A small fractional of the samples have tiny cracks at the corners of the solder joint and substrate interface. We observed that the solder materials around cracks appeared to be very rough and the corners of the solder joints are also very rough though there may not have obvious cracks.



(a) (b) (c)

Figure 3.63. Typical cross sections of thermal fatigue failed single barrel-shaped solder joints.

3.3.2.2.2 Stacked Hourglass/Column-Shaped Joints

Figure 3.64 shows the typical electrical resistance increases of stacked hourglass/column-shaped solder joints during temperature cycling. Again the curves can be divided into three periods, corresponding to crack initiation, crack propagation and catastrophic failure. The average total fatigue life of stacked hourglass/column-shaped solder joints is about 3500 cycles, which is greater than single bump barrel-shaped solder joints. Compared with the electrical resistance change curves of single bump barrel-shaped solder joints, both the crack initiation time and crack propagation time is longer. However, it is obvious that crack propagation time increased more than crack initiation time.

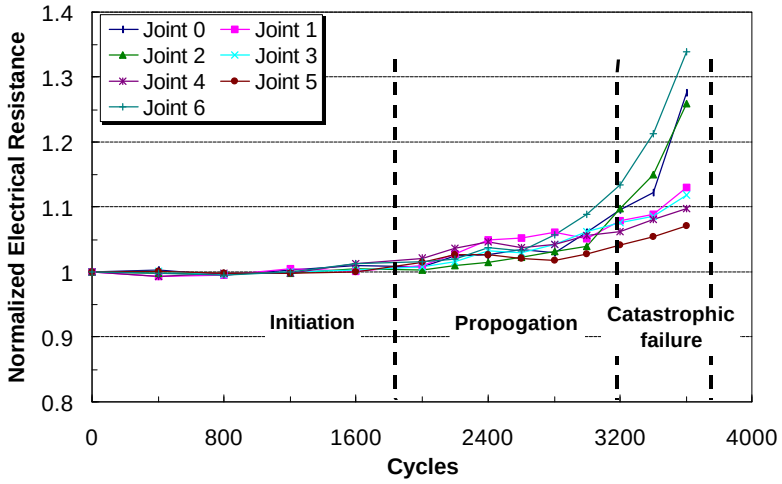


Figure 3.64. Typical electrical resistance increases of stacked hourglass/column-shaped solder joints during temperature cycling.

Figure 3.65 shows typical C-SAM images of the interface between stacked hourglass/column-shaped solder joints and chip after 1400, 2000, 2400, 2800, 3200, 3400 and 3600 temperature cycles, respectively. We can see from Figure 3.65 that the solder joints

appeared quite homogeneous and pretty well defined after 1400 cycles. However, some parts of the solder joints had faded or were not present at all after 2000 temperature cycles and gradually more and more areas became faded or were disappeared. Also we can see from the C-SAM images that cracks are initiated at the outer end of the solder joints and propagate centripetally towards the neutral point just like what we observed in the single barrel-shaped solder joints. We also calculated solder joint crack areas at different temperature cycles using the National Instruments IMAQ Vision Builder software. Figure 3.66 shows the fractional crack area of solder joint and chip pad interface for the seven solder joints on a test chip at 1400, 2000, 2400, 2800, 3200, 3400 and 3600 temperature cycles.

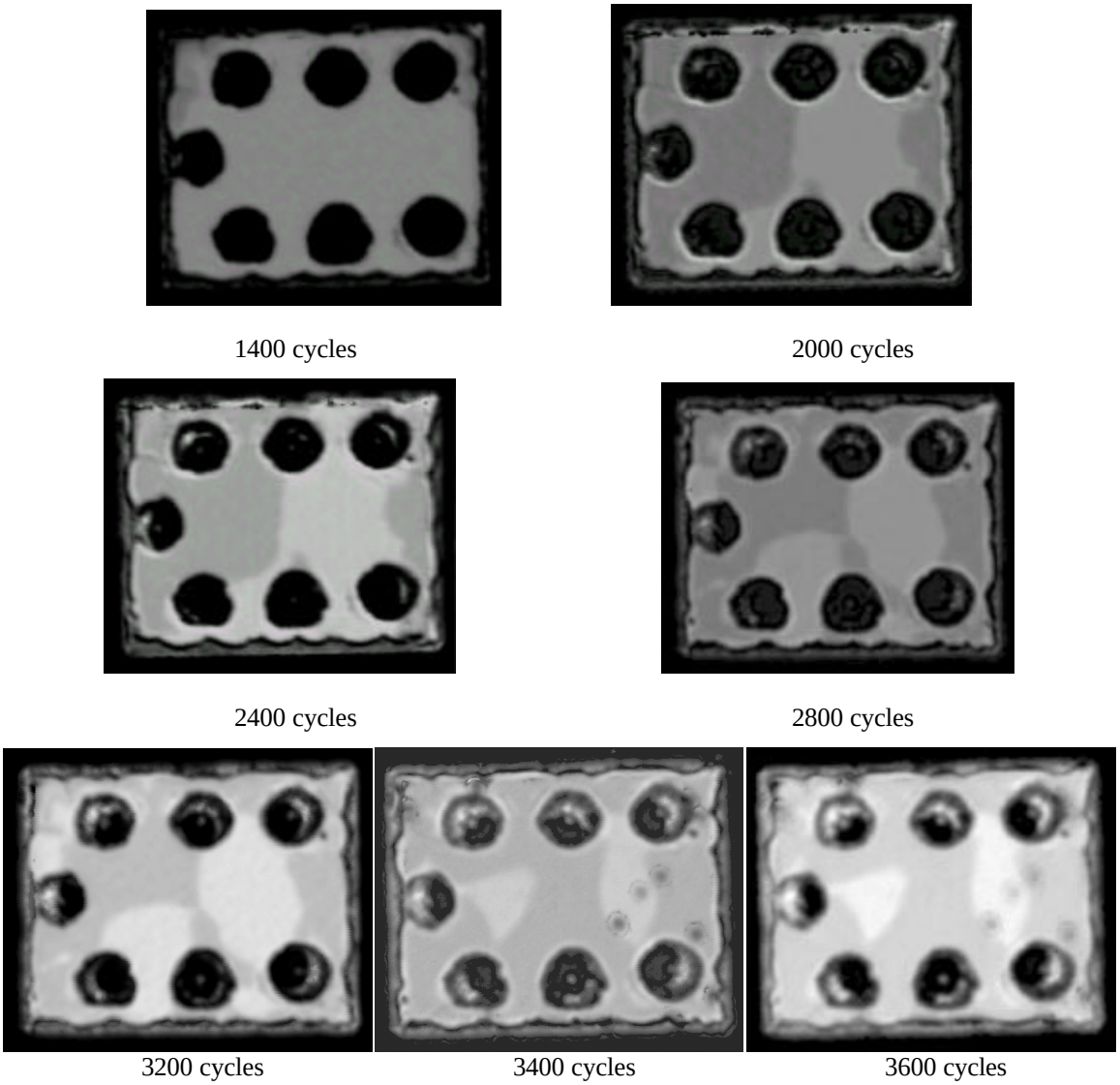


Figure 3.65. C-SAM images of the interface between stacked hourglass/column-shaped solder joints and chip during temperature cycling.

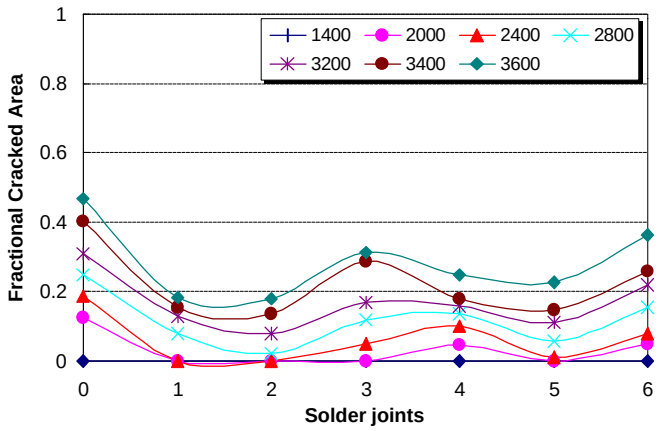
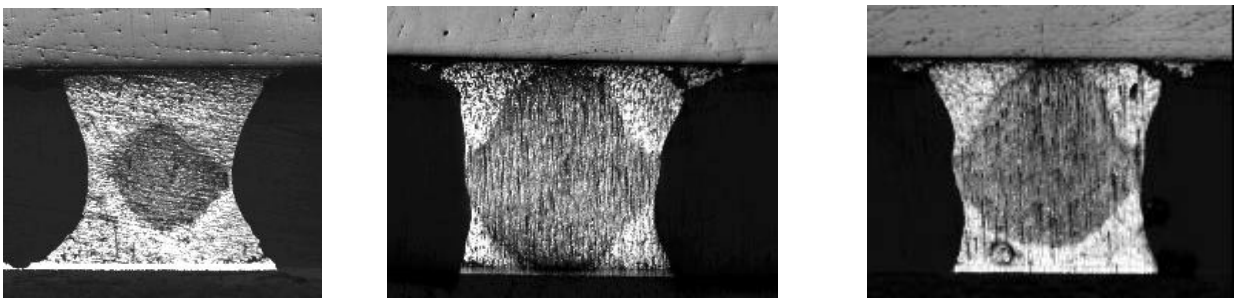


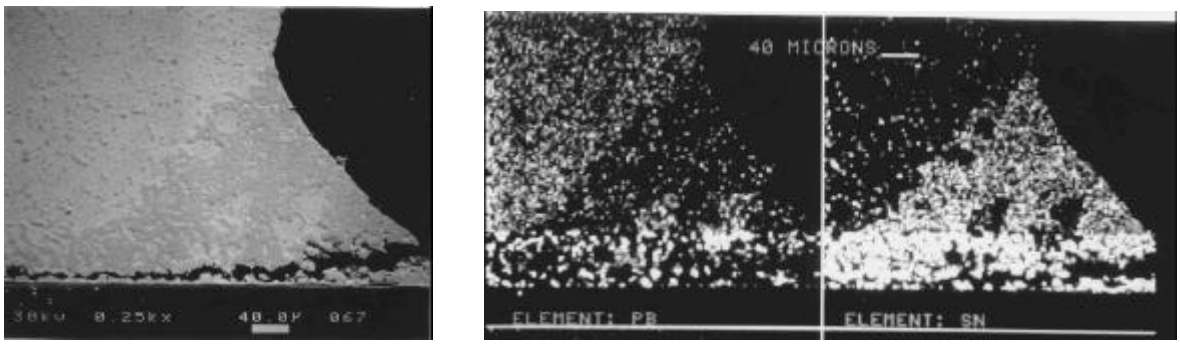
Figure 3.66. The fractional crack area of solder joint and chip pad interface for the seven solder joints on a test chip at different temperature cycles.

Figure 3.67 shows typical cross sections of thermal fatigue failed stacked hourglass/column-shaped solder joints. In Figure 3.67 (a), there is a big crack close to or at the interface between solder joint and silicon chip at one corner, while there is one smaller crack at the diagonal corner. For the sample shown in Figure 3.67 (b), there is a bigger crack at one of the solder joint upper corners and a smaller one at the other upper corner, while there is one or sometimes two tiny cracks at the lower solder joint corners. The failed sample in Figure 3.67 (c) has two cracks at the upper solder joint corners and sometimes, the two cracks are connected. There are no obvious cracks at the lower corners. The interfaces between the different solder layer inside the triple-stacked solder joint is robust and there is no fatigue failure at these interfaces. Figure 3.68 is a SEM and EDX mapping of one corner of a fatigue failed triple-stacked solder joint. The left EDX picture shows the Pb element EDX mapping, while the right one shows the Sn element mapping. EDX results showed that the boundaries of different solder compositions are still well defined, just like those as processed samples.



(a) (b) (c)

Figure 3.67. Typical cross sections of thermal fatigue failed stacked hourglass/column-shaped solder joints.



(a) (b)

Figure 3.68. (a) SEM picture; (b) EDX mapping of one corner of a fatigue failed triple-stacked solder joint.

3.3.2.2.3 Stacked Barrel-Shaped Joints

Figure 3.69 shows the typical electrical resistance increases of stacked barrel-shaped solder joints during temperature cycling. The curves is also divided into three periods, corresponding to crack initiation, crack propagation and catastrophic failure. The average total fatigue life of stacked barrel-shaped solder joints is about 3000 cycles, which is greater than single bump barrel-shaped solder joints, but lower than stacked hourglass/column-shaped solder joints. We can see that the crack initiation time of stacked barrel-shaped solder joints is roughly the same as that of single bump barrel-shaped solder joints, while the crack propagation time is similar to that of stacked hourglass/column-shaped solder joints.

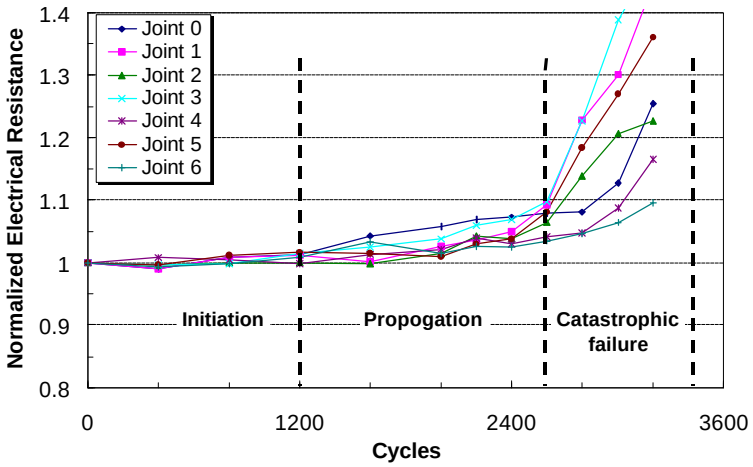


Figure 3.69. Typical electrical resistance increases of stacked barrel-shaped solder joints during temperature cycling.

Figure 3.70 shows typical C-SAM images of the interface between stacked barrel-shaped solder joints and chip after 1400, 2000, 2400, 2800, 3000, and 3200 temperature cycles,

respectively. The fourth solder joint was not processed well and it failed very early. Different from stacked hourglass/column-shaped solder joints, but similar to single bump barrel-shaped solder joints, some parts of the solder joint and chip pad interface had faded or were not present after 1400 temperature cycles, as we can see from Figure 3.70. Afterwards, more and more areas gradually became faded or were disappeared. However, from the C-SAM images, we can know that the cracks in stacked barrel-shaped solder joints do not grow as fast as those in single barrel-shaped solder joints. This is in agreement with the electrical resistance change curves which showed that the crack propagation time for stacked barrel-shaped solder joints is longer. Similar to the previous two cases, cracks in stacked barrel-shaped solder joints are also initiated at the outer end of the solder joints and propagate centripetally towards the neutral point.

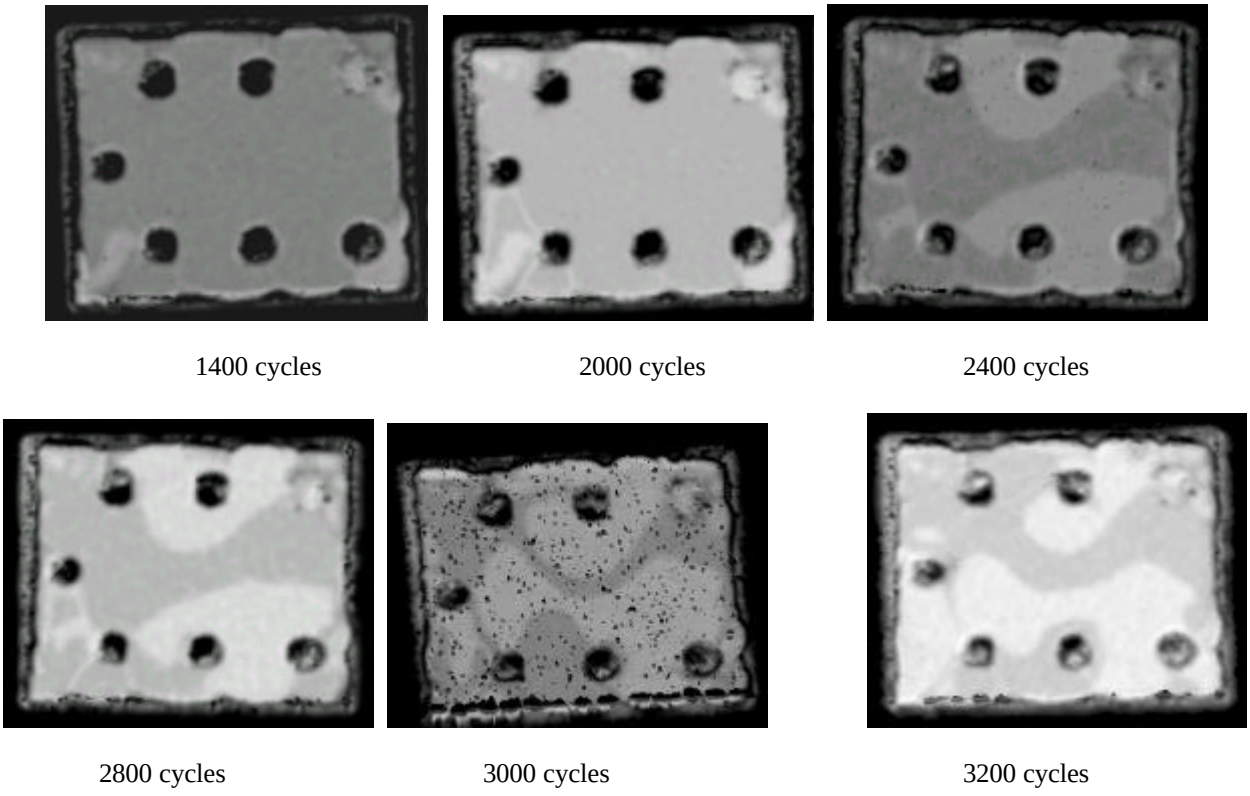


Figure 3.70. C-SAM images of the interface between stacked barrel-shaped solder joints and chip during temperature cycling.

Figure 3.71 shows typical cross sections of thermal fatigue failed stacked barrel-shaped solder joints. Due to the difficulty of precise control of solder paste volume and smaller pad size in this stacked barrel-shaped solder joint design, the fabricated solder joint geometry is not ideal.

The fabricated barrel-shaped solder joints dominantly failed at the interface between solder joint and chip pad, as shown in Figure 3.71.

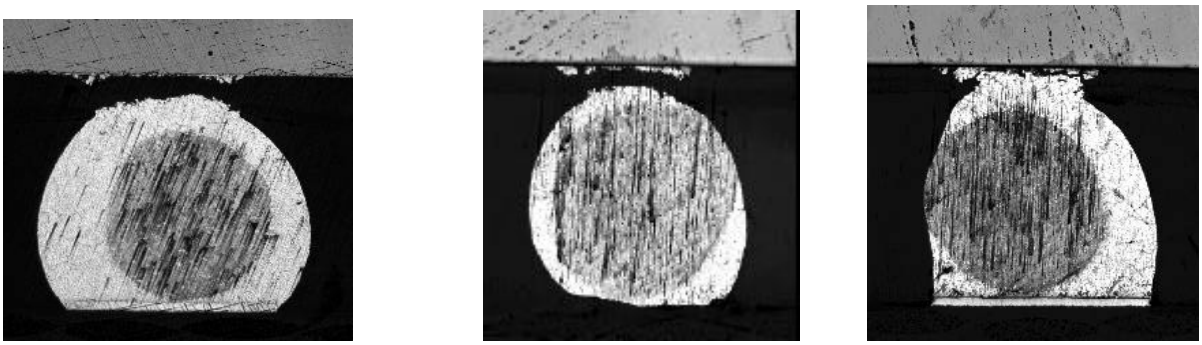


Figure 3.71. Typical cross sections of thermal fatigue failed stacked barrel-shaped solder joints.

3.4 Discussion

In this section, we analyze solder joint fatigue failure physics based on temperature cycling and adhesion test results. The effects of solder joint shape and height on thermal fatigue are discussed.

3.4.1 Solder Joint Fatigue Failure Physics

3.4.1.1 Fatigue Damage Process

Based on our experimental results on temperature cycling, solder joint fatigue failure process for all the different configurations can be divided into three phases: the initiation of macroscopic cracks, the propagation of the cracks, and catastrophic failure of the solder joint. The schematic in Figure 3.72 illustrates the solder joint fatigue damage process. In the crack initiation period, there is no obvious increase of electrical resistance. Electrical resistance increases gradually in the crack propagation phase and there is a sudden change of resistance in the catastrophic failure. C-SAM images showed strong correlation between the initiation and growth of cracks in solder joints and the change of electrical resistance of solder joints.

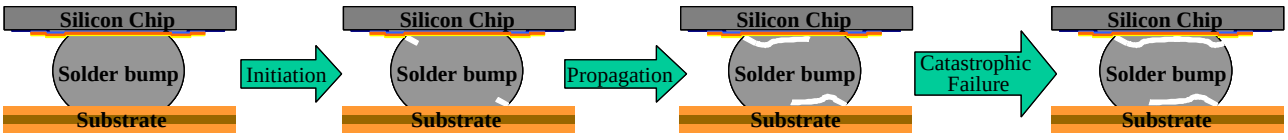


Figure 3.72. Illustration of solder joint fatigue damage process.

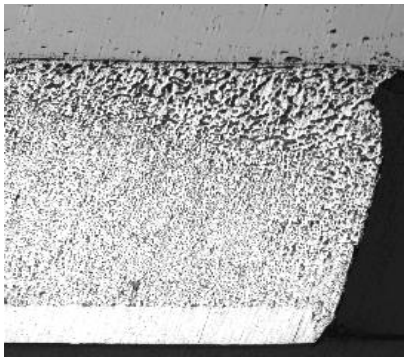
According to the literature, it is well accepted that the general fatigue process of a metal when subjected to cyclic stress can be divided into the following stages [28]:

1. Crack initiation-includes the early development of fatigue damage which can be removed by a suitable thermal anneal.
2. Slip-band crack growth-involves the deepening of the initial crack on planes of high shear stress. This frequently is called stage I crack growth.
3. Crack growth on planes of high tensile stress-involves growth of well-defined crack in direction normal to maximum tensile stress. Usually called stage II crack growth.
4. Ultimate ductile failure-occurs when the crack reaches sufficient length so that the remaining cross section can not support the applied load.

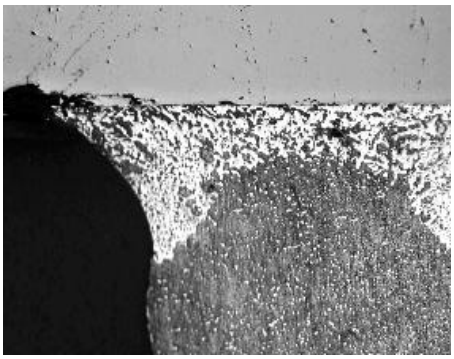
In our case, the first two stages were combined in the crack initiation phase since phenomenologically there was no evident resistance increase and macroscopically there were no obvious cracks in solder joints. Naturally, the crack propagation and catastrophic failure phases correspond to the third and fourth stages we mentioned before. As we introduced in section 3.1.2, there are a large number of solder joint fatigue models in the literature which were used to explain and/or predict solder joint fatigue behavior and lifetime. These models were classified into four major categories: (i) plastic strain-based approach; (ii) creep strain-based approach; (iii) energy-based approach; and (iv) fracture mechanics-based approach. Unfortunately, our experimental data can be explained by none of the four category models. Basically, these models only characterize and emphasize one aspect of the solder joint fatigue behavior. Both plastic strain-based approach and creep strain-based approach regard the irreversible inelastic deformation is the driving force of micro damage processes. Thus these two types of approaches only describe and predict crack initiation life. The energy-based approach presents a kind of combination of strain-based and stress-based approaches. Clearly, the models in this category also only predict the fatigue life of a solder joint until the appearance of macroscopic cracks. On the other hand, the propagating mechanism of the cracks inside a solder joint under cyclic loading is controlled by fracture mechanics. Fracture mechanics approach assumes a microscopic flaw or crack initiator exists in solder joint and begins to grow from the beginning of thermal cycle. Therefore, the fracture mechanics-based approach predicts only the part of fatigue life when a macroscopic crack propagates through the solder joint to cause its electric

and/or mechanical failure. Only recently, some new models such as damage evolution model [29] were proposed in electronic packaging field to characterize and predict both parts of fatigue lives due to crack initiation and propagation. These models normally use finite element technique to calculate thermal strains and stresses. The relative proportion of the total cycles to failure that are involved with each phases depends on the solder joint geometry, material and test conditions, as we showed in the previous sections. However, it can be concluded that each of the crack initiation, crack propagation and catastrophic failure stages need to be considered in order to fully study the solder joint fatigue behavior and accurately predict fatigue lifetime.

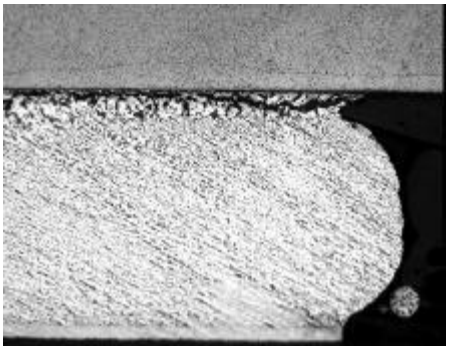
It is well known that a metal deforms under cyclic strain by slip in the so-called stage I crack growth period [28]. Ridges and grooves called slip-band extrusions and slip-band intrusions will be formed on the surface of a metal subjected to fatigue deformation. In our research, coarsened zones were observed in solder joints close to the chip and solder joint interface, especially at the corners, and sometimes also at the regions close the solder joint and substrate interface after a certain number of temperature cycles. Figure 3.73 shows the coarsened bands in temperature cycled solder joints before and after macrocrack formation for both single bump barrel-shaped solder joints and stacked hourglass-shaped solder joints. Apparently, the coarsened zones are the weak regions developed under cyclic strains and these regions are more likely to have cracks. Other researchers also reported the appearance of these coarsened bands in thermal fatigued solder joints and it was reported that the coarsened band is composed of a large primary Pb-rich phase [30]. We believe that these coarsened zones are also caused by slip under cyclic strains. Therefore, phenomenologically, the crack initiation phase in solder joint may undergo progressive events involving deformation by slip, slip-band extrusions and slip-band intrusions formation, and microcrack initiation and propagation.



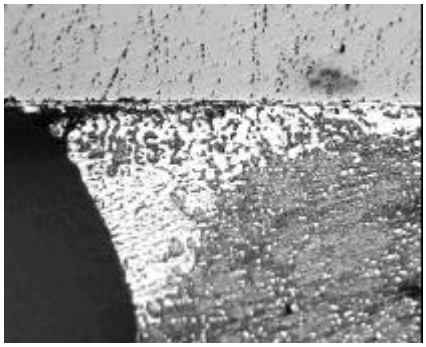
(a)



(b)



(c)



(d)

Figure 3.73. Coarsened zones in temperature cycled solder joints; (a) and (b) before macrocrack formation; (c) and (d) after macrocrack formation and propagation.

There is no evident electrical resistance increase at 800 temperature cycles for both single bump barrel-shaped and stacked hourglass-shaped solder joints, especially for stacked hourglass-shaped solder joint, there is even no obvious crack at 1400 cycles according to C-SAM images. However, tensile and shear tests showed that tensile and shear loads of single bump barrel-shaped and stacked hourglass-shaped solder joints reduce after 800 temperature cycles. This probably can be explained by the formation of the coarsened zone in the crack initiation stage. As we discussed above, before macrocracks are formed, slip-band extrusions and slip-band intrusions occur and they gradually evolve into microcracks. The adhesion strength may be degraded by these slip-band extrusions and slip-band intrusions or microcracks.

3.4.1.2 Preferred Crack Initiation Location and Propagation Direction

From the C-SAM images, side view pictures and cross section pictures of the thermal cycling samples, we know that fatigue cracks in solder joints usually are initiated at a free surface, especially at the corners of the solder joints. Furthermore, from the C-SAM images of the interfaces between silicon chip and single bump barrel-shaped, stacked barrel-shaped, and stacked hourglass/column-shaped solder joints, it is evident that cracks in all the solder joint configurations at the silicon chip side are initiated at the outer end of the solder joints and propagate centripetally towards the neutral point, as shown in Figure 3.74 (a). Also, as we discussed before, cracks tend to appear in pairs at the diagonal corners of solder joints. This can be understood when we consider the mechanics of solder joint assembly during temperature cycling.

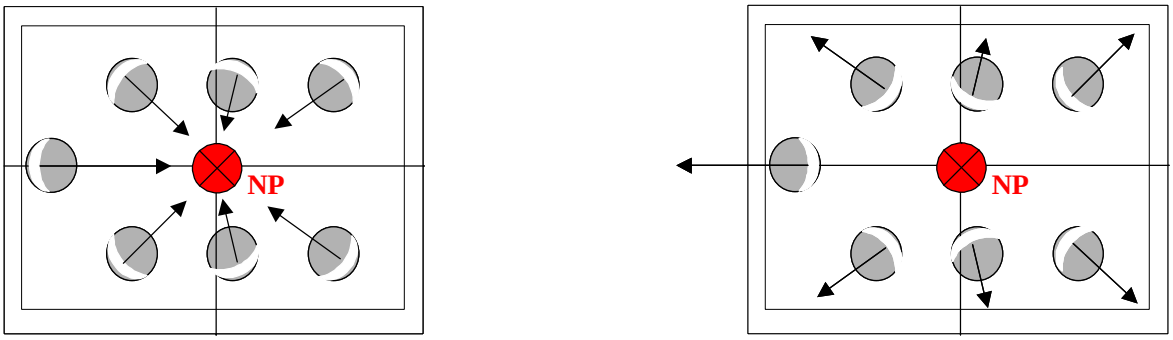
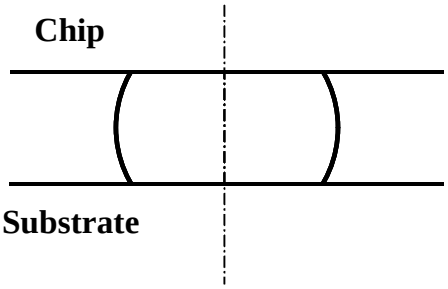


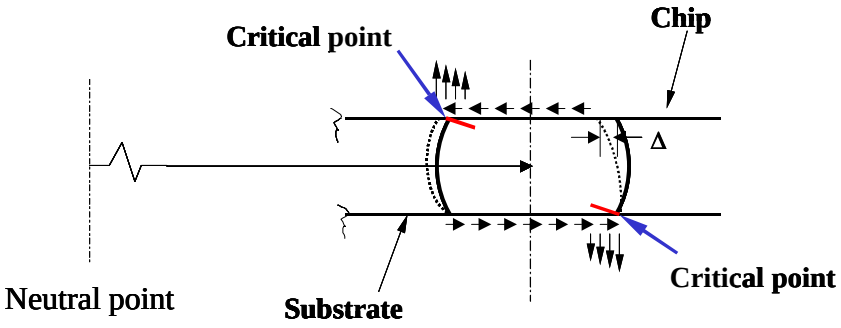
Figure 3.74. Illustration of preferred crack initiation location and propagation direction; (a) silicon chip side; (b) substrate side.

During temperature cycling, shear stresses and strains are developed in solder joints due to the CTE mismatch between silicon chip and substrate. The shear displacement gives rise to bending moments at the interface in order to maintain rotational equilibrium [31-32]. Therefore, there exist normal stresses in solder joint assembly. It is the combination of shear and normal stresses that cause solder joint fatigue and the resultant stresses are maximized at the interface regions. Figure 3.75 shows the schematic of solder joint assembly mechanics during temperature cycling. During the heating process, the substrate expand more than the silicon chip, thus there is shear forces in the right direction at the substrate side and in the left direction at the chip side, which in turn give rise to normal forces to realize rotational balance. Therefore, on heating, there are tensile stresses at the inner and outer ends of solder joint at the chip and substrate side respectively. Superimposed with the shear stress, these locations have the highest total stress and thus are the weakest locations on heating. On cooling, the reverse scenario applies, that is, the outer end of solder joint at the chip side and the inner end of the solder joint at the substrate side have the highest total stress and thus are the most vulnerable locations. Failure in solder joint thermal fatigue usually begins at one of these high-stress points. Figure 3.76 shows the preferred locations for crack initiation on heating and cooling in solder joints. However, the magnitudes of the shear displacement and tensile stress at the solder joint corners on heating and cooling are quite different. Due to the fact that solder relaxes slowly at low temperature when the thermal cycle proceeds into the cold region and increasing faster at high temperature during the heating process, the constraint to silicon chip expansion is much higher on cooling than that on heating [31]. As a result, there are higher shear displacement and lower tensile stress at the inner and outer corners of solder joint at the chip and substrate sides, respectively, on heating, while there

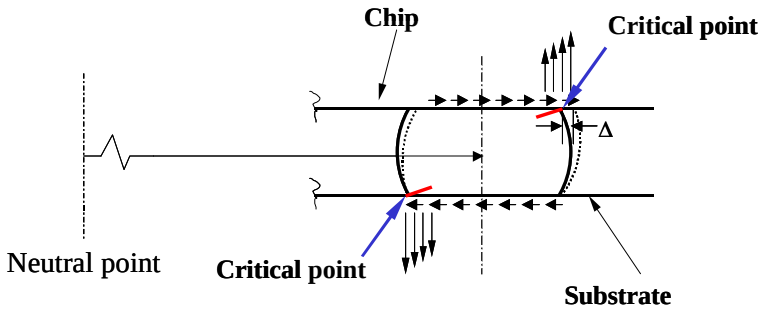
are lower shear displacement and greater tensile stress at the outer and inner corners of solder joint at the chip and substrate sides, respectively, on cooling. The higher stress during cooling process more likely induces cracks. We think this is the reason why cracks at the silicon chip side in all the solder joint configurations are dominantly initiated at the outer end of the solder joints and propagate centripetally towards the neutral point, as shown in Figure 3.74 (a). In turn, we can know that cracks at the substrate side are mainly initiated at the inner end of the solder joints and propagate centrifugally from the neutral point, as shown in Figure 3.74 (b). This also explains why cracks have the tendency to appear in pairs at the diagonal corners of solder joints. For the above discussion, we only considered global CTE mismatch. Actually, local CET mismatches between solder joint and silicon at the chip side and solder joint and substrate at the substrate side are also important. As we know, the CET mismatch between solder joint and substrate is smaller than that between solder joint and chip, thus there is higher stress at the solder joint and chip interface as a result of both global and local CTE mismatch. This can explain why there always are larger cracks at the chip side and smaller cracks at the substrate side and sometimes there are no cracks at all at the substrate interface.



(a)



(b)



(c)

Figure 3.75. Schematic of solder joint assembly mechanics during temperature cycling. (a) before temperature cycling; (b) during heating process; and (c) during cooling process.

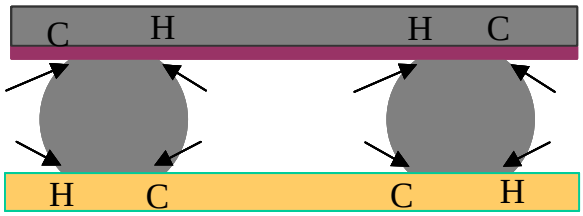
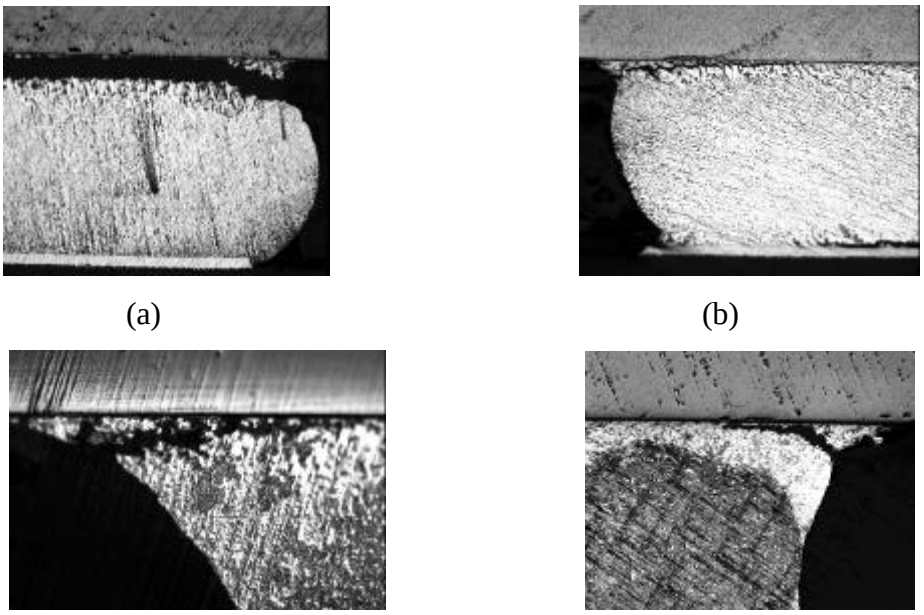


Figure 3.76. Preferred locations for crack initiation on heating and cooling in solder joints.

Once macrocracks are generated at the high stress locations, they will propagate and lead to failure. In general, the crack path is through the coarsened zone near or at the solder/chip and/or solder/substrate interfaces, as shown in Figure 3.77.



(a) (b)

(c) (d)

Figure 3.77. Typical crack paths in solder joint fatigue failure; (a) and (b) for single bump barrel-shaped solder joints and (c) and (d) for stacked hourglass-shaped solder joints.

3.4.2 Effects of Solder Joint Shape and Height on Thermal Fatigue

3.4.2.1 Comparison of the Temperature Cycling Results of the First Set of Samples

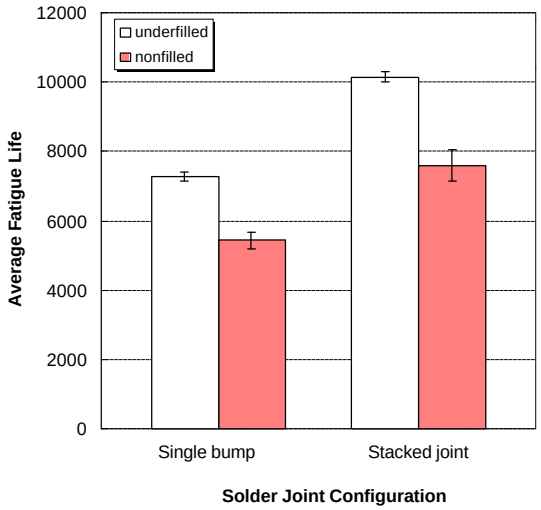


Figure 3.78. Average fatigue life of different solder joint configurations: single bump barrel-shaped solder joints with and without underfill; stacked hourglass/column-shaped solder joints with and without underfill.

Figure 3.78 summaries the average total fatigue life of single bump barrel-shaped solder joints with and without underfill, and stacked hourglass/column-shaped solder joints with and without underfill. As we can see, for the same solder joint structure, the fatigue life of underfilled case is longer than its non-underfilled counterpart. It is well recognized that underfill can improve solder joint reliability. For different solder joint structures, it is clear that stacked hourglass/column-shaped solder joint has longer fatigue life than single bump barrel-shaped solder joint, that is, stacked hourglass/column-shaped solder joint improved fatigue life time by about 40% over the conventional single bump barrel-shaped solder joint. We believe that this reliability improvement is due to both joint standoff height and shape. The other major difference between these two solder joint structures is the contribution of crack propagation life to the total fatigue life. Figure 3.79 shows the average crack initiation, crack propagation and catastrophic failure time of non-underfilled single bump barrel-shaped solder joints and stacked hourglass/column-shaped solder joints. As we can see from Figure 3.79, average crack propagation time of single barrel-shaped solder joints is about 30% of the average total fatigue lifetime and is about 48% of the average crack initiation time. On the other hand, the average crack propagation time of stacked hourglass/column-shaped non-underfilled solder joints is

about 40% of the average total fatigue lifetime and is about 78% of the average crack initiation time. In the other words, crack initiation time is improved by about 15% using stacked solder joint while crack propagation time is increased by about 90%. Thus, we can conclude that the fatigue life improvement of stacked hourglass/column-shaped solder joint over single bump barrel-shaped solder joint is mainly due to the prolonged crack propagation time.

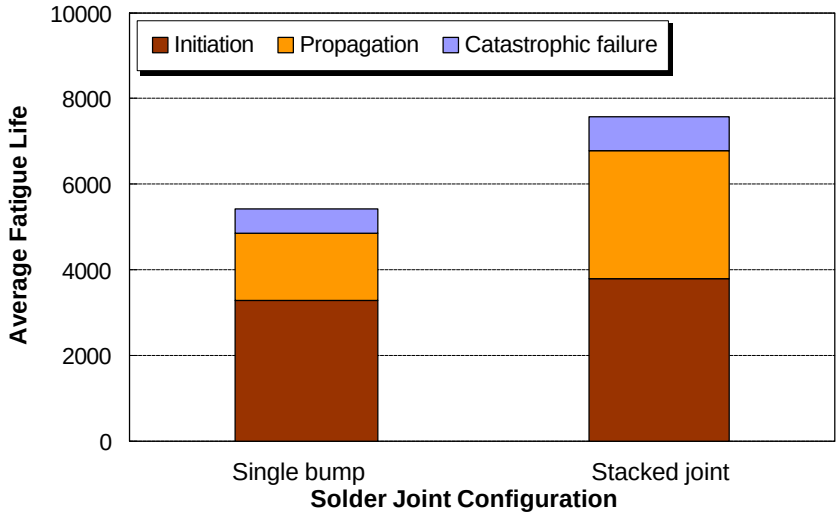


Figure 3.79. Average crack initiation, crack propagation and catastrophic failure time of non-underfilled single bump barrel-shaped solder joints and stacked hourglass/column-shaped solder joints.

Actually, we can see from the curves of electrical resistance change versus temperature cycling number in Figure 3.44 and Figure 3.52 that the slopes of electrical resistance increase in the crack propagation phases are quire different for non-underfilled single bump barrel-shaped solder joints and stacked hourglass/column-shaped solder joints. We used linear line to fit the curves of electrical resistance change versus temperature cycling number in the crack propagation phases. Figure 3.80 shows the electrical resistance increase slopes for a typical non-underfilled single bump barrel-shaped solder joint and stacked hourglass/column-shaped solder joint. We can see that the slope of this particular single bump barrel-shaped solder joint is over 6×10^{-5}, while that of the stacked hourglass-shaped solder joint example is lower than 2×10^{-5}. Figure 3.81 is a comparison of electrical resistance increase rate for the entire seven non-underfilled single bump barrel-shaped solder joints in the test chip and seven stacked hourglass/column-shaped solder joints in a test chip. The resistance increase slopes of the solder joints in a test chip are not completely uniform, but it is very obvious that the average of the slopes of single bump barrel-shaped solder joints is much higher than that of the slopes of

stacked hourglass/column-shaped solder joints, as shown in Figure 3.81. As we discussed before, electrical resistance increase is due to crack formation and growth in solder joints. The higher resistance increase rate of single bump barrel-shaped solder joints indicates that crack propagation rate of single bump barrel-shaped solder joints is faster than that of high standoff stacked hourglass-shaped solder joints. We attribute the crack propagation rate difference of single bump barrel-shaped solder joints and stacked hourglass-shaped solder joints to the geometry (standoff height and/or shape) difference between them. Please see discussion section of this chapter for further discussions.

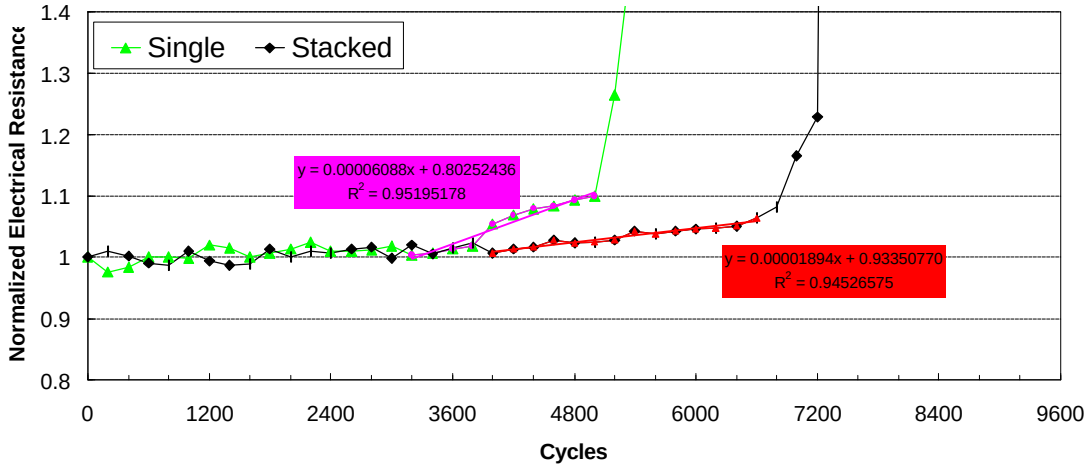


Figure 3.80. Electrical resistance increase slopes for a typical non-underfilled single bump barrel-shaped solder joint and stacked hourglass/column-shaped solder joint.

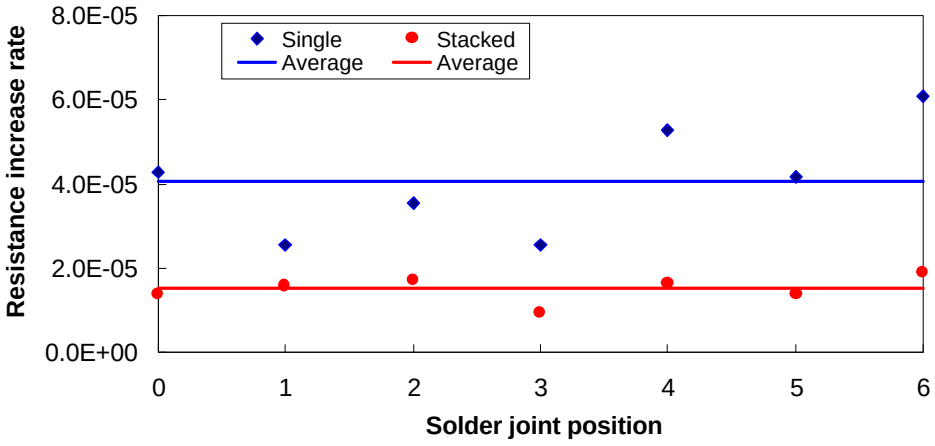


Figure 3.81. A comparison of electrical resistance increase rate for non-underfilled single bump barrel-shaped solder joints and stacked hourglass/column-shaped solder joints.

3.4.2.2 Comparison of the Temperature Cycling Results of the Second Set of Samples

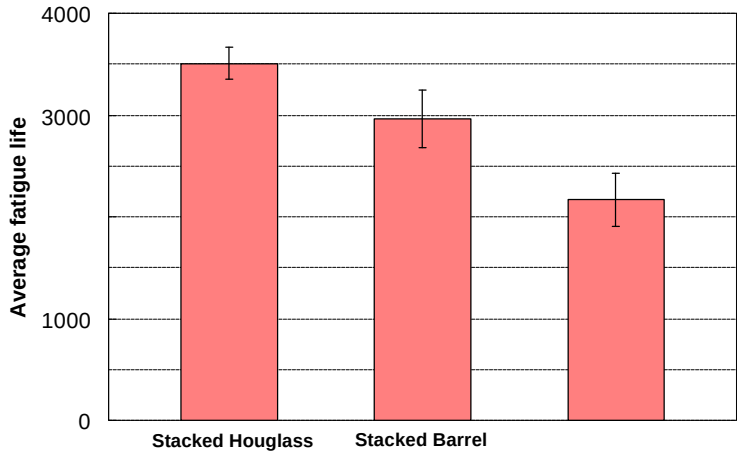


Figure 3.82. Average fatigue life of different solder joint configurations: stacked hourglass/column-shaped solder joints, stacked barrel-shaped solder joints, and single bump barrel-shaped solder joints.

Figure 3.82 summaries the average total fatigue life of stacked hourglass/column-shaped solder joints, stacked barrel-shaped solder joints, and single bump barrel-shaped solder joints. It is clear that stacked hourglass/column-shaped solder joints have the longest fatigue lifetime and single bump barrel-shaped solder joints have the shortest lifetime, the lifetime of stacked barrel-shaped solder joints being in between, but closer to that of stacked hourglass/column-shaped solder joints. Stacked hourglass/column-shaped solder joint improved fatigue lifetime by about 60% over the conventional single bump barrel-shaped solder joint. We believe that this reliability improvement is due to both joint standoff height and shape. Figure 3.83 shows the average crack initiation, crack propagation and catastrophic failure time of stacked hourglass/column-shaped solder joints, stacked barrel-shaped solder joints, and single bump barrel-shaped solder joints. The crack initiation and propagation times are quite different for these three solder joint configurations. As we can see from Figure 3.83, the average crack initiation times of stacked barrel-shaped solder joints and single barrel-shaped solder joints are almost the same, while the average initiation time of stacked hourglass/column-shaped solder joints is longer. On the other hand, the average crack propagation time of stacked barrel-shaped solder joints is at the same level as that of stacked hourglass/column-shaped solder joints, with the average crack propagation time of single bump barrel-shaped solder joints being the shortest. By using stacked hourglass/column-shaped solder joints, the crack initiation time is improved by

30-40% over barrel-shaped solder joints. By using stacked high standoff solder joints, the crack propagation time is increased by about 100%. Therefore, we may conclude that increasing standoff height of solder joint is a more effective way of improving solder joint fatigue reliability.

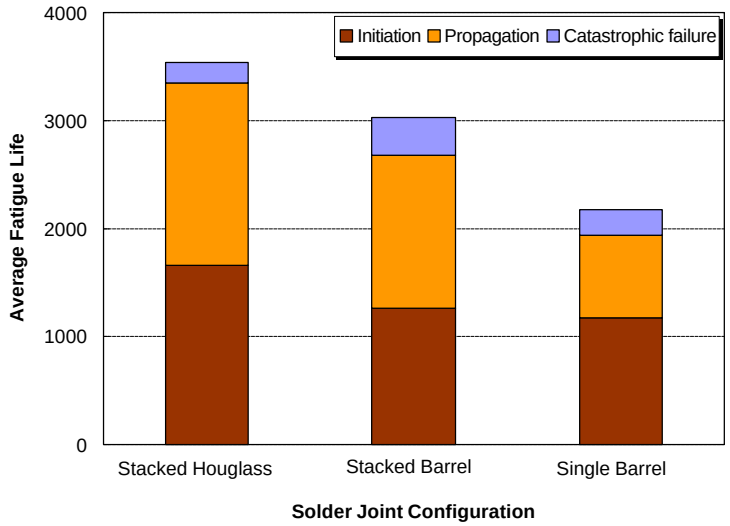


Figure 3.83. Average crack initiation, crack propagation and catastrophic failure time of stacked hourglass/column-shaped solder joints, stacked barrel-shaped solder joints, and single bump barrel-shaped solder joints.

From the curves of electrical resistance change versus temperature cycling number in Figure 3.60, Figure 3.64, and Figure 3.69, we can see that the slopes of electrical resistance increase in the crack propagation phases are quire different for single bump barrel-shaped, stacked hourglass/column-shaped and stacked barrel-shaped solder joints. Again, we used linear line to fit the curves of electrical resistance change versus temperature cycling number in the crack propagation phases. Figure 3.84 shows the electrical resistance increase slopes for a typical single bump barrel-shaped solder joint, stacked hourglass/column-shaped solder joint and stacked barrel-shaped solder joint. The slope of this particular single bump barrel-shaped solder joint is over 6×10^{-5}, while those of the stacked hourglass-shaped and stacked barrel-shaped solder joint examples are in the range of $3\text{-}4\times10^{-5}$. Figure 3.85 is a comparison of electrical resistance increase rate for the entire seven single bump barrel-shaped solder joints in a test chip, seven stacked hourglass/column-shaped solder joints in a test chip and seven stacked barrel-shaped solder joints in another test chip. It is obvious that the average of the slopes of single bump barrel-shaped solder joints is much higher than that of the average slopes of stacked hourglass/column-shaped and barrel-shaped solder joints, as shown in Figure 3.85. As we

showed before, solder joint crack areas at different temperature cycles were calculated. Figure 3.86 is the average crack area increase rate during temperature cycling for single bump barrel-shaped solder joints and stacked hourglass/column-shaped solder joints. It is evident that crack area in single bump barrel-shaped solder joints increases much faster than that in stacked hourglass/column-shaped solder joints. This is in agreement with the higher resistance increase rate of single bump barrel-shaped solder joints than high standoff stacked hourglass-shaped solder joints.

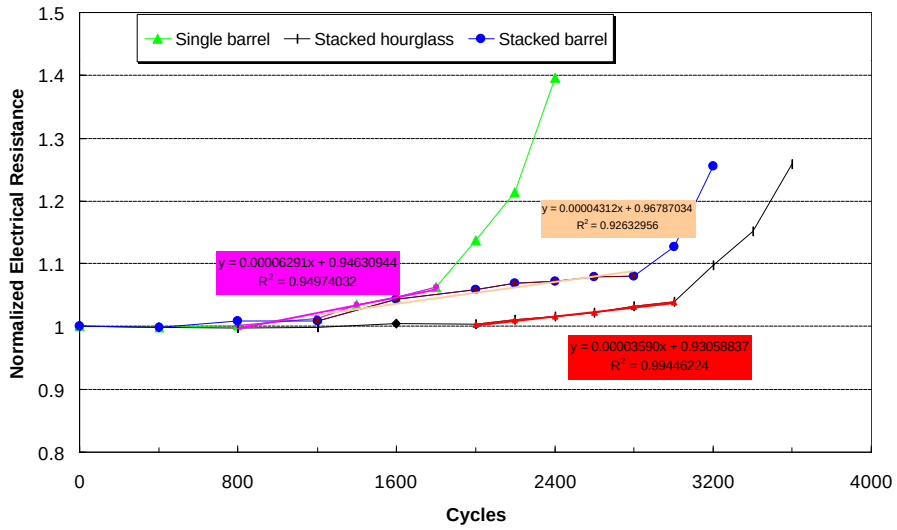


Figure 3.84. Electrical resistance increase slope for a typical stacked hourglass/column-shaped solder joint, stacked barrel-shaped solder joint, and single bump barrel-shaped solder joint.

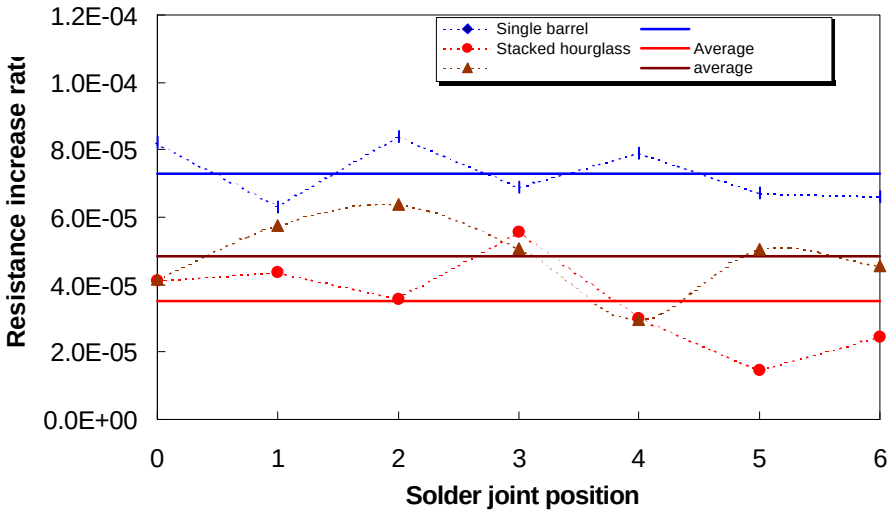


Figure 3.85. A comparison of electrical resistance increase rate for single bump barrel-shaped solder joints, stacked hourglass/column-shaped solder joints and stacked barrel-shaped solder joints.

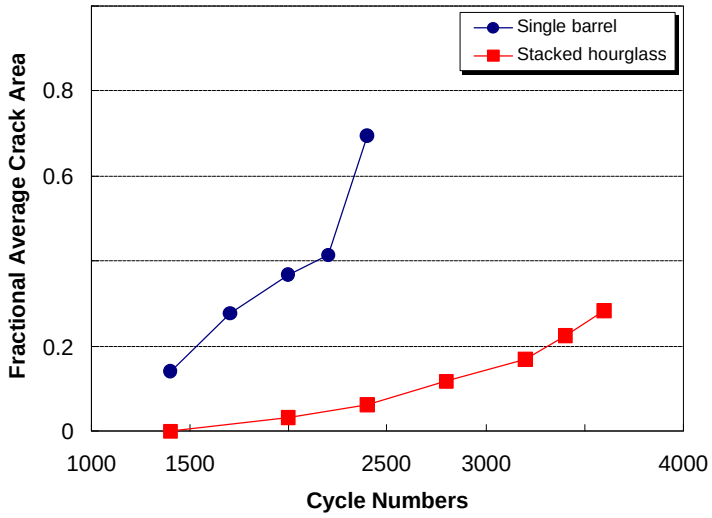


Figure 3.86. Average crack area increase rate during temperature cycling for single bump barrel-shaped solder joints and stacked hourglass/column-shaped solder joints.

3.4.2.3 Analysis of Shape and Standoff Height Effects

Mathematical calculations and finite element modeling have shown that the hourglass-shaped solder joints would have the lowest plastic strain during a temperature cycle, thus the longest lifetime [33-38]. However, these studies did not separate the effects of shape and height on solder joint reliability. Majority of these studies always keep solder volume constant and then analyze the stress and strain distribution in different solder joint configurations and use some fatigue models to predict the lifetimes of the solder joint configurations. As can be obviously seen, for the same solder volume and same pad size, hourglass-shaped solder joint would have the greatest standoff height, column-shaped is next and barrel-shaped solder joint has the lowest height. Apparently solder joint standoff height also affect fatigue lifetime. Therefore, it is not clear in literature whether solder joint shape is the dominant factor or standoff height is more effective in improving solder joint reliability in the hourglass-shaped solder joints.

Our temperature cycling tests on single bump barrel-shaped solder joints and stacked hourglass-shaped solder joints verified that high standoff hourglass-shaped solder joints have improved fatigue lifetime. For the first set of samples, the average total fatigue life is improved about 40% by using high standoff hourglass-shaped solder joint. The fatigue lifetime is gained mostly by prolonging the crack propagation time. Specifically, the average crack initiation time of high standoff hourglass-shaped is improved by only about 15% over low standoff barrel-

shaped solder joints, while the crack propagation time is increased by about 90%. We believe the overall fatigue lifetime improvement is mainly due to the geometry of stacked hourglass-shaped solder joint. However, both the shape and height of the two solder joint configurations are different, thus it is difficult to distinguish the effects of shape and height on fatigue. Table 3.3 is a summary of the average contact angle, height, midpoint diameter and shape factor of the first set single bump barrel-shaped and stacked hourglass-shaped solder joints. The contact angles, heights, midpoint diameters were measured by using National Instruments IMAQ Version Builder software. The shape factor is defined as: R (ratio)=(the diameter of the midpoint of the solder joint)/(pad diameter).

Table 3.3. Geometry of the first set of temperature cycling samples.

	Contact angle (degree)	Height (mm)	Midpoint diameter (mm)	Shape Factor
Stacked Hourglass	66	1.06	0.91	0.83
Single Barrel	121	0.58	1.27	1.16

For the second set of temperature cycling samples, stacked hourglass/column-shaped solder joint improved average total fatigue lifetime by about 60% over the conventional single bump barrel-shaped solder joint. Again, the prolonged crack propagation time is the major contribution to the total fatigue lifetime improvement. Interestingly, the total fatigue lifetime of stacked barrel-shaped solder joints is only slightly lower than that of stacked hourglass/column-shaped solder joints. From Figure 3.83, we can see that the average crack propagation time of stacked barrel-shaped solder joints is at the same level as that of stacked hourglass/column-shaped solder joints. However, the crack initiation time is lower than that of stacked hourglass/column-shaped solder joints. The difference between the total fatigue lifetimes of the stacked barrel-shaped solder joint and stacked hourglass/column-shaped solder joint is mainly due to the difference between the crack initiation times of these two solder joint configurations. On the other hand, from the solder joint structure of view, the major difference between these two solder joint configurations is the shape (contact angle and shape factor) with the triple-stacked solder layers being the same. Table 3.4 is the average geometry data of each solder joint configuration for the second set of temperature cycling test samples. The height of the stacked barrel-shaped solder joint and stacked hourglass/column-shaped solder joint is almost the same.

In contrast, the shape of single bump barrel-shaped and stacked barrel-shaped solder joints are similar and they have almost the same average initiation time. We know that the total fatigue lifetime as well as the time for each fatigue damage processes are primarily determined by the solder joint geometry, material and test conditions. Therefore, we can conclude that solder joint shape is the dominant factor in determining crack initiation time.

As shown in Figure 3.82, the total fatigue lifetime of stacked barrel-shaped solder joints is 40% higher than that of conventional single bump barrel-shaped solder joints though the stacked barrel-shaped solder joints have much smaller pad size. The crack propagation time of stacked barrel-shaped solder joint is much longer than that of single bump barrel-shaped solder joint and the average crack initiation times of both of the configurations are the same. The difference between the total fatigue lifetimes of the stacked barrel-shaped solder joint and single bump barrel-shaped solder joint is contributed from the difference of their crack propagation times. From Table 3.4, we can see that the two barrel-shaped solder joint structures have similar shape, but very different standoff heights. On the other hand, as we discussed above, stacked barrel-shaped solder joint and stacked hourglass/column-shaped solder joint have the same standoff height and their average propagation time are almost the same. Thus, we may attribute the origin of the difference of solder joint crack propagation time to the difference of standoff height. However, note that the stacked barrel-shaped solder joint is composed of three solder layers with the middle ball being high-lead solder material, while the single bump barrel-shaped solder joint is made up of only eutectic solder material. The middle high-lead solder ball has different properties from eutectic solder and it may also have effect on crack propagation time though fatigue failure normally occurs at the eutectic solder layer and chip/substrate interface.

Table 3.4. Geometry of the second set of temperature cycling samples.

	Contact angle (degree)	Height (mm)	Midpoint diameter (mm)	Shape Factor
Stacked Hourglass	62	1.02	0.93	0.85
Stacked Barrel	124	1.07	1.08	1.54
Single Barrel	120	0.64	1.26	1.15

It is commonly known that, for fatigue failure, slip-band and/or microcracks occur at one or more points that have high localized stress and then gradually spread by fracture of the

material at the edges of the cracks where the stress is highly concentrated. The movements of slip and growth of mocrocracks are related to local stress and cyclic strain. Therefore, the time needed for microcracks grow into macrocracks might be affected by local stress and strain. This may explain why solder joint shape is the dominant factor in determining crack initiation time. Generally, solder joint fatigue failure occurs first at the interfaces between solder joint and silicon chip, and solder bump and substrate due to the high thermal stress concentration at these adhering interfaces, especially at the corners [36, 38-39]. Finite element modeling showed that hourglass-shaped solder joint have much lower stress at the solder joint corners [36, 38, 40]. Analytically, it is well accepted that the stress and strain field near bi-material bonding or contact edges show singular behavior, which can induce a considerably larger stress than the nominal stress. It has been shown that the singularity increases and becomes more significant with the increasing of the contact angle [41-42]. The smaller contact angle of the hourglass-shaped solder joint structure reduces the order of the singularity. Our tensile and shear tests experimentally proved that hourglass-shaped solder joint has high adhesion stress than barrel-shaped solder joint. In summary, smaller contact angle and thus less singularity might be one reason that hourglass-shaped solder joint has longer crack initiation time.

Another reason that hourglass-shaped solder joint improve crack initiation time could be that the slender shape change the stress distribute and thus there is lower stress concentration at the solder joint corners. The waisted configuration of the hourglass-shaped solder joint is more compliant and flexible, so stresses imposed at the interfaces between solder bump and silicon chip, and solder bump and substrate are less than those for barrel-shaped solder joints. The hourglass shape may be effective in avoiding the strain localization characteristic of the bulged solder joint, and consequently affect failure mode development. In the hourglass solder joint, the reduced cross section is at the middle between the PCB and the chip; therefore, a portion of deformation takes place in the ductile middle section of the solder joint, and this deformation is away from the brittle interface of the solder joint to the chip and the board. In contrast, the barrel joint has the reduced cross section at the interface of the solder joint to the chip and board, where the mechanical properties are normally poor. Our tensile and shear tests did show that hourglass-shaped solder joint fracture at or close to mid neck point while barrel-shaped solder joint always fail at the interfaces. Temperature cycling test also showed that some hourglass-shaped solder joints failed inside the solder joint structure, as shown in Figure 3.55 and Figure 3.56.

We concluded from our experimental results that solder joint crack propagation time is mainly determined by solder joint standoff height. This probably can be explained by the laws that governing the fatigue crack propagation for stage II growth of a metal. One of the laws for crack propagation for stage II growth can be expressed in terms of total strain by a single power-law expression which extends from elastic to plastic strain region [28]:

$$\frac{da}{dN} = Ce^{m} \qquad \text{Equation 7}$$

The effective strain in solder joint can be expressed as effective strain=$\frac{b\Delta a\Delta Ta}{h}$ [30]. Where b is effective factor, $\Delta\alpha$ is the difference in the coefficients of thermal expansion between the joined materials, ΔT is the temperature change, *a* is the distance from the neutral expansion point of the joined materials, and h is the height of the solder joint. High solder joint standoff will have lower effective strain with the other parameter being the same. In turn, lower effective strain gives slower crack propagation rate according to equation 5. Stacked solder joints have improved standoff height, thus they have prolonged crack propagation time and overall fatigue lifetime.

A tall compliant solder joint has enhanced mismatch absorption capability. A high standoff solder joint can be distorted in temperature cycling, as shown in Figure 3.87, and thus release the thermal stress built in the solder joint. Furthermore, tall solder joint also changes the stress and strain distribution in solder joint and protect the weak interfaces of solder joint to chip and substrate [43-45]. IBM's ceramic column grid array was reported to have fatigue cracks through high-lead column region as shown in Figure 3.88 [43-45].

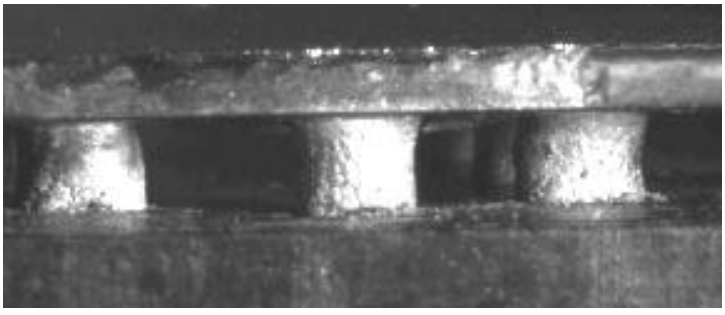


Figure 3.87. High standoff solder joint distortion in temperature cycling.

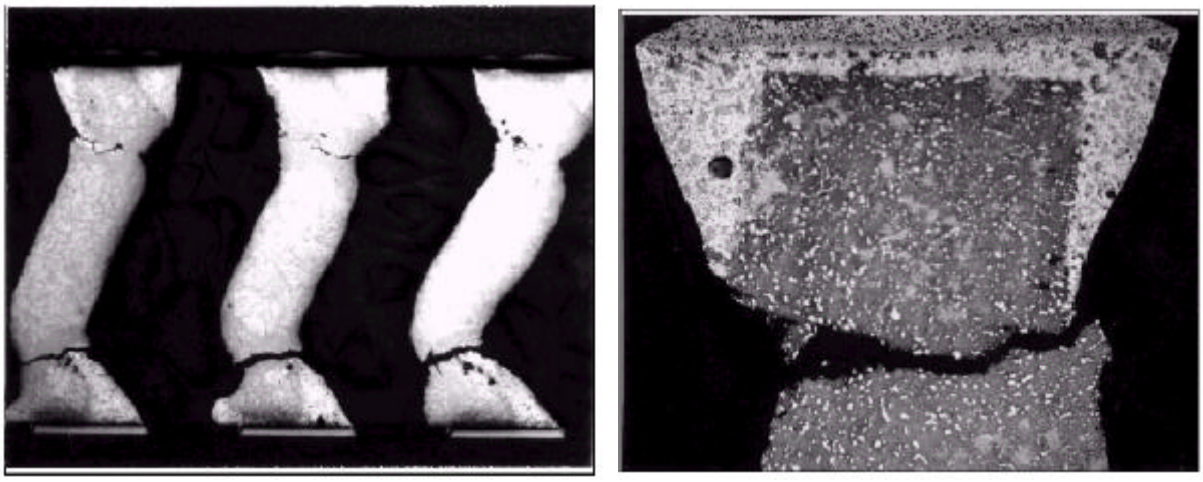
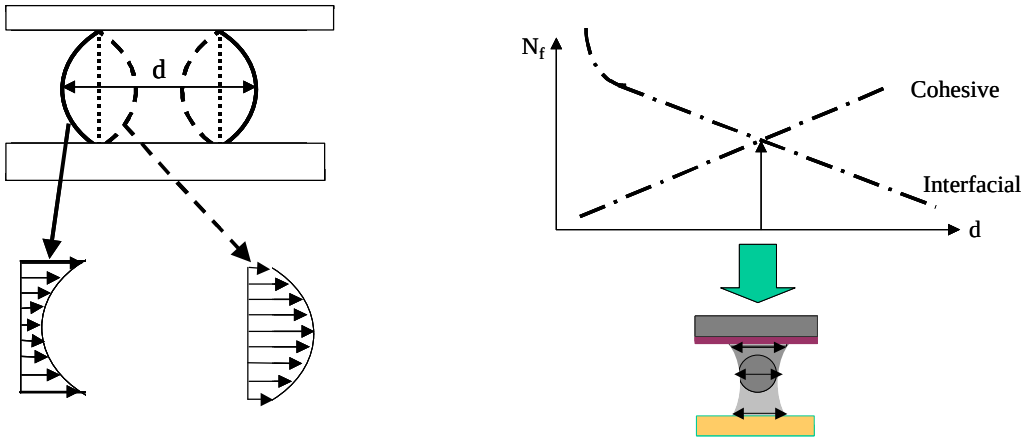


Figure 3.88. Fatigue failed ceramic column grid array [45].

From the above discussion, we know that increasing solder joint standoff height is a more effective way of improving solder joint reliability though solder joint shape is also important. Therefore, for solder joint reliability optimization, the most important thing is to increase solder joint standoff height to the maximum that the solder joint fabrication process allows. However, it is very difficult to increase solder joint height without significantly suffering solder joint pitch, I/O density and cost. Normally, large joint-to-joint separation is required to obtain reliable joint heights. After solder joint height is maximized, the next step of reliability optimization is control solder joint shape. As we discusses before, solder joint shape changes stress distribution in solder joint. Figure 3.89 (a) shows the schematic stress distribution in barrel and hourglass-shaped solder joints. For barrel shape, stresses are very high at the interfaces, especially at the corners due to high singularity, while the midpoint stress is very low. Thus interfacial failure is the dominant failure mode for barrel-shaped solder joint. On the contrary, stresses at the mid neck point are significantly higher than those at interfaces if the shape ratio (midpoint diameter/pad size) is very small, and as a result, cohesive failure could be the dominant failure mode. As shown in Figure 3.89 (b), we probably can find the right d (or shape ratio) that maximize the solder joint fatigue lifetime at this d or shape ratio, fatigue failure would randomly distributed among the interfaces and mid neck point.



(a) (b)

Figure 3.89. Solder joint reliability optimization by controlling solder joint shape with the same height and pad size; (a) schematic stress distribution in different solder joint shapes; (b) reliability optimization through interfacial and cohesive failure.

3.5 Summary and Conclusions

A precise analysis and prediction of solder joint thermal fatigue in flip chip assembly is immensely difficult. A lot of factors affect solder joint fatigue behavior. The following are the major factors but not the least:

1. Extend of thermal expansion coefficient mismatch;
2. Temperature gradient in an assembly;
3. Temperature range;
4. Heating and cooling rate;
5. Upper temperature;
6. Dwell tempetature at upper temperature;
7. Geometry of the solder joint;
8. Degree of compliancy of the assembly;

The adhesion strength of as-processed and thermal cycled barrel-shaped and stacked hourglass-shaped solder joints was tested using both tensile and shear tests. Test results showed that stacked hourglass-shaped solder joint has much high adhesion strength than barrel-shaped solder joint. This is explained as hourglass-shaped solder joint has less singularity than barrel-shaped one since it has smaller contact angle. The tensile and shear loads of barrel-shaped solder joints during temperature cycling reduce faster than those of hourglass-shaped ones. This

indicates that barrel-shaped solder joints degrade earlier and faster and thus have lower fatigue lifetime.

The reliabilities of fabricated solder joints including low standoff barrel-shaped solder joints and high standoff stacked solder joints with barrel and hourglass/column shapes were evaluated by accelerated temperature cycling tests. Test results clearly show that high standoff hourglass-shaped solder joint has the highest fatigue lifetime, with high standoff barrel-shaped solder joint in between and low standoff barrel-shaped solder joint has the shortest fatigue lifetime. Solder joint fatigue damage process can be divided into three phases corresponding to crack initiation, crack propagation and catastrophic failure. C-SAM images, side view pictures and cross section pictures of the thermal cycling samples showed that fatigue cracks in solder joints usually are initiated at a free surface, especially at the corners of the solder joints during the cooling process. Electrical resistance measurement and scanning acoustic microscopy imaging showed that cracks appeared in barrel-shaped solder joints earlier than in hourglass-shaped solder joint, and furthermore, these results showed that cracks propagate faster in the low standoff solder joint than in the high standoff solder joints. We attributed solder joint shape to be the dominant factor affecting crack initiation time and solder joint height to be major factor in determining crack propagation time. Experimental results showed that about 30% of the total fatigue lifetime improvement of high standoff hourglass-shaped solder joint over low standoff barrel-shaped solder joint contributed from crack initiation time, while about 65% gained from crack propagation.

From our experimental results on reliability assessment of low standoff barrel-shaped solder joints and high standoff stacked solder joints with barrel and hourglass/column shapes, we may draw the following conclusions:

- Solder joint fatigue damage process consists of crack initiation, crack propagation and catastrophic failure. Each of these stages needs to be considered in order to fully study the solder joint fatigue behavior and accurately predict fatigue lifetime;
- Solder joints are mainly damaged in the cooling process of a temperature cycle;
- High standoff hourglass-shaped solder joint has improved thermal fatigue lifetime;

- High standoff hourglass-shaped solder joint could shift the fatigue failure location;
- Solder joint shape and height are the dominant factors affecting crack initiation and propagation time, respectively;
- Increasing solder joint height is a more effective way of improving solder joint reliability.

3.6 References

[1] Pasquale Sullo, "Basic Concepts of Reliability," CPES Reliability Tutorial, CPES Annual Seminar, September 19, 1999.

[2] L. F. Coffin, Jr., "A Study of the Effects of Cyclic Thermal Stresses on a Ductile Metal", ASME Transactions, Vol. 76, pp. 931-950, 1954.

[3] S. S. Manson, "Fatigue: A Complex Subject – Some SPL Approximations", Experimental Mechanics, Vol. 5, pp. 193- 226, 1965.

[4] H. D. Solomon, "Life Prediction and Accelerated Testing", The Mechanics of Solder Alloy Interconnects, S. N. Burchett et al. Editors, Van Nostrand Reinhold, pp. 199-313, 1993.

[5] H. D. Solomon, "Fatigue of 60/40 Solder," IEEE Transactions on Components, Hybrids, and Manufactory Technology, CHMT-9: 423-432, December, 1986.

[6] K. C. Norris and A. H. Landzberg, "Reliability of Controlled Collapse Interconnections," IBM J. Research Devel., Vol. 13, No. 3, 266-271, May 1969.

[7] Rao R. Tummala, Eugene J. Rymaszewski and Alan G. Klopfenstein, Microelectronics Packaging Handbook, Chapman & Hall, 1996.

[8] Knetch S., Fox L., "Integrated matrix creep: application to accelerated testing and lifetime prediction." In: Lau JH, editor, Solder Joint Reliability Theory and Applications, New York: Van Nostrand Reinhold, 1991 (Chapter 16).

[9] Syed AR, "Thermal fatigue reliability enhancement of plastic ball grid array (PBGA) packages," ECTC, pp. 1211-1216, 1996.

[10] Syed AR, Panczak T, Darveaux R, Lee S, Lee C, and Partridgr J, "Solder joint reliability of chip array BGA," Pan Pacific Microelectronics Symposium, Maui, 1998.

[11] H. D. Solomon, “Life Prediction and Accelerated Testing”, The Mechanics of Solder Alloy Interconnects, S. N. Burchett et al. Editors, Van Nostrand Reinhold, pp. 199-313, 1993.

[12] W. Engelmaier, “Surface Mount Solder Joint Long-term Reliability: Design, Testing, and Prediction”, Soldering and Surface Mount Technology, Vol. 1, pp. 12-22, 1989.

[13] A. Dasgupta, C. Oyan, D. Barker, and M. Pecht, “Solder Creep-Fatigue Analysis by an Energy-Partitioning Approach”, ASME Transactions, Journal of Electronic Packaging, Vol. 114, pp. 152-160, 1992.

[14] A. S. Tetelman and A. J. McEvily, “The Mechanics of Fracture,” Fracture of Structure Materials, Wiley, New York, 1967.

[15] Y. H. Pao, “A Fracture Mechanics Approach to Thermal Fatigue Life Prediction of Solder Joints”, IEEE Transactions on Components, Hybrids, and Manufacturing Technology, CHMT, Vol.15, pp.559-570, 1992.

[16] Paris, P. C., and F. Erdogan, “A critical Analysis of Crack Propagation Laws,” Trans. ASME, Journal of Basic Engineering, 85, pp. 528-534, 1963.

[17] Semiconductor Data Book, IXYS Corporation, Santa Clara, CA, 1998.

[18] Shatil Haque, “Processing and Characterization of Device Solder Interconnection and Module Attachment for Power Electronics Modules,” Virginia Tech, Blacksburg, Dec. 1999.

[19] C. Federman, Sonix Publications, Sonix Inc., 1998.

[20] J.E. Semmens, S.R. Martell and L.W. Kessler, “Evaluation of Flip Chip Interconnects Using Acoustic Microscopy for Failure Analysis and Process Control Applications”, Proceedings of the 4th International Conference on Multichip Modules, 1995.

[21] L.W. Kessler, “Acoustic Microscopy”, Nondestructive Evaluation and Quality Control: Metals Handbook, Vol. 17, 9th Edition, ASM International, 1989, pp. 465-482.

[22] T.E. Adams, “Acoustic Micro-Imaging of Multichip Modules”, Surface Mount Technology, Lake Publishing, June 1991.

[23] John Goings, “Live and Acoustic”, The European Test Industry Journal: Test Technology – Inspection Methods, Vol. XXV, No. 4, May 1999, pp. 22-23.

[24] C. Diaz de Leon, M. Nassirian, C. Todd and R. Chowdhury, “Failure Analysis of Flip-Chip Interconnections through Acoustic Microscopy”, Proceedings of the 22nd International Symposium for Testing and Failure Analysis, Los Angeles, CA, November 18-22, 1996.

[25] J. Sigmund and M. Kearney, “Tomographic Acoustic Micro Imaging (TAMI) Improves Acoustical Analysis of Flip Chip Packages”, Sonix Incorporated, Springfield, VA.

[26] Joel Sigmund and Michael Kearney, “TAMI Analysis on Flip Chip Packages”, Advanced Packaging, July/August 1998.

[27] Tomographic Acoustic Micro-Imaging, Application Note, Sonix Incorporated, 1998.

[28] George E. Dieter, “Mechanical Metallurgy,” McGraw-Hill, New York, 1976.

[29] Z. Qian, W. Ren and S. Liu, “A Damage Coupling Framework of Unified Viscoplasticity for the Fatigue of Solder Alloys,” ASME Transactions, Journal of Electronic Packaging, Vol.121, September 1999.

[30] Jennie S. Hwang, “Modern Solder Technology for Competitive Electronics Manufacturing,” McGraw-Hill, 1996.

[31] Rao R. Tummala, Eugene J. Rymaszewski and Alan G. Klopfenstein, Microelectronics Packaging Handbook, Chapman & Hall, 1996.

[32] L. S. Goldman, “Geometric Optimization of Controlled Collapse Interconnections,” IBM J. Research Devel., 251-269, May 1969.

[33] Satoh R, Ohshima M, Komura H, Ishi I, and Serizawa K, “Development of a New Micro-solder Bonding Method for VLSIs,” Proc. 1983 IEPS, pp. 455-461.

[34] Satoh R, Arakawa K, Harada M, Matsui K, " Thermal fatigue life of Pb-Sn alloy interconnections," IEEE Transactions Components, Hybrids, and Manufacturing Technology, 1991;Vol. 14: 224 -232.

[35] Goldman LS, “Geometric Optimization of Controlled Collapse Interconnections,” IBM J. Research Devel., 1969; 251-269.

[36] Ho TH, Lee JY, Lee RS, and Lin AW, “Linear Finite Stress Simulation of Solder Joints on 225 I/O Plastic BGA Packages Under Thermal Cycling,” ECTC, pp. 930, 1995.

[37] Kitano M and Honda M, "Shape Prediction of Solder Bump Joint by Surface Tension Analysis and Fatigue Strength Evaluation," ASME Advances in Electronic Packaging 1997, EEP-Vol. 19-2, 1407-1413.

[38] Yu Q, Shiratori M, and Ohshima Y, " A study of the effects of BGA solder geometry on fatigue life and reliability assessment," Proceedings of Thermal and Thermomechanical Phenomena in Electronic Systems, 1998. ITHERM'98. Pp. 229 -235.

[39] Lau JH, Flip Chip Technologies, McGraw Hill, 1995.

[40] Bingzhi Su, Saeed Hareb, and Y. C. Lee, “Solder joint reliability modeling for a 540-I/O plastic Ball-Grid-Array Assembly,” International conference on multichip modules and high density packaging, pp.422-428, 1998.

[41] Body DB, "Two Edge-Bonded Elastic Wedges of Different Materials and Wedges Angles under Surface Tractions", Journal of Applied Mechanics, pp 526-528, Dec., 1952.

[42] Willams ML and Pasadena C, "Stress Sigularities Resulting From Various Boundary Conditions in Angular Corners of Plates in Extension", Journal of Applied Mechanics, pp 377-386, June, 1971.

[43] Hong BZ; Ray SK, " Ceramic column grid array technology with coated solder columns," Proceedings of the IEEE 50th Electronic Components & Technology Conference, pp.1347 - 1353, 2000.

[44] Master RN, Cole MS, Martin GB, Caron A, " Ceramic column grid array for flip chip applications," Proceedings of the IEEE 45th Electronic Components and Technology Conference, pp. 925 -929, 1995.

[45] S. K. Ray, M. Interrante, L. Achard, M.S. Cole, I. DeSousa, L. Jimarez, G. Martin, and C. Reynolds, “CLASP Ceramic Column Grid Array Technology for Flip Chip Carriers,” Advanced Packaging Technology Tutorial, Proceedings of SEMICON West, July 13-14, 1999.