# Form-Factor-Constrained, High Power Density, Extreme Efficiency and Modular Power Converters

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## ABSTRACT

Enhancing performance of power electronics converters has always been an interesting topic in the power electronics community. Over the years, researchers and engineers are developing new high performance component, novel converter topologies, smart control methods and optimal design procedures to improve the efficiency, power density, reliability and reducing the cost. Besides pursuing high performance, researchers and engineers are striving to modularize the power electronics converters, which provides redundancy, flexibility and standardization to the end users. The trend of modularization has been seen in photovoltaic inverters, telecommunication power supplies, and recently, HVDC applications.

A systematic optimal design approach for modular power converters is developed in this dissertation. The converters are developed for aerospace applications where there are stringent requirement on converter form factor, loss dissipation, thermal management and electromagnetic interference (EMI) performance. This work proposed an optimal design approach to maximize the nominal power of the power converters considering all the constraints, which fully reveals the power processing potential. Specifically, this work studied three-phase active front-end converter, three-phase isolated ac/dc converter and inverter. The key models (with special attention paid to semiconductor switching loss model), detailed design procedures and key design considerations are elaborated. With the proposed design framework, influence of key design variables, e.g. converter topology, switching frequency, etc. is thoroughly studied.

Besides optimal design procedure, control issues in paralleling modular converters are discussed. A master-slave control architecture is used. The slave controllers not only follow the command broadcasted by the master controller, but also synchronize the high frequency clock to the master controller. The control architecture eliminates the communication between the slave controllers but keeps paralleled modules well synchronized, enabling a fully modularized design.

Furthermore, the implementation issues of modularity are discussed. Although modularizing converters under form factor constraints adds flexibility to the system, it limits the design space by forbidding oversized components. This work studies the influence of the form factor by exploring the maximal nominal power of a double-sized converter module and comparing it with that of two paralleled modules. The tradeoff between modularity and performance is revealed by this study. Another implementation issue is related to EMI. Scaling up system capacity by paralleling converter modules induces EMI issues in both signal level and system level. This work investigates the mechanisms and provides solutions to the EMI problems.

# Form-Factor-Constrained, High Power Density, Extreme Efficiency and Modular Power Converters

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## GENERAL AUDIENCE ABSTRACT

As penetration of power electronics technologies in electric power delivery keeps increasing, performance of power electronics converters becomes a key factor in energy delivery efficacy and sustainability. Enhancing performance of power electronics converters reduces footprint, energy waste and delivery cost, and ultimately, promoting a sustainable energy use. Over the years, researchers and engineers are developing new technologies, including high performance component, novel converter topologies, smart control methods and optimal design procedures to improve the efficiency, power density, reliability and reducing the cost of power electronics converters. Besides pursuing high performance, researchers and engineers are striving to modularize the power electronics converters, enabling power electronics converters to be used in a "plug-and-play" fashion. Modularization provides redundancy, flexibility and standardization to the end users. The trend of modularization has been seen in applications that process electric power from several Watts to Megawatts. This dissertation discusses the design framework for incorporating modularization into existing converter design procedure, synergically achieving performance optimization and modularity.

A systematic optimal design approach for modular power converters is developed in this dissertation. The converters are developed for aerospace applications where there is stringent

requirement on converter dimensions, loss dissipation, and thermal management. Besides, to ensure stable operation of the onboard power system, filters comprising of inductors and capacitors are necessary to reduce the electromagnetic interference (EMI). Owning to the considerable weight and size of the inductors and capacitors, filter design is one of the key component in converter design. This work proposed an optimal design approach that synergically optimizes performance and promotes modularity while complying with the entire aerospace requirement. Specifically, this work studied three-phase active front-end converter, three-phase isolated ac/dc converter and three-phase inverter. The key models, detailed design procedures and key design considerations are elaborated. Experimental results validate the design framework and key models, and demonstrates cutting-edge converter performance.

To enable a fully modularized design, control of modular converters, with focus on synchronizing the modular converters, is discussed. This work proposed a communication structure that minimizes communication resources and achieves seamless synchronization among multiple modular converters that operate in parallel. The communication scheme is demonstrated by experiments.

Besides, the implementation issues of modularity are discussed. Although modularizing converters under form factor constraints adds flexibility to the system, it limits the design space by forbidding oversized components. This work studies the impact of modularity by comparing performance of a double-sized converter module with two paralleled modules. The tradeoff between modularity and performance is revealed by this study.

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Their experience in power electronics product development provides solid foundation for the complete of this work.

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# Chapter 1. Introduction

Since its introduction in 1950s, power electronics has been one of the key enablers in industry. As the world is seeking a more sustainable future, power electronics represents the key technology in tackling the emerging challenges, e.g. renewable electricity, zero-emission vehicle and transportation electrification. This work focuses on power electronics converters in more-electric aircrafts (MEA), where electrical components replaces onboard mechanical, pneumatic and hydraulic systems to reduce take-off weight. The MEA demands high reliability, high availability, high power density and high efficiency. This works discusses the underlying technologies that enables the high performance power converter, the design framework that systematically explores the optimal design, and demonstrates the prototypes that satisfies the MEA demand.

This chapter presents the application background, followed by literature review on design framework and modularity of power electronics converters.

## 1.1 Application: More-Electric Aircrafts

For decades, the aerospace industry has been striving to reduce the cost and environmental impact of aircrafts. Reducing take-off weight is one of the major approaches of reducing fuel use and emissions. The concept of more-electric aircraft (MEA) is proposed in this context. The MEA uses electrical components to replace onboard mechanical, hydraulic and pneumatic systems to decrease take-off weight. This concept is depicted by Fig. 1-1 [1], where the electrical system consumes the most non-propulsive power in a MEA while the pneumatic and hydraulic systems

consume the most in a conventional aircraft. A study conducted by NASA expects a 10% reduction in the take-off weight and a 9% reduction in fuel burn for a 200-seater aircraft by switching to MEA technologies [2].

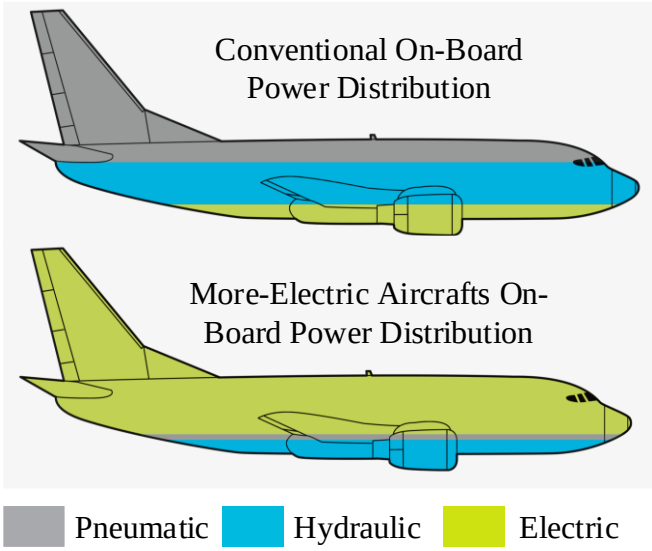



**Fig. 1-1. Breakdown of non-propulsive onboard power on a conventional aircraft and a more-electric aircraft. A more-electric aircraft uses more electric power to execute flight control, air conditioning, etc.**

The aerospace industry has started the practice of MEA concept. In early 2000, electrical system replaces one of the three traditional hydraulic systems on Airbus A380. The 600 kVA system is the first high power electrical system on commercial aircrafts. Later, the Boeing 787 Dreamliner extends the use of electrical systems in an innovative manner. It incorporates a no-bleed-air system that eliminates pneumatic systems and uses electric system to support the functions that are formerly powered by bleed air [3]. Furthermore, Boeing 787 uses 230 Vac variable frequency (360 Hz ~ 800 Hz) distribution system, which eliminates the gearboxes between jet engines and generators and further reduces take-off weight [3]. The total electrical capacity on a Boeing 787 is 1.5 MW, representing 150 % more electrical load than Airbus A380. Although, the transition to all-electric aircraft is still many years in the future, the aerospace industry is taking

steps towards the goal. Recently, Airbus, Siemens and Rolls Royce team up to develop a hybrid-electric flight demonstrator where one out of the four jet engines is replaced by a 2 MW motor [4]. A roadmap of aircraft electrification from Boeing (shown in Fig. 1-2) [3] shows the millstones towards all-electric aircraft. It is projected electrical system will gain more penetration, and ultimately, drive the aircraft directly.

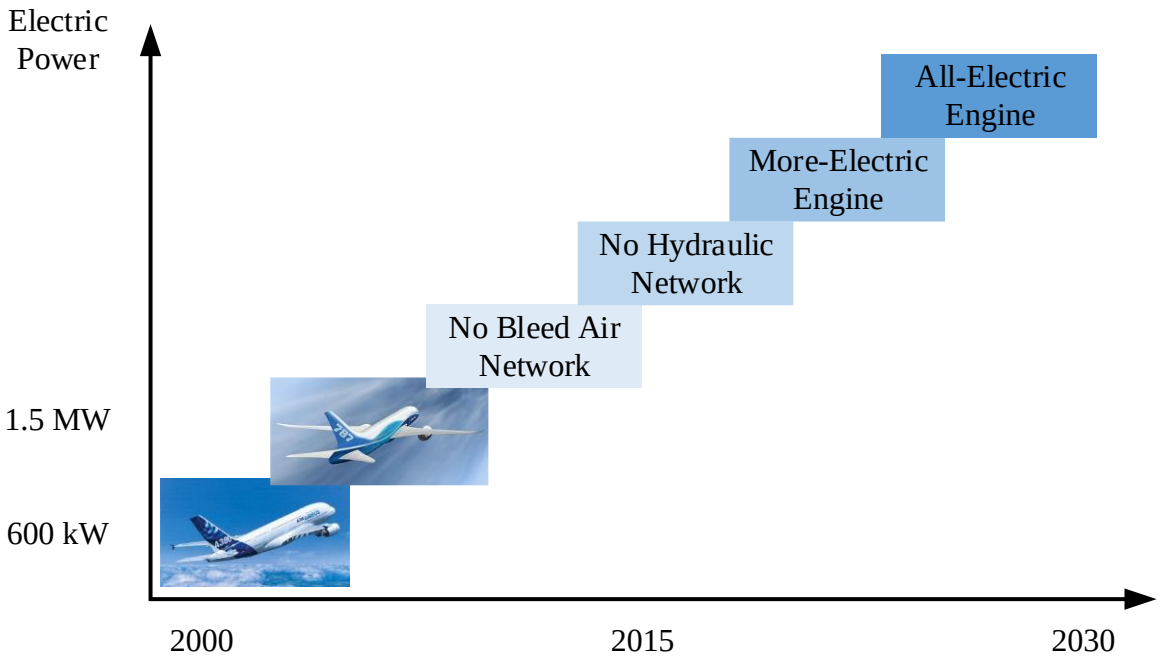



**Fig. 1-2. Roadmap of aircraft electrification [3].**

Power electronics is a key enabling technology in the MEA. Taking Boeing 787 as an example, it has a total of 1 MW of power electronics load. The interconnecting power electronics converters and the associated loads are summarized in Fig. 1-3. The power electronics converters convert variable frequency outputs of generator to various onboard buses (±270 Vdc, 28 Vdc, 230 Vac and 115 Vac) to power the loads. The MEA demands high reliability, high availability, high power density and high efficiency power converters. Besides, it puts stringent design requirements such as electromagnetic interference (EMI) requirement, power quality requirement and thermal

management requirement [5, 6]. The design framework of the converters should tackle the requirements while optimizing the performance, which is one of the main research topic in this work.

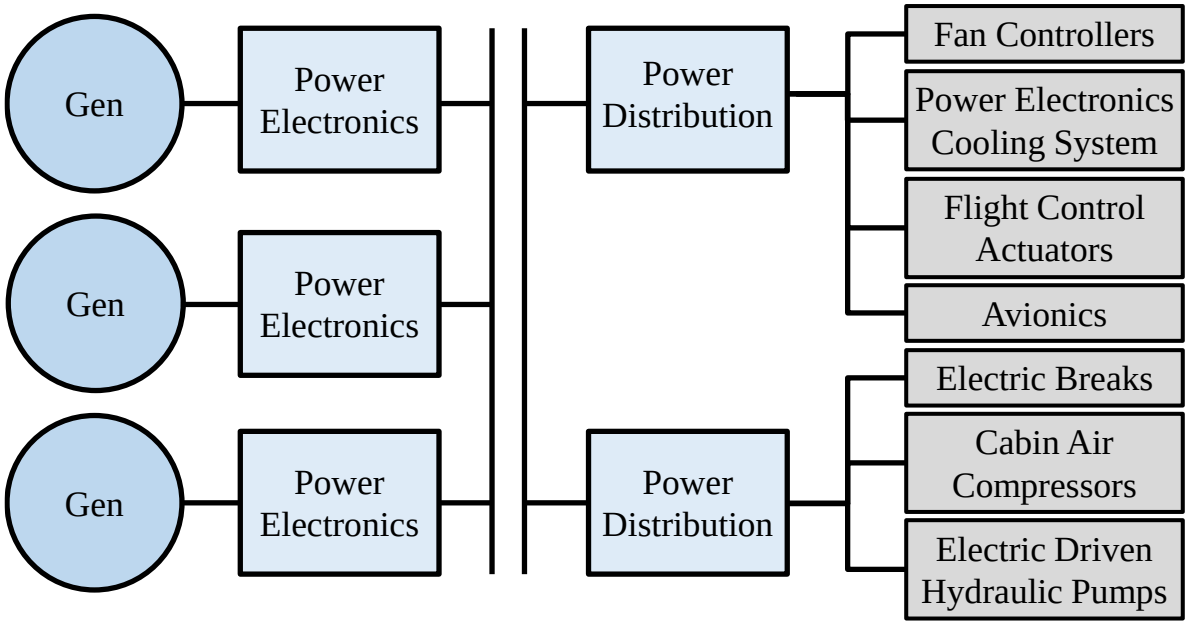



**Fig. 1-3. Power electronics load on a more-electric aircraft [3]. Power electronics converters are the key components interconnecting the generators, buses and loads.**

## 1.2 Design of Power Electronics Converters

### *1.2.1 Generic Design Framework*

Design is the process of conceiving a system that will subsequently by implemented and operated for some beneficial purpose [7]. In the context of this work, it refers to the conceiving of a power electronics converter or system. Modern system design involves optimization, of which the goal is to find a system design that will minimize some objective function. A generic design framework is formulated as:

$$\min/\max F(x) \quad (1),$$

$$\text{s.t. } g(x) \le 0 \quad (2),$$

where $F(x) = [F_1(x) \quad \cdots \quad F_z(x)]^T$ is the objective function, $x = [x_1 \quad \cdots \quad x_i \quad \cdots \quad x_n]^T$ is the design vector consisting of the design variables, s.t. is the abbreviation of "subject to", and $g(x) = [g_1(x) \quad \cdots \quad g_n(x)]^T$ represent design constraints [7]. The design framework is also depicted as block diagrams showing in Fig. 1-4, where the simulation model takes design vector *x* as input, evaluates the objective function *F(x)* and design constraints *g(x)*, and the optimizer takes *F(x)* as input and searches for new design vectors that can further optimize *F(x)*.

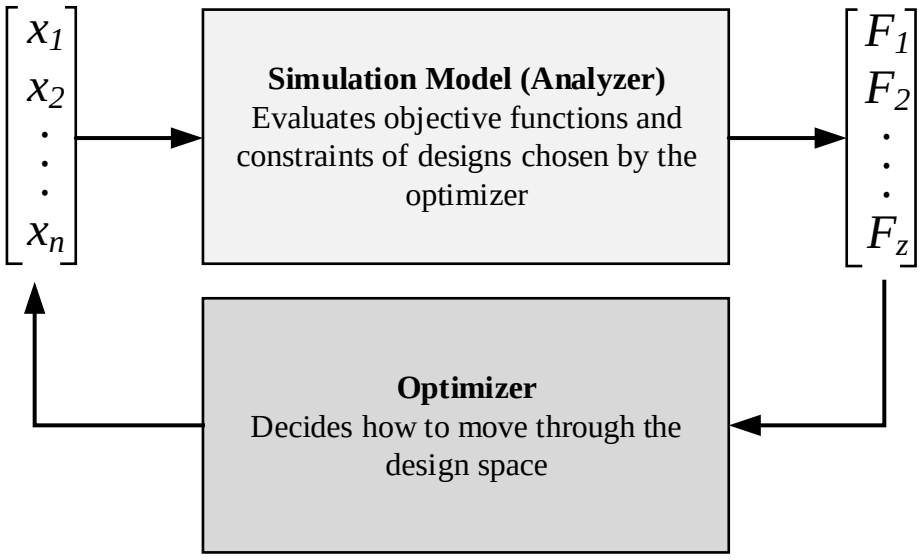



**Fig. 1-4. Generic design framework, modified from [7].**

At the core of the design are the simulation model and optimizer. The simulation model is categorized into physical model and mathematical model, and the the mathematical model is further categorized into analytical model and numerical model. A literature review on simulation models used in power electronics converter design is presented in section 1.2.3. The optimization

algorithm is categorized into direct search, numerical methods and metaheuristic methods. A literature review on optimization algorithms used in power electronics is presented in section 1.2.3.

### *1.2.2 Performance Measures of Power Electronics Converters*

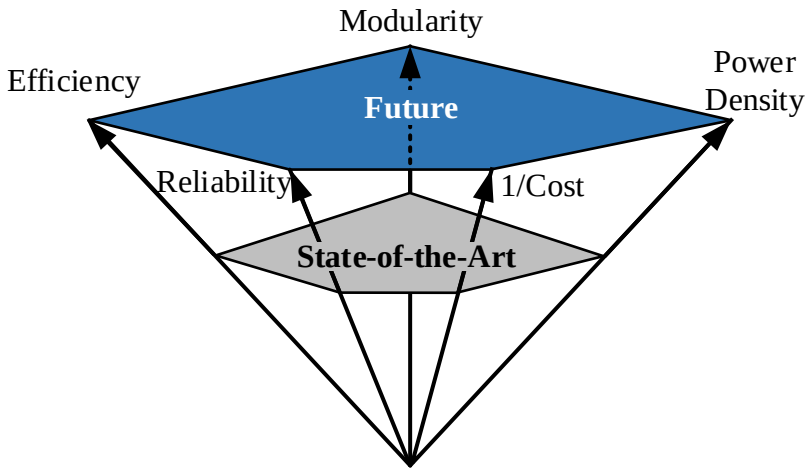



**Fig. 1-5. Main performance measures of power electronics converters and the trend, modified from [8].**

Performance of power electronics converters is measured by various performance indices, namely, efficiency, power density, cost, reliability and modularity [8]. Power converter designers are pursuing higher efficiency, higher power density, higher reliability, higher modularity while lower cost (including manufacture cost, maintenance cost and operational cost), and this trend is depicted by Fig. 1-5. However, owning to the coupling of performance measures, enhancing multiple performance measures might be conflicting. For example, to increase power density, a common approach is to increase switching frequency such that smaller passive components are required to handle the energy in switching frequency. However, it induces elevated semiconductor switching loss and ac conduction loss. Therefore, a tradeoff study is necessary, and the final design selection in most cases represents compromise between performance measures (e.g. compromise between efficiency and power density).

### *1.2.3 Design of Power Electronics Converters*

The design framework for power electronics converters should be able to handle a number of issues dictated by the nature of converter design:

- ► There might be a number of conflicting objective functions (stated in section 1.2.2).
- ► The design of power electronics converter involves various disciplines, namely, electrical circuit, electromagnetism, semiconductor, thermodynamics, etc. Different simulation and modeling tools are used to analyze these disciplines. The design framework should allow easy data transfer between the tools, e.g. data transfer between Matlab Simulink that is in charge of circuit analysis and ANSYS Maxwell that simulates inductor designs.
- ► The design might involve multiple design teams. The design framework should be able to operate in a distributed manner but allowing easy data transfer between teams. Even for single designer, a distributed design framework can accelerate the process by operating concurrent design using a multiprocessor computer.

Many design approaches have been proposed and used in design of power electronics components and converters. These approaches target at optimizing different objective functions using various simulation models and optimization algorithms under a variety of design frameworks. The following paragraphs present the literature review from the aforementioned aspects.

- ► Objective Functions

Common objective functions used in design of power electronics components and converters are efficiency (or loss), power density (or size and weight), cost and reliability. Prior the introduction of multi-objective optimization [8], design variable (topology, switching frequency,

devices, etc.) selection in most designs are based either on rule-of-thumb (e.g. a 70 kHz switching frequency to facilitate EMI filter design) and experience of the designer or on single-objective (depicted in Fig. 1-6) optimization. The objective function of the single-objective optimization includes efficiency [9-15] and weight or power density [16-21].

The experience-based procedure is unable to guarantee an optimal design because it highly depend on knowledge experience of the designer. The single-objective optimization based procedure may result in poorly designed overall system if a single objective function is aggressively pursued [22], e.g. aggressively pursuing high efficiency may results in bulky, lossy and costly design.

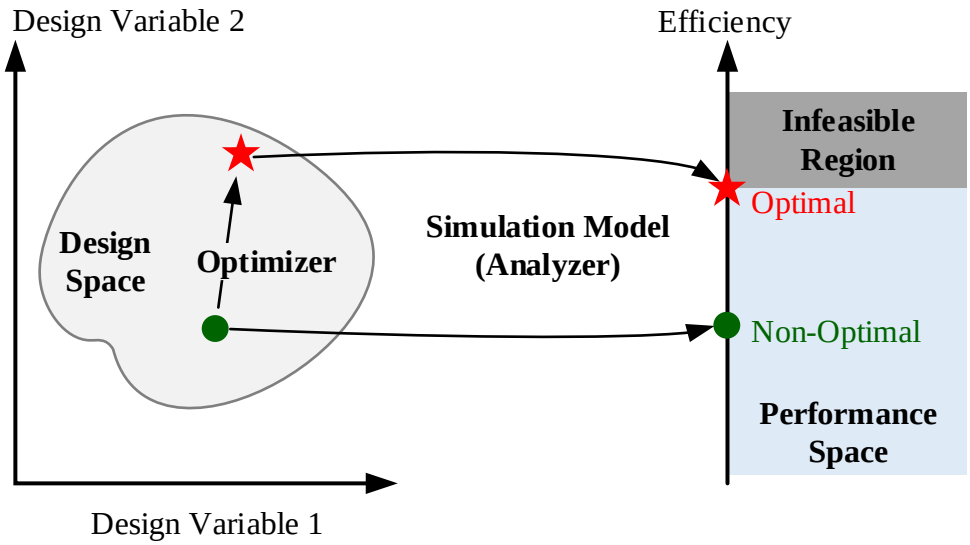



**Fig. 1-6. Single-objective optimization framework. An example of two-design-variable system is shown. The objective function is efficiency and is to be maximized. The simulation model calculates the efficiency and evaluates design constraints based on design variables. The optimizer searches for the design vector that leads to optimal efficiency.**

[8, 23] introduce multi-objective optimization to design of power electronics systems. This approach concurrently evaluates multiple objective functions, e.g. efficiency and power density, thus a more comprehensive design is achieved. The objective functions being evaluated using the

multi-objective optimization approach are efficiency-power density [5, 24-27], efficiency-weight [28, 29], efficiency-cost [30], efficiency-power density-cost [31] and efficiency-volume-failure rate [32]. Although the design that optimizes performance of all objective functions best suits the problem, it is rarely found since the optimization of multiple objective functions is likely to be conflicting, i.e. enhancing one objective function by adjusting design variables may worsen the other objective functions. Therefore, the outcome of a multi-objective optimization is usually depicted by Pareto front (two objectives) [8] or surface (three objectives) [31, 32] that represents tradeoff between objective functions. Pareto front (or surface) is the set of all Pareto optimal (also referred to as Pareto efficient) designs. A design is Pareto optimal if it is impossible to improve any performance indices without making at least one other performance index worse off. The design procedure and the outcome of a two-objective optimization is visualized by Fig. 1-7 as an example.

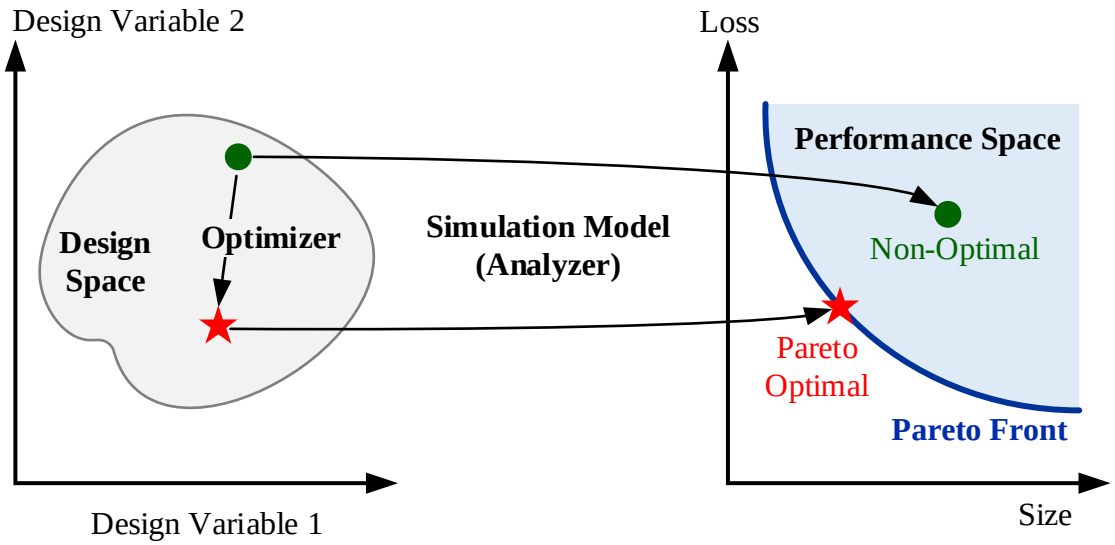



**Fig. 1-7. Multi-objective optimization framework. An example of two-design-variable system is shown. The objective functions are loss and size, and they are to be minimized. The Pareto optimal designs (it is impossible to reduce the loss and size of the Pareto optimal designs**

**concurrently) form the Pareto front, demonstrating the tradeoff between the two objective functions.**

Some other objective function including current quality [33], insulation capacitance of isolated power supplies [34], leakage magnetic field of wireless chargers for electric vehicles [35] and parasitic parameters in power modules and gate driving circuits [36, 37] are found in literatures.

This work uses nominal power as objective function. For the problem of concern, maximizing the nominal power exploits the form factor limit and loss budget of the modular converter and leads to optimal design.

► Optimization Algorithm

For the optimizer, various algorithms has been used for searching optimal designs of power electronics component and converters, e.g. direct search as in [5, 9, 24-27, 35, 38-40], numerical algorithms as in [8, 41] and heuristic algorithms as in [36, 37, 42-47]. However, deriving numerical models used in numerical algorithms is impractical owning to the complexity and nonlinear nature of power electronics systems. The metaheuristic algorithms, e.g. genetic algorithm, particle swarm and simulated annealing, render non-deterministic results. Their convergence and ability to find global optimal points highly depend on the initial values and optimization settings. However, there is no clear guidelines on setting these parameters for power electronics applications. Therefore, direct search is used herein.

► Simulation Models

At the core of the design is simulation models, of which the accuracy and complexity determines the fidelity and calculation speed of the design. The simulation models used in analyzing performance of key components (semiconductor devices, magnetic components) are discussed as follow.

For semiconductor devices, most literatures focus on characterization of the switching transients and switching loss. Although analytical models using data sheet information [48-51] and SPICE models [52, 53] provides quick estimation of switching loss, performing double pulse tests (DPT) [54-57] is able to take the device temperature [56-59], parasitics of external connections (e.g. printed circuit board) and capability of the gate drivers into account, thus rendering more complete and accurate modeling. An empirical model of switching loss (with respect to switching current, voltage, temperature, etc.) can be built from DPT results and is later used in converter design. A few circuit simulation software, e.g. PLECS, has included similar empirical models for real-time switching loss and temperature estimation. In this work, a complete characterization of candidate devices is presented in Chapter 2.

For design of magnetic components, the focuses are on winding loss modeling and core loss modeling. Finite element analysis (FEA) software (e.g. ANSYS Maxwell) is widely used in modeling winding loss considering skin effect, proximity effect and fringing effect. For analytical solutions, [60] is widely used in modeling winding loss of solid conductors. It is also being used in modeling winding loss of planar magnetics of high switching frequency power converters where the winding (implemented by PCB trace) is too thin to be finely meshed in FEA software [61]. For applications using litz wire, the winding loss can be calculated by methods discussed in [62-65]. These methods requires the knowledge of the magnetic field that penetrates the winding, which is either calculated through 1D approximation [66] or through FEA simulation. Core loss is mostly modeled by empirical models such as Steinmetz's equation [67], generalized Steinmetz's equation [68] and improved Steinmetz's equation [69]. The excitation of the latter is not limited to sinusoidal excitation, which suites the design of pulse width modulated converters. However, these

models neglects the flux density dc bias. Advanced models [65, 70-72] takes this factor into account by deriving empirical models based on experimental data. However, deriving the model for a variety of cores could be time consuming as the influence of dc bias is depend of operation point and material.

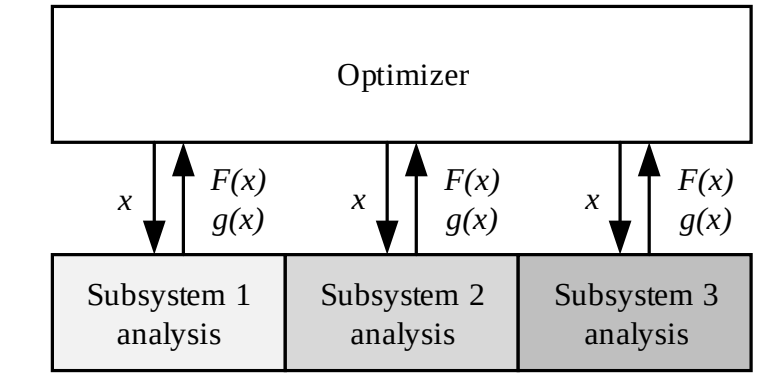
Furthermore, virtual prototyping and multi-domain simulation are interesting topics to the power electronics community [20, 73, 74]. This methodology links the analysis of different disciplines, e.g. electric, magnetics, thermal and mechanical, allowing for concurrent multi-domain design and optimization. An example of virtual prototyping is demonstrated by [75] where the authors use iSight to integrate the electrical and thermal design of an integrated (IPEM). Ref. [76] proposes a tool that integrates the electric, thermal and parasitic analysis model for power module design. It uses order reduction (MOR) techniques to replace FEA-type simulation, which improves the calculation speed. The virtual prototyping tool could improve the fidelity of the simulation models since coupling effect of various disciplines are considered concurrently. It might potentially be integrated with optimization tools for fully automated prototyping of power electronics converters.

► Design Framework

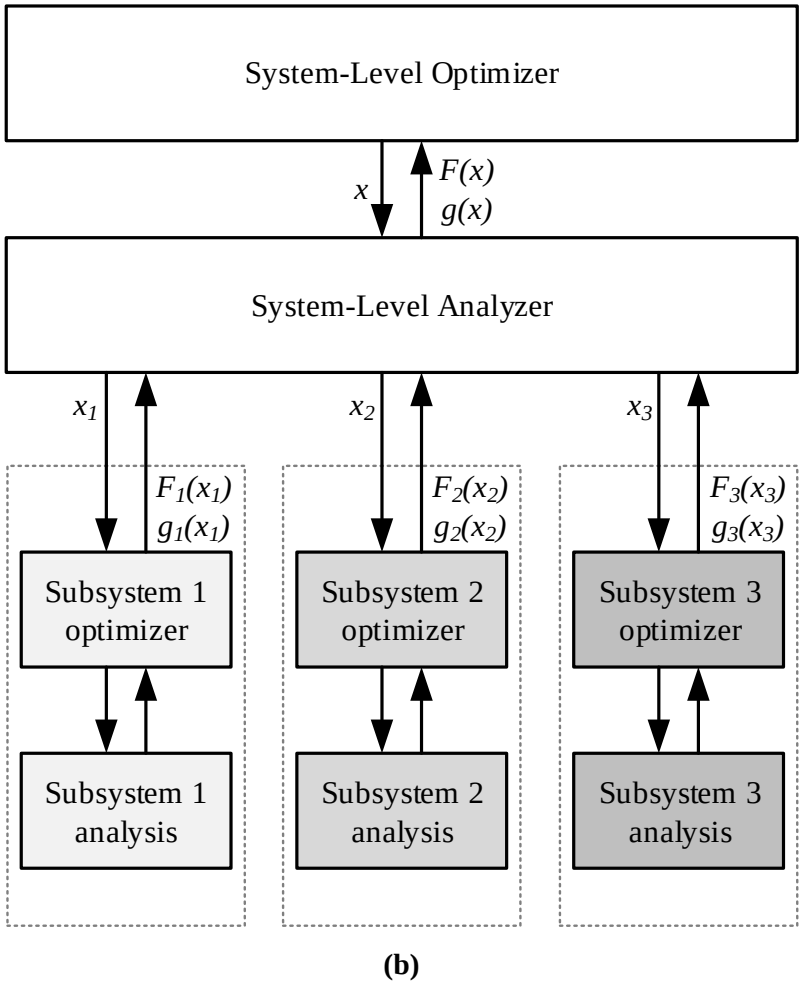
The optimization framework belongs to one of the two categories: single-level optimization and multi-level optimization. The two frameworks are visualized in Fig. 1-8 (a) and (b) [7].

The single-level optimization (shown in Fig. 1-8 (a)) has one optimizer oversees the value of the design variables and objective. The value of design variable changes according to the centralized optimizer. The subsystem analyzers are asked to evaluate constraints and objective

functions. Single-level architecture is mostly used in optimization of key components in a converter. Examples are [9, 34, 35, 61, 77].




**(a)**




**(b)**

**Fig. 1-8. Single-level and multi-level optimization framework, modified from [7] (a) Single-level framework, centralized optimization. (b) Multi-level optimization, distributed optimization.**

Contrary to the single-level optimization, multi-level (shown in Fig. 1-8 (b)) optimization distributes not only the optimization but also decision making through the subsystems. This framework provides autonomy to various disciplines and facilitates concurrent calculation. Thanks to the multidisciplinary nature of power electronics converters, most literatures [9, 21, 24-27, 31, 35, 38, 39, 44, 74, 78-80] employs a multi-level design architecture, e.g. there are inner loops for component design and output loop for selection of converter-level parameters. However, the design procedures presented in these literatures are developed specifically for the topology of concern, and is not readily transferrable to other topologies and applications. This work generalizes the design framework using the concept of bi-level problem programming (presented in following paragraphs), making it easier to adopt. Besides optimizing converter performance, this work uses the multi-level optimization framework to: maximize nominal power of modular converters (presented in Chapter 3); design a two-stage converter where the two stages are strongly coupled (presented in Chapter 4); compare topologies and investigate the impact of key design variables in converter design (presented in Chapter 3 and Chapter 5).

The multi-level optimization for engineering problems has been widely discussed in aerospace community where the design normally involves large number of design variables and integration of various disciplines [81]. There are two mainstream multi-level frameworks, namely, collaborative optimization (CO) [82] and bi-level integrated system synthesis (BLISS) [83-85] used in aerospace community. In CO, the system-level optimizer provides design variable targets to the subsystems, and the subsystem optimizer finds designs that minimizes the difference

between current states and the targets while complying with the local constraints [83, 85]. A CO problem has two levels and the system-level problem is formulated as:

$$\min F_{sys} \tag{3},$$

$$\text{wrt}: x_0 = \text{target variables} \tag{4},$$

$$\text{s.t. } J_k = 0 \forall \text{ subproblems}_k \tag{5},$$

where wrt stands for "with regard to". The system-level optimizer searches for $x_0$ such that it minimizes objective function $F_{sys}$ and reduces $J_k$ (termed compatibility constraints). The subproblems are formulated as:

$$\min J_k = (\text{target variables - } k^{th} \text{ local variables})^2 \tag{6},$$

$$\text{s.t. } k^{th} \text{ local constraints} \tag{7}.$$

All the design variables in CO is overseen by both system-level and subsystem-level optimizers, and it decouples the design of subsystems by letting optimizers of both levels changes the design variables. The CO suits optimization problems where the design variables are limited but strong coupling between subproblems exists. For power electronics converter design, where there are a large number of design variables, the CO could be too complicated to solve.

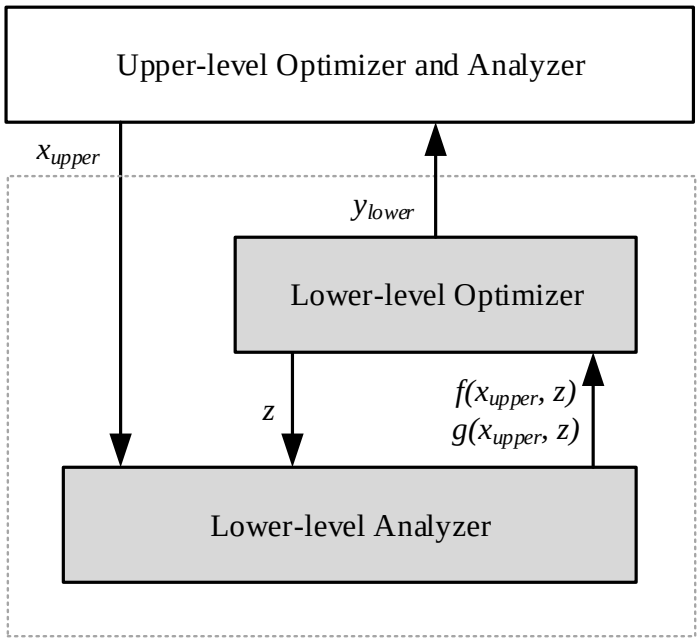



**Fig. 1-9. Simplified block diagram of bi-level integrated system synthesis, modified from [83].**

In BLISS, instead of providing design variable targets, it sends system-level design variables to the subsystem analyzers, and these variables stay as constant during the subsystem design [83]. A simplified BLISS design framework modified from [83] (original figure is Figure 8.16 in [83], the surrogate input $y^v$ and weighing term $w$ are omitted) is depicted in Fig. 1-9. The subsystem-level (lower-level) optimizer searches for local design variables that minimizes the local objective functions while complying with local constraints. The system-level (upper-level) optimizer searches for system-level design vector that optimizes the ultimate objective function while complying with the system-level constraints. The complete BLISS is formulated based on response surface methodology and post-optimal analysis such as sensitivity analysis [84, 85], which is too complicated to be used in design of power electronics converters.

Nevertheless, BLISS is essentially a bi-level programming problem (BLPP) [86], which is defined as "a mathematical program that contains an optimization problem in the constraints" [87]. The upper-level problem of a bi-level optimization is formulated as:

$$\min F(x_{upper}, y_{lower}) \tag{8}$$

$$\text{s.t. } G(x_{upper}, y_{lower}) \leq 0 \tag{9}$$

where the $F$ represents upper-level objective function, G represents upper-level constraints, $x_{upper}$ is the upper-level design variable, and $y_{lower}$ is the lower-level design vector that solves the lower-level problem ("the optimization problem in the constraints") and is defined by the lower-level optimization problem below:

$$\min f(x_{upper}, z) \tag{10}$$

$$\text{s.t. } g(x_{upper}, z) \leq 0 \tag{11}$$

$$y_{lower} \in \arg\min\{f(x_{upper}, z) : g(x_{upper}, z)\} \tag{12}$$

where $z$ is the lower-level design vector, and $g(x_{upper}, z)$ represents lower-level constraints.

The framework of BLPP fits design of power electronics converter. The converter-level variables, e.g. topology, switching frequency and values of passive components, are constant in component design. The design of components needs optimizers that searches for component-level design variables. The objective function of converter-level design is likely to be component-level objective functions combined in certain manner, e.g. converter loss is the sum of component loss. These converter design procedures matches the structure of BLPP. Therefore, BLPP is used in this work. Furthermore, for more complicated power converter system or design, e.g. two-stage converter, BLPP can be cascaded to form a multi-level framework that consists of more than two levels. Detailed design framework is elaborated in Chapter 3 and Chapter 4.

## 1.3 Modular Power Electronics

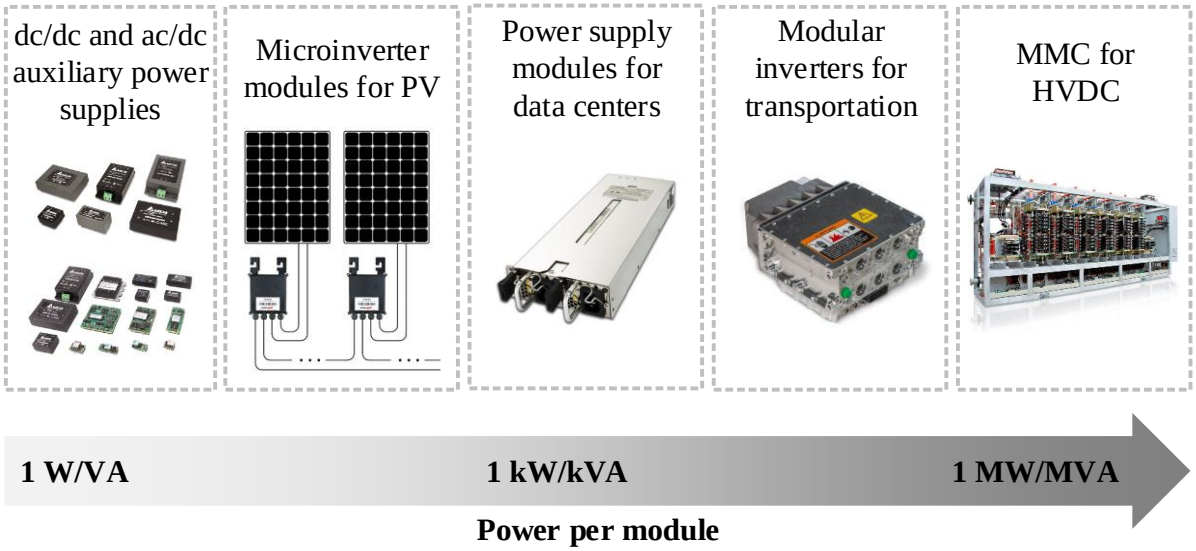



**Fig. 1-10. Modular power electronics converters in various applications from watt-level to megawatt-level.**

Since the first introduction of power electronics building blocks (PEBB) by U.S. Office of Naval Research (ONR) [88], modularizing power electronics converters has gain tremendous interest, a trend that has be seen in power supplies in small auxiliary power supplies [89], renewable energy applications [90], telecommunication power supplies [91], vehicular applications [92], and recently, high voltage DC (HVDC) applications [93, 94]. Some of the modular products for abovementioned applications are summarized in Fig. 1-10. For these applications, modularity provides the system with redundancy for reliable operation [91], flexibility for high performance [95] and product standardization for low lifecycle cost [88, 96, 97]. To reap the benefits, module specifications (e.g. form factor, footprints, etc.) and communication between modules should be clearly defined by the system designers so that module designers produce standardized converters by complying with the specifications. This coordinates with the objective of Distributed-Power Open Standards Alliance (DOSA) [89], an industrial

organization striving to establish standards for DC/DC converter modules. The control and communication of converter modules working in parallel has been discussed in [98-102], and will be discussed in Chapter 5. The module specifications are defined primarily by packaging considerations such as thermal, interconnections, manufacturing economics, etc. [88].

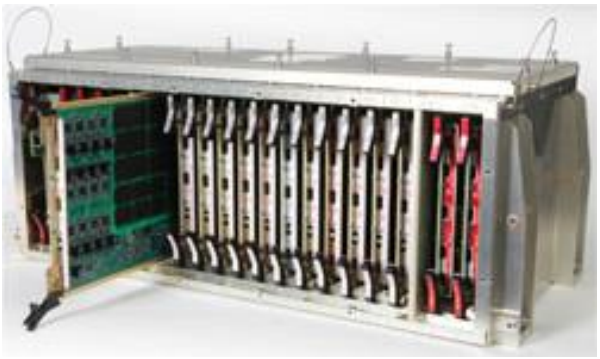


**Fig. 1-11. Onboard power distribution and management system with modular power converters [103]. The form factor of each module is constrained by the chassis. The entire chassis is enclosed, thus all modules are natural convection cooled. To avoid overheating, there is loss budget specified for each module.**

Specifically, this work aims at designing modular power converters for aerospace applications, where the form factor of each module is determined by the chassis, the loss budget is determined by system thermal management limit and the cooling is natural convection. A commercial onboard power distribution and management system is shown in Fig. 1-11 to demonstrate the system assembly and constraints. The power distribution and management system use solid-state power controllers to increase the reliability by eliminating lower reliability components. To maximize system capacity and reveal performance potential under such constrains, the nominal power is not specified and is to be maximized herein. Optimization of power electronics converters, either single-objective optimization focusing on efficiency [9] or power density [21], or multi-objective optimization focusing on efficiency-power density [5, 24], efficiency-cost [30] or other key performance measures [33, 78], has been widely used and discussed for decades. However, these

design approaches cannot be directly applied, because the objective functions (efficiency and power density) in aforementioned literatures are design constraints (loss and form factor), and the primary objective function is nominal power herein. Only a few literatures [38, 39] discuss nominal power maximization for modular converters. This work uses BLPP to formulate the nominal power maximization problem, and the approach will be presented in Chapter 3. This approach not only renders the optimal converter design, but also quantitatively evaluates influence of design constrains (form factor, loss budget, etc.) and compares converter topologies. For evaluating influence of design constrains, an issue frequently discussed between system-level and module-level designers., this work compares the maximal nominal power of a converter module that has doubled height and loss budget with that of two converter modules working in parallel. The results and discussion will be elaborated in Chapter 5.

## 1.4 Organization of This Work

This work discusses the design framework, models, control and modularity issues of form-factor-constrained, loss-budget-limited modular power converters for aerospace applications. It is organized as follows.

Chapter 1 introduced the background application and presents literature surveys on design framework for power electronics converters and modular converters.

Chapter 2 presents characterization of SiC MOSFETs with focus on its switching transients under various temperatures in a phase-leg configuration, a key test of which the results are used in converter design to model the switching loss. It is proposed to conduct two tests to accurately

characterize the switching transients. The test setup, the testing results and data processing are elaborated.

Chapter 3 focuses on the nominal power optimization of a form-factor-constrained loss-budget-limited active front-end converter (AFE). The nominal power optimization problem is converted to a sets of loss-size multi-objective optimization problems by using BLPP. The loss-size multi-objective problem is formulated using BLPP so that all the components are optimized locally and concurrently. The models for converter and component design are elaborated. A 1.2 kW Vienna rectifier prototype is constructed based on the design procedure, which validates the models and the procedure. Furthermore, a control method is proposed to compensate the turn-off delay of MOSFETs in Vienna rectifiers. The method is experimentally verified.

Chapter 4 extends the design of a single stage converter discussed in Chapter 3 to a two-stage isolated converter. The converter system consists of an AFE and an isolated dc/dc converter. However, the design constraints apply to the entire system. To deal with the two stages, another BLPP is cascaded to the design presented in Chapter 3. Models with attention paid to component model of dc/dc stage are detailed. Furthermore, the influence of the interconnecting dc bus voltage, a critical parameter to both stages, is studied. A 1.2 kW prototype consists of a Vienna rectifier and an LLC resonant converter is constructed. The testing results are presented.

Chapter 5 presents the design and control of a modular inverter. Four topology including three hard-switching topologies and one soft-switching topology are considered, and their performance is compared by their maximum nominal power. Regarding modularity of power converter, an investigation on influence of form factor on maximum nominal power is presented. Besides converter design, the control architecture for paralleling the inverter modules is discussed. EMI

issues associated with parallel operation is analyzed. The testing results of a single module as well as paralleled modules are presented.

Chapter 6 concludes this work and proposes future work.

# Chapter 2. Measurement and Characterization of SiC MOSFET Switching Transients

## 2.1 Chapter Introduction and Prior Art

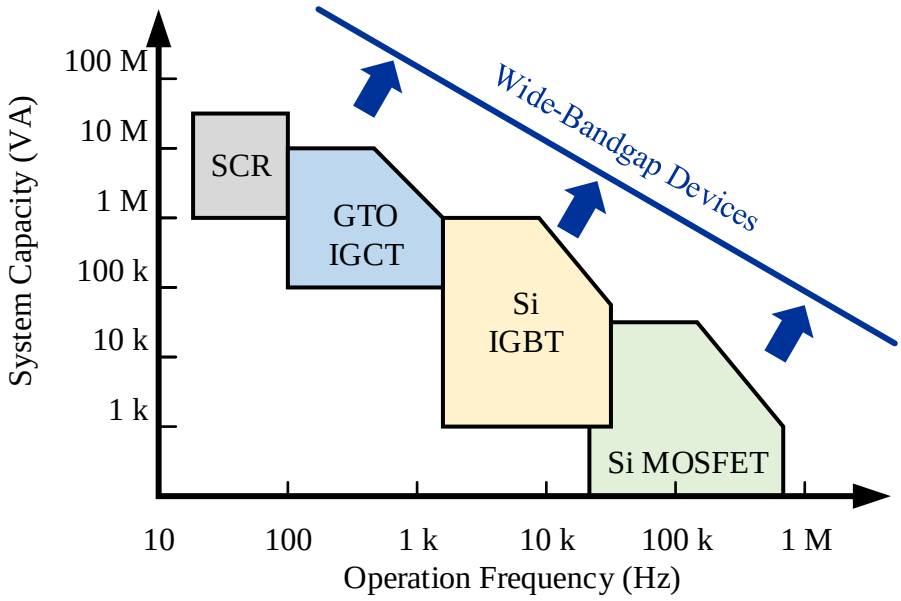



**Fig. 2-1. Wide-bandgap power semiconductor device feature superior performance. It enhances performance of power converters with different power levels.**

Wide-bandgap (WBG) semiconductor devices have been the main driving force of recent power electronics advancements [31, 104]. They are pushing the performance boundary from watt-level applications to mega-watt-level applications thanks to their ability to operate at high breakdown voltage, wide temperature range and high switching frequency. The trend is depicted by Fig. 2-1. Specifically, for low voltage applications (blocking voltage less than 400 V), researchers have demonstrated converters that achieved boosted efficiency [105] and higher power density [104] thanks to the use of gallium nitride (GaN) MOSFETs. While for medium voltage

applications (greater than 400 V but less than 10 kV), silicon carbide (SiC) MOSFETs show superior conduction and switching performance in a wide temperature range [106]. Besides performance enhancement [39] as of GaN-based converters, SiC-based converters feature simple thermal management [107], reduced manufacture cost and lifetime cost [31]. For high voltage applications (greater than 10 kV), SiC MOSFET and IGBT [108] are potential replacements for GTO, IGCT and SCR. [109, 110] report using 15 kV SiC MOSFETs in a solid-state transformer for grid applications. To exploit benefits of WBG semiconductor devices, a comprehensive loss characterization, upon which circuit designers estimates semiconductor loss and optimize converter performance [56, 57, 59, 111, 112], is necessary. For conduction loss, on-resistance vs. temperature information provided in datasheets is normally accurate enough. However, characterizing switching loss is challenging, for the loss is highly dependent of testing condition and circuit parasitic [112]. In addition, reverse recovery loss from body diodes (PIN type, intrinsic) in SiC MOSFETs, which varies with switching current, transition speed, temperature and many other conditions, complicates the characterization [56, 57, 113]. Therefore, circuit designers usually conduct double pulse test (DPT) to measure switching loss. This chapter focuses on SiC MOSFETs switching transient study and loss characterization under 25 ºC to 150 ºC. Although only SiC MOSFETs are under test, the setup and the switching loss mechanism that are analyzed in this chapter apply to Si and GaN devices.

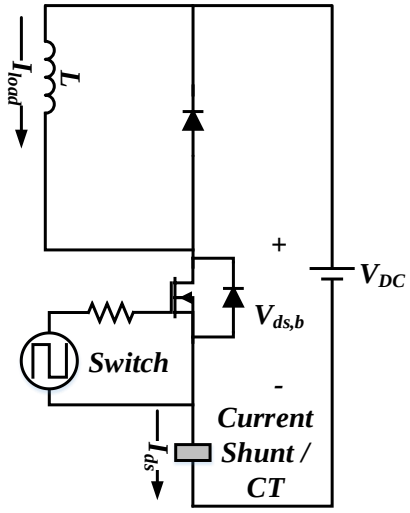



**Fig. 2-2. Double pulse tester using diode as commutating device.**

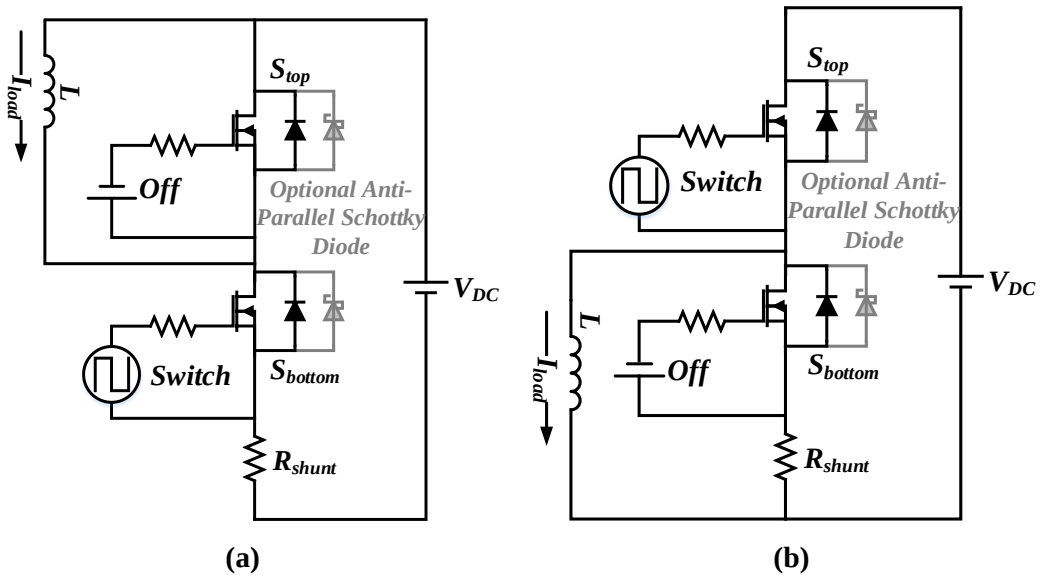



**Fig. 2-3. (a) Bottom-device-switching test schematic. (b) Top-device-switching test schematic. Note that anti-paralleled Schottky diodes are optional.**

Specifically, this chapter starts with the DPT setup for characterizing SiC MOSFETs that are in a phase-leg configuration. In most literatures [56-59], DPT circuits use diodes as top device for freewheeling and MOSFETs on the bottom as device under test (DUT) (configuration shown in Fig. 2-2). The current flowing through the DUT is measured by a low inductance shunt resistor [59] or a current transformer [57], and the drain-to-source voltage is measured by a voltage probe.

The switching energy is calculated from integrating the product of DUT voltage and current over time under the assumption that the freewheeling diode (top device) is "lossless". However, it will be shown in this chapter that there is considerable loss dissipated in top device no matter what type the device is. Furthermore, this configuration does not reflect the switching loss in a converter phase leg that consists of two MOSFETs owning to the unaccounted reverse recovery loss of body diode. To characterize the switching loss in a phase-leg configuration throughly, two tests are needed, namely, one with top device switching and the other with bottom device switching, (schematics shown in Fig. 2-3 (a) and (b) respectively). The top-device-switching configuration [113] (shown in Fig. 2-3 (b)) is a direct measurement of reverse recovery behavior of bottom device, and it shares the same equipment with the bottom-device-switching configuration. Comparing to other test setups for reverse recovery characterization, where either indirect current measurement (e.g. derive reverse recovery behavior of top device through measurements of bottom device in Fig. 2-3 (a)) [57] or an additional current measurement [114] is required, the bottom-device-switching configuration is accurate and easy-to-use.

With the aforementioned setup, the switching and reverse recovery characteristics of various SiC MOSFETs ($2^{nd}$ and $3^{rd}$ generation devices from Wolfspeed) is studied. Ref. [57] reported the reverse recovery characteristics of CREE's $1^{st}$ generation device (CPMF1200S080B). The influence of switching voltage, switching current, di/dt and temperature is thoroughly studied. Other literatures reported modeling of reverse recovery loss by different approaches. Ref. [56] proposed a physics-based reverse recovery model while [59] proposed a numerical model extracted from testing results. This chapter focused on evaluating devices with different die size (different die sizes but the same generation) and with different technologies ($2^{nd}$ and $3^{rd}$ generation

from Wolfspeed) in a wide temperature range (25 ºC ~ 150 ºC). The loss related to charging the nonlinear junction capacitors and reverse recovery is analyzed in detail, which serves as fundamental for future switching loss modeling.

The testing results are used to model the switching loss in converter design that is presented in Chapter 3, Chapter 4 and Chapter 5.

## 2.2 Hardware Setup for Top-Device-Switching and Bottom-Device-Switching Tests

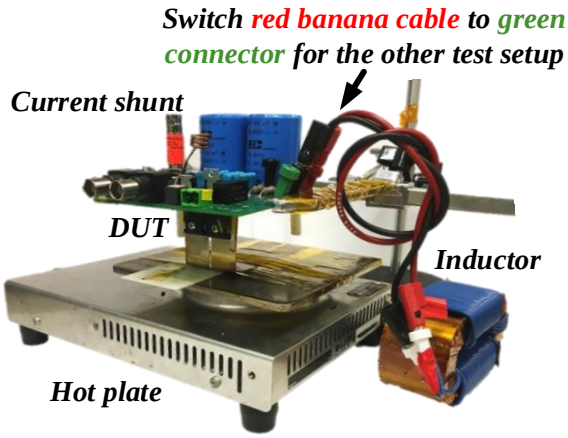



**Fig. 2-4. Hardware setup of the two tests. They share the same hardware. Changing the inductor and gate signal connection changes the test type.**

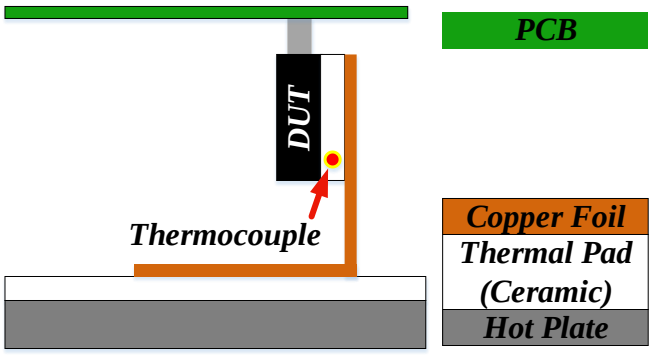


**Fig. 2-5. Heating setup of the DUT.**

The two tests share the same hardware, and the hardware setup is shown in Fig. 2-4. The connection of inductor and gate signals need to be changed for different tests. Optional diodes could be mounted in parallel with the MOSFETs for evaluating necessity of anti-parallel diodes. In addition, the device under test (DUT) is attached to a hot plate for junction temperature control, and a thermocouple is attached closely to the DUT to monitor the junction temperature (configuration shown in Fig. 2-5). For current measurement, a low inductance, high bandwidth current shunt (T&M Research Products SSDN-10) is used. For drain-to-source voltage measurement, a high voltage passive probe (Tektronix TPP0850) is used. The measurement ground is fixed at source of bottom device for both tests. All switches are driven by IXDN614CI (up to 35 V, 14 A) gate drivers. The gate resistance is changed for difference devices to keep the same *di/dt* during turn-on. Driving voltage is 20 V/ -5 V for 2$^{nd}$ generation devices and 15 V/ - 5 V for 3$^{rd}$ generation device.

## 2.3 Analysis on Switching Transients

This section presents the data processing and results of the tests. Four devices from Wolfspeed: C2M0080120D (1200 V, 80 mΩ), C2M0040120D (1200 V, 40 mΩ), C2M0025120D (1200 V, 25 mΩ) and C3M0065090D (900 V, 65 mΩ) are tested. The first three are of the same technology (Wolfspeed's 2$^{nd}$ generation) but different die size. The latter is of the newest technology (3$^{rd}$ generation) and similar die size with C2M0080120D. These devices are tested under 540 V switching voltage (typical DC bus voltage on a modern airplane [39]), 2 ~ 36 A current and 25 ~ 150 ºC junction temperature. In this work, the switch that is kept off during the test is termed

"commutating switch", and the other is termed "switching switch". The switch that is between positive rail and ac terminal is termed "top switch" or $S_{top}$, and the other is termed "bottom switch" or $S_{bottom}$.

In this section, the testing results and post-testing data processing of C2M0025120D is discussed as an example. The waveform analysis and post-testing data processing applies to other devices.

### *2.3.1 Analysis of Turn-on Transient Based on Simplified Waveforms*

This section analyzes the turn-on transients with simplified waveforms. First, assume the output capacitance of the two MOSFETs is zero, and there is no reverse recovery effect from the body diodes. Assume without losing generality, a bottom-device-switching test is conducted, and the switching switch (bottom switch) is turning on. The ideal waveforms of the turn-on transients and the corresponding schematic are depicted in Fig. 2-6. As $I_{top}$ reaches zero, $V_{top}$ starts to rise. The changing rate of both $I_{top}$ and $V_{top}$ is controlled by gate voltage. Because either $I_{top}$ or $V_{top}$ is zero at any time, there is no energy dissipated from or stored in the top switch. The energy dissipated from the bottom switch ($E_{on,ideal}$) is induced by the overlap of voltage and current and is calculated by:

$$E_{on,ideal} = \int_{t_0}^{t_2} V_{bottom}(t) I_{bottom}(t) dt \quad (13).$$

In this chapter, the loss induced by overlap of voltage and current during switching switch turn-on is termed voltage-current overlap loss, $E_{overlap}$.

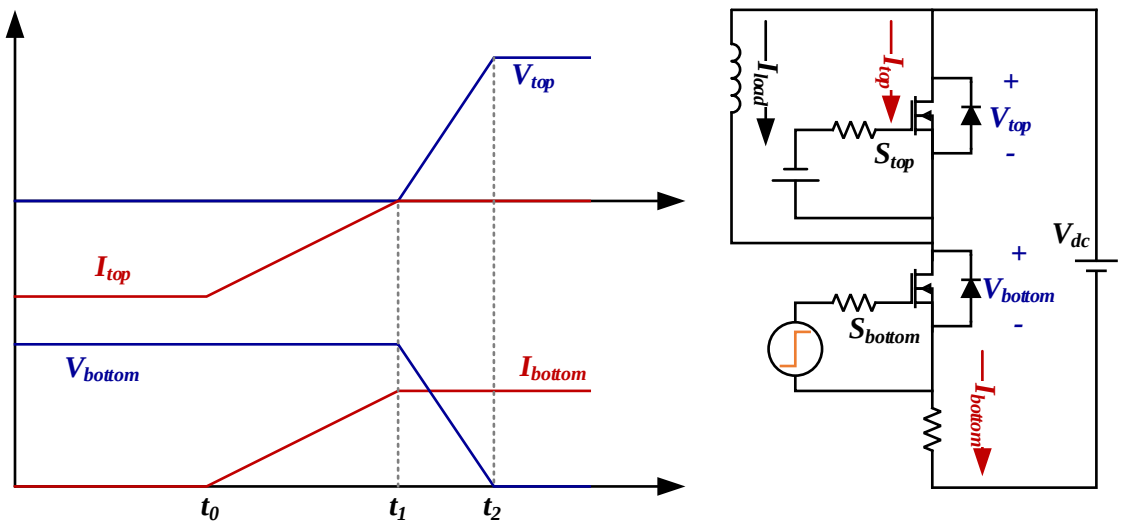



**Fig. 2-6. Ideal current and voltage waveforms (assuming zero output capacitance and no reverse recovery effect) during turn-on of bottom switch.**

Considering the reverse recovery effect of body diode and output capacitance of the MOSFETs, additional current that represents the reverse recovery charge and output capacitor charge going into the top switch is observed, and this phenomenon is depicted in Fig. 2-7. The "current bump" is observed when voltage of top device is building up (between $t_1$ and $t_2$). Charge is needed to remove the minority carriers from the body diode and to charge the output capacitor. The charge is provided by the dc source. The excessive energy ($E_{dc,excessive}$) associated with providing the charge is calculated by:

$$E_{dc,excessive} = \int_{t_1}^{t_2} V_{top}(t) I_{top}(t) + V_{bottom}(t)(I_{bottom}(t) - I_{load})dt = \int_{t_1}^{t_2} V_{top}(t) I_{top}(t) + V_{bottom}(t) I_{top}(t) dt = V_{dc} \int_{t_1}^{t_2} I_{top}(t) dt \quad (14).$$

Part of $E_{dc,total}$ is stored in the output capacitor of top switch (also the commutating switch in this analysis), and the rest is dissipated. Term $\int_{t_1}^{t_2} I_{top}(t)dt$ in (14) represents the total charge ($Q_{total}$)

provided by the dc source, including reverse recovery charge ($Q_{rr}$) and charge in the output capacitor of commutating switch ($Q_{oss}$).

$$Q_{total} = \int_{t_1}^{t_2} \mathrm{I}_{top}(\mathrm{t})dt = Q_{rr} + Q_{oss} \tag{15}.$$

However, there is no practical method to separate $Q_{rr}$ and $Q_{oss}$ in real measurement. Therefore, datasheet information is used to calculate $Q_{oss}$:

$$Q_{oss}(V_{ds}) = \int_{0}^{V_{ds}} C_{oss}(v)dv \tag{16},$$

where $Q_{oss}$ is a function of drain-to-source voltage $V_{ds}$. Then, $Q_{rr}$ is calculated by:

$$Q_{rr} = Q_{total} - Q_{oss}(V_{dc}) \tag{17}.$$

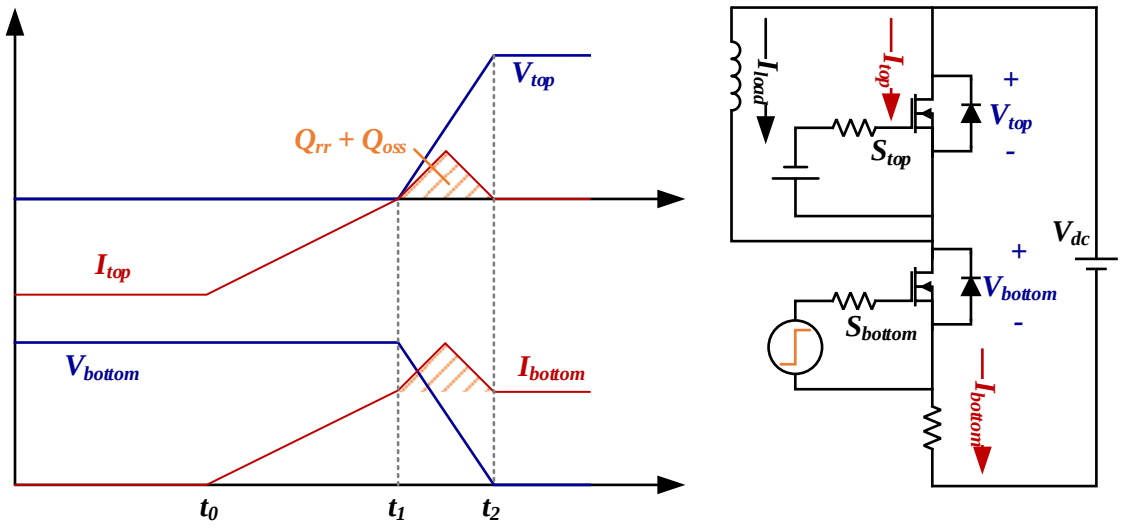



**Fig. 2-7. Voltage and current waveforms considering the reverse recovery effect and output capacitor. The "current bump" represents the charge for reverse recovery effect and output capacitor.**

The aforementioned analysis is the basis of quantifying the loss from various loss mechanisms, namely, reverse recovery loss ($E_{rr}$) of the body diode, output capacitor energy dissipated in channel

of switching switch ($E_{oss,channel}$), commutating device capacitive charge induced loss ($E_{oss,induced}$, different from $E_{oss,channel}$) and voltage-current overlap loss ($E_{overlap}$).

► **Reverse recovery loss, $E_{rr}$**

The reverse recovery loss is calculated by:

$$E_{rr} = V_{dc} Q_{rr} \tag{18}.$$

All the reverse recovery charge is provided by the dc source and will not return to the circuit (unlike charge stored in the output capacitor).

► **Output capacitor loss, $E_{oss,channel}$**

The output capacitor loss $E_{oss,channel}$ represents the energy stored in the output capacitor of switching switch ($S_{bottom}$ in Fig. 2-7) and dissipated in the channel during device turn-on. It cannot be measured by external sensors (e.g. current shunt shown in Fig. 2-3) as the energy is dissipated internally. It is calculated using datasheet information:

$$E_{oss,channel} = \int_0^{V_{dc}} C_{oss}(v) v dv \tag{19},$$

where $C_{oss}(v)$ represents the output capacitance at drain-to-source voltage $v$ and can be got in datasheet.

► **Capacitive charge induced loss, $E_{oss,induced}$**

The capacitive charge induced loss $E_{oss,induced}$ measures the loss induced by charging the output capacitor of the commutating device, e.g. $S_{top}$ in Fig. 2-10 (a). The charging of output capacitor is modeled as a dc source providing charge to a nonlinear capacitor. The energy provided by the dc source for charging the capacitor is calculated by:

$$E_{total,oss} = V_{dc} Q_{oss} \tag{20},$$

where $Q_{oss}$ is calculated by (16). The energy stored in the capacitor is $E_{oss}$ (equals to $E_{oss,channel}$), thus the capacitive charge induced loss is calculated by:

$$E_{oss,induced} = E_{total,oss} - E_{oss} = V_{dc} Q_{oss} - \int_0^{V_{dc}} C_{oss}(v) v dv \tag{21}.$$

If the output capacitor is linear, i.e. not varying with the voltage, the capacitive charge induced loss will equal to the energy stored in the capacitor. However, owning to the nonlinearity, they are not equal. Equation (21) must be used to accurately quantify the loss.

► **Voltage-current overlap loss, $E_{overlap}$**

The rest of the energy dissipation is caused by the overlap of drain-to-source voltage and current.

The total turn-on loss ($E_{on}$) is separated into four parts by their originating source:

$$E_{on} = E_{rr} + E_{oss,channel} + E_{oss,induced} + E_{overlap} \tag{22}.$$

The loss mechanisms and calculation is summarized in TABLE I.

**TABLE I. ORIGINS OF TURN-ON LOSS AND THEIR PROPERTIES**

| | **Origin** | **Dissipated in** | **Related equations** |
|---|---|---|---|
| $E_{rr}$ | Reverse recovery effect of body diode of commutating switch | Both switches | (18) |
| $E_{oss,channel}$ | Capacitive energy of switching switch | Switching switch | (19) |
| $E_{oss,induced}$ | Capacitive charge of commutating switch | Both switch | (21) |
| $E_{overlap}$ | Overlap of voltage and current during switching switch turn-on | Switching switch | (27) |

### *2.3.2 Analysis of Turn-on Transients Using Measured Waveforms*

Fig. 2-8 and Fig. 2-9 show the waveforms during bottom device turn-on in bottom-device-switching tests and top device turn-on in top-device-switching tests, prospectively. The switching current is 36 A and voltage is 540 V. The corresponding test schematics are shown in Fig. 2-10.

The waveforms in Fig. 2-8 shows the turn-on drain-to-source voltage ($V_{bottom1}$) and current ($I_{bottom1}$) of the switching switch (bottom switch). $I_{bottom1}$ rises as the gate signal is applied. When $I_{bottom1}$ reaches load current, the same instant when $I_{bottom2}$ in Fig. 2-9 reaches zero, $V_{bottom1}$ starts to fall. The energy dissipated in the bottom device ($E_{oss,channel}$ cannot be measured by the setup) is calculated by:

$$E_1 = \int V_{bottom1}(t) I_{bottom1}(t) dt \tag{23}.$$

The integral interval should last until the ringing on voltage and current is well damped.

As is discussed in previous section (section 2.3.1), it is necessary to measure the current and voltage of the commutating device during device turn-on to get a complete loss characterization. This is done by the top-device-switching test (the schematic is shown in Fig. 2-10 (b)), and the waveforms are captured during top device turn-on .The energy flows into the commutating device is calculated by:

$$E_2 = \int V_{bottom2}(t) I_{bottom2}(t) dt \tag{24},$$

where waveforms of $V_{bottom2}$ and $I_{bottom2}$ are depicted in Fig. 2-9. The waveforms represents the drain-to-source voltage and current of commutating switch ($S_{bottom}$ in Fig. 2-10 (b)) during turn-on of switching switch ($S_{top}$ in Fig. 2-10 (b)), which resembles the voltage and current of $S_{top}$ in the

bottom-device-switching test (Fig. 2-10 (a)). Part of $E_2$ is stored in the output capacitor of $S_{top}$, because $S_{top}$ is blocking the dc bus voltage. The other part is dissipated. The stored energy equals to $E_{oss}$ (calculated in (19)).

Considering the capacitive energy of switching switch dissipated but not measured, and the energy stored in output capacitor of commutating, the total energy dissipated during device turn-on is:

$$E_{on} = E_1 + E_{oss,channel} + E_2 - E_{oss} = E_1 + E_2 \quad (25).$$

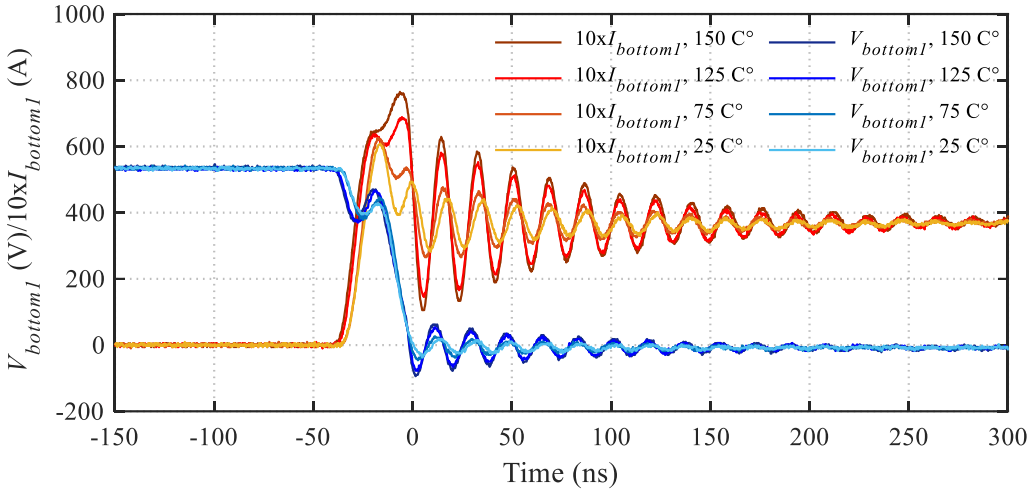



**Fig. 2-8. Bottom-device-switching test, bottom device turns on at 540 V, 36 A.**

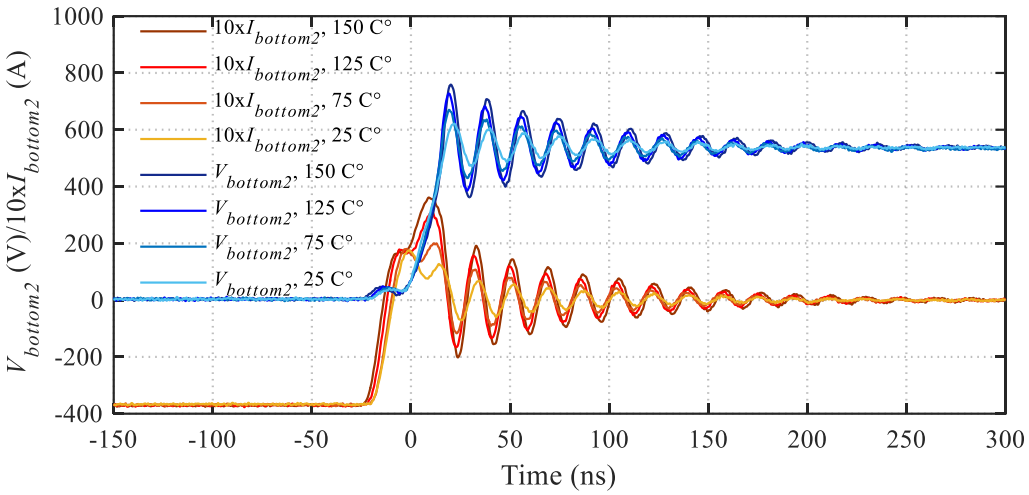
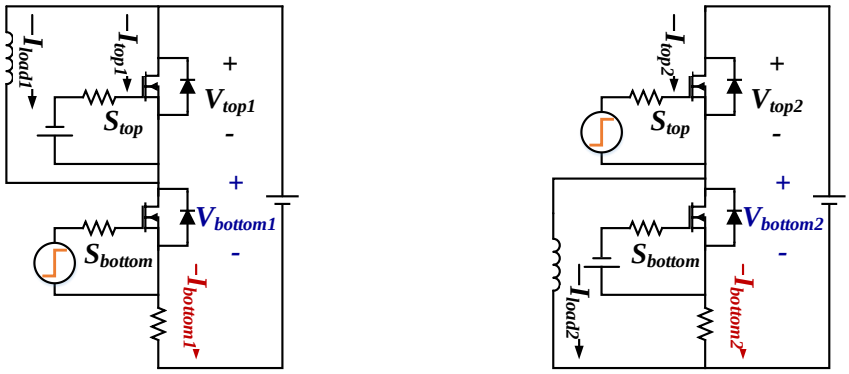



**Fig. 2-9. Top-device-switching test, top device turns on at 540 V, 36 A.**




**(a)** **(b)**

**Fig. 2-10. (a) Test setup for Fig. 2-8. (b) Test setup for Fig. 2-9.**

Furthermore, the measured waveforms are used to quantify the four types of loss described in section 2.3.1, namely, $E_{rr}$, $E_{oss,channel}$, $E_{oss,induced}$ and $E_{overlap}$. The total charge ($Q_{total}$) is calculated using the measured current in top-device-switching test. An example is depicted in Fig. 2-11. The $Q_{total}$ is calculated as:

$$Q_{total} = \int_{t_1}^{t_2} I_{bottom2}(t)\,dt \tag{26}.$$

Using (16) and (17), the output capacitor charge $Q_{oss}$ and reverse recovery charge $Q_{rr}$ are calculated accordingly. With this information and (18), (19) and (21), $E_{rr}$, $E_{oss,channel}$ and $E_{oss,induced}$ are calculated. The $E_{overlap}$ is expressed by:

$$\begin{aligned} E_{overlap} &= E_{on} - E_{rr} - E_{oss,channel} - E_{oss,induced} \\ &= E_1 + E_2 - V_{dc}Q_{rr} - \int_0^{V_{dc}} C_{oss}(v)vdv - (V_{dc}Q_{oss} - \int_0^{V_{dc}} C_{oss}(v)vdv) \\ &= E_1 + E_2 - V_{dc}(Q_{rr} + Q_{oss}) = E_1 + E_2 - V_{dc}\int_{t_1}^{t_2} I_{bottom2}(t)dt \end{aligned} \quad (27).$$

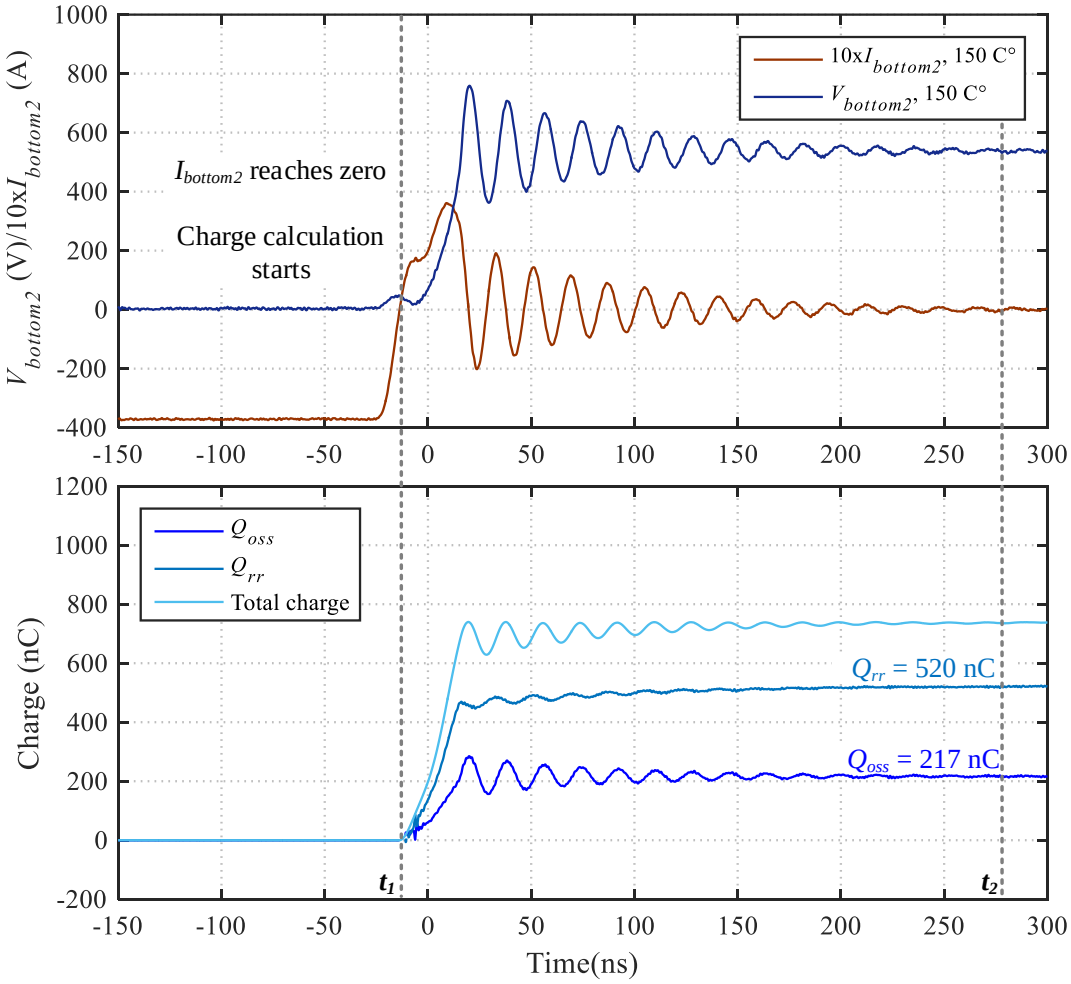
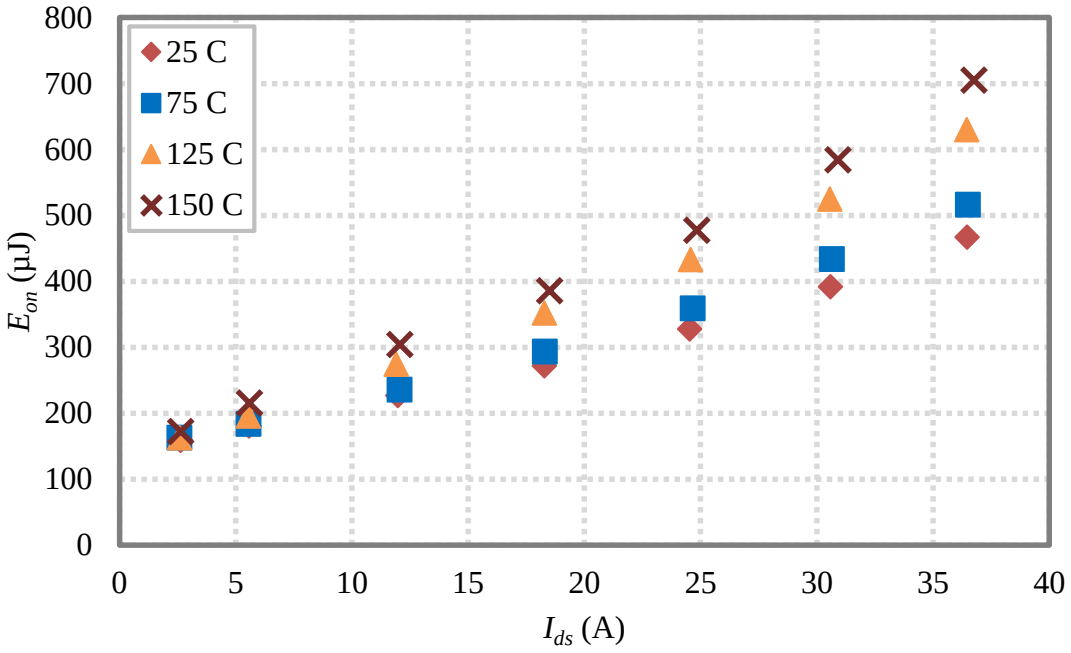
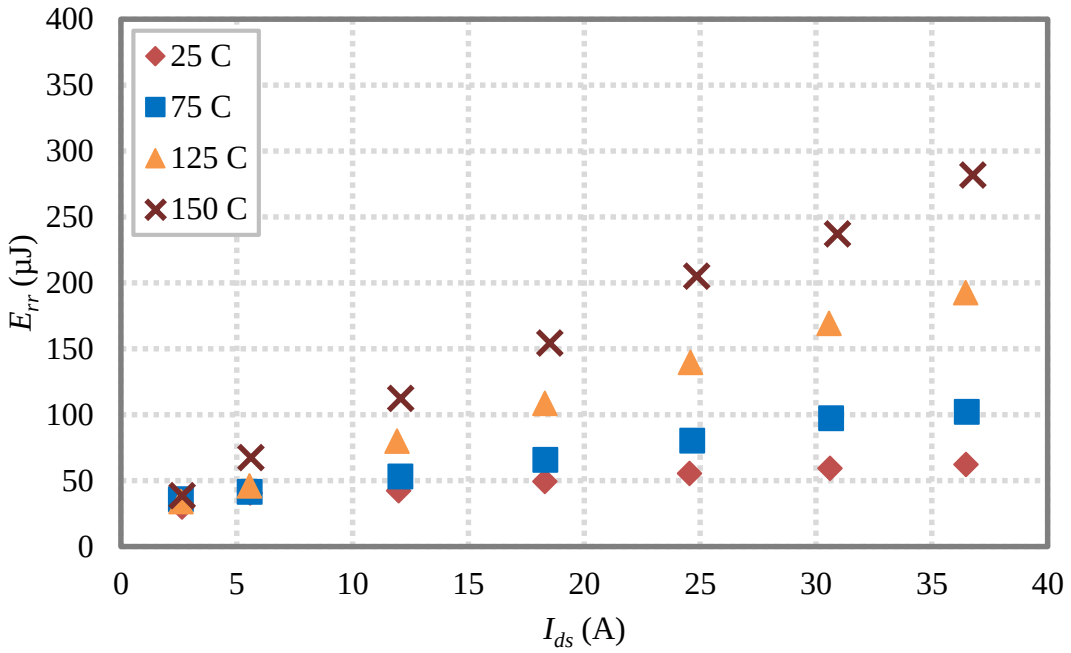



**Fig. 2-11. Waveforms demonstrating the calculation of $Q_{rr}$ and $Q_{oss}$.**

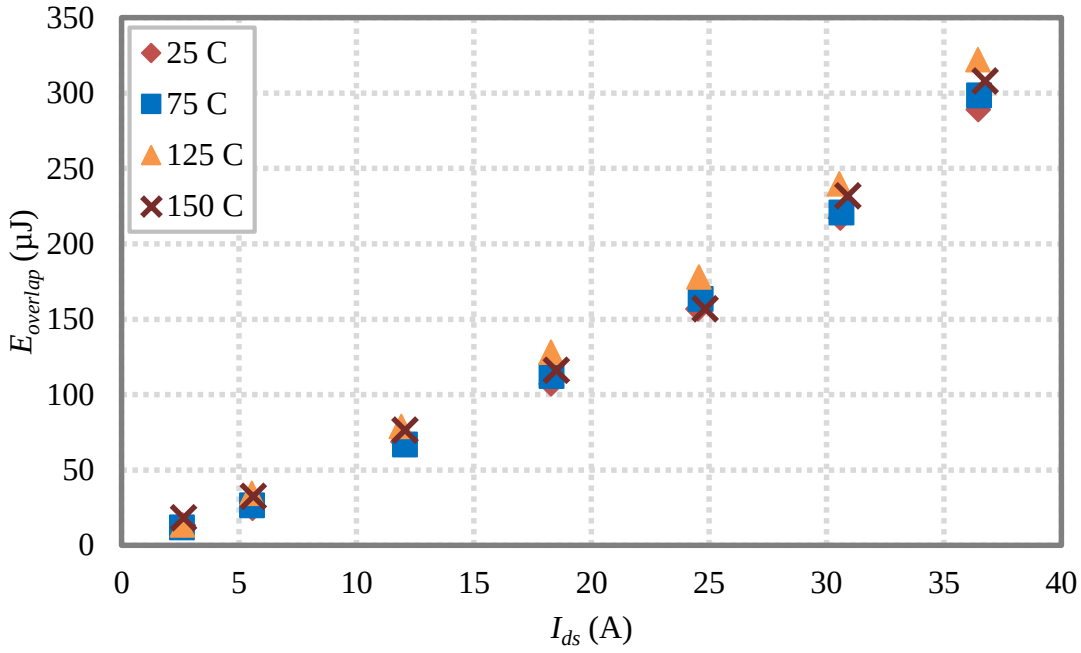
The tests are conducted under various current levels and device temperatures. The results of turn-on energy ($E_{on}$, calculated by (25)), the reverse recovery loss ($E_{rr}$, calculated by (18)) and voltage-current overlap loss ($E_{overlap}$, calculated by (27)) are summarized in Fig. 2-12 (a), (b) and (c) respectively. The $E_{oss,channel}$ (calculated by (19)) and $E_{oss,induced}$ (calculated by (21)) are constant and not depicted. They are 41.4 µJ and 74.4 µJ respectively (note that $E_{oss,induced} > E_{oss,channel}$) for the device under test (CREE C2M0025120D).




**(a)**




**(b)**




**(c)**

**Fig. 2-12. Energy dissipation related to turn-on of C2M0025120D. (a) Turn-on loss, $E_{on}$. (b) Reverse recovery loss, $E_{rr}$. (c) Voltage-current overlap loss, $E_{overlap}$.**

As temperatures rises, the turn-on loss $E_{on}$ increases. As is observed from Fig. 2-12 (b) and (c), major loss increase is from aggravated $E_{rr}$. The $E_{overlap}$ stays constant at elevated temperatures. This matches with the waveforms in Fig. 2-8 and Fig. 2-9 that the *di/dt* and *dv/dt* stays constant but the amplitude of the "current bump" increases as temperature increases. In [9, 59], it is assumed that the voltage-current overlap loss is determined by gate speed and is independent of other factors (temperature, reverse recovery charge, etc.), an assumption served as foundation of most piecewise linear switching model [9, 59]. This observation backs the switching models in aforementioned literatures.

The energy breakdown of the turn-on loss of the DUT at 150 ºC is depicted in Fig. 2-13. The $E_{rr}$ and $E_{overlap}$ dominate the turn-on energy.

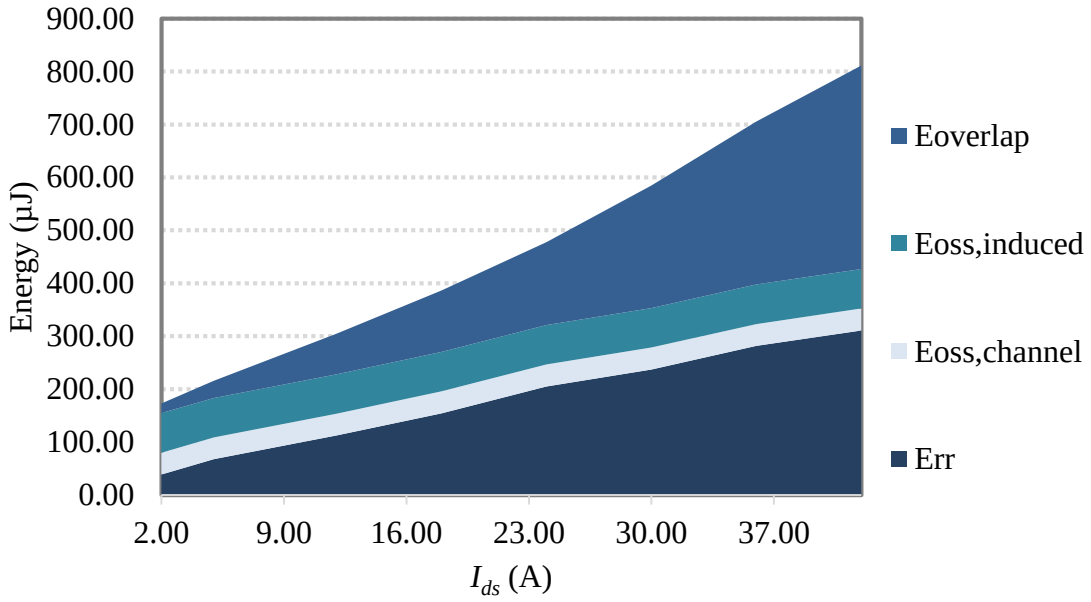



**Fig. 2-13. Turn-on energy breakdown of C2M0025120D, tested with 540 V voltage and 150 Cº temperature.**

Furthermore, the energy dissipated in the commutating switch ($E_{commutating}$) is nontrivial. It is expressed as:

$$E_{commutating} = E_2 - E_{oss} \quad (28),$$

where $E_2$ is calculated by (24) and $E_{oss}$ is calculated by (19). It is 4 % to 12 % of the total turn-on loss for phase leg consisting of CREE C2M0025120D MOSFETs (depicted in Fig. 2-14). For C2M0040120D devices, it is up to 13 %. For C2M0080120D MOSFETs, it is up to 19 %. As $E_{commutating}$ can only be directly measured by the top-device-switching test, it is necessary to conduct it to get an accurate and complete result.

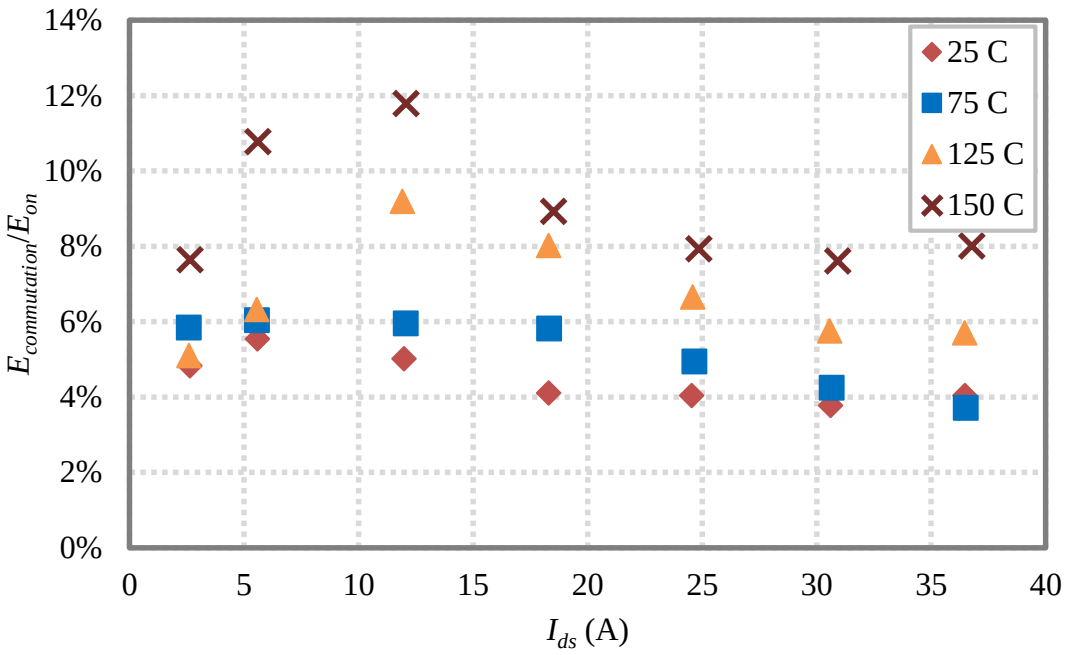



**Fig. 2-14. The percentage of $E_{communtation}$ over $E_{on}$ vs. current. The results of C2M0025120D device is shown here.**

### *2.3.3 Analysis of Switching Transients during Device Turn-off*

To measure the turn-off loss, both bottom-device-switching test and top-device-switching test are conducted, and the measured waveforms are shown in Fig. 2-15 and Fig. 2-16 respectively.

The bottom-device-switching tests measure the energy related to turn-off of the switching switch. The energy consists of the energy dissipated owning to voltage-current overlap and the energy stored in the output capacitor of switching device. The turn-off loss $E_{off}$ is calculated by:

$$E_{off} = \int V_{bottom3}(t) I_{bottom3}(t) dt - E_{oss} \quad (29),$$

where $V_{bottom3}$ and $I_{bottom3}$ are shown in Fig. 2-15, and $E_{oss}$ is calculated by (19). The measured $E_{off}$ under various temperatures and current levels are summarized in Fig. 2-18. The temperature does not have big influence on turn-off loss.

The top-device-switching tests measure the energy returned from the output capacitor of the commutating device to the circuit (load inductor or source), as the voltage and current have opposite polarity during the transient (shown in Fig. 2-16). The energy was stored during the turn-on of switching switch (described in section 2.3.1). This test can be used to check if the probes are calibrated and deskewed properly, as the returned energy should be equal to $E_{oss}$.

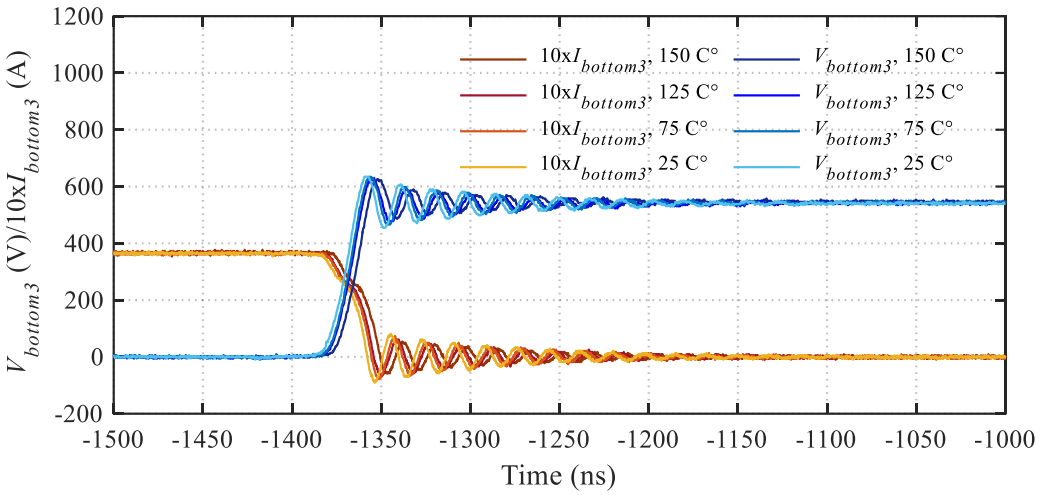



**Fig. 2-15. Bottom-device-switching test, bottom device turns off at 540 V, 36 A.**

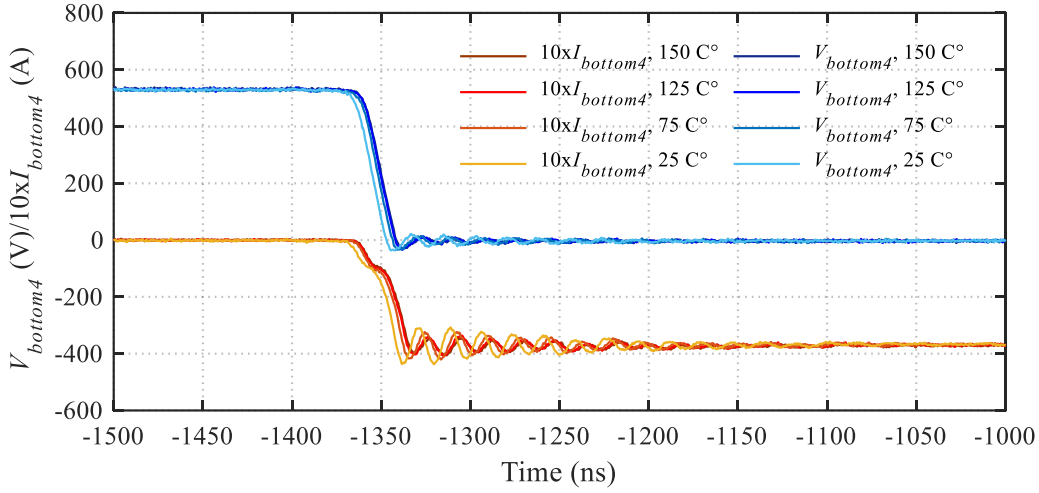
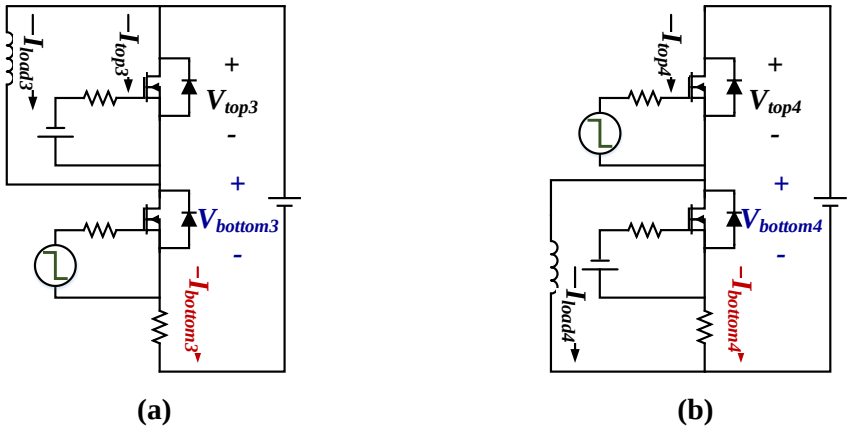



**Fig. 2-16. Top-device-switching test, bottom device turns off at 540 V, 36 A.**




**(a)** **(b)**

**Fig. 2-17. (a) Test setup for Fig. 2-15. (b) Test setup for Fig. 2-16.**

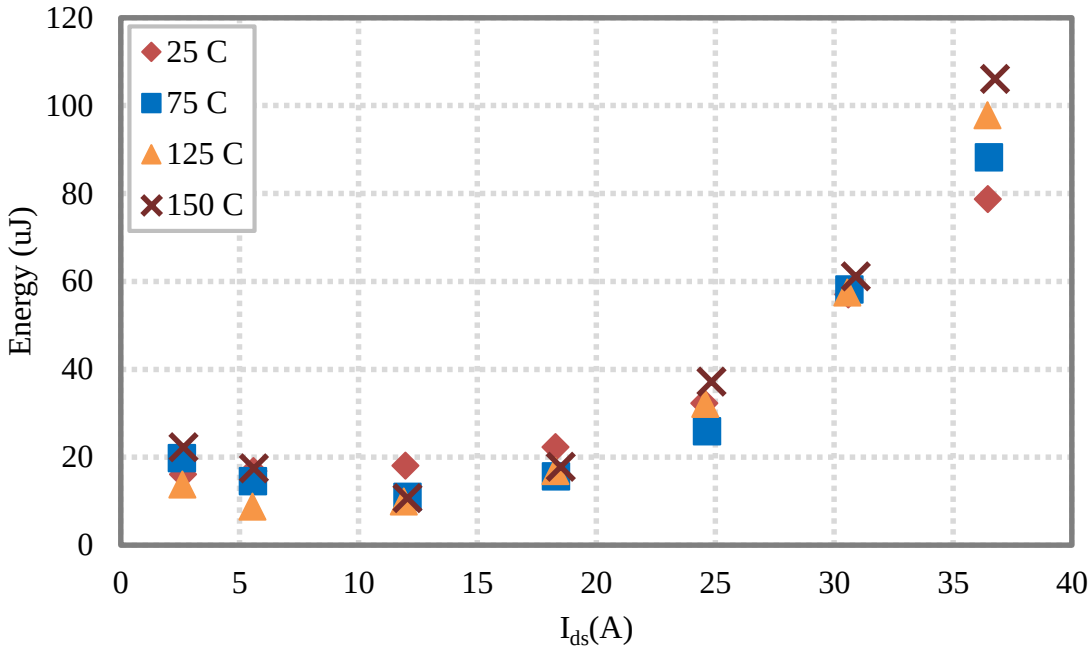
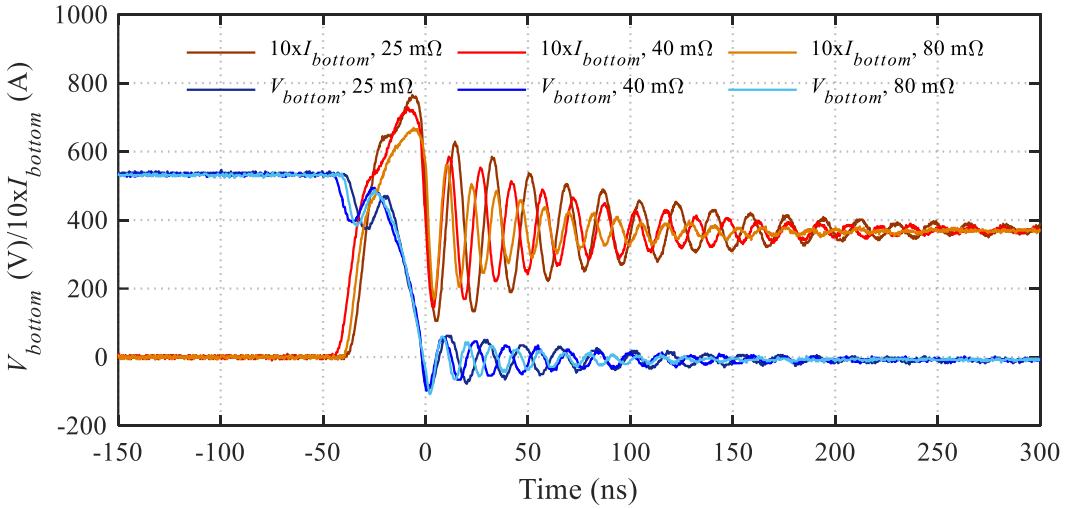



**Fig. 2-18. Turn-off loss of C2M0025120D, $E_{off}$.**

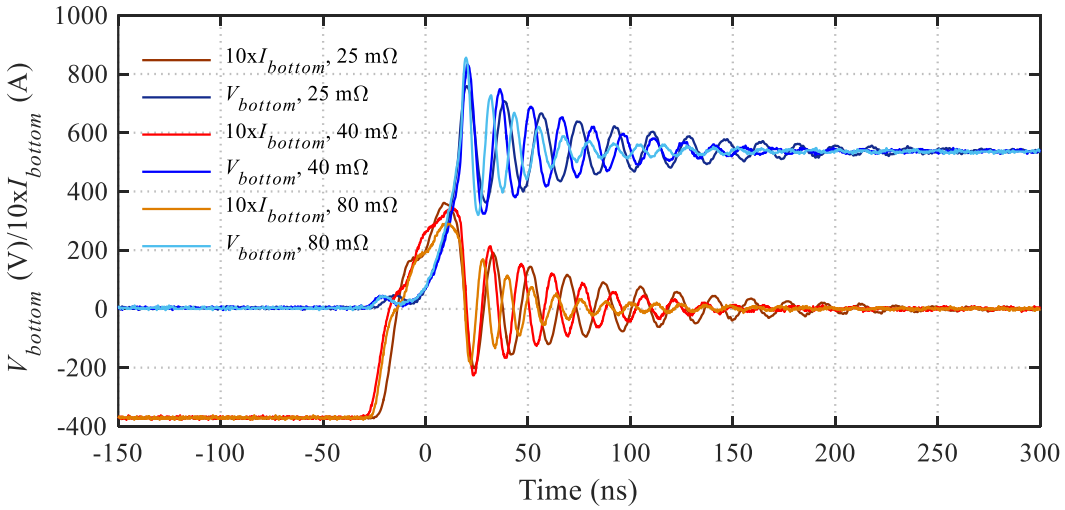
## 2.4 Comparison between Devices with Different Die Sizes

In this section, switching waveforms of MOSFETs with different die sizes (25 mΩ, 40 mΩ and 80 mΩ) are compared. Their part numbers are C2M0025120D, C2M0040120D and C2M0080120D respectively. Fig. 2-19 shows the transient waveforms of the devices under test at 36 A, 540 V at 150 °C. Despite of different die sizes and junction capacitance, their *di/dt* and *dv/dt* are similar. In addition, the turn-on loss ($E_{on}$) and reverse recovery loss ($E_{rr}$) are depicted in Fig. 2-20 (a) and (b). Although 25 mΩ device (of the largest die size) is the lossiest at current levels below 20 A, 40 mΩ device dissipates the most energy at higher current owning to its highest reverse recovery induced loss (demonstrated in Fig. 2-20 (b)). One explanation to this is that,

besides the aforementioned factors, the reverse recovery is related with the total number of active device cells (active die size) as well as the current density in each cell. This observation indicates that larger die size (or junction capacitance) does not necessarily associate with higher switching loss. Device candidates should be carefully tested and/or modeled when designing converters.

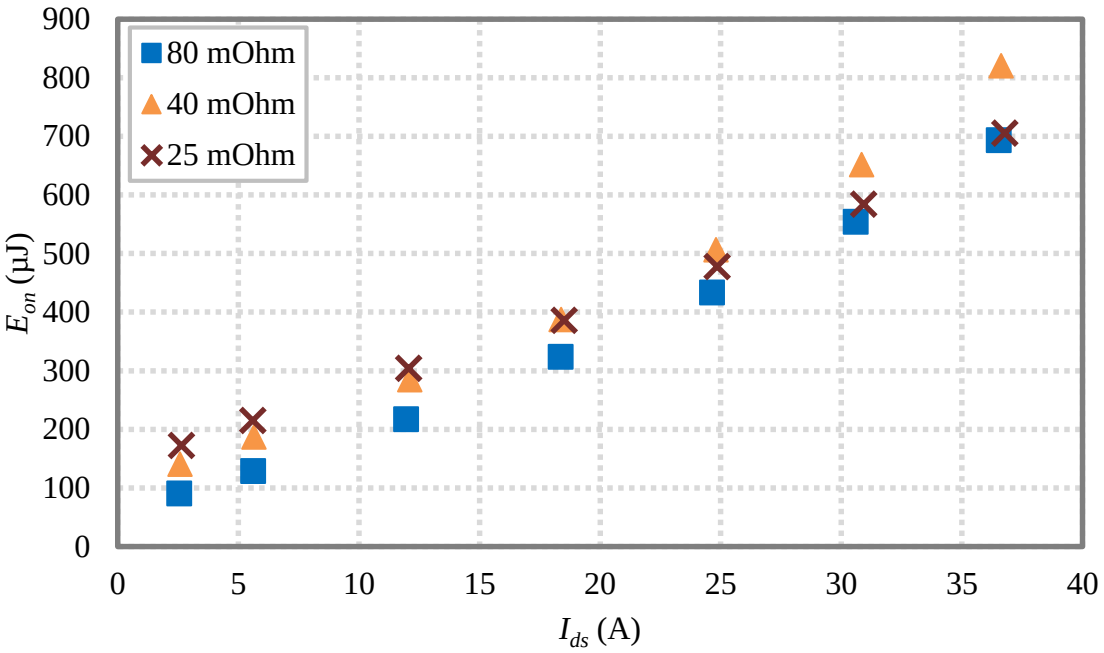



**(a)**

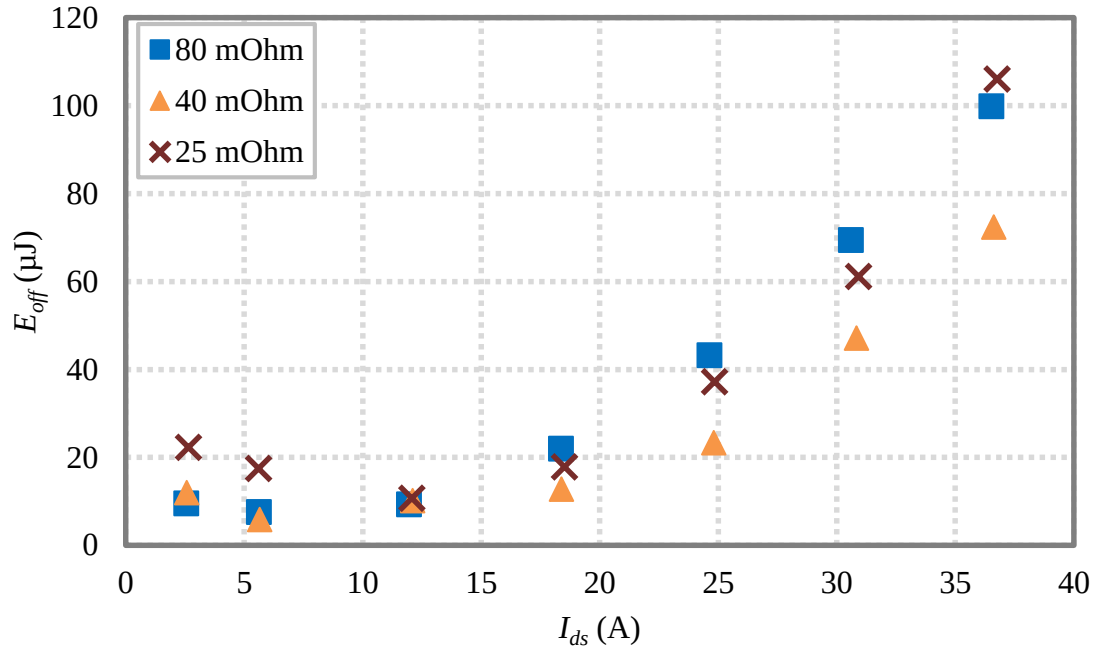



**(b)**

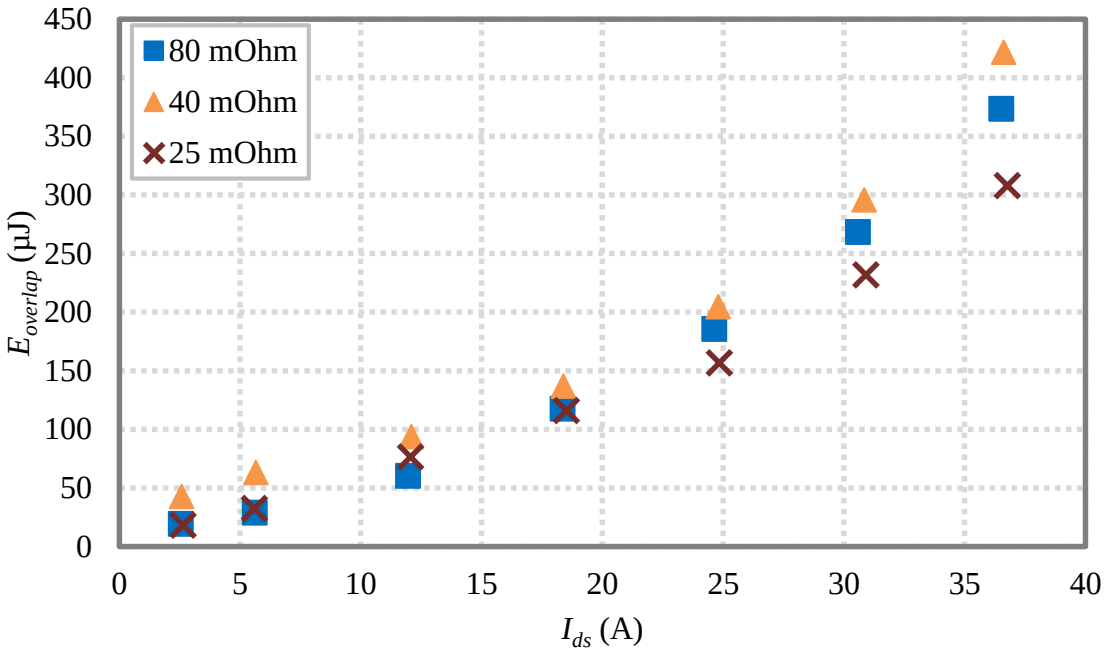
**Fig. 2-19. Voltage and current waveforms of devices with different die sizes (C2M0025120D, C2M0040120D and C2M0080120D) under 150 C°. (a) Bottom-device-switching test, bottom device turn-on. (b) Top-device-switching test, top device turn-on.**


80 mOhm
40 mOhm
25 mOhm
$E_{on}$ (µJ)
$I_{ds}$ (A)
0
100
200
300
400
500
600
700
800
900
0
5
10
15
20
25
30
35
40

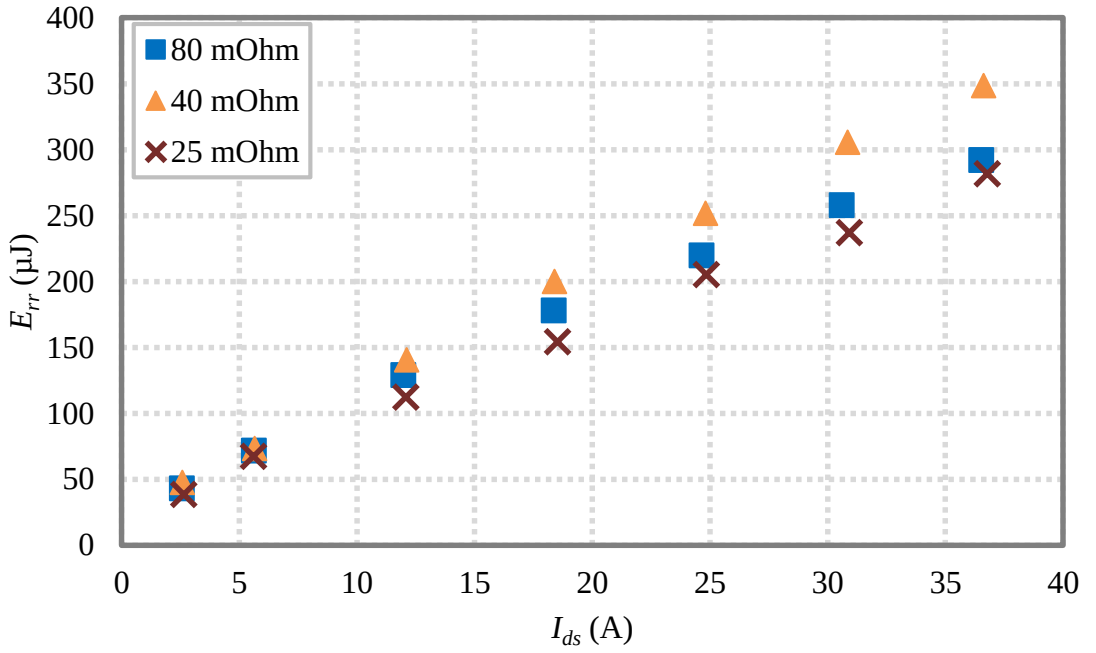
**(a)**


80 mOhm
40 mOhm
25 mOhm
$E_{off}$ (µJ)
$I_{ds}$ (A)
0
20
40
60
80
100
120
0
5
10
15
20
25
30
35
40

**(b)**




**(c)**

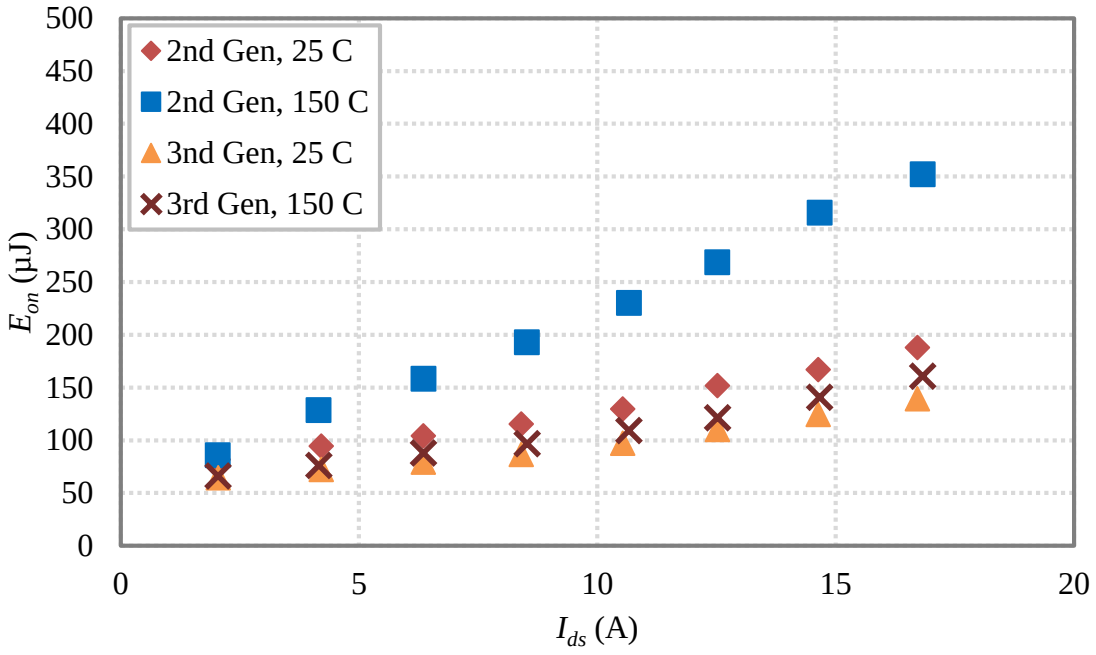



**(d)**

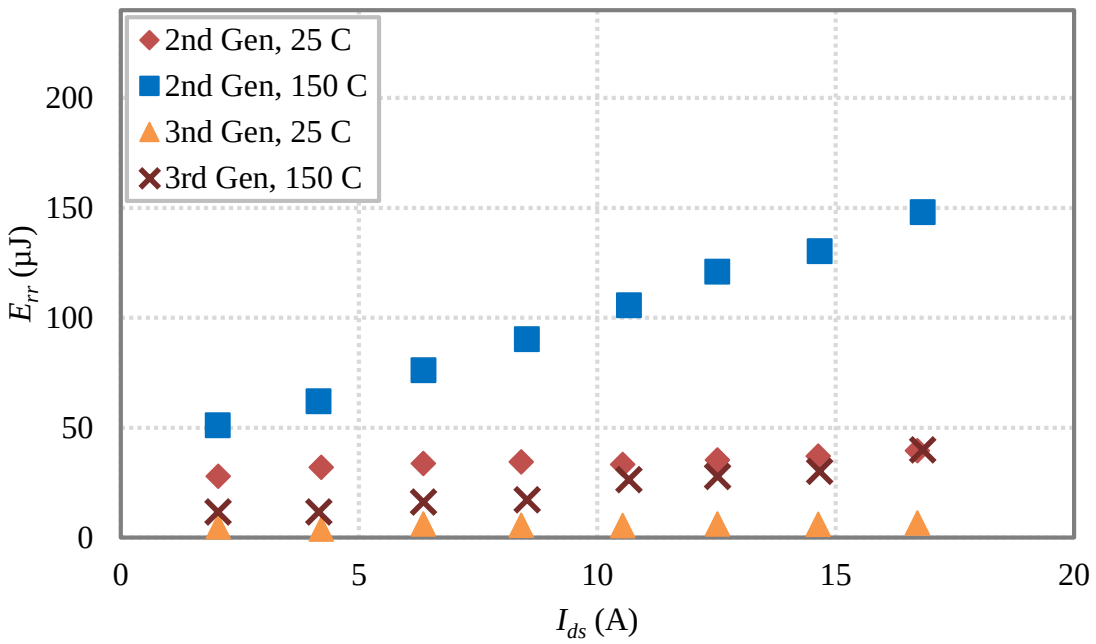
**Fig. 2-20. (a) Turn-on loss of the DUTs at 150 °C, $E_{on}$. (b) Turn-off loss of the DUTs at 150 °C, $E_{off}$. (b) Voltage-current overlap loss of of the DUTs at 150 °C, $E_{overlap}$. (b) Revere recovery induced loss of DUTs at 150 °C, $E_{rr}$.**

## 2.5 Comparison between 2nd and 3rd Generation Devices

A comparison of Wolfspeed's 2nd generation device (C2M0080120D) and 3rd generation device (C3M0065090D) is presented in this section. The two DUTs are of similar die size and junction capacitance. However, they perform differently at high junction temperature. The difference lies in the reverse recovery induced loss, which is depicted in Fig. 2-21 (b). Despite comparable augmentation ratio of reverse recovery induced loss, the 3rd generation device enjoys minute reverse recovery charge partially thanks to its thinner n- drift layer (though it has lower voltage rating). For applications that requires blocking voltage less than 600 V, e.g. 540 V dc bus voltage in modern aircrafts, the third generation device is a better fit than its 2nd generation counterpart.




**(a)**




**(b)**

**Fig. 2-21. Comparison between CREE 2nd and 3rd generation devices. (a) Turn-on loss of 2nd and 3rd generation device, $E_{on}$. (b) Revere recovery induced loss of 2nd and 3rd generation devices, $E_{rr}$.**

## 2.6 Chapter Conclusion

This work uses two tests, namely, top-device-switching and bottom-device-switching tests, to characterize switching of MOSFETs accurately. Its necessity is backed by theoretical analysis and experimental results (without conducting top-device-switching the test, an error up to 19 % was found). Detailed data processing is presented, where partitioning turn-on loss is in focus. The results show that, with the same driving circuit, voltage-current overlap induced loss does not change much when junction temperature changes while reverse recovery induced loss increases at elevated temperature. The turn-on loss partition and analysis suggest that modeling turn-on loss should be partitioned into three segments, namely, voltage-current overlap modeling, capacitive

charge modeling and reverse recovery modeling. Furthermore, the tests have been conducted in a wide temperature range (25 °C ~ 150 °C) with different MOSFETs (various die sizes and technologies). The testing results show the complexity of relating die size to switching loss. In addition, the comparison between 2$^{nd}$ and 3$^{rd}$ generation devices demonstrates the superiority of 3$^{rd}$ generation devices.

# Chapter 3. Nominal Power Maximization of Power Converters – An Active Front-End Converter Case Study

## 3.1 Chapter Introduction and Prior Art

This chapter focuses on design of modular active front-end converters that mount to racks and can work in parallel to allow scalability. In this design, converter form factor is fixed by dimensions of chassis racks. Furthermore, thermal management and electromagnetic interference (EMI) are of great importance to system integration, which renders a set of electrical and mechanical design constraints. Although this scenario is frequently seen in commercial converter design [115, 116], few literatures talk about design approach considering all the constraints while optimizing the performance. This chapter presents a novel approach for designing form-factor-constrained power electronics converters. The design objective is to maximize nominal power of the power supply unit under the constraints of form-factor, heat dissipation, EMI and cooling. Designing for maximum nominal power unveils the potential of modular power converters given the practical limitations and leads to optimal system design. Specifically, a three-phase active front-end converter for aerospace applications is under investigation. The system schematic is shown in Fig. 3-1, and the specifications and design constrains are listed in TABLE II. The bi-level integrated system synthesis (BLPP) introduced in Chapter 1 is used to frame the design procedure.

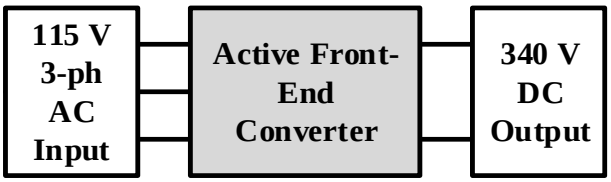



**Fig. 3-1. System under investigation. The active front-end converter converts 115 Vac variables frequency three-phase input to 340 Vdc output (internal output, not connected to any bus).**

**TABLE II. SINGLE-PHASE AFE CONVERTER TARGETS AND SPECIFICATIONS**

| Items | Target/Specification |
|---|---|
| Input Voltage | Single phase 115 Vac |
| Input Frequency | 360 Hz ~ 800 Hz |
| Output Voltage | 340 V |
| Output Power | TBD |
| Loss budget | 18 W |
| Form Factor | 35 $in^2$ x 1 in |
| Cooling | Free Convection Air-Cooling |
| Power Quality Standard | DO-160E |
| EMI Standard | DO-160E |

Besides converter design, a control method is proposed to improve input power quality for the constructed prototype (a Vienna rectifier) in order to meet power quality standard in question. The power quality issue caused by junction capacitors of diodes and active switches in Vienna rectifiers has been reported in [33, 117]. [33] claims that charging and discharging of junction capacitors results in "turn-off delay" in phase leg output voltage, and it distorts the input current. Both literatures use a feedforward loop to compensate the delay time, but with different models for delay time calculation. Ref. [33] uses a numerical model extracted from experimental observation. Although the model is accurate, its extraction is time-consuming. On the other hand, [117] derives an analytical model based on the assumption that voltage rising slope is constant during turn-off.

However, as it will be shown in this chapter, the aforementioned assumption is inaccurate owning to non-linear junction capacitance, and the model should be modified. In this chapter, a delay time model based on datasheet information is developed, upon which the control method for power quality improvement is proposed and experimentally verified.

## 3.2 Nominal Power Maximization for Form-Factor-Constrained Converter

### *3.2.1 Bi-level programming problem (BLPP) for Nominal Power Maximization*

The nominal power maximization is an optimization problem, of which the typical formulation is

$$\min/\max F(x) \tag{30},$$

$$\text{s.t. } g(x) \le 0 \tag{31},$$

where $F(x) = [F_1(x) \quad \cdots \quad F_z(x)]^T$ are the objective functions, $x = [x_1 \quad \cdots \quad x_i \quad \cdots \quad x_n]^T$ is the design vector consisting of the design variables, and $g(x) = [g_1(x) \quad \cdots \quad g_n(x)]^T$ represent design constraints [7]. Using a single-level optimization framework (framework depicted in Fig. 1-6), the nominal power maximization problem is described as:

$$\max P_{\text{nominal}}(x) \tag{32},$$

$$\text{s.t. } g(x) \le 0 \tag{33}.$$

In the above expression, $P_{nominal}(x)$ is the nominal power to be maximized, and it is a function of vector $x$, which consists of design variables in a converter, e.g. topology, switching frequency,

component selection, etc. *g(x)* stands for the design constraints such as form factor, loss budget and EMI standard. Despite the simple form, it is hard to formulate this maximization problem owning to the complication of linking converter design vatiables to its nominal power. Therefore, this work proposes to translate the problem into a BLPP [83] problem of which the upper-level optimization is formulated as:

$$\max P_{\text{nominal}}(x_{upper}, y_{lower}) = p_{\text{nominal}} \text{ where } x_{upper} = p_{\text{nominal}} \quad (34),$$

$$\text{s.t. } G(x_{upper}, y_{lower}) = [P_{loss}(x_{upper}, y_{lower}) - 18 \quad A_{converter}(x_{upper}, y_{lower}) - 35]^T \le 0 \quad (35),$$

where the objective function, nominal power, equals to the upper-level design variable ($x_{upper}$), $p_{nominal}$, and $y_{lower}$ is defined by the lower-level optimization described below:

$$\min f(x_{upper}, z) = [P_{loss}(x_{upper}, z) \quad A_{converter}(x_{upper}, z)]^T \quad (36),$$

$$\text{s.t. } g(x_{upper}, z) \le 0 \quad (37),$$

$$y_{lower} \in \arg\min\{f(x_{upper}, z) = [P_{loss}(x_{upper}, z) \quad V_{converter}(x_{upper}, z)]^T : g(x_{upper}, z)\} \quad (38),$$

where $z$ is the design vector, $P_{loss}$ represents converter loss, $A_{converter}$ represents converter area and $g(x_{upper}, z)$ represents all design constraints except loss and form factor limitations. The solution to the lower-level problem is $y_{lower}$. The lower-level optimization, per se, is a loss-size multi-optimization problem, which have been widely discussed and used in power converter design [5, 24, 31]. Multiple Pareto optimal designs, i.e. $y_{lower}$ consisting of a group of design vectors that leads to Pareto optimal $f(x_{upper}, z)$, are expected. The bi-level nominal power maximization problem is visualized in Fig. 3-2.

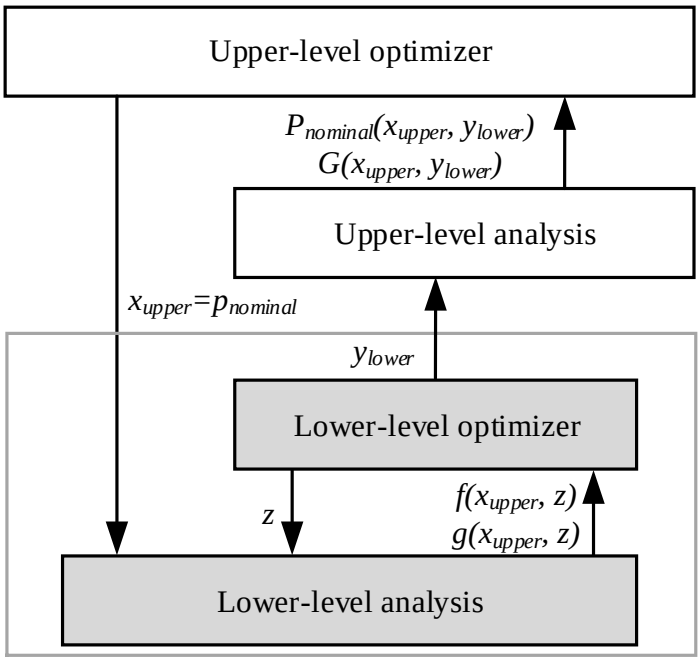



**Fig. 3-2. Bi-level optimization framework for nominal power maximization.**

### *3.2.2 BLPP for Converter Loss-Size Multi-Objective Optimization*

Instead of single-level optimization framework, this work applies BLPP to the loss-size optimization. The loss-size optimization problem is decomposed into converter-level (upper-level) and component-level (lower-level) so that all components are optimized locally and concurrently, and the framework is depicted in Fig. 3-3. The converter-level optimization problem is formulated as:

$$\min f_{converter}(p_{nominal}, x_{converter}, y_{comp}) = [\sum_{i=1}^{n} P_{loss,i}(p_{nominal}, x_{converter}, y_{comp,i}) \quad \sum_{i=1}^{n} A_i(p_{nominal}, x_{converter}, y_{comp,i})]^T \tag{39},$$

$$\text{s.t. } g_{converter}(p_{nominal}, x_{converter}, y_{comp}) \le 0 \tag{40},$$

where $x_{converter}$ is the converter-level design vector consists of switching frequency, EMI filter parameters (structure, inductance and capacitance), $P_{loss,i}$ represents loss, $A_i$ represents area of the i$^{th}$ component and $g_{converter}(p_{nominal}, x_{converter}, y_{comp})$ represents all design constraints except loss and form factor limitations.

Each component-level optimization is formulated as:

$$\min f_{comp,i}(w_{converter}, z_i) = [P_{loss,i}(w_{converter}, z_i) \quad A_i(w_{converter}, z_i)]^T \tag{41},$$

$$\text{s.t. } g_{comp,i}(w_{converter}, z_i) \le 0 \tag{42},$$

$$y_{lower,i} \in \arg\min\{ f_{comp,i}(w_{converter}, z_i) = [P_{loss,i}(w_{converter}, z_i) \quad A_i(w_{converter}, z_i)]^T : g_{comp,i}(w_{converter}, z_i)\} \tag{43},$$

where $w_{converter}$ consists of $x_{converter}$ and necessary parameters that are simulated by converter-level analyzer, e.g. current flowing through components, $z_i$ is the component-level design vector and $g_{comp,i}(w_{converter}, z_i)$ represents design constraints of the i$^{th}$ component.

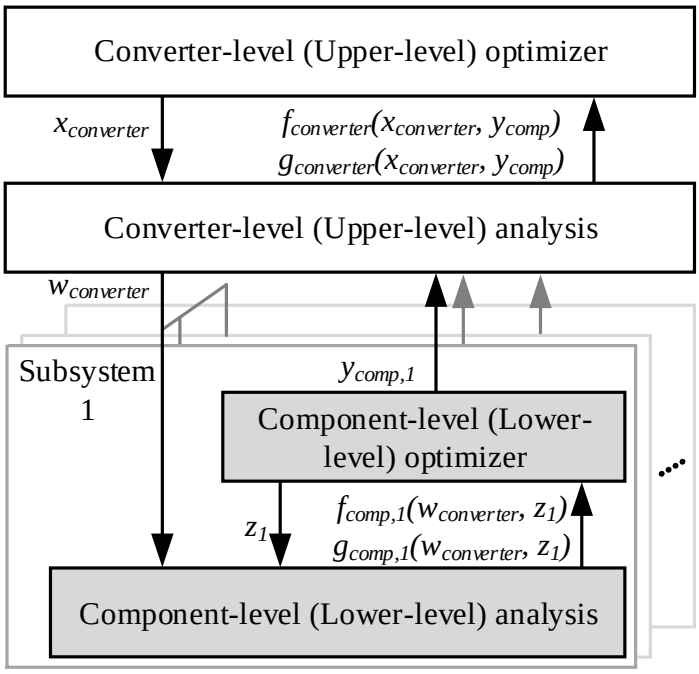



**Fig. 3-3. BLPP for converter loss-size multi-objective optimization.**

### *3.2.3 Overall Optimization Framework and Implementation*

Combining the aforementioned optimization frameworks renders the overall framework for nominal power maximization, and it is depicted in Fig. 3-4. Two BLPP problems are cascaded. The upper section of Fig. 3-4 depicts the design flow while the lower depicts expected results. The optimization results of component-level design are Pareto fronts demonstrating the loss-size tradeoff of the specific component with certain converter-level parameters. Integrating the Pareto optimal component designs renders Pareto optimal converter design. The former is a necessary but not sufficient condition for the latter. This is proven by contradiction. Assume that a Pareto optimal converter design is a result of integrating component designs, and at least one of the component designs is not Pareto optimal. In this example, we take loss and size as the two performance indices. A better converter design with smaller size and less loss would result by replacing the non-Pareto-optimal component designs that are smaller and renders less loss (this replacement is always valid

since the component is not Pareto optimal and there is always designs that renders both smaller size and less loss). The resultant better converter design contradicts with the assumption that the previous converter design is Pareto optimal. The contradiction proves that the higher-level Pareto optimal design is an integration of lower-level designs that are Pareto optimal. Therefore, when integrating lower-level designs, system designers only need to consider Pareto optimal designs.

The nominal power optimizer checks if the Pareto optimal converter designs comply with the form factor and loss budget constraints, and the maximal nominal power and final valid designs are found accordingly. For search algorithms, direct search is used.

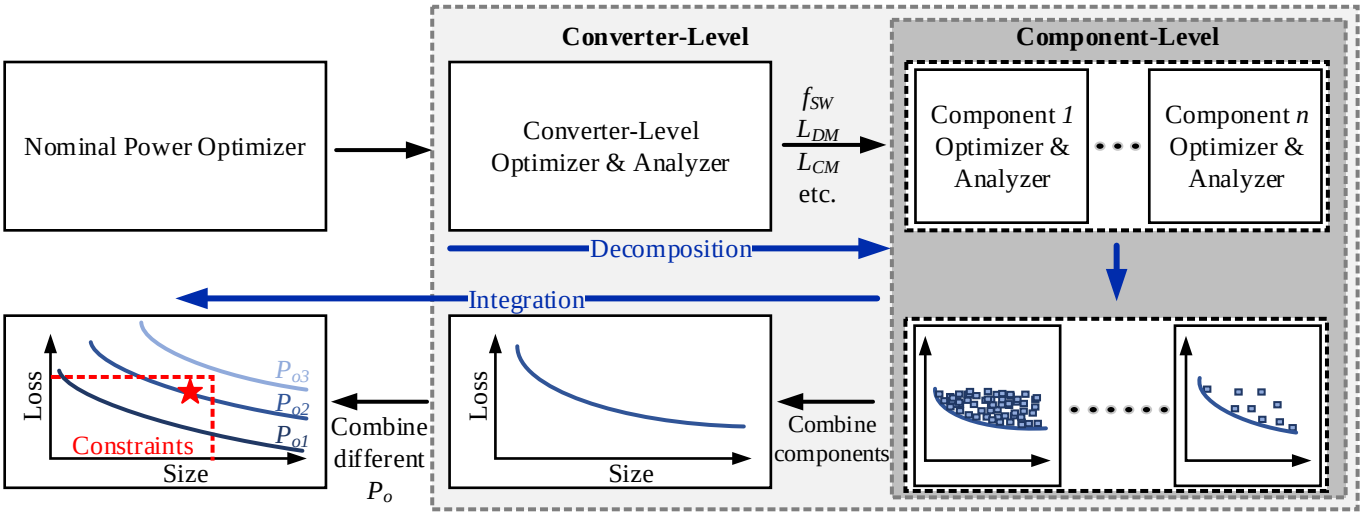



**Fig. 3-4. Overall optimization framework for and expected results of nominal power maximization.**

## 3.3 Design Procedure, Key Models and Design Results

Detailed converter design procedures incorporating the aforementioned optimization framework is depicted in Fig. 3-5. The design consists of three levels: nominal power maximization loop, converter level design and component level design. The nominal power maximization loop renders nominal power based on which the converter level and component level

design are conducted. The design variables and key models in converter level and component level designs are detailed in this section.

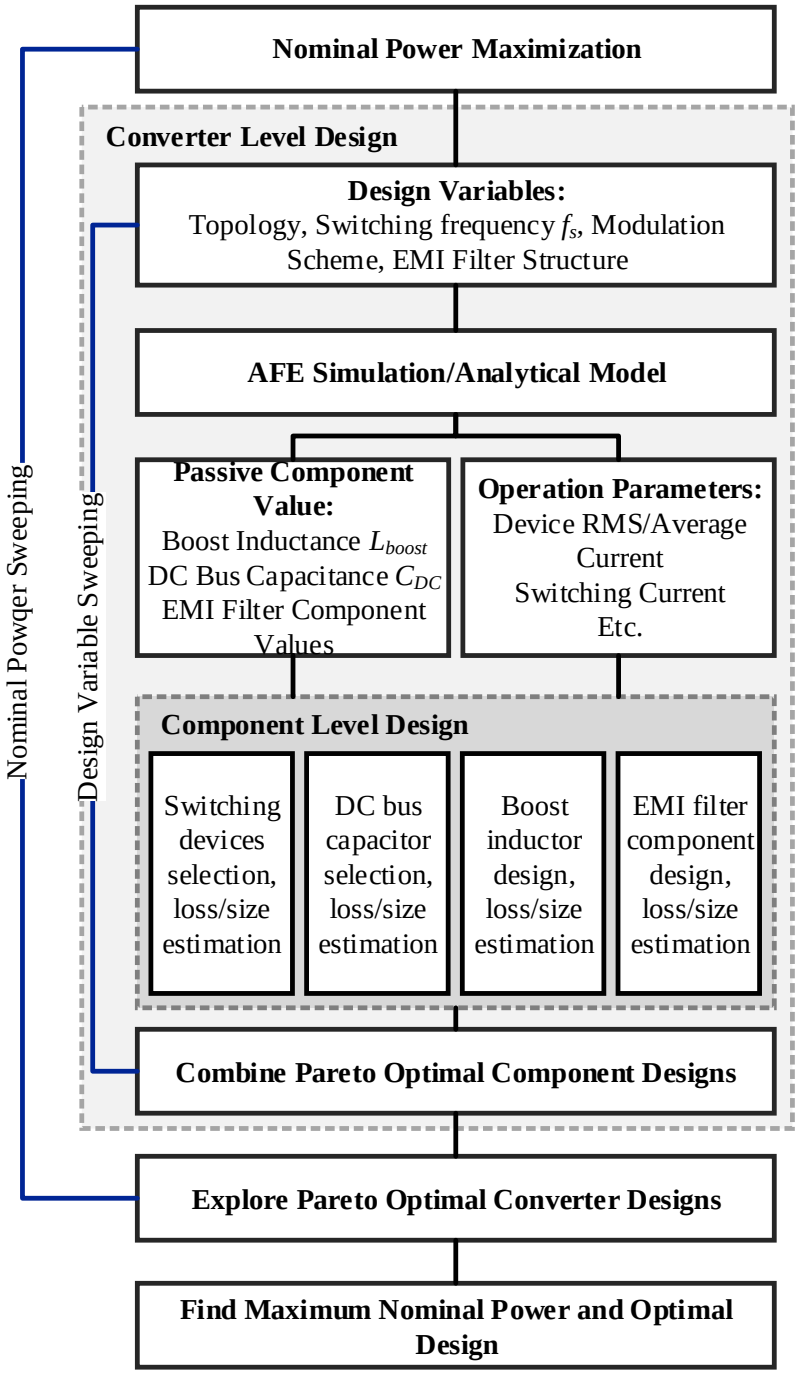



**Fig. 3-5. Nominal power maximization procedure of AFE converter based on BLPP.**

### *3.3.1 Converter Level Design*

In converter level design, combinations of key design variables (topology, switching frequency, etc.) of AFE are swept. Based on the design variable combinations, values of passive components (filter inductance, filter capacitance and DC bus capacitance) are calculated through simulation and analytical models to address EMI and power quality requirements. Operation parameters (e.g. current through diodes/MOSFETs) needed for component design are also calculated.

### *3.3.2 AFE Converter Level Design Variables*

Converter topology is one of the key converter level variables. Two candidates, two-level boost rectifier and Vienna rectifier (converter schematics shown in Fig. 3-6), are considered. Two-level boost rectifier has been widely used in industry thanks to their simplicity. It features low semiconductor conduction loss and bidirectional power flow. On the other hand, Vienna rectifier is a three-level converter, which features reduced switching voltage. Furthermore, Vienna rectifier is a unidirectional converter. Unlike two-level boost rectifier where the current commutates between two MOSFETs, specifically, between MOSFET body diode and the other MOSFET, current in Vienna rectifier commutates between diodes and MOSFETs. This feature, on one hand, reduces switching loss by using SiC Schottky diodes that eliminates reverse recovery loss, on the other hand, limits the operation range of Vienna rectifier. The two topologies are carefully compared through the nominal power maximization.

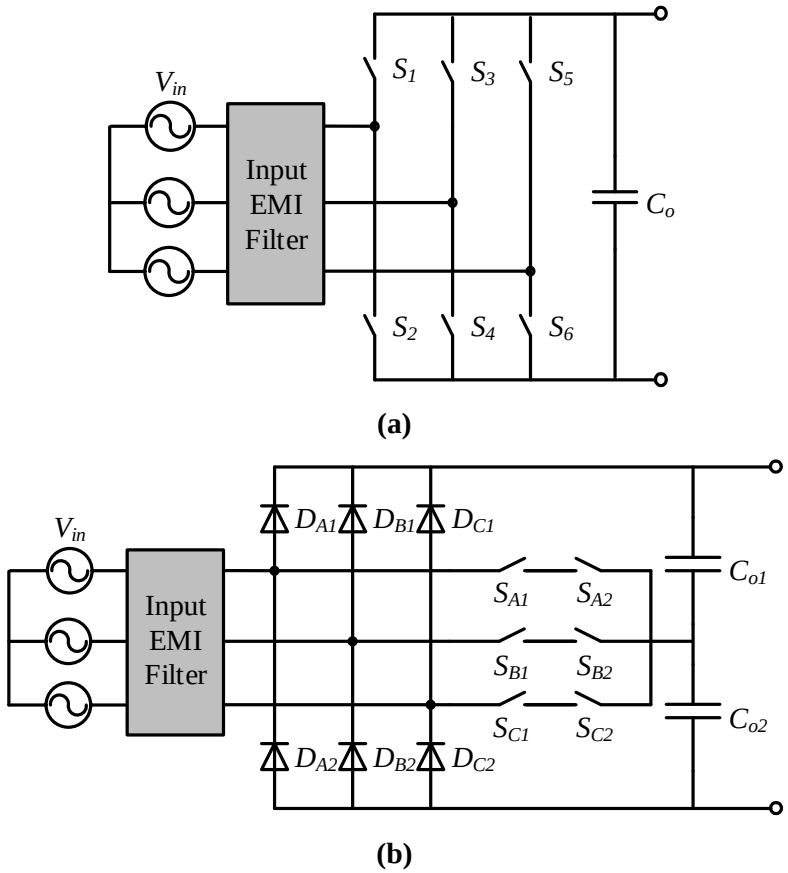



**Fig. 3-6. AFE topology candidates. (a) Two-level boost rectifier. (b) Vienna rectifier.**

For other converter level design variables, center aligned PWM are selected as modulation scheme. Switching frequency is swept from 36 kHz to 100 kHz for two-level boost rectifier. For Vienna rectifier, 36 kHz to 200 kHz is used. The lower bound of switching frequency is selected based on power quality standard. The power quality standard has limitations up to $40^{th}$ order harmonics, which is 32 kHz given 800 Hz input frequency. Switching frequencies below 36 kHz results in large input filter to mitigate sideband noise in power quality standard range, thus is not considered. LCL and LCLCL input filter structure (shown in Fig. 3-7 (a) and (b)) are input EMI filter structure candidates. The inductors that are the closest to phase legs ($L_{boost}$) are termed boost inductors, and the other differential mode (DM) inductors ($L_{DM1}$ and $L_{DM2}$) are termed DM filter inductors in this work.

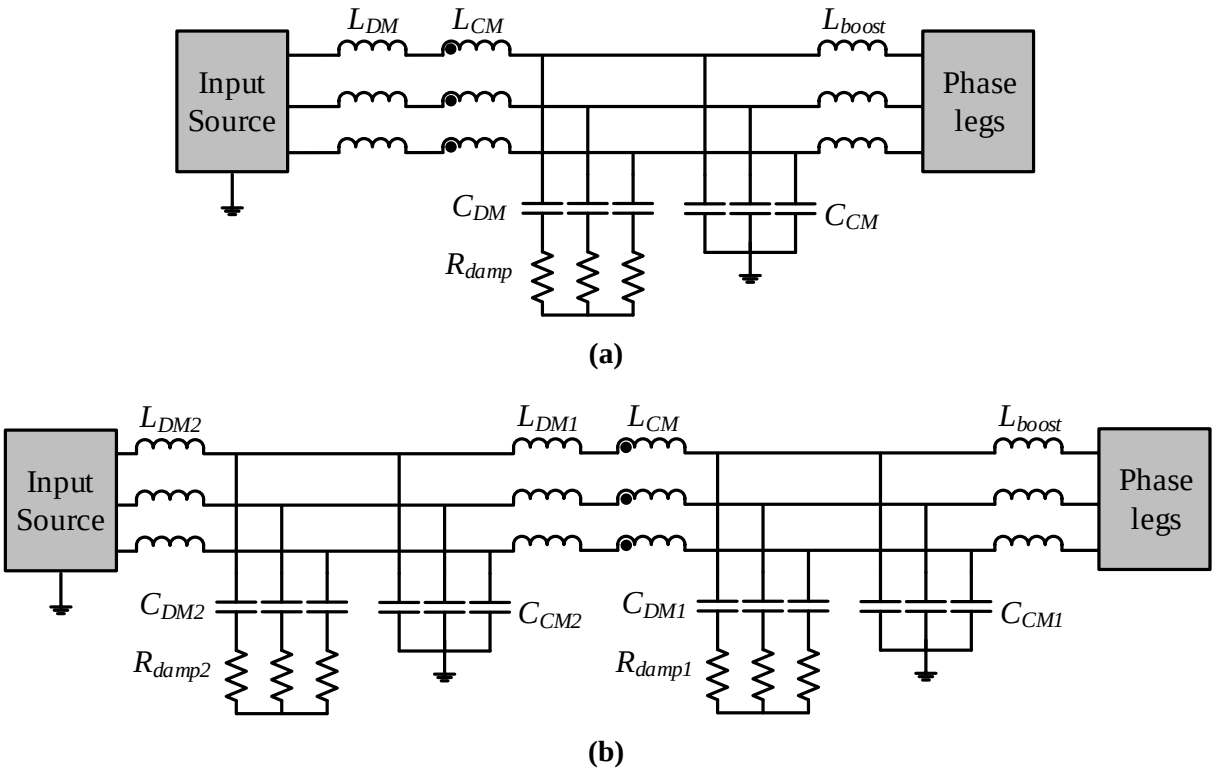



**Fig. 3-7. Input EMI Filter Structure. (a) LCL structure. (b) LCLCL structure.**

### *3.3.3 Sizing Passive Component Value*

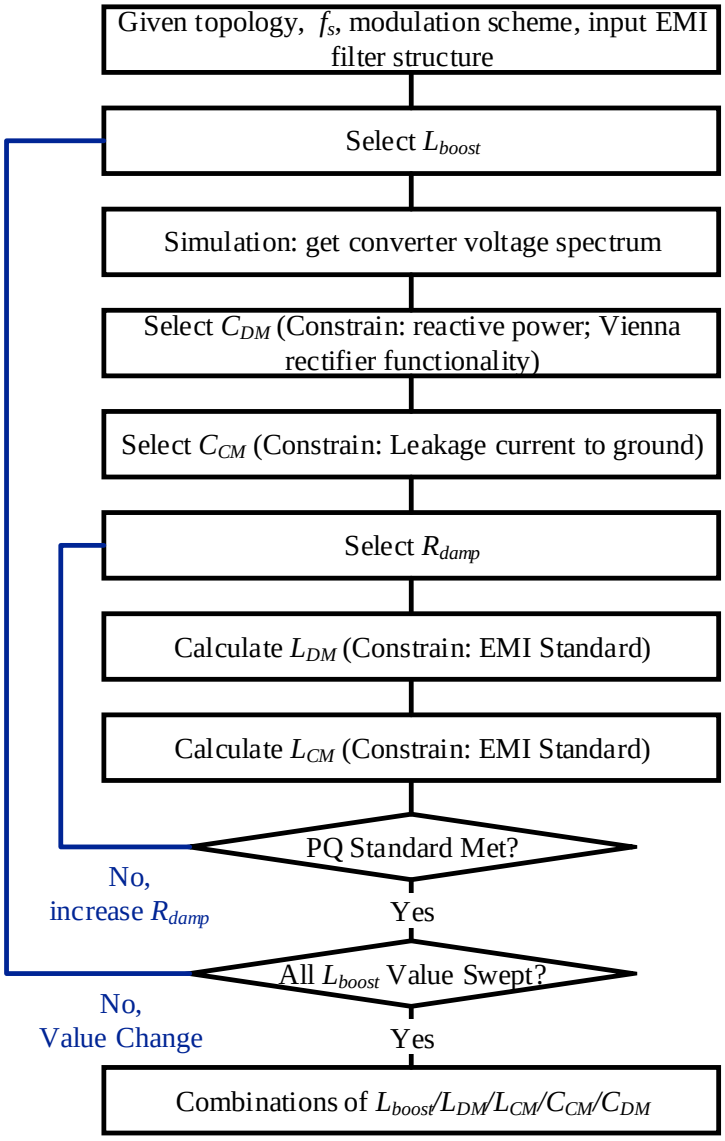



**Fig. 3-8. EMI filter component value calculation procedure.**

The procedures for calculating parameters of the components in the EMI filter is graphically depicted as block diagrams in Fig. 3-8. Boost inductance $L_{boost}$ is picked up first. Common mode (CM) capacitance is limited to 20 nF per phase considering line-to-ground leakage current limit. Design of DM capacitance differs for the two topologies. For two-level boost rectifier, DM capacitance is limited to 2.5 μF per phase to limit the total reactive power drawn from EMI filter.

For Vienna rectifier, the angle between phase leg current and voltage should be low enough to ensure correct modulation [5], which gives limitations on total allowed filter capacitance. The angle limit is given by:

$$\theta_{\text{limit}} = \left| \arcsin\left(\frac{1}{\sqrt{3}M} - \frac{\pi}{6}\right) \right| = 0.124 rad \tag{44}$$

where $M$ is the modulation index and is defined as $V_{in,peak}/(V_{DC}/2)$ (equals to 0.96 in this design). Assuming unity power factor is achieved at input terminals, this limits the angle between filter reactive power and converter active power:

$$\arctan\left(\frac{|Q_{filter}|}{P_o}\right) \approx \arctan\left(\frac{|2\pi f_{in} L_{filter} I_{in,RMS}{}^2 - 2\pi f_{in} C_{filter} V_{in,RMS}{}^2|}{I_{in,RMS} V_{in,RMS}}\right) < \theta_{\text{limit}} \tag{45}$$

where $L_{filter}$ is the total inductance including boost inductance and DM filter inductance per phase, $C_{filter}$ is the total capacitance per phase. It is clearly shown that the total allowed filter capacitance is related to input frequency, active power and total filter inductance. In this design, the capacitance is selected to ensure the correct modulation under half load with 800 Hz input frequency. The relationship between allowed filter capacitance and total filter inductance is graphically shown in Fig. 3-9, based on which the DM capacitance for Vienna rectifier can be selected (use boost inductance to select the capacitance firstly, iterations might be needed if total DM filter inductance is comparable to or larger than boost inductance). A damping resistor is added in series with the DM capacitor to damp the unwanted current noise in power quality standard band (up to 32 kHz) induced by filter resonance.

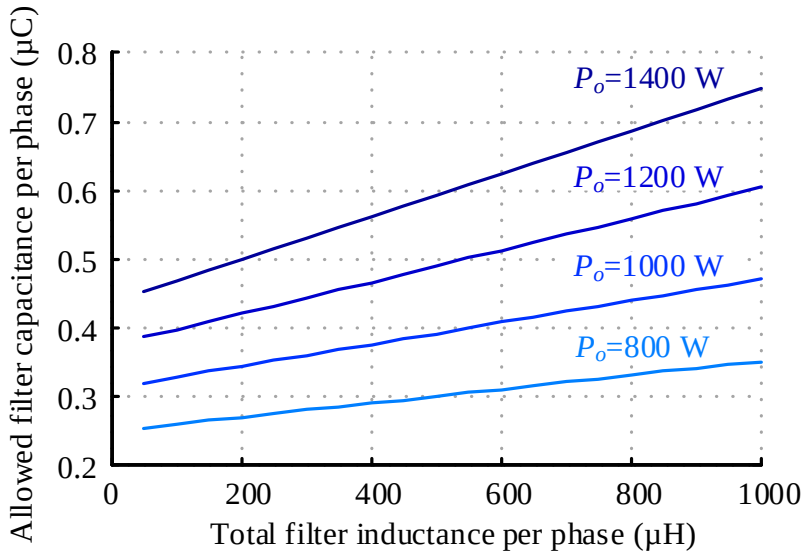



**Fig. 3-9. Relationship between allowed filter capacitance and total filter inductance.**

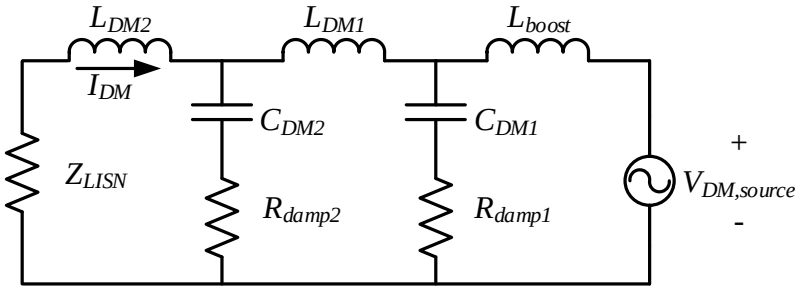



**Fig. 3-10. Converter differential mode (DM) model.**

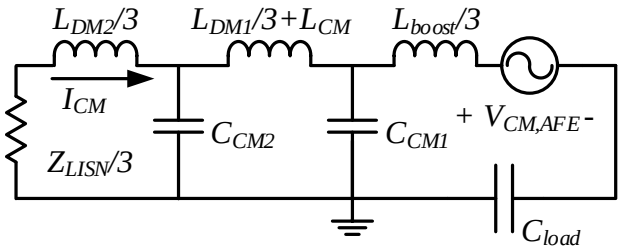



**Fig. 3-11. Converter common mode (CM) model. $C_{load}$ represents parasitic capacitor between load or following stages and power ground. For design of LCL filter, $L_{DM2}$, $C_{DM2}$, $R_{damp2}$, $C_{CM2}$ are not needed.**

Given the converter level design variables, the output voltage spectrum of each phase leg (referred as $V_{a,ph}$, $V_{b,ph}$ and $V_{c,ph}$) can be calculated through Matlab Simulink simulation model (analytical models are also possible, e.g. applying double Fourier transform to modulator reference

and carrier). With the voltage spectrum, selected filter capacitance and damping resistance, DM inductance and CM inductance is calculated based on the EMI standards, DM model (shown in Fig. 3-10) and CM model (shown in Fig. 3-11) [5, 21, 118, 119]. In the DM model, noise source $V_{DM,AFE}$ is calculated by $V_{a,ph} - (V_{a,ph} + V_{b,ph} + V_{c,ph})/3$. In the CM model, $V_{CM,AFE}$ is calculated by $(V_{a,ph} + V_{b,ph} + V_{c,ph})/3$. The capacitance between load and power ground is considered (shown as $C_{load}$ in Fig. 3-11), and a 100 pF capacitance is assumed in the study. Because the design requires eliminating the heat sinks, the parasitic capacitors between heat sinks and power ground [118] are not included herein.

By sweeping boost inductance and following the design procedures, the required DM filter inductance and boost inductance to fulfill the EMI and power quality requirements is calculated, and the result is depicted by Fig. 3-13. In contrast to observations in [21, 79] that three-level converters lead to smaller EMI filters than their two-level counterparts, Vienna rectifiers require higher DM filter and boost inductance in this work. This results from two aspects: 1) owning to the modulation limitation, Vienna rectifiers use smaller DM filtering capacitance (referring to Fig. 3-9 and comparing with 2.5 μF per phase for two-level boost rectifiers), and it requires higher DM filter inductance when boost inductance is the same. 2) Sideband noise of Vienna rectifiers is more spread-out, resulting in higher noise within power quality standard band. Higher boost inductance is required to comply with power quality standard. To illustrate the noise spectrum difference, the phase leg voltage spectrum of the two converters at 800 Hz input frequency and 68 kHz switching frequency are shown in Fig. 3-12. For the first sideband, though Vienna rectifiers present lower peak amplitude at the center of the sidebands, the spread-out sideband noise has higher amplitude. Therefore, Vienna rectifier requires higher noise attenuation (lower filter admittance) within power

quality standard band, where the attenuation is mainly provided by boost inductors. An example of DM filter admittance of the two converters is given in Fig. 3-12. The boost inductance and DM filter inductance are 150 μH and 10 μH respectively for two-level boost rectifier, and are 350 μH and 26 μH respectively for Vienna rectifier. Though the two filters provide similar admittance in EMI standard range, filter of Vienna rectifiers must provide lower admittance within power quality standard band to accommodate the power quality requirement.

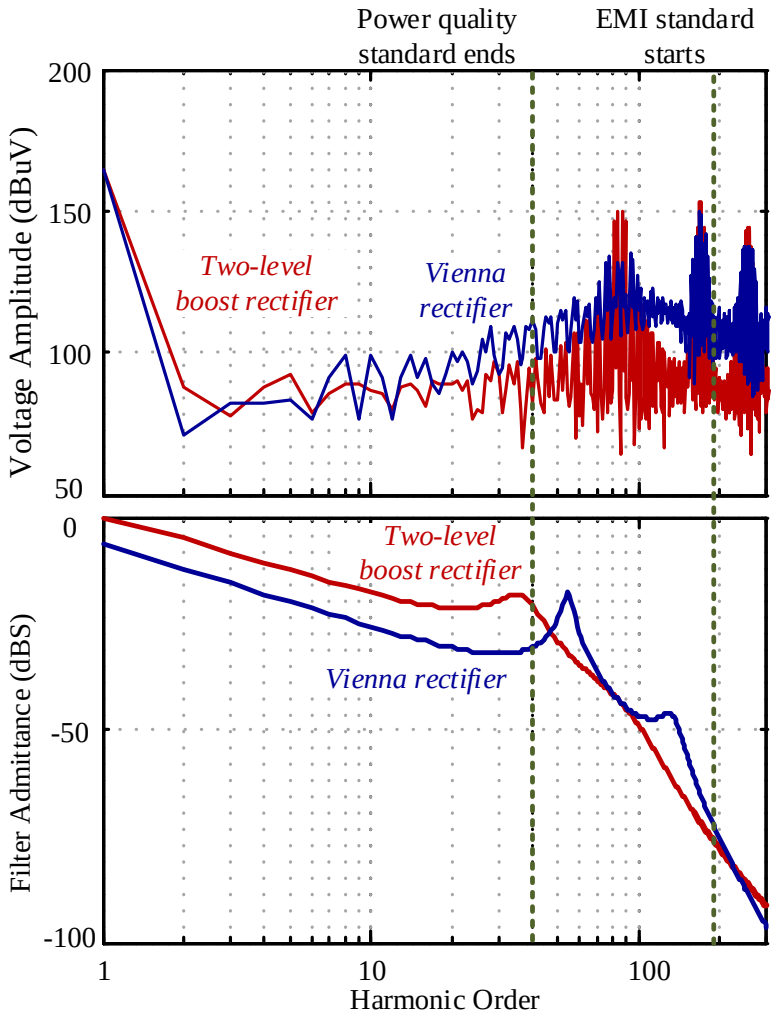



**Fig. 3-12. DM noise amplitude (68 kHz switching frequency for both topologies) and DM filter admittance (both meets power quality and EMI standard). Vienna rectifier features lower**

**amplitude within EMI standard range while producing higher amplitude noise in power quality range.**

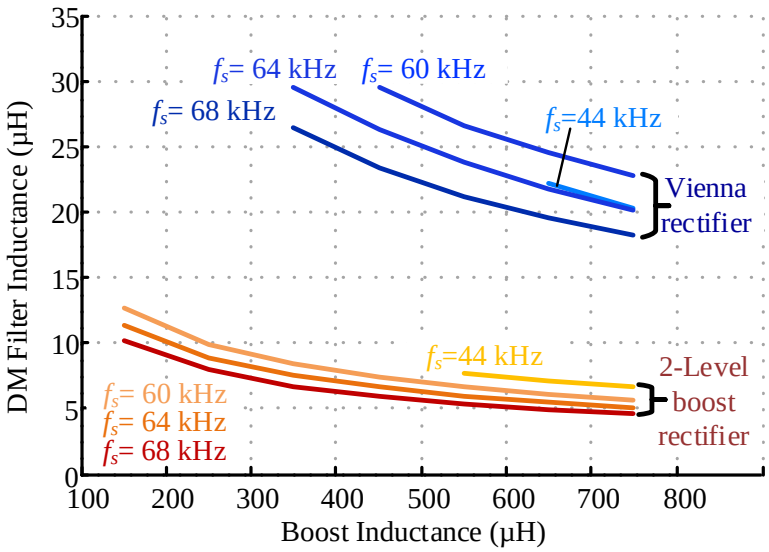



**Fig. 3-13. DM filter design of the two topologies. Two-level boost rectifier features lower inductance thanks to the bigger DM capacitance and lower noise amplitude in power quality range.**

For DC bus capacitance, it is designed such that the voltage rise on DC bus capacitors at sudden load drop (full load to no load) will not exceed the voltage limit of their selves and that of the semiconductor devices. Additionally, for Vienna rectifier, which is a three-level converter, the low frequency ripple on the two DC bus capacitors (also known as neutral point ripple) may influence the input power quality. Third order harmonics can be found on neutral point voltage, which will result in $5^{th}$ and $7^{th}$ harmonics in input current. DC bus capacitance should be large enough to ensure the compliance of power quality standard. It should be noted that, for Vienna rectifier, neutral point ripple is also influenced by input frequency and modulation index. These factors should be carefully considered when determining the DC bus capacitance.

All the possible combinations of feasible passive component value resulting from converter level design will be fed to component level design for converter loss and size estimation.

### *3.3.4 Component Level Design*

In component level design, all components are designed and optimized based on the values given by converter level design and commercially available components. Their size and loss are estimated.

For semiconductor devices, 1200 V SiC MOSFETs with 25 mΩ ~ 160 mΩ on-resistance from CREE are selected as switch candidates for two-level boost rectifier. 600 V Si MOSFETs are not considered in this design owning to their high reverse recovery loss. 250 V Si MOSFETs with 20 mΩ and 60 mΩ on-resistance from Infineon together with 650 V SiC Schottky diodes with 5 A ~ 20 A current rating from Infineon and CREE are device candidates for Vienna rectifier. For semiconductor loss estimation, MOSEFT conduction loss is estimated based on the RMS current through it and its on-resistance. MOSFET switching loss is modeled using device double pulse test data.

MOSFET conduction and switching losses are highly temperature dependent. Relationship between MOSFET on-resistance and junction temperature can be found in datasheet. Relationship between MOSFET switching loss and junction temperature are characterized by double pulse tests under various junction temperatures. An example of measured total switching energy of a phase leg of two-level boost rectifier and Vienna rectifier implemented with candidate devices under 25 °C and 150 °C junction temperatures is given in Fig. 3-14. Both phase legs in the test switch at 340 V DC bus voltage V, i.e. MOSFETs in the two-level phase leg switches at 340 V while

MOSFETs in a Vienna phase leg switches at 170 V. It is observed that a two-level phase leg consumes much more switching energy at high junction temperature than at room temperature while the switching energy increase in a Vienna phase leg at elevated junction temperature is small. The aggravated reverse recovery charge at increased junction temperature in a two-level phase leg results in the large switching energy increase (as shown in section 2.3.2). For Vienna rectifier, where MOSFETs commutates with SiC Schottky diodes, the energy increase mainly comes from increased current and voltage overlap during switch transition. The device junction temperature is estimated using an iteration loop [5] in order to achieve accurate temperature and loss estimation. Furthermore, driving the two phase legs takes different energy per switch. For example, the two-level phase leg composed of 80 mΩ MOSFETs takes 3.1 µJ (-5V/20V driving voltage) per switch while Vienna phase leg using 20 mΩ MOSFETs takes 0.5 µJ (0V/9V driving voltage). The driving loss has been considered during design.

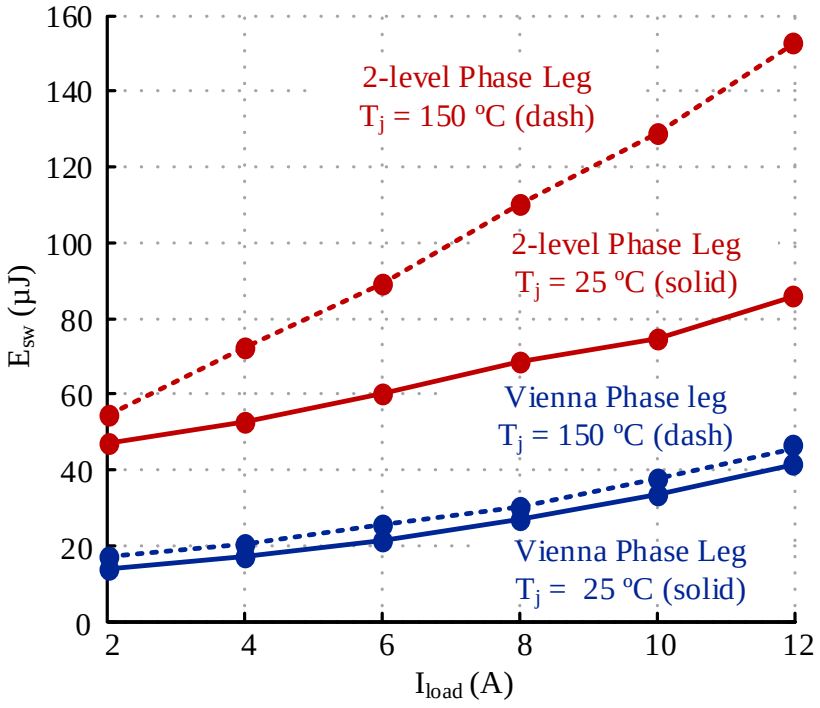


**Fig. 3-14. Measured switching energy of a two-level boost rectifier phase leg implemented with 1200 V SiC MOSFET (CREE C2M0080120D) and a Vienna rectifier phase leg implemented with 250 V Si MOSFET (Infineon IPB200N25N3G) and 650 V SiC Schottky diodes (Infineon IDH20G65C5) under different junction temperatures.**

For boost inductors and DM filtering inductor implementation, Ferroxcube 3C95 ferrite cores (effective volume: 5470 $mm^3$ ~ 52600 $mm^3$), Magnetics Inc. MPP iron powder cores (effective volume: 960 $mm^3$ ~ 10600 $mm^3$) are considered. For CM choke, VAC Vitroperm nanocrystalline cores (effective volume: 360 $mm^3$ ~ 8772 $mm^3$) are considered. Epcos MKP and MKT Film capacitors are considered for DC bus and EMI filtering capacitors. The conduction loss of these passive components is estimated based on device characterization and RMS current through the devices calculated in converter level design. The core loss of the inductors is estimated based on flux density change in the core calculated in converter level design and core characteristics. Improved Generalized Steinmetz Equation (iGSE) [69] is used for core loss calculation.

For component size estimation, since height of the converter is limited to 1 in, it is assumed that no inductors, capacitors and semiconductor devices are placed over other devices. Thus, the footprint area is taken as the performance index representing the device size.

### *3.3.5 Design Results*

A Matlab program is developed to integrate and perform the nominal power maximization and aforementioned models. The results of the two topology candidates with various nominal power ratings are shown in Fig. 3-15 and Fig. 3-16. The dots in these graphs denote design points that integrate component-level Pareto optimal designs (procedure described in section 3.2.2). Their switching frequencies are denoted by different colors. The frequencies that lead to majority of the Final Pareto optimal designs are colored yellow.

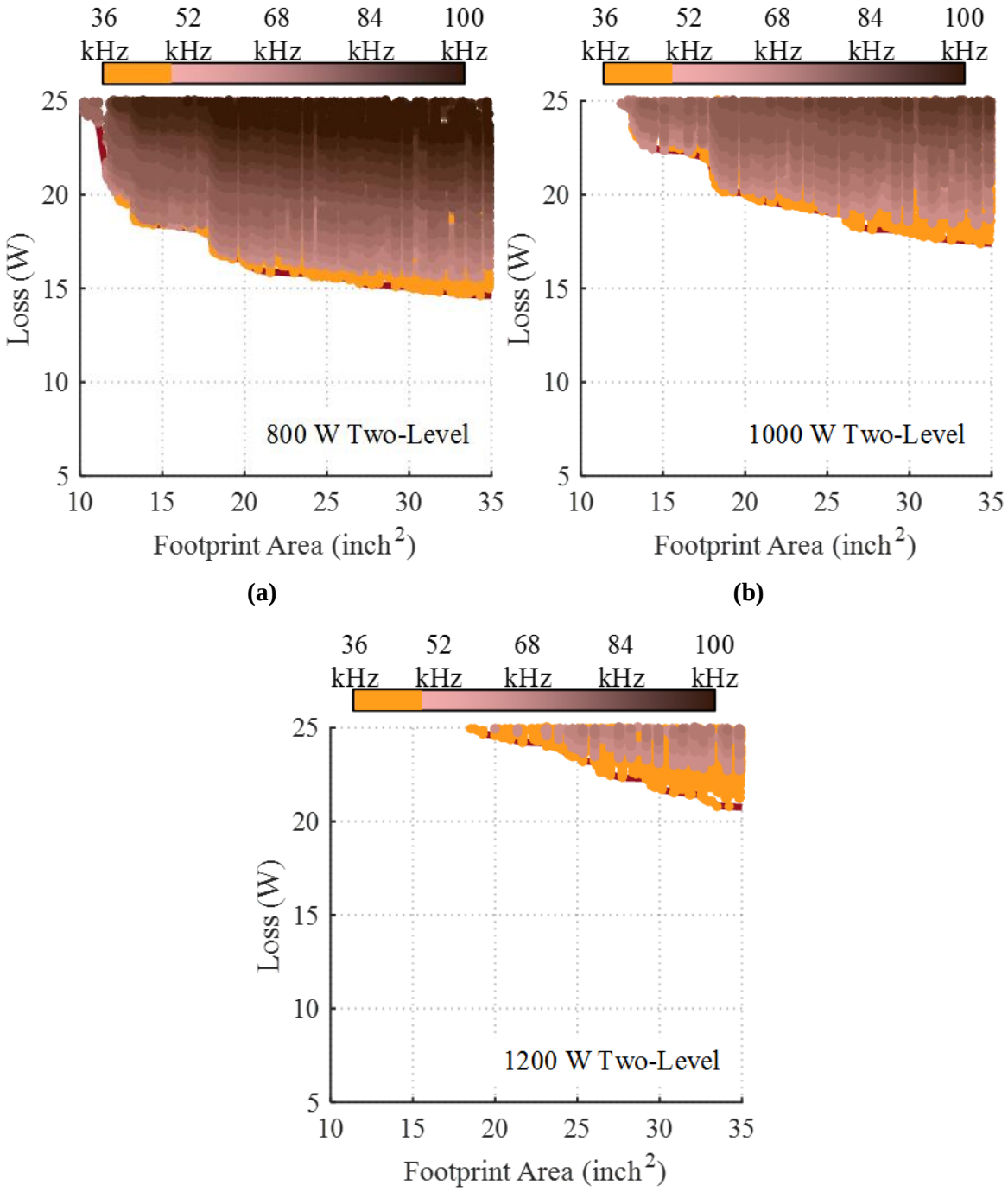



**Fig. 3-15. Loss-size Pareto fronts and design points with various switching frequencies of 2-level boost rectifier. Yellow dots denotes designs with 36 kHz to 48 kHz switching frequency. (a) 800 W designs. (b) 1000 W designs. (c) 1200 W designs.**

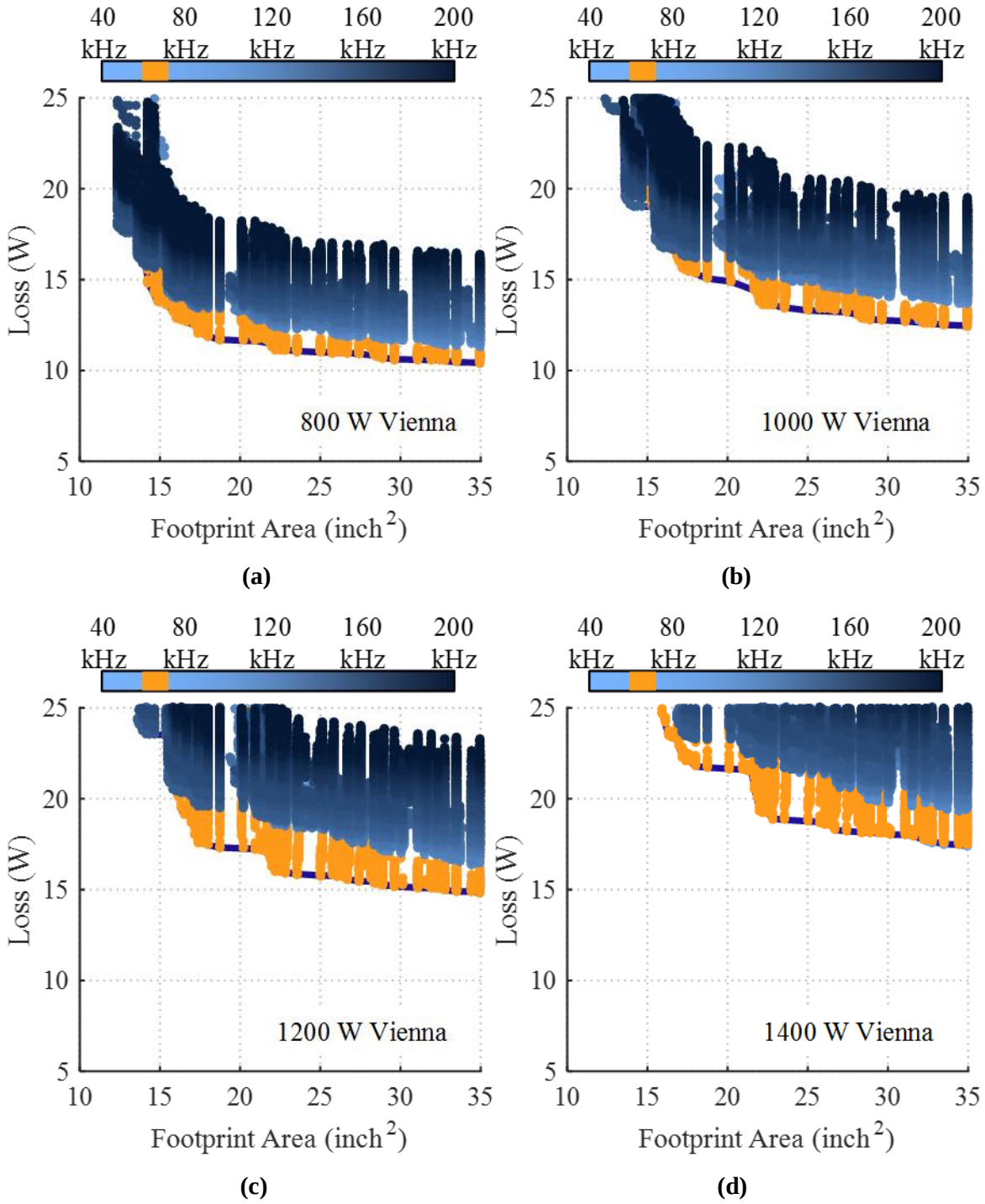



**Fig. 3-16. Loss-size Pareto fronts and design points with various switching frequencies of Vienna rectifier. Yellow dots denote designs with 60 kHz to 72 kHz switching frequency. (a) 800 W designs. (b) 1000 W designs. (c) 1200 W designs. (d) 1400 W designs.**

For two-level boost rectifier, the designs with 36 kHz to 48 kHz switching frequency dominates the Pareto optimal designs, and the optimal designs with 36 kHz to 48 kHz switching frequency are denoted by yellow dots in Fig. 3-15. To demonstrate the design tradeoffs, the switching frequency, the boost inductance (shown in Fig. 3-17), loss breakdown (shown in Fig. 3-18 and Fig. 3-19) and footprint area breakdown (shown in Fig. 3-20) of the Pareto optimal designs with 800 W nominal power are depicted. All the designs use CREE C2M0160120D (1200 V, 160 mΩ) SiC MOSFET. The design that takes the smallest footprint area uses 68-kHz switching frequency and 250-μH boost inductance. Comparing with other designs, it sacrifices switching loss and EMI filter loss (including loss from DM inductors, DM capacitors, CM chokes) to shrink the footprint area. Moving towards higher efficiency designs along the Pareto front, the switching frequency decreases while boost inductance increases. Significant switching loss reduction is observed. As the design changes from 68 kHz switching frequency to 40 kHz, the switching loss reduced by 5.3 W. In order to accommodate increased inductance and to reduce loss, cores with bigger sizes are used to implement boost inductors and DM inductors. Furthermore, as is observed from the right part of Fig. 3-18, Fig. 3-19 and Fig. 3-20, aggressively increasing the core size improves the efficiency but marginally. These are designs of which the semiconductor device losses dominate and the switching frequency is limited by power quality standard (described in section 3.3.1). To further improve the efficiency, semiconductor devices with better performance are needed.

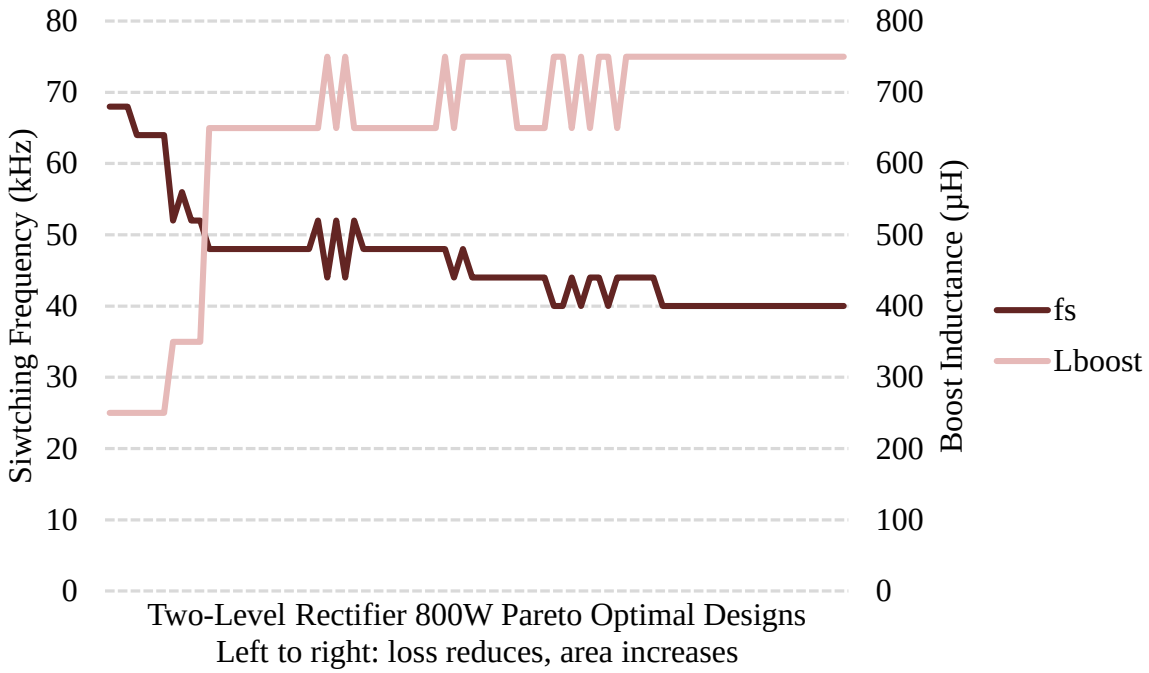



**Fig. 3-17. Switching frequency and boost inductance of Pareto optimal designs of 800 W two-level boost rectifier.**

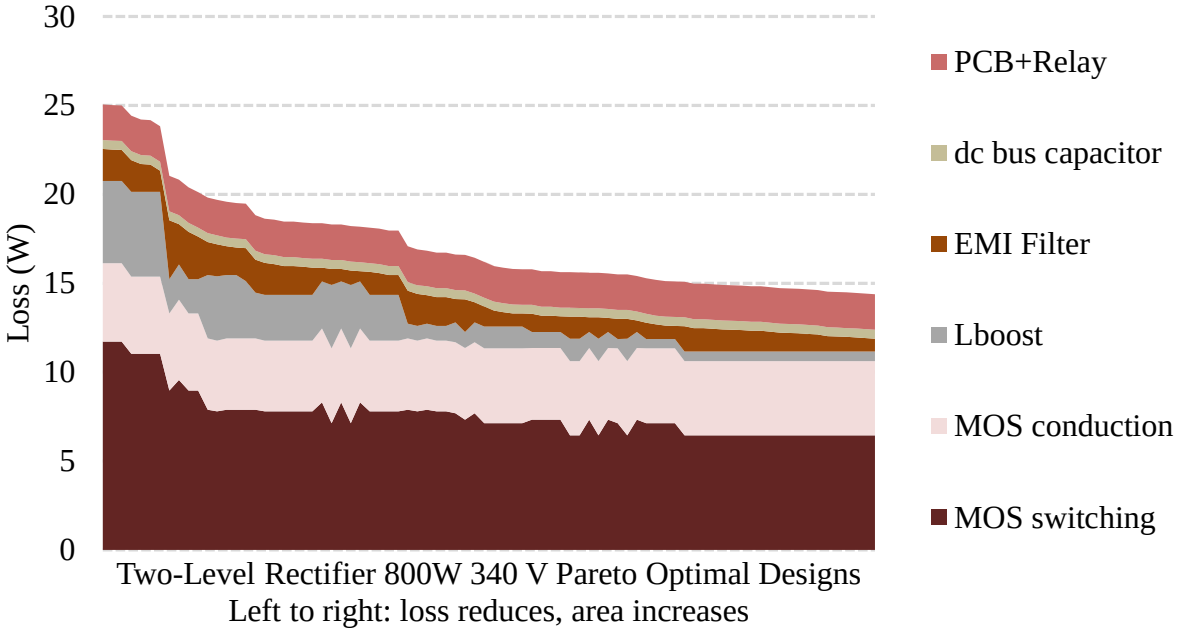



**Fig. 3-18. Loss breakdown of Pareto optimal designs of 800 W two-level boost rectifier.**

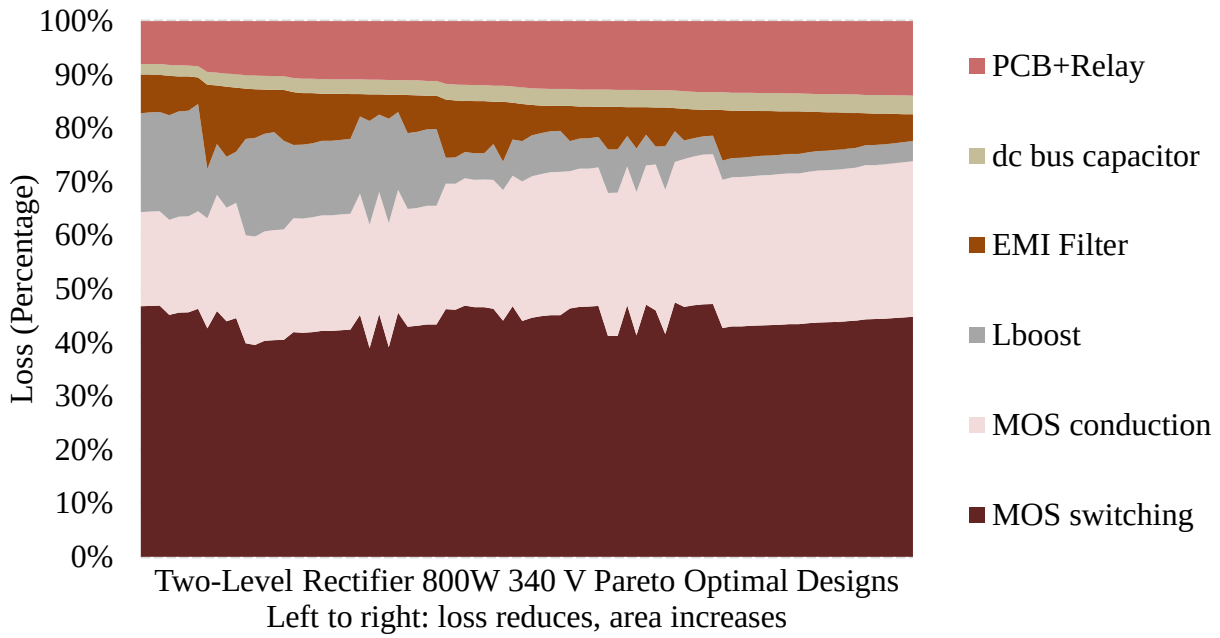



**Fig. 3-19. Percentagewise loss breakdown of Pareto optimal designs of 800 W two-level boost rectifier.**

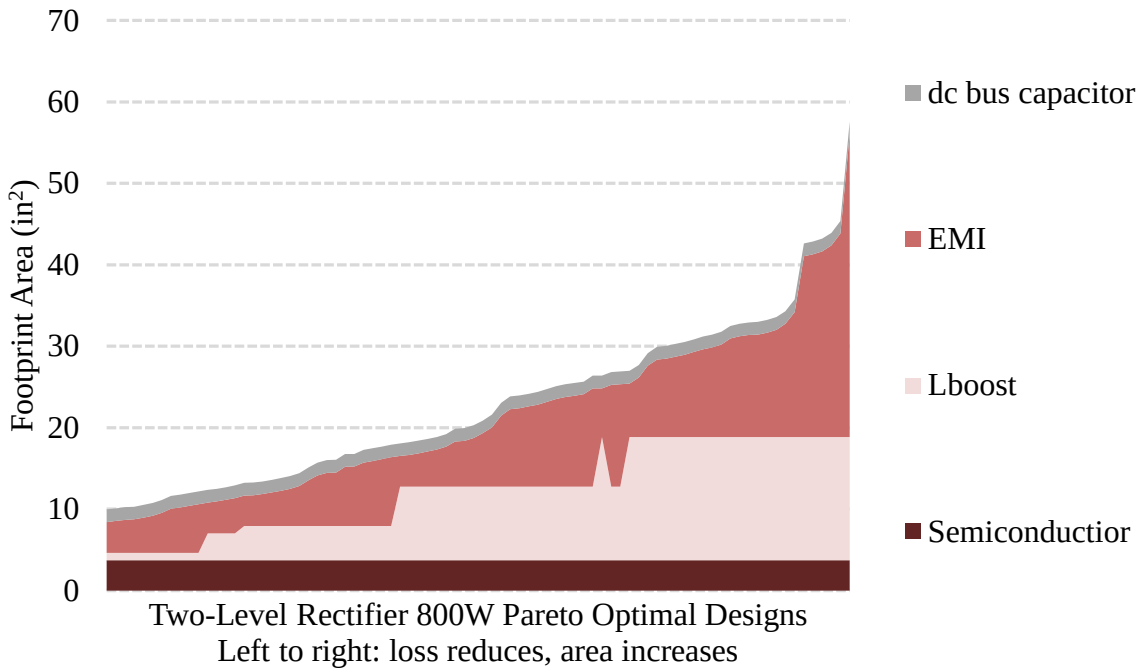



**Fig. 3-20. Footprint area breakdown of Pareto optimal designs of 800 W two-level boost rectifier.**

For Vienna rectifier, the designs with 60 kHz to 72 kHz switching frequency dominates the Pareto optimal designs. The switching frequency, the boost inductance (shown in Fig. 3-21), loss

breakdown (shown in Fig. 3-22 and Fig. 3-23) and footprint area breakdown (shown in Fig. 3-24) of the Pareto optimal designs with 1200 W nominal power are depicted. The switching loss in Vienna rectifier is much smaller than that of two-level boost rectifier, which widens the design space. The optimal designs with compact size (left part of the optimal designs) use switching frequency that is close to 150 kHz while the designs with low loss (right part of the optimal designs) use switching frequency between 60 kHz to 68 kHz. As the switching frequency decreases, majority of the loss reduction is done by using bigger cores for boost inductor and DM inductors. However, the loss reduction from passive components saturates as the loss from semiconductor devices dominates. Therefore, further performance enhancement relies on improvements in semiconductor devices. Especially, improvement in Schottky diodes could largely improve the performance of Vienna rectifier, as the diode conduction loss is one of the major loss sources no matter what the switching frequency is.

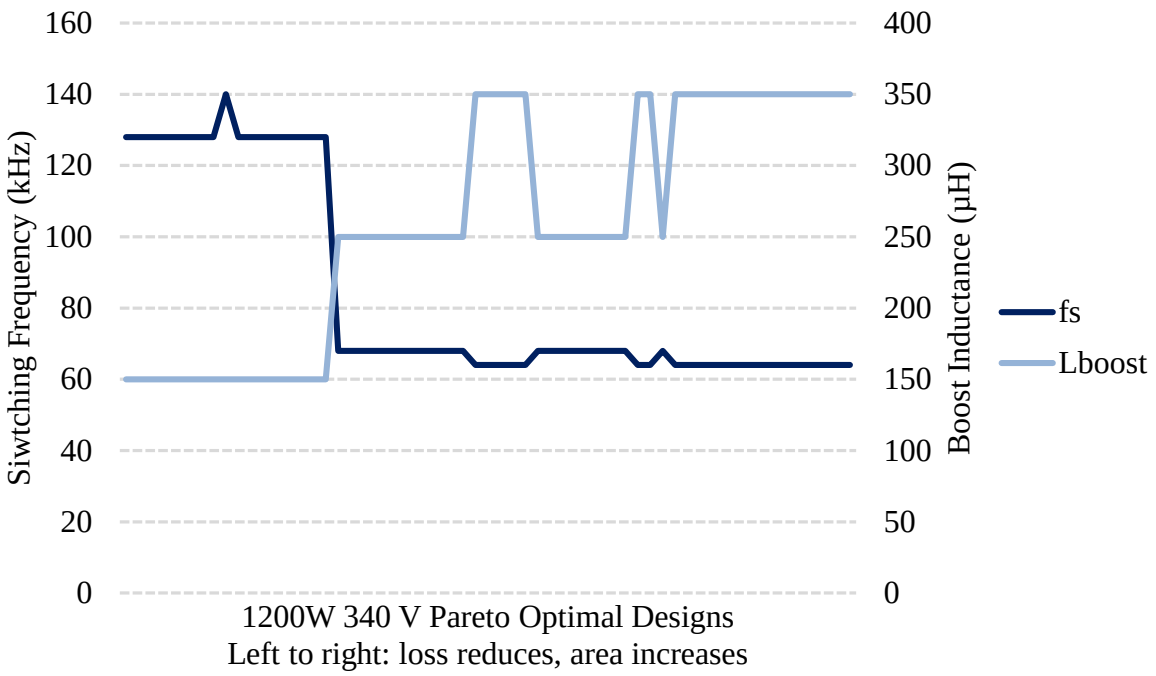



**Fig. 3-21. Switching frequency and boost inductance of Pareto optimal designs of 1200 W Vienna rectifier.**

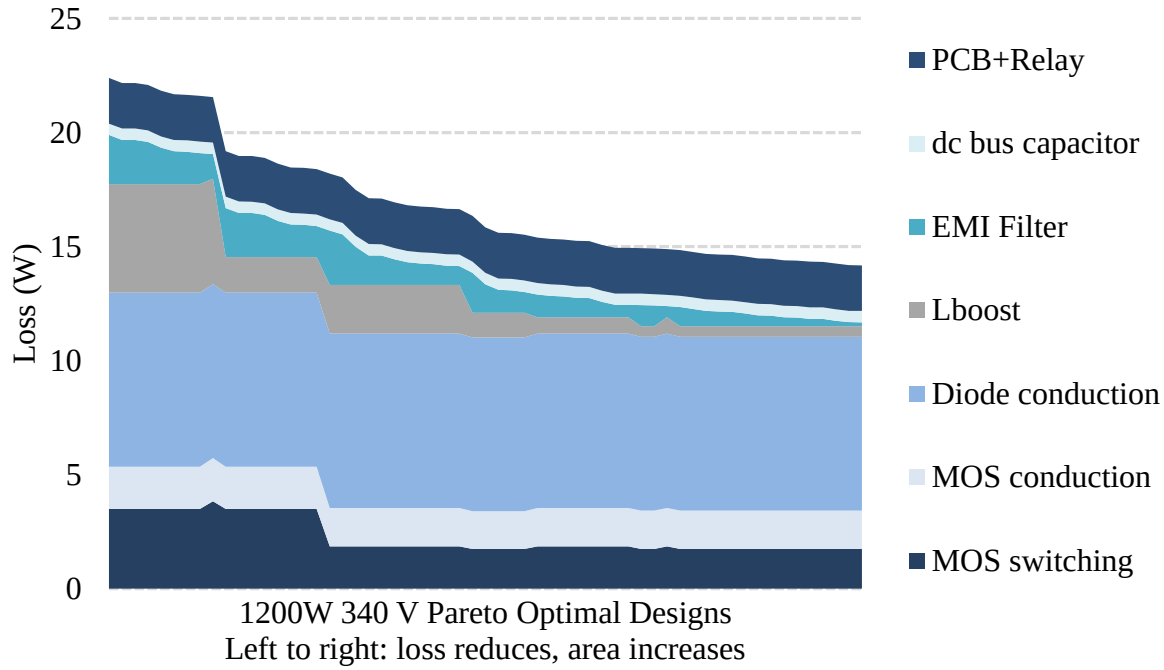



**Fig. 3-22. Loss breakdown of Pareto optimal designs of 1200 W Vienna rectifier.**

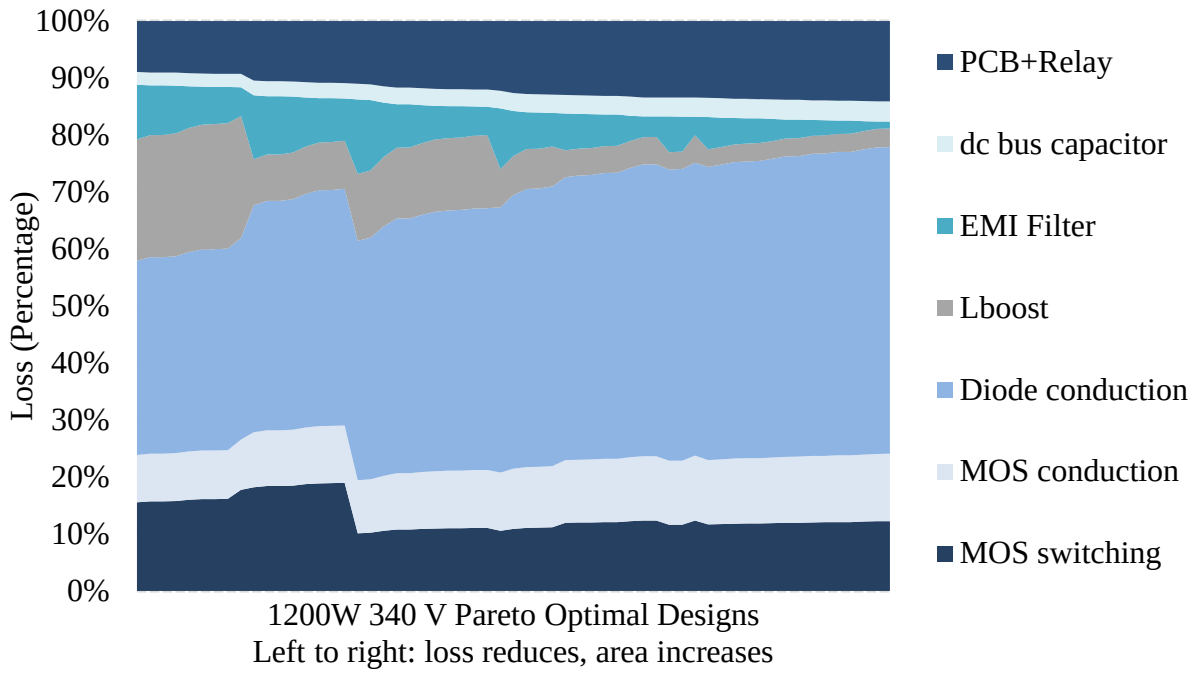



**Fig. 3-23. Percentagewise loss breakdown of Pareto optimal designs of 1200 W Vienna rectifier.**

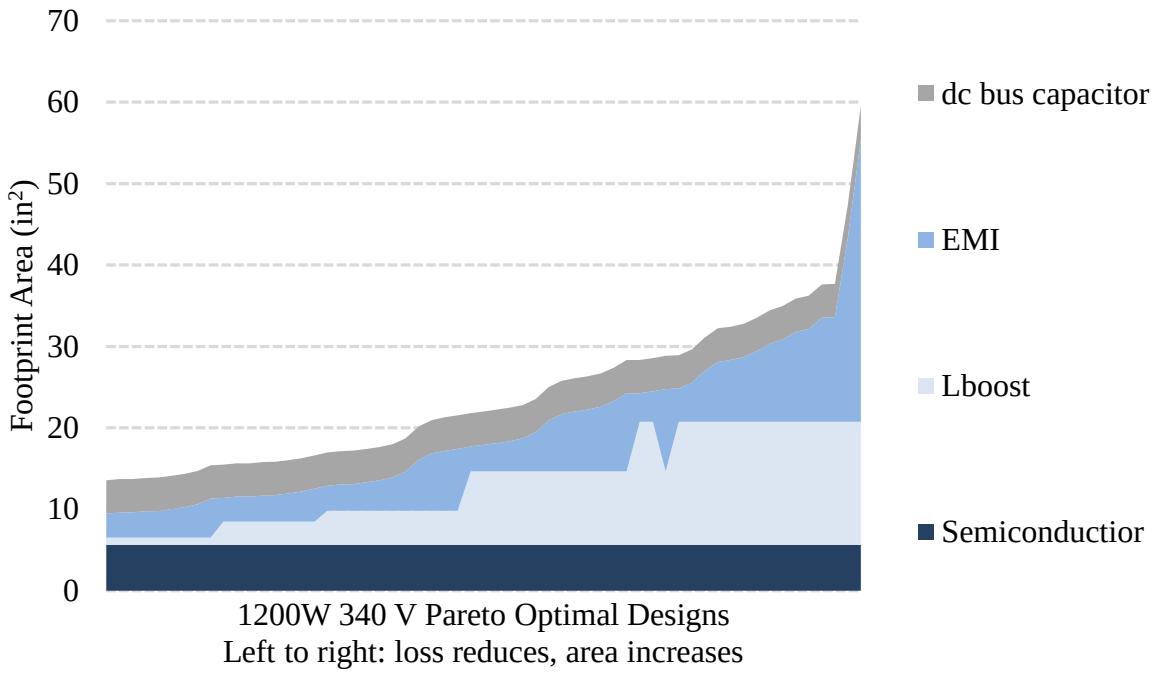
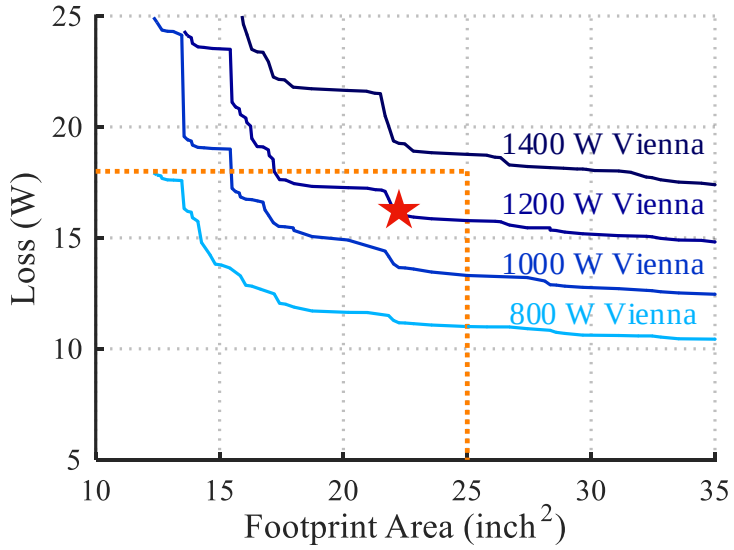


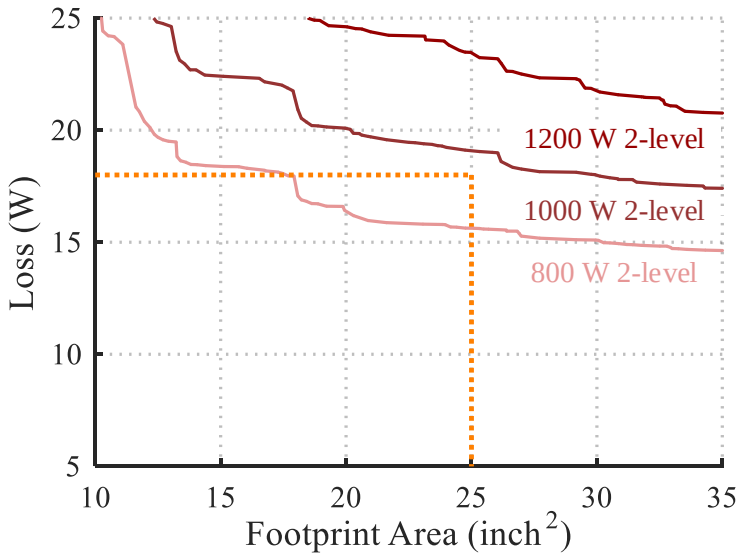

**Fig. 3-24. Footprint area breakdown of Pareto optimal designs of 1200 W Vienna rectifier.**

The loss-size Pareto fronts of the two topologies under different nominal power ratings are summarized in Fig. 3-25. Considering the loss budget (18 W) and form factor constraints (35 $in^2$

x 1 in) while leaving 10 $in^2$ x 1 in layout margin, it is observed that two-level boost rectifier achieve a maximum of 800 W nominal power while Vienna rectifier achieves 1200 W maximum nominal power. The final design of the 1200 W Vienna rectifier that renders 16.1 W loss and 22 $in^2$ area is denoted by a red star in FIG.




**(a)**




**(b)**

**Fig. 3-25. AFE stage loss-size Pareto front under different rated power. (a) Vienna rectifier, achieving 1200 W maximum nominal power. (b) Two-level boost rectifier, achieving 800 W nominal power.**

## 3.4 Constructed Prototype and Experimental Results

This section presents the implementation and testing results of the 1200 W optimal design. The design parameters of the optimal design is listed in TABLE III.

**TABLE III. DETIALED IMPLEMENTATION OF THE VIENNA RECTIFIER**

| | | | | | | |
|---|---|---|---|---|---|---|
| Input EMI Filter | Structure | Boost Inductance | DM Filter Inductance | DM Filter Capacitance | CM Filter Inductance | CM Filter Capacitance |
| | $L_{boost}$+CLCL | 350 µH | 35 µH | 0.22 µF | 230 µH | 10 nF |
| Converter | Topology | Switching Frequency | MOSFETs | Diodes | DC Bus Capacitance | |
| | Vienna rectifier | 64 kHz | IPB200N25N | IGH20G65C5 | 15 µF | |

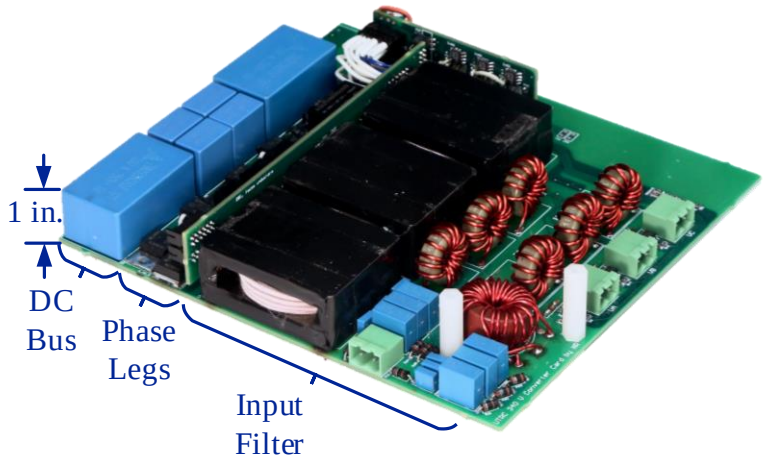



**Fig. 3-26. 1200 W Vienna rectifier prototype.**

The constructed prototype is shown in Fig. 3-25. The dimensions of the prototype is 36 $in^2$ x 1 in, achieving 33 W/$in^3$ power density.

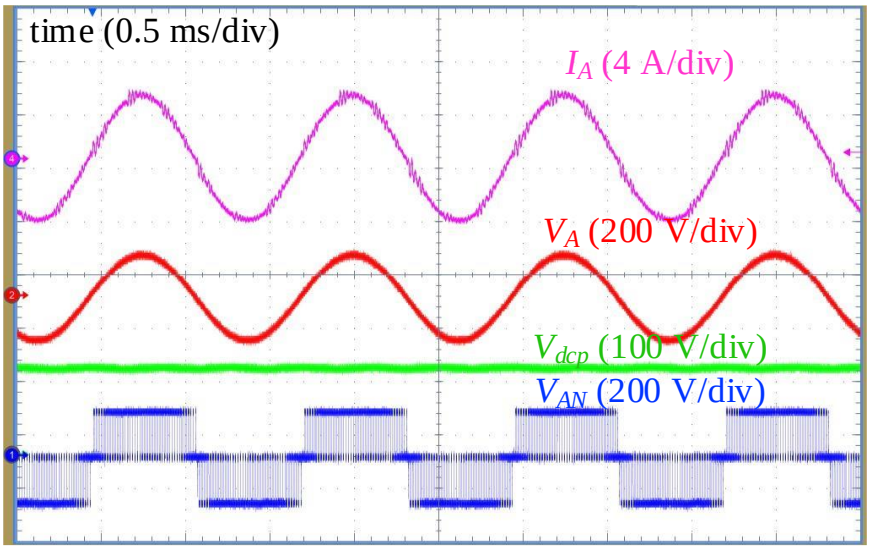



**Fig. 3-27. Experimental waveforms under 1200 W load 800 Hz input. From top to bottom: input current in phase A, input phase voltage of phase A, upper dc bus capacitor voltage and phase leg output voltage of phase A referring to dc bus neutral point.**

Experimental waveforms of the prototype are shown in Fig. 3-27. The input current ($I_A$), input phase voltage ($V_A$), DC bus capacitor voltage ($V_{dcp}$) and phase leg output voltage referring to DC bus neutral ($V_{AN}$) are measured at 1200 W load and 800 Hz input frequency.

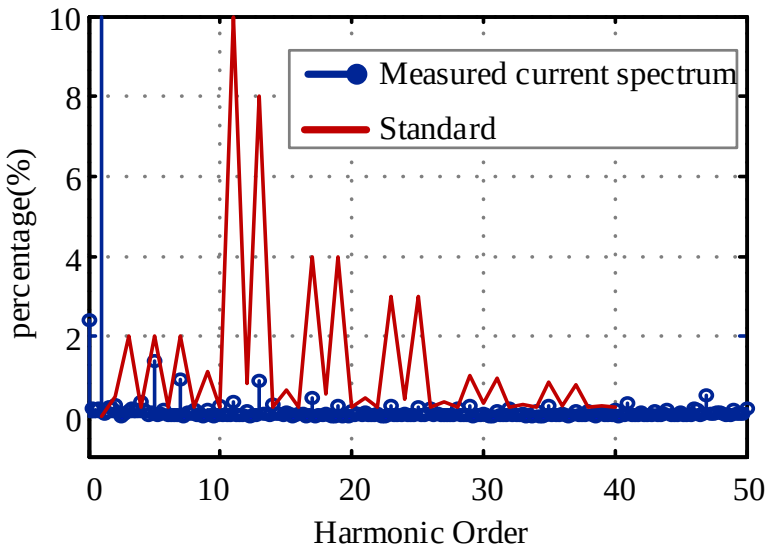



**Fig. 3-28. Measured input current harmonics in power quality standard range (up to 40$^{th}$ order) and the power quality standard [6].**

The measured input current low frequency harmonics (with 360 Hz and 800 Hz input) and the power quality standard are summarized in Fig. 3-28. These are results with the turn-off compensation scheme to be presented in Section V. The low frequency current harmonics comply with the power quality standard.

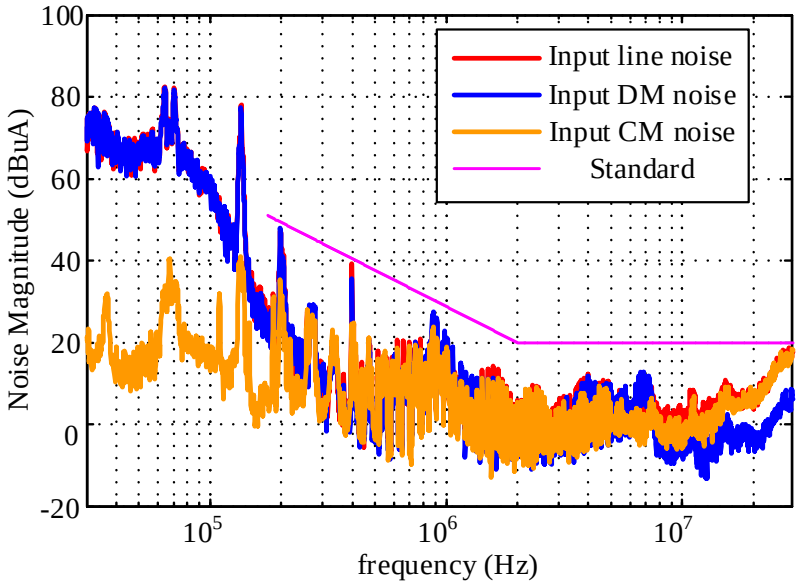



**Fig. 3-29. Measured input EMI noise spectrum and the EMI standard [6].**

The input line, DM and CM noise is measured by An ETS Lindgren 91550-1 current transformer that connects to an Agilent 7402A EMC spectrum analyzer. The results are summarized in Fig. 3-29, and they comply with the DO-160 EMI standard.

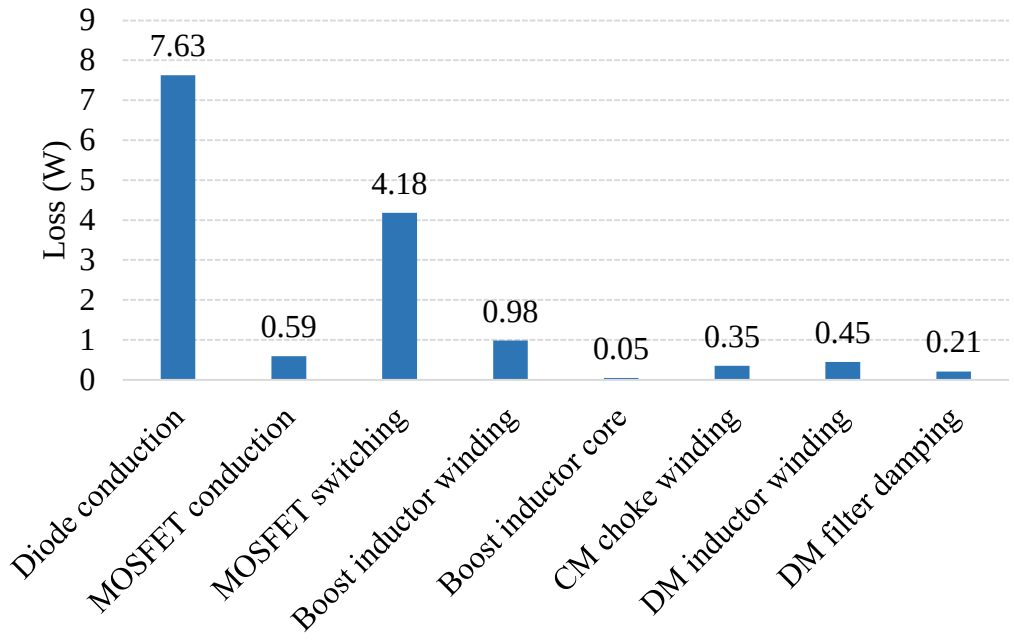



**Fig. 3-30. Calculated loss breakdown of the prototype.**

The converter loss and efficiency is measured by a Yokogawa PZ4000 power analyzer. All the tests are conducted with 115 V input voltage and 400 Hz input frequency. The data was recorded when temperature of all the devices reached steady state (after 30 minutes of operation). The total measured loss at full load is 17.5 W, consisting of 16.3 W power stage loss and 1.2 W auxiliary power consumption. The measured full load efficiency is 98.5 %. The calculated loss breakdown is summarized in Fig. 3-30.

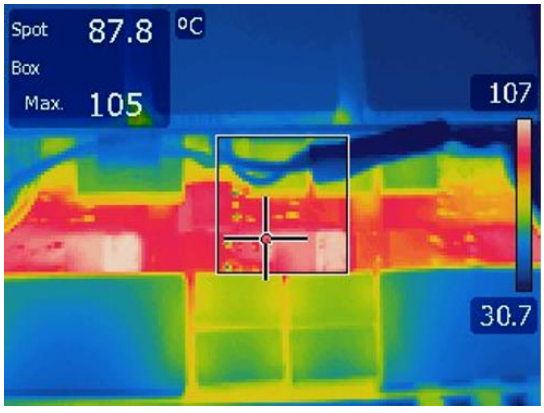


**Fig. 3-31. Thermal graphic of the phase leg area.**

The devices surface temperature is measured by FLIR E40 thermal camera. The tests are conducted at 25 °C lab ambient. The thermal graphic is shown in Fig. 3-31. The hottest spot is found on the diodes and the surface temperature is 107 °C, which leaves enough margin considering its 175 °C temperature limit. The MOSFETs reaches 82 °C and is safe considering the 150 °C temperature limit. The temperatures of other components are below 40 °C and they are proper for safe operation.

## 3.5 Method for Turn-off Delay Compensation

Complying with the power quality standard ($2^{nd}$ ~ $40^{th}$ current harmonics) is critical in aerospace applications. In the constructed prototype, it is observed that there is significant $5^{th}$, $7^{th}$, $11^{th}$ and $13^{th}$ order harmonics in input current, leading to failure in complying the power quality standard. [120] claim that the turn-off delay of MOSFETs induces the low frequency harmonics. In the prototype, to achieve high efficiency and natural convection cooling, MOSFETs with low on-resistance and high junction capacitance are used, which further increases the turn-off time and worsen the power quality. In this section, the mechanism of turn-off delay is studied, and a control method to enhance power quality by compensating the delay is proposed and discussed.

### 3.5.1 Analysis on Turn-off Delay

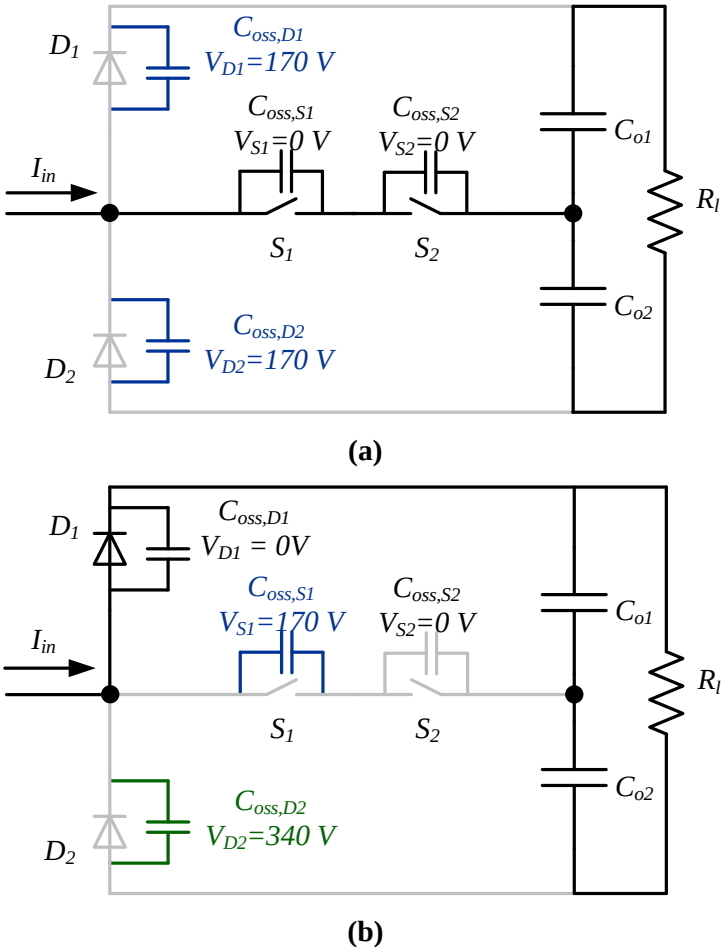



**Fig. 3-32. Blocking voltages of the semiconductor devices and conducting paths of a phase leg in Vienna rectifier. (a) Current flows from source to the middle point through $S_1$ and $S_2$. (b) Current flows from source to the positive rail through $D_1$.**

Fig. 3-32 depicts the current commutation during MOSFET turn-off. Assume without loss of generality that the converter operates in positive half cycle, and the current flows from the source to the dc bus. During MOSFET turn-off, the current commutates from the two MOSFETs ($S_1$ and $S_2$ in Fig. 3-32) to the top diode ($D_1$). Before the top diode conducts, its output capacitor should be fully discharged while that of MOSFET $S_1$ and diode $D_2$ should be charged to establish a constant phase leg output voltage. The output capacitor of $S_1$ should be charged to half of the dc bus voltage

(170 V) while output capacitor of $D_2$ is charged from half of the dc bus voltage (170 V) to full voltage (340 V). All the charge, including the charge discharged from $D_1$, is provided by the input current. Therefore, although the MOSFET channels can be turned off quickly (determined by the turn-off gate voltage, gate resistance and gate-source capacitance), the turn-off procedure can be long if the current is too small to charge and discharge fast. Typical waveforms of gate-to-source voltage $V_{gs}$ and drain-to-source voltage $V_{ds}$ during MOSFET turn-off are depicted in Fig. 3-33. $t_{delay}$ represents the time from falling of $V_{gs}$ to establishment of $V_{ds}$, and it consists of falling time of $V_{gs}$ and rising time of $V_{ds}$. During this transition, the phase leg output voltage-second deviates from ideal case and the deviation is calculated by:

$$VS_{loss} = t_{delay} V_{DC} - \int_0^{t_{ds,r}} v_{ds}(t)dt \quad (46).$$

The voltage-second loss induces low frequency harmonics.

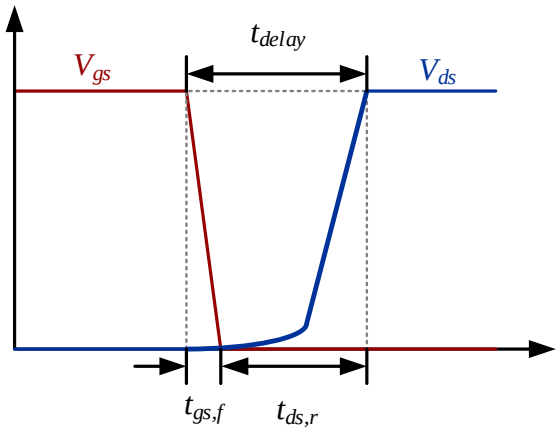



**Fig. 3-33. Typical gate-to-source voltage and drain-to-source voltage waveforms during MOSFET turn-off.**

During its rising, $V_{ds}$ is not a linear function of time (an assumption made in [117]) owning to the nonlinearity of output capacitors of semiconductor devices. Because the charge of the output

capacitors are provided by input current, assuming a constant input current during the transition, $V_{ds}$ over time ($v_{ds}(t)$) during its rising is found through:

$$I_{in}t = \int_0^{v_{ds}(t)} C_{oss,S1}(v)dv + \int_{V_{dc}/2}^{V_{dc}/2-v_{ds}(t)} C_{oss,D1}(v)dv + \int_{V_{dc}/2}^{V_{dc}/2+v_{ds}(t)} C_{oss,D2}(v)dv \quad (47),$$

where $I_{in}$ is the input current, and $C_{oss,S1}(v)$, $C_{oss,D1}(v)$ and $C_{oss,D2}(v)$ represents the $S_1$, $D_1$ and $D_2$ output capacitance when the blocking voltage equals to $v$. The output capacitance over voltage information can be got from datasheets. There is no closed form expression for $v_{ds}(t)$ owning to the nonlinearity of the output capacitors, but it can be solved through numerical methods (e.g. Newton-Raphson method). The total rising time $t_{ds,r}$ is calculated by:

$$t_{ds,r} = \frac{\int_0^{V_{dc}/2} C_{oss,S1}(v)dv + \int_{V_{dc}/2}^{0} C_{oss,D1}(v)dv + \int_{V_{dc}/2}^{V_{dc}} C_{oss,D2}(v)dv}{I_{in}} = \frac{Q_{oss}}{I_{in}} \quad (48),$$

where $Q_{oss}$ is the total charge replenished or discharged by the input curremt. $t_{ds,r}$ is inversely proportional to input current.

### *3.5.2 A Control Method for Compensating the Turn-off Delay*

The voltage-second loss can be compensated by turning-off the MOSFETs earlier, which is illustrated in Fig. 3-34. The compensation time $t_{comp}$ satisfies:

$$t_{comp}V_{DC} + \int_0^{t_{ds,r}} v_{ds}(t)dt = t_{delay}V_{dc} = (t_{gs,f} + t_{ds,r})V_{dc} \quad (49).$$

The integral $\int_0^{t_{ds,r}} v_{ds}(t)dt$ is proportional to input current $I_{in}$ , i.e. it can be expressed as:

$$\int_0^{t_{ds,r}} v_{ds}(t)dt = \frac{h_{comp}}{I_{in}} \quad (50),$$

where $h_{comp}$ is constant and can be calculated offline. Therefore, the compensation time is calculated by:

$$t_{comp} = t_{gs,f} + t_{ds,r} - \frac{\int_0^{t_{ds,r}} v_{ds}(t)dt}{V_{dc}} = t_{gs,f} + \frac{Q_{oss}}{I_{in}} - \frac{k_{comp}}{V_{dc}I_{in}} = t_{gs,f} + \frac{1}{I_{in}}(Q_{oss} - \frac{h_{comp}}{V_{dc}}) = t_{gs,f} + \frac{k_{comp}}{I_{in}} \quad (51),$$

where $t_{gs,f}$ is determined by gate driver design and is almost constant, and $Q_{oss} - \frac{h_{comp}}{V_{dc}}$ can be calculated offline.

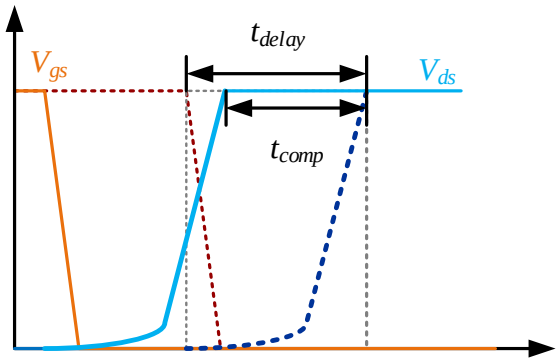



**Fig. 3-34. Basis of the compensation: predicting the delay time and shifts the gate signal.**

A feedforward loop is proposed to compensate the turn-off delay to enhancing power quality. The loop is highlighted in the control block diagrams in Fig. 3-35. The compensation loop uses input current information and (EQU) to calculate the turn-off compensation time, and the result is added to the turn-off time calculated by the modulator.

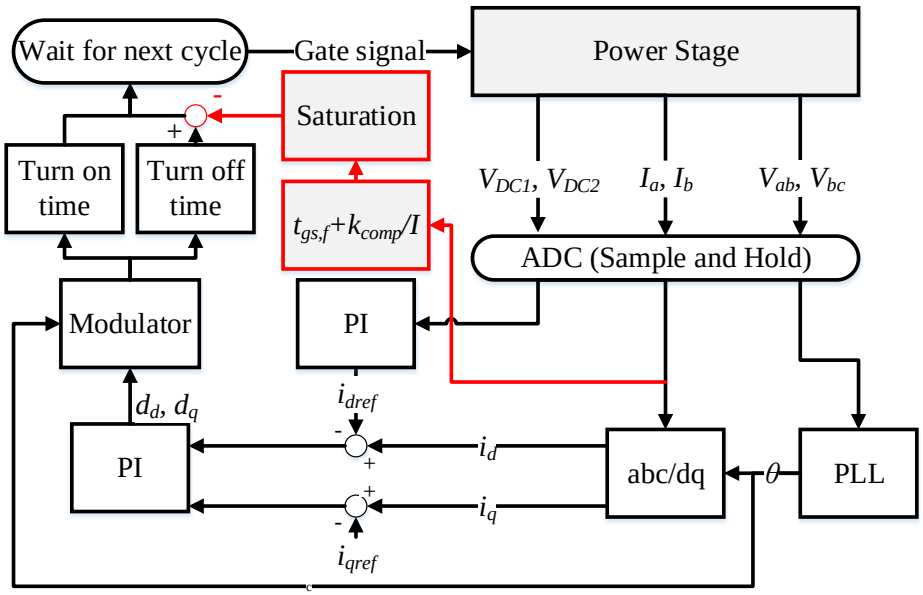
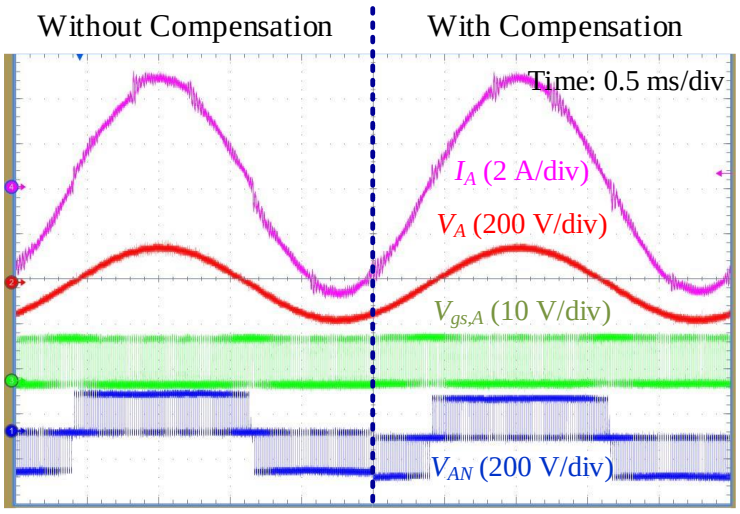
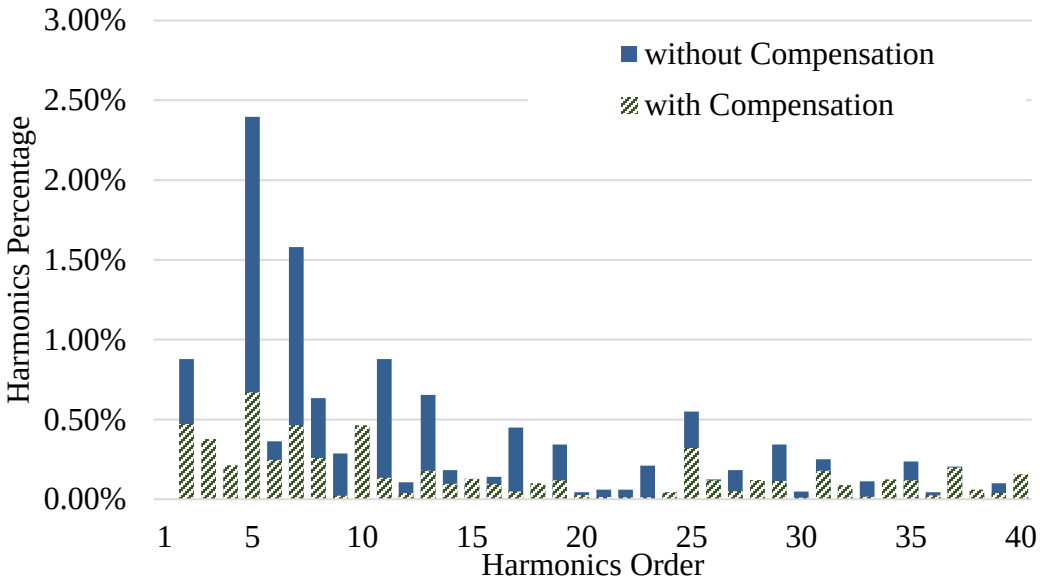



**Fig. 3-35. Block diagram of the control system. The proposed feedforward compensation loop is highlighted.**

Experiments with and without the turn-off compensation loop under full and half load conditions are conducted. Fig. 3-36 (a) shows the waveforms under 400 Hz input, full load condition while Fig. 3-37 (a) shows the half load condition tests. The harmonics spectrums are summarized in Fig. 3-36 (b) and Fig. 3-37 (b), and it is observed that the 5$^{th}$ and 7$^{th}$ harmonics reduce significantly by applying the compensation. Without the compensation, the 5$^{th}$ and 7$^{th}$ harmonics are 2.4 % and 1.6 % of the the fundamental component under full load, and they reduces to 0.7 % and 0.5 % under full load with the compensation. For the half load operation, the 5$^{th}$ and 7$^{th}$ harmonics changes from 7.1 % and 4.5 % to 1.8 % and 1.7 %. The total harmonics distortion (THD) is improved from 3.6 % to 1.7 % under full load, and from 9.7 % to 4.1 % under half load. The testing results shows the validity of the proposed method.

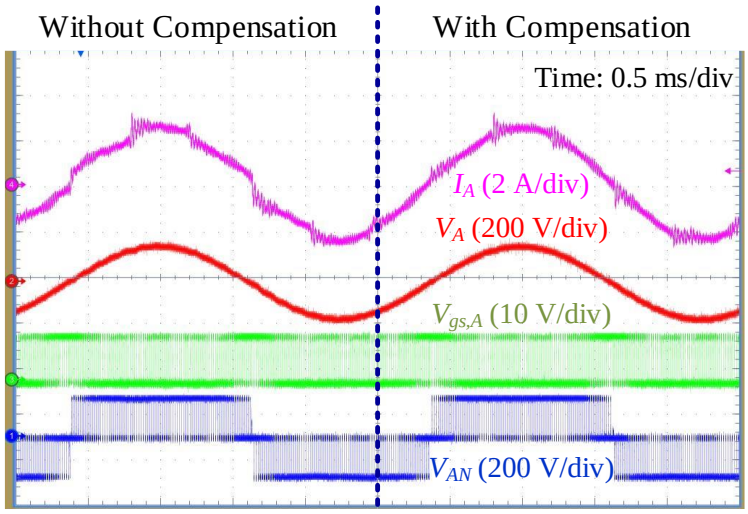



**(a)**

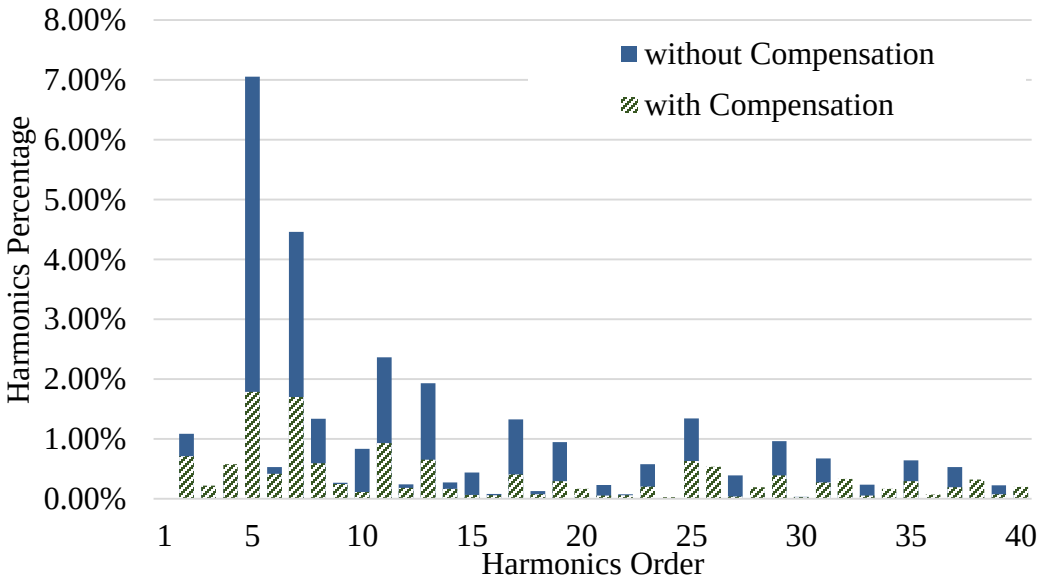



**(b)**

**Fig. 3-36. Input current waveforms and its spectrum with and without the proposed compensation method under full load 400 Hz input frequency. (a) The waveforms. (b) The spectrums.**




**(a)**




**(b)**

**Fig. 3-37. Input current waveforms and its spectrum with and without the proposed compensation method under half load 400 Hz input frequency. (a) The waveforms. (b) The spectrums.**

## 3.6 Chapter Conclusion

This chapter presents the design framework for nominal power maximization based on BLPP. This approach not only finds the optimal design but also renders fair comparison of converter topologies. The design of an active front-end converter is investigated using the framework. The Vienna rectifier achieves 1200 W design while the two-level boost rectifier achieves 1000 W design. The 1200 W Vienna rectifier prototype meets the form factor, loss constraints and complies with the DO-160E EMI and power quality standards, which verifies the design framework and models used in the the design. The prototype achieves 98.5 % full load efficiency and 33 W/in$^3$ power density, and it is natural convection cooled.

A control method is proposed to compensate the MOSFET turn-off delay in the prototype, which improves the power quality. The method uses datasheet information and is implementation-friendly to microcontroller. A feedforward loop is added to the control system, enabling online turn-off delay compensation. The effectiveness of the method is experimentally verified: under full load condition, the input current THD is improved from 3.6 % to 1.7 %; under half load, the input current THD is improved from 9.1 % to 4.7 %.

# Chapter 4. Two-Stage Three-Phase Isolated AC/DC Converter

## 4.1 Chapter Introduction and Prior Art

This chapter focuses on the design and optimization of a modular rack-mount isolated AC/DC converter for aerospace applications. Similar to the previous design, the converter form factor is given by the dimensions of the chassis. For system-level integration, total converter loss and cooling method, in addition to form factor, are predefined, and the converter nominal power is not specified but to be maximized. Detailed specifications, as well as electromagnetic interference (EMI) and power quality standards, are listed in TABLE IV.

**TABLE IV. CONVERTER SPECIFICATIONS**

| | | | |
|---|---|---|---|
| Nominal Power | TBD | Form Factor | 60 in2 x 1 in |
| Input Voltage | 3-Phase 115 V | EMI Standard | DO-160E [6] |
| Input Frequency | 360 Hz ~ 800 Hz | Power Quality Standard | DO-160E |
| Output Voltage | 28 V | Cooling | Natural Convection |
| Loss Budget | 35 W | Galvanic Isolation | Yes |

To perform the required function, either a one-stage structure [121-127] or a two-stage structure [24, 128, 129], where front-end converters join with DC/DC converters, is applicable. Though most single-stage structures eliminate the internal DC bus capacitor (Ref. [125] is an exception), they usually require more semiconductor devices and complex control owning to the matrix-type operation [124]. Furthermore, these implementations suffer from low efficiency (with 95.5 % efficiency in [125] being the highest reported) and high total harmonic distortion (THD)

(usually greater than 5 %). Therefore, the two-stage structure, of which the two stages are well developed, is adopted in this design and its schematic is depicted in Fig. 4-1.

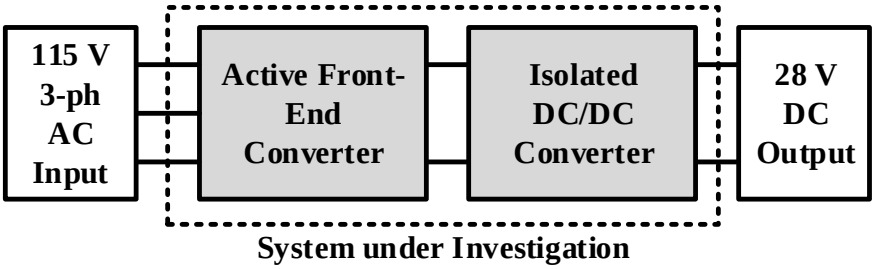



**Fig. 4-1. System under investigation. The two-stage system consists of an active front-end converter and an isolated dc/dc converter in a cascaded configuration.**

Although two-stage structure is widely used (e.g. power supplies in data centers), most literatures focus on design of a single stage assuming that the internal dc bus decouples the design [105, 130]. This chapter uses the bi-level programming problem (BLPP) to structure the design problem, which enables concurrent design and optimization of the two stages as well as all component. Furthermore, with the aforementioned design approach, the impact of DC bus voltage, a key parameter to both stages, is studied. Authors of [128] have investigated the influence of internal DC bus voltage on efficiency of a two-stage battery charger for electric vehicles. It is observed in [128] that, comparing with a 600 V constant DC bus voltage, a maximum of 2 % efficiency improvement is achieved by varying the voltage. Similar observations and approach have been reported in [129], where the authors deliberately varies the DC bus voltage to facilitate the design of second-stage converter. Efficiency improvement is achieved by operating the second-stage resonant converter close to its resonant frequency. Unlike [128, 129] where the battery charger application calls for wide-range output voltage, this work deals with fixed output voltage, and the objective is to maximize nominal power. This chapter investigates the issue by setting the

DC bus voltage as a design variable rather than a constant. The impact is revealed by sweeping the voltage and comparing the performance.

## 4.2 Nominal Power Maximization of Two-Stage Form-Factor-Constrained Converter

The nominal power maximization framed by BLPP is discussed in section 3.2. This chapter uses similar approach to convert the nominal power maximization problem to a loss-size multi-objective optimization problem. Besides, to tackle the two-stage converter issue, an additional layer of BLPP problem is added between system-level loss-size optimization and loss-size optimization of a single converter, and this additional BLPP layer is detailed in this section.

### *4.2.1 BLPP for Two-Stage System Loss-Size Multi-Objective Optimization*

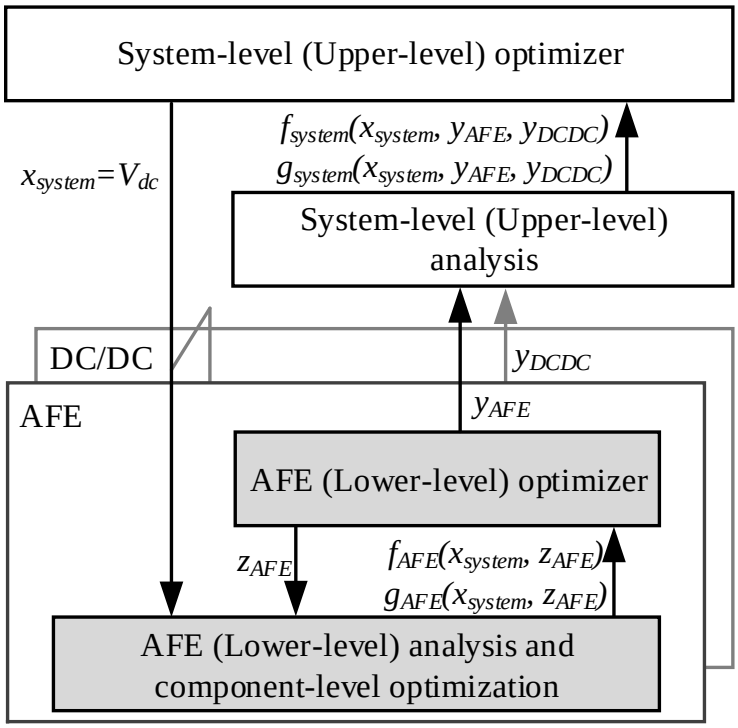



**Fig. 4-2. BLPP for the two-stage converter design. Specifying dc bus voltage by system-level optimizer decouples the converter-level designs.**

The loss-size optimization of the two-stage system is first decomposed into system-level (upper-level) and converter-level (lower-level) design, and then into converter-level (upper-level) and component-level (lower-level) design so that all lower-level designs are optimized locally and concurrently. The first decomposition distributes the design from the two-stage system to the design of AFE and isolated dc/dc converter separately and is depicted in Fig. 4-2. The system-level (upper-level) design specifies the dc bus voltage, with which the design of the two cascaded converter stages are decoupled. In this two-stage system, dc bus voltage greatly influences the functionality and performance of both stages. It should be higher than the input peak line-to-line voltage (in this case, 283 V) to avoid modulation saturation of AFE [131]. It should allow the second-stage LLC resonant converter to operate close to its resonant frequency, where the nominal

voltage gain is unity [132]. Furthermore, as dc bus voltage increases, it induces severer EMI noise and more semiconductor stress [79, 119, 133]. Therefore, the dc bus voltage candidates are selected to be 310 V, 340 V, 370 V and 400 V. These voltage levels are close to multiples of 28 V output nominal voltage, e.g. 340 V is close to 12 times of 28 V, and they facilitates transformer design in the isolated dc/dc converter.

The system-level optimization problem is formulated as:

$$\begin{aligned}&\min f_{system}(p_{nominal}, x_{system}, y_{AFE}, y_{DCDC})\\&=[P_{loss,AFE}(p_{nominal}, x_{system}, y_{AFE}) + P_{loss,DCDC}(p_{nominal}, x_{system}, y_{DCDC})\\&A_{AFE}(p_{nominal}, x_{system}, y_{AFE}) + A_{DCDC}(p_{nominal}, x_{system}, y_{DCDC})]^T\end{aligned} \quad (52),$$

$$\text{where } x_{system} = V_{dc} \quad (53),$$

$$\text{s.t. } g_{system}(p_{nominal}, x_{system}, y_{AFE}, y_{DCDC}) \le 0 \quad (54),$$

where $x_{system}$ is the system-level design vector and equals to dc bus voltage, $y_{AFE}$ and $y_{DCDC}$ are the solutions to the optimization of AFE and dc/dc converter, $P_{loss,AFE}$ and $P_{loss,DCDC}$ represents loss of AFE and dc/dc stage, $A_{AFE}$ and $A_{DCDC}$ represents footprint area of AFE and dc/dc stage, and $g_{system}$ $(p_{nominal}, x_{system}, y_{AFE}, y_{DCDC})$ represents all the system-level design constraints (e.g. EMI noise of the two-stage converter) except loss and form factor limitations.

### *4.2.2 BLPP for AFE and dc/dc Converter Loss-Size Multi-Objective Optimization*

Design of AFE and dc/dc converter share the same framework, and it is discussed in section 3.2.2.

### *4.2.3 Overall Optimization Framework and Implementation*

Combining the aforementioned optimization frameworks renders the overall framework for nominal power maximization, and it is depicted in Fig. 4-3. The upper section of Fig. 4-3 depicts the design flow while the lower depicts expected results. The optimization results of component-level design are Pareto fronts demonstrating the loss-size tradeoff of the specific component with certain converter-level (AFE or dc/dc) parameters. Integrating the Pareto optimal component designs renders Pareto optimal converter designs. Similarly, integrating the Pareto optimal converter designs renders Pareto optimal two-stage system design. The nominal power optimizer checks if the Pareto optimal system designs comply with the form factor and loss budget constraints, and the maximal nominal power and final valid designs are found accordingly.

The literature review on optimization algorithms is presented in section 3.2.3. Direct search is applied herein.

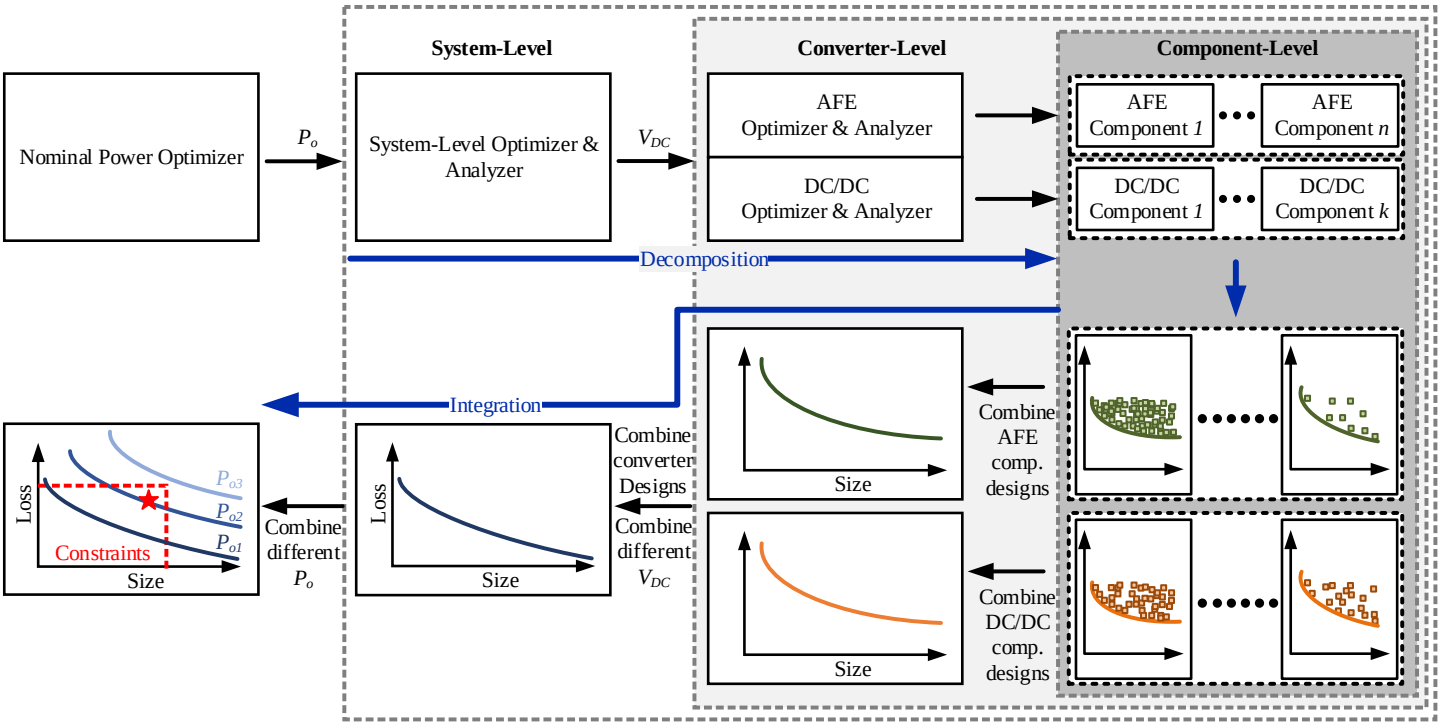
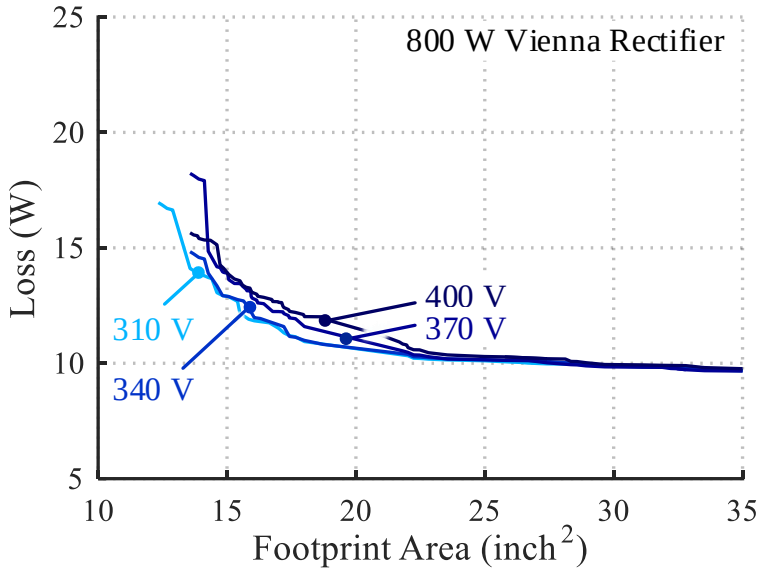



**Fig. 4-3. Overall optimization framework for and expected results of nominal power maximization.**

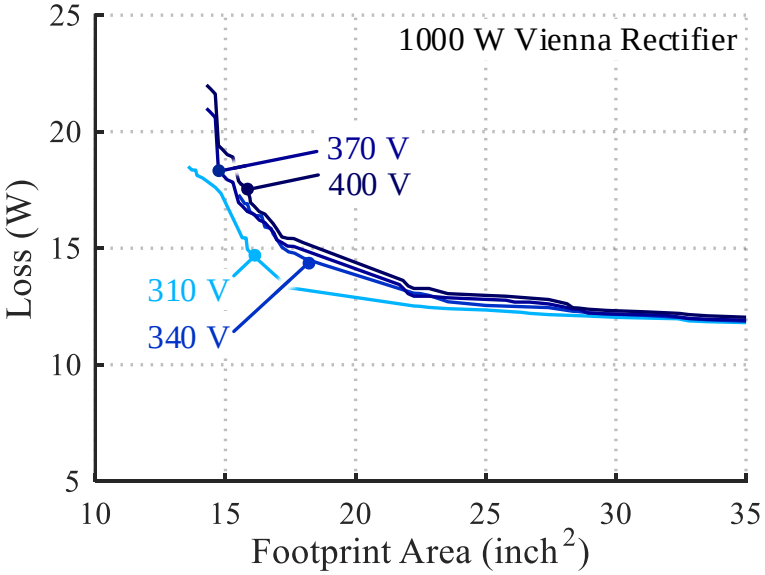
## 4.3 Design of Active Front-End Converter

The design procedure of active front-end converter is discussed in section 3.3. In this chapter, Vienna rectifier is selected for AFE converter thanks to its good performance (discussed in section 3.3). Different from the last chapter, the dc bus voltage in this design is a design variable from the system level. The impact of dc bus voltage is discussed in this chapter.

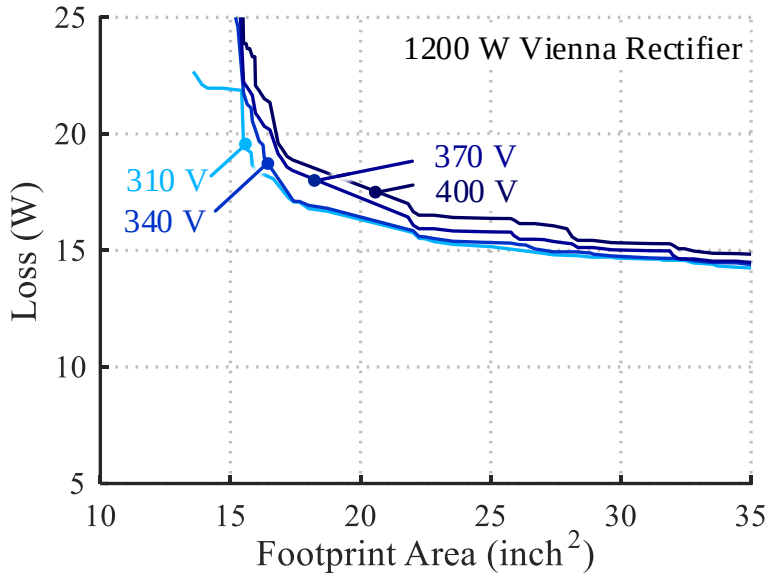
Detailed converter-level and component-level design procedure is shown in Fig. 3-5. Multiple loss-size Pareto fronts are generated under various dc bus voltages and the results are summarized in Fig. 4-4. As shown in Fig. 4-4 (a), design results with the four dc voltages and 800 W nominal power demonstrates similar performance. As nominal power increases (Fig. 4-4 (a) through Fig. 4-4 (d)), designs with higher dc voltages shows more loss with the same footprint area.


800 W Vienna Rectifier
Loss (W)
Footprint Area (inch$^2$)
310 V
340 V
370 V
400 V
25
20
15
10
5
10
15
20
25
30
35

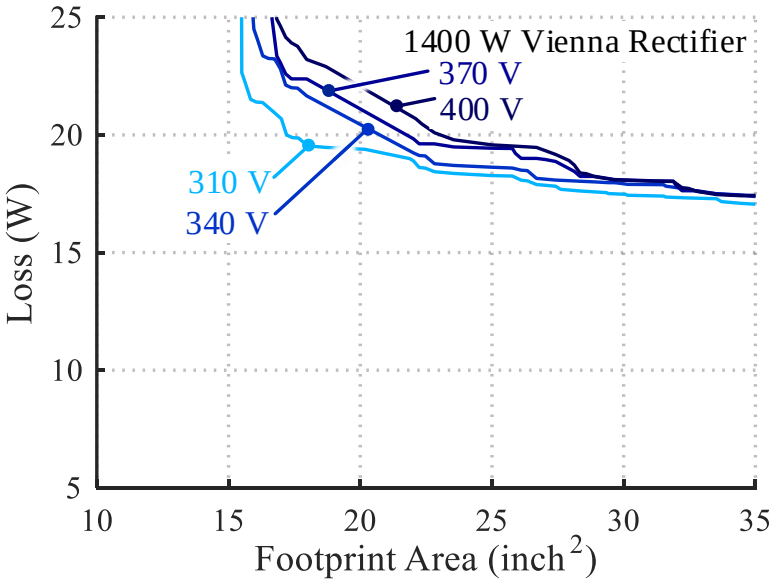
**(a)**


1000 W Vienna Rectifier
Loss (W)
Footprint Area (inch$^2$)
310 V
340 V
370 V
400 V
25
20
15
10
5
10
15
20
25
30
35

**(b)**




**(c)**




**(d)**

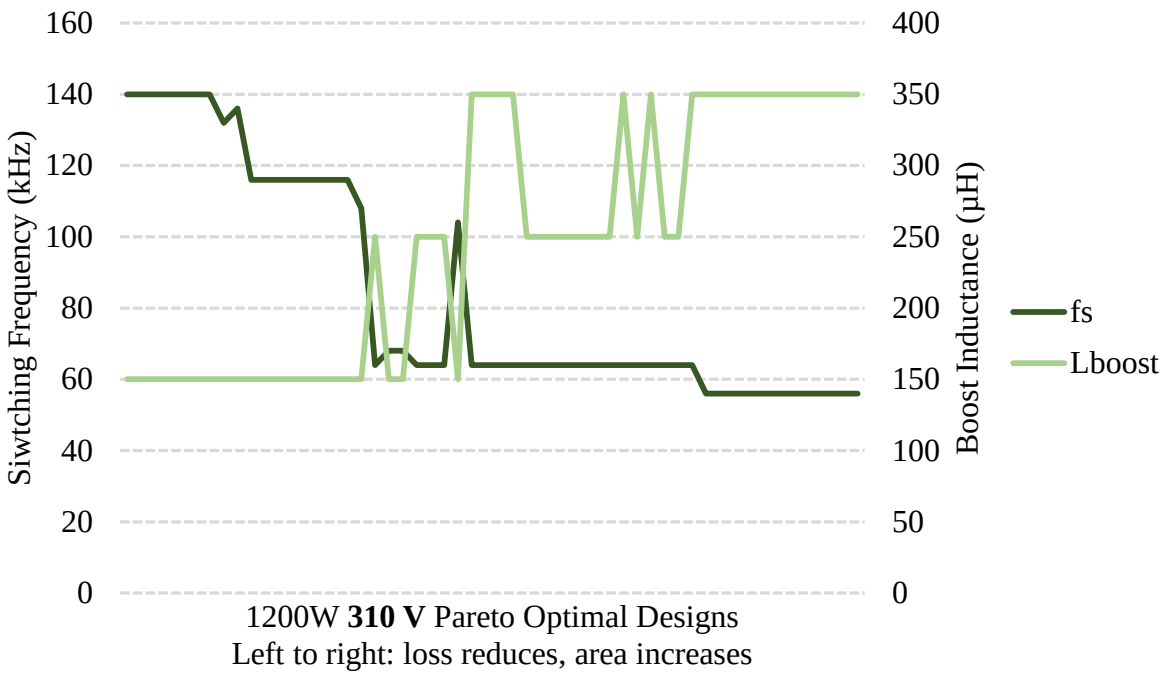
**Fig. 4-4. Pareto fronts of Vienna rectifier under various nominal power (800 W ~ 1400 W) and dc bus voltages (310 V to 400 V). (a) 800 W designs. (b) 1000 W designs. (c) 1200 W designs. (d) 1400 W designs.**

The dc bus voltage influences loss distribution and EMI filter design, thus resulting in different performance. Its impact can be perceived by comparing the design details of Pareto optimal designs with 310 V and 400 V dc bus voltage under 1200 W nominal power. The switching

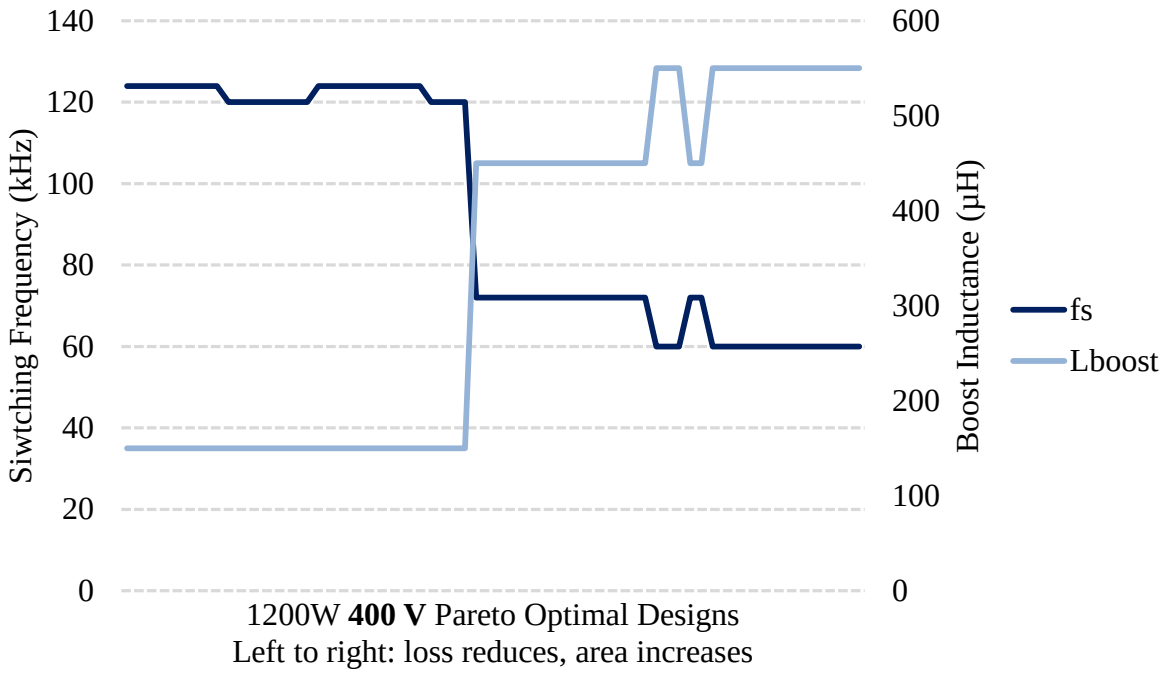
frequency and boost inductance of the Pareto optimal designs are shown in Fig. 4-5, and the percentagewise loss breakdown is shown in Fig. 4-6.

The designs with the two dc bus voltage levels use similar switching frequencies, i.e. they use switching frequency over 100 kHz to achieve high power density and use switching frequency close to 60 kHz to achieve high efficiency. However, the boost inductance in 400-V designs is larger than that of 310-V designs, leading to higher loss if the same core is used (as is observed in Fig. 4-6).

Besides increased boost inductor loss, 400-V designs generate higher switching loss owning to higher switching voltage. However, as modulation index in 400-V designs is smaller than that of 310-V designs, diode conduction time in 400-V designs is shorter, and MOSFETs conduct with longer time in 400-V designs. Therefore, 400-V designs have lower diode conduction loss and higher MOSFET conduction loss than their 310-V counterparts. In 800-W and 1000-W designs where the MOSFET conduction property prevails that of diodes, the reduced diode conduction loss compensates the increased boost inductor, MOSFET switching and MOSFET conduction loss, and designs with different dc bus voltages present similar performance. As dc bus voltage increases, the loss increase from the aforementioned components exceeds the loss reduction from diodes, thus designs with lower dc bus voltage achieve lower loss with the same footprint area.

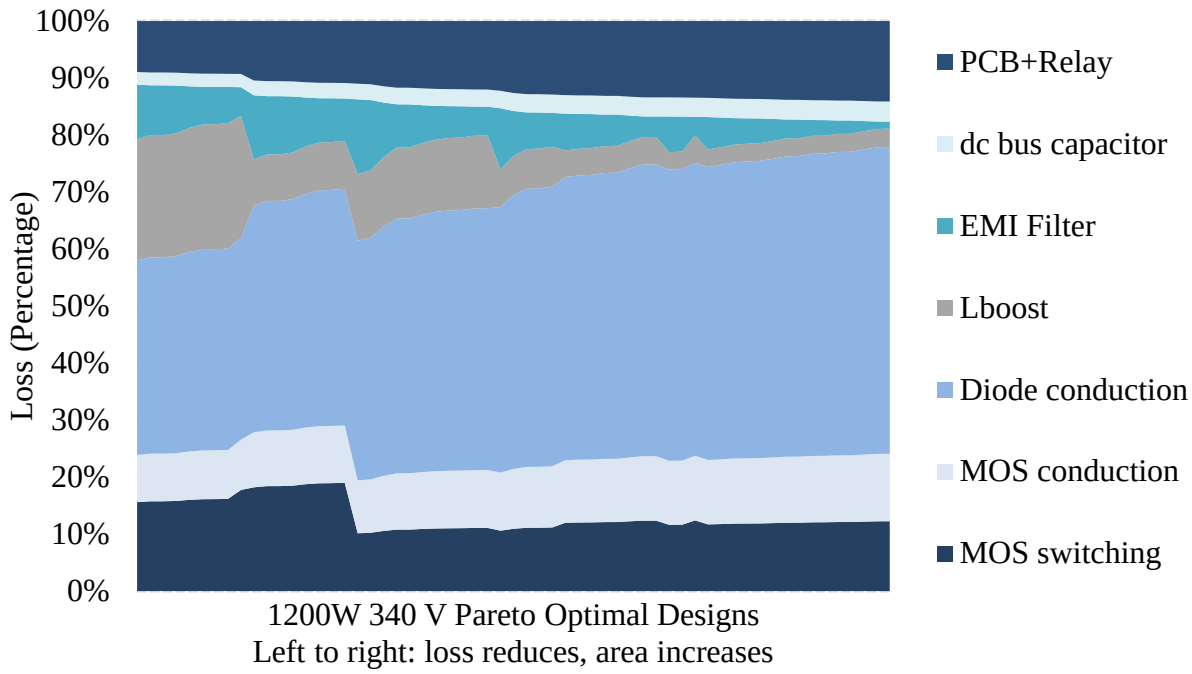



**(a)**

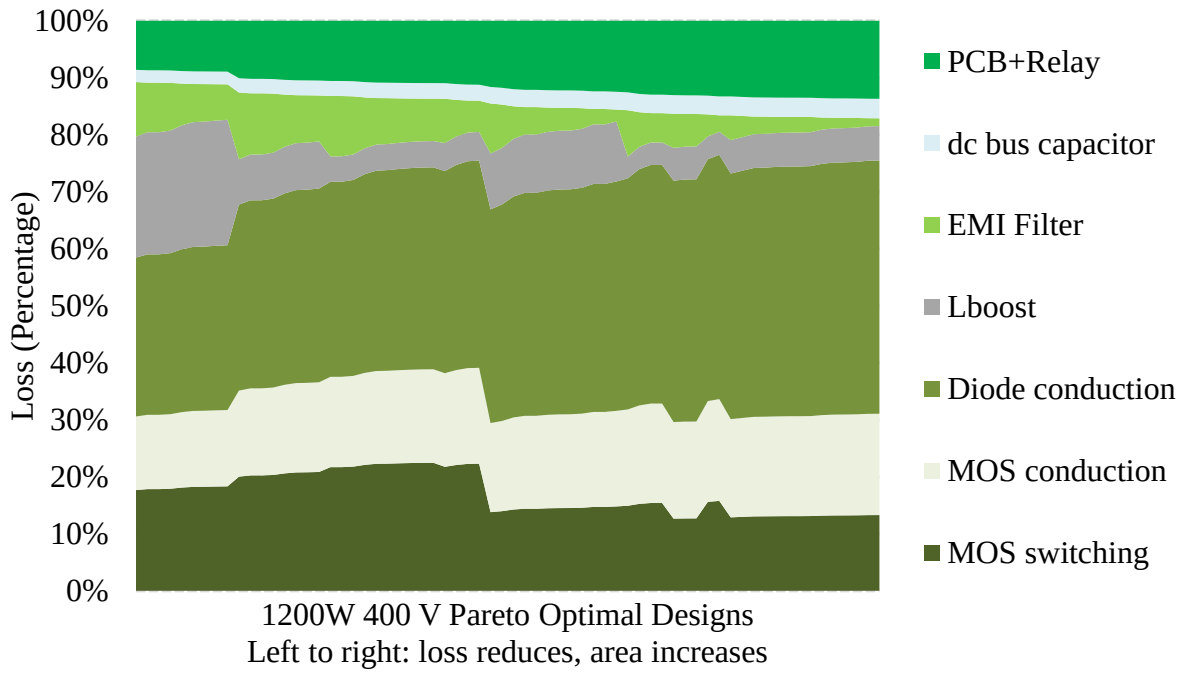



**(b)**

**Fig. 4-5. Switching frequency and boost inductance of Pareto optimal designs of 1200 W Vienna rectifier with different dc bus voltage. (a) 310 V dc bus voltage. (b) 400 V dc bus voltage.**




**(a)**




**(b)**

**Fig. 4-6. Percentagewise loss breakdown of Pareto optimal designs of 1200 W Vienna rectifier with different dc bus voltage. (a) 310 V dc bus voltage. (b) 400 V dc bus voltage.**

## 4.4 Design of Isolated DC/DC Converter

For isolated DC/DC converter stage, LLC resonant converter operating as DC transformer were selected as topology candidates. The regulation of output voltage is guaranteed by regulation of internal dc bus. The circuit schematic is shown in Fig. 4-7. Detailed design and optimization is depicted as block diagrams in Fig. 4-8. Both converter-level and component level designs are shown.

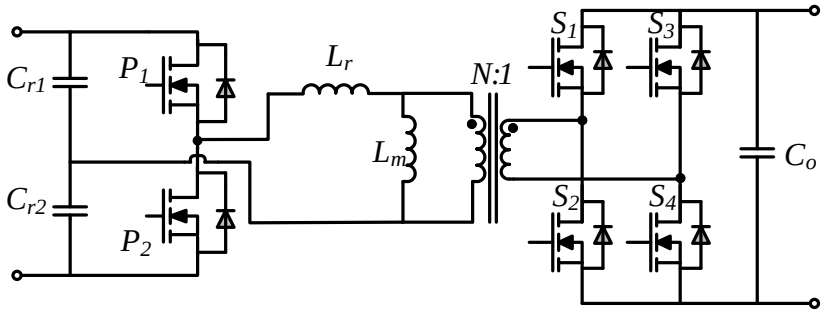



**Fig. 4-7. LLC resonant converter schematic.**

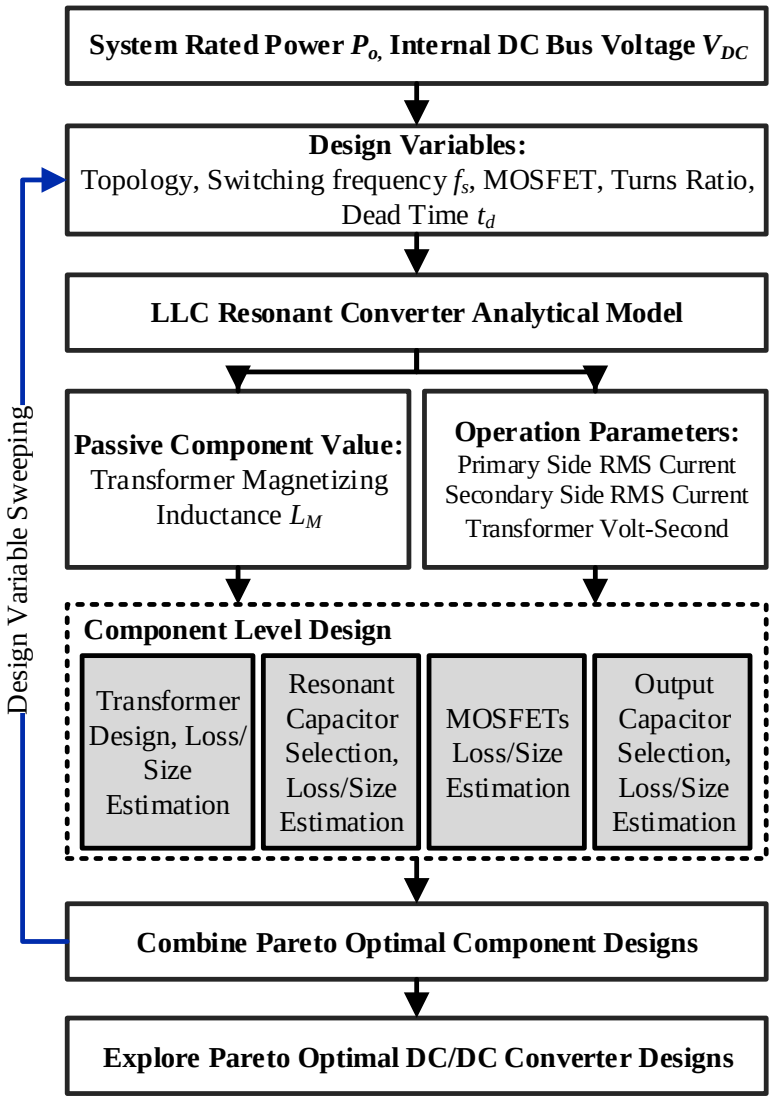



**Fig. 4-8. DC/DC stage converter-level and component-level design procedure based on BLPP.**

### *4.4.1 Converter-Level Design of Isolated DC/DC Converter*

The basic design principles for LLC resonant converters have been presented in [134-136]. Some of the key equations are included here for better understanding of the design procedure and design variable selection. For an LLC resonant converter, to achieve ZVS for primary side

MOSFETs, magnetizing inductance $L_m$ and dead time $t_d$ should satisfy (55) to ensure that primary side MOSFETs are fully charged and discharged during voltage transition period [135].

$$L_m \le \frac{T_s t_d}{16 C_{oss,pri}} \tag{55}$$

where $T_s$ is the switching period and $C_{oss,pri}$ is the total time-equivalent output capacitance of primary side MOSFETs. Moreover, it is claimed in [135] that, to minimize primary side RMS current, $L_m$ should be as large as possible. For an LLC resonant converter, the transformer magnetizing inductance is designed so that:

$$L_m = \frac{T_s t_d}{16 C_{oss,pri}} \tag{56}$$

Considering the primary side dead time and the relationship described in (56), primary side RMS current $I_{RMS,pri}$ (RMS current flows through resonant tank) and secondary side RMS current $I_{RMS,sec}$ can be expressed as:

$$I_{RMS,pri} = \frac{1}{4\sqrt{2}} \frac{V_o}{n R_L} \sqrt{\frac{256 n^4 {C_{oss}}^2 {R_L}^2}{{t_d}^2} + 4\pi^2 + \frac{16\pi^2 (T_s t_d + {t_d}^2)}{{T_s}^2}} \tag{57}$$

$$I_{RMS,\sec} = \frac{\sqrt{3}}{24\pi} \frac{V_o}{R_L} \sqrt{\frac{(5\pi^2 - 48) n^4 {R_L}^2 {T_s}^3}{{L_m}^2 (T_s + 2t_d)} + \frac{12\pi^4 T_s}{T_s + 2t_d} + \frac{48\pi^4 ({t_d}^2 + t_d T_s)}{T_s (T_s + 2t_d)}} \tag{58}$$

where $V_o$ is the output voltage, $n$ is turns ration of the transformer, $R_L$ is the load resistance and $L_m$ satisfies (56). Equation (3) and (4) illustrate that, with determined switching frequency, primary side dead time, output capacitor of primary side MOSFETs and operation point, primary side and secondary side RMS current can be analytically calculated. The converter loss can be estimated

based on the calculated RMS current. Therefore, besides converter topology, the other design variables in converter level design of DC/DC stage should be: switching frequency, primary side dead time and MOSFET selection. For design variable candidates, switching frequency is swept from 20 kHz to 140 kHz. 1200 V SiC MOSFETs and 600 V Si MOSFETs are considered as primary side MOSFET candidates for LLC resonant converter. Primary side dead time is swept from 1% of switching period to 10% of switching period.

### *4.4.2 Component-Level Design of Isolated DC/DC Converter*

In DC/DC converter component-level design, loss and size from MOSFETs, transformer, resonant capacitors and output capacitors in a LLC converter is modeled and estimated. With primary side and secondary side RMS current calculated in converter-level design, conduction loss from MOSFETs could be estimated. Switching loss from MOSFETs are estimated based on double pulse tests. Thanks to the zero-voltage-switch characteristic of primary side switches and zero-current-switch characteristic of secondary side MOSFETs, only turn-off loss from primary side MOSFETs are considered.

Transformer in an LLC resonant converter consumes considerable loss and takes a large portion of size. Special attention has been paid to its optimization. An optimization loop, where transformer core dimensions are taken as design variables, was developed to explore the loss-size Pareto fronts of the transformer. The core shape and the dimension of the transformer core that are taken as design variables are shown in Fig. 4-11. The turn ratio is determined by dc bus voltage. For 310 V, 340 V, 370 V and 400 V design, the turn ratio is 5.5:1, 6:1, 6.5:1 and 7:1, respectively.

For 310 V and 370 V design, secondary side turn number should be even so that primary side turn number is integer.

The conduction loss of transformer is one of the major losses in this converter. Owning to skin and proximity effects, conduction loss of transformer windings cannot be directly calculated using the winding DC resistance. To minimize transformer ac winding loss, litz-wire is used to implement both primary side and secondary side windings. Models for litz-wire transformer winding AC resistance calculation developed in Ref. [64] are adopted to calculate winding conduction loss analytically. Ref. [64] sinusoidal current with peak value $I_{peak}$, immersed in a changing magnetic field with flux claimed that the total ac loss of litz-wire with length $l$, number of strands $N$, diameter per strand $d$, conducting density $B$ (field generated by neighboring litz-wire bundles) can be expressed as:

$$P_{AC} = \frac{\pi l N d^4 \sigma}{64} \left\langle \left[ \left( \frac{dB}{dt} \right)^2 \right] \right\rangle \quad (59),$$

where σ is the conductivity of the conductor, [·] represents time average, <·> represents spatial average. Furthermore, with the consideration of flux generated by the bundle itself, a more complete ac loss expression can be got [137]:

$$P_{AC} = \frac{\pi l N d^4 \sigma}{64} \left( \left\langle \left[ \left( \frac{dB}{dt} \right)^2 \right] \right\rangle + \frac{I_{peak}^{\ 2}}{2\pi^2 d_{bundle}^{\ 2}} \right) \quad (60),$$

where $d_{bundle}$ is the diameter of the whole litz-wire bundle.

The analytical method needs the knowledge of magnetic field distribution within the window area of transformer. The distribution can be accurately calculated through finite element analysis

(FEA) simulation. However, for converter design/optimization purpose where cores with different dimensions and different winding structure will be examined, an analytical expression for magnetic field calculation is preferred. Herein, it is assumed that magnetic field within window area is in parallel with the legs of the cores (e.g. center leg of an E-core). Therefore, the magnetic strength distribution (proportional to the flux density) can be calculated by Ampere's law analytically (example shown in Fig. 4-9). Given core dimensions and winding structure (including strands number and strands diameter of litz-wire), winding ac loss can be analytically calculated. An example of calculated winding resistance at different frequency together with the measurement results are given in Fig. 4-10. In this example, primary side windings are implemented with 1650 strands of AWG 44 wires, secondary side windings are implemented with 2430 strands of AWG 38 wires. The core dimensions and winding arrangement are shown in Fig. 4-9. The winding resistance is the sum of primary side winding resistance and secondary side winding resistance referred to primary side and it is measured from primary side with one of the secondary side windings shorted. It can be clearly seen that the calculated resistance matches well with the measured one within the frequency range of interest, validating the model described above.

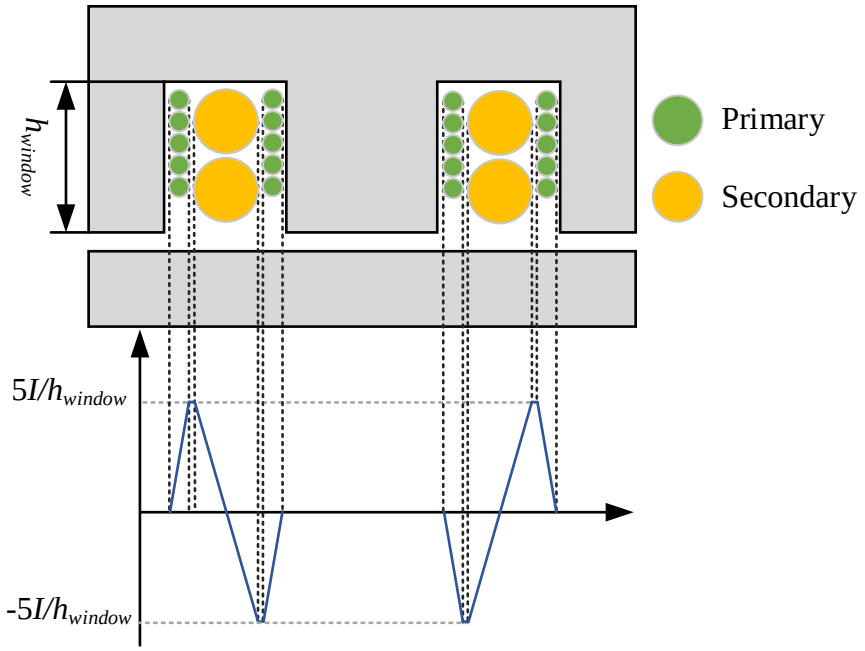



**Fig. 4-9. Estimation of magnetic field strength distribution.**

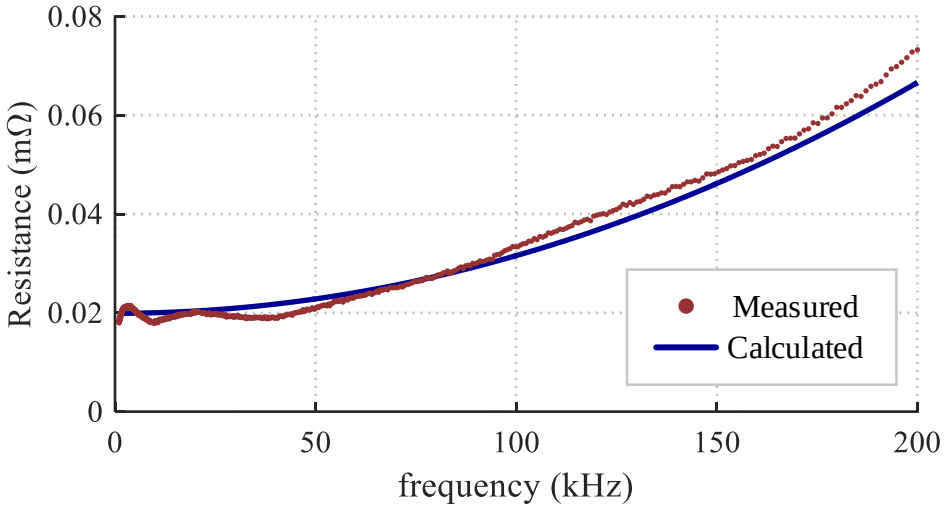



**Fig. 4-10. Relationship between AC current frequency and transformer winding resistance. blue line: value calculated from model; red dots: measured value.**

Under given operation condition, namely, primary side current, secondary side current and switching frequency, a loss-size Pareto front of the transformer can be locally identified. A transformer loss-size Pareto front example where nominal power is 1200 W, dc bus voltage is 340 V, primary side RMS current is 8.3 A, secondary side RMS current is 49 A and switching

frequency is 70 kHz is shown in Fig. 4-12. Although many design points are generated in this example, only Pareto optimal design points are kept for higher level design.

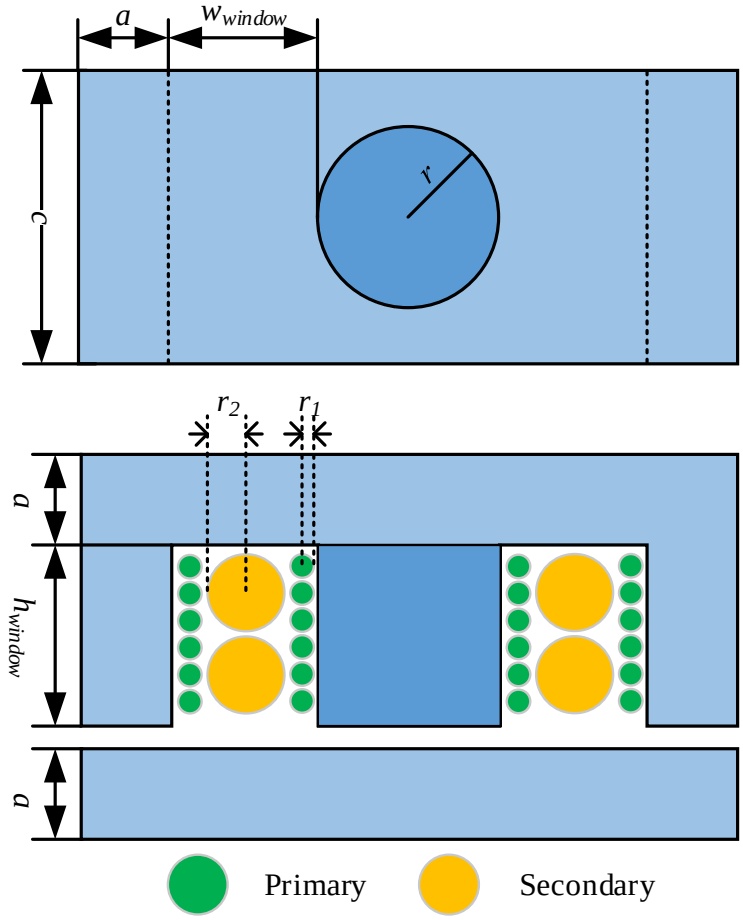



**Fig. 4-11. Design variables of transformer design. Both core dimensions and winding constructions are variable.**

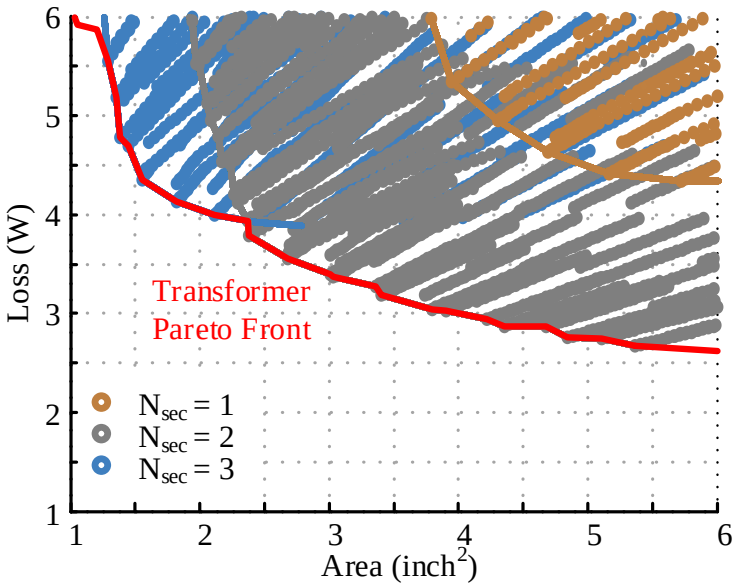


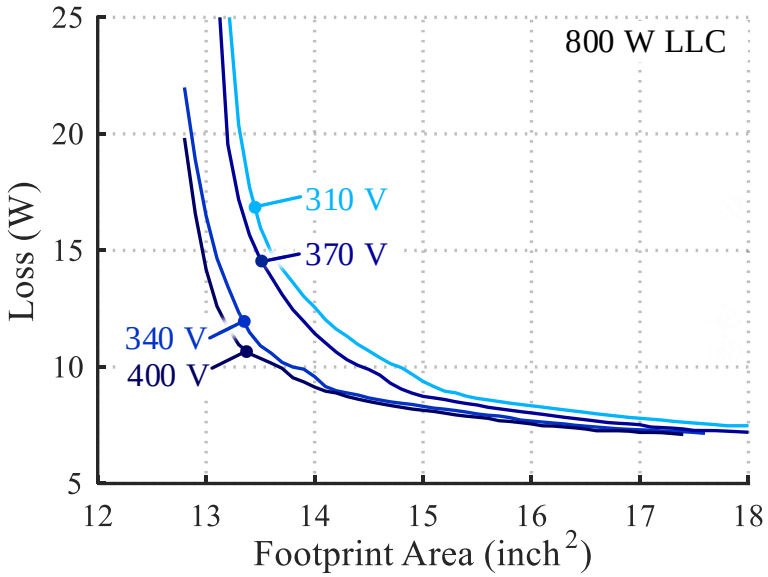

**Fig. 4-12. Loss-footprint area Pareto fronts of transformer (under certain converter-level design and operational conditions). Designs achieved by different number of secondary side winding are marked by different colors. The Pareto front is identified by designs from 2-turn designs and 3-turn-designs. The 1-turn designs present poor efficiency mainly owning to large core loss.**

### *4.4.3 DC/DC Stage Design Results*

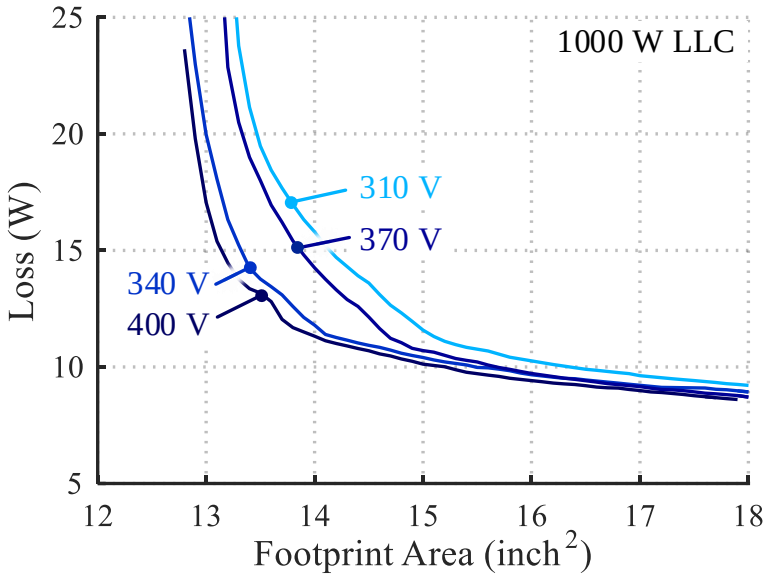
Combining Pareto optimal designs of components renders Pareto optimal dc/dc converter designs, and the loss-size Pareto fronts under various nominal power ratings and dc bus voltages are summarized in Fig. 4-13.

340 V and 400 V dc bus voltage render better designs than the other two voltage levels. In 310 V and 370 V designs, the secondary side turn number of the transformer is limited to even numbers. As the core size reduces, flux density increase and core loss increases. Total transformer loss can be reduced by increasing turn number to reduce core loss (as is observed in Fig. 4-12). However, with secondary side turn number limited to even number, 310 V and 370 V designs lack the designs achieved by using 3 turns on the secondary side and lead to higher loss.

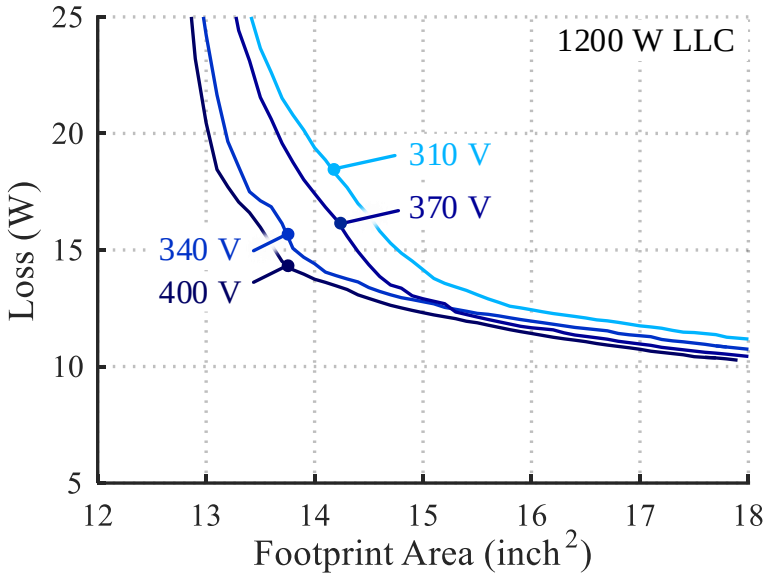
Comparing 340 V designs with 400 V designs, 340 V designs render higher loss owning to higher primary side rms current. For example, with 1200 W nominal power, 400 V design has a primary side rms current of 7.21 A while 340 V design has 8.34 A, generating 34 % more conduction loss in primary side MOSFETs. The abovementioned observation applies to comparison between 310 V and 370 V designs as well.



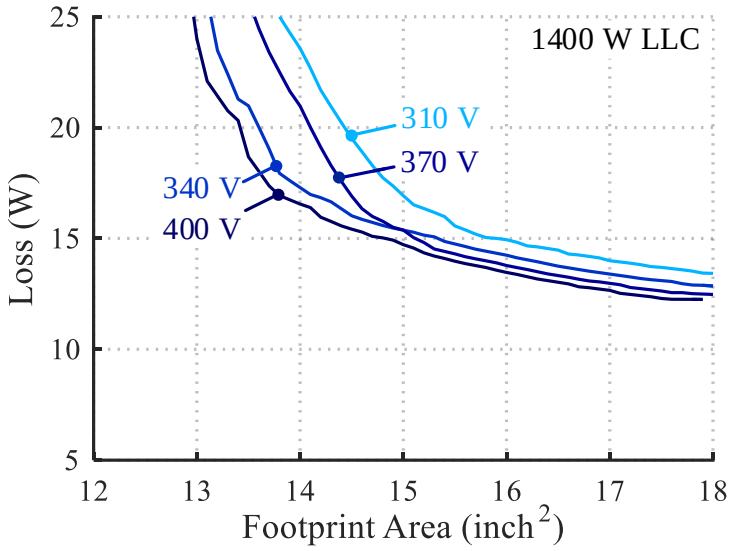

**(a)**


1000 W LLC
310 V
370 V
340 V
400 V
Loss (W)
Footprint Area (inch$^2$)
25
20
15
10
5
12
13
14
15
16
17
18

**(b)**


1200 W LLC
310 V
370 V
340 V
400 V
Loss (W)
Footprint Area (inch$^2$)
25
20
15
10
5
12
13
14
15
16
17
18

**(c)**




**(d)**

**Fig. 4-13. Pareto fronts of dc/dc converter under various nominal power levels (800 W ~ 1400 W) and dc bus voltage levels (310 V ~ 400 V). (a) 800 W designs. (b) 1000 W designs. (c) 1200 W designs. (d) 1400 W designs.**

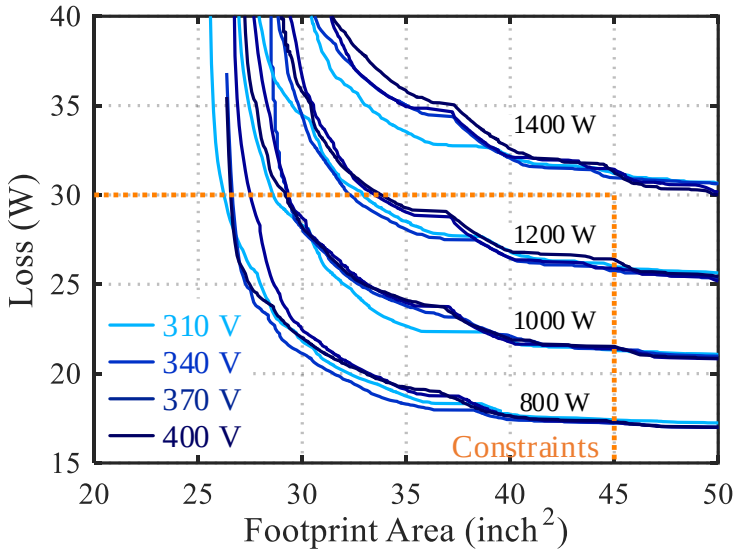
## 4.5 Design Results of the Two-Stage System

### *4.5.1 Loss-Size Pareto Fronts of the Two-Stage System*

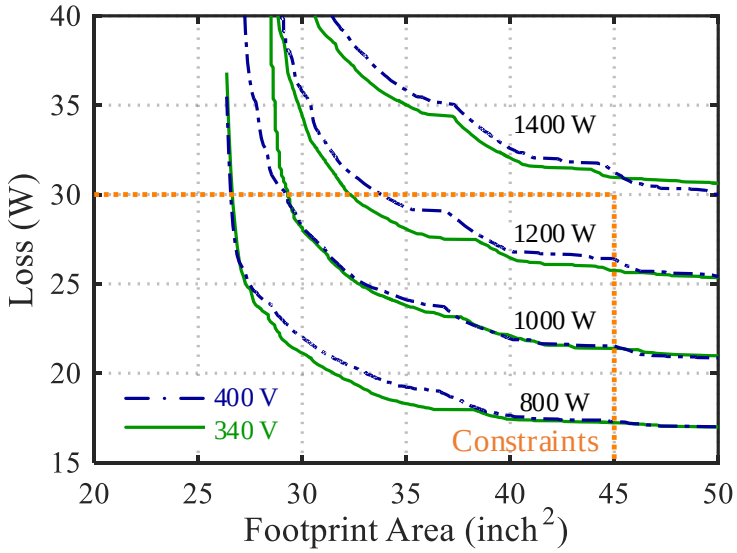
Integrating the loss-size Pareto fronts of AFE and dc/dc converter under the same dc voltage and nominal power renders the Pareto fronts of the two-stage converter. Combining Pareto fronts under the same nominal powers and different dc voltages demonstrates the influence of the dc bus voltage. Combining all Pareto fronts together and comparing them to the loss budget and form factor limits renders the maximum nominal power and feasible designs, and all the Pareto fronts as well as the loss and size constraints are depicted in Fig. 4-14 (a).

To demonstrate the influence of dc bus voltage on overall performance, Pareto fronts of 340 V and 400 V designs are summarized in Fig. 4-14 (b). Overall, they demonstrate similar performance.

As is discussed in Section III and IV, comparing with 340 V design, 400 V design leads to higher loss in AFE owning to elevated switching and EMI filter loss, and lower loss in dc/dc converter thanks to reduced conduction loss in primary side. The two factors compensate each other in the overall design, leading to similar performance.




**(a)**




**(b)**

**Fig. 4-14. Pareto frons of the two-stage system. (a) Pareto fronts of all voltage and power levels. (b) Pareto fronts of 340 V and 400 V designs.**

### *4.5.2 Detailed Design*

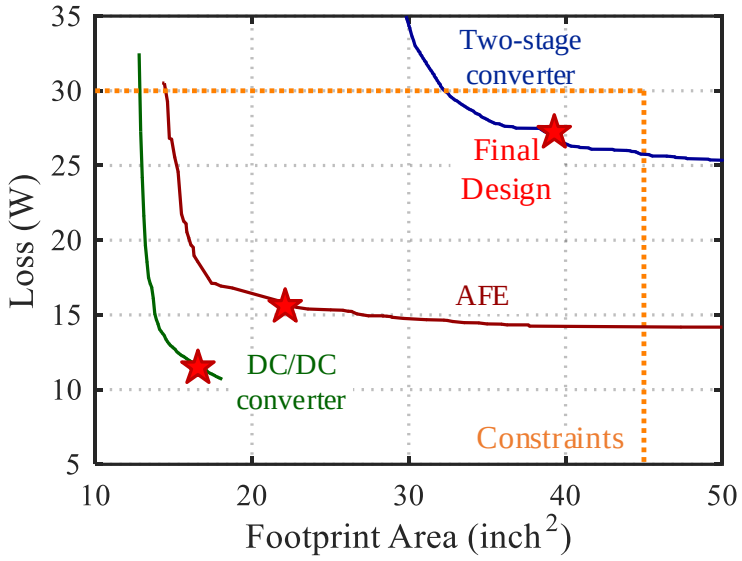



**Fig. 4-15. The final design. The final design of two-stage converter is selected first. The final design of AFE and dc/dc stage is retrieved accordingly.**

As is observed in Fig. 4-14, a nominal power of 1200 W is achievable considering all the design constraints. In the final design, a dc bus voltage of 340 V is selected considering degrading of 250 V MOSFETs while leaving enough headroom for modulation. In Fig. 4-15, the red star on two-stage converter Pareto fronts represents the final design, which gives 38.5 in$^2$ total foot print area (height of all component is lower than 0.8 in; approximately 30% more PCB area is expected in real layout) and 27.1 W loss (additional 3 W loss from auxiliary system is expected, rendering 30 W total loss). This specific design point comes from integrating a 16.1 W 22 in$^2$ AFE design (denoted by a red star on AFE Pareto front) and an 11.0 W 16.5 dc/dc converter design (denoted by a red star on DC/DC converter Pareto front). The converter schematics is shown in Fig. 4-16. The values of key design variables of the final design are listed in

TABLE V.

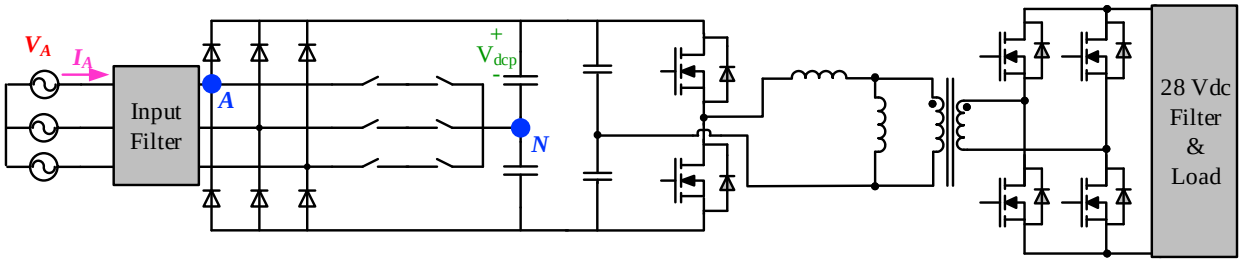



**Fig. 4-16. Converter schematics of the final design.**

**TABLE V. DETAILED CONVERTER DESIGN**

| | | | | | | |
|---|---|---|---|---|---|---|
| System Design | Rated Power | Internal DC Bus Voltage | | | | |
| | 1.2 kW | 340 V | | | | |
| Input EMI Filter | Structure | Boost Inductance | DM Filter Inductance | DM Filter Capacitance | CM Filter Inductance | CM Filter Capacitance |
| | $L_{boost}$+CLCL | 330 µH | 25 µH | 0.22 µF | 230 µH | 10 nF |
| AFE | Topology | Switching Frequency | MOSFETs | Diodes | DC Bus Capacitance | |
| | Vienna rectifier | 68 kHz | IPB200N25N | IGH20G65C5 | 15 µF | |
| DC/DC | Topology | Switching Frequency | Primary MOSFET | Secondary MOSFET | DC Bus Capacitance | |
| | LLC resonant Converter | 37 kHz | C2M0025120D | BSC010N04Ls *4 | 500 µF | |

## 4.6 Constructed Prototype and Experimental Results

Finally, a 1200 W converter prototype (picture shown in Fig. 4-17) was built and tested. This free convection cooled prototype exhibited 22 W/in$^3$ power density.

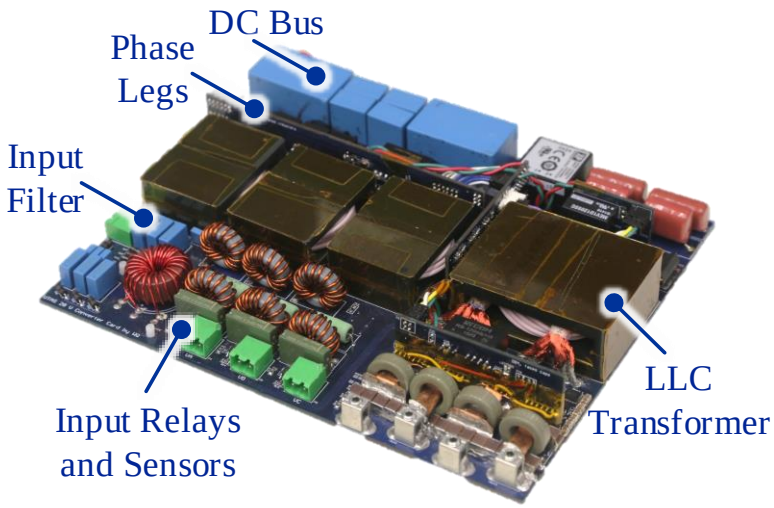
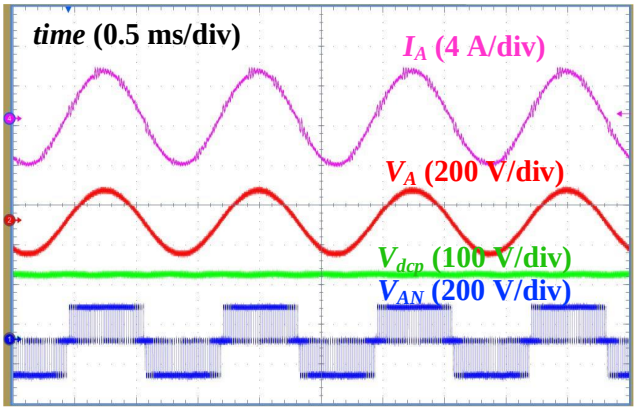


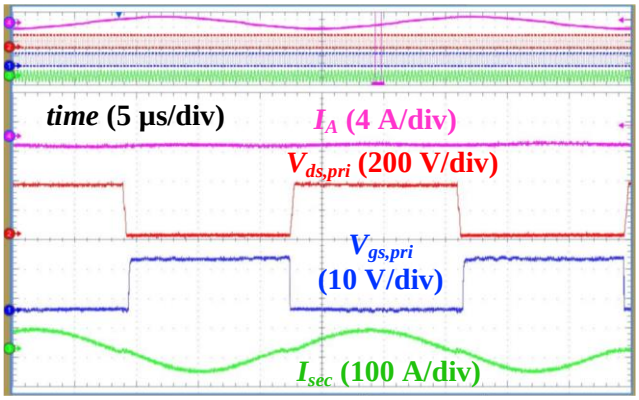

**Fig. 4-17. Converter prototype.**

Experimental waveforms of AFE stage are shown in Fig. 4-18 (a) where input current ($I_A$), input phase voltage ($V_A$), DC bus capacitor voltage ($V_{dcp}$) and phase leg output voltage referring to DC bus neutral ($V_{AN}$) were measured at full load and 800 Hz input frequency.

Experimental waveforms of DC/DC stage are shown in Fig. 4-18 (b) where input current ($I_A$), drain-to-source voltage of one of the primary side MOSFETs ($V_{ds,pri}$), the corresponding gate-to-source voltage ($V_{gs,pri}$) and secondary side current ($I_{sec}$) were measured at full load. The sero-voltage-switching of the primary side MOSFET can be observed.




**(a)**




**(b)**

**Fig. 4-18. Experimental waveforms. (a) AFE stage. (b) Isolated DC/DC stage.**

The total measured loss at full load (1.16 kW input power) at room temperature thermal steady state was 34.0 W (16.3 W from Vienna rectifier, 16.2 W from LLC converter and 2.5 W from auxiliary system if measured separately), rendering 97.1% efficiency. These results matches well with the 30 W estimated loss. All devices maintained a minimum of 20 ºC of temperature margin at full load steady state operation at lab ambient and without active cooling. The compliance with EMI (measured EMI noise spectrum is shown in Fig. 4-19) and power quality standard was experimentally verified, which validated the EMI filter design.

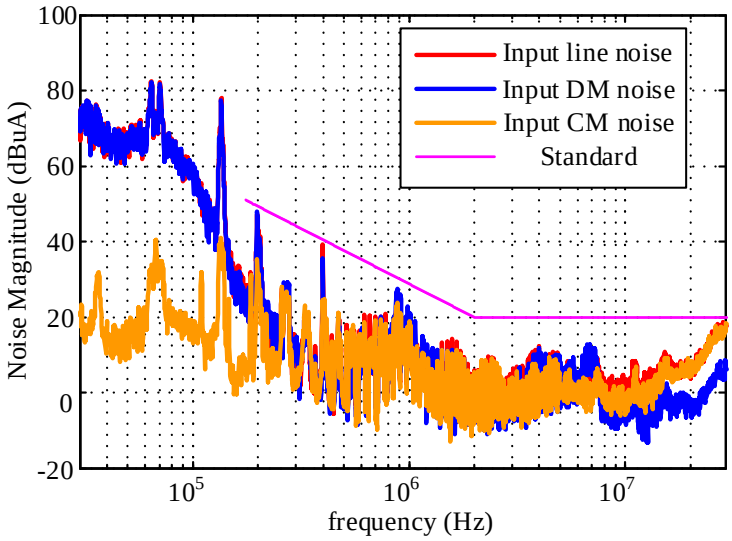



**Fig. 4-19. EMI standard and Measured EMI noise.**

## 4.7 Chapter Conclusion

The design and optimization approach for a three-phase isolated ac/dc converter is presented in this chapter. The design objective was to maximize the converter power rating for fixed dimensions while considering specific design limitations. This objective was realized by exploring the system loss-size Pareto front, from which the final notional design was determined. The system loss-size Pareto front was determined through collaborating lower-level system Pareto fronts or design points. To partition the design optimization process, the analysis has been divided into three levels of design: system level, converter level and component level design. Key design variables in this converter were swept and analyzed as appropriate in their particular level (e.g. power rating was swept in system level design while topology was swept in converter level design). The design and optimization was finished and the final design was determined.

From the parameters determined by the final selected Pareto-front design point, a converter was constructed. The converter consists of a Vienna rectifier as the AFE converter and an LLC resonant converter as the dc/dc converter providing galvanic isolation and voltage step-down was constructed. The resultant 1200 W convection cooled converter exhibits 22 W/in$^3$ power density. 97.1% full load efficiency was achieved. Additionally, the prototype met the EMI and power quality standards. The models involved in the design were validated and the design estimations were verified experimentally.

# Chapter 5. Modular Inverter

## 5.1 Chapter Introduction and Prior Art

This chapter aims at designing a modular inverter for aerospace applications. The parameters specified by the system are listed in TABLE VI, despite that the nominal power is to be maximized to optimize system capacity. This work uses bi-level programming problem (BLPP) to maximize the nominal power. Furthermore, this approach not only renders the optimal converter design, but also quantitatively evaluates influence of design constrains (form factor, loss budget, etc.) and compares converter topologies. For evaluating influence of design constrains, this work compares the maximal nominal power of a converter module that has doubled height and loss budget with that of two converter modules working in parallel. The results and discussion will be elaborated in section 5.4.4.

**TABLE VI. CONVERTER SPECIFICATIONS**

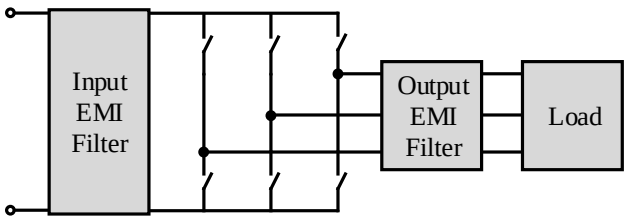
| | | | |
|---|---|---|---|
| Nominal Power | TBD | Form Factor | 60 $in^2$ x 1 in |
| Input Voltage | 540 V dc | EMI Standard | DO-160E |
| Output Voltage | Three-phase 200 V ac | THD under resistive load | 8 % |
| Output Frequency | 50 ~ 2000 Hz | Cooling | Natural Convection |
| Loss Budget | 35 W | Topology | TBD |

For topology comparison, two-level voltage source inverter, three-level neutral-point-clamped inverter [138], T-type inverter [138] and triangular conduction mode (TCM) [25] inverter, are evaluated, of which the latter is mostly reported in single power factor correction under 1 kW [25, 130, 139] and is recently applied to higher power, three-phase applications [31, 140] thanks to the

advancement of wide-bandgap (WBG) semiconductor devices. In effect, two-level voltage source inverters have been dominant in the industry, a choice supported by their inherent simplicity. However, if high power density and high efficiency is sought, three-level inverters represents better solutions thanks to their low switching voltage. [79] shows three-level neutral-point-clamped (NPC) topologies achieves lighter EMI filter weight for AC/AC power conversion systems than its two-level counterparts. A 10 kW T-type inverter (without EMI filters) with over 99% efficiency has been demonstrated in [12]. This type of topology is increasingly being adopted for these applications, a trend that has been made easier by the recent availability of integrated power semiconductor modules in various three-level configurations. With the development of WBG semiconductor devices, switching frequency and efficiency of three-level inverters is pushed higher [141]. On the other hand, thanks to extremely low turn-off loss of WBG power MOSFETs, zero-voltage switching (ZVS) topologies for three-phase power conversion become popular in academia recently [140, 142]. For three-phase power conversion, ZVS could be achieved with or without auxiliary circuits. The early development of ZVS three-phase topology uses auxiliary circuits to bring DC voltage to zero at switching instants (referred to as DC link resonant converter) [143, 144] or auxiliary circuits that links to each phase-leg to help charge and discharge the switch output capacitors to enable ZVS. The topologies without auxiliary circuits gains more interest thanks to their simplicity. Pole inverter proposed in [145] utilizes energy stored in output inductors to charge and discharge switch output capacitors. To achieve ZVS, current in output inductor changes polarity twice in each switching cycle and this operation mode is commonly referred to as triangular conduction mode (TCM) or critical conduction mode (CRM). In this work, term triangular conduction mode is used. Pole converter operating with TCM has been developed and

reported for three-phase four-wire applications in [142] they all shows promising performance. In this work, a pole inverter with a "pseudo fourth wire" created by decoupling capacitors is evaluated, thus term "capacitor-decoupled TCM inverter" will be used in this work.

All the aforementioned topologies are designed and evaluated based on silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFET) that have suitable voltage blocking capabilities (≥ 900 V). Although increased switching speed of wide-bandgap devices reduces switching loss, it causes electromagnetic interference (EMI) issues in control circuitries. These issues have been addressed in [146-148]. [146] reports a false turn-on caused by a dv/dt over 100 V/ns during the turn-off of a gallium nitride (GaN) device, and the work solves the issue by using low-capacitance digital isolator. [147] focuses on SiC MOSFET based applications where optocoupler transmits the gate signals. The authors add an additional isolation barrier between optocoupler ground and gate driver ground to ensure signal integrity. [148] proposes a structure for auxiliary power to orient the noise from signal ground to power ground. Furthermore, [148] experimentally demonstrates the effectiveness of the proposed structure by measuring the noise current that flows to control ground during device transitions. However, these literatures only cover single phase-leg (converter) design. Paralleling phase-legs or converters adds noise sources as well as noise victims to the system. The EMI issues of the paralleled modular converters will be discussed in section 5.5.4.




**(a)**

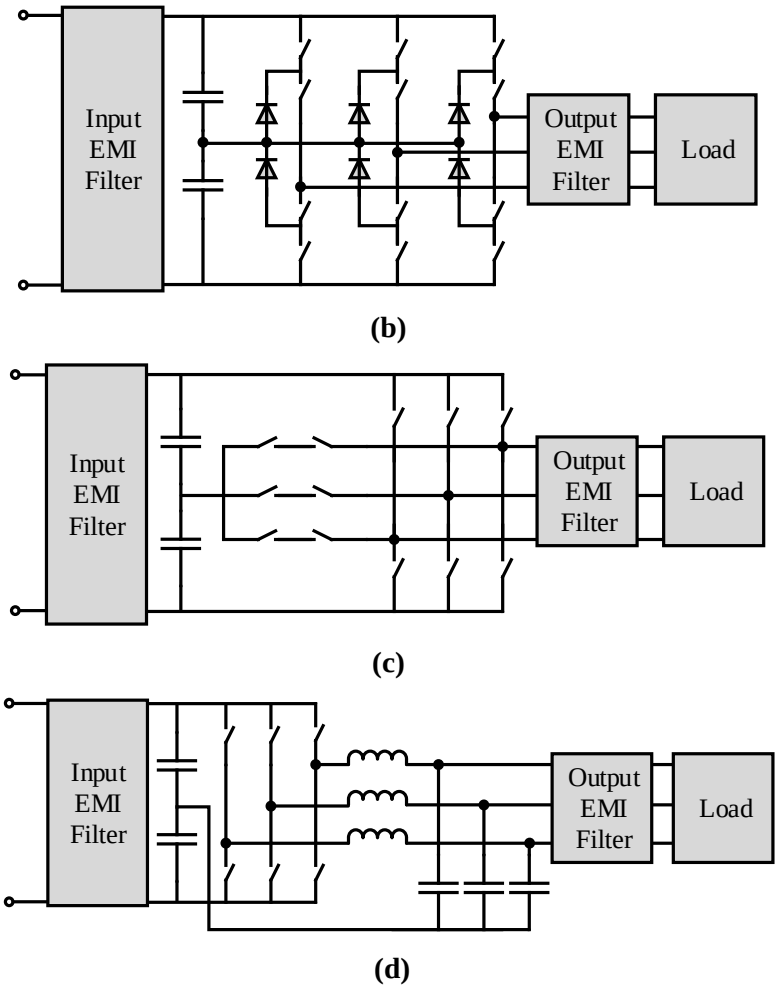



**Fig. 5-1. Topologies under evaluation. (a) Two-level voltage source inverter. (b) Three-level neutral-point-clamped inverter. (c) T-type inverter. (d) Capacitor-decoupled TCM inverter.**

## 5.2 Nominal Power Maximization of Modular Inverter

The design framework for nominal power maximization of modular inverter is depicted in Fig. 5-2, which is similar to the design framework discussed in section 3.2.

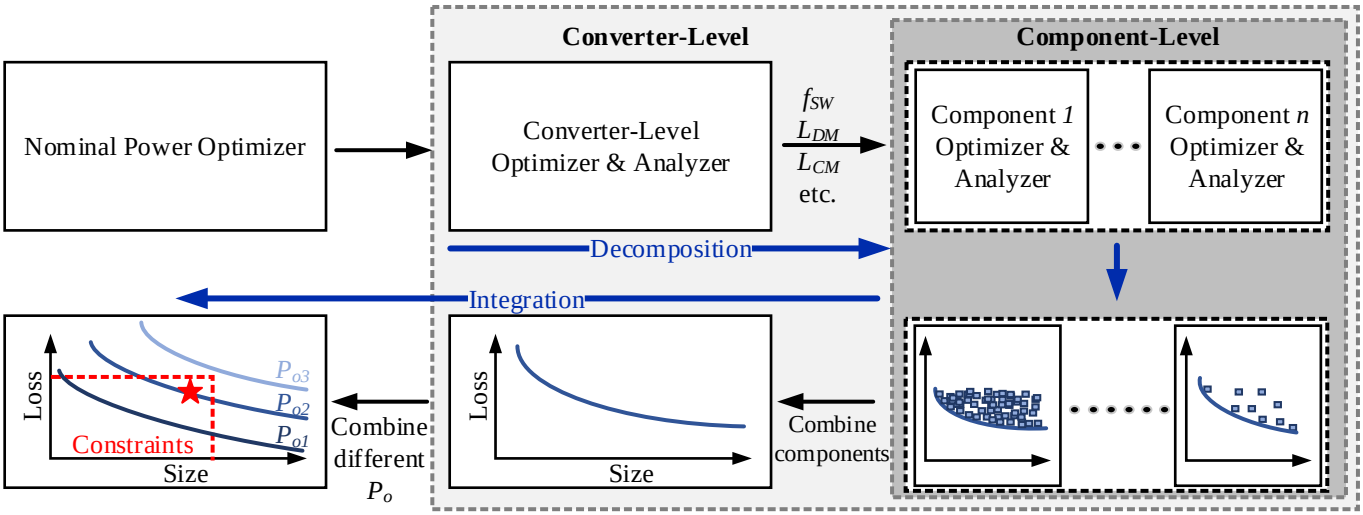



**Fig. 5-2. Overall optimization framework for and expected results of nominal power maximization.**

## 5.3 Converter Design Procedure

There are four three-phase inverter topologies considered in this chapter: two-level voltage source inverter, three-level NPC inverter, T-type inverter and capacitor decoupled TCM inverter. Capacitor decoupled TCM inverter is a soft-switched inverter whereas the other three are hard-switched PWM inverters. The different operating principles render different design procedures and they will be elaborated in this section. To compare the topologies, the aforementioned nominal power optimization is conducted for the four topologies separately.

### *5.3.1 Design Procedure for Hard-Switched Topologies*

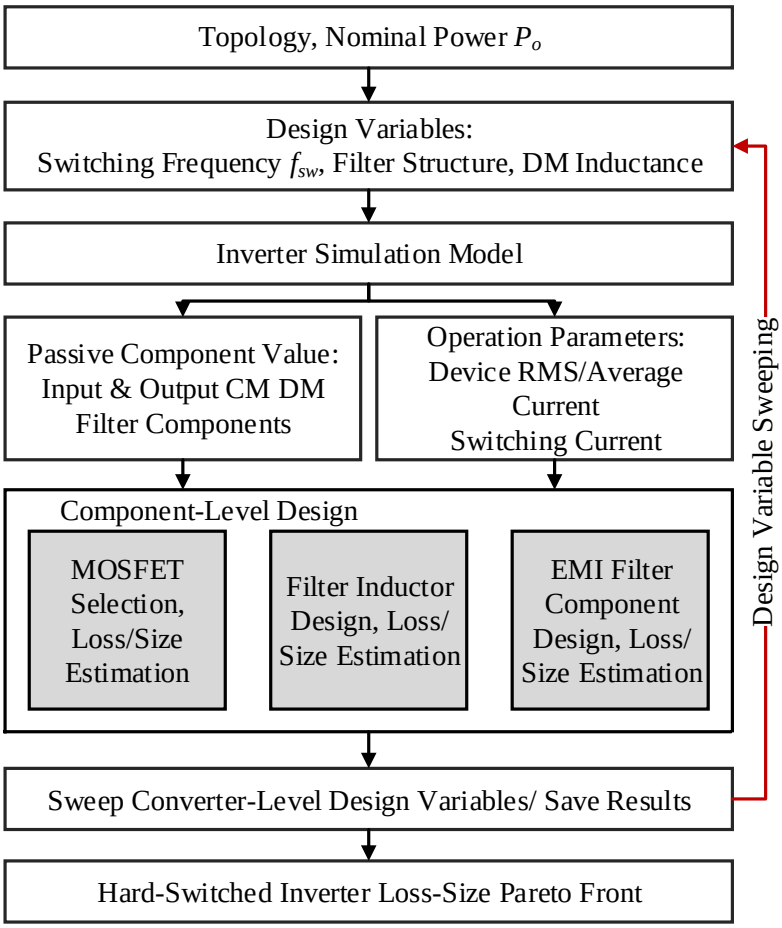
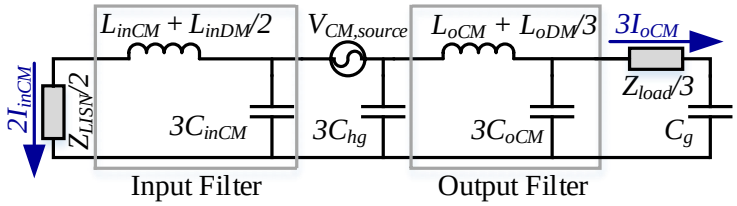



**Fig. 5-3. Design procedure for hard-switched converters.**

The design procedure for hard-switched topologies is depicted in Fig. 5-3. Given nominal power and topology, the design starts with specifying converter-level design variables, namely, switching frequency, EMI filter structure (one-stage or two-stage structure for input and output) and output differential mode (DM) inductance (largely impact filter size and current ripple). To size the parameters of EMI filtering components, common mode (CM) model and DM model [79] depicted in Fig. 5-4 are used, where the CM and DM noise spectrums are calculated by simulation models. The fixed parameters used in EMI filter design are listed in TABLE VII, and the other

parameters (inductance and capacitance) of EMI filter components are determined such that the converter meets EMI and THD requirements.

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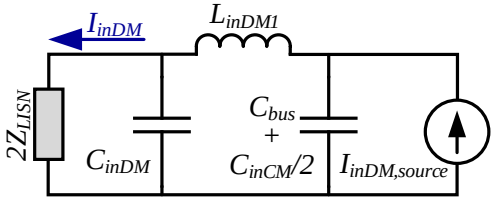



**(b)**

**Fig. 5-4. EMI models for filter sizing. (a) CM model with one-stage LC filter. (b) DM model with one-stage filter.**

**TABLE VII. FIXED PARAMETERS IN EMI FILTER DESIGN**

| Notation | Description | Value |
|---|---|---|
| $Z_{LISN}$ | Impedance of linear impedance stabilization network (LISN) | 50 Ω |
| $C_{hg}$ | Parasitic capacitance between device thermal pad and ground of each phase | 20 pF per device |
| $Z_{load}$ | Load impedance | $j\omega \times 500\mu H + R_{load}$ |
| $C_g$ | Parasitic capacitance between load neutral and ground | 2 nF |
| $C_{inCM}/C_{oCM}$ | Input/Output CM capacitance | 20 nF per line |
| $C_{bus}$ | Input DC bus capacitance | 25 μF |

Operation parameters required for component physical design and loss estimation, e.g. RMS current through MOSFETs, volt-sec applied on filtering inductors, are acquired from simulation model. All the information, namely, converter-level design variables, detailed EMI filter designs and operation parameters are fed to the component-level design and they are considered as specifications in component-level design.

In component-level design, selection and physical implementation of all components are accomplished, and their loss and size are estimated correspondingly.

For active switches, 1200 V (C2M0080120D, C2M0040120D and C2M0025120D) and 900 V (C3M0065090J) SiC MOSFETs from CREE are considered. Their switching loss is measured from double pulse tests (DPT). Conduction characteristics and thermal characteristics are taken from their datasheets. Both switching loss and conduction loss are subject to device junction temperature. In order to accurately estimate loss from MOSFETs, DPT were carried out under different junction temperatures. A thermal iteration was carried out in each design loop to estimate the steady state device temperature and the corresponding loss. Heat sinks in different sizes are considered in the design.

Diodes used in three-level NPC inverter are implemented with 600 V or 650 V SiC Schottky diodes from CREE and Infineon. Diode conduction characteristics with consideration of device temperature is taken from their datasheets. Its capacitive charge loss is considered and it is dissipated in correspond MOSFETs.

For differential mode (DM) inductors, ferrite cores and iron-powder cores in different sizes are considered. Litz wire is used to implement inductor windings and AC effect is neglected in winding loss estimation. Core loss is calculated based on volt-sec information acquired from simulation model and improved generalized Steinmetz equation (iGSE) [69]. Influence of flux DC bias on core loss is neglected.

For CM chokes, nanocrystalline cores in different sizes are considered. Solid copper wire is used for winding implementation and skin effect is considered in winding loss estimation. Core

loss and saturation are both derived from simulated volt-sec information. iGSE is applied for core loss estimation.

All capacitors are implemented with film capacitors.

Upon finishing component-level design under certain combination of converter-level design variables, Pareto fronts of each components are identified. Combining the Pareto optimal component designs renders the Pareto optimal converter designs and the converter-level Pareto fronts, which represents the performance tradeoff under certain combination of converter-level design variables, e.g. 48 kHz switching frequency, $4^{th}$ order input and output filter, 70 μH DM inductance. Sweeping different combinations of design variables results in the overall loss-size Pareto fronts that illustrates the tradeoff between loss and size under given nominal power.

### *5.3.2 Design Procedure for Capcitor-Decoupled TCM Inverter*

Capacitor-decoupled TCM inverter is an inverter with three phases decoupled by three Y-connected capacitors and a wire connecting neutral of the capacitors and neutral of DC bus. This neutral-connecting wire serves as the forth wire where the zero-sequence component of the three-phase currents flows through. With the fourth wire, current in each phase is controlled independently, and the control techniques have been developed and reported in [25, 149] for single-phase power-factor-correction rectifiers. Fig. 5-5 shows a typical current waveform of output inductor in a capacitor-decoupled TCM inverter. The current is triangular, and its polarity changes twice each switching cycle, eliminating turn-on loss of MOSFETs (generally termed zero-voltage-switching or ZVS [150]). Switching frequency in this inverter mainly depends on inductance of the output inductor and output voltage.

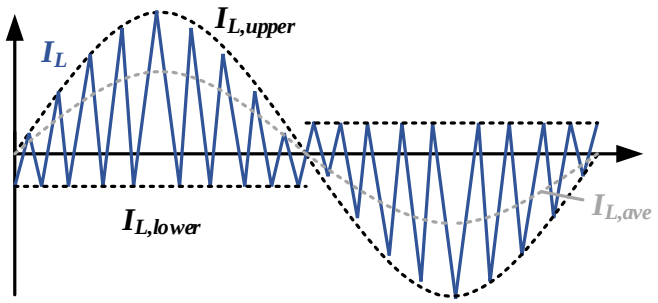



**Fig. 5-5. Inductor current waveforms of capacitor-decoupled TCM inverter.**

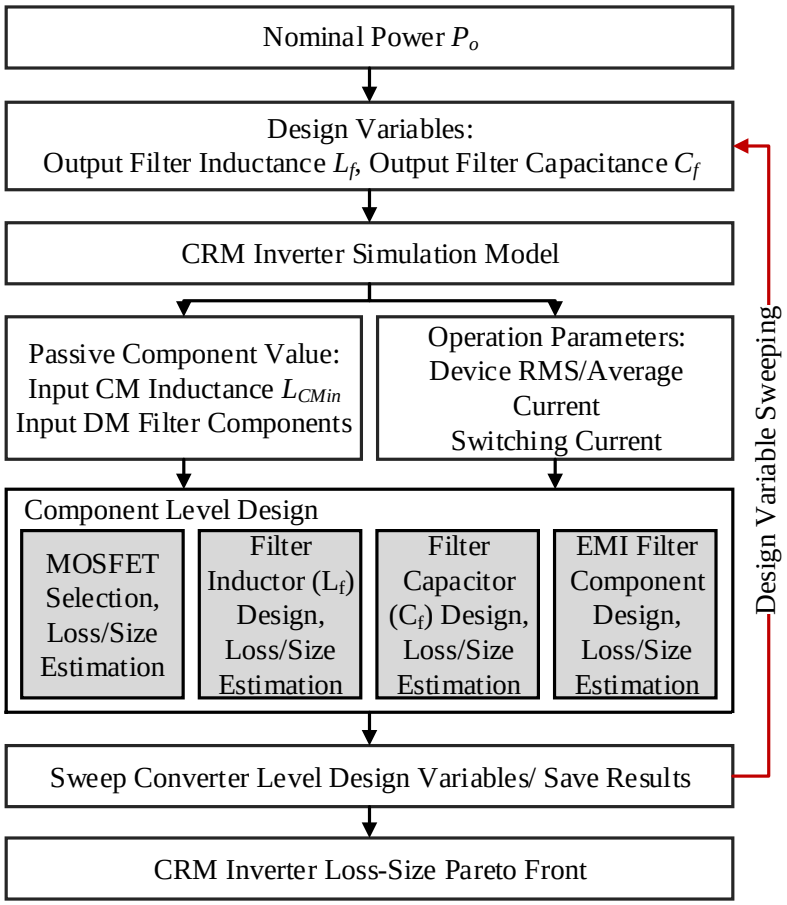



**Fig. 5-6. Design procedure for capacitor-decoupled TCM inverter.**

The converter design and optimization procedure is depicted in Fig. 5-6. Converter-level design variables are output inductance $L_f$ and output (decoupling) capacitance $C_f$ which determine the switching frequency. Besides, $C_f$ should be large enough such that its voltage ripple is small enough to ensure functionality. With certain combination of the two, EMI noise spectrum and

operation parameters for component design are acquired from simulation model and EMI model (DM model is similar to hard-switched topologies and CM model is shown in Fig. 5-7, of which the derivation is documented in [118]), and EMI filter designs could be derived accordingly. The decoupling capacitor is a low impedance path for CM noise, which eliminates the necessity of output CM filter.

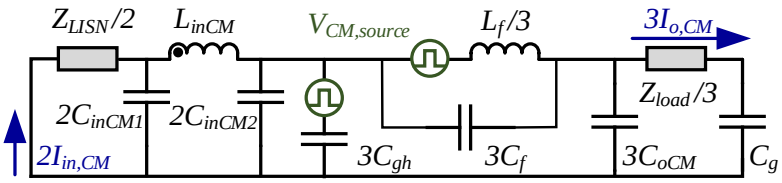



**Fig. 5-7. CM model for filter sizing in capacitor-decoupled TCM inverter.**

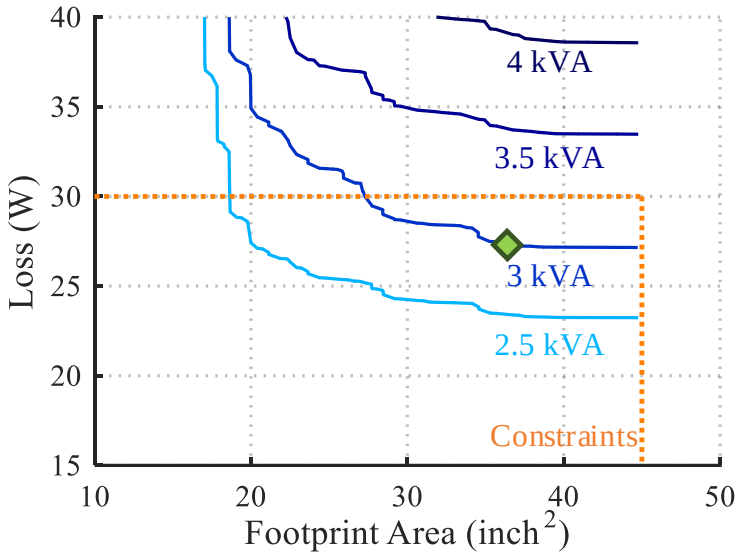
Similar to hard-switched PWM inverters, component-level design for capacitor-decoupled TCM inverter uses parameters derived from converter-level design as specifications. Design and optimization of each component are carried out independently. Models used in the component design of this inverter are the same as those of hard-switched PWM inverters. Pareto fronts of each components are combined in order to identify converter Pareto fronts.

## 5.4 Module Design Results

### *5.4.1 Loss-Size Pareto Fronts of Evaluated Topologies*

For nominal power maximization, the design and optimization procedures described above have been carried out under different power levels for different topologies, as is depicted in Fig. 3-4. The Pareto fronts of different topologies under different nominal power are summarized in Fig. 5-8. These graphs show that two-level voltage source inverter, three-level NPC inverter, T-type inverter and capacitor-decoupled TCM inverter achieve maximum nominal power of 3 kVA,

4 kVA, 5 kVA and 3.5 kVA, respectively. T-type inverter achieves the highest nominal power and is selected for prototyping, and the final design is marked with a red star in Fig. 5-8 (c).

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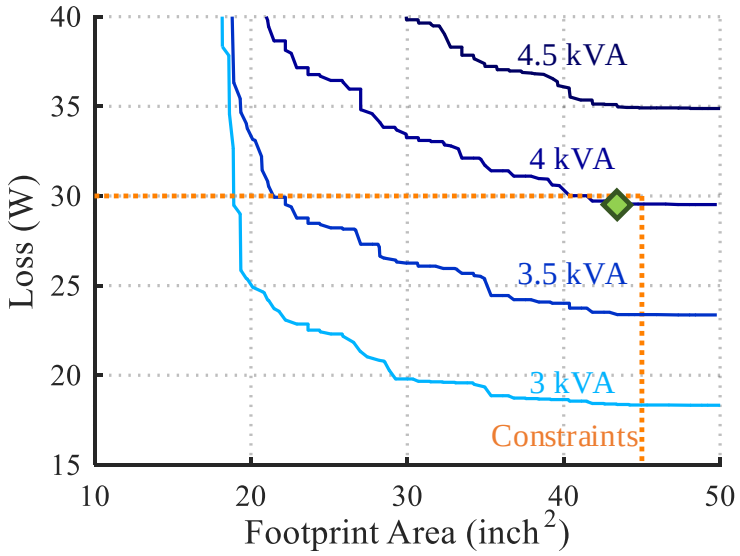


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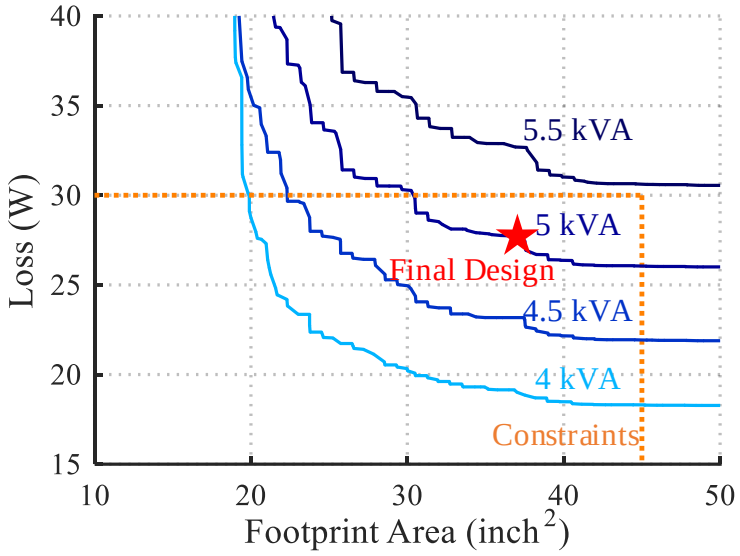


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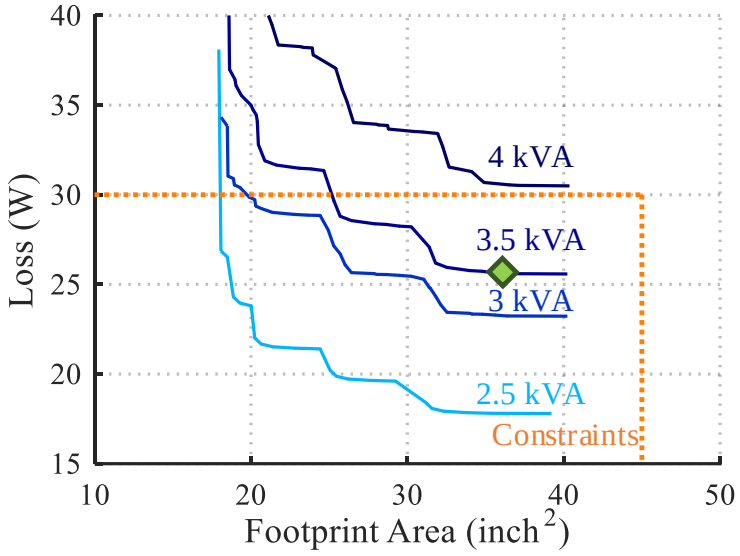



**(d)**

**Fig. 5-8. Loss-size Pareto fronts of topology candidates. The diamonds represent optimal designs, and the star represent the final design. (a) Two-level voltage source inverter. (b) Three-level NPC inverter. (c) T-type inverter. (d) Capacitor-decoupled TCM inverter.**

### *5.4.2 Comparison of Optimal Designs*

Besides exploring the optimal design, this study unveils the capability and design trade-offs of the topology candidates. The green diamonds in Fig. 5-8 denote one of the optimal designs of each topology. These nominal-power-maximum design points are selected so that their loss and footprint area are similar to the final T-type design. Key parameters of these designs are summarized in TABLE VIII. The loss and footprint area breakdown of the these designs and that of the final design are summarized and compared in Fig. 5-9 and Fig. 5-10 respectively.

**TABLE VIII. KEY PARAMETERS OF DESIGNS THAT ACHIEVES THE MAXIMUM NOMINAL POWER**

| | Switching frequency | Output DM Inductance | Output DM Capacitance | Semiconductor devices |
|---|---|---|---|---|
| Two-level, 3 kVA | 72 kHz | 190 µH | 0.1 µF | CREE C3M0065090D |
| NPC, 4 kVA | 40 kHz | 270 µH | 0.2 µF | CREE C3M0065090J + Infineon IDH20G65C5 |
| T-type, 5 kVA | 68 kHz | 70 µH | 0.6 µF | CREE C3M0065090J |
| TCM, 3.5 kVA | 38 kHz ~ 360 kHz | 30 µH | 2.3 µF | CREE C2M0080120D |

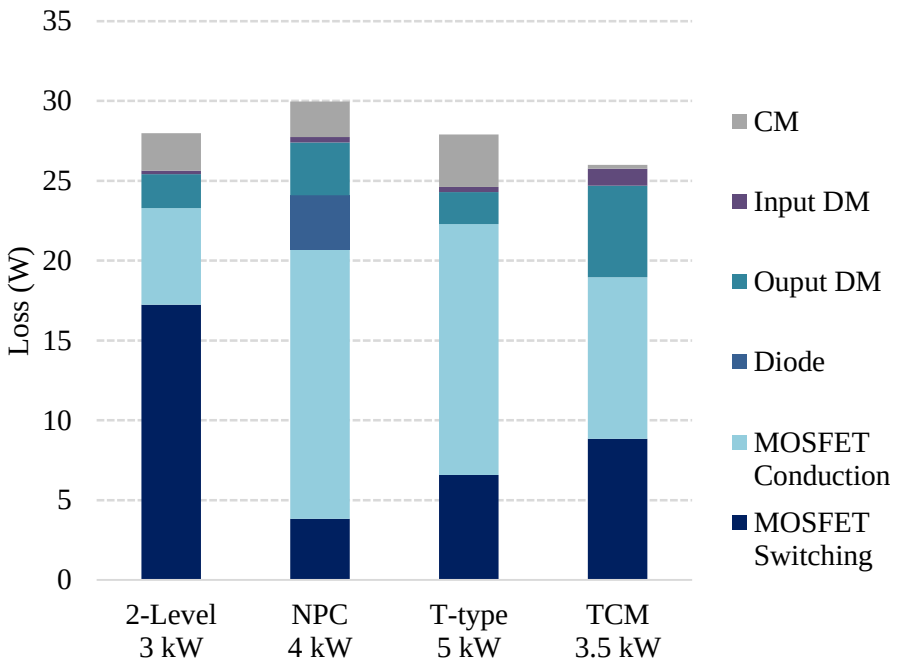



**Fig. 5-9. Loss breakdown of nominal-power-maximum designs of the four topologies.**

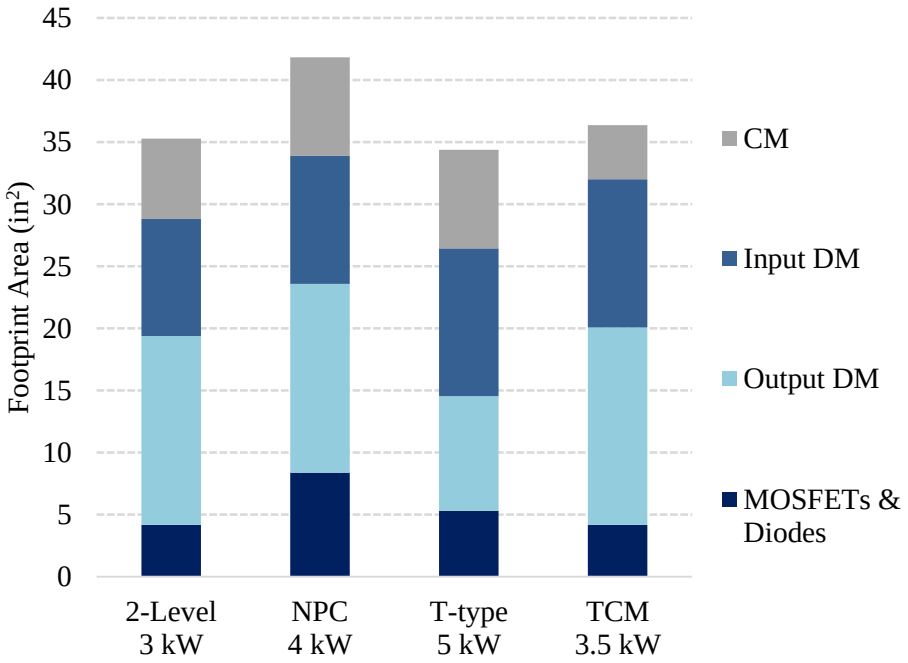



**Fig. 5-10. Footprint area breakdown of nominal-power-maximum designs of the four topologies.**

#### *5.4.2.1 3 kVA design of two-level voltage source inverter*

Two-level inverter requires larger EMI filter size comparing with its three-level counterparts owning to the concentrated noise spectrum [38]. Furthermore, the height constraint (1 in) in this work limits the core dimensions. As a result, there is no valid design that operates lower than 72 kHz switching frequency while keeping the CM chokes unsaturated. The selected optimal design operates with 72 kHz switching frequency, which leads to massive switching loss. Compared with other topologies that either switch at half of DC bus voltage or eliminates turn-on loss, its switching loss takes majority of the loss budget and impedes further increase in nominal power within design constraints.

#### *5.4.2.2 4 kVA design of three-level NPC inverter*

Three-level NPC inverter enjoys all the benefits of a three-level converter, namely, reduced switching voltage and smaller filter size comparing with its two-level counterpart [21, 79]. However, in each switching state, either two MOSFETs or one MOSFET and one diodes conduct current, which results in excessive conduction loss when comparing with T-type inverter. As is observed in Fig. 5-9, with the same MOSFET selection but lower output power, three-level NPC converter renders 20.6 W semiconductor conduction loss, 5.6 W more than that of T-type inverter.

Although three-level NPC inverter does not achieve the lowest semiconductor loss, it leads to the smallest semiconductor footprint area thanks to elimination of heat sink. Comparing with two-level inverter, it enjoys larger device count. Comparing to T-type inverter, it distributes semiconductor loss more evenly (in NPC inverter, 1.9 W on side MOSFETs, 1.5 W for middle MOSFETs and 0.6 for diodes each; in T-type inverter, 3.2 W on side MOSFETs and 0.4 W on

middle MOSFETs each). In applications where thermal management is of primary concern, three-level NPC inverter is a promising topology.

#### *5.4.2.3 5 kVA design of T-type inverter*

T-type inverter achieves the highest nominal power thanks to its lower switching loss comparing with two-level inverter and lower conduction loss comparing to three-level NPC converter. Detailed implementation will be presented in section III. *C*.

#### *5.4.2.4 3.5 kVA design of capacitor-decoupled TCM inverter*

The capacitor-decoupled TCM inverter suffers from high conduction loss caused by decoupling capacitors and TCM operation. The capacitors required for decoupling the three-phases consumes massive reactive power at high frequency output condition, e.g. 3.47 kVar from 2.3 μF capacitors at 200 V, 2000 Hz output, and induces high current flowing through MOSFETs and output DM inductors. The TCM operation further increases the rms current in these devices owning to the triangular current. For the 3.5 kVA design where 5.8 A rms load current is required at 200 V output voltage and 2000 Hz output frequency, leading to 10.0 A rms current in inductors and phase legs. Although the optimal design applies MOSFETs with 25 mΩ devices, it generates considerable MOSFET conduction loss. Furthermore, the output DM filter loss exceeds other topologies owning to higher conduction loss and core loss (flux density variation is large under TCM operation).

Despite the elimination of MOSFET turn-on loss, the turn-off loss and driving loss are nontrivial. It turns off at current peaks that are much higher than PWM inverters owning to the

abovementioned issues. A 6.1 W turn-off loss and 2.7 W driving loss are estimated from this design.

However, the capacitor-decoupled TCM inverter features miniature CM filter. The decoupling-capacitors are low-impedance paths for CM noise, which eliminates the need for output CM filter. As is observed in Fig. 5-10, this design achieves a CM filter size that is 45 % smaller than the size of others.

### *5.4.3 Selected Design, Constructed Prototype and Experimental Results of a Single Module*

The complete schematics of the selected 5 kVA T-type inverter design is shown in Fig. 5-11. It consists of an CLC input DM filter, LCLC input CM filter, three phase-legs, an LC output DM filter and an LC output CM filter. All active switches are implemented with 900 V SiC MOSFETs from CREE. Detailed implementation of the converter prototype is listed in TABLE IX. The constructed prototype is shown in Fig. 5-12. The prototype is controlled by a Microsemi M2S010 FPGA located on the left bottom corner. The dimensions of the prototype are 56 $in^2$ x 1 in, which is within the given form-factor constraint and leads to a power density of 89 $VA/in^3$. The prototype weighs 1120 g.

**TABLE IX. DETAILED IMPLEMENTATION OF THE T-TYPE INVERTER MODUE**

| | | | |
|---|---|---|---|
| Nominal Power | 5 kVA | $C_{in,DM2}$ | 9 µF |
| Switching Frequency | 68 kHz | $C_{NP1}$, $C_{NP2}$ | 70 µF |
| MOSFETs | CREE C3M0065090J | $L_{o,CM}$ | 600 µH |
| $L_{in,CM1}$, $L_{inCM,2}$ | 300 µH | $C_{o,CM}$ | 20 nF |
| $C_{in,CM1}$, $C_{in,CM2}$ | 10 nF | $L_{o,DM}$ | 70 µH |
| $L_{in,DM}$ | 10 µH | $C_{o,DM}$ | 600 nF |

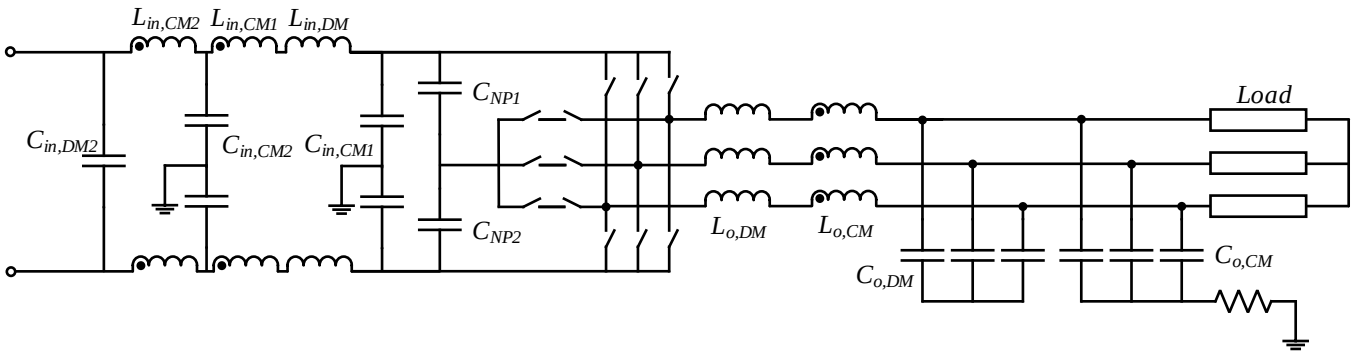



**Fig. 5-11. Schematics of final design.**

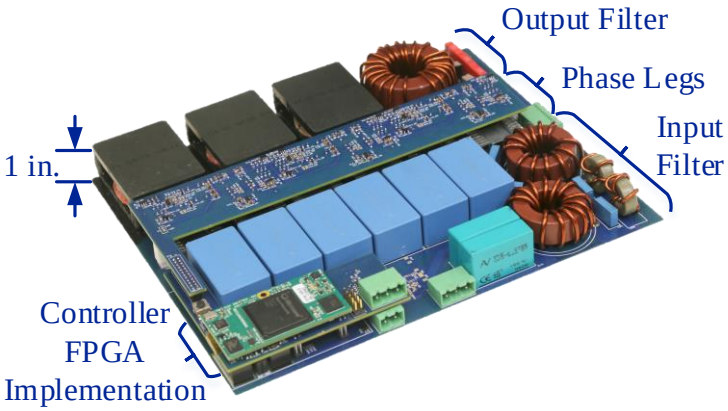



**Fig. 5-12. Prototype modular inverter.**

The experimental waveforms under 5 kVA output power with 2000 Hz output frequency and 200 Vrms output line to neutral voltage is shown in Fig. 5-13. Resistor in series with a 500 μH inductor is used as load for each phase. In Fig. 5-13, red waveform on top is output line-to-line voltage of between phase A and phase B; blue waveform is phase-leg output voltage of phase B referred to neutral point; green waveform is output current of phase B.

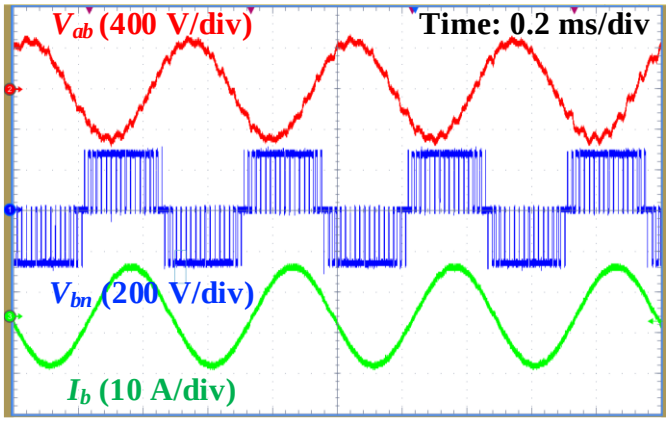


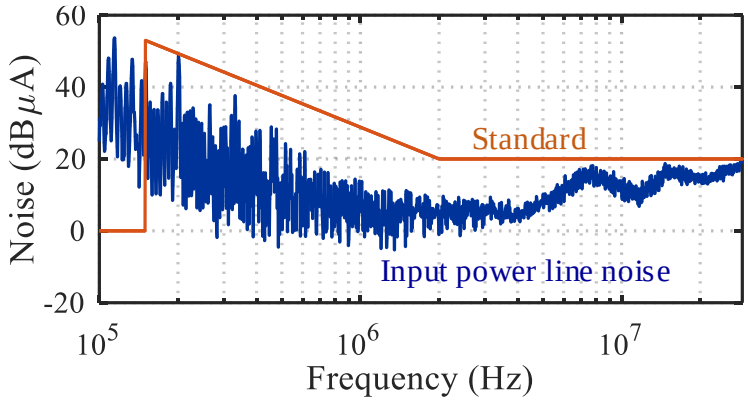

**Fig. 5-13. Experimental waveforms at 2000 Hz, 5 kVA output.**

Power stage loss and efficiency are measured with a Keysight PA2203A power analyzer. Measurement suggests a 32.0 W loss from 5 kVA output power test. Gate drivers, control circuits and other auxiliary circuits add 4.4 W loss, and the full load efficiency is 99.2 % (36.4 W total loss). The prototype is natural-convection cooled. The device temperatures are measured by thermocouples, and steady state results are listed in TABLE X. They all keep a safety margin from their temperature limits.

**TABLE X. MEASURED DEVICE TEMPERATURE AT STEADY STATE**

| | | | |
|---|---|---|---|
| Side MOSFETs | 137 °C | $L_{in,DM}$ | 31 °C |
| Middle MOSFETs | 83 °C | $L_{in,CM1}$ | 55 °C |
| $L_{o,DM}$ | 58 °C | $L_{in,CM2}$ | 35 °C |
| $L_{o,CM}$ | 51 °C | | |

EMI performance of the prototype was tested. An ETS Lindgren 91550-1 current transformer that connects to an Agilent 7402A EMC spectrum analyzer measures the current noise spectrum. The results are shown in Fig. 5-14, and they comply with DO-160E EMI standard.

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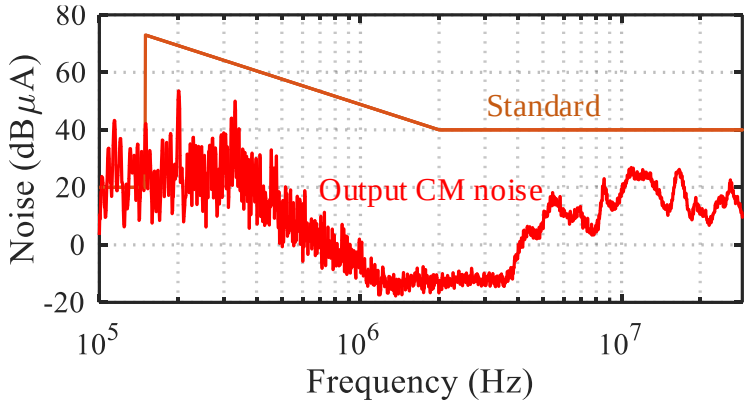



**(b)**

**Fig. 5-14. Measured EMI noise at 2000 Hz, 5 kVA output. (a) Input line noise and DO-160E standard. (b) Output CM noise and DO-160E standard.**

### *5.4.4 Influence of Form Factor on Maximum Nominal Power*

Although modularizing converters under form factor constraints adds flexibility to the system, it limits the design space by forbidding oversized components. Under height constraint of 1 in, magnetic cores with width, length and height exceed 1 in are inapplicable. MOSFETs in To-247 package cannot be mounted vertically (it exceeds 1-in height considering PCB thickness). Few heat sinks are applicable, which hinders nominal power increase owning to insufficient device cooling. The influence of the constrained form factor is revealed by exploring the maximal nominal power of a double-sized converter module and comparing it with the aforementioned designs.

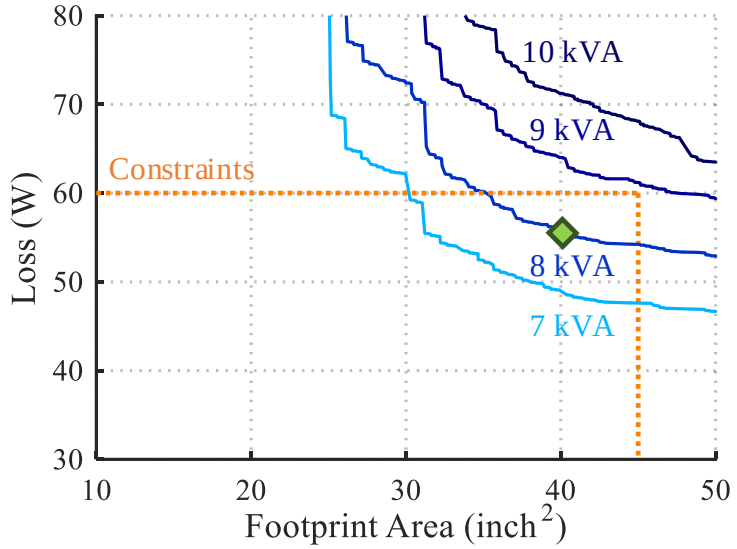
Specifically, the height constraint, which limits the use and placement of oversized components the most, is changed to 2 in, and the area constraint is kept the same (60 $in^2$).

The loss-size Pareto fronts of 2-in two-level inverter and T-type inverter under various nominal power levels are shown in Fig. 5-15. Based on aforementioned investigation, three-level NPC inverter is less efficient that T-type inverter, and capacitor-decoupled TCM inverter is improper for high power, high output frequency applications. Therefore, they are not included. As is observed in Fig. 5-15, the 2-in two-level inverter achieves a maximal nominal power of 8 kVA, which gains 33 % more power than two 1-in, 3-kVA design. The T-type inverter achieves a maximal nominal power of 14 kVA, delivering 40 % more power than its 1-in counterparts. The results illustrates the tradeoff between flexibility and power density. Converter module with large form factor renders higher power density but are less flexible. Optimal system calls for smart combination of converter module in different form factors and power levels that provide optimal power density and flexibility, which is of future research interest.

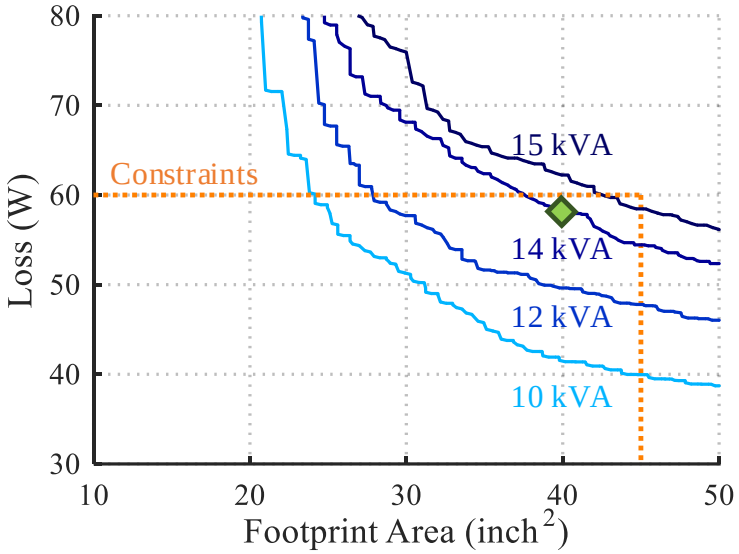
Optimal designs of the 8 kVA two-level inverter and 14 kVA T-type inverter are selected from the Pareto fronts. The design parameters are listed in TABLE XI, and the loss and size breakdown are summarized in Fig. 5-16.

**TABLE XI. KEY PARAMETERS OF THE OPTIMAL TWO-IN DESIGNS**

| | Switching frequency | Output DM Inductance | Output DM Capacitance | Semiconductor devices |
|---|---|---|---|---|
| Two-level 8 kVA | 48 kHz | 50 µH | 1.9 µF | CREE C2M0025120D |
| T-type 14 kVA | 48 kHz | 30 µH | 4.6 µF | CREE C2M0025120D |




**(a)**




**(b)**

**Fig. 5-15. Loss-size Pareto fronts of topology candidates with double height. (a) Two-level voltage source inverter. (b) T-type inverter.**

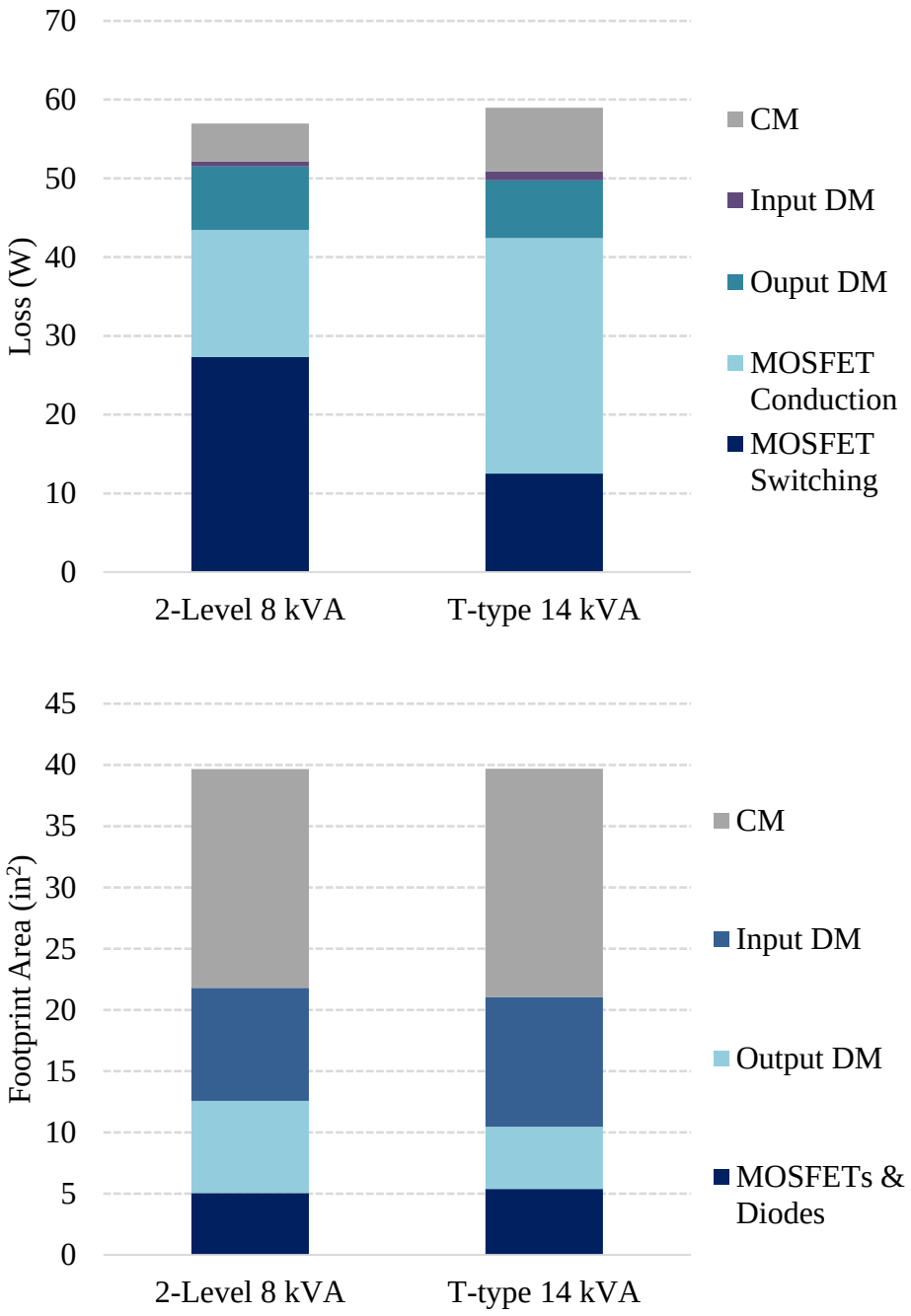



**Fig. 5-16. Loss and footprint area breakdown of nominal-power-maximum designs of the 2-in converter modules.**

## 5.5 Paralleling Modular Inverters

The modular design provides the system with flexibility in adjusting power level through choosing the number of modular converters that operates in parallel. To verify the functionality, two abovementioned modular inverters are constructed and to be operated in parallel. The control system and EMI issues induced by paralleling operation are presented in this section.

### *5.5.1 Control Architecture for Paralleling Modular Inverters*

There are two mainstream control architectures for parallel operation, namely, droop control [151-153] and master-slave control [102, 154-157]. Droop control is a distributed control, i.e. the controller of each converter does not follow any centralized controller thus eliminating communication between controllers. Thanks to its distributed nature, droop control is widely discussed in control of distributed energy source. In this application, each converter is assigned a droop resistance that determines the output voltage reference. As a result, the converter performs as a voltage source with internal resistor (equals to droop resistance), which allows good load sharing and voltage regulation [151-153]. On the other hand, master-slave control architecture consists of a number of slave controllers that follows the command given by a master controller. The master controller is in charge of the outer voltage loop (or frequency, speed loop in motor control applications) and generates current references for the slave controllers. Each converter controlled by the slave controllers operates as a current source, enabling parallel operation.

This work adopts master-slave control as the application requires a master controller that takes charge of the outer control loop (possibly voltage loop, frequency loop or speed loop). To allow for modular design, the communication between slave controllers should be eliminated. As the system does not have additional filters (which is against modular approach) for circulating current

mitigation (e.g. coupling inductors in [9, 77, 158, 159]), the system relies on the existing filters of each module and the control system to mitigate circulating current. The switching of the switches in each module should be synchronized such that the turn-on and turn-off instant of the corresponding switches are close enough to avoid large switching frequency circulating circulating current. This requires synchronizing switching frequency carriers of all module, i.e. the carriers reach peaks and valleys at the same time. [157] use an additional synchronization wire and dedicated synchronization pulse (broadcasted with low frequency) to tackle the discrepancy of oscillators in distributed power converters. [160] proposes to broadcast a switching frequency clock to which the carriers are synchronized. This work synchronizes the modules using phase-lock loops in the local controllers and an external reference clock generated by the central controller. This synchronization scheme synchronizes not only the carriers but also pulse width modulation (PWM) clock that is of much higher frequency than switching frequency, providing higher control accuracy.

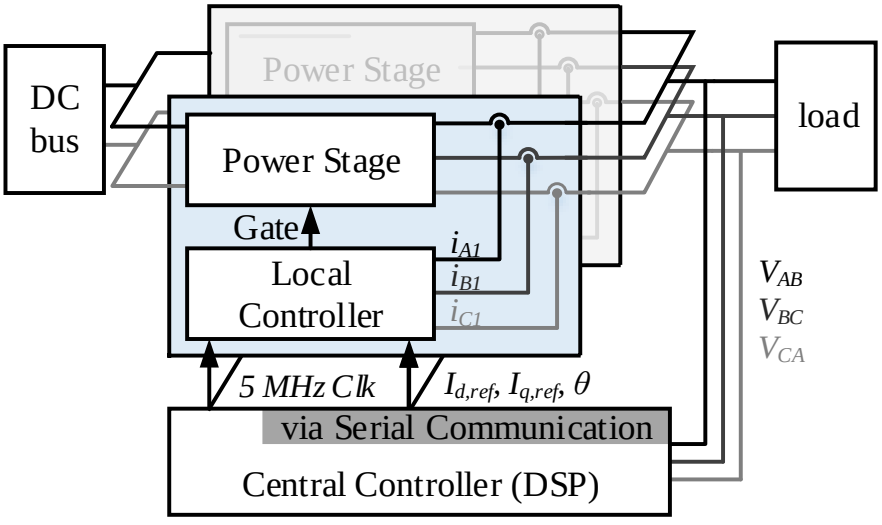



**Fig. 5-17. Control architecture for paralleling operation.**

To achieve the aforementioned requirements, a control system consisting of two levels of controllers, namely, local controller and central controllers, are developed. The overall control architecture is depicted in Fig. 5-17. The central (master) controller is implemented by a Texas Instrument TMS320C28343 DSP, and the local (slave) controllers are implemented by a Microsemi M2S010 FPGAs and are included in each converter modules.

Central controller supervises the outer control loop (output voltage loop in this design) and is in charge of synchronizing local controllers. Specifically, the central controller senses the output voltages, and closes the output voltage loop. The current references in d-q frame ($I_{d,ref1}$, $I_{q,ref1}$, etc.) generated by the voltage loop is transmitted to local controllers via Serial Peripheral Interface (SPI) communication specification and RS-485 standard. Besides current references, the output angle ($\theta$) is transmitted. To synchronize the local controllers, the central controller broadcasts a 5 MHz clock signal (function described in the following paragraph). The communication architecture is depicted in Fig. 5-18, where the CLK_SPI, RD_EN and DATA wires are for data transmission through SPI communication, and CLK_SYNC wire transmits the abovementioned 5MHz clock signal. The 5MHz-frequency is selected such that it does not exceed the data rate limit of RS-485 standard.

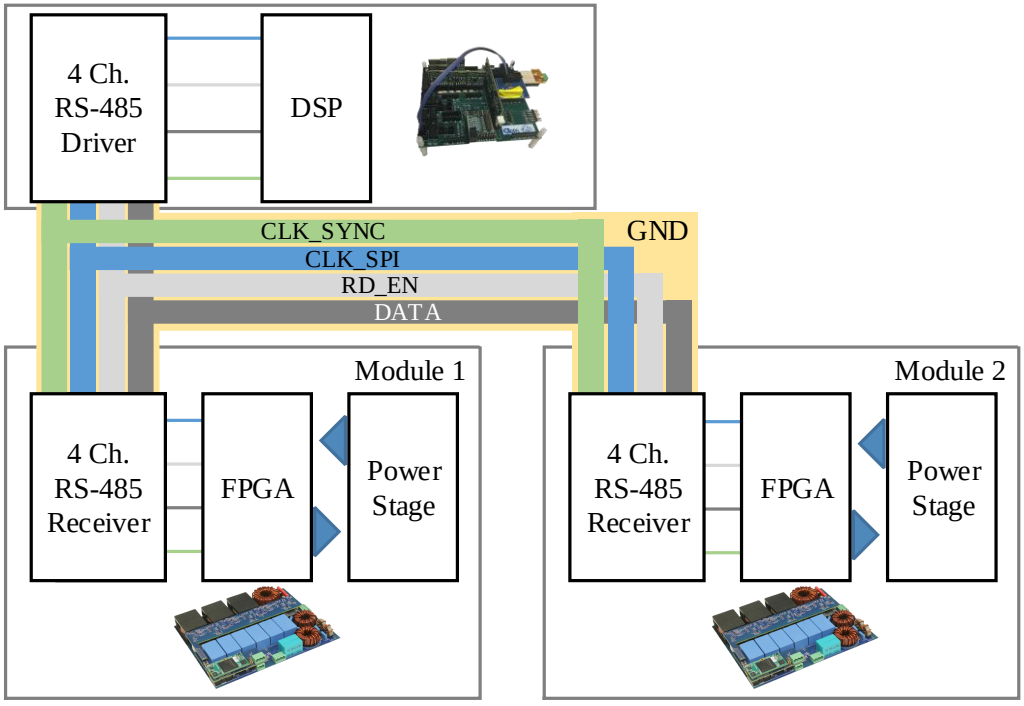



**Fig. 5-18. Communication architecture.**

The clock broadcasted by CLK_SYNC wire serves as external reference clock of all local controllers. The local controllers use phase-locked loops (PLL) to generate higher frequency clocks internally for local functions. One of the clock is a 200 MHz clock for PWM, as PWM function requires high-resolution clock. The other is a 20 MHz clock for other control functions, e.g. control of analog-digital conversion. As the converter modules are located closely in a chassis (see Fig. 1-11) and the same RS-485 receivers are used, the data discrepancy from in the CLK_SYNC wire is negligible, enabling well synchronized 200 MHz clocks and 20 MHz clocks in the local controllers. The synchronization scheme is depicted by Fig. 5-19.

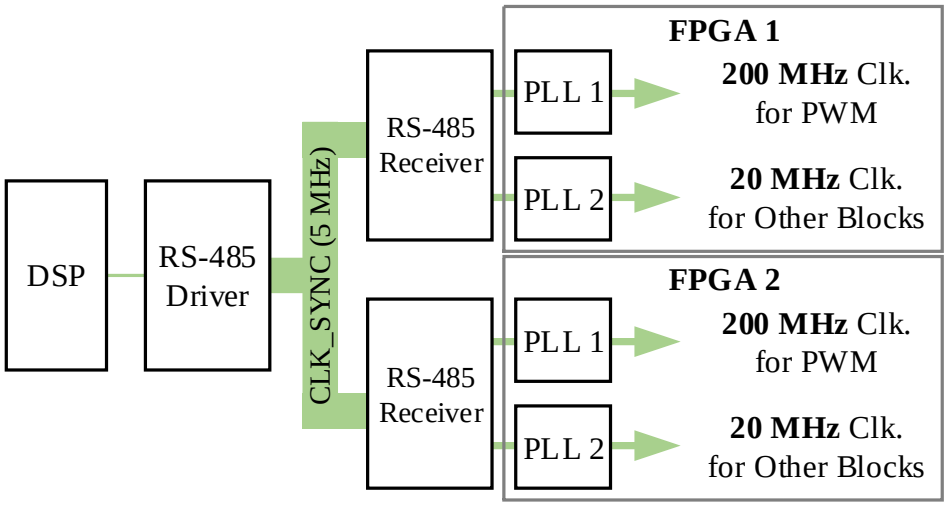



**Fig. 5-19. Synchronization using an additional wire (CLK_SYNC) and PLLs in local controllers.**

### *5.5.2 Local Controller Implementation*

This section describes the implementation of local controllers. Each converter module contains a local controller (shown in FIG) that is in charge of closing the current loop, controlling the neutral point balance and generating gate signals. The functional blocks related to the current loop and gate signal generation are show as block diagrams in FIG. The local controller senses the output currents using three in-module Hall sensors, transforms the currents to d-q frame, and compares with current references ($I_{d,ref}$ and $I_{q,ref}$) received from central controller. The error term is fed to two proportional-integral (PI) controllers of which the results are duty cycle information in d-q frame ($d_d$ and $d_q$). The two duty cycles are then transformed to a-b-c frame ($d_a$, $d_b$ and $d_c$). An zero-sequence term ($d_z$) is injected to increase the modulation index. The zero-sequence term being injected in this design is expressed as:

$$d_z = -\frac{d_{\max} + d_{\min}}{2} \quad (61),$$

where $d_{max}$ and $d_{min}$ are the maximum and minimum value among $d_a$, $d_b$ and $d_c$ respectively [161]. With the injection, the resulting duty cycles ($d_{az} = d_a + d_z$, $d_{bz} = d_b + d_z$, $d_{cz} = d_c + d_z$,) are fed to the modulator. A carrier-based modulator based using the aforementioned 200 MHz local clock is used to generate gate signals. Despite the parallel operation, there is no control loop for handling the circulating current [100, 101, 154, 156, 162]. The converter modules are mounted in the same chassis and are close to the others such that the output impedance difference, as is discussed in [163], is negligible. With current loop closed in each converter module, the low frequency circulating current is suppressed. Furthermore, given presence of output DM inductors and CM inductors, the circulating in switching frequency is mitigated. Thus, no circulating current control loop is needed, which simplifies the control and communication design while enabling modular design approach.

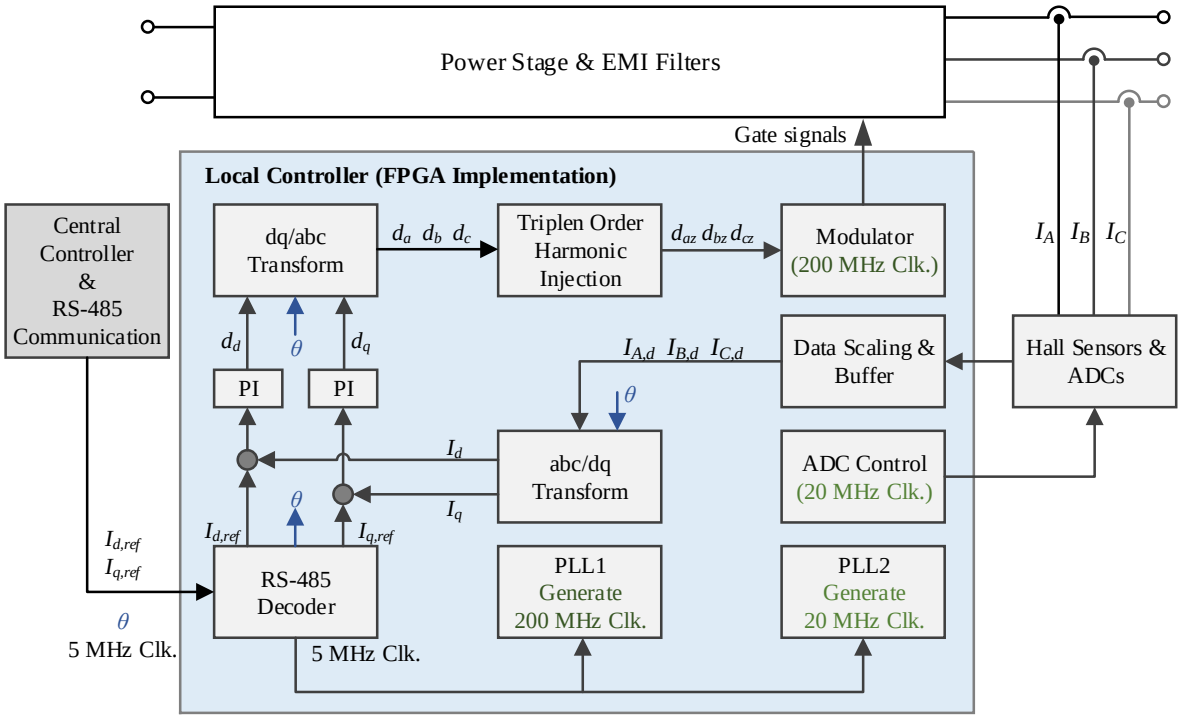



**Fig. 5-20. Functional blocks related to current loop in the local controller.**

The modulator implementation as well as the timing of the control functions are depicted by FIG. The top parts of the graphs shows the modulator implementation, where two band-shifted triangular carriers [164, 165] are used. If the duty cycle is positive, the phase leg output voltage will clamp either to the positive rail or to the neutral point. If the duty cycle is negative, it will switch between negative rail and neutral point. The current reference ($I_{d,ref}$, $I_{q,ref}$) and angle information ($\theta$) used in the present calculation was received from the central controller in the previous switching cycle. The total time for the other control functions, namely, sensing and duty cycle calculation, is designed to be less than half of the switching period such that the sample and hold (S/H) of ADCs aligns with the peaks of the carriers and the duty cycle is updated at the valleys.

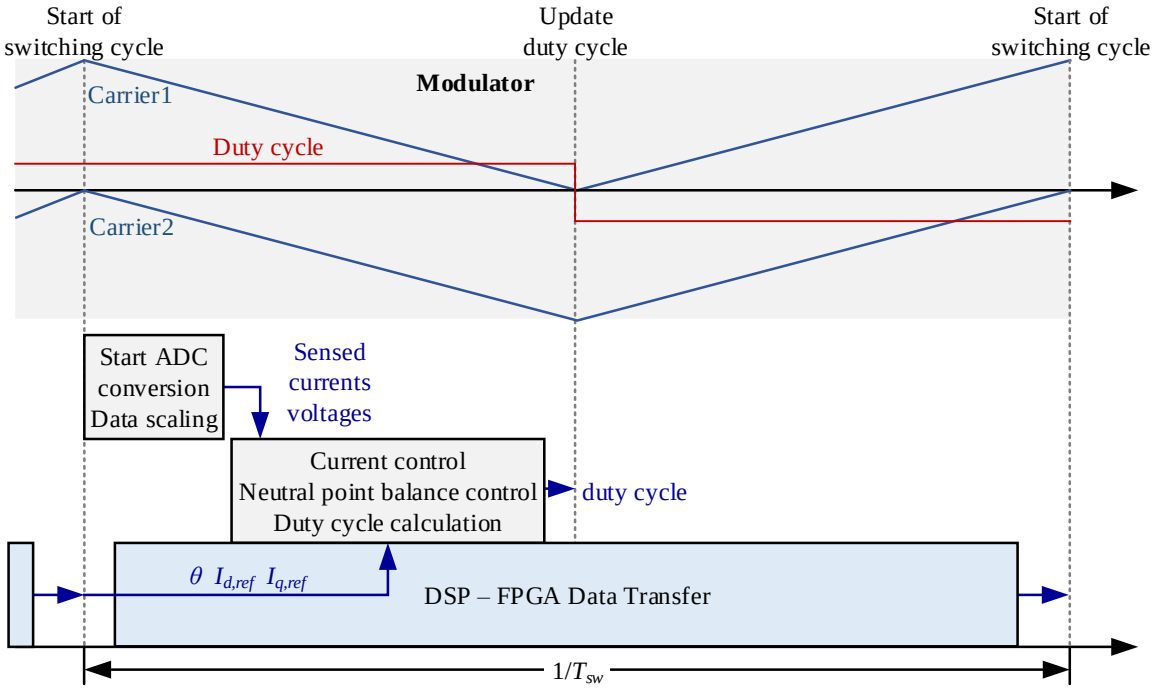



**Fig. 5-21. Timing of the controller and the carrier-based band-shifted modulator.**

Starting the S/H of ADCs at the beginning of each switching cycle while updating the duty cycle at the end may induce control error. In a modulator using band-shifted carriers, change of

duty cycle polarity will result in switching of the corresponding phase leg. FIG shows an example where the phase leg voltage $V_{an}$ switches from zero to negative when the duty cycle changes from positive to negative. In this case, if the S/H of ADCs and the duty cycle update occurs simultaneously, the S/H takes places at the same instant when the phase leg switches (this is shown in Fig. 5-22). The high dv/dt of phase leg switching (20 ~ 30 V/ns with SiC MOSFETs) may induce erroneous S/H and resulting in the false tripping. Such control error is observed in experiments and is demonstrated in Fig. 5-23. The overcurrent protection is falsely tripped when $V_{an}$ changes polarity.

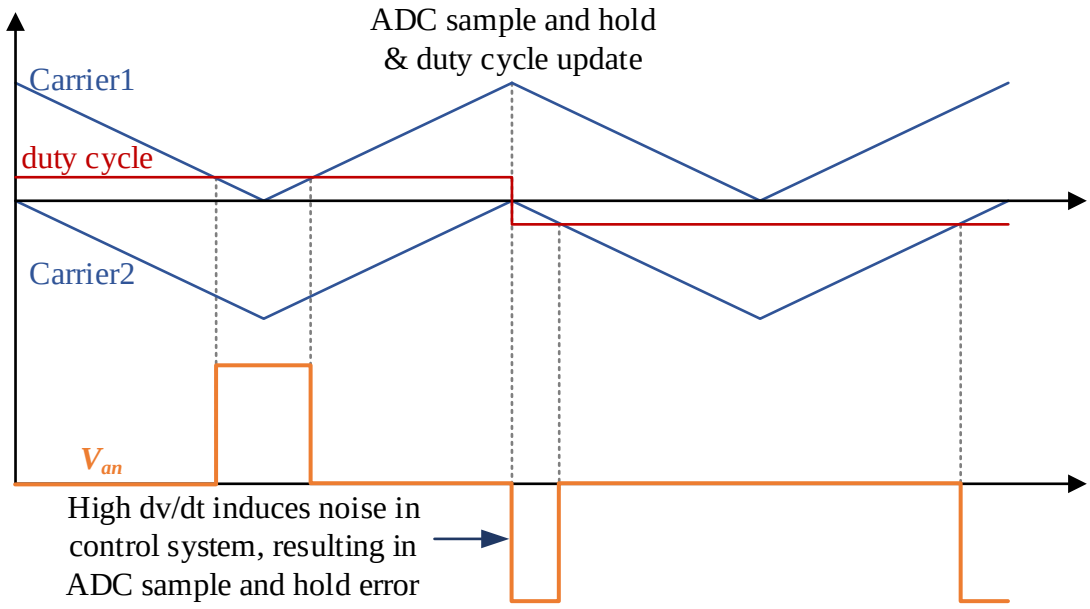



**Fig. 5-22. ADC S/H takes place at the same instant as duty cycle update. In three-level converter, there is a switching behavior at the same instant when duty cycle changes polarity. The ADC S/H aligns with the phase leg voltage change, and may result in erroneous sensing.**

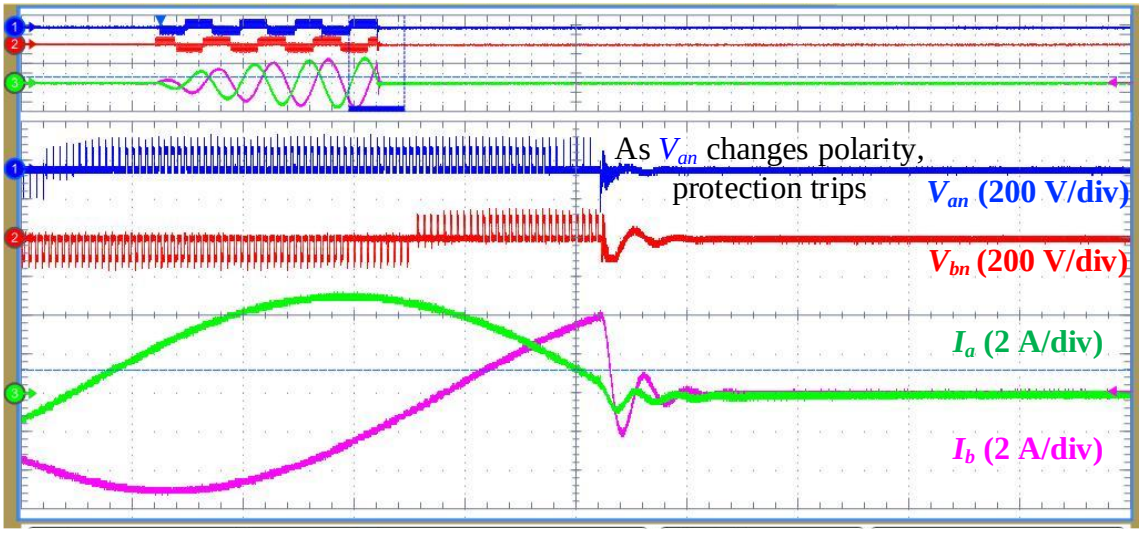



**Fig. 5-23. False protection tripping at the instant when phase leg output voltage changes polarity. Impropriate timing depicted in Fig. 5-22 induces the false tripping.**

Compressing the total time of the control functions within half of switching periods splits the S/H and duty cycle update, hence avoids the S/H error. This timing scheme is shown in Fig. 5-24. With this timing, the S/H will not align with phase leg switching no matter how much or what polarity the duty cycle is. In experiments, the abovementioned control error is avoided by adopting this timing scheme.

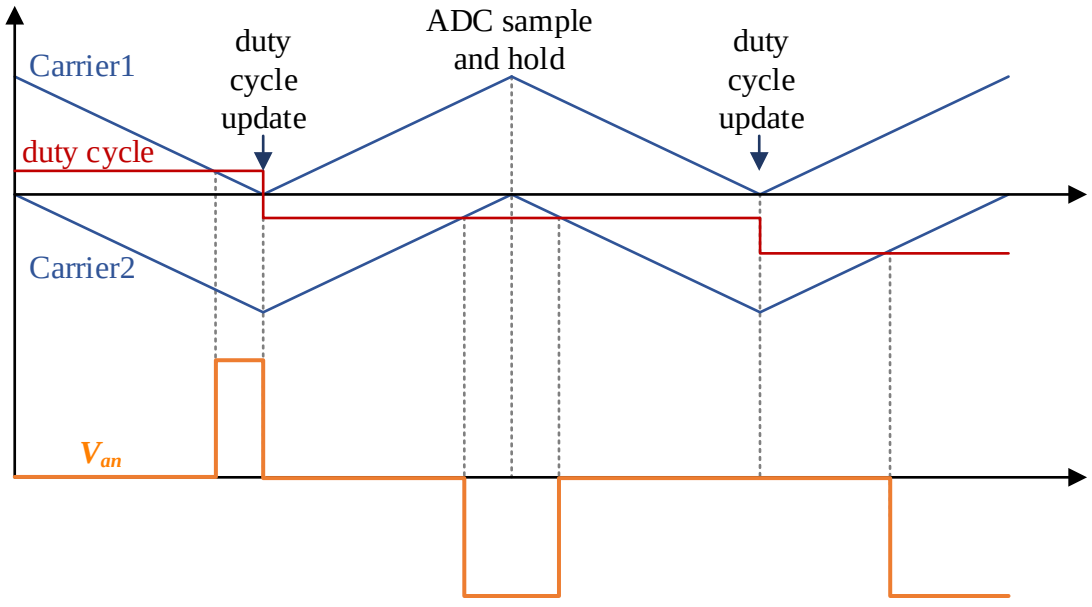
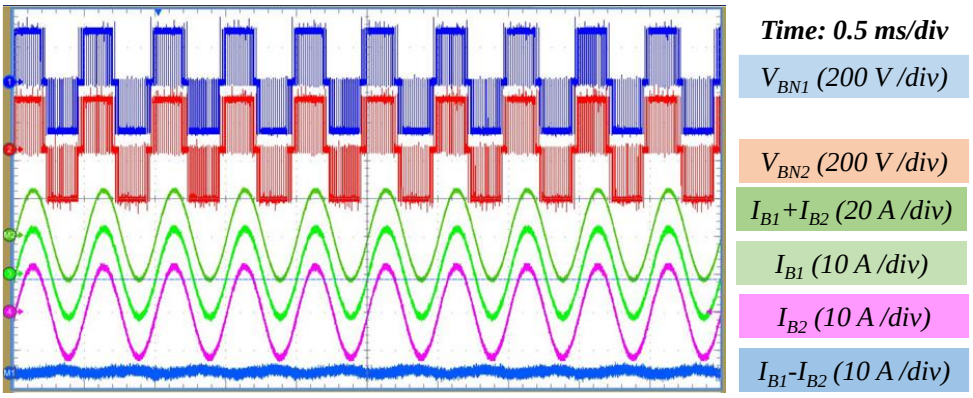


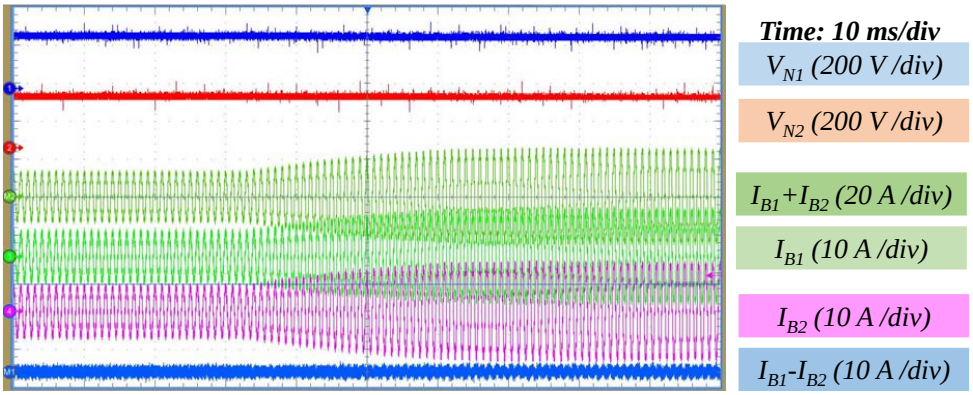
**Fig. 5-24. Using the timing scheme described in Fig. 5-21, avoids alignment of ADC S/H and duty cycle update, no matter how duty cycle changes value or polarity.**

### *5.5.3 Experimental Results of the Paralleled System*

The operating waveforms of two paralleled converter modules in steady state and during load transient are shown in Fig. 5-25. Fig. 5-25 (a) demonstrates the steady state operating waveforms at 2000 Hz output frequency and full load. From top to bottom, the graph demonstrates the phase leg output voltages, the overall output current, the output current of each module and the current difference. As is observed, the two modules synchronize well, and the current difference is small such that it neither distorts module output currents nor induces large excessive conduction loss. Fig. 5-25 (b) shows the waveforms during a load change from 25 % to 100 %. Besides the overall output current, the output current of each module and the current difference, the voltages of top DC bus capacitors ($C_{NP1}$ in Fig. 5-11) are included. The waveforms do not show any harsh transient, and the module output currents are well balanced.




**(a)**




**(b)**

**Fig. 5-25. Operating waveforms of paralleled modular inverters. (a) Steady state waveforms at 2000 Hz output frequency and 10 kVA output power. (b) Waveforms during load transient. The output power changes from 2.5 kVA to 10 kVA. The output frequency is 2000 Hz.**

### *5.5.4 EMI Issues of Paralleling Modular Inverters*

Although the high switching speed of SiC MOSFETs reduces switching loss, its high dv/dt induces noise current propagating to the control circuitries and triggers control failure [146, 147]. In this work, it is observed that paralleling converter modules aggravates the EMI issue, e.g. current protection is falsely tripped when two converter modules work in parallel while it does not happen when the converter modules work separately. The EMI issues are analyzed by investigating the propagation paths between the control ground and the high dv/dt terminals, i.e. phase leg output terminals.

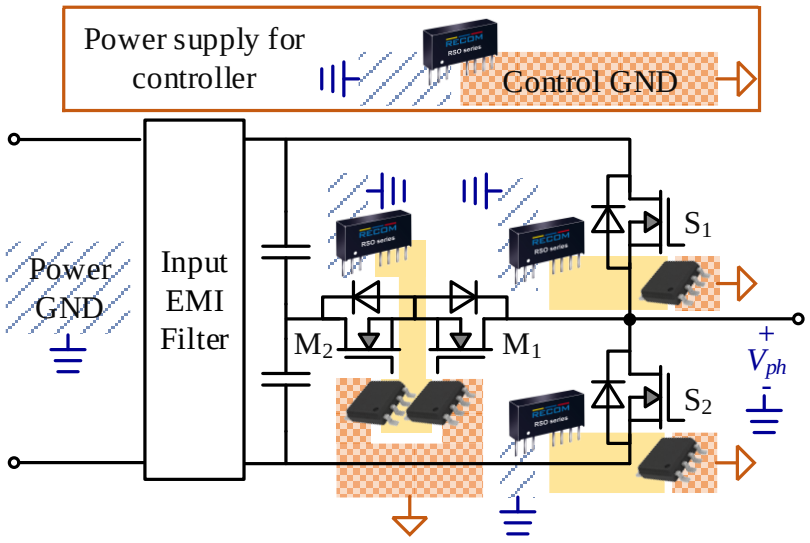



**Fig. 5-26. Architecture of auxiliary power for control and gate drivers.**

The auxiliary power architecture for one phase leg is depicted in Fig. 5-26. In this system, the neutral point of DC bus is the power ground, which is also where grounds of isolated power supply (Recom RSO series) primary sides tie to. The power supply modules isolate the sources of the MOSFETs as well as control ground from the power ground. Digital isolators (Silicon Labs Si827x) add insulation barriers between control ground and sources of MOSFETs. Nevertheless, neither the isolated power supplies nor the digital isolators provide absolute isolation. As the MOSFETs switch, the phase leg output voltage (denoted by $V_{ph}$) drastically changes referring to the power ground, and the high dv/dt (20 ~ 30 V/ns for SiC devices) induces noise current flows through the parasitic capacitors between the primary and secondary sides of the isolated power supplies and digital isolators [146-148]. To be more specific, when MOSFET $S_1$ and $M_1$ switch ($M_2$ is on and $S_2$ is off [1212]), the source of $S_1$ jumps, and the noise current flows through its isolated power supply and digital isolator. When $S_2$ and $M_2$ switch, isolated power supply and digital isolator of $M_2$ become the noise path. The noise current contaminates control ground and leads to control failure.

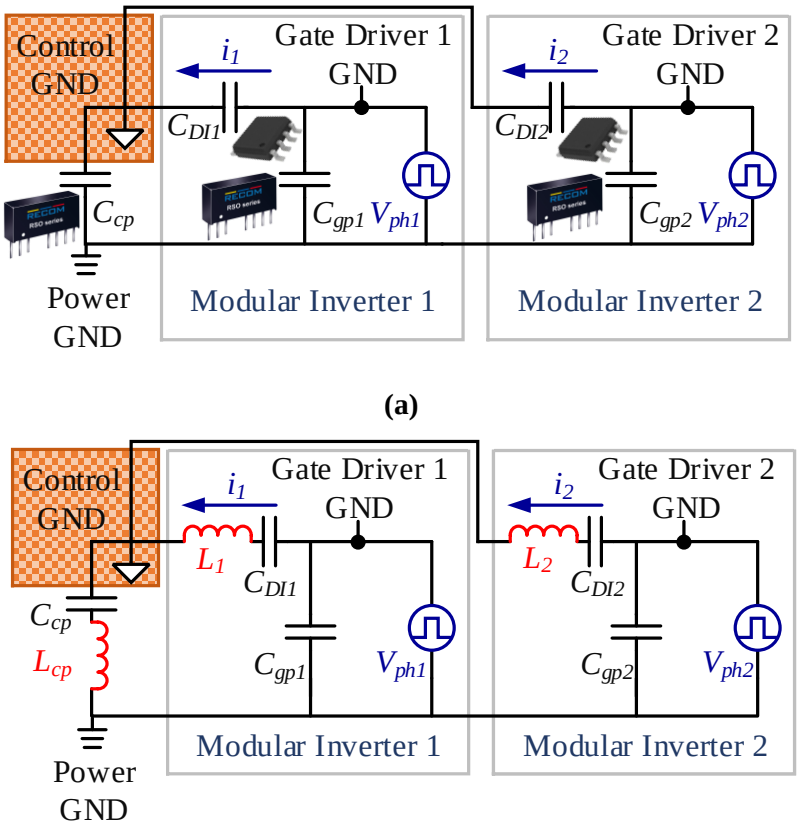



**Fig. 5-27. Simplified circuit highlighting noise propagation paths from noise sources to the control ground. (a) Noise propagation paths when two modules works in parallel. (b) Increasing impedance of critical noise paths by adding chokes.**

A simplified circuit showing the noise propagation paths between phase leg output terminal and control ground is depicted in Fig. 5-27, where two converter modules working in parallel are shown. $V_{ph1}$ and $V_{ph2}$ denote the phase leg output voltages, $C_{gp1}$ and $C_{gp1}$ the parasitic capacitors of power supplies for gate drivers, $C_{DI1}$ and $C_{DI2}$ the parasitic capacitors of digital isolators, $i_1$ and $i_2$ the noise current, and $C_{cp}$ the parasitic capacitor of power supply for controller. Noise current $i_1$ is subject to $V_{ph1}$, $C_{DI1}$ and $C_{cp}$ while i2 is subject to $V_{ph2}$, $C_{DI2}$ and $C_{cp}$. Since $C_{DI1}$ and $C_{DI2}$ (about 0.5 pF each) are much smaller than $C_{cp}$ (about 30 pF), $i_1$ and $i_2$ can be approximated by $V_{ph1}$ / $Z_{CDI1}$ and $V_{ph2}$ / $Z_{CDI2}$ respectively, where $Z_{CDI1}$ and $Z_{CDI2}$ are the impedance of the $C_{DI1}$ and $C_{DI2}$. As two

converter modules operates in parallel, the noise current doubles, and the control failure (e.g. false tripping) is prone to happening.

The problem is solved by introducing high impedance components to the aforementioned path to mitigate the noise current. Common mode chokes are added between controller and digital isolators ($L_1$ and $L_2$), as well as between power ground and controller power supply ($L_{cp}$). The modified schematic is shown in Fig. 5-27 (b). The paralleled modules work properly after the modification.

## 5.6 Chapter Conclusion

Power converter modularity is an emerging and intriguing topic in power electronics. This chapter discusses the design and control of form-factor-constrained modular inverters. Because the system consists of inverter modules working in parallel, optimal design of each module leads to optimal system design. Thus, this chapter starts with optimization of the inverter modules, where the nominal power of the inverter module is to be maximized. Bi-level optimization is applied in the optimization framework. Four topologies, including three hard-switching topologies and one soft-switching topology, are included. The loss-size Pareto fronts under various nominal powers reveal that a maximum of 5 kVA nominal power can be achieved by T-type inverter.

A 5 kVA T-type inverter module prototype is constructed based on the optimization results. The module meets the form factor, EMI and thermal requirement, and achieved 99.2 % full load efficiency (36.4 W total loss) and 88 W/in$^3$ power density. The semiconductor device temperature reach 137 °C under natural convection cooling.

To scale up the system capability, a control system is developed for paralleling inverter modules. The control system consists of a central controller (DSP implementation) for output voltage control and multiple local controllers (FPGA implementation) for output current control of each module. All the local controllers are synchronized to the central controller through a dedicated clock wire. The local controllers do not communicate with each other, and there is no circulating current control. With the control architecture, two inverter modules working in parallel are tested, and the results show the functionality of the control implementation.

However, paralleling modules induces EMI problem. The switching of MOSFETs generates noise current that propagates through digital isolators and auxiliary power supplies and contaminate control ground. The total noise current is proportional to the number of paralleled modules, and control failure is observed when two modules are working in parallel. Adding chokes to the critical noise paths solves the problem, but better auxiliary power architecture is still sought.

The influence of form factor on module performance is finally discussed. The form factor limits the device selection and layout thus constrains performance (in this case, the maximum nominal power). The influence is revealed by comparing the maximum nominal power of an inverter module with doubled thickness and loss budget with two paralleled modules. The results show that the double-thickness module, thanks to easier thermal management and more freedom in EMI filter design, can achieve 33 % ~ 40 % more nominal power. In other words, larger form factor leads to higher power density and less flexibility. Determining optimal form factor requires tradeoff study at system level.

# Chapter 6. Conclusion

This work generalizes the converter design framework based on bi-level problem programing, presents the design and control of nominal-power-maximized modular converters and discusses the issues of converter modularization.

The work starts with presenting the characterization of switching transient of SiC MOSFETs, a key model in converter design. This work conducts two tests, namely, top-device-switching and bottom-device-switching tests, to characterize switching of MOSFETs accurately. Its necessity is backed by theoretical analysis and experimental results (without conducting top-device-switching the test, an error up to 19 % was found). Detailed data processing is presented, with which the turn-on energy is partitioned into four segments, namely, voltage-current overlap energy $E_{overlap}$, capacitive charge loss $E_{oss,channel}$, capacitive charge induced loss $E_{oss,induced}$ and reverse recovery loss $E_{rr}$. With the same driving circuit, $E_{overlap}$ does not change much when junction temperature changes while $E_{rr}$ increases at elevated temperature. The $E_{oss,channel}$ is different from $E_{oss,induced}$ owning the non-linearity of MOSFET output capacitors. Furthermore, the tests have been conducted in a wide temperature range (25 °C ~ 150 °C) with different MOSFETs (various die sizes and technologies). The testing results show the complexity of relating die size to switching loss mainly because reverse recovery loss is dependent of current density. In addition, the comparison between 2nd and 3rd generation devices demonstrates the superiority of 3rd generation devices.

Next, this work presents the design framework for nominal power maximization based on bi-level programming problem (BLPP). This approach not only finds the optimal design but also

renders fair comparison of converter topologies. The design of an active front-end converter is investigated using the framework. The optimal 1200 W Vienna rectifier prototype meets the form factor, loss constraints and complies with the DO-160E EMI and power quality standards, which verifies the design framework and models used in the the design. The prototype achieves 98.5 % full load efficiency and 33 W/in$^3$ power density, and it is natural convection cooled. To improve the input power quality, a control method is proposed to compensate the MOSFET turn-off delay in the prototype. The method uses datasheet information and is implementation-friendly to microcontroller. The effectiveness of the method is experimentally verified: under full load condition, the input current THD is improved from 3.6 % to 1.7 %; under half load, the input current THD is improved from 9.1 % to 4.7 %.

The design of a more complicated converter system, namely, a two-stage three-phase isolated ac/dc converter, is investigated based on the aforementioned design framework. Complete model for design of the second stage, an LLC resonant converter, is presented with special attention paid to the analytical model of litz-wire-wound transformer. An additional BLPP layer is added to accommodate the design of the two-stage system. This additional layer reveals the influence of dc bus voltage on overall performance. The design results show that increasing dc bus voltage induces loss increase in active front-end converter while lowers the loss in the second stage. The loss change in the two stages nearly compensates each other, and the performance of the overall system does not change much when dc bus voltage changes. The final 1200 W design uses 340 V dc bus voltage, achieves 97.1 % efficiency, 22 W/in$^3$ power density and natural convection cooling. The design meets the form factor constraint, the 35 W loss budget, the EMI and power quality standard.

The last chapter focuses on topology comparison, control of parallel operation and EMI issues in converter modularity. Four topologies, namely, two-level voltage source inverter, three-level neutral-point-clamped inverter, T-type inverter and triangular conduction mode inverter, are investigated for motor drive application. The T-type inverter achieves the highest nominal power. The prototype achieves 99.2 % full load efficiency, 89 W/in$^3$ power density and natural convection cooling. A master-slave control architecture with designated synchronization scheme is used to parallel the modular converters. The proposed control scheme achieves good synchronization and eliminates the communication between converter modules, enabling a fully modularized design. The system-level issues of converter modularization, namely, influence of form factor and EMI issue are studied. For the former issue, the double-thickness module, thanks to easier thermal management and more freedom in EMI filter design, can achieve 33 % ~ 40 % more nominal power, demonstrating the tradeoff between flexibility and performance. For the latter, paralleling modular converters aggravates signal level and system level EMI noise. To tackle the noise in both level, module designers should take the maximum paralleling number into account when designing the filter for input, output and control system.

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