Synchronous-Conduction-Mode Tapped-Inductor Buck Converter for Low-Power, High-Density Application

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ABSTRACT

General-purpose step-down converter is essential in electronic system for processing energy from high-voltage rail to low-voltage circuits. The applications can be found at the auxiliary supplies in automobile, industrial and communication systems. Buck converter is a common circuit topology to fulfill step-down conversion, especially in low-power application since it is well-studied and straightforward. However, it suffers from low duty cycle under high step-down condition, and typically operates in continuous conduction mode (CCM) that generates large switching loss. On the other hand, as an extension of the buck converter, tapped-inductor (TI) buck converter has larger duty cycle while maintaining the structural simplicity. Therefore, the main objective of this thesis is to explore the potential of TI buck converter as a wide conversion range, high power density and high efficiency topology for low power application. To achieve high efficiency at switching frequency of MHz-level, synchronous conduction mode (SCM) is applied for turn-on losses elimination.

The operation principle and power stage design of SCM TI buck is first introduced. The design of high switching frequency coupled inductor is emphasized since its size plays a critical role in power density. Loss breakdown is also provided to perform a comprehensive topological study. Secondly, detailed zero-voltage-switching (ZVS) condition of SCM TI buck is derived so that the converter does not experience redundant circulating energy. The experimental results of 15-W SCM TI buck converter prototypes are provided with 90.7% of peak power stage efficiency.

The size of coupled inductor is down to 116 mm^3. To enhance light-load efficiency, a variable frequency control scheme based on derived ZVS conditions is implemented with the switching frequency ranging from 2 MHz to 2.9 MHz.

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GENERAL AUDIENCE ABSTRACT

General-purpose step-down converter is essential in electronic system for processing energy from high-voltage rail to low-voltage circuits. The applications can be found at the auxiliary supplies in automobile, industrial and communication systems. Typically, the ultimate goals of general-purpose step-down converter are versatility, high efficiency and compact size.

Recently, tapped-inductor (TI) buck converter is studied since it could overcome the drawback of commonly used buck converter under high step-down conversion. Therefore, the potential of TI buck converter as a general-purpose step-down converter candidate is explored in this thesis, including control method, hardware design, etc. The thesis verifies that TI buck converter could have compact size while remaining efficient and adaptable.

To my parents,
Kang-Hsiung Yeh
Hui-Yin Chen

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Chapter 1

Introduction

1.1 Overview of General-Purpose Step-down Converter

Every electronic system has power supplied from a battery or line source [1], establishing main dc voltage rail. The rail voltage depends on application. For example, in a near future, on-board vehicle electrical system may have a 48-V dc rail [2]. On the other hand, computation, sensing, communication and various functions rely on circuits operating with low dc voltage, like 5 V and 3.3 V [3]. Many of these low-voltage circuits are designed for peripheral devices which consume limited power, for instance, advanced driver assistance system (ADAS) and infotainment system in automobile application [4]. As a result, low-power step-down converter (i.e., general-purpose step-down converter) is essential and it can serve as auxiliary power supply as well. The illustration of an electronic system example is shown in Figure 1.1 and red block represents general-purpose step-down converter.

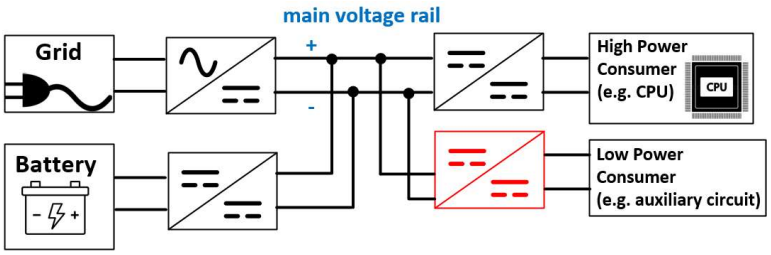


Figure 1.1. Example of electronic system

Numerous commercial products target on the need for such general-purpose step-down conversions [5]-[7] and the following specifications are significant. First of all, input and output voltage range determines the field in which a converter fits. Wide operating range leads to versatile

product preferred by system designers. Second, all converters together could contribute to a noticeable loss, so efficiency is also of great importance. Typically, maximum output current of a converter is specified since efficiency is ought to be optimized according to the load range. To consider low-power application, in this thesis, the output current is no more than 3 A. Finally, power supplies could consume up to half of the board space of an electronic system [1], so dimensions matter. Whether a general-purpose converter product requires external inductor [5] or owns integrated inductor [6]-[7], magnetic component has dominating impact on overall size.

1.2 State-of-the-Art High Step-Down Converter Topologies

It has been mentioned in the last section that a general-purpose converter should adapt to various working conditions, and one of the challenging scenarios is high step-down conversion, for instance, converting 60 V to 3.3 V. Therefore, state-of-the-art topologies for high step-down converter are summarized and discussed in this section.

To begin with, the buck converter, as a well-studied single-stage topology, stands out for its simplicity and has already been commercialized [5]-[7]. Nevertheless, under high step-down conversion, its narrow duty cycle limits controllability due to short conduction time of the main switch [8]. The situation is even worse when high switching frequency is utilized for downsizing energy storage components. Besides, when high-switching-frequency buck converter operates in continuous conduction mode (CCM), switching loss also becomes problematic. Isolated topologies of buck converter including forward, full-bridge and half-bridge converter can adjust duty cycle by transformer turns ratio, but they are too complicated for low power design.

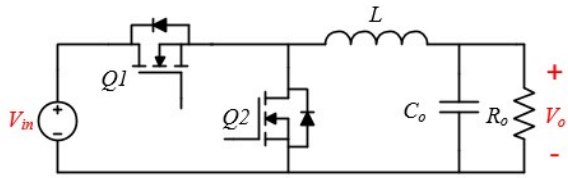
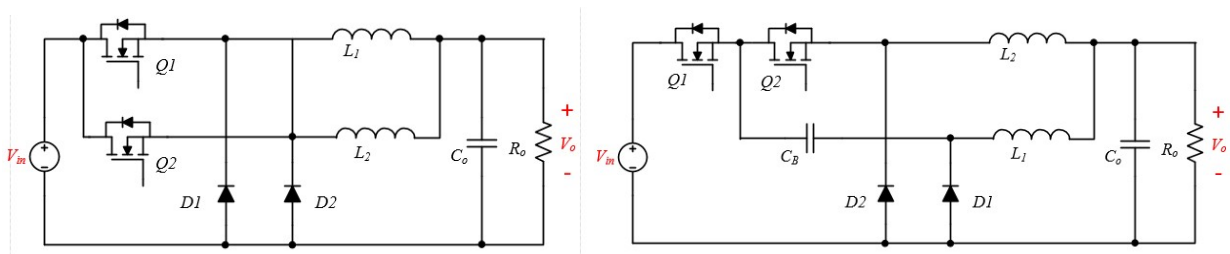


Figure 1.2. Buck converter with synchronous rectifier

Interleaving technique is applied to buck converter when load current is large in applications such as point-of-load (POL) [9]. Conventional interleaved buck converter alleviates component current stress, but the issue of narrow duty cycle remains under high step-down conversion. To solve the problem, a modified interleaved buck converter featuring both current splitting and duty cycle extension is proposed in [10], as shown in Figure 1.3(b). However, compared with single-phase buck converter, the doubled component amount still holds the converter back from low-power application.



(a) (b)

Figure 1.3. Interleaved buck converter: (a) conventional topology and (b) modified topology in [10]

An alternative solution is two-stage converters [11]-[13] or even topologies with more stages. In [11], 12 V to 1.2 V conversion is fulfilled by a two-phase buck converter cascaded with another four-phase buck converter. In [12] and [13], buck-type converter has switching-capacitor (SC) front stage, which is an efficiency way to curtail input voltage for buck stage. An example of two stage SC-buck converter is demonstrated in Figure 1.4 [12]. However, the complicated circuit structure raises design difficulty, cost and size so again it is not favorable to low-power product.

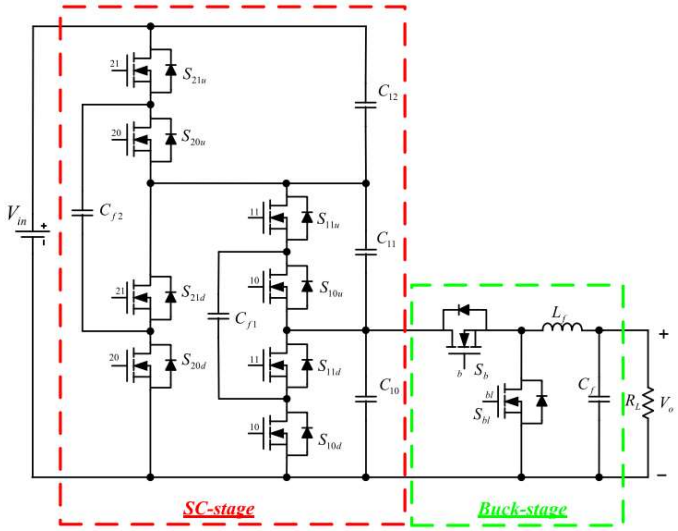


Figure 1.4. Two stage SC-buck converter

Multilevel buck converter [14]-[15] or buck-type converter using voltage divider technique [16] also serves as a candidate for high step-down topology. It has advantage of cutting down device voltage stresses [14], [16], which is especially useful in the case of high input voltage, or reducing voltage across inductor to decrease inductance needed [15]. In [16], the converter even features duty cycle doubling. Unfortunately, for low input voltage (< 100 V) applications, the benefit of voltage stress reduction is not prominent. Besides, the gate driving circuit in multilevel converter could be an issue [17].

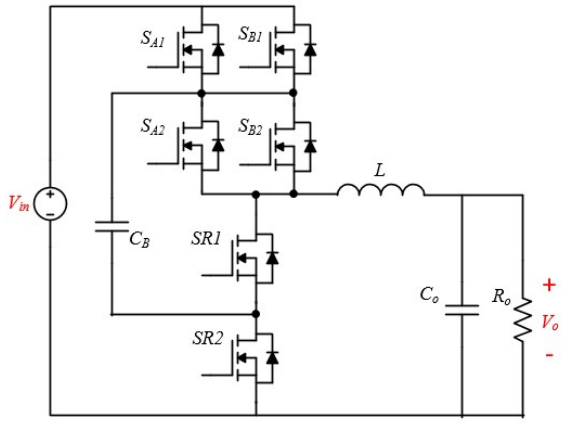


Figure 1.5. Asymmetrical three-level buck converter in [15]

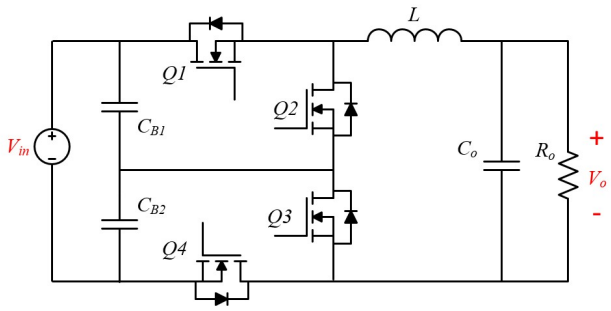
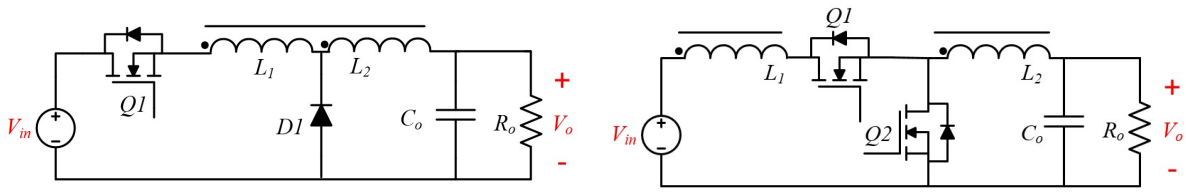


Figure 1.6. Buck-type converter with voltage dividing technique in [16]

Most of the topologies to undertake high step-down conversion aim for applications with a higher power level, but the circuit complexity becomes a problem when they are adapted to low power application. Therefore, high step-down converter with limited components is desired and a family of converter using coupled inductor serves the need. Tapped-inductor (TI) buck converter is the fundamental topology among these converters, and it is also the subject of this thesis [18]-[20].

TI buck converter has same component amount as buck converter and features extended duty cycle. Furthermore, by re-arranging the position of high-side switch and primary winding, simple bootstrap gate driver can be utilized in TI buck [19]. In this case, tapped-inductor becomes a coupled inductor, but the circuit is still called TI buck for consistency.



(a) (b)

Figure 1.7. TI buck converter: (a) original version in [18] and (b) modified version in [19]

Based on TI buck converter, hybrid-transformer-based (HTB) buck converter was proposed in [21] to extend duty cycle additionally but it requires external resonant inductor. Therefore, series-capacitor tapped buck (SC-TaB) converter was proposed in [22] to perform

resonance through leakage inductor. In [23], the converter is further modified into hybrid resonant buck converter for avoiding the use of isolated gate driver. These TI buck-based converters have duty cycle larger than TI buck converter and enhanced soft-switching function. Nevertheless, unlike TI buck, its maximum voltage conversion ratio could be less than 0.5 [22]-[23]. As a result, the attempt to achieve wide operation range backfires. Moreover, the losses from auxiliary switch could overwhelm the soft-switching benefit it brings.

In conclusion, TI buck converter is the simplest topology featuring extended duty cycle. Compared with other approaches regarding high step-down or wide operation range, it is advantageous in low-power application.

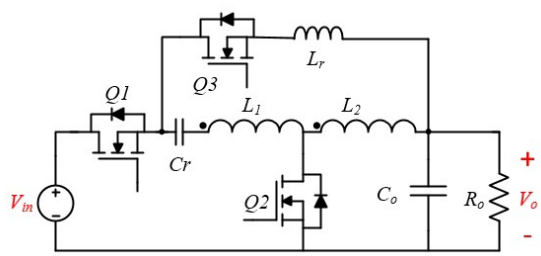


Figure 1.8. Hybrid-transformer-based (HTB) buck converter

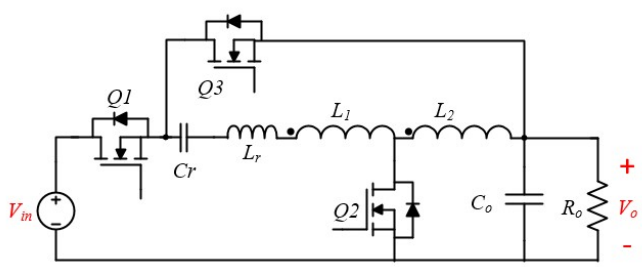


Figure 1.9. Series-capacitor tapped buck (SC-TaB) converter

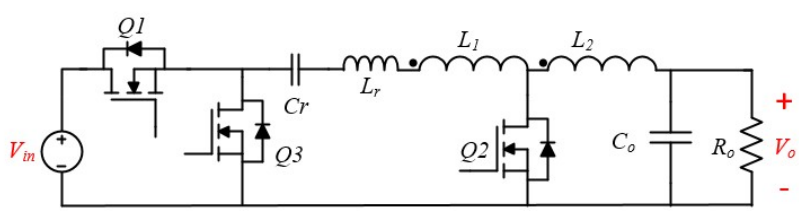


Figure 1.10. Hybrid resonant buck converter

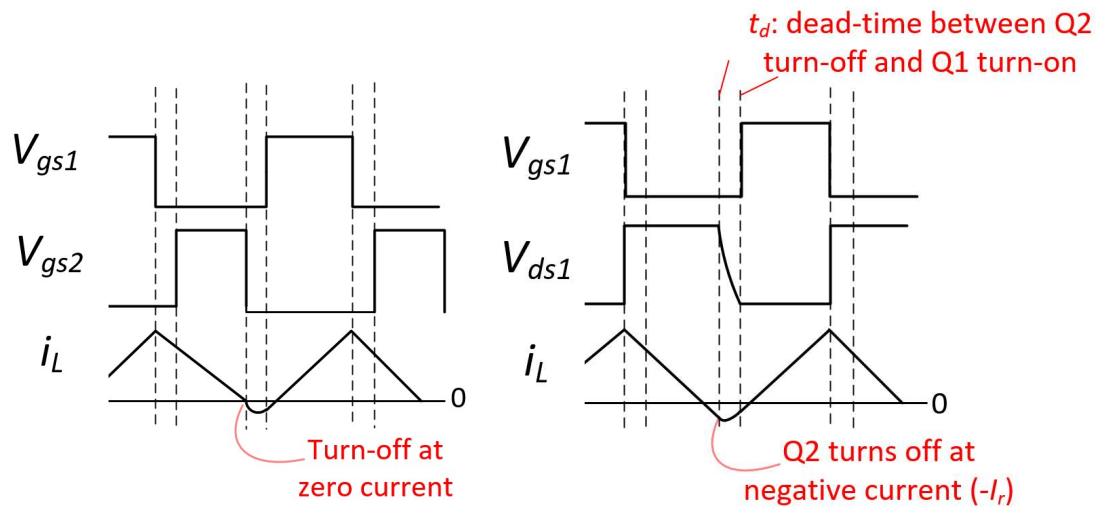
1.3 Synchronous Conduction Mode

It has been mentioned in the last section that CCM buck converter suffers from hard switching. For a CCM buck converter with synchronous rectifier (Figure 1.2), bottom device naturally has ZVS turn-on. However, the hard turn-on of top device is harmful not only because of large switching losses but also the voltage spike it creates.

It is possible to obtain ZVS of top device by running the buck converter in critical conduction mode (CRM), which is also known as boundary conduction mode (BCM). In CRM, inductor current rebounds once it touches zero, as shown in Figure 1.11 (a), so current ripple is larger than the ripple under CCM. Moreover, the ZVS of top device holds only when $V_{in} < 2V_o$ [24].

To broaden ZVS region, synchronous conduction mode (SCM) was proposed as shown in Figure 1.11 (b) [25]-[26]. Inductor current flows into opposite direction to enhance ZVS mechanism. In general, ZVS can be obtained under all working conditions if sufficient reverse current I_r and dead-time t_d are provided. The detailed ZVS conditions for SCM buck converter can be found in [25].

The idea of SCM can be extended to TI buck converter as well. With the aid of SCM, TI buck converter can obtain ZVS at both switches and operate in high switching frequency. Consequently, power density can be increased.



(a) (b)

Figure 1.11. Inductor current waveform: (a) CRM buck converter and (b) SCM buck converter

1.4 Research Objectives and Thesis Outline

The potential of TI buck converter has been introduced in previous section. The primary target of this research is to evaluate its performance as a general-purpose step-down converter. The design of the converter has several critical requirements.

(1) General-purpose step-down converter should cover wide operation range, from high step-down conversion (e.g., 60 V to 3.3 V) to low step-down conversion (e.g., 24 V to 12 V).

(2) Efficiency is the most significant indicator of converter performance.

(3) The size of magnetic component has strict constraint. In order to apply compact magnetic core, switching frequency is pushed to MHz range.

In MHz range, switching loss is considerable so soft-switching technique is urged. In [18], CRM is applied to TI buck converter, creating ZVS of top device. Unfortunately, ZVS function realized by CRM is restricted to converter working condition. In order to solve the issue, it is proposed in this thesis that TI buck converter operates in SCM. In this way, the converter is capable of top device ZVS, regardless of working condition. Finally, the thesis is organized as follows:

Chapter 1 presents the application scope and summarizes relevant state-of-art topologies to explain why TI buck converter is a good candidate for general-purpose step-down converter.

Chapter 2 provides theoretical background in terms of the TI buck converter including basic operation principle, zero-voltage-switching feature realized by SCM and voltage mode control scheme.

Chapter 3 introduces the design and implementation of SCM TI buck converter, especially the magnetic core and PCB winding of compact coupled inductor.

Chapter 4 demonstrates experimental results and loss breakdowns.

Finally, research summary and proposed future work are shown in Chapter 5.

Chapter 2

Synchronous-Conduction-Mode TI Buck Converter Topology and Operation

2.1 Principle of Operation

The topology of TI buck converter is shown in Figure 2.1 and turns ratio n is defined in (2.1). In early stage, leakage inductance of coupled inductor is neglected, so magnetic model becomes an ideal transformer (N_1:N_2) with magnetizing inductor L_m. Note that L_m is placed at output end to accord with the inductor of buck converter. Moreover, when n equals zero, Figure 2.1 degenerates into buck converter.

$$n = \frac{N_1}{N_2} \tag{2.1}$$

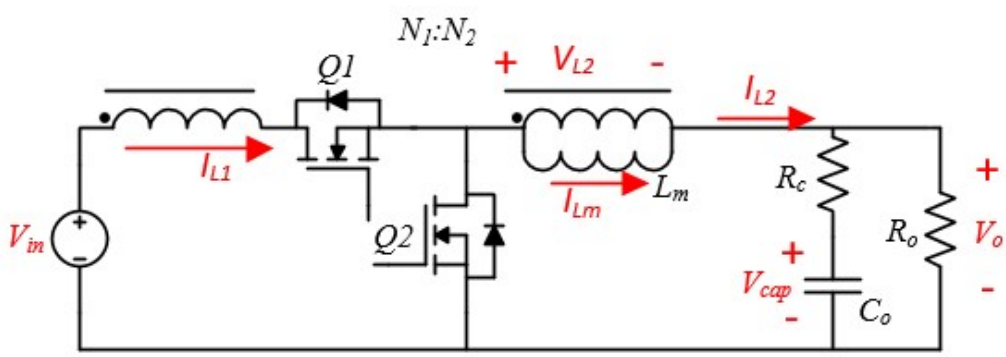


Figure 2.1. TI buck converter topology

Similar to buck converter, the operation mode of TI buck converter can be defined by magnetizing current (I_{Lm}). When I_{Lm} is always positive, the converter operates in continuous conduction mode (CCM). When I_{Lm} rebounds once it reaches zero, the converter operates in critical conduction mode (CRM) or boundary conduction mode (BCM). Finally, when I_{Lm} goes

into negative region, the converter operates in synchronous conduction mode (SCM) [20].The steady-state waveforms of SCM TI buck converter is shown in Figure 2.2 and the operation principles in different states are explained as follows.

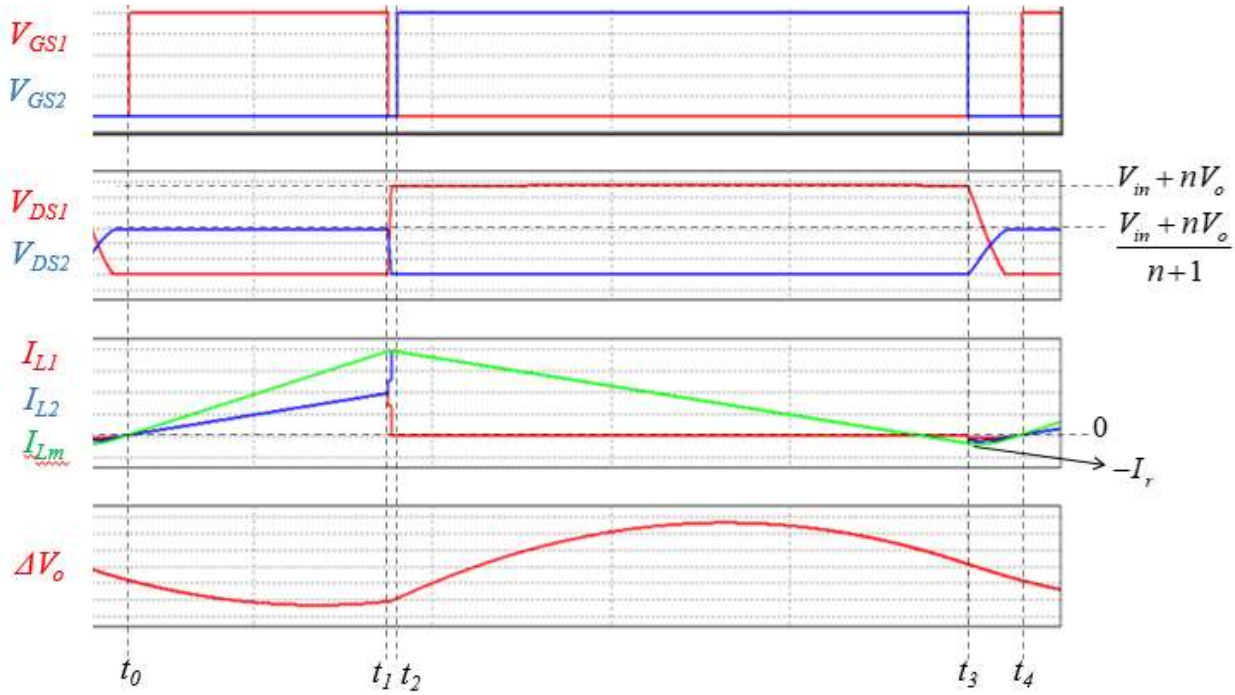


Figure 2.2. Steady-state waveforms of SCM TI buck converter

State 1 [t_0-t_1]: Initially, Q1 turns on by soft-switching and initiates power delivery stage. Coupled inductor absorbs energy in this state. Two windings are in series-aiding configuration and I_{L2} (=I_{L1}) increases linearly.

State 2 [t_1-t_2]: After Q1turns off, the C_{oss} of Q2 discharges quickly due to large current (I_{L2}). Therefore, the body diode of Q2 begins to conduct current also immediately after t_1 and ZVS of Q2 can be obtained in next state. Additionally, due Ampere's circuital law and the continuity of magnetic flux, I_{L1} is reflected to the other side, adding current on top of original I_{L2}. Consequently, current "jump" can be observed from I_{L2} waveform.

State 3 [t_2-t_3]: Q2 turns on by soft-switching and continues the freewheeling. I_{L2} equals I_{Lm}, decreasing linearly. Before I_{Lm} reaches zero-crossing-point (ZCP), energy is released from

coupled inductor. In SCM, I_{L2} eventually flows into opposite direction. When I_{L2} is reversed, energy is deposited in coupled inductor to ready for ZVS of Q1.

State 4 $[t_3\text{-}t_4]$: After Q2 turns off, the energy in L_m helps discharge the output capacitance (C_{oss}) of Q1. Once C_{oss} of Q1 is fully discharged, its body diode conducts. As a results, Q1 can turn on with zero-voltage in state 1. The ZVS of Q1 is the main feature of SCM and unlike the ZVS of Q2, it is more difficult to achieve. Therefore, the voltage commutation is slower and longer dead-time is required. The ZVS conditions of Q1 are derived in later section.

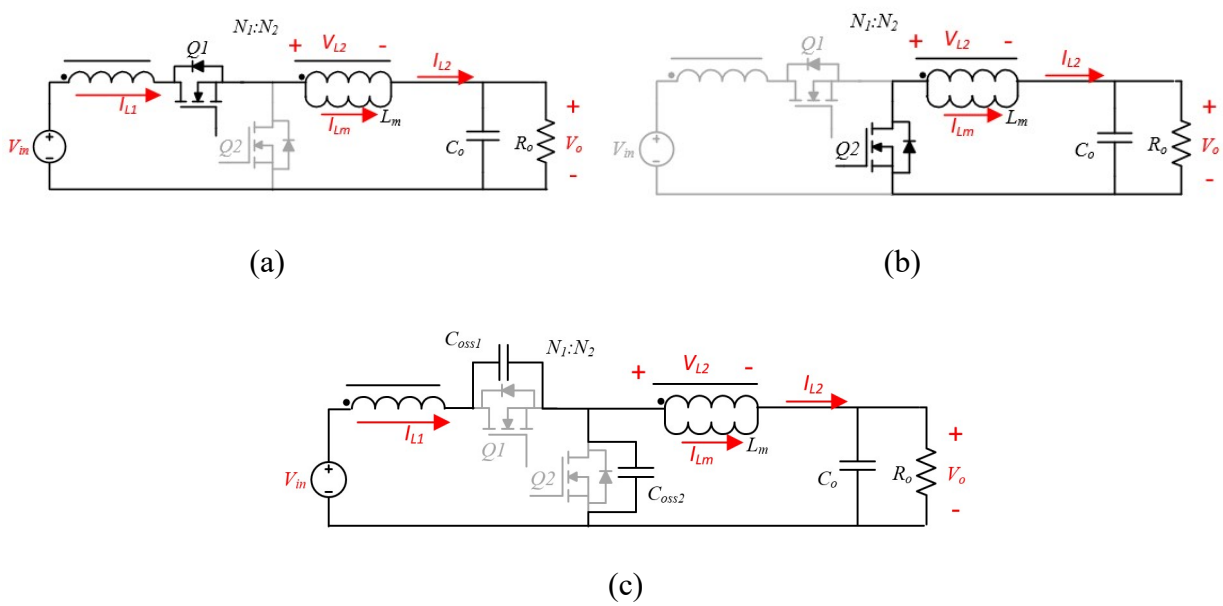


Figure 2.3. TI buck converter operation mode: (a) power delivery stage (state 1), (b) freewheeling stage (state 2 and state 3) and (c) voltage commutation stage (state 4)

2.2 Duty Cycle and Component Stresses

The duty cycle of TI buck converter can be calculated by voltage-second balance of L_m. To simplify the equation, assume dead-time (state 2 and state 4) durations are negligible. When Q1 is turned on, the voltage across L_m (V_{L2}) is lower than V_{in} since primary-side winding N_1 helps dividing voltage, as described by (2.2). When Q1 is turned off, the voltage across L_m is same as

the one in buck converter and described by (2.3). By voltage-second-balance equation (2.4), the conduction time of Q1 should be longer in TI buck for its lower V_{L2} from (2.2). Therefore, TI buck converter has wider duty cycle over buck converter, as derived in (2.5).

$$V_{L2} = \frac{V_{in}N_2 + V_o N_1}{N_1 + N_2} - V_o \tag{2.2}$$

$$V_{L2} = -V_o \tag{2.3}$$

$$\left(\frac{V_g N_2 + V_o N_1}{N_1 + N_2} - V_o\right) D T_s = V_o (1 - D) T_s \tag{2.4}$$

$$D = \frac{V_o (n+1)}{V_o n + V_{in}} \tag{2.5}$$

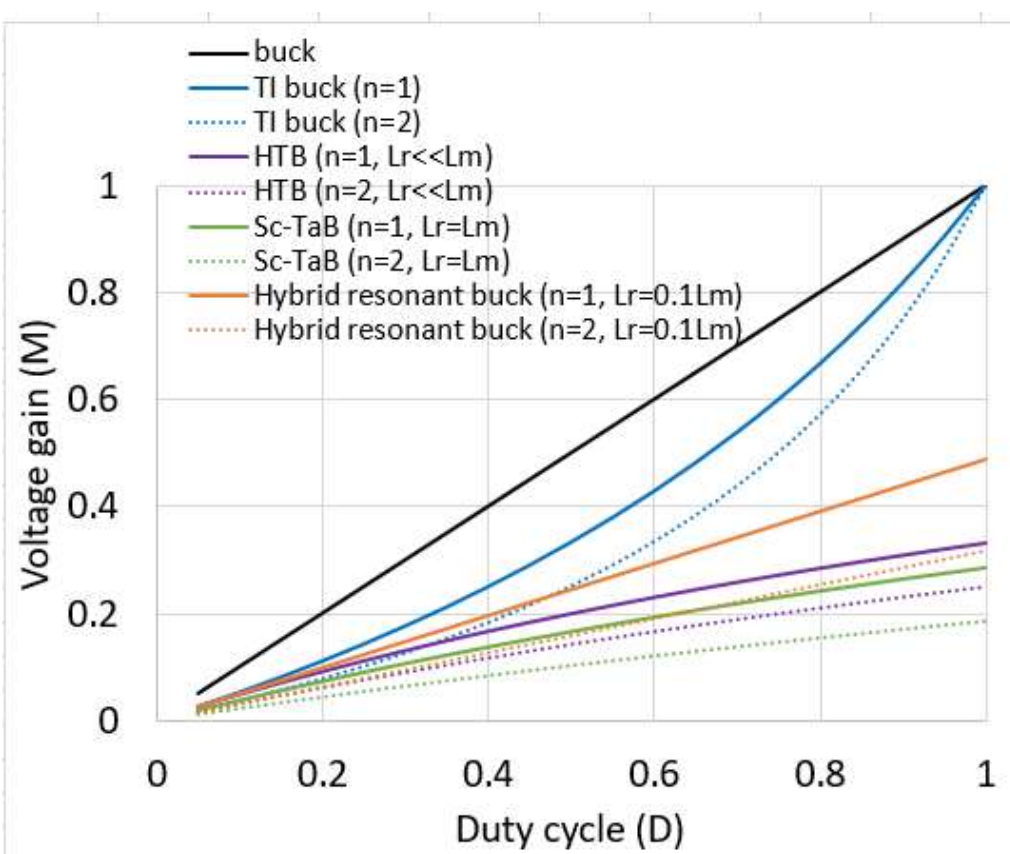


Figure 2.4. Voltage gain versus duty cycle for buck, TI buck, HTB, Sc-TaB and hybrid resonant buck

The voltage gain ($M=V_o/V_{in}$) versus duty cycle curves are summarized in Figure 2.4. Compared with buck converter, TI buck converter has extended duty cycle, which is beneficial in high step-down conversion. On the other hand, compared with other coupled-inductor-based topologies like HTB, Sc-TaB, hybrid resonant buck converter [21]-[23], TI buck converter has wider working region. Its voltage gain can range from 0 to 1.

Once duty cycle is decided, the average current of Q1 and Q2 can easily be derived, as shown in (2.6) and (2.7). From the formulas, Q2 handles larger current under high step-down condition.

$$I_{Q1,avg} = DI_o \tag{2.6}$$

$$I_{Q2,avg} = (1-D)I_o \tag{2.7}$$

The voltage stress for the device can be derived by Kirchhoff's voltage law (KVL), as shown in (2.8) and (2.9). Since primary and secondary-side winding create voltage-dividing effect, Q2 has voltage stress lower than V_{in}. When n equals 1, the voltage stress of Q2 is almost halved.

$$V_{Q1,\max} = V_{in} + nV_o \tag{2.8}$$

$$V_{Q2,\max} = \frac{V_{in} + nV_o}{n+1} \tag{2.9}$$

2.3 Zero-Voltage-Switching Conditions

In order to remove turn-on losses and corresponding voltage spike, EMI noises, ZVS technique is desired. In Figure 2.1, Q2 has ZVS easily because large current (I_{L2}) helps its Coss discharge quickly. The same phenomenon occurs in general synchronous buck converter. However, the ZVS of Q1 is more difficult. In CRM TI buck converter, the ZVS condition of Q1 is (2.10) 55[18].

$$n \geq \frac{V_{in}}{V_o} - 2 \tag{2.10}$$

In this thesis, SCM is applied to TI buck converter to extend ZVS region of Q1. To discharge C_{oss} of Q1 before it turns on, two critical conditions should be satisfied: (1) enough reverse magnetizing current (I_r in Figure *2.2*) and (2) sufficient dead-time t_d (between t_3 and t_4 in Figure *2.2*). In [25], the ZVS condition of SCM buck converter is derived by considering time-domain resonant model. The idea can be applied to SCM TI buck converter as well.

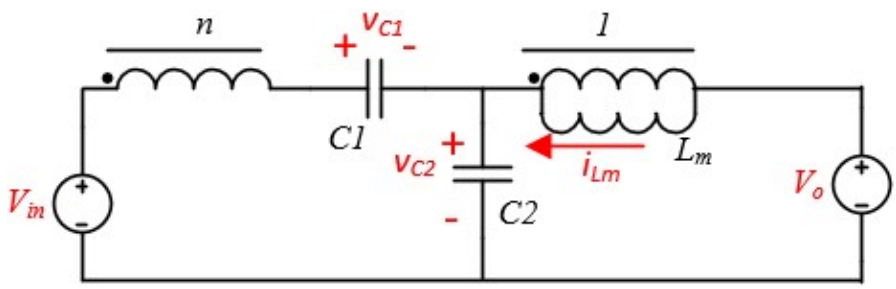


Figure 2.5. Equivalent resonant circuit model in state 4

Figure 2.5 shows the equivalent circuit model in state 4. Few assumptions are applied. First, output filtering capacitor (C_o) is large enough so that output voltage remains constant within state 2. Second, the windings are perfectly coupled so leakage inductance can be neglected. Third, the C_{oss} of Q1 and Q2 (*C1* and *C2* in Figure 2.5) are linear.

At t_3, reverse magnetizing current has magnitude of I_r. Also, since Q2 is conducted in previous state, voltage across *C2* is 0. The voltage of *C1* can be found in (2.8). To sum up, the initial conditions are listed in (2.11).

$$\begin{cases} i_{Lm}(0) = I_r \\ v_{c1}(0) = V_{in} + nV_o \\ v_{c2}(0) = 0 \end{cases} \tag{2.11}$$

In state 4, the behavior of the converter is dominated by the resonance between *C1*, *C2* and L_m. The resonant equations can be listed by using KVL and KCL, as shown in (2.12).

$$\begin{cases} V_o = v_{c2} + L_m \dfrac{di_{Lm}}{dt} \\ V_{in} + nL_m \dfrac{di_{Lm}}{dt} = v_{c1} + v_{c2} \\ i_{Lm} + (n+1)C_1 \dfrac{dv_{c1}}{dt} = C_2 \dfrac{dv_{c2}}{dt} \end{cases} \tag{2.12}$$

The solution to differential equation (2.11), (2.12) is shown in (2.13), where resonant frequency ω_r and characteristic impedance Z_r are defined in (2.14) and (2.15).

$$\begin{cases} i_{Lm}(t) = I_r \cos(\omega_r t) + \dfrac{V_o}{Z_r} \sin(\omega_r t) \\ v_{c2}(t) = Z_r I_r \sin(\omega_r t) + V_o(1 - \cos(\omega_r t)) \\ v_{c1}(t) = (V_{in} - V_o) - (n+1)\sqrt{V_o^2 + I_r^2 Z_r^2} \sin(\omega_r t - \tan^{-1}(\dfrac{V_o}{I_r Z_r})) \end{cases} \tag{2.13}$$

$$\omega_r = \frac{1}{\sqrt{L((n+1)^2 C_1 + C_2)}} \tag{2.14}$$

$$Z_r = \sqrt{\frac{L}{(n+1)^2 C_1 + C_2}} \tag{2.15}$$

Whenever v_{c1} reaches zero, the body diode of Q1 conducts (assuming ideal diode) and ZVS can be obtained in next state. In the other word, minimum v_{c1} should be less than zero. Consequently, the ZVS condition in terms of I_r can be derived, as shown in (2.16). Moreover, v_{c1} should reach zero before dead-time runs out, so the ZVS condition in terms of t_d is shown in (2.17).

$$I_r \geq \sqrt{\frac{C_1 + \dfrac{1}{(n+1)^2} C_2}{L_m}} \sqrt{(V_{in} + nV_o)(V_{in} - (n+2)V_o)} \tag{2.16}$$

$$t_d \geq \frac{1}{\omega_r} \left[\sin^{-1}\left(\frac{V_{in} - V_o}{(n+1)\sqrt{V_o^2 + I_r^2 Z_r^2}} \right) + \tan^{-1}(\frac{V_o}{I_r Z_r}) \right] \tag{2.17}$$

If I_r happens to be the minimal value (i.e., $I_{r,min}$) that allows Q1 ZVS (i.e., equality in (2.16) holds), then its corresponding ZVS condition of t_d can be simplified as (2.18).

$$t_d \geq \frac{1}{\omega_r}\left[\frac{\pi}{2} + \tan^{-1}\left(\frac{V_o}{I_r Z_r}\right)\right] \tag{2.18}$$

With (2.16) and (2.17), the figure of ZVS region can be plotted, as shown in Figure 2.6. The upper right corner is where ZVS can be obtained since it has sufficient I_r and t_d. The lines in the figure define ZVS boundary under different circumstances and the vertical part indicates $I_{r,min}$. Given a fixed turns ratio n and fixed V_o, I_r requirement is higher when V_{in} is higher from Figure 2.6. Besides, TI buck converter with higher n is able to achieve Q1 ZVS with lower I_r, but in the meantime, longer t_d is necessary. The case of n=0 indicates buck converter whose I_r constraint is the highest yet t_d constraint is the lowest.

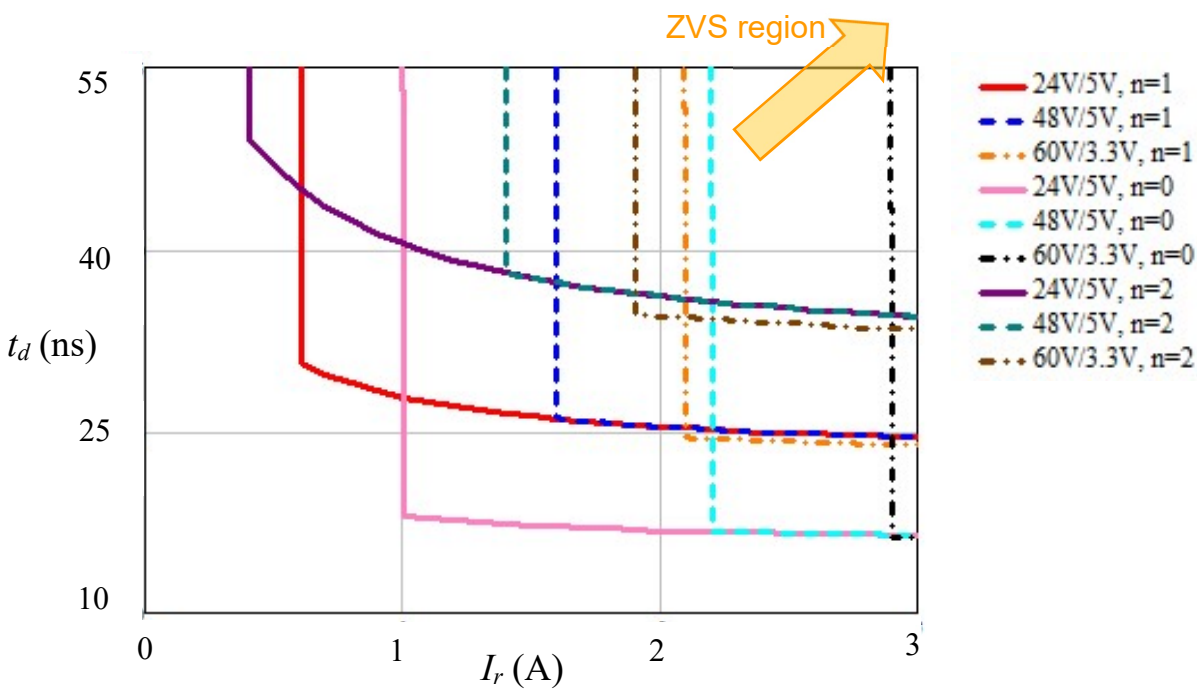


Figure 2.6. ZVS region (C_1 = 186 pF, C_2 = 310 pF, L_m = 200 nH)

An accurate ZVS condition is important because excessive t_d leads to extra body diode conduction loss. In addition, excessive I_r creates redundant circulating energy, which generates

additionally current ripple and magnetic flux. The wasted power could be only tens or hundreds of milliwatt. However, in lower power application, every minute loss affects power efficiency, so delicate model of top-device ZVS comes in handy.

2.4 Control Scheme with Variable Switching Frequency

To minimize circulating energy, it is desired for SCM TI buck converter to turn off bottom device once I_{Lm} reaches $I_{r,min}$. To control the valley current, switching frequency has to adjust according to different working condition.

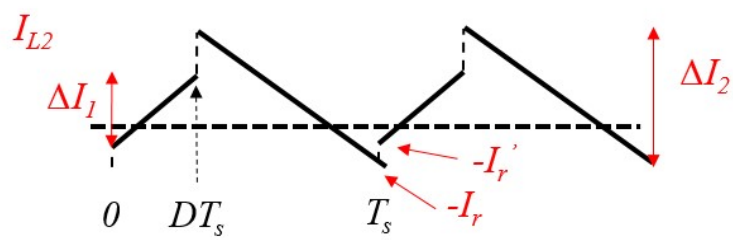


Figure 2.7. Current waveform of secondary-side winding under SCM

Figure 2.7 shows current waveform of secondary-side winding, which has average current same as load current, as described in (2.19). Note that dead-time is once again neglected to simplify the expression. Secondary-side current increment (ΔI_1) and decrement (ΔI_2) are calculated in (2.20). The current jump at Q2 turn-off can be solved by Ampere's circuital law, as shown in (2.21). In practical design, some margin will be set up to guarantee the ZVS of Q1, but in this section, it is assumed I_r equals $I_{r,min}$.

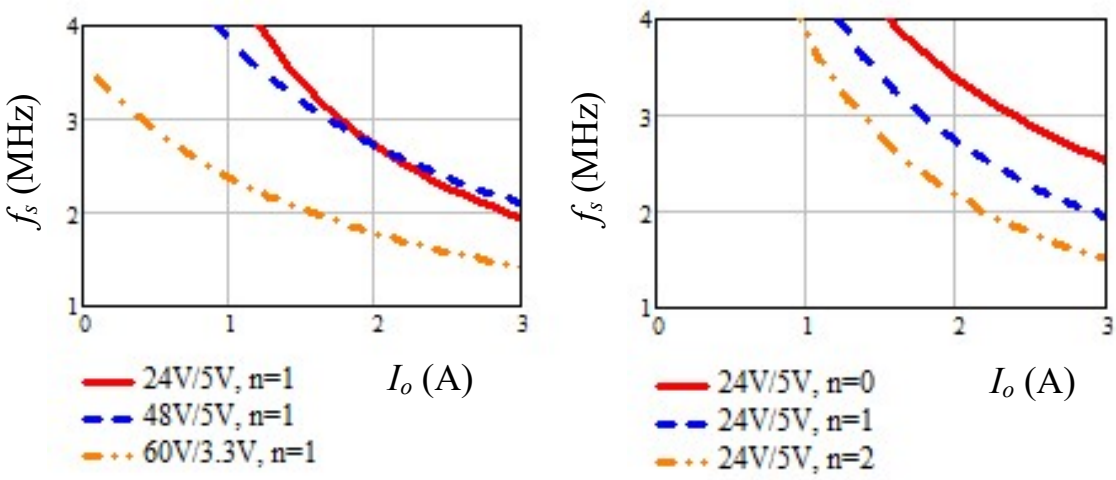
$$I_o = \langle I_{L2} \rangle = \left(\frac{\Delta I_1 - 2I_r'}{2}\right)D + \left(\frac{\Delta I_2 - 2I_r}{2}\right)(1-D) \tag{2.19}$$

$$\Delta I_1 = \frac{(V_{in} - V_o)D}{(n+1)^2 L_m f_s},\ \Delta I_2 = \frac{V_o(1-D)}{L_m f_s} \tag{2.20}$$

$$I_r' = \frac{I_r}{n+1} \tag{2.21}$$

The equation of switching frequency (f_s) can be derived by summarizing (2.19)-(2.21), as listed in (2.22) and plotted in Figure 2.8 (given $C_1 = 186\ pF$, $C_2 = 310\ pF$, $L_m = 200\ nH$).

$$f_s = \frac{\dfrac{(V_{in} - V_o)D^2}{2(n+1)^2 L_m} + \dfrac{V_o(1-D)^2}{2L_m}}{I_o + (\dfrac{D}{n+1} + (1-D))I_{r,\min}} \tag{2.22}$$



(a) (b)

Figure 2.8. Switching frequency versus load current: (a) fixed turns ratio and (b) fixed working condition

From Figure 2.8, f_s raises as load current (I_o) or turns ratio (n) decreases. Furthermore, designer should keep in mind that f_s is not unrestricted. In a real converter, switching frequency affects magnetic permeability, gate driver capability and so on. Therefore, an upper bound like 3 MHz is set and limits the f_s at light-load condition.

Valley current mode control and constant on-time control are the most intuitive way to realize the desired circulating energy minimization [27]. It turns off Q2 once I_{L2} goes beyond the threshold $I_{r,min}$. Nevertheless, to implement either control method, high-bandwidth short-delay current sensor is required. Otherwise, the valley point of the current cannot be precisely captured.

An alternative way is using indirect method to adjust switching frequency according to (2.22), which requires information of V_{in}, V_o, I_o. Since I_o is output dc current, its sensing circuit does not need high bandwidth. As the name implies, indirect method has no direct information of valley current of I_{L2}. Instead, it works by estimating the valley current. From the perspective of control, switching frequency variation is a slow outer loop and only serves for efficiency optimizing purpose. The output voltage regulation is still performed by duty cycle control.

2.5 Small-Signal Analysis under Voltage Mode Control

From previous section, switching frequency is updating slowly to optimize power efficiency, so high-bandwidth voltage loop is assumed to be immune from the effect of switching frequency variation. As a result, the concept of traditional voltage mode control (VMC) can be applied to TI buck converter. This section is mean to briefly introduce the dynamic performance of VMC TI buck converter, providing analog controller designer helpful information.

Dynamic performance of switch-mode power supply (SMPS) can be analyzed by state-space averaging model [28]. For TI buck converter (as shown in Figure 2.1), a few assumptions are made: ideal switches, perfect coupling, zero winding resistance, small R_c (equivalent series resistance (ESR) of C_o) compared to R_o. The state variables are magnetizing current i_{Lm} and output filtering capacitor voltage v_{cap}. After weighted averaging by duty ratio, the state-space representation is found in (2.23).

$$\begin{cases} \begin{bmatrix} L_m & 0 \\ 0 & C_o \end{bmatrix} \begin{bmatrix} \dot{i}_{Lm} \\ \dot{v}_{cap} \end{bmatrix} = \begin{bmatrix} \dfrac{-R_c D}{(n+1)^2} - D'R_c & \dfrac{-D}{n+1} - D' \\ \dfrac{D}{n+1} + D' & \dfrac{-1}{R_o} \end{bmatrix} \begin{bmatrix} i_{Lm} \\ v_{cap} \end{bmatrix} + \begin{bmatrix} \dfrac{D}{n+1} & \dfrac{-R_c D}{n+1} - D'R_c \\ 0 & 1 \end{bmatrix} \begin{bmatrix} v_{in} \\ i_o \end{bmatrix} \\ [v_o] = \begin{bmatrix} \dfrac{R_c D}{n+1} + D'R_c & 1 \end{bmatrix} \begin{bmatrix} i_{Lm} \\ v_{cap} \end{bmatrix} + \begin{bmatrix} 0 & R_c \end{bmatrix} \begin{bmatrix} v_{in} \\ i_o \end{bmatrix} \end{cases} \quad (2.23)$$

Next, perturbation and linearization process are added to (2.23) and then DC terms can be cancelled off. In is way, small-signal state-space average model is obtained. The most significant information we can learn from the model is control to output voltage transfer function (G_{vd}), which is derived by ceasing all other perturbations (like $\hat{i}_o$ and $\hat{v}_{in}$). The formula of G_{vd} is listed in (2.24) and verified in software Simplis, as shown in Figure *2.9* (V_{in} = 24 V, V_o = 5 V, L_m = 180 nH, n = 1, C_o = 10 μF, R_c = 10 mΩ, R_o = 1.7 Ω, f_s = 2 MHz).

$$G_{vd} = \frac{\hat{v}_o}{\hat{d}} = K_{vd} \frac{1+\frac{s}{\omega_z}}{1+\frac{s}{Q_o\omega_o}+\frac{s^2}{\omega_o^2}}$$

$$K_{vd} = V_{in}\frac{n+1}{(D+(n+1)D')^2},\ \omega_z = 1/(R_cC_o - \frac{L_m}{R_o}\frac{nD}{(\frac{D}{n+1}+D')^2})$$

$$\omega_o = (\frac{D}{n+1}+D')\frac{1}{\sqrt{L_mC_o}},\ Q_o = \frac{(\frac{D}{n+1}+D')\sqrt{L_mC_o}}{\frac{L_m}{R_o}+R_cC_o(\frac{D}{(n+1)^2}+D')} \tag{2.24}$$

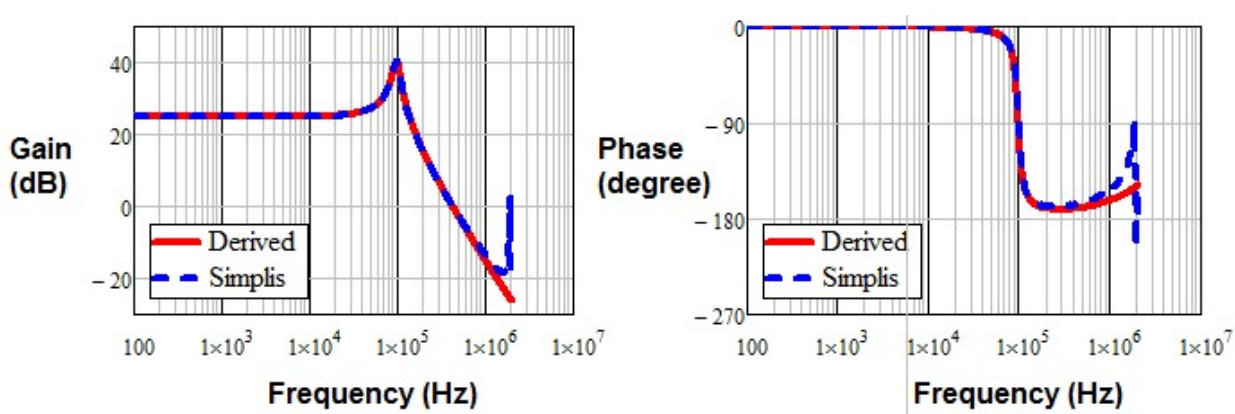


Figure 2.9. Control to output transfer function

Similar to VMC buck converter, the G_{vd} of VMC TI buck converter has a low-frequency LC double pole (ω_o) and a high-frequency ESR zero (ω_z), yet there are still notable differences. For instance, the ω_o varies with different working condition, as demonstrated in Table 2.1 (L_m =

180 nH, n = 1, C_o = 10 μF). Also, chances are that ω_z becomes right-half-plane (RHP) zero and brings instability issue. Fortunately, ω_z is high-frequency zero in lower power application, so it does not have strong impact on the bandwidth of loop gain. The compensator in VMC is ought to be designed according to G_{vd} characteristics.

Table 2.1. LC double (ω_o) location

V_{in}/V_o	$f_o=\omega_o/2\pi$
24 V/12 V	79 kHz
24 V/5 V	98 kHz
48 V/5 V	107 kHz
60 V/3.3 V	112 kHz

Chapter 3

Prototype Design and Implementation

The specifications of SCM TI buck converter prototype is shown in **Error! Reference source not found.**. Devices and gate drivers are commercially available products and coupled inductor is customized design. The first version of prototype is built using silicon MOSFETs to validate operational principle of SCM TI buck converter. Later versions target on efficiency optimization through gallium nitride (GaN) device and revised magnetic design. This chapter is mainly for showing the design and implementation process of the prototypes.

Table 3.1. Prototype specifications

Input voltage *(V_{in})*	24 V to 60 V
Output voltage *(V_o)*	3.3 V to 12 V
Output current *(I_o)*	Up to 3 A
Target switching frequency (f_s) @ 24V-5V conversion, full load condition	2 MHz

3.1 Device and Gate Driver Selection Guideline

The voltage and current rating of Q1 and Q2 are summarized in (2.6)-(2.9). In the case of $n = 1$, the voltage rating of Q2 is almost halved despite of slight increment in Q1 voltage rating. Dropping voltage rating is beneficial since device can own higher figure of merit (FOM) [29]. (3.1) is the formula of Baliga high-frequency figure of merit (BHFFOM), where $R_{on,sp}$ and $C_{in,sp}$ are specific on-resistance and specific input capacitance. From (3.1), high FOM means low $R_{on,sp}*C_{in,sp}$, which leads to low power losses.

$$BHFFOM = \frac{1}{R_{on,sp} C_{in,sp}} \tag{3.1}$$

$R_{on,sp}$ and $C_{in,sp}$ are resistance and capacitance per unit area while die size, the area, can be assigned by semiconductor manufacturer. Large die size typically lowers on-resistance but enlarges parasitic capacitance. Die size plays an important role in the balance between conduction loss and switching loss, which relate to on-resistance and parasitic capacitance respectively.

On-resistance (R_{ds}) creates ohmic power loss, as shown in (3.2), where α and T_j are temperature coefficient and junction temperature. In high step-down conversion, Q2 has larger rms current mostly due to longer conduction time. The rms current of Q1 and Q2 can be calculated by (3.3) and (3.4).

$$P_{Q,cond} = I_{rms\_Q}^2 R_{ds} (1+\alpha(\mathrm{T}_j\text{-}25°\mathrm{C})) \tag{3.2}$$

$$I_{rms\_Q1} = \sqrt{\frac{D}{3}\left(I_r'^2 + \left(I_r' + \Delta I_1\right)^2 + I_r'\left(I_r' + \Delta I_1\right)\right)} \tag{3.3}$$

$$I_{rms\_Q2} = \sqrt{\frac{1-D}{3}\left(I_r^2 + \left(I_r + \Delta I_2\right)^2 + I_r\left(I_r + \Delta I_2\right)\right)} \tag{3.4}$$

On the other hand, parasitic capacitance affects switching loss. MOSFET with larger parasitic capacitance requires more gate charge to turn on the device, so switching time (t_{sw_on}) is prolonged. Figure 3.1 [30] shows the ideal turn-on waveform of MOSFET and the switching time can be roughly estimated by (3.5), where V_{driver}, $V_{plateau}$, R_{driver}, R_g are gate driving voltage, device plateau voltage, gate driver resistance, gate resistor. Q_{gd} is the miller gate charge responsible for plateau voltage and Q_{gs2} is the gate charge from threshold voltage (V_{th}) to $V_{plateau}$. It is clear from (3.5) that larger gate charge requires longer t_{sw_on}. Besides, the switching loss can be estimated by (3.6) and it is proportional to t_{sw_on}. The turn-off process of MOSFET follows the

same trend that larger parasitic capacitance leads to higher switching loss, as shown in (3.7) and (3.8). Fortunately, both switches in SCM TI buck converter feature ZVS turn-on and hence only turn-off losses appear, as shown in (3.9) and (3.10).

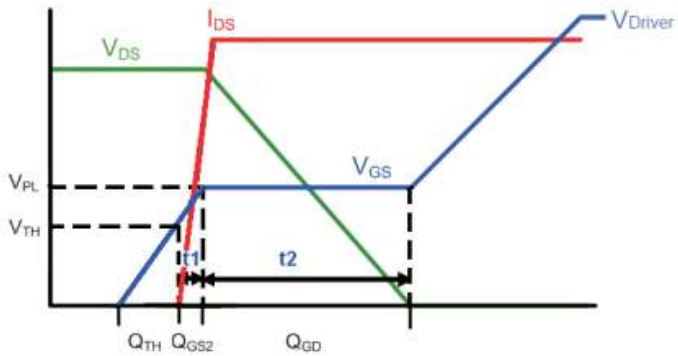


Figure 3.1. Ideal waveforms at device turn-on

$$t_{sw\_on} = \frac{Q_{gs2}}{I_{g1(on)}} + \frac{Q_{gd}}{I_{g2(on)}} = \frac{(Q_{gs2}+Q_{gd})(R_{driver}+R_g)}{V_{driver}-V_{plateau}} \tag{3.5}$$

$$P_{sw\_on} = \frac{1}{2} V_{DS} I_{DS} f_s t_{sw\_on} \tag{3.6}$$

$$t_{sw\_off} = \frac{Q_{gs2}}{I_{g1(off)}} + \frac{Q_{gd}}{I_{g2(off)}} = \frac{(Q_{gs2}+Q_{gd})(R_{driver}+R_g)}{V_{plateau}} \tag{3.7}$$

$$P_{sw\_off} = \frac{1}{2} V_{DS} I_{DS} f_s t_{sw\_off} \tag{3.8}$$

$$P_{sw\_Q1} = \frac{1}{2}\left(V_{in} + nV_o\right)(I_r' + \Delta I_1) t_{sw\_off\_Q1} f_s \tag{3.9}$$

$$P_{sw\_Q2} = \frac{1}{2}\frac{V_{in}+nV_o}{n+1} I_r t_{sw\_off\_Q2} f_s \tag{3.10}$$

On top of (3.6) and (3.8), there are also capacitive turn-on loss and reverse recovery loss in MOSFET drain-source channel when it comes to hard-switching configuration. Capacitive loss represents wasted energy in C_{oss}, as shown in (3.11). Besides, the body diode of silicon MOSFET has terrible reverse recovery problem which adds on additional power loss as shown in

(3.12). Nevertheless, SCM recycles the energy in C_{oss} and turns off the body diode of Q2 at zero current. Consequently, the losses described in (3.11) and (3.12) do not apply to SCM TI buck converter.

$$P_{Coss} = \frac{1}{2} C_{oss} V_{DS}^2 \tag{3.11}$$

$$P_{DRR} = Q_{rr} V_{DS} f_s \tag{3.12}$$

Power loss is also found in gate driving process. In every switching cycle, C_{gs} is charged to V_{driver} and then the energy is released. Also, same amount of energy will be dissipated in gate driving loop (R_{driver}+R_g), so total gate driver loss is described by (3.13), where Q_g is switching gate charge. It is worth mentioning that Q_g becomes smaller in ZVS scenario, because voltage commutation period occurs before device turn-on. As a result, the Miller plateau region as well as the accompanying charge, Q_{gd}, are eliminated from the Q_g [31].

$$P_{gate} = Q_g V_{driver} f_s \tag{3.13}$$

With the device power losses introduced so far, a few design trade-offs can be brought up. First of all, the choice between large (die size) or small device. In SCM TI buck converter, the losses related to R_{ds} are listed in (3.3) and (3.4) and the losses related to parasitic capacitance are shown in (3.9), (3.10) and (3.13). Typically, two kind of losses are supposed to be similar since in this way, total loss can be minimized. However, commercial discrete MOSFETs are barely designed for such low-power application. Even though the chosen devices are almost smallest ones on market, switching-related losses still surpass the conduction loss, as shown in later chapter.

Second, V_{driver} does affects R_{ds} and an example is shown in Figure 3.2 [32]. R_{ds} is reduced when V_{driver} is raised, but an obvious drawback is the augmented gate driver loss. Not

only V_{driver} in (3.13) rises, but the related gate charge Q_g increases as well. Since rms currents are not high in this thesis, there is room to drop V_{driver} to suppress high-frequency gate driver loss. Moreover, the driving voltage of commercial GaN device is currently around 5 V, lower than the V_{driver} of silicon MOSFETs, and provides tremendous advantage in terms of overall efficiency. Aside from V_{driver}, the selection of gate driver should also take driving capability into account. Driving capability is usually in terms of current handling ability. It is better for designer to ensure that I_{g1}, I_{g2} in (3.5) and (3.7) stay below rated pull-up and pull-down current.

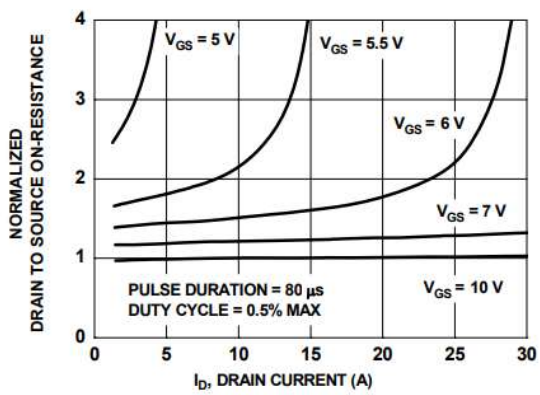


Figure 3.2. Normalized on-resistance versus driving voltage for FDS86141

Finally, when current flows through the body diode of MOSFET, it creates undesired conduction loss. The forward voltage of body diode (V_{sd}) is usually higher than the voltage drop across on-state MOSFET, so unnecessary dead-time should be avoided. The dead-time conduction loss can be calculated by (3.14), where I_{ds} is the average current within dead-time t_{dead}. Although GaN MOSFET does not have body diode, its voltage drop during reverse conduction is even worse than the V_{sd} of silicon MOSFET. Therefore, the dead-time should also be carefully decided.

$$P_{dt} = V_{sd} I_{ds} t_{dead} f_s \tag{3.14}$$

3.2 Coupled Inductor Design Guideline

3.2.1 Magnetic Core

Coupled inductor is crucial to the performance of SCM TI buck converter and this section starts from the magnetic core design.

For MHz-level converter, the core material has to be capable of high frequency operation. The permeability versus frequency curve for chosen P61 material from ACME is shown in Figure 3.3 [33], where μ' and μ'' are initial permeability and amplitude permeability. From Figure 3.3, μ' drops to zero before 5 MHz, which means the core does not work properly above it. In addition, high power density circuit could have thermal issue, so it is also important to ensure the consistency of permeability over temperature range.

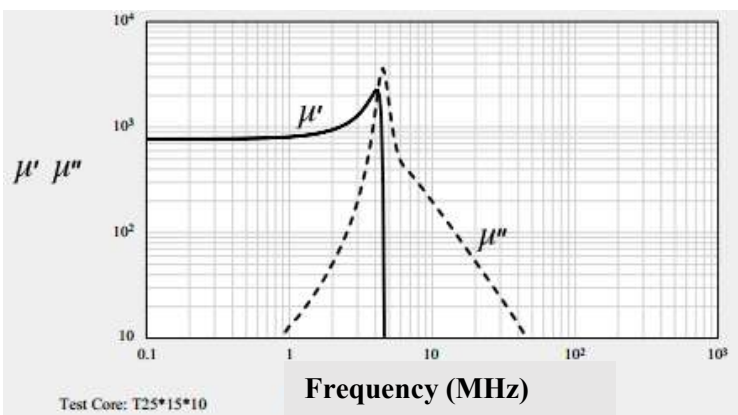


Figure 3.3. Permeability versus frequency for P61 material

A basic property of core material is the B-H curve, as demonstrated in Figure 3.4 [33]. When magnetic flux (B) is too intense, the material tends to lose its permeability, which is known as saturation. Saturation could be hazardous to converter for the sake of over-current. From Figure 3.4, the magnetic flux should be kept below 300 mT and practical design sets even more margin. The magnetic flux can be calculated by (3.15) and thus it reaches maximum at the moment of t_1.

$$B = \frac{I_{Lm} L_m}{N_2 A_e} \tag{3.15}$$

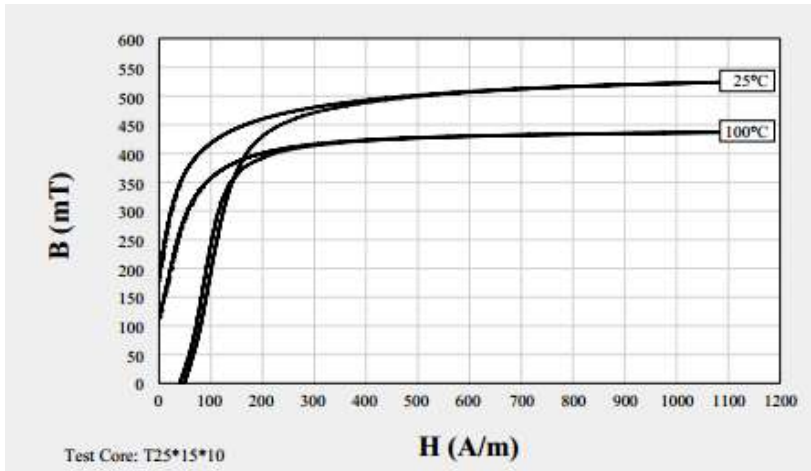


Figure 3.4. B-H curve for P61 material

The target switching frequency (2 MHz) at 24V-5V full-load condition has been stated previously. If n is given, then L_m is decided by (2.22). Furthermore, I_{Lm} is also decided since voltage-second of L_m only relates to V_{in} and V_{out}. Consequently, a design trade-off shows up from (3.15): secondary-side number of turns (N_2) and cross-sectional area (A_e). To keep B low, either more N_2 or wider A_e is needed. An EE core diagram is shown in Figure 3.5 [33] to illustrate how geometric shape affects the trade-off. To broaden A_e, the length (***C*** dimension) should be extended; to accommodate more N_2, window height (***F*** dimension) should be extended. Meanwhile, core size is restricted. In addition, a narrow width of window area (***E-D*** dimension) limits the winding trace but helps increase A_e.

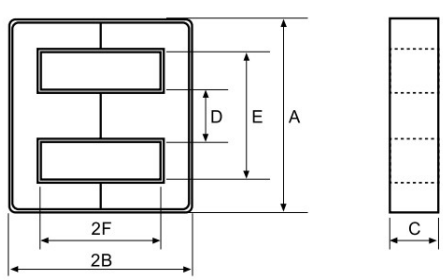


Figure 3.5. EE core dimensions

Since P61 is Manganese-Zinc high-μ material, air gap is utilized. L_m is dominated by the length of air gap (l_g) and proportional to the square of N_2, as shown in (3.16), where μ_o, μ_r, l_e are vacuum permeability, material relative permeability, core effective length. Table 3.2 shows core design with different number of turns yet same L_m (= 188 nH) and ΔB (146 mT @ 24V-5V, f_s = 2MHz). With N_2 increasing, l_g is also increased. Typically, large air gap generates strong fringing effect, which could create additional eddy current loss.

$$L_m = N_2^2 A_e \frac{\mu_o}{l_g + \frac{l_e}{\mu_r}} \approx N_2^2 A_e \frac{\mu_o}{l_g} \tag{3.16}$$

Table 3.2. Core design with different number of turns

N_2	A_e (mm^2)	l_g (mm)
4	2.8	0.3
3	3.7	0.23
2	5.6	0.15
1	11.2	0.08

In TI buck converter, the magnetic flux ripple ($\Delta B_{P\text{-}P}$) can be calculated by (3.17) and the core loss density (P_{CV}) can be estimated from (3.18) provided by the manufacturer, where k_{CV}, k_f and k_b are constant coefficients. SCM TI buck converter mainly utilizes the first quadrant of B-H curve, but the impact of dc magnetic flux on core loss is not considered in this thesis.

$$\Delta B_{p-p} = \frac{V_o(1-D)}{N_2 A_e f_s} \tag{3.17}$$

$$P_{CV} = k_{CV} f^{k_f} \left(\frac{\Delta B_{p-p}}{2}\right)^{k_b} \tag{3.18}$$

3.2.2 PCB Windings

In previous theoretical analysis, coupled inductor is assumed to be perfectly coupled. But in real circuit, leakage inductance exists whenever magnetic flux flows through the air rather than ferrite core, as modeled in Figure 3.6. Leakage inductance deteriorates TI buck converter especially at the moment of t_1. I_{L1} reaches its peak value and then suddenly Q1 turns off. So at t_1, L_{r1} has large current without free-wheeling path and thus resonates with device C_{oss}. Such high-frequency resonance creates noises in the converter and harms the efficiency.

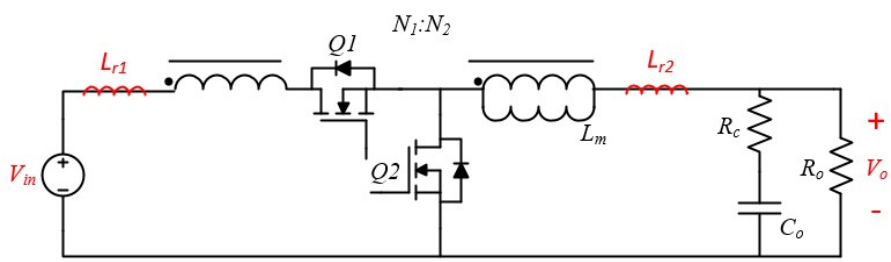


Figure 3.6. Leakage inductance in TI buck converter

To minimize the leakage inductance, the winding strategy has to be carefully designed. High-frequency winding can be realized by litz wire, which reduces skin effect by integrating numerous thin threads. Nevertheless, it is difficult for automatic winding machine to fit such compact design. If bobbin is utilized to aid winding, it will eat up large portion of window area. As a result, litz-wire strategy cannot maintain quality or control the leakage percentage.

On the other hand, PCB winding can be massively reproduced without quality control issue, so it is preferred in our application. The leakage inductance can be reduced by interleaving technique, as illustrated in Figure 3.7. According to simulation in finite element analysis (FEA) software Maxwell, winding pairs in Figure 3.7(a), (b) and (c) have coupling coefficient (k) of 0.967, 0.983 and 0.982. The latter two arrangements both have low leakage inductance; however, in freewheeling stage, proximity effect is reduced by interleaved version 2.

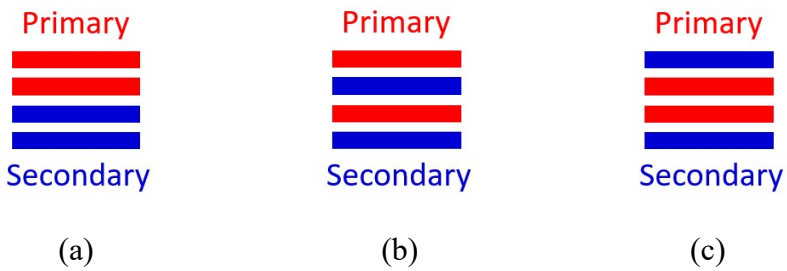


Figure 3.7. Arrangement of PCB windings (2 turns to 2 turns): (a) non-interleaved version, (b) interleaved version 1 and (c) interleaved version 2

Turns ratio n is associated with entire converter performance, from duty cycle, current ripple to efficiency. In this thesis, n is fixed at one mainly because high-n design needs more total number of turns (N_1+N_2), which is hard to squeeze in the small window area. On top of spacing problem, higher number of turns leads to stronger proximity effect [34]. Coupled inductor in TI buck converter has series-aiding configuration, so every turn has identical current direction. Currents in same direction attract each other, creating uneven current distribution and extra conduction loss.

The reason of uneven current distribution also comes from skin effect, which means ac current tends to concentrate within the region between outer surface and a level called the skin depth (δ_s). The skin depth is calculated by (3.19), where σ and f are conductivity and frequency under concern. At 2 MHz, the skin depth of copper is 46 μm, about the thickness of 1.5-oz copper. Therefore, the skin effect is not serious in terms of effective thickness, but it decides the effective width, as shown in Figure 3.8. Since resistance is inversely proportional to the cross-sectional area of current, the relationship between ac resistance (ACR) and frequency can be described in (3.20). Besides, a single-turn PCB trace (1.5-oz thickness, 1-mm width) is simulated in finite element analysis (FEA) software Maxwell. The simulation result is shown in Figure 3.9, which basically matches (3.20). Note that single-turn simulation excludes proximity effect and like (3.20), considers only skin effect.

$$\delta_s = \sqrt{\frac{1}{\pi f \mu_r \mu_o \sigma}} \tag{3.19}$$

$$ACR \propto \frac{1}{\delta_s} \propto \sqrt{f} \tag{3.20}$$

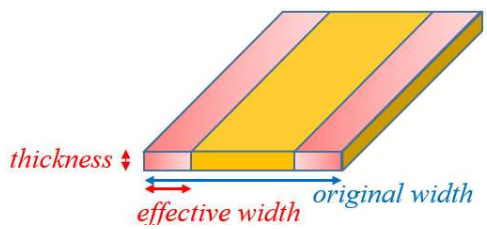


Figure 3.8. Skin effect in PCB trace

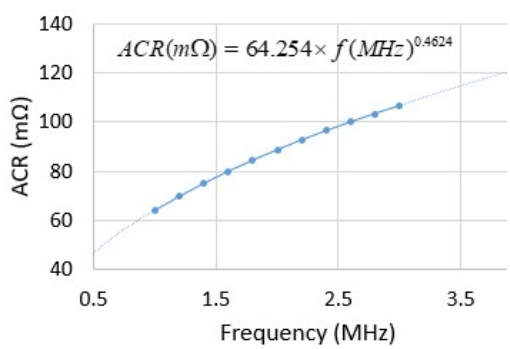
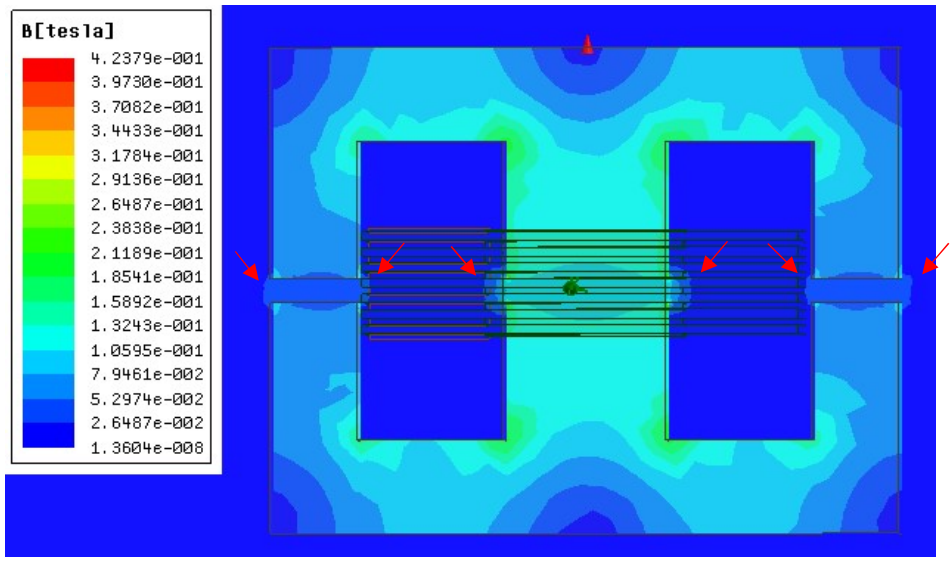
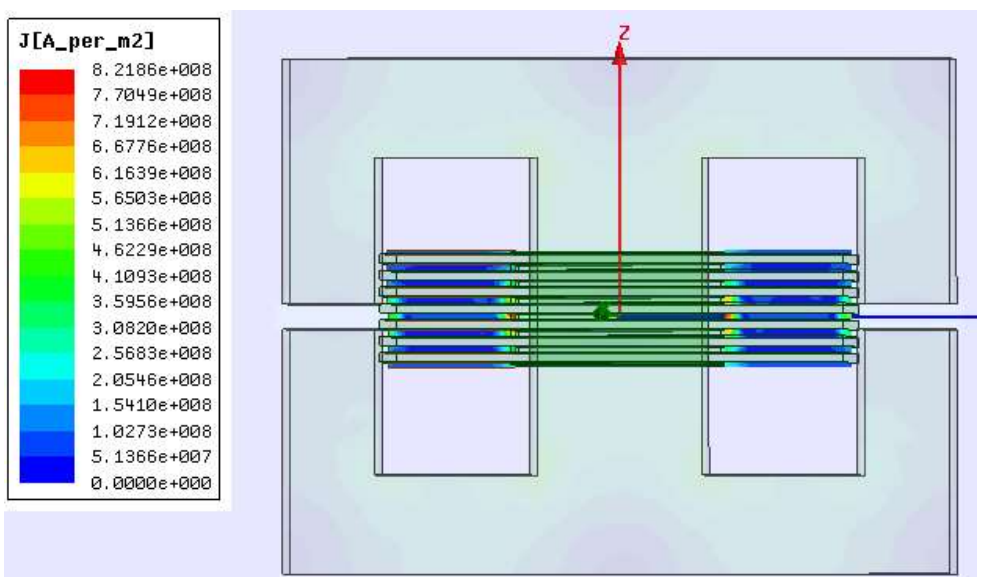


Figure 3.9. Simulated ACR versus frequency for single-turn PCB trace

Another critical concern for winding design is the fringing effect. Fringing effect occurs near the air gap where magnetic flux scatters due to low permeability of atmosphere. Scattered flux could interact with windings and induce eddy current [35]-[36]. The situation is even worse in compact magnetic design because the room for dodging magnetic flux is limited. Figure 3.10 is a simulation example in Maxwell demonstrating fringing effect. Figure 3.10(a) shows magnetic flux distribution and red arrows point at the positions of fringing effect. Figure 3.10(b) shows current density distribution, which is high around the air gap. Such eddy current increases winding ACR and severe copper loss. Therefore, air gap should be kept away from the windings or be the distributed type [36].



(a)



(b)

Figure 3.10. Fringing effect: (a) magnetic flux distribution and (b) current density distribution

Figure 3.11 shows the concept of separating dc and ac current since they see different winding resistance. For simplicity, the frequency of ac current is assumed to be f_s, despite that ac current in Figure 3.11 has components of even higher frequency according to Fourier analysis. In

summary, the copper loss can be estimated by (3.21), where rms current components are calculated through (3.22)-(3.27).

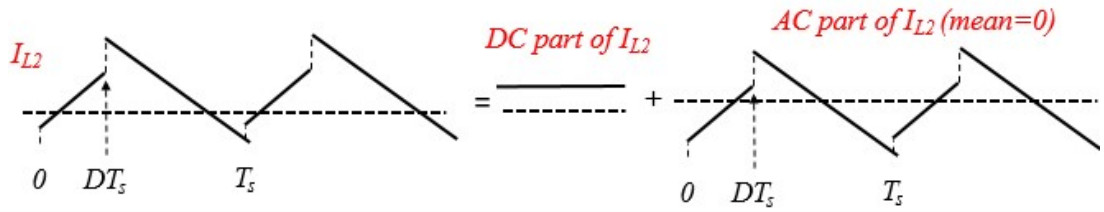


Figure 3.11. Separation of dc and ac current

$$P_{Cu} = I_{pri\_DC}{}^2 DCR_{pri} + I_{\sec\_DC}{}^2 DCR_{\sec} + I_{pri\_AC}{}^2 ACR_{pri} + I_{\sec\_AC}{}^2 ACR_{\sec} \tag{3.21}$$

$$I_{pri\_DC} = I_{in} = \frac{V_o I_o}{V_{in}} \tag{3.22}$$

$$I_{\sec\_DC} = I_o \tag{3.23}$$

$$I_{pri\_ac} = \sqrt{\frac{D}{3}\left((I_r' - I_{in})^2 + \left(I_r' + \Delta I_1 - I_{in}\right)^2 + (I_r' - I_{in})\left(I_r' + \Delta I_1 - I_{in}\right)\right)} \tag{3.24}$$

$$I_{\sec\_ac} = \sqrt{I_{\sec\_ac\_D}{}^2 + I_{\sec\_ac\_D'}{}^2} \tag{3.25}$$

$$I_{\sec\_ac\_D} = \sqrt{\frac{D}{3}\left((I_r' - I_o)^2 + \left(I_r' + \Delta I_1 - I_o\right)^2 + (I_r' - I_o)\left(I_r' + \Delta I_1 - I_o\right)\right)} \tag{3.26}$$

$$I_{\sec\_ac\_D'} = \sqrt{\frac{1-D}{3}\left((I_r - I_o)^2 + \left(I_r + \Delta I_2 - I_o\right)^2 + (I_r - I_o)\left(I_r + \Delta I_2 - I_o\right)\right)} \tag{3.27}$$

3.3 Power Stage Design Summary and Implementation

Device selection of SCM TI buck converter prototype is shown in Table 3.3 along with device parameters. Two sets of devices are selected: silicon version and GaN version. Silicon version consists of two discrete MOSFETs: Q2 has smaller R_{ds} since it handles larger current. Q1 has smaller parasitic capacitance for reducing hard turn-off loss. On the other hand, GaN version is realized by a half-bridge MOSFET module. With devices integrated together and ball grid array

(BGA) package, loop parasitic inductance can be reduced [38]. Otherwise, parasitic inductance could generate high-frequency noises or even slow down the switching [39]. The voltage rating of Q2 in EPC2105 is not optimized since commercial half-bridge module is usually designed for buck converter. Also note that silicon device is driven at 8 V so involved Q_g is higher than the values in Table 3.3. Consequently, GaN devices are beneficial for saving gate driver loss.

Table 3.3. Device selection of prototype

	FDS86141	CSD18504Q5A	EPC2105	
Description	Silicon MOSFET	Silicon MOSFET	Asymmetrical half-bridge GaN MOSFET	
Position	Q1	Q2	Q1	Q2
Device rating (voltage and continuous drain current)	100 V, 7 A	40 V, 50 A	80 V, 9.5 A	80 V, 38 A
R_{ds} (@25°C)	21 mΩ	6 mΩ	10 mΩ	2.3 mΩ
C_{oss} (@V_{ds}=0.5* voltage rating)	186 pF	310 pF	200 pF	800 pF
Q_g (@V_{gs}=5 V)	6.7 nC	8.2 nC	2.5 nC	10 nC
V_{sd} (@V_{gs}=0 V)	0.8 V (@I_{sd}=7 A)	0.8 V (@I_{sd}=17 A)	~2V (@I_{sd}=7 A)	~2V (@I_{sd}=17 A)

TI buck converter has two versions of coupled inductor design: coupled inductor version I (CI-v1) and coupled inductor version II (CI-v2). Efficiency difference with CI-v1 and CI-v2 is presented and discussed later. The dimensions of magnetic cores are summarized in Table 3.4. CI-v1 uses EE core structure, as shown in Figure 3.5, and CI-v2 uses EI core structure, as shown in Figure 3.12. In both versions, the core material is P61 from ACME electronics.

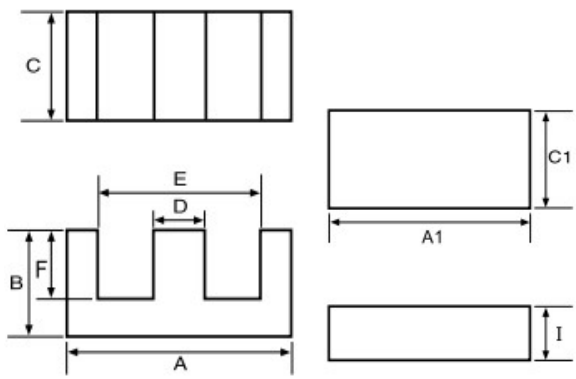


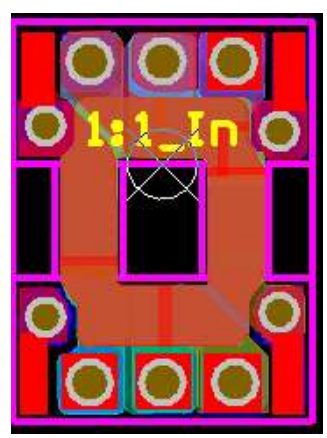
Figure 3.12. EI core dimensions

Table 3.4. Magnetic core dimensions

(unit: mm)	type	*A*	*B*	*C*	*D*	*E*	*F*	*A1*	*C1*	*I*
CIv-I	EE	5.25	2.66	1.95	1.35	3.80	1.98	-	-	-
CIv-II	EI	5.25	2.66	3.90	1.35	3.80	1.98	5.25	3.90	0.68

PCB windings are designed according to magnetic core shape, as shown in Figure 3.13 and Figure 3.14, where red and blue arrow indicate primary and secondary side.

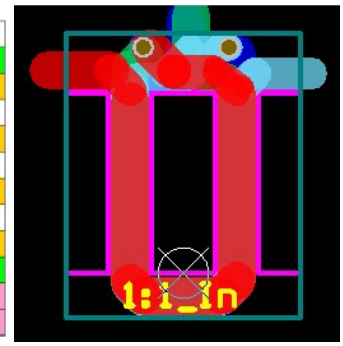
	Layer		Type	Thickness (mil)	
	Top side solder mask			0.70	mils
P →	L1	TOP	copper+plating	1.40	mils
			dielectric layer	3.00	mils
S ←	L2		copper	2.10	mils
			dielectric layer	3.00	mils
P →	L3		copper	2.10	mils
			dielectric layer	3.00	mils
S ←	L4		copper	2.10	mils
			dielectric layer	3.00	mils
P →	L5		copper	2.10	mils
			dielectric layer	3.00	mils
S ←	L6		copper	2.10	mils
			dielectric layer	3.00	mils
P →	L7		copper	2.10	mils
			dielectric layer	3.00	mils
S ←	L8	Bottom	copper+plating	1.40	mils
	Bottom side solder mask			0.70	mils
	TOTAL			37.80	mils
				0.96	mm



(a) (b)

Figure 3.13. PCB winding for CI-v1: (a) PCB stack-up and (b) PCB layout

	Layer	Type	Thickness (mil)		
		Top side solder mask		0.70	mils
P →	L1	TOP	copper+plating	2.10	mils
			dielectric layer	5.00	mils
S ←	L2		copper	2.10	mils
			dielectric layer	5.00	mils
S ←	L3		copper	2.10	mils
			dielectric layer	5.00	mils
P →	L4	Bottom	copper+plating	2.10	mils
		Top side solder mask		0.70	mils
	TOTAL			24.80	mils
				0.63	mm



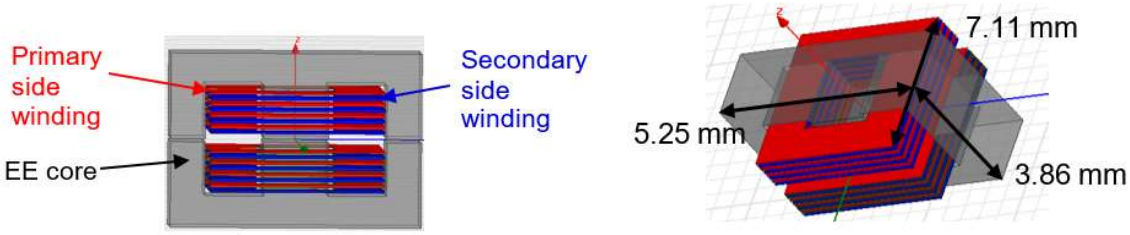
(a) (b)

Figure 3.14. PCB winding for CI-v2: (a) PCB stack-up and (b) PCB layout

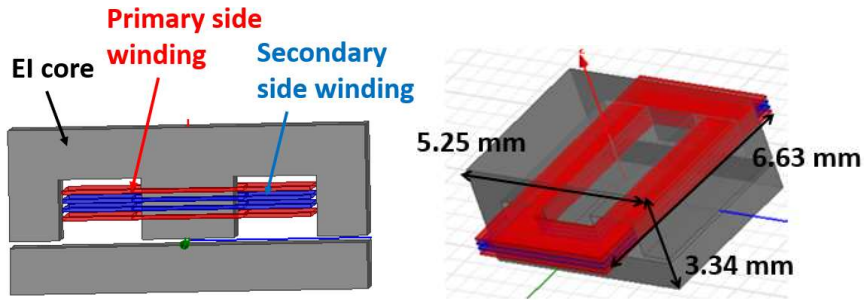
The designs of coupled inductor are summarized in Table 3.5. CI-v1 and CI-v2 have identical turns ratio and magnetizing inductance. However, CI-v2 has less number of turns in order to reduce proximity effect. As a result, CI-v2 requires wider A_e yet its total volume is shrank due to shortened height. The shorter l_g of CI-v2 helps alleviate fringing effect. Moreover, CI-v2 utilizes EI core so air gaps are located at the corners. In this way, the eddy current loss from fringing effect can be reduced as well. In conclusion, CI-v2 should outperform CI-v1 because of lower ACR and lower copper loss. The 3D model of CI-v1 and CI-v2 are shown in Figure 3.15.

Table 3.5. Summary of coupled inductor design

	n	L_m	PCB windings	Core shape	A_e	l_g	Volume
CI-v1	1	194 nH	4 turns to 4 turns, 2 pieces in parallel	EE	2.8 mm^2	0.3 mm	144 mm^3
CI-v2			2 turns to 2 turns, 1 piece	EI	5.6 mm^2	0.15 mm	116 mm^3



(a)



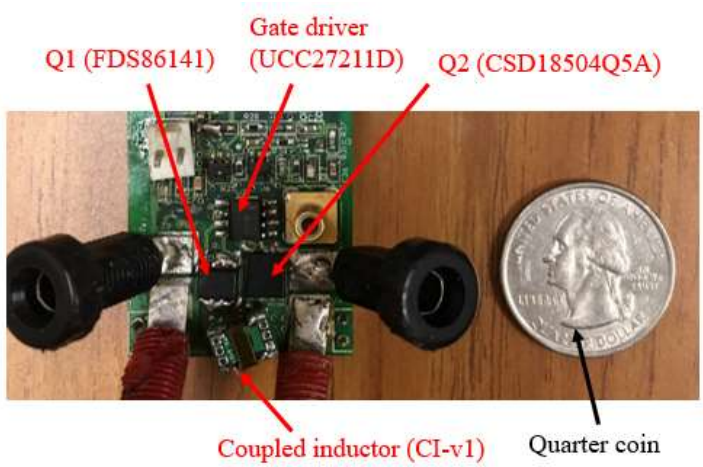
(b)

Figure 3.15. 3D model of coupled inductor: (a) CI-v1 and (b) CI-v2

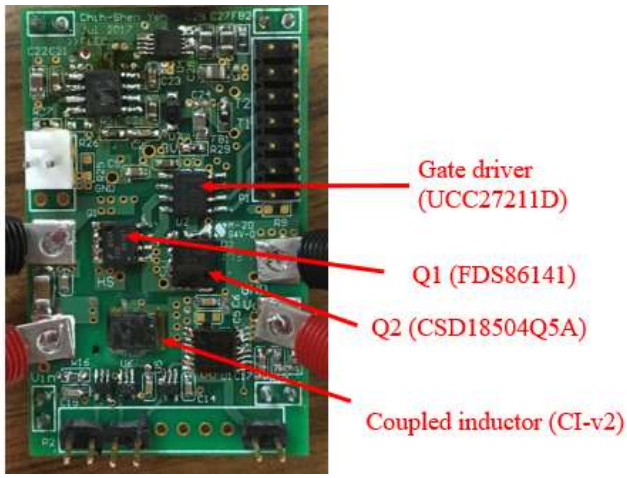
Finally, a few hardware prototypes are assembled, as shown in Table 3.6 and Figure 3.16.

Table 3.6. Summary of hardware prototypes

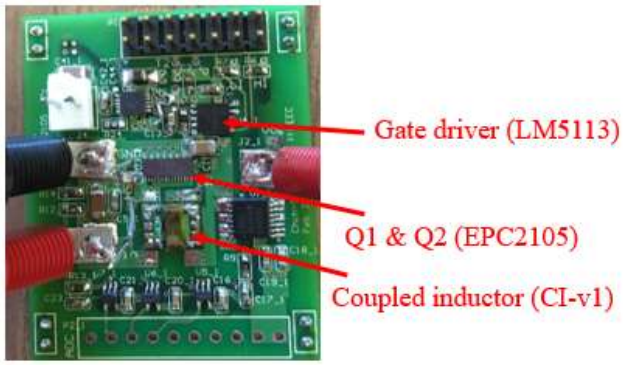
Q_1	FDS86141	EPC2105
Q_2	CSD18504Q5A	
Gate driver	UCC27211	LM5113
C_o	10 μF	
L_m	194 nH	
f_s	2~2.9 MHz	
N_1:N_2	1:1	



(a)



(b)



(c)

Figure 3.16. Photograph of hardware prototype: (a) with Silicon devices & CI-v1, (b) with Silicon devices & CI-v2, (c) with GaN devices & CI-v1

3.4 Implementation of Feedback Control System

PWM signals for hardware prototypes are generated by digital signal processor (DSP) TMS320F28377D. Voltage regulation is executed by duty cycle control with 1.2 MHz of output voltage ADC sampling rate. The calculation of duty cycle is done within one ADC sampling rate through control law accelerator (CLA), a 32-bit floating point math processor of the DSP, and then updating occurs in next cycle. The block diagram of voltage loop is shown in Figure 3.17, where *LPF1*, *LPF2*, *ZOH*, *K*, Z^{-1} are 2.3-MHz analog low-pass-filter, 15.4 MHz analog low-pass-filter,

zero-order-hold effect of ADC sampling, digital controller, delay effect from duty cycle updating [40]. *ZOH* and Z^{-1} have tremendous effect on the prototypes and their s-domain expression can be found in (3.28) and (3.29). In specific, *ZOH* and Z^{-1} cause phase delay and hinder the possibility of high bandwidth. Figure 3.18 shows the bode plot of function $ZOH*Z^{-1}$. Setting bandwidth to be around 100 kHz is not a smart choice either, because the LC double pole in power stage (as shown in Figure 2.9) has gain peak, which could create undesired second crossover. When second crossover appears, the real bandwidth rises and possibly makes the system unstable. Hence, the bandwidth of voltage loop is at most tens of kHz, below LC double pole. In this scenario, simple PI controller can serve the need. If designer wants to push to a higher bandwidth, analog controller should be implemented to avoid digital delay issue.

$$ZOH(s) = \frac{1 - e^{-sT_{sample}}}{sT_{sample}} \tag{3.28}$$

$$Z^{-1}(s) = e^{-sT_{sample}} \tag{3.29}$$

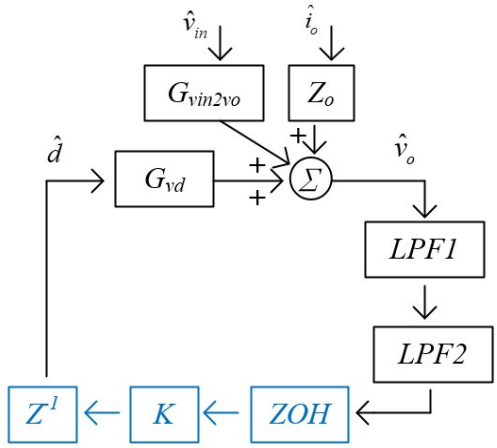


Figure 3.17. Block diagram of voltage loop

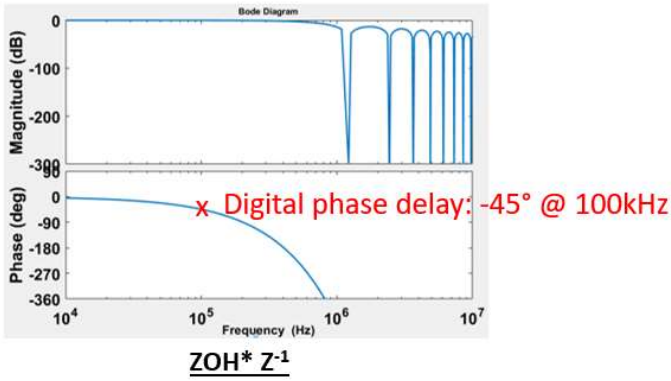


Figure 3.18. The effect of digital delay

Aside from duty cycle, switching frequency is also variable but with updating rate of 3 Hz. Variable f_s is only for efficiency optimization so fast updating is unnecessary. V_o, V_{in}, I_o are sensed and averaged by 32 sampling points. Switching frequency is calculated by (2.22).

Chapter 4

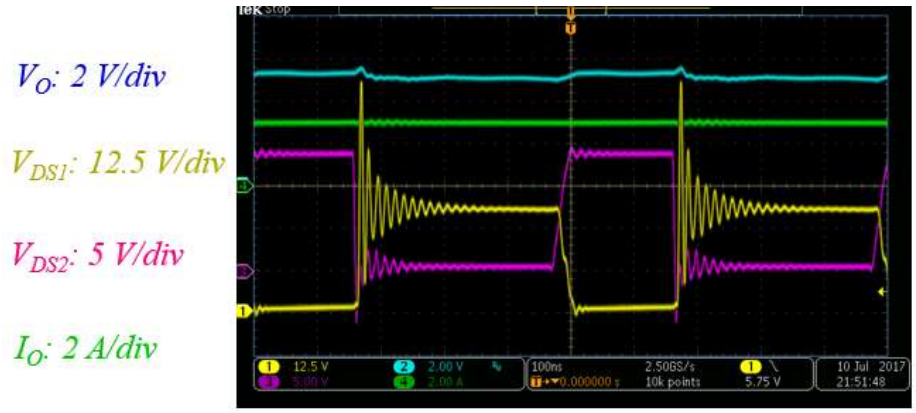
Experimental Results and Loss Analysis

4.1 Converter Operations Verification

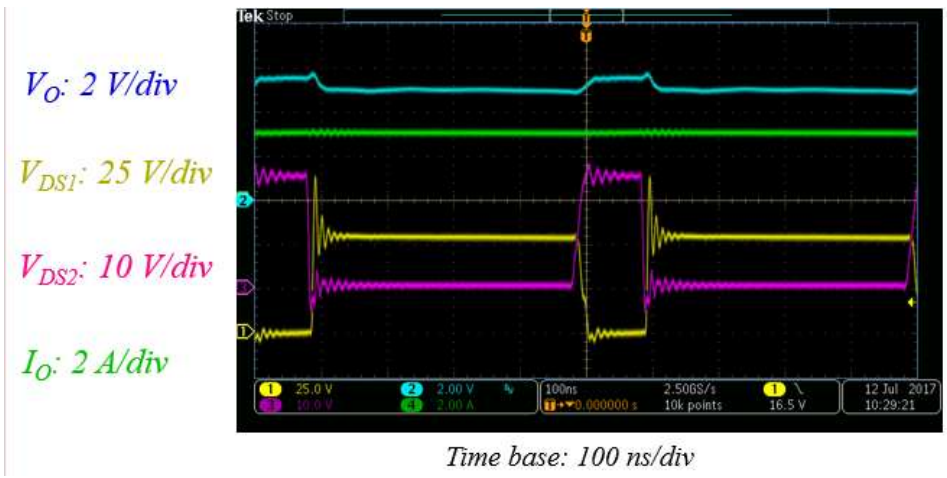
In experiments, power stage input voltage (V_{in}) comes from a variable dc power supply. The converter output is connected to a dc electronic load. Note that gate driver and sensing circuit are supplied by an extra dc power supply.

Figure 4.1 shows steady-state waveforms of SCM TI buck converter prototype with GaN device and CI-v1. In both Figure 4.1 (a) and (b), f_s is 2 MHz and I_o is 3 A. The main purpose of Figure 4.1 is to validate duty cycle and component stress formula. Under 24 V-5 V conversion, duty cycle, Q1 voltage stress, Q2 voltage stress are 34.4%, 29 V, 14.5 V; under 48 V-5 V conversion, duty cycle, Q1 voltage stress, Q2 voltage stress are 18.9%, 53 V, 26.5 V, as validated in Figure 4.1. Note that aforementioned voltage stresses in this paragraph indicate the steady-state stress (after ringing ceases).

The real voltage stress has to take voltage spike into account. In Figure 4.1, voltage spike appears in the waveform of V_{ds1} and the reason can be attributed to the leakage inductance L_{r1}. Before Q1 turns-off, magnetizing current I_{Lm} reaches its peak. Later, the hard turn-off process of Q1 turns the energy in L_{r1} into undesired ringing between device C_{oss} and L_{r1}. On the other hand, voltage commutation after Q2 turn-off is calmer since the current in L_m is not large. But consequently, dead-time needs to be longer.



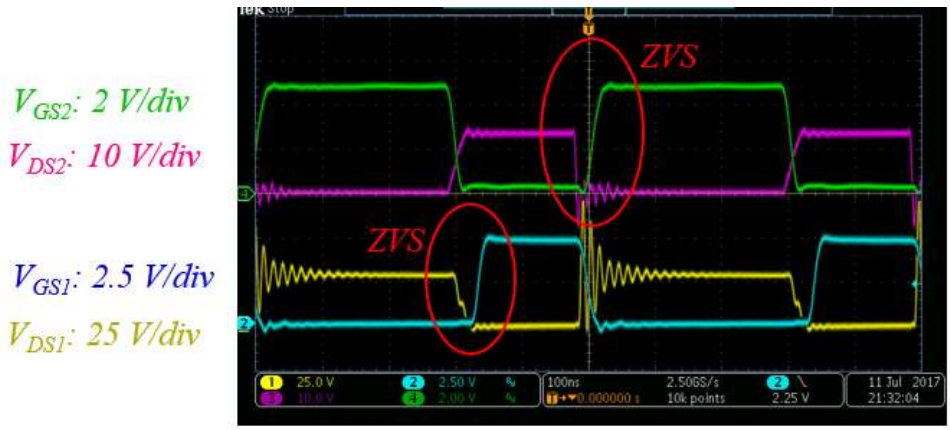
(a)



(b)

Figure 4.1. Steady-state waveforms of SCM TI buck converter: (a) 24 V-5 V conversion and (b) 48 V-5 V conversion

The ZVS waveforms of SCM TI buck converter are shown in Figure 4.2. L_m is designed to obtain Q1 ZVS at following conditions: 24 V-5 V conversion, full load, f_s of 2 MHz. According to Figure 2.8(a), ZVS of Q1 at 48 V-5 V, full load condition can be obtained by higher f_s. Therefore, the converter achieves the ZVS with f_s of 2 MHz in Figure 4.2(b), since I_r is higher than the requirement. For both switches, V_{ds} drops to zero before V_{gs} goes beyond device threshold voltage, so turn-on losses are eliminated.



Time base: 100 ns/div

(a)

Time base: 100 ns/div

(b)

Figure 4.2. ZVS waveforms of SCM TI buck converter at full load: (a) 24 V-5 V conversion and (b) 48 V-5 V conversion

4.2 Efficiency Comparison

The efficiency of the converter is measured by multimeters. Power stage efficiency is defined by (4.1), and the overall efficiency includes the auxiliary power loss (power losses in gate driver, sensing circuit and auxiliary power supply), as shown in (4.2). V_{aux} and I_{aux} are voltage and current of extra dc power supply. Only the power consumption of DSP is excluded from efficiency measurement, because it can be replaced with an analog controller in the product level.

$$\eta_{pwr} = \frac{V_o I_o}{V_{in} I_{in}} \tag{4.1}$$

$$\eta_{tot} = \frac{V_o I_o}{V_{in} I_{in} + V_{aux} I_{aux}} \tag{4.2}$$

The switching frequency has profound impact on the efficiency, from switching loss, core loss to ACR of windings. In some cases, SCM TI buck converter operates with fixed switching frequency just for performance comparison.

4.2.1 Comparison of Coupled Inductor Design

First, the prototypes in Figure 3.16(a) and (b) are compared. Both prototype use silicon device and the only difference is in coupled inductor design. As analyzed in the previous chapter, CI-v2 has smaller impact from proximity and fringing effects, so the efficiency is better, as verified in Figure 4.3. Figure 4.3 is the power stage efficiency under 24 V-5 V conversion and fixed f_s at 2 MHz. The efficiency is improved by 1.6% at full load condition. For fixed f_s control, the current and magnetic flux ripple remain the same throughout entire load range. Therefore, the efficiency improvement is more obvious under light-load condition.

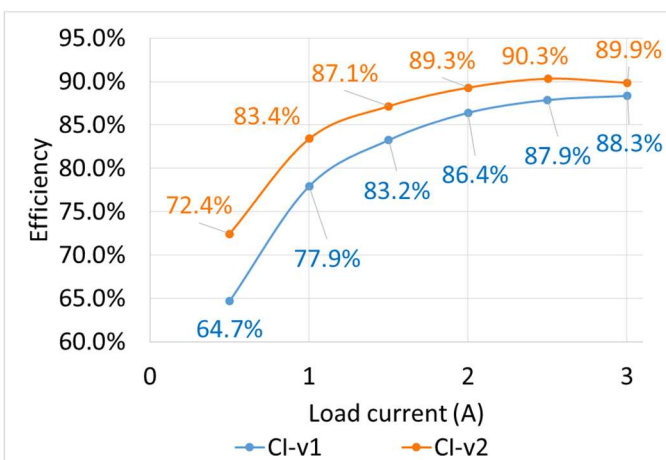
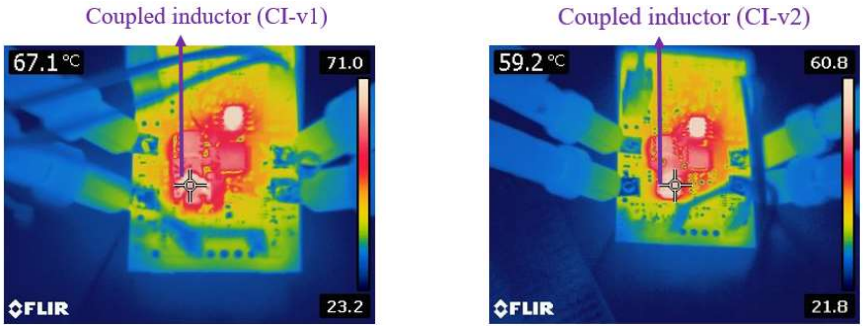


Figure 4.3. Power stage efficiency comparison (CI-v1 versus CI-v2, fixed f_s)

The superior performance of CI-v2 is also verified by thermal image, as shown in Figure 4.4 under no-load condition. Despite of smaller contact area with atmosphere, CI-v2 has temperature almost 8°C lower than CI-v1.



(a) (b)

Figure 4.4. Thermal image under no-load condition: (a) with CI-v1 and (b) with CI-v2

After applying variable frequency control by (2.22), the power stage efficiency becomes Figure 4.5. CI-v2 still has better performance.

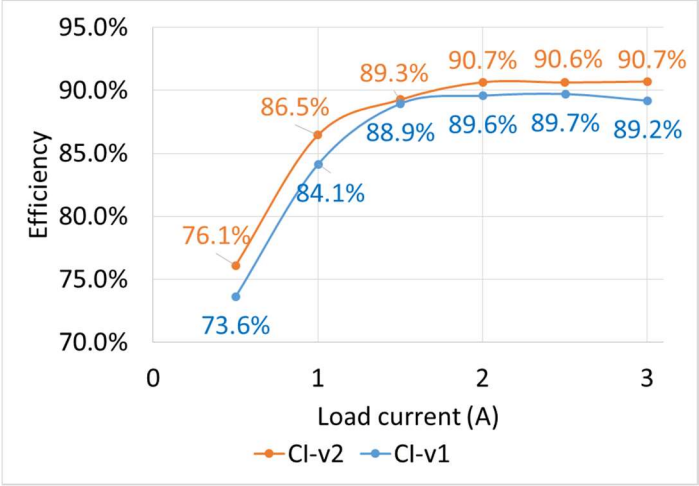


Figure 4.5. Power stage efficiency comparison (CI-v1 versus CI-v2, variable f_s)

4.2.2 Comparison of Silicon and GaN Device

The prototypes in Figure 3.16(a) and (c) have same coupled inductor CI-v1 but different devices. Figure 4.6 shows the power stage efficiency of the prototypes under fixed f_s at 2 MHz. In general, efficiency differs by less than 2% between two prototypes.

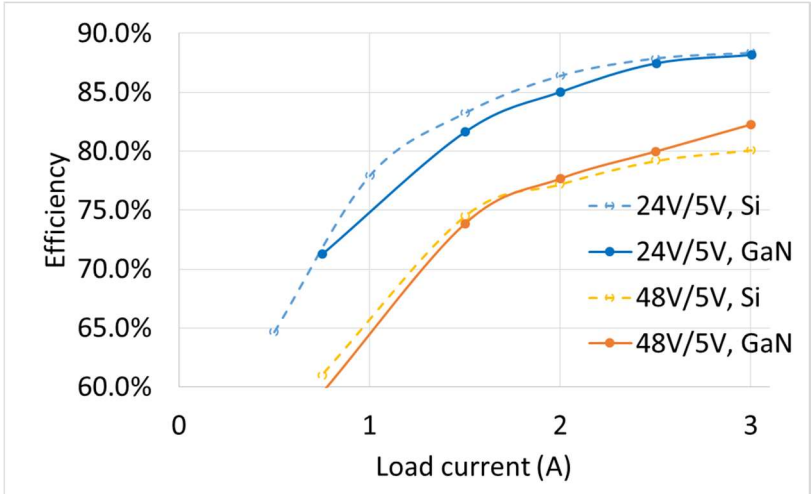


Figure 4.6. Power stage efficiency comparison (silicon device versus GaN device, fixed f_s)

Nevertheless, silicon devices are driven at 8 V and the auxiliary power loss is 0.465 W at 2 MHz. On the other hand, GaN devices are driven at 5 V and the auxiliary power loss is mere 0.061 W at 2 MHz. The difference is caused by gate charge, V_{driver} and quiescent loss of gate driver. Also, due to ZVS feature, auxiliary power loss is basically independent of load current. After auxiliary power loss is considered, the overall efficiency is plotted in Figure 4.7. The prototype using GaN devices outperforms the other.

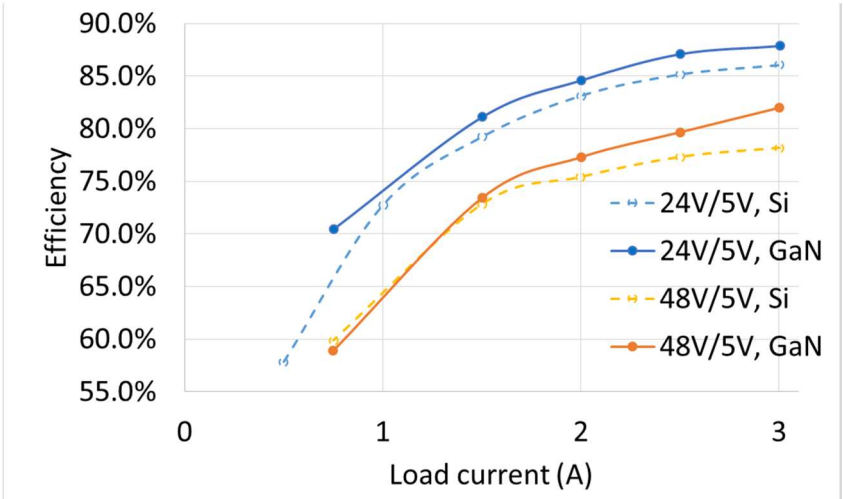


Figure 4.7. Overall efficiency comparison (silicon device versus GaN device, fixed f_s)

4.2.3 Efficiency with Variable Switching Frequency

The variable switching frequency scheme minimizes current ripple and magnetic flux ripple without losing ZVS feature. At full load condition, the optimized f_s is designed at 2 MHz. The optimized f_s increases as load current decreases. Under 24 V-5 V conversion, the power stage efficiency with and without switching frequency variation are compared in Figure 4.8. Figure 4.8 is tested with the prototype using silicon device and CI-v1. It is verified from Figure 4.8 that variable switching frequency scheme improves light-load efficiency.

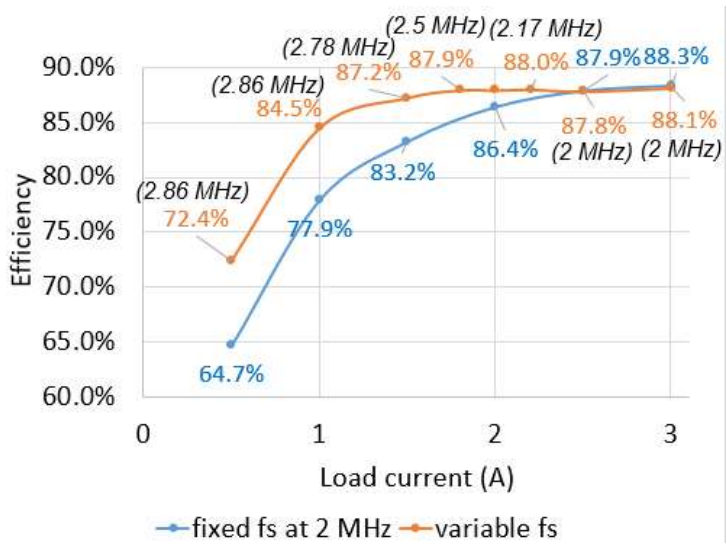


Figure 4.8. Power stage efficiency comparison (fixed f_s versus variable f_s)

4.3 Loss Breakdown

Power losses of SCM TI buck converter are introduced in this thesis and summarized in Table 4.1 along with their estimating formula. Loss breakdown of the prototype using silicon device and CI-v1 is shown in Figure 4.9. The loss breakdown is based on full load condition and f_s of 2 MHz.

Table 4.1. Summary of power stage component losses

MOSFET Conduction Loss ($P_{Q,cond}$)	$P_{Q,cond} = I_{rms\_Q}^2 R_{ds}(1+\alpha(T_j\text{-}25°C))$ (3.2)
MOSFET Switching Loss (P_{sw_off})	$P_{sw\_off} = \frac{1}{2} V_{DS} I_{DS} f_s t_{sw\_off}$ (3.8)
Dead-Time Body Diode Conduction Loss (P_{dt})	$P_{dt} = V_{sd} I_{ds} t_{dead} f_s$ (3.14)
Gate Driver Loss (P_{gate})	$P_{gate} = Q_g V_{driver} f_s$ (3.13)
Copper Loss (P_{Cu})	$P_{Cu} = I_{pri\_DC}{}^2 DCR_{pri} + I_{\sec\_DC}{}^2 DCR_{\sec} + I_{pri\_AC}{}^2 ACR_{pri} + I_{\sec\_AC}{}^2 ACR_{\sec}$ (3.21)
Core Loss (P_{Fe})	$P_{CV} = k_{CV} f^{k_f} (\frac{\Delta B_{p-p}}{2})^{k_b}$ (3.18) $P_{Fe} = P_{CV} \times (core\ volume)$

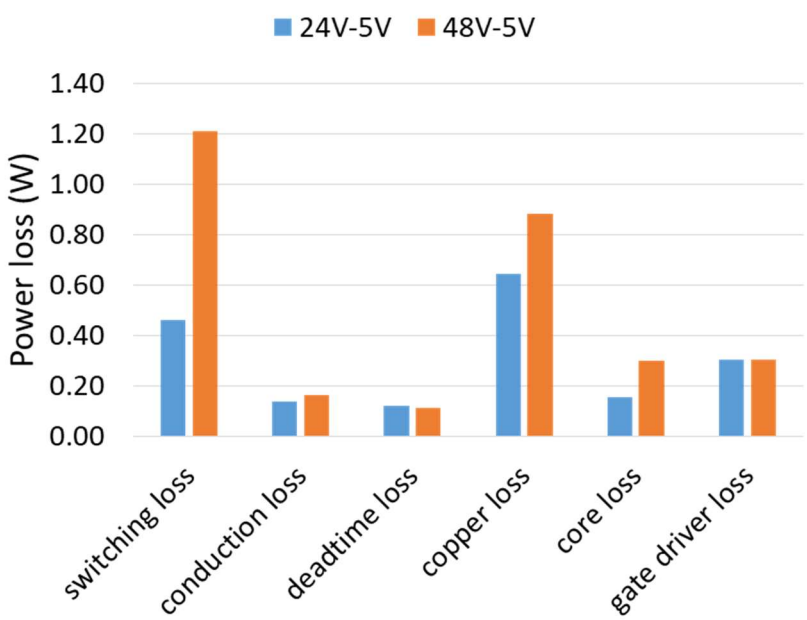


Figure 4.9. Loss breakdown of SCM TI buck converter

The design of the prototype can be examined by Figure 4.9. First, switching loss is larger than conduction loss because it is difficult to find smaller devices on the commercial market. The switching loss mainly comes from the turn-off loss of Q1, being proportional to the V_{ds} after turn-off. Therefore, the switching loss is more than doubled under 48 V-5 V conversion.

Plenty of power losses are generated by coupled inductor. Due to size restriction, cross-sectional areas for both current and magnetic flux are not enough. The design considerations for high-frequency magnetic component have been discussed in this thesis. Modifying the coupled inductor is significant since copper loss is dominant under 24 V-5 V conversion.

Finally, gate driver loss is also noticeable. Nevertheless, it can be greatly reduced if GaN devices and lower V_{drive} are applied.

Chapter 5

Conclusion and Future Work

5.1 Conclusions

It is proposed in this thesis to operate TI buck converter under SCM. Moreover, detailed ZVS conditions of Q1 have been derived for delicate efficiency optimizing scheme. The potential of TI buck converter, as a candidate of general-purpose step-down converter, has been explored. The thesis work includes the derivation of theoretical basis, converter components design, hardware implementation and experimental verification.

TI buck converter is able to operate in entire step-down range with duty-cycle extension, which is preferred in high-step down conversion. Besides, with the aid of SCM, turn-on losses can be eliminated and the switching frequency can be pushed to MHz-level, which helps shrinking the size. Consequently, the design targets of general-purpose step-down converter can be satisfied: wide voltage conversion range, high power density and high efficiency.

A few prototypes are built to verify the design concepts. GaN devices are verified to have lower gate driver loss. The importance of avoiding proximity and fringing effects is demonstrated by comparing CI-v1 and CI-v2. The proposed method realizes SCM by indirect switching frequency variation from 2 MHz to 2.9 MHz and is confirmed to improve light-load efficiency. The peak power-stage efficiency of 15-W prototype is 90.7% at 24 V-5 V conversion and at least 82.3% at 48 V-5 V conversion. The dimensions of coupled inductor are down to 5.25 mm * 6.63 mm * 3.34 mm, which is smaller than most of the commercial products.

5.2 Future Work

GaN devices, modified coupled inductor and variable switching frequency scheme are helpful to converter efficiency, so in the future, all beneficial options should be implemented on a single prototype to gain highest efficiency.

As mentioned in the thesis, the main drawback of SCM TI buck converter comes from the leakage inductance. Moreover, other parasitic inductance, like common source inductance in gate driving loop, also creates additional losses or driving difficulty [30]. The parasitic issue could be alleviated when the converter is implemented on IC-level, which is usual for general-purpose step-down converter. Nevertheless, DSP does not fit in the compact package. As a result, controller will eventually be composed of analog circuits and the design of the analog controller has to be studied.

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