CHAPTER I

INTRODUCTION

Power electronics modules are traditionally custom-designed and require a labor-intensive manufacturing process. The resulting products are usually characterized by problems in quality, reliability, long design cycles, and high cost. Recent research results concerning components and processing within the field of power electronics have not yielded the overall improvement needed for the next generation of power electronics[1,2]. In recent years, an integrated systems approach to standardizing power electronics components and packaging techniques in the form of power electronics building blocks has emerged as a new concept in the area of power electronics[3]. Power electronics building blocks are envisioned as integrated power modules consisting of power semiconductor devices, power integrated circuits, sensors and protection circuits for a wide range of applications, such as inverters for motor drives and converters for power processing equipment. As a result, it is quite evident that packaging of integrated power modules is a central driver in the future of power electronics technology. This research is focused on designing and processing of an innovative three-dimensional packaging architecture for power electronics modules with soldered device interconnections and subsequent characterization of its critical interfaces.

1.1 MOTIVATION FOR 3-DIMENSIONAL PACKAGING OF POWER MODULES

Circuits assembly and packaging technologies for power electronics have not kept pace with those of low-power electronics, like the packaging of integrated circuits (ICs). From an electrical design point of view, traditional power modules are normally quite simple; however, these modules are often extremely difficult to fabricate due to high voltages and large currents, as well as thermal management considerations associated with the high power modules. Inside the state-of-the-art power modules, interconnection of power devices is accomplished with wire bonds (as shown in Figure 1.1.1), which are prone to noise, parasitic oscillations, fatigue and eventual failure.

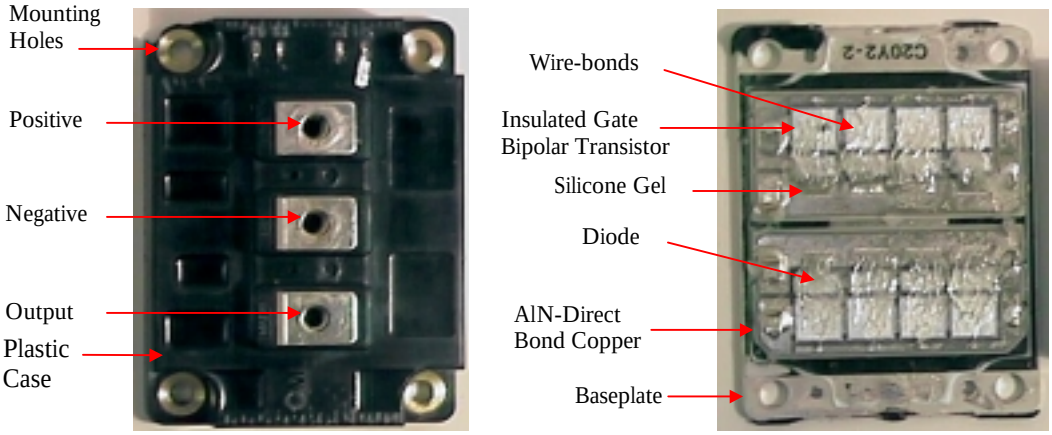

Figure 1.1.1. Outside and inside of a commercial wire-bond module[5]

As a result, the lifetime of commercially available, state-of-the-art wire-bonded plastic power modules is limited only to a few years. Some of the more specific reliability problems associated with the wire-bond technology are listed below[4,5].

- The proximity effect resulting from bonding wires coupling affects the current distribution among the Insulated Gate Bipolar Transistor (IGBT) cells within one chip as well as among the paralleled chips. This imbalance will unevenly load the paralleled IGBTs with different fatigue mechanism, even though they are designed for identical operations.
- Magnetic field induced by the close-coupled bonding wires causes the problem of the device stress and bonding wire fatigue. The lateral mechanical force has a tendency to peel the aluminum coating off the silicon chip. In most cases, the IGBT chip surface tends to crack or the bonding wire opens after power cycling test and thermal cycling.
- Commercially available, state-of-the-art wire-bond module has large parasitic inductance associated mainly with the packaging of terminal leads, which is related to the planar packaging techniques. Since the bottom conductor pads have to accommodate both wire-bonds and terminal leads carrying a high current density, they occupy a large area of the module substrate (non-silicon area) contributing to parasitic inductance. As more IGBTs are paralleled, the inductance of the conductor pads becomes more dominant.

Several new technologies are under development by the module manufacturers to replace wirebonds[6,7]. New technologies that are under development to eliminate wire bonds typically employ spin-coating or tape-casting for laying down dielectric, dry or wet etching for opening up the contact pads and thin film deposition or plating for interconnecting devices. Other available techniques for device interconnections include gold stud-bumps and pressure contact assembly on the device pad[8,9,10]. General Electric (GE) researchers have developed the thin-film power overlay technology for packaging power devices; they use thin-film deposition followed by electroplating processes for device interconnections[6]. Recent power modules developed at Semikron contain spring-loaded metal strips that form electrical contacts on power devices by mechanical force[11]. Ferreira *et al.* proposed a packaging concept involving multiple layers of electromagnetic materials and switching function layers[12]. Linden *et al*. developed a power circuit substrate and packaging technology combining multichip module-laminated (MCM-L) technology with Insulated Metal Substrate (IMS) technology[13]. All of these technologies have yet to prove their manufacturability, reliability, and cost effectiveness.

Power electronics modules in the form of hybrid packaging are quite feasible and economical for a wide range of power applications. Several manufacturers such as International Rectifier, Toshiba, Powerex, Eupec, Fuji and IXYS now offer hybrid packaging with switching devices assembled in planar structures[14]. In some cases, the gate drives and control, and protection circuits are put together in a subassembly and incorporated in a single module. This type of integration approach increases the size and cost of the module, introduces undesirable degrading parasitics and is prone to failure. Also, the package is fundamentally limited in power due to thermal management problems, an essentially one-dimensional heat flow path. Consequently, this approach is only realized in low-power applications, ranging from a few hundred watts to a few kilowatts. As a result, innovative three-dimensional integration technologies must be developed[6,15].

1.2 INTRODUCTION TO METAL POSTS INTERCONNECTED PARALLEL PLATE STRUCTURE (MPIPPS)

A primary objective of this research was to design and fabricate a reliable, high performance packaged PEBB (power electronics building block) modules by eliminating the use of wire bonds for device interconnection. Our analysis on the package layout suggests that laminated terminal and package structure can reduce the conductor trace inductance. Compact packaging, such as close device spacing and tight utilization of substrate area, and the "hybrid" type of packaging such as integrated gate resistors and clamping capacitors, are desirable for a power module to have less packaging parasitic inductance and high reliability. The basic concept of multi-layer package is to sandwich the semiconductor devices into the bottom and the top layers so that the interconnections between the devices go to the top layer rather than stay in the bottom layer, thus eliminating wire-bonds.

A new PEBB packaging configuration called MPIPPS (metal posts interconnected parallel plate structure) was designed and built to operate at 3.3 kW per phase input power in the first phase of the module packaging research. Electrical modeling work was performed to verify and optimize the circuit layout of this new packaging design, and to justify the use of a multi-layer design over conventional wire bond designs. These investigations found that wire-bond modules have large parasitic inductance, which mainly originates from the packaging terminal leads. The MPIPPS design (as shown in Figure 1.2.1) uses copper posts to replace wire bonds and allows incorporation of active cooling directly on the power devices to maximize thermal management. The feasibility of this packaging approach was demonstrated by constructing PEBB modules consisting of two IGBTs, two power diodes, some gate resistors, varistors and a capacitor.

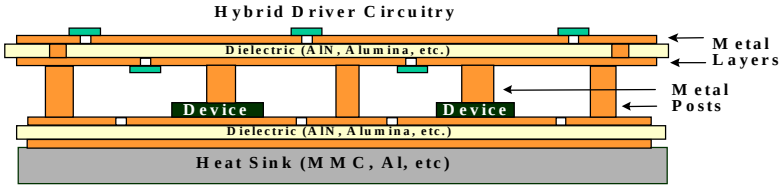

Figure 1.2.1. MPIPPS cross-section structure

The interior space between the parallel plates and the copper posts can be filled with a solid (or non-flowing liquid) dielectric for thermal spreading. More importantly, this structure provides the possibility of flowing a dielectric fluid directly through the module to carry heat away from the surface area of the devices, copper posts and parallel plates. The power module has two layers of metallization with the devices sandwiched between the metallic layers. The bottom layer is an AlN-DBC (aluminum nitride-direct bond copper) with copper thickness about 10 mil. The copper layer is etched to a desired pattern where the IGBTs and diodes are attached by soldering. The copper posts, which have different sizes and heights for IGBT, diode, and top and bottom DBC plate connections, are soldered on top of devices and copper metallization on AlN substrate. The top DBC plate is etched to a desired pattern and attached on to the copper posts of the bottom DBC plate to complete the electrical layout. A few gate driver circuitry elements and passive components are placed inside this package.

The feasibility of this packaging approach has been demonstrated by constructing PEBB modules consisting of two IGBTs, two power diodes, a few gate resistors and varistors and a capacitor. Upon successful completion of 3.3 kW module, the research was continued for higher power (20 kW) module fabrication in the second phase of the packaging research. In chapter 2, MPIPPS package design, fabrication and test results for two different power levels are presented.

1.3 SIGNIFICANCE OF INTERFACE ENGINEERING IN PACKAGE FABRICATION

Integration in power electronics is a rather complex issue due to the incompatibility of materials and processing methods used in fabrication, and due to the high energy level these components must handle. Moreover, high-density packaging creates high heat fluxes with limited area and volume for thermal dissipation. In most cases, the selected bonding agents (typically, solder, conductive/non-conductive epoxies and thermal grease) in a packaging scheme introduce interfaces and/or interlayers of finite thickness. Interfaces are sharp boundaries between two dissimilar materials while interlayers are transition regions with a significant thickness between two bonded materials; an interlayer is likely to have different chemistry, structure and properties from the two bonded materials and to form two interfaces on either side of the interlayer.

Although in thermal and electrical modeling, these layers are considered uniform and homogeneous, providing excellent thermal contact, in reality, these layers are quite non-uniform and consist of voids and other irregularities, which introduce anomalous thermal spreading and unpredictable electrical performance[16,17]. Moreover, while strong interfaces and/or interlayers are necessary to ensure mechanical integrity of the bonded components, they are responsible for lowering the electrical and thermal

conductivities of the assemblage. Each interface decreases the performance of the system substantially as well as increases the manufacturing cost. In a commercially available wire-bonded power electronics module, as shown in Figure 1.3.1, from the device attachment to the baseplate, there exists several interfaces (silicon device - solder - molybdenum tab - solder - flexible copper - solder - copper of DBC substrate - solder - copper baseplate), none of which are systematically processed or characterized for proper thermal management and reliable operation of the power module.

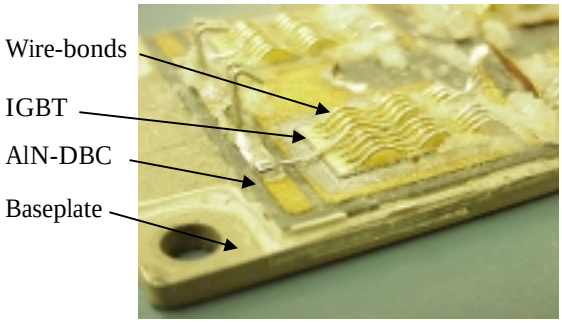

Figure 1.3.1. Components and interfaces of a commercial module (shown without the top plastic case)

Consequently, to successfully implement a packaging concept, such as MPIPPS, it is imperative to resolve many challenging issues related to materials and processing, which will result in improved reliability of the power electronics modules. From the cross-sectional view of the MPIPPS module (as shown in Figure 1.2.1), it is evident that the bonding techniques need to be optimized for joining different layers in the design. For example, eliminating wire bonds required the development of a solderable interface on the emitter contact of the IGBT and on the anode of the diodes, which is critical from an electrical point of view. From a thermal management point of view, attachment of a heatspreader to an MPIPPS module substrate needs to be optimally processed to minimize thermal resistance at that interface.

This research is focused into characterizing two specific interfaces of an MPIPPS module (as shown in Figure 1.3.2), the first interface of interest is the device interconnection interface while the second one is the module to heat spreader attachment interface. The device-pad to interconnection interface has been characterized for its electrical resistance, which is at the heart of implementing a direct chip attachment protocol, as proposed in the MPIPPS design. On the other hand, the module to heat-spreader interface serves the most critical task of heat dissipation and ensures proper thermal management of a three-dimensional power module structure. Furthermore, from a reliability point for view, the module to heatspreader interface is the most crucial interface in the whole package structure due to the significant mismatching of CTE with the silicon device.

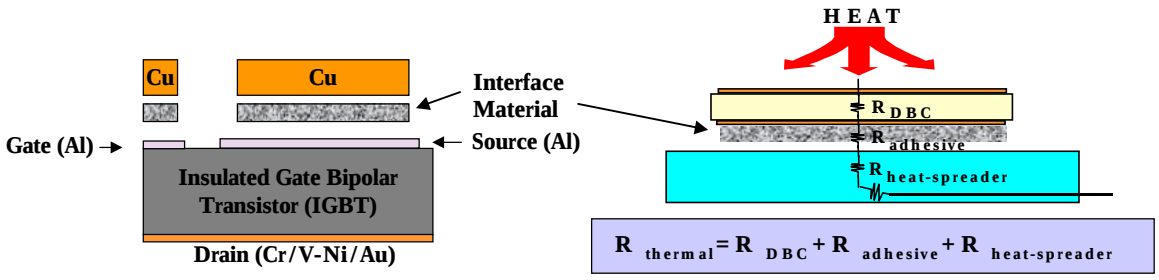

Figure 1.3.2. Cross-section view of critical interfaces: (a) device interconnection interface, (b) module to heat spreader attachment interface

In the following sections, the selected interfaces and their significances in the packaging scheme are discussed. Outlines for the proposed work on the selected interfaces are also presented.

1.3.1 Processing and Characterization of Device Interconnection Interface

In recent years, electronic packaging industry has experienced a tremendous boost in adopting flip-chip technology in all fronts of packaging applications. This increased level of acceptance of solder interconnect technology can be attributed to its increased speed, higher packaging density, and performance. Continuous improvements are sought in the areas of cost reduction, increased package density and enhanced reliability. In fact, the three most commonly used device interconnection methods are face-up wire bonding, face-up tape-automated bonding (TAB), and flip chip. Among these three methods, flip-chip solder interconnection technology provides the highest packaging density, greatest number of I/Os, shortest possible leads, lowest inductance, highest frequency, best noise control, smallest device footprints, and lowest packaging profile[18,19,20,21]. From a reliability point of view, solder joints must maintain mechanical as well as electrical performance in both power and thermal cycling of the module. Reliability is also a major concern for large area solder bumping of a chip. The device and the solder have different coefficients of thermal expansion, which may induce thermal stress and strain. In the case of power devices, such as IGBTs, the contact pads are larger than usual IC contact pads and hence, the reliability issues are even more pronounced. As a result, there must come an extension of the flip chip interconnection to accommodate larger and denser chips without affecting system reliability. Most importantly, implementation of the solder interconnection is required for power devices, thus eliminating the conventional wire-bond technology for device interconnection. Table 1.3.1 compares a few parameters, including reliability of the common interconnection methods.

Table 1.3.1. Parameters of the three different interconnections

Parameters for Comparison	**Wirebonding**		**TAB**	**Solder-Bump**
Connection Metallurgy	Al	Au	Cu	Pb-Sn
Resistance (Ω)	0.035	0.03	0.02	0.002
Inductance (nH)	0.65	0.65	2.10	0.200
Capacitance (pF)	0.006	0.006	0.04	0.001
I/O density (cm^{-2})	400	400	400	1600
Rework	Poor	Poor	Poor	Good
Failure rate (%/1000 h)	1×10^{-5}	1×10^{-5}	na	$<1\times10^{-3}$

To eliminate wire bonds by using soldered post interconnects on the power devices (diodes and IGBTs) for enhanced electrical and thermal performances, we need to make the device contact pads solderable. Currently, the device manufacturers for IGBTs and diodes use aluminum contact pads, which are not solderable. As a result, we investigated thin film deposition of solderable films on the Al contact pads of the power devices. The larger contact area of power devices greatly reduces current crowding and eliminates mechanical forces generated between wire bonds. This design also allows mechanical and thermo-mechanical forces to be distributed over a larger area, thus reducing equivalent mechanical stresses at the device connections. In order to implement solderable interconnects on IGBT pads, the following specific tasks are implemented.

- **Selection of an Under-Bump-Metallurgy (UBM):** Based on the IBM's C4 (controlled collapse chip connection) technology, a number of UBM techniques are in use in the microelectronics industry. Although the UBM metallizations are standard processes in IC packaging, their implementation to power devices are not fully researched. Therefore, we thoroughly investigated the available UBM schemes to carefully select a few, which will provide low-stress and low-contact resistance for device interconnections.
- **Processing of Solderable Metallization and Device Interconnection:** Based on the availability and suitability of UBM processes, we have employed three different UBM schemes with two different types of deposition processes. First, we examined thin film deposition of Ti-Ni-Cu and Cr-Cu systems by sputtering technique to make the contact pads of IGBTs and diodes solderable. Ti and Cr are used for the adhesion layer while Ni and a Cu thin film layers are deposited to make solderable contacts. The

third UBM scheme includes an electroless process of Zn-Ni-Au metallization on the device contact pads. Moreover, with a processed UBM, it is essential to select a compatible solder and deposition scheme, which will provide a reliable interconnection upon reflow.

- **Characterization of Device Interconnection Interface:** Developing a process of metallization for power devices is just one part of the solution; the performances of the new technology will eventually determine the breadth of its application. To ensure reliable performance of a solder interconnection, interface characterization is performed with micro-analytical techniques such as SEM and XPS, which would establish design rules for the solder interconnect technology for power devices.

Processing of the selected UBM processes and subsequent characterization of processed devices are presented in chapter 3.

1.3.2 Characterization of Interfacial Thermal Resistance

High power levels of power electronic modules such as an MPIPPS module, require thermal management techniques involving large capacity heat sinks, external cooling mechanism (e.g. air-flow) and careful management of interfacial thermal resistance. In order to optimize the device and module performance, the operating temperatures have to be kept within an acceptable range with a well-designed thermal management protocol. In most practical applications, the heat generated by the power devices is transferred to the ambient environment. Attaching a heat spreader to the semiconductor package surface facilitates this heat transfer process between the devices and the surrounding environment. An extensive amount of research has been performed over the years in the area of selecting an optimum heat spreader for specific applications[22,23,24,25,26]. Once the heat spreader is selected, it has to be attached optimally to the semiconductor package to ensure efficient thermal management through the thermal interface, which is created in the attachment process.

Attachment of a heat spreader to a package requires that two solid surfaces be brought together into intimate contact. Unfortunately, regardless of the process, solid surfaces are never completely flat or smooth enough to provide a perfect thermal contact. All surfaces have microscopic roughness as well as macroscopic non-planarity. In most cases, as two surfaces are brought together, less than one percent of the surfaces make physical contact while as much as 99% of the surfaces are separated by a thin layer of interstitial air[27,28]. Although some heat is conducted through the contact points, which are physically connected, most of the heat is handled by the air gaps. Since air is a very poor heat conductor, we need to eliminate the air gaps by using a more conductive material than air and thus, improve the interface thermal performance. Several types of thermally conductive materials are used to eliminate the air gaps from a thermal interface. Most commonly used interface materials include thermal grease, reactive compounds, elastomers, solders and pressure sensitive adhesive tapes, which are designed to conform surface irregularities. In most cases, the adhesive manufacturer provides only the thermal conductivity data, which is a bulk property and is of limited practical value for thermal designing of the package. A more useful data is the thermal resistance, which describes the resistance to heat flow in a more practical manner.

The rate of conductive heat transfer, Q, across the interface is given by[27],

$$\mathbf{Q = [kA\,(T_c - T_s)]\,/\,L}$$

where, k = thermal conductivity of the interface material
A = area of heat transfer
L = interface thickness
T_c = device case temperature and
T_s = heat sink temperature

As a result, the thermal resistance of an interface can be expressed as,

$$\mathbf{R_{c\text{-}s} = (T_c - T_s)\,/\,Q} \qquad \textbf{or} \quad \mathbf{R_{c\text{-}s} = L\,/\,(kA)}$$

Hence, the thermal resistance of the joint is directly proportional to the interface thickness and inversely proportional to the thermal conductivity of the interface material as well as to the contact area of the heat transfer. Therefore, thermal resistance should be minimized by:

- making the interface as thin as possible,
- increasing thermal conductivity by selecting a highly thermally conductive material, and
- eliminating interstitial air gaps.

Predicting the thermal performance of a packaged assembly has always been a weak link between thermal modeling and reliability analysis. Researchers have used finite element and analytical modeling, which employs an electrical resistance analog of parallel and series resistors, ignoring any contributions from the contact resistances. However, interfacial contact resistance is quite a significant factor in determining the total thermal resistance of a package since the uncertainty of the contact resistance can be large. Studies have shown that the contact or the interfacial resistance contributes a significant portion of the package thermal resistance[29,30,31]. Accordingly, the proposed research is focused towards process tailoring and characterization of interfacial thermal resistance of the module to heat-spreader attachment layer, which would allow us to identify the structure-property relationship of the interface layers. In order to achieve the overall objective of interfacial thermal characterization, the following experimental work are implemented:

- **Processing of the Selected Materials for Heatspreader Attachment:** In most electronic packaging applications, the attachment materials are solders and organics. Most common solders are tin-lead alloys, which provide both electrical and thermal paths. Organic attachment materials or epoxies are usually selected based on specific electrical and thermal needs. We will investigate electrically conductive (or insulating) bonding materials in pre-formed films and paste forms containing metallic (or polymeric) powder particles in an organic binder vehicle. These materials are easier to apply and can be processed by a low-temperature curing cycle; however, they generally result in thick interlayers which may have low electrical as well as thermal conductivity because of the organic content. Processing parameters such as applied pressure during bonding as well as reflow/curing environment will be varied to fabricate sample test structures for subsequent thermal resistance measurements.
- **Thermal Resistance Measurements for the Module to Heatspreader Interface:** Thermal testing needs to be incorporated into module testing to evaluate thermal performance and validate thermal modeling. The common test methods measure steady-state heat flux through a flat specimen. For the calculation purpose, it is assumed that the materials are homogeneous. In reality, some of the materials are not homogeneous, however, the assumption does not detract from the usefulness of the test methods. The term thermal conductivity applies to homogeneous materials. Thermally conductive insulating materials are usually heterogeneous since they typically include fillers, binders, reinforcements such as glass fiber mesh or a layer of a polymeric film. In general, the test methods are useful with either homogeneous or composite thermally conductive sheet materials. We will investigate the common techniques available for interface resistance measurements and evaluate their applicability to our test package structures. Once we have selected the measurement technique, thermal resistance of the test structures will be measured.
- **Defect Quantization of Interface Layers via Acoustic Micrography Imaging:** In recent years, acoustic microscopy has emerged as a non-destructive failure analysis tool to evaluate different package designs in the semiconductor industry[32,33,34]. Using acoustic micrographs of the bonding layers, we may detect internal discontinuities in materials and components. Furthermore, this study will allow us to optimize the bonding processes with a proper selection of a bonding material, which will minimize the void-fraction to ensure improved thermal management. The images of voids, cracks, disbonds and delaminations would enable us to distinguish the irregularities from one another. The most important feature of this tool is that it is non-destructive, which gives the researcher more opportunities for further electrical or thermal testing.

It is expected that characterization of the interfaces of these tested samples would allow us to establish a correlation between interfacial thermal resistance and void formation as a function of process variables, such

as applied pressure and process environment. Furthermore, this work would enable us to tailor the bonding process of the selected interface material for the module to heat-spreader attachment, with a minimized void-fraction to ensure improved thermal management of power modules. Processing and characterization work on the module attachment interface as well as the analyses and conclusions of this work are presented in chapter 4.

Packaging of power electronics building blocks is a critical part of the Navy's strategic approach to power electronic systems. The accomplishments on this research to date and the future endeavors reported here will significantly advance the current packaging effort and establish a solid foundation for the development and implementation of future power electronics modules with enhanced reliability.

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