OPTIMIZED HARMONIC STEPPED-WAVEFORM FOR MULTILEVEL INVERTER

CHAPTER 1

INTRODUCTION

1.1 Harmonics in Electrical Systems

One of the biggest problems in power quality aspects is the harmonic contents in the electrical system. Generally, harmonics may be divided into two types: 1) voltage harmonics, and 2) current harmonics. Current harmonics is usually generated by harmonics contained in voltage supply and depends on the type of load such as resistive load, capacitive load, and inductive load. Both harmonics can be generated by either the source or the load side. Harmonics generated by load are caused by nonlinear operation of devices, including power converters, arc-furnaces, gas discharge lighting devices, etc. Load harmonics can cause the overheating of the magnetic cores of transformer and motors. On the other hand, source harmonics are mainly generated by power supply with non-sinusoidal voltage waveform. Voltage and current source harmonics imply power losses, Electromagnetic Interference (EMI) and pulsating torque in AC motor drives. Any periodic waveform can be shown to be the superposition of a fundamental and a set of harmonic components. By applying Fourier transformation, these components can be extracted. The frequency of each harmonic component is an integral multiple of its fundamental. There are several methods to indicate of the quantity of harmonics contents. The most widely used measure in North America is the total harmonics distortion (THD) [3], which is defined in terms of the amplitudes of the harmonics, H_n, at frequency $nw_{0,}$

where w_0 is frequency of the fundamental component whose amplitude of H_1 and n is integer. The THD is mathematically given by

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} H_{(n)}^{\ 2}}}{H_1} \tag{1.1}$$

1.2 Conventional Two-Level and Three-Level Voltage Source Inverter

Switch-mode dc-to-ac inverters used in ac power supplies and ac motor drives where the objective is to produce a sinusoidal ac output whose magnitude and frequency can both be controlled. Practically, we use an inverter in both single-phase and three-phase ac systems. A half-bridge is the simplest topology, which is used to produce a two-level square-wave output waveform. A center-tapped voltage source supply is needed in such a topology. It may be possible to use a simple supply with two well-matched capacitors in series to provide the center tap. The full-bridge topology is used to synthesize a three-level square-wave output waveform. The half-bridge and full-bridge configurations of the single-phase voltage source inverter are shown in Fig. 1.1 and 1.2, respectively.

In a single-phase half-bridge inverter, only two switches are needed. To avoid shoot-through fault, both switches are never turned on at the same time. S_1 is turned on and S_2 is turned off to give a load voltage, V_{AO} in Fig. 1.1, of $+V_s/2$. To complete one cycle, S_1 is turned off and S_2 is turned on to give a load voltage, V_{AO}, of $-V_s/2$. In full-bridge configuration, turning on S_1 and S_4 and turning off S_2 and S_3 give a voltage of V_S between point A and B (V_{AB}) in Fig. 1.2, while turning off S_1 and S_4 and turning on S_2 and S_3 give a voltage of $-Vs$.

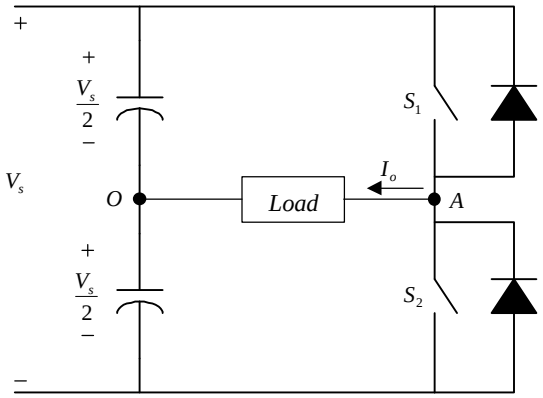

Figure 1.1 Half-bridge configuration.

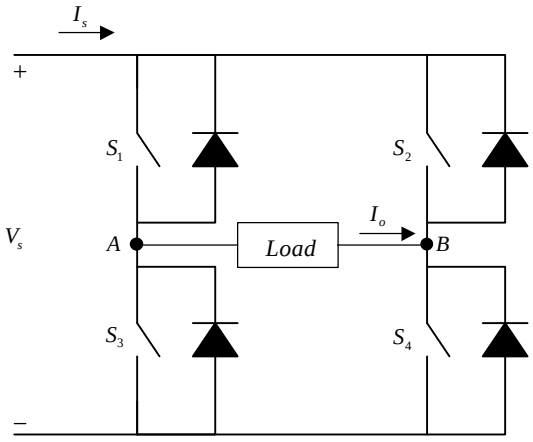

Figure 1.2 Full-bridge configuration.

To generate zero level in a full-bridge inverter, the combination can be S_1 and S_2 on while S_3 and S_4 off or vice versa. The three possible levels referring to above discussion are shown in Table 1.1.

Table 1.1 Load voltage with corresponding conducting switches.

Conducting Switches	Load Voltage V_{AB}
S_1, S_4	$+V_s$
S_2, S_3	$-V_s$
S_1, S_2 or S_3, S_4	0

Note that S_1 and S_3 should not be closed at the same time, nor should S_2 and S_4. Otherwise, a short circuit would exist across the dc source. The output waveform of half-bridge and full-bridge of single-phase voltage source inverter are shown in Fig. 1.3 and 1.4, respectively.

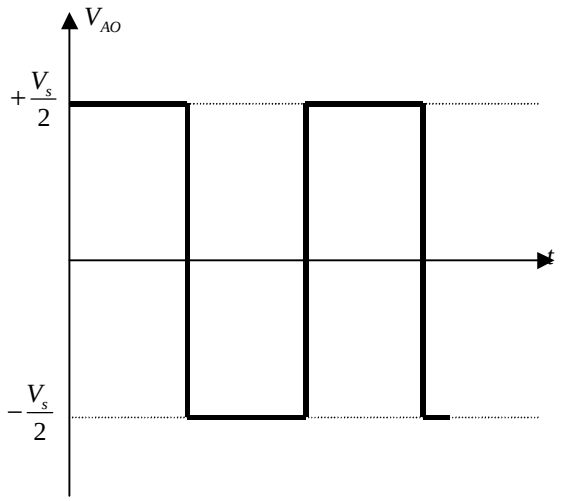

Figure 1.3 Output waveform of half-bridge configuration.

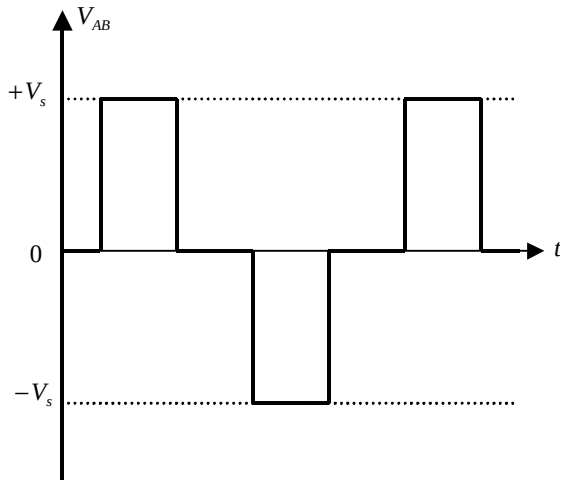

Figure 1.4 Output waveform of full-bridge configuration.

1.3 Multilevel Voltage Source Inverter

The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output [1], [2], [3]. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The so-called multilevel starts from three levels. As the number of levels reach infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints.

In this thesis, three capacitor voltage synthesis-based multilevel inverters are introduced, i.e.

1) Diode-Clamped Multilevel Inverter [1], [2].
2) Flying-Capacitor Multilevel Inverter [1].
3) Cascaded-Inverters with Separated DC Sources [1].

1.3.1 Diode-Clamped Multilevel Inverter (DCMI)

The diode-clamped multilevel inverter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. To produce m levels of the phase voltage, an m-level diode-clamp inverter needs m-1 capacitors on the dc bus. A three-phase five-level diode-clamped inverter is shown in Fig. 1.5. The dc bus consists of four capacitors, i.e., C_1, C_2, C_3, and C_4. For a dc bus voltage V_{dc}, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level, $V_{dc}/4$, through clamping diodes. DCMI output voltage synthesis is relatively straightforward.

To explain how the staircase voltage is synthesized, point O is considered as the output phase voltage reference point. Using the five-level inverter shown in Fig. 1.5, there are five switch combinations to generate five level voltages across A and O. Table 1.2 shows the phase voltage level and their corresponding switch states.

From Table 1.2, state 1 represents that the switch is on, and state 0 represents the switch is off. In each phase leg, a set of four adjacent switches is on at any given time. There exist four complimentary switch pairs in each phase, i.e., S_{a1}-$S_{a'1,}$ S_{a2}-$S_{a'2,}$ ..., and S_{a4}-$S_{a'4.}$

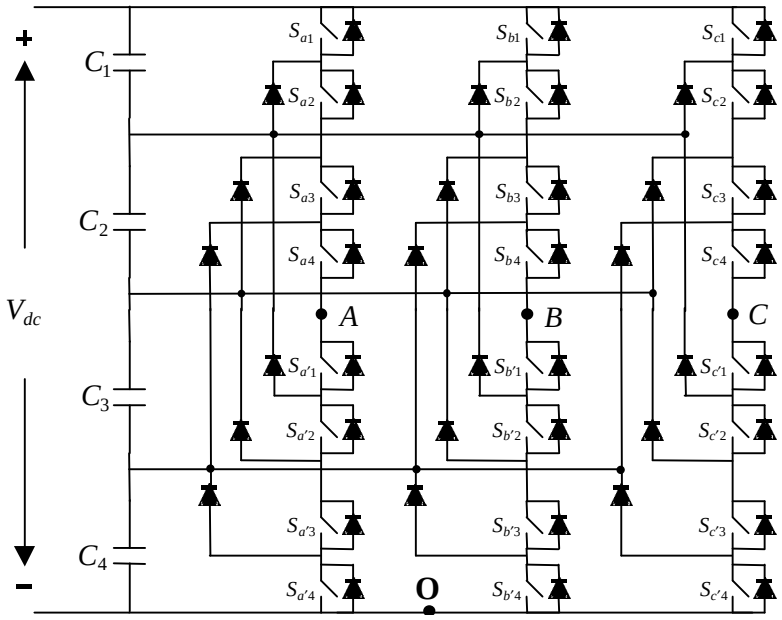

Figure 1.5 A three-phase five-level diode-clamped inverter.

Table 1.2 Diode-clamped five-level inverter voltage levels and their switch states.

Output	Switch State							
V_{AO}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3Vdc/4$	0	1	1	1	1	0	0	0
$V_3=Vdc/2$	0	0	1	1	1	1	0	0
$V_2=Vdc/4$	0	0	0	1	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

1.3.2 Flying-capacitor Multilevel Inverter (FCMI)

A FCMI shown in Fig. 1.6 uses a ladder structure of dc side capacitors where the voltage on each capacitor differs from that of the next capacitor. To generate *m*-level staircase output voltage, *m*-1 capacitors in the dc bus are needed. Each phase-leg has an identical structure. The size of the voltage increment between two capacitors determines the size of the voltage levels in the output waveform.

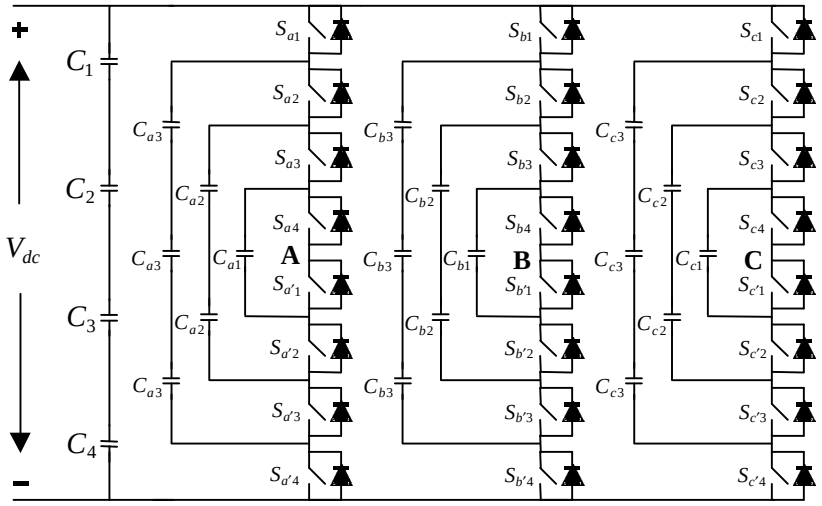

Figure 1.6 A three-phase five-level flying-capacitor inverter

It is obvious that three inner-loop balancing capacitors for phase leg A, C_{a1}, C_{a2}, and C_{a3} are independent from those for phase leg B. All phase legs share the same dc link capacitors, C_1-C_4. Table 1.3 shows a possible switch combination of the voltage levels and their corresponding switch states.

Table 1.3 A possible switch combination of the voltage levels and their corresponding switch states.

Output V_{AO}	Switch State							
	S_{a1}	S_{a2}	S_{am-1}	S_{am}	$S_{a'1}$	$S_{a'2}$	$S_{a'm-1}$	$S_{a'm}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_3=V_{dc}/2$	1	1	0	0	1	1	0	0
$V_2=V_{dc}/4$	1	0	0	0	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

In fact, there is more than one combination to produce output voltages V_2, V_3, and V_4. That makes the FCMI more flexibility than DCMI. Table 3, however, shows only one possible combination.

1.3.3 Multilevel Inverter Using Cascaded-Inverters with Separated DC Sources

The last structure introduced in this thesis is a multilevel inverter, which uses cascaded inverters with separate dc sources (SDCSs). The general function of this multilevel inverter is the same as that of the other two previous inverters. The multilevel inverter using cascaded-inverter with SDCSs synthesizes a desired voltage from several independent sources of dc voltages, which may be obtained from either batteries, fuel cells, or solar cells. This configuration recently becomes very popular in ac power supply and adjustable speed drive applications. This new inverter can avoid extra clamping

diodes or voltage balancing capacitors. A single-phase m-level configuration of such an inverter is shown in Fig 1.7

Each SDCS is associated with a single-phase full-bridge inverter. The ac terminal voltages of different level inverters are connected in series. By different combinations of the four switches, S_1-S_4, each inverter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$, and zero. The ac output of each of the different level of full-bridge inverters are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. Note that the number of output phase voltage levels is defined in different way from those of two previous inverters. In this topology, the number of output phase voltage levels is defined by $m = 2s+1$, where s is the number of dc sources.

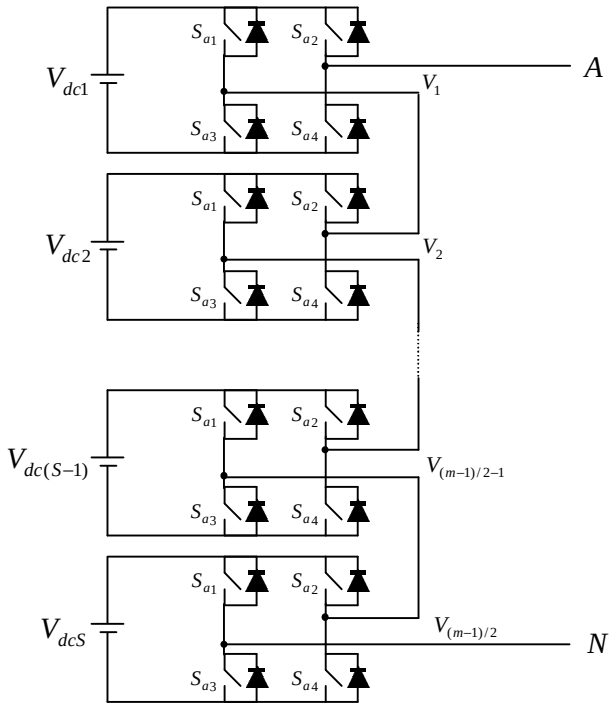

Figure 1.7 Single-phase structure of a multilevel cascaded inverter.

A 7-level cascaded-inverters based inverter, for example, will have three SDCSs and three full-bridge cells. Minimum harmonic distortion can be obtained by controlling the conducting angles at different inverter level, which will be proposed in Chapter 3.

For a three-phase system, the output voltage of the three cascaded inverters can be connected in either wye or delta configuration. For example, a wye-configured m-level inverter using cascaded-inverters with s separated capacitors is illustrated in Fig. 1.8.

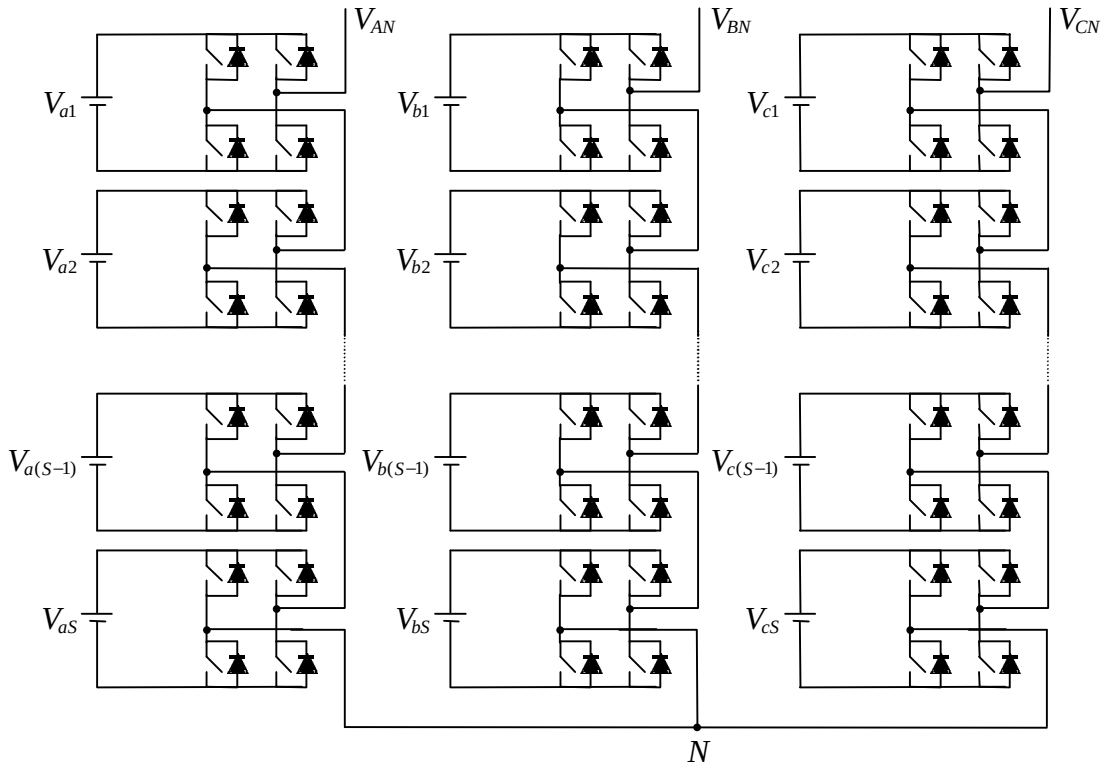

Figure 1.8 A general three-phase Wye-configuration cascaded-inverters based inverter.

1.3.4 Comparison among Three Multilevel Inverters in Application Aspects

In high power system, the multilevel inverters can appropriately replace the exist system that use traditional multi-pulse converters without the need for transformers. All

three multilevel inverters can be used in reactive power compensation without having the voltage unbalance problem [1]. In back-to-back intertie application, however, it is not possible to use multilevel inverter using cascaded-inverters with SDCSs because a short circuit will be introduced when two back-to-back inverter are not switching synchronously. To overcome such a problem, a transformer having one primary winding and several secondary windings can be used. On the other hand, the structure of separated dc sources is well suited for various renewable energy sources such as fuel cell, photovoltaic, biomass, etc. This structure is, therefore, suited for an ac power supply in vehicle system utilities. In the adjustable speed drive application, the multilevel inverters can be used for a utility compatible adjustable speed drive (ASD) with the input from the utility constant frequency ac source and the output to the variable frequency ac load. The major differences, when using the same structure for ASDs and for back-to-back interties, are the control design and the size of the capacitor. Because the ASD needs to operate at different frequencies, the dc link capacitor needs to be large enough to avoid a large voltage swing under transient state.

Table 1.4 compares the power component requirements per phase leg among the three multilevel voltage source inverter mentioned above. Table 1.4 shows that the number of main switches and main diodes, needed by the inverters to achieve the same number of voltage levels, is the same. Clamping diodes do not need in flying-capacitor and cascaded-inverter configuration, while balancing capacitors do not need in diode-clamp and cascaded-inverter configuration. Implicitly, the multilevel converter using cascaded-inverters requires the least number of components.

Table 1.4 Comparison of power component requirements per phase leg among three multilevel Inverters

Inverter Configuration	Diode-Clamp	Flying-capacitors	Cascaded-inverters
Main switching devices	2(m-1)	2(m-1)	2(m-1)
Main diodes	2(m-1)	2(m-1)	2(m-1)
Clamping diodes	(m-1)(m-2)	0	0
DC bus capacitors	(m-1)	(m-1)	(m-1)/2
Balancing capacitors	0	(m-1)(m-2)/2	0

Another advantage of cascaded-inverter is circuit layout flexibility. Modularized circuit layout and packaging is possible because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitor. The number of output voltage levels can be easily adjusted by adding or removing the full-bridge cells.

1.4 Modulation Topologies for Multilevel Inverter

It is generally accepted that the performance of an inverter, with any switching strategies, can be related to the harmonic contents of its output voltage. Power electronics researchers have always studied many novel control techniques to reduce harmonics in such waveforms. Up-to-date, there are many techniques, which are applied to inverter topologies. In multilevel technology, there are several well-known modulation topologies as follows:

1) Sinusoidal or “Subharmonic” Natural Pulse Width Modulation (SPWM) [4], [8].

2) Selective Harmonic Eliminated Pulse Width Modulation (SHE PWM) [4] or Programmed-Waveform Pulse Width Modulation (PWPWM) [10]
3) Optimized Harmonic Stepped-Waveform Technique (OHSW) [3], [13]

There are some advantages and disadvantages among these three techniques. All of these techniques will be briefly introduced in the following sections.

1.4.1 Sinusoidal Natural Pulse Width Modulation (SPWM)

Sinusoidal pulse width modulation is one of the primitive techniques, which are used to suppress harmonics presented in the quasi-square wave. Note that only triangular carrier is considered in this thesis. Fig. 1.9 illustrates a simple idea to generate a SPWM waveform. In the modulation techniques, there are two important defined parameters: 1). the ratio $P = \omega_c/\omega_m$ known as frequency ratio, and 2). the ratio $M = A_m/A_c$ known as modulation index, where ω_c is the reference frequency, ω_m is the carrier frequency, A_m is reference signal amplitude, and A_c is carrier signal amplitude.

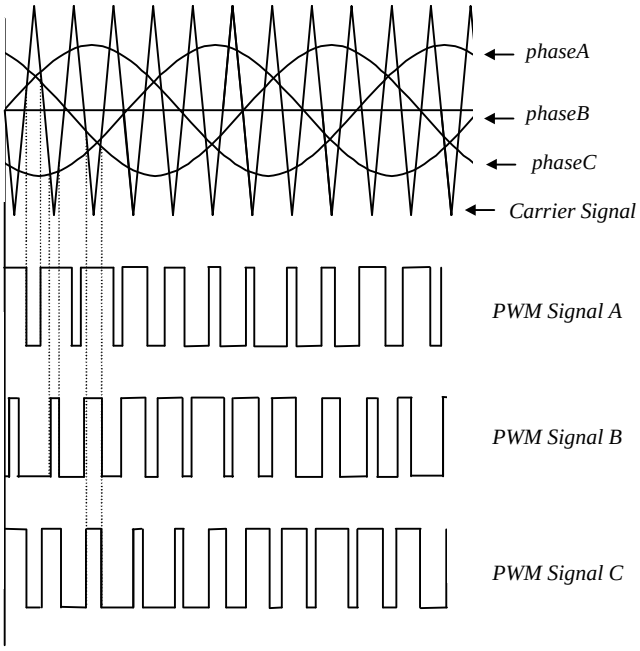

Figure 1.9 Three-phase two-level natural SPWM with a triangular-carrier

According to the work of Bowes [4], the phase voltage can be described by the following expressions:

$$V(t) = M\frac{E}{2}\cos(w_m t + f) + \frac{2E}{p}\sum_{m=1}^{\infty} J_0\left(\frac{mpM}{2}\right)\sin\left(\frac{mp}{2}\right)\cos(mw_c t)$$

$$+\frac{2E}{p}\sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}\frac{J_n\left(\frac{mpM}{2}\right)}{m}\sin\left(\frac{(n+m)p}{2}\right)\cos(mw_m t + nw_c t + (m+n)f) \qquad (1.2)$$

where w_m is the angular frequency of modulating or sinusoidal signal.

w_c is the angular frequency of the carrier signal.

M is modulation index.

E is the dc supply voltage.

f is the displacement angle between modulating and carrier signals.

and J_o and J_n are Bessel functions of the first kind.

From (1.2), the amplitude of the fundamental frequency components of the output is directly proportional to the modulation depth. The second term of the equation gives the amplitude of the component of the carrier frequency and the harmonics of the carrier frequency. The magnitude of this term decreases with increased modulation depth. Because of the presence of $\sin(mp/2)$, even harmonics of the carrier are eliminated. Term 3 gives the amplitude of the harmonics in the sidebands around each multiple of the carrier frequency. The presence of $\sin((m+n)p/2)$ indicated that, for odd harmonics of the carrier, only even-order sidebands exist, and for even harmonics of the carrier only odd-order sidebands exist. In addition, increasing carrier or switching frequency does not decrease the amplitude of the harmonics, but the high amplitude harmonic at the carrier frequency is shifted to higher frequency. Consequently, requirements of the output filter can be improved. However, it is not possible to improve the total harmonic distortion without using output filter circuits.

In multilevel case, SPWM techniques with three different disposed triangular carriers [8] were proposed as follows:

1) All the carriers are alternatively in opposition (APO disposition)
2) All the carriers above the zero value reference are in phase among them, but in opposition with those below (PO disposition)
3) All the carriers are in phase (PH disposition)

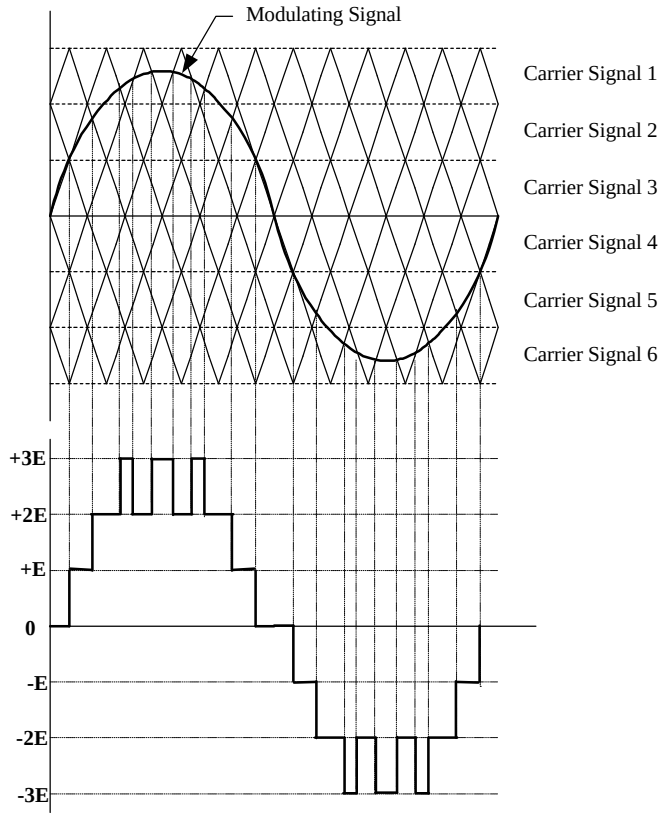

Figure 1.10 APO disposition

For example, Fig. 1.10 shows the APO disposition SPWM applied to a 7-level voltage waveform. To find the analytical expression of the multilevel SPWM waveforms, a complicated double-Fourier-series modulation-model method is approached [8]. For example, the final expression for APO disposition is given as

$$v(t) = MV\sin(w_m t + f)$$

$$+ 2\frac{V}{p}\sum_{\substack{n=3\\ odd}}^{+\infty}\left\{M\left[\frac{\sin[(n-1)p/2]}{n-1} - \frac{\sin[(n+1)p/2]}{n+1}\right] + \frac{2}{n}\cos(n\frac{p}{2})\right\}\sin(nw_m t + nf)$$

$$+ 4\frac{V}{p^2 N'}\sum_{m=1}^{+\infty}\frac{1}{m}\sum_{n=-\infty}^{+\infty}\left\{J_n(mMN'p)\frac{p}{2} - \sum_{\substack{h\neq -n\\ odd}} J_h(mMN'p)\frac{1}{(n+h)}\sin[(n+h)\frac{p}{2}]\right\}\sin(mw_c t + nw_m t + nf) \quad (1.3)$$

Note: V=N′E and N′=(N-1)/2, where N is the number of output voltage levels, and all the rest of parameters are referred to those in Equation (1.2).

Equation (1.3) explicitly shows that the multilevel technique expression turns out to be the same format as two-level SPWM's, which consists of three terms. Because all other harmonics amplitude divided by N′ which also appears in the argument of the Bessel's function as a multiplying factor, the last two terms of the equation point out the improvements in the harmonics reduction obtained by multilevel technique. It is, however, still not possible to improve THD without any filter circuits.

1.4.2 Selective Harmonic Eliminated Pulse Width Modulation (SHE PWM)

Since the advent of the family of new semiconductors, tremendous interest has been renewed in inverter technology. The ability of switching devices having turn-off times in the range of a few microseconds or submicroseconds, has increased the flexibility of achieving a practically sinusoidal output by employing sophisticated switching patterns in inverter circuit. Selective harmonic eliminated PWM technique is introduced by Patel [5]. The idea of such a method is that the basic square-wave output is "chopped" a number of times, which are obtained by proper off-line calculations.

A general method of harmonic elimination in the half-bridge inverter will be discussed here. Fig 1.11 shows a general output waveform with 2N chops per half-cycle.

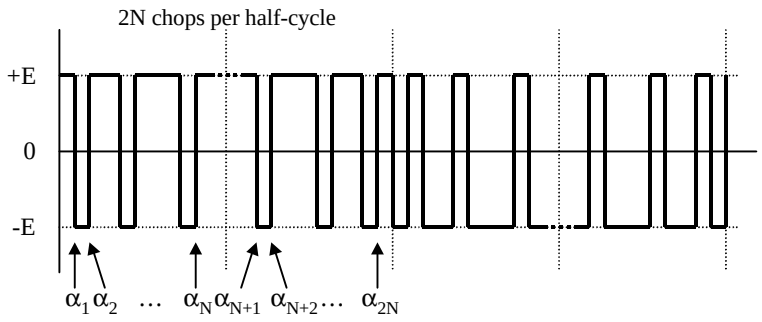

Figure 1.11 Waveform of a 2-level SHE PWM

It is assumed that the periodic waveform has quarter-wave symmetry, i.e.

$$a_k = p - a_{2N-k+1} \quad \text{, for } k = N+1, N+2, \ldots, 2N \tag{1.4}$$

To obtain the amplitude of each harmonic content, Fourier series is applied, and the final result is giving as:

$$Hn = \begin{cases} \dfrac{4E}{np}\left[(-1)^N\left(1+2\sum_{k=1}^{N}(-1)^k\cos(na_k)\right)\right] & for \quad odd \;\; n \\ 0 & for \quad even \;\; n \end{cases} \tag{1.5}$$

Equation 1.5 shows that *M-1* odd harmonics (3^{rd}, 5^{th},…) and *M-1* non-triplen odd harmonics can be eliminated from single-phase output waveform and three-phase output waveform, respectively, by solving *N*'s following equations:

$$H_1(a) = ME$$

$$H_k(a) = 0 \text{ , } k \text{ is a given eliminated harmonic order}$$

where M is modulation index and $E = V/2$, V is the dc voltage supply (1.6)

Due to nonlinear and transcendental characteristics, for each given *M*, equation (1.6) has to be numerically solved for proper switching angles [5]. To obtain fast convergence, the initial values must be chosen to be close enough to the exact solutions. This is one of the most difficult tasks associated with the selective harmonic eliminated technique. Several predicting schemes were developed and applied to overcome such a problem [12].

In solving nonlinear equation, however, is limited at three levels because of the solution difficulties. The three-phase three-level SHE PWM will be theoretically discussed in chapter 4. The results will be simulated in three-phase full-bridge circuit and verified by hardware prototype in chapter 5 and 6, respectively. The Optimized harmonic stepped-waveform topology then developed for multilevel inverter, which will be introduced in the following topic.

1.4.3 Optimized Harmonic Stepped-Waveform Technique (OHSW)

The optimized harmonic stepped-waveform technique is very suitable for a multilevel inverter circuit. By employing this technique along with the multilevel topology, the low THD output waveform without any filter circuit is possible. Switching devices, in addition, turn on and off only one time per cycle. That can overcome the switching loss problem, as well as EMI problem. Fig. 1.12 shows a general quarter-symmetric 11-level OHSW waveform.

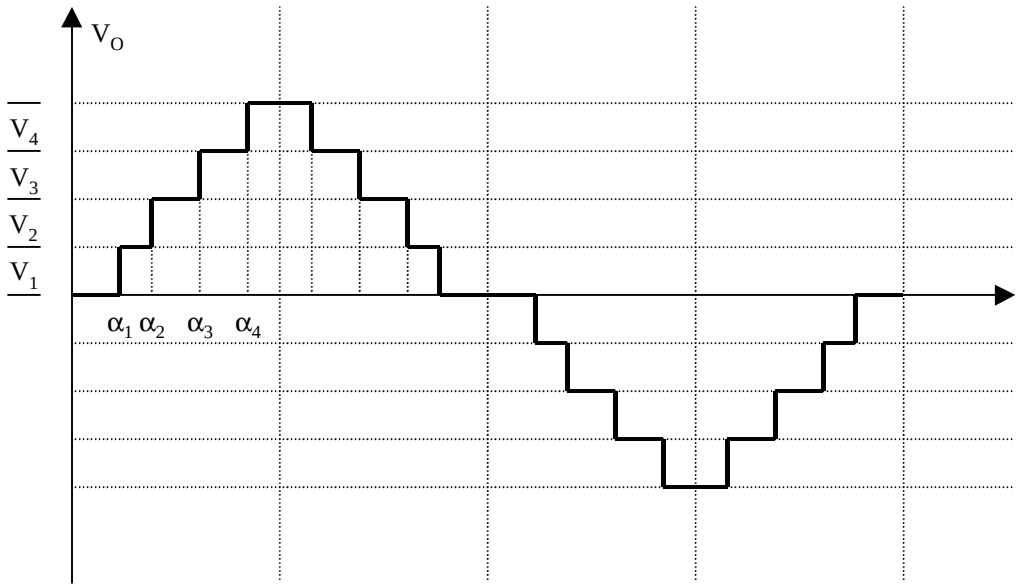

Figure 1.12 Eleven-level OHSW output waveform.

In Fig. 1.12, V_1 to V_4 are dc voltage supplies, which are from either regulated capacitors or separated dc sources. Consider the waveform, there are three possible optimization techniques for reducing the low-order harmonics: 1) step heights are optimized with equally spaced steps; 2) step spaces are optimized with the steps of equal height; and 3) optimizing both heights and spaces. In the fixed-input scheme, the second optimization technique is more feasible than the other two techniques. In the thesis, therefore, the second optimization technique will be proposed.

With the equal amplitude of all dc sources, the expression of the amplitude of the fundamental and all harmonic contents are given as:

$$H_n(a) = \begin{cases} \dfrac{4E}{np} \displaystyle\sum_{k=1}^{m} \cos(n a_k) & \textit{for odd } n \\ 0 & \textit{for even } n \end{cases}$$

where

E is dc voltage supply

m is the number of dc sources

and a_k is the optimized harmonic switching angles (1.7)

Basically, the low-order surplus harmonics needed to be eliminated. Equation (1.7) shows that M-1 odd harmonics (3^{rd}, 5^{th},…) and M-1 non-triplen odd harmonics (5^{th}, 7^{th}, …) can be eliminated from single-phase output waveform and three-phase output. The 3^{rd}, 5^{th}, 7^{th}, and 9^{th} harmonic, for example, can be eliminated from single-phase eleven-level output waveform. The OSHW technique will be discuss in the detail in chapter 3.

1.5 Objective of the thesis

As discussed in 1.3, the concept of multilevel inverter using cascaded-inverters with separated dc sources is very interesting due to many reasons. This topology is required the least number of components, among all multilevel inverters, to achieve the same number of voltage levels. It is also possible to be modularized circuit layout and packaging because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitors. In addition, soft-switching technique can be applied in this structure to avoid bulky and lossy resistor-capacitor-diode snubbers, as part of future research [26].

Among modulation techniques being used these days, optimized harmonic stepped-waveform technique is suitable for multilevel inverter topologies. By employing

this technique along with the multilevel topology, a low THD output waveform without any filter circuit is possible. Besides, switching devices switch only one time per each cycle. That can improve the switching loss problem, as well as EMI problem.

In this thesis, the optimized harmonic stepped-waveform techniques will be applied to the multilevel inverter using cascaded-inverters with separated dc sources. The objective of the thesis is as follows:

1) Propose the method to find proper switching angles to minimize the total harmonic distortion in multilevel voltage waveform.
2) Study the relationship between the number of output levels and the total harmonic distortion with different modulation index.
3) Compare the results of the multilevel inverter using cascaded-inverters with OHSW technique to those of the full-bridge inverter with SHE PWM.
4) Simulate the results by computer program.
5) Verify the results from the computer simulation with the hardware prototype.
6) Make conclusions from the result observed.

This thesis consists of seven chapters. The theory of a cascaded-inverter with separated dc sources will be described in chapter 2. Chapter 3 will talk about the optimized harmonic stepped-waveform for a multilevel inverter. The selective harmonics elimination for a three-level inverter will be theoretically discussed in Chapter 4. The simulation results and experimental results will be presented in Chapter 5 and 6, respectively. Finally, Chapter 7 will conclude all work.