Dependence of Set, Reset and Breakdown Voltages of a MIM Resistive Memory Device on the Input Voltage Waveform

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Abstract

Owing to its excellent scaling potential, low power consumption, high switching speed, and good retention, and endurance properties, Resistive Random Access Memory (RRAM) is one of the prime candidates to supplant current Nonvolatile Memory (NVM) based on the floating gate (FG) MOSFET transistor, which is at the end of its scaling capability. The RRAM technology comprises two subcategories: 1) the resistive phase change memory (PCM), which has been very recently deployed commercially, and 2) the filamentary conductive bridge RAM (CBRAM) which holds the promise of even better scaling potential, less power consumption, and faster access times. This thesis focuses on several aspects of the CBRAM technology. CBRAM devices are based on nano-ionic transport and chemo-physical reactions to create filamentary conductive paths across a dielectric sandwiched between two metal electrodes. These nano-size filaments can be formed and ruptured reliably and repeatedly by application of appropriate voltages. Although, there exists a large body of literature on this topic, many aspects of the CBRAM mechanisms and are still poorly understood. In the next paragraph, the aspects of CBRAM studied in this thesis are spelled out in more detail.

CBRAM cell is not only an attractive candidate for a memory cell but is also a good implementation of a new circuit element, called memristor, as postulated by Leon Chua. Basically, a memristor, is a resistor with a memory. Such an element holds the promise to mimic neurological switching of neuron and synapses in human brain that are much more efficient than the Neuman computer architecture with its current CMOS logic technology. A memristive circuitry can possibly lead to much more powerful neural computers in the future. In the course of the research undertaken in this thesis, many memristive properties of the resistive cells have been found and used in models to describe the behavior of the resistive switching devices.

The research performed in this study has also an immediate commercial application. Currently, the semiconductor industry is faced with so-called latency scaling dilemma. In the past, the bottleneck for the signal propagation was the time delay of the transistor. Today, the transistors became so fast that the bottleneck for the signal propagation is now the RC time delay of the interconnecting metal lines. Scaling drives both, resistance and parasitic capacitance of the metal lines to very high values.

In this context, one observes that resistive switching memory does not require a Si substrate. It is therefore an excellent candidate for its implementation as an o n-chip memory above the logic circuits in the CMOS back-end, thus making the signal paths between logic and memory extremely short. In the framework of a Semiconductor Research Corporation (SRC) project with Intel Corporation, this thesis investigated the breakdown and resistive switching properties of currently

deployed low k interlayer dielectrics to understand the mechanisms and potential of different material choices for a realization of an RRAM memory to be implemented in the back-end of a CMOS process flow.

Acknowledgment

"*Trust in the Lord with all your heart, and lean not on your own understanding, in all your ways acknowledge Him, and He shall direct your paths.*" Proverbs 3:5-6

I would like to express my deepest gratitude to my advisor Dr. Marius Orlowski who has been my source of inspiration during the entire degree. Under his guidance I have evolved not only as a researcher but also as fellow human being. He has provided me the valuable opportunity to pursue research and has been kind and extremely encouraging towards me trying out new ideas. Whatever I have accomplished so far has been possible because of his continued support and guidance especially during difficult times. I feel privileged to have known such a great person personally.

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Thesis Objective and Organization

The objective of this work is to understand the working mechanisms of resistive switches and interconnect structures device based on electrical characterizations and computational models, and evaluate its applications to nonvolatile memory and modern day chaotic circuits. This thesis is organized in 7 chapters.

Chapter 1 lays the foundation to the thesis. It gives us a glimpse to the fundamental theories and underlying physics that serve as the guidelines for the entire work. The basic principles and behaviors of MIM have been illustrated by dividing it into two parts: (i) Interconnect Structure (ii) Resistive Memory. The quasi-static I–V sweeping and constant voltage bias is used to characterize the electrical performance of the devices. Metal and oxygen vacancy (V_O) filaments are investigated under bias voltages with opposite polarities.

Chapter 2 presents the fabrication process. The procedure remains mostly common to both resistive switches and interconnect structures. The devices are designed in crossbar layout and island structure respectively. They have typically been processed by electron beam evaporation and lift-off technology. This chapter also gives a list of the samples that have been fabricated using the explained procedure.

Chapters 3, 4, 5 and 6 summarize the work that have been done for this thesis. They are independent from each other and make use of the important concepts stated in Chapter 1.

Chapter 3 presents the vacancy filament switching of Cu/TaO_x/Pt devices. This chapter discusses the feasible mechanism pertaining to the formation of the vacancy bridge. Various device structures have been identified to study the technique that could possily be involved in the formation of the oxygen vacany nanofilament. A comparative analysis has been performed between these conductive bridges bridges and valuable insights were formed. The physical behavior of an oxygen vacancy is illustrated in terms of various parameters, viz.: complaince current, linear ramp rate, on resistance, thickness of the dielectric, voltage bias etc.

Chapter 4 presents the circuit elements based on Cu/TaO_x/Pt devices. A statistical dependence of set voltage, V_{SET}, on the preceding reset voltage, V_{RESET}, is observed in resistive RRAM memory arrays and explained in terms of two interlocking mechanisms. This dependence can be replicated on a single device by intentionally varying V_{RESET} values by various linear voltage ramp rates. The latter mechanism is well modeled under the assumption that a critical heat deposited locally in the filament triggers the rupture of the filament.

Chapter 5 discusses a contribution of electrodes into the functioning of a resistive swtich. Keeping Cu/TaO_X/Pt as a benchmark, electrodes have been replaced with Ta and Ti one at a time, resulting into four unique devices. They have been individually studied by positive and negative voltage sweeps. The I-V characteristics attained in the process gives a brilliant insights based on the fine

differences observed. It also serves as a conclusion for some of the important characterization in Chapter 6

Chapter 6 presents a collaboratory work between Intel Inc and Virginia Tech. The problems associated with aggressive scaling of devices have been addressed by studying the nature of switching of a low-k dielectric Cu interconnect structure. A reliability study of time dependent dielectric breakdown has been performed to understand the basic principles that govern the functioning of various kinds of low-k organo-silicate materials. A possibility of resistive switching has also been investigated in the process. This is an ongoing project and therefore only the data available till date has been utilised to prepare the thesis.

Finally, Chapter 7 summarizes the conclusions of this work and recommends possible future areas of investigation.

My Specific Contribution to this work

- Manufacturing Resistive Switches
- Preparation of samples for ILD Characterization to be performed by Intel Inc.
- Deposition of top electrode on the Intel's interconnect structures.
- Study Characterization and Modelling of the V_{SET} and V_{RESET} interdependence.
- Mechanisms of formation for the oxygen vacancy filaments in a $Cu/TaO_X/Pt$ device.
- Investigation of the impact of the choice of materials for the metal electrodes on the formation and rupture of conductive filaments.
- Characterization of Intel's MIM structures for dielectric breakdown and resistive switching properties.

Chapter 1: Introduction to Resistive Switching and its Basic Mechanisms

This chapter starts with an introduction to semiconductor devices and serves as the motivation to this thesis. The metal/insulator/metal (MIM) structures are discussed based on their challenges and opportunities in modern industries. Literature has been reviewed to lay a foundation to the fundamental concepts pertained to a typical MIM structure.

1.1 Semiconductor Industry – Current Scenario

In the past 25 years, aggressive scaling in semiconductor devices has taken its toll, according to Moore's law, leading to the shrinkage of integrated circuit feature size (channel length/half-pitch) from 1 μm to as low as 14 nm as of 2014. The one-dimensional scaling factor is about 0.7 for the feature size in every two years which yield a factor of 0.5 for the device footprint [1,2]. The smaller feature size allows more transistors on a single chip, more functions of the circuits, faster switching and lower cost for each function. Such an effect is instigated by the fierce competition in the market. Figure 1.1 illustrates the trend of technology node shrinkage.

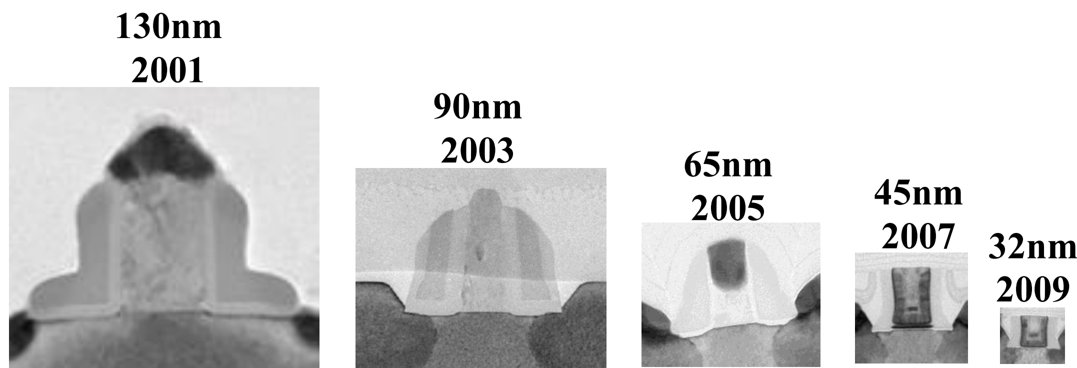


Figure 1.1: Moore's Law and Ever Shrinking devices. Intro to Low-k/Cu Interconnects and Time Dependent Dielectric Breakdown (TDDB) Sean W. King, Logic Technology Development, Technology Manufacturing Group, Intel Corporation, Intel Technical Lecture Series, September 2014. Used with the permission of Dr. Sean King, Intel Corporation.

With memory devices, the scaling factor gets even worse. Nowadays, huge amount of information are stored in hard disk drives, DRAM, flash memory (NAND/NOR), and solid state drives. However with the advent of non-volatile memory (NVM), interests has sort of shifted to mainstream memory devices particularly in the academia and industries [2]. NVM can store information after removal of power supply, which is very important for energy-efficient electronics and computing. It can also reduce the weight and increase the speed of portable personal devices. As a result, NVM devices are being developed more rapidly than any other data storage technologies.

The state-of-the-art NVM is flash memory, including NAND and NOR [3]. Flash memory was invented by Toshiba in 1980s. The basic device structure and operating mechanism are shown in Figure 1.2. The flash memory device is a MOSFET with an additional metal gate which is known as floating gate.

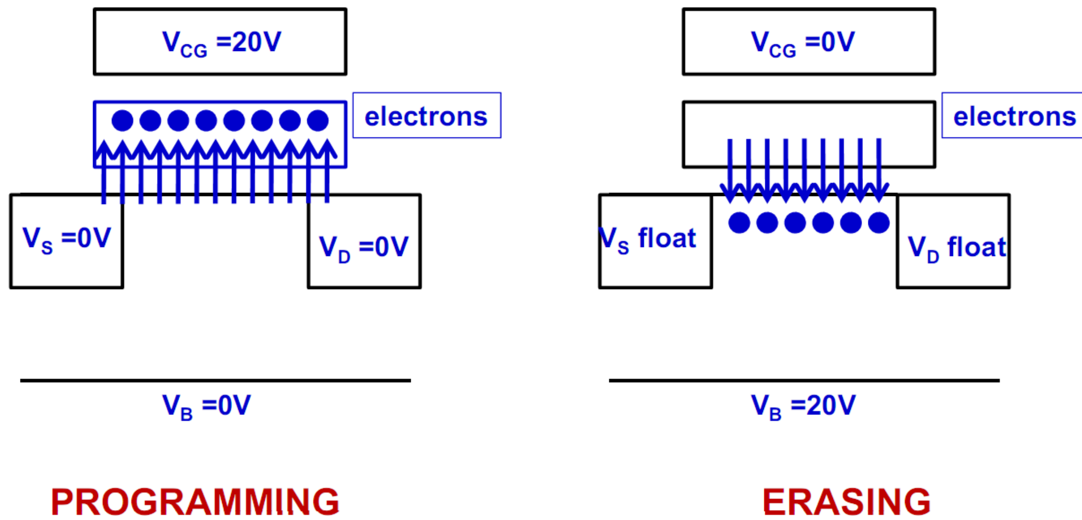


Figure 1.2. Device structure and operating mechanism of flash memory (floating gate device).

When a high voltage (~20 V) is applied to the control gate (non-floating), the electrons tunnel from the control gate and get stored in the floating gate. This asperities assisted tunneling procedure is called Fowler-Nordheim tunneling. The electrons stay on the floating gate after the gate voltage is removed, since the floating gate is surrounded by insulator (SiO_2) and has no way to leak out. A high write/erase voltage is needed to charge/discharge the floating gate. This is how the information is stored. The charges stored on the floating gate, leads to the increase in the threshold voltage of the device is significantly. The two states of the device (with and without charges on the floating gate) can be identified as “0” and “1” for data storage which can be distinguished by applying a read voltage (>threshold voltage).The International Technology Roadmap for Semiconductors (ITRS) roadmap of scaling has been given in Figure 1.3. No NVM is known to have been scaled successfully below 20nm, so far.

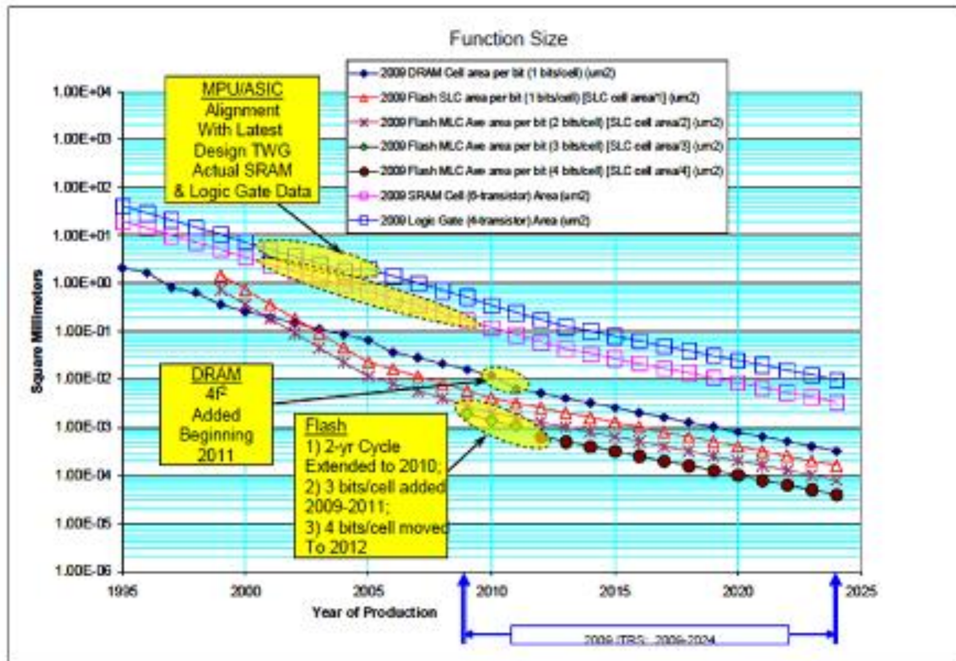


Figure 1.3: 2009 ITRS Product Function Size Trends. The International Technology Roadmap for Semiconductors, Semiconductor Industry Association, www.itrs.net., November 2012.

1.2 MIM Devices – Memory and Interconnects

In order to extend Moore's law in the next few decades, different classes of new technologies have been proposed and demonstrated in the field of semiconductor devices. Figure 1.4 is brilliant illustration of how modern day chips look, perceivable to the human eye. The phenomena in

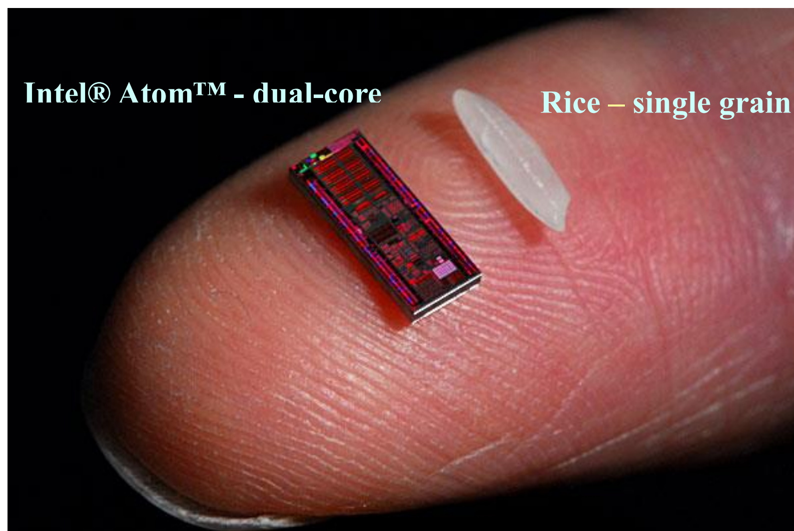


Figure 1.4: 47 Million Transistors 45nm node Hi-k Metal Gate 193 dry Litho. Intro to Low-k/Cu Interconnects and Time Dependent Dielectric Breakdown (TDDB) Sean W. King, Logic Technology Development, Technology Manufacturing Group, Intel Corporation, Intel Technical Lecture Series, September 2014. Used with the permission of Dr. Sean King, Intel Corporation.

nanostructures and quantum physics are extensively utilized for the emerging memory devices. Besides interconnect applications, the computing logics are also being developed based on the unique memory device characteristics.

Emerging research while developing resistive switching (RS) devices has exhibited the mechanism where a dielectric is intentionally broken down and "reformed" under voltage control to paradoxically perform various memory and logic applications.[5] The development of these RS devices has shown that switching/breakdown can occur due to the formation of either a metal or oxygen vacancy filament in the dielectric. The goal of this thesis is to combine these RS test methodologies to the investigation of low-k/Cu interconnect structure in order to come up with a more reliable device.

1.2.1 Interconnect Devices – Evolving Technology and its Reliability

According to the ITRS, device scaling will reach a sub-nanometer range and this will in turn encourage the exponential increase in the number of cores available in a single chip. This increase has brought interconnects to the forefront of the challenges facing the computing industry giving rise to new problems based on performance, robustness and longevity. This brings our industry to an alleged standstill and is probably one of the major concerns today.

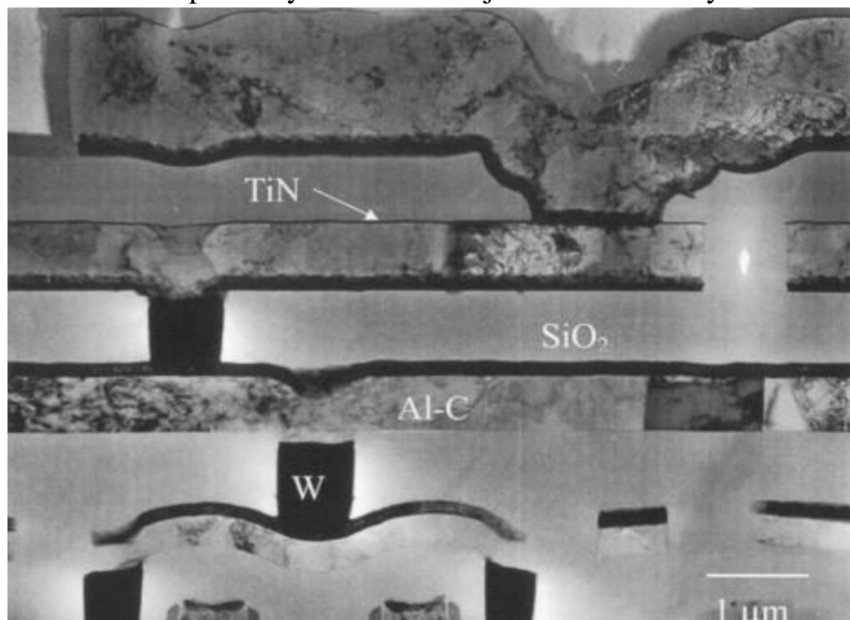


Figure 1.5: A transmission electron microscope image of a cross-section of an interconnect structure. Reliability of Interconnect Structures, Z. Suo, pp. 265324 in Volume 8: Interfacial and Nanoscale Failure (W. Gerberich, W. Yang, Editors), Comprehensive Structural Integrity (I. Milne, R. O. Ritchie, B. Karihaloo, Editorsinchief), Elsevier, Amsterdam 2003. Used under fair use, 2015.

Interconnect structures are known to have complex architectures, diverse materials, and small feature sizes. Figure 1.5 shows a transmission electron microscope image of an interconnect structure [43]. A three-dimensional network structure of conductor lines is built up on a silicon wafer containing the dielectric. These are the active devices. The conductor lines, serve as the vias. Feature sizes are as small as 100 nm. Traditional interconnect structures use aluminum as the

conductor, and silica as the dielectric. To make faster devices, the conductor must have higher conductivity, and the dielectric must have lower dielectric constant. The conductor lines at different levels are linked with copper vias.
With dense interconnect structures come reliability challenges which could typically be a result from material deposition, thermal expansion mismatch, and electron migration. The developed stress could be in the GPa range. Owing to the requirements in the type of conductors, dielectrics, or barriers, interconnect materials have dissimilar thermal expansion coefficients. On cooling from the fabrication temperature, the structures acquire stresses. Limited cross-sectional area also adds to the wear and tear. Metal atoms that diffuse in the line due to this electric current, generate arrays of successive tension where atoms deplete, and compression where atoms accumulate.

Interconnect reliability in integrated structures have been a persistent problem since 1967. The tools have been incorporated into industrial practice in material selection, process control, and failure analysis. Low dielectric constant materials have low stiffness; their effects on interconnect reliability are the focus of current studies.[4-9] However the associated failure modes can be listed as: cracking, de-bonding, ratcheting, voiding, and electron migration. These provide us the opportunities to conduct a fundamental study of the mechanical behavior of diverse materials, in integrated structures, on a small size scale.[7]

The introduction of copper and low dielectric-constant materials has given a new dimension to study cracking and de-bonding in small structures. The fundamental study will impact other major technologies. We still need to find a trade-off between what to understand, compute, and measure. The tension between the relentless trend of miniaturization and the disquieting lack of a method to design for reliability will inspire innovations for years to come.[43]

1.2.2 Memory Devices - Evolving Technology and its Reliability

In recent years, many emerging nonvolatile memory technologies are invented challenging the dominant position of flash memory. Ferroelectric memory (FeRAM), oxide resistive memory (RRAM), conductive bridge resistive memory (CBRAM), phase change memory (PCM), nano-electro-mechanical systems (NEMS) memory, and spin-transfer torque magnetic memory (STTRAM) are all intensively being investigated and developed. The local heating effect causes the phase change memory utilizes to induce the material phase transition from amorphous and crystalline states, interchangeably [11]. Thus the device resistance changes according to the material phase transition. The ferroelectric memory takes advantage of the ferroelectric phenomenon [12].

Among the emerging technologies, the resistive memory and spin-transfer torque memory [13], [14], CBRAM employs reduction-oxidation reaction to cause resistive switching, whereas STTRAM uses electron spins in the current to revolutionize the traditional magnetic memory. CBRAM and STTRAM are both based on multi-layer thin film stack structure and can be integrated in the back end of line of CMOS process. The compact cell size of both devices can be

Table 1.1- Summary of the flash memory and emerging memory technologies according to the ITRS roadmap [10]. Red, orange, and green colors mean poor, moderate, and good.

Parameter	Flash Memory	PCM	STTRAM	Resistive Memory	FeRAM	NEMS Memory
Scalability	Orange	Green	Orange	Green	Orange	Red
MLC	Green	Green	Red	Green	Red	Red
Endurance	Green	Orange	Green	Green	Green	Red
3D integration	Orange	Green	Orange	Orange	Red	Red
Fabrication cost	Green	Green	Orange	Orange	Orange	Red
Write Energy	Orange	Red	Orange	Orange	Green	Orange
Write Voltage	Red	Green	Green	Green	Green	Green

decreased to $4F^2$ in the crossbar array. Here F is the feature length defined by the lithography process which is half-pitch length for crossbar architecture. The state-of-the-art and emerging technologies are summarized in Table 1.1 according to ITRS roadmap [10].

1.3 Low-k dielectric Interconnect Structure

Current state of the art interconnect structures utilized for integrated nano-scale logic and memory devices are fabricated using copper (Cu) as the interconnect metal and low dielectric constant (i.e. "low-k") amorphous organo-silicate (a-SiOC:H) materials as the intermetal or interlayer dielectric (ILD) [7,9]. Such low-k/Cu interconnect structures present numerous thermal, mechanical, and electrical reliability challenges that limit the performance and lifetime of the integrated device. One of the primary electrical reliability challenges for low-k/Cu interconnects is time dependent dielectric breakdown (TDDB) of the low-k ILD.[8]

A typical Intel interconnect structure has been shown in Figure 1.6. The incorporation of low-k dielectric materials as interlayer dielectrics in integrated circuits has its own set of associated problems like leakage current and dielectric breakdown. There is an important need within the semiconductor industry to understand the factors that contribute to time-dependent dielectric breakdown (TDDB) and leakage mechanisms in ILD films [4]. Position of the energy bands, their relative status to the states in the electrodes, and the influence of traps within the film and its interfaces are the key factors that influence the electronic transport properties in insulating films. Several techniques of characterization are performed to on the interfacial barriers and trapping states in such films, in order to gain an understanding of the process of breakdown in ILD.

Figure 1.7 above gives an example of a typical time dependent dielectric breakdown on stressing the device continuously with a bias voltage. With these studies, it is possible to investigate the

evolution of the films under the high temperature and voltage conditions used in testing, as well as under standard usage conditions.

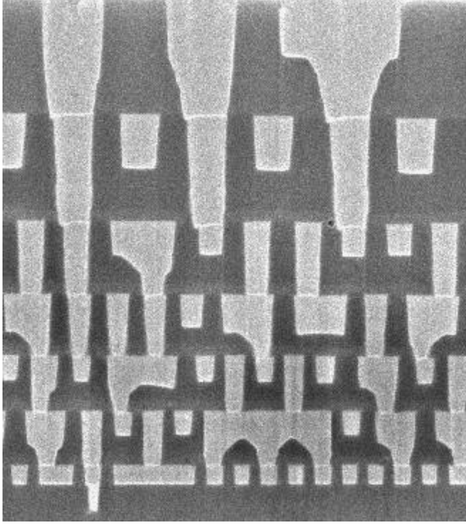


Figure: 1.6: A typical Interconnect Structure Intro to Low-k/Cu Interconnects and Time Dependent Dielectric Breakdown (TDDB) Sean W. King, Logic Technology Development, Technology Manufacturing Group, Intel Corporation, Intel Technical Lecture Series, September 2014. Used with the permission of Dr. Sean King, Intel Corporation.

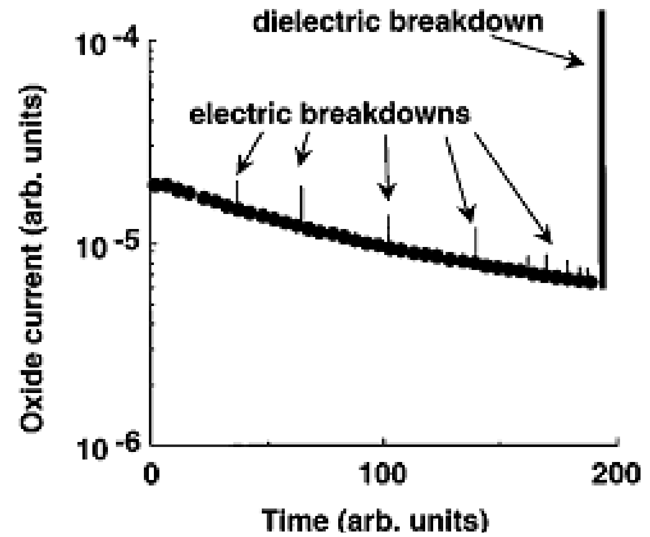


Figure 1.7: Time Dependent Dielectric Breakdown Intro to Low-k/Cu Interconnects and Time Dependent Dielectric Breakdown (TDDB) Sean W. King, Logic Technology Development, Technology Manufacturing Group, Intel Corporation, Intel Technical Lecture Series, September 2014. Used with the permission of Dr. Sean King, Intel Corporation.

1.4 Resistive Memory

In this section, the nano-crossbar resistive switch will be one of the major topic for discussion. Its evolution, different mechanisms involved in its operation and its applications will be studied. Scientists have postulated various mechanisms to explain the resistive switching behavior. It is alleged that metal ion migration and the subsequent formation and rupture of the metal conductive filament render the memory aspect to this otherwise simple MIM structure. It has also been observed that formation of conduction path via oxygen ion transport takes place in an altogether different stress conditions. The need to understand the switching mechanism when the conventional switch structure is modified during fabrication so as to affect ion formation and thereby the resulting quality of the filament has been investigated.

1.4.1 Definition

A resistive switch also called resistive random access memory or precisely RRAM/ReRAM is one of the most sorted out research topics in the field of non-volatile memory development. It depends upon nano-ionic based filament formation through redox reactions which are capable of developing a stable pathway to carry information. These reactions to induce the resistance switching phenomenon. The basic structure of a resistive switch is a MIM structure – Metal/Insulator/Metal structure. Oxides, higher chalco-genides or ionic solids are most commonly

used as the insulator rendering it typically nonconductive under normal conditions. [2]. However, they exhibit resistive memory behavior under some specially manipulated bias conditions. Occasionally they are known to exhibit resistive switching behavior and are impressive because of simple structure, ease of fabrication and excellent compatibility with the complementary metal oxide semiconductor backend technology.

1.4.2 Modes of Operation

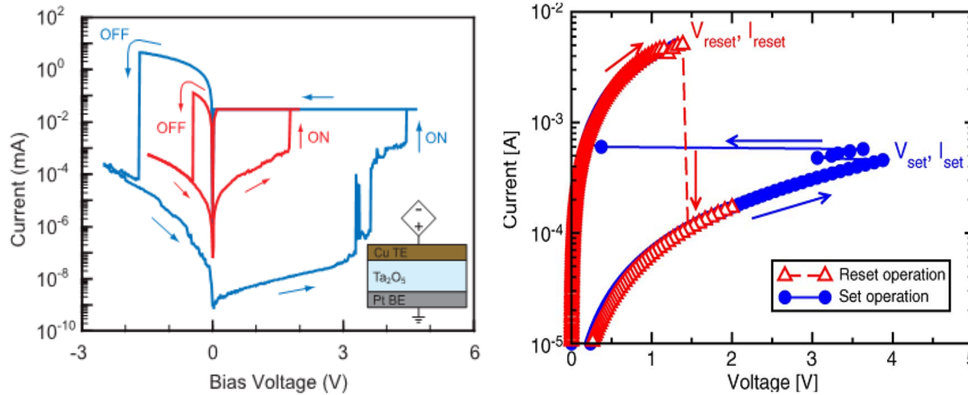


Figure 1.8 : Bipolar and Unipolar modes of operations. J. E. Brewer and M. Gill, Nonvolatile memory technologies with emphasis on flash: a comprehensive guide to understanding and using NVM devices, John Wiley & Sons, Hoboken, 2008. Used under fair use, 2015.

A resistive switch is essentially a two terminal device that transitions between a high resistive state (HRS) and a low resistive state (LRS) by the application of a SET and RESET linear voltage sweep. Conventionally both these states are expected to be reliable, stable and nonvolatile. There are two modes of operation of the resistive switch, unipolar mode and the bipolar mode. In the bipolar mode the resistive switching takes place in different quadrants of the I-V characteristic In other words, it changes from HRS to LRS on the application of positive voltage, then it will change from LRS to HRS on the application of negative voltage. In the unipolar mode the resistive switching is dependent on the magnitude of the applied voltage and not the polarity that is it changes from HRS to LRS and vice-versa in the same quadrant. Figure 1.8 shows the two basic operation modes i.e. bipolar and unipolar modes operation of the resistive memory cells [32] [33].

1.4.3 Important Terminologies

Resistive switches has their distinct set of terminologies which will be used through various sections of this thesis. They have been defined below.

Forming Voltage

This voltage is denoted by $V_{FORM.}$ Forming is the phenomena of the formation of the conductive filament in the electrolyte for the first time in a fresh/untested device. Forming voltages are typically higher and are proportional to the thickness of the dielectric. The interfacial redox reactions allows the ions to migrate from one electrode and pile up on the other electrode, thus leading to the “formation” of the conductive pathway.[2]

Set Voltage

This voltage is denoted by VSET. SET is the phenomena of building back the conductive filament bridge after it has been disintegrated at least once either by the Joule's heating or by electrochemical migration of ions. Set voltages are logically lower than forming voltage, since this time the bridge is being "re-formed" only partially.

SET and FORM leads the device into the low resistive state (L.R.S) also called the ON state. The resistance of the switch during this state is also called as the ON resistance or the R_{ON}.

Reset Voltage

This Voltage is denoted by $V_{RESET.}$ RESET is the phenomena of rupturing or breaking of the conductive filament bridge either by the ion migration (bipolar mode) or thermal dissolution caused by Joule's heating (unipolar mode). As indicated in Figure 1.9, the rupture takes place at the apex of the conical conductive filament. It is postulated the resistance being the highest at this locations, leads to an hugely elevated temperature leading to the disintegration of the bridge. This also explains why the bridge ruptures partially. Reset leads the device into the high resistive state (H.R.S) or the OFF state. The resistance of the switch during the reset state is also called as R_{OFF}.

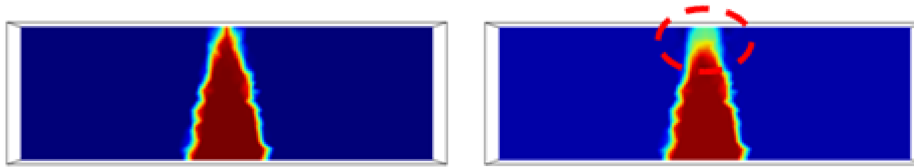


Figure 1.9: Conductive filament rupture by thermal dissolution

It is assumed that when the migrating ions when topped by the inter electrode Pt, on being stressed with a positive voltage sweep, these ions start piling on top of each other. This leads to the formation of the electrode. The on- resistance is thus calculated considering the shape of the filament formed.

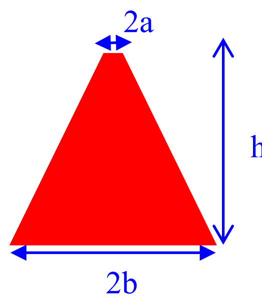


Figure 1.10: Conductive Filament Model for calculation of R_{ON}

With the assumed dimensions given in Figure 1.10, the on-resistance can be calculated as:

$$R = \rho \frac{h}{\pi ab}$$

Compliance Current

During the form or set operation, a limiting current called the compliance current is applied to the resistive switching circuit from the external circuit so as to prevent the permanent damage of the device by the flow of excess current and thereby excessive heat into the circuit. This current is denoted by I_{CC}. The normal range of compliance current used in the present work is 0. 1 mA which allows the device operation with any damage. For reset operation, ideally no compliance current must be used. However, in order to ensure relative resistive switching, a compliance current as high as 0.1 A is used.

Resistance Ratio

The ratio of the R_{OFF}/R_{ON} is termed as the resistance ratio of the resistive switch. Typically R_{OFF}/R_{ON} ratios > 10 are required for cost effective RRAM chips [2].

Endurance

Endurance of a resistive switch denotes the maximum number of times the cell can be set and reset until the ON or OFF state falls out of the predefined acceptance window [2].

Retention

Retention is the ability of the resistive memory cell to keep the stored information if the cell is not powered. [2]

1.4.4 Device Structure

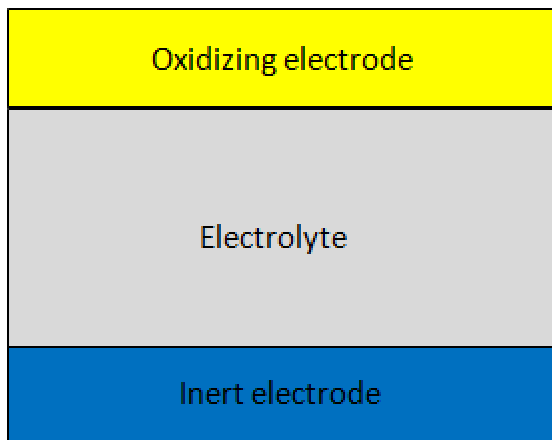


Figure 1.11: Stack structure of a CBRAM

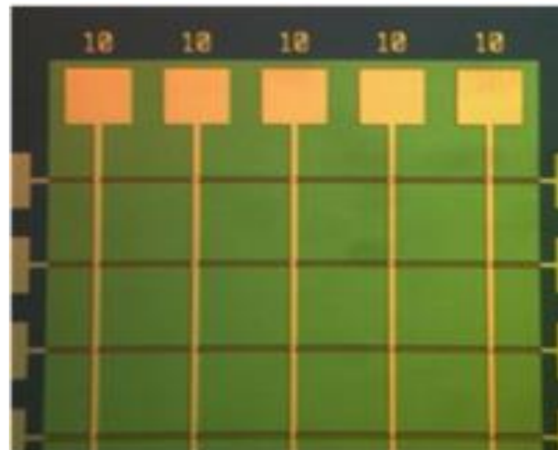


Figure 1.12: Optical micrograph of the crossbar architecture

Conductive Bridge RAM, a subset of RRAM is being considered as the future of nonvolatile memory devices due to its extremely low power consumption and higher scalability, high switching speed and good retention and endurance properties [16]. The basic structure of a conductive bridge RAM is given in Figure 1.11. It typically a two terminal device have a combination of: active metal electrode/solid electrolyte/inert metal electrode. The active metal can be any oxidizing metal like Cu or Ag which is have a high activation energy, thus yielding ions readily. Ni, though not widely reported is known to serve as an active metal.[18] For the

interlayer dielectric, a large array of material is available for the purpose namely; Cu_2S, SiO_2, GeS, Ta_2O_5, AgGeSe, TaSiO, HfO_2., which allow the transport of ions, with greater mobility as compared to regular solid state materials [17]. For the inert electrode, metals like Pt, Ir or W are generally used. The simplest schematic of a nano-crossbar resistive switch as seen under an optical microscope is as shown in Figure 1.12. The top and the bottom electrode lines run perpendicular to each other.

Basic Operation

The switching mechanism in a CBRAM is mostly believed to be based on the formation and rupture of a conductive filament either due to migration of metal ions (from the active electrode) through the solid electrolyte towards the cathode (thereby forming a metal filament between the anode and the cathode) [19] or the migration of oxygen ions towards the active electrode (formation of conductive path by the means of an oxygen vacancy filament) [20]. When a positive bias is applied, the active electrode (anode) gets oxidized and the fast metal ions begin drifting through the dielectric only to be stopped by the inert/bottom electrode (cathode) under the electric field and get reduced thereby forming the conductive metal filament there. This conductive filament keeps growing vertically from the cathode until it makes a contact with the anode. This is like a self-accelerated mechanism. When the anode and cathode are connected by the complete the ionic filament, a conductive path is formed thus leading the device to a low resistance state. A pictorial representation of the bridge formation has been shown in Figure 1.13.

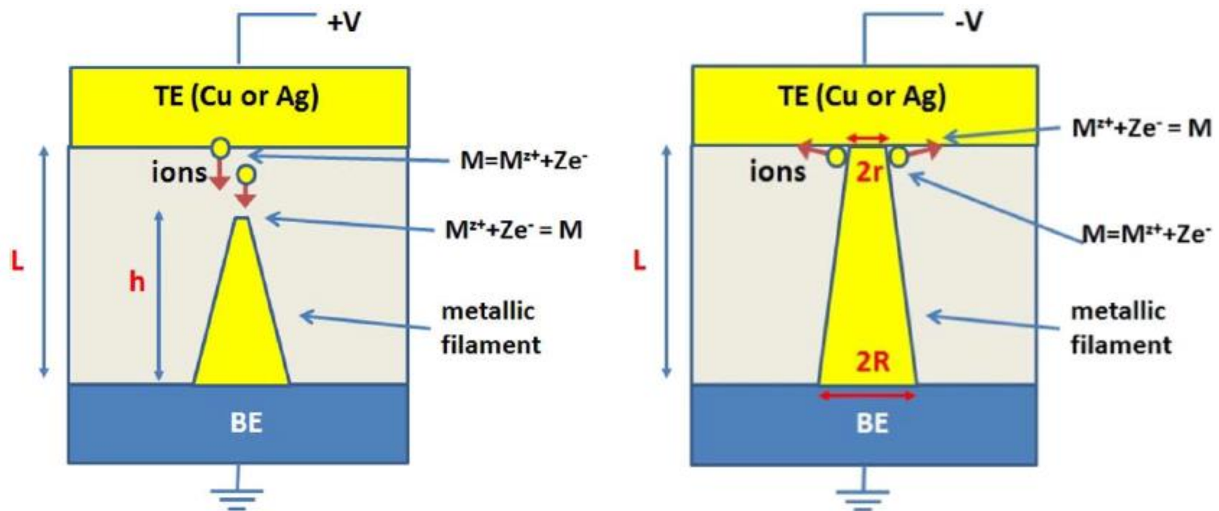


Figure 1.13: Schematic of the switching process in CBRAM cell. (a) CF grows vertically and (b) CF laterally dissolves. Shimeng Yu and H.S. Philip Wong, "Compact Modeling of Conducting Bridge RandomAccess Memory (CBRAM)," IEEE Transactions on Electron devices, vol. 58, no. 5, pp. 13521360, May 2011. Used under fair use, 2015.

Again the oxygen vacancy [O] conductive filament can also be established in TaO_x by applying a negative forming voltage on the Cu electrode and therefore the same device conforms to RRAM functionality. According to what has been observed so far, the Cu- and [O]- based switching can be well separated by the polarity and magnitude of the set voltages [26]. During the RRAM

functionality which is exhibited under negative bias voltages, the following electrode-reduction reaction occurs in the TaO_x layer:

$$TaO_x + 2e^- \rightarrow TaO_{x-1} + O^{2-} \quad (1)$$

The O^{2-} ions migrate from the Cu electrode to the Pt electrode under the negative bias voltages. The vacancies [O] left behind by O^{2-} ions form conductive filaments and the resistive state changes. Figure 1.14 illustrates the switching process that is likely to take place due to vacancy migration across the electrode. As mentioned earlier, the process is very stochastic. A deeper study has been

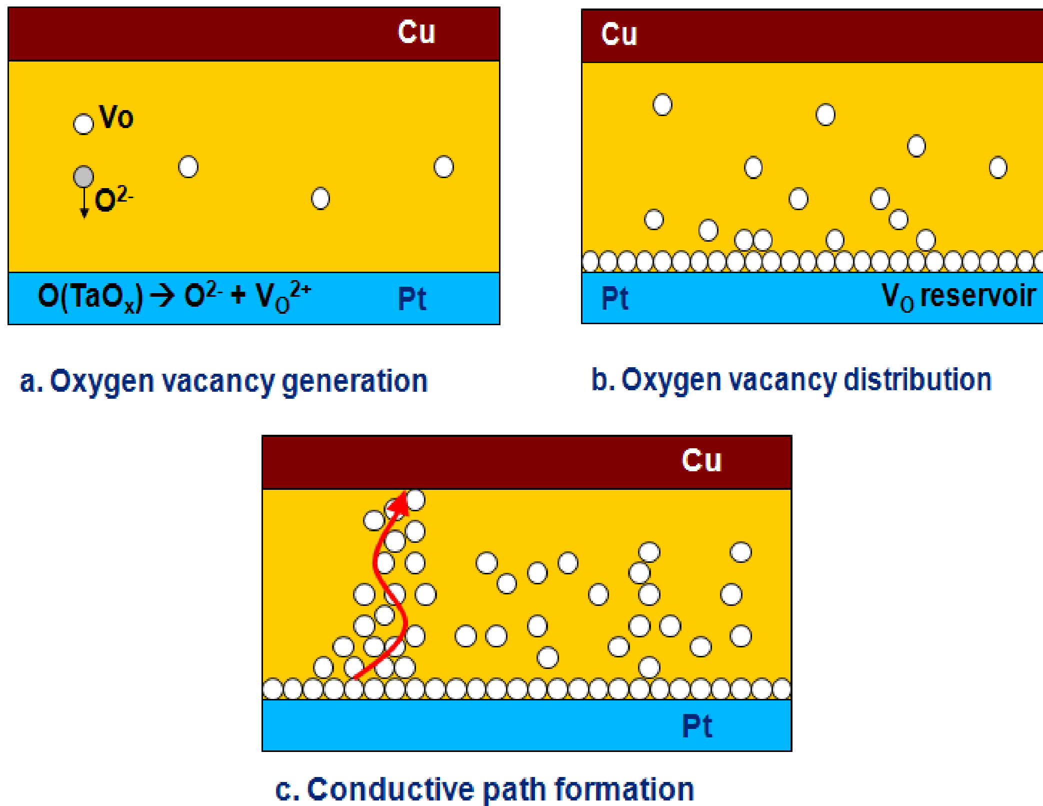


Figure 1.14: Switching process in CBRAM cell due to [O] vacancy filament

performed in Chapter 3 which talk about the building mechanism of the nanofilament via oxygen vacancies.

1.4.5 Pt/TaO_x/Cu Device

1.4.5.1 Choice of Material

Resistive switching property is displayed by a wide range of material. Since the major focus here is on the purpose of putting the resistive switches to use in the nonvolatile memory area, on optimum range of set voltage are required.

Tantalum Pentaoxide (Tantalum Oxide)

The reasons to choose Ta_2O_5 are given as follows:

- It was observed that the Ta_2O_5 switch has threshold voltages above the operating voltages of the CMOS devices and hence they are the most appropriate to be used in the nonvolatile switching [24] [25].
- Ta_2O_5 as the solid electrolyte here is that it has smaller ionic diffusion coefficient for Cu^+ ions, and thus the threshold voltage for set is comparatively larger than other electrolytes and hence it has better retention properties.

However in the PVD or e-beam evaporation, tantalum oxide is obtained in the form of TaO_X. TaO_x has a much higher endurance that is 10^{10} cycles as compared to 10^4 of Ta_2O_5. This phenomenon turned out to be a boon in disguise. Figure 1.15 shows the two different types of conductive filaments inside a single Pt/TaO_x/Cu switch. A thickness of 32nm has been maintained for this thesis through deposition.

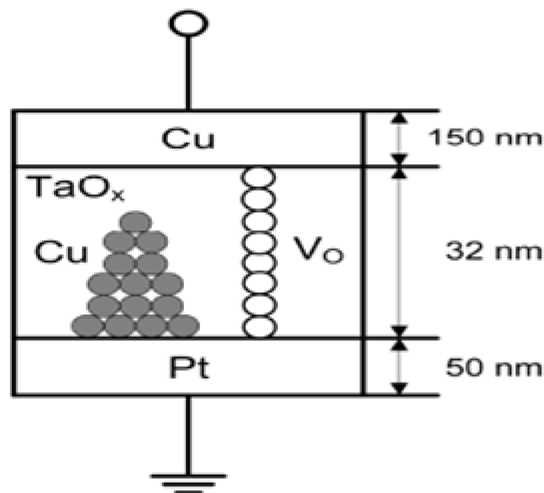


Figure 1.15: Structure of a single switch

Copper

Copper has been chosen over other metal like Ag or Ni, for the following reasons:

- Higher activation energy
- Lower cost

A thickness of 150nm has been deposited in order to ensure proper probing during characterization.

Platinum

Platinum has been chosen over other metals like Ru or W, for the following reasons:

- Reasonable melting point thereby avoiding unnecessary heating up of substrate.
- Inert and noble metal.
- Smooth deposition is possible through PVD

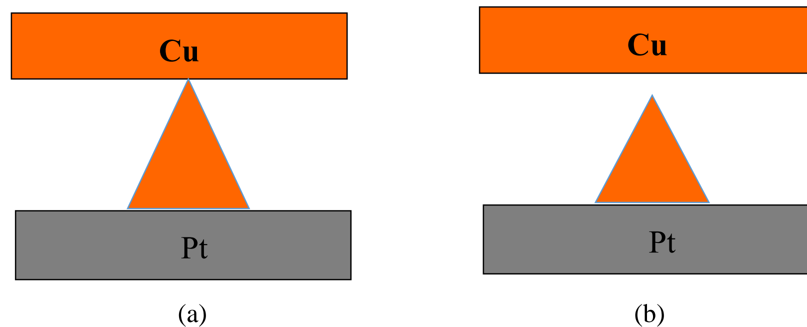
The thickness of the Pt lines deposited was kept consistent at 60 nm for all the devices. However a very thin layer of Ti (12nm) is deposited prior to Pt deposition, which provides a good adhesion for Pt with thermally deposited silicon oxide.

1.4.5.2 Switching mechanism

The Pt/TaO_x/Cu resistive devices are typically set and reset by applying positive and negative voltages to the Cu electrode while the Pt inert electrode is kept grounded. A Cu or oxygen vacancy conductive filament (CF) forms and ruptures during the set and reset operations, and the device works as a CBRAM in terms of the conduction mechanism. In this research, the Ta_2O_5 film is considered to be oxygen deficient (TaO_x) due to its e-beam deposition process. A parallel plate capacitor forms when the high-k dielectric TaO_x is sandwiched between micron-sized metal electrodes.

1.4.5.3. Structure of a Cu Filament

It is believed that the Cu filament evolution has in essence 4 stages i.e. vertical growth, lateral growth, lateral dissolution and vertical dissolution based resulting from electric field driven ion migration. Just before the SET, the electric field is concentrated across the tip and as a result drives the ion migration vertically while before a RESET operation there is a lateral electric field at the top of the filament which drives the ion migration laterally [7]. Based on this theory the structure of the conductive filament during the set and reset process should have a structure as given by Figure 1.16.



(a) (b)

Figure 1.16: Resistive switch (a) ON state and (b) OFF

1.4.5.4 Electrical Characterization

For the purpose of electrical characterization, the Keithley 4200 –SCS (Semiconductor Characterization System) has been used at various temperatures. However for Cu/TaOx/Pt devices, characterization has been done only at room temperatures. This system allows a complete characterization of devices, materials and semiconductor processes.

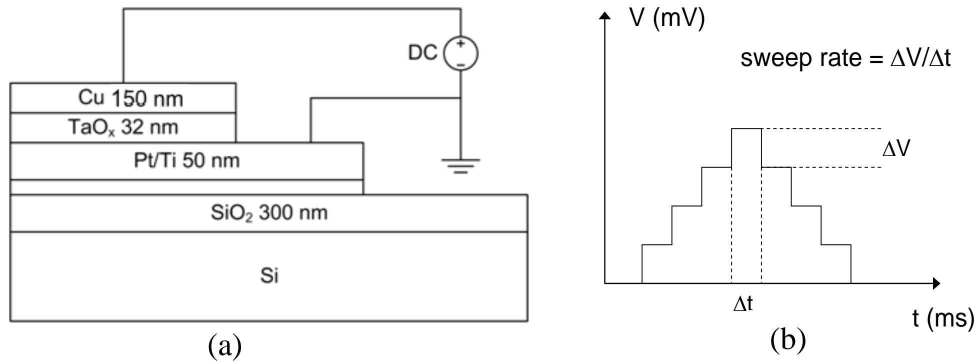


Figure 1.17: Experimental Set –Up (a) Cross sectional view of Cu/TaO_x/Pt nonvolatile memory devices (b) Schematic illustration of voltage sweeping mode in DC characterization

The two most important parameters of the characterization circuit are the sweep rate and compliance current. Sweep rate is defined as the rate of change of voltage with time. The devices are stressed with a linear ramp voltage having a natural interval time of 50ms per step size. In other words if the devices has a sweep rate of 0.01V step size, it essentially means that the sweep rate is 0.2V/s. Typically, a two-terminal memristor is formed at each cross point of a crossbar architecture as shown in the optical micrograph seen in Fig.1.12. The bottom Pt electrode has been deposited by evaporation and patterned by lift-off on a thermally oxidized Si wafer. The top Cu electrode lines were processed in the same way but patterned perpendicularly to the bottom Pt lines. The width of the metal lines varies between 1μm and 35μm. The experimental set-up is represented in Fig 1.17(a) and a dual sweep rate to trace the current with respect to voltage as given in Figure 1.17 (b)

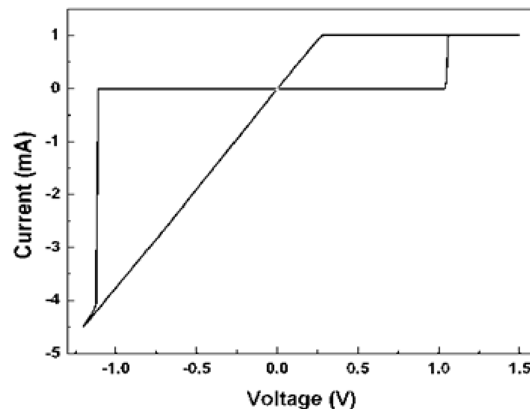


Figure 1.18: The bipolar switching characteristic of a single Cu/TaO_x/Pt cell.

When a positive voltage is applied to the active electrode, Cu cations dissolve in the solid electrolyte and migrate through it. Cu cations are electrochemically reduced on the Pt cathode. As more Cu atoms accumulate, a nanoscale metalic filament (CF) forms a conductive path between two electrodes. The state transition from HRS to LRS is called SET process characterized by a critical voltage V_{set}. For a fresh device cell, a significantly higher positive voltage is needed for the SET process, which is known as forming voltage. For our devices the forming voltage is in the range of 4-6V. A high current passing through the filament can rupture the bridge and restore HRS.

This is called RESET process of the device characterized by a critical voltage V_{reset}. Fig.1.18 shows a typical behavior of one switching cycle of an individual switching device. The voltage is ramped from 0 V on the positive voltage axis. As long as the switch is in the OFF state the current is very small. When the voltage reaches a critical voltage of V_{set} a conductive bridge is established and the current jumps abruptly being only limited by compliance current I_{cc} lest the device be damaged. Then the voltage is swept back and, for voltages sufficiently close to zero, an ohmic behavior is observed until a negative voltage V_{reset} is reached when the CF is ruptured and the current collapses to a small value.

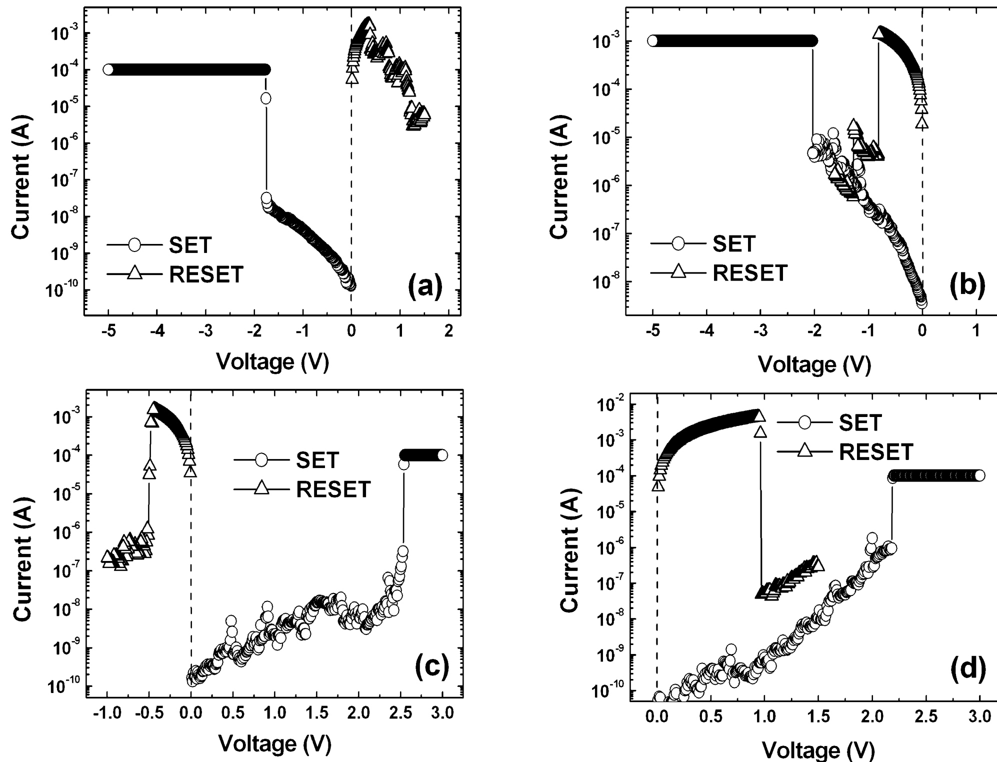


Figure 1.19. I-V characteristics of bipolar and unipolar switching. (a) Bipolar switching of V_O CF. (b) Unipolar switching of V_O CF. (c) Bipolar switching of Cu CF. (d) Unipolar switching of Cu CF. Tong Liu, Mohini Verma, Yuhong Kang and Marius K. Orlowski, "Coexistence of Bipolar and Unipolar Switching of Cu and Oxygen Vacancy Nanofilaments in Cu/TaOx/Pt Resistive Devices," ECS Solid State Lett. 2012, vol.1, issue 1, pp q11q13. Used under fair use, 2015.

A Cu/TaO_x/Pt device can be switched between the HRS and LRS based on the formation and rupture of two types of nanofilaments in the same device: Cu and oxygen vacancy conductive bridges based on the polarity of switching voltage in both bipolar and unipolar regimes [26]. In the next chapter we will be discussing at length in the mechanisms involved in the formation and rupture of the different kinds of conductive bridge. Figure 1.19 (a) and (b) show unipolar switching and bipolar switching by the V_O filament and 1.19 (c) and (d) show unipolar switching and bipolar switching by the Cu filament respectively. We will discuss more on this in the next section.

1.4.5.5 Cu and Oxygen Vacancy Conductive Nanofilaments

Two mechanisms are considered to explain the CF rupture: the electrochemical dissolution and Joule heating. Due to the ohmic behavior of a metallic CF, these two effects cannot be separately investigated in the RESET process. Once the metallic nanofilament connects the two electrodes, it will grow laterally to increase the diameter and reduce the resistance. This can be controlled by application of higher I_{CC}. The dependence of R_{ON} on the compliance current is shown in Figure 1.20(a). The slope of the plot was found out to be the minimum possible value of SET voltage. Since R_{ON} depends on I_{CC}, multi-bit storage in a single device can be implemented by controlling the cell LRS by different programming current. The multilevel switching based on R_{ON} change has been demonstrated on various types of resistive memory devices [31,34,35]. The retention of Cu CF at room temperature is shown in Figure 1.20(b).

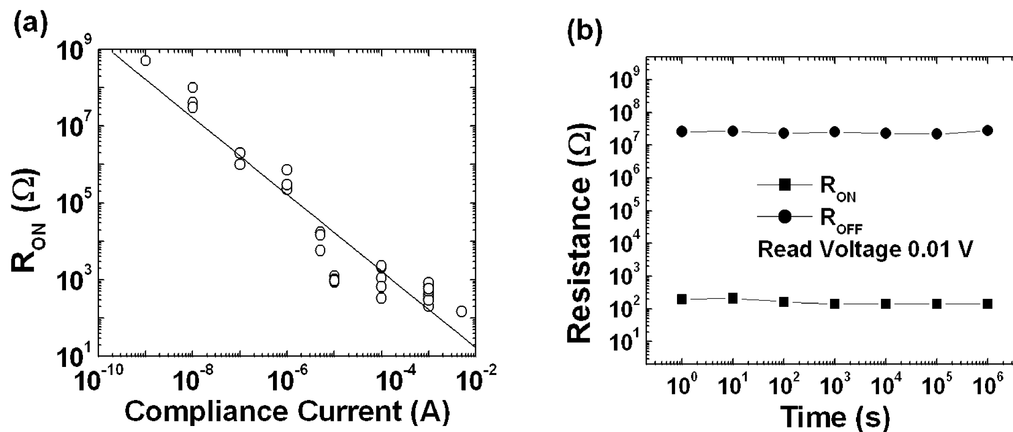


Figure 1.20: (a) Dependence of R_{ON} of individual resistive switches as a function of the compliance current applied to the cells during the set operation. (b) Retention of Cu CF at room temperature. The Cu CF was formed with compliance current of 1 mA. Tong Liu, Yuhong Kang, Mohini Verma, and Marius Orlowski, "Novel highly Nonlinear Memristive Circuits for Neural Networks," WCCI 2012 IEEE World Congress on Computational Intelligence, June, 1015, 2012 Brisbane, Australia. Used under fair use, 2015.

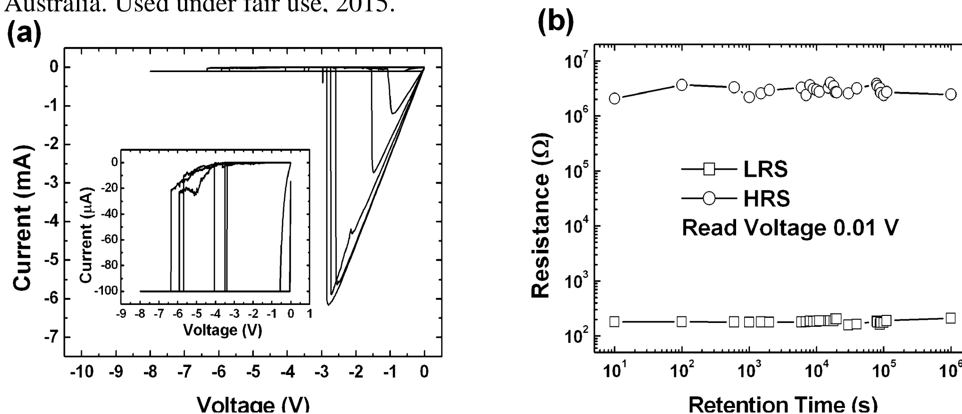


Figure 1.21. (a) Repeated unipolar switching characteristics for V_O CF in a Cu/TaOx/Pt device. (b) Retention property of the V_O CF at 25 °C. The ON/OFF resistance ratio is 10^4. The LRS and HRS stays nearly constant up to 10^6 seconds. Tong Liu, Mohini Verma, Yuhong Kang and Marius K. Orlowski, "Coexistence of Bipolar and Unipolar Switching of Cu and Oxygen Vacancy Nanofilaments in Cu/TaOx/Pt Resistive Devices," ECS Solid State Lett. 2012, vol.1, issue 1, pp q11q13. Used under fair use, 2015.

Repeated unipolar switching characteristics of the V_O nanofilament are shown in Figure 1.21(a) for V_O CF in a single $Cu/TaO_x/Pt$ device. The bias voltage ramps along the negative axis for set

and reset operations. The transition between HRS and LRS is more or less abrupt. Significantly higher forming voltages, V_{FORM}, are apparently necessary for the V_O CF formation in fresh devices. The retention property of the two states has been characterized at room temperature. The read voltage of 0.01 V is used to measure R_{ON} and R_{OFF}. Figure 1.21(b) shows very uniform LRS and HRS distribution of a single Cu/TaO_x/Pt device for V_O CF with the retention time up to 10^6 s. The LRS is about 190 Ω and HRS is about 2.5 MΩ respectively, that is, an OFF/ON ratio above 10^4.

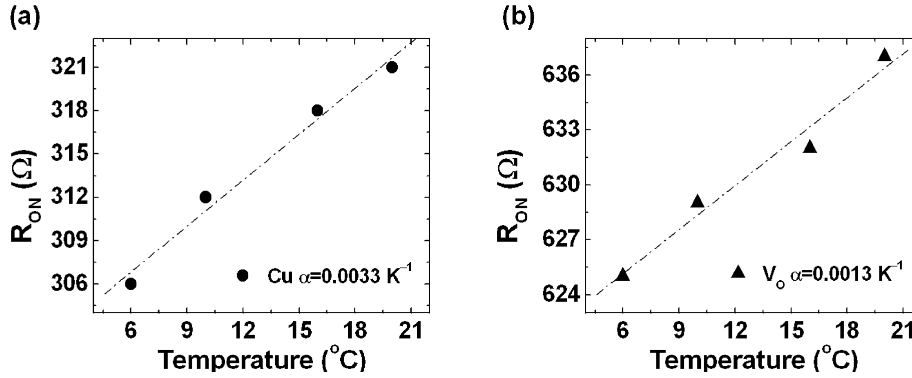


Figure 1.22: R_{ON} temperature coefficient α of (a) Cu CF and (b) V_O CF. Tong Liu, Mohini Verma, Yuhong Kang and Marius K. Orlowski, "Coexistence of Bipolar and Unipolar Switching of Cu and Oxygen Vacancy Nanofilaments in Cu/TaOx/Pt Resistive Devices," ECS Solid State Lett. 2012, vol.1, issue 1, pp q11q13. Used under fair use, 2015.

R_{OFF} is measured right after the rupture of the respective CF.

The resistances are measured from 0 °C to 20 °C for low R_{ON} values of two kinds of filaments, as shown in Figure 1.22. The temperature coefficient α is 0.0033 K^{-1} for Cu CF, whereas the value is 0.0013 K^{-1} for V_O CF. The measurement results are quite close to the reported data from NiO-based ReRAM devices and Cu CF based CBRAM [36], [37].

As the coefficient measured for the Cu nanofilament is very close to the bulk value of Cu, it reinstates our belief that the nanofilament is built out of migrating Cu^+ ions. The positive temperature coefficient of V_O CF implies that the filament is metallic instead of semiconducting for the low R_{ON} value. The difference between the two coefficients underscores that two different conduction mechanisms are at work.

The bipolar switching cycles have been repeated on Cu/TaO_x/Pt devices. Figure 1.23(a) and 1.24(b) show the statistical V_{SET} and V_{RESET} distributions of a single Cu/TaO_x/Pt device with Cu and V_O CFs. In Figure 1.23(b), the range of V_{SET} much wider than V_{RESET}. This wide range could be attributed to the non-uniform oxygen vacancy structures in the TaO_x layer of different devices. Figure 1.23 (c) and 1.23 (d) show the statistical R_{ON} and R_{OFF} distributions of Cu/TaO_x/Pt devices with Cu and V_O CFs. The R_{OFF}/R_{ON} ratios are above 10^4.

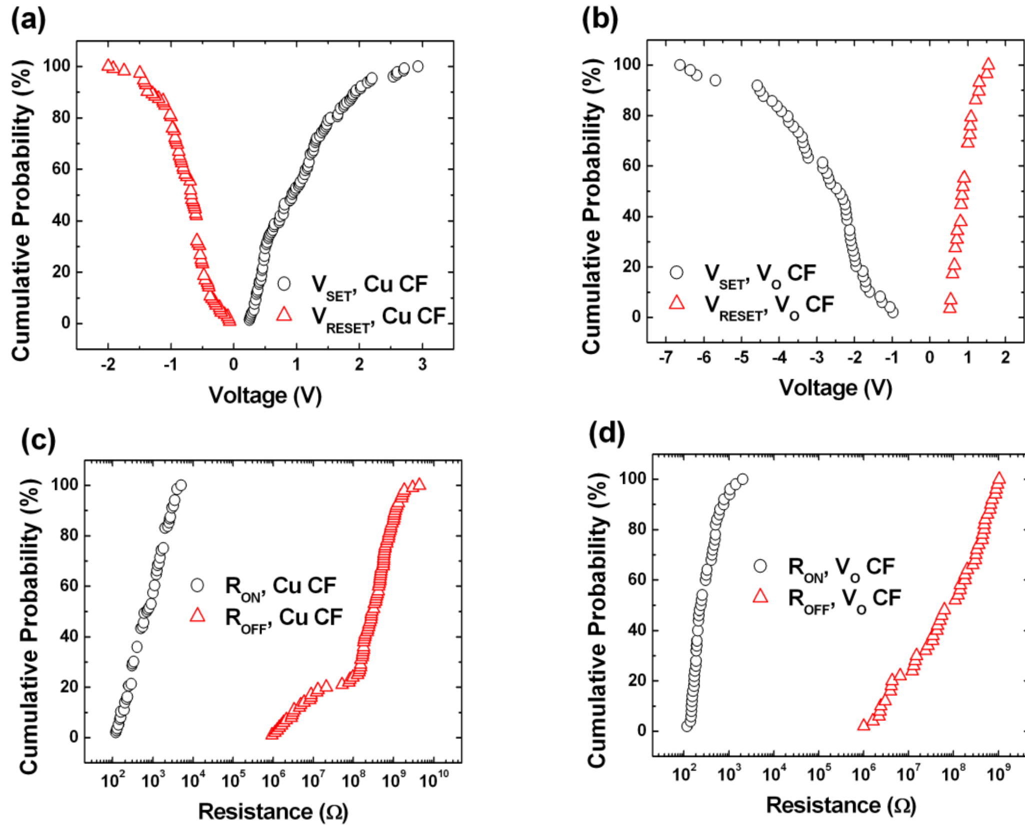


Figure 1.23. (a) V_{SET} and V_{RESET} distributions of Cu/TaO_x/Pt devices. The SET voltage is positive for Cu CFs. (b) V_{SET} and V_{RESET} distributions of Cu/TaO_x/Pt devices. The SET voltage is negative for V_O CFs. (c) R_{ON} and R_{OFF} distributions of Cu CFs in Cu/TaO_x/Pt devices. The read voltage is 0.1 V for R_{OFF}. (d) R_{ON} and R_{OFF} distributions of V_O CFs. The device sizes are 10 μm, 15 μm, 20 μm, 25 μm, 30 μm, and 35 μm. Y. Kang, T. Liu, and M. K. Orlowski, "Pulse operation of a floating electrode memristive device," IEEE Trans. Electron Devices, vol. 60, no. 4, pp. 14761479, Apr. 2013. Used under fair use, 2015.

The ranges of RESET voltages for Cu CFs and V_O CFs are comparable. However, the ranges for the SET voltages can be very different. This may indicate that O^{2-} has a higher potential barrier than Cu^+ for the redox reaction on the electrodes. The work function difference of anode and cathode contributes to the asymmetric distribution of SET voltages [38]. Pt has a higher work function (5.35 eV) than Cu (4.35 eV), resulting in a built-in voltage of about 1 V across the dielectric. When the negative voltage is applied to Cu electrode, this voltage difference has to be overcome before an effective voltage drops on the oxide layer. Thus the built-in voltage shifts the effective voltages asymmetrically for Cu and V_O CFs formation. The main difference in the SET voltages is, however, due to the difference of mobility of Cu^+ and O^{2-}, requiring higher fields for O^{2-} than for Cu^+ migration. Therefore, the SET voltage for Cu CF is significant lower than that of V_O CF.[31]

Figure 1.24(a) shows the statistical V_{SET} and V_{RESET} distributions for the V_O CF conduction. The V_{RESET} distributions show narrow and symmetrical shape, indicating the RESET mechanism is voltage polarity independent requiring the same magnitude of reset current. This shows that the rupturing of the V_O filament is mainly thermally driven by the local Joule heating. Figure 1.24(b)

shows the SET voltages of Cu and V_O CFs. The ranges of reset voltages are quite close (0 to ±2 V) for the Cu CFs and V_O CFs of Cu/TaO_x/Pt devices.

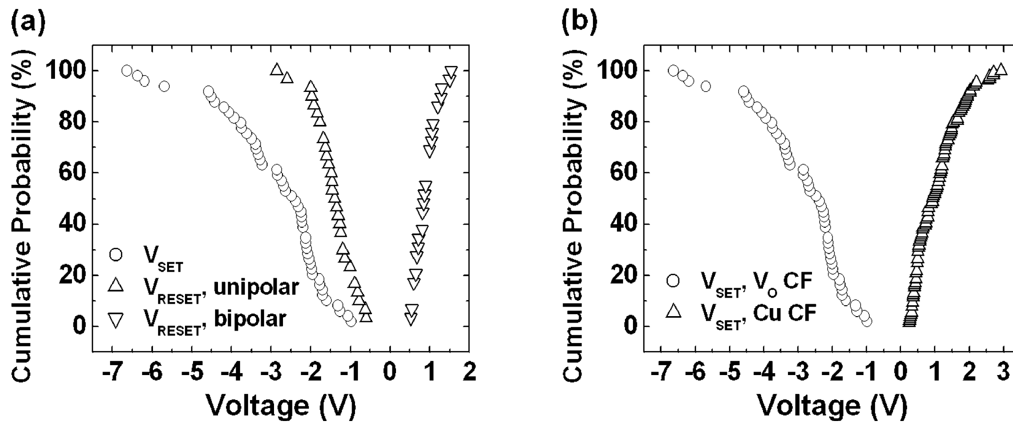


Figure 1.24. (a) V_{SET} and V_{RESET} distributions of Cu/TaOx/Pt devices with V_O CFs. Both positive and negative reset voltages can be used to rupture the conductive filaments. (b) Comparison of set voltages of Cu and V_O CFs. The V_O CF needs higher V_{SET} than the Cu CF. Tong Liu, Mohini Verma, Yuhong Kang and Marius K. Orlowski, "Coexistence of Bipolar and Unipolar Switching of Cu and Oxygen Vacancy Nanofilaments in Cu/TaOx/Pt Resistive Devices," ECS Solid State Lett. 2012, vol.1, issue 1, pp q11q13. Used under fair use, 2015.

The large variation of V_{SET} and V_{RESET} poses a serious challenge for this kind of memory device. The wide distribution of V_{SET} and V_{RESET} may be narrowed down by engineering the mechanism of bridge formation. A more practical approach has been taken based on this problem statement in the latter half of the report.

Chapter 2: Fabrication of Resistive Switching Cells

This chapter can be divided into fabrication of two different devices. The Cu/TaO_x/Pt switch is one of conductive bridge random access memory (CBRAM) devices. It also belongs to the generic concept of resistive memory which is based on redox reaction of the two metal electrodes. Therefore it is also known as electrochemical metallization memory (ECM), atomic switch, or programmable metallization cell (PMC) [1][6]. Under high electric field, Cu ions dissolve and migrate in the TaO_x layer. These cations are stopped by the inert Pt electrode and accumulate to form a Cu nanofilament, or nanobridge. When the filament connects Cu and Pt electrodes, the memory state of the device switches from high resistance to low resistance.

The other device fabricated is a MIM structure. Current state of the art interconnect structures utilized for integrated nano-scale logic and memory devices are fabricated using copper (Cu) as the interconnect metal and low dielectric constant (i.e. “low-k”) amorphous organo-silicate (a-SiOC:H) materials as the intermetallic or interlayer (ILD) dielectric. Such low-k/Cu interconnect structures present numerous thermal, mechanical, and electrical reliability challenges that limit the performance and lifetime of the integrated device. One of the primary electrical reliability challenges for low-k/Cu interconnects is time dependent dielectric breakdown (TDDB) of the low-k ILD [9].

2.1 Introduction

After years of development, the Cu interconnection is finally compatible with the Back-End-Of-Line (BEOL) of Si CMOS process. Therefore Cu is an ideal low cost material for the anode of resistive memory embedded in Si integrated circuit. Various oxides and chalcogenides are intensively being explored for the solid electrolyte of Cu ions. One of the important criteria is the electrolyte material must be also compatible to Si CMOS technology. Since resistive memory is embedded in BEOL, the oxide is the better material solution for the insulating purpose. Exotics generally do not diffuse out from oxide materials and there is less opportunity to contaminate the CMOS process. [28]

The other part is basically an attempt to reduce parasitic capacitance by introducing low-k dielectric instead of regular oxide as an ILD. Unlike the previous part, this ILD was deposited by using chemical vapor deposition processes. This ensured a much more even spread of the material on the wafer.

The parasitic capacitance may generate transient charging current if the voltage slew rate is very high. However, in the DC characterization scheme, the bias voltage is slowly ramped up from 0 V to V_{SET}. The voltage sweep rate (dV/dt) is less than 2 V/s. The complete characterization process is quasi-static so that the transient current is minimized for our large area devices.

2.2 Fabrication Processes

2.2.1 Test Structures

All the devices mentioned in the previous sections were fabricated on two types of silicon wafers. Resistive switches were developed on 4 inch diameter silicon wafers in a crossbar array on a thermally oxidized Si wafer. Whereas the Intel interconnect devices were built on 2”×2” silicon wafer. The metal electrodes and the solid state electrolyte were deposited by e-beam evaporation and were patterned by lift-off technology. The various devices fabricated during the course of this current work are describes below with the exact thickness of each layer.

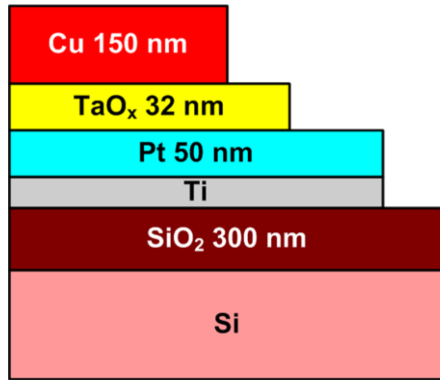


Figure 2.1. Schematic layer structure of the cross section of Cu/TaO_x/Pt resistive memory device.

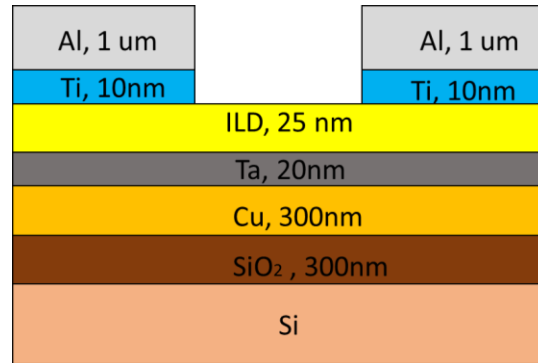


Figure 2.2. Schematic layer structure of the cross section of low-k interconnect structure.

The cross-section view of Cu/TaO_x/Pt device and low-k dielectric interconnect structure are shown in Figure 2.1 and 2.2 respectively. The resistive switches have a crossbar architecture which can achieve the minimum footprint. The Cu anodes and Pt cathodes are perpendicular to each other and each cross point is a device cell since they have a blanket layer of dielectric in between. Special pads are provided to make necessary electrical connection.

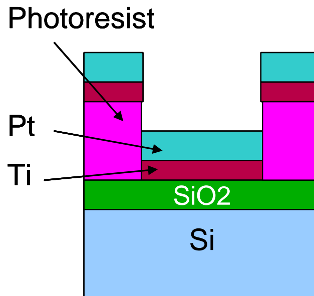
Whereas the interconnected structure bears an island architecture. The top electrode Al/Ta forms island drops of material on blanket layers of lower electrode and dielectric. Every island is capable to form a device. The common factor lies in the electrical characterization of the two devices. The equivalent circuit of the device stack is one resistor in parallel with one parasitic capacitor.

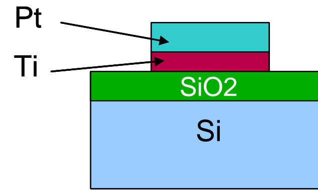
2.2.2 Process Flow for the MIM device

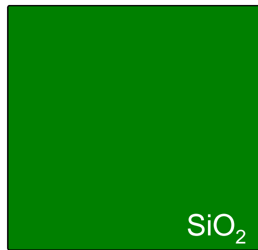
A process flow was designed by the no of utilized material layers. Since the resistive switches have three layers of material to complete the entire structure, the same process flow is repeated three times with different prerequisites and pre-conditions.

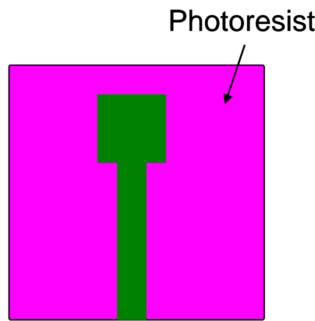
In the sections that follow, a detailed review of the process flow as well the various optimizations applied to each of the process steps for the different devices will be discussed. All the devices have been fabricated on Si substrates having thermally grown oxide to improve adhesion. The fabrication process flow is shown in Figure 2.3 for each layer a Cu/TaO_x/Pt device. The process,

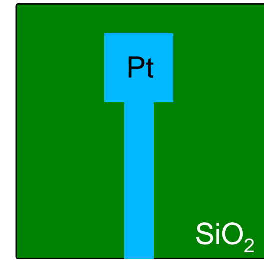
therefore, is the same for the interconnect device too. The masks used for photolithography are however different in the case of the two devices. This chapter will discuss the fabrication procedures of resistive switches at length.

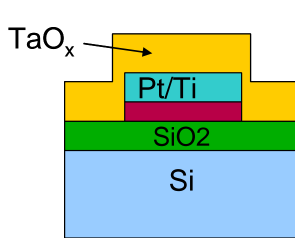


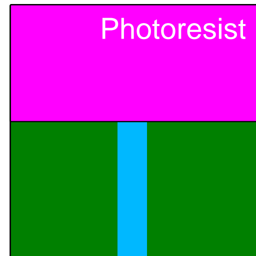


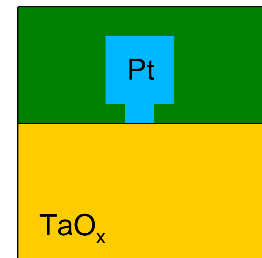


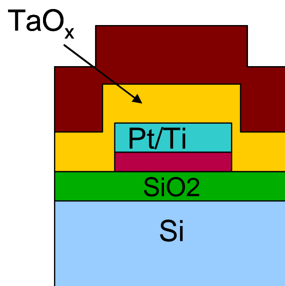












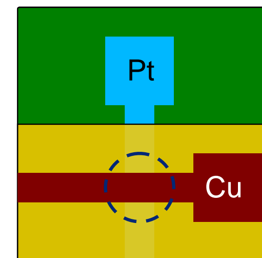


Figure 2.3: Process flow of Cu/TaO_x/Pt conductive bridge resistive devices. (1) Thermal oxidation of Si substrate. (2) Lithography and Pt/Ti e-beam evaporation. (3) Pt/Ti lift-off. (4) Lithography, TaO_x e-beam deposition, and TaO_x lift-off. (5) Lithography, Cu e-beam deposition, and Cu lift-off. Tong Liu, Yuhong Kang, Mohini Verma, and Marius Orlowski, "Novel highly Nonlinear Memristive Circuits for Neural Networks," WCCI 2012 IEEE World Congress on Computational Intelligence, June, 1015, 2012 Brisbane, Australia. Used under fair use, 2015.

2.3 Characterization of Process Steps

In order to make sure that the user is handling only limited no of parameters while fabricating a samples, the processing steps have been well tried and tested. They are performed under optimum cleanroom conditions, and each process step was individually characterized to make sure that each of them is repeatable and gives the best possible results are obtained. As mentioned earlier, the following section will be describing the process sequence for depositing one layer of material. The process is redundant and can be utilized to create a stack of multiples layers. The pattern of deposition is dependent on the mask used, which is unique for every material.

2.3.1 Cleaning Procedures

In semiconductor device fabrication/processing, cleaning is one of the most important process steps which need to be performed especially before a high temperature processing step like solid state diffusion, oxidation or chemical vapor deposition. Contamination of silicon devices results in degradation of device performance and poor reliability and thus it is extremely important to control the contamination of semiconductor devices from particulate, metallic, organic or other contaminants like native oxide. Most of these contamination sources are from the various processing steps and hence it is extremely important to clean the substrate properly during the processing.

There are two major cleaning mechanisms i.e. dry cleaning and wet chemical cleaning and among these two basic mechanisms various cleaning recipes are used to remove the different types of contaminants from the Si surface. In wet chemical cleaning, solvents or acids are used either to dissolve the contaminant by converting it into a soluble compound or to wash it off by force. In dry or vapor cleaning, the contaminants are removed from the wafer surface in the gas phase by converting it into a volatile compound or by knocking it off the Si surface. The most commonly used cleaning solvents in semiconductor processing are acetone, isopropyl alcohol (IPA) and De-ionized (DI) water. Cleaning a wafer surface with acetone, isopropyl alcohol and DI water, in that specific order removes residual organic impurities from the wafer surface. Any solvent clean of silicon wafers is always followed by a DI water rinse, subsequent blow drying using a nitrogen gun which is then followed by a dehydration bake.

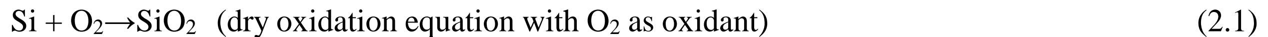
2.3.2 Thermal Oxidation of silicon substrates

After thoroughly cleaning the wafer, silicon wafer is oxidized thermally to grow silicon dioxide. The cleanroom facility at Virginia Tech has a thermal oxidation furnace in which wet/dry thermal oxidation can be carried up to the maximum temperature of 1050 °Celsius for 4 inch wafers. The furnace has 3 thermocouples and when loading the wafers into the furnace, it is made sure that the front of the quartz wafer boat is in line with the middle thermocouple to ensure the uniform oxide growth on all the wafers.

The fresh and cleaned Si wafers is placed carefully on the quartz boat. The furnace control temperature is set at 600 °Celsius and high purity nitrogen gas is purged into the furnace chamber

to prevent premature oxidation on the wafer. In the meantime the boiler is set at a temperature of 95-97 °Celsius and the reactor is turned to work at an efficiency of 35%. Once the boiler and furnace temperature has been attained, the quart boat along with the wafers are loaded inside the furnace. The furnace temperature is now set to 1050 °Celsius. As soon as the required temperature of 1000 °Celsius is achieved, the nitrogen purge is stopped and oxygen gas in introduced into the chamber and dry oxidation of the wafer is carried out at least for 5 minutes at a pressure of 1 Pa. After the dry oxidation run is concluded, wet oxidation is performed. For this the oxygen gas supply is made to pass through a bubbler containing water at about 95-97 °Celsius and this combination of oxygen and water vapor is introduced into the furnace and wet oxidation is carried out. A pressure of 0.7 Pa is maintained this time.

The rate of oxide growth dry/wet is predicted by Deal-Grove model [29]. The graphical representation of Deal-Grove Calculator is given in Figure 2.4. The various factors influencing thermal oxidation include temperature, ambient type (dry O_2, H_2O), pressure inside the chamber, substrate doping and substrate crystallographic orientation. For the devices covered during this work, about 750 nm - 800 nm of silicon dioxide was deposited on the silicon at a furnace temperature of 1050 ° Celsius which takes around 2 hours to complete. After the completion of the wet oxidation run, another run of dry oxidation is performed for another 5 minutes. After this the oxygen supply is cut off and nitrogen gas is purged into the chamber and the furnace temperature controller is set at 600 °Celsius. Once the furnace temperature comes back to approximately 600 °Celsius, the wafer boat is taken out of the furnace and allowed to cool down to room temperature before further processing. The thickness of the silicon dioxide film can be measured by using the Filmetric- interferometer thin film thickness measurement.



$Si + O_2 \rightarrow SiO_2$ (dry oxidation equation with O_2 as oxidant) (2.1)

$Si + 2H_2O \rightarrow SiO_2 + 2H_2$ (wet oxidation equation with H_2O as oxidant) (2.2)

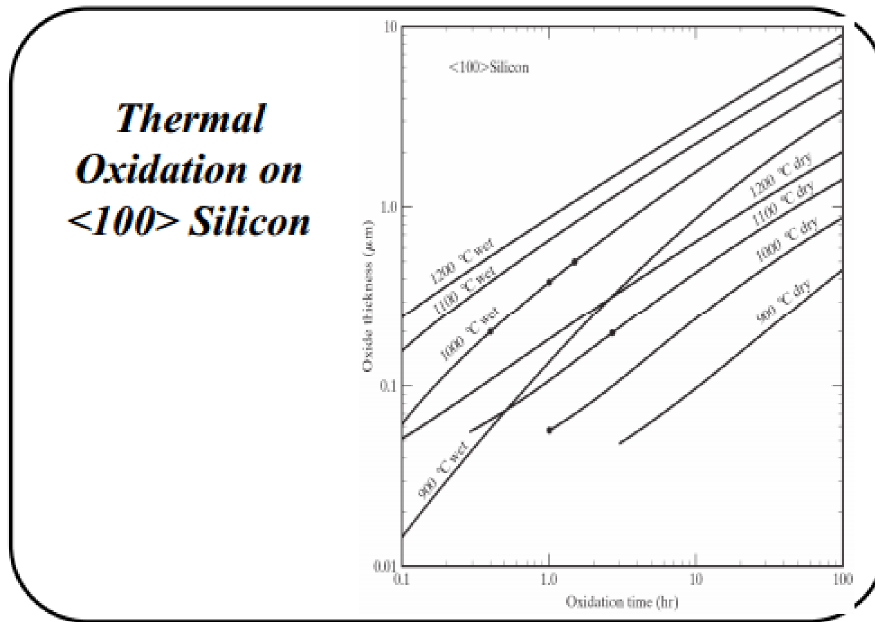


Figure 2.4: Thermal oxidation of a silicon wafer of crystallographic orientation '100'. Thermal Oxidation, http://www-inst.eecs.berkeley.edu/~ee143/fa05/lectures/Lec_05.pdf. Used under fair use, 2015.

2.3.3 Photolithography

Photolithography, also termed optical lithography or UV lithography, is a process used in microfabrication to pattern parts of a thin film or the bulk of a substrate. It uses light to transfer a geometric pattern from a photomask to a light-sensitive chemical "photoresist", or simply "resist," on the substrate. A series of chemical treatments then either engraves the exposure pattern into, or enables deposition of a new material in the desired pattern upon, the material underneath the photo resist. For example, in complex integrated circuits, a modern CMOS wafer will go through the photolithographic cycle up to 50 times.[30]

Photolithography involves the use of a liquid called photoresist which is a photosensitive polymer consisting of three components: a base material (resin), a photoactive compound (PAC) and a solvent. This photoresist is spread out on the silicon substrate in the form of a thin film using a spin coater. The thickness of the photoresist film depends upon the spin coater chuck's rotation speed and photoresist viscosity among many other factors. The properties of the PAC change on the exposure to ultraviolet light thereby either inhibiting or promoting the dissolution of the resin in the developer solution based on the type of photoresist. There are two different types of photoresist available: positive photoresist and negative photoresist. In case of a positive photoresist, the PAC is deactivated and the photoresist breaks down upon exposure and the exposed areas are washed away using a developer solution leaving the unexposed areas which are insoluble in the developer thereby giving a positive image of the mask in the photoresist. In a negative photoresist, the photoresist in the exposed areas polymerize and are rendered insoluble while the unexposed areas are washed away by the developed solution leaving a reverse image of the mask in the photoresist. A glass photomask patterned with chrome was used here. The portion of the photo mask covered with chrome is opaque and does not allow the ultraviolet light to pass

through it while the remaining of the photo mask areas are transparent and allow the UV light to pass through it. [15]

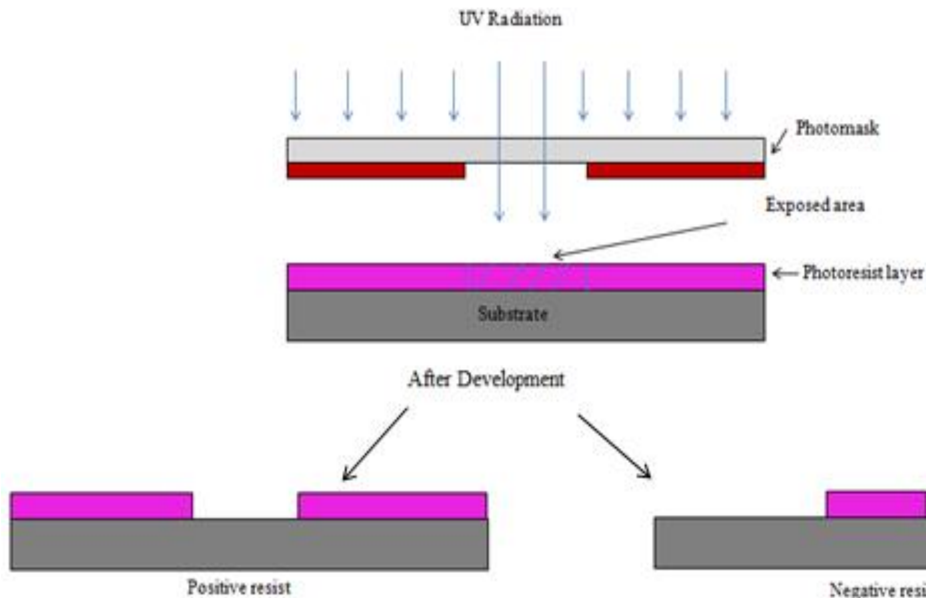


Figure 2.5: Negative and Positive Photolithography

The mask aligner MA-6 has been used for all the photolithographic processing. MA-6 is suitable for use with either the I-line (365 nm) or the G-line (436nm) wavelength. Here channel 2 of the MA-6 (436nm wavelength) which is set at a constant intensity of 10.8 mW/cm^2 has been used for exposure of all the samples. Figure 2.5 gives the technique for photolithography.

2.3.4 Mask Layout:

A catalog mask was designed for fabricating the samples. Typically a quartz photomask has been used for this purpose. In the resistive switch, three different mask pattern are required for the bottom electrode (Pt), the electrolyte (TaO_x) and the top electrode (Cu) individually. The feature size ranges from 1µm to 35µm. The mask is designed in such a way that there are 100 devices for each size. Figure 2.6 shows the catalog comprising 4 mask patterns out of which 3 are put to use for fabricating a Cu/TaO_X/Pt device. Any of the 4 masks can be used by rotating the mask by 90° clockwise and placing it on the mask holder. The mask on the top of the catalogue is used for patterning the bottom electrode. The one on the right is used for patterning the solid electrolyte and the one on the left is used for patterning the top electrode. Each of these masks has an alignment mark which is located at the bottom left corner.

However for the Low-k dielectric Cu interconnect structure an island mask is used. After blanket deposition of the bottom electrode and the interlayer dielectric, this mask is used to develop just the top electrode features. Since the bottom electrodes are blanket depositions, it does not require any geometrical patterning. The white islands made in Figure 2.7 is the chrome plot which will eventually form the top electrode in the device. The mask has a dimension of 4”×4”×0.60”.

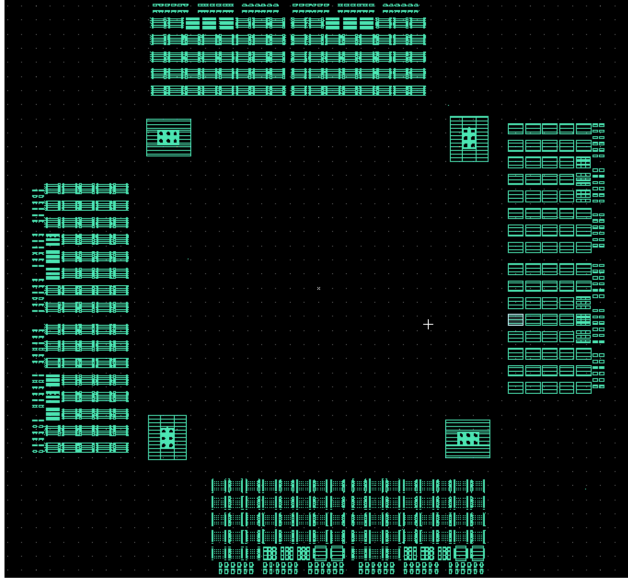


Figure 2.6: Complete Design of the RS mask

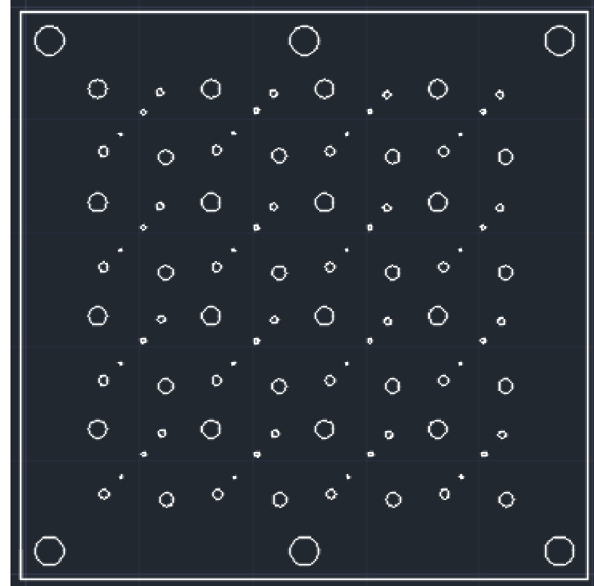


Figure 2.7: Complete Design of the interconnect mask

2.3.5 Photoresist recipe

As already mentioned in the process flow, negative photolithography technique had been used for the fabrication processing of nanocrossbar resistive switches. For this purpose the photoresist AZ 5214 E-IR is used. Before the application of the photoresist the wafer first needs to be cleaned using the most widely used solvent cleaning technique i.e. acetone and IPA. It is extremely important to clean the wafer with IPA thoroughly to remove any traces of acetone from the substrate. After this the wafer is cleaned by running de-ionized water for about 2 minutes. This is followed by blow drying using a nitrogen gun to remove excess moisture. After this hexamethyldisilazane (HMDS) which promotes photoresist adhesion on silicon and other substrates as well is spun coated on the substrate surface. The cleaned wafer is placed on the spinner and the vacuum is enabled to ensure proper sealing.

A generous amount of HMDS is poured drop wise on the wafer and the liquid evenly spread the liquid out on the surface by manually rotating the spinner holder. The necessary program is selected in the spinner. The spinner is set to run at the rate of 500 rpm for the first 15 seconds and then 2500 rpm for the next 45 seconds. This is followed by the soft bake of HMDS at 110 °Celsius for 1 minute on the hot plate. This baking of HMDS is extremely important to sustain the smaller features during the liftoff procedure. Typically the metal lines of features of 1µm to 2 µm would liftoff along with the photoresist. Baking of HMDS improves the adhesion of the photoresist and hence the resolution of the smallest metal lines. However, over baking can cause the unwanted photoresist to stay back on the wafer, even after developing. Therefore, it is important to maintain the optimum time and temperature for baking. After this the photoresist is spin coated on to the substrate so as to obtain a photoresist layer of thickness slightly greater than 1 µm. The photoresist thickness depends on the viscosity of the photoresist as well as the rotational speed of the spin

coater. In order to ensure the uniformity of the photoresist, the spin coating of AZ 5214 E-IR is spun at a rate of 1200 rpm for 45 seconds. Photoresist spin coating is followed by softbake done on the hot plate at 110 ° Celsius for 1 min to evaporate the solvent thereby improving resist adhesion.

After this UV hard exposure is done using the constant intensity channel-2 of the MA-6 (435 nm wavelength and an intensity of 11.5mW/cm^2) for about 16 seconds in vacuum contact mode. Necessary alignment is also done before exposure. The mask is required to fitted in the mask holder of MA-6. The next step is the reversal bake on the hot plate at 110 deg for 2 minutes which renders the exposed resist areas insoluble in the developer. However it is very important to have a delay of at least 1 minute between the first UV exposure and image reversal bake for a 1µm thick photoresist film. This delay ascertains the outgassing of nitrogen to prevent bubble formation during reversal bake. It is at this juncture that the mask pattern emerges on the photoresist. Then the flood exposure is performed which is at least greater than 200 mJ/cm^2 (g-line for about 36 sec). This second exposure also called as the flood exposure since no mask is used during this exposure and it increases the solubility of the unexposed resist areas and during the process improves developer's selectivity and resolution properties.

Flood exposure is then followed by the development process. The developer solution used for AZ 5214 E-IR is MF-319. MF-319 is a mild developer and provides a good precision with respect to feature size obtained even if the wafer is left in the solution longer than the intended time. The development time is approximately 90 sec and requires some agitation to remove the unwanted photoresist. After the development the negative image of the mask is obtained on the substrate. The wafer is then rinsed in the DI water for more than 1 minute and then blow dried with a nitrogen gun and the remaining photoresist pattern is observed under an optical microscope to ensure correct pattern transfer. The height of the photoresist can also be measure by the usage of Dektak.

2.3.6 Physical Vapor Deposition

Physical vapor deposition is a method for depositing thin films on the silicon substrate by the means of actual physical transfer of the source from either a crucible or sputter target on to the substrate surface in the gaseous phase. The PVD tool used in Virginia Tech cleanroom facility is the Kurt Lesker PVD 250 which has been used extensively for e-beam evaporation based thin film deposition during the course of this research. The source material which comes in the form of pellets is preconditioned in a crucible and to start with the deposition the substrate as well as the source present inside the PVD chamber has to be brought to a very low pressure in the range of 2×10^{-6} - 4×10^{-6} Torr. Once this low pressure is achieved a beam of electrons is focused on the crucible thus melting the material inside and the evaporation begins thus coating the inside of the chamber. The chamber also has a quartz crystal which monitors the actual rate of deposition as well as the thickness of the film. The PVD runs both in the automatic and manual deposition mode. For this fabrication manual mode has been used.

In the manual mode, the user controlled parameters are longitudinal and lateral amplitudes of the e-beam, and the current flow in the system. The rate of current flow control the following aspects:

- The rate of meltdown of the crystal thus causing e-beam evaporation.
- The rate of deposition which is monitored in kÅ/s.
- The substrate temperature which cannot be monitored through.

It is advisable to find a good trade-off between deposition rate and substrate heating. Very high current may result in a faster deposition time but in this case, the quality of deposition will be very poor. Current level above 300mA have been known to result in an uneven texture of material deposition.

The voltage level maintained hovers around 7.35V. There is a quartz crystal inside the PVD chamber which monitors the deposition rate and reports the thickness of the film to the user based on the density, tooling factor and Z-ratio of the material being evaporated. Z-ratio of a material is defined as the parameter that corrects the frequency change to a thickness transfer function for the effects of acoustic impedance mismatch between the crystal and the evaporated material. This value is unique for every material. It is important to note down that before starting the deposition, the crystal needs to be replaces if its life falls below a value of 33%.

The electron beam evaporation (PVD250) is illustrated in Figure 2.8. The deposited material is melted in the crucible at the bottom of the chamber. The electron beam is generated from a tungsten filament (Telemark) and deflected to the graphite crucible. The vacuum pump maintains the low pressure in the PVD chamber. The substrate chuck rotates constantly at 5 rounds/min during deposition to improve the thickness uniformity of the deposited thin film. The evaporation is started when the chamber pressure reaches ~10^{-6} torr. The substrate temperature was monitored to be around 25 °C without heating the substrate chuck.[15] The deposition rates and parameters of Ti, Pt, Cu, and TaO_x are listed in Table 2.1. The deposition rates are measured by quartz crystal microbalance in PVD, the Filmetrics F20 optical system, and the Dektak profiler.

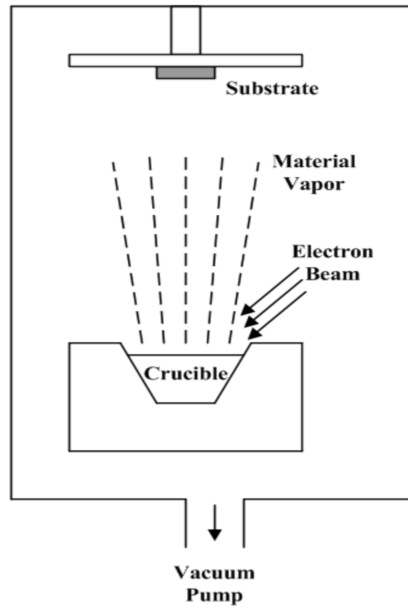


Figure 2.8. Schematic illustration of the electron beam deposition

Table 2.1 Summary of Electron Beam Deposition for Cu/TaO_x/Pt Device.

Material	**Ti**	**Pt**	**TaO_x**	**Cu**
Layer Thickness (nm)	20	50	32	150
E-Beam Deposition Rate (Å/s)	1	1.5	1	4
Melting Temperature (°C)	1668	1768	1872	1085
E-Beam Current (mA)	120	330	130	120
E-Beam Base Pressure (Torr)	2×10^{-6}	2×10^{-6}	2×10^{-6}	2×10^{-6}
Density (g/cm^3)	4.43	21.45	8.2	8.93
Z-ratio	0.628	0.245	0.3	0.437
Tooling Factor	140	140	140	140

2.3.7 Lift off

Liftoff and etching are two most commonly employed patterning techniques employed in combination with photolithography. While etching is a subtracting technique well suited for Atomic Layer Deposition (ALD), liftoff is well suited for Physical Vapor Deposition (PVD). To avoid sophisticated dry etching steps, the lift-off technology is used for removing excessive materials and patterning the active region. Considering the requirement of lift-off, negative lithography is employed for defining the device active region. Acetone has been used as the liftoff solvent. The lift off of Pt is comparatively very easy since Pt and TaO_X lifts off within 2-3 minutes of the wafer being immersed into the acetone. It is to be noted that we do not employ ultrasonic mechanical vibrations while doing the lift off platinum since it might lead to the lift off the material from the needed areas. On the contrary the procedure for liftoff of Cu is to immerse the wafer in acetone and then subject it to ultrasonic vibrations for 5-6 minutes. During sonication, it is advisable to keep the wafer upside down in order to avoid the lifted off fine metal particles sticking back to the surface, while pulling the wafer out from the acetone solution. This can cause a complete device failure. Figure 2.9 illustrates a typical lift-off mechanism.

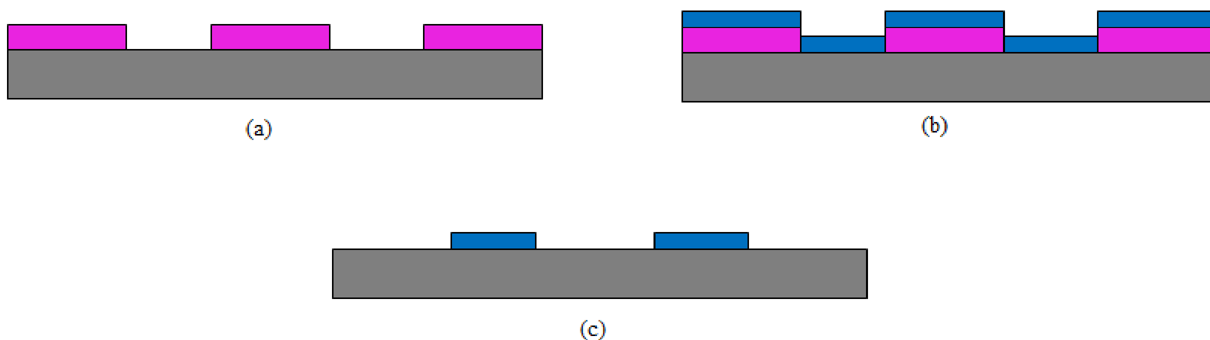


Figure 2.9: Lift off Process (a) Photoresist coat and patterning, (b) Thin film deposition and (c) removal of photoresist and thin film above it, after lift off

2.4 Summary

The $Cu/TaO_x/Pt$ devices have been fabricated by electron beam evaporation and lift-off technology. Samples Fabricated are given as follows:

Simple CBRAM devices

1) Pt (60nm)/ TaOx (32nm) / Cu(150nm)

Interconnect Devices

1) Pt (60nm)/ TaOx (40nm)/ Ta (70nm)
2) Ta (50nm)/ TaOx (40nm)/ Cu (150nm)
3) Ti (80nm)/ TaOx (40nm)/ Cu (150nm)

Chapter 3: Mechanism of Formation of Oxygen vacancy Conductive Filaments

3.1 Introduction

In this chapter it is demonstrated that multilevel switching of oxygen vacancy (V_O) conductive filaments (CF) is characterized by the relation $R_{ON} = A/ I_{CC}{}^n$ between ON-state resistance (R_{ON}) and compliance current (I_{CC}). In contrast to metallic (Cu, Ag) CFs, where the exponent *n* for various devices is found universally to be ≈ 1, we find for V_O CFs n=1.36. Hence, the identification of the constant A with a universal minimum SET voltage, as in the case of metallic CFs, is no longer valid. We argue that an exponent n>1 implies two distinct mechanisms responsible for the formation of V_O CFs. 1st mechanism is similar to the formation mechanism for metallic CFs and accounts for the unity part of the exponent, while the 2nd mechanism is responsible for the remainder (n-1). This hypothesis is corroborated by data of V_O CFs in resistive switching cells with and without active electrodes such as Pt/TaO_x/Cu and Pt/TaO_x/Pt.

3.2 Experimental Set –up

When different levels of compliance current (I_{CC}) are applied to a CBRAM device, a characteristic dependence of LRS resistance (R_{ON}) on I_{CC} is observed. This had been earlier explained during the introduction of the thesis.

$$R_{on} = \frac{A}{I_{CC}{}^n} \tag{3.1}$$

Where; n is a fitting parameter close to 1 for metallic CFs and A is a constant in units of volt. The $R_{ON} - I_{CC}$ relation in eq. (3.1) has been reported to be valid for numerous anode/electrolyte/cathode material systems [14-21]. In [21] it has been shown that the constant A in eq. (1) is universally correlated to the minimum SET voltage ($V_{SET(MIN)}$) for all metallic conductive filaments reported so far. $V_{SET(MIN)}$, required to switch the memory from OFF- to On-state, can be extracted from V_{SET} measurements at small voltage sweep rates. Since such an analysis is largely lacking for oxygen vacancy CFs, it is the objective of this paper to close this gap. Our results show that for V_O CFs the exponent n is significantly larger than 1 indicating that there are two mechanisms responsible for formation of V_O CFs. Experimental data on resistive switching Pt/I/Cu and Pt/I/Pt cells with dielectric I=Ta_2O_5 (ALD), TaO_x (PVD), SiO_2 (PVD) are evaluated to elucidate the formation mechanisms of oxygen vacancy nanofilament.

Figure 3.1 shows the device structure and the quasi-static bias voltage in the I–V sweeping operation. The process and electrical characterization of these devices have been reported in Chapters 1 and 2. The resistive devices are fabricated in a crossbar array on the thermally oxidized Si substrate. Both metal electrodes and oxide are deposited by electron beam evaporation and patterned by lift-off technology. The oxygen-deficient TaO_x is deposited by evaporating TaO_x pellets without O_2 injection to the evaporation chamber or more commonly known as the PVD. The top Cu or Pt electrode runs perpendicularly to the bottom Pt electrode. The thickness of TaO_x is 32nm and 16 nm. In some cells Ta_2O_5 of 16 nm has been deposited by Atomic Layer Deposition.

In this way following devices have been manufactured: $Pt/Ta_2O_5/Cu$, $Pt/TaO_x/Cu$, $Pt/TaO_x/Pt$, $Pt/Ta_2O_5/Pt$, $Pt/SiO_2/Cu$, and $Pt/SiO_2/Pt$. The area of device under test is square and the size varies from (5×5) to (35×35) μm^2. An electroforming operation is needed for a fresh device cell before the regular switching cycles. I–V characteristics are measured by Keithley 4200-SCS at room temperature. The Pt bottom electrode being the inert electrode acts as the stopping electrode. It is therefore grounded and the bias voltage was applied to the Cu or Pt top electrode which serves as the active electrode.

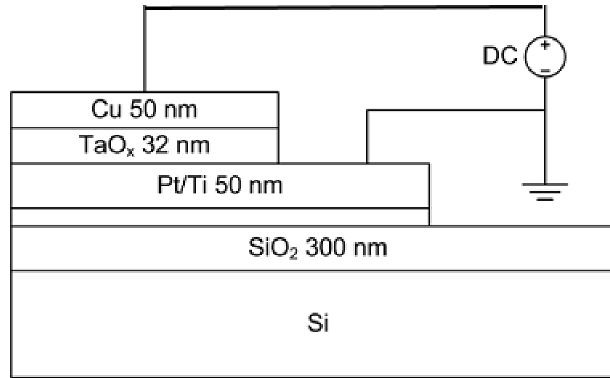


Figure 3.1: Experimental set-up

3.3 Experimental Results

In Figure 3.2, a typical set and reset unipolar operation for V_O CF in Pt/TaO_x(16 nm)/Pt is shown. The V_{SET}=-2.1 V at I_{CC}=1 mA and V_{RESET}=-0.9 V. Similar data has been obtained for Pt/Ta_2O_5(16 nm)/Cu devices. While the ranges of set and reset voltages are the same for both PVD and ALD devices, the forming voltages for ALD devices are significantly higher ($\Delta V \approx 2V$) than for PVD cells.

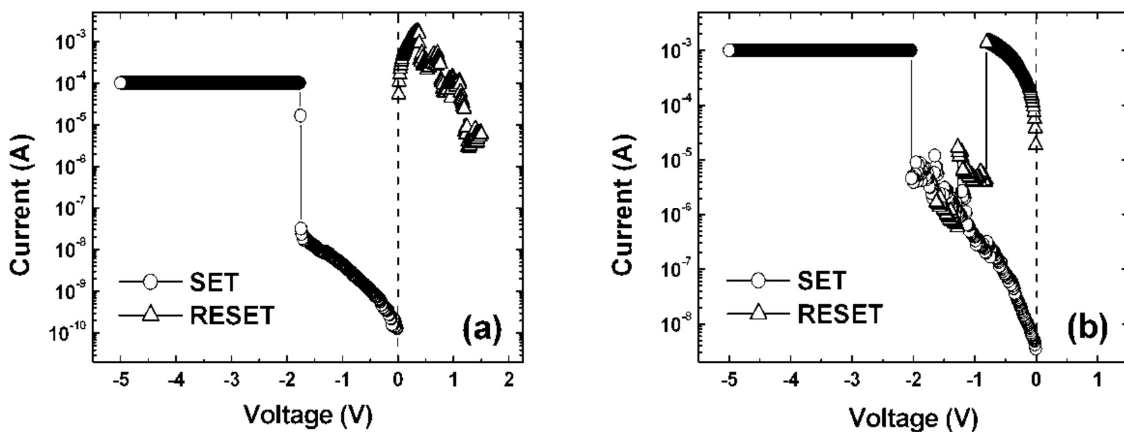


Figure 3.2. Set and (a) bipolar and (b) unipolar reset of V_O

In Figure 3.3, the R_{ON} of V_O CFs is shown as a function of the compliance current I_{CC}. On a double logarithmic scale, one can see that R_{ON} decreases linearly with I_{CC}, according to eq.(1). The parameters extracted parameters are A=0.022 and n=1.36. This constitutes a significant departure

from our previous conclusion of n=1 found for all metallic CFs. As a consequence of n>1, the constant A can no longer be interpreted as the universal minimum switching voltage [21]. However, locally, i.e. for a small I_{CC} interval, we can still fit the data to eq.(1) with n=1 and extract following values for the constant A in units of volt: for $I_{CC} \approx$ 10nA A=1.7V, for Icc ≈ 0.1mA A=0.52 V, and for I_{CC} =10mA A=0.06V.

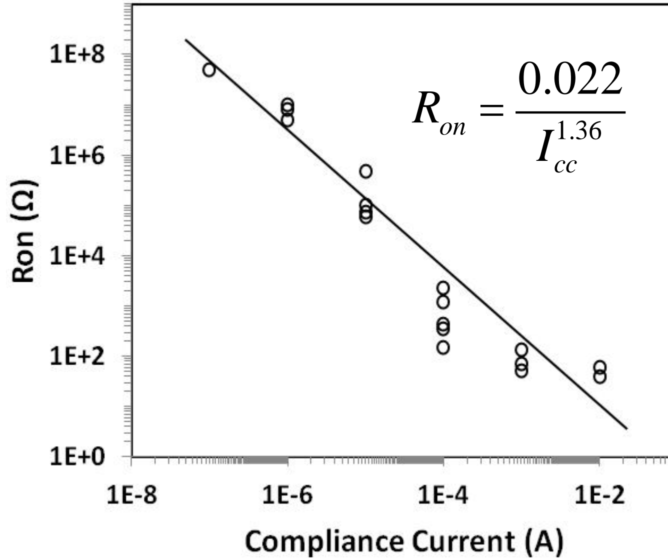


Figure 3.3 R_{ON} versus I_{CC} for V_O CF in Pt/Ta_2O_5/Cu device with 16 nm Ta_2O_5.

One is then led to the conclusion that at low I_{CC} currents the minimum set voltage is high and at high I_{CC} currents very low. As in [21] we have measured the set voltage of V_O CF as a function of voltage sweep rate, ramp rate (rr). We find that as in the case of metallic CFs the SET voltage is decreases almost linearly with the logarithm of rr. However, in contrast to metallic CFs, the V_{SET} for V_O CF does not saturate at a minimum set voltage, even at such slow ramp rates as rr=2 mV/s. This is shown in Figure 3.4 below.

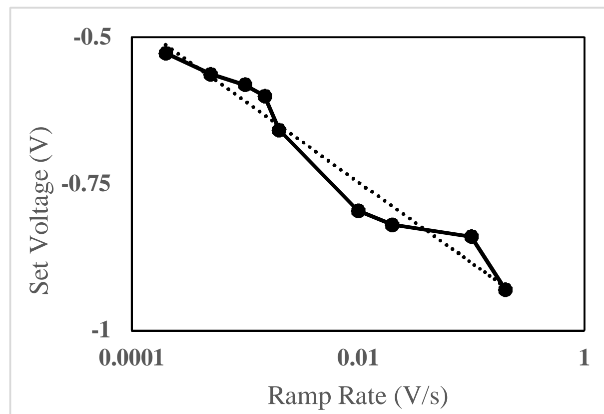


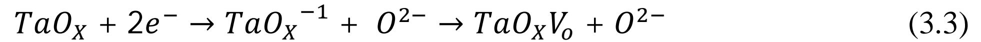
Figure 3.4: Variation of V_{SET} w.r.t. Ramp Rate for vacancies

3.4 V_O Formation and Set Models

There is a wide consensus [10] that at the interface between the active electrode (Cu) and the metal oxide dielectric a redox reaction is taking place:

$$Cu \rightarrow Cu^{+} + e^{-} \qquad \text{(Reduction-Oxidation)} \qquad (3.2)$$

When positive bias is applied to the active electrode Cu+ ions migrate toward the inert electrode (Pt) and are stopped at the Pt interface, extending thus the inert electrode into the oxide. This aggregation of Cu atoms grows then at an ever accelerated rate toward the active Cu electrode until a complete bridge is formed. In other words, the mechanism basically lies in the piling Cu atoms upon Cu atoms due to increased electric field between the inert electrode extended into the dielectric and the active Cu electrode. In case of negative bias, the oxidation reaction eq. (3.2) provides an efficient injection mechanisms of electrons into the oxide while Cu^{+} ions are returned to the Cu electrode. It is crucial to consider the action of electrons under a negative bias. The electrons are injected and may charge and dislodge the negative oxygen ion from the metal oxide matrix leaving behind a neutral oxygen vacancy V_O according to the reaction:



$$TaO_X + 2e^{-} \rightarrow TaO_X{}^{-1} + O^{2-} \rightarrow TaO_X V_o + O^{2-} \qquad (3.3)$$

It should be noted that a similar reaction would be possible for singly charged oxygen ion. However, a singly negative oxygen ion has been ruled out as highly unstable in a metal oxide matrix. At this point it is important to consider where such reaction for equation (3.3) is taking place. Since the redox reaction (3.2) takes place at the Cu/TaO_x interface and produces a large number of electrons, the creation of V_O will take place at the interface as well.

Since the oxygen vacancy is known to provide a local Fermi level close to the conduction band, the vacancy will extend the active electrode into the oxide and act as a conduit of more electrons. Thus it is likely that another V_O will be formed below the first one extending thus the partial V_O filament deeper into the oxide. This, in turn, leads to an increased electric field between the end of the partial V_O CF and the inert electrode Pt. This growth mechanism is illustrated in Figure 3.5.

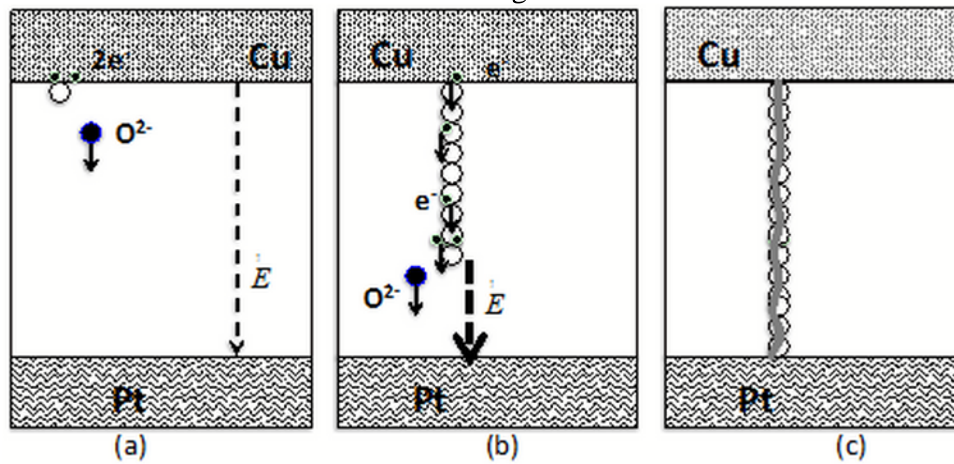


Figure 3.5 Surface-initiated V_O filament growth triggered by reactions (2) and (3).

Clearly, this self-accelerating mechanism is similar to the formation of Cu CF at positive bias, described above.

An alternative and competing mechanism for creation of oxygen vacancies is that electrons migrate into the oxide by hopping mechanism and at some point undergo reaction (3.3) but now in the bulk rather than at the surface as illustrated in Figure 3.6(a). This mechanism is assumed to be at work in the dielectric breakdown, particularly of metal oxides. Over the stress time, more and more of vacancies will be generated in the same way leading to an intermediate state depicted in Figure 3.6(b). This process of creating increased density of vacancies will reach a critical concentration of vacancies allowing for a conductive percolation path between the two electrodes as shown in Figure 3.6(c). Note that this mechanism will be present irrespective of the nature of the top electrode. A conductive path across the dielectric is established when the density of created vacancies reaches a critical level to allow for a conductive percolative path. Obviously, the second mechanism of V_O formation represents a very stochastic process and lacks the self-accelerating feedback of the first mechanism. Hence, it is less efficient in creating a V_O conductive nano-filament.

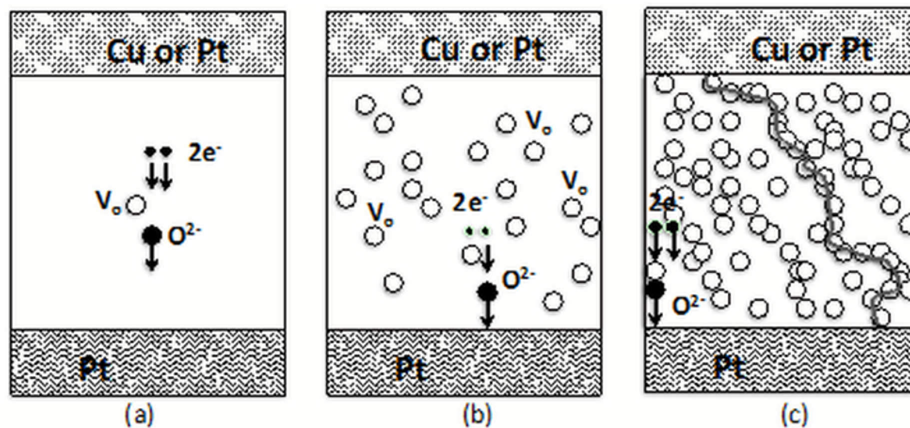


Figure 3.6: Random bulk growth of the V_O filament triggered by reaction (3.3) only

In general case, both mechanisms will be at work at the same time, cooperating and enhancing each other. However, it is possible to separate them by considering two cells with and without the active electrode: Pt/TaO_x/Cu and Pt/TaO_x/Pt. In Pt/TaO_x/Cu the first mechanism will be present with a copious injection of electrons at the Cu/TaO_x interface, while this mechanism will be absent in the Pt/TaO_x/Pt cell. Typical form and set characteristics for Pt/TaO_x/Pt is shown in Figure 3.7. The form and set voltages are significantly higher than for the Pt/TaOx/Cu cell.

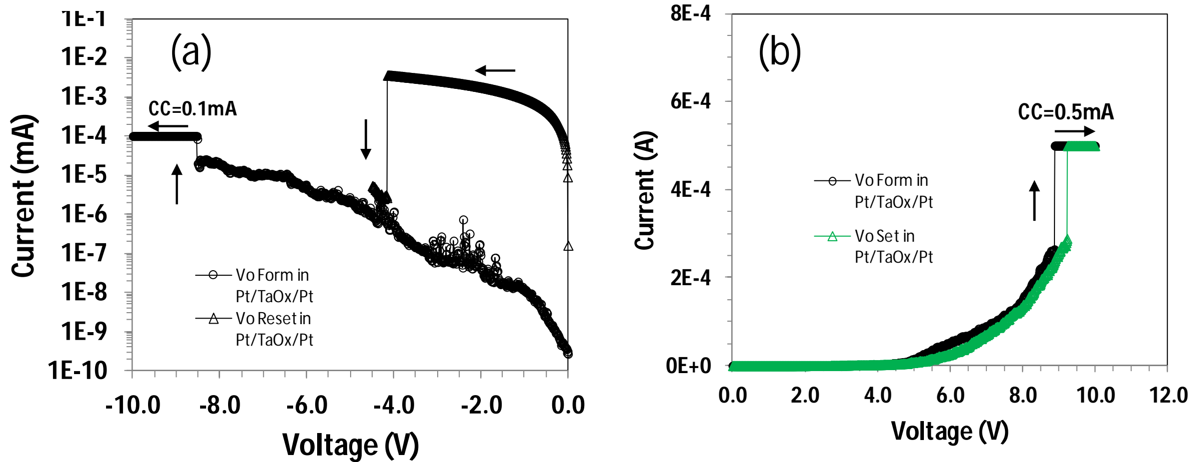


Figure 3.7: Switching characteristics of V_O CF in Pt/TaO_x/Pt resistive devices. (a) Forming and reset operations. (b) Set operation under positive and negative bias.

Thus it is much easier to create a V_O CF in Pt/TaO_x/Cu than in Pt/TaO_x/Pt devices for the same TaO_x thickness, requiring larger electrical fields or longer times for the case when the set operation is performed at a constant voltage stress. In Figure 3.8 the set operation for the Pt/Ta_2O_5/Pt cell is shown at two different set currents. It was found that for all set currents below 0.1 mA only volatile V_O CF could be formed. Only for compliance currents above 1 mA stable non-volatile V_O CFs could be formed. At higher set currents the cell could be set and reset but less than 10-20 times before it was permanently damaged.

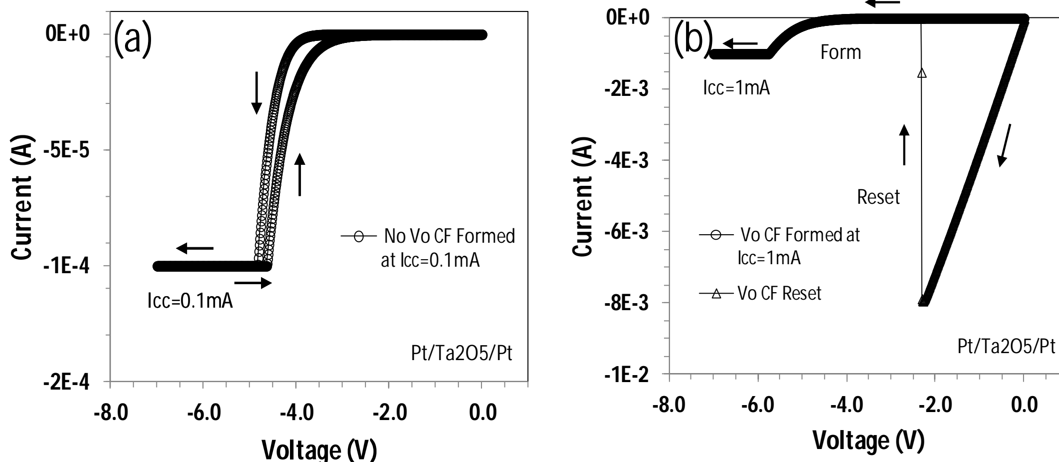


Figure 3.8: Switching characteristics of V_O CF in Pt/Ta_2O_5/Pt resistive devices. (a) Attempts to set V_O CF at low I_{CC} =0.1 mA (b) set operation at large I_{CC} =1 mA and subsequent reset operation

To investigate the role of a dielectric further, we have fabricated Pt/SiO_2/Cu and Pt/SiO_2/Pt devices. The thickness of SiO_2 layer is d_{SiO2}=32, 16, and 8 nm. SiO_2 is known to be very stable and not susceptible to oxide damage via V_O formation. For both types of devices with d_{SiO2} =32 nm we were unable to form V_O CF even at voltages as high as 15V. Corresponding, typical I-V characteristics are shown in Figure 3.9.

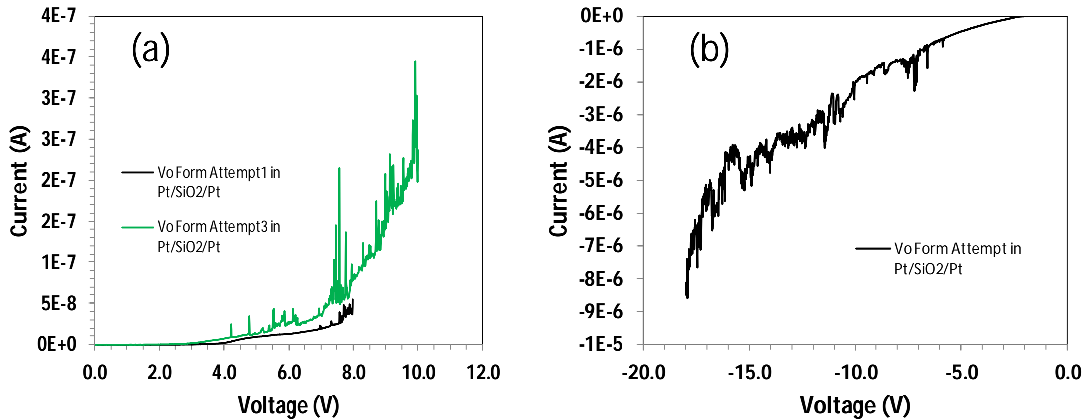


Figure 3.9: Failed attempts to form V_O CF in $Pt/SiO_2/Pt$ devices with d_{SiO2}=32 nm. (a) at positive voltage bias. (b) at negative voltage bias.

The experiments demonstrate the crucial role of the active electrode and the oxidation reaction (2) induced by it in the formation of the V_O CFs. Also the circumstance that $Pt/Ta_2O_5/Pt$ cells were switchable only a few times before suffering permanent damage points to a large component of the stochastic formation of a critical concentration of V_O conducive to irreversible conductive path(s) between the two electrodes. The density is so high that after several set operations several conductive paths can be formed that can no longer be ruptured.

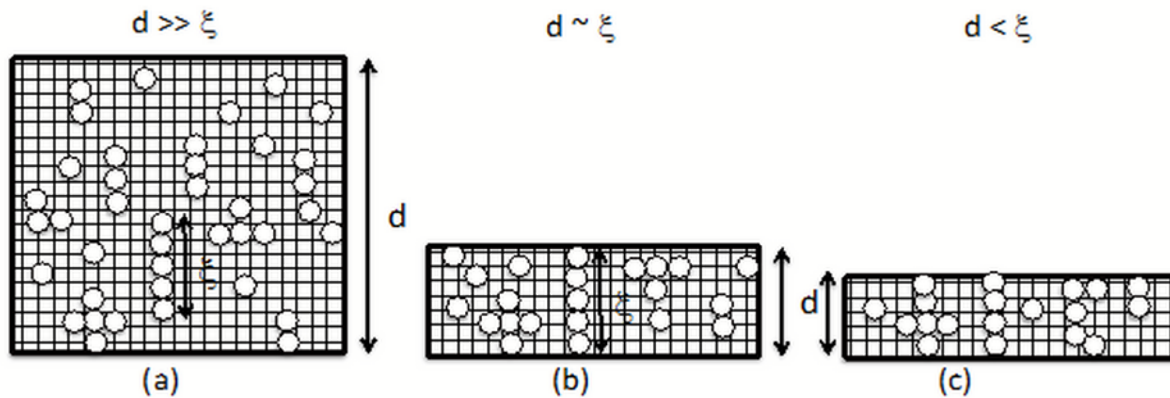


Figure 3.10: Percolation model for V_O CF formation as a function of dielectric thickness. (a) the thickness d >> ξ - no V_O CF can form. (b) d ~ ξ - Vo CF can form but switch unreliably. (c) d < ξ - V_O CF can be switched reliably

For d_{SiO2} =16 nm devices V_O CF could be formed but not reliably set and reset. For d_{SiO2} = 8 nm the V_O CF could be readily formed, set and reset. These results indicate that the dielectric thickness is critical to the operation of V_O CF-based filamentary switching. We explain this behavior by the percolated V_O cluster size model illustrated in Figure 3.10. This model supplements the bulk model explained in Figure 3.5. In SiO_2 devices, the activation energy to form O_2-V_O pairs is much larger than TaO_x and Ta_2O_5. Hence both the surface-initiated and bulk mode V_O CF growth mechanisms are ineffective in generating sufficient levels of oxygen vacancies to create a conductive percolation path. A sufficiently high concentration of V_O can be translated in a maximum V_O cluster size ξ. Our data on SiO_2 devices indicates that both d_{SiO2}=32 nm and 16 nm are larger than

maximum length of oxygen vacancy cluster, but d_{SiO2}=8 nm length comes in the range of characteristic lengths of oxygen vacancy clusters as shown in Figure 3.9 (c).

3.5 Summary - Proposed Analogy

A comprehensive study of oxygen vacancy formation has been conducted for several dielectrics and different combination of Cu and Pt electrodes. The formation mechanism of oxygen vacancy monofilament is different that of conductive nanofilaments formed by metal ions. While Cu and Ag formation is dominated by one mechanism of piling metal ions upon each other (assuming presence of an inert counter-electrode) and extending the inert electrode into the dielectric, the formation of V_O CF is a synergy of two different mechanisms: a surface-initiated mechanism and a bulk mechanism.

We believe that the presence of the two mechanisms manifests itself in the exponent n of the relation (3.1) being, in case of VO CFs, substantially larger than one. The surface-initiated mechanism accounts for n=1 for both metal and oxygen vacancy nanofilaments, reflecting the self-accelerating mechanism of filament build-up, while n-1>0 is indicative of the bulk mechanism responsible for more gradual accumulation of defects (here: oxygen vacancies). The experimental data of the various memory cells has shown clearly the importance of the oxidizing (active) electrode in the formation of stable and resettable V_O CFs. The bulk model of V_O CF formation applies also to the generation of V_O -O_2- pairs at the surface but is fed by the large supply of electrons at the oxidizing (Cu) electrode. The supply of electrons at the surface comes directly from the active electrode under the negative voltage bias. The oxygen vacancy cluster formation mode provides a larger cross-section to capture an electron in the dielectric layer and is more efficient to transport the electron to the next site to extend the partial filament toward the counter-electrode. This model allows to consistently explain the various phenomena observed in the resistive switching devices discussed here. Among the Pt/I/Pt devices only Pt/TaOx/Pt devices were amenable to formation of V_O CFs. The results presented here shed also light on the possible mechanisms of generation of a permanent damage (dielectric breakdown). For example, when the maximum size of V_O clusters formed in dielectrics with a high activation energy is in the range of the dielectric film thickness, the ON state may result in several parallel conductive paths. Such a configuration is difficult to rupture since the current in a given branch may be not high enough to initiate a rupture, triggered by deposited Joules heating, along several conductive paths.

Chapter 4: Study of Interdependence between V_{SET} and V_{RESET} Voltages for Cu Conductive Filaments – Characterization and Modelling

4.1 Introduction

A statistical dependence of set voltage, V_{SET}, on the preceding reset voltage, V_{RESET}, is observed in resistive RRAM memory arrays and explained in terms of two interlocking mechanisms. This dependence can be replicated on a single device by intentionally varying V_{RESET} values by various linear voltage ramp rates. The latter mechanism is well modeled under the assumption that a critical heat deposited locally in the filament triggers the rupture of the filament. Mechanisms are proposed to explain the impact of different ramp rates of the reset operation on the ruptured gap in the filament that affect the V_{SET} value of the subsequent set operation. Based on these observations, a one-time tightening procedure is designed leading to tight V_{SET} and V_{RESET} distributions. Resistive switching (RS) devices suffer from broad distributions of set or write and reset or erase threshold voltages [24,25]. Therefore, understanding the mechanisms how one (e.g. reset) operation impacts the subsequent complementary (e.g. set) operation is of interest. Here, we report an observed interdependence between V_{RESET} and V_{SET} distributions and propose mechanisms to explain experimentally observed data.

4.2 Characterization and Experiment Set-Up

We have fabricated Cu/TaOx/Pt switches at room temperature with 32 nm thick oxygen-deficient TaOx formed by e-beam evaporation. Typically, a two-terminal memristor is formed at each cross point of a crossbar architecture as shown in the optical micrograph seen in Figure 4.1 (a).

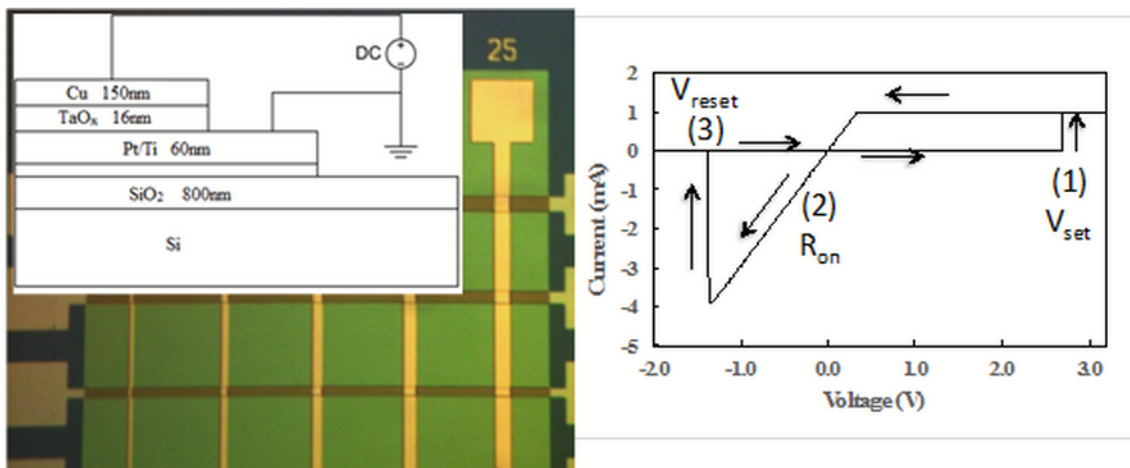


Figure 4.1(a) Optical micrograph of the crossbar architecture. The insert shows the device cross section with layer thicknesses specified. (b) A typical I-V characteristics of Cu/TaO_x/Pt device with a sharp set transition at positive V_{set} (1) voltage and a sharp reset voltage V_{RESET} (2). An ohmic behavior of the ON-state between V_{set} and V_{RESET} can be observed characterized by resistance R_{on} (2).

Figure 4.1(b) shows a typical behavior of one switching cycle of an individual switching devices.

4.3 Results and Discussion

Statistical analysis of V_{SET} and V_{RESET} values shows a characteristic correlation when a V_{SET} value is plotted versus the preceding V_{RESET} value for a multitude of array cells as shown in Figure 4.2. Despite a lot of scatter, it is seen that, in general, the subsequent V_{SET} increases with the increase of the preceding $|V_{RESET}|$. Here, the set/reset conditions have been kept fixed. The conditions for the set operation are: compliance current I_{cc}=0.1mA and voltage ramp rate rr=2V/s, and the corresponding conditions for reset operation are: rr=2V/s and no current limitation. It should be stressed, however, that the general dependence of V_{SET} decreasing with increasing $|V_{RESET}|$ has been observed for all kind of set and reset conditions showing the same trend with slightly stronger or weaker average slope. In order to understand this effect in more detail, we have studied the mechanism by changing V_{RESET} values deliberately on the same device by applying different ramp rates during the reset operation.

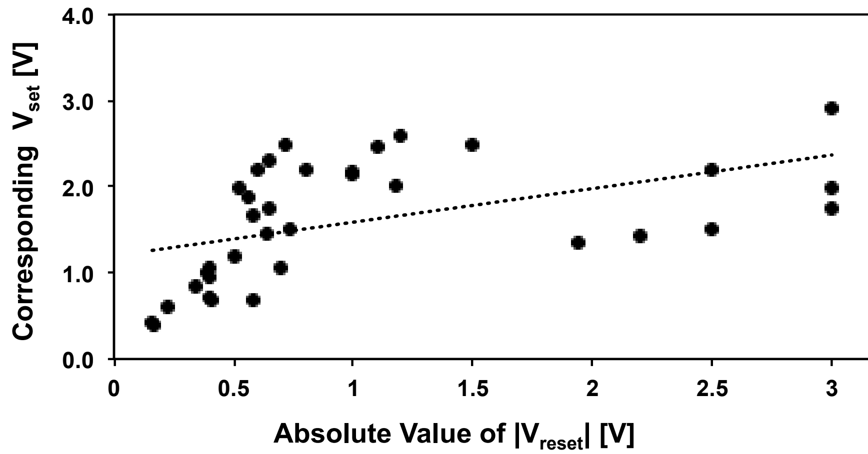


Figure 4.2 Experimental dependence of V_{SET} on preceding V_{RESET} for a multitude of array cells.

It has been observed in the past that faster ramp rate leads to larger $|V_{RESET}|$ values in both unipolar and bipolar reset modes [26,27]. A typical dependence of V_{RESET} as function of voltage ramp rate for is shown in Figure 4.3. In order to better understand this dependence, we assume that the rupturing of the conductive filament (CF) is a combined result of high electric fields and of Joules heating which raises the temperature at the most fragile part of the CF such that the Cu ions are dislodged and the filament dissolves locally. The thermal effect is supported by the strong electric field which sets in as soon as the filament is ruptured and sweeps the still highly mobile Cu^{+} ions back to the Cu electrode, creating, a final gap Δ^* in the filament. We assume that the rupturing is triggered when a critical amount of heat Q_{CRIT} is deposited at the weakest link (i.e. highest local serial resistance) of the CF. Since in our experiments, a conventional linear ramp rate $V(t)=rr\times t$ is used, the instantaneous power P(t) consumed during the reset operation is $P(t)=V^2(t)/R_{on}$ and the critical Joules heat Q_{CRIT} will be reached when the device RESETs at V_{RESET}

at which the filament is ruptured and the current collapses. For a linear voltage sweep, V_{RESET} translates to the reset time of $t_{RESET}=V_{RESET}/rr$. Hence, we obtain for Q_{CRIT}:

$$Q_{crit} = \int_0^{t_{reset}} V^2(t)/R_{on}dt = \int_0^{V_{reset}/rr} \frac{rr^2 \times t^2}{R_{on}} dt \qquad (4.1)$$

where R_{on} is the ON-state resistance of the device. The integral in (1) can be evaluated analytically and the resulting equation can be solved for V_{RESET}. One obtains:

$$V_{reset} = \sqrt[3]{3 \times Q_{crit} \times rr \times R_{on}} \sim \sqrt[3]{rr} \qquad (4.2)$$

Here, the key assumption is that the critical heat Q_{CRIT} is a constant for a given device, or for a class of devices manufactured in the same way. We mention that the dependence on critical heat instead on critical temperature T_{CRIT} as postulated elsewhere [28-30], has the advantage that it can be tied directly to the imposed experimental conditions in terms of the driving voltage V(t), simplifying thus the analysis. This 1st order relation appears to be valid for sufficiently large ramp rates rr. From experiments on RS devices [21] it is known that there are a minimum V_{SET} and a minimum V_{RESET} voltage, respectively for set and reset operation, which is not captured by eq. (4.1). One may attribute this circumstance to a minimum electric field needed to trigger the rupture in the filament, to remove the mobile ions from the filament. For very wide pulses or very low ramp rates, the local dissipation time of the Joules heat could be another limitation for eq. (4.1). According to simulations [28,29,31] the dissipation time has been estimated to be 1 ns -10 ns, but could be significantly larger. Taking the limitations together and realizing that as experimentally observed that there is a minimum $|V_{RESET}|$ voltage below which the device cannot be reset at any ramp rate, we can fit the behavior of V_{RESET} as a functions of ramp rate rr by the following equation:

$$|V_{reset}| = |V_{reset,\min}| + \gamma\sqrt[3]{rr} \qquad (4.3)$$

where $V_{RESET,min}$ and γ are parameters extracted from the experimental data and summarized in Table 4.1.

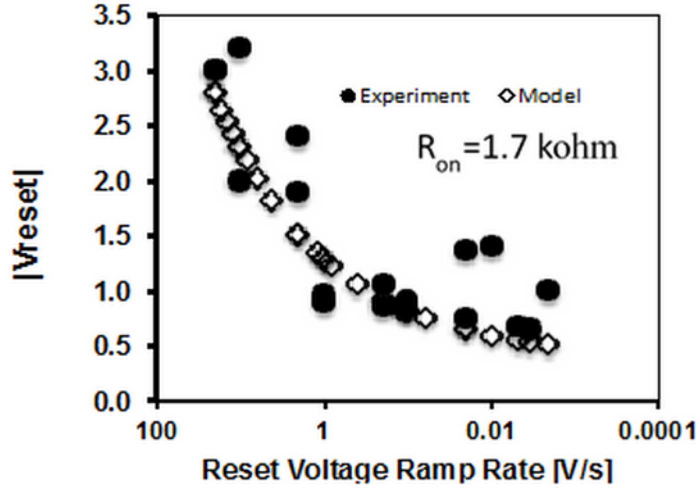


Figure 4.3 $|V_{reset}|$ as a function of voltage ramp rate for R_{on}=1.7kΩ: experimental data and model given in eq.(4.3).

In Figure 4.3 the experimental dependence of V_{RESET} on the ramp rate rr is shown. Clearly, it can be observed that $|V_{RESET}|$ decreases with decreasing ramp rate. If one assumes the validity of eq.(4.3) and fits parameters of eq.(4.3) to the experimental data shown in Figure 4.3 one extracts $|V_{RESET,min}|$=0.4 [V] and γ=0.9 $[V]^{2/3}[s]^{1/3}$. To test the physics of eq. (4.3) further, we note also that a cubic root dependence of the parameter γ on R_{on} is predicted as implied in eq.(4.2) and shown more explicitly in eq.(4.4)

To test the physics of eq. (3) further, we note also that a cubic root dependence of the parameter γ on R_{on} is predicted as implied in eq.(2) and shown more explicitly in eq.(4.4):

$$\gamma = \sqrt[3]{3 \times Q_{crit} \times R_{on}} \tag{4.4}$$

This is an important technology dependence as it allows to accelerate the rate of $|V_{RESET}|$ increase with higher R_{on} values. R_{on}, on the other hand, can be controlled by the level of applied compliance current, I_{cc}, according to the well-known relation between on-resistance R_{on} and compliance current I_{cc} [18, 32-37]:

$$R_{on} = \frac{V_{set,\min}}{I_{cc}^{n}} \tag{4.5}$$

(with n ≈ 1 for metallic CFs). The relation (5) is important for other reasons, as it enables multilevel memory applications. As stated before, the set operation conditions for data in Figure 4.3 were rr=2V/s and I_{cc} =0.1 mA. According to eq. (4.5) R_{on} can be varied by imposing different levels of the compliance current I_{cc}. In the following, the measurements of Figure 4.3 have been repeated for three different R_{on} values as shown in the 2nd column of Table 1 according to I_{cc} listed in the 1st column.

Table 4.1: Fit of the parameters $V_{reset,min}$ and γ of eq.(3) to experimental data of V_{reset} vs ramp rate for five different R_{on} values generated at five different levels of I_{cc}

I_{CC} (A)	R_{ON} (Ω)	$V_{RESET,MIN}$ (V)	γ (([V]$^{2/3}$[s]$^{1/3}$)
10^{-5}	1.7×10^{4}	0.4	1.22
3×10^{-5}	5.7×10^{4}	0.4	1.05
10^{-4}	1.7×10^{3}	0.4	0.90
3×10^{-4}	5.7×10^{3}	0.4	0.87
10^{-3}	1.7×10^{2}	0.4	0.76

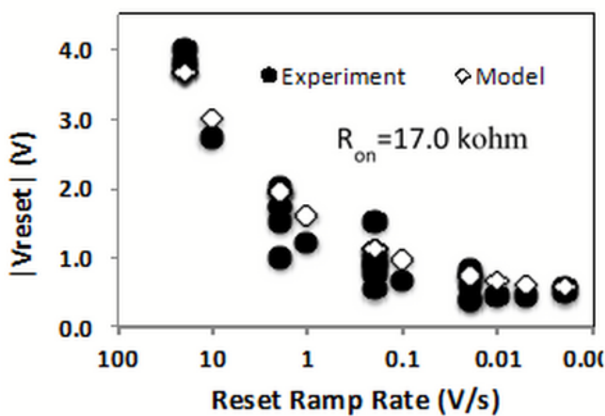


Figure 4.4 $|V_{reset}|$ as a function of voltage ramp rate for R_{on}=17.0 kΩ: experimental data and model given in eq.(4.3).

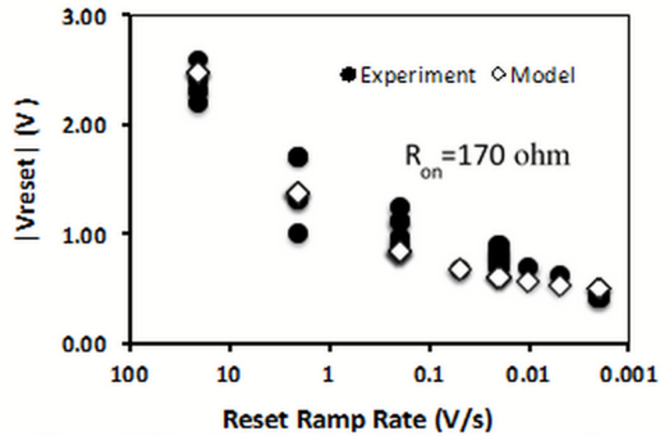


Figure 4.5 $|V_{reset}|$ as a function of voltage ramp rate for Ron=170 Ω: experimental data and model given in eq.(4.3).

The fit of eq. (4.3) to experimental data for R_{on}=17 kΩ and R_{on}=170 Ω are shown in Figure 4.4 and Figure 4.5, respectively. Both Figures show qualitatively the same behavior as displayed in Figure 4.3. The extracted parameters $V_{RESET,min}$ and γ are summarized in two last columns of Table 4.1. It can be seen that in agreement with the prediction of the model given in eq.(4.1) and eq.(4.2) the γ parameter decreases with decreasing R_{on}, while $V_{RESET,min}$ is found to be constant at $|V_{RESET,min}|$=0.4V independent of I_{cc} or R_{on}, for all three cases, giving further credence to the validity of the assumption. $V_{RESET,min}$ is the lowest voltage under which the cell is able to reset. Experimentally, it can be realized only at very slow ramps. The specific value of $V_{RESET,min}$ is characteristic for the materials of the specific resistive cell. It is, however, independent of the oxide thickness. In Figure 4.6 the γ parameter is plotted as a function of R_{on} on a double logarithmic scale. Using the following equation we can fit experimental data of Figure 4.6:

$$\gamma = \gamma_o + \sqrt[3]{3\times Q_{crit} \times R_{on}} \tag{4.6}$$

with γ_o=0.6 ([V]$^{2/3}$[s]$^{1/3}$) and Q_{CRIT}=6μJ. The agreement between the data for γ extracted from experiment and predicted behavior is eq. (4.6) is surprisingly good. Thus our experiments indicate that the macroscopic heat needed to rupture the conductive filament, in our devices, is in the range of a few of micro Joule. This value can be considered an upper boundary, for the local rupturing energy as Q_{CRIT}, according to Kirchhoff rules is the total energy dissipated in the conductive filamentary resistance R_{on} during the entire reset process. The energy needed to rupture the filament locally can be only a fraction of it. Also, in the very simple model of eq. (4.1) the electric field's action on the ions is not accounted for.

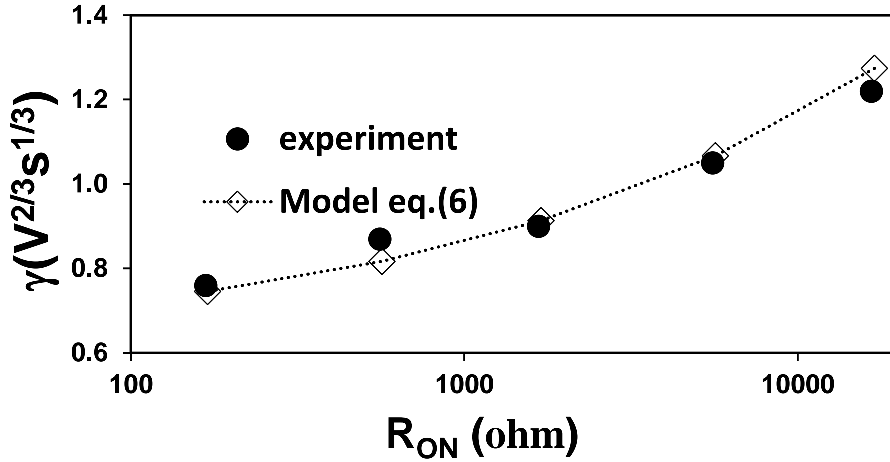


Figure 4.6: γ parameter as a function of R_{on} extracted to fit experimental data in Figs. 4.3, 4.4, 4.5. The dashed line is the model prediction given in eq.(4.6).

On the other hand, if one would assume literally that the heat is deposited during the dissipation time τ_{diss} of 1-10 ns, as reported in the literature [28,29,31] one would have to evaluate heat required for local dissolution of the filament as:

$$Q'_{crit} = \int_{V_{reset}/rr-\tau_{diss}}^{V_{reset}/rr} \frac{rr^2 \times t^2}{R_{on}} dt \approx \frac{V_{reset}^2}{R_{on}} \tau_{diss} (\tau_{diss} << t_{reset}) \tag{4.7}$$

instead of eq.(4.1). Since, in our experiments $t_{RESET}=V_{RESET}/rr$ is of order of 1-10,000 s it is vastly larger than τ_{diss} =1 ns-10 ns, Q'_{CRIT} can be approximated with great accuracy by the expression given in eq. (4.7) indicating that V_{RESET} would be independent of the ramp rate – in obvious contradiction to the experimental data. Moreover, model of eq.(4.7) could not be applied to our data since our reset operation begins always at 0 V and not at a voltage already very close to V_{RESET}. A more adequate understanding could be obtained if one would follow Chua's postulate [3], that models of I-V characteristics for resistive switching devices are devoid of predictive power and that instead a model for a memristor's set and reset operations should be expressed in

terms of flux φ and total charge q only, i.e. independent of any specific driving input. Here the flux φ as defined by Chua and given by:

$$\varphi(t) = \int_{-\infty}^{t} V(t)dt$$

encompasses the entire history of the voltage stress and q is the corresponding time integral of the current applied to the device. For a voltage-controlled memristor, flux φ is the essential variable of Chua's constitutive memristor relations [3]. One observes that boundaries for the integral in eq.(4.1) conform with Chua's postulates. Moreover, for linear voltage ramp one can find that as defined in eq.(4.1):

$$Q_{crit} \propto \frac{\varphi^{3/2} t_{reset}}{R_{ON}}$$

The above analysis indicates that the general physics and trends are captured well by the simple model in eq. (4.1). No doubt, the model could be supplemented by a one additional physics. For example, for ions to be moved in electrical field the Cu atoms need to be oxidized first which will require some time before they can be subjected to a drift in an electric field. Nevertheless, in view of the complicated chemo-, electro-, and physical reactions during the rupturing process, the simple reference of eq.(4.1) describes surprisingly well the dependence of V_{reset} on the ramp rate including the dependence on the on-state resistance, R_{on}.

4.4 Physical Significance and Application

We turn now our attention to the impact of the rupturing conditions on V_{SET} during a subsequent set operation. At the moment, when the rupturing takes place, an initial gap Δ_{init} in the CF is being created as shown in Figure 4.7 (a).

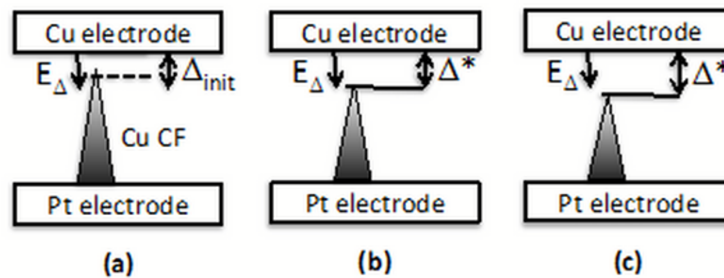


Figure 4.7. (a) Initial gap Δ_{init} of Cu CF at the time of dissolution t* ; electrical field $E_\Delta = V_{reset}/\Delta_{init}$ (b) final gap Δ* for small V_{reset} (c) final gap for large V_{reset} at t= t*+τ_{diss}.

At the same time, current collapses and the heating is immediately arrested, but the Cu^+ ions are still highly mobile during the cooling off period characterized by time τ_{diss} of the Joules heat dissipation. The final gap Δ* depends, therefore on the electrical field EΔ present in the gap during the time τ_{diss} during which the heat in the weak link of the conductive filament is being dissipated. With the rapidly decreasing temperature, the mobility of the ions will decrease swiftly and the very

high ion transport will be reduced significantly to the one that occurs at room temperature during the set operation, for example. Hence, a measure of how the initial gap widens (or how many ions are being removed) by the electric field is given by:

$$\Delta^{+} = \frac{V_{reset}}{\Delta_{init}} \times \mu_{Cu^{+}}(T) \times \tau_{diss} \qquad (4.8)$$

The final ruptured gap is given, therefore, by $\Delta^{*} = \Delta_{init} + \Delta^{+}$. The concept of Δ^{*} and Δ_{init} for small and large V_{RESET} is shown in Figure 4.7 (b) and (c). High V_{RESET} value will cause a high field in the initial gap Δ_{init} in the filament. In the short time just after the initial rupture, Cu+ ions will be still hot enough to be moved in the high field across the gap. This means that at higher V_{RESET} more Cu+ ions will be driven back to the Cu electrode resulting in a wider final gap Δ^{*} for which a dynamic model has been given [38]. A ruptured nanofilament with a larger gap Δ^{*} will require a larger subsequent set voltage V_{SET} to render the nanofilament fully conductive again, than for CF with smaller gap Δ^{*}. This is, on a much smaller spatial scale, a reflection of the linear dependence of forming voltage V_{form} on the thickness of the dielectric [39] where a relation it has been observed that $V_{form}-V_{form,min}=\alpha \cdot t_{ox}$. Here the constant α is a characteristic of the oxide material and t_{ox} is the thickness of the dielectric which for forming operation is the gap Δ^{*}. This translates into a dependence of V_{SET} as a function of the final gap of the ruptured CF:

$$V_{set} - V_{set,min} \sim \Delta^{+} = \Delta^{*} - \Delta^{init} \qquad (9)$$

From equations (8) and (9) one obtains:

$$(V_{set} - V_{set\,\min}) \sim (|V_{reset}| - |V_{reset\,\min}|) \qquad (10)$$

The relation (10) is in qualitative agreement with experimental data as shown in Figure 4.8. Figure 4.8 shows essentially the same relation between V_{SET} and V_{RESET} as Figure 4.2.

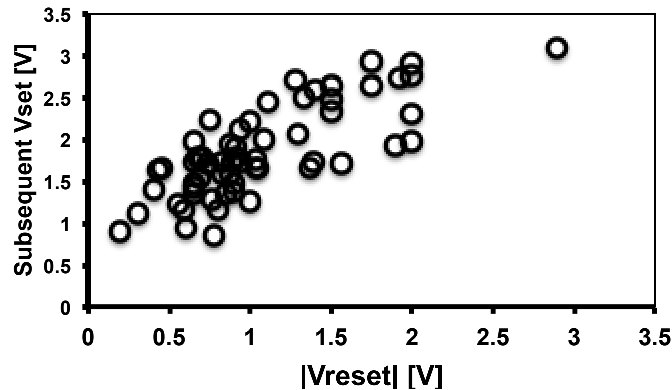


Figure 4.8 V_{set} versus $|V_{reset}|$ measured on the same device. The spread in the V_{reset} values has been generated by different ramp rates applied during the reset operation.

However, while data in Figure 4.2 is a result of many different cells contributing (V_{RESET}, V_{SET}) pairs for fixed reset conditions, Figure 4.8 is a collection of (V_{RESET}, V_{SET}) pairs for one and the

same device, where the spread in V_{RESET} has been generated by application of different ramp rates during the reset operation. The impact of the reset ramp rate on V_{RESET} and via V_{RESET} on V_{SET} can be used to tighten the V_{SET} and V_{RESET} distributions for the case when linear voltage ramp is being used. Since, in a memory array application the devices would be programmed and erased by pulses and not by voltage sweeps, this method of tightening the threshold voltage distributions would be commercially irrelevant.

However, even for so-called rectangular pulses it takes always a finite time for the leading and trailing edge of the pulse to go from logical 0 (low voltage) to logical 1 (high voltage) and back from 1 to 0, respectively. The non-vanishing transition time for the pulse edges amounts essentially to a fast voltage sweep, especially when the total pulse time width is kept at a minimum time in order to expedite high-speed programming. It should be also kept in mind that leading (and trailing) edges of the pulse are not always well controlled, nor even exactly repeatable. Moreover, based on the present analysis, other pulse parameters such as edge non-linearity, jitter, preshoot, overshoot, ringing and settling time of the pulse are liable to affect actual V_{RESET} values. Thus, in such broadly defined scope of voltage sweeps, and given a large spread of initial V_{SET} values, one could reset the devices with high V_{SET} at a lower ramp rate than devices with low V_{SET} values. The subsequent set operations on the devices would result in tighter distributions for V_{SET} and V_{RESET}.

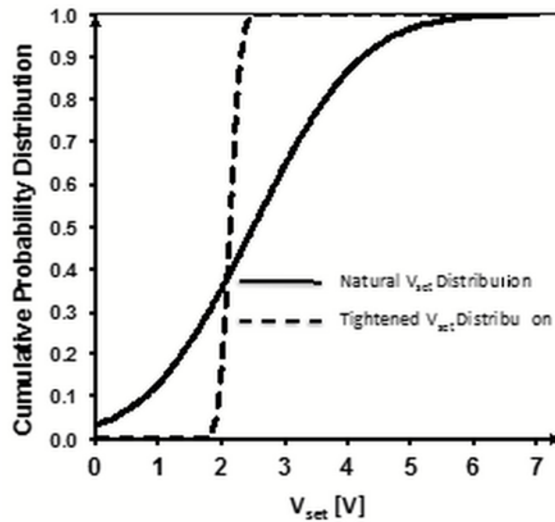


Figure 4.9 Experimental smoothed cumulative V_{set} distributions for the natural data (solid line) and for the tightened distribution after the tightening procedure using different reset voltage ramp rates.

A rather academic example of the tightening procedure is demonstrated in Figure 4.9 where smoothed cumulative V_{SET} distributions are shown for the natural V_{SET} distribution and the distribution after the tightening procedure. The natural distribution has been chosen somewhat excessively, but not unrealistically, broadened to demonstrate the tightening effect. The raw experimental data consisted essentially of three clusters of V_{SET} values: (i) centered on V_{SET}=1.0V,

(ii) centered on V_{SET}=3.8V, and (iii) data lying in-between. For the natural distribution, the mean value and standard deviation are $V_{SET,m}$=2.5V and σ=1.35V, respectively and shown in Fig 10(a). The devices of cluster (i) underwent a reset operation at ramp rate 1V/s, the devices of cluster (ii) at a ramp rate of 1mV/s, while devices with natural V_{SET} in-between have been reset at 10mV/s. After this very simple and not further optimized procedure, a very tight distribution has been obtained with $V_{SET,m}$=2.13V and σ = 0.14V as seen in Figure 4.9.

The raw data for the tightened distribution is shown in Figure 4.10(b). A repeated application of the procedure shows that, after V_{SET} distribution has been compacted, the subsequent V_{RESET}

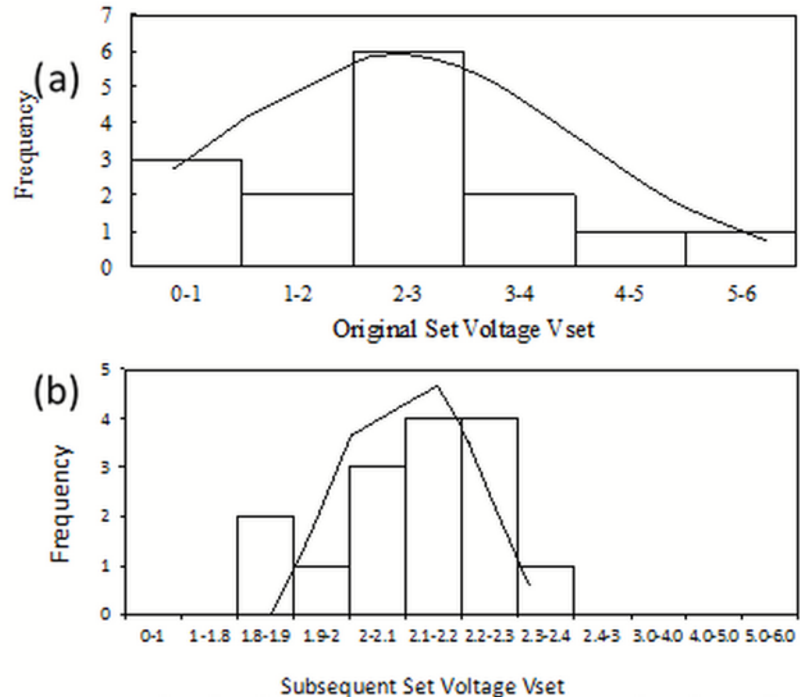


Figure 4.10 raw data for Figure 4.9: a) histogram of frequencies of set voltage values for the natural distribution. b) histogram of frequencies of set voltage values for the tightened distribution. In both cases solid line indicates the respective normal distribution.

distribution is already tight even when the same uniform reset ramp rate is applied to all cells. This is could be of practical importance because it means that once the distribution has been tightened using different ramp rates the subsequent set and reset distributions will remain tight or become even tighter under subsequent applications of uniform set and reset conditions to all cells.

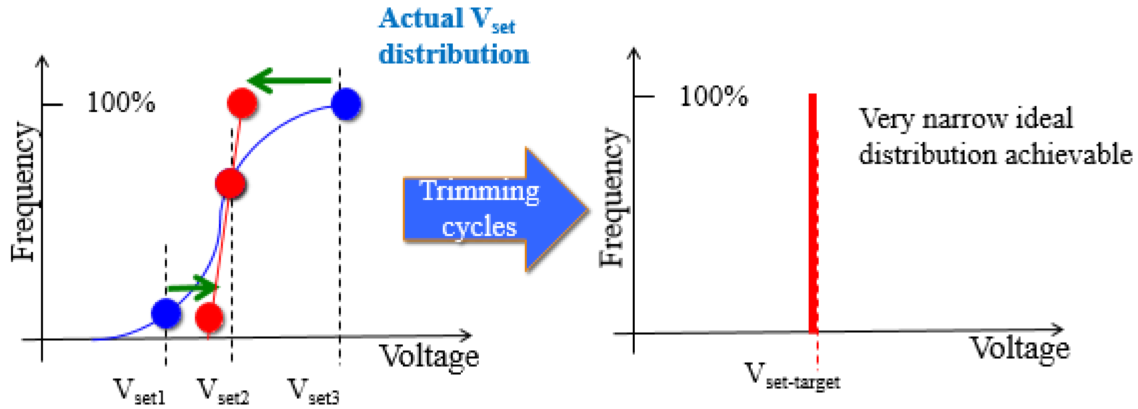


Figure 4.11: Schematic Representation of the Proposed Technology

Figure 4.11 illustrates a more interactive mode for tightening an array of memory cells. This figure gives a general idea on how the tightening operation can be carried out on a set of devices. This lasting tightening effect is demonstrated in Figure 4.12 and Figure 4.13. An array of fresh cells has been subjected to forming operation first. Subsequently, all the cells have been reset at uniform ramp rate of rr=0.2V/s. The resulting reset distribution is shown as curve 1 in Figure 4.12. It can be seen that distribution is rather broad. Subsequently, the cells have undergone a set operation at uniform rr=0.2V/s and at I_{cc}=0.1mA.

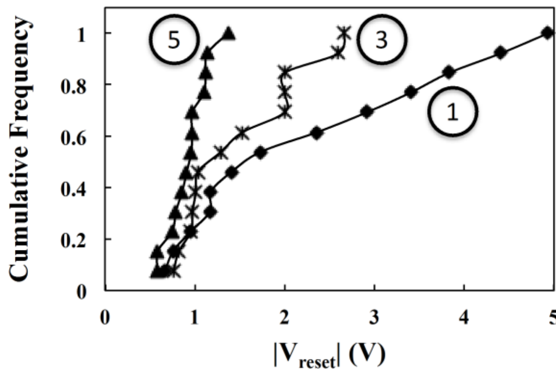


Figure 4.12. V_{reset} distributions. 1 denotes V_{reset} distribution after the first reset operation following the forming operation, the reset operation is done at uniform ramp rate of rr=0.2V/s; 3 denotes V_{reset} distribution after the 2nd trimming reset operation at variable ramp rate; 5 denotes 3rd V_{reset} distribution after 3rd reset operation at a uniform ramp rate of rr=0.2V/s.

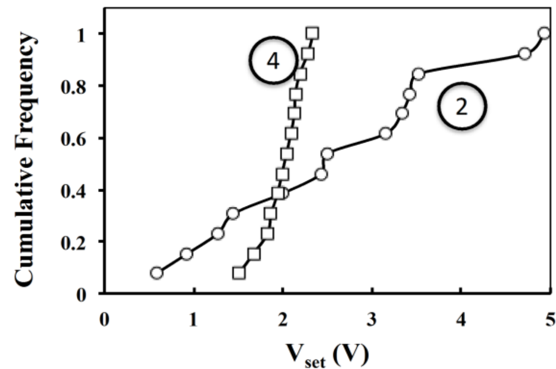


Figure 4.13. V_{set} distributions. 2 denotes V_{set} distribution after the first set operation, the reset operation is done at uniform ramp rate of rr=0.2V/s; 4 denotes V_{set} distribution after the 2nd set operation following the trimming reset (distribution 3 in Figure 4.12) at a uniform ramp rate of 0.2V/s.

The resulting set distribution is shown in Figure 4.13 as curve 2. V_{SET} distribution 2 is also rather broad. After the set operation, the cells have been subjected to a trimming reset operation with variable ramp rates as described in the context of Figure 4.9. Cells with high V_{SET} values have been

reset at a low ramp rate and cells with low V_{SET} values have been reset at high ramp rate. The ramp rate used ranged from 0.01V/s to 20V/s. The resulting (trimmed) reset distribution is tight and is shown as curve 3 in Figure 4.12. To demonstrate the convergence effect of the tightening procedure, all cells have now been from the on-set at a uniform ramp rate of 0.2V/s as in the case of distribution 2. However now, the resulting V_{SET} distribution becomes very tight as shown in curve 4 in Figure 4.13.

Memory cells conditioned in such a way can be now reset again at a uniform ramp rate of 0.2V/s resulting in a very tight V_{RESET} distribution 5 shown in Figure 4.12. All subsequent set and reset operations at uniform set and reset conditions result in similarly tight or even tighter V_{SET} and $|V_{RESET}|$ distributions. This means that the tightening operation has to be performed only once, and leads to a self-sustaining convergence to very tight V_{SET} and $|V_{RESET}|$ distributions, in other words, both V_{SET} and V_{RESET} distributions converge to tighter distributions. It is of interest to explore how this mechanism would impact $|V_{RESET}|$ values for pulses with different leading edge properties which is beyond the capabilities of our Keithley 4200-SCS equipment.

4.5 Summary

In summary, an experimentally observed dependence between V_{SET} and V_{RESET} values for subsequent set and reset operations has been reported. This dependence has been observed for (V_{SET}, V_{RESET}) pairs of different devices and also by a single device whereby the spread in V_{RESET} has been introduced by different reset ramp rates. A model for the V_{RESET} as a function of the ramp rate has been proposed under the premise that there is a critical macroscopic Joules heat, defined in terms of external macroscopic variables, the applied voltage and resistance of the filament R_{on}, needed to rupture the conductive filament. This very simple model describes the general dependence surprisingly well and predicts moreover the dependence of V_{RESET} on the on-state resistance, R_{on}, of the device, which has been fully borne out by subsequent measurements. The discrepancy of, at least, ten orders of magnitude between the very short heat dissipation τ_{diss} (ns) and very long reset time t_{RESET} (100 s) has been discussed and it has been pointed out that an adequate description of a memristive device should be undertaken within the scope of Chua's memristor theory which postulates the dependence of the memristor conductance on the voltage flux, which is a time integral of the voltage waveform for the entire time interval $(0,t_{RESET})$ of the reset operation. The dependence of subsequent V_{SET} on the preceding V_{RESET} has been explained in terms of the gap in the filament generated by the rupturing process. The $V_{SET} \sim V_{RESET}$ dependence can be leveraged, theoretically, to tighten the V_{SET} and V_{RESET} distributions. Although, the method has been demonstrated only for a linear voltage sweep, it has been pointed out that it may be of relevance for pulse programming, as any pulse is characterized by a finite leading edge that can be viewed as a fast voltage ramp. Clearly, more work in this area is needed to assess the effects of pulse parameters other than mere pulse height and pulse width, over the resulting V_{RESET} distributions.

Chapter 5: Impact of Electrode, Metal and Material on the Formation and Rupturing of Conductive Filament

5.1 Introduction

The field of resistive switch memory devices has become a growing avenue for research in industry as well as in academia. In spite of the great developments made, there are certain aspects still little understood and unexplained. In an attempt to understand the interplay of various kinds of electrodes and dielectrics in resistive switches, four new interconnect structures were fabricated and characterized. The motivation behind this experiment was to bridge the gaps of understanding between the standard Cu/TaO_X/Pt devices and the possibility of incorporating similar structures in a back-end-of-line CMOS process.

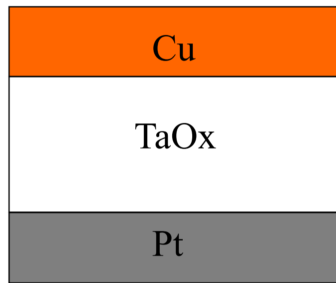


Figure 5.1 – Standard Cu/TaO_X/Pt device structure. Our traditional resistive switching devices displaying "clean" resistive switching for both, Cu and V_o filaments. This device is "well" understood and serves as a benchmark for the following cells.

Modern day interconnect structures use frequently Ta and Ti as Cu diffusion barrier and as glue layers. In this chapter we are trying to understand how each of Ta and Ti electrodes would impact the resistive switching performance. In our experiments we, keeping Cu/TaO_X/Pt as a benchmark, and in these derivative cells, only one electrode is being changed at a time.

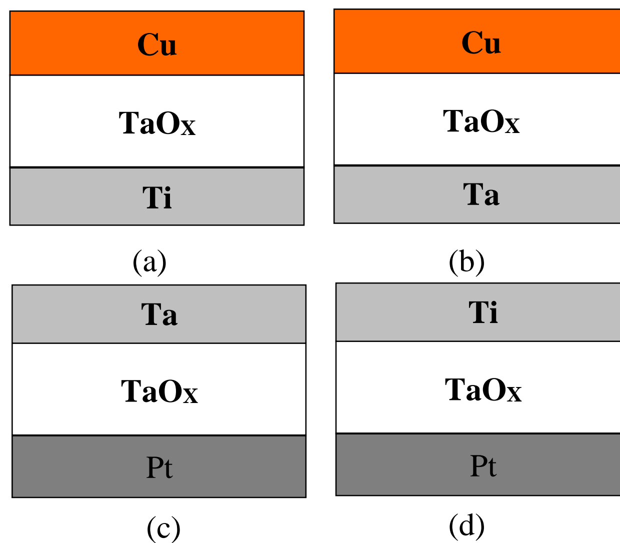


Figure 5.2: Derivative Devices (a) Cu (150nm) / TaOx (40nm)/ Ti (80nm) (b) Cu (150nm) / TaOx (40nm)/ Ta (50nm) (c) Ta (70nm) / TaOx (40nm)/ Pt (60nm) (d) Ti (50nm)/ Ta_2O_5(16nm)/ Pt (60 nm)

Figure 5.2 (a)-(d) gives us the schematic representation of the different devices that have been fabricated. The devices undergo basic voltage sweeps for characterization and conclusions have been derived from the results accordingly.

Cu and Pt are known to be an ideal active and inert electrode respectively. By switching one of them to Ti or Ta would help us to observe finer nuances of I-V switching characteristics. From the switching characteristics we can infer which mechanisms are important in resistive switching. This insights should equip us with a roadmap for a suitable material choice to realize resistive switching devices that can be implemented in the back-end CMOS process. The conclusions derived from this section can be utilized for more advanced interconnect structures.

5.2 Cu/TaOx/Ti Device

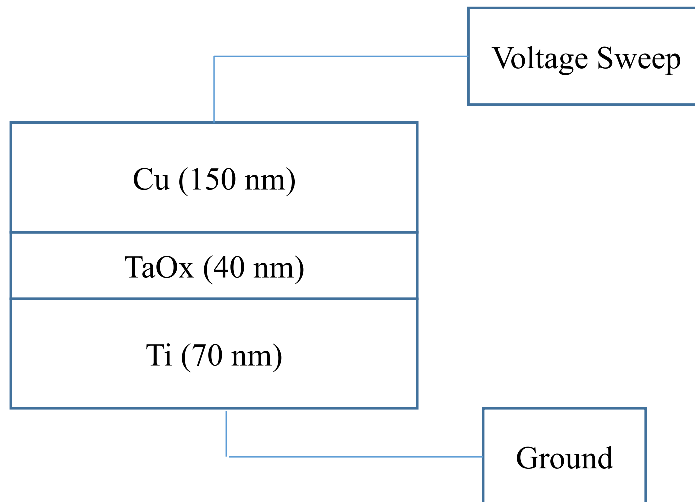


Figure 5.3: Experimental Set - Up

Figure 5.3 illustrates the experimental set up. We stress the device with positive and negative bias consecutively and make appropriate conclusion.

Positive Voltage Sweep

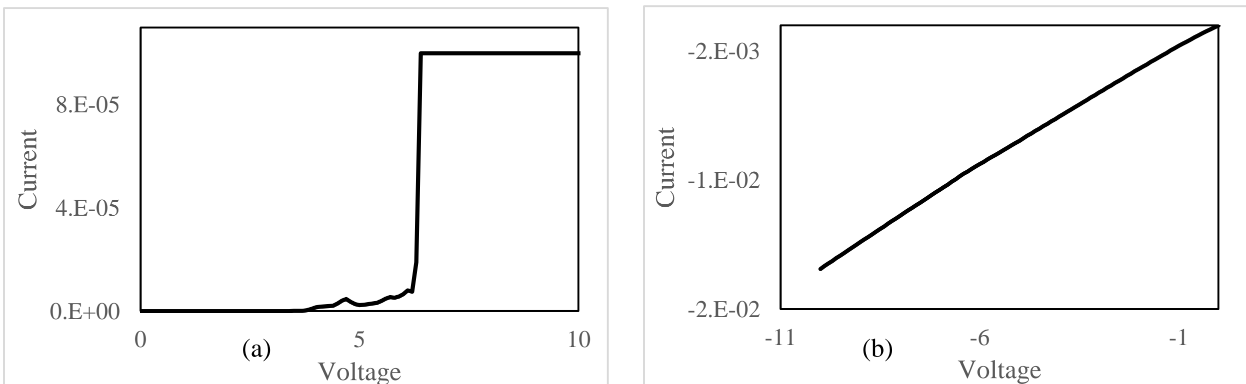


Figure 5.4: I-V Characteristics for positive sweep (a) SET (b) RESET

The SET and the RESET I-V Characteristics are given in Figure 5.4. It is evident that the forming voltage is approximately around 6V which is similar to a typical Cu/TaO_X/Pt device with 40nm dielectric. However it goes through a permanent dielectric breakdown, and hence cannot switched back to a low resistive state. This observation was made a compliance current of 0.1 mA and R_{ON} was found to be 570Ω. This motivated to develop a study of the variation of R_{ON} with respect to $I_{CC.}$ Table 5.1 summarizes our findings.

Table 5.1: Variation of R_{ON} with I_{CC}

Icc (mA)	Ron (Ω)	State of Conductive Bridge
0.01	250000	Volatile
0.05	400	Permanent
0.1	560	Permanent
0.5	753	Permanent
1	983	Permanent

Characterization carried out a $I_{CC} \leq 0.01$ mA led to the formation of a volatile conductive filament which disintegrate as soon as the device is unpowered and has a very high RON. For ICC > 0.05 mA, a conductive bridge is stable but leads to a permanent dielectric breakdown as discussed earlier, i.e. the cell is permanently damaged. In Cu/TaOx/Pt devices a permanent damage is also observed but only at large compliance currents I_{CC} (> 1mA). According to the model discussed before, at large I_{CC} we would expect a more cylinder-like shape of the filament. In Figure 5.5 the R_{ON} resistance is plotted as a function of a compliance current on a linear and on logarithmic scale.

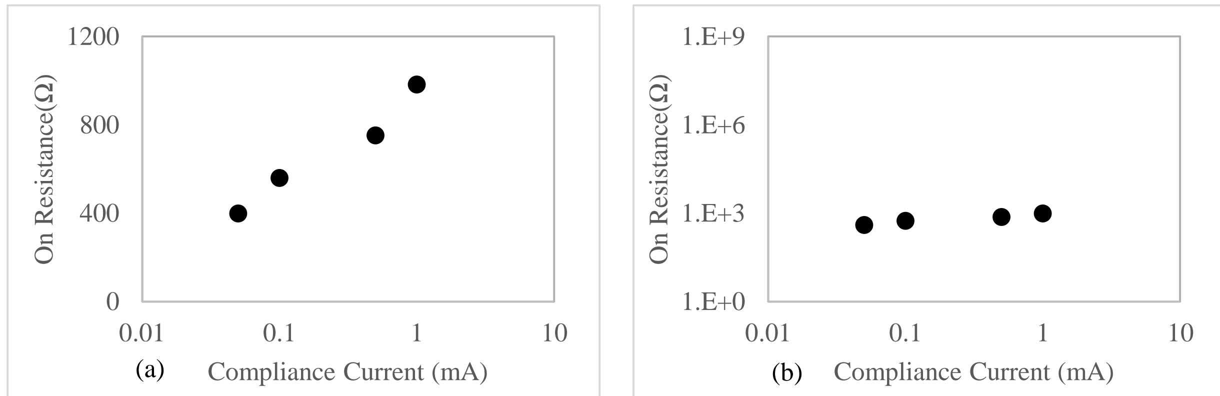


Figure 5.5: Variation of R_{ON} with I_{CC} (a) R_{ON} on a linear scale (b) R_{ON} on a logarithmic scale

The observed behavior is stark contrast to the results obtained for Cu/TaO_X/Pt devices, see Figure5.6 for Cu filaments and Figure 3.3 in chapter 3 for V_O filaments. R_{ON} was expected to decrease with the increase of I_{CC} but opposite behavior is being observed: Ron increases slightly with Icc. This compels us to infer that the building mechanism and structure of the conductive

filament in the case of Cu/TaO_X/Ti device is very different to that of our standard resistive memory devices Cu/TaOx/Pt.

In a Cu/TaO_X/Pt electrode, the conductive filament being conical in structure, an increase in compliance current brings about an increase of the cone radius at the top of the truncated cone. Due to this the apex of the cone's top increases laterally which decreases the R_{ON}. At some threshold voltage, this the diameter of conductive filament becomes so large, that it fails to generate critical heat (critical temperature) necessary to rupture the nanofilament. This effect has been portrayed in Figure 5.6.

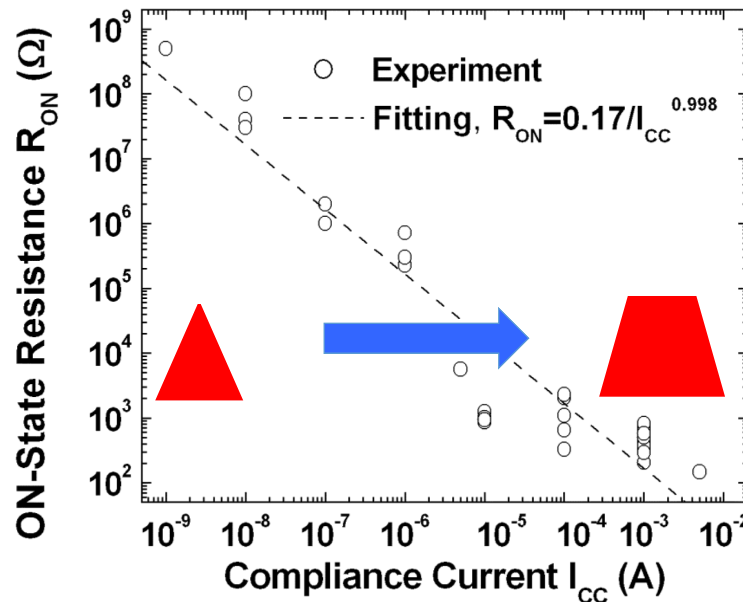


Figure 5.6: CF Structure with increasing I_{CC} in a Cu/TaO_X/Pt device.

As mentioned before filaments with a truncated cone shape approaching that of a cylinder are difficult or impossible to rupture. Figure 5.7 shows the hypothesized difference in the structure of the conductive filament formed in Cu/TaO_X/Pt and Cu/TaO_X/Ti respectively.

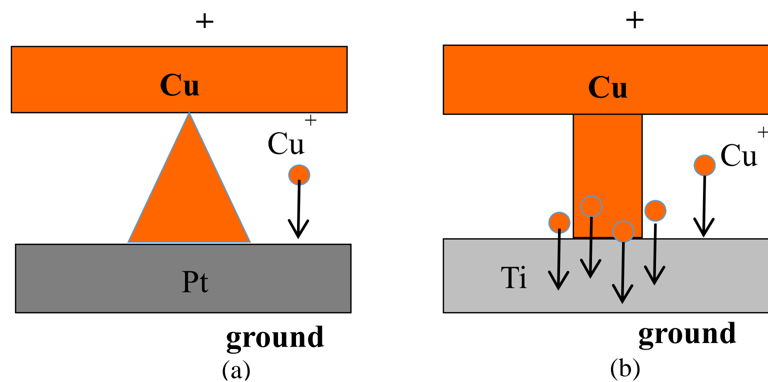


Figure 5.7: Supposed Conductive filament structures (a) Cu/TaO_X/Pt (b) Cu/TaO_X/Ti

Possible explanation: In Cu/TaO_X/Pt, the inert electrode Pt as an inert metal does not allow dissolution of Cu atoms in Pt, forcing the Cu filament to assume a more or less conical shape. The conical shape is conducive to rupturing at the top of the cone, because the largest part of resistance resides at the top. However, in the case of Cu/TaO_X/Ti device, Ti does not prevent Cu^+ ions dissolution into the Ti electrode, hence no broad base is being formed at Ti electrode; the filament assumes a more or less cylindrical shape. A cylindrical resistor does not have a conspicuous constriction characterized by a high resistance. Therefore it is more likely that the filament cannot be ruptured at all. This also explains the stable nature of R_{ON} as I_{CC} is increased as shown in Figure 5.5(b). The filament structure already being a cylinder, does not provide the scope of further addition of ions alongside the walls of the filament.

Negative Voltage Sweep

The I-V characteristic have been given in Figure 5.8. The permanent dielectric breakdown is again evident from the figures below.

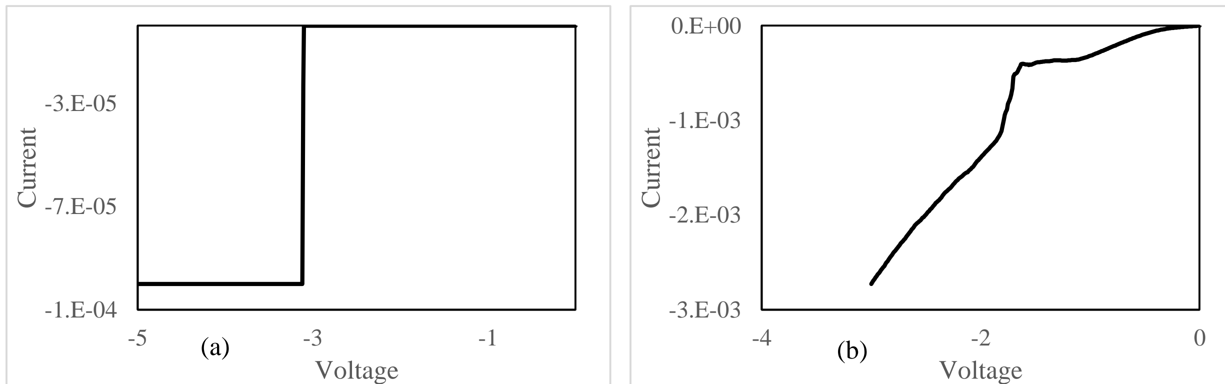


Figure 5.8: I-V Characteristics for negative sweep (a) SET (b) RESET

The plot again confirm similar behavior. A conductive filament was formed which damaged the dielectric permanently.

Possible explanation: We can thus hypothesize that, at negative bias a setting behavior is observed. In analogy to the Cu/TaOx/Pt devices we are explaining this tentatively by formation of oxygen vacancy filaments.

In contrast to Cu/TaOx/Pt devices, the Cu/TaOx/Ti cells cannot be ruptured and are permanently damaged. There is a possible explanation of this phenomenon. In case of Cu/TaOx/Pt, the inert Pt electrode, forces oxygen ions to accumulate at the bottom. In case of Ti cells, Ti serves as a gettering site for oxygen. In other words, the high oxygen affinity that Ti bears, compels it to settle down in the form of TiO_2. This, in turn, weakens the base of filament comprised of oxygen vacancies. Thus, similarly as in the case of Cu filament the more cylindrical shape of the filament renders it difficult to rupture.

Another hypothesis would be that the conductive filament is due to Ti^+ ions. Here, also, because Cu is not an inert electrode Ti ions would not stop at Cu interface but dissolve into Cu. Thus, a Ti filament would result in a cylinder-like shape which is difficult to be ruptured.

5.3 Cu/TaOx/Ta Device

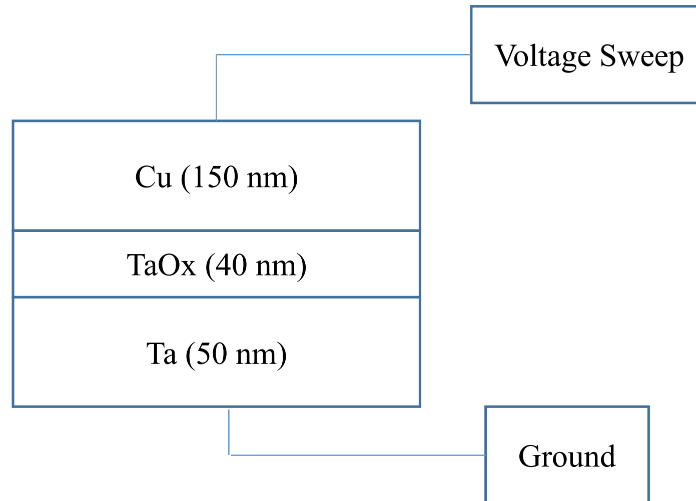


Figure 5.9: Experimental Set - Up

Figure 5.9 illustrates the experimental set up. We stress the device with positive and negative bias consecutively and make appropriate conclusion.

Positive Voltage Sweep

We attempt to analyze the SET and RESET I-V characteristics consecutively. The characteristics have been shown in Figure 5.10.

The device can be set as shown in Fig 5.10(a) at about 4V. But the reset characteristics looks very erratic and noisy. Figure 5.10 shows the switching characteristics of the same devices performed two times. It brings forth the fact the even without the presence of an absolute stopping electrode Pt, some unreliable form of resistive switching was observed. It is also worthwhile to mention that a device upon being tested multiple number of times would fail to demonstrate resistive switching. This makes us conclude that the conductive bridge formation can be achieved but is highly unreliable and stochastic. Repeated set-reset switching leads to permanent dielectric breakdown. Nevertheless a phenomenon makes this device a potential candidate in memory device application.

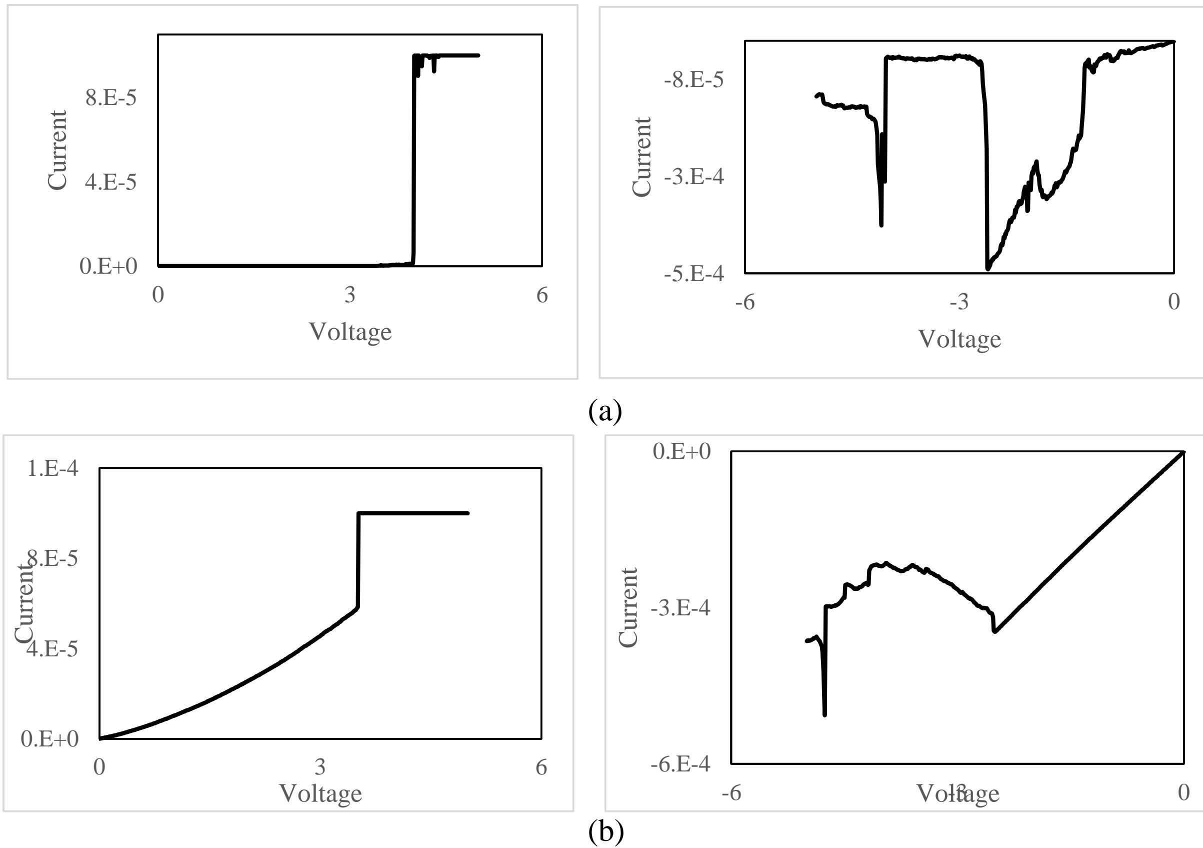


Figure 5.10: I-V Characteristics for positive sweep (a) SET/RESET 1 (b) SET/RESET 2

Possible explanation: Cu/TaOx/Ta cell is similar to Cu/TaOx/Ti cell and all the mechanism discussed for the Ti cell apply here. However, the diffusion of Cu into Ta is less pronounced then Cu into Ti.

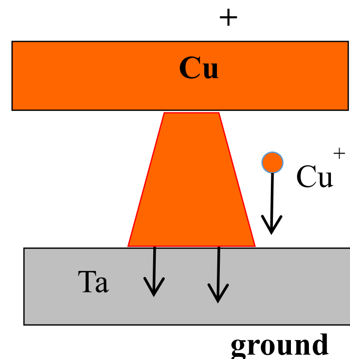


Figure 5.11: Supposed Conductive filament structures for Cu/TaO_X/Ta device

Figure 5.11 shows the hypothesized structure of the conductive filament for a Cu/TaO_X/Ta device. As opposed to Figure 5.6 (a) and (b) the conductive filament in all probability is less “conical” than that of Cu/TaO_X/Pt. Ta does not stop Cu+ ions very well, hence no broad base is being formed an Ta electrode; However, Ta has a higher stopping power for Cu as opposed to Ti. Since Ta is not an entirely inert electrode, we also do not observe reliable form of switching. Hence, the shape

is still truncated cone-like but close to a cylinder. Therefore, the device shows some tendency to reset (rupture).

Negative Voltage Sweep

We see some unreliable resistive switching as manifested in the I-V characteristics given in Figure 5.12. Figure 5.12 (a) gives the typical SET characteristics and (b) and (c) are two independent examples of attempt to RESET the bridge. It is evident that in Figure 5.12 (b), that the bridge shows some traits of the resistance switching back to HRS, although ultimately it undergoes through a permanent dielectric breakdown. In Figure 5.12 (c), a clear dielectric breakdown can be observed.

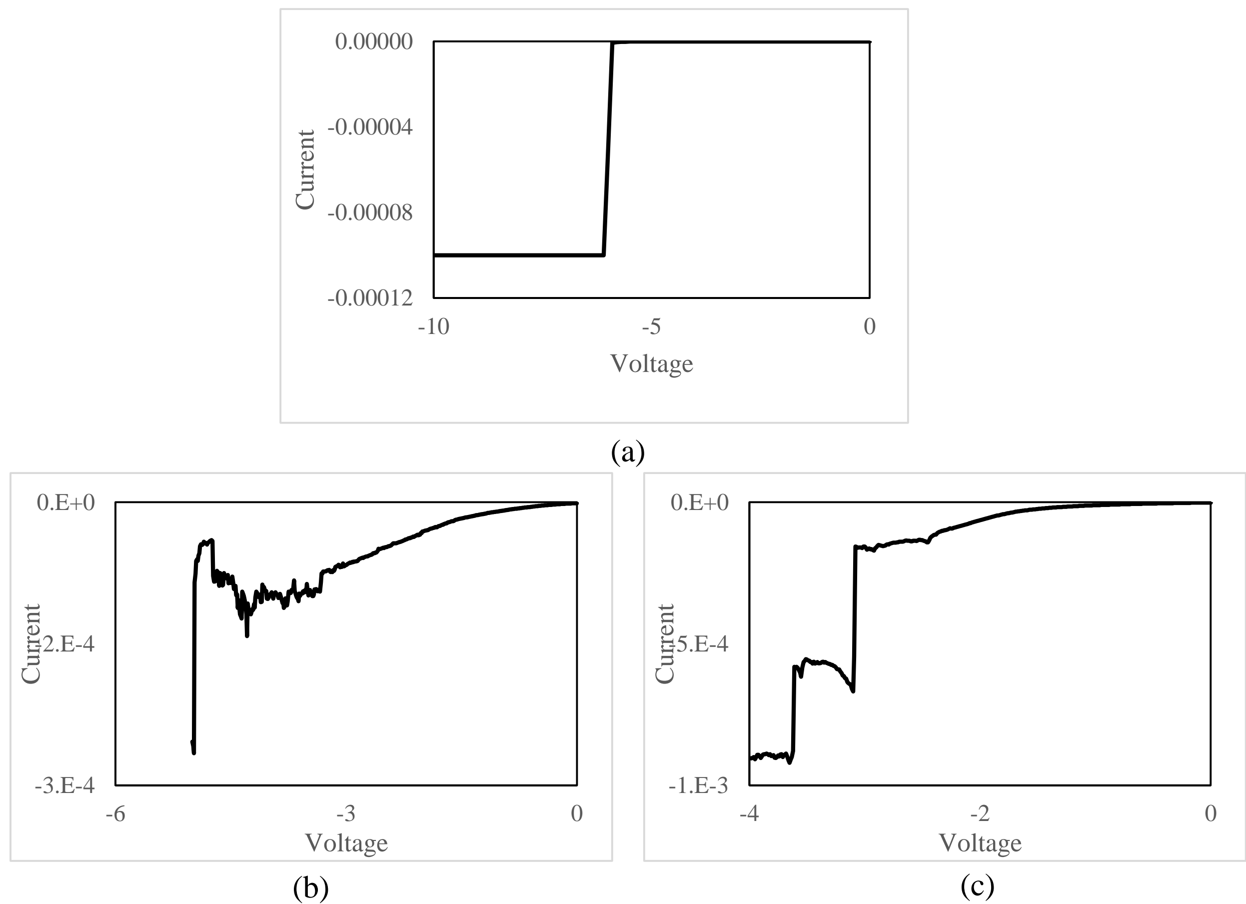


Figure 5.12: I-V Characteristics for negative sweep (a) SET (b) RESET 1 (c) RESET 2

Possible explanation: At negative bias a setting (resistive switching) behavior is observed. In analogy to the Cu/TaOx/Pt devices we are explained tentatively by formation of oxygen vacancy filaments. In contrast to Cu/TaOx/Pt devices, the Cu/TaOx/Ta cells cannot be ruptured and are permanently damaged. There is a possible explanation of this phenomenon: In case of Cu/TaOx/Pt, the inert Pt electrode, forces oxygen ions to accumulate at the bottom. In case of Ta cells, Ta serves as a gettering site for oxygen, but somewhat less efficiently than in the case of Ti cells. This, in turn, weakens the base of filament comprised of oxygen vacancies. Thus, similarly as in the case of Cu filament the more cylindrical shape of the filament renders it difficult to rupture. Therefore Cu/TaOx/Ta cells show some tendency to reset.

Another hypothesis would be that the conductive filament is due to Ta^{+} ions. Here, also, because Cu is not an inert electrode Ta^{+} ions would not stop at Cu interface but dissolve into Cu. Thus, a Ta filament would result in a cylinder-like shape which is difficult to be ruptured.

5.4 Ta/TaOx/Pt Device

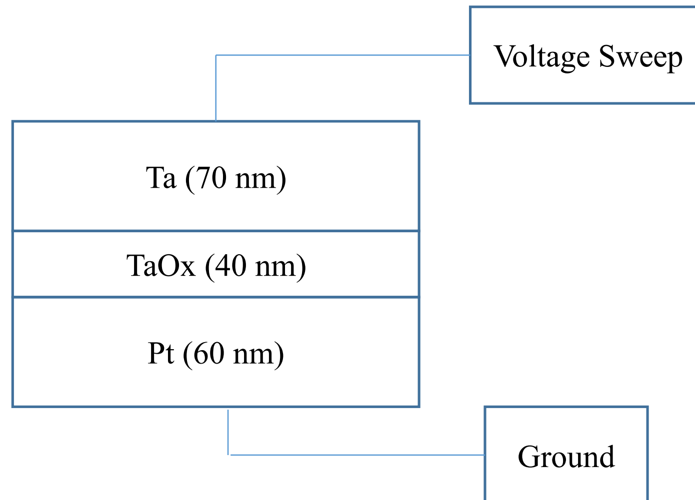


Figure 5.13: Experimental Set - Up

Figure 5.13 illustrates the experimental set up. We stress the device with positive and negative bias consecutively and make appropriate conclusion.

Positive Voltage Sweep

We attempt to analyze the SET and RESET I-V characteristics consecutively. Figure 5.14 gives the basic idea for such procedures.

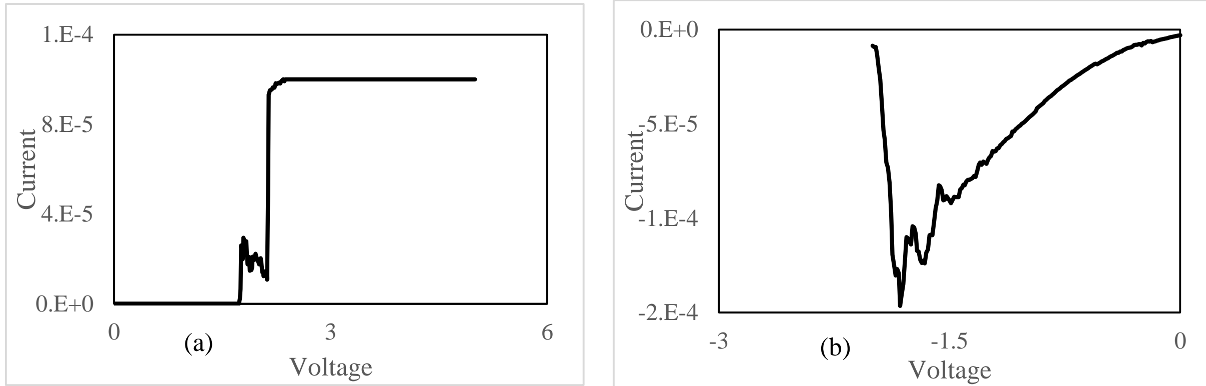


Figure 5.14: I-V Characteristics for positive sweep (a) SET (b) RESET

The results obtained from the I-V characteristics are similar to what we expected. Due to the presence of a stopping electrode, this device exhibits resistive switching. However, similar to the previous device, the switching is unreliable and a devices would be unable to exhibit consistent resistive switching more than a couple of times. The other interesting observation made from the figures above is the quasi ohmic nature of the RESET characteristics.

Possible explanation: Such characteristics are exhibited due to formation of Ta filament. Ta^{+} ions are stopped at the inert Pt electrode and a cone-like shape of a filament is produced. Ta filament appears to be less stable than corresponding Cu filaments and it displays quasi ohmic behavior during reset. The device can reset but is not as "clean" as in case of Cu/TaOx/Pt devices. The reason for this could be related to an interplay of two effects. On the one hand,Ta diffuses much easier in TaO_X which is inherently oxygen deficient, than Cu. On the other hand, the redox reaction $Ta \rightarrow Ta^{+} + e^{-}$ is much less efficient (higher activation energy) than $Cu \rightarrow Cu^{+} + e^{-}$. The first mechanism provides for a quick transport of Ta^{+} ions across the dielectric, while the second mechanism provides very limited supply of Ta^{+} ions. Thus both mechanisms work at cross-purpose producing fragile filaments and erratic switching behavior.

Negative Voltage Sweep

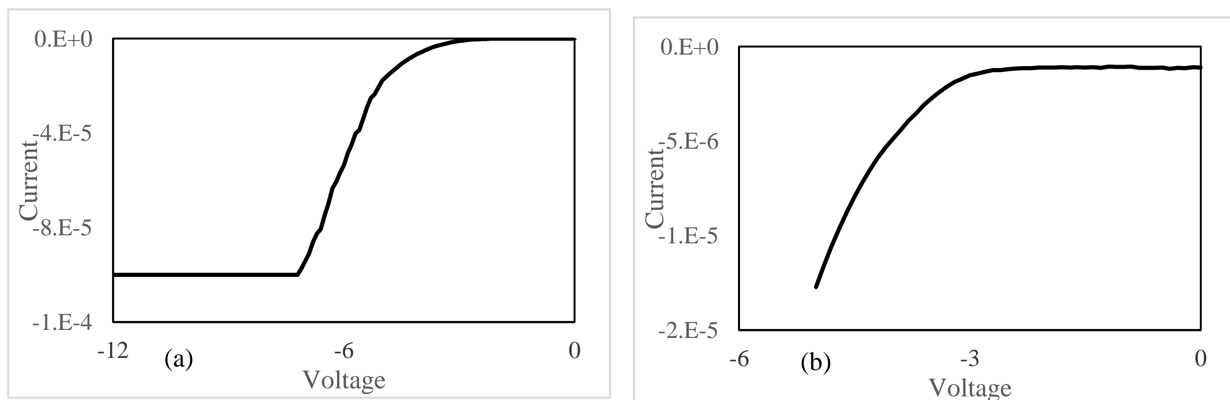


Figure 5.15: I-V Characteristics for negative sweep (a) SET (b) RESET

The volatile nature of the conductive filament can be observed in Figure 5.15. In the set operation, the current increases gradually and no abrupt resistance transition can be observed. It is clear that the conductive formed during the SET operation disappears as soon as the device is unpowered and hence during the RESET Operation, the devices behaves like a fresh one. Thus we do not observe any abrupt formation of a conductive path via oxygen vacancies. This device is no candidate for resistive switching.

Possible explanation: Due to the weak redox reaction occurring at the interface of Ta and TaO_X, there is no efficient mechanism to form mobile oxygen ions therefore there is no mechanism to produce a self- accelerating mechanism to build a stable oxygen vacancy filament. The increased conduction is an effect of randomly created oxygen vacancies in the bulk of TaO_X. With no electric field applied the percolative path collapses. Thus it can be concluded, that Ta/ TaO_X/Pt can serve as a potential candidate for memory application owing to its characteristics of resistive switching for Ta filament formation. The presence of a stopping electrode like Pt makes it easier for the migrating Ta^+ ions to form a conductive path through the electrode. It also facilitates in the formation of a conical structure which can be disintegrated through Joule's heating by application of a high current.

5.5 Ti/Ta_2O_5/Pt Device

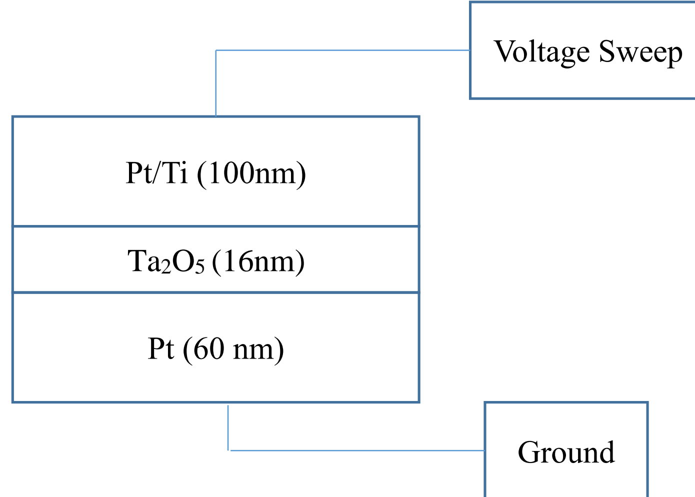


Figure 5.16: Experimental Set - Up

Unlike the previous samples, in this sample, the dielectric Ta_2O_5 has been deposited through ALD. Hence this layer is stoichiometric and thus far less oxygen deficient as the PVD TaO_X. Figure 5.16 illustrates the experimental set-up.

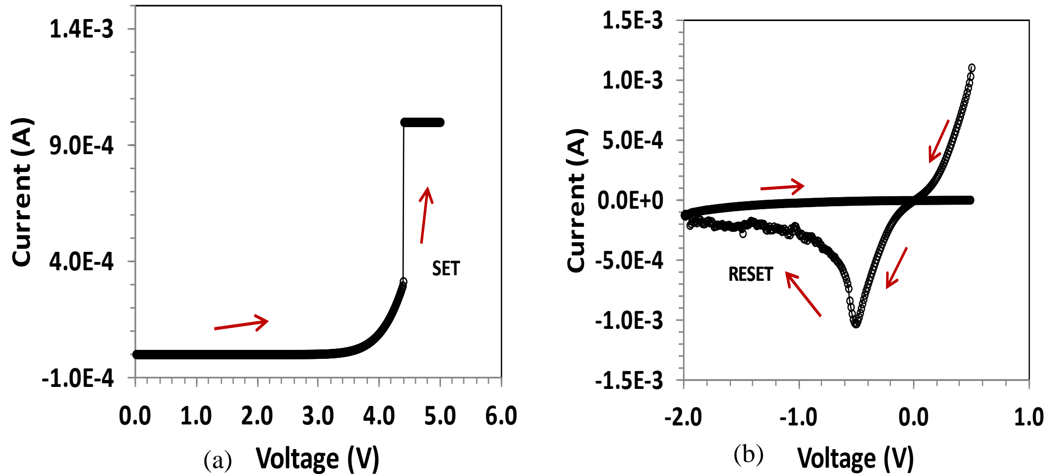


Figure 5.17: I-V Characteristics for positive sweep (a) SET (b) RESET

Figure 5.17, presents the SET and the RESET phenomenon for Ti/Ta_2O_5/Pt device. Again, similar to the previous sample, these devices also exhibit an unreliable form of resistive switching. The reset characteristics indicate the quasi ohmic nature of the conductive filament. Thus, Ti/TaOx/Pt devices display some extent of resistive switching; it can be formed, reset, and set again. However a second reset leads in most cases to a permanent damage.

Possible explanation: Ti undergoes a weak redox reaction. It is expected that some Ti^+ ions migrate through Ta_2O_5 and are stopped at the inert electrode Pt. However, since Ti is known to

have a strong affinity for oxygen, many of Ti^{+} ions undergo a local oxidation reaction in Ta_2O_5 creating a complex compound of the form $Ta_{2-X}Ti_XO_5$, which is apparently stable implying that it is relatively difficult to extract Ti^{+} atoms back from the Ta_2O_5 oxide. Therefore it is difficult to rupture such a Ti filament which is strongly anchored in the oxide matrix.

Negative Voltage Sweep

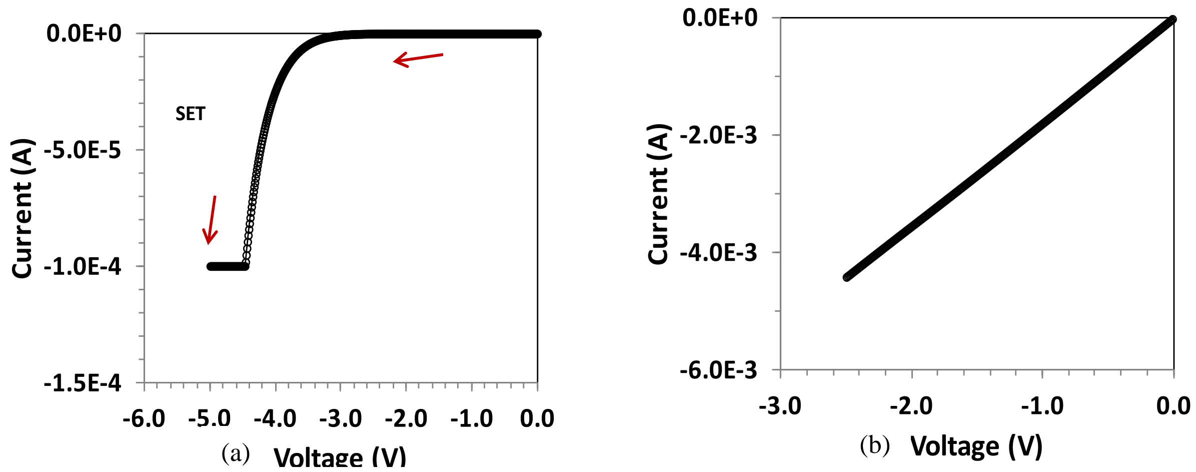


Figure 5.18: I-V Characteristics for negative sweep (a) SET (b) RESET

The gradual nature SET characteristics in Figure 5.18 (a) generally indicates a volatile filament. However, on characterizing for reset, it was observed that the dielectric was permanently damaged.

Possible Explanation: As explained in the previous section, Ti being a getter for oxygen, is trapped in the dielectric, while migrating from one electrode to another. The complex compound $Ti+Ta2O5 \rightarrow Ta_{2-X}Ti_XO_5$ reaction is difficult to reverse and that is why we observe the ohmic nature in the reset characteristic with no indication of a rupturing of the filament.

5.6 Summary

A consistent picture emerges out of the filamentary resistive switching observed in the samples studied under this chapter.

- In order to realize resistive switching by metallic conductive filaments, a device must have an efficient active electrode. Active electrode enables metallic filament formation and is a necessary but not a sufficient condition for such resistive switching.
    - Among tested metals, Cu renders the best achievable results owing to its lower ionization potential: $Cu \rightarrow Cu^{+} + e^{-}$.
    - Ta has the properties of an active electrode but is not as efficient as Cu. It tends to provide less of the ions which provide the building blocks for the filament. This leads to resistive switching, however very unreliably.

    - Ti is somewhat more active than Ta. Like Ta it lacks the ability to readily render ions to form the conductive filament.
- The other important condition for a device to be able to exhibit resistive switching is having an inert electrode. This electrode acts as the stopping and diffusion barrier that inhibits the movement of migrating ions produced by the active electrode and, as a result, a conductive filament is formed most advantageously in the form of a pyramid or a truncated cone.
    - Pt proves to be best choice amongst the given array of materials. It acts as an excellent stopping electrode and make devices a potential candidate for memory applications.
    - Ti displays a small degree of the inert property. Its stopping power for migrating ions is low and as a result of which these active electrode metal ions get diffused into the Ti electrode. The geometry of the filament is weakened at the base and takes on a cylindrical shape rather than cone shape and therefore cannot be easily ruptured, since it lacks a "weak link" at which a gap in the filament can be formed.
    - Ta apparently lies somewhere between Pt and Ti, in terms of exhibiting inert properties. It has the ability of stopping migrating ions but not as effective as Pt. This leads to the formation of a truncated cone-like filament structure having a broad top. Similarly to the cylinder shape, such a structure of a filament is also difficult to rupture.

Chapter 6: Search for Appropriate Material to Implement Resistive Switching Memory in the Back-end of Modern CMOS Process (SRC Project in collaboration with Intel)

6.1 Introduction

Aggressive scaling of the gate oxide thickness for higher transistor currents and hence higher switching speeds has aggravated reliability of interconnect dielectric and also created a time delay bottleneck on the side of interconnects. The primary factors for this are high interconnect capacitances and highly resistive metal lines. Figure 6.1 demonstrates the so-called latency or interconnect communication bottleneck. While in the past the limiting factor for signal propagation was the transistor, today it is the interconnect part. Another demonstration of the latency issue is shown in Table1 for three generations of leading edge transistors.

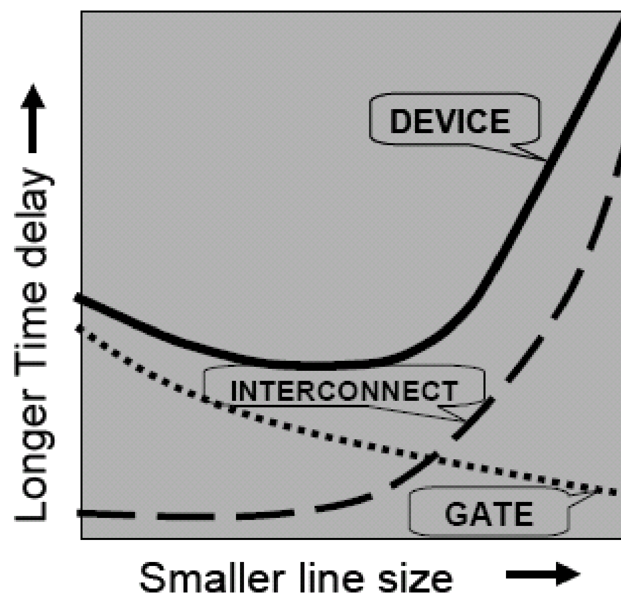


Figure 6.1: Increasing Time Delay

Table 6.1: Three generations of leading edge transistors

	L_G=1.0 mm	L_G=100 nm	L_G=35 nm
MOSFET τ (ps)	**20**	**5**	**2.5**
Interconnect Delay (ps)	**1**	**30**	**250**

To address this problem CMOS manufacturer have to use dielectrics with a dielectric constant as low as possible in order to lower the parasitic capacitance. Intel has identified many organo-silicates as an alternative for the SiO2 based dielectric materials. Time dependent Dielectric

Breakdown (TTDB) has been an intense topic of research over the past two decades. In order to evaluate intrinsic oxide reliability, time-to-breakdown (t_{TDDB}) measurement of capacitors are made under really harsh environments like higher stress voltage and/or higher temperature and the lifetime under normal operational condition is thus then extrapolated. Such a reliability assessment usually involves extrapolation of dielectric lifetime based on three discreet parameters: area, temperature and voltage scaling. Although percentile and area scaling based on Weibull distribution and percolation theory is widely accepted, the model developed in the process is still a subject of much controversy.

The most preliminary data collected from TDDB analysis state that logarithm of t_{TDDB} is inversely proportional to the electric field applied to the oxide. The thermochemical model based on the interaction of molecular dipoles with the electric field is commonly known as the E-model. By treating the dielectric as a collection of dipoles, the free activation energy for the breakdown reaction rate was expressed as series expansion of the oxide field E, from which t_{TDDB} was derived by ignoring the non-linear terms.

$$\log(t_{TDDB}) \propto -\left(\frac{E_a}{kT} - \beta E\right) \tag{6.1}$$

Here, E_a stands for activation energy. Activation energy is usually in the range of eV and is the amount of energy required by the dielectric to overcome their ionization potential and undergo a breakdown. β represents the acceleration factor, which is again dependent on the dipole moment of the dielectric. It is evident that the Arrhenius relation 6.1 exhibits a linear behavior as shown in Figure 6.2 [41]. In this particular case, the device is p^+ gate oxide grown on n-substrate with SiO_2 (t_{ox} = 12nm).

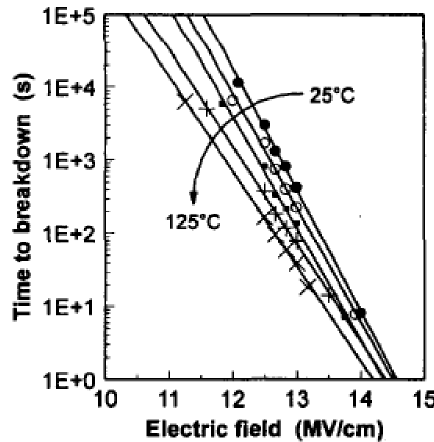


Figure. 6.2: Arrhenius plot for break time against electric field

Oxide reliability becomes the major concern for quality in microelectronics as the critical dimensions scale down. In particular, in an industrial context, the oxide reliability has to be checked in order to qualify the technology, i.e. to guarantee the insulator properties during the whole operating lifetime of the product. Classically, oxide lifetime is estimated for the nominal biasing conditions and for various temperatures, after compiling degradation results obtained at

accelerated stress conditions (higher electric field and/or higher temperature). However, this estimate implies the use of an extrapolation model as follows: i) extrapolation at low electric field with a TDDB (Time Dependent Dielectric Breakdown) model and ii) extrapolation through the Arrhenius law from higher temperatures (100°C-170 C) to room temperature. In both cases, the knowledge of the TDDB activation energy is necessary for a valid extrapolation.

Chapter 5 has influenced our understanding in terms of the behavior of Ta and Ti as anode and cathode in an interconnect circuit. In this chapter we attempt to study similar MIM systems with a low-k dielectric.

6.2 Statement of Work

In this project we are working with interconnect structures. In order to address the issues of time delay, Intel came up with the alternative low k materials to replace regular dielectric SiO2 with. Many such dielectric material, (typically organo-silicates) have been identified for this purpose. Figure 6.3 illustrates the current and the future changes proposed for interconnect structures.

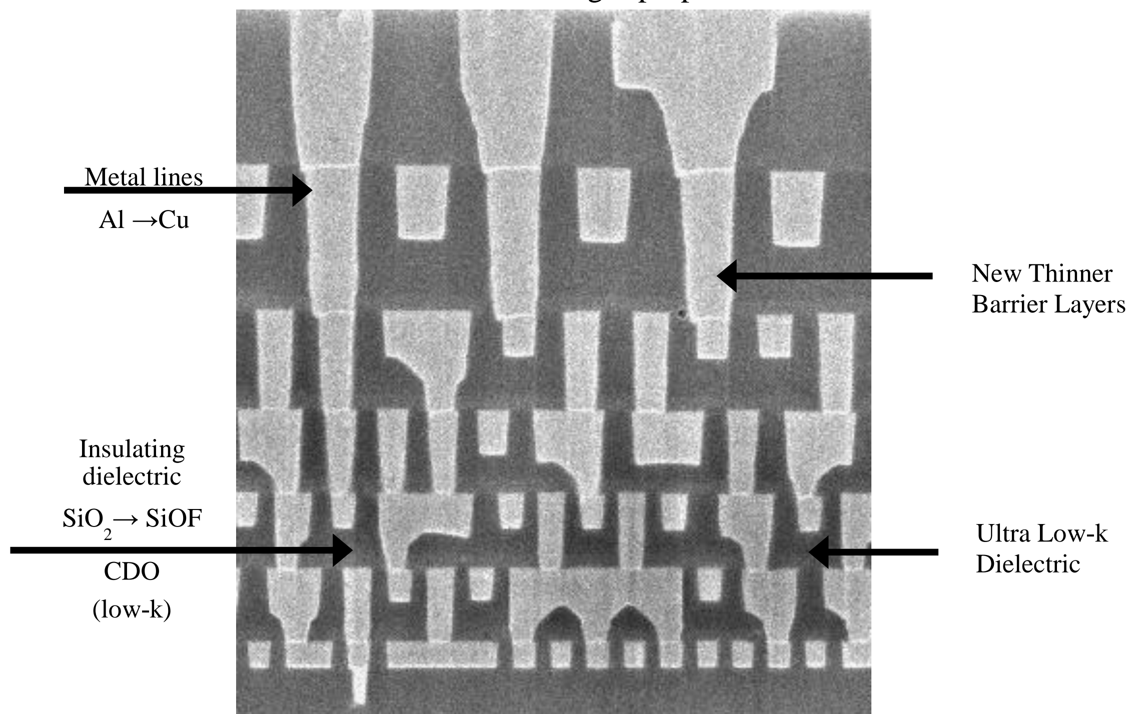


Figure 6.3: Interconnect structures with proposed changes

The aim of this project to analyze the electrical reliability of such interlayer dielectric material. One of the most common method to confirm electrical reliability is to perform a time dependent dielectric breakdown. Figure 6.4 gives us a schematic representation of the device structure which is typically metal-insulator-metal structure (MIM). Such a structure is stressed under harsh conditions like high electric fields, elevated temperatures and prolonged time periods, in order to seek for a condition wherein the dielectric undergoes a breakdown or, in other words, fails to provide adequate isolation of the metal electrodes from each other. From an application point of view, if the identified materials survive such harsh testing conditions, it would indicate immunity

to failure, and, hence, a high reliability of the device. Therefore, we would like to have information to what limits dielectric can be stressed.

A potential bias is applied to the device by connecting a voltage bias across the top and the bottom metal electrode. The primary deliverables of this project are listed as follows.

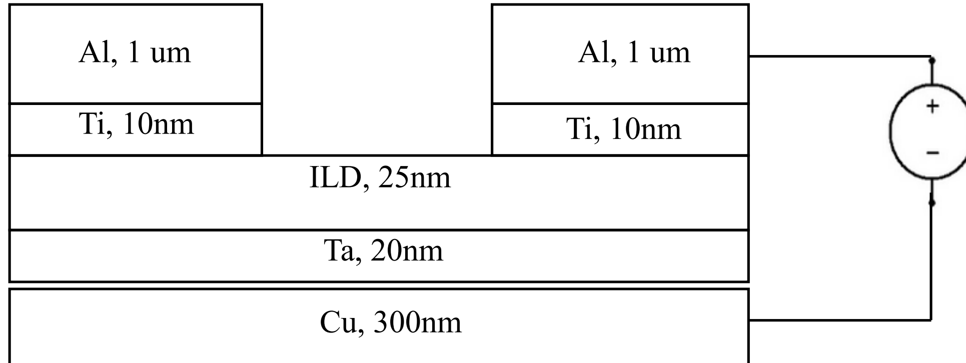


Figure 6.4: Schematic layer structure of the cross section of low-k interconnect structure

- Fabrication of low-k/Cu test structures for TDDB and RS testing (Materials to be supplied by Intel, fabrication at Intel and/or VTech).
- Development and publication of a methodology/protocol for performing combined TDDB and RS testing of low-k/Cu interconnect structures.
- Application of the above methodology to the fabricated low-k/Cu interconnect structures with a final report on the results and suggested future improvements.

6.2.1 Device Layout

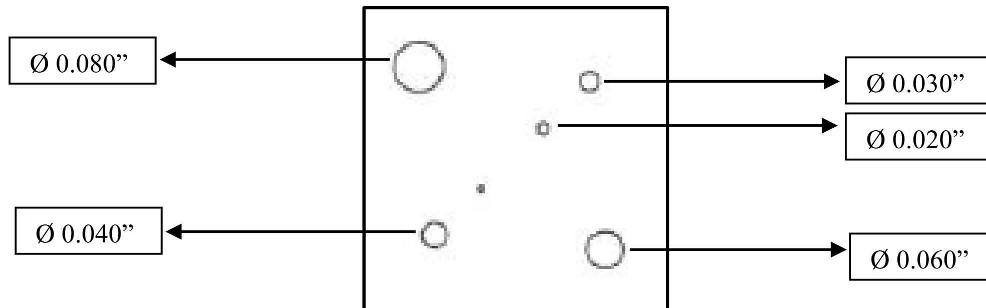


Figure 6.5: Feature size of the device available on the samples (measurement not to scale)

Different feature size have been provided and this gives us the opportunity to play around with the current density while performing a voltage sweep test. This layout is repeated all over the sample and remains constant for all type of samples. Figure 6.5 gives us the test sample layout.

6.2.2 Objectives/Technical Specifications

The scope of the project has been summarized as follows:

- Fabrication of low-k/Cu test structures for TDDB and RS testing (Materials to supplied by Intel, fabrication at Intel and/or Virginia Tech)

- Development of test methodology for performing combined TDDB and RS measurements of approved fabricated low-/Cu interconnect structures.
- Application of the above test methodologies to the above fabricated low-k/Cu interconnect structures.
- Summary report of the results from the combined TDDB/RS testing with conclusions and suggestions for further improvements.
- Definitive conclusion on whether failure is due to Cu filament formation or oxygen vacancy formation.
- Evaluation of low-k dielectrics as a potential dielectric in RS devices.

6.2.3 Samples Received from Intel

Table 6.2 gives a list of the interlayer dielectric that have been provided by Intel for electrical characterization. We have chosen 7 of the said 15 samples in order to carry on with the analysis.

The samples marked in blue are the ones which have been tested so far in this project. All the samples have a similar dielectric thickness of 25nm and this has been intentionally done in order to simplify the measurement techniques. k(SiO_2) is known to be 3.9. We notice that in this case k is larger for most ILD layers provided in the table compared with SiO_2

Table 6.2: Intel/VT Low-k TDDB Samples

Sample #'s	Bottom Electrode	Dielectric	Dielectric Constant-k	Dielectric Density (g/cm3)	Dielectric Thk (nm)	Top Electrode
693	Ta/Cu	SiN:H	6.5	2.5	100	Al/Ti
680	Ta/Cu	SiO2	4.3	2.25	100	Al/Ti
682	Ta/Cu	SiOC:H	3.2	1.5	100	Al/Ti
687	Ta/Cu	SiC:H	5	1.8	100	Al/Ti
679	Ta/Cu	SiCN:H	5.85	2.25	100	Al/Ti
694	Ta/Cu	SiO2	4.3	2.25	25	Al/Ti
684	Ta/Cu	SiOC:H	3.2	1.5	25	Al/Ti
697	Ta/Cu	SiCOH	4.8	2	25	Al/Ti
695	Ta/Cu	SiC:H	7.2	2.5	25	Al/Ti
686	Ta/Cu	SiC:H	5	1.8	25	Al/Ti
685	Ta/Cu	SiCN:H	5.85	2.25	25	Al/Ti
688	Ta/Cu	SiNC:H	4.8	1.8	25	Al/Ti
676	Ta/Cu	SiN:H	6.5	2.5	25	Al/Ti
692	Ta/Cu	SiON:H	6.3	2.5	25	Al/Ti

6.3 Development of Test Methodology

Our test methodology consists of several steps that are described in more detail below:

Step 1: Voltage Sweep Test

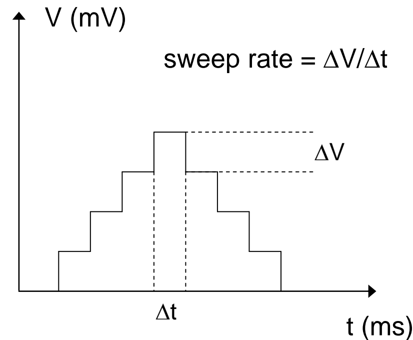


Figure 6.6: Schematic illustration of voltage sweeping mode memory devices in DC characterization

The devices are stressed with a linear ramp voltage having a (hardwired) interval time of 50ms per step size. In other words if a step size of 0.01V is chosen, it means that the sweep rate is 0.01V/50ms=0.2V/s. The schematic diagram of a dual sweep from 0V to a maximum voltage and back to 0V is given in Figure 6.6. The voltage is ramped up from 0V at a specified step size and until a specified stop voltage is reached. The voltage is then stepped back to zero volts. The process and electrical characterization of these devices have been performed using Keithley 4200 SCS.

From the device layout structure depicted in Figure 6.3, we know that it has a MIM cross-section. Consequently, on initial application of voltage bias, the device does not conduct electricity and hence the current measured is merely in the range of nA and fA which can practically be stated to be zero as observed breakdown current are above μA. Eventually due to continuous and gradual voltage ramp, when sufficiently high stress has been exerted on the device, more or less abrupt reduction of the resistance of the dielectric takes place, as seen in Figure6. At some critical voltage which typically exceeds the breakdown voltage, the dielectric is rendered electrically conductive. However, in order to prevent the device from being completely damaged, we limit the maximum current flowing through the device to I_{CC} chosen in most cases to be 0.1 mA. Despite this current limitation some samples become permanently damaged upon reaching I_{CC}.

In Figure 6.7 an I-V characteristic for sample no 684 is shown. The samples are tested multiple times at various temperature conditions viz. room temperature, 50, 100 and 150C. There are essentially two outcomes after performing the linear voltage stress:

- Permanent dielectric breakdown – This means that the dielectric has been permanently damaged and cannot be reset back to high resistance state, and hence cannot be used for further experimentation.
- Temporary dielectric breakdown - This means that the dielectric recovers after the removal of power supply. On retesting, such samples undergo a new breakdown.

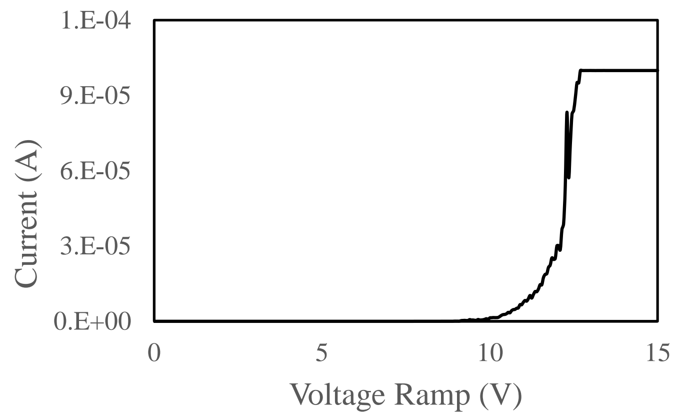


Figure 6.7: Current Vs. Voltage plot for dielectric breakdown.

Since the ultimate aim is to understand the underlying physics of dielectric breakdown, samples which can be re-tested are preferred.

Step 2: Current Density vs. Electric Field

Since the device area-size is varying for different sample (See Figure 6.4), current density is a better indicator to investigate the dielectric breakdown in order to establish a strong relation between current density and electrical field. Figure 6.7 serves as a model graph for plotting current density against electric field. As expected, the current density increases and attains the compliance current in a lesser period of time at higher temperatures as opposed to room temperature. The dashed line in Figure 6.8 represents the locus of current densities at a constant electric field and at different temperatures allowing extraction of the activation energy according to eq. (6.1) given at the beginning of this chapter.

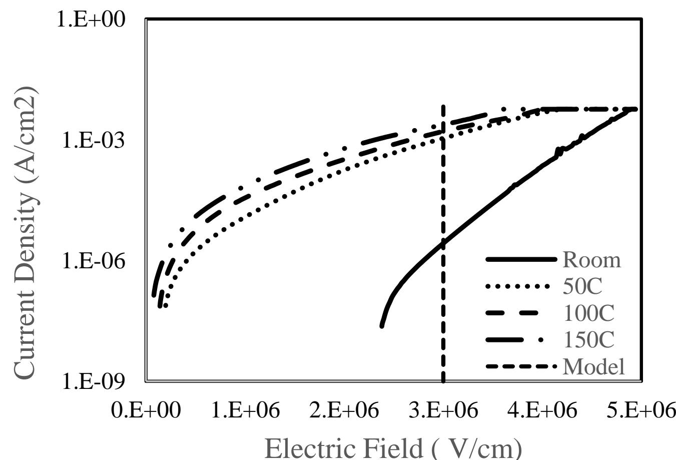


Figure 6.8: Variation of Current Density with temperature

Step 3: Arrhenius Relation for the defect generation rate

Let the generation rate of the vacancies during dielectric breakdown be given by a factor G. The unit of G should be s^{-1}. By definition G can be given by:

$$G = \frac{\text{\# of vacancies (defects)}}{\text{time}}$$

By now we know that, the generation rate complies with Arrhenius Relation. However there can be two cases possible in this situation.

Case 1: When $E_a \gg \beta E$

The following equation illustrates the generation rate of vacancies at extremely low electric fields (in the order of 100 V/cm or smaller).

$$G = G_O e^{-\left(\frac{E_a}{kT}\right)} \quad (6.2)$$

Where, G_o is a proportionality constant and $E_a$is in eV.

Case 2: When $E_a > \beta E$

Such a situation arises when the values of βE though less but comparable, in the terms of magnitude, to E_a. This can happen only at very high electric fields (usually in the order of a few MV/cm). It is usually in this domain that the dielectric undergoes a breakdown and the generation rate G, is given by,

$$G = G_O e^{-\left(\frac{E_a - \beta E}{kT}\right)} \quad (6.3)$$

Where, $\beta = p\left(\frac{2+\varepsilon}{3}\right)$, p being the dipole moment and ε being the dielectric constant.

$E_a$is in eV, and E is the breakdown field in V/cm.

Thus at a critical breakdown field E_{crit}, when $\beta E = E_a$, the generation rate will be given by G_O. Now in this plot since we are plotting current density against inverse of thermal voltage we develop the relation as:

$$J \propto G_O e^{-\left(\frac{E_a - \beta E}{kT}\right)}$$

Or conversely,
$$J = J_O e^{-\left(\frac{E_a - \beta E}{kT}\right)} \quad (6.4)$$

Where, J_O is a proportionality constant given by $J_O = cG_O$.. In this chapter we will be using Equation 6.4 for most of our calculations and plots.

However what we leave out over here is the consideration of the Poole-Frenkel Effect. The Poole–Frenkel effect describes how, in a large electric field, the electron doesn't need as much thermal energy to get into the conduction band (because part of this energy comes from being pulled by the electric field), so it does not need as large a thermal fluctuation and will be able to move more frequently.

The standard quantitative expression for the Poole–Frenkel effect is:

$$J \propto E \exp\left(\frac{-q\left(\phi_B - \sqrt{qE/(\pi\epsilon)}\,\right)}{k_B T}\right) \tag{6.5}$$

,where $\emptyset_B$ is the voltage barrier in zero applied field for the electron to move across the dielectric.

Step 4: Calculation of Activation Energy

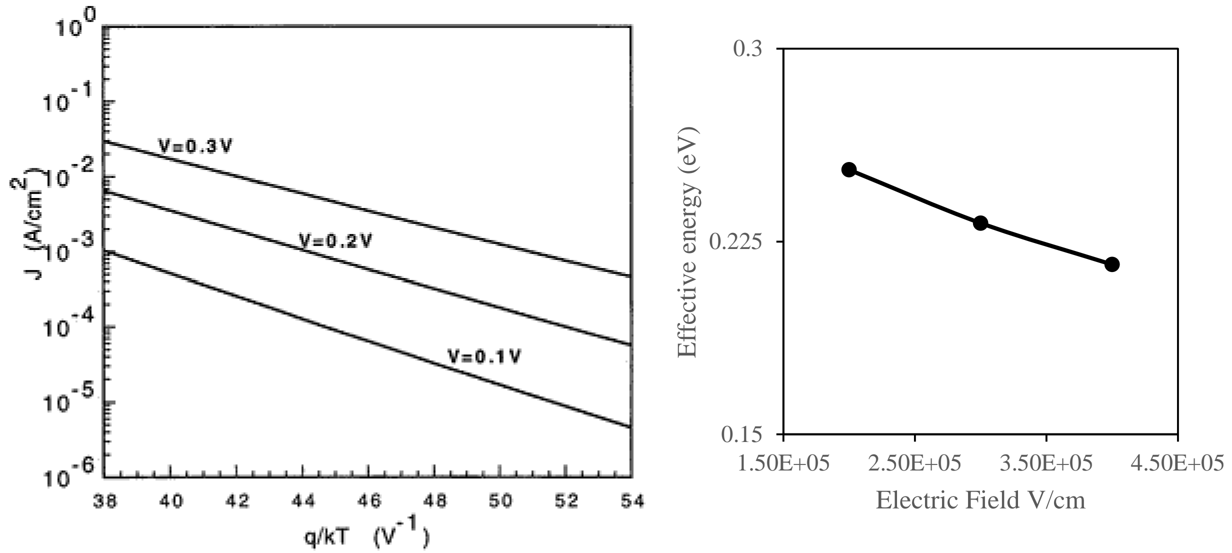


Figure 6.9: (a) Current density vs. reciprocal temperature (b) Effective Activation Energy vs. Electric Field.

Figure. 6.9 (a) shows the temperature dependence of the current density at some particular bias voltage. A linear relationship between the current density taken on a logarithmic scale and the reciprocal thermal voltage (kT) has been obtained [42]. This plot is done by considering a constant applied electric field. Thus different values of electric field would result in different Arrhenius Plots having possibly different slopes. However, it is worth noticing that the respective slope of the pre-exponential factor to Arrhenius plot (Effective Activation energy, E_a-βE) is an important finding since it denotes that the generation rate of the vacancies complies with the Arrhenius plot. $E_{a,}$ denotes the original activation energy, β is the dipole moment factor and E is the respective electric field. The relation has been already explained in relation 6.4.

Further plots between effective activation energy and electric field can be plotted to further find out the values of the E_a and β. This has been indicated in Figure 6.8(b). We consider the equation derived from relation 6.4 and is given by:

$$E_{eff} = E_a - \beta E \tag{6.6}$$

The slope yield β and the intercept yields E_a.

Step 5: Time Dependent Dielectric Breakdown

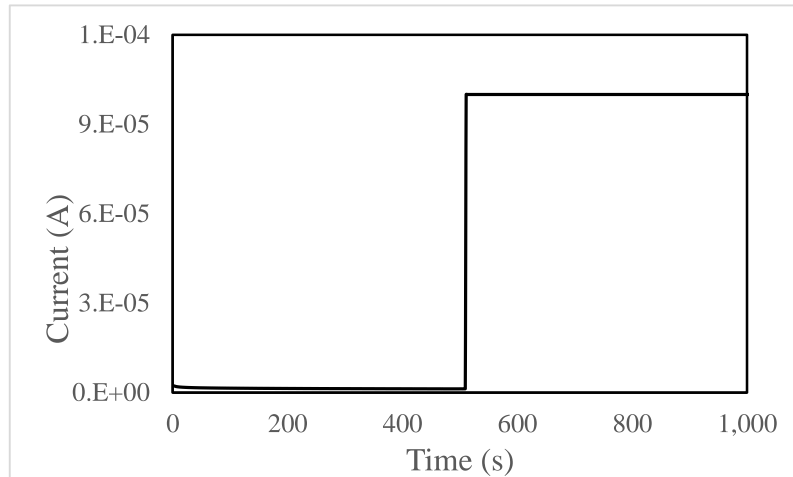


Figure 6.10: TDDB Analysis under constant voltage

Figure 6.10 gives us a general representation of the variation of dielectric current when a high constant voltage is applied and the current is measured as a function of time. We correlate the time t_{TDDB} when the current increases abruptly (in Figure6.10 this time is ~520 s) with the defect generation rate in the following way:

$$1/t_{TDDB} \propto G$$

6.4 Results and Discussions

In this section we report the results of the test methodology described above on several different samples that have been investigated.

Sample no 695

Sample #'s	Bottom Electrode	Dielectric	Dielectric Constant-k	Dielectric Density (g/cm3)	Dielectric Thk (nm)	Top Electrode
695	Ta/Cu	SiC:H	7.2	2.5	25	Al/Ti

Figure 6.11 gives the schematic representation of the experimental setup. The five differently sized devices were individually tested for repeatability as explained in the Section 6.3.

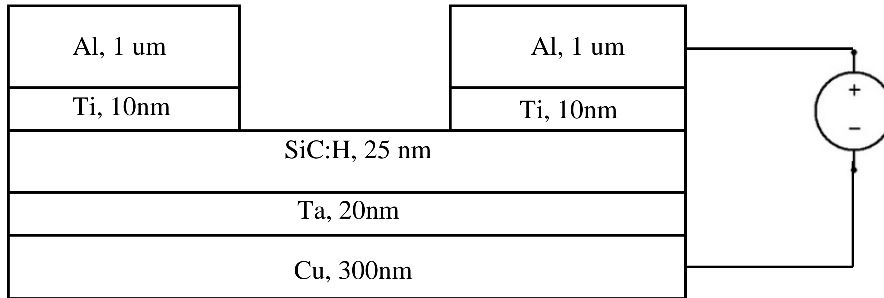


Figure 6.11: Experimental Set-up for Sample no 695

Figure 6.12 shows the **soft volatile** SET range for sample no 695. We have limited the compliance current to 0.1 mA in order to prevent the sample being permanently damaged.

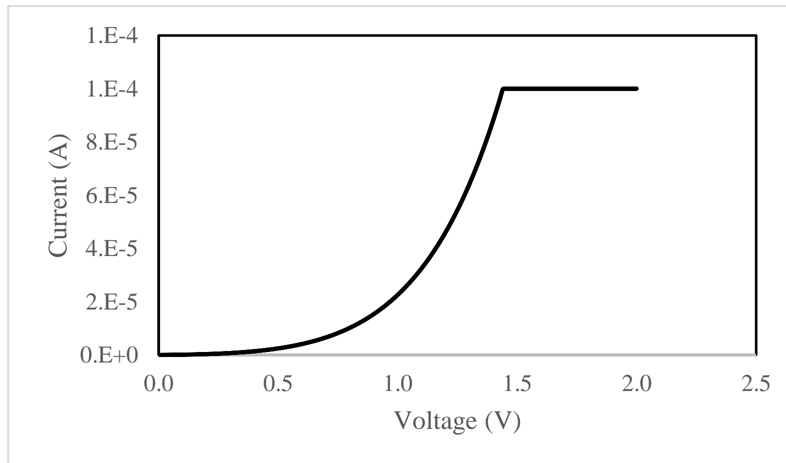
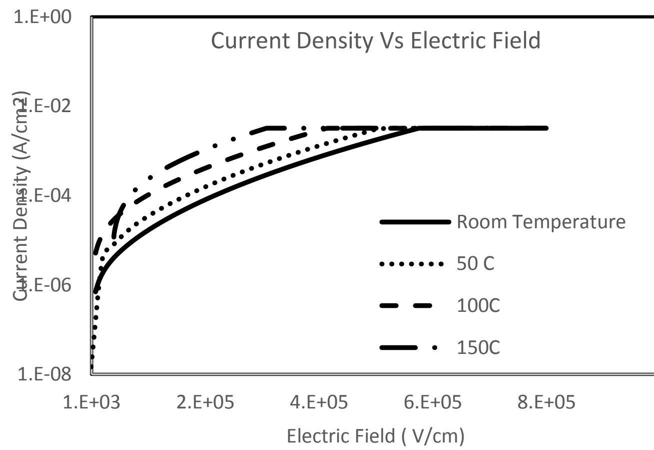


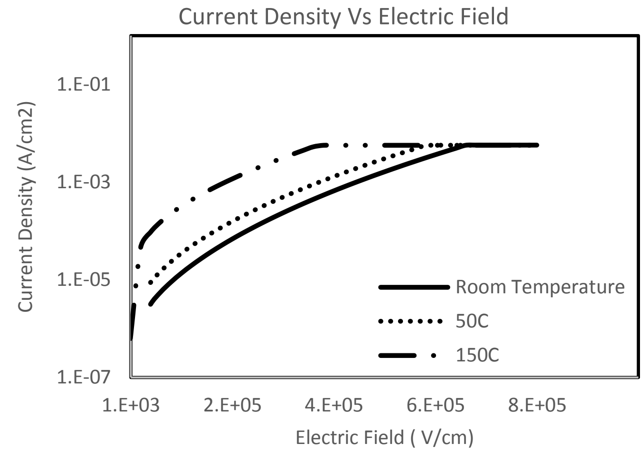
Figure 6.12: I-V Characteristics

The result of the first test on sample 695 is shown in Figure 6.12. It is seen that the current increase is very gradual without any abrupt change. Such a gradual current increase is called soft breakdown of the dielectric. Soft volatile set means also that the conductive path disappears when the device is no longer powered. Or in other words, the dielectric recovers when the electric field is removed. This affords us with the opportunity to test the device again and again. This is particularly convenient because it eliminates the chances of having variation of the quality of the dielectric across the sample. Figure 6.11 illustrates the I-V characteristics. The behavior in Figure 6.12 indicates that the device is probably not resistive switching capabilities for memory applications.

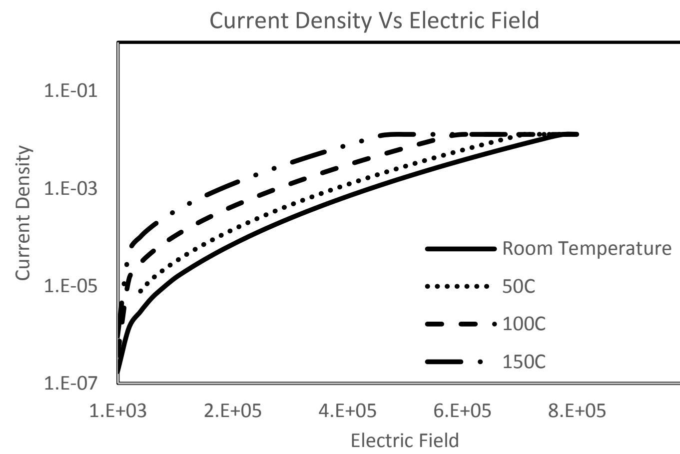
Current Density *vs* Electric Field



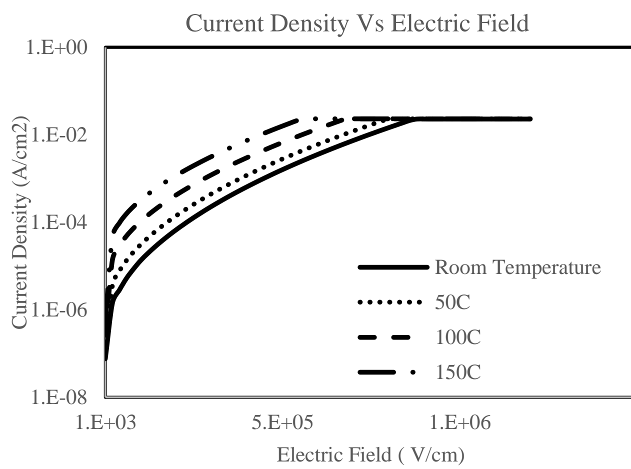
0.08 inch



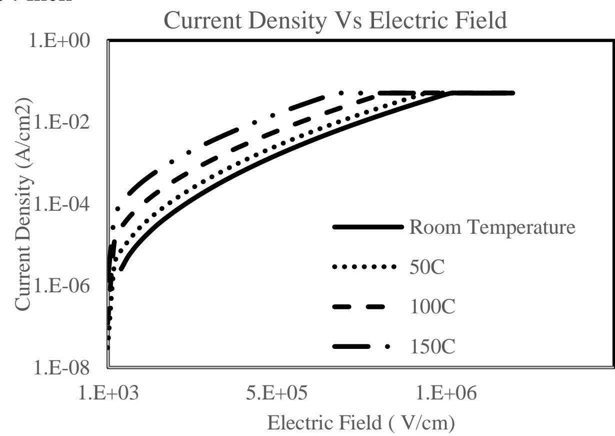
0.06 inch



0.04 inch



0.03 inch



0.02 inch

Figure 6.13: Current Density Vs Electric Field for different device size

Figure 6.13 shows that current density increases with increasing temperature. This means that higher temperature provides the mobile carriers with higher thermal energy and this leads to a faster dielectric breakdown.

Analysis of Thermal Behavior

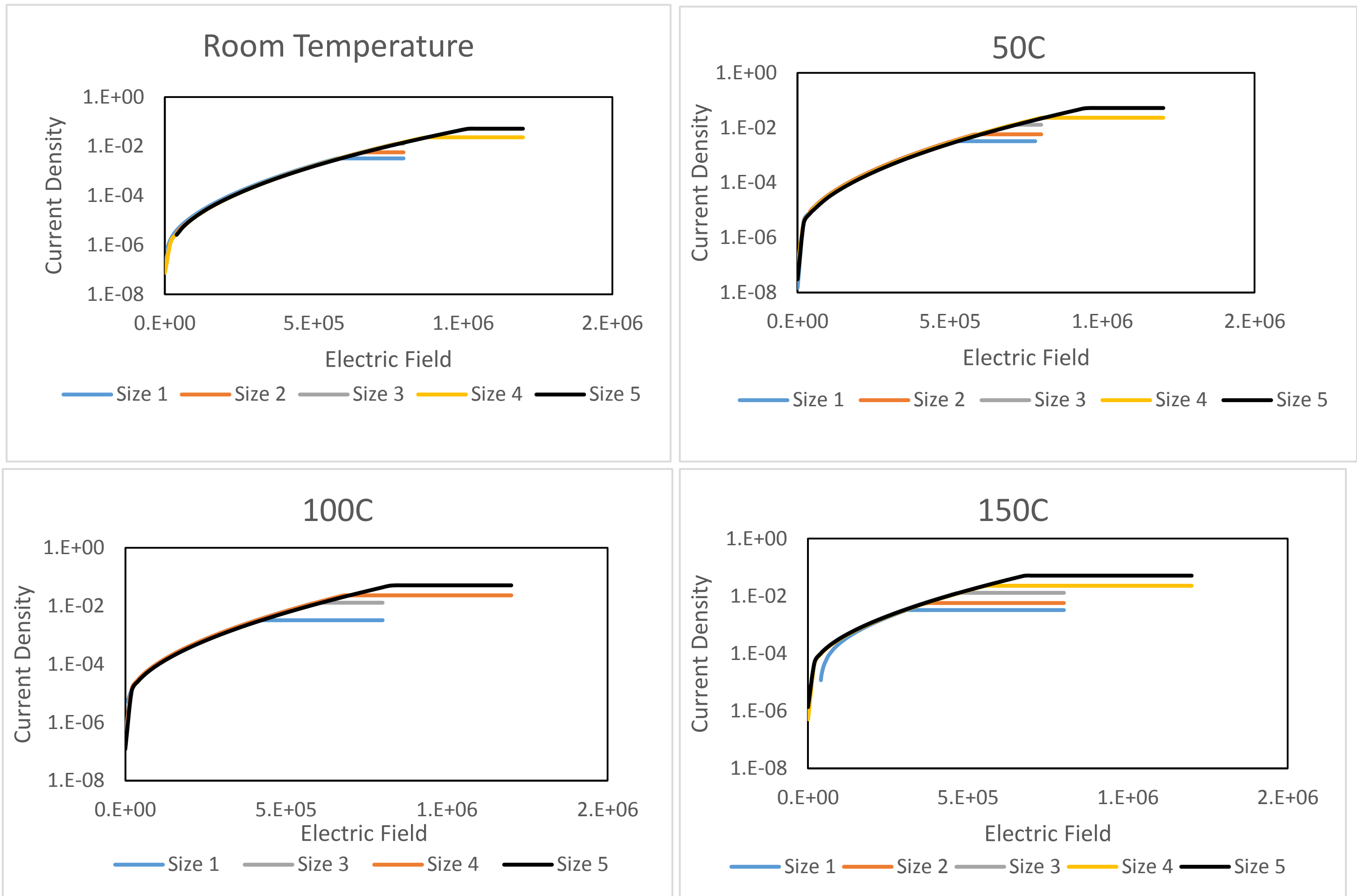


Figure 6.14: Current Density Vs Electric Field for various temperatures

Figure 6.14 shows that all devices trace the same line exept for different current limitations.. Since we have five different device sizes for the sample, current density could be given as follows:

$$J = I_1 A_1 = I_2 A_2 = I_3 A_3 = I_4 A_4 = I_5 A_5$$

Each of the graph shows that the current density before it reaches the compliance current is constant for all sample sizes.

Arrhenius Plot and Extraction of Activation Energy

We have chosen the 0.02 inch diameter device size for the calculation of activation energy. The plot for current density at a particular electric field against inverse of thermal voltage is given in Figure 6.15.

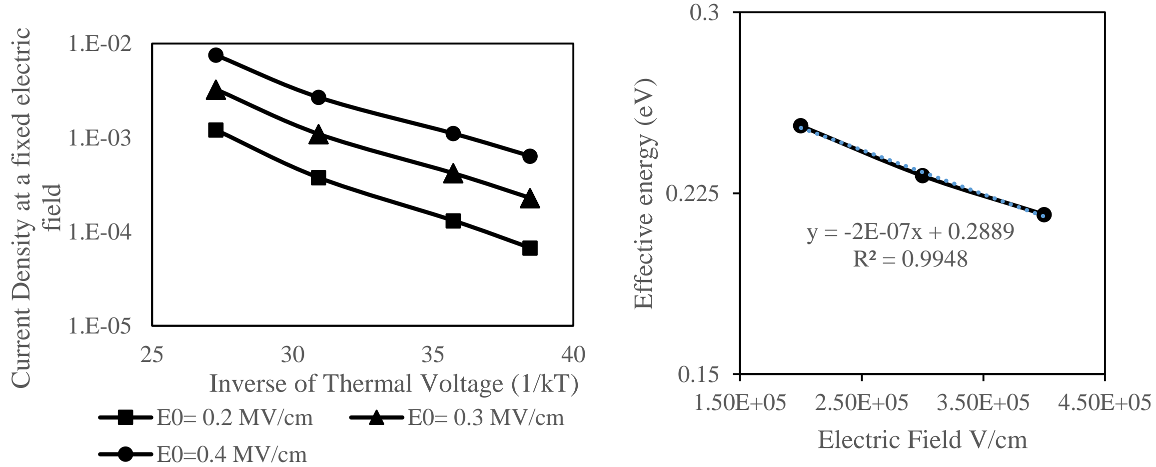


Figure 6.15: Current density against inverse thermal voltage

The three curves are more or less parallel to each other and slope in the graph remains constant for the three of them. The plot indicates that the defect generation mechanism is the dominant mechanism for the leakage current for this sample. From Figure 6.15 three effective energies were calculated from the three plot. The final parameters were calculated as:

$$\mathrm{E_a} = 0.2889\ \mathrm{eV} \qquad \beta = 20\ e - \mathrm{Å} \qquad E_{bd} = 1.44\ MV/cm$$

The low activation energy and moderately high dipole moment factor as opposed to values found for conventional high-k metal oxides cited in the literature, result in a relatively low breakdpwn electric field thus yielding a low SET Voltage (< 2V). The pre-exponential constant J_O has been calculated as 1.088 calculated for 0.2 MV/cm.

Sample No 688

Sample #'s	Bottom Electrode	Dielectric	Dielectric Constant-k	Dielectric Density (g/cm3)	Dielectric Thk (nm)	Top Electrode
688	Ta/Cu	SiNC:H	4.8	1.8	25	Al/Ti

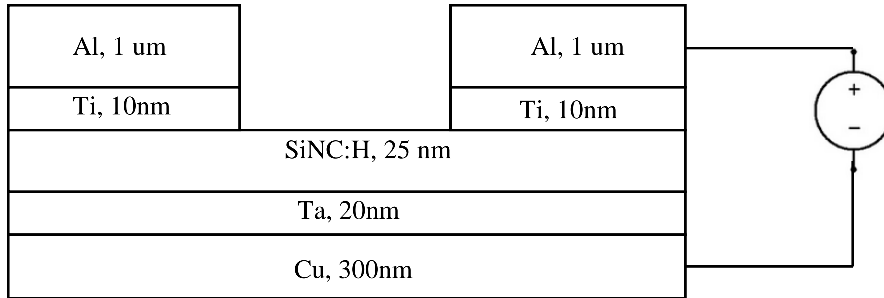


Figure 6.16: Experimental Set-up for Sample no 688

Figure 6.16 gives the schematic representation of the experimental setup. The five differently sized devices were individually tested for repeatability as explained in the test methodology and the following results were obtained.

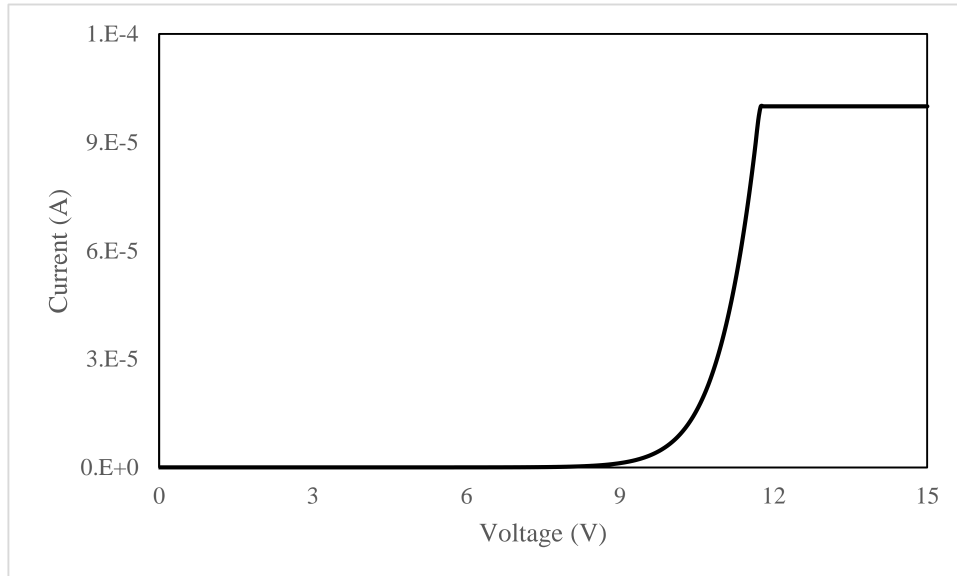


Figure 6.17: I-V Characteristic at room temperature (300K)

Figure 6.17 shows a **soft volatile** SET behavior for sample no 688. We have limited the current range in the sample to 0.1 mA in order to try to avoid a permanent damage to the device. The relative onset of the transition to high conductivity state can be observed between 10-12 V. Similar to the previous samples, this device does not exhibit resistive switching.

Current Density vs Electric Field

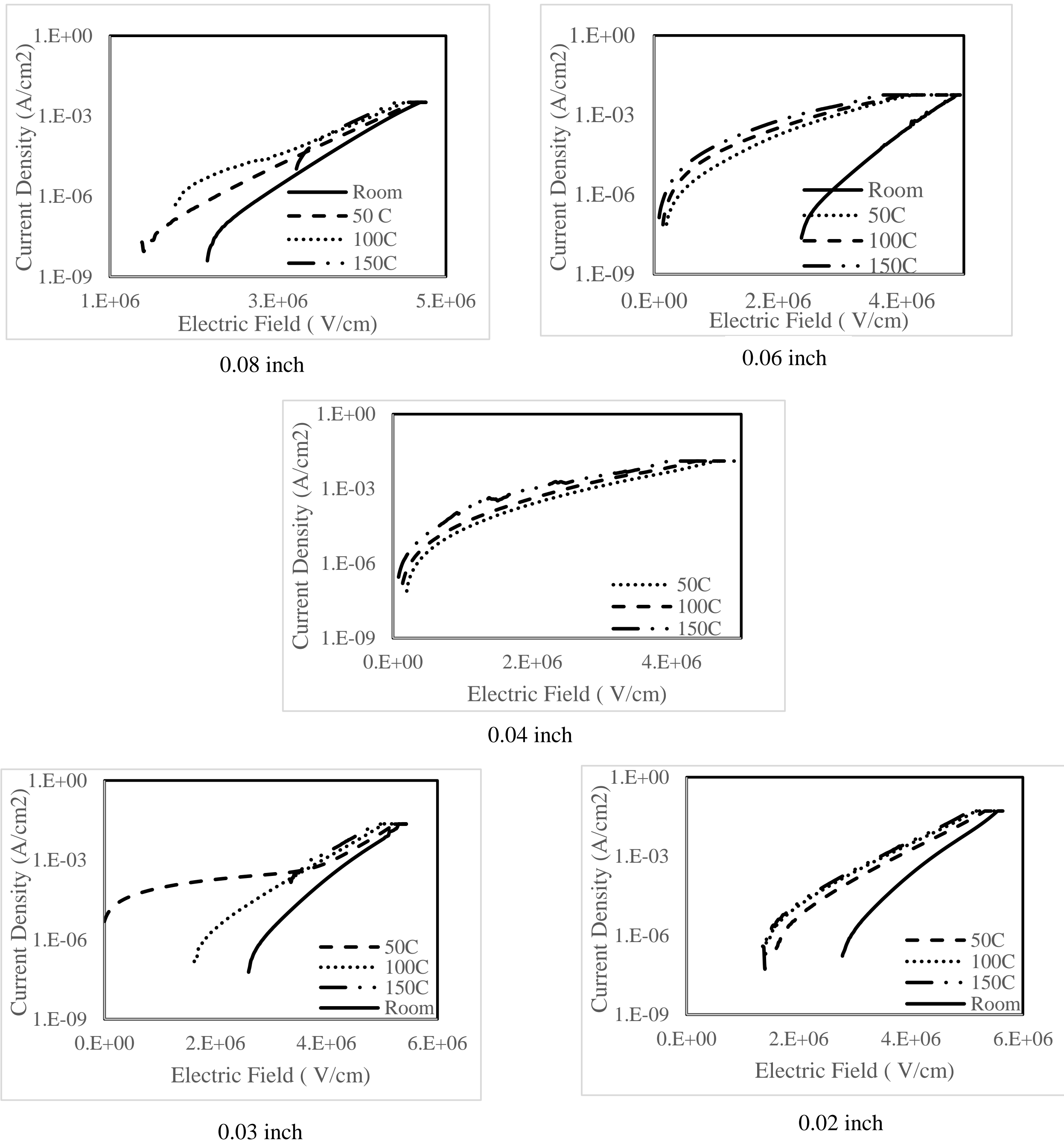


Figure 6.18: Current Density Vs Electric Field for different device size

Unlike in Figure 6.13, in Figure 6.18 we see that the changes in the current density with temperature are not very gradual. We have some occasional disturbances and surprising crossovers. However, the general picture still remains similar and indicating that similar mechanisms responsible for the breakdown are at work.

Analysis of the Thermal Behavior

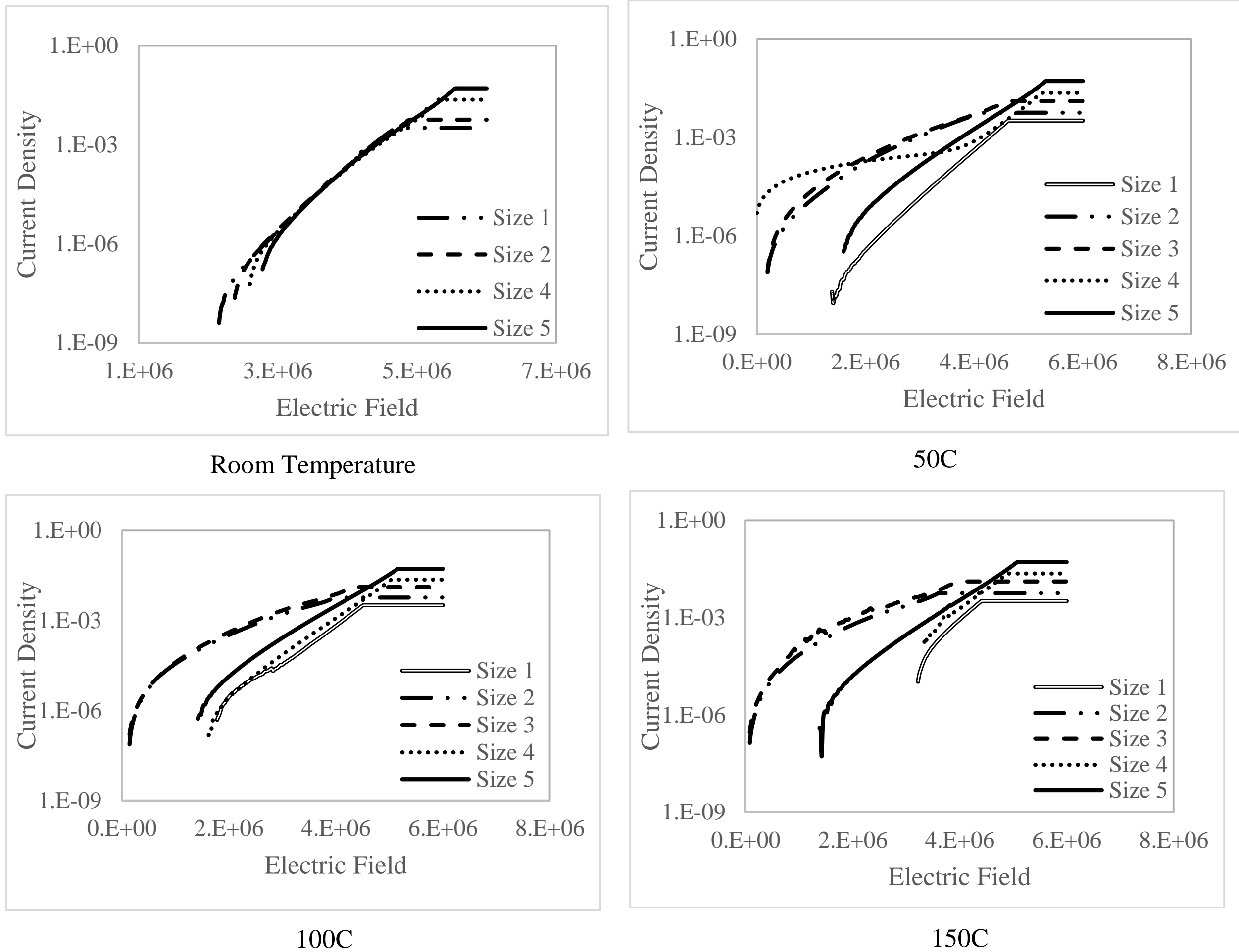


Figure 6.19: Current Density vs Electric Field for various temperatures

Figure 6.19 shows a little bit surprising behavior. The current density for a particular device at a particular temperature, hovers in the same range. Occasionally we find some strange crossovers. Especially for size 3 and 4 which are 0.04” and 0.03” diameter respectively.

Arrhenius Plot and Extraction of Activation Energy

Since the plots look pretty promising, we chose the 0.02 inch diameter device size for the calculation of activation energy. The plot for current density at a particular electric field against inverse of thermal voltage is given in Figure 6.20.

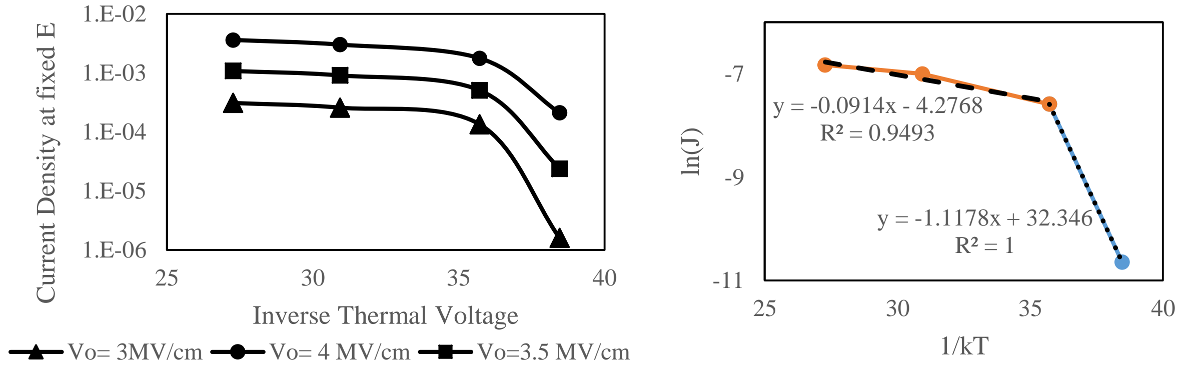


Figure 6.20: (a) Current density against inverse thermal voltage (b) Calculation of activation energy

Figure 6.20 shows rather a very complicated behavior when compared with the corresponding Figure for sample 695 shown in Figure 6.15. Figure 6.20(a) shows current density for three electrical fields as a function of inverse temperature. However, unlike Figure 6.15, the slope changes significantly. One can argue that two distinct slopes can be distinguished with a gradual transition. The existence of two slopes could argue existence of a very different mechanism involved in the generation of defects. The concepts related to Schottky emission or Poole-Frenkel emission is probably not applicable over here. Thus the extraction of activation energy and dipole moment factor remains unresolved in this case.

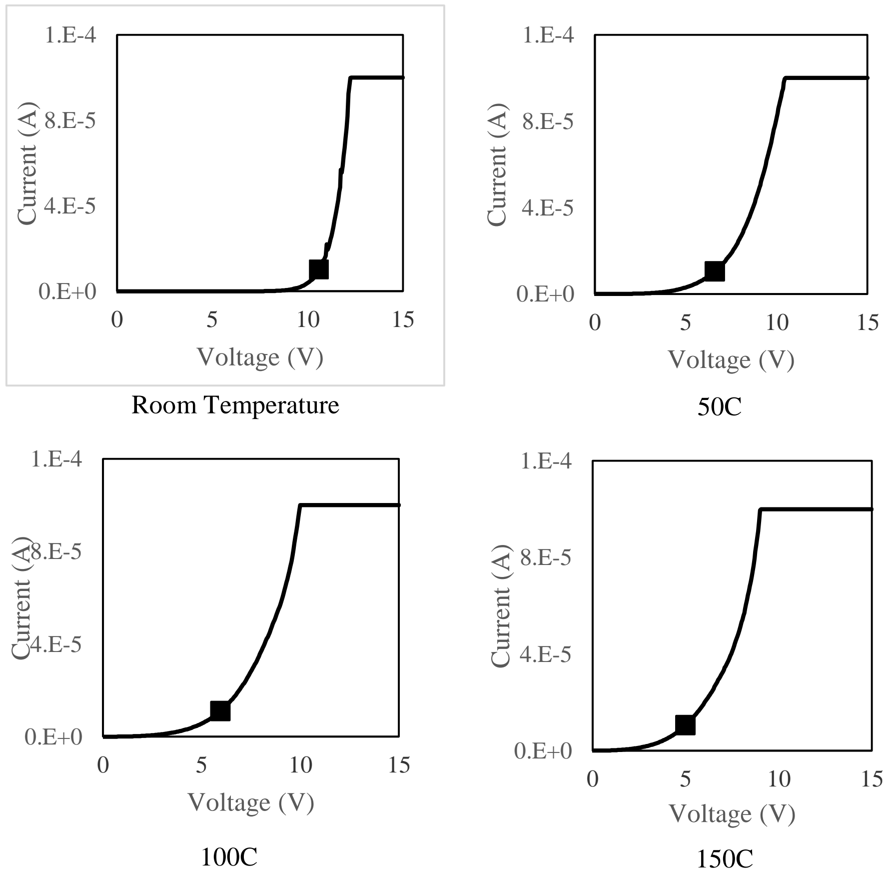


Figure 6.21: Variation of onset current with temperature for 0.06" device

In Figure 6.21 the same I-V characteristic is shown for Sample no 688 for different temperatures. The black point traces the current value of 10µA as we approach 150C. One can see that the onset of high currents can be observed at 5V as opposed to 10V observed at room temperature.

Time dependent dielectric breakdown

In Figure 6.22 the inverse of the breakdown time is plotted as a function of electric field for two temperatures: 100 and 170 C. In both case we find a linear dependence

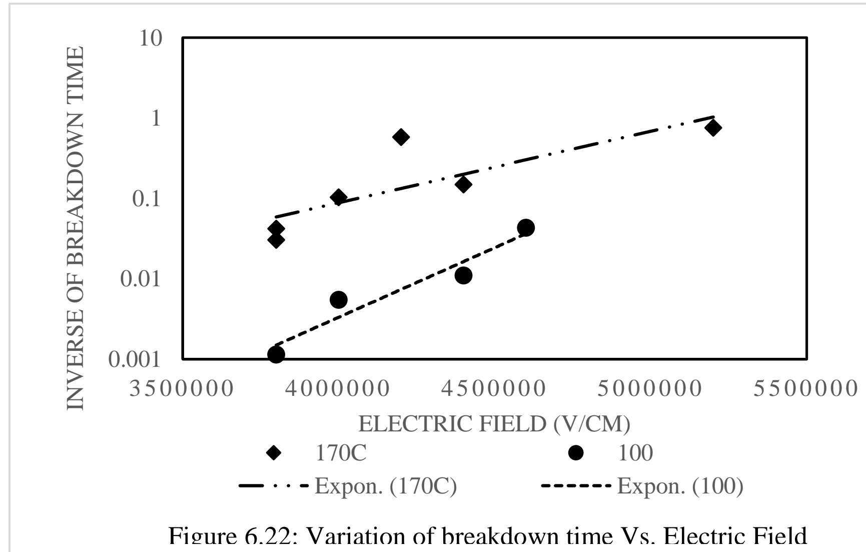


Figure 6.22: Variation of breakdown time Vs. Electric Field

We believe that Figure 6.22 is an important finding because it clearly illustrates that carrier generation does not comply with Poole-Frenkel Effect and that:

$$\ln\left(\frac{1}{t_{TDDB}}\right) \propto E$$

Two slopes were calculated from the plot, which is the factor β/kT explained in eq 5. The generation rate for the vacancies can thus be established. The slope values we calculated was approximately: $m_1 = 1.95 \times 10^{-6}$ e − cm and $m_2 = 3.83 \times 10^{-6}$e − Å .

As explained earlier, critical breakdown filed is given by:

$$E_{crit} = \frac{E_a}{\beta}$$

Now for the two temperature values we have calculate two values of β have as follows:

β_{170} = 7.67 eÅ and β_{100} = 12.93 eÅ

The two β values clearly reinstate our findings in the Arrhenius Plot. We can also understand that that dielectric breakdown in this case is an interplay of different forces. However this observation brings forth the fact that tested devices are expected to be robust at or around room temperatures, owing to the high activation energy. At higher temperature (>100C), the dielectric is likely to show a rapid degradation, that is, undergo a breakdown.

Sample No 684

Sample #'s	Bottom Electrode	Dielectric	Dielectric Constant-k	Dielectric Density (g/cm3)	Dielectric Thk (nm)	Top Electrode
684	Ta/Cu	SiOC:H	3.2	1.5	25	Al/Ti

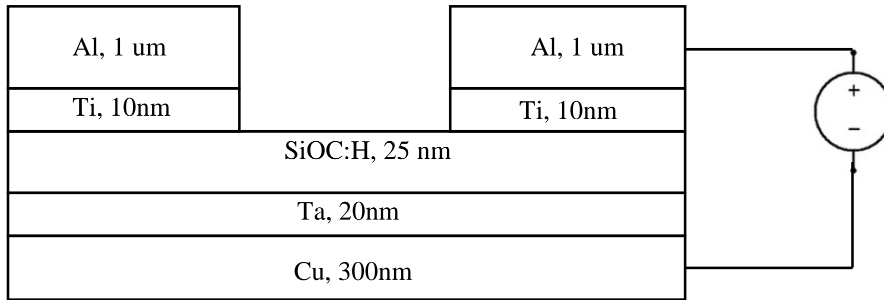


Figure 6.23: Experimental Set-up for Sample no 684

Figure 6.23 gives the schematic representation of the experimental setup. The five differently sized devices were individually tested for repeatability as explained in the test methodology and the following results were obtained.

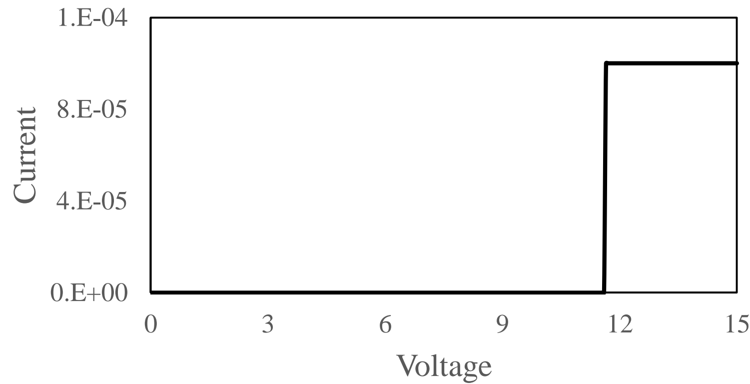


Figure 6.24: I-V Characteristics

I-V characteristics shown in Figure 6.24 is rather different compared with Figure 6.17 of the sample 688. The SET characteristics shows a sharp transition to low resistance state at about 11.3V in contrast to the soft current build-up of the previous sample 688. Also, the conductive bridge formed in this case is a **permanent** one which means the dielectric is permanently damaged. Hence, for every new test s fresh sample was needed to be characterized. This essentially means that even though the device does exhibit a stable resistive switching from HRS to LRS, the change is a permanent one and cannot be switched back as in the case of a Cu/TaO_X/Pt device. The device is, therefore unsuitable for memory application.

Current Density Vs Electric Field

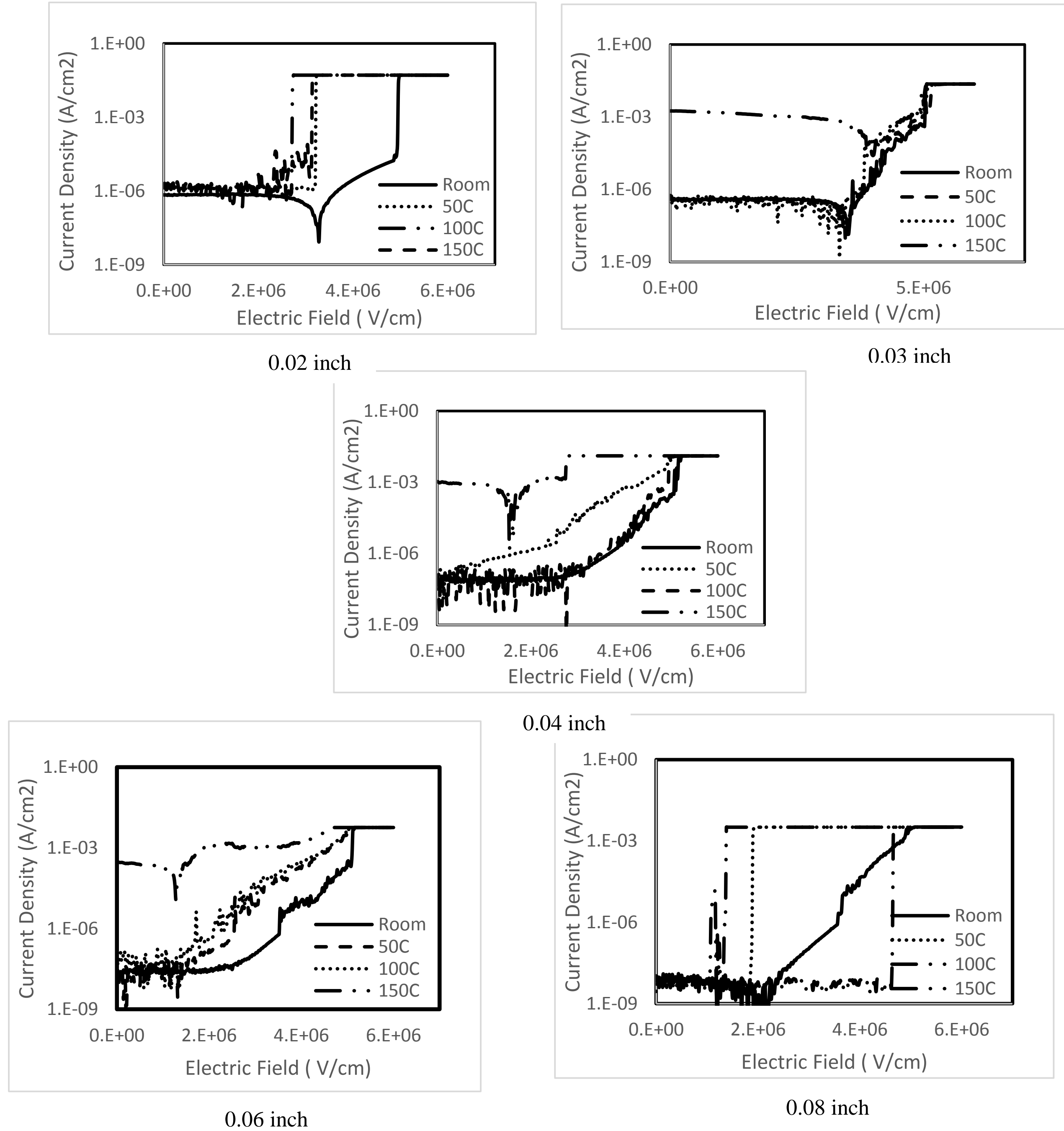


Figure 6.25: Erratic current density variation

We can well observe the erratic nature of the current density in Figure 6.25. There is an absence of a clear trend of current density increasing with temperature. Characterizing a fresh sample for every observation is a major roadblock for attaining a robust conclusion because of the following reasons:

- The dielectric is likely to have point defects and the distribution of these defects across the sample may be very stochastic. Thus, in principle, different cells may be not completely equivalent.
- Since we are yet to conclude on the internal structure of the conductive bridge, it is difficult if tests would have any effect on the subsequent test done the same device size at a different temperature.

All the above factors reduce the repeatability and reproducibility of the experiments greatly. The fact is visible in the erratic results given above (Figure 6.25). In Figure 6.26 the current is plotted as a function of electrical field for three temperatures: i) room temperature, ii) 50 C iii) 100C , and iv) 150C for a sample of 0.06 inch diameter sized device.

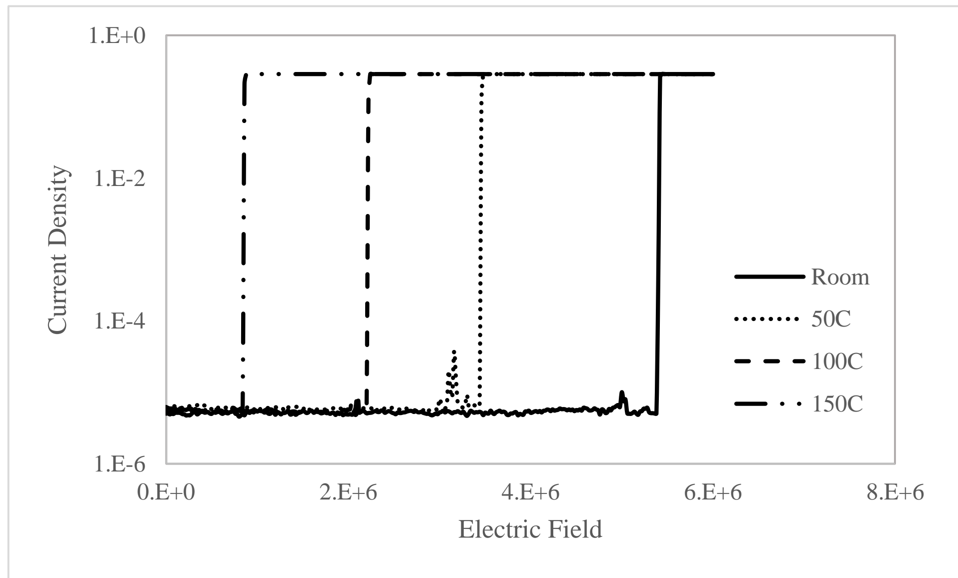


Figure 6.26: Current Density Vs Electric Field for 0.06” device

Clearly, the onset of high currents decreases with increasing temperature. The transition to the low resistance state is very abrupt. Other observations are listed as follows:

- The change in current density is so rapid that even the logarithmic axis of current density is unable to capture the fine nuances of this transition.
- Apparently, after stressing the device significantly with some positive voltage, the conductive bridge formation takes place almost immediately after the voltage sweep has crossed some critical voltage values.
- The conductive state of the dielectric breakdown is permanent.

The final conclusion can be summarized as follows. Figure 6.25 appears to indicate that the dielectric is not uniform from sample to sample, meaning that we are dealing with different dielectric as the position gets changed for nominally the same material. This may be caused by a very non-uniform distribution of defects such as voids.

Arrhenius Plot and Extraction of Activation Energy

Owing to the sharp change in resistive state from high resistance (HRS) to low resistance (LRS), initial plot of current density against thermal voltage was non-conclusive. The compliance current was increased from 0.1mA to 5mA in order to capture the switching better. However, the results were still quite inconclusive as observed in Figure 6.27 (a).

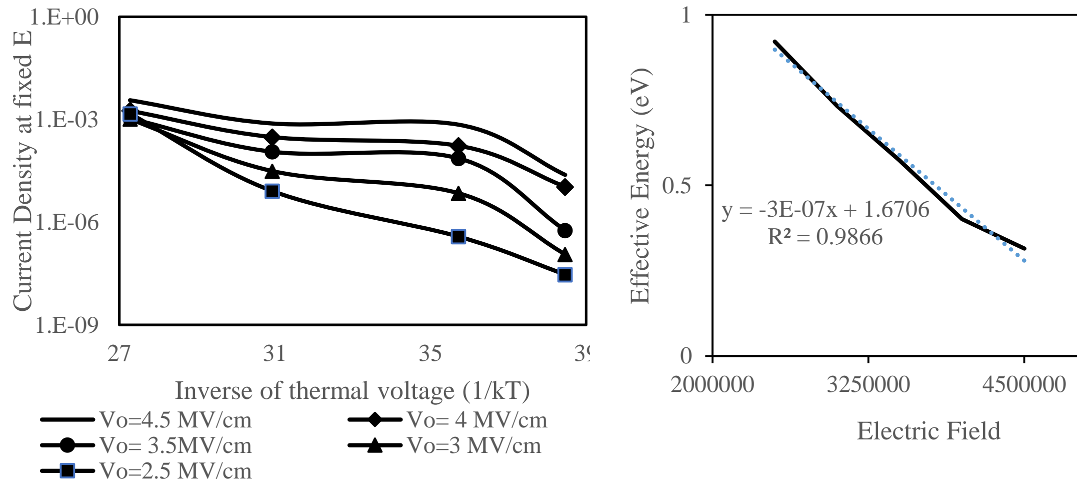


Figure 6.27: Arrhenius Plot for 0.06” device (a) Current density vs. inverse of thermal voltage (b) effective energy vs. electric field.

This graph has been plotted from the erratic values obtained from Figure 6.25. It is not saying much because of a very sharp increase in current. Therefore, we conclude that for this sample the mechanism of eq. (6.5) is not applicable, or in other words, the breakdown is not the result of stochastic accumulation of defects. The sharp transition indicates rather formation of a conductive filament, however, such that cannot be ruptured. In the figure above the plots for various electric field sort of converges into one points that is at 150C. The convergence of lines at the highest temperature is an artifact of limiting the current by the imposition of the compliance current. Therefore, the last point should be excluded from further analysis.

However by calculating the variation of the effective activation energy with respect to electric field we have:

$$\mathrm{E_a} = 1.6706\ \mathrm{eV} \qquad \beta = 30\ e - \text{Å} \qquad E_{bd} = 5.57\ MV/cm$$

The critical breakdown field makes sense because it usually takes in a pretty high voltage to cause a voltage breakdown. (>10V). However the pre-exponential constant remains unresolved because of the erratic nature of the current density variation.

Time dependent Dielectric breakdown

The TDDB plot against electric field, shown in Figure 6.28, turned out to be surprisingly clear-cut. We believe that Figure 6.28 is an important finding because this clearly illustrates that carrier generation does not comply with Poole-Frenkel Effect and that the relation: $\ln(\frac{1}{t_{TDDB}}) \propto E$ holds. The slope of this line will give us the factor β explained in eq. 5 and the generation rate for the carriers can be established.

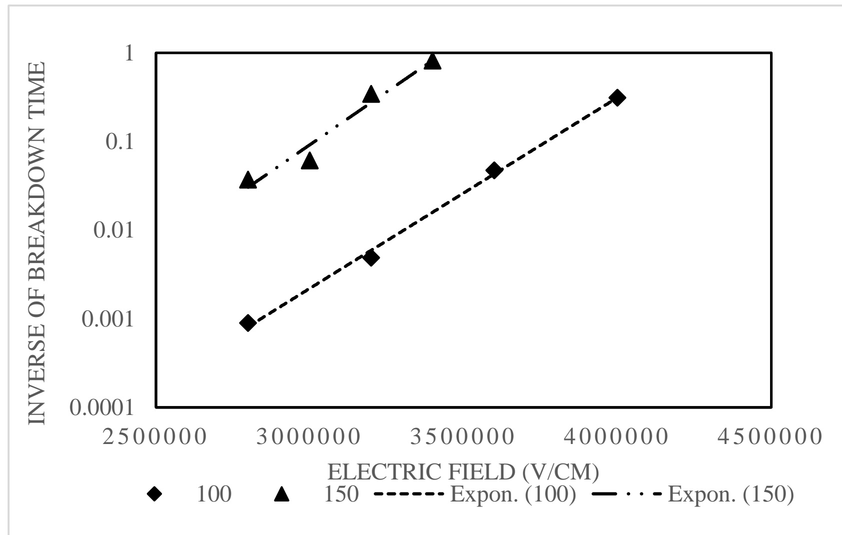


Figure 6.28: Variation of breakdown time Vs. Electric Field

From the graph we found:

$$m = 5 \times 10^{-6}$$

This translates to a value of $\beta_{100} = 16.16$ e − Å and $\beta_{150} = 18.33$ e − Å

This also states that some definite activation energy is manifested during the carrier generation of Sample No 684.

Sample No 692

Sample #'s	Bottom Electrode	Dielectric	Dielectric Constant-k	Dielectric Density (g/cm3)	Dielectric Thk (nm)	Top Electrode
692	Ta/Cu	SiON:H	6.3	2.5	25	Al/Ti

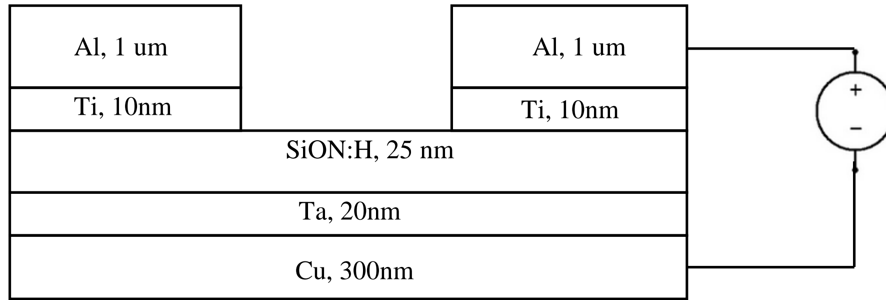
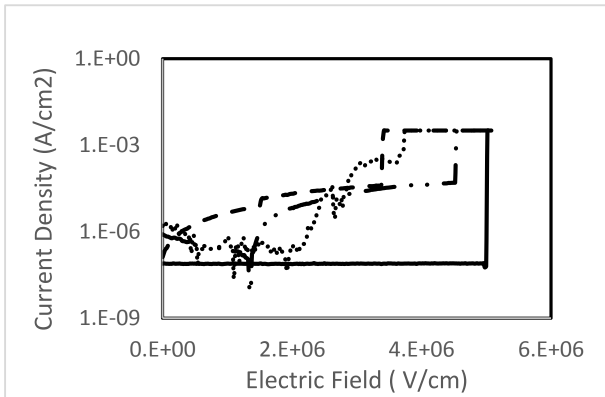


Figure 6.29: Experimental Set-up for Sample no 692

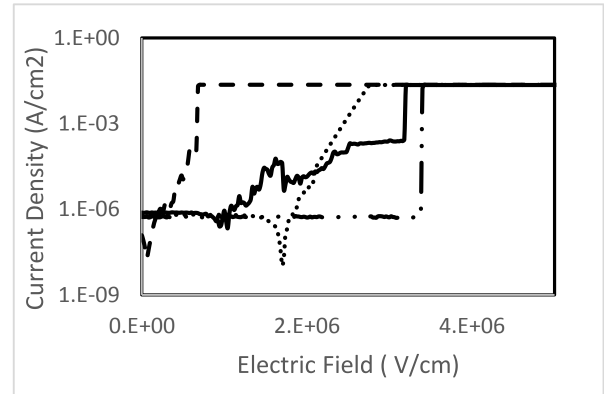
Figure 6.29 gives the schematic representation of the experimental setup. The five differently sized devices were individually tested for repeatability as explained in the test methodology and the following results were obtained.

I-V characteristics for this sample is similar to Sample no 684. The SET characteristics are sharp and does not follow a soft current build-up like the previous samples. Also, the conductive bridge formed in this case is a **permanent** one which means every test was required to be repeated on a fresh sample. It has posed similar roadblocks as in Sample No 684 and hence does not exhibit resistive switching tendencies.

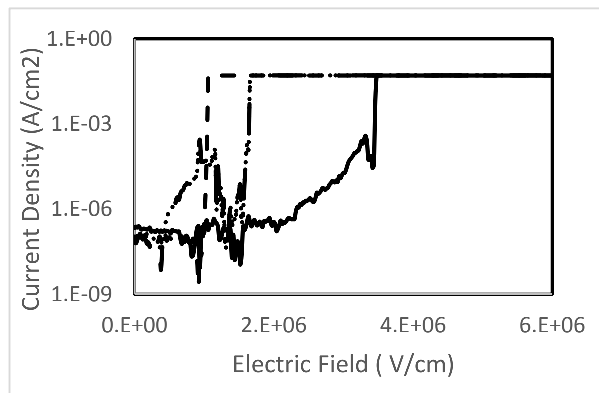
Current Density vs Electric Field



0.08 inch



0.03 inch



0.02 inch

Figure 6.30: Erratic switching of current density

Repeatability of the measurements for these samples was a big issue for this sample. The fact is well evident in Figure 6.30. After several trials a reasonable plot was obtained for 0.06 inch diameter sized device and is given in Figure 6.31.

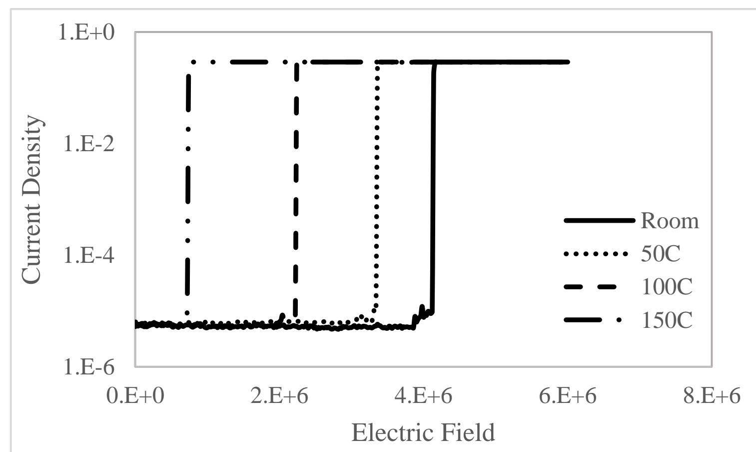


Figure 6.31: Current Density Vs Electric Field for 0.06” device

This graph is satisfactory and similar in more than one aspect to Sample no 684. This sample also exhibits abrupt change of resistive state.

Arrhenius Plot and Extraction of Activation Energy

Owing to the sharp change in resistive state from HRS to LRS, initial plot of current density against thermal voltage was inconclusive. The compliance current was increased from 0.1mA to 5mA in order to better capture the switching.

Time Dependent Dielectric Breakdown

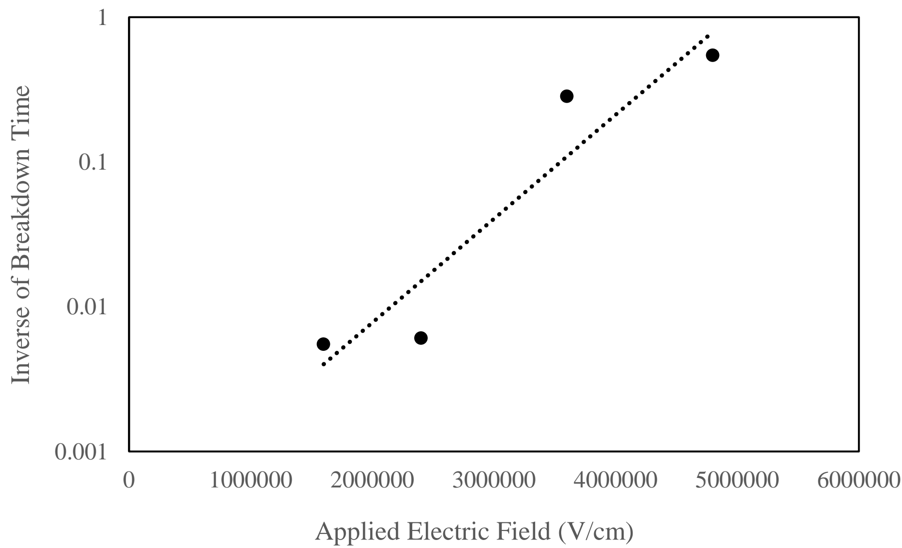


Figure 6.32: TDDB Analysis at 50C for Sample no 692

Figure 6.32 shows the time dependent dielectric breakdown analysis done for Sample no 692 at 50C. The characterization yields a slope value of:

$$m_1 = 2\times10^{-6}$$

Consecutively we calculate the dipole moment factor β to be 2.79 e-Å. The dipole moment factor value is rather low in comparison to other samples.

Sample No 685

Sample #'s	Bottom Electrode	Dielectric	Dielectric Constant-k	Dielectric Density (g/cm3)	Dielectric Thk (nm)	Top Electrode
685	Ta/Cu	SiCN:H	5.85	2.25	25	Al/Ti

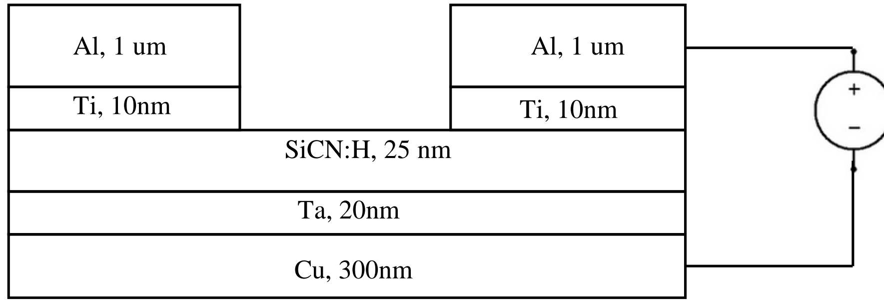


Figure 6.33: Experimental Set-up for Sample no 685

Figure 6.33 gives the schematic representation of the experimental setup. The five different sized devices were individually tested for repeatability as explained in the test methodology and the following results were obtained.

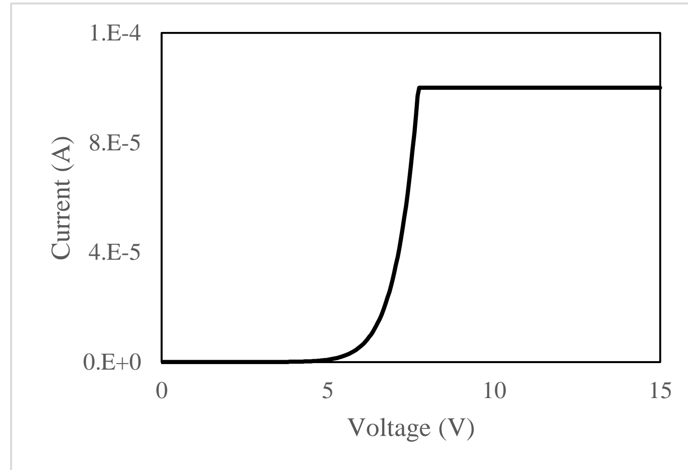
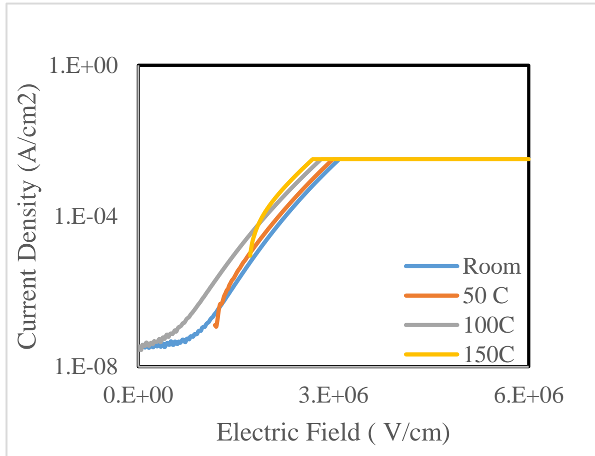


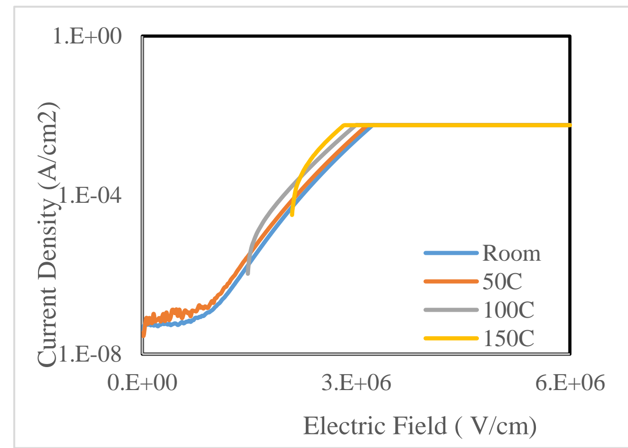
Figure 6.34: Voltage Sweep Test

Figure 6.34 shows the **soft volatile** SET range for sample no 695. We have limited the current range in the sample to 0.1 mA in order to avoid a permanent damage of the MIM sample. This device also did not exhibit any resistive switching tendencies.

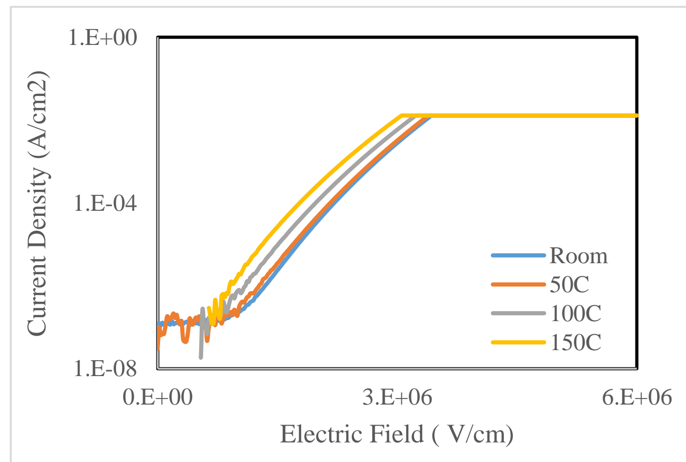
Current Density Vs Electric Field



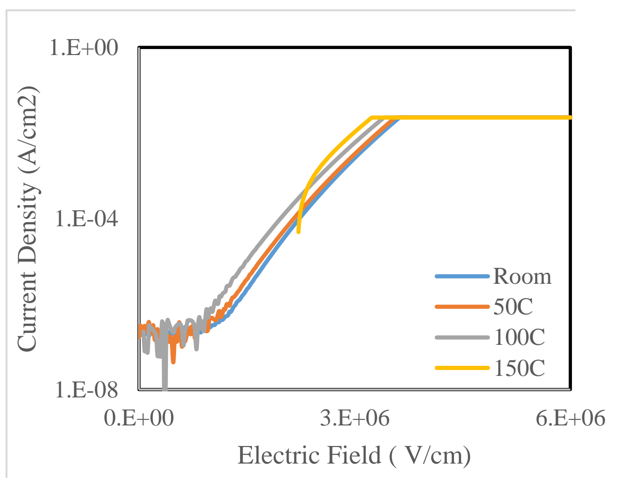
0.08 inch



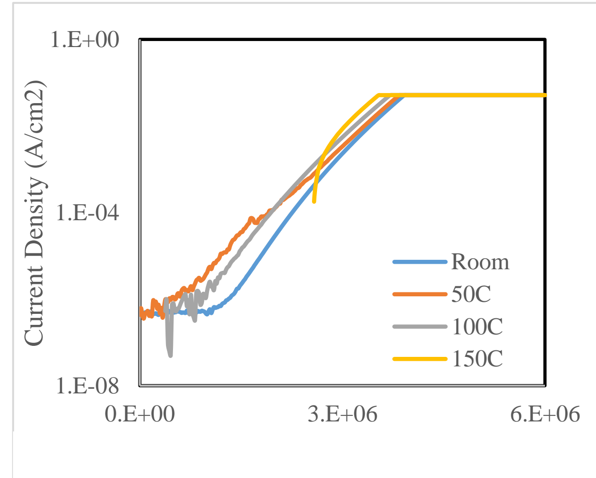
0.06 inch



0.04 inch



0.03 inch



0.02 inch

Figure 6.35: Current Density Vs Electric Field for different device size

Similar to Sample no 695, in Figure 6.35 we see that the current density gradually increases as the temperature increases. The nature of the graph is very stable and could possibly prove to be good choice of ILD.

Analysis of Thermal Behavior

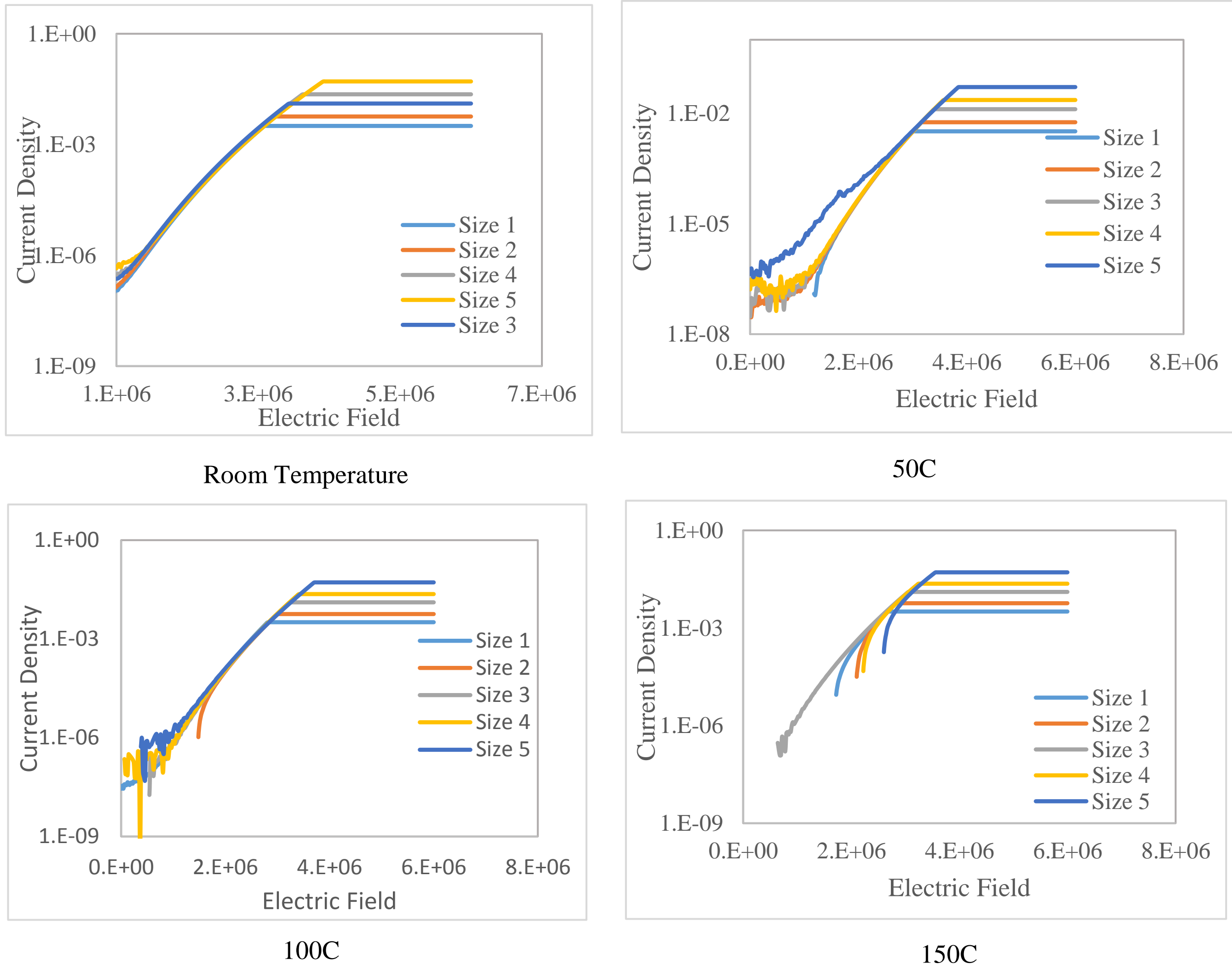


Figure 6.36: Current Density Vs Electric Field for various temperatures

Again as expected, in Figure 6.36, the current density remains constant. Since we have five different device sizes for the sample, current density could be given as follows:

$$J = I_1A_1 = I_2A_2 = I_3A_3 = I_4A_4 = I_5A_5$$

Each of the graph shows that the current density before reaching the compliance current is constant for all sample sizes.

Arrhenius Plot and Extraction of Activation Energy

The plot for current density at a particular electric field against inverse of thermal voltage is given in Figure 6.37

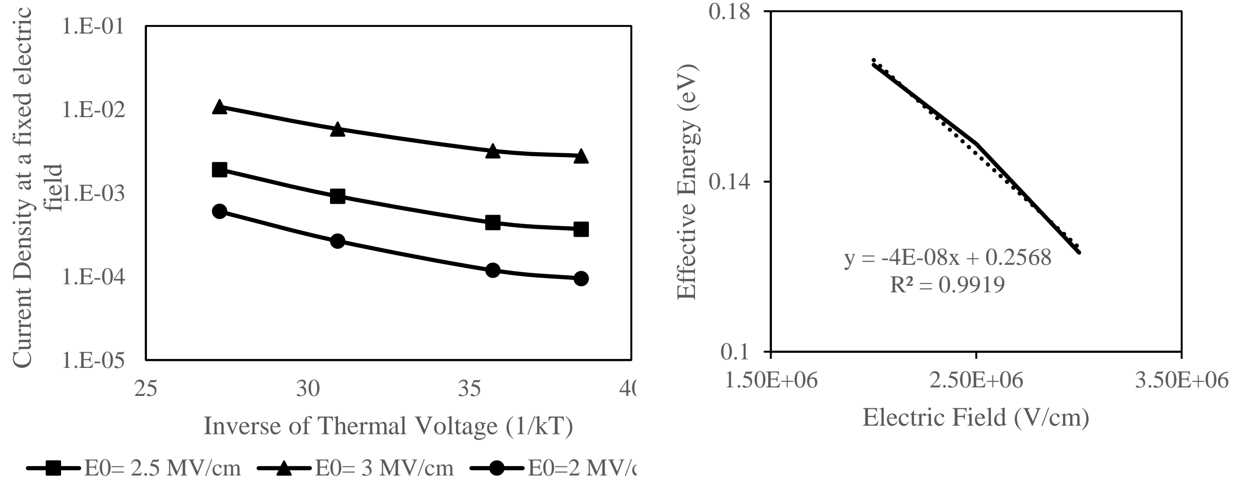


Figure 6.37: Arrhenius Plot for 0.06" device (a) Current density vs. inverse of thermal voltage (b) effective energy vs. electric field.

In Figure 6.35 (a) though all the three plots have similar nature, on close observation one can notice their almost straight line behavior. The value of the activation energy can be extracted from Figure 6.35(b). The data utilized for this plot has been obtained from 0.06 inch device size. From Figure 6.35 three effective energies were calculated from the three plot. The final parameters were calculated as:

$$\mathrm{E_a} = 0.2568 \text{ eV} \qquad \beta = 4\ e - \text{Å} \qquad E_{bd} = 6.42\ MV/cm$$

The low activation energy and low dipole moment factor as opposed to values found for conventional high-k metal oxides cited in the literature, result in an expected value breakdown electric field. The pre-exponential constant J_O has been calculated as 0.0525 calculated for 2 MV/cm.

Sample No 697

Sample #'s	Bottom Electrode	Dielectric	Dielectric Constant-k	Dielectric Density (g/cm3)	Dielectric Thk (nm)	Top Electrode
697	Ta/Cu	SiCOH	4.8	2	25	Al/Ti

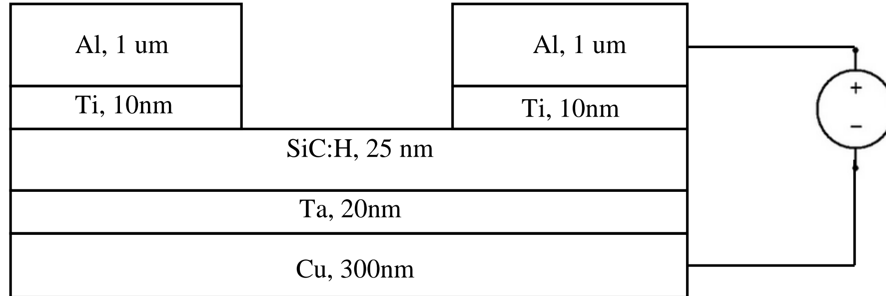


Figure 6.38: Experimental Set-up for Sample no 697

Figure 6.38 gives the schematic representation of the experimental setup. The five different sized devices were individually tested for repeatability as explained in the test methodology and the following results were obtained.

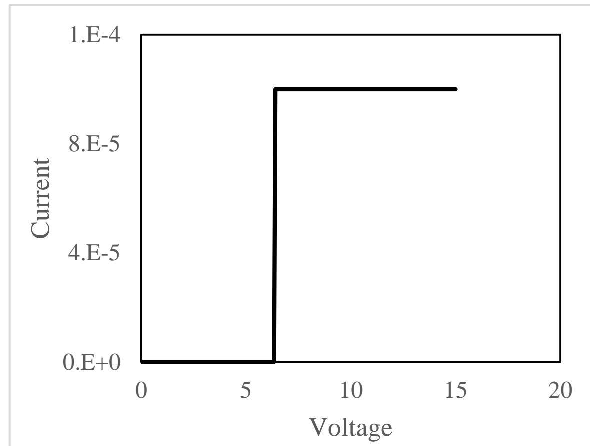
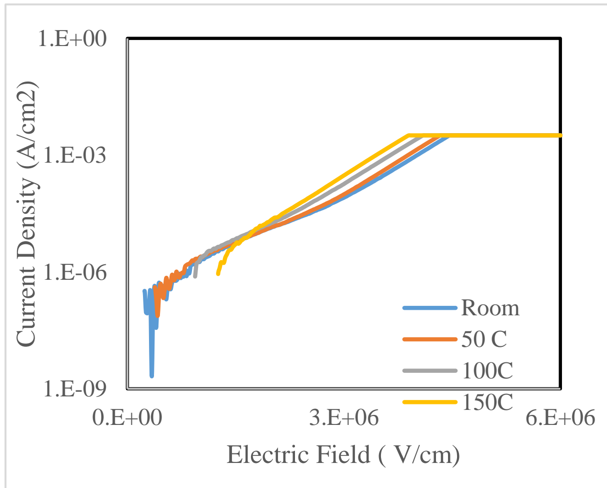


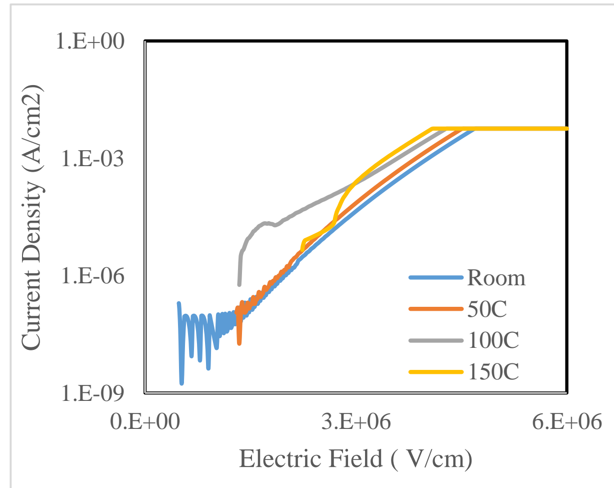
Figure 6.39: Voltage Sweep Test

I-V characteristics shown in Figure 6.39 is similar to Sample no 684. The SET characteristics are sharp and does not follow a soft current build-up like the previous samples. Also, the conductive bridge formed in this case is a **permanent** one which means every test was required to be repeated on a fresh sample. The devices are not “reset-able”.

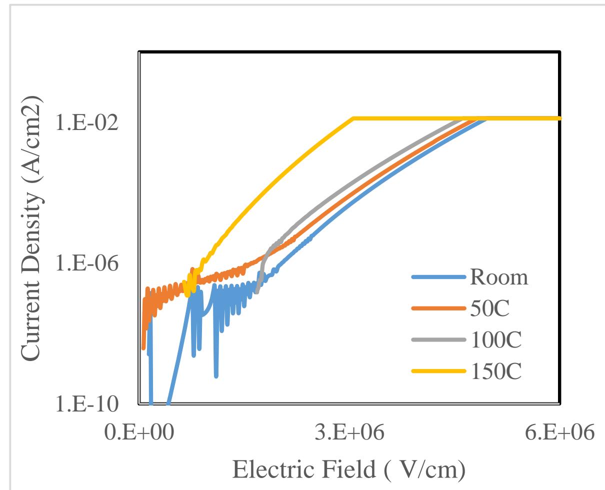
Current Density Vs Electric Field



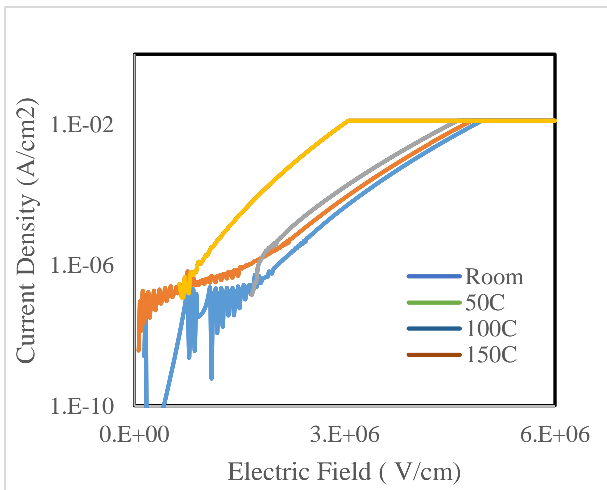
0.08 " inch



0.06 " inch



0.04 " inch



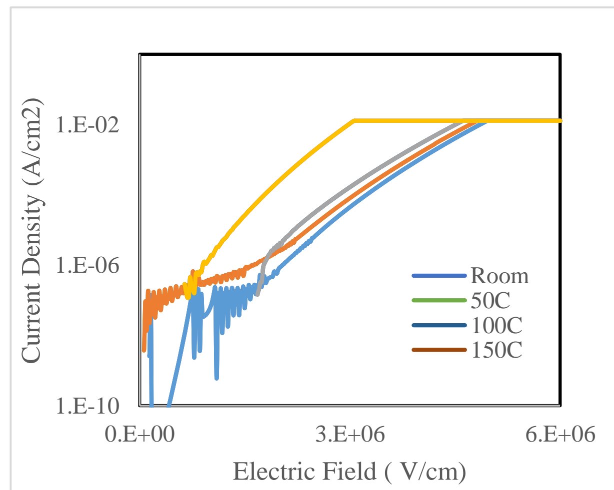


Figure 6.40: Current Density Vs Electric Field for different device size

Figure 6.40 shows the smooth variation of current density with respect to applied electric field. Similarly after performing a temperature based study we extract the Arrhenius plot. We postulate that similar to previous devices for a particular device at a particular temperature, the current density remains constant. Since we have five different device sizes for the sample, current density could be given as follows:

$$J = I_1A_1 = I_2A_2 = I_3A_3 = I_4A_4 = I_5A_5$$

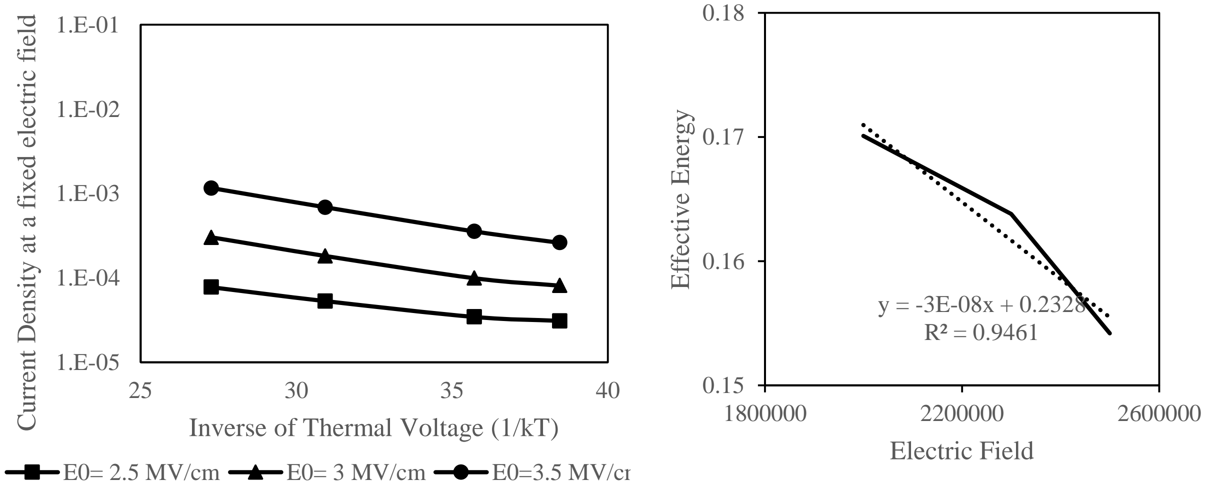


Figure 6.41: Arrhenius Plot (a) Current density vs. inverse of thermal voltage (b) effective energy vs. electric field.

Figure 6.41 again provides a very consistent picture. An almost constant value of activation energy can be calculated owing to the parallel nature of the line plotted at different electric field. The data utilized for this plot has been obtained from 0.04 inch device size.

The parameters extracted out from the above plots are given as follows:

$$E_a = 0.2328 \text{ eV} \qquad \beta = 3\ e - \text{Å} \qquad E_{bd} = 7.76\ MV/cm$$

The low activation energy and low dipole moment factor as opposed to values found for conventional high-k metal oxides cited in the literature, result in an expected value breakdown electric field. The pre-exponential constant J_O has been calculated as 0.1124 calculated for 2.5 MV/cm.

Sample No 676

Sample #'s	Bottom Electrode	Dielectric	Dielectric Constant-k	Dielectric Density (g/cm3)	Dielectric Thk (nm)	Top Electrode
676	Ta/Cu	SiN:H	6.5	2.5	25	Al/Ti

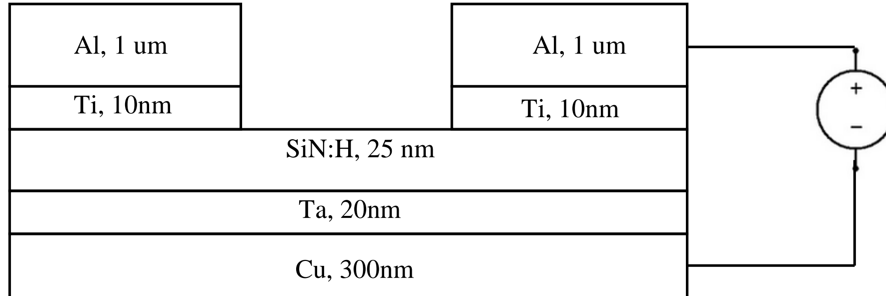


Figure 6.42: Experimental Set-up for Sample no 676

Figure 6.42 gives the schematic representation of the experimental setup. The five different sized devices were individually tested for repeatability as explained in the test methodology and the following results were obtained.

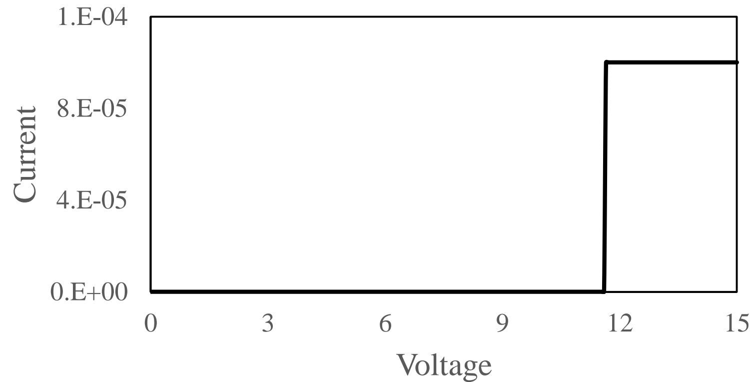
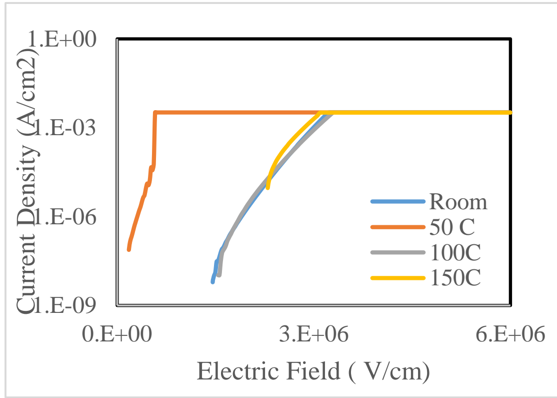


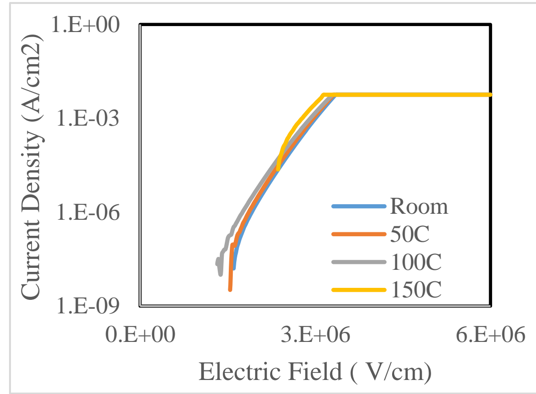
Figure 6.43: I-V Characteristics

I-V characteristics shown in Figure 6.43 is rather different as opposed to the previous sample. The SET characteristics are sharp and does not follow a soft current build-up like the previous samples. Also, the conductive bridge formed in this case is a **permanent** one which means the dielectric is permanently damaged. Hence for every test s fresh sample is characterized. These devices do not possess resistive switching capabilities.

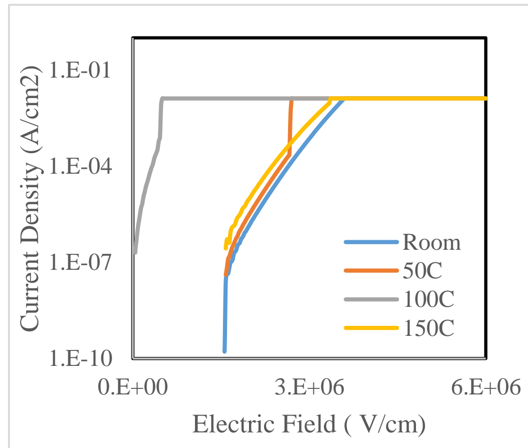
Current Density Vs Electric Field



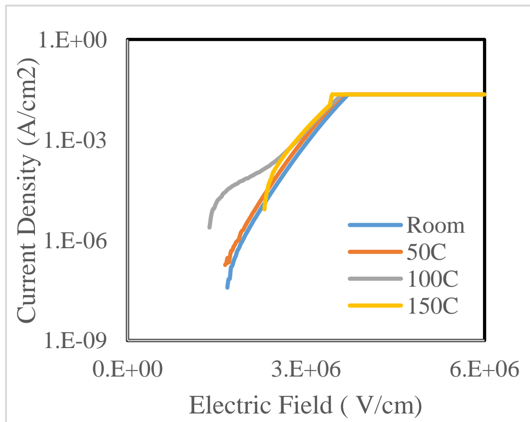
0.08 inch



0.06 inch



0.04 inch



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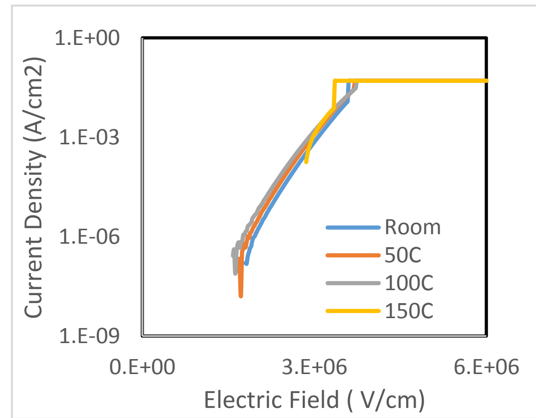

0.02 inch

Figure 6.44: Current Density Vs Electric Field for different device size

Figure 6.44 shows the gradual variation of current density. Apart from a few surprising crossovers, the general picture is similar to the most of the previously characterized devices.

Analysis of Thermal Behavior

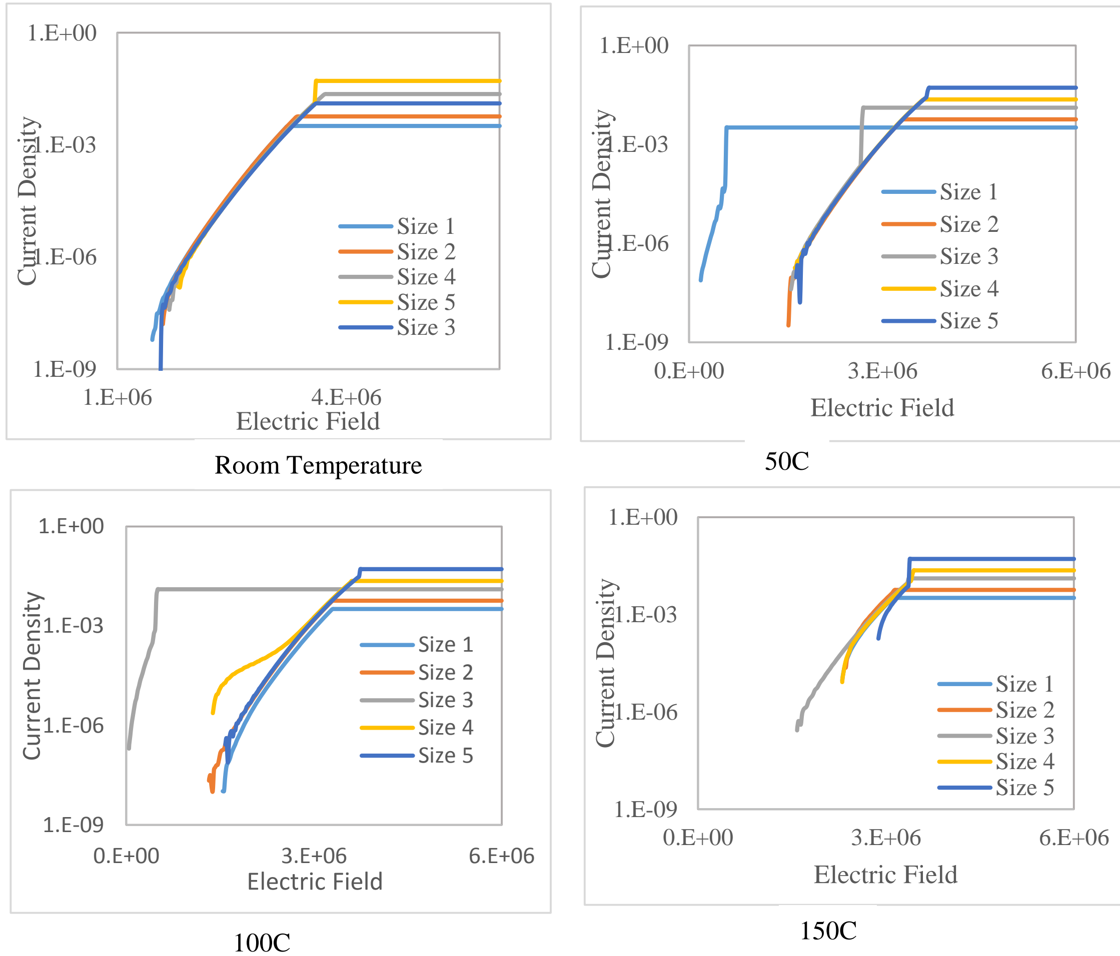

Figure 6.45: Current Density Vs Electric Field for various temperatures

Again as expected, in Figure 6.45, the current density remains constant. Since we have five different device sizes for the sample, current density could be given as follows:

$$J = I_1A_1 = I_2A_2 = I_3A_3 = I_4A_4 = I_5A_5$$

Each of the graph shows that the current density before reaching the compliance current is constant for all sample sizes.

Arrhenius Plot

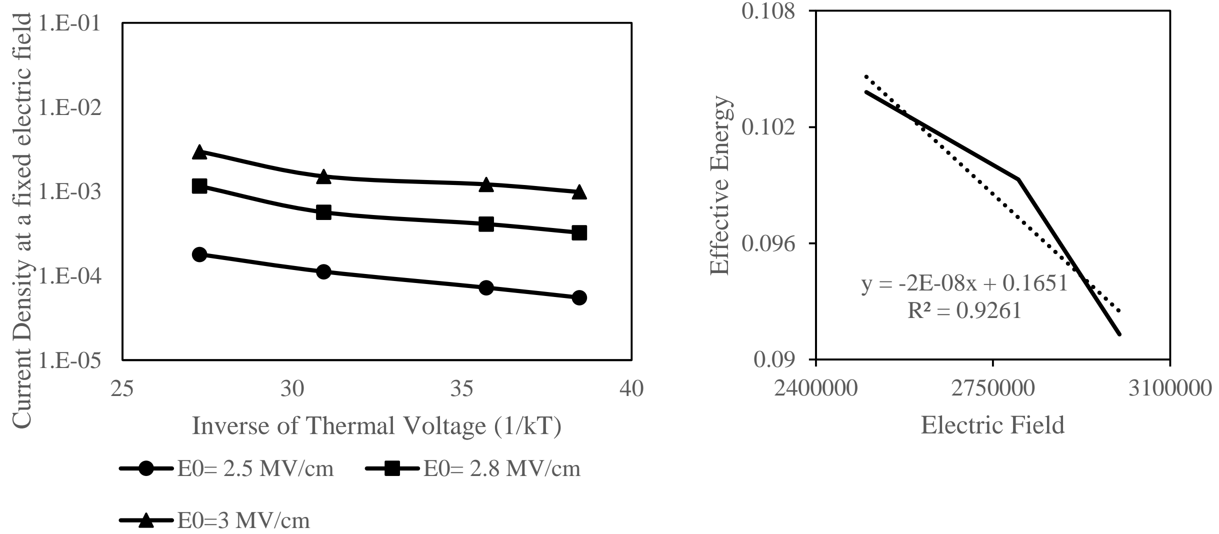

Figure 6.46: Arrhenius Plot (a) Current density vs. inverse of thermal voltage (b) effective energy vs. electric field.

Figure 6.46 again provides a very consistent picture. An almost constant value of activation energy can be calculated owing to the parallel nature of the line plotted at different electric field. The data utilized for this plot has been obtained from 0.06 inch device size. The parameters extracted out from the above plots are given as follows:

$$\mathrm{E_a} = 0.1651\ \mathrm{eV} \qquad \beta = 2\ e - \text{Å} \qquad E_{bd} = 8.26\ MV/cm$$

The low activation energy and low dipole moment factor as opposed to values found for conventional high-k metal oxides cited in the literature, result in an expected value breakdown electric field. The pre-exponential constant J_O has been calculated as 0.0029 calculated for 2.5 MV/cm.

Summary of the results at a glance

Table 6.3: Arrhenius Plot							
Sample No	**Dielectric**	**Dielectric Constant-k**	**Activation Energy (Ea) in eV**	**Dipole Moment factor (β) in e-Å**	**Critical Breakdown field (MV/cm)**	**Electric field for constant calculation (MV/cm)**	**Proportionality Constant Jo (Factor of Go)**
684	SiOC:H	3.2	1.6706	30	5.57E+06	Unresolved	
697	SiCOH	4.8	0.2328	3	7.76E+06	2.5	0.1124
695	SiC:H	7.2	0.2889	20	1.44E+06	0.2	1.0874
685	SiCN:H	5.85	0.2568	4	6.42E+06	2	0.0525
688	SiNC:H	4.8	Unresolved				
676	SiN:H	6.5	0.1651	2	8.26E+06	2.5	0.0029
692	SiON:H	6.3	Unresolved				

Table 6.4 TDDB Plot					
Sample No	**Dielectric**	**Dielectric Constant-k**	**Temperature**	**β**	**Resistive Switching**
684	SiOC:H	3.2	100	16.16	No
			150	18.33	
697	SiCOH	4.8	Unresolved		No
695	SiC:H	7.2	Unresolved		No
685	SiCN:H	5.85	Unresolved		No
688	SiNC:H	4.8	100	12.93	No
			170	7.67	
676	SiN:H	6.5	Unresolved		No
692	SiON:H	6.3	50	2.79	No

The observations made can be listed as follows:

- None of the samples exhibit resistive switching for memory applications.
- Sample no 676 has the lowest defect generation rate.
- Sample no 684 has the highest activation energy. This is owing to the fact that the dipole moment is immensely large However in room temperatures, Sample no 688 is likely to have a very high activation but we are unsure about the mechanism. As opposed to other samples, this samples is less likely to undergo dielectric breakdown.
- More tests are required on sample no 684 and 692 in order to resolve the sharp transition from HRS to LRS. This will help in resolving the Arrhenius Plot and related calculations.

6.5 Conclusions

- The electron emission in the devices characterized do not comply with the Poole-Frenkel Model
- The samples can broadly be classified into two categories.
  - Some of the samples display abrupt breakdown. Such a feature is conducive to resistive switching. However this kind of breakdown leads to a permanent damage in the dielectric and this renders the devices ON forever.
  - The other kind of samples exhibit a soft breakdown. Here samples undergo a graduate degradation of dielectric thus results in the formation of a conductive path. However, once disconnected from the power supply, this conductive path formed disappears. The resistive switching observed is inherently volatile.
- None of the samples characterized in this chapter exhibits non-volatile resistive switching. Such structures need to be modified in order to show resistive switching.
- As already explained in Chapter 5, the best chance to expect resistive switching is possible if the device possesses the following properties:
  - An active metal that can be ionized in to the dielectric thus providing the building material for the metallic filament or for the opposite bias conditions would provide a large pool of free electrons to create defect reaction of the type:
  - $O + 2e^- \rightarrow >O^{2-} + V_O$. i.e. electron ionizes oxygen (if present) of the dielectric, the oxygen ion migrates in the high electric field and leaves an oxygen vacancy behind (V_O).
  - An inert counter electrode that can lead to formation of a conductive filament with a highly resistive constriction, for example a “cone-like” tip and therefore is “reset-able”.
- More studies need to be carried out in order to understand the contribution of the ILD completely. From literature a set of materials have been identified that could serve as electrode for possible memory application making use of Intel ILDs. The following devices have been proposed for future study. The structures listed below have been recommended to Intel for manufacturing and characterization:
  - Cu/ILD/W
  - TaN/ILD/TiN
  - Cu.ILD/TaN
  - Cu/ILD/TiN
  - Ti/ILD/W

Chapter 7: Summary and Future Work

This chapter summarizes the results obtained on metal/insulator/metal devices and their suitability for resistive switching memory applications. A reliable resistive switching mechanism is proposed to be based on the formation and rupture of a metallic conductive filament that displays some sort of constriction or weak link. If filaments without a weak are formed, it is difficult to rupture them, and, consequently, a repeated resistive switching is not possible. In this work we have identified metal-insulator-metal (MIM) structures and materials that display both types of filaments. This may serve as a guide for a selection of suitable materials rendering multiple resistive switching viable. Possible future areas of research are outlined below to better understand the formation and dissolution of metallic and oxygen vacancy filaments and their relation to commonly known volatile and non-volatile dielectric breakdown mechanisms.

7.1 Summary

The metal-oxide-semiconductor structures are a prime candidate for a continued scaling of the flash memory cell size. However, the continued scaling runs into a latency problem with signal propagation in the interconnecting metal lines. The time delay due to interconnect negates most of the advantages of smaller and faster memory devices. To overcome the fundamental scaling limitation of CMOS devices and signal latency obstacles, emerging non-CMOS device technologies are proposed to be implemented in CMOS interconnect metallization above the CMOS logic circuitry. In order to make such back-end memory viable, the new nonvolatile memory has to be rendered compatible with CMOS back-end processing and materials used therein. Researchers have investigated in several directions viz., various voltage waveforms, alternate material structures and several techniques of characterization in order to optimize the emerging technology. In this research, MIM devices are fabricated with different choices of materials for the electrodes and characterized for a better understanding of the physics of resistive switching memory and its relation to various modes of dielectric breakdown.

This thesis is broadly divided into two segments: a) Cu/TaO_X/Pt resistive switching memory and b) low-k dielectric metal interconnect structures. Through similar characterization methods, different aspects of the devices were studied, analyzed and models for underlying mechanisms derived.

Resistive switching in Cu/TaO_X/Pt devices manifests itself in two different forms, viz. Cu and oxygen vacancy conductive filaments. Our investigation has revealed that the mechanism for the two kinds of filaments are quite different. In contrast to Cu nanofilaments, an oxygen vacancy nanofilament formation appears to involve the interaction of two separate mechanisms: a surface-initiated mechanism and a bulk mechanism of creation of oxygen vacancies as described in Chapter 3. The two mechanisms manifest themselves in a rather complex dependence of the on-resistance R_{on} as a function of the compliance current. In case of Cu filament only the surface-mechanism appears to be at work resulting in the relation $R_{on}=V_{SET,MIN}/I_{CC}$.

In a separate study, it was also found that for a resistive switching device, a mostly linear interdependence exists between the RESET voltage and the subsequent SET voltage and vice versa. The use of this dependence allows the users to condition the read voltage of a device by changing the ramp rate of the applied voltage sweep. Resistive switching (RS) devices suffer from broad distributions of SET or write and RESET or erase threshold voltages. Thus by the application of a method proposed here, a very tight distribution of the read and erase voltages may be obtained as opposed to the broad natural distributions of the fresh device. Such a tightening procedure for the V_{SET} and V_{RESET} distributions is indeed very desirable for modern day semiconductor industry.

Intel, as the leading CMOS manufacturer, challenged with the latency problem of interconnect and in an effort to mitigate the problem, has identified several low-dielectric materials as an alternative for the CVD SiO_2, in a Cu interconnect structures. Lower k value of the interlayer dielectric in the CMOS back-end will reduce parasitic capacitance and, hence, the signal time delay. Owing to the immense potential lying in the field of resistive switching devices, Intel alongside Virginia Tech is investigating the possibility to incorporate the fundamental concepts of resistive switching in back-end-of-line to overcome latency and several reliability problems. Electric reliability of the various metal-insulator-metal structures was characterized by performing a time-dependent dielectric breakdown. It was observed dielectric with lower density were unreliable because of their fluffy (porous) nature and not well understood breakdown mechanisms. The challenge is to collocate resistive switching memory with the back-end metallization and to find compatible materials and processing techniques for the two different functionalities. Our collaboration with Intel has yielded first encouraging results.

7.2 Future Work

This research explores and evaluates the switching characteristics and mechanisms of metal/insulator/metal devices. In order to fully exploit the advantages of resistive switching devices, future investigation can be done in the following areas.

1. A robust processing technology needs to be formulated. To improve the electrical performance and reliability of resistive memory, the dielectric material has to be engineered in such a way as to possess low k dielectric constant and at the same time good electrolytic properties for metal and/or oxygen ions. The rationale for the ideal resistive switching material system has not yet been well developed. The material properties are closely related to the processing method (various PVD, ALD and CVD) which finally determines the device performances. Therefore further research is required to better understand the electrode-electrolyte interaction and refine the processing technologies.

2. Linear voltage sweep has proven to be one of most resourceful modes for I-V characterization. However, so far, all the experiments were conducted keeping 0 V as the origin for the starting voltage of the sweep. We have explained successfully the impact of the ramp rate on the V_{SET} and V_{RESET} values of a resistive switching cells as described in Chapter 4. The key to the explanation was the assumption that for a local dissolution of a

filament a critical Joules heat is needed. The critical Joules heat $Q_{crit,}$ for our routine characterization procedure, is given by $Q_{crit} = \int_0^{V_{reset}/rr} \frac{rr^2 t^2}{R_{on}} dt \qquad eq.(1)$

where the ramp started always at V=0. One of the aspects of future research is to investigate the effects of resistive switching having a non-zero start voltage during RESET or SET operation. From the expression given above one would expect a higher V_{RESET} when the starting voltage is closer to V_{RESET} rather than being zero. With lower boundary, being no longer zero, the upper boundary of the integral of eq.(1) has to be higher in order to accommodate the same Q_{crit}. Indeed, the Figure 7.1 appears to confirm this for a negative starting voltage. One observes that V_{RESET} moves to higher values. However, for positive starting voltage, one is obtaining surprisingly a larger V_{RESET} voltage too as shown in Fig.7.1, whereas from eq.(1) one would expect a lower V_{RESET} value. One would expect this, especially for a large ramp rate, that starting at a large positive voltage V_{RESET} would be small, because a lot of Joules heat has been deposited in the filament. Therefore, a positive starting voltage to assist a rupture of nanofilaments at low V_{RESET} values. However the results achieved so far portray a different picture altogether. Figure 7.1 demonstrates the effect showing that with starting positive voltage V_{RESET} increases. This calls for further investigation of the effect and its underlying mechanisms. The same dependence of the starting voltage on the V_{SET} voltage for a linear voltage sweep should be also investigated.

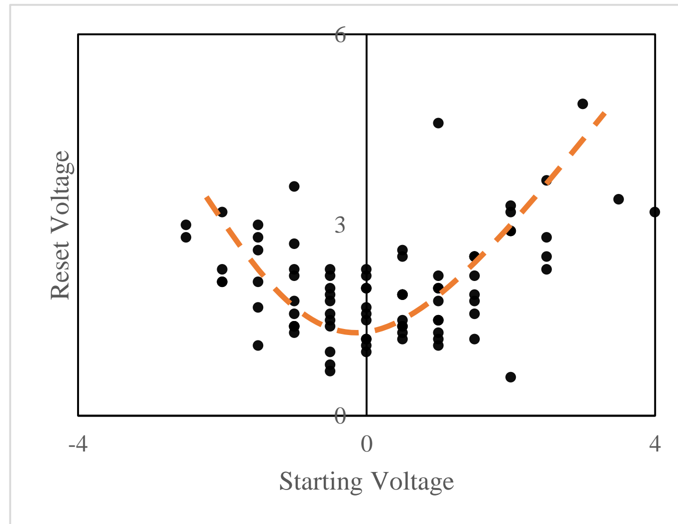

Figure 7.1: Effect of various start voltage on $V_{RESET.}$

3. Chapter 4 gives us an insight on the interdependence of SET and RESET voltages for Cu conductive filaments in Cu/TaO_X/Pt resistive switches. The results display a possibility on how one can achieve tighter distribution of operating voltages ranges. The same study can actually be carried out for the oxygen vacancy conductive filament. It will be an interesting study because of the known fact the mechanism of vacancy formation is different from that

Cu conductive filament. The primary aim would be to observe and analyze the behavior between the two mechanisms. Some preliminary ground work is been conducted for this prospect and is shown in Figure 7.2.

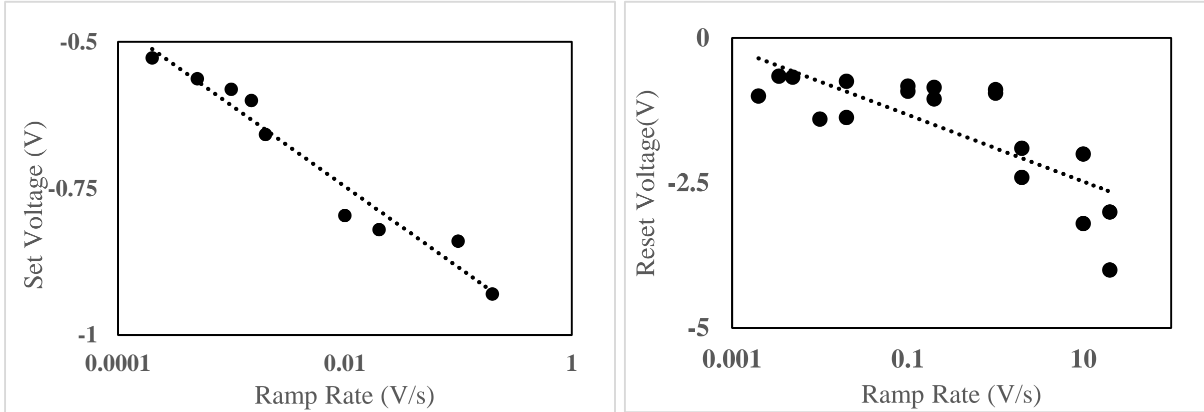

Figure 7.2: (a) Variation of V_{SET} w.r.t. Ramp Rate for vacancies (b) Variation of V_{RESET} w.r.t. Ramp Rate for vacancies.

It is seen that for oxygen vacancy filaments V_{SET} and V_{RESET} are increasing with increasing ramp rate. This is the same qualitative behavior observed for Cu filaments. However, in case of Cu filaments, the V_{SET} versus ramp rate curve is almost proportional to the logarithmic of the ramp rate in the interval from 0.01 to 2 V/s. However, when the ramp rate is less than 0.01 V/s, there is a clear departure from this behavior as the SET voltage stays essentially flat indicating a minimum SET voltage [Jap. J. Appl. Phys. 52 (2013) 084202] . In case, of oxygen vacancy filament, as shown in Fig. 7.2(a), no such saturation could be observed down to a ramp rate of 0.002 V/s. The probing of V_{SET} at smaller ramp rates was not possible due to limitation of our equipment. Nevertheless, the lack of any indication of a minimum SET voltage for V_o filaments is in qualitative agreement with the discussion of Figure 3.3 in Chapter 3, showing the dependence of the on-state resistance R_{ON} as a function of compliance current I_{CC}.

4. The Intel SRC project comes with immense opportunities. Alternative combination of interconnect structures, including the choice of metal electrodes, and interlayer dielectrics are being investigated for this purpose. This opens up a whole new possibility of establishing mechanism related to dielectric reliability and even future memory application. It will be really rewarding to have a set of materials that could exhibit similar characteristics as that of Cu/TaO_x/Pt. One of the challenges here is to replace Pt with a suitable and less costly alternative for a commercially viable manufacturing. One candidate that can be tested in the near future is tungsten (W).

5. Radiation materials science is another broad subject covering many forms of irradiation and matter. Immunity of memory cells to radiation is an important reliability aspect. It will be an interesting study to analyze the effects of total ionization dose on interconnect devices and its interplay with the complex structure. Exposure of Cobalt-60 has been

identified for this kind of exposure. Important conclusions could be deduced on whether it could affect the possibility of resistive switching. Intel is interested in this kind of investigation and is willing to provide support.

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Chapter 1-2

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