CHAPTER 7 : Conclusions and Future work

This thesis has presented a methodology and various design techniques for development of a teaching module on the World Wide Web. An educational module was developed as a part of the current thesis which aims at effectively educating acquisition and maintenance personnel on use of VHDL for design and maintenance of digital systems. While developing the module, care was taken to make the material as interesting as possible, so as to involve the user in his/her learning process, while maintaining objectivity.

The material in the educational module included the following research work: An effective testing methodology was developed where the test bench model developed to test the MUT at the behavioral level could be reused at the lower levels of abstraction. This was made possible by the use of configurations, generics and a good coding style. A technique for implementing mixed abstraction level and mixed data type models using configurations was developed. Methodologies were developed for memory testing, regression testing and diagnostic testing. Also WAVES was used to develop test benches for the Sobel edge detector. All the restrictions and modifications to WAVES outputs, needed to effectively test and diagnose digital systems have been documented.

Some of the avenues in which future work is possible are as follows :

The Sobel Edge detector model was developed at the behavioral, RTL and the gate level of abstraction. Testing was also carried out at all of these levels. As a part of the future work for the Acquisition course, an ISA (Instruction Set Architecture) model and a Performance model of the Sobel Edge detector could be developed along with the corresponding test bench to verify its

operation. As a part of the maintenance course, the following topics would be really worth teaching on the website :

- Integration of DFT (Design for testability) into the model. This would be especially useful for models containing a mixture of ASIC/FPGA models and COTS parts.

- Built-in self-test (BIST) which is a design technique in which parts of the circuit are used to test the circuit itself. This technique can be applied to the Sobel Edge detector model.

- Board level testing and simulation could be explained by developing a board layout of the Sobel edge detector and developing testing techniques for board level design.

- Teach test plan techniques using the goal tree editor results (from TPALS project). Use the goal tree editor to define the test plan for the Sobel Edge detector.

- Tutorial on how to program a model on a programmable device. We can develop FPGA models of all the filters and the magnitude processors and teach this module.

The web-site for the courseware can be further made more interactive by using all the new software available for Website development and enhancement. One way is to make use of the emerging Java technology to effectively improve the website. With applets written in Java, one can design web pages that include animation, graphics and other special effects.