A FIR Filter Embedded Millimeter-wave Front-end for High Frequency Selectivity

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ABSTRACT

Millimeter wave (mm-Wave) has become increasingly popular frequency band for next-generation high-speed wireless communications. In mm-Wave, the wireless channel path loss is severe, demanding a high output power in transmitters (Tx) to meet a required SNR in receivers (Rx). Due to the intractable speed-power tradeoff ingrained in silicon processes, however, achieving a high power at mm-Wave, particularly over W-band (> 90 GHz), is challenging in silicon power amplifiers. To relieve the output power burden, phased-arrays are widely adopted in mm-Wave wireless communication systems – namely, by leveraging a parallel power combining in the space domain, inherent in the phased arrays, the required output power per array element can be reduced significantly with increasing array size. In large arrays (> 100's – 1000's number of arrays), the required output power per element could be small, typically around several 10's mW or less in silicon-based phased arrays. In such small-to-medium scale output power level, the static power dissipations by transistor knee voltage and passive components could be a significant portion of the output power, decreasing power efficiency of power amplifiers drastically. This poses a significant concern on the power efficiency of the large-scale silicon-based phased arrays in mm-Wave. Another critical problem in mm-Wave wireless systems design is the increase of passive reactive components loss caused by worsening skin depth effect and increasing dielectric loss through silicon substrate. This essentially degrades the reactive components quality factor (Q) and limits frequency selectivity of the silicon-based mm-Wave systems. This thesis tackles these two major technical challenges to provide high frequency selectivity with maintaining high power efficiency for future mm-Wave wireless systems over W-band and beyond. First, various high-efficiency techniques such as impedance tuning with a reactive component at a cascoding stage in

conventional stacked power amplifiers or load-pull based inter-stage matching technique, rather than conventional conjugate matching, have been applied to W-band CMOS and SiGe BiCMOS amplifiers to improve power efficiency with 5-10 dBm output power level, suitable for a large phased array applications, as detailed in Chapter 2 and 3. Second, a 4-tap finite impulse response (FIR) filter based receiver architecture is presented in Chapter 4. The FIR filtered receiver leverages a sinc-pulse type frequency nulls built-in in the transmission-line based FIR filter's frequency response to increase frequency selectivity. The proposed FIR filtered receiver achieves > 40-dB image rejection by placing an image signal at the null frequency at D-band, one of the largest image rejection performance at the highest frequency band reported so far.

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GENERAL AUDIENCE ABSTRACT

Due to recent advances in Silicon based solid-state technologies, the interest towards the millimeter wave (mm-Wave) frequency band has been emerging for next-generation high-speed wireless communication applications. One of the most significant parameters in a communication system would be the output power of a transmitter. However, the output power is limited especially at mm-wave frequencies. A phased array is one of the viable solutions to overcome this burden by utilizing a parallel power combing in the space domain. The required output power per element can be relieved, typically around several tens of mill watts or less. There are two major factors limiting the output power, which are the high loss of passive and active devices. This dissertation presents solutions to overcome these challenges. In addition, a 4-tap finite impulse response (FIR) filter based receiver architecture is introduced, which rejects unwanted image signals in heterodyne systems by utilizing sinc-pulse type frequency nulls. The proposed FIR filter achieves more than 40 dB of image rejection at D-band (110-170 GHz), which is one of the highest filtering performance in the millimeter-wave frequency band.

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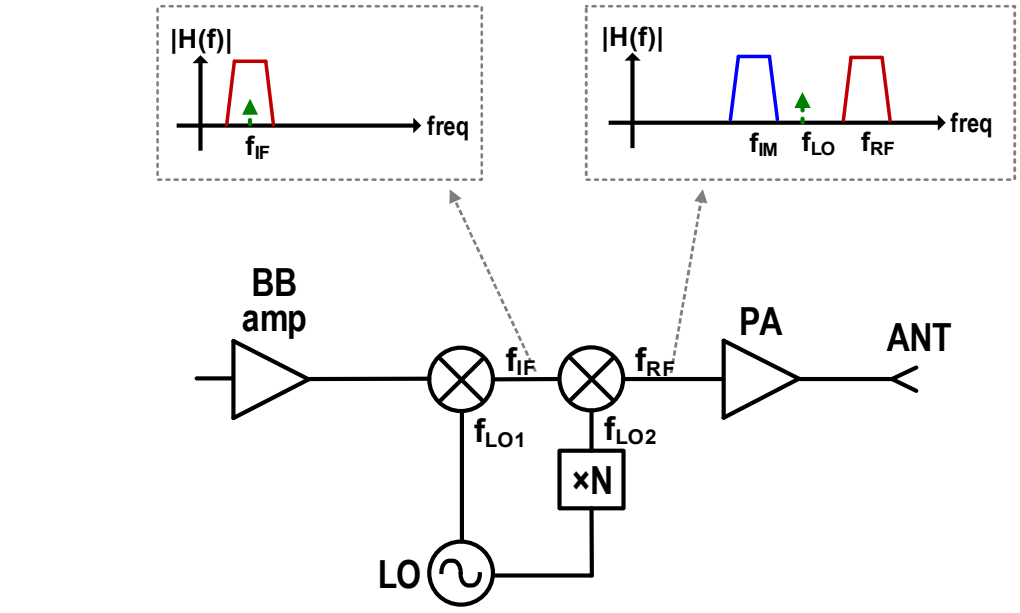
Chapter 1.

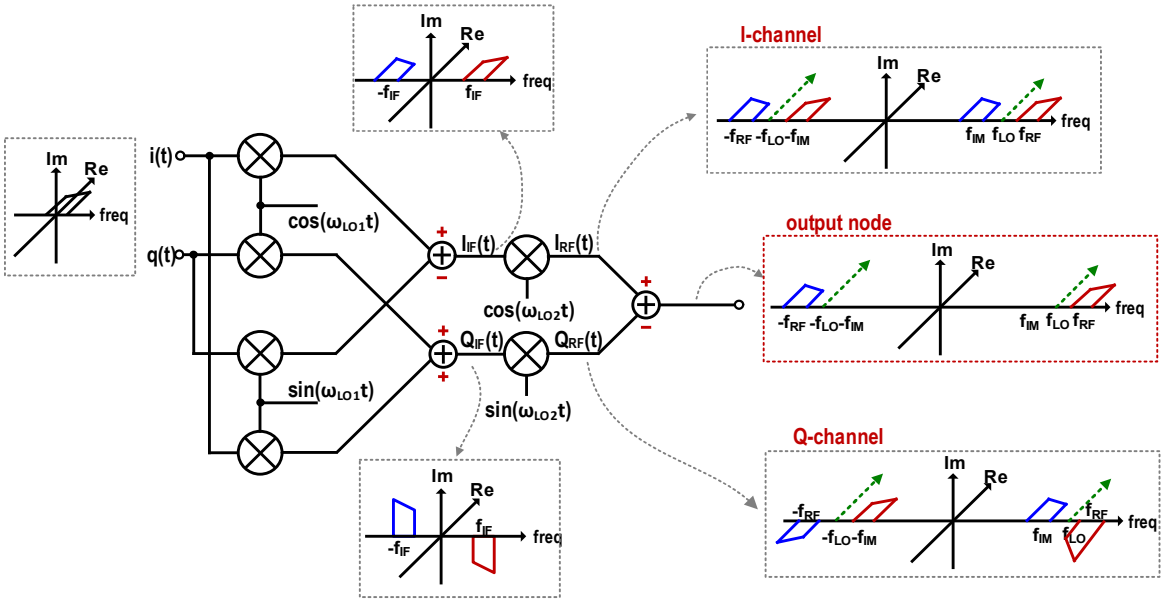
Introduction

1.1 Motivation

In the wireless communication systems at millimeter (mm)-Wave band, particularly for the silicon-based mm-Wave transceivers operating at W-band and beyond, RF heterodyne transceivers could be better choice over homodyne transceivers because the spectral purity of silicon-based oscillators in homodyne systems is quite limited at such high frequencies. Namely, the large phase noises of silicon-based oscillators at the high-end mm-Wave band could be infiltrated into signal paths by a homodyne mixer and degrade the spectral purity of transmit and receive signals in the homodyne systems. The heterodyne systems allow better phase-noise oscillators operating at much lower LO frequency than homodyne systems, enabling better spectral purity in the mm-Wave wireless communications. However, image issues are always present in the RF heterodyne transceivers [1-1]. To understand this issue, a generic heterodyne transmitter is shown in Fig. 1-1(a) where base-band (BB) signal is up-converted to RF band by two-step up-conversion mixers which are driven by f_{LO1} and f_{LO2}, respectively. After the second mixer, the image signal is also up-converted to the lower side of LO ($f_{LO} = f_{LO1} + f_{LO2}$) with the same frequency offset from f_{RF} to f_{LO}. If IF band is not large enough, the image signal can be transmitted to the receiver together with the RF signal. It may cause signal-to-noise ratio (SNR) degradation to the receivers, challenging to meet a required SNR specification. In order to relieve this image issue in the RF heterodyne systems, one popular solution is to utilize double quadrature mixers, popularly termed as complex mixing or single-side band mixing, as shown in Fig.



(a)



(b)

Fig. 1-1. (a) a generic RF heterodyne transmitter with image issue. (b) RF heterodyne transmitter with I/Q LO.

1-1(b). In the I-channel, the BB signal and image don't experience phase shift by being multiplied by cosine LO. However, they undergo ±90° phase shift with being multiplied by sine LO, so the signal and image are out-of-phased at the RF band at Q-channel. After

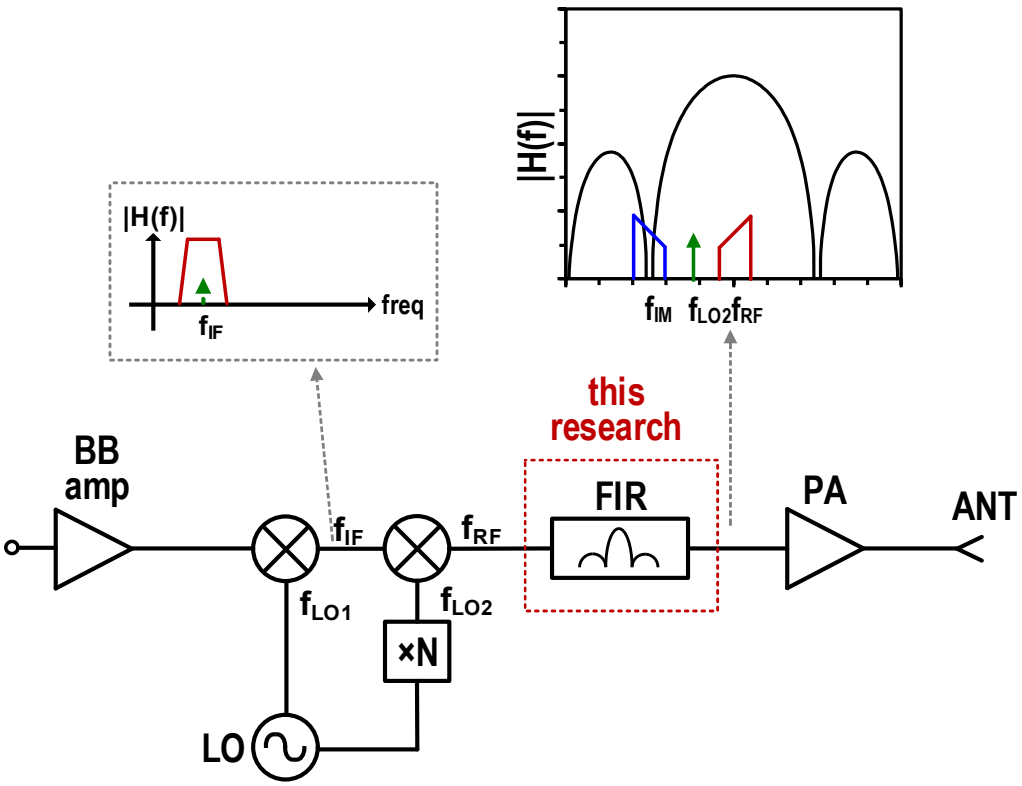


Fig. 1-2. Image rejection by FIR filtering at RF heterodyne transmitters.

combining signals at the final output, only signal is survived, allowing single sideband transmission However, the image rejection ratio of the double quadrature-mixers based approach is highly dependent on the amplitude and phase matching of I and Q signals. The I/Q matching for both RF and LO paths is increasingly challenging as increasing operation frequency due to worsening layout mismatch effects at higher frequencies - the image rejection ration is often limited to less than 30 dB at W-band and higher frequency bands in the double quadrature-mixer based approaches.

In this work, a FIR filter is proposed for a high image rejection without using the complex I/Q frequency conversion in the mm-Wave heterodyne systems. Basic functionality of FIR filter is to shape Sinc profile creating frequency nulls periodically in the frequency response. The frequency nulls built-in in the FIR filter can be leveraged to filter out image signals as illustrated in Fig. 1-2. The FIR filters are widely used in digital, analog and low RF domain for various filtering purposes, but never attempted for image rejection purpose

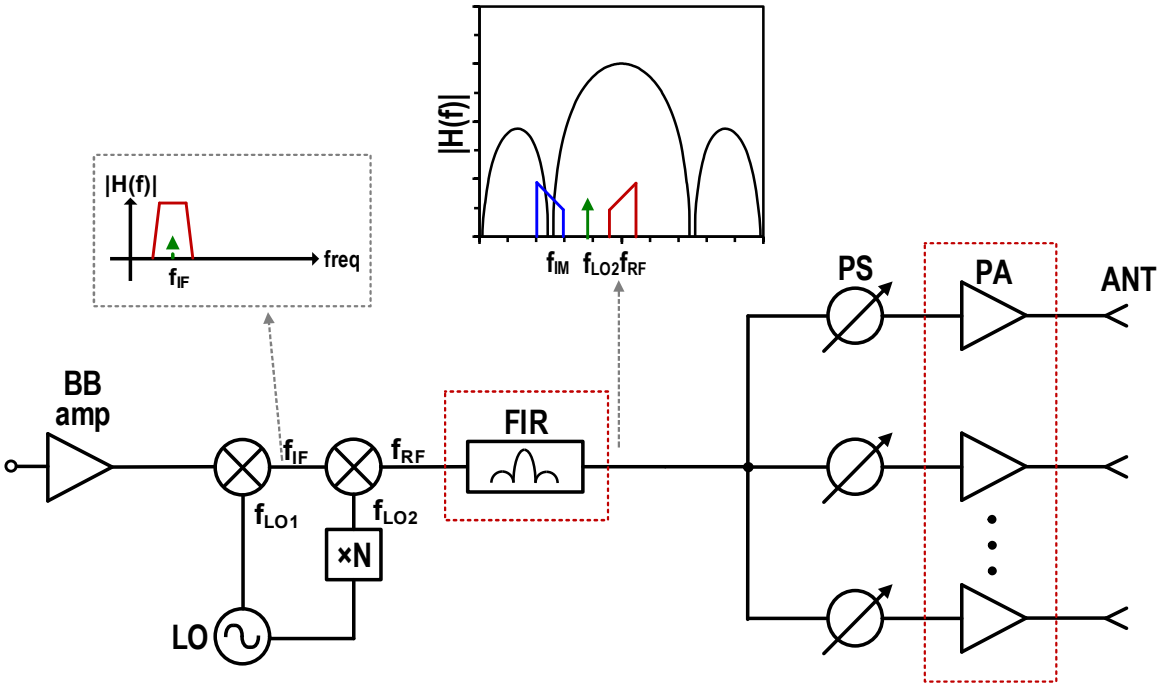


Fig. 1-3. A phased array transmitter.

at the mm-Wave regime (>30 GHz) [1-2∼4]. This work addresses design issues of the FIR filter at mm-Wave and provides details of design procedures.

Another critical issue in mm-Wave transmitters, especially in silicon-based transmitters, is to achieve high output power. As frequency increases, the layout parasitic of active (FETs) and passive devices (inductors and capacitors) become dominant, limiting the output power capability and quality factor (Q) of active and passive devices, respectively. One viable solution to increase output power could be combining output powers using passive power combiners. However, the power combiners at mm-Wave are still quite lossy, degrading the power efficiency at mm-Wave [1-5∼6]. The phased array based power combining in the space domain could be an alternative solution eliminating the power loss after power amplifiers and therefore improving the overall system power efficiency. The phased array based transmitters also take advantage of the spatial filtering inherited in the phased arrays for better signal selectivity in the space domain [1-7∼8]. In general, the output power requirement of an unit PA in the phased array based transmitters could be much relaxed, compared with single-input-single-output (SISO) based transmitters, allowing silicon-based

power amplifiers with several 10's mW output power in typical large-scale arrays (array number > 100's – 1000's). Even in this low-to-medium scale output power level, it is important to design unit PAs to be highly power efficient for the entire array systems to maintain a high power efficiency. In this work, various high-efficiency techniques such as impedance tuning with a reactive component at a cascoding stage in conventional stacked power amplifiers or load-pull based inter-stage matching technique, rather than conventional conjugate matching, have been applied to W-band CMOS and SiGe BiCMOS amplifiers to improve power efficiency with 5-10 dBm output power level, suitable for a large phased array applications, as detailed in the following chapters.

1.2 Dissertation Organization

The main objective of this dissertation is to study and design high efficiency power amplifiers and FIR filters for a high power efficiency with a high frequency selectivity in the mm-Wave heterodyne phased array transceivers. As mentioned, it is critical to suppress losses in the transistor interconnects and passive components to maintain a high power efficiency in the power amplifiers. While there are several types of high efficiency techniques such as class-F, class-F^{-1}, or class-E, those high efficiency techniques require multi-resonance complex load networks to resonate out selective harmonic components at the load. The complexity of the load networks eventually leads to a high loss from the passive components comprising the load networks, typically resulting in worse power efficiency than the conventional class-A or class-AB techniques at W-band and higher frequencies (> 90 GHz). It is important to minimize the load complexity to minimize loss from the passive components. Therefore, this thesis is particularly focused on the efficiency improvement study of class-A or class-AB topologies such as cascode stacked amplifiers, common-source or common-emitter amplifiers. In the FIR filter study, transmission-line based delay lines are utilized to realize a 4-tap FIR filter at D-band for a proof of concept demonstration. The thesis is comprised as following.

In Chapter 2, a high efficiency technique in the 2-stage stacked power amplifiers with low-to-medium output power are studied. The first stage is a driving amplifier based on a common-source configuration to provide a high gain and the second stage of the PA adopts a stacked topology which is also known as a series power combining. The PA design procedure, implementation details in 32 nm SOI CMOS technology, and measurement results of the power amplifiers are provided to verify the power efficiency improvement.

In Chapter 3, a high-efficiency technique based on inter-stage load-pull matching is investigated using a 2-stage common-emitter (CE) power amplifier in 0.13-μm SiGe BiCMOS technology. The output stage of the PA is comprised of a LC matching network having a minimum complexity. A series matching capacitor also functioning as a DC block and a shunt matching inductor also working as a DC feed constitute the LC load network. To maximize power efficiency, the inter-stage matching network of the 2-stage PA is

realized with load-pull simulation, rather than relying on conventional conjugate matching approach. The whole design procedure measurement results of small and large signal characteristics are provided.

In Chapter 4, a 0.13-μm SiGe BiCMOS 4-tap FIR filter is designed at D-band. A novel impedance-scaled delay-line based FIR filter architecture is proposed to overcome shortcomings of conventional FIR filers. An in-depth performance comparison study between the conventional FIR topology and the proposed FIR filter is conducted in this chapter. In the silicon realization, the FIR filter is particularly optimized for receiver applications mainly because of lack of high power measurement equipment at D-band. The main small-signal characteristics, S-parameters and NF, and image rejection test outcomes are discussed in this chapter.

Reference

[1-1] Behzad Razavi, RF microelectronics, Prentice Hall, 2011.

[1-2] P. K. Meher, "New Approach to Look-Up-Table Design and Memory-Based Realization of FIR Digital Filter," in IEEE Trans-actions on Circuits and Systems I: Regular Papers, vol. 57, no. 3, pp. 592-603, March 2010.

[1-3] S. Park, D. Shin, K. Koh and S. Raman, "A low-power 3.25GS/s 4th-order programmable analog FIR filter using split-CDAC coef-ficient multipliers for wideband analog signal processing," 2018 IEEE International Solid - State Circuits Conference - (ISSCC), San Francisco, CA, 2018, pp. 62-64.

[1-4] R. Bhat, J. Zhou and H. Krishnaswamy, "Wideband Mixed-Domain Multi-Tap Finite-Impulse Response Filtering of Out-of-Band Noise Floor in Watt-Class Digital Transmitters," in IEEE Journal of Solid-State Circuits, vol. 52, no. 12, pp. 3405-3420, Dec. 2017.

[1-5] J. Oh, B. Ku and S. Hong, "A 77-GHz CMOS Power Amplifier With a Parallel Power Combiner Based on Transmission-Line Transformer," in IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 7, pp. 2662-2669, July 2013.

[1-6] P. Haldi, D. Chowdhury, P. Reynaert, G. Liu and A. M. Niknejad, "A 5.8 GHz 1 V Linear Power Amplifier Using a Novel On-Chip Transformer Power Combiner in Standard 90 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 43, no. 5, pp. 1054-1063, May 2008.

[1-7] A. Hajimiri, H. Hashemi, A. Natarajan, Xiang Guan and A. Komijani, "Integrated Phased Array Systems in Silicon," in Proceedings of the IEEE, vol. 93, no. 9, pp. 1637-1655, Sept. 2005.

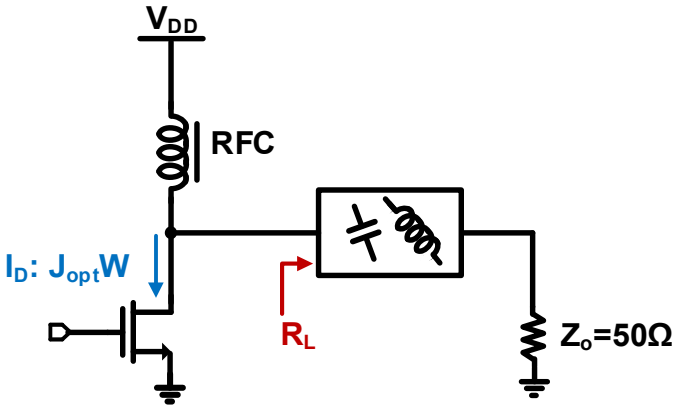
[1-8] Kwang-Jin Koh, J. W. May and G. M. Rebeiz, "A Q-band (40–45 GHz) 16-element phased-array transmitter in 0.18-μm SiGe BiCMOS technology," 2008 IEEE Radio Frequency Integrated Circuits Symposium, Atlanta, GA, 2008, pp. 225-228.

Chapter 2.

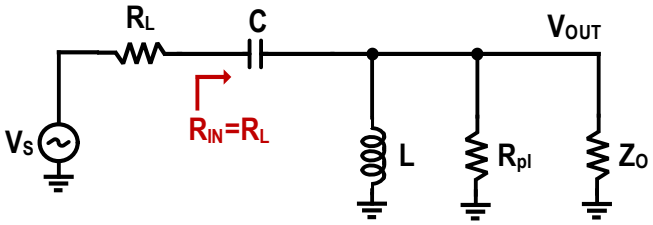
W-band Stacked Power Amplifier in 32nm SOI CMOS Technology

2.1 Introduction

With the advancement of CMOS technology, the demand for low-cost CMOS based millimeter-wave integrated circuits has increased for many wireless applications, such as high-speed wireless communications, fiber-grade millimeter-wave backhauls, high-resolution radar and imaging sensors. In order to facilitate the cost-effective CMOS mm-Wave wireless systems at W-band and higher frequencies (> 90 GHz), a large-scale phased array typically comprised of several hundreds to several thousands of array elements for transmitter and receiver (T/R) modules, are highly demanded for the same cell coverage as contemporary cellular communications [2-1]. Among many performance specifications of the T/R modules, power efficiency is one of crucial metrics for the large silicon arrays to be practical, as they could draw huge DC power due to the massive integration level. Power amplifiers (PAs) are one of major power hungry circuit blocks in T/R modules. The efficiency of PAs can largely affect the overall power efficiency of T/R modules. However, achieving a high efficiency with a high output power in silicon PAs is challenging, mostly due to the low breakdown voltage and high loss of passive and active components in scaled CMOS processes. At high frequencies, the loss from passive components increases because of their relatively low Q-factor. In Fig. 2-1(a), the output load impedance, Z_O (typically, 50 Ω), is transformed to the optimum impedance (R_{opt}) to attain maximum output power. During this transform, the efficiency is defined as,



(a)

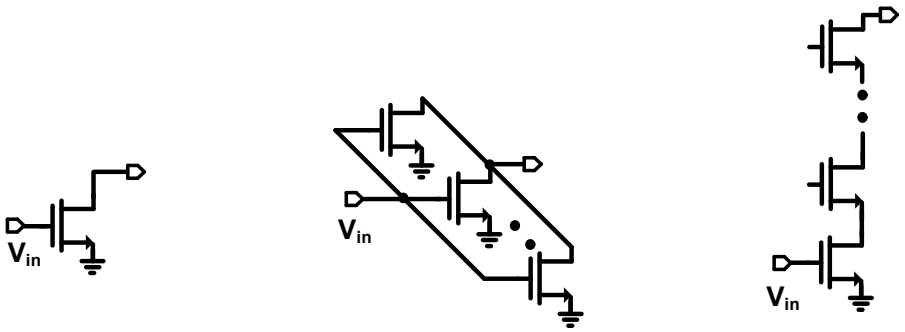


(b)

Fig. 2-1. (a) Output matching network and (b) example of LC output matching network.

$$\eta = \frac{P_L}{P_{IN}} = \frac{4R_L}{|V_S|^2} \frac{|V_{out}|^2}{2\left(R_{pl} \,\|\, Z_O\right)} = \frac{Q_{ind}}{Q_{ind} + Q_T} \tag{2.1}$$

, where, $Q_{ind}= R_{pl}/(\omega L)$ and $Q_T=\sqrt{(\frac{Z_O}{R_L} - 1)}$. In general, the supply voltage is limited by the low break-down voltage and hence, the current of the transistor is required to increase for the required P_{out}, causing low optimum load impedance ($R_{opt}=V_{DD}/I_{D)}$ which could be much smaller than Z_O. Therefore, the efficiency of passive matching network, η is reduced with given Q_{ind}. In order to increase the optimum impedance, a stacked PA topology is introduced and is compared with parallel FETs. First, unit common-source (CS) is presented in Fig. 2-2. It is assumed that unit FET is set the drain current of I_D and supply voltage of V_{DD}. Then, input capacitance of C_{gs} is loaded. The maximum output power is set to $(1/2)I_DV_{DD}$ with $R_{opt}=V_{DD}/I_D$. N parallel FET is comprised of N unit FET connected to parallel with same



	Unit FET	N parallel	N stacked
Peak drain current	$2I_D$	$N(2I_D)$	$2I_D$
Peak drain voltage($V_{DS,sat}$=0)	$2V_{DD}$	$2V_{DD}$	$N(2V_{DD})$
Input capacitance	C_{gs}	NC_{gs}	C_{gs}
output impedance	R_{opt}	$\frac{R_{opt}}{N}$	NR_{opt}
Output power	$\frac{1}{2} I_D V_{DD}$	$N(\frac{1}{2} I_D V_{DD})$	$N(\frac{1}{2} I_D V_{DD})$

Fig. 2-2. Comparison of FET topologies, unit FET, parallel FET and stacked FET for the output power and the optimum output impedance.

bias condition. In this case, the drain current is increased by N resulting in NI_D. The supply voltage is kept constant to V_{DD} and the input capacitance is increased by N times. The optimum output impedance defined as V_{DD}/NI_D is decreased by N times compared that of unit FET. Therefore, the effective R_{opt} will be reduced further, causing severe loss-factor in the passive matching network. In contrast, for the N stacked topology, the supply voltage is increased by N to NV_{DD} and the drain current is still constant with that of the unit FET [2-2]. Therefore, the output power is increased and N times higher than that of the output power, resulting in NI_DV_{DD}. Finally, the optimum output impedance is increased by N times to NR_{opt}. Therefore, the transformation Q-factor, Q_T is increased around Z_O to boost the efficiency, η.

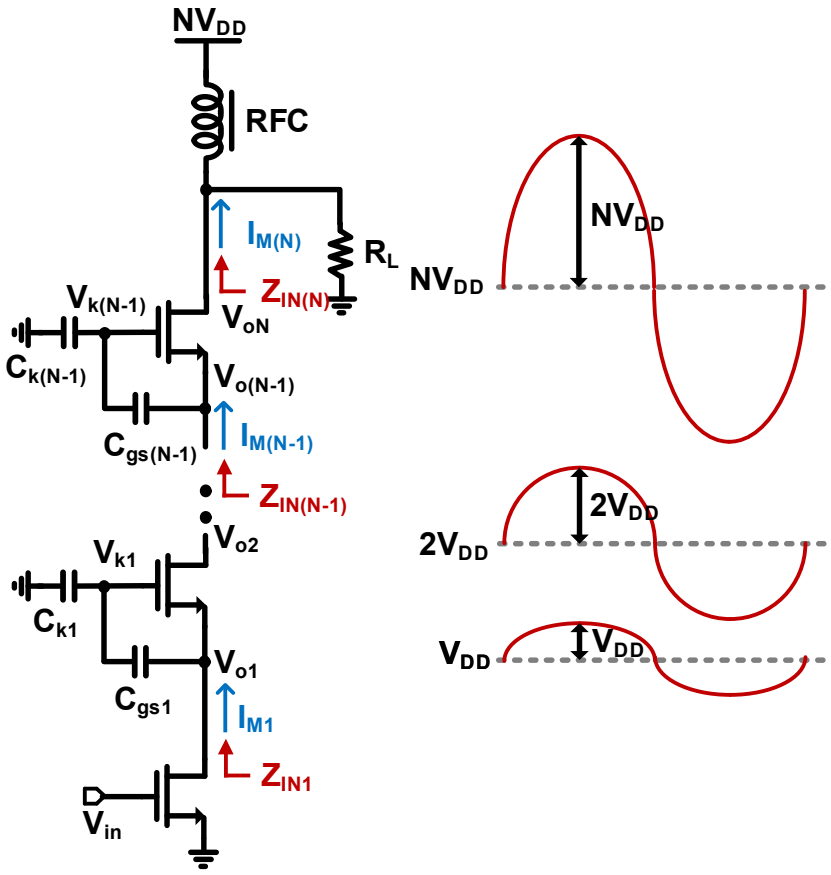


Fig. 2-3. A general topology for N stacked power amplifiers.

2.2 Stacked Power Amplifiers in Millimeter-wave

Fig. 2-3 shows the N stacked topology. The external capacitor is utilized at each gate node to secure appropriate impedance for maximum output power. The supply voltage is set to NV_{DD} and each drain voltage is set for same drain-source voltage distribution. For example, the drain voltage at the bottom stage is set to V_{DD} and that of 2^{nd} stage from the bottom FET is $2V_{DD}$. When the input signal is applied, it satisfies uniform drain-source voltage distribution. In order to do that, the impedance seen to each drain node should be scaled down from the top FET to the bottom FET. First, the impedance seen at the drain of bottom FET, Z_{IN1} is expressed as

$$Z_{IN1} = \left(1 + \frac{C_{gs1}}{C_{k1}}\right) \frac{1}{g_{m1} + sC_{gs1}} \approx \left(1 + \frac{C_{gs1}}{C_{k1}}\right) \frac{1}{g_{m1}} . \quad (2.2)$$

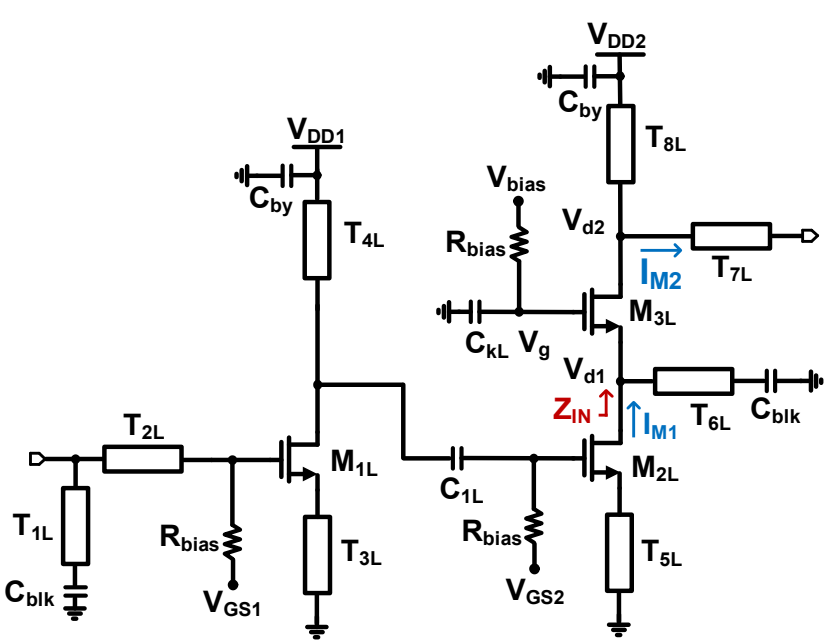
Like this way, the impedance seen at the drain of N-1's stage, $Z_{IN(N-1)}$ is

$$Z_{IN(N-1)} = \left(1 + \frac{C_{gs(N-1)}}{C_{k(N-1)}}\right) \frac{1}{g_{m(N-1)} + sC_{gs(N-1)}} \approx \left(1 + \frac{C_{gs(N-1)}}{C_{k(N-1)}}\right) \frac{1}{g_{m(N-1)}} . \quad (2.3)$$

The current generated from the bottom FET, I_{M1} is shared to each drain node, under the condition of that g_m is greater than sC_{gs}. Then, Z_{IN1} is set to the optimum impedance for the maximum output power, $(1/2)I_DV_{DD}$ by adjusting g_m and C_k. At the voltage node of V_{O2}, the voltage swing should be $2V_{DD}$ so that Z_{IN2} is twice of Z_{IN1}. It is determined by C_{k2}, the external gate capacitance. Like this way, the voltage swing at the drain of top FET is NV_{DD} for uniform drain-source voltage distribution. Finally, the output power is increased by N times compared to that of output power of unit FET without the stress of the break-down voltage.

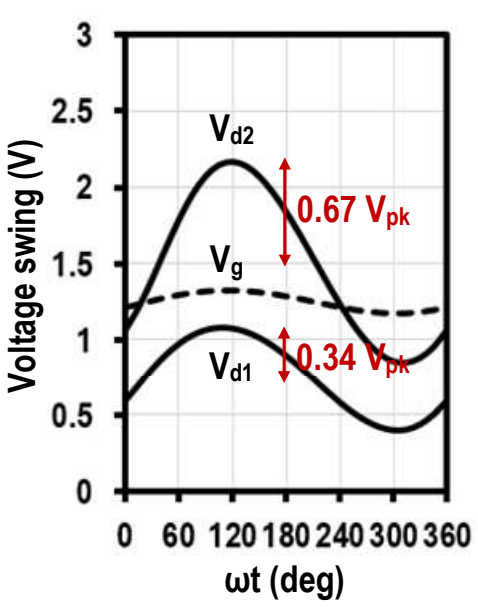
2.3 Circuits Design

Fig. 2-4(a) shows the schematic of a two-stage power amplifier with low output power. All transistors are modeled with Cadence RC extraction up to the second metal layer (M2) and electromagnetic (EM) modeling up to the top metal layer (LB). With this type of design procedure, the simulated f_{max} of a NFET with width of 80 (0.5×160) μm drops from 605 to 223 GHz. In the in/output matching networks, DC blocking (or series matching) capacitors are not used because there are no DC current paths through the waveguide RF probes. This enables to avoid the relatively high loss from capacitors with low Q-factor. All capacitors, including DC block capacitors (C_{blk}) and bypass capacitors (C_{by}), are designed by custom-made vertical natural (VN) capacitors, which are not provided in the PDK. Transmission lines (T-lines) are realized as ground coplanar waveguide (GCPW) lines using the LB layer for the signal line and side ground plane. The E1 layer (4th layer from the top layer) is used for the ground plane under the signal path to shield the effect of dummy metals under the E1



M_{1L}	0.5x40 μm
M_{2L}	0.5x60 μm
M_{3L}	0.5x60 μm
T_{1L}	5/10/110 μm
T_{2L}	5/10/115 μm
T_{3L}	5/10/40 μm
T_{4L}	5/10/75 μm
T_{5L}	5/10/10 μm
T_{6L}	5/10/200 μm
T_{7L}	5/10/420 μm
T_{8L}	5/10/240 μm
C_{kL}	160 fF
C_{1L}	100 fF
C_{blk}	400 fF
C_{by}	400 fF

(a)



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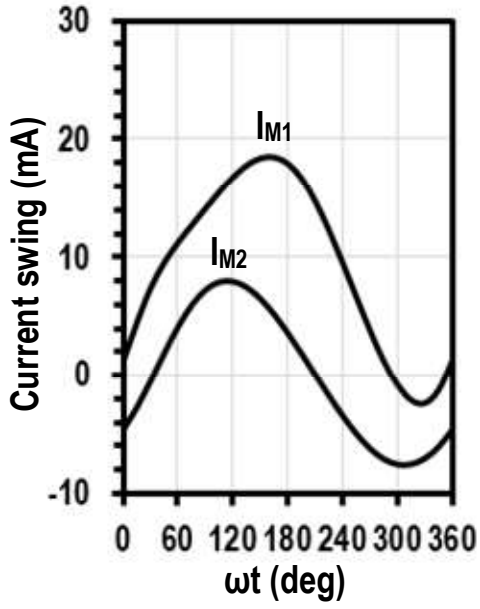
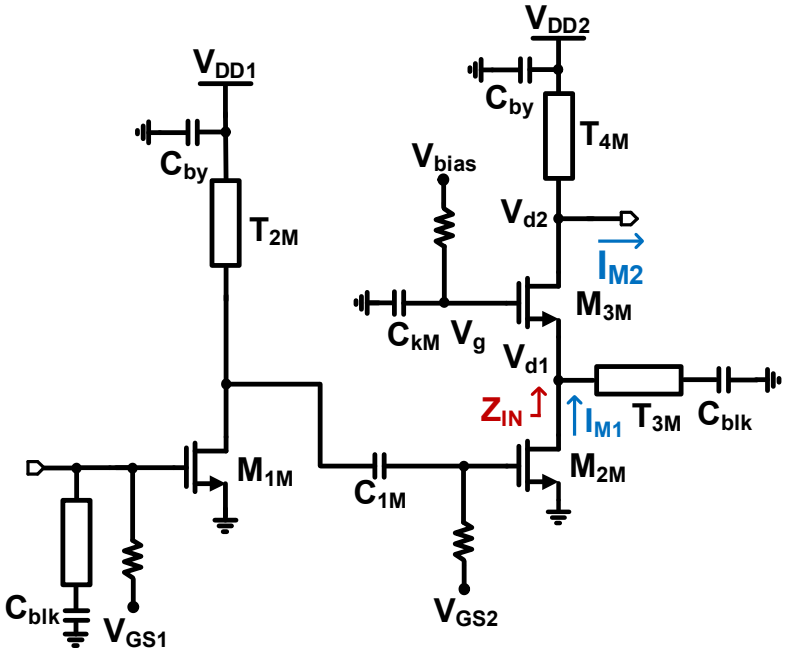


(c)

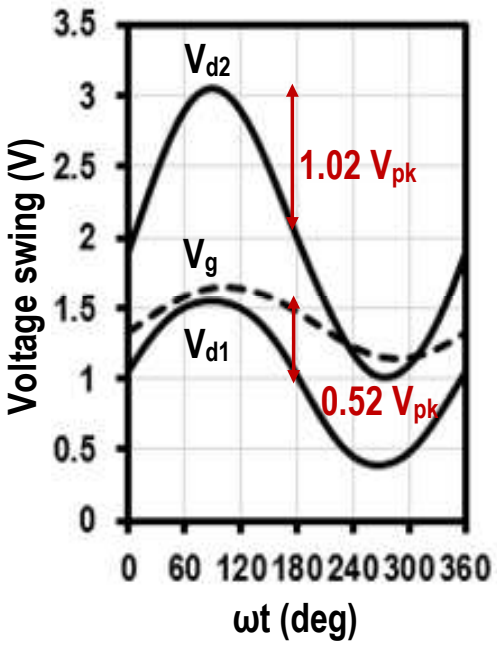
Fig. 2-4. (a) schematic of 2-stage power amplifier for low Pout (b) voltage wave-form in the stacked topology and (c) current waveform in the stacked topology .

layer, which are not considered in EM modeling. For a low output power, the size of the

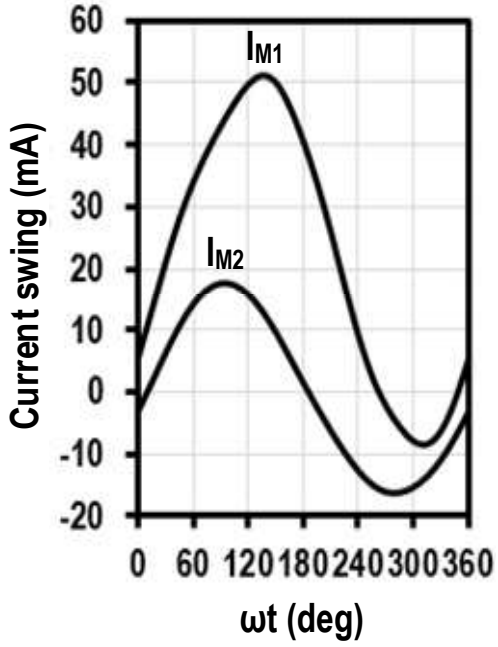


M_{1M}	0.5x160 μm
M_{2M}	0.5x200 μm
M_{3M}	0.5x200 μm
T_{1M}	10/10/80 μm
T_{2M}	10/10/70 μm
T_{3M}	10/10/160 μm
T_{4M}	10/10/115 μm
C_{kM}	160 fF
C_{1M}	110 fF
C_{blk}	400 fF
C_{by}	400 fF

(a)



(b)



(c)

Fig. 2-5. (a) The schematic of 2-stage power amplifier for medium Pout (b) voltage wave-form in the stacked topology and (c) current waveform in the stacked topology.

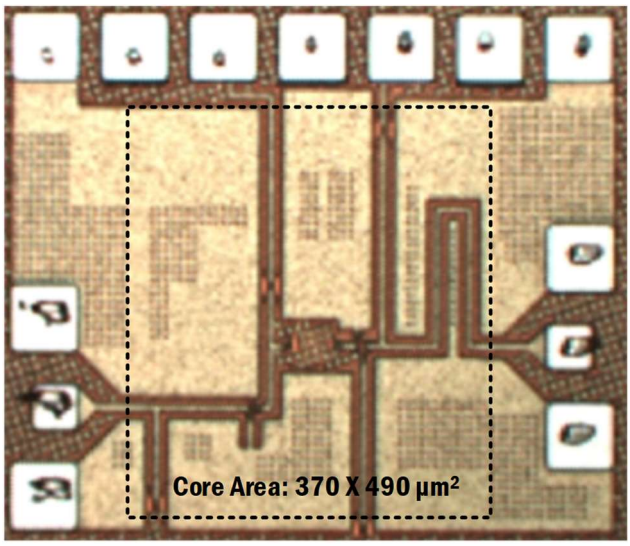
FET in the output stage is chosen to be 30 (0.5×60) μm, which exhibits a saturated power

around 5 dBm. Source degeneration T-lines (T_{3L} and T_{5L}) are used for both stages to secure stability as well as to realize wide-band matching network. At the drain node of M_{3L}, a shunt inductor (T_{8L}) is used to make Z_{opt} to a real value of R_{opt} and a quarter-wave transformer (T_{7L}) is used to convert 50 Ω to R_{opt}, which is 84 Ω. At the inter-stage node, a shunt T-line (T_{6L}) is utilized to modulate Z_{IN} (=28+j16= 32ej30° Ω), instead of Ropt/2 (42 Ω) for in-phase and uniform drain-source voltage swings through several iterations. This compensates the mismatch between the current to the output load resistance ($7.8e^{j240°}$ mA) and the current to the source of M_{3L} ($10e^{j215°}$ mA). In Fig. 2-4(b), the simulated voltage swings at each drain nodes are shown at the 1-dB compression point which achieve the relation of Vd2 ≅ 2Vd1.

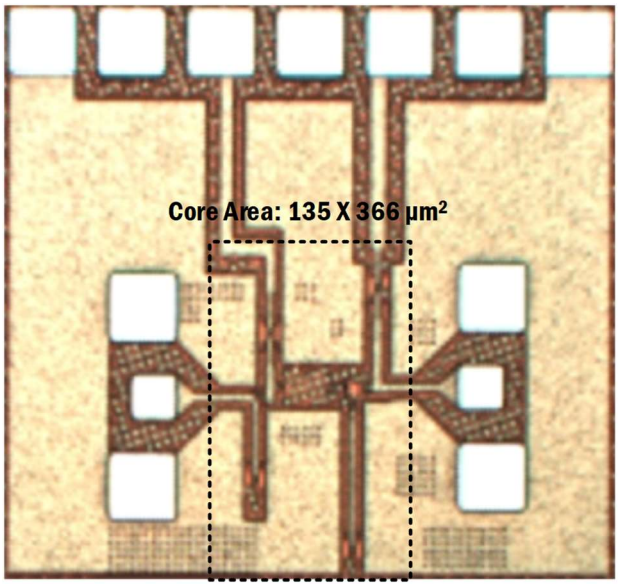
For a PA with medium output power in Fig. 2-5(a), the FET size of the output stage is chosen to have a saturated output power more than 10 dBm. As the width of the FET is increased, the MAG of the FET is decreased due to the parasitic components. Consequently, the achievable PAE also drops with the low power gain, which is below than 10 dB. The width of the FET for the output stage is set to 100 (0.5×200) μm, where the unit finger width is also optimized for maximum gain. In this case, Z_{opt} at the output is set to 50 Ω by tuning the effective output capacitance with a shunt inductance (T_{4M}). This allows to avoid additional lossy matching networks to transform 50 Ω to the lower impedance. At the inter-stage, the impedance looking into the source of M_{3M} is modulated to 12+j13 Ω instead of a half of R_{opt} (25 Ω). Fig. 2-5(b) shows the simulated drain voltage swings at the 1dB compression point. It also shows the compensation of current mismatch through the inter-stage matching. At the voltage swing, it achieves the uniform drain-source voltage distribution.

2.4 Measurement Results

The power amplifiers are implemented in IBM 32 nm SOI CMOS technology. The chip photographs of the PAs are shown in Fig. 2-6. The chip sizes of the low and medium output power PAs are 0.58 × 0.58 mm2 (0.37 × 0.49 mm2 w/o pads) and 0.68 × 0.63 mm2 (0.17 × 0.35 mm2 w/o pads), respectively.



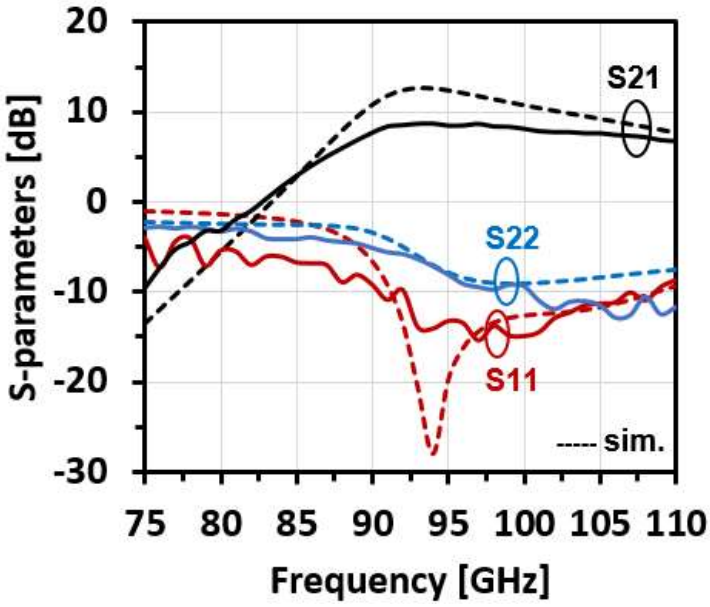
(a)



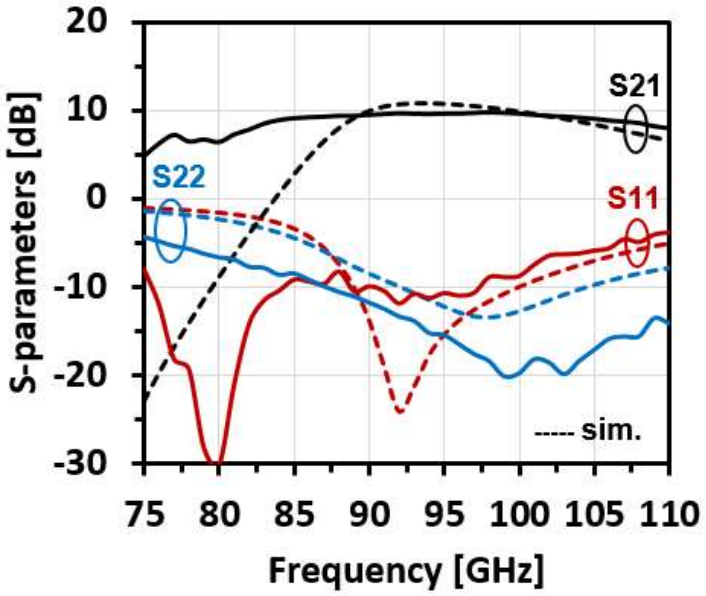
(b)

Fig. 2-6. Chip photos of (a) a power amplifier of low output power and (b) a power amplifier of medium output power.

On wafer S-parameter measurement is performed with SOLT calibration. Cascade ACP110 ground-signal-ground (GSG) probes and an Agilent network analyzer (N5247A) combined with frequency extenders (VDI VNAX) at W-band are used for small signal



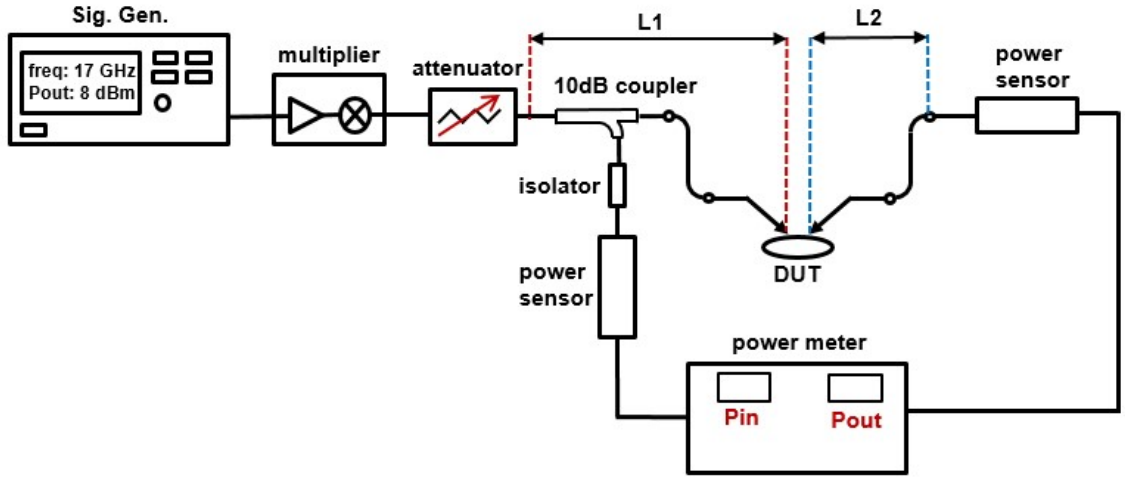
(a)



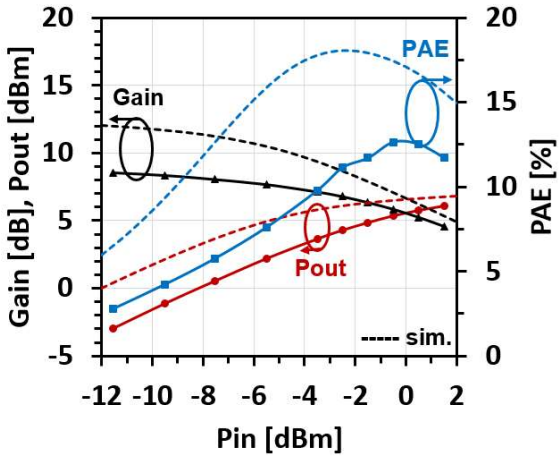
(b)

Fig. 2-7. Measured and simulated S-parameters of (a) a power amplifier of low output power and (b) a power amplifier of medium output power.

measurement. Fig. 2-7 presents the simulated and measured S-parameters of the PAs. The low output power PA shows a peak gain of 8.8 dB at 94 GHz and a 3-dB bandwidth of more than 23 (87 - >110) GHz under the bias point of V_{DD1}/V_{DD2}=1.0/1.5 V and I_{D1}/I_{D2}=2/9 mA.



(a)



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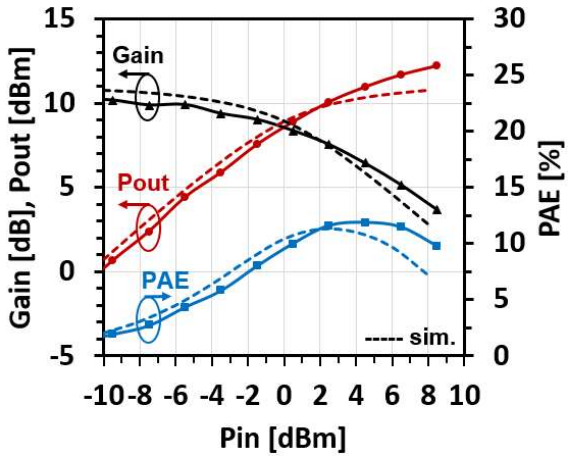


(c)

Fig. 2-8. (a) set-up for large signal measurement and gain, Pout and PAE of (b) a power amplifier of low output power and (c) a power amplifier of medium output power.

The input return loss is >10 dB at 90-109 GHz, but the output return loss is low due to the power matching. The medium output power PA shows a peak gain of 9.7 dB at 94 GHz and a 3-dB bandwidth of more than 34 (76 - >110) GHz under the bias point of V_{DD1}/V_{DD2}=1.0/2.0 V and I_{D1}/I_{D2}=16/19 mA. The input return loss is shifted down, but > 10 dB at 76-4 GHz. Fig. 2-8(a) shows the power measurement setup. The W-band waves are generated using a signal generator (Agilent E8257D) followed by a frequency multiplier (OML S10M_AG). The input loss (L1) and output loss (L2) including a 10 dB coupler, WR-

TABLE 2-I. PERFORMANCE COMPARISON OF W-BAND POWER AMPLIFIERS

Reference	Tech.	Freq. (GHz)	Gain (dB)	Psat (dBm)	Peak PAE (%)	Supply (V)	Area (mm^2)
[2-3]	45 nm CMOS	89	8	17	9	4.2	0.06
[2-4]	45 nm CMOS	89	10.2	15.8	11	2.8	0.05
[2-5]	45 nm CMOS	91	12.4	19.2	14	3.4	0.23
[2-6]	45 nm CMOS	80	11	12.4	14.2	2.0	0.32*
This work	32 nm CMOS	94	8.8	6.1	12.6	1.5	0.18
This work	32 nm CMOS	94	9.7	12.2	11.8	2.0	0.06

*: area including pads

10 waveguides, and GSG probes are calibrated out to correspond input and output pads as a reference plane. Fig. 2-8(b), (c) present the large signal measurement results. The low output power PA shows measured OP1dB of 2.2 dBm and Psat of 6.1 dBm with peak PAE of 12.6 % at 94 GHz. The medium output power PA shows measured OP1dB of 7.5 dBm and Psat of 12.2 dBm with peak PAE of 11.8 % at 94 GHz. Table 2-I presents a comparison of this work with the state-of-the-art W-band power amplifiers implemented in CMOS technology.

2.5 Summary

This chapter presents two W-band two-stage stacked power amplifiers based on a 32nm SOI CMOS technology. The stacked-FET topologies are adopted for maximum output power. Y_{IN} is modulated to maintain in-phase and equal drain-source voltage swings at each drain nodes. The small-scale output power PA shows more than 6 dBm of output power with a peak PAE of 12.6 % and medium-scale output power PA achieves more than 12 dBm of output power with a peak PAE of 11.8 % at 94 GHz, both suitable for a large phased array application

Reference

[2-1] B. Sadhu et al., "A 28-GHz 32-Element TRX Phased-Array IC With Concurrent Dual-Polarized Operation and Orthogonal Phase and Gain Control for 5G Communications," in IEEE Journal of Solid-State Circuits, vol. 52, no. 12, pp. 3373-3391, Dec. 2017

[2-2] S. Pornpromlikit, J. Jeong, C. D. Presti, A. Scuderi and P. M. Asbeck, "A Watt-Level Stacked-FET Linear Power Amplifier in Silicon-on-Insulator CMOS," in IEEE Transactions on Microwave Theory and Techniques, vol. 58, no. 1, pp. 57-64, Jan. 2010.

[2-3] J. Jayamon, A. Agah, B. Hanafi, H. Dabag, J. Buckwalter and P. Asbeck, "A W-band stacked FET power amplifier with 17 dBm Psat in 45-nm SOI CMOS," Silicon Monolithic Integrated Circuits in RF Systems (SiRF), 2013 IEEE 13th Topical Meeting on, Austin, TX, 2013, pp. 156-158.

[2-4] A. Agah, J. Jayamon, P. Asbeck, J. Buckwalter and L. Larson, "A 11% PAE, 15.8-dBm two-stage 90-GHz stacked-FET power amplifier in 45-nm SOI CMOS," Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International, Seattle, WA, 2013, pp. 1-3.

[2-5] A. Agah, J. A. Jayamon, P. M. Asbeck, L. E. Larson and J. F. Buckwalter, "Multi-Drive Stacked-FET Power Amplifiers at 90 GHz in 45 nm SOI CMOS," in IEEE Journal of Solid-State Circuits, vol. 49, no. 5, pp. 1148-1157, May 2014.

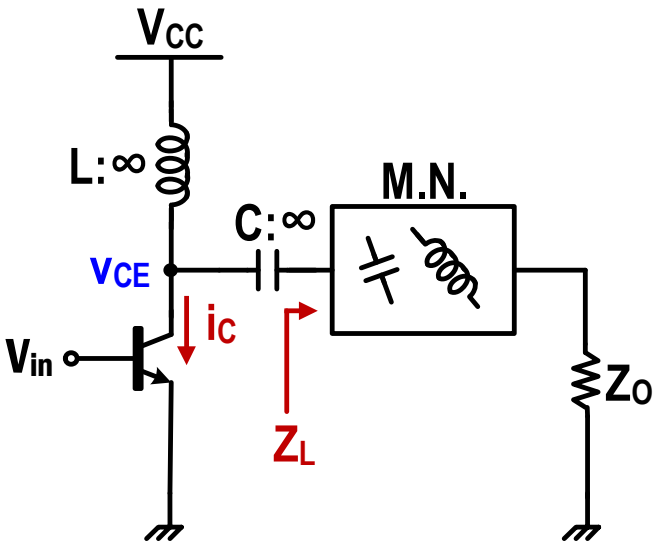
[2-6] J. Kim, H. Dabag, P. Asbeck and J. F. Buckwalter, " Q -Band and W -Band Power Amplifiers in 45-nm CMOS SOI," in IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 6, pp. 1870-1877, June 2012.

Chapter 3.

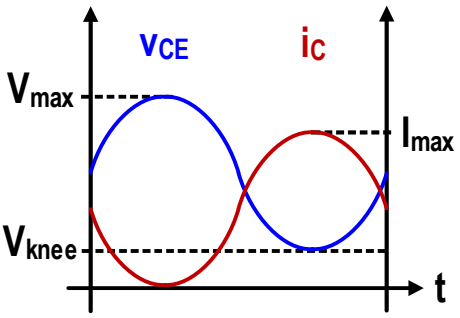
W-band 2-stage Common-Emitter Class AB Power Amplifier in 0.13μm BiCMOS Technology

3.1 Introduction

As described in Chapter 1, phased array systems are comprised of multi-channel elements and SNR is increased with the number of elements due to the coherent signals and non-coherent noise combining in the receiver (Rx). In Transmitters (Tx), the required output power of each element is relieved due to the equivalent isotropically radiated power (EIRP) increasement of antenna array. However, the efficiency of each power amplifier is critical and determines the total Tx efficiency because it is the most power-hungry block. There are several techniques to increase the efficiency, such as adjusting the conduction angle of the collector current or harmonic load tuning. Class A operation shows a conduction angle of 2π in the collector current, i_C, as shown in Fig. 3-1(b). As the power dissipated in the transistor is defined as $\frac{1}{T}\int_0^T V_{CE}(t)i_C(t)dt$, the maximum efficiency of class A is only 50(1-$\frac{V_{knee}}{V_{cc}}$) %, where V_{cc} is the supply voltage and V_{knee} is the knee voltage that indicates the required minimum V_{CE} for a forward active operation. In class AB operation as shown in Fig. 3-1(c), the conduction angle of the collector current is between π and 2π. In this mode, there are some time duration where the power dissipation is zero resulting in a maximum collector efficiency of 78.5(1-$\frac{V_{knee}}{V_{cc}}$) %, which occurs during the conduction angle of π.



(a)



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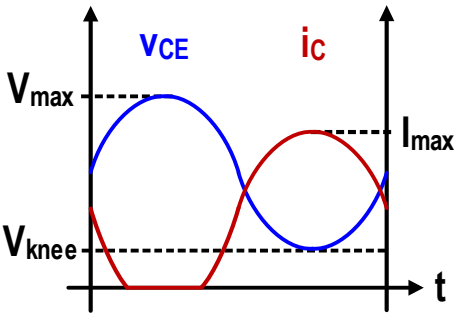
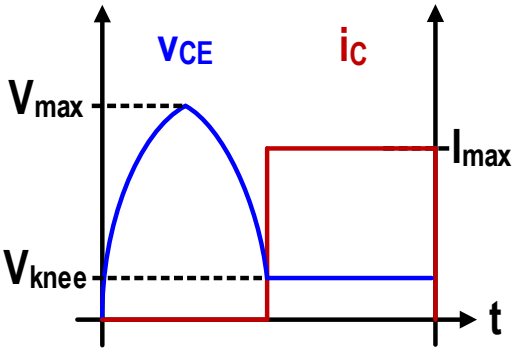


(c)

Fig. 3-1. (a) The model of power amplifier with ideal DC feed and block, the collector voltage and current in time domain of (b) class A and (c) class AB.

Therefore, Class AB mode is widely used for efficient power amplifiers. Class B and C



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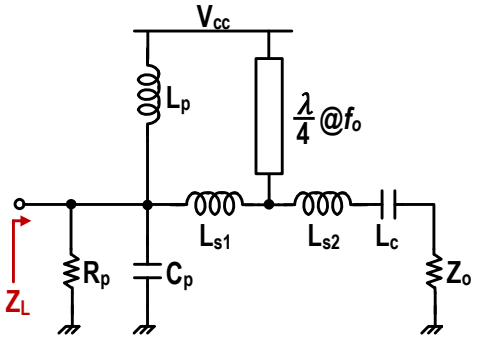

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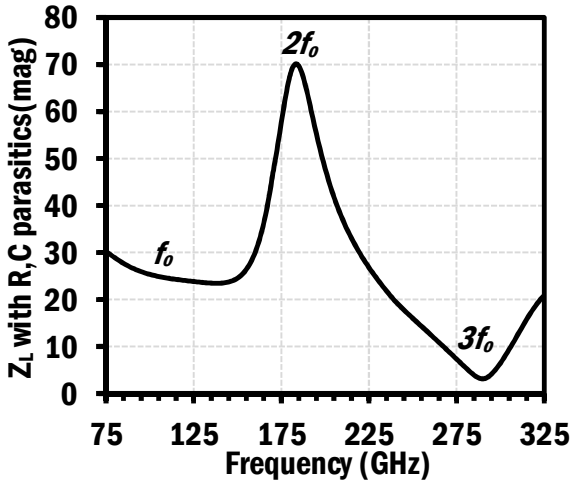


(c)

Fig. 3-2. (a) The collector voltage and current waveform in time domain of class F^{-1} and (b) the output matching of class F^{-1} and (c) the magnitude of impedance at f_o, $2f_o$ and $3f_o$.

operation could be better choice in terms of the efficiency, but the linear gain is too low and

the linearity becomes worse, which is not optimium for linear power amplifiers.

Class F and F^{-1} are also well-known PA architectures for high efficiency. The waveforms of the collector voltage and current of class F^{-1} are shown in Fig. 3-2(a). Harmonic impedance tuning is necessary for rectangular-shaped collector current and half-sine pulse of the collector voltage. Practically, only the 2nd and 3rd harmonic impedance tunings are considered. In class F^{-1} mode, the impedance of the 2nd harmonic should be high and the impedance of the 3rd harmonic should be low for a half-sine wave collector voltage. However, it is challenging to achieve high impedance at the 2nd harmonic due to the loss of passive components and relatively low resistance seen at the collector of HBTs at high frequency range (>100 GHz). The load network including the parasitic resistor, R_p, and capacitor, C_p, of HBTs is shown in Fig. 3-2(b). The values of R_p and C_p are extracted as 100 Ω and 20 fF from a HBT with L_e of 9 μm. The magnitude of the load at the 2nd harmonic is 70 Ω and the 3rd harmonic is 4 Ω. When is the impedances are applied to the load of class F^{-1} mode, the efficiency improvement is negligible due to the low impedance of the 2nd harmonic. Therefore, class AB mode is adopted for the power amplifier developed in this work to obtain high efficiency.

3.2 Design of Class AB Power Amplifier at W-band

When the required output power is high, over 20-30 dBm, the supply voltage, V_{CC}, is determined by the breakdown voltage for reliability issues. Thus, the size of the transistor is chosen to satisfy the required current for the output power. However, when the required output power is relatively low, the supply voltage and other parameters can be relaxed leading to a more flexible design. Fig. 3-3(a) shows a schematic to determine the supply voltage, *Vcc* and the emitter length, L_e. The source impedance is transformed to the conjugate of the input impedance of the transistor, Z_{in}, and ideal DC feed and blocking capacitor are used so that the load doesn't affect the performance of PA. If V_{CC} is lowered, L_e must be increased to obtain the required Pout. In this condition, the optimum load impedance to maximize the PAE can be shown with load-pull simulation. Fig. 3-3(b) shows the P_{out} and PAE as a function of the current density, J_C (mA/μm), for different V_{CC} and L_e values. The

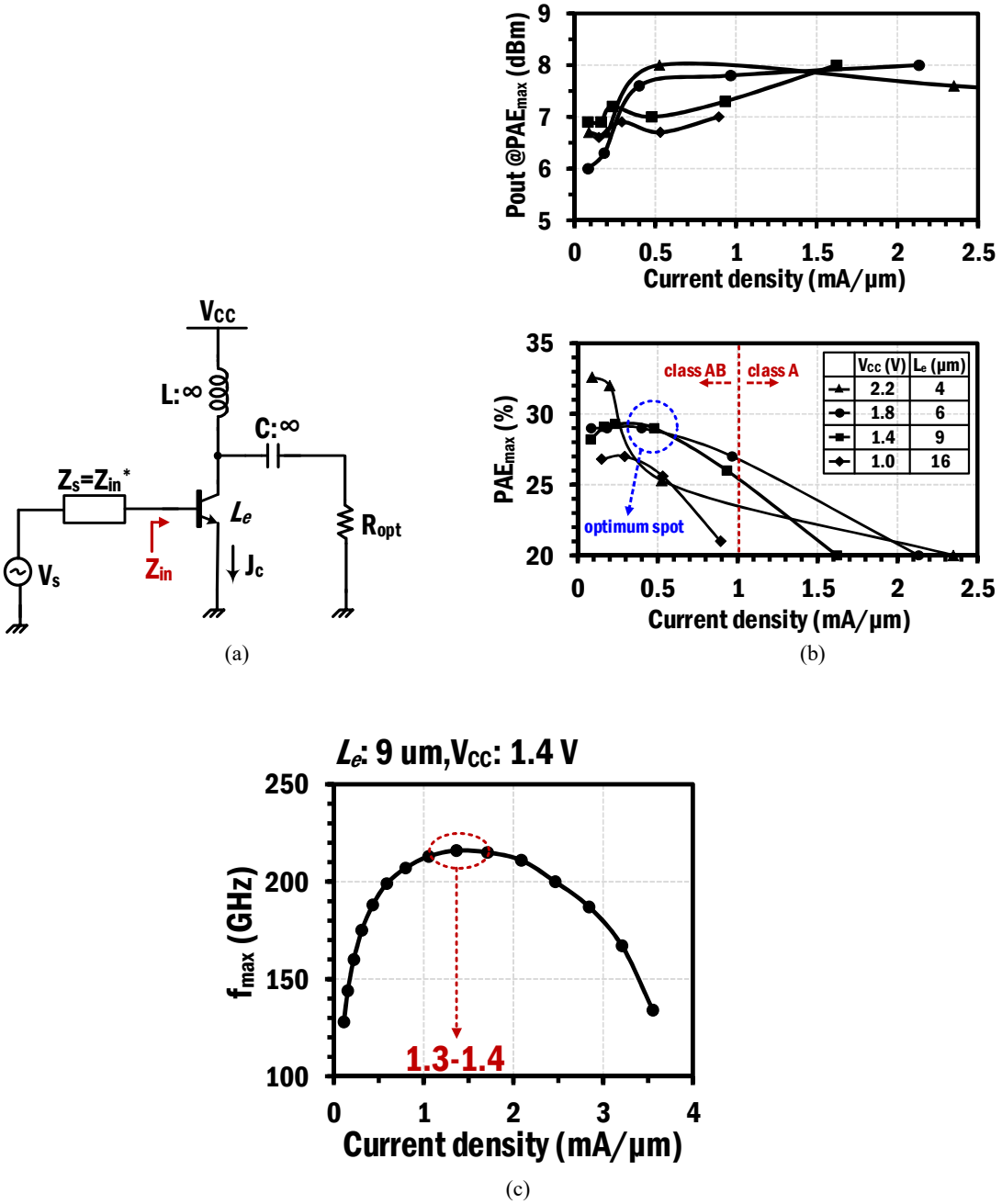
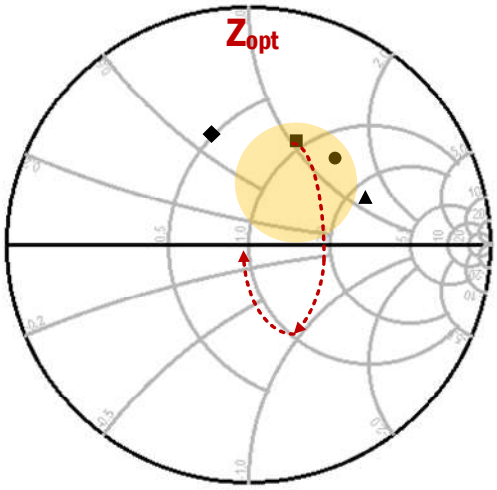


Fig. 3-3. (a) The schematic of power amplifier for determining R_{OPT} and (b) peak PAE swept by current density with several cases of V_{CC} and L_e and (c) f_{max} swept by current density.

PAE in the region for J_C > 1 mA/μm decreases with the increasing current density in class A mode. The PAE in the region for J_C < 0.3 mA/μm decreases with decreasing current density. In addition, this operation region is unsuitable for linear PAs due to low linear gain



(a)

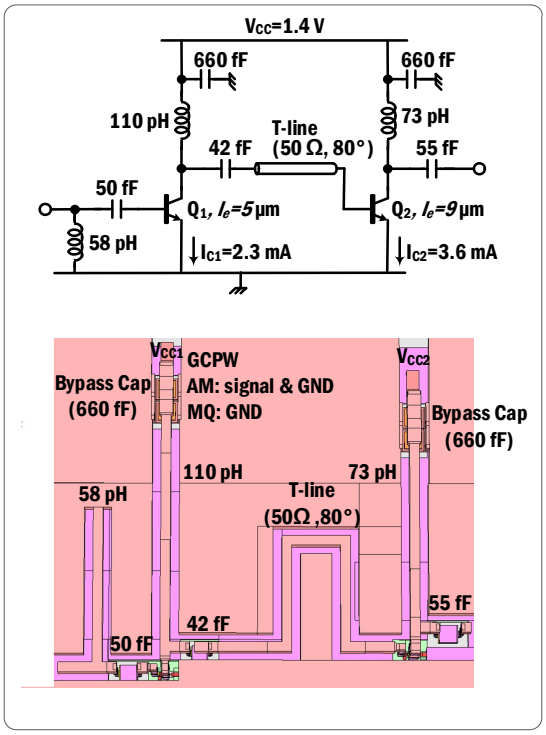
	V_{CC} (V)	L_e (μm)	J_c (mA/μm)	Z_{opt} (Ω)	C_{out} (F)	L_{out} (H)
▲	2.2	4	0.44	121+j49	25f	135p
●	1.8	6	0.40	80+j84	22f	115p
■	1.4	9	0.38	38+j40	45f	75p
◆	1.0	16	0.34	17+j24	150f	55p

(b)

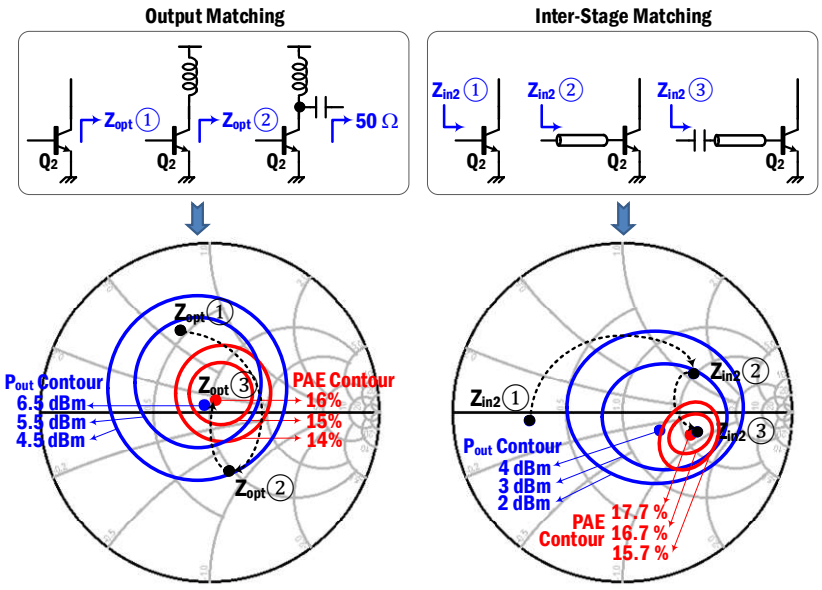
Fig. 3-4. (a) the output matching trajectory, (b) several cases of V_{CC} and L_e for optimum impedance.

of 1-2 dB. Therefore, the optimum of J_C can be chosen in the region of 0.3-0.5 mA/μm. Fig. 3-3(c) shows the f_{max} as a function of J_C. The peak f_{max} of 230 GHz can be achieved with J_C of 1.3-1.4 mA/μm, but the current density of 0.3-0.5 mA/μm is chosen for maximum PAE at the expense of maximum linear gain.

The loss of passive matching networks is a critical factor that should be considered for high PAE of PAs. One popular technique to decrease the loss would be to use a simplistic design. Therefore, shunt inductors for DC feeding and series capacitors for DC blocking as well as other matching components with finite values are utilized in this work. However, other matching networks, such as series inductors and shunt capacitors have advantages in filtering out the harmonics due to its low-pass characteristics. Shunt inductors and series capacitors with moderate values (C_{out}: 45 fF, L_{out}: 75 pH) can transform Z_o of 50 Ω to Z_{opt} in the shaded area (yellow circle). Any Z_{opt} outside the shaded area requires large or small passive components to increase the loss or accuracy in EM modeling.



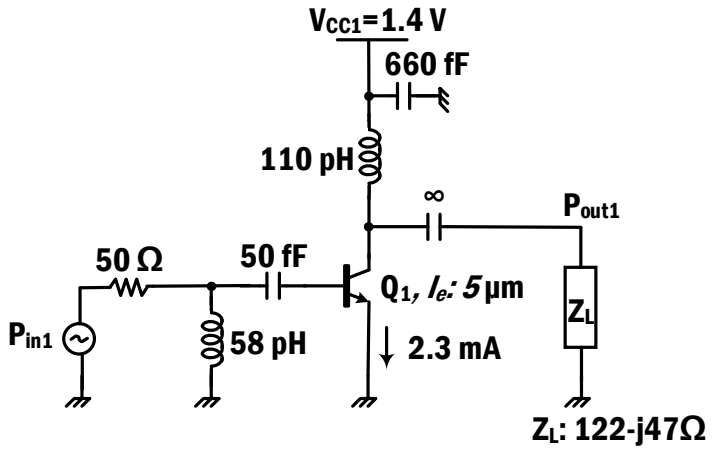
(a)



(b)

Fig. 3-5. (a) The schematic of 2-stage PA and 3D EM photo and (b) matching trajectory to the optimum impedance for peak PAE.

Fig. 3-5 (a) shows a schematic of 2-stage common-emitter PA operating in class AB mode. To obtain the maximum PAE, the output and inter-stage are matched for peak PAE.



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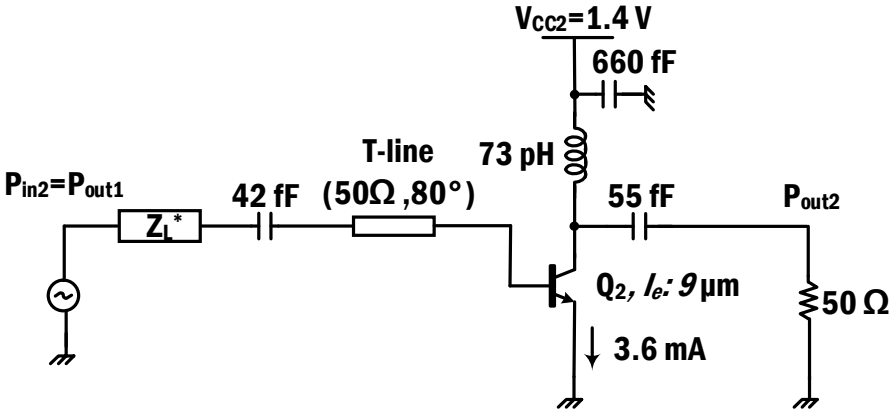


(b)

@peak PAE point

	1st stage	2nd stage	cascade
P_{in} (dBm)	0 (1.0mW)	4 (2.5mW)	0 (1.0mW)
P_{out} (dBm)	4 (2.5mW)	6.3 (4.3mW)	6.3 (4.3mW)
Gain (dB)	4.0	2.3	6.3
P_{DC} (mW)	8.5	12.2	20.7
PAE (%)	17.7	14.5	15.9

(c)

Fig. 3-6. (a) 1st stage and (b) 2nd stage of power amplifier and (c) the performance of individual stage .

The procedure of matching is shown in Fig. 3-5(b). When the output matching circuit is configured as in Fig. 3-5 (b), the optimum load seen at the collector of Q_2, Z_{opt}①, is

inductive due to the parasitic capacitance at the collector node of Q_2. Therefore, using a DC feed inductor (73 pH, Q=14) transforms the optimum load to be located on the 50-Ω unit circle as Z_{opt}②. Finally, a series DC block capacitor (55 fF, Q=17) moves the optimum impedance to 50 Ω. Note that the output matching circuit is in its simplest form by leveraging DC feed inductor and DC blocking capacitor, resulting in a minimum loss from the passive network. In simulations, the P_{out} at a peak PAE point is 6.3 dBm with ~2.3 dB of saturated power gain in the output stage. As can be seen in Fig. 3-5 (b), the PAE at the 50-Ω matching point is better than 14% in the output stage – in a standalone output stage simulation the peak PAE is 14.5%. The driver is designed to produce ~4 dBm P_{out} with a highest possible PAE, ~17.7% PAE. For this, the driver output is also matched for a maximum PAE, not for a maximum power transfer. In Fig. 3-5(b), first the impedance at the base of Q_2, Z_{in2}① (14.7-*j*1.3 Ω), is moved to Z_{in2}② (99+*j*60 Ω) by a series T-line. Then, a series capacitor (42 fF) is cascaded to locate the impedance Z_{in2}② to Z_{in2}③ (132-*j*16 Ω) close to the optimum impedance for a maximum PAE of Q_1. Finally, a series capacitor (50 fF, Q=12) followed by a shunt inductor (58 pH, Q=15) matches the Q_1 input to 50 Ω.

The cascaded performance of the 2-stage PA is analyzed in Fig. 3-6. In Fig. 3-6 (a), the first stage is loaded by the input impedance of the second stage, Z_L=122-j47 Ω. The source impedance of the second stage is set to the conjugate of Z_L in Fig. 3-6 (b) to deliver the output power of the first stage (P_{out1}) to the second stage without any loss. Based on this separation, the performance of each stage will be identical to that of cascade PA. The simulation performances of each stage and cascaded PA at the peak PAE power at 94 GHz are summarized in Fig. 3-6 (c). In the cascade PA, the overall PAE is determined by

$$PAE = PAE_2 \times \left(1 + \frac{1}{G_{P1}}\frac{G_{P1}-1}{G_{P2}-1}\right)\left(1 + \frac{PAE_2}{PAE_1}\frac{1}{G_{P1}}\frac{G_{P1}-1}{G_{P2}-1}\right)^{-1} \quad (3.1)$$

, where $G_{P1,2}$ are the power gains and $PAE_{1,2}$ are the PAE of the first and the second stage, respectively. The simulated PAE_1 is 17.7% and PAE_2 is 14.5%, resulting in 15.9% PAE. This is well matched with ~16% of simulation PAE of the 2-stage class-AB PA.

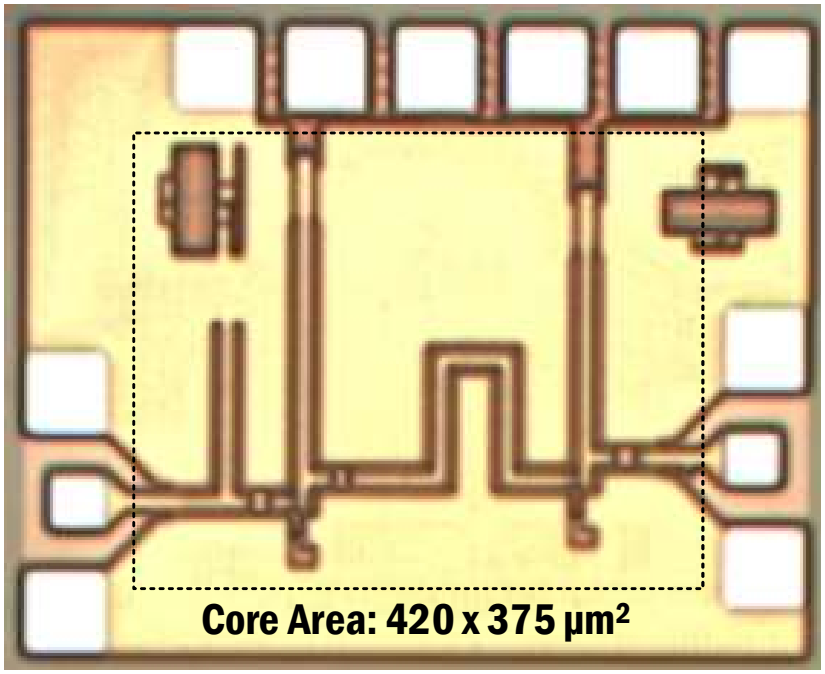
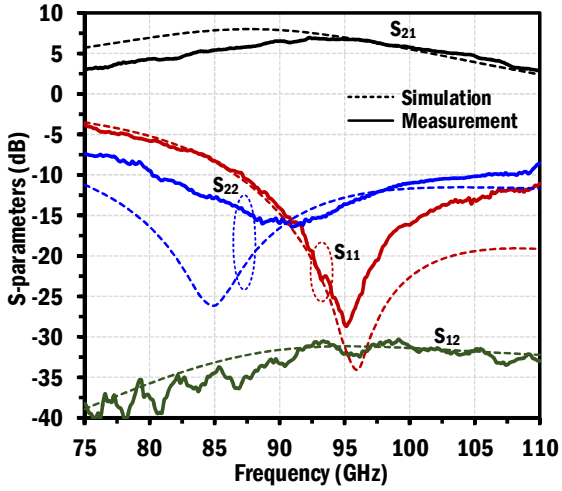


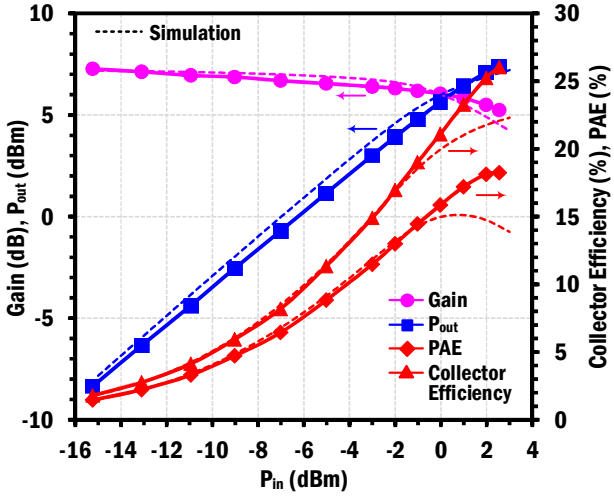
Fig. 3-7. The chip photograph of 2-stage power amplifier.

3.3 Measurement of S-parameters and Large Signal of Power Amplifier

The PA is fully EM modeled using SONNET and characterized with a standalone test chip shown in Fig. 3-7. The core area is 420 x 375 μm^2 excluding pads. The small and large-signal measurement results of the PA are shown in Fig. 3-8 (a) and (b). The small-signal power gain (S_{21}) is 6.8 dB at 94 GHz with a 3-dB bandwidth of 78.5 – 107.2 GHz. The measured impedance matching characteristics are S_{11} < -10 dB @ 87-110 GHz and S_{22} < -10 dB @ 80.3-108.3 GHz with the quiescent collector currents of I_{C1}/I_{C2} = 2.3/3.6 mA from 1.4 V supply voltage. In the large-signal characterizations, the measured P_{sat} is 7.4 dBm and OP_{-1dB} is 3.9 dBm at 94 GHz. In the test chip, it is observed that the gain compression behavior is a bit milder than simulation and the PA achieves peak PAE of 18.2 % at P_{sat}, a few % better than the simulation. At this power level, the DC collector currents (I_{C1}/I_{C2}) are increased up to 5.5/9.6 mA, resulting in total 21.1 mW of DC power consumption in the 2-stage PA. Finally, the PAE performance is compared with recent silicon PAs at similar frequency range in Fig. 3-9. It is apparent that the PAE decreases as decreasing output power



(a)



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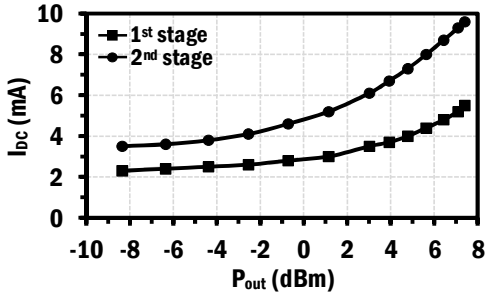


(c)

Fig. 3-8. (a) S-parameters of power amplifier and (b) large-signal measurement of power amplifier and (c) increase of DC current of 1st and 2nd stage as the increased output power.

due to a finite knee voltage effect, posing a challenge to achieve a high PAE at lower P_{out}.

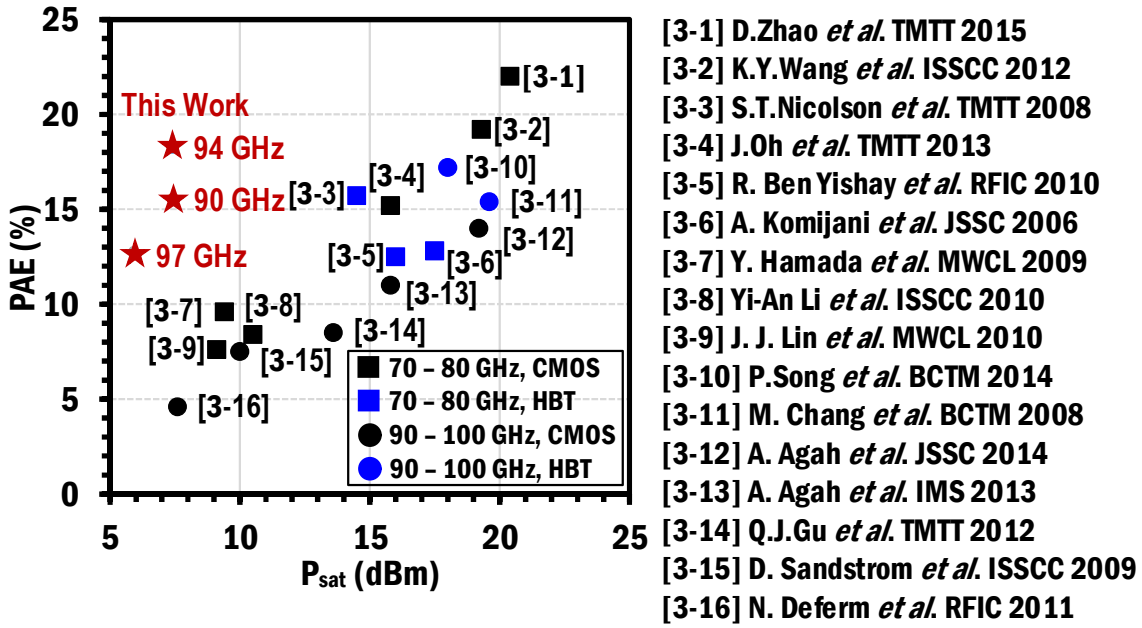


Fig. 3-9. Comparison of PAE with state-of-art power amplifiers at mm-wave (>70GHz).

By simplifying the output matching network by setting 50-Ω R_{opt} and optimal inter-stage matching for a high PAE, the presented PA achieves one of the best PAEs even with a low P_{sat}.

3.4 Summary

This chapter presents a W-band two-stage common-emitter power amplifier based on a 0.13μm BiCMOS technology. The bias and transistor size of the power amplifier in class AB mode is carefully optimized to have an optimum current density for a maximum PAE. The complexity of the matching network comprised of series capacitor and shunt inductor is minimized for a minimum loss from the passive network. Furthermore, the output and inter-stage are matched for a peak PAE based on load-pull simulations. The presented PA shows 7.4 dBm of output power with a peak PAE of 18.2 %, suitable for W-band phased array applications

Reference

[3-1] D. Zhao and P. Reynaert, "An E-Band Power Amplifier With Broadband Parallel-Series Power Combiner in 40-nm CMOS," IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 2, pp. 683-690, Feb. 2015.

[3-2] K. Y. Wang, T. Y. Chang and C. K. Wang, "A 1V 19.3dBm 79GHz power amplifier in 65nm CMOS," 2012 IEEE International Solid-State Circuits Conference, San Francisco, CA, 2012, pp. 260-262.

[3-3] S. T. Nicolson, K. H. K. Yau, S. Pruvost, V. Danelon, P. Chevalier, P. Garcia, A. Chantre, B. Sautreuil, and S. P. Voinigescu, "A Low-Voltage SiGe BiCMOS 77-GHz Automotive Radar Chipset," IEEE Transactions on Microwave Theory and Techniques, vol. 56, no. 5, pp. 1092-1104, May 2008.

[3-4] J. Oh, B. Ku and S. Hong, "A 77-GHz CMOS Power Amplifier With a Parallel Power Combiner Based on Transmission-Line Transformer," IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 7, pp. 2662-2669, July 2013.

[3-5] R. Ben Yishay, R. Carmon, O. Katz and D. Elad, "A high gain wideband 77GHz SiGe power amplifier," 2010 IEEE Radio Frequency Integrated Circuits Symposium, Anaheim, CA, 2010, pp. 529-532.

[3-6] A. Komijani and A. Hajimiri, "A Wideband 77-GHz, 17.5-dBm Fully Integrated Power Amplifier in Silicon," IEEE Journal of Solid-State Circuits, vol. 41, no. 8, pp. 1749-1756, Aug. 2006.

[3-7] Y. Hamada, M. Tanomura, M. Ito and K. Maruhashi, "A High Gain 77 GHz Power Amplifier Operating at 0.7 V Based on 90 nm CMOS Technology," IEEE Microwave and Wireless Components Letters, vol. 19, no. 5, pp. 329-331, May 2009.

[3-8] Y. A. Li, M. H. Hung, S. J. Huang and J. Lee, "A fully integrated 77GHz FMCW radar system in 65nm CMOS," 2010 IEEE International Solid-State Circuits Conference - (ISSCC), San Francisco, CA, 2010, pp. 216-217.

[3-9] J. J. Lin, K. H. To, D. Hammock, B. Knappenberger, M. Majerus and W. M. Huang, "Power Amplifier for 77-GHz Automotive Radar in 90-nm LP CMOS Technology," IEEE Microwave and Wireless Components Letters, vol. 20, no. 5, pp. 292-294, May 2010.

[3-10] P. Song, A. Ç. Ulusoy, R. L. Schmid, S. N. Zeinolabedinzadeh and J. D. Cressler, "W-band SiGe power amplifiers," 2014 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), Coronado, CA, 2014, pp. 151-154.

[3-11] M. Chang and G. M. Rebeiz, "A wideband high-efficiency 79–97 GHz SiGe linear power amplifier with ≫ 90 mW output," 2008 IEEE Bipolar/BiCMOS Circuits and Technology Meeting, Monteray, CA, 2008, pp. 69-72.

[3-12] A. Agah, J. A. Jayamon, P. M. Asbeck, L. E. Larson and J. F. Buckwalter, "Multi-Drive Stacked-FET Power Amplifiers at 90 GHz in 45 nm SOI CMOS," IEEE Journal of Solid-State Circuits, vol. 49, no. 5, pp. 1148-1157, May 2014.

[3-13] A. Agah, J. Jayamon, P. Asbeck, J. Buckwalter and L. Larson, "A 11% PAE, 15.8-dBm two-stage 90-GHz stacked-FET power amplifier in 45-nm SOI CMOS," 2013 IEEE MTT-S International Microwave Symposium Digest (MTT), Seattle, WA, 2013, pp. 1-3.

[3-14] Q. J. Gu, Z. Xu and M. C. F. Chang, "Two-Way Current-Combining W-Band Power Amplifier in 65-nm CMOS," IEEE Transactions on Microwave Theory and Techniques, vol. 60, no. 5, pp. 1365-1374, May 2012.

[3-15] D. Sandstrom, M. Varonen, M. Karkkainen and K. Halonen, "W-band CMOS amplifiers achieving +10dBm saturated output oower and 7.5dB NF," 2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, San Francisco, CA, 2009, pp. 486-487,487a.

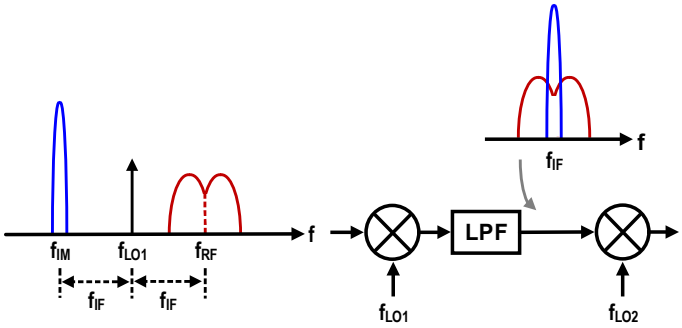
[3-16] N. Deferm, J. F. Osorio, A. de Graauw and P. Reynaert, "A 94GHz differential power amplifier in 45nm LP CMOS," 2011 IEEE Radio Frequency Integrated Circuits Symposium, Baltimore, MD, 2011, pp. 1-4.

Chapter 4.

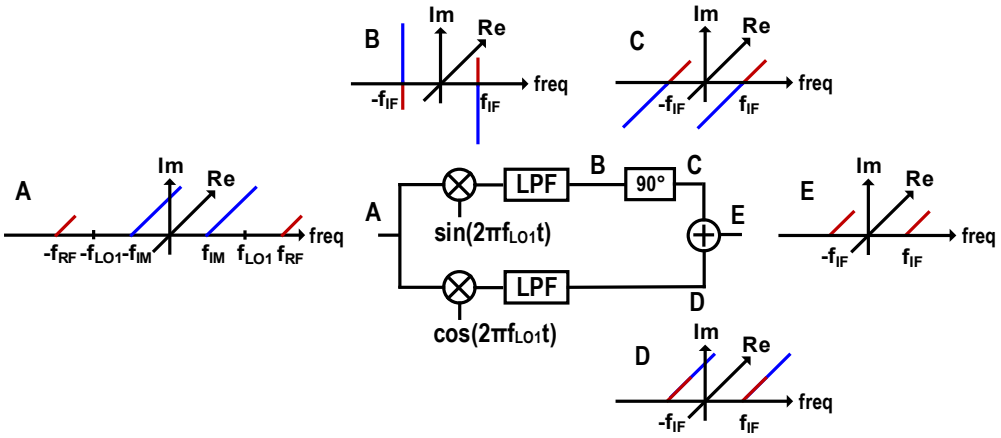
A FIR Filter for Image Rejection in Heterodyne Transceiver at D-band

4.1 Introduction

The heterodyne transceivers are distinguished by the utilization of intermediate frequency (IF), allowing better phase noise oscillators at much lower frequency for LO generation at mm-Wave, compared with homodyne transceivers. In heterodyne receivers, images should be rejected before being down-converted to IF, not to degrade SNR of the receivers. In this section, the image issue is discussed in detail. In Fig. 4-1(a), an RF signal is located around f_{RF} and LO frequency is set the lower side of f_{RF}. When the RF signal is down-converted to IF band by a RF mixer, any strong interferer at image frequency, f_{IM} located at the same frequency offset from f_{RF} to f_{LO} is also down-converted to IF frequency, degrading SNR at the output of the receiver. In general, the Hartley and Weaver image rejection architectures are popular. Both techniques utilize mixers driven by I/Q LO. In Hartley topology, a pair of I/Q LO and a 90° phase shifter are used. At I-channel, RF signal and image pass through I-channel mixer, which are multiplied by cosine LO and they don't experience phase shift during the down-conversion to IF. Therefore, they keep the same polarity at IF band. In contrast, RF signal and image undergo $\pm$90° phase shift after passing through Q-channel mixer driven by sine LO. Then their phase is rotated $\pm$90° by a phase shifter. Finally, after combining them together, only signal is survived and image is cancelled out. The Weaver topology presented in Fig. 4-1 (c) also needs I/Q path, but two pair of I/Q



(a)



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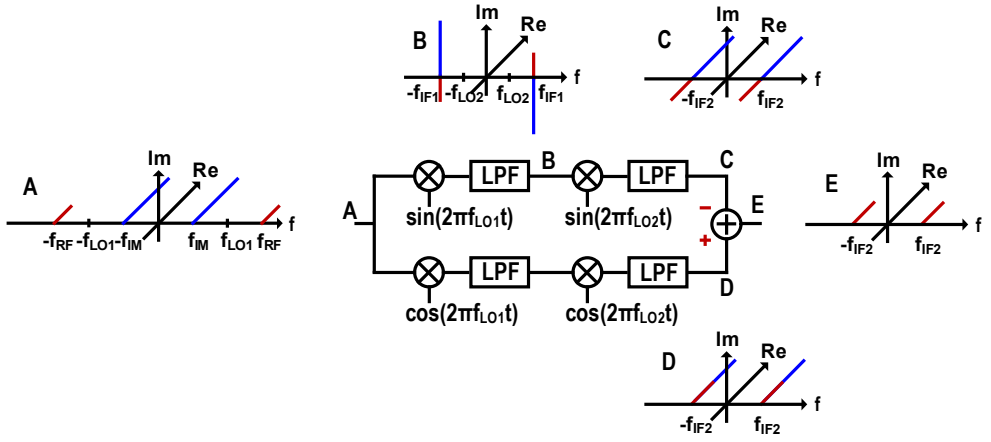
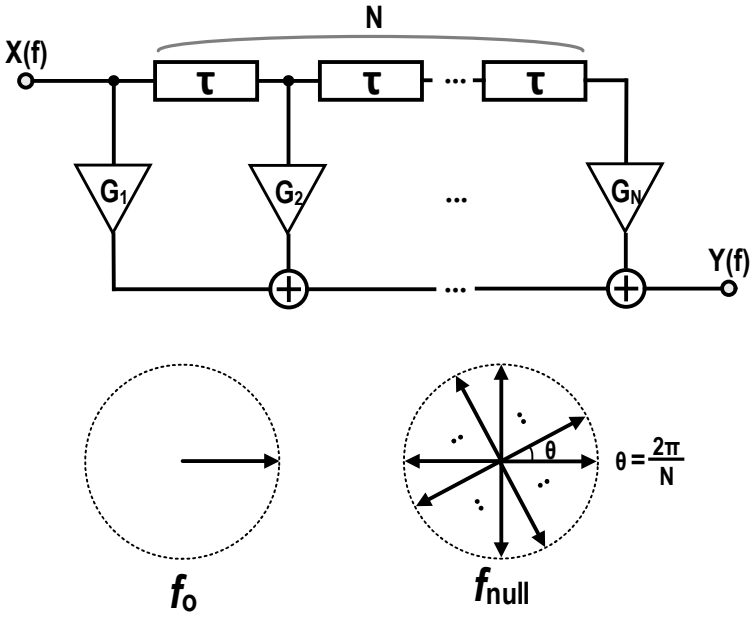


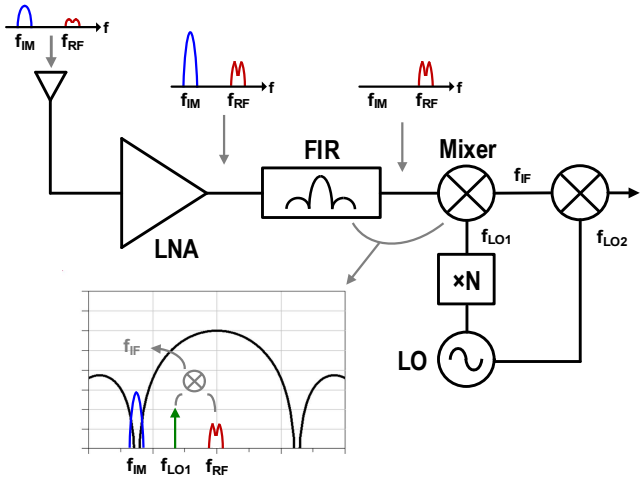
(c)

Fig. 4-1. (a) image issue in heterodyne receiver at IF frequency and image rejection architecture for (b) Hartley and (c) Weaver topology.

LO. At the end of I- channel, RF signal and image are located at the 2nd IF frequency with



(a)



(b)

Fig. 4-2. (a) the general type of FIR filter and (b) FIR filter for image rejection in heterodyne receiver.

same polarity, but they undergo ±90° phase shift. Thus, the signal maintains the opposite polarity of that of I-channel and the image keep the same polarity with that of I-channel. After the down-conversion to 2nd IF band, they are subtracted each other and only signal is survived at the output. The main drawback of these filters is to need I/Q mixers for image rejection, increasing DC power consumption and system complexity, which is not suitable

for low power application at mm-Wave. In this work, a novel filtering architecture based on FIR filters is introduced to overcome this issue. In general, a FIR filter is comprised of delay lines, adders and weighting elements (not always necessarily) as shown in Fig.4-2(a). The basic functionality of the FIR filters is to shape a Sinc-pulse type frequency magnitude response with a linear phase characteristic. At the center frequency, f_o, the signals at each tap are in-phase and amplified at the output of the filter. However, at null frequencies, the signals at each tap experience same magnitude but the phases of the signals are equally distributed over 2π radian, $\Delta\theta=2\pi/N$, as shown in Fig. 4-2(a). Therefore, they are cancelled out after adding at the output of the filter. The transfer function of the FIR will be expressed as

$$H(f) = G\frac{\sin(\pi fN\tau)}{\sin(\pi f\tau)}e^{-j(\pi f(N-1)\tau)}. \tag{4.1}$$

The null frequencies are generated periodically at every frequency interval of f_o times k/N, k=1,2, ⋯N-1, N+1⋯. Therefore, center frequency is located at f_o and the first low side null-frequency is $f_{null}=(N-1/N)f_o$. If mixer LO frequency is chosen to the middle of f_o and f_{null}, image can be rejected at RF heterodyne receiver as shown in Fig. 4-2(b).

4.2 An Analysis of FIR Filters at Millimeter-wave Range

4.2.1 Power Gain Analysis of FIR Filters

The N-tap FIR filter can be designed as shown in Fig. 4-3. The delay line is comprised of a series of transmission lines (T-lines) terminated with resistor of Z_O. This delay line is widely used in distributed amplifiers at RF domain [4-1~5]. The physical length of each T-line is λ at f_O with characteristic impedance of Z_O. The N's weighting amplifiers (W-amps) are connected to each tap for providing a power gain. The input impedance of W-amps, Z_{IN} should be high enough not to experience loading effect which is modeled as MZ_O (M: scaling factor). The output of W-amps and the input of adders are conjugate-matched to Z_O for maximum power gain. At the output stage, N-1's adders are necessary to combine the signals in-phase at f_O and nullifying signals at f_{null}. The source impedance of FIR filter is matched

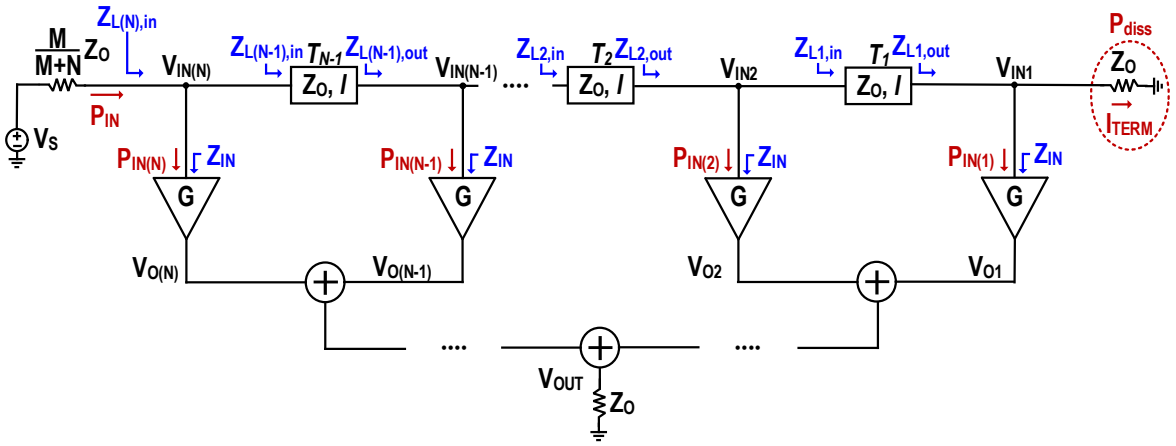
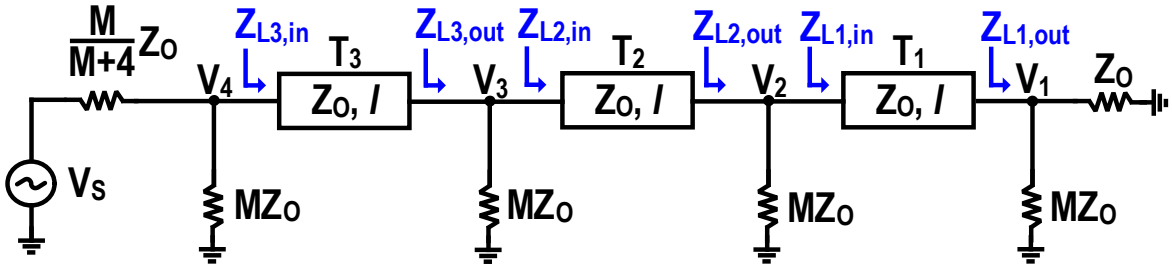


Fig. 4-3. N-tap FIR with a delay line of series of T-lines terminated Zo.

to $MZ_O/(M+N)$ which is the output impedance of preceding stage. Under this matched condition at f_O, the maximum available power from the source, P_{AVS}, will be $P_{IN} = P_{AVS} = (M+N)V_S^2/(4MZ_O)$. The voltages at each tap and the currents flowing to the input of each W-amp are $V_S/2$ and $V_S/(2\,MZ_O)$, respectively. The power delivered to the input of each W-amps is $P_{IN(1)} = P_{IN(2)} = \cdots = P_{IN(N)} = V_S^2/(4MZ_O)$, where voltage and current are RMS value. Then, the rest of DC power is dissipated by the terminated resistor, Z_O, resulting in $P_{diss} = V_S^2/(4Z_O)$. Each inserted power to the input of W-amps is multiplied by the maximum power gain of W-amp (G_{MAX}) due to the conjugated-match between the output of W-amp and the input of the adder. Then, the power from the output of each W-amp is combined by the N-1's adders considered as a power combiner, generating the output power of $P_{OUT} = V_S^2 G_{max} N/(4MZ_O)$. Finally, the transducer power gain of FIR filter, G_T is

$$G_T = \frac{P_{OUT}}{P_{AVS}} = \frac{N}{M+N} G_{MAX} \,. \tag{4.2}$$



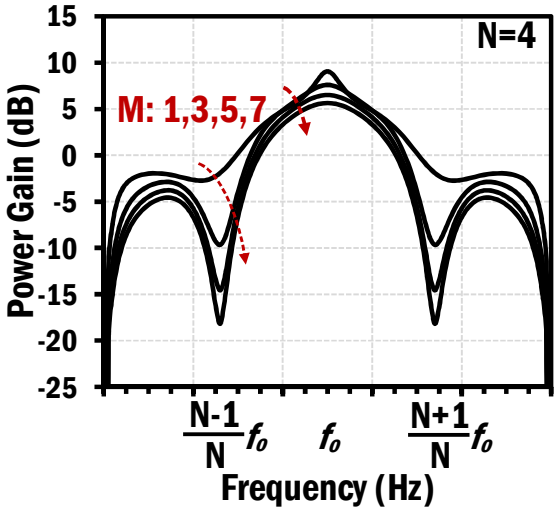
(a)

	f_o	f_{null}
$Z_{L1,in}$	$\frac{M}{M+1}Z_O$	$\frac{M+1}{M}Z_O$
$Z_{L1,out}$	$\frac{M}{M+1}Z_O$	$\frac{M}{M+1}Z_O$
$Z_{L2,in}$	$\frac{M}{M+2}Z_O$	$\frac{M^2+M+1}{M(M+1)}Z_O$
$Z_{L2,out}$	$\frac{M}{M+2}Z_O$	$\frac{M(M+1)}{M^2+M+1}Z_O$
$Z_{L3,in}$	$\frac{M}{M+3}Z_O$	$\frac{M^3+2M^2+M+1}{M(M^2+M+1)}Z_O$
$Z_{L3,out}$	$\frac{M}{M+3}Z_O$	$\frac{M(M^2+M+1)}{M^3+2M^2+M+1}Z_O$

(b)

Fig. 4-4. (a) 4-tap delay line terminated with Z_O considering the loading effect with MZ_O. (b) the in/output impedance of each T-lines at f_O and f_{null}.

As seen in this equation, given the number of taps, N, G_T is decreased when the scaling factor of M, (Z_{IN}=MZ_O) is increased. Therefore, the input impedance of W-amps, Z_{IN} can't be large to avoid the loading effect.



(a)

M	G_T (dB)	D_{null} (dB)	Att. (dB)
1	9	-2.3	11.3
3	7.6	-9.3	16.9
5	6.5	-13.4	19.9
7	5.6	-16.2	21.8

(b)

Fig. 4-5. (a) frequency response of FIR filter with various value of M and (b) table for the power gain at f_O, null-depth at f_{null} and attenuation between f_O and f_{null} with M=1,3,5 and 7.

There is a trade-off between the power gain at f_O and the null-depth at f_{null} dependent on the scaling factor of M. In order to understand this effect, a 4-taps delay line is configured by a series of T-lines terminated resistor, Z_O and a load of MZ_O, equivalent to the input impedance of W-amps are loaded at each tap as shown in Fig. 4-4(a). If the input and output impedance of each T-line is known, the voltage of each tap is calculated based on the power conservation law. Let's assume that T-line is lossless, then the input power entering to the T-line is conserved at the output of T-line. For instance, at f_o, the input and output impedance at each T-line are same that $Z_{L1,in} = Z_{L1,out} = MZ_O/(M+1)$, $\cdots, Z_{L3,in} = Z_{L3,out} = MZ_O/(M+3)$ as shown in Fig. 4-4(b). Therefore, voltages from each tap can be in-phase

signal at f_o as $|V_4|=|V_3|=|V_2|=|V_1|=|V_S|/2$. However, the input and output impedance of each T-line at f_{null} are not same but $Z_{L1,in} = (M+1)Z_O/M$, $Z_{L1,out} = MZ_O/(M+1)\cdots, Z_{L3,in} = (M^3+2M^2+M+1)Z_O/M(M^2+M+1)$, $Z_{L3,out} = M(M^2+M+1)\,Z_O/(M^3+2M^2+M+1)$. These unequal input and output impedance cause the magnitude and phase mismatches of each tap voltage at f_{null}. In this case, voltages at each tap at f_{null} can be calculated as below,

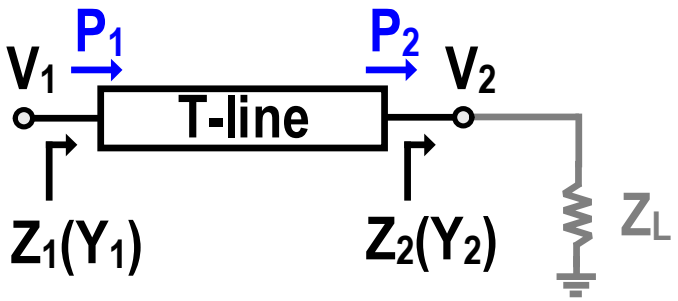
$$V_1 = -j\frac{V_S}{\frac{1}{M+4}\left(M+\frac{M+5}{M}+\frac{M+1}{M}+\frac{(M+5)(M^2+1)(M+1)}{M^3}\right)} \tag{4.3}$$

$$V_2 = -\frac{V_S}{\frac{M^2+M+1}{(M+4)(M+1)}+\left(\frac{M+5}{M+4}\right)\left(\frac{M^3+2M^2+M+1}{M^2(M+1)}\right)} \tag{4.4}$$

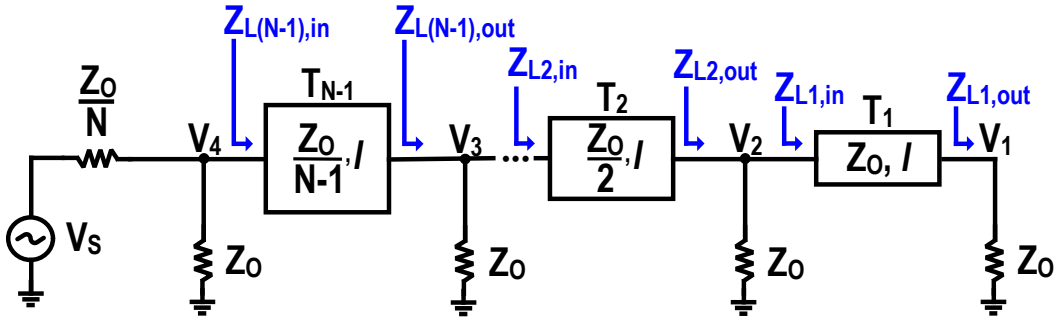
$$V_3 = j\frac{V_S}{\frac{M+5}{M+4}\frac{M^3+2M^2+M+1}{M(M^2+M+1)}+\frac{M}{M+4}} \tag{4.5}$$

$$V_4 = \frac{V_S}{\frac{M+5}{M+4}+\frac{M^2(M^2+M+1)}{(M+4)(M^3+2M^2+M+1)}} \tag{4.6}$$

It shows amplitude mismatch between each tap voltages, resulting to finite null-depth after combing. In addition, it is verified by a simulation with several different scaling factor of M. In this simulation, T-lines and power combiners are lossless and G_{max} of W-amps is set to 10 dB. When M is unity, it achieves the power gain of 9 dB at f_o, but the null-depth at f_{null} is -2.3 dB, only 11.3 dB attenuation between f_O and f_{null}. It is increased up to 21.8 dB with



(a)



	f_o	f_{null}
$Z_{L1,in}$	Z_0	Z_0
$Z_{L1,out}$	Z_0	Z_0
$Z_{L2,in}$	$\frac{Z_0}{2}$	$\frac{Z_0}{2}$
$Z_{L2,out}$	$\frac{Z_0}{2}$	$\frac{Z_0}{2}$
$Z_{L(N-1),in}$	$\frac{Z_0}{N-1}$	$\frac{Z_0}{N-1}$
$Z_{L(N-1),out}$	$\frac{Z_0}{N-1}$	$\frac{Z_0}{N-1}$

(b)

Fig. 4-6. (a) the inserted and delivered power through lossless T-line, (b) a delay-line with a series of T-lines of scaled characteristic impedance.

M=7, but the power gain is decreased to 5.6 dB at f_O. Its relation is organized in Fig. 4-5(b) with M=1,3,5,7.

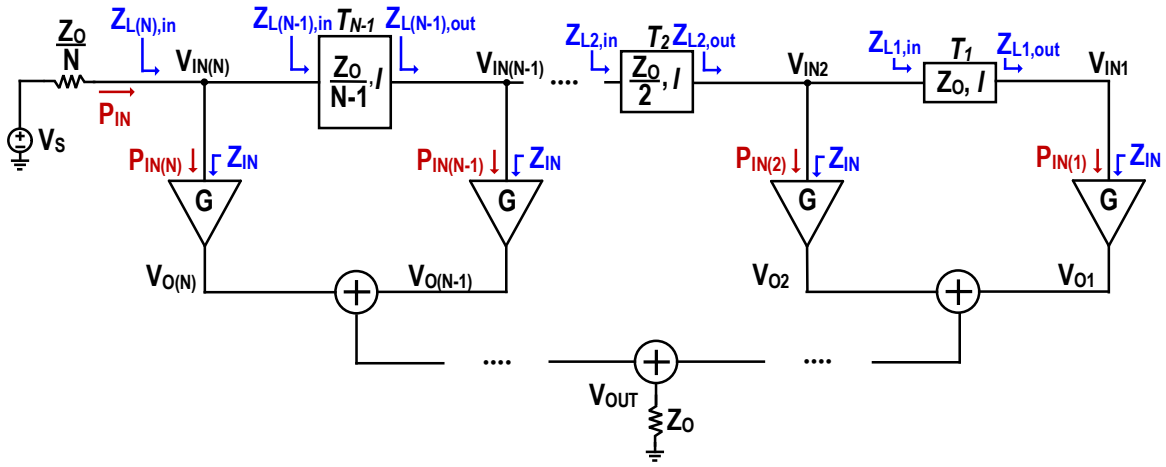


Fig. 4-7. Proposed N-tap FIR filter with scaled characteristic impedance of T-lines for delay lines.

In order to relieve this trade-off between the power gain and null-depth, it is important to analyze where this mismatch comes from. The T-line with a load of Z_L is presented in Fig. 4-6(a). If T-line is lossless, the inserted time-average power (P_1) is transferred to the load (P_2) without any loss. It can be presented as

$$P_1 = |V_1|^2 \,\mathrm{Re}(Y_1), \tag{4.7}$$

$$P_2 = |V_2|^2 \,\mathrm{Re}(Y_2). \tag{4.8}$$

To maintain the same voltages at input and output of T-line, the real part of input and output admittance should be same. Under this perception, the delay line without trade-off between the power gain and the finite null-depth is proposed based on the scaled characteristic impedance of T-lines without terminated Z_O as shown in Fig. 4-6(b). The characteristic impedance of each T-line is scaled down from the rightmost T-line to the leftmost T-line. For example, the characteristic impedance of T-line of T_1 is Z_O and that of T2 is $Z_O/2$. Likewise, the characteristic impedance of T_{N-1} is scaled down to $Z_O/(N-1)$. In addition, the terminated resistor can be removed to avoid power loss and the input impedance of W-amps is not necessarily to be high avoiding the load effect. In this case, the loading of Z_O is used. This delay line can be designed with the same input and output impedance of each T-line at both frequencies, f_o and f_{null}. For example, the input and output impedance of T-line,

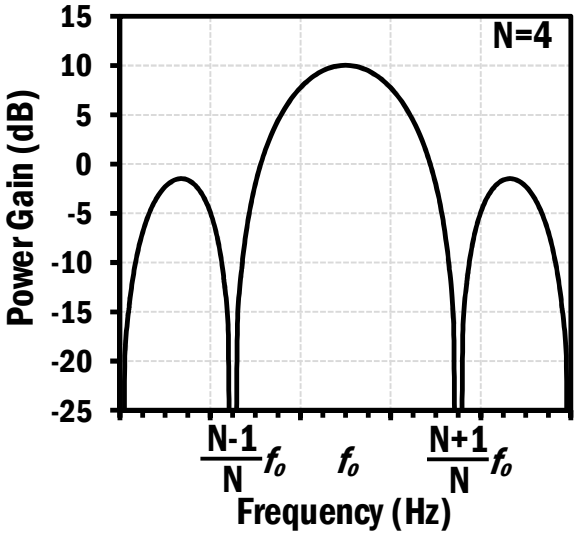


Fig. 4-8. Frequency response of proposed FIR filter.

T1 is same that $Z_{L1,in} = Z_{L1,out} = Z_O$ at f_o and f_{null}, simultaneously. All the way left, T-line of T_3 also satisfies that $Z_{L(N-1),in} = Z_{L(N-1),out} = Z_O/(N-1)$ at f_o and f_{null}.

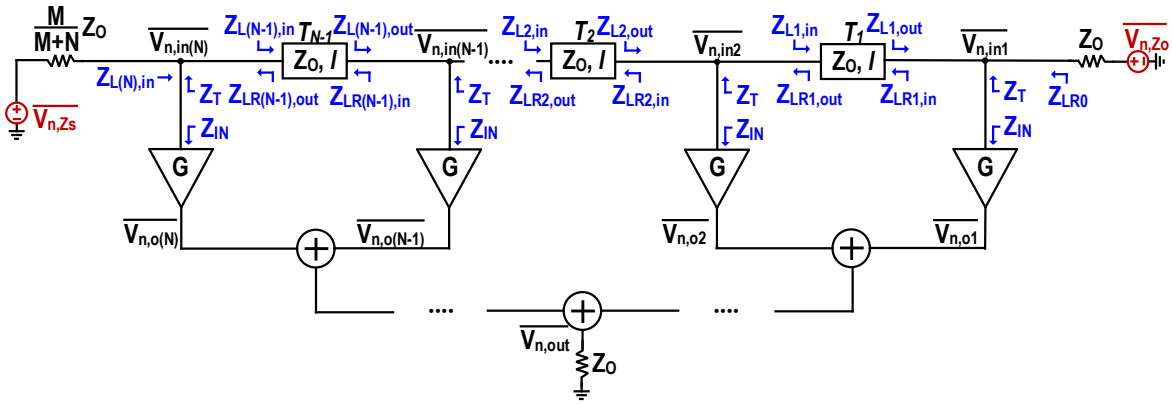
N-tap FIR filter based on this delay line is presented in Fig. 4-7. In this topology, the input impedance of W-amp, Z_{IN} is Z_O, not necessarily to be high for avoiding the loading effect. Then, thanks to the scaled characteristic impedance of each T-lines, the beginning and the end of output impedance at T-line is same at all frequency including f_o and f_{null}. In this case, the source impedance is matched to the input impedance of FIR filter as Z_O/N. The maximum available power from source is applied to the input of FIR filter at f_O, which is $P_{IN} = P_{AVS} = NV_S^2/(4Z_O)$. It is equally distributed to the input of W-amps without power dissipation at the terminated resistor. Its input power is multiplied with G_{max} of W-amps and combined by power combiners as $P_{OUT} = V_S^2 G_{max} N/(4Z_O)$. Finally, the transducer power gain is

$$G_T = \frac{P_{OUT}}{P_{AVS}} = G_{MAX} . \tag{4.9}$$

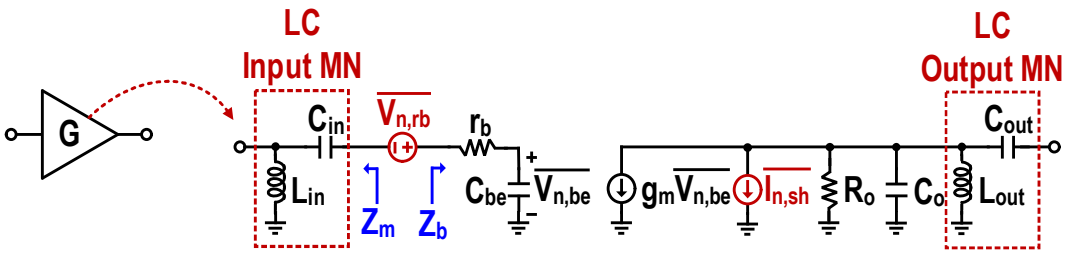
This topology can utilize G_{max} of W-amps without any loss of power. Furthermore, there is no trade-off between the gain at f_O and the null-depth at f_{null} as shown in Fig. 4-8. The total power gain of FIR filter is 10 dB as same as that of W-amps showing the infinite null-depth.

4.2.2 Noise Analysis of FIR Filters

The noise figure (NF) is one of the critical metrics in wireless receiver to obtain the required SNR. Even though NF of FIR filter is suppressed by the available power gain of preceding stage (e.g., LNA) based on Friis' equation [4-6], it is worthwhile to analyze NF of FIR filter itself. The general form of NF is $1+\overline{V_{n,out}^2}/(A_V^2 4kTR_S)$, where $\overline{V_{n,out}^2}$ is the output noise voltage from system excluding the contribution of source resistor, R_S, A_V is voltage gain from the source to the output, k is Boltzmann constant (1.38×10^{-23} J/K) and T is absolute temperature, respectively. Therefore, it is important to calculate the output noise voltage and the voltage gain with a given system. In case of the FIR filter comprised of the delay line with constant Z_O's T-lines terminated Z_O, the voltage gain is easily calculated that $A_V^2 = \frac{NG_{max}}{4M}$. Next is to identify the noise source of FIR filter. A FIR filter with all noise model is shown in Fig. 4-9(a). Thermal noise from the terminated Z_O is one of the noise source modelled as $\overline{V_{n,Z_O}^2}$=4kTZ_O Next, the W-amp is modeled in Fig. 4-9(b). r_b and C_{be} are base resistor and base-emitter capacitor and C_{in} and L_{in} are input matching capacitor and inductor. g_m, R_O and C_O are HBT's trans-conductance, output resistor and capacitor. C_{OUT} and L_{OUT} are the output matching component. Assume that the input and output matching networks are lossless. One of noise sources in this model are thermal noise voltage of r_b modeled as $\overline{V_{n,rb}^2}$=4kTr_b. Another noise source is shot noise current at the collector modeled as $\overline{I_{n,sh}^2}$ =2qI_C, where q is electric charge ($1.6\text{x}10^{-19}$C), I_C is DC collector current, respectively. The output noise voltage, $\overline{V_{n,out}^2}$ can be calculated by each noise source based on superposition. First, in order to calculate the output noise voltage due to the terminated Z_O, $\overline{V_{n,Z_O}^2}$ is placed at the end of delay line. At f_o, the input and output impedances of each T-line from the terminated Z_O are same that



(a)



(b)

Fig. 4-9. Noise model in N-tap FIR filters with (a) a delay line terminated Zo and (b) noise model of W-amps.

$$Z_{LR0}=\frac{M}{M+2N}Z_O, Z_{LR1,in}=Z_{LR1,out}=\frac{M}{M+2N-1}Z_O,$$
$$Z_{LR2,in}=Z_{LR2,out}=\frac{M}{M+2N-2}Z_O,\cdots, \quad . \tag{4.10}$$
$$Z_{LR(N-1),in}=Z_{LR(N-1),out}=\frac{M}{M+N+1}Z_O$$

Then, the noise voltages loaded at each tap are equally distributed as

$$\overline{V_{n,in1}^2}=\overline{V_{n,in2}^2}=\cdots=\overline{V_{n,in(N)}^2}=\overline{V_{n,Z_O}^2}\left(\frac{M}{2(M+N)}\right)^2 \tag{4.11}$$

due to the same input and output impedances between each T-line, (e.g., $Z_{LR1,in} = Z_{LR\ ,in}$, … ,$Z_{LR(N-1),in} = Z_{LR(N-1),out}$) and power conservation law. It is transferred to each C_{be} as

$$\overline{V_{n,be(Z_O)}^2} = \overline{V_{n,Z_O}^2}\left(\frac{M}{2(M+N)}\right)^2\left|\frac{C_{in}}{C_{in}+C_{be}}\frac{1}{1+s(C_{in}\parallel C_{be})r_b}\right|^2 \tag{4.12}$$

, where $\overline{V_{n,be(Z_O)}^2}$ is noise voltage developed at each C_{be} due to $\overline{V_{n,Z_O}^2}$. Another noise source is $\overline{V_{n,rb}^2}$ from base-resistor, r_b of 1_{st} to N_{th} W-amps. First, it is assumed that only $\overline{V_{n,rb}^2}$ of W-amp in N_{th} tap is existed and $\overline{V_{n,rb}^2}$ from other W-amps are nullified. The partial noise voltage is transferred to C_{be} of its W-amp as

$$\overline{V_{n,be(1)}^2} = \overline{V_{n,rb}^2}\left|\frac{1}{(Z_b+Z_m)}\frac{1}{sC_{be}}\right|^2 \tag{4.13}$$

, where Z_b and Z_m are the impedance seen to the base and delay lines as shown in Fig. 4-9(b). Another noise path is toward delay line and distributed to C_{be} of other W-amps of 1_{st} to $(N\text{-}1)_{th}$ taps. The noise voltage loaded in each T-lines is

$$\overline{V_{n,in(1)}^2} = \overline{V_{n,in(2)}^2} = \cdots = \overline{V_{n,in(N)}^2} = \overline{V_{n,rb}^2}\left|\frac{-Z_T}{Z_b+Z_m}\frac{sL_{in}}{Z_T+sL_{in}}\right|^2 \tag{4.14}$$

, where Z_T is the impedance seen to delay line at the input of W-amps as $MZ_O/(2M+2N-1)$. It is also equally distributed due to the equal input and output impedance between each T-lines that

$$
\begin{aligned}
Z_{L1,in} &= Z_{L1,out} = \frac{M}{M+1} Z_O, \\
Z_{L2,in} &= Z_{L2,out} = \frac{M}{M+2} Z_O, \cdots, \qquad . \\
Z_{L(N-1),in} &= Z_{L(N-1),out} = \frac{M}{M+N-1} Z_O
\end{aligned}
\tag{4.15}
$$

Then, it is distributed to each C_{be} at W-amps in 2nd to Nth taps as

$$
\overline{V_{n,be(2)}^2} = \overline{V_{n,rb}^2} \left| \frac{-Z_T}{Z_b + Z_m} \frac{sL_{in}}{Z_T + sL_{in}} \right|^2 \left| \frac{C_{in}}{C_{in} + C_{be}} \frac{1}{1 + s\left(C_{in} \parallel C_{be}\right) r_b} \right|^2 \tag{4.16}
$$

Next, other base resistors of W-amp from 2nd to Nth taps also contain the noise voltage of $\overline{V_{n,rb}^2}$ and transfer noise directly and indirectly to each C_{be} with same mechanism explained above. Finally, the total noise voltage at each C_{be} due to the terminated Z_O and N's base resistors is

$$
\overline{V_{n,be}^2} = \overline{V_{n,be(Z_O)}^2} + \overline{V_{n,be(1)}^2} + \left(N-1\right) \overline{V_{n,be(2)}^2} \tag{4.17}
$$

, where the coefficient of $\overline{V_{n,be(2)}^2}$, (N-1) comes from the uncorrelated noise of N's r_b. It is converted to noise current by g_m at collector and the combined with collector's shot noise current as $\overline{I_{n,c}^2}=g_m^2\overline{V_{n,be}^2}+\overline{I_{n,sh}^2}$, transferring to the output of W-amp under the conjugate-matching condition with lossless LC components. The noise power transferred to the output load resistor, Z_O is $P_{n,o(N)}=\frac{1}{4}(g_m^2\overline{V_{n,be}^2}+\overline{I_{n,sh}^2})R_O$, then the output noise voltage is expressed as

$$
\overline{V_{n,o(N)}^2} = \overline{V_{n,o(N-1)}^2} = \cdots = \overline{V_{n,o(1)}^2} = \frac{1}{4}\left(g_m^2 \overline{V_{n,be}^2} + \overline{I_{n,sh}^2} \right)\left(R_O Z_O \right). \tag{4.18}
$$

Each output noise voltage at W-amps experience the voltage gain of $1/\sqrt{N}$ thru the N's power combiner array, where its analysis is explained in detail in Appendix II. While combing the noises at the output of power combiners, careful consideration is necessary due to the correlation of noise each other. Finally, the output voltage noise can be expressed as

$$\overline{V_{n,out}^2}$$
$$= \frac{R_O Z_O}{4}\left(g_m^2 \left(\left(\frac{\overline{V_{n,be(Z_O)}}}{\sqrt{N}} \right)^2 N^2 + \left(\frac{\overline{V_{n,be(1)}}}{\sqrt{N}} + \frac{V_{n,be(2)}}{\sqrt{N}}(N-1) \right)^2 N \right) + \left(\frac{\overline{I_{n,sh}}}{\sqrt{N}} \right)^2 N \right) \quad . \quad (4.19)$$
$$= \frac{R_O Z_O}{4}\left(g_m^2 \left(\overline{V_{n,be(Z_O)}^2} N + \overline{V_{n,be(1)}^2} + (N-1)^2 \overline{V_{n,be(2)}^2} + (N-1)\left(C + C^*\right) \sqrt{\overline{V_{n,be(1)}^2}\,\overline{V_{n,be(2)}^2}} \right) + \overline{I_{n,sh}^2} \right)$$

The noise from the terminated Z_O, $\overline{V_{n,Z_O}^2}$ is fully correlated at the output due to the same noise transfer that N-path noises are combined at the output by N^2. Next, the noise from N's base resistors, r_b are uncorrelated which is combined by N. However, each r_b contributes the output noise with two different transfer paths. As explained in this section, one noise path for $\overline{V_{n,be(1)}^2}$ and the other N-1 paths for $\overline{V_{n,be(2)}^2}$. These noises are partially correlated presented by correlation coefficient of C as

$$C = \frac{\overline{V_{n,be(1)} V_{n,be(2)}^*}}{\sqrt{V_{n,be(1)}^2 V_{n,be(2)}^2}} = \frac{\left(\frac{1}{(Z_b + Z_m)} \frac{1}{sC_{be}} \right) \left(\frac{-Z_T}{Z_b + Z_m} \frac{sL_{in}}{Z_T + sL_{in}} \frac{C_{in}}{(C_{in} + C_{be})} \frac{1}{1 + s(C_{in} \| C_{be}) r_b} \right)^*}{\sqrt{\left| \frac{1}{(Z_b + Z_m)} \frac{1}{sC_{be}} \right|^2 \left| \frac{-Z_T}{Z_b + Z_m} \frac{sL_{in}}{Z_T + sL_{in}} \frac{C_{in}}{(C_{in} + C_{be})} \frac{1}{1 + s(C_{in} \| C_{be}) r_b} \right|^2}} . \quad (4.20)$$

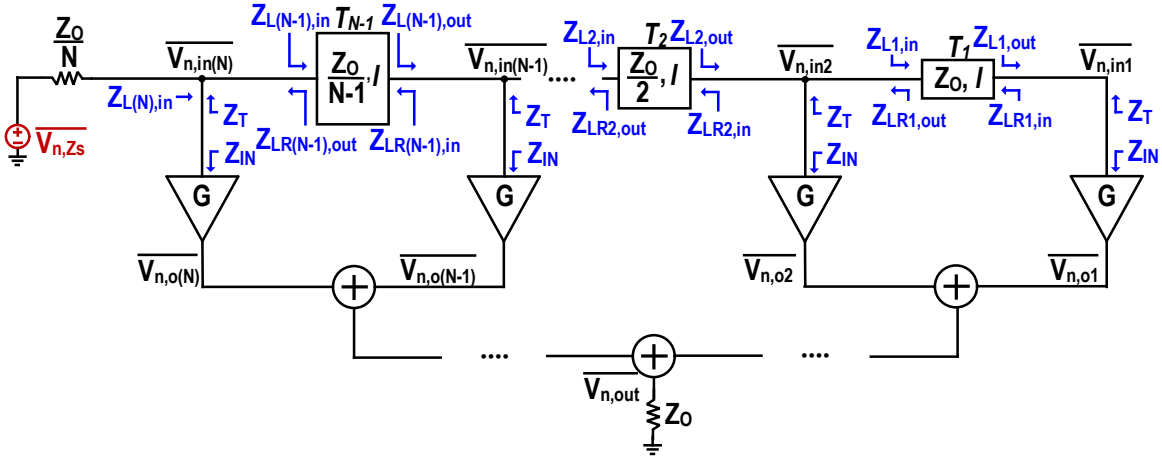
The noises from the N's collector shot noise currents is uncorrelated each other that are combined by N at the output of combiners.

The total NF is

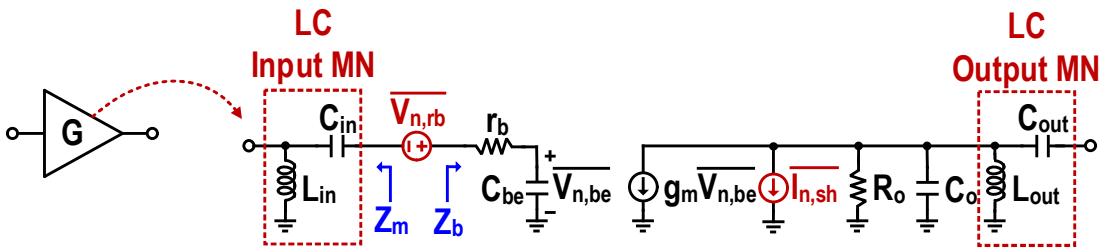
$$NF = 1 + \frac{\overline{V_{n,out}^2}}{A_V^2 (4kTR_s)} = 1 + \frac{4(M+N)\overline{V_{n,out}^2}}{NG_{\max}(4kTZ_O)} \quad (4.21)$$

, where $A_V^2 = NG_{max}/(4M)$ and $R_s = MZ_O/(M+N)$, respectively. $\overline{V_{n,out}^2}$ is expressed in (4-19).

For the noise analysis of proposed FIR filter comprised the delay line with scaled characteristic impedance of T-line, the noise sources are also modeled in Fig. 4-10(a), (b). All noise source is same with previous one except the one in the terminated Z_O. The mechanism of noise transfer is same with above, but impedances of forward/reverse in/output of T-lines and Z_T are different as $Z_{L1,in} = Z_{L1,out} = Z_O$, $Z_{L2,in} = Z_{L2,out} = Z_O/2$,



(a)



(b)

Fig. 4-10. Noise model in N-tap FIR filters with (a) a scaled Zo delay line and (b) noise model of W-amps.

$\ldots, Z_{L(N-1),in} = Z_{L(N-1),out} = Z_O/(N-1)$. $Z_{LR1,in} = Z_{LR1,out} = Z_O/(2N-1)$, $Z_{LR2,in} = Z_{LR2,out} = Z_O/(2N-2)$, $\ldots, Z_{LR(N-1),in} = Z_{LR(N-1),out} = Z_O/(N+1)$, and $Z_T = Z_O/(2N-1)$. Then, the expression of the noise voltage at the output is

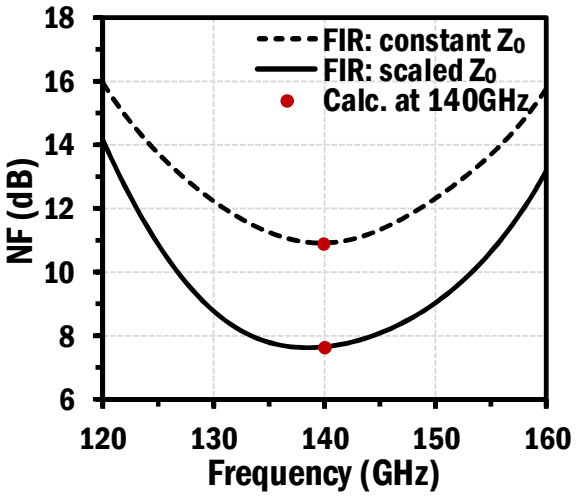
$$\overline{V_{n,out}^2} = \frac{R_O Z_O}{4}\left(g_m^2 \left(\frac{V_{n,be(1)}}{\sqrt{N}} + \frac{V_{n,be(2)}}{\sqrt{N}}(N-1) \right)^2 N + \left(\frac{\overline{I_{n,sh}}}{\sqrt{N}} \right)^2 N \right)$$

$$= \frac{R_O Z_O}{4}\left(g_m^2 \left(\overline{V_{n,be(1)}^2} + (N-1)^2 \overline{V_{n,be(2)}^2} + (N-1)\left(C + C^*\right)\sqrt{\overline{V_{n,be(1)}^2}\,\overline{V_{n,be(2)}^2}} \right) + \overline{I_{n,sh}^2} \right)$$

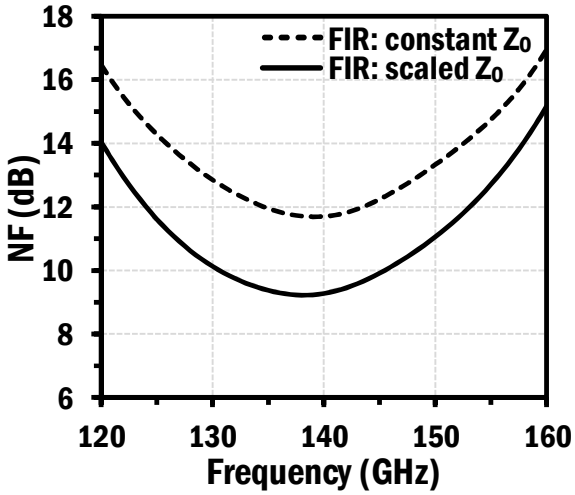
(4.22)

The NF is also expressed as

$$NF = 1 + \frac{\overline{V_{n,out}^2}}{A_V^2 \left(4kTR_s\right)} = 1 + \frac{4\overline{V_{n,out}^2}}{G_{\max}\left(4kTZ_O\right)} \tag{4.23}$$



(a)



(b)

Fig. 4-11. The simulated result of NF with (a) ideal components with modelled noise source and (b) 8HP PDK for HBT.

, where $A_V^2 = NG_{max}/4$ and $R_s = Z_O/N$, respectively.

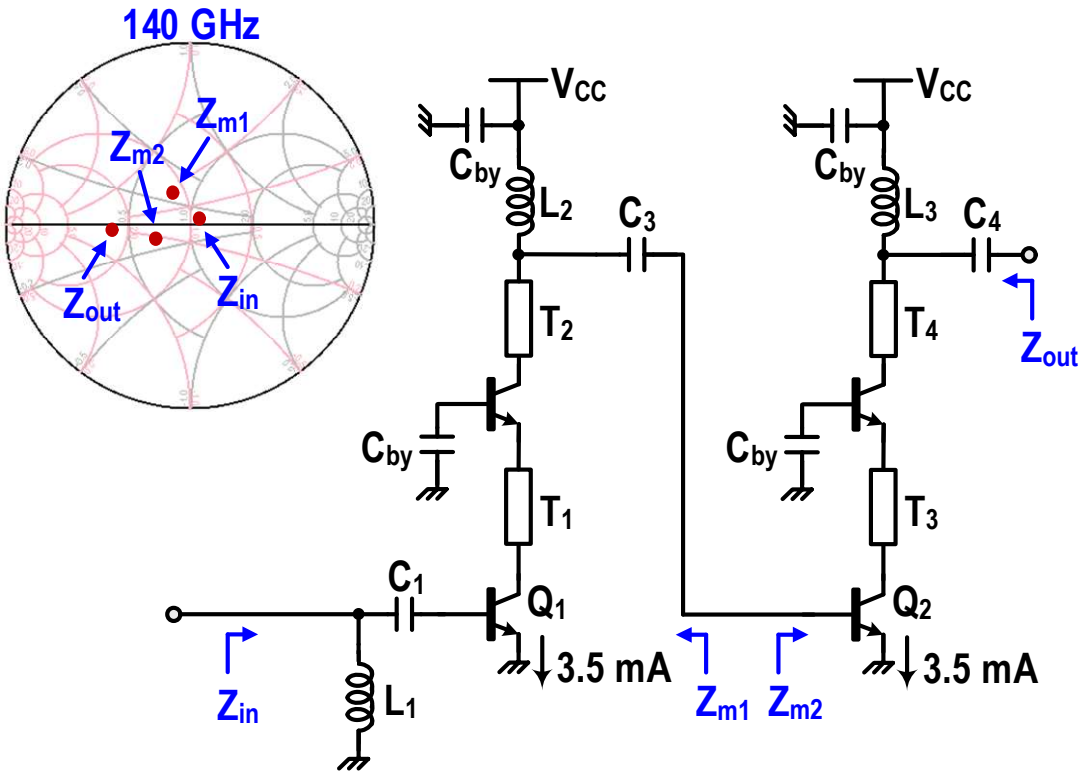
Both NF are referred by the output impedance of preceding stage, fairly compared in cascade system. Its analysis is verified with a simulation of ideal passive, active components with modeled noise sources and ideal passive components, HBT PDK model of IBM 8HP technology. In ideal active one, the collector shot noise is modelled with I_c=3 mA, which is

$\overline{I_{n,sh}}$=31pA and r_b=40 Ω extracted from PDK model. In addition, the values of noiseless parameter for C_{be}, g_m, R_o and C_o are also extracted from 8HP PDK effectively, which are 50 fF, 70 mS, 500 Ω and 15 fF and G_{max} of ideal active transistor and PDK is set for 9 and 8.5 dB at 140 GHz, respectively. Fig. 4-11(a), (b) presents the simulated NF for ideal one and HBT from PDK. Ideal one shows NF of 10.9 and 7.6 dB for each FIR filter with constant Z_O and scaled Z_O delay line at 140GHz. At 140 GHz, the calculated NF based on equations of (4-20,22) are exactly same with simulation. NF from PDK is 11.7 and 9.3dB for each FIR filter with constant Zo and scaled Zo delay.

4.3 Implementation of Proposed 4-tap FIR Filter

A pre-amplifier of 2-stage cascode is followed by the 4-tap FIR filter, providing a gain (>10 dB) around 140 GHz shown in Fig. 4-12. All HBT is sized L_e=3 μm for low power consumption. Supply voltage, V_{CC} is set to 2.8 V, DC collector current, I_C for 3.5 mA for each stage. The input port is matched to 50 Ω with series capacitor, C_1 (≈40 fF) and shunt inductor designed with T-line, L_1 (≈70 pH). Bypass Capacitor, C_{by} is designed with MIM cap with EM simulation, (≈400 fF). The inter-stage is also matched with T_2 (50 Ω, 32°), L_2 (≈32 pH) and C_3 (≈200 fF). The output impedance of 1st stage, Z_{m1} is 38+j15 Ω and the input impedance of 2nd stage to base node, Z_{m2} is 30-j2 Ω, slightly mismatched from the conjugate-match condition at 140 GHz. At the output impedance of 2nd stage is matched to 20 Ω, instead of 50 Ω for the conjugate-match with the input impedance of the following stage likewise 1st stage output matching but different component values.

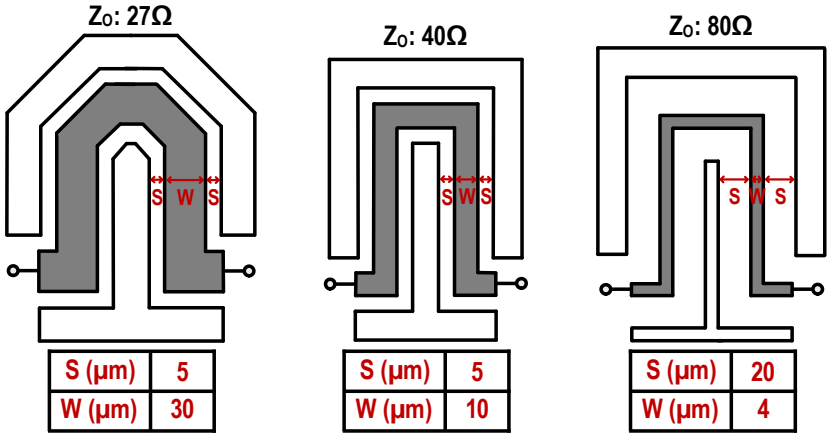
A delay line is implemented with scaled characteristic impedance for each T-lines. The 4-tap delay line requires three T-lines with different characteristic impedance. In this technology, the available characteristic impedance is 20 ~ 80 Ω based on GCPW, top metal (AM) for signal and ground and 3rd one from the top metal (MQ) for ground. The characteristic impedances of each T-line, Z_{O1}, Z_{O2} and Z_{O3} are designed with 80, 40 and 27 Ω, respectively. For a high characteristic impedance, the width of signal line is to be narrow, which the width of signal lines is 4, 10 and 30 μm and the space between signal line and



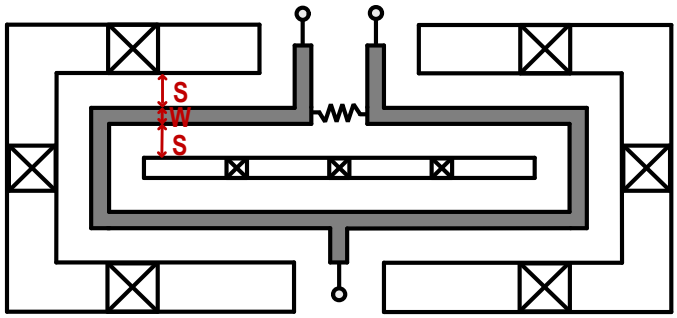
	f_O
Z_{in}	50 Ω
Z_{m1}	38+j15 Ω
Z_{m2}	30-j2 Ω
Z_{out}	20 Ω

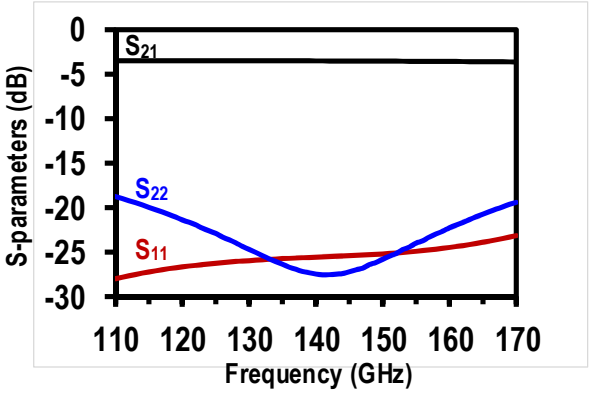
Fig. 4-12. The schematic of pre-amplifier.

ground plane at the top metal is for 20, 5 and 5 μm, respectively. The required physical length of each T-line is λ at f_O, 140 GHz, which is around 1100 μm. Fig. 4-13(a) presents the physical dimension of each T-lines. The loss of each T-line, λ at 140 GHz is around 1 dB.



(a)

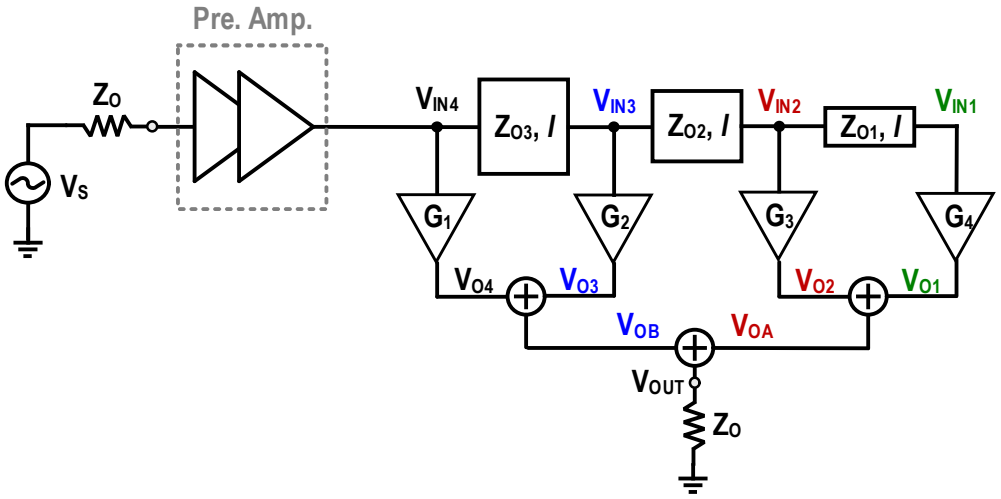




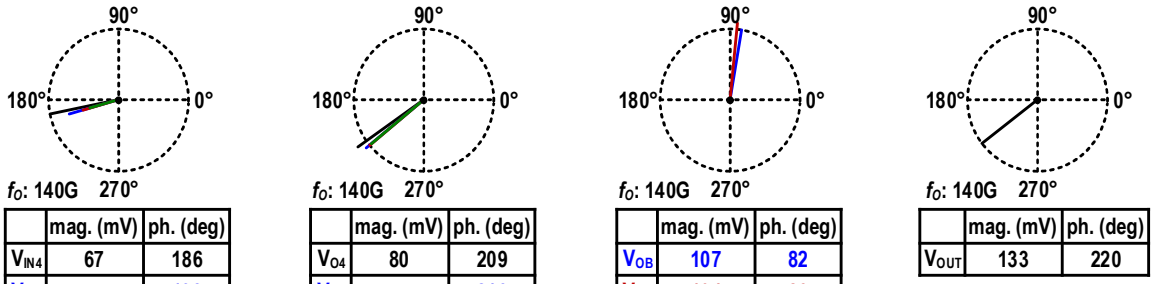
(b)

Fig. 4-13. Delay lines with 80, 40 and 27 Ω and the layout and S-parameters of Wilkinson power combiner at 140 GHz.

A W-amp is implemented of 1-stage cascode amplifier. It is designed to be similar to the pre-amplifier, but the input impedance is set to 80 Ω and the output impedance of 50



(a)



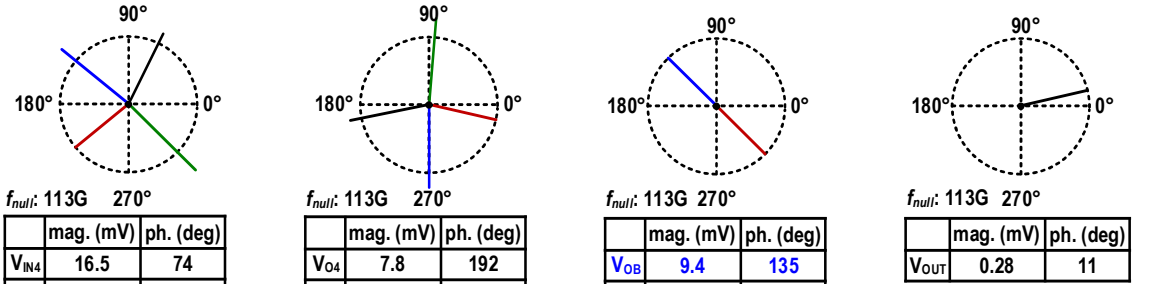
	mag. (mV)	ph. (deg)
V_{IN4}	67	186
V_{IN3}	55	193
V_{IN2}	46	192
V_{IN1}	41	190

	mag. (mV)	ph. (deg)
V_{O4}	80	209
V_{O3}	77	216
V_{O2}	75	218
V_{O1}	74	218

	mag. (mV)	ph. (deg)
V_{OB}	107	82
V_{OA}	104	86

	mag. (mV)	ph. (deg)
V_{OUT}	133	220

(b)



	mag. (mV)	ph. (deg)
V_{IN4}	16.5	74
V_{IN3}	17.3	150
V_{IN2}	12.6	220
V_{IN1}	18.8	321

	mag. (mV)	ph. (deg)
V_{O4}	7.8	192
V_{O3}	8.4	270
V_{O2}	7.0	346
V_{O1}	9.8	85

	mag. (mV)	ph. (deg)
V_{OB}	9.4	135
V_{OA}	9.5	313

	mag. (mV)	ph. (deg)
V_{OUT}	0.28	11

(c)

Fig. 4-14. (a) FIR filter with pre-amplifier and (b) phase diagram of signal combining at f_o and (c) phase diagram of signal nullifying at f_{null}.

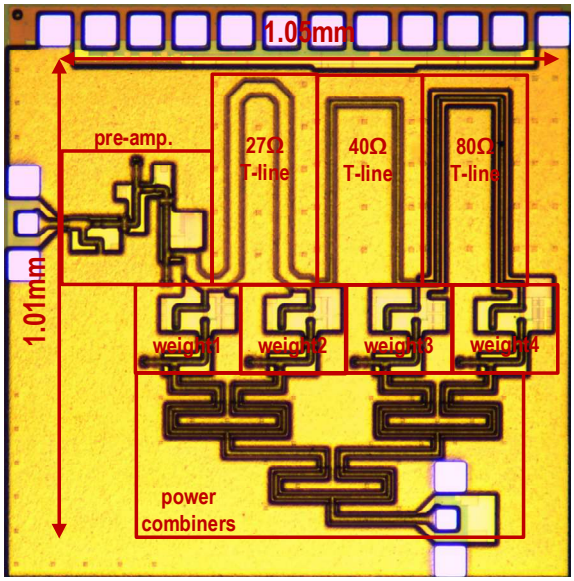
Ω to match with the next stage. The gain is varied by controlling I_C. In simulation, the gain

is varied from 6.8 to 3.8 dB of 1 dB step with I_C of 3.5 ~ 1.7 mA range.

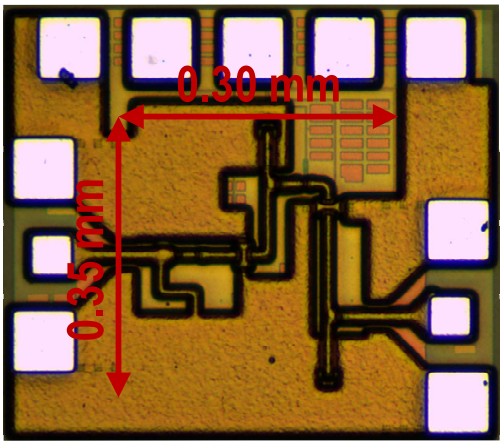
Three Wilkinson power combiners are utilized for 4-tap signal combining after W-amps. The input/output is matched to 50 Ω and shows S_{11}/S_{22} less than -10 dB through D-band. The characteristic impedance of λ/4 line is 70.7 Ω implemented by GCPW transmission line, which is the width of signal line is 4 μm and the space between the signal line and GND plane of 14 um. The simulated insertion loss is 3.4~3.6 dB with whole D-band range, which can be utilized as a power combiner at both f_O and f_{null} without any significant loss.

The simulation of signal combing at f_O (140 GHz) and nullifying at f_{null} (113 GHz) at each stage are presented with phase diagram in Fig. 4-14(b), (c) and each node voltages are noted in Fig. 4-14(a). At 140 GHz, the voltages loaded at each T-lines, V_{IN1} to V_{IN4} shows some amplitude mismatch due to the loss of T-lines, (magnitude of V_{IN1}=41, V_{IN2}=46, V_{IN3}=55, V_{IN4}=67 mV with the input power of -25 dBm, 18 mV referred to 50 Ω). It is compensated by the variable gain of W-amps before power combining, (magnitude of V_{O1}=74, V_{O2}=75, V_{O3}=77, V_{O4}=80 mV). Finally, it is combined in-phase to 133 mV by Wilkinson combiner. In contrast, a signal is cancelled out at f_{null}. Due to the low gain of pre-amplifier at f_{null}, the magnitude of voltages loaded at each T-lines is that V_{IN1}=18.8, V_{IN2}=12.6, V_{IN3}=17.3, V_{IN4}=16.5 mV with quadrature phase difference. Finally, it is cancelled out at power combiners with out of phase signal of V_{OA}=9.5e^(j313°) mV and V_{OA}=9.4e^(j135°), resulting to V_{OUT}=0.28e^(j11°).

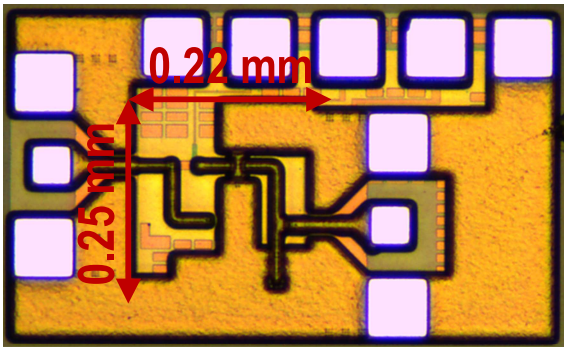
4.4 Experimental Results of 4-tap FIR filter and block-out circuits



(a)



(b)



(c)

Fig. 4-15. Chip microphotograph of (a) the proposed FIR filter, (b) the pre-amplifier and (c) the weighting amplifier.

The proposed FIR filter is implemented in 0.13μm BiCMOS technology, and its chip photograph is shown in Fig. 4-15. The core chip area without the pads is 1.05 x 1.01 mm^2. The FIR filter is characterized with on-wafer testing using GSG probes for RF signal measurement. TRL calibration is done for S-parameter measurement. A network analyzer is connected to D-band frequency extender for S-parameter at D-band range. S-parameter is shown in Fig. 4-16. The measured peak power gain is 13dB at 150GHz, presenting BW_{-3dB} of 140-153 GHz. The low-side null frequency (f_{null}) is measured with null-depth of -33dB at

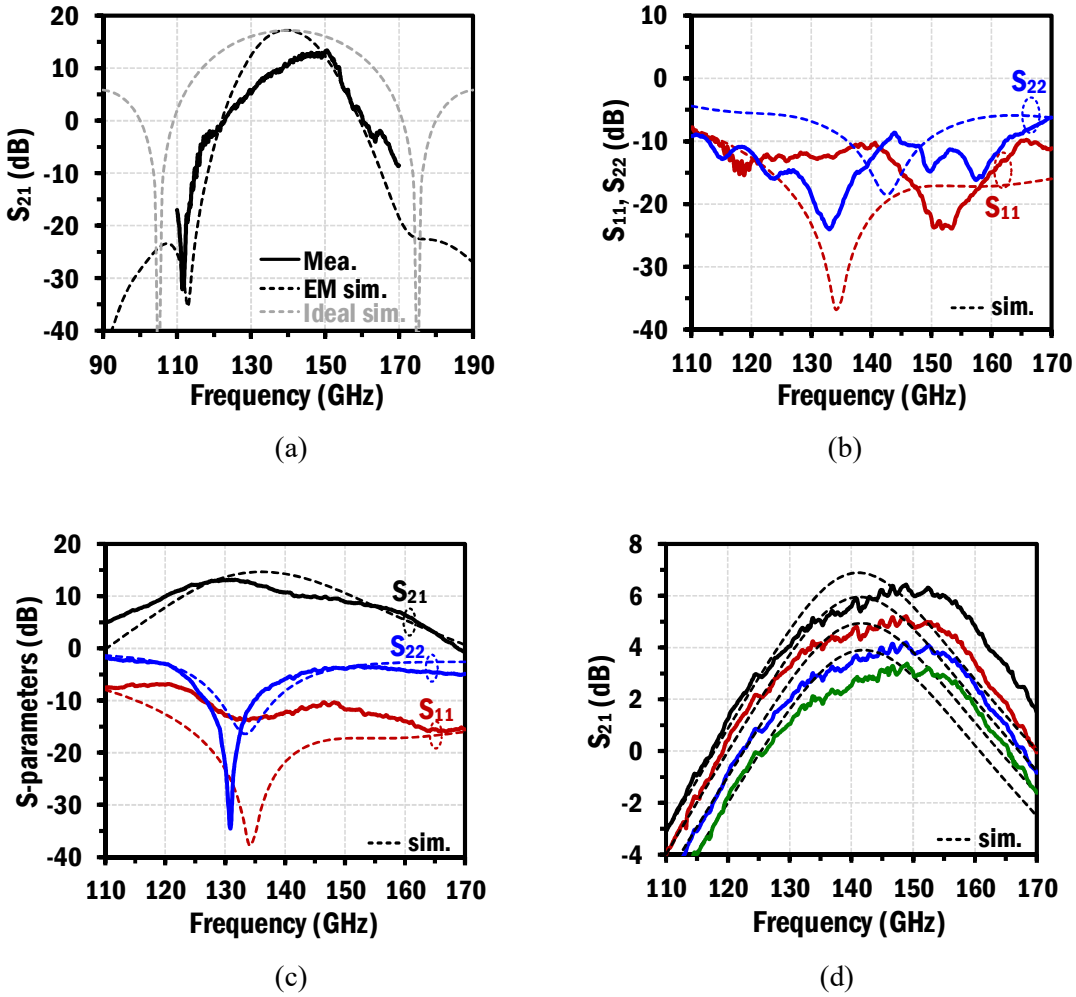


Fig. 4-16. (a) The measured S21 FIR filter, (b) S11/S22 of FIR filter, (c) S-parameters of pre-amplifier and (d) the variation of gain of W-amp.

111.5GHz, showing ≥40dB attenuation between the null and center frequency range. Input, output matching (S_{11},S_{22}) is shifted, but still less than -10dB around center frequency range. Stand-alone circuits, pre-amplifier and weighting amplifier are also measured. The area of pre-amplifier and weighting amplifier excluding pads is 0.3x0.35 mm^2 and 0.22x0.25 mm^2, respectively. The peak gain of pre-amplifier is 13dB at 13GHz with BW_{-3dB} of 120-143 GHz. Input matching, S_{11} is less than -10 dB from 126 to 170GHz. The output is matched to 20 Ω , not 50 Ω for conjugate-matched to the input of core FIR filter, presenting S_{22} is -3 to -5 dB at the center frequency range (140-153 GHz). The gain of weighting amplifier is varied

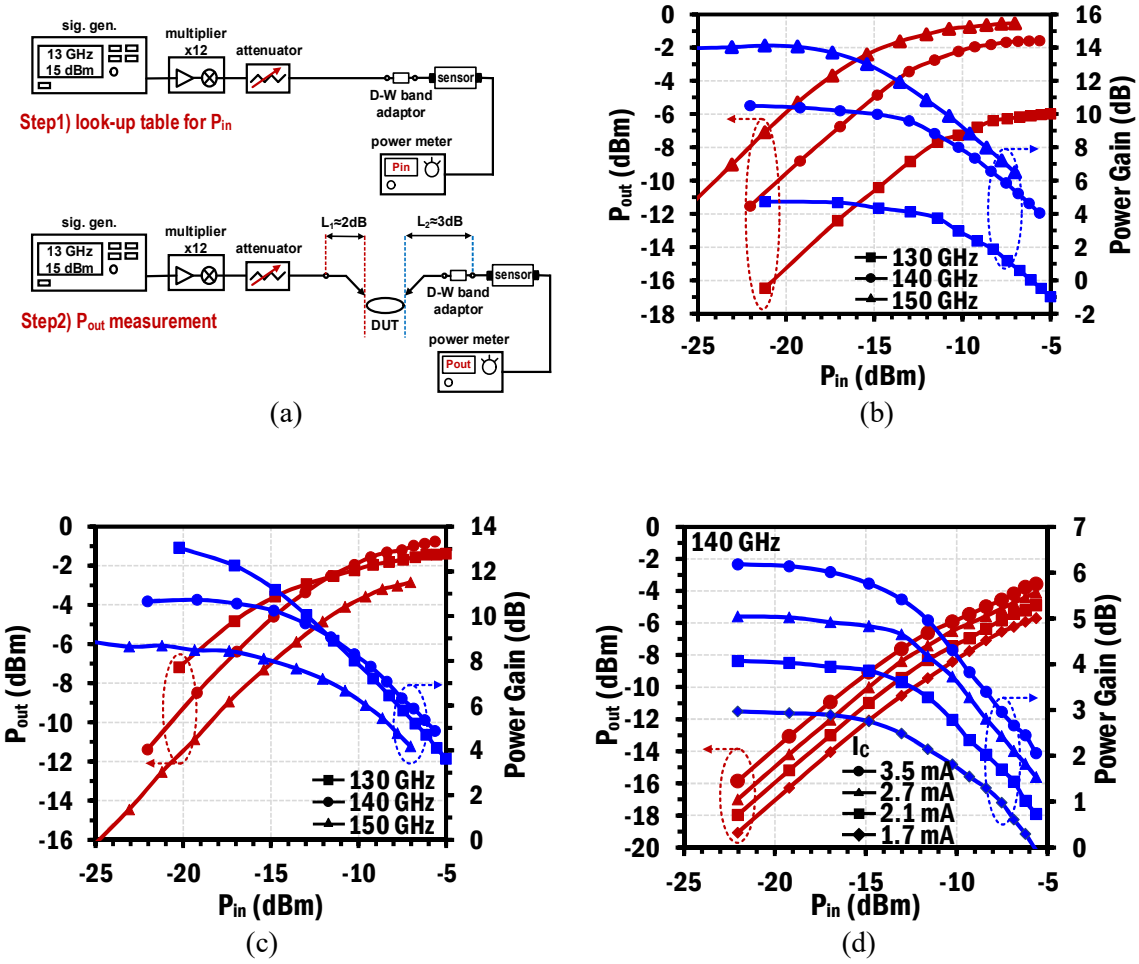


Fig. 4-17. (a) The large signal measurement setup, the measured large signal of (b) FIR filter, (c) pre-amplifier and (d) weighting amplifier.

to compensate the loss of delay line and it is measured from 6 to 3 dB with 1dB steps in Fig. 4-16(d).

Large signal is also measured for FIR filter, pre-amplifier and weighting amplifier. D-band signal is generated by signal generator followed by frequency extender. At the output side, the power meter (PM5) is directly connected to the output GSG probe and wave guide and D-to-W band adaptor. The output 1dB compression point (OP_{-1dB}) of FIR filter is measured at 130, 140 and 150GHz that are -7.5, -2.5 and -2.4 dBm, respectively. The linearity of pre-amplifier is also measured at 130, 140 and 150GHz that are -4.7, -3.4 and -5.9 dBm, respectively. For the weighting amplifier, large signal of OP_{-1dB} is measured at 140GHz which is -6.8, -7.4, -7.6 and -9.3dBm with 3.5, 2.7, 2.1 and 1.7mA, respectively.

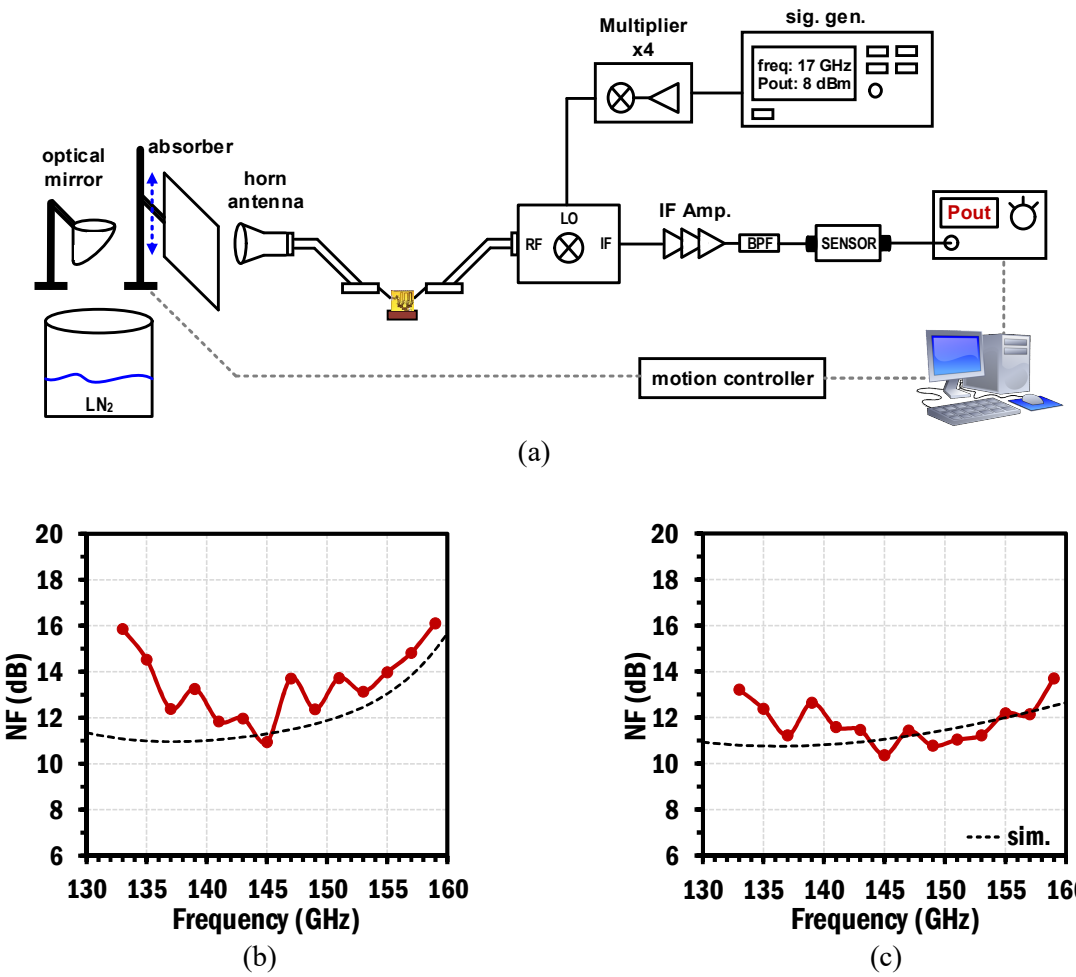


Fig. 4-18. (a) NF setup by Y-factor method and measured NF of (b) FIR filter and (c) pre-amplifier.

Noise measurement is conducted by using Y-factor method. It utilizes two different temperature radiating different power from different temperature. Cold temperature source is used with liquid nitrogen (LN2) for 77K and ambient temperature is used as hot temperature source for 290K. With cold temperature source, output noise power can be measured as $N_{O,cold}$ and output noise power by ambient temperature is $N_{O,hot}$, where are expressed as

$$N_{O,cold} = GkT_{cold}B + GkT_eB \tag{4.24}$$

$$N_{O,hot} = GkT_{hot}B + GkT_eB. \tag{4.25}$$

TABLE 4-I. PERFORMANCE COMPARISON OF IMAGE REJECTION IN MMW RANGE

Reference	RF Freq. (GHz)	IR Topology	IRR (dB)	IF Freq. (GHz)	IP_{-1dB} (dBm)	NF (dB)	P_{diss} (mW)	Process
This work	140	FIR filtering	43	28.5	-15.4	11	48 (IR Filter)	0.13μm SiGe
IMS 2018 Ma *et al.*	35-105	Quadrature LO	43@ 105GHz	5	-21.5	5-11.5	598.5 (Rx)	0.12μm SiGe
JSSC 2013 Shahramian *et al.*	70-100	Quadrature LO	42@ 90GHz	0.01	-35~-25	<7	500 (1ch. Tx+Rx)	0.18μm SiGe
TMTT 2013 Lin *et al.*	64 - 84	Quadrature LO	25@ 95GHz	0.00125	-24	N/A	40.8 (IR Mixer)	65nm CMOS
ISSCC 2010 Sandstrom *et al.*	75 - 95	Quadrature RF	15 - 20	1-8	-5.3	N/A	120 (Tx)	65nm CMOS
TMTT 2016 Hsieh *et al.*	60-84	Quadrature RF	23 - 33.9	4-6.5	-25.2	8.9	46 (Rx)	90nm CMOS

Y-factor is defined the ratio of the output noise power by hot temperature to the noise power by cold temperature as

$$Y = \frac{N_{O,hot}}{N_{O,cold}} = \frac{T_{hot} + T_e}{T_{cold} + T_e} \tag{4.26}$$

, then the equivalent noise temperature, Te is determined as

$$T_e = \frac{T_{hot} - YT_{clod}}{Y - 1} \tag{4.27}$$

Finally, NF is expressed as

$$NF = 1 + \frac{T_e}{T_o} \tag{4.28}$$

, where T_o is reference temperature, 290K. In Fig. 4-18(a), NF measurement set-up is described that noise temperature is distinguished by motorized absorber. When absorber is placed in the mirror and horn antenna ambient temperature is used for noise source and it is placed up the cold noise power focused by optical mirror is applied to horn antenna. Then, the output noise power from two different temperature is down converted to IF frequency at 1840 MHz by sub-harmonic mixer and amplified by IF amplifiers of 45dB gain and filtered

out 1750-1930MHz. NF acquired by this method is total NF of system from the horn antenna to IF filter. It needs to be de-embedded by Friis' law as

$$NF_{total} - 1 = (NF_{probe} - 1) + \frac{(NF_{FIR} - 1)}{G_{probe}} + \frac{(NF_{probe} - 1)}{G_{probe}G_{FIR}} + \frac{(NF_{mix} - 1)}{G_{probe}G_{FIR}G_{probe}} + \frac{(NF_{Amp} - 1)}{G_{probe}G_{FIR}G_{probe}G_{mix}}$$
$$NF_{FIR} = \left(NF_{total} - \left(NF_{probe} + \frac{(NF_{probe} - 1)}{G_{probe}G_{FIR}} + \frac{(NF_{mix} - 1)}{G_{probe}G_{FIR}G_{probe}} + \frac{(NF_{Amp} - 1)}{G_{probe}G_{FIR}G_{probe}G_{mix}} \right) \right) G_{probe} + 1 \quad (4.29)$$

NF of FIR filter is measured in Fig. 4.18(b) that shows 11-14 dB range at 135-155 GHz. The NF of pre-amplifier is also measured in Fig. 4.19(c) that shows 10-12 dB range at 135-155 GHz where NF of core FIR filter is sufficiently compressed by the gain of pre-amplifier of >10 dB.

Table 4-I presents the comparison of image rejection in millimeter-wave range with this works. It shows 43dB attenuation with state-of-art performance at D-band reange.

4.5 Summary

A 4 tap FIR filter operating at D-band has been proposed and analyzed. Characteristics of the FIR filter have been compared to the FIR filter with conventional delay line. The proposed FIR filter relieves the loading effect due to the finite impedance of W-amps, maximizing the power gain at the operating frequency and generating infinite null depth. In depth noise analysis and comparison of the noise performance between the proposed FIR filter and conventional FIR filter are presented in this chapter. To verify performance of the proposed FIR filter, a test chip was been designed and fabricated using 0.13 μm BiCMOS technology. The prototype FIR filter is measured peak power gain of 13dB at 150 GHz with BW_{-3dB} of 140-153 GHz. The measured low-side null frequency (f_{null}) is 111.5 GHz and the measured with null-depth is -33dB, achieving ≥40dB attenuation. The input and output matching (S_{11},S_{22}) are better than -10dB around center frequency range

Reference

[4-1] B. Agarwal et al., "112-GHz, 157-GHz, and 180-GHz InP HEMT traveling-wave amplifiers," in IEEE Transactions on Microwave Theory and Techniques, vol. 46, no. 12, pp. 2553-2559, Dec 1998.

[4-2] P. V. Testa, C. Carta and F. Ellinger, "Analysis and Design of a 220-GHz Wideband SiGe BiCMOS Distributed Active Combiner," in IEEE Transactions on Microwave Theory and Techniques, vol. 64, no. 10, pp. 3049-3059, Oct. 2016.

[4-3] J. F. Buckwalter and J. Kim, "Cascaded Constructive Wave Amplification," in IEEE Transactions on Microwave Theory and Techniques, vol. 58, no. 3, pp. 506-517, March 2010.

[4-4] P. V. Testa, C. Carta, M. Barahona and F. Ellinger, "0.5–20-GHz UWB Distributed Combiners and Dividers for Multi-Antenna Transceivers," in IEEE Transactions on Microwave Theory and Techniques, vol. 65, no. 9, pp. 3087-3098, Sept. 2017.

[4-5] K. Eriksson, I. Darwazeh and H. Zirath, "InP DHBT Distributed Amplifiers With Up to 235-GHz Bandwidth," in IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 4, pp. 1334-1341, April 2015.

[4-6] Behzad Razavi, RF microelectronics, Prentice Hall, 2011.

Appendix A.

Power Dissipation at Transistors

In this chapter, the definition of power is explained in detail to help understand power amplifiers. First, let's investigate the instantaneous power with steady-state sinusoidal voltage and current which are noted as

$$\begin{aligned} v(t) &= V_m \cos(\omega_o t + \theta_V), V = V_m e^{j\theta_V} \\ i(t) &= I_m \cos(\omega_o t + \theta_I), I = I_m e^{j\theta_I} \end{aligned} \tag{A.1}$$

, where V_m and I_m are peak voltage and current magnitude and θ_V and θ_V are phase of voltage and current, respectively. The expression of instantaneous power becomes

$$p(t) = v(t)i(t) = \frac{V_m I_m}{2}\cos(\theta) + \frac{V_m I_m}{2}\cos(\theta)\cos(2\omega_o t) - \frac{V_m I_m}{2}\sin(\theta)\sin(2\omega_o t) \tag{A.2}$$

, where θ=θ_V-θ_I, the phase difference of voltage and current. Now, it can be noted by the average power and reactive power as

$$\begin{aligned} P &= \frac{V_m I_m}{2}\cos(\theta) \\ Q &= \frac{V_m I_m}{2}\sin(\theta) \end{aligned} \tag{A.3}$$

Where P is average power and Q is reactive power. The average power is the power consumed at the resistor or that is transformed from electric to non-electric energy [A-1]. The reactive power is a power to be stored in reactive passive devices (e.g., inductors or

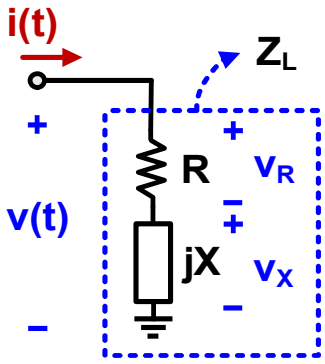


Fig. A-1. Power transfer to the complex load, Z=R+jX (R: resistance, X: reactance).

capacitors). Another useful concept of power is complex power (S) which is defined by P+jQ. In phasor domain, complex power is noted as below.

$$S = \frac{1}{2} V \cdot I^* = \frac{V_m I_m}{2} \cos(\theta) + j \frac{V_m I_m}{2} \sin(\theta). \tag{A.4}$$

For example, Figure A-1 presents voltage and current flowing the load impedance. In this scenario, the power consumed in the resistor and power stored in reactive components are noted as

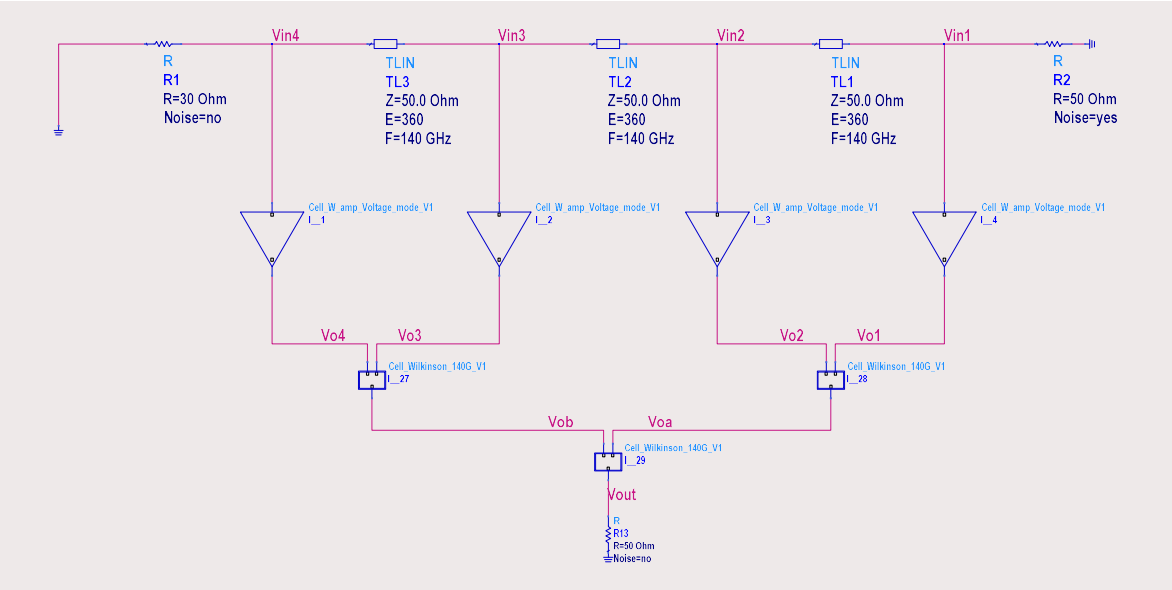
$$\begin{aligned} P &= \frac{1}{2} |I|^2 R = \frac{1}{2} \frac{|V_R|^2}{R} \\ Q &= \frac{1}{2} |I|^2 X = \frac{1}{2} \frac{|V_X|^2}{X} \end{aligned}. \tag{A.5}$$

Reference

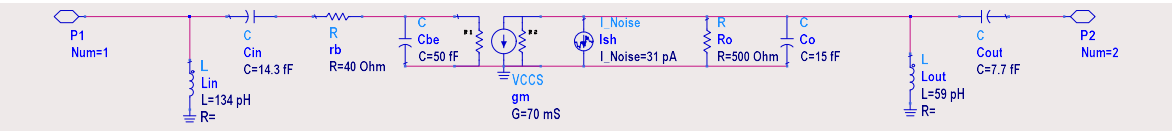
[A-1] James W. Nillson, Electric circuits, Prentice Hall, 2005.

Appendix B.

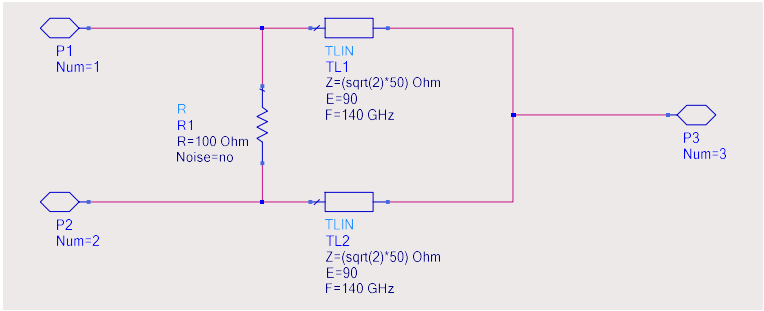
A Verification of Noise Analysis by Simulation Tool, ADS in Chapter 4



(a)



(b)



(c)

Fig. B-1. (a) noise model in 4-tap FIR filters with a scaled Zo delay line, (b) noise model of W-amps and (c) noiseless Wilkinson power amplifier.

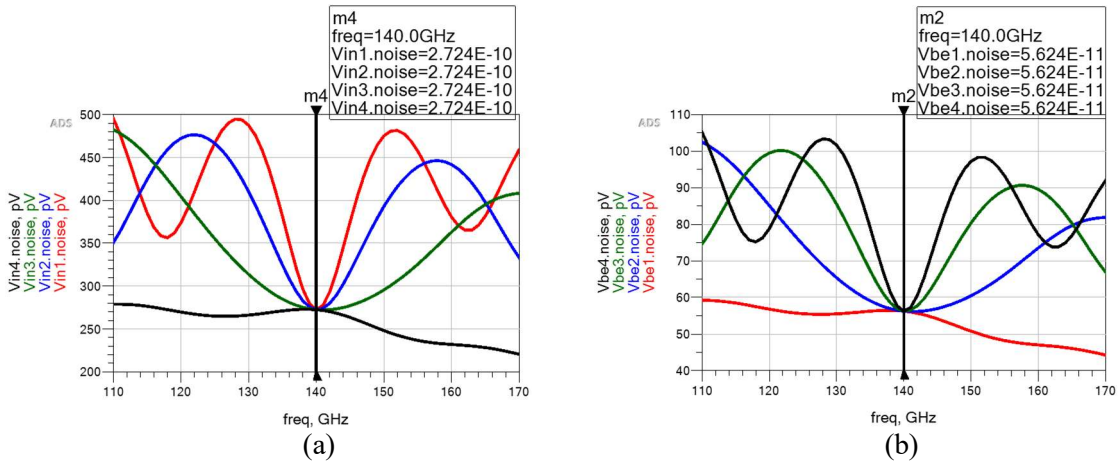
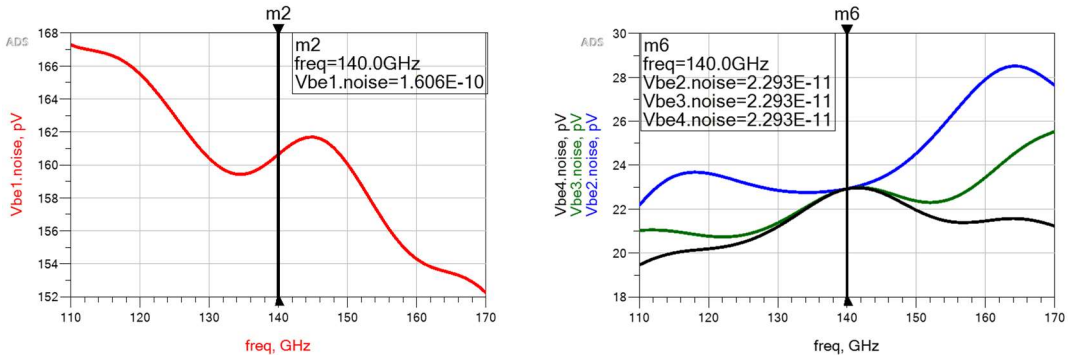


Fig. B-2. Simulation result: noise developed at (a) each tap in the delay-line and (b) each C_{be} of W-amps only due to the noise source of the terminated resistor, Zo.

It is worthwhile to verify the noise of N-tap filter calculated in Ch.4. The simulation tool, ADS is used to verify the quantitative analysis of noise. Unlike the signal analysis, the noise analysis should be done, considering the correlation between noises carefully [B In this simulation, 4-tap FIR filter is designed to analyze the noise characteristics. For the FIR filter with constant Zo delay lines, all T-line is modelled as Z_o of 50 Ω, electrical length, θ=2π at 140 GHz. In W-amp in Fig. B-1(b), L_{in}=134 pH, C_{in}=14.3 fF for the input matching and r_b=40 Ω, C_{be}=50 fF, g_m=70 mS, R_o=500 Ω, C_o=15 fF for effective intrinsic device. For the output matching, L_{out}=59 pH, C_{out}=7.7 fF are set to 50 Ω conjugate matching. Fig. B-1(c) shows ideal noiseless and lossless Wilkinson power combiner working at 140 GHz centered. First, set the terminated resistor, Zo at the end of delay line as only noise source to determine the noise voltage developed at each voltage across base-emitter capacitor of W-amps, $\overline{V_{n,be(Z_O)}^2}$. According to the eq. 4-11, the noise voltage loaded at each tap in the delay line is



(a) (b)

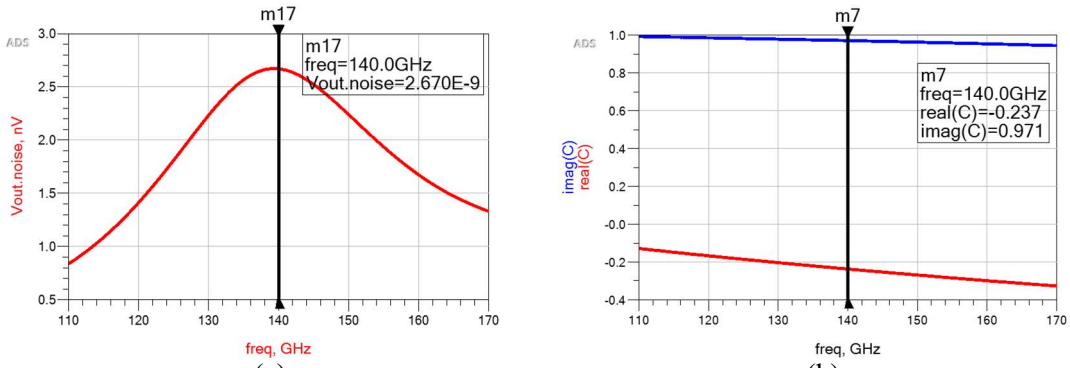
Fig. B-3. Simulation noise developed at C_{be} of W-amps only due to the noise source of a base resistor, (a) $\overline{V_{n,be(1)}^2}$ and (b) $\overline{V_{n,be(2)}^2}$.

$$\begin{aligned}\overline{V_{n,in1}} = \overline{V_{n,in2}} = \cdots = \overline{V_{n,in(N)}} = \overline{V_{n,Z_O}}\left(\frac{M}{2(M+N)}\right) \\ = \sqrt{4kTZ_o}\left(\frac{M}{2(M+N)}\right) = 0.89n\left(\frac{6}{2(6+4)}\right) = 0.27nV\end{aligned} \tag{B.1}$$

Its calculation is well matched with simulation result in Fig. B-2(a). Then, the noise voltage developed at each C_{be} of W-amp with eq. 4-12 as

$$\begin{aligned}\overline{V_{n,be(Z_O)}} = \overline{V_{n,Z_O}}\left(\frac{M}{2(M+N)}\right)\left|\frac{C_{in}}{C_{in}+C_{be}}\frac{1}{1+s(C_{in}\,\|\,C_{be})r_b}\right| \\ = 0.89n\left(\frac{6}{2(6+4)}\right)\left|\frac{14.3}{14.3+50}\frac{1}{1+j(2\pi 140G)(14.3\,\|\,50)f40}\right| = 0.056nV\end{aligned} \tag{B.2}$$

This value is also well matched in simulation result in Fig. B-2(b). Another noise source to develop the noise voltage at C_{be} of each W-amp is base resistor noise, $\overline{V_{n,rb}^2}$. In this case, let's set the noise source from the only one base resistor, r_b at W-amplifier. It affects the noise voltage to $\overline{V_{n,be(1)}^2}$ and $\overline{V_{n,be(2)}^2}$. With eq. 4-13, 16,



(a) (b)

Fig. B-4. (a) output noise voltage at the 4-tap FIR filter and (b) correlation coefficient, C.

$$\overline{V_{n,be(1)}} = \overline{V_{n,rb}} \left| \frac{1}{(Z_b + Z_m)} \cdot \frac{1}{sC_{be}} \right|$$

$$= 0.81n \left| \frac{1}{\left(40 - j\frac{1}{(2\pi 140G)\cdot 50f}\right) + \left(15.8 \,\|\, \left(j(2\pi 140G)\cdot 134p\right) - j\frac{1}{(2\pi 140G)\cdot 14.3f}\right)} \cdot \frac{-j}{(2\pi 140G)\cdot 50f} \right| \quad \text{(B.3)}$$

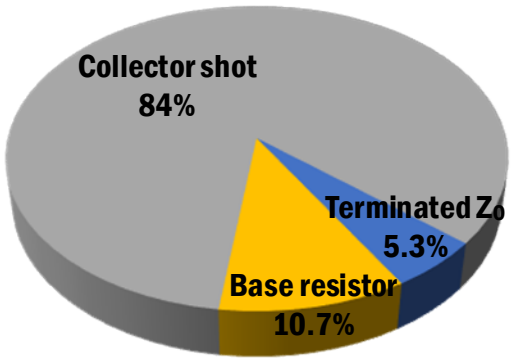
$$= 0.16nV = 16\cdot 10^{-11} V$$

$$\overline{V_{n,be(2)}} = \overline{V_{n,rb}} \cdot \left| \frac{-Z_T}{Z_b + Z_m} \cdot \frac{sL_{in}}{Z_T + sL_{in}} \right| \cdot \left| \frac{C_{in}}{C_{in} + C_{be}} \frac{1}{1 + s(C_{in} \,\|\, C_{be}) r_b} \right|$$

$$= 0.81n \cdot \left| \frac{-15.8}{\left(40 - j\frac{1}{(2\pi 140G)\cdot 50f}\right) + \left(15.8 \,\|\, \left(j(2\pi 140G)\cdot 134p\right) - j\frac{1}{(2\pi 140G)\cdot 14.3f}\right)} \cdot \frac{j(2\pi 140G)\cdot 134p}{15.8 + j(2\pi 140G)\cdot 134p} \right| . \quad \text{(B.4)}$$

$$\cdot \left| \frac{14.3}{14.3 + 50} \cdot \frac{1}{1 + j(2\pi 140G)\cdot (14.3 \,\|\, 50) f \cdot 40} \right| = 2.29\cdot 10^{-11} V$$

The calculated values of $\overline{V_{n,be(1)}^2}$ and $\overline{V_{n,be(2)}^2}$ at 140 GHz are 16×10^{-11} V and 2.29 $\times 10^{-11}$V, respectively. These two calculated values are well matched to the simulation result in Fig. B-3(a), (b). With the effective noise voltage at C_{be}, the output noise voltage based on eq. 4-19 can be calculated. While in calculation, it is critical to figure out the correlation coefficient, C as defined in eq. 4-20.



	$V^2_{n,out}$ (V^2)
$I_{n,shot}$	$6.0e^{-18}$
r_b	$0.77e^{-18}$
Z_o	$0.38e^{-18}$
total	$7.15e^{-18}$

Fig. B-5. Output noise contribution from each noise sources.

$$C=\frac{\overline{V_{n,be(1)}V^{*}_{n,be(2)}}}{\sqrt{V^2_{n,be(1)}V^2_{n,be(2)}}}=\frac{\left(\frac{1}{(Z_b+Z_m)}\frac{1}{sC_{be}}\right)\left(\frac{-Z_T}{Z_b+Z_m}\frac{sL_{in}}{Z_T+sL_{in}}\frac{C_{in}}{(C_{in}+C_{be})}\frac{1}{1+s(C_{in}\|C_{be})r_b}\right)^{*}}{\sqrt{\left|\frac{1}{(Z_b+Z_m)}\frac{1}{sC_{be}}\right|^2\left|\frac{-Z_T}{Z_b+Z_m}\frac{sL_{in}}{Z_T+sL_{in}}\frac{C_{in}}{(C_{in}+C_{be})}\frac{1}{1+s(C_{in}\|C_{be})r_b}\right|^2}} \quad \text{(B.5)}$$

$$=\frac{(0.174-j0.096)\cdot(-0.019-j0.021)^{*}}{0.199\cdot 0.028}=-0.237+j0.971$$

Finally, the output noise voltage, $\overline{V_{n,out}}$ can be calculated with this correlation coefficient, C, as

$$\overline{V_{n,out}}$$

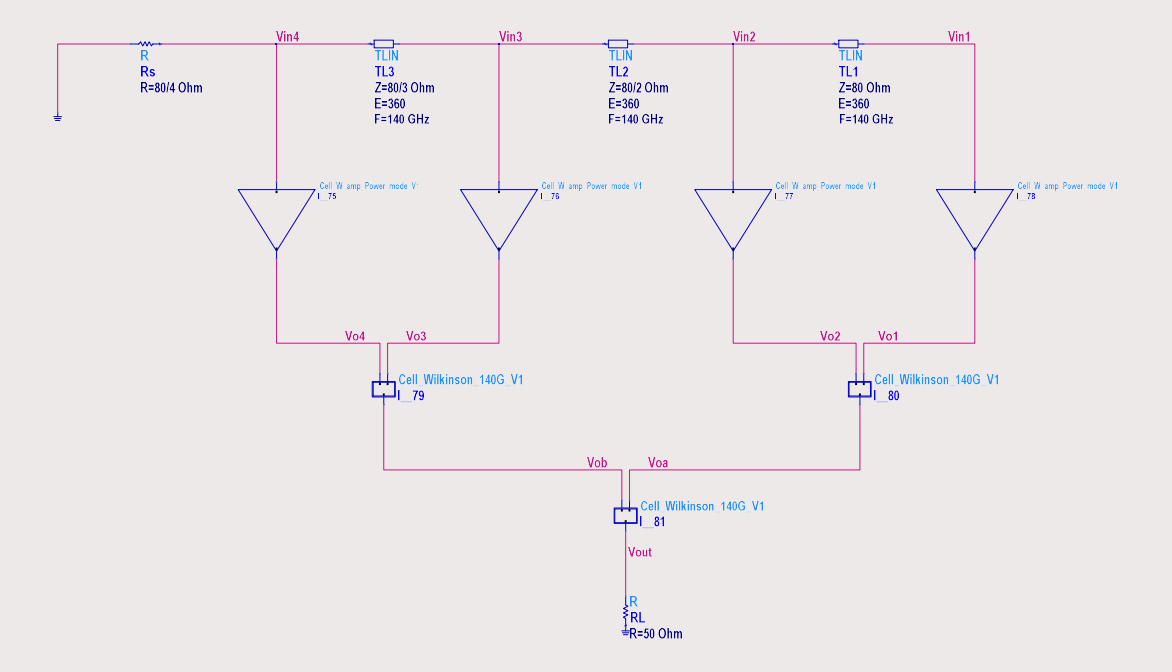
$$=\sqrt{\frac{R_O Z_O}{4}\left(g_m^2\left(\left(\frac{\overline{V_{n,be(Z_O)}}}{\sqrt{N}}\right)^2N^2+\left(\frac{V_{n,be(1)}}{\sqrt{N}}+\frac{V_{n,be(2)}}{\sqrt{N}}(N-1)\right)^2N\right)+\left(\frac{\overline{I_{n,sh}}}{\sqrt{N}}\right)^2N\right)}$$

$$=\sqrt{\frac{R_O Z_O}{4}\left(g_m^2\left(\overline{V^2_{n,be(Z_O)}}N+\overline{V^2_{n,be(1)}}+(N-1)^2\overline{V^2_{n,be(2)}}+(N-1)(C+C^{*})\sqrt{\overline{V^2_{n,be(1)}V^2_{n,be(2)}}}\right)+\overline{I^2_{n,sh}}\right)} \quad \text{(B.6)}$$

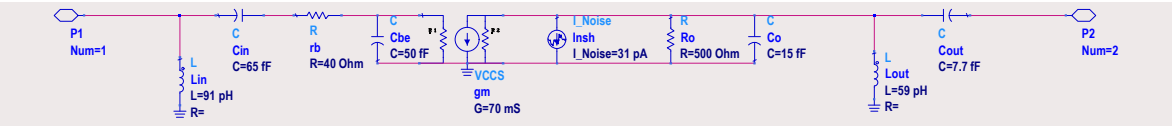
$$=\sqrt{\frac{500\cdot 50}{4}\left(0.07^2\left(4\cdot(0.56n)^2+(0.16n)^2+9\cdot(22.9p)^2+3\cdot(-0.474)\cdot(0.16n\cdot 22.9p)\right)+(31p)^2\right)}$$

$$=2.68nV$$

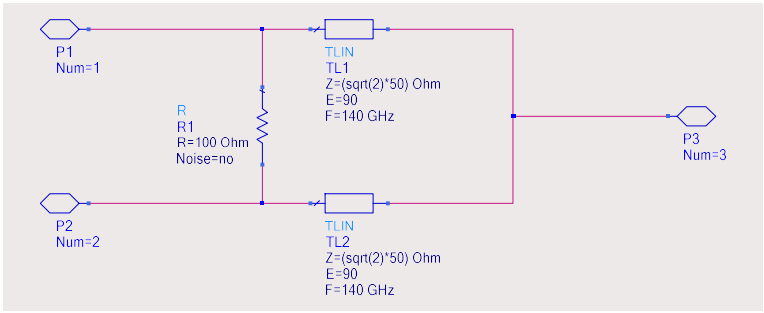
Fig. B-5 shows the noise contribution and the output noise voltage to the total output noise voltage from each noise sources. The output noise voltages from the Zo, r_b and shot collector



(a)



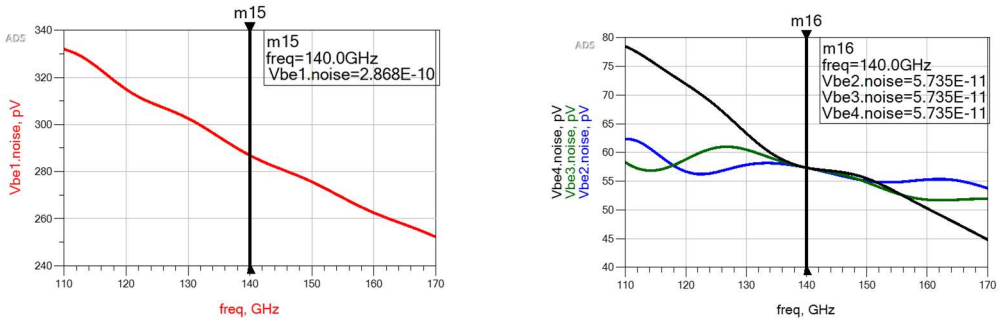
(b)



(c)

Fig. B-6. (a) noise model in 4-tap FIR filters with a scaled Zo delay line and (b) noise model of W-amps and noiseless/lossless Wilkinson power combiner.

noise are $0.38 \times 10^{-18}V^2$, $0.77 \times 10^{-18}V^2$ and $6.0 \times 10^{-18}V^2$, respectively. The collector shot noise is dominant noise source to the output voltage contributed 84% of total noise.

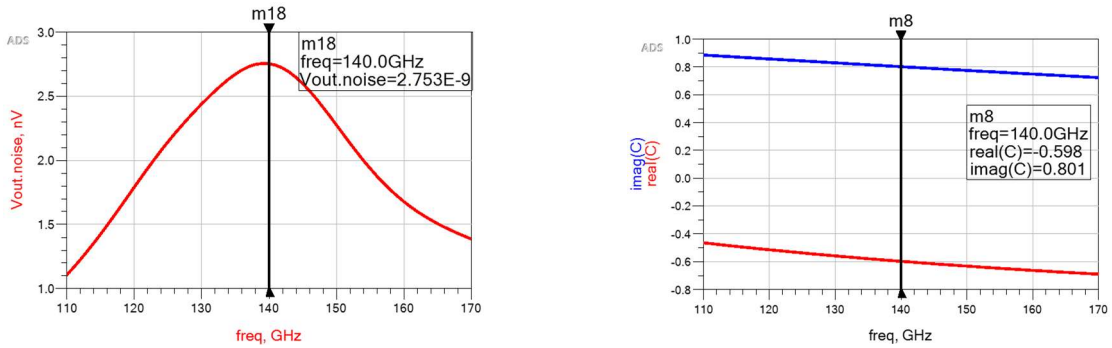


(a) (b)

Fig. B-7. Simulation noise developed at C_{be} of W-amps only due to the noise source of a base resistor, (a) $\overline{V_{n,be(1)}^2}$ and (b) $\overline{V_{n,be(2)}^2}$.

Next, the quantitative noise analysis of 4-tap FIR filter with a scaled Zo delay line can be performed with similar way so far. For delay line with scaled Zo, T-lines are modelled as Zo of 80, 40, 26.7 and 20 Ω from the rightmost end of line to the source and an electrical length of each T-line is θ=2π at 140 GHz. In W-amp at Fig. B-6(b), components value is set that L_{in}=91 pH, C_{in}=65 fF for input matching and r_b=40 Ω, C_{be}=50 fF, g_m=70 mS, R_o=500 Ω, C_o=15 fF for effective intrinsic device. For the output matching, L_{out}=59 pH, C_{out}=7.7 fF are set. Fig. B-6(c) shows ideal lossless and noiseless Wilkinson power combiner at 140 GHz. In this case, there is no noise source from the terminated resistor of delay line. Therefore, the first noise source is the base resistor of each W-amp, $\overline{V_{n,rb}^2}$. It affects the noise voltage to $\overline{V_{n,be(1)}^2}$ and $\overline{V_{n,be(2)}^2}$. With eq. 4-13, 16,

$$\begin{aligned}\overline{V_{n,be(1)}} &= \overline{V_{n,rb}}\left|\frac{1}{(Z_b+Z_m)}\cdot\frac{1}{sC_{be}}\right| \\ &= 0.81n\left|\frac{1}{\left(40-j\frac{1}{(2\pi 140G)\cdot 50f}\right)+\left(11.4\,\|\left(j(2\pi 140G)\cdot 91p\right)-j\frac{1}{(2\pi 140G)\cdot 65f}\right)}\cdot\frac{-j}{(2\pi 140G)\cdot 50f}\right| \\ &= 0.29nV\end{aligned} \tag{B.7}$$



(a) (b)

Fig. B-8. (a) output noise voltage at the 4-tap FIR filter and (b) correlation coefficient, C.

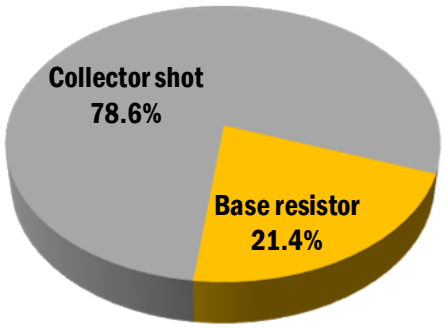
$$\overline{V_{n,be(2)}} = \overline{V_{n,rb}} \cdot \left| \frac{-Z_T}{Z_b + Z_m} \cdot \frac{sL_{in}}{Z_T + sL_{in}} \right| \cdot \left| \frac{C_{in}}{C_{in} + C_{be}} \frac{1}{1 + s(C_{in} \parallel C_{be}) r_b} \right|$$

$$= 0.81n \cdot \left| \frac{-11.4}{\left(40 - j\frac{1}{(2\pi 140G)\cdot 50f}\right) + \left(11.4 \parallel \left(j(2\pi 140G)\cdot 91p\right) - j\frac{1}{(2\pi 140G)\cdot 65f}\right)} \cdot \frac{j(2\pi 140G)\cdot 91p}{11.4 + j(2\pi 140G)\cdot 91p} \right| \cdot \left| \frac{65}{65+50} \cdot \frac{1}{1 + j(2\pi 140G)\cdot(65 \parallel 50) f \cdot 40} \right| = 5.7 \cdot 10^{-11} V \quad \text{(B.8)}$$

Transfer function is same with two different delay lines, but only difference is components value for input matching and delay line. According to eq. B.7,8, the calculated values of $\overline{V_{n,be(1)}^2}$ and $\overline{V_{n,be(2)}^2}$ At 140 GHz are 29.0×10^{-11}V and 5.7×10^{-11}V, respectively. These two calculated values are well matched to the simulation result in Fig. B-7(a), (b). With the effective noise voltage at Cbe, the output noise voltage is expressed as

$$\overline{V_{n,out}} = \sqrt{\frac{R_O Z_O}{4}\left(g_m^2 \left(\frac{V_{n,be(1)}}{\sqrt{N}} + \frac{V_{n,be(2)}}{\sqrt{N}}(N-1) \right)^2 N + \left(\frac{\overline{I_{n,sh}}}{\sqrt{N}} \right)^2 N \right)}. \quad \text{(B.9)}$$

Before calculating this value, the correlation coefficient, C defined at eq. 4.20 should be calculated



	$V^2_{n,out}$ (V^2)
$I_{n,shot}$	5.96e-18
r_b	1.62e-18
total	7.58e-18

Fig. B-9. Output noise voltage at the FIR filter and (b) correlation coefficient, C by simulation.

$$C = \frac{\overline{V_{n,be(1)} V^*_{n,be(2)}}}{\sqrt{V^2_{n,be(1)} V^2_{n,be(2)}}} = \frac{\left(\frac{1}{(Z_b+Z_m)}\frac{1}{sC_{be}}\right)\left(\frac{-Z_T}{Z_b+Z_m}\frac{sL_{in}}{Z_T+sL_{in}}\frac{C_{in}}{(C_{in}+C_{be})}\frac{1}{1+s(C_{in}\|C_{be})r_b}\right)^*}{\sqrt{\left|\frac{1}{(Z_b+Z_m)}\frac{1}{sC_{be}}\right|^2\left|\frac{-Z_T}{Z_b+Z_m}\frac{sL_{in}}{Z_T+sL_{in}}\frac{C_{in}}{(C_{in}+C_{be})}\frac{1}{1+s(C_{in}\|C_{be})r_b}\right|^2}} \quad \text{(B.10)}$$

$$= \frac{(0.214 - j0.283)\cdot(-0.071)^*}{0.355\cdot 0.071} = -0.598 + j0.801$$

C is -0.598+j0.801 at 140 GHz, which can be useful to complete the output noise voltage. Finally, the output noise voltage, $\overline{V_{n,out}}$ can be calculated as below.

$$\begin{aligned}
&\overline{V_{n,out}} \\
&= \sqrt{\frac{R_O Z_O}{4}\left(g_m^2\left(\frac{V_{n,be(1)}}{\sqrt{N}} + \frac{V_{n,be(2)}}{\sqrt{N}}(N-1)\right)^2 N + \left(\frac{I_{n,sh}}{\sqrt{N}}\right)^2 N\right)} \\
&= \sqrt{\frac{R_O Z_O}{4}\left(g_m^2\left(\overline{V^2_{n,be(1)}} + (N-1)^2\overline{V^2_{n,be(2)}} + (N-1)(C+C^*)\sqrt{\overline{V^2_{n,be(1)}}\,\overline{V^2_{n,be(2)}}}\right) + \overline{I^2_{n,sh}}\right)} \\
&= \sqrt{\frac{500\cdot 50}{4}\left(0.07^2\left((0.29n)^2 + 9\cdot(57p)^2 + 3\cdot(-1.196)\cdot(0.29n\cdot 57p)\right) + (31p)^2\right)} \\
&= 2.76nV
\end{aligned} \quad \text{(B.11)}$$

This value (=2.76 nV) is also well matched with simulation result in Fig. B-8(a). Fig. B-9 shows the noise contribution and the output noise voltage to the total output noise voltage from each noise sources. The output noise voltages from the base resistor (r_b) and shot

collector noise are $1.62 \times 10^{-18} V^2$, $5.96 \times 10^{-18} V^2$, respectively. The collector shot noise is dominant noise source to the output voltage contributed 78.6% out of total output noise voltage.

Reference

[B-1] Behzad Razavi, RF microelectronics, Prentice Hall, 2011.