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# CONTROLLED ON-TIME POWER FACTOR CORRECTION CIRCUIT WITH INPUT FILTER

by

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Thesis submitted to the Faculty of the

Virginia Polytechnic Institute and State University

in partial fulfillment of the requirements for the degree of

Master of Science

in

Electrical Engineering

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May, 1990

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(ABSTRACT)

An active power factor correction circuit with controlled on-time is proposed. The circuit has a simpler control scheme than the power factor correction circuit with hysteresis control, and yet is able to attain high power factor. A very important aspect of this work was the formulation of the design guidelines for the input filter for the power factor correction circuit. Conventional methods of filter design may introduce an unwanted phase shift between the input voltage and current, thereby degrading the power factor. The cause of this phase shift is explained and based upon it, the design guidelines for the input filter are established . The FFT is used to more accurately define the input filter attenuation requirement. A comparision is made between power factor correction circuit with controlled on-time and the power factor correction circuit with hysteresis control (with input filter for both of them) on the basis of their minimum weight. A regulated 100 W, 120 VAC input and 300 V output power factor correction circuit was implemented on a breadboard. Ridley's small signal switch model [10] for the power factor correction circuit with hysteresis control is successfully applied to this control scheme to close the loop.

# Acknowledgements

I wish to express my sincere appreciation to my advisor Dr. Fred. C. Lee for his encouragement and support during the course of my research work and also for the opportunity to work in the area of power electronics. I wish to thank Dr. B.H. Cho and Dr. V. Vorperian for their contribution as members of my committee.

My deepest thanks go to Mr. Ray Ridley for his unlimited advice and supervision of this work. Special thanks are also extended to Mr. Richard Gean for his assistance during the hardware implementation of the circuit. I would also like to express my thanks to my fellow students in the VPEC for their friendship and help.

I wish to thank my wife Naobahar for her help, understanding and patience during the course of my study at VPEC. I thank my daughters Nabila and Maliha for their sacrifice, which at present, they may not comprehend.

A special thanks to my brother-in-law Mohammad A. Alam for his keen interest in my career. His support has made it possible for me to complete my studies at Virginia Tech.

Finally, I wish to thank my parents Dr. and Mrs. Faziruddin Ahmed for their encouragement and guidance throughout my life.

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# Chapter 1. INTRODUCTION AND OVERVIEW

## *1.1 Introduction*

The issue of active power factor correction of switched mode power converters has gained considerable attention recently. This is due to the continuously increasing use of solid state power converters which have a low power factor, and to an ever increasing concern for the efficient utilization of energy provided by the utility power distribution network. The quality of the power supplied (low distortion, low harmonic content) is also very important to equipment such as computers and communication devices.

The strongest incentive for using power factor correction is that it is being made mandatory by regulatory agencies. IEEE Standard 519 is being revised and updated to a "Recommended Practice." The maximum harmonic content fed into the utility at the point of common connection is related to the ratio of the load current to short circuit current. For a low ratio of 20, for example, the

maximum allowable third harmonic is 4%. A more difficult standard is IEC 555.2. This document has been advisory in past years, but at a recent CBEMA (Computer and Business Machine Manufacturers' Association) meeting, it was reported that Austria had begun to enforce the standard. West Germany and many countries from England to Australia will follow suit. IEC 555.2 allows a maximum third harmonic of 2.3 A with decreasing limits for higher harmonics. These limits will become more stringent when a new revision (77A) is accepted [18].

Active power factor correction circuits can increase the power factor of the switched mode power supplies (SMPS) from 0.65 to between 0.95 to 0.99 and reduce the harmonic distortion to less than 5% for a 0.99 power factor [1]. In addition, the added cost of incorporating the power factor circuit in the power supply is partially offset by some additional benefits [2] such as:

- tapless/switchless operation over the full 90-270 V line voltage range. The power factor correction circuit can be configured to preregulate for this input range. The input voltage range switch of the conventional SMPS considered to be the greatest single source of failure [5] can thus be avoided.
- reduction of the size of the output capacitor.
- regulated d.c. output makes the design of the downstream dc-to-dc converter simpler.

## *1.2 Power Factor Concept For Switched Mode Power Supplies*

Power factor can be defined as the ratio of the input power in watts to the product of rms input voltage and rms input current measured with an rms voltmeter and ammeter:

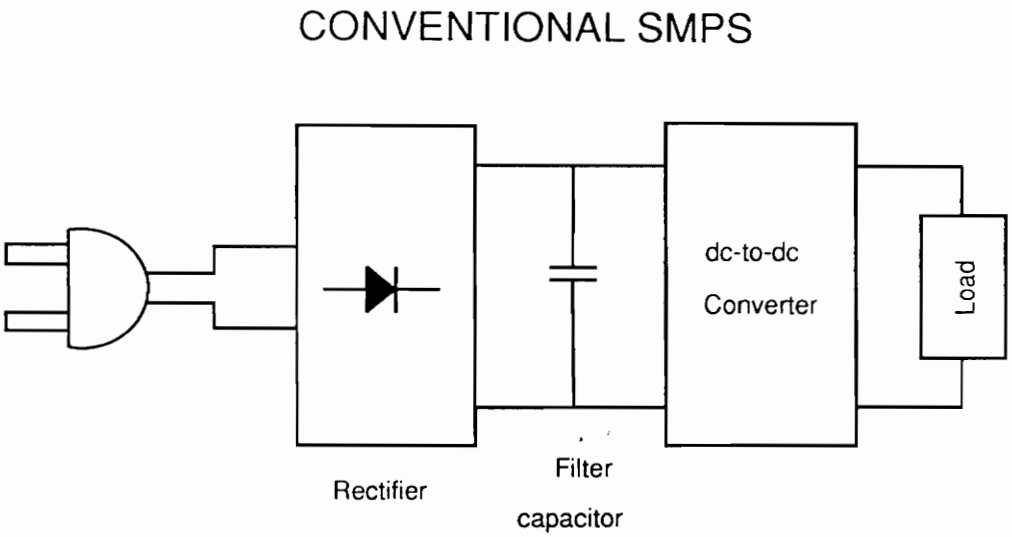
$$Power\ Factor = \frac{True\ Input\ Power\ in\ Watts}{(rms\ volt)(rms\ ampere)}.$$

For sinusoidal input voltage and input current, the current will lead or lag the voltage by angle $\theta$, depending upon the nature of the reactive load. In this case the power factor can be simply expressed as:

$$Power\ factor = \cos\theta.$$

However, this traditional concept of the power factor, using phase shift between the current and the voltage, is not applicable to a switched mode power supply. In an off-line SMPS with a bulk input filter, the low power factor (typically lower than 0.65), is not due to the current and voltage being out of phase, but is due to the current with high harmonic contents.

Off-line switched mode power supplies usually employ an uncontrolled bridge rectifier with a bulk input filter capacitor. The block diagram of an SMPS and its associated waveforms are shown in Fig 1.1. The bulk capacitor smooths the rectified voltage to the desired ripple and also provides the holdup requirement



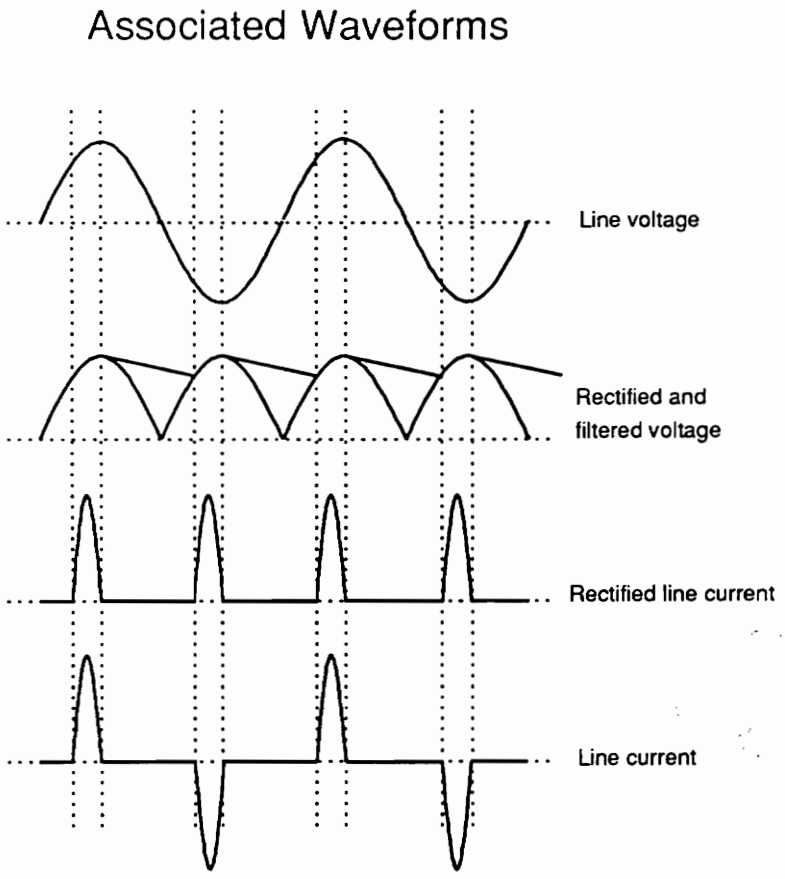




Fig 1.1 Block diagram of conventional SMPS

in case of a brief line failure. This input capacitor is the cause of the low power factor. It draws current from the line during relatively short periods. These narrow current pulses with high peaks cause a low power factor, high RMS current, and they are very rich in harmonics.

High harmonic content does not necessarily imply a low power factor [2]. If the fundamental and all harmonics of the current are in phase with the corresponding harmonics of the voltage, then the power factor will be unity. In SMPSs, the input voltage is sinusoid, but the current is rich in harmonics, this explains the low power factor.

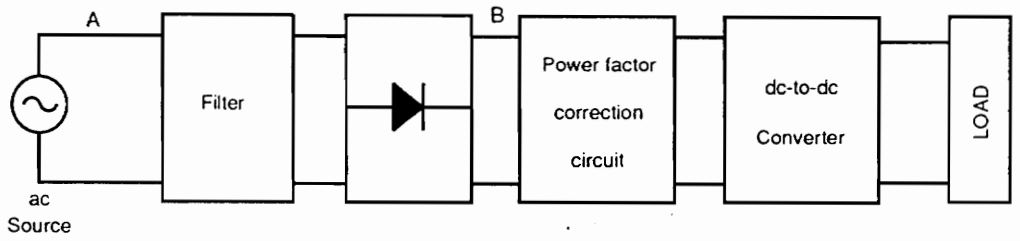
Power factor correction can be broadly divided into two methods:

- passive power factor correction, and
- active power factor correction.

Passive power factor correction uses only passive components such as inductors and capacitors which work at line frequency. Since line frequencies are in the range of 47 to 440 Hz, the components are much larger than those used in the active method. This makes the passive method not feasible where there is an effort to reduce the size and cost.

In the active method, the power factor correction circuit is inserted in front of the switched mode power supply (Fig. 1.2.). This power factor correction circuit synthesizes the input current so that the average input current is also sinusoidal and is in phase with the input voltage. An input filter is required to filter the high frequency current ripple going back to the source and also to meet

# SMPS WITH POWER FACTOR CORRECTION CIRCUIT




## Associated Waveforms

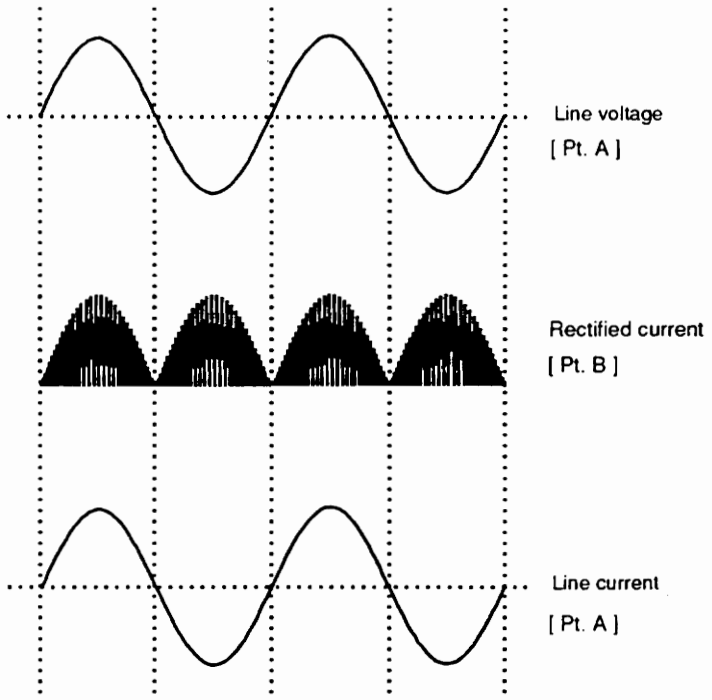



Fig 1.2 SMPS with power factor circuit

the EMI regulatory specification. With the active method, the filter components are small when high switching frequency is employed, and the power factor can be made almost unity.

## *1.3 Objective of This Study*

The objective of this study was to find an active power factor correction circuit which has a simpler control scheme than the power factor correction circuit with hysteresis control, and yet is able to attain high power factor. With this objective, an active power factor correction circuit with controlled on-time was analyzed and implemented on hardware. The power factor attained with an input filter was almost unity.

Another major objective was the formulation of the design guidelines for the input filter for the power factor correction circuit. It was shown that the conventional method of input filter design may introduce an unwanted phase shift between the input voltage and the input current, thereby degrading the power factor. The cause of this phase shift was explained, and design guidelines for the input filter to avoid this phase shift were established. These design guidelines are also applicable to power factor correction circuit with hysteresis control.

Another objective was to make a quantitative comparision between this power factor correction circuit and one with hysteresis control to determine which is suitable at a given power level.

# CHAPTER 2. ANALYSIS OF A POWER FACTOR CORRECTION CIRCUIT WITH CONTROLLED ON-TIME

## *2.1 Introduction And Motivation For This Control Method*

Active power factor correction can have various power stage configurations [2]. These are buck, boost, and buck boost. Also, several different control laws can be implemented for the power factor correction circuit for active shaping of the input current. These are:

- constant switching frequency control [16,17],
- hysteresis control [3,16],
- on-time control [16], and

- off-time control [16]

The last three methods have variable switching frequencies. All methods have advantages and disadvantages [3,16,17]. The choice of control method depends upon power level, complexity, cost, and designer's preference. The hysteresis control with variable frequency has the following advantages [3]:

- Inductor current follows exactly the line voltage, achieving high power factor and minimal harmonic current.
- Minimal current stress on the the transistor when the inductor current operates in continuous conduction mode.
- No external ramp compensation required, as in the constant frequency control.

Some disadvantages of this control are:

- Current sense. A resistor is inserted in series with the boost inductor, since both the peak and valley inductor current information are required. Care must be taken to reduce the noise in the sensed current.
- Circuit operates with variable frequency. Therefore, the recently introduced ICs dedicted for power factor correction cannot be used to implement this control.

The constant frequency control has the following advantages:

- Current sense. Only the peak inductor current information is required. A current transformer inserted in series with the transistor is sufficient.
- Constant frequency operation. Recently introduced ICs for power factor correction can be used to implement this control scheme.
- Minimal current stress on the transistor when operates in continuous conduction mode.

The disadvantages are:

- External ramp compensation is required for stability considerations for constant frequency control with greater than 50 % duty cycle.
- Only the peak inductor current exactly follows the line voltage. The average inductor current is distorted at the begining and end of the half line cycle.

Recently a number of ICs specifically designed for power factor correction have been introduced by different manufacturers. These are ML4812 by Micro Linear Corp, UC1854/UC2854/UC3854 by Unitrode, TDA4819A and TDA4814A by Siemens. CS320 and CS321 by Cherry Semiconductors Corporation can be used to implement hysteric, constant off time, and fixed frequency current mode controls. CS320 can be configured to implement the hysteric control for power factor correction.

ML4812 by Micro Linear is designed to implement a boost type power factor correction with fixed frequency, peak current mode control [20,21]. The inductor current is monitered with a current sense transformer in series with the MOSFET

to get a proportional voltage. When the voltage proportional to the sensed current is greater than the reference sinewave (produced by the multiplier output) the MOSFET is turned off. The MOSFET is subsequently turned on when the next fixed frequency clock occurs. The output of the multiplier is basically an attenuated replica of the input sine wave from the bridge rectifier multiplied by the dc output of the error amplifier. As with any peak current feedback control with fixed frequency, slope compensation for duty cycle above 50% is required.

The UC1854 family is designed to implement a fixed frequency, average current mode method for configuring a boost converter to control input current [18]. There is a voltage loop which accomplishes the regulation of the preregulator's output voltage. It includes a voltage error amplifier and a multiplier. The multiplier is used to combine the AC input voltage waveform and the output of the voltage error amplifier. The output of the multiplier determines the input current instantaneously in order to follow the AC voltage, but with an average level to maintain the output regulation. There is a seperate current loop. The multiplier provides a current output into the summing junction of the current amplifier. This amplifier then controls the PWM to achieve the fixed frequency average current mode control. This method of control does not require slope compensation.

TDA4814A and TDA4819A is designed to configure a boost converter to operate at the boundary of CCM and DCM for the implementation of power factor correction [19]. A detector winding is located in the power stage inductor to turn on the MOSFET. The input current is sensed with a resistor and is

compared with the multiple of the scaled input voltage and the output of the voltage error amplifier. The MOSFET is turned off when the scaled sensed inductor current is greater than the output of the error amplifier. This control is similar to the controlled on-time in the sense that in both, the boost converter works at the boundary of CCM and DCM but this scheme also requires the current to be sensed by a resistor.

It can be seen that each IC has its own strategy of implementation of the power factor correction control. Each has its own advantage and disadvantage. In this thesis an active power factor correction circuit with a controlled on-time is proposed. It has a simpler control, and yet is able to attain high power factor. Very simply, this control scheme can be described as follows: For steady state operation, the on-time of the switch is constant. The inductor current ramps up during this on-time. At the end of the on-time, the switch is turned off, and the inductor current is allowed to ramp down to zero. The switch is turned on again as soon as the inductor current reaches zero. This way the converter is forced to work at the boundary of continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The average output voltage is controlled by varying the on-time of the switch. The control voltage (output of the error amplifier) is considered a slow varying signal compared to the line voltage, therefore the on-time can be considered constant over a rectified line cycle. The 120 Hz ripple of the output voltage is removed from the control voltage using a notch filter. In the hysteresis control method, the inductor current is forced to switch between the upper and the lower references. The variable hysterisis control has been exten-

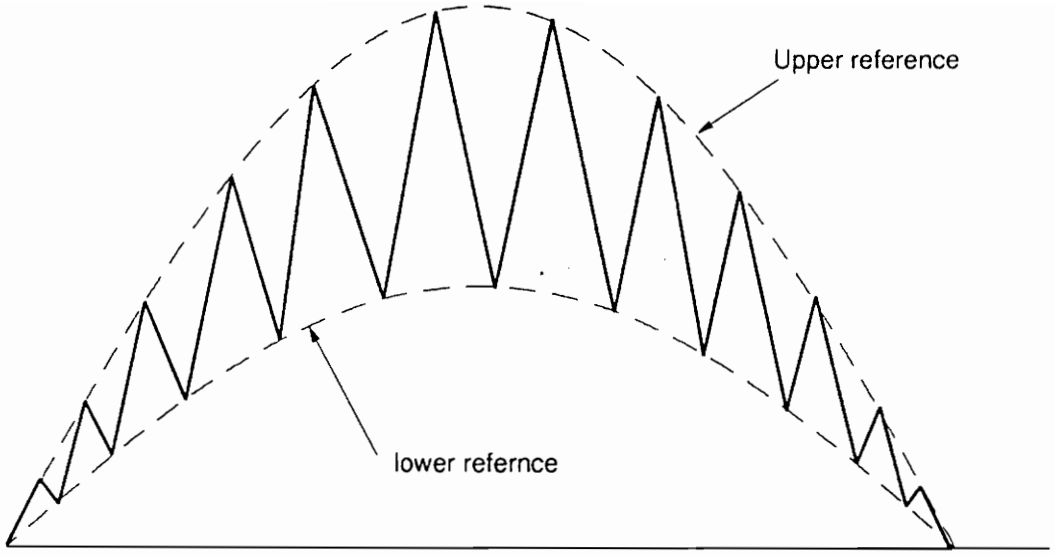



Fig. 2.1a Inductor current for hysteresis control

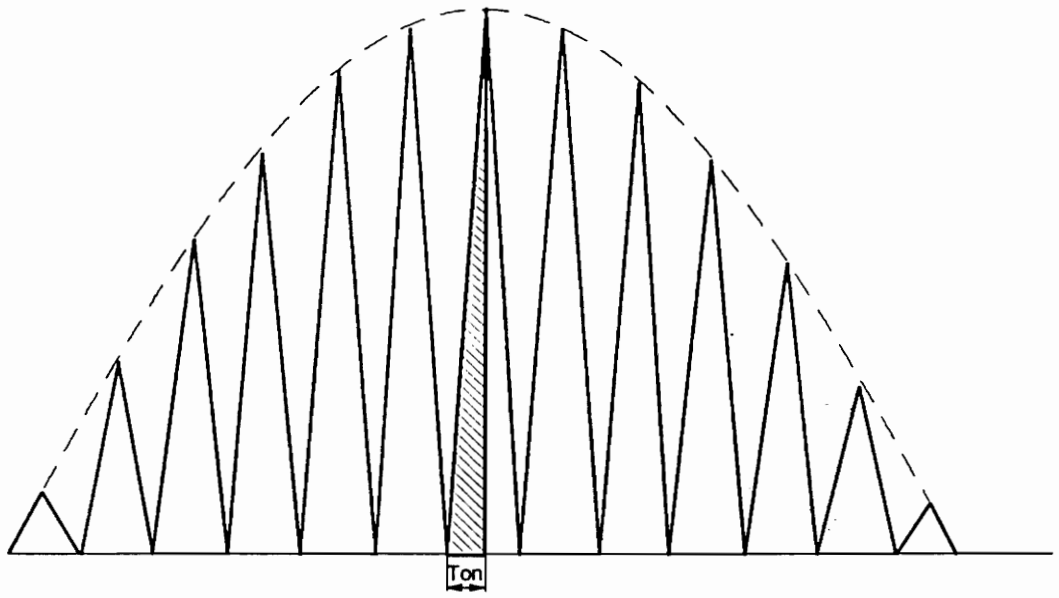



Fig. 2.1b Inductor current for on-time control

sively analyzed by C. Zhou in [3]. The inductor currents for the hysteresis control and the controlled on-time control are shown in Fig. 2.1.a and 2.1.b, respectively. The idea of this control scheme was inspired by hysteresis control. Following are some of the motivations which prompted the investigation of this method of control:

- The on-time is essentially constant in the hysteresis control over most of the rectified line period [3]. During the analysis of the hysteresis control, it was observed that, although the switching frequency is variable over a rectified line cycle (maximum at the begining and at the end of the rectified line cycle), the on-time of the switch did not change by much during the major portion of the line cycle. (This is shown in Fig. 2.2.) This observation motivated study of a control scheme with on-time constant over the rectified line cycle.

- Simplification of the control is achieved in two ways:

  1. simplification of current sensing, and

  2. exclusion of the multiplier.

  In hysteresis control the current is sensed with a small resistance in series with the inductor. As this resistance is in the path of the main power flow, it has to be very small to reduce losses. Therefore the sensed signal needs to be amplified. The rectified input voltage also needs to be sensed with a set of voltage dividers. The sensed rectified line voltage is then scaled to define the

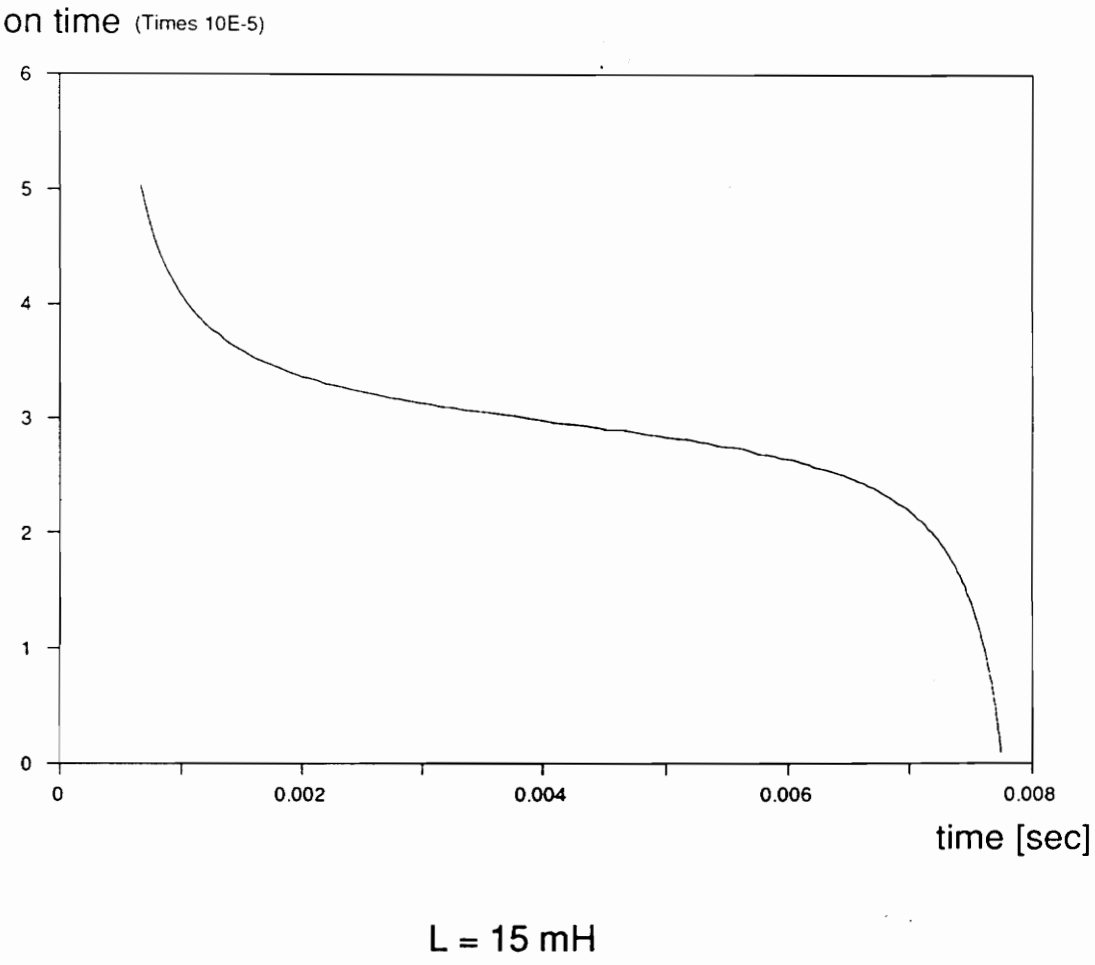



Fig. 2.2 On-time of switch with hysteresis control

upper and lower current references. To control the output voltage, the error voltage is multiplied by the sensed rectified line voltages to vary the upper and lower current references. In this proposed controlled on-time method, the only information needed is the zero crossing of the inductor current. This can be very simply obtained by the sensing of the inductor voltage through another winding on the power stage inductor core. The multiplier is no longer required.

- Smaller inductor size. In the controlled on-time scheme the converter works at the boundary of continuous and discontinuous conduction modes; therefore, the inductor size is smaller than in the hysteresis control which works in continuous conduction mode.

- The MOSFET is turned on with zero current; therefore, there are no losses during turn on of the switch.

- There are no diode reverse recovery losses.

- No additional control circuitry is required to overcome the problem of very high switching frequency at the beginning and end of the line cycle.

Disadvantages include:

- a higher ripple current,
- higher core losses, and

- a bigger input filter.

From the above discussion it can be seen that this control scheme should be quite attractive for lower power levels as it not only simplifies the control scheme but also reduces the power stage inductor size.

## *2.2 Description Of The Method*

The functional diagram of this method is shown in Figure 2.3. The power factor correction circuit has four major parts:

- the input filter;
- a full-wave uncontrolled rectifier;
- a boost converter (which consists of an inductor L, MOSFET switch Q, blocking diode D, and capacitor C.) [The boost topology is suitable as its output voltage is higher than the input line voltage, thereby reducing the size of the holdup capacitor [3];] and
- the control circuitry.

The time-variant duty cycle as shown in Fig. 2.4 follows the following control laws:

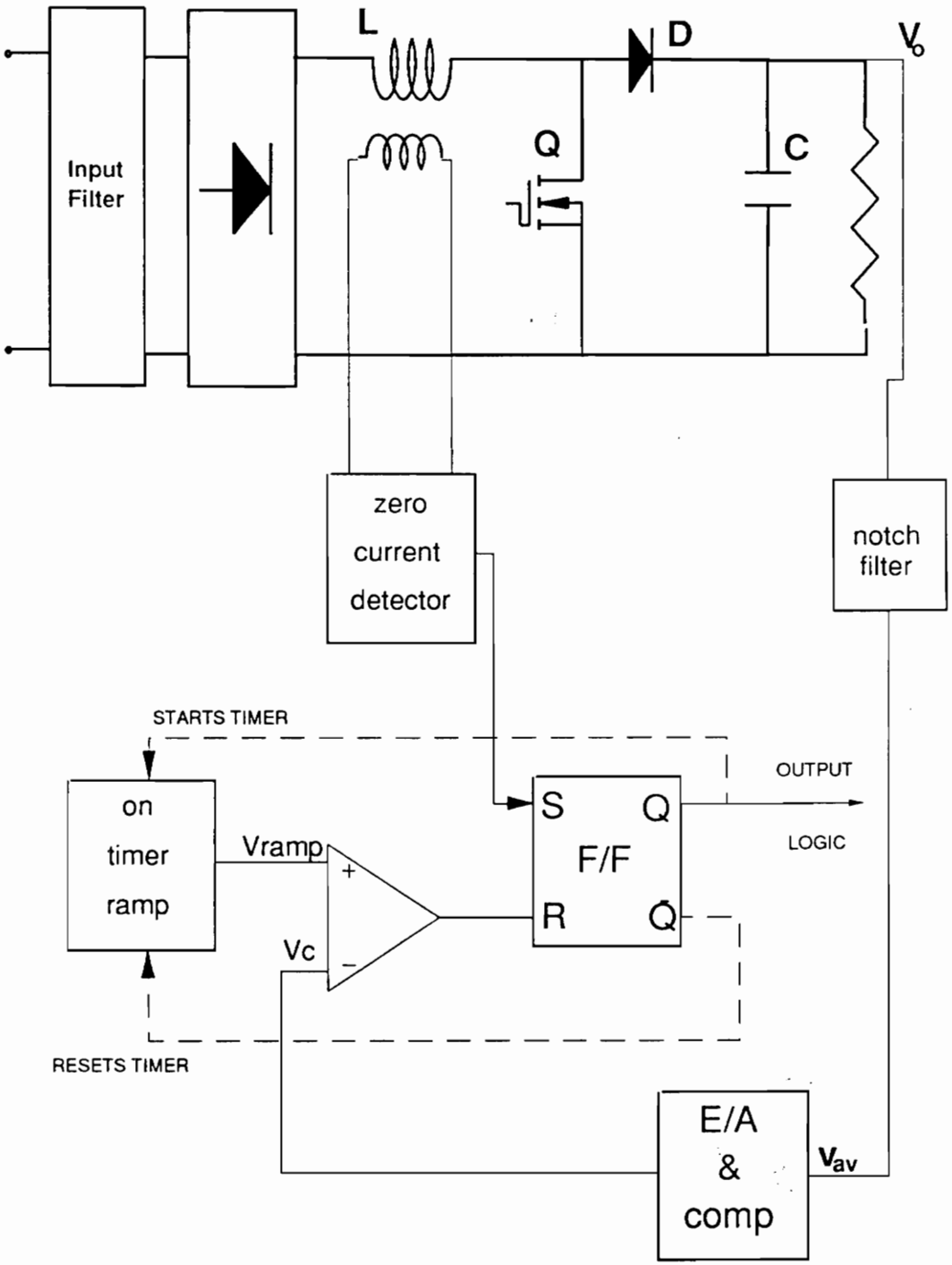



Fig. 2.3 Functional diagram of controlled on-time power factor correction circuit

- The on-time is assumed constant over the rectified line cycle. The inductor current ramps up during the on-time $T_{on}$, and energy is stored in inductor L.

- Switch Q is turned off at the end of $T_{on}$. The inductor current starts to decay, and the energy stored in L is transferred through the diode to the capacitor and load. The MOSFET is turned on again when the currrent decays to zero.

- The output voltage is controlled by varying the on-time $T_{on}$. The output voltage has a 120 Hz ripple superimposed on it. The value of this voltage ripple is independent of the switching frequency and depends only on the size of the output capacitor. In order to close the control loop, this 120 Hz ripple in the output voltage should be filtered by a notch filter or by limiting the bandwidth of the voltage error amplifier to less than 20 Hz. The input signal of the error amplifier $V_{oav}$ (shown in Fig 2.3) is the scaled average value of the output voltage $V_0$. The average output voltage is assumed to be slow varying and therefore, for the purpose of analysis, the on-time can be considered constant over a rectified line cycle.

Figure 2.4 shows some waveforms to illustrate the workings of the controlled on-time scheme in the steady state condition. For $V_c$ = constant (steady state) the on-time is fixed. The off-time is variable depending on the input voltage over the rectified line period. Figure 2.5 shows the control waveforms on an expanded time scale (two switching periods of the MOSFET). To illustrate the mechanism of the output voltage control the steady state $V_c$ is perturbed by a large $\hat{V}_c$. The resultant

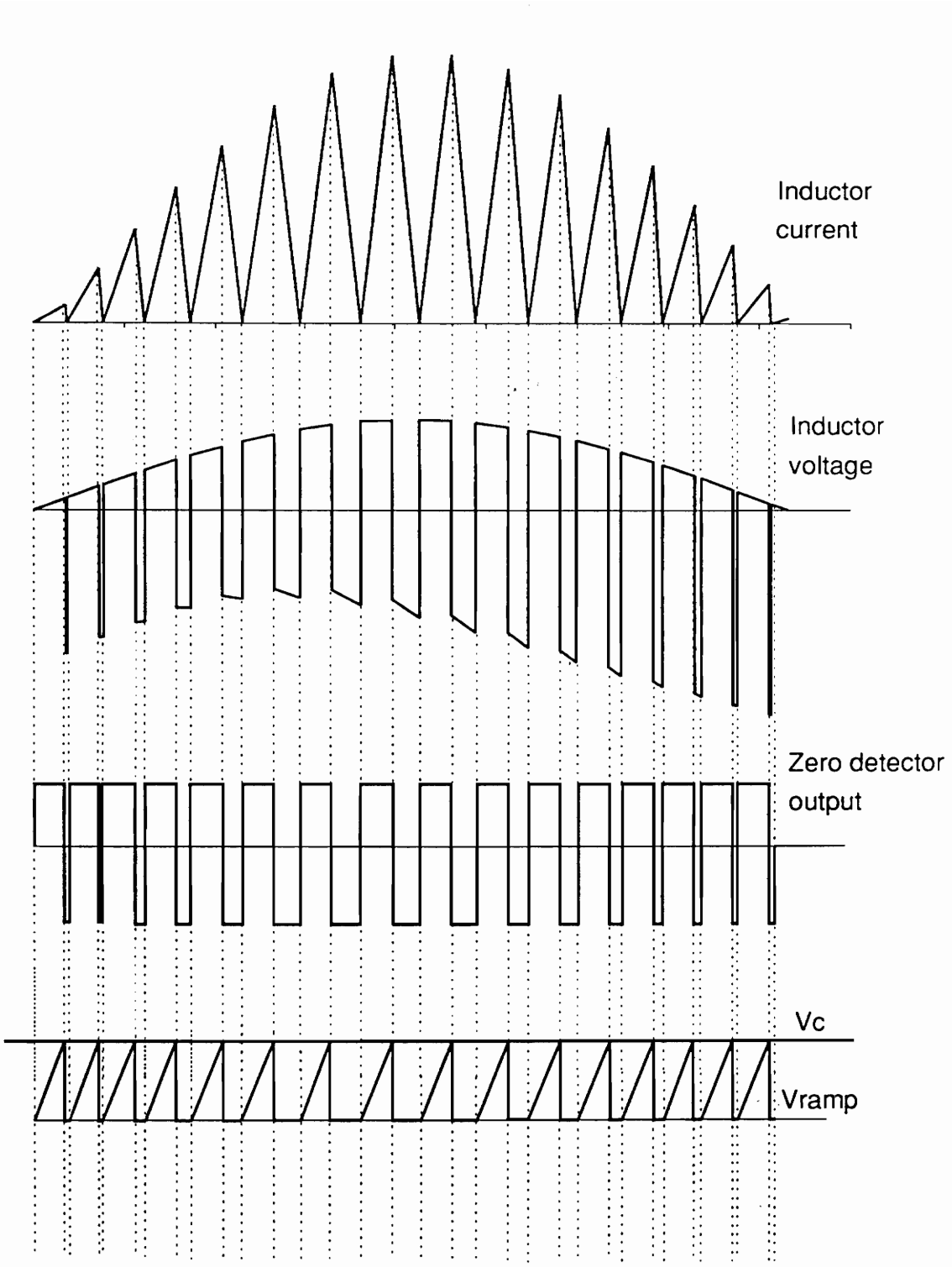



Fig. 2.4 Control waveform

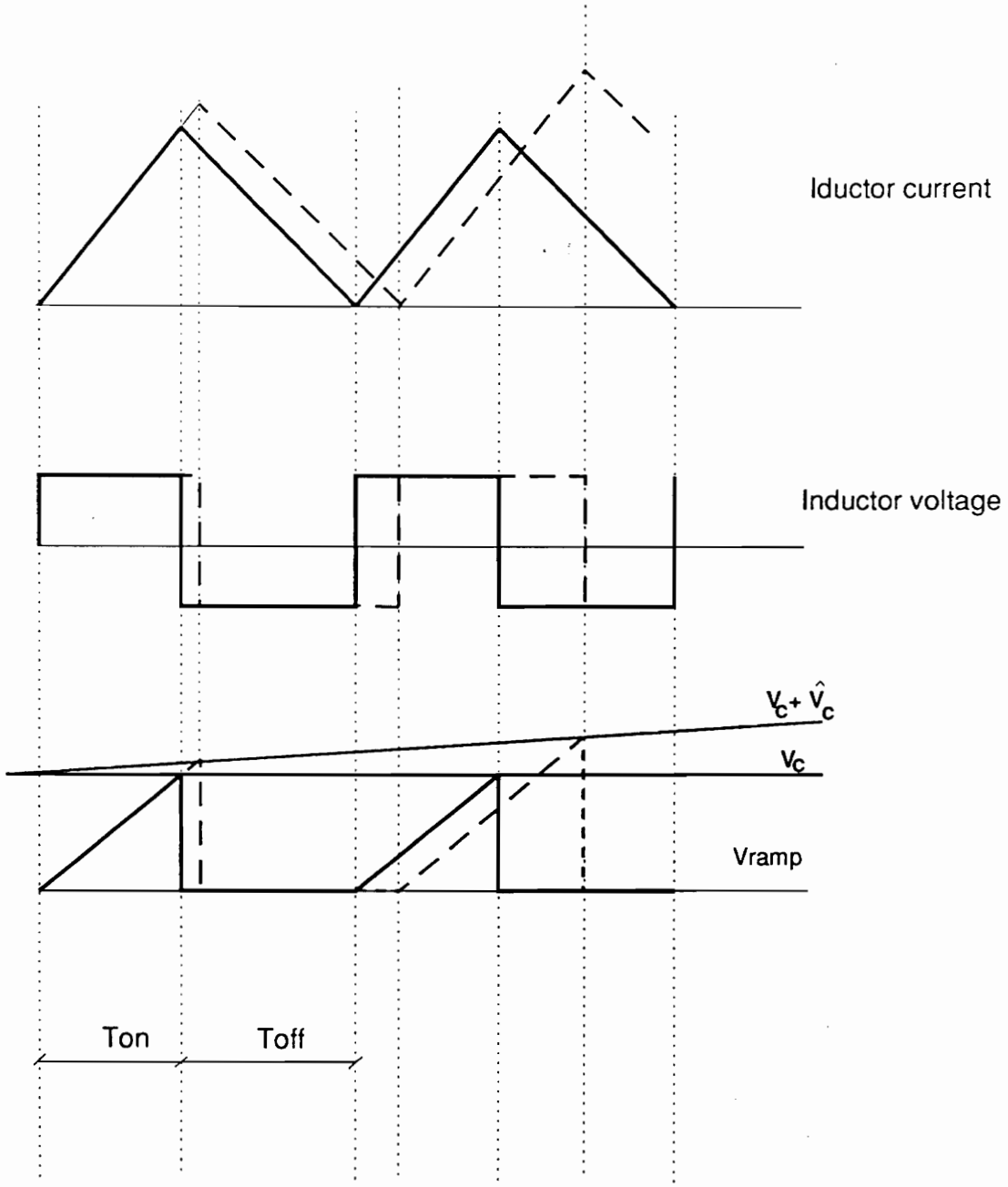



Fig. 2.5 Expanded control waveforms for two switching cycles

waveforms are shown by dotted lines. The description of the workings of the circuit is as follows:

When the MOSFET is off, the output of the flip-flop as shown in Fig. 2.3 is low, and the inductor current decays. When the inductor current has decayed to zero, the zero-current detector (comparator) forces the output of the F/F high. This switches on the MOSFET and at the same time starts the on-time ramp, $V_{ramp}$. The on-time ramp is compared with the output of the E/A (compensator); when the on-time ramp has become equal to the output of the E/A (after $T_{on}$ ), the comparator resets the F/F. This will switch off the MOSFET and also resets the on-time ramp. $T_{on}$ will remain constant if the average output voltage of the converter remains constant. If the scaled average output voltage $V_{oav}$ decreases, then the output of the E/A $V_c$ increases. This will increase the on-time, resulting in more current being pumped to the load, thereby bringing up the output voltage of the converter. The off-time is controlled by the zero current detector.

## *2.3 Cosmir Simulation Of The Power Stage*

To verify this control concept, a boost power factor correction circuit with the proposed controlled on-time was simulated on an IBM PC using COSMIR [4]. The results of the simulation are shown in Figs. 2.6 and 2.7. The simulation was for an input rms voltage of 120 V, 60 Hz. The output voltage was 300 V, and the

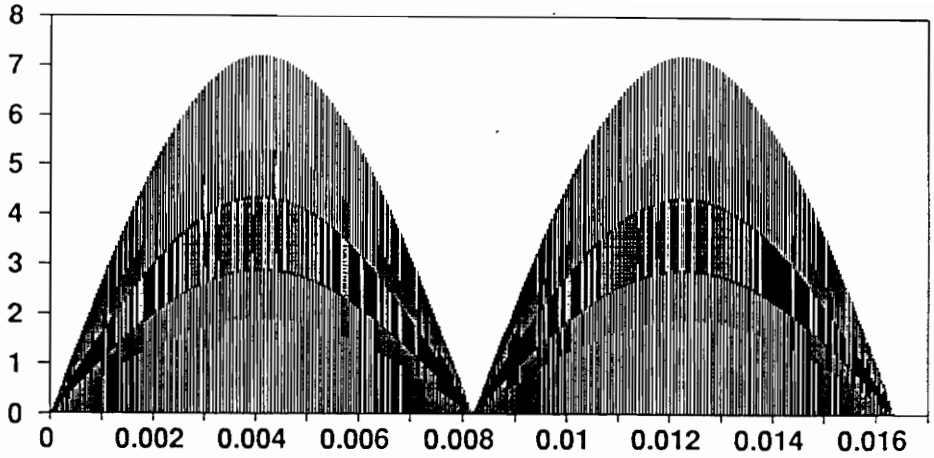


Fig. 2.6a Inductor current

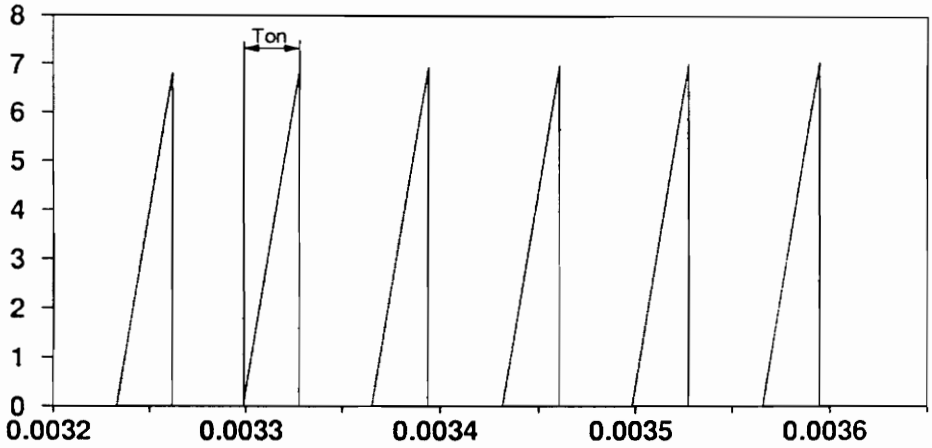


Fig. 2.6b Switch current on expanded time scale

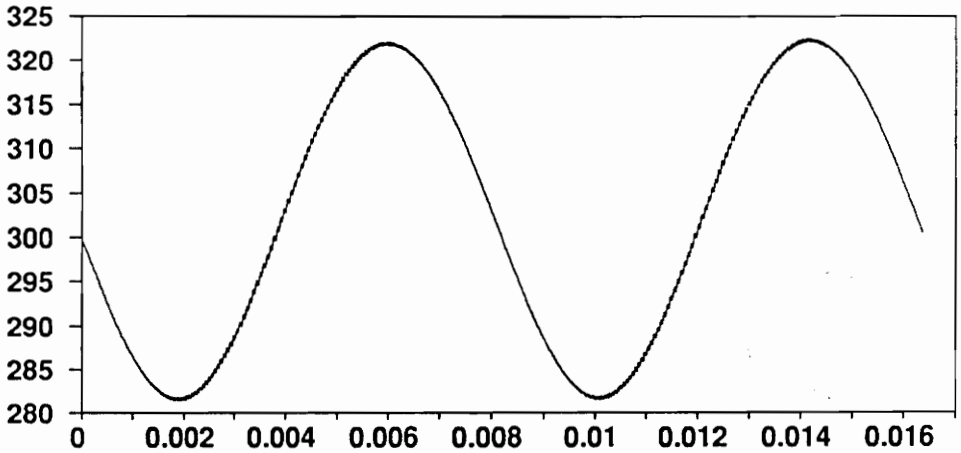


Fig. 2.6c Output voltage

Fig. 2.6 COSMIR simulation of power factor correction circuit

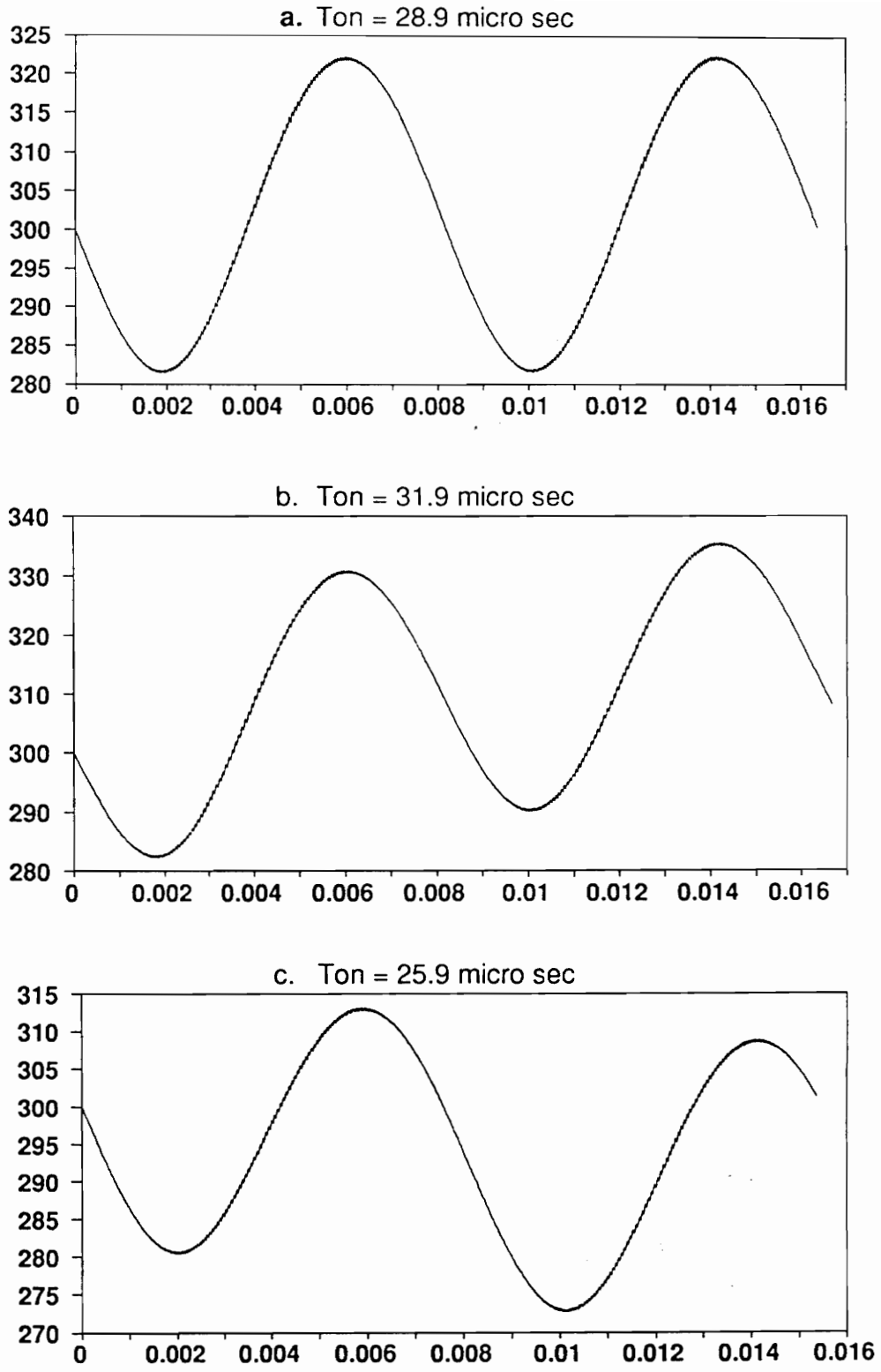



Fig. 2.7 Output voltage for variation of Ton

output power was 300 W. The output capacitor was chosen to be 66.3 $\mu$F with a 40 V peak to peak ripple. The inductor was 0.695 mH. The inductor was chosen for a minimum frequency of 15 kHZ. The on-time for the above conditions was calculated to be 28.9 $\mu$sec. (The circuit diagram for the COSMIR simulation and the input files for COSMIR are given in Appendix B.)

Figure 2.6a shows the simulated inductor current waveform. The current envelope is sinusoidal because the input voltage is sinusoidal, and the output voltage is basically constant. The maximum peak of the inductor current is defined by the output power. For a fixed input voltage, output voltage and output power, the switching frequency is determined by the value of L. But the minimum size of L is limited by switching losses. Figure 2.6b shows the switch current on an expanded time scale. Figure 2.6.c shows the output voltage. The output voltage has the high frequency switching ripple superimposed upon it. This high frequency ripple is very small compared to the 120 Hz ripple which depends on the size of the output capacitor. In Fig. 2.7, the effect on the output voltage of varying the on-time is shown. Figure 2.7a shows the steady state condition for $T_{on}$ = 28.88 $\mu$ sec. In Fig. 2.7b, the on-time was increased to 31.88 $\mu$ sec. This causes the output voltage to ramp up to a higher steady state value. In Figure 2.7c, $T_{on}$ = 25.9 $\mu$ sec, resulting in the output voltage ramping down to a lower value.

## 2.4 Power Factor Circuit Analysis

In this section, the power factor correction circuit is analyzed, and to facilitate the design of power stage components, analytical expressions are derived for various parameters of the power stage. These expressions are also used in Chapter 4 for the nonlinear optimization of the power stage using CADO. Analytical expressions were derived for the following parameters:

- duty cycle,
- on-time,
- off-time,
- output voltage ripple,
- RMS switch, diode, and inductor currents, and
- power factor without input filter.

For the analysis, the following assumptions were made:

- The rectified line voltage $V_p \sin \omega t$ is assumed constant over the MOSFET switching period $T_p$. This assumption is valid since the MOSFET switching period is very small compared to the rectified line period.

- On-time $T_{on}$ is considered constant over half of the line cycle.

### 2.4.1 Duty cycle

The boost converter with the proposed controlled on-time is operated at the boundary of continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Figure 2.8 shows the equivalent circuit diagrams for the on-time and the off-time intervals, and Fig. 2.9 shows an expanded time scale of the inductor current for one switching period of MOSFET. For DCM we have:

$$|\Delta i_{on}| = |\Delta i_{off}|,$$

where:

$\Delta i_{on}$ - increase of inductor current during on-time, and

$\Delta i_{off}$ - decrease of inductor current during off-time

$$\Delta i_{on} = \frac{1}{L}\int_{t}^{t+dT_p} V_p \sin \omega t \, dt \qquad (2.4.1.1)$$

$$\Delta i_{off} = \frac{1}{L}\int_{t+dT_p}^{t+T_p} V_0 - V_p \sin \omega t \, dt. \qquad (2.4.1.2)$$

With equations (2.4.1.1) and (2.4.1.2), assuming that $T_p$ is much smaller than half of the line period, we get the duty cycle at the time instant $t$:

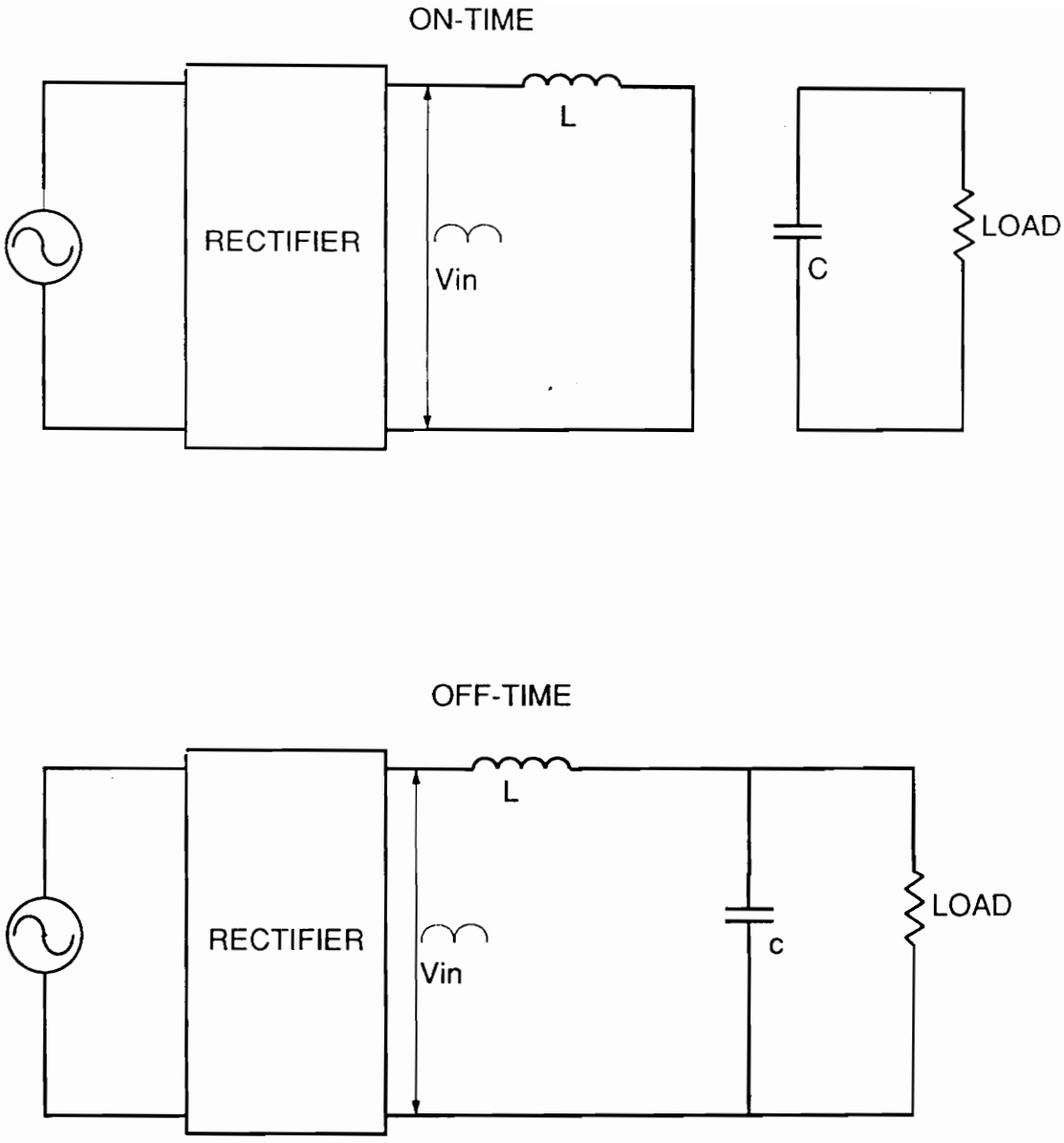



Fig. 2.8 Power stage equivalent diagram during on-time and off-time

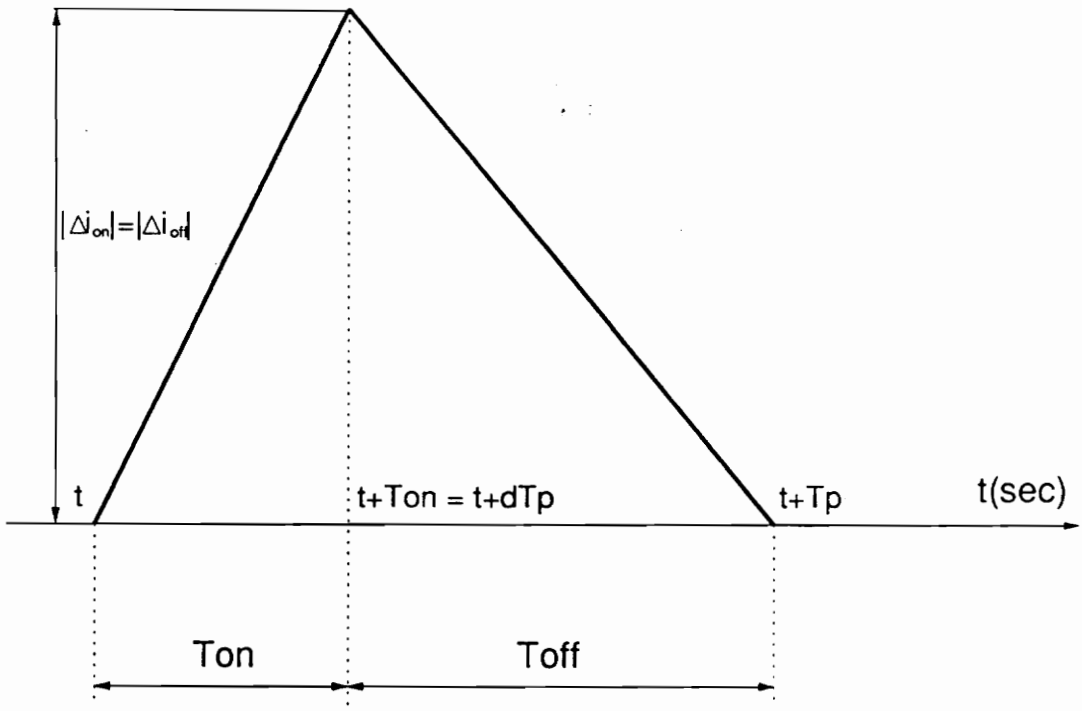



Fig. 2.9 Inductor current during one switching cycle

$$d(t) = 1 - \frac{V_p}{V_0} \sin \omega t. \qquad (2.4.1.3)$$

In Eq. (2.4.1.3), $V_p$ is the peak of the input sinusoidal voltage, $V_0$ is the output voltage, $\omega = 2\pi f_l$, and $f_l = 120$ Hz. The expression for the duty cycle in Eq. (2.4.1.3) is exactly same as the expression for the duty cycle of the power factor correction circuit with hysteresis control [2].

### 2.4.2 On-time

The output voltage is regulated by controlling $T_{on}$. Therefore an analytical expression relating the on-time to the output voltage is useful. Assuming no losses, we have:

$$P_0 = P_{in} = \frac{V_p}{\sqrt{2}} \cdot \frac{I_m}{\sqrt{2}}. \qquad (2.4.2.1)$$

From Fig. 2.9 we see that:

$$I_m = \frac{1}{2} I_p = \frac{T_{on} V_p}{2L}. \qquad (2.4.2.2)$$

Substituting (2.4.2.2) in (2.4.2.1), we get:

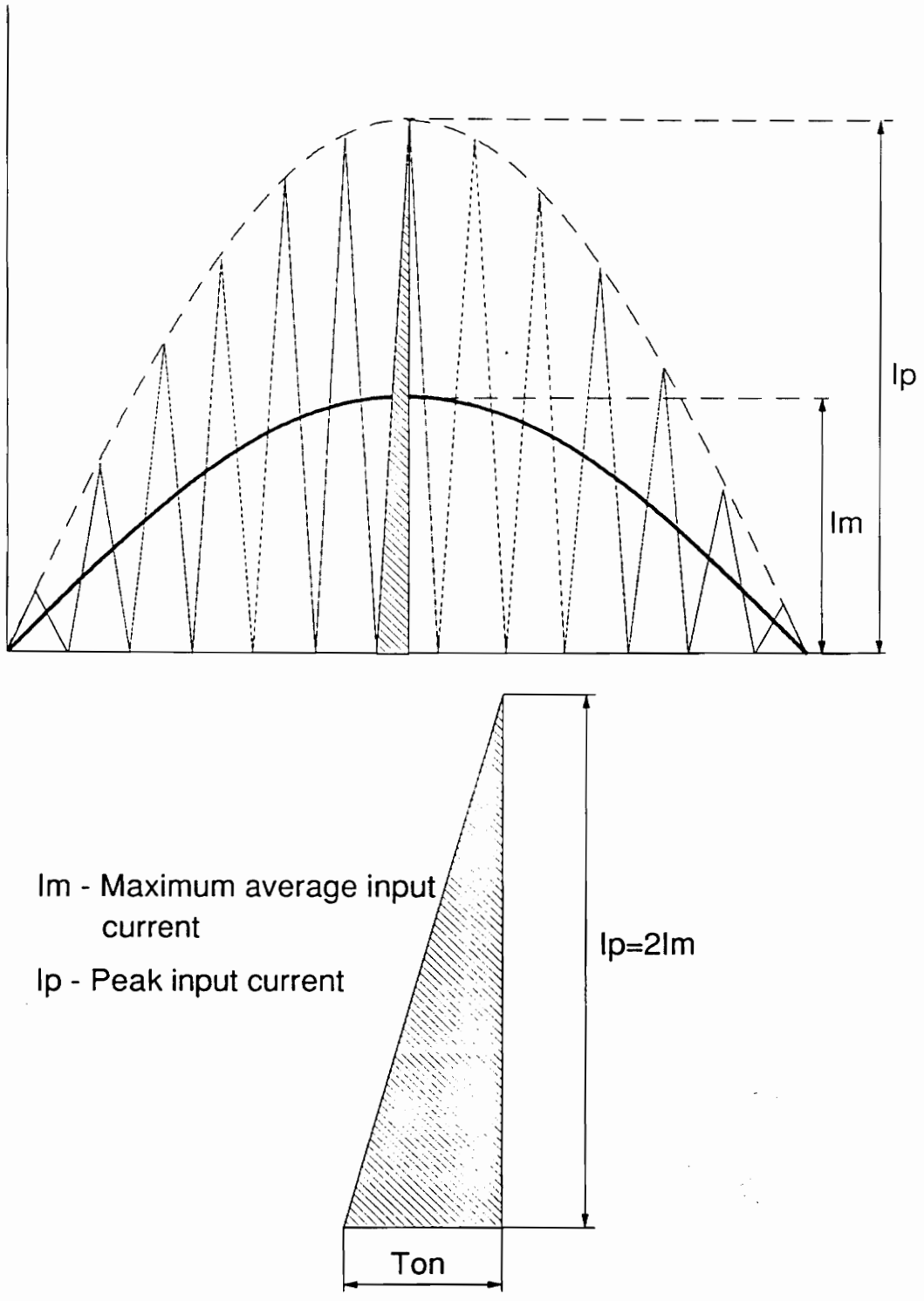



Fig. 2.10 Inductor current during one rectified line period

$$T_{on} = \frac{4P_0 L}{V_p^2}, \tag{2.4.2.3}$$

or

$$T_{on} = \frac{4V_0 I_0 L}{V_p^2}. \tag{2.4.2.4}$$

In Eq. (2.4.2.2), $I_m$ is the maximum average input current (Fig. 2.10), L is the power stage inductor, and $I_0$ is the load current. Equations (2.4.2.3) and (2.4.2.4) can be used to calculate the on-time for a given input voltage, output voltage or power, and the inductor L.

### 2.4.3 Off-time

The expression for the off-time can easily be found using the following definition of duty cycle:

$$d(t) = \frac{T_{on}}{T_{on} + t_{off}}. \tag{2.4.3.1}$$

Elimination of $d(t)$ gives:

$$t_{off}(t) = \frac{T_{on}(V_p \sin \omega t)}{V_0 - V_p \sin \omega t}. \tag{2.4.3.2}$$

The analysis of the circuit is complicated by the fact that even if we assume $T_{on}$ constant, $t_{off}$ is variable. Therefore the switching frequency is variable. To calculate the switching losses, we need to know the switching frequency. The instantaneous frequency can be derived as:

$$f_s(t) = \frac{1}{T_{on} + t_{off}}. \tag{2.4.3.3}$$

Substituting $T_{on}$ and $t_{off}$ in Eq. (2.4.3.3), we get:

$$f_s(t) = \frac{V_p^2(V_0 - V_p \sin(\omega T))}{4P_0 V_0 L}. \tag{2.4.3.4}$$

The frequency constant $K_{freq}$ is defined as:

$$K_{freq} = \frac{1}{T_s} \int_0^{T_s} f_s(t)\ dt, \tag{2.4.3.5}$$

where $T_s$ is the rectified line period,

or

$$K_{freq} = \frac{V_p^2}{4P_0 V_0 L} \left[ V_0 - \frac{2V_p}{\pi} \right]. \tag{2.4.3.6}$$

$K_{freq}$ is used to estimate the switching losses in the nonlinear design optimization program CADO of the power stage in Chapter 4.

### 2.4.4 Output voltage ripple

For the boost topology the output current is given by:

$$i_0 = d' I_m \sin \omega t, \tag{2.4.4.1}$$

where

$$d' = 1 - d(t) = \frac{V_p}{V_0} \sin \omega t. \tag{2.4.4.2}$$

From (2.4.4.1) and (2.4.4.2), we get:

$$\begin{aligned} i_0 &= \frac{V_p I_m}{V_0} (\sin \omega t)^2 \\ &= \frac{1}{2} \frac{V_p I_m}{V_0} - \frac{V_p I_m}{2V_0} \cos 2\omega t \end{aligned} \tag{2.4.4.3}$$

or

$$i_0 = I_0 - \Delta I_0 \tag{2.4.4.4}$$

Therefore the maximum average capacitor current will be:

$$I_{cmax} = \frac{V_p I_m}{2V_0}. \tag{2.4.4.5}$$

The output voltage ripple can then be defined as:

$$V_r = I_{cmax}\frac{1}{\omega C} = \frac{V_p I_m}{2V_0 \omega C}. \qquad (2.4.4.6)$$

From the above equation the minimum capacitor required for a specified output voltage ripple can be defined as:

$$C_{min} = \frac{V_p I_m}{2V_0 V_r \omega}. \qquad (2.4.4.7)$$

### 2.4.5 Inductor RMS current

In this section, the diode, switch, and the inductor rms currents are derived. First the rms current is derived for one switching period of the MOSFET. Then the rms current is derived by integration over the rectified line period. (Details of this derivation are in Appendix A.) From Appendix A1, A2, and A3 we have:

$$i_{swrms} = \sqrt{\frac{T_{on}^2 V_p^2}{3L^2}\left[\frac{1}{2} - \frac{4\pi V_p}{3V_0}\right]} \qquad (2.4.5.1)$$

$$i_{drms} = \sqrt{\frac{4V_p}{3\pi V_0}\left[\frac{V_p^2 T_{on}^2}{3L^2}\right]} \qquad (2.4.5.2)$$

$$i_{lrms} = \sqrt{\frac{T_{on}^2 V_p^2}{6L^2}} = \frac{1}{\sqrt{6}} I_p, \qquad (2.4.5.3)$$

where $i_{swrms}$, $i_{drms}$, and $i_{lrms}$ are switch, diode, and inductor rms currents, respectively. We can see that the rms currents are independent of the selection of the value of L because for the same output power, the change in L is compensated by a proportional change in $T_{on}$. These rms current are used in CADO to calculate the conduction losses in the power stage.

### 2.4.6 Power factor without input filter

The power factor is given by the following equation:

$$P.F. = \frac{P_{in}}{I_{rms}\, V_{rms}}, \tag{2.4.6.1}$$

where $P_{in}$ is the true input power defined as:

$$P_{in} = \frac{1}{T_s} \int_0^{T_s} v(t)\, i(t)\ dt.$$

Here i(t) and v(t) are the instantaneous line current and voltage, $I_{rms}$ and $V_{rms}$ are the rms values of the input current and voltage, and $T_s$ is the rectified line period.

$$\begin{aligned} P_{in} &\simeq \frac{1}{T_s} \int_0^{T_s} V_p \sin \omega t \quad I_m \sin \omega t \ dt \\ &= \frac{1}{2}\, V_p\, I_m = \frac{1}{4}\, V_p\, I_p \end{aligned} \tag{2.4.6.2}$$

where $V_p$ is peak input voltage, $I_m$ is maximum average input current, and $I_p$ is the maximum peak input current. Also we have:

$$V_{rms} = \frac{V_p}{\sqrt{2}} \quad \text{and} \quad I_{rms} = \frac{1}{\sqrt{6}} I_p. \tag{2.4.6.3}$$

Putting Eqs. (2.4.6.2) and (2.4.6.3) in (2.4.6.1.), we get:

$$P.F. = 0.866.$$

We see that the power factor attained without an input filter is 0.866. This low value is due to the high ripple of the input current. This power factor can easily be improved to almost unity by attenuating the high frequency current ripple with a small input filter. This input filter is required not only to improve the power factor, but also to meet the electromagnetic interference (EMI) regulatory specifications. (The attenuation requirement of the input filter to meet the EMI specification is much higher. Therefore, the filter needed to meet the EMI specification will make the power factor almost unity.) Detailed analysis of the input filter is given in Chapter 3.

# CHAPTER 3. INPUT FILTER ANALYSIS AND DESIGN

## *3.1 Introduction*

An input filter is usually required between any PWM converter and the power source. This prevents the regulator switching current from being reflected back to the source. Input filters for SMPSs have been extensively analyzed, and it may seem that the conventional input filter design for SMPS could also be applied to the power factor correction circuit. However, it was discovered that application of this conventional method of input filter design to power factor correction circuits may introduce an unwanted phase shift between the input voltage and current, thereby degrading the power factor. The cause of this phase shift is analyzed, and design guidelines for the input filter for the power factor correction circuit are established.

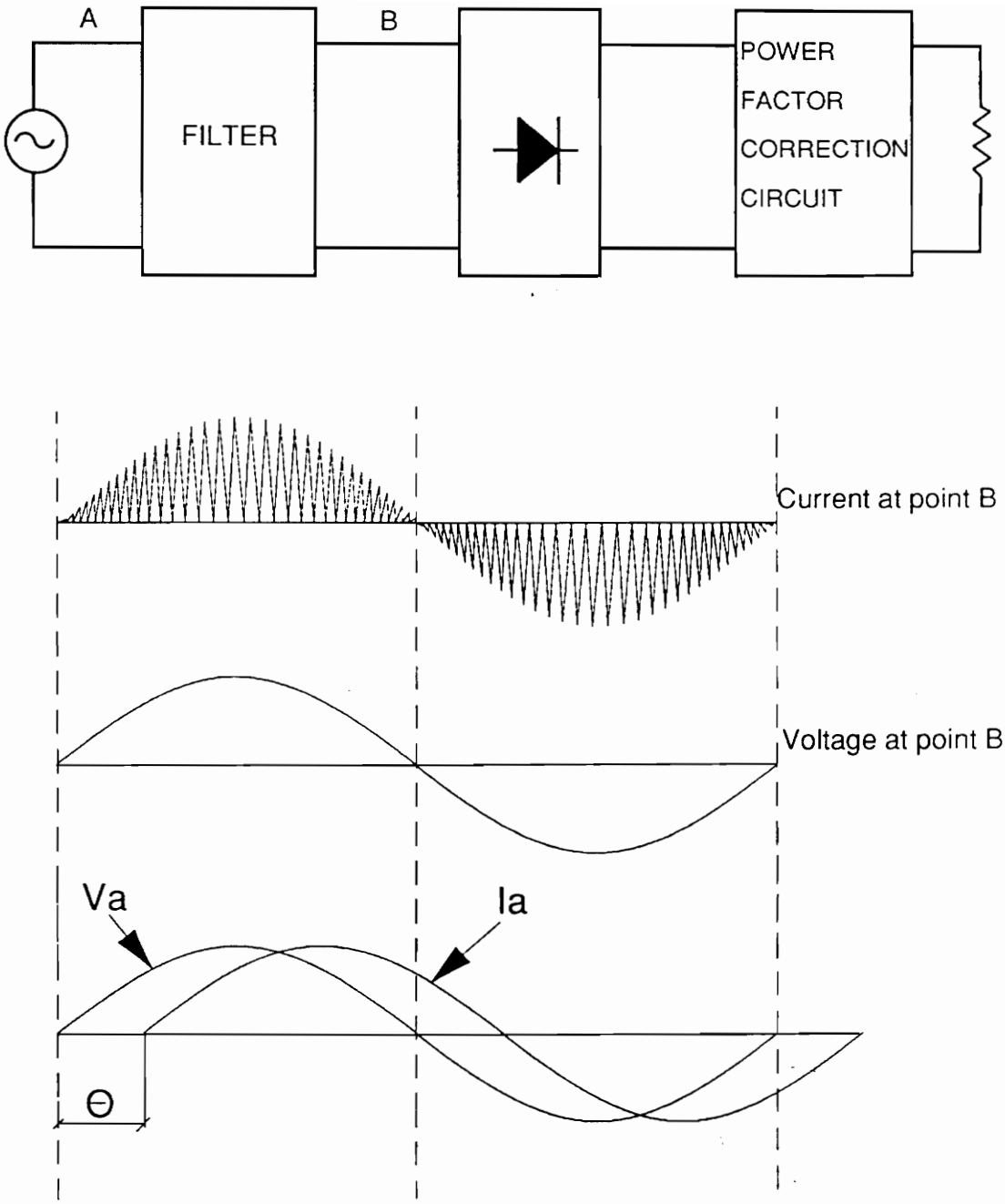



Fig. 3.1 Phase shifting effect of the input fiter

For the power factor correction circuit with variable hysteresis control, the current ripple and consequently the power factor can be controlled by varying the hysteresis window $\delta$ [3]. The smaller the hysteresis window, the lower the current ripple and higher the power factor. But a smaller hysteresis window increases the switching frequency, thereby increasing the switching losses. A compromise has to made between the hysteresis window and efficiency. So for the power factor correction circuit with hysteresis control, the primary purpose of the input filter is to suppress the inductor current ripple and prevent its reflection to the source.

For the power factor correction circuit with on-time control, it was shown in Chapter 2 that without an input filter, the power factor attained is 0.867. This is because of the very high ripple current. In this method of control, the input filter is required not only to attenuate the ripple current, but also to improve the power factor. The required attenuation of the filter is primarily defined by the amount of attenuation needed to meet the regulatory specification for conducted electromagnetic interference (EMI).

## *3.2 Effect Of Input Filter And Definition Of Input Filter Requirement*

The low power factor of switched mode power supplies is due to the high amplitude pulsed current drawn from the source during a relatively short time of half of the line period. The active power factor correction circuit synthesizes

the input current so that it flows during the entire line period and is in phase with the input voltage, thereby increasing the power factor to almost unity. This is illustrated in Fig 3.1. The average input current and the input voltage at point B are in phase. If the input filter is not properly designed, it may cause the input current and the input voltage to be shifted in phase (point A in Fig. 3.1). Therefore, even though the input current is sinusoidal, it is out of phase with the input voltage due to the improper design of the input filter. So the power factor will be degraded. This imposes some additional requirements on the input filter of the power factor correction circuit. Therefore, for the power factor correction circuit, we have the following requirements for the input filter:

- The input filter should not produce a phase shift betwen the input voltage and the input current.

- The input filter should provide proper attenuation to meet the regultory specifications for the input current ripple.

- The input filter should have minimum resonant peaking to avoid undesired interaction with the power stage.

## *3.3 Input Filter Analysis*

### 3.3.1 Input impedance

For sinusoidal input currents and voltages, a phase shift will occur between them if the load is not resistive at the input voltage frequency. For power factor correction circuits, the input voltage is sinusoidal, and the input current is actively shaped so that it is also sinusoidal. In power factor circuits, the loads which the voltage source sees are the input filter and the power stage of the power factor correction circuit. Therefore, in order to avoid any phase shift between the input voltage and the input current, the input filter must be designed so that the input impedance is resistive at line frequency. The equivalent circuit diagram for the input impedance is shown in Fig. 3.2. A two stage filter is considered because, for the same attenuation, it is lighter in weight than a single stage filter and the resonant peaking can be controlled by an $R_c$, which is not in the main power transmission path [12]. The most important reason for selecting a two stage filter is that for higher power it is not possible to get the attenuation required by VDE (Verband Deustche Electrotechnisher) specifications with a single stage filter and at the same time fulfill the conditions needed to avoid phase shifting problems. In the equivalent circuit of the input filter and the power factor correction circuit for the derivation of the analytical expression of the input impedance (shown in Fig. 3.2) the power stage has been represented by R:

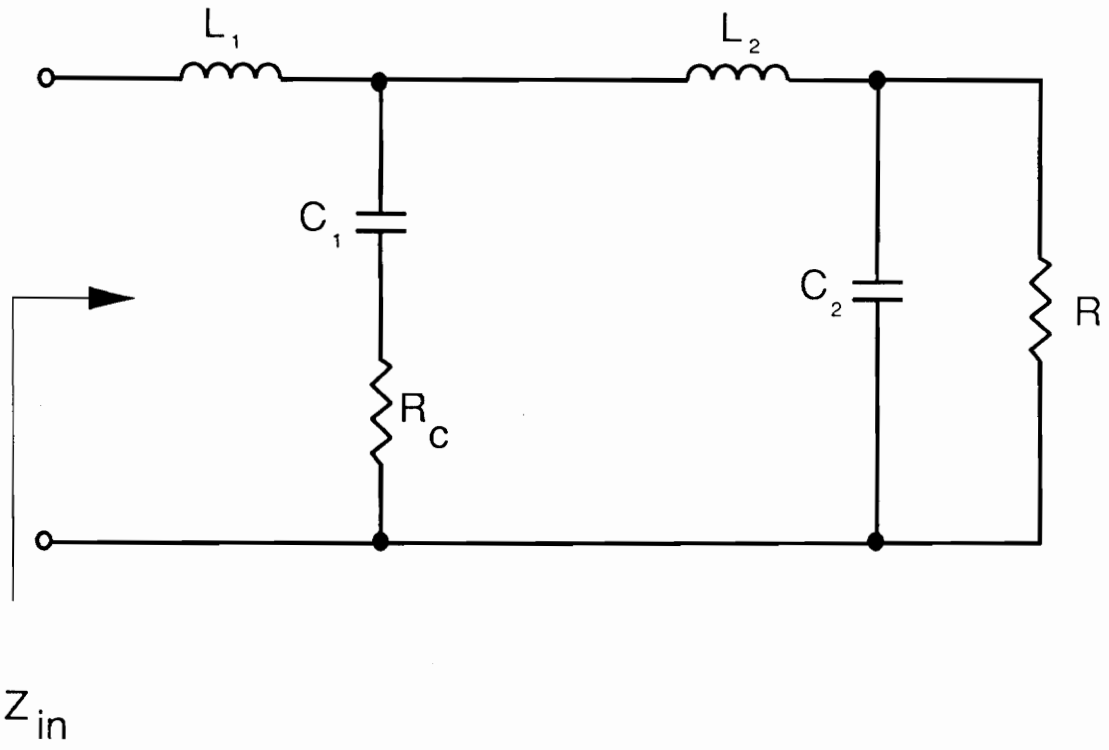



Fig. 3.2 Schematic for input impedance derivation

$$R = \frac{V_p^2}{2P_0}, \tag{3.3.1.1}$$

where R is the small signal input impedance of the power factor correction circuit [10], $V_p$ is the peak input voltage, and $P_0$ is the output power of the power factor correction circuit.

The input impedance with conditions ($L_1 >> L_2$ and $C_1 >> C_2$) can be expressed in analytical form as:

$$Z_{in} = \frac{\left(1 + \frac{s}{Q_1\omega_1} + \frac{s^2}{\omega_1^2}\right)\left(1 + \frac{s}{Q_2\omega_2} + \frac{s^2}{\omega_2^2}\right)}{\left(1 + \frac{s}{\omega_4}\right)\left(1 + \frac{s}{Q_3\omega_3} + \frac{s^2}{\omega_3^2}\right)}, \tag{3.3.1.2}$$

where

$$\omega_4 = \frac{1}{RC_1}, \tag{3.3.1.3}$$

$$\omega_1 = \frac{1}{\sqrt{L_1C_1}}, \tag{3.3.1.4}$$

$$\omega_2 = \frac{1}{\sqrt{L_2C_2}}, \tag{3.3.1.5}$$

$$\omega_3 = \frac{1}{\sqrt{L_2C_1}}, \tag{3.3.1.6}$$

$$Q_1 = \frac{1}{R_c}\sqrt{\frac{L_1}{C_1}}, \text{ and} \tag{3.3.1.7}$$

$$Q_2 = \frac{1}{R_c}\sqrt{\frac{L_2}{C_2}}. \tag{3.3.1.8}$$

For simplification of analysis, all the parasitics of the inductor and the capacitor are ignored. $R_c$ is the equivalent series resistance (esr) of the capacitor $C_1$ plus the series resistance required to dampen the resonant peaking of the filter.

To avoid any phase shift, we must make sure that none of the poles and zeros of the input impedance cause a phase shift at line frequency. Poles $\omega_1$ , $\omega_2$, and zero $\omega_3$ are complex; and as they are located at much higher frequencies than the line frequency, they do not contribute any phase shift at the line frequency. $\omega_4$ is a single pole, and therefore to avoid any phase at line frequency, it must be at least one decade above line frequency $f_l = 60$ Hz. That is, we should have:

$$f_4 \geq 10 f_l. \tag{3.3.1.9}$$

Substituting Eq. (3.3.1.3) in (3.3.1.9), we obtain:

$$C_1 \leq \frac{1}{20\pi R f_l}. \tag{3.3.1.10}$$

Equation (3.3.1.10.) defines the condition for avoiding phase shift between the input voltage and current. R is defined by the input voltage and the output power of the power stage, so the only variable for the filter in Eq. (3.3.1.10) is $C_1$. Therefore, this equation determines the maximum value of $C_1$. This equation also

shows that if the input filter is designed for some given line frequency, then for higher line frequency, the power factor may suffer.

### 3.3.2 Attenuation

#### *3.3.2.1 VDE specification interpretation for power factor circuit*

In switched mode power supplies, the input filter is generally the primary means of solving the conducted electromagnetic interference problem. The attenuation requirement of the filter is defined by the maximum amplitude of the noise ripple in the input current of the SMPS, and the maximum allowable conducted emmission allowed by the regulatory specification. Therefore, before the required attenuation for the input filter can be defined, the maximum current ripple should be known, which regulatory specification to meet should be decided, and its specification for the power factor correction circuit should be properly interpreted.

There are many regulatory agencies which control the generation of interference in the commercial and military sectors. Most countries have their own EMI specifications and corresponding regulatory agencies. The agencies in the commercial sector include the Federal Communications Commission (FCC) for the United States, Verband Deustche Electrotecknisher (VDE) for West Germany, and the International Special Committee on Radio Interference (CISPR). Also there is the military standard MIL-STD-461C.

In this thesis, VDE specifications are used to calculate the required attenuation of the input filter, because VDE specifications are perhaps the most stringent commercial EMI specifications. (VDE conducted emissions specifications are shown in Fig. 3.3.)

To measure the conducted emissions generated by test equipment, both VDE and FCC specifications require the use of the voltage measurement method. This requires a line impedance stabilazation network (LISN). Statistical distribution of the mains impedance shows an approximate 40 dB variation of the mains impedance, which can result in a 40 dB variation of the measured value of the conducted emission [15]. A standard LISN is used to overcome this problem. It provides a stabilized impedance to the high frequency conducted emissions without any hinderance to the normal flow of power to the equipment under test.

The conceptual schematic diagram of the LISN is shown in Fig. 3.4. At low line frequencies, the LISN is a low impedance path from the power source to the load and high impedance path from the source to the ground (Fig.3.4.b). At high noise frequency, LISN provides a high impedance path from the load to the power source, and an impedance of 50 Ω from load to ground (Fig. 3.4.c). The 50 Ω impedance is the input impedance of the receiver. Therefore the conducted emissions are measured as the voltage drop across the 50 Ω load. In Fig. 3.3 we see that the magnitude of the conducted emissions is given in $dB\mu V$:

$$EMI[dB\mu V] = 20 \log \frac{V_n[\mu V]}{1[\mu V]}. \qquad (3.3.2.1)$$

Therefore:

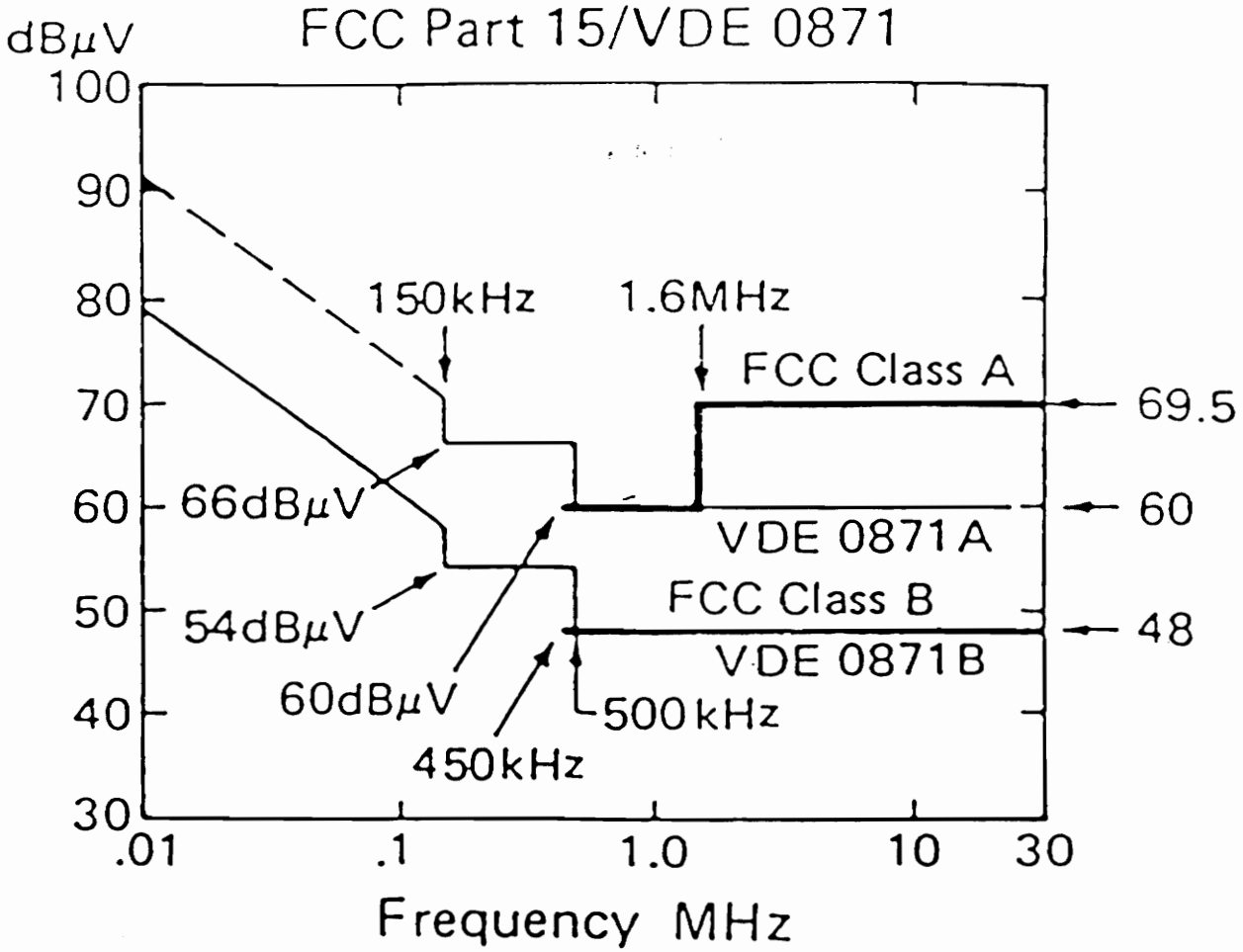
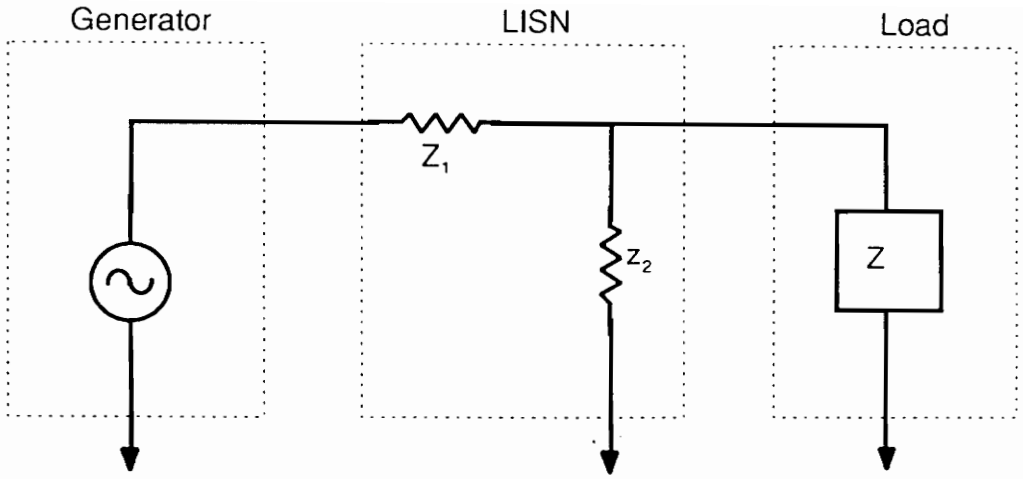
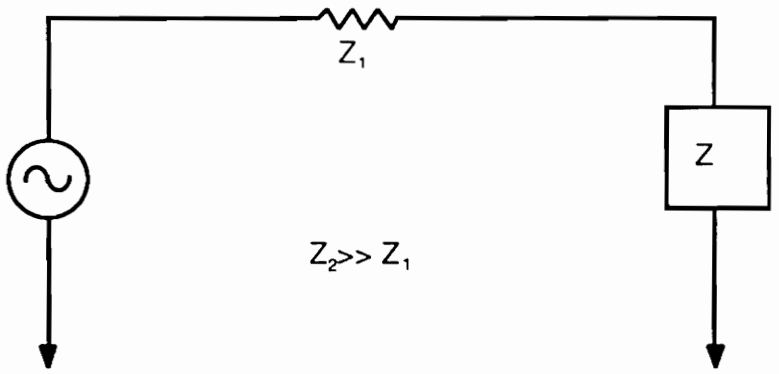


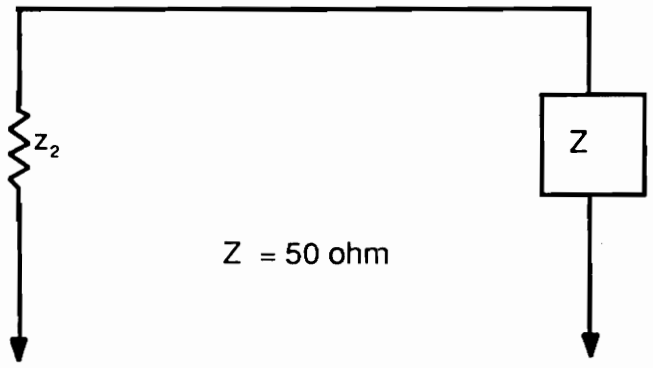

Fig. 3.3 VDE conducted emmision specification




a) Conceptual LISN




b) At line frequency




c) At noise frequency

Fig. 3.4 Conceptual schematic of LISN

$$V_n[\mu V] = 10^{\frac{V_n[dB\mu V]}{20}}, \qquad (3.3.2.2)$$

where $V_n$ is the noise voltage, and the expressions in brackets are the units.

### *3.3.2.2 First approximation of filter attenuation*

The definition of the required filter attenuation may seem complicated because both the frequency and the amplitude of the input current over a rectified line period are variable. The current ripple over one rectified line period is shown in Fig. 3.5. From Fig. 3.5 (and Eq. (2.4.3.4) for the instantaneous switching frequency), we see that the maximum amplitude of current ripple occurs where the switching frequency is minimum. Therefore, as a first approximation, if the filter is designed to attenuate the maximum ripple (where the frequency is minimum), then it should be able meet the specification for higher frequency ripple (having lower amplitudes). The attenuation $K_A$ can then be defined as follows:

$$K_A = \frac{i_g}{I_p}, \qquad (3.3.2.3)$$

and the frequency:

$$f_{smin} = \frac{1}{T_s}, \qquad (3.3.2.4)$$

where $i_g$ is the input current ripple defined by the VDE specification, $I_p$ is the maximum inductor current ripple, and $T_s$ is the maximum period. (These are

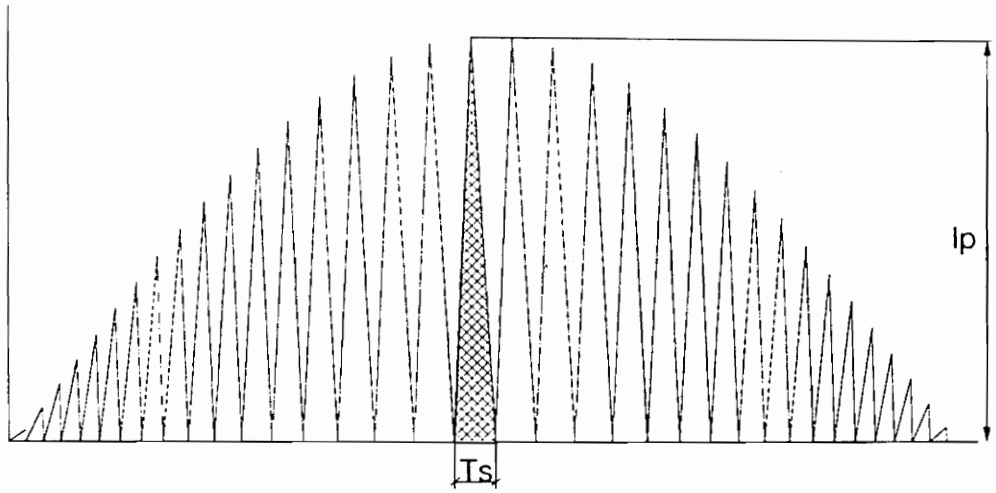



Fig. 3.5a Input current without input filter

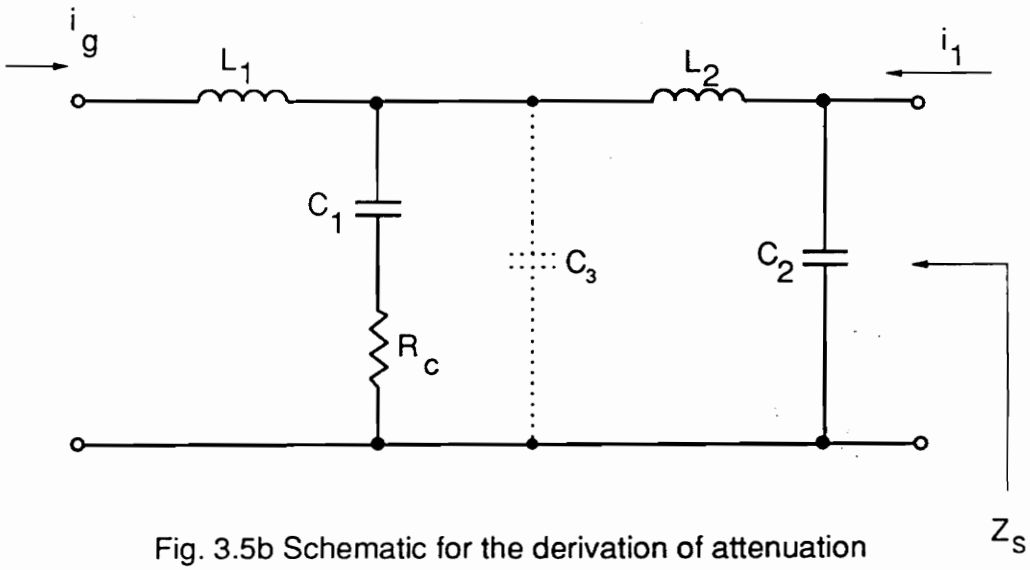
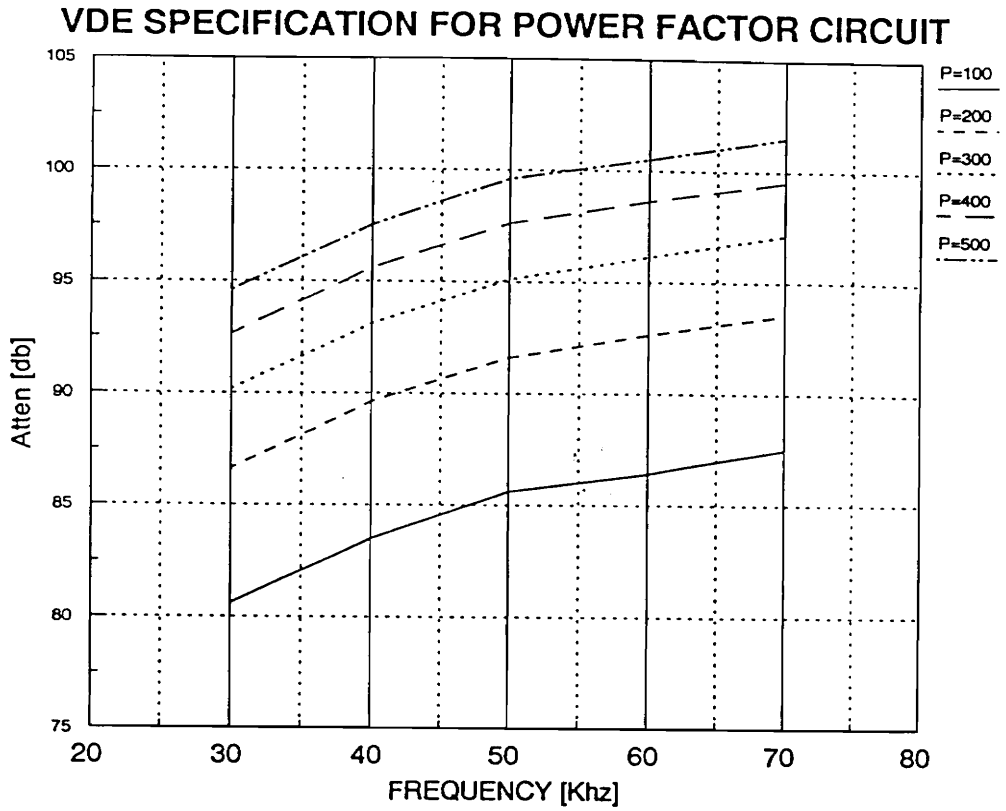



Fig. 3.5b Schematic for the derivation of attenuation




ATTENUATION [DB]

| Freq Khz | 30 | 40 | 50 | 60 | 70 |
|---|---|---|---|---|---|
| $P_0 = 100$ | -80.6 | -83.5 | -85.5 | -86.0 | -87.5 |
| $P_0 = 200$ | -86.6 | -89.6 | -91.6 | -92.6 | -93.5 |
| $P_0 = 300$ | -90.16 | -93.08 | -95.1 | -96.1 | -97.1 |
| $P_0 = 400$ | -92.6 | -95.6 | -97.6 | -98.6 | -99.5 |
| $P_0 = 500$ | -94.6 | -97.5 | -99.6 | -100.5 | -101.5 |

Fig. 3.6 VDE interpretation for power factor correction circuit

shown in Fig 3.5.) Figure 3.6 shows the attenuations required to meet the VDE specifications at different power levels and at different minimum switching frequencies. The attenuation requirement for the same power level increases at higher frequencies because the VDE requirement increases with frequency.

Figure 3.5b shows the schematic of the two stage filter used to derive the analytical expression for the attenuation $K_A$ . The attenuation for the filter with the condition $L_1 >> L_2$ and $C_1 >> C_2$ can be expressed in analytical form as:

$$K_A = \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{Q_1\omega_1} + \frac{s^2}{\omega_1^2}\right)\left(1 + \frac{s}{Q_2\omega_2} + \frac{s^2}{\omega_2^2}\right)}, \qquad (3.3.2.5)$$

where

$$\omega_1 = \frac{1}{\sqrt{L_1 C_1}}, \qquad (3.3.2.6)$$

$$\omega_2 = \frac{1}{\sqrt{L_2 C_2}}, \qquad (3.3.2.7)$$

$$\omega_z = \frac{1}{R_c C_1}, \qquad (3.3.2.8)$$

$$Q_1 = \frac{1}{R_c}\sqrt{\frac{L_1}{C_1}}, \text{ and} \qquad (3.3.2.9)$$

$$Q_2 = \frac{1}{R_c}\sqrt{\frac{L_2}{C_2}}. \qquad (3.3.2.10)$$

From the expresssion of $K_A$, we see that it is desirable to place the zero $\omega_z$ higher than the switching frequency to attain maximum attenuation. The maximum value of $\omega_z$ is inversely proportional to $R_c$ . (The maximum value of $C_1$ is already fixed by Eq. (3.3.1.10).) But the $R_c$ has to be made large to reduce the resonant peaking, therefore, $\omega_z$ cannot be made very large. The dotted $C_3$ shown in Fig. 3.5b introduces a pole $\omega_3$. If $\omega_3$ is placed below the minimum switching frequency, then it helps to increase the attenuation of the filter. But $\omega_3$ should be placed sufficiently higher than $\omega_2$ and $\omega_z$ ( $\omega_2 >> \omega_1$ ) in order to avoid increasing the resonant peaking.

### *3.3.2.3 Filter attenuation based on Fast Fourier Transform of input current*

Definition of the filter attenuation based on the maximum inductor current ripple at minimum frequency results in overdesign of the filter. As the weight of the filter constitutes a major portion of the weight of the power factor correction circuit, every endeavor should be made not to overdesign it. A more accurate way of designing the filter is to find the amplitude spectrum of the inductor current. Then the attenuation of the filter can be defined based on the harmonic with the maximum amplitude. This way the required attenuation of the filter, and thereby its cost, can be reduced.

The amplitude spectrum of the input current was defined using the FFT routine of the IMSL math library on the mainframe. COSMIR simulation was used to generate the input data vector for the FFT routine. Figure 3.7 shows the amplitude spectrum of the input current for the power factor correction circuit

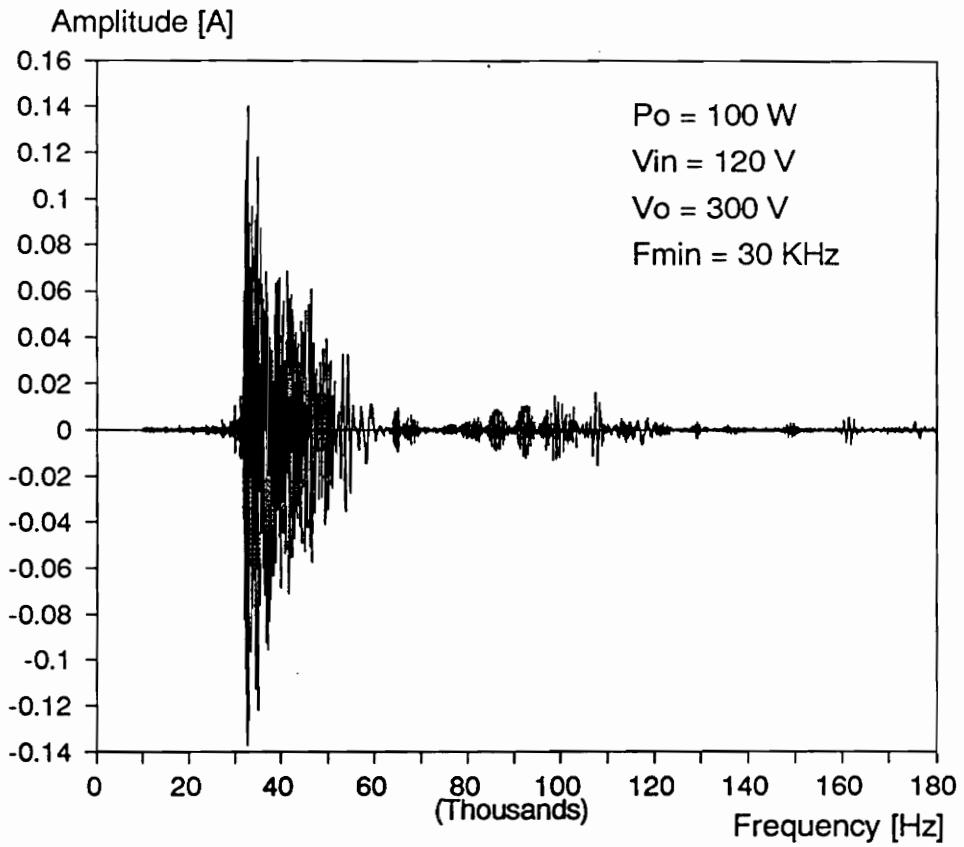



Fig. 3.7 Amplitude spectrum of input current without filter

without an input filter. This amplitude spectrum is for the power factor correction circuit with input voltage $V_{in}$ = 120 VAC, output voltage $V_0$ = 300 V, $P_0$ = 100 W, and L = 1.04 mH ( $f_{min}$ = 30 Khz). It can be seen that maximum harmonic occurs at 32 KHz, and its amplitude is 0.14 A. Based on this, the filter attenuation can be calculated to meet VDE specifications. This is shown in the design example in Section 3.5.

### 3.3.3 Output impedance

It is very important in filter design that there be minimum interaction between the filter and the power stage. To assure this, the input impedance of the power stage should be much larger than the output impedance of the filter [13,14]:

$$Z_{inp} >> Z_{out}. \tag{3.3.3.1}$$

$Z_{inp}$ and $Z_{out}$ are shown in Fig. 3.8. To assure this condition, the analytical expression for the output impedance of the filter has been derived. For condition $L_1 >> L_2$ and $C_1 >> C_2$, it is:

$$Z_{out} = \frac{\frac{s}{\omega_x}\left(1 + \frac{s}{Q_3\omega_3} + \frac{s^2}{\omega_3^2}\right)}{\left(1 + \frac{s}{Q_1\omega_1} + \frac{s^2}{\omega_1^2}\right)\left(1 + \frac{s}{Q_1\omega_1} + \frac{s^2}{\omega_1^2}\right)}, \tag{3.3.3.2}$$

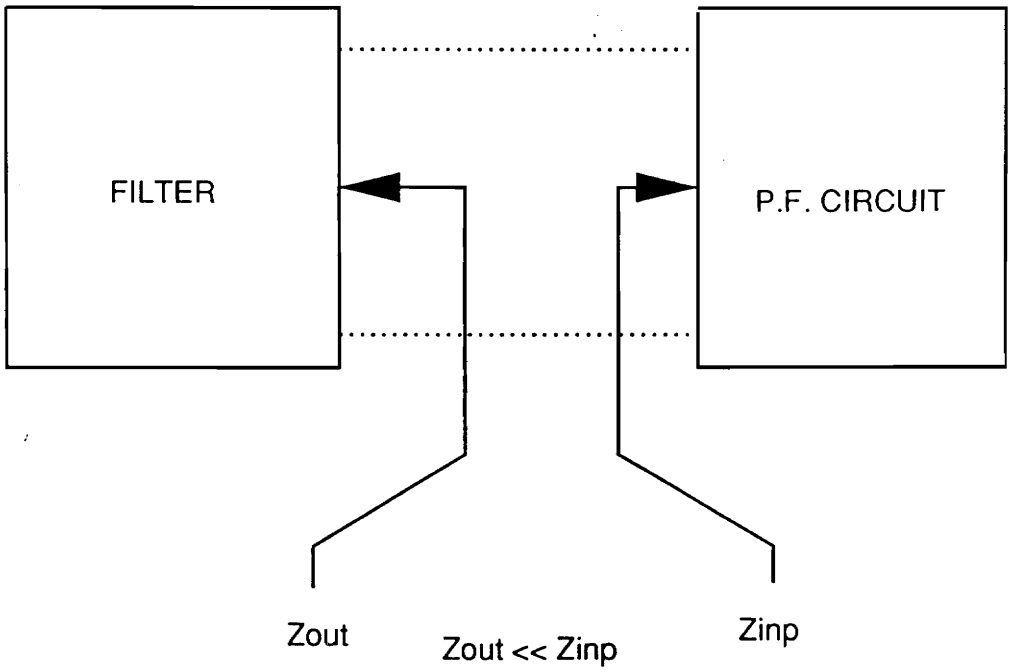



Fig. 3.8 Output impedance consideration

where

$$\omega_x = \frac{1}{L_1}, \tag{3.3.3.3}$$

$$\omega_3 = \frac{1}{\sqrt{L_2 C_1}}, \text{ and} \tag{3.3.3.4}$$

$$Q_3 = \frac{1}{R_c}\sqrt{\frac{L_2}{C_1}}. \tag{3.3.3.5}$$

$\omega_1$, $\omega_2$, $Q_1$ and $Q_2$ are same as before.

## *3.4 Input Filter Design Guidelines*

Based on the analysis in Section 3.3, we can come up with the following guidelines for the design of the input filter for a power factor correction circuit:

1. Definition of the required filter attenuation. Two methods of determination of the required filter attenuation are discussed:

   - *a) Approximate Method:* The attenuation is defined with the maximum current ripple (at minimum switching frequency). The maximum current ripple $I_p$ and the minimum switching frequency can be defined using the following equations:

$$I_p = \frac{4P_0}{V_p \eta}, \text{ and} \tag{3.4.1}$$

$$f_{smin} = \frac{V_p^2(V_0 - V_p)}{4P_0 V_0 L}. \tag{3.4.2}$$

- *b) FFT Method:* Filter attenuation is defined based on FFT of the input current as discussed in Section 3.3.2.3

The approximate method can be used to obtain a quick estimation of the filter attenuation without the use a of computer. For more accurate filter design, the FFT method should be used, but it does requires access to computers.

2. Definition of the maximum value of $C_1$. From Eq. (3.3.1.10), we get:

$$C_1 = \frac{1}{20\pi f_l R}. \tag{3.4.3}$$

3. Maximization of the first corner frequency, $\omega_1 = \frac{1}{\sqrt{L_1 C_1}}$, for low $L_1$ and low $Q_1$. The first corner corner frequency $\omega_1$ is defined by the switching frequency and the required attenuation.

4. Maintenance of sufficient separation between $\omega_2 = \frac{1}{\sqrt{L_2 C_2}}$ and $\omega_1$ to satisfy the conditions $L_1 >> L_2$ and $C_1 >> C_2$.

5. Maximization of $\omega_r$ (for maximum attenuation). Its location is determined by the $R_c$ for required attenuation of the resonance peaking.

6. Introduction of another pole, $\omega_4$, by adding capacitor $C_3$ parallel to the $C_1$, $R_c$ branch of the filter. This is shown in Fig. 3.5.b as a dotted capacitor. $\omega_4$ should be below the switching frequency to increase the attenuation, but it should be sufficiently higher than $\omega_2$ and $\omega_r$ to avoid increasing the resonant peaking.

## *3.5 Design Example*

In this design example an input filter is designed to meet the VDE specification applied to a power factor correction circuit. The specifications of the power stage are given in Table 3.9a.

The input filter was first designed based on the attenuation requirement defined by the approximate method. The minimum frequency $f_{smin}$ and the maximum current ripple $I_r$ were calculated using Eqs. (3.4.1) and (3.4.2). The required attenuation $K_A$ was calculated to meet the VDE specification. The calculated values of $f_{smin}$, and $K_A$ are given in Table 3.9b. Figure 3.9 shows the asymptote of $K_A$ for the designed filter. The location of the two poles, $f_1$ and $f_2$, and the zero $f_z$ are given in Table 3.9b.

The next step is the calculation of the filter components. The maximum value of the capacitor $C_1$ should be defined using Eq. (3.4.3) in order to avoid phase

shift between the input current and input voltage. The importance of the proper selection of $C_1$ is illustrated in Figs. 3.10 and 3.11. In Fig. 3.10, the value of $C_1$ is intentionally selected to be greater than its maximum value (for $f_4$ = 300 Hz). The filter component values are shown in Table 3.10. Figure 3.10 shows the PSPICE and COSMIR simulations of the overplot of the input voltage and current. The PSPICE simulation was done for the filter, with the small signal input impedance of the power stage R as load. The COSMIR simulation was done for the filter and the actual power stage as shown in Fig. 3.14. These simulations show that 1) improper selection of $C_1$ introduces a phase shift, and 2) the similar results of these two simulations show that the analysis using R is valid for the large input current ripple. Table 3.11 shows the filter parameters with $f_4 = 600Hz$ (fulfilling the condition to avoid phase shift). The COSMIR and PSPICE simulations both show almost no shift between the input current and voltage. Fig. 3.12a shows the input impedance phase of the two stage filter with R as load, with $C_1$ selected for $f_4$ at 300 Hz. We can see that at line frequency there is a phase of 12° due to the location of $f_4$ at 300 Hz. This agrees with the phase shift between the voltage and current shown in Fig. 3.10. Fig. 3.12b shows the input impedance phase of the filter with $C_1$ selected for $f_4$ at 600 Hz.

Figure 3.13 shows the filter output impedance asymptote for the filter. It can be seen that in order to avoid any interaction with the power stage, $Q_1$ and $Q_2$ of the filter should be less than at least 19 dB, as otherwise the output impedance of the filter $Z_{out}$ will be greater than the input impedance of the power stage $Z_{inp}$ at the resonant frequencies. To attain this, the $R_c$ was increased from 4.3 ohm to 19.5 ohm. This reduced $Q_1$ to 10.1 dB. The increase of $R_c$ however shifted the

zero to lower frequency thereby, reducing the attenuation at the switching frequency to 77.3 dB. Capacitor $C_3 = 0.25\mu F$ was added parallel to the $C_1$- $R_c$ branch, to increase the attenuation back to -80.6 dB. This is shown in Fig. 3.13.

The filter was then designed using FFT. The amplitude spectrum of the input current for the same power stage was defined in section 3.3.2.4, and the maximum amplitude was determined at 32 KHz to be equal to 0.14 A. The filter attenuation required to meet the VDE specification was $K_A$ = -56.6 dB. Filter components were calculated and are given in Table 3.15. For verification, the power factor circuit with the designed input filter was simulated on COSMIR, and the amplitude spectrum of the input current was defined. This is shown in Fig. 3.15. The maximum amplitude is 227 $\mu A$ at 31.6 KHz meets VDE specifications ($251\mu A$).

TABLE 3.9A

Power Stage Specification

| $P_0$ | $V_{in}$ | $V_0$ | L | $f_{smin}$ | $I_p$ |
|---|---|---|---|---|---|
| 100 W | 120 VAC | 300 V | 1.04 mH | 30 KHz | 3.0 A |

TABLE 3.9B

Filter Design:

| $f_1$ | $f_2$ | $f_z$ | R | $K_A$ | $f_s$ |
|---|---|---|---|---|---|
| 1 KHz | 4 KHz | 10 KHz | 144.5 ohm | -80.6 dB | 30 KHz |

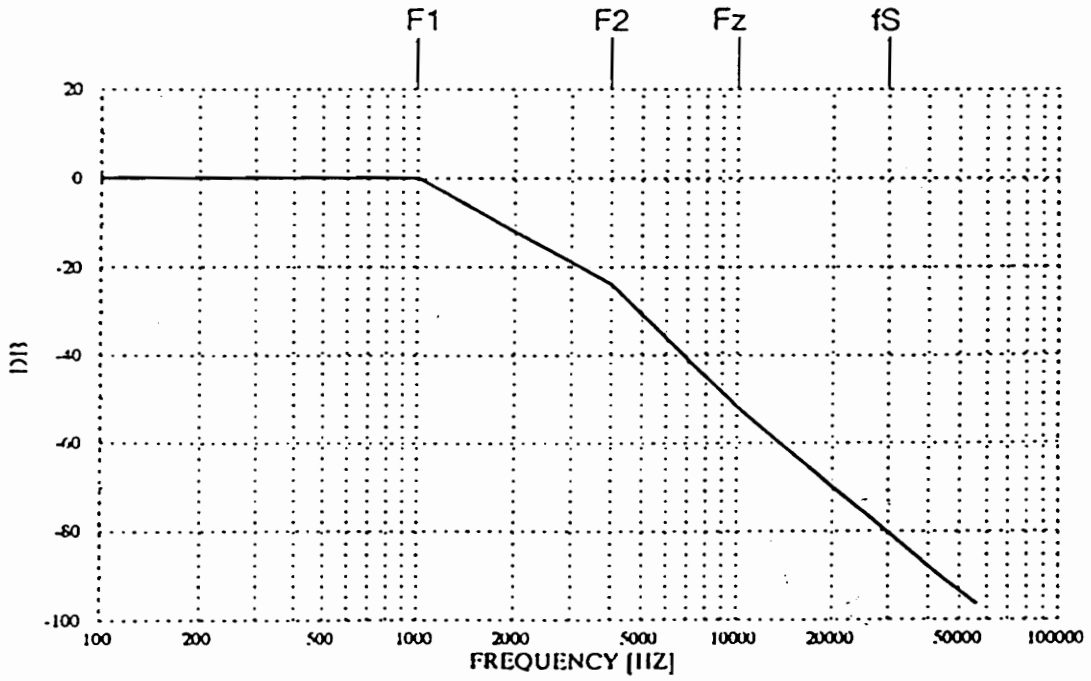
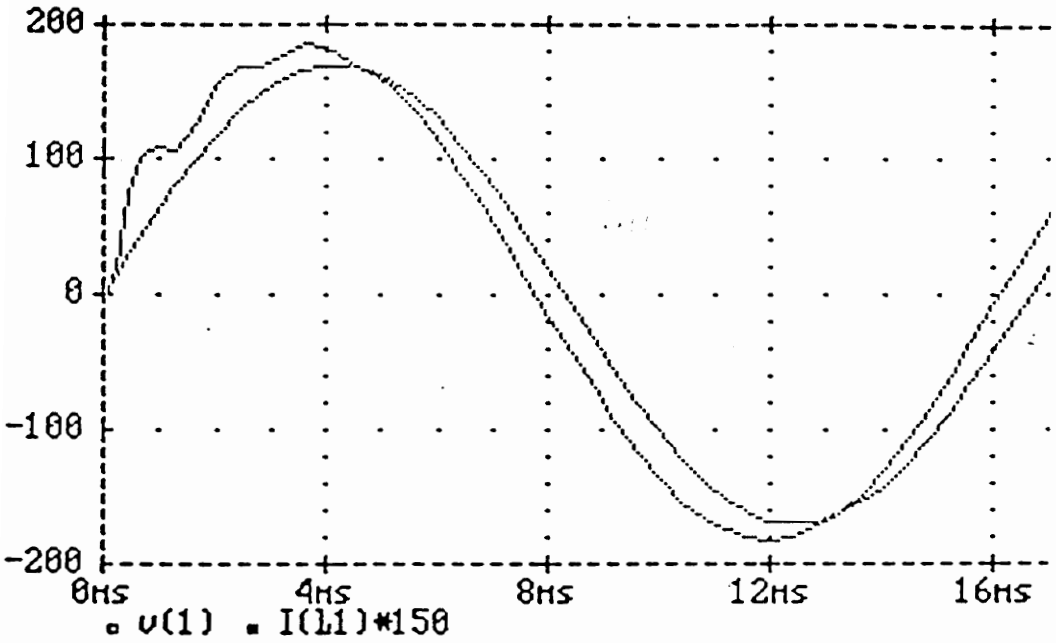



Fig. 3.9 Asymptote of filter attenuation

TABLE 3.10

Filter Parameters for $f_4 = 300Hz$

| $C_1[\mu F]$ | $C_2[\mu F]$ | $L_1[mH]$ | $L_2[mH]$ | $R_c[mH]$ |
|---|---|---|---|---|
| 3.67 | 0.73 | 7.03 | 2.16 | 4.3 |



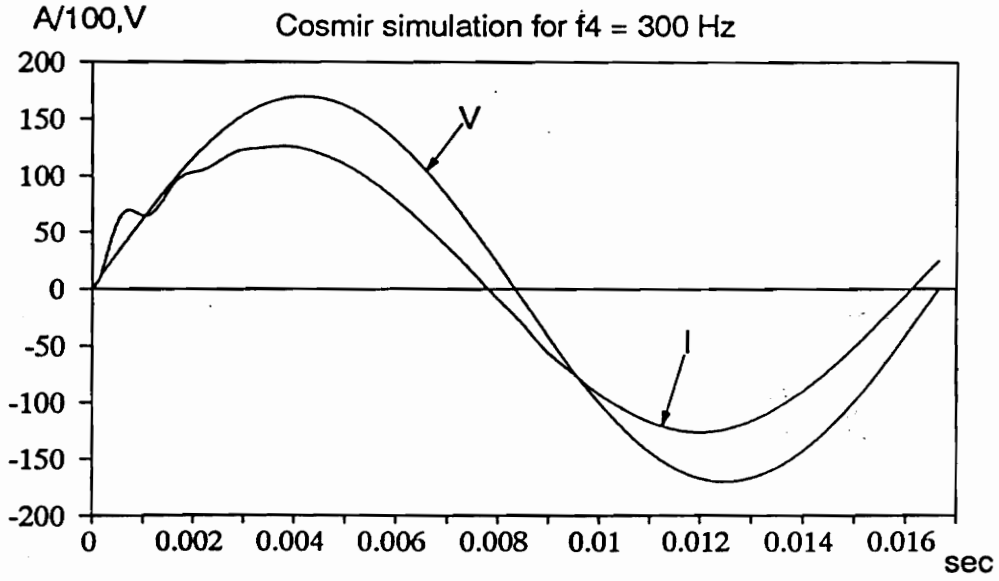
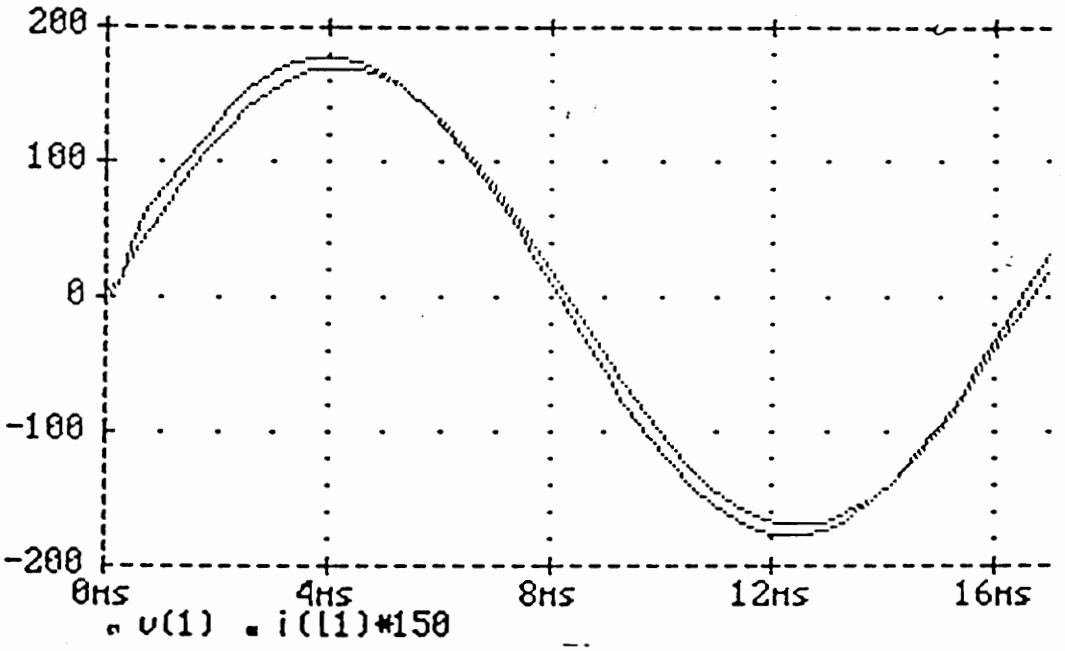




Fig. 3.10 COSMIR and PSPICE simulations for improper selection of C1

TABLE 3.11

Filter parameters for $f_4 = 600Hz$

| $C_1[\mu F]$ | $C_2[\mu F]$ | $L_1[mH]$ | $L_2[mH]$ | $R_c[\Omega]$ | $Q_1[dB]$ | $Q_2[dB]$ |
|---|---|---|---|---|---|---|
| 1.81 | 0.36 | 14 | 4.3 | 8.8 | 20 | 21 |



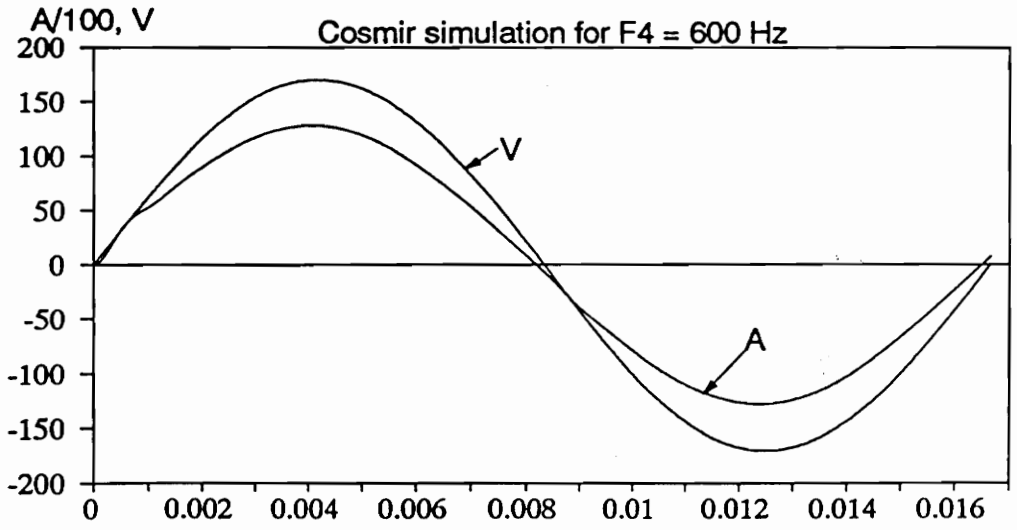




Fig. 3.11 COSMIR and PSPICE simulation for F4 = 600 Hz

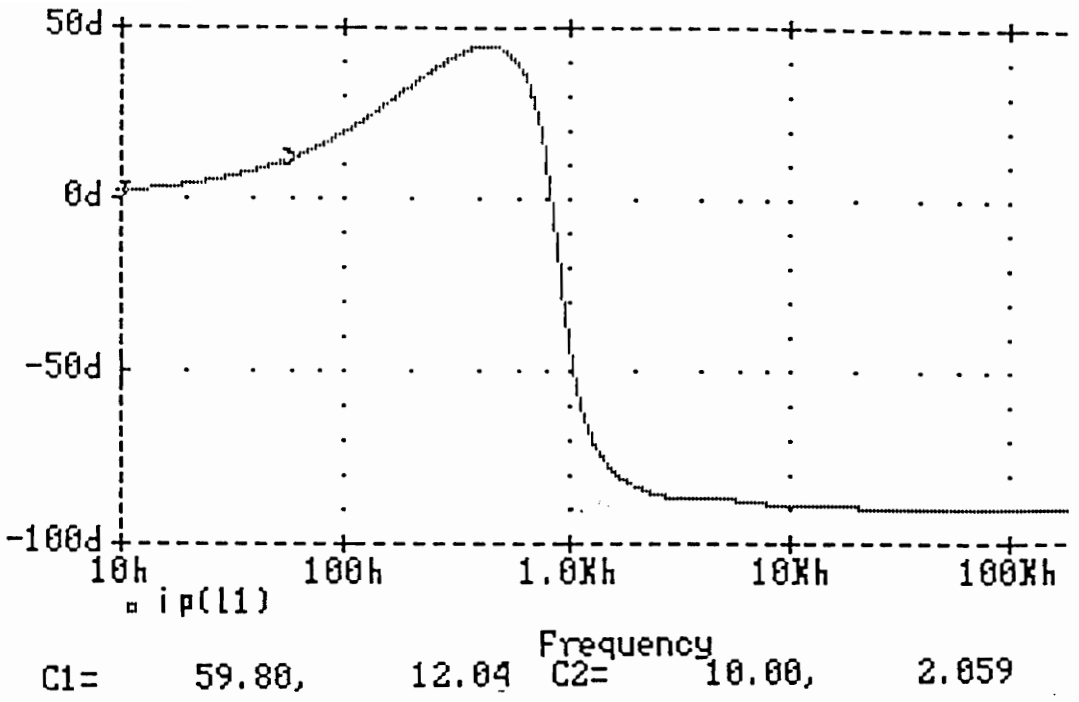



Fig. 3.11a Input impedance phase for $f_4$= 600 Hz

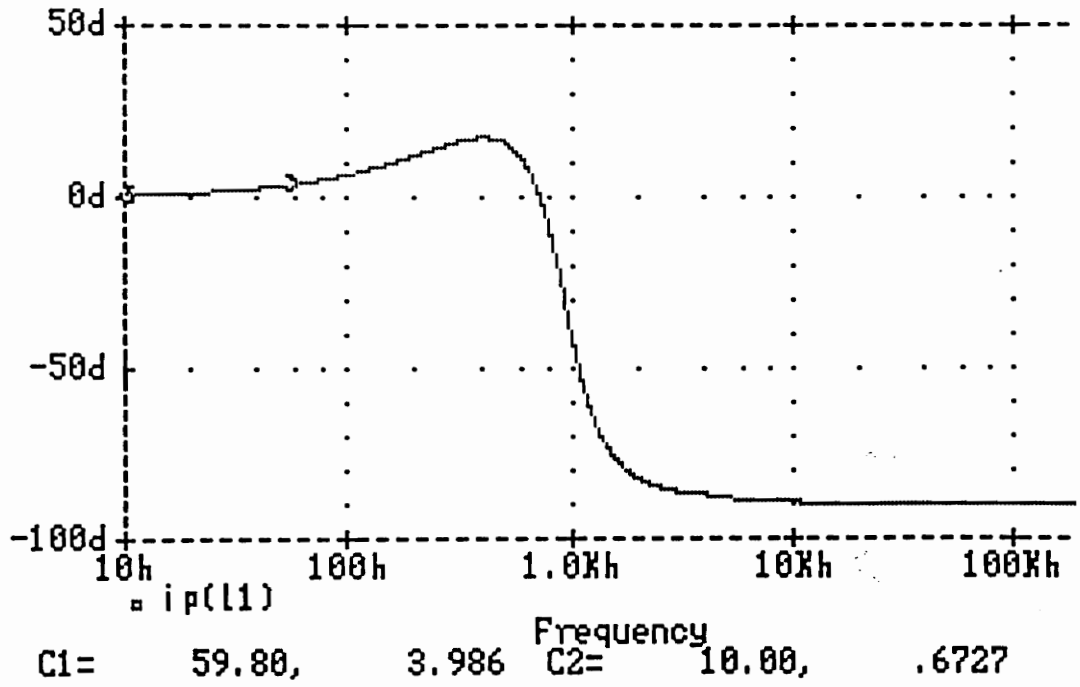



Fig. 3.10a Input impedance phase for $f_4$= 300 Hz

TABLE 3.12

| $f_x[Hz]$ | $f_3[KHz]$ | $Z_{outmax}$ | $R_{in}$ | $Q_{max}$ |
|---|---|---|---|---|
| 11 | 1.8 | 40.5 | 59 | < 19 |

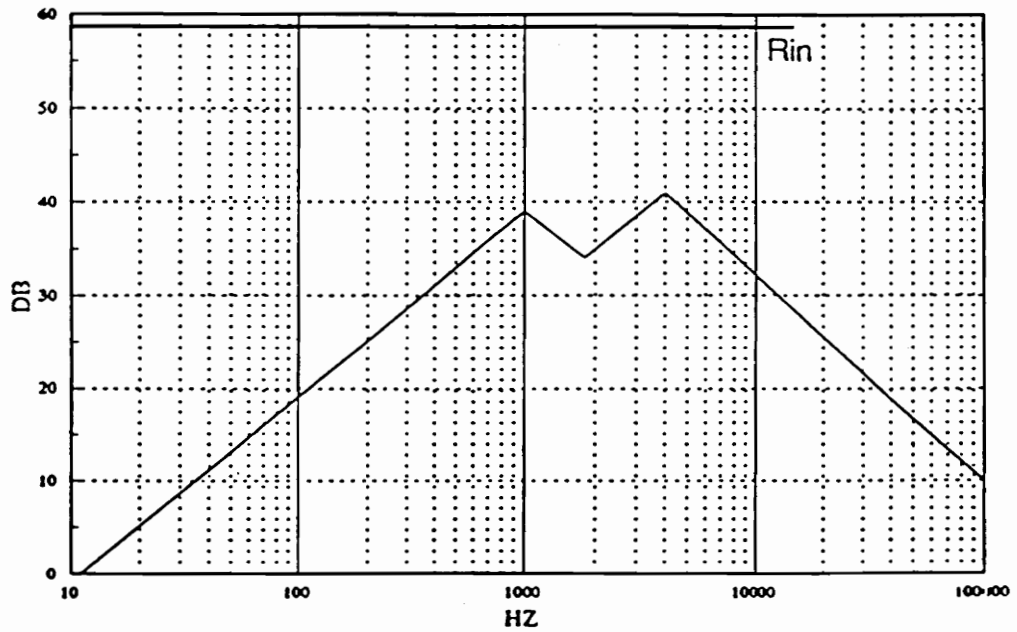



Fig. 3.12 Output impedance asymptote

TABLE 3.13

| $R_c\,[\Omega]$ | $Q_1\,[dB]$ | $Q_2\,[dB]$ | $A_{30}\,[dB]$ | $C_3\,[\mu F]$ | $A_{30C3}\,[\mu F]$ |
|---|---|---|---|---|---|
| 19.3 | 10.1 | 9.2 | -77.3 | 0.25 | -80.6 |

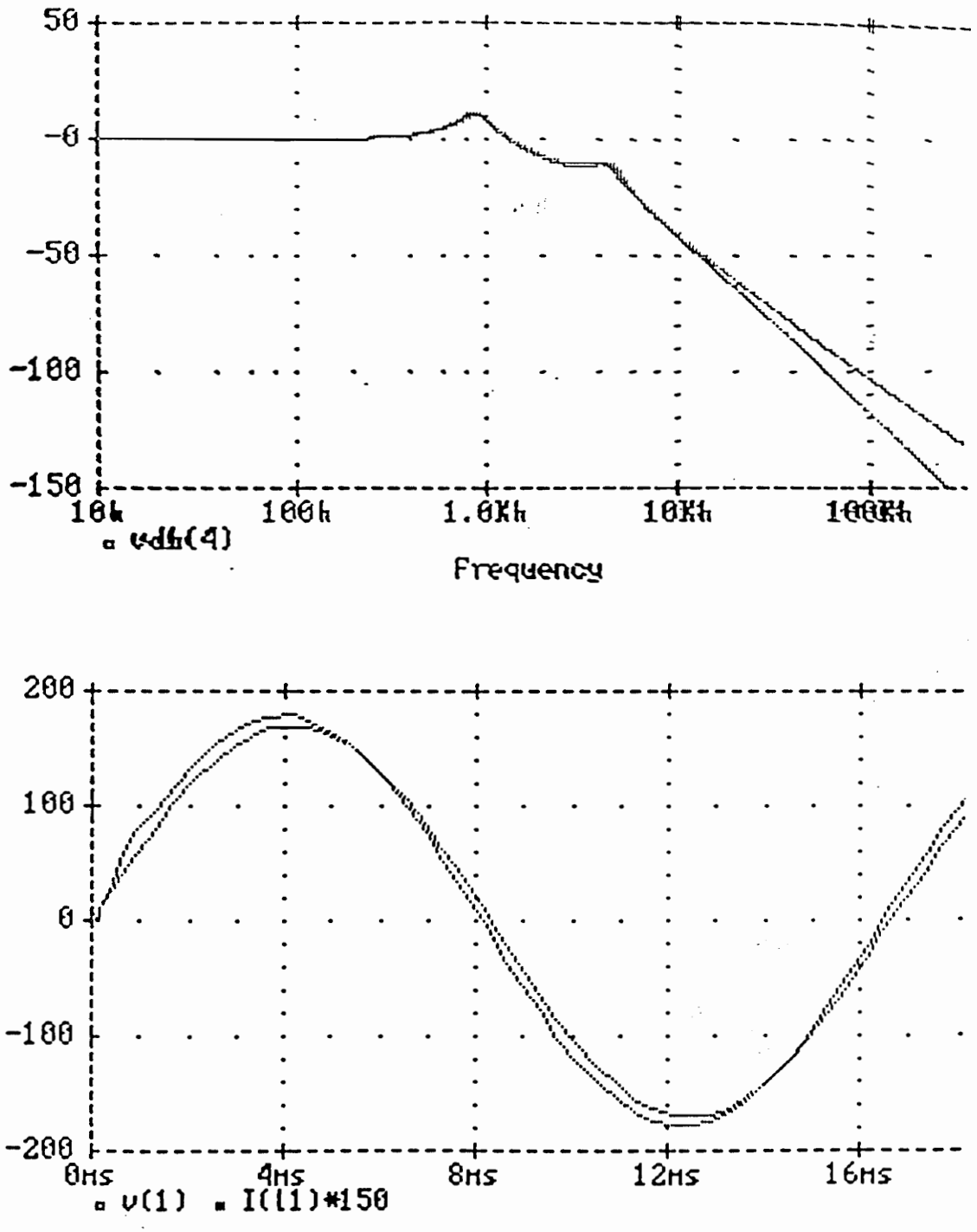



Fig. 3.13 Final filter design simulation with C3

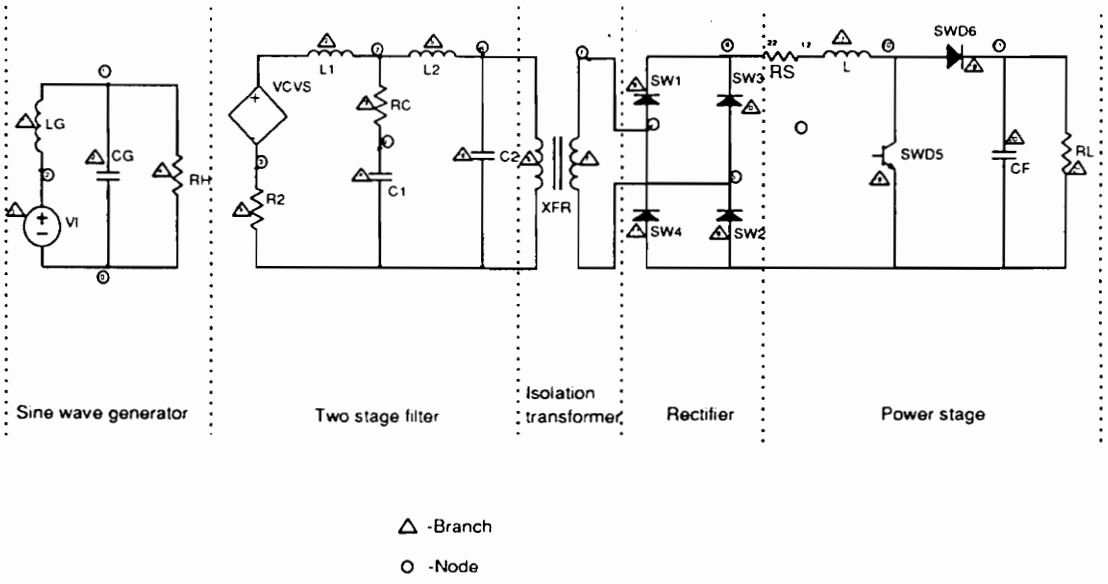



Fig. 3.14 Schematic of power factor correction circuit with input filter for COSMIR simulation

TABLE 3.15A

| $K_A[dB]$ | $f_s[KHz]$ | $f_1[KHz]$ | $f_2[KHz]$ | $f_3[KHz]$ | $f_z[KHz]$ |
|---|---|---|---|---|---|
| -56 | 32 | 1.5 | 10 | 3 | 20 |

TABLE 3.15B

| $C_1[\mu F]$ | $C_2[\mu F]$ | $L_1[mH]$ | $L_2[mH]$ | $R_c[\Omega]$ |
|---|---|---|---|---|
| 1.81 | 0.36 | 6.25 | 0.84 | 29.5 |

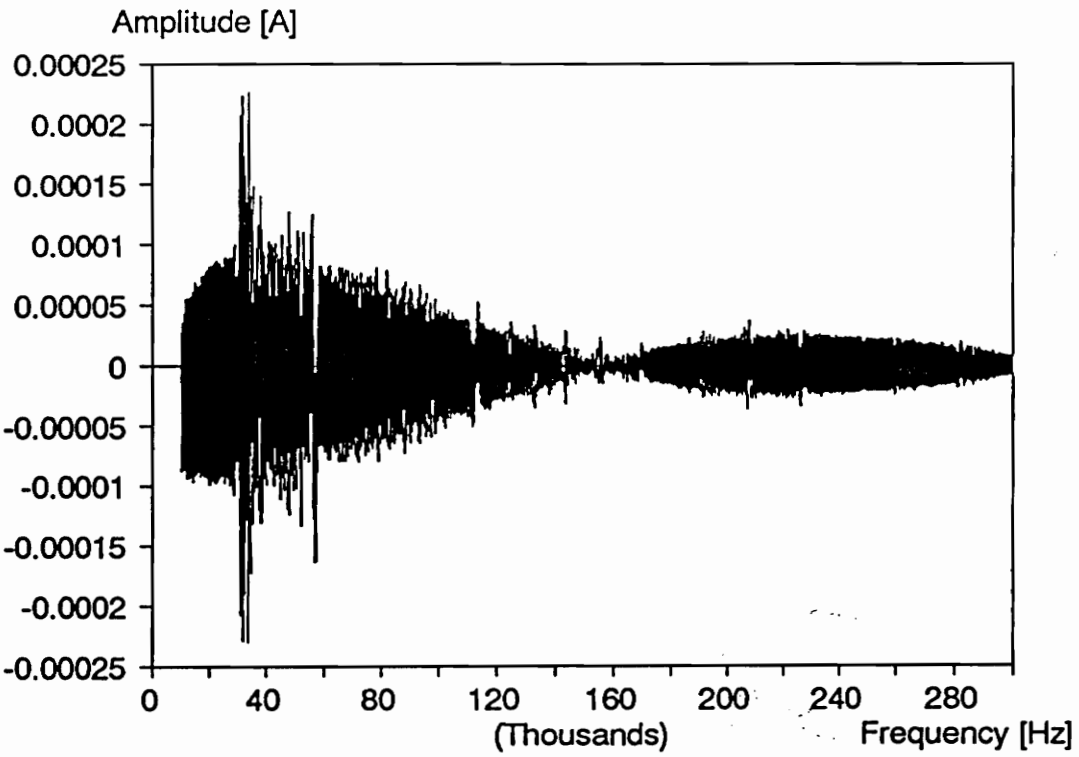



Fig. 3.15 Amplitude spectrum of input current with input filter

# CHAPTER 4. COMPARISION OF ON-TIME & HYSTERESIS P.F.C. WITH INPUT FILTERS

## *4.1 Introduction*

The proposed power factor correction circuit (P.F.C.) with controlled on-time control scheme was inspired by hysteresis control [3]. Therefore a more quantitative comparision of these two power factor correction circuits is made in this chapter. The objective of this chapter is twofold.

1. To derive the optimal design of the power stage with an input filter
2. To make a comparision of this power factor correction circuit with a power factor correction circuit with hysteresis control.

It is obvious that the inductor size for the controlled on-time P.F.C. which is operating at the boundary of CCM and DCM will be smaller than the inductor

of P.F.C. with hysteresis control for the same power, input and output voltage , and efficiency. But the input filter is an integral part of the power factor correction circuit, and therefore, for a complete and fair comparision, it must be taken into consideration. The input filter of the power factor correction circuit with controlled on-time will be bigger than the input filter for the power factor circuit with hysteresis control for the same power, due to the much higher input current ripple in controlled on-time P.F.C. At low power the controlled on-time power factor correction circuit should be more attractive due to its smaller combined size. But at higher power levels, the size of the filter for controlled on-time P.F.C. will become increasingly larger and its combined weight will become heavier than the P.F.C. with hysteresis control.

Power factor is becoming more and more important at levels much below 1 KW for office environments where there is a high concentration of personal computers or wordprocessors. So it is important to be able to define which topology will be more suitable for a given power level. To make power factor correction attractive to the customer, cost and simplicity will be the major factors. Faced with the two options of a cheaper converter with low power factor or one which costs a few dollars more but has almost unity power factor, the user will find the second option quite attractive. Therefore it is quite important to be able to define which topology is most suitable for a given power level.

## *4.2 Description Of The Procedure of Comparision*

Comparision between a power factor correction circuit with controlled on-time and a power factor correction circuit with hysteresis control (with input filter for both of them) has been done on basis of their minimum weights. Following is the procedure for the comparision:

- For the definition of the minimum weight of the power factor correction circuit with controlled on-time the computer aided nonlinear optimization program CADO [8] was used. (The nonlinear program for the minimum power stage weight is described in Section 4.4.1) To define the minimum weight of the power factor correction circuit with hysteresis control, the CADO program for its minimum weight from reference [3] was used.

- The minimum weights of the power stages of both the power factor correction circuits were defined using nonlinear optimization programs. For both the circuits, the input voltage, the output voltage, efficiency, and the output power were kept the same. For the power factor correction circuit with hysteresis control the hysteresis window $\delta$ was fixed at 30 %. The hysteresis window was fixed at 30 % as otherwise the nonlinear optimization program of the power factor correction circuit with hysteresis control tended to make it 200 % (where the size of the inductor is minimum).

- The designed power stages for the minimum weight which were obtained using CADO in the previous point were simulated using COSMIR [4]. The COSMIR results for the inductor current were used to generate the FFT of the inductor current. The FFT of the inductor current was used to define the filter attenuation requirement to meet the VDE specification.

- Two stage filters were designed for both power factor correction circuits, and values of $L_1$ and $L_2$ of the filters were defined.

- For defining the minimum weight of the filter inductors defined in the previous point, a nonlinear optimization program for the minimum weight of the inductor was written using CADO. It is described in Section 4.4.2. Using it, the weights of the filter inductors were defined. The total weight of the power factor correction circuits were then defined by adding the filter inductors weight and the power stage weight.

## *4.3 Results and Conclusions of the Comparision*

The procedure defined in Section 4.2 was used to compare the controlled on-time power factor correction circuit and a hysteresis power factor correction circuit at two power levels. The first comparision was made at a low power level of 100 W, and the second comparision was made at a higher power level of 500 W.

For both comparisions, the values of the input voltage, the output voltage, and the efficiency were kept the same. The results of the comparisions are given in Table 4.2.b for 100 W power level and in Table 4.1.b for the 500 W power level. From the results of the comparision, the following observations and conclusions can be made.

1. At both power levels, the weight of the power stage for the controlled on-time is less than the weight of the power stage in hysteresis control. Their difference increases at higher power levels.

2. At both power levels, the weight of the filter for the controlled on-time is more than the weight of the filter for hysteresis control. The weight of the filter for on-time control increases more rapidly at higher power levels than it does for hysteresis control.

3. At the low power level of 100 W, the total weight for the on-time control is less than the total weight for the hysteresis control. But with increasing power, the difference diminishes, and at 500 W the total weight for the hysteresis control becomes less.

4. The general conclusion that can be drawn is that the on-time control seems to be more suitable for lower power level applications of up to approximately 450 W. For power levels above 500 W, hysteresis control should be considered.

TABLE 4.1.a

| Power [W] | Input Voltage [V] | Output Voltage [V] | Efficiency [%] |
|---|---|---|---|
| 500 | 120 | 300 | 95 |

TABLE 4.1.b

| | | C.C.M. | | D.C.M. | |
|---|---|---|---|---|---|
| | | Inductor [mH] | Weight [gm] | Inductor [mH] | Weight [gm] |
| Power Stage | | 1.012 | 438.1 | 0.208 | 19.5 |
| Filter | $L_1$ | 0.695 | 105.3 | 3.43 | 560.7 |
| | $L_2$ | 0.085 | 8.7 | 0.26 | 32.4 |
| Total filter weight | | - | 114 | - | 593.1 |
| Total Weight | | - | 552.1 | - | 612.6 |

Fig. 4.1 Comparision of results at 500 W

TABLE 4.2.a

| Power [W] | Input Voltage [V] | Output Voltage [V] | Efficiency [%] |
|---|---|---|---|
| 100 | 120 | 300 | 95 |

TABLE 4.2.b

| | | C.C.M. | | D.C.M. | |
|---|---|---|---|---|---|
| | | Inductor [mH] | Weight [gm] | Inductor [mH] | Weight [gm] |
| Power Stage | | 7.94 | 211 | 1.04 | 19.5 |
| Filter | $L_1$ | 2.9 | 36 | 6.25 | 84 |
| | $L_2$ | 0.37 | 5.6 | 0.84 | 9.9 |
| Total filter weight | | - | 46.6 | - | 93.9 |
| Total Weight | | - | 252.6 | - | 113.4 |

Fig. 4.2 Comparision of results at 100 W

## 4.4 Nonlinear Optimization Design Routines

Two nonlinear optimization design routines (CADO) were developed to optimize the power stage inductor and the input filter inductors. The nonlinear design program can be broken into several elements: design variables and design constants, design equations, and design constraints. An objective function must also be expressed mathematically. The design variables, design equations, and design constraints are identified and put into the program in their proper forms. Each of these elements are described in detail in section 4.4.1 for the power stage and section 4.4.2 for the filter inductor.

### 4.4.1 Nonlinear Optimization Program For The Power Stage

#### 4.4.1.1 Design variables

The design variables are the unknown quantities which are selected by the optimization routine. For the power stage the following quantities are identified as the design variables:

- Efficiency of the power stage, $\eta$

- Core center leg width, $C_w$
- Inductor winding turns, $n$
- Copper size, $A_{cp}$
- Core window width, $W_w$
- Minimum switching frequency, $f_{smin}$

The output capacitor is determined by the given output voltage ripple and the holdup time, and therefore is not defined as a design variable. The inductor value is defined explicitly by the switching frequency; it therefore is also excluded from the design variable. Fig. 4.1 shows the physical layout of an EE core used for the inductor. There are four dimensions which determine an EE core: the center leg width, $C_w$, the center leg thickness, $C_t$ , the window width, $W_w$, and the window height, $W_h$. Only $C_w$ and $W_w$ are considered as design variables. The core thickness, $C_t$, is related to the core center leg width, $C_w$, by a design constant, $K_1$. The core window height, $W_h$, is related to the window width, $W_w$, by constant, $K_2$. The value of $K_1$ and $K_2$ are usually between 1 and 3 for a given manufacturer's core.

### 4.4.1.2 Design constants

Device characteristics, design specifications, and material parameters are known design constants. The design constants are given listed Table 4.3.

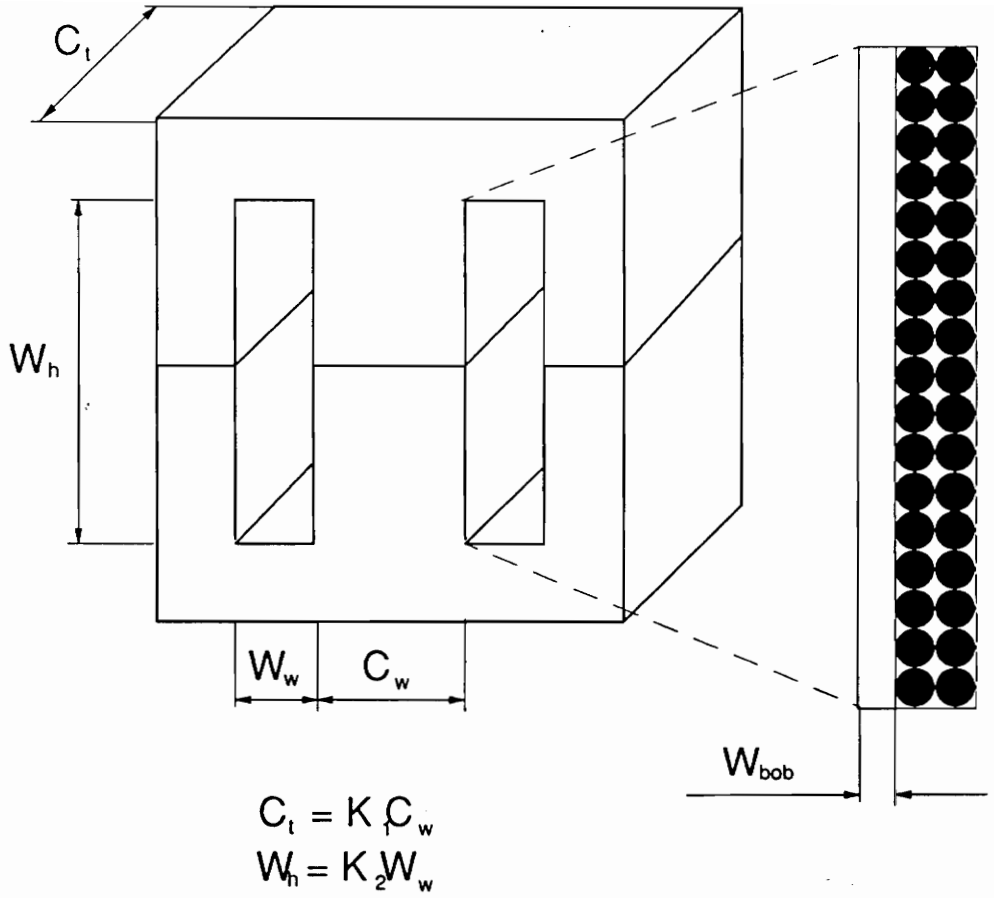



Fig. 4.1 Core geometry and winding layout of EE core

TABLE 4.3 POWER STAGE DESIGN CONSTANTS

| Elements | Symbols | Descriptions | Values |
|---|---|---|---|
| SWITCH MOSFET | $T_r$ | Turn-on rise time | 150 nS |
| | $T_f$ | Turn-off fall time | 150 nS |
| | $R_{ds}$ | On resistance | 0.5 Ω |
| | $C_g$ | Gate capacitance | 1300 pF |
| | $V_g$ | Gate voltage | 15 V |
| | $C_{oss}$ | Output capacitance | 210 pF |
| DIODE | $V_f$ | Foward drop | 0.65V |
| | $T_{dr}$ | Turn-on rise time | 100 nS |
| | $T_{df}$ | Turn-off fall time | 100 nS |
| INDUCTOR | $B_{sp}$ | Maximum flux density | 0.3 T |
| | $F_c$ | Winding pitch factor | 1.9 |
| | $F_w$ | Winding fill factor | 0.4 |
| | $W_{bob}$ | Bobbin thickness | 1.0 mm |
| | $K_1$ | Core leg aspect ratio | 1.0 |
| | $K_2$ | Window aspect ratio | 3.0 |
| | ρ | Copper resistivity | $1.72 \times 10^{-8}$ |

TABLE 4.3 (Cont)

| Elements | Symbols | Descriptions | Values |
|---|---|---|---|
| | $D_c$ | Copper density | $8900Kg/M^3$ |
| | $D_i$ | Core density | $7800Kg/m^3$ |
| INPUT VOLTAGE | $E_i$ | Nominal voltage amplitude | 170 V |
| | $E_{imin}$ | Low line voltage amplitude | 140 V |
| | $E_{imax}$ | High line voltage amplitude | 200 V |
| OUTPUT | $V_0$ | Output voltage | 300 V |
| | $P_0$ | Output power | 100-500 W |
| | $V_r$ | Output voltage ripple | 15 V |

### 4.4.1.3 Design equations

The design equations are used to calculate the circuit parameters that simplify the expressions for the constraints and objective functions. The design equations are explained in this section. The peak inductor current is given by:

$$I_p = \frac{4P_0}{E_i \eta}$$

The amplitude of the average inductor current is given by:

$$I_m = \frac{I_p}{2}$$

The maximum peak inductor current is defined as:

$$I_{pmax} = \frac{4P_0}{E_{imin} \eta}$$

The output filter capacitor can be calculated by:

$$C = \frac{V_p I_m}{2V_0 V_{r0}}$$

From Fig. 4.1 we can define the window area of the EE core as:

$$WA = K_2 W_w^2$$

The core cross sectional area, $A_p$, is:

$$A_p = K_1 C_w^2$$

The mean length turn, MLT, of the winding is:

$$MLT = 2(1 + K_1)F_c C_w$$

The mean magnetic path length, $Z_p$, measured through the center leg and around one of the outer legs is:

$$Z_p = 2(1 + K_2)W_w + \frac{\pi C_w}{2}$$

The power stage inductor, $L_f$, is defined as:

$$L_f = \frac{E_i^2(V_0 - E_i)}{4000 P_0 V_0 f_{smin}}$$

where $f_{smin}$ is the minimum switching frequency in Hz. The effective permeability, $\mu_{eff}$, is:

$$\mu_{eff} = \frac{L_f Z_p}{\mu_0 n^2 W A}$$

$\mu_0$ is the absolute permeability. $\mu_0 = 4\pi 10^{-7}$

The winding buildup, $B_w$, is:

$$B_w = \frac{nA_{cp}}{K_2 F_w W_w}$$

The core air gap, GAP, can be approximated as:

$$GAP = \frac{Z_p}{\mu_{eff}}$$

The inductor winding DC resistance, $R_l$ is given by:

$$R_l = \frac{n\rho MLT}{A_{cp}}$$

The maximum flux swing in the inductor core, $\Delta B$ is given by:

$$\Delta B = \frac{L_f I_{pmax}}{nA_p}$$

The weight of the inductor core, $Y_1$, is defined as:

$$Y_1 = D_i A_p Z_p$$

where $D_i$ is the core material density The weight of the inductor winding, $Y_2$. is:

$$Y_2 = nD_c A_{cp} XMLT$$

where $D_c$ is the copper density The switch loss (MOSFET), $P_q$, is the sum of the conduction loss, gate-source capacitance loss, output capacitance loss, and switching loss. From Appendix A1 to A4 and Chapter 2.

$$P_q = R_{ds} i_{swrms}^2 + C_g V_g^2 K_{freq} + \frac{2}{3} C_{coss} V_0^2 K_{freq} + \frac{(V_0 I_p T_{fall} K_{freq})}{3.57}$$

where $T_{fall}$ is the fall time of the MOSFET. The diode loss, $P_d$, is the sum of the switching loss and conduction loss. Referring to Appendix A and Chapter 2 we have:

$$P_d = \frac{(V_0 I_p T_{rise} K_{freq})}{3.57} + \frac{2E_i}{\pi V_0} \frac{P_0 V_f}{V_0}$$

where $T_{rise}$ is the rise time of the MOSFET. The inductor loss, $P_f$, includes the copper loss and the core loss. The core loss expression is derived from reference [8]

$$P_f = R_l i_{lrms}^2 + 23.1 A_p Z_p \left[ \Delta \frac{B}{3.6} \right]^{2.6} \left[ \frac{K_{freq}}{2} \right]^{1.3}$$

The efficiency of the power stage,. $\eta$, is defined as:

$$\eta = \frac{P_0}{P_0 + P_q + P_d + P_f}$$

### 4.4.1.4 Design constraints

The physical design problem has a number of constraints which must not be violated when selecting design variables. Design constraints can be specified to be either equalities or inequalities. The constraints can be functions of design variables, constants or parameters defined by the design equations. For the power stage ten design constraints have been identified. These are:

- This design constraint is the minimum efficiency constraint.

$$\eta \geq EFFUSER$$

where EFFUSER is the designer specified efficiency. This is used to force the program to meet the minimum efficiency requirment. The program will always give circuit components with the specified EFFUSER requirement satisfied.

- This constraint ensures that the winding and the bobbin can fit into the selected core window area.

$$WA > \frac{nA_{cp}}{F_w} - W_{bob}K_2W_w$$

- This constraint prevents inductor core saturation.

$$B_{sp} = \frac{I_{pmax}L_f}{nA_p}$$

- This constraint limits the maximum efficiency that can be achieved

$$\eta < 1$$

- This limits the minimum wire size

$$A_{cp} \geq 7.29 \times 10^{-8} \quad (30AWG)$$

- These two constraints are related to practical core size considerations.

$$C_w \geq C_w^{min}$$

$$W_w \geq W_w^{min}$$

where $C_w^{min}$ and $W_w^{min}$ are the minimum core size for a given manufacturer's core.

- This constraint gives the fact that the minimum number of turns cannot be less than one

$$n \geq 1$$

- This constraint is used to limit the minimum switching frequency

$$f_{smin} \geq FSUSER$$

where FSUSER is the designer defined minimum switching frequency.

- The minimum efficiency cannot be less than 50%

$$\eta > 0.5$$

#### 4.4.1.5 Objective function

The objective of the boost power factor correction circuit optimization is to minimize its weight. As the output capacitor is fixed as soon as the output voltage ripple is specified, the only component that affects the weight of the circuit is the inductor. Therefore, the objective function is:

$$F = Y_1 + Y_2$$

Where F is the objective function of the power stage, $Y_1$ is the inductor core weight, and $Y_2$ is the winding weight.

#### 4.4.1.6 Design output

The design output can be the final selected value of the variables, or any useful parameter defined in the design equation. The following parameters are printed after the program is run.

- Efficiency, $\eta$
- Inductor, $L_f$
- Inductor turns, $n$
- Wire size, $A_{cp}$
- Core center-leg width, $C_w$
- Core window width, $W_w$

- Output capacitance, $C_f$
- Inductor weight, $F$
- Inductor wire dc resistance, $R_l$
- Effective permeability and core gap, $\mu_{eff}, GAP$
- The maximum and average current amplitude, $I_p, I_{in}$
- The transistor and diode losses, $P_q$, $P_d$
- The filter loss, $P_f$
- The minimum switching frequency, $F_{smin}$

## *4.4.2 Nonlinear Optimization Program For The Filter Inductor*

### 4.4.2.1 Design variables

This nonlinear optimization program optimizes a given filter inductor for minimum weight. For this routine the parameters listed below are identified as the design variables:

- Core center leg width, $C_{wf}$
- Inductor turns, $n_f$
- Copper size, $A_{cpf}$
- Core window width, $W_{wf}$

An EE core is considered for the inductor of the filter. There are four dimensions which characterize an EE core. These are shown in Fig. 4.1. As discussed in Section 4.4.2.1, only two of these $C_{wf}$ and $W_{wf}$ (Core center-leg width and core window width) are considered as variables. The other two, core center leg thickness $C_{tf}$, and core window height $W_{hf}$ are expressed through the constants $K_1$ and $K_2$.

### 4.4.2.2 Design constants.

The design constants are listed in Table 4.4

### 4.4.2.3 Design equations

The design equations are explained below. The output power of the filter is given by:

$$P_{0f} = \frac{P_0}{\eta}$$

The input rms voltage is:

$$V_{rmsf} = \frac{E_i}{\sqrt{2}}$$

The input rms current of the filter inductor is:

TABLE 4.4 FILTER INDUCTOR DESIGN CONSTANTS

| Elements | Symbols | Descriptions | Values |
|---|---|---|---|
| INDUCTOR | $B_{sp}$ | Maximum flux density | 0.3 T |
| | $F_c$ | Winding pitch factor | 1.9 |
| | $F_w$ | Windng fill factor | 0.4 |
| | $W_{bob}$ | Bobbin thickness | 1.0 mm |
| | $K_1$ | Core leg aspect ratio | 1.0 |
| | $K_2$ | Window aspect ratio | 3.0 |
| | $\rho$ | Copper resistivity | $1.72 \times 10^{-8}$ |
| | $P_0$ | Output power of boost converter | |
| | $\eta$ | Converter efficiency | |
| | $E_{if}$ | Nominal input voltage amplitude | |
| | $E_{imin}$ | Low line input voltage amplitude | |

$$I_{rmsf} = \frac{P_{0f}}{V_{frms}}$$

The maximum filter inductor current ripple can be approximated by:

$$I_{pf} = \frac{2P_0}{E_{imin}\eta}$$

All filter core parameters, such as the core window area, WAF, the core cross sectional area, $A_{pf}$, the mean length turn, MLTF, the mean magnetic path length, $Zpf$, winding build-up, $B_{wf}$, effective permeability, $\mu_{eff}$, core air gap, GAPF, and the inductor winding resistance, $R_{lf}$ are given by expressions which are exactly same as in the previous optimization routine for the power stage core (in Section 4.4.2.3.) Therefore, they are not repeated here.

The maximum flux swing in the inductor core, $\Delta B_f$, is given by:

$$\Delta B_f = \frac{I_{pf}L_f}{A_{pf}n_f}$$

The losses in the filter are the conduction loss, $P_{rf}$, and the core loss, $P_{cf}$. They are defined as:

$$P_{rf} = I_{rmsf}^2 R_{lf}$$

$$P_{cf} = 23.1 A_{pf} Z_{pf} \left[ \frac{\Delta B_f}{3.6} \right]^{2.6} (120)^{1.3}$$

The efficiency of the inductor is given by:

$$\eta_f = \frac{P_{0f}}{P_{0f} + P_{rf} + P_{cf}}$$

The filter inductor weight is defined by the core weight, $Y_1$, and the copper weight, $Y_2$:

$$Y_1 = D_i A_{pf} Z_{pf}$$

$$Y_2 = n_f D_c A_{cpf} XMLTF$$

### 4.4.2.4 Design contraints

For this optimization program seven design constraints are identified. They are listed below:

- This design constraint is the minimum efficiency constraint,

  where EFFUSERF is the designer specified efficiency.

- This constraint ensures that the winding and the bobbin can fit into the selected core window area

$$WAF > \frac{n_f A_{cp}}{F_w} - W_{bob} K_2 W_w$$

- This constraint prevents inductor core saturation

$$B_{sp} = \frac{I_{pf} L_f}{n_f A_{pf}}$$

- This constraint limits the maximum efficiency that can be achieved

$$\eta_f < 1$$

- This limits the minimum wire size

$$A_{cpf} \geq 7.29 \times 10^{-8} \quad (30AWG)$$

- These two constraints are related to the practical core size considerations

$$C_{wf} \geq C_{wf}^{\min}$$

$$W_{wf} \geq W_{wf}^{\min}$$

where $C_{wf}^{\min}$ and $W_{wf}^{\min}$ are the minimum core size for a given manufacturer's core.

- This constraint gives the fact that the minimum number of turns cannot be less than one

$$n_f \geq 1$$

### 4.4.2.5 Objective function

The objective of this optimization routine is to minimize the weight of the filter inductor. Therefore, the objective function is:

$$F = Y_1 + Y_2$$

Where F is the objective function , $Y_1$ is the inductor core weight, and $Y_2$ is the winding weight.

### 4.4.3.4 Design output

The following parameters are printed after the program is run.

- Efficiency, $\eta_f$
- Inductor turns, $n_f$
- Wire size, $A_{cpf}$
- Core center-leg width, $C_{wf}$
- Core window width, $W_{wf}$
- Inductor weight, $F$
- Inductor wire dc resistance, $R_{lf}$
- Effective permeability and core gap, $\mu_{eff}, GAPF$

# CHAPTER 5. HARDWARE IMPLEMENTATION OF THE P.F. CORRECTION CIRCUIT

## *5.1 Introduction*

A 100 W power factor correction circuit with controlled on-time with a two stage input filter was implemented on a breadboard. The control circuit for the controlled on-time power factor correction circuit, described in Chapter 2 with a functional diagram (Fig. 2.3), was implemented using discrete components, (explained in Section 2). The breadboard performance is discussed in Section 3. The loop was closed for a resistive load. Ridley's small signal switch model [10] for power factor correction circuit with hysteresis control is shown to be applicable for the power factor correction circuit with controlled on-time and has been used.

The open loop and closed loop small signal measurements are shown in Section 4.

## *5.2 Control Circuit*

The detailed control circuit for the closed loop implementation of the controlled on-time power factor correction circuit is shown in Fig. 5.1. There are two comparators, 'A' and 'B'. An LM311 have been used for these comparators. Comparator 'A' compares the sensed inductor voltage to a very small negative voltage on its inverting input. This forces the output of the comparator high (to set the flip-flop and turn on the MOSFET) when the inductor current ramps down to zero and the sensed inductor voltage rises to zero. Comparator 'B' compares the on-time ramp with control voltage $V_c$. The on-time ramp is started when the MOSFET is switched on. When the on-time ramp becomes greater than the control voltage, the output of the comparator goes low, resetting the flip-flop and thereby turning off the MOSFET. The on-time ramp is generated by current source LM 334Z feeding the capacitor. The capacitor has a bypass switch (2N2222). When the switch is off, the current source feeds the capacitor and the linear on-time ramp is generated. A start up circuit is needed to initially start the circuit and is deactivated when the control circuit takes over. The current source LM 334Z can easily and more cheaply be implemented using discrete elements. DS 0026 is used as the MOSFET driver. A notch filter and a compensator is

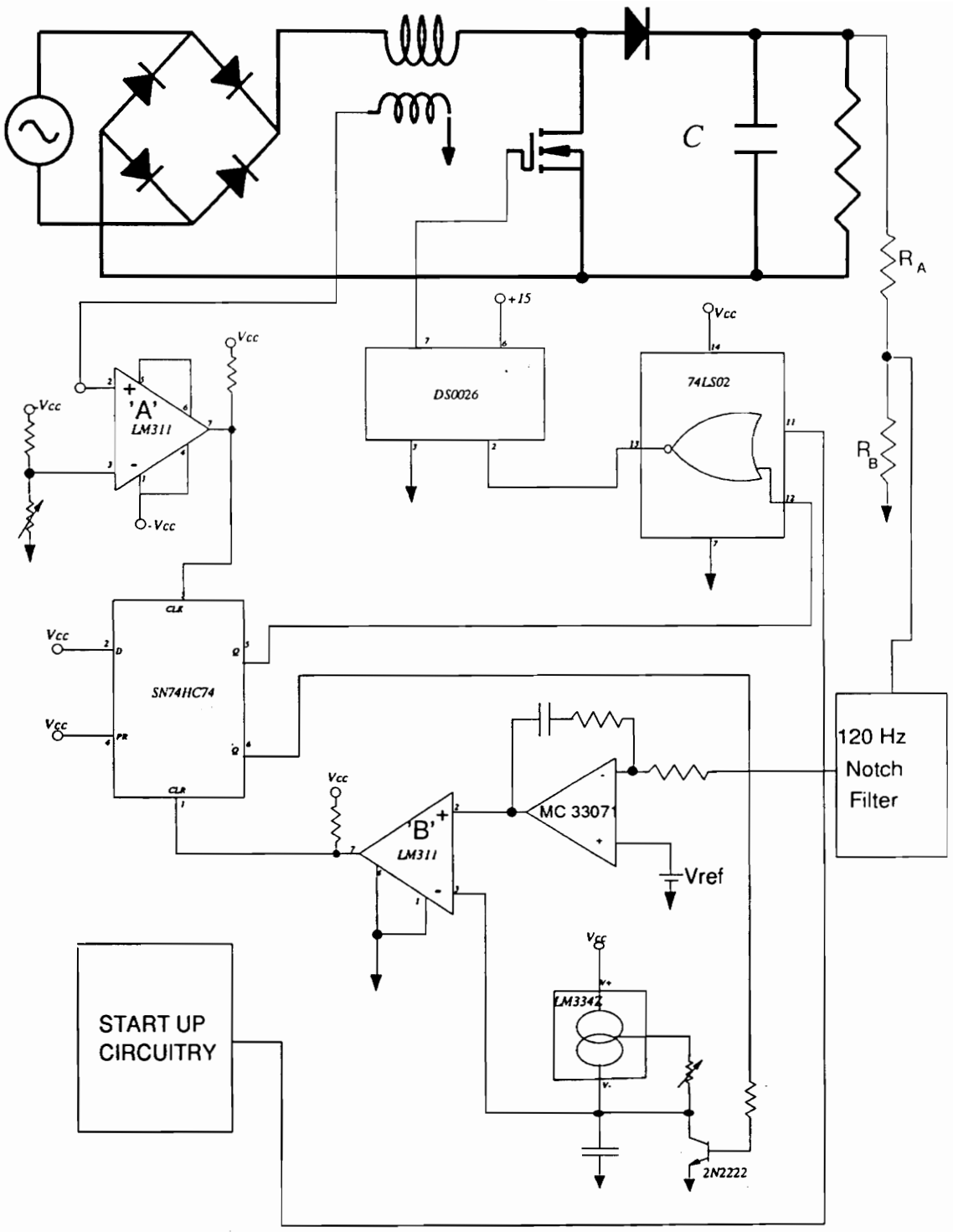



Fig 5.1 Control circuit for controlled on-time

needed to close the loop. Op-amp MC 33071 is used for the compensator. The compensator design is discussed in section 4. For open loop operation, a constant control voltage is fed to the non-inverting input of the comparator 'B'.

## *5.3 Breadboard Performance*

A 100 W output power, 300 V output voltage, 120 V rms input voltage power factor correction circuit with a two stage input filter was implemented on a breadboard. The power stage inductor, the capacitors, and the inductors of the input filter were built using the values obtained in the design example in Chapter 3. For the output capacitor, a 430 $\mu$F electrolytic capacitor was used.

Figure 5.2a shows the input voltage and the input current. It can be seen that with proper design of the input filter there is no phase shift between the input voltage and input current. Figure 5.2b shows the input voltage and output voltage. The output voltage ripple frequency is twice that of the input voltage. Figure 5.2c shows the power stage inductor current with its high frequency switching ripple. The maximum amplitude of the inductor current ripple is approximately twice the maximum value of the input current. Figure 5.2d shows the inductor current on an expanded time scale. Figure 5.2e and Fig. 5.2f show the control waveforms along with the inductor current waveform. It can be seen in Fig.5.2e that $V_c$ does not contain 120 Hz ripple. Figure 5.2f shows the same waveforms on an expanded time scale. The measured line voltage was $V_l$ = 119.8

(A) - Line voltage (50 V/ div.)
(B) - Line current (1 A/ div.)

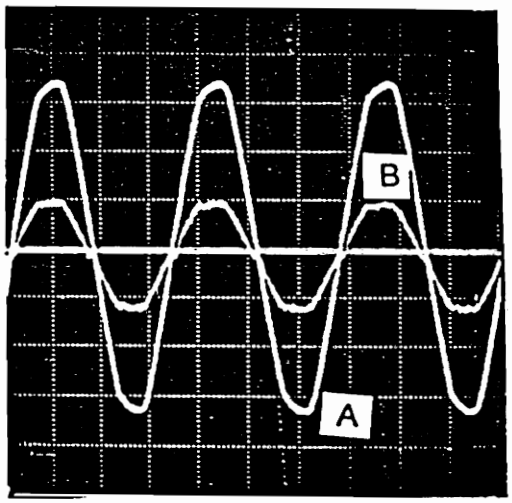



Fig. 5.2a Line voltage and line current

(A) - Input voltage (50 V/ div.)
(B) - Output voltage (10 V / div.)

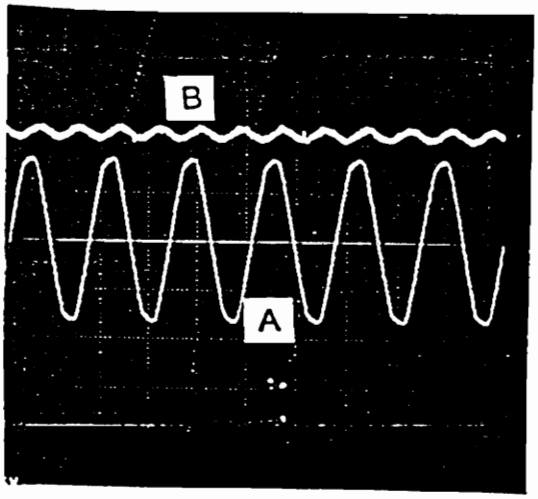



Fig. 5.2b Input voltage and output voltage

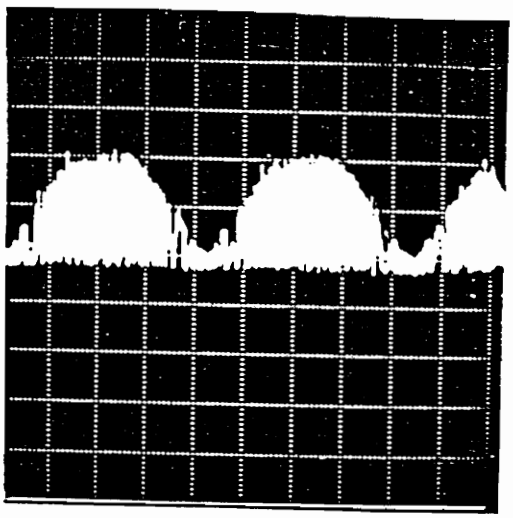


Fig. 5.2c Inductor current (1A/div)

Vertical scale - (1 A/ div)
Horizontal scale - (10 micro sec./ div.)

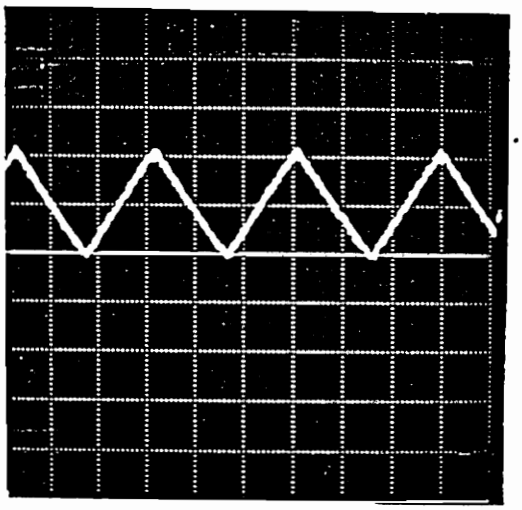
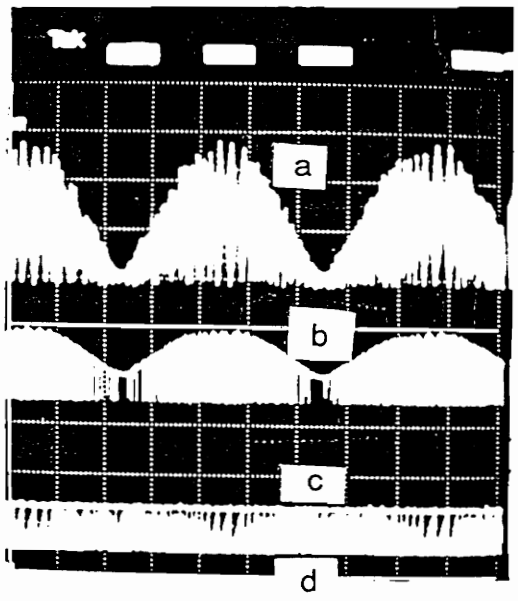
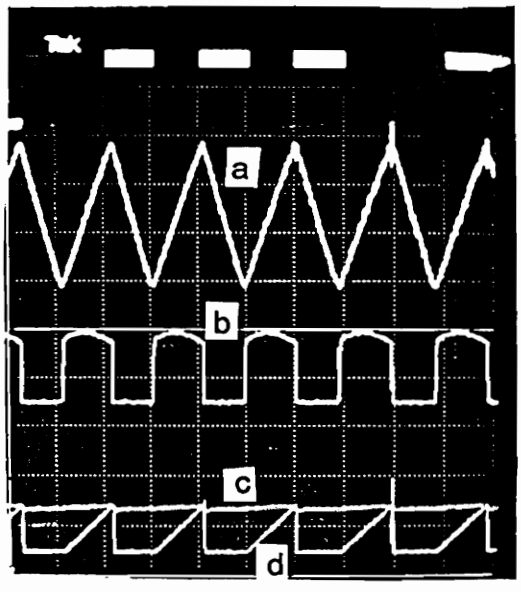


Fig. 5.2d Inductor current on expanded time scale




(a) - Inductor current (1A/div)
(b) - Inductor voltage (1V/div)
(c) - Control voltage Vc
(d) - On-time ramp (10V/div)

Fig. 5.2e Inductor current and control waveforms




(a) - Inductor current (1A/div)
(b) - Inductor voltage (1V/div)
(c) - Control voltage Vc
(d) - On-time ramp (10V/div)

Fig. 5.2f Inductor current and control waveforms on expanded time scale

V, the line rms current was $I_l$ = 0.84 mA, and the measured real input power was $P_{in}$ = 101 W. This gave a power factor of 0.996.

## 5.4 Small Signal Open And Closed Loop Measurements

The output of the power factor correction circuit needs to be regulated as it simplifies the regulation of the downstream converters. Ridley [10] developed a small signal switch model for the power factor correction circuit with hysteresis control. It is shown that this model can be applied for the power factor correction circuit with controlled on-time. Therefore the compensator design rules proposed by Ridley have been applied for this circuit.

### 5.4.1 Switch model review

For hysteresis control, the control law governing the input current is given by [10]:

$$i_i = \frac{v_i}{K} v_c, \tag{5.4.1.1}$$

where $i_i$ is the rms input current, $v_i$ is the rms input voltage, and $v_c$ is the control voltage (output of the compensator). For hysteresis control, this law is obvious. The switch model for the power factor correction circuit with hysteresis was de-

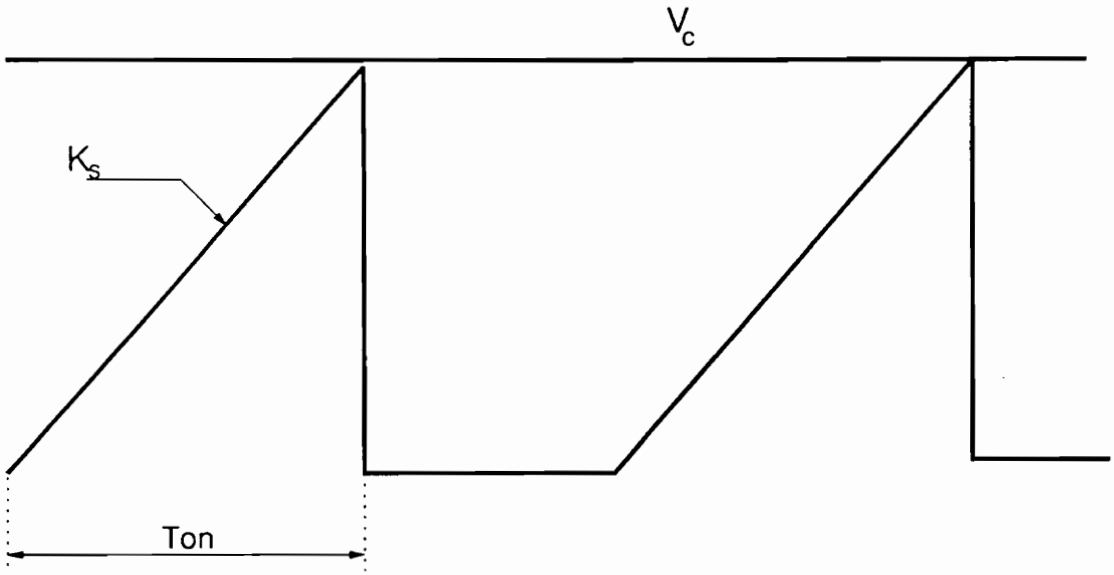



Fig. 5.3 On-timer ramp waveform

Fig. 5.4 A

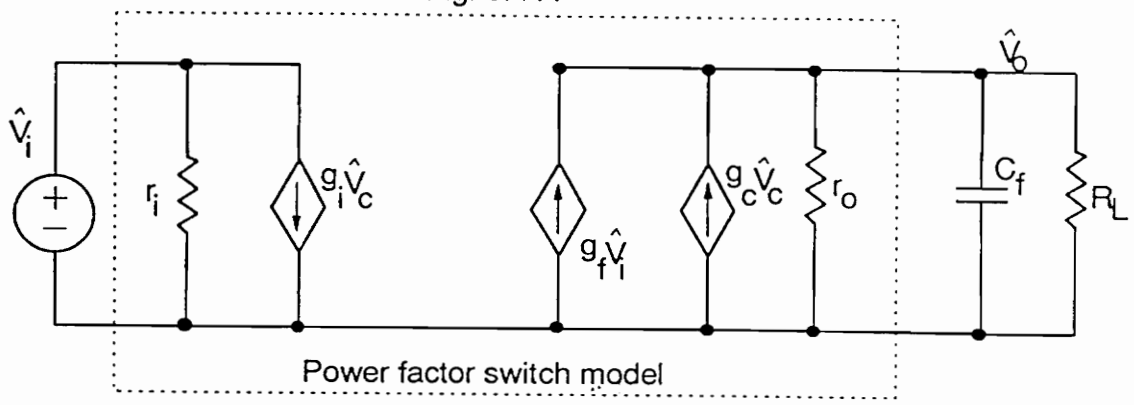



TABLE 5.4 B

| M | K | $K_s$ | $r_i$ | $g_i$ | $r_o$ | $g_f$ | $g_c$ |
|---|---|---|---|---|---|---|---|
| $\frac{V_o}{V_i}$ | $\sqrt{3}K_sL$ | $\frac{V_c}{T_{on}}$ | $\frac{r_o}{M^2}$ | $\frac{V_i}{K}$ | $\frac{V_o}{I_o}$ | $\frac{2M}{r_o}$ | $\frac{V_i}{KM}$ |

TABLE 5.4 C

| $P_o$ W | $V_{inom}(rms)$ V | $V_{imax}(rms)$ V | $V_{imin}(rms)$ V | $T_{on}$ μsec | $L_f$ mH | $C_f$ μF | $V_o$ V |
|---|---|---|---|---|---|---|---|
| 100 | 120 | 130 | 110 | 14.4 | 1.04 | 430 | 300 |

Fig.5.4 Switch Model

veloped based on this control law and the power balance equation. If the control law for the input current for the controlled on-time power factor circuit can be expressed in the form given by Eq. (5.4.1.1), then Ridley's small signal switch model will remain unchanged for on-time control.

For on-time control, the input rms current, derived in Chapter 2, was:

$$i_i = \frac{T_{on} V_p}{\sqrt{6}\, L}, \tag{5.4.1.2}$$

where $i_i$ is the input rms current, $V_p$ is the peak input voltage, and L is the power stage inductor. Or:

$$i_i = \frac{T_{on} v_i}{\sqrt{3}\, L}, \tag{5.4.1.3}$$

where $v_i$ is the input rms current. From Fig. 5.3 it can be seen that the on-time $T_{on}$ can be expressed in terms of the slope of the on timer ramp $K_s$ and the control voltage $V_c$:

$$T_{on} = \frac{V_c}{K_s}, \tag{5.4.1.4}$$

From Eq. (5.4.1.3) and (5.4.1.4) we get:

$$i_i = \frac{v_i}{K} v_c, \tag{5.4.1.5}$$

where

$$K = \sqrt{3}\, K_s L. \qquad (5.4.1.6)$$

Eq. (5.4.1.5) defines the control law for the input current for the on-time power factor correction circuit. It is exactly same as for the hysteresis control.

The small signal switch model is shown in Fig. 5.4a. Table 5.4b gives the parameters for the switch, and Table 5.3c gives the circuit component values for the 100 W, 300 V output voltage power factor correction circuit.

### 5.4.2 Open loop control to output measurements

The open loop control-to-output measurement set-up is shown in Fig. 5.5. The difficulty in this measurement is the high output voltage which can damage the input of the impedance analyzer. Textronics oscilloscope 2445, which has a signal out connector, has been used as a buffer and as an amplifier for the output voltage. The output voltage was attenuated by -40 dB. A low frequency perturbation is superimposed on the steady state open loop control volatge $V_c$ . This modulates the steady state on-time, and as a result, the inductor current and the output voltage are modulated.

From Ridley's switch model the control-to-output transfer function for the resistive load is given by:

$$\frac{\hat{v}_0}{\hat{v}_c} = \frac{G_1}{1 + \frac{s}{\omega_p}}, \qquad (5.4.2.1)$$

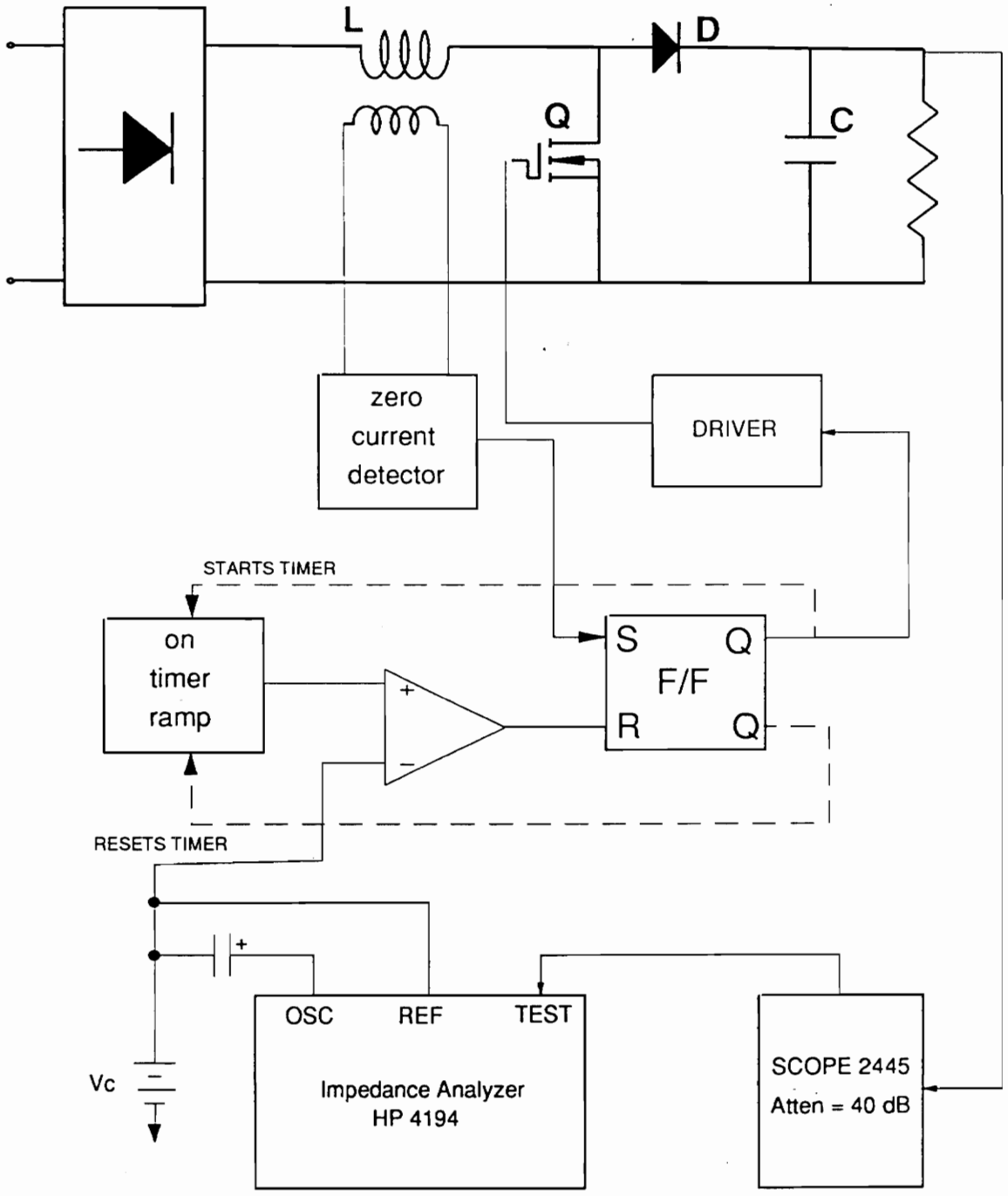



Fig. 5.5 Open loop control to output measurement set-up

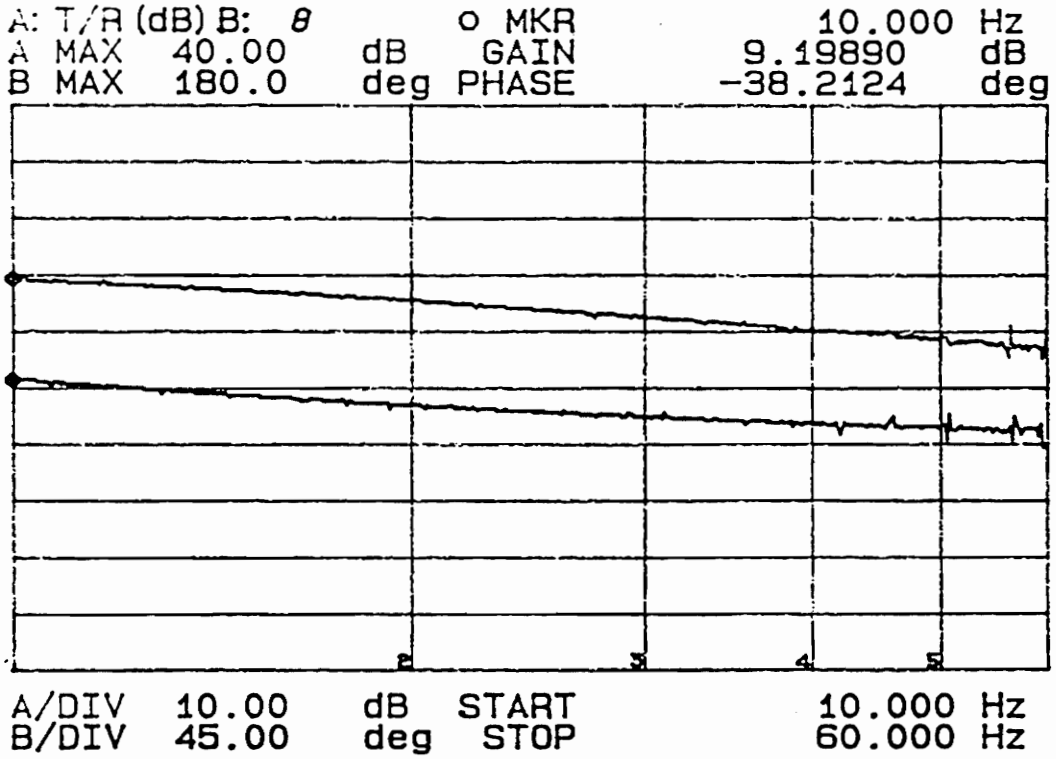



Fig. 5.6 Measured open loop control to output transfer function

where

$$G_1 = \frac{g_c R_L}{2}, \text{ and} \tag{5.4.2.2}$$

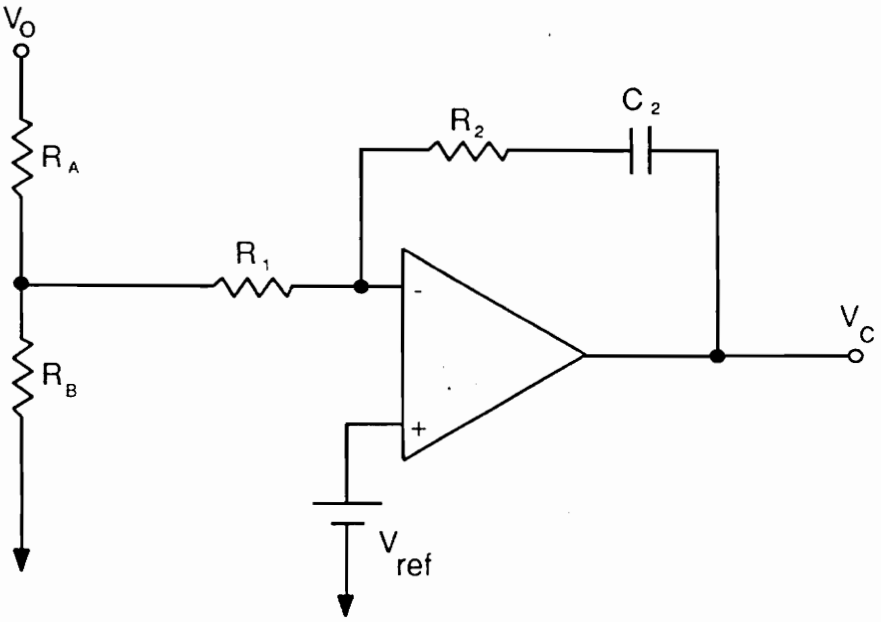
$$\omega_p = \frac{2}{C_f R_L}, \tag{5.4.2.3}$$

where $R_L$ is the load and $C_f$ is the output capacitor. The right half plane zero of the boost converter and the filter capacitor esr zero have been ignored because the rectified line frequency (120 Hz.) is much lower than these zeros.

The measured control-to-output transfer function is shown in Fig. 5.6. The -40 dB output voltage attenuation has to be taken into consideration when plotting the control-to-output transfer function. The pole $\omega_p$ is lower than 10 Hz, and therefore cannot be seen on the measurement.

### 5.4.3 Closed loop gain measurement

To close the loop, the compensator proposed by Ridley has been used. The integral and lead compensator works well for the on-time power factor correction circuit for resistive load. The integral and lead compensator can be implemented by the circuit shown in Fig. 5.7. The gain asymptote for this compensator is also shown in Fig. 5.7. For a resistive load the zero of the compensator should be located at the same frequency as the pole of the control-to-output transfer function



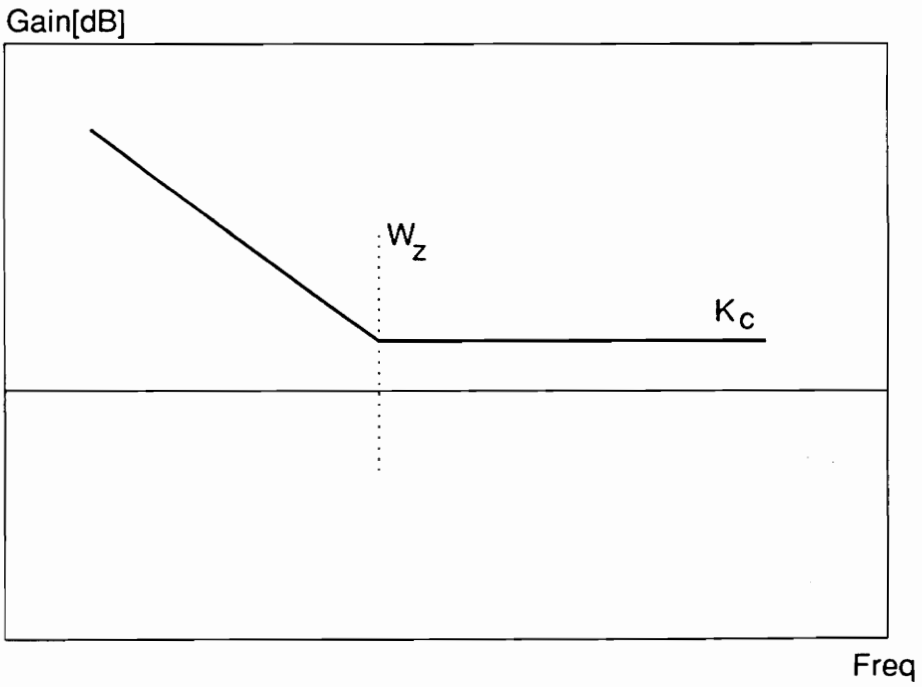




Fig. 5.7 Compensator network and it's gain asymptote

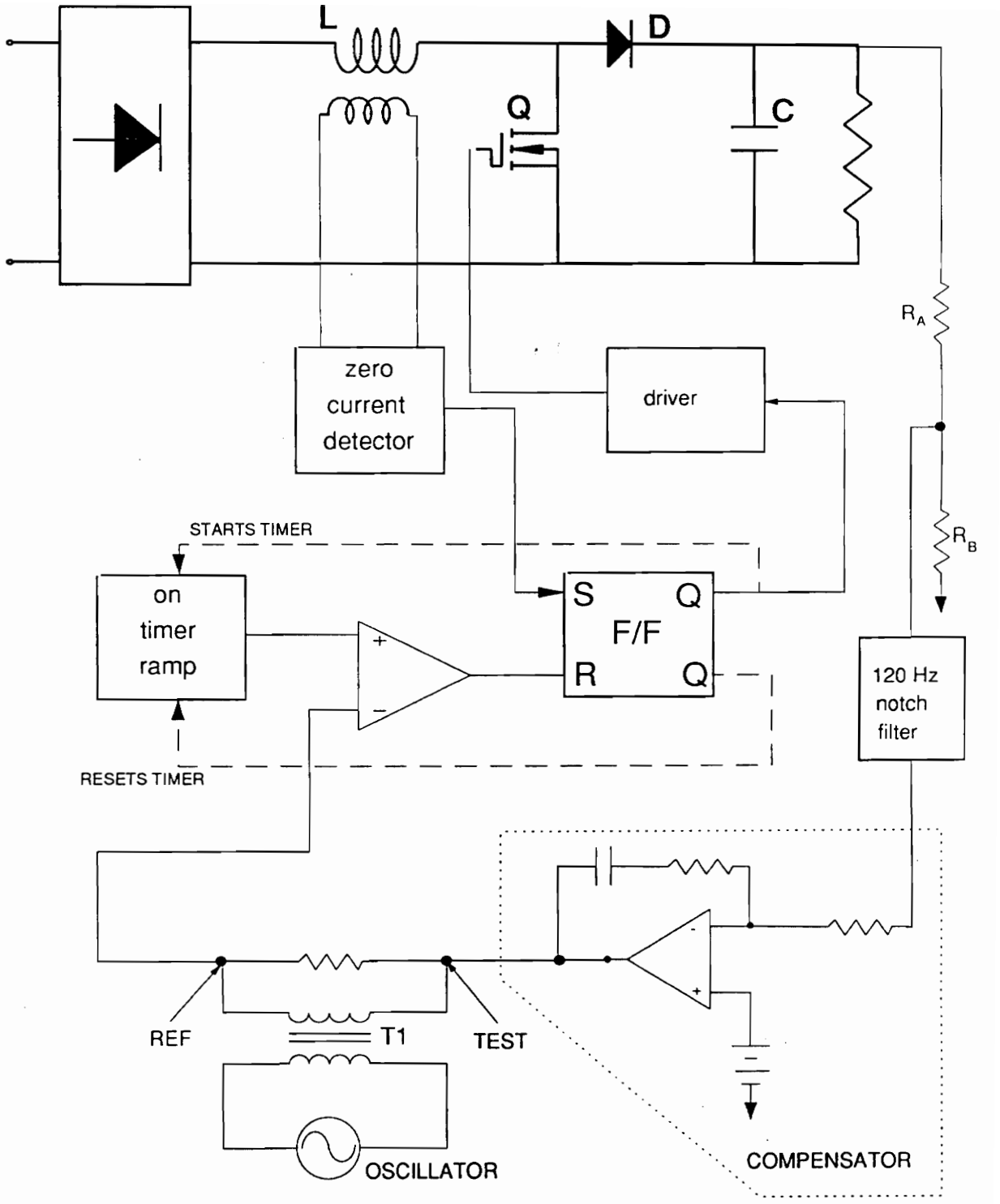



Fig. 5.8 Closed loop gain measurement set-up

given by Eq. (5.4.2.3). For the compensation network shown in Fig. 5.7, the zero $\omega_z$ and the high frequency gain $K_c$ are given by:

$$\omega_z = \frac{1}{R_2 C_2}, \text{ and} \tag{5.4.2.1}$$

$$K_c = \frac{R_2}{R_1}. \tag{5.4.2.2}$$

The high frequency gain $K_c$ can be defined as:

$$K_c = \frac{60\pi C_f}{\eta} \frac{KM_{\min}}{V_{imax}} \frac{R_A + R_B}{R_B}, \tag{5.4.2.3}$$

where $\eta$ is the efficiency, $M_{\min}$ is the ratio of the output voltage to the maximum input rms voltage, and $V_{imax}$ is the maximum rms input voltage. The compensator transfer function is given by:

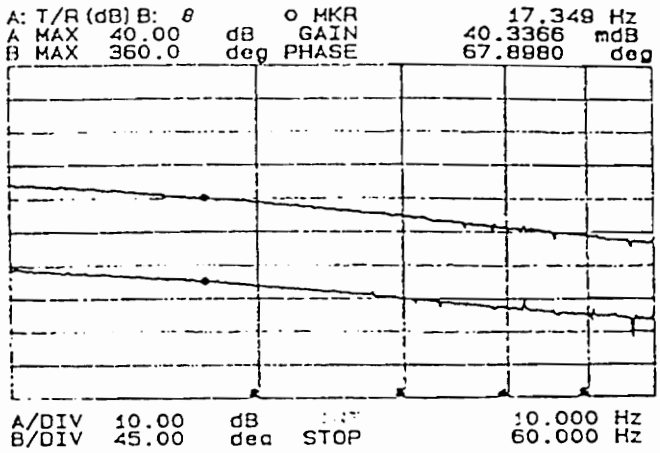
$$\frac{\hat{v}_c}{\hat{v}_o} = \frac{K_c \omega_z}{s}\left(1 + \frac{s}{\omega_z}\right). \tag{5.4.2.4}$$

From (5.4.2.1) and (5.4.2.4) the closed loop gain T can be defined as:

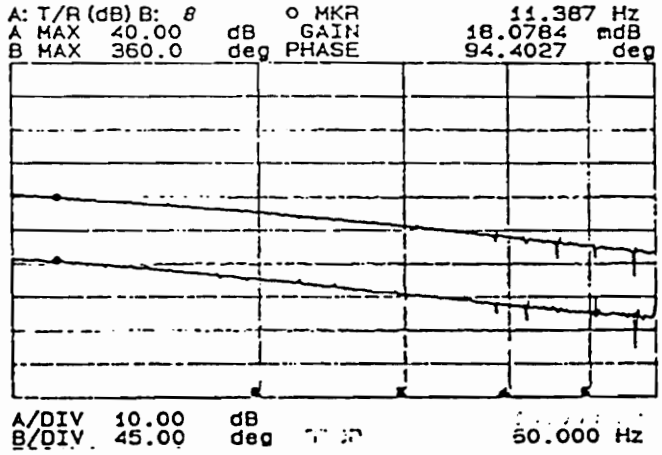
$$T = \frac{60\pi V_i M_{\min}}{V_{imax} M} \frac{1}{s}, \tag{5.4.2.5}$$

and the loop gain crossover frequency is given by:

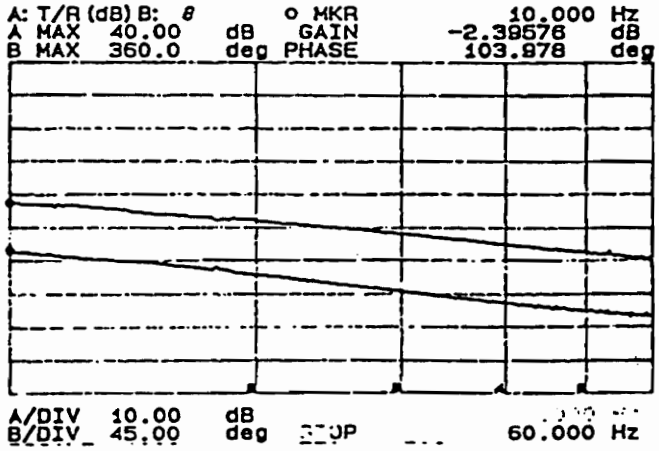
$$f_c = 30\left(\frac{V_i}{v_{imax}}\right)^2. \tag{5.4.2.6}$$




At high line (135V)




At nominal line (120V)




At low line (110 V)

Fig. 5.9 Closed loop gain measurement

Figure 5.8 shows the experimental set-up for measuring the closed loop gain T. Transformer T1 should be able to transfer the low frequency signal. Figure 5.9 shows the measured loop gain T for high line voltage (135 V rms), nominal line (120 V rms), and low line (110 V rms).

# CHAPTER 6. CONCLUSIONS

## *6.1 Present Contributions*

An active boost power factor correction circuit with controlled on-time is proposed which has a simpler control scheme than does an active power factor correction circuit with hysteresis control, and yet it still attains almost unity power factor. Analytical expressions are derived for the rms switch, diode and inductor currents, output filter capacitor, transistor and diode losses. These expressions are used in a nonlinear optimization program for the power stage.

Design guidelines for an input filter for this power factor correction circuit are established. It is shown that the conventional method of design for an input filter for the power factor correction circuit may introduce an unwanted phase shift between the input voltage and current, thereby degrading the power factor. The cause of this phase shift is explained, and design guidelines for the input filter are formulated. The input filter design is illustrated in a design example. Both

SPICE and COSMIR simulations are used to verify these design guidelines for the filter. The fast fourier transform (FFT) of the inductor current is used to more accurately define the attenuation requirement of the input filter.

A comparision between the power factor correction circuit with controlled on-time and a power factor correction circuit with hysteresis control (with input filters for both of them) is made on the basis of their minimum weights. The general conclusion of this comparision is that the on-time control seems to be more suitable for power levels up to approximately 450 W. For power levels above 500 W, hysteresis control should be considered.

A regulated 100 W, 120 VAC input, 300 V output power factor correction circuit with a two stage input filter was implemented on breadboard. With proper design of the input filter, the input voltage and current were in phase. A power factor of almost unity was attained. It is shown that the small signal switch model for the power factor correction circuit with hysteresis control developed by Ridley [10] can be applied to this control scheme. Therefore the design guidelines proposed by Ridley were successfully applied in designing the compensator and closing the loop.

## *6.2 Future Work*

The two stage input filter analyzed in this work is for differential mode noise. For the common mode noise, a common mode choke is required. Common mode

choke design for the power factor correction circuit should be studied. Ferrite has been used for the first stage inductor of the input filter. The value of this inductor is normally large. Use of a high permeability material, such as steel, could be investigated to reduce the size of this inductor.

# Appendix A DERIVATION OF THE ANALYTICAL EXPRESSIONS FOR THE POWER STAGE

## *A1. MOSFET RMS Current*

The difficulty associated with the derivation of the RMS current is due to variability of the switching frequency. Therefore, the RMS current is defined first for one switching period. Then the RMS current for the switch can be approximated by integrating it over the rectified line period. This approximation is reasonable, because the switching frequency is much higher than the 120 Hz rectified line frequency. Fig A.1 shows the switch current for an arbitrary switching period. The RMS current over one switching period can be defined as:

$$\begin{aligned}\frac{1}{t_2}\int_0^{t_2} i^2(t)\ dt &= \frac{1}{t_2}\int_0^{t_1}(bt)^2\ dt \\ &= \frac{1}{t_2}\frac{b^2 t_1^3}{3} \\ &= \frac{T_{on}}{T_{on}+t_{off}}\frac{b^2 T_{on}^2}{3} \\ &= d(t)\frac{b^2 T_{on}^2}{3}\end{aligned} \tag{A1.1}$$

where $bT_{on} = \Delta i_{on} = \dfrac{V_p}{V_0}\sin(\omega t)\, T_{on}$, $t_1 = T_{on}$, and $t_2 = t_{off}$. Substituting $d(t)$ and $bT_{on}$ in Eq (A1.1), and integrating it over one rectified line period, we get:

$$\begin{aligned} i_{swrms}^2 &= \frac{1}{T_s}\int_0^{T_s}\left[ d(t)\frac{b^2 T_{on}^2}{2}\right] \\ &= \frac{1}{3T_s}\int_0^{T_s}\left[\left(1-\frac{V_p}{V_0}\sin\omega t\right)\left(\frac{V_p^2}{L^2}(\sin\omega t)^2 T_{on}^2\right)\right]dt \end{aligned}$$

Taking the integral, we get the switch RMS current $i_{swrms}$:

$$i_{swrms} = \sqrt{\frac{T_{on}^2 V_p^2}{3L^2}\left[\frac{1}{2}-\frac{4\pi V_p}{3V_0}\right]}$$

where L is the power stage inductor, $V_p$ is the peak input voltage, $V_o$ is the output voltage, and $T_s = \dfrac{\pi}{\omega}$ .

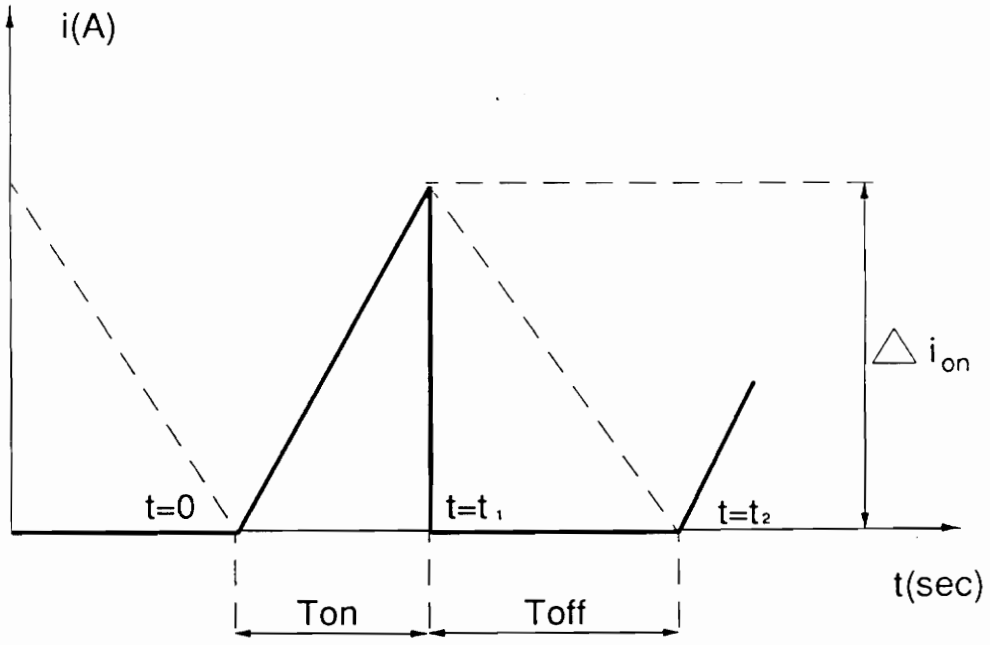



Fig. A.1 Switch current

## *A2. Diode RMS Current*

The diode RMS current is derived in the same way. Fig. A1.2 shows the diode current over one switching period. The diode RMS current over one switching period is defined as:

$$\frac{1}{T_{on}+t_{off}}\int_0^{T_{on}+t_{off}} i^2(t)\ dt = \frac{1}{T_{on}+t_{off}}\int_0^{t_{off}} (a-bt)^2\ dt$$

$$= \frac{t_{off}}{T_{on}+t_{off}}\left[ a(a-bt_{off}) + \frac{b^2t_{off}^2}{3} \right]$$

$$= d'(t)\frac{b^2t_{off}^2}{3}$$

where $bt_{off} = \Delta i_{on}$ , $d'(t) = 1 - d(t)$, and $a = \Delta i_{on} = \dfrac{V_p}{L}\sin \omega t \bullet T_{on}$. Then the diode RMS current is given by:

$$i_{drms} = \sqrt{\frac{1}{T_s}\int_0^{T_s}\left[ d'(t)\left( \frac{b^2t_{off}^2}{3} \right)\right] d(t)}$$

$$= \sqrt{\frac{4V_p}{3\pi V_0}\left[ \frac{V_p^2T_{on}^2}{3L^2} \right]}$$

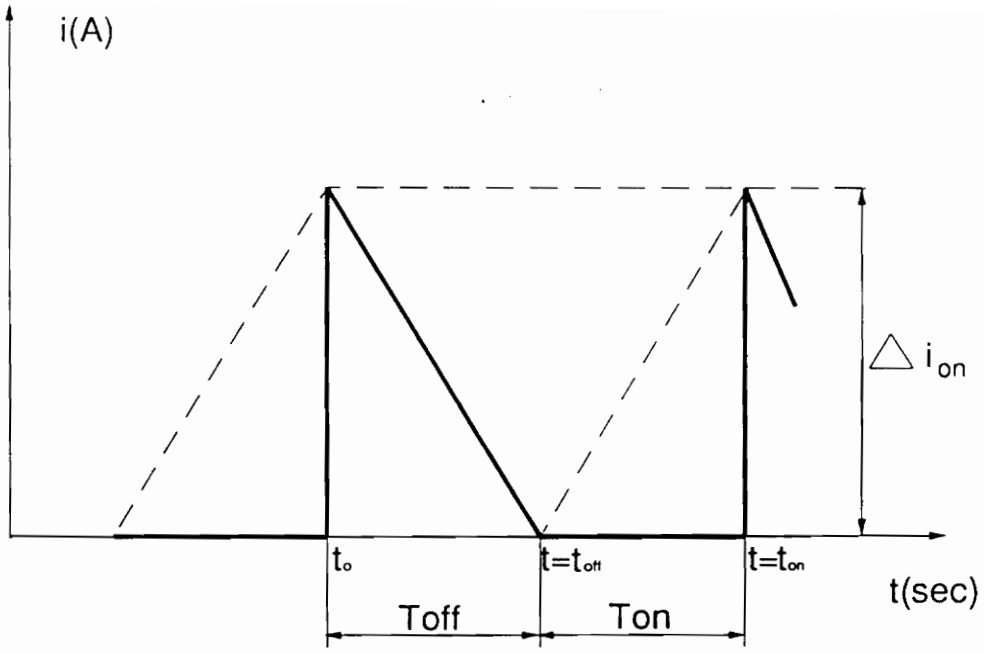



Fig. A.2 Diode current

## *A3. Inductor RMS Current*

The inductor RMS current can be derived using the expressions for the RMS currents for the diode and switch. Using KVL, we have

$$i_{lrms}(t) = i_{swrms}(t) + i_{drms}(t)$$

$$i_{lrms}^2(t) = i_{swrms}^2(t) + i_{drms}^2(t) + 2i_{swrms}(t)i_{drms}(t)$$

$$\text{since} \quad i_{swrms}(t)i_{drms}(t) = 0$$

Therefore:

$$i_{lrms}^2 = i_{drms}^2 + i_{swrms}^2,$$

then

$$\frac{1}{T_s}\int_0^{T_s} i_{lrms}^2(t)d(t) = \frac{1}{T_s}\int_0^{T_s} i_{swrms}^2(t)d(t) + \frac{1}{T_s}\int_0^{T_s} i_{drms}^2(t)d(t).$$

Substituting the values of $i_{swrms}$ and $i_{drms}$, we get:

$$i_{lrms} = \sqrt{\frac{T_{on}^2 V_p^2}{6L^2}} = \sqrt{\frac{1}{6} I_p^2}$$

## *A4. Switching Losses*

For estimation of the MOSFET and diode switching losses, the switching loss expression in reference [11] is used. In general it has the following expression for an inductive load:

$$\text{switch loss} = \frac{V_{ds} f_s}{2} (I_{d1} t_{rise} + I_{d1} t_{fall}),$$

where $V_{ds}$ is the transistor drain-source voltage when it is off, $f_s$ is the switching frequency, and $t_{rise}$ and $t_{fall}$ are the rise and fall times of the switch. For the controlled on-time power factor correction circuit, the boost power stage works at the boundary of DCM and CCM. The transistor waveform is shown in Fig. A3. For the transistor there are no losses during turn-on, and for the diode there is no loss during turn-off. $V_{ds}$ for the power factor ciruit with a boost topology is equal to the output voltage, $V_0$. The switching frequency is approximated by the $K_{freq}$ calculated in Chapter 2. The transistor and the diode losses are estimated by

$$P_q = \frac{V_0 K_{freq} I_p t_{fall}}{3.57}, \text{ and}$$

$$P_d = \frac{V_0 K_{freq} I_p t_{rise}}{3.57}.$$

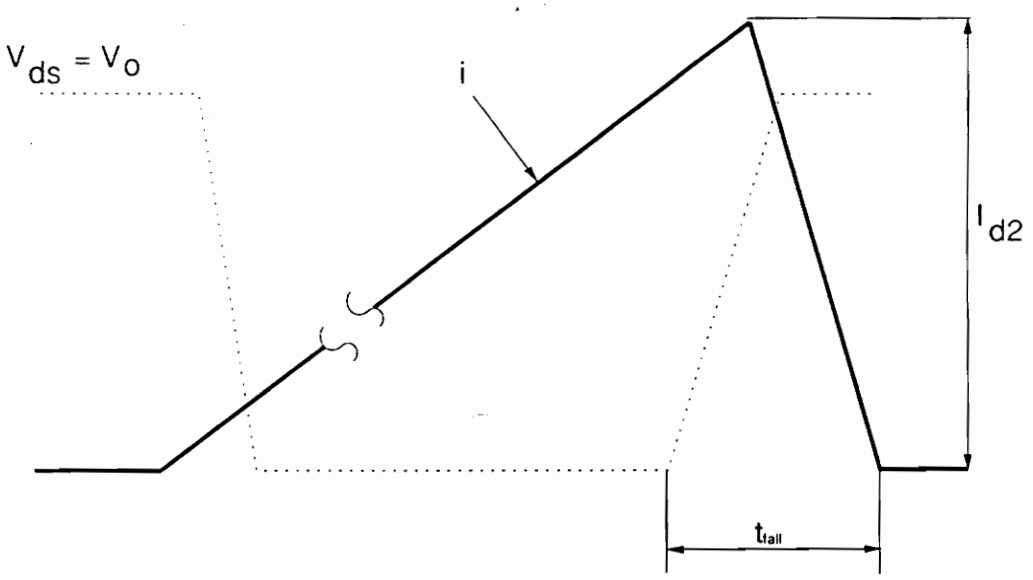



Fig. A.3 Switch current waveform for calculating losses

# Appendix B COSMIR FILE LISTING

## *B.1 Cosmir Files for P.F. Circuit Without Input Filter*

Two input files, INPUT1.DAT and INPUT2.DAT, are needed to run a COSMIR simulation. These are listed in Table C1.1 and Table C1.2. The circuit diagram for the COSMIR simulation is given in Fig. C.1. The numbers in the circle are the nodes, and the numbers in the triangle are the branch numbers. For the generation of the input sine wave, a parallel L-C resonant circuit is used. The values of the L and C of the resonant circuit determine the frequency of the generated input sine wave. The amplitude depends on the initial conditions of the L and C. The values of the L and C of the sine wave generator are selected by the following equation:

$$L = C = \frac{1}{2\pi f}, \qquad (C.1)$$

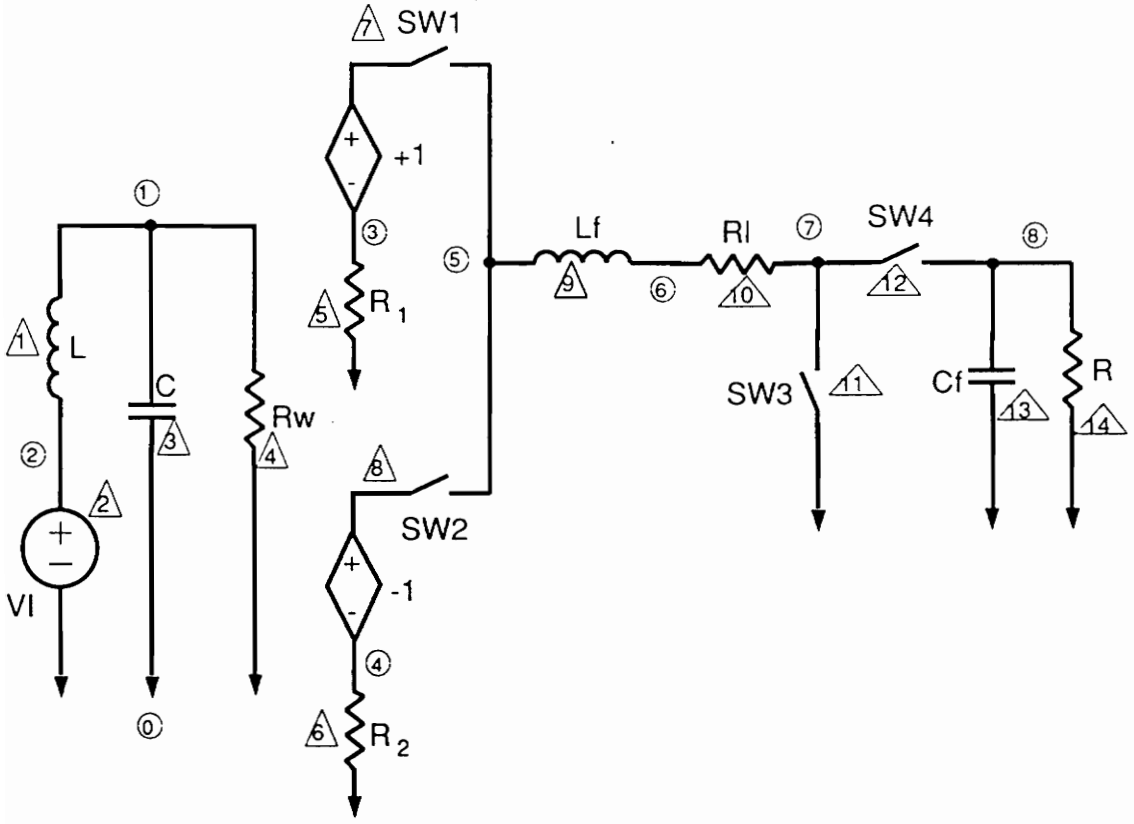



Fig. B.1 Circuit diagram for COSMIR simulation

```
************************************************************
********************* TABLE C1.1 ***************************
************************************************************

TITLE= POWER FACTOR CORRECTION CIRCUIT WITHOUT INPUT FILTER

START = SW1 SW3

*** COMPONENT DESCRIPTION CARDS ***

** Sinusoidal Voltage Source **

L=2.65D-3                       B=1             N=(2,1)
C=2.56D-3                       B=3             N=(0,1)
VI                              B=2             N=(0,2)
RH=20D+6                        B=4             N=(1,0)
** Rectifier **
R2=0.00001                      B=6             N=(4,0)
VCVS=-1                         B=4,6
R1=0.00001                      B=5             N=(3,0)
VCVS=1                          B=4,5
SWD=1                           B=7             N=(3,5)
SWD=2                           B=8             N=(4,5)
** Power Stage **
LF=3.49D-4                      B=9             N=(5,6)
RL=.0001                        B=10            N=(6,7)
SWD=3                           B=11            N=(7,0)
SWD=4                           B=12            N=(7,8)
CF=66.3D-6                      B=13            N=(8,0)
** Load **
R=295                           B=14            N=(8,0)

** OUTPUT CARDS ***

*source voltage
Y1=VB(B4)
*inductor current
Y2=CB(B9)
*output voltage
Y3=VB(B14)

*** SWITHING BOUNDARY CONDITIONS ***

*Turn on condition for switch #4 (Diode)
TON(4) = -T3  + 14.44E-6
*Turn on condition for switch #3 (MOSFET)
TON(3) =  Y2  - 0.01
*Turn on condition for switch #1
TON(1) = -Y1
*Turn on condition for switch #2
TON(2) =  Y1

END
```

```
*****************************************************************
********************** TABLE C2.2 ***************************
*****************************************************************


2                  /(ONLY THE SWITCHING POINTS)
20                 /(NIT-MAX ITERATION USED IN NEWTON METHOD)
1                  /(MC-#OF STEP INPUTS)
1.E-6              /(EPS-TOLERANCE FOR CALCULATING PHI & D)
17.0000E-3          /(TF-FINAL SIMULATION TIME)
0.000
300.0
170.0
0.0                /(INITIAL STATES)
1.E20
1.E20
1.E20
1.E20              /(UPPER LIMIT TO STATES)
-1.E20
-1.E20
-1.E20
-1.E20             /(LOWER LIMIT TO STATES)
5.0D-6
5.0D-6
5.0D-6
5.0D-6            /(FIXED TIME STEPS)
0.0
0.0               /(STEP CHANGE)
1.0
1.0E-8
1.0E-8
1.0E-8
1.0E-8
1.0E-8
1.0E-8
1.0E-8
1.0E-8
1.0E-8
```

for $f = 60$ Hz , $L = C = 2.65 \times 10^{-3}$. To start the sine wave at zero voltage, the initial condition of the capacitor is selected to equal zero, and the initial condition for the inductor current can be selected as follows:

$$i_L(0) = A \omega C = A, \qquad (C.2)$$

where A is the amplitude of the input line voltage. For 120 V rms the input line voltage $i_L(0) = 120\sqrt{2} = 170V$. The initial condition for the output filter capacitor is 300 V, (the output voltage). The full bridge rectifier is modelled by controlled voltage sources with +1 and -1 gains and the switches SW1 and SW2. Switch SW4 is the power stage diode, and SW3 is the power stage MOSFET. SW4 turns on at the end of the on-time, and SW3 turns on when the inductor current ramps down to zero. The first part of the INPUT1.DAT file is the nodal description of the circuit, and the switching boundary condition cards determine the on-time control. In INPUT2.DAT file, the total simulation time and the initial conditions of the states must be defined. The small numbers (0.001) in the switching boundary conditions in the INPUT1.DAT files are to avoid any numerical problems.

## *B.2 COSMIR Files for P.F. Circuit with Input Filter*

For verification of the input filter design, the power factor correction circuit with the two stage input filter and the rectifier was simulated. Fig. 3.14 shows the

circuit diagram for the COSMIR simulation. The circled numbers are the nodes, and the triangled numbers are the branch numbers. The INPUT1.DAT and the INPUT2.DAT are given in Tables C2.1 and C2.2, respectively. The L and C of the input sine wave generator and their initial conditions are selected as before. The initial conditions for all the filter states are selected to equal to zero.

```
*************************************************************
********************** TABLE C2.1 ***************************
*************************************************************

 TITLE= POWER FACTOR CORRECTION CIRCUIT WITH INPUT FILTER

 *** COMPONENT DESCRIPTION CARDS ***

START=SWD5

** Sinewave voltage generator and isolation transformer **
 LG=2.65D-3                    B=1                    N=(2,1)
 CG=2.65D-3                    B=2                    N=(1,0)
 VI                            B=3                    N=(0,2)
 RH=20D+8                      B=4                    N=(1,0)
 R2=0.1                        B=5                    N=(0,3)
 VCVS=-1                       B=4,5

** filter **
L1=14.90D-3                    B=12                   N=(3,7)
RC=8.900                       B=13                   N=(7,9)
C1=1.70D-6                     B=14                   N=(9,0)
L2=4.300D-3                    B=15                   N=(7,8)
C2=0.36D-6                     B=16                   N=(8,0)
XFR=1.                         B=6,7                  N=(8,0,4,5)

** Full-bridge rectifier                                        **
 SW=1                          B=8                    N=(4,6)
 SW=2                          B=9                    N=(0,5)
 SW=3                          B=10                   N=(5,6)
 SW=4                          B=11                   N=(0,4)

** power stage **

L=1.040D-3                     B=17                   N=(12,10)

SWD=5                          B=18                   N=(10,0)
SWD=6                          B=19                   N=(10,11)
CF=5.89D-5                     B=20                   N=(11,0)
RL=900.0                       B=21                   N=(11,0)
RS=0.0001                      B=22                   N=(6,12)

SAME=SW1,SW2
SAME=SW3,SW4

*** OUTPUT CARDS ***

 *Source Voltage
 Y1=VB(B4)
 *Inductor current
 Y2=CB(B17)
```

```
*Inductor L1 current
Y3=CB(B12)
*output voltage
Y4=VB(B21)
*Rectifier Current
Y5=CB(B8)
*Rectifier Current
Y6=CB(B10)
*Rectifier Voltage
Y7=VB(B8)
*Rectifier Voltage
Y8=VB(B10)
*Rectifier Voltage
Y9=VB(B9)
*Rectifier Voltage
Y10=VB(B11)

***SWITCHING BOUNDARY CONDITION CARDS ***

*Turn on/off condition for the same switch SW1 & SW2
TON(1)=  -Y7 -Y9 +0.01
TOFF(1)=  Y5 +0.0001
*Turn on/off condition for the same switch SW3 & SW4
TON(3)=  -Y8 -Y10 +0.01
TOFF(3)=  Y6 + 0.0001
*Turn on condition for the switch SW5 (Power stage MOSFET)
TON(5)= Y2 - 0.01
*Turn on condition for the switch SW6 (Power stage Diode)
TON(6) = -T5 + 14.44D-6

END
```

```
*********************************************************
********************** TABLE C2.2 ***********************
*********************************************************


1          /OUTPUT SWITCHING POINTS ONLY
20         /MAX ITERATIONS USED IN NEWTON'S METHOD
1          /NUMBER OF STEP CHANGES
1.D-6      /TOLERANCE FOR CALCULATING PHI AND D
16.666D-3  /TOTAL SIMULATION TIME
0.000
0.0
0.0
300.0
170.0
0.0
0.0
0.00     /INITIAL STATES
1.D20
1.D20
1.D20
1.D20
1.D20
1.D20
1.D20
1.D20     /UPPER LIMITS TO STATES
1.D20
1.D20
1.D20
1.D20
1.D20
1.D20
1.D20
1.D20     /LOWER LIMITS TO STATES
1.0D-6
1.0D-6
1.0D-6
1.0D-6
1.0D-6
1.0D-6
1.0D-6
1.0D-6    /FIXED TIME STEP FOR EACH TOPOLOGICAL MODE
0.0
0.0
1.0       /STEP CHANGE
1.D-8
1.D-8
1.D-8
1.D-8
1.D-8
1.D-8     /TOLERANCES FOR SWITCHING BOUNDARY CONDITIONS
```

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# Vita

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Before joining VPI&SU he worked for ten years as an instrument engineer and was involved in the installation and commissioning of process control instrumentation for refineries in Iraq and for a nuclear research reactor in Bangladesh.