Cascode GaN HEMT Gate Driving Analysis

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***Abstract*—The aim of this paper is to analyze the conventional cascode gate driving to understand the switching transition and to provide a design guide for the GaN HEMT and its associated packaging. A double-pulse tester has been designed and fabricated with minimum parasitic inductance to avoid unnecessary parasitic ringing. The switching behaviors in both turn-on and -off are analyzed through topological study and explained through SPICE simulation. Two different cascode devices were tested to show the impact of threshold voltage and low-voltage Si MOSFET selection.**

Keywords—Cascode GaN, Gate driving, HEMT

I. Introduction

The depletion-mode (d-mode) gallium nitride (GaN) high electron mobility transistor (HEMT) has been regarded as a relatively high reliable device due to a higher threshold voltage V_{th} compared to the enhancement mode (e-mode) GaN devices. Especially, the V_{th} level can be adjusted through the thickness of the gate insulation layer. However, the normally-on feature of d-mode HEMT is not desirable in most applications. Commercial products have already adopted various cascode approaches to stack a high-voltage GaN HEMT and a low-voltage silicon (Si) MOSFET to make them a normally-off device [1-5]. These commercial devices all integrate the two devices inside the package and are not flexible for the gate drive design. For a better understanding of gate driving characteristic, it is desirable to work on the discrete GaN HEMT and Si MOSFET with individual gates available for measurement. The package or layout, though, has to be highly integrated to minimize parasitic inductances that tend to ring with the junction capacitances. In this paper, a high-voltage GaN metal-insulator-semiconductor (MIS) HEMT device is adopted for gate driving analysis [6].

The gate driving method can be implemented using either the conventional cascode approach [3-5] or direct drive [7-8] method. In the conventional cascode approach, the HEMT gate is tied to the MOSFET source to produce a negative voltage across the gate and source of the HEMT, which is the same as the voltage from source to drain of the MOSFET. On the other hand, the direct drive GaN HEMT gate is also connected to the source but through a diode, which still produces a negative gate voltage but the diode blocking allows the GaN gate to be controlled directly. The conventional cascode approach is preferred for low-cost and seamless integration into existing MOSFET driver circuits.

In this paper, we conduct a detailed analysis of the conventional cascode gate driving approach to gain insights into switching transitions and to provide a design guide for the GaN HEMT and the associated components selection. The switching behaviors during both turn-on and -off phases are examined through topological study and explained the findings using SPICE circuit simulation. A commercial device (TP65H150G4LS) and an in-house developed device (GSNTD63BD1) were tested to show the impact of threshold voltage and low-voltage Si MOSFET selection. A double-pulse tester has been designed and fabricated with minimum parasitic inductance for testing and verification.

II. Cascode GaN HEMT Device and Test Circuit

Fig. 1(a) depicts a d-mode GaN HEMT cascode device with parasitic capacitances and inductances. The d-mode GaN HEMT and Si MOSFET contain gate-source capacitances $C_{gs\text{-}H}$ and $C_{gs\text{-}M}$, gate-drain capacitances $C_{gd\text{-}H}$ and $C_{gd\text{-}M}$, and drain-source capacitances $C_{ds\text{-}H}$ and $C_{ds\text{-}M}$. On the main power loop, L_{d1}, L_{d2}, and L_s are lumped wire-bond parasitic inductances. On the gate drive loop, L_g and L_w are wire-bond inductances for MOSFET and HEMT respectively.

To better understand the switching delay and transient operation, the device is analyzed and simulated without parasitic inductances. Fig. 2 shows the complete switching test circuit without inclusion of parasitic inductances. A diode D_1 and an inductor L are connected between a dc bus voltage and the drain of the cascade device. The inductor serves as a current source, and the diode serves for freewheeling when the device is turned off. The gate of the Si MOSFET is connected to a gate drive circuit with gating voltage V_g through a gate resistance R_g. In actual test circuit, R_g for gating on and off are different. Fig. 3(a) and 3(b) describe detailed turn-on and -off switching transients.

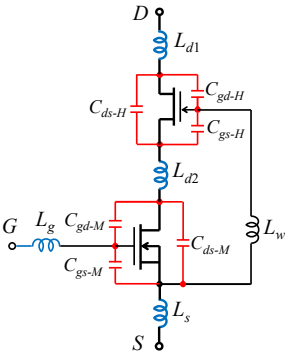


Fig. 1 A d-mode GaN HEMT cascade device with parasitic components.

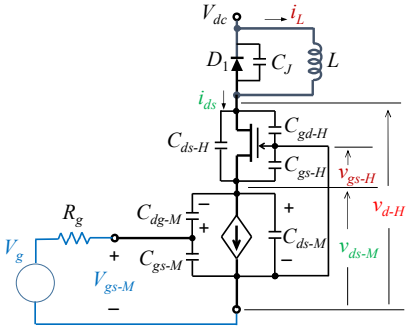


Fig. 2. Simplified device circuit for analysis.

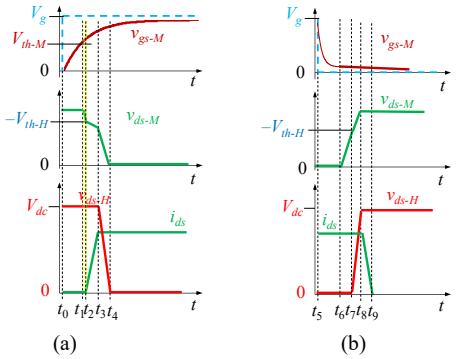


Fig. 3. (a) Turn-on transient waveforms, (b) turn-off transient waveforms.

a. Turn-on Transient Topological Study

Turn-on Period 1 (t_{01}): Turn-on delay due to MOSFET gate charging. From t_0 to t_1, $C_{gs\text{-}M}$ is charged, and $v_{gs\text{-}M}$ rises to $V_{th\text{-}M}$. For turn-on transient, $v_{gs\text{-}M}$ steps up with a voltage V_g that charges the MOSFET gate capacitance $C_{gs\text{-}M}$. From t_0 to t_1, the time constant is $R_gC_{gs\text{-}M}$, and the v_{gs} loop equation can expressed in (1). After rearrangement and integration, the time interval from t_0 to t_1 (t_{01}) can be solved and expressed in (2). Notice that t_1 is the time that MOSFET gate voltage reaches the threshold voltage $V_{th\text{-}M}$, and the MSOFET starts conducting. This t_{01} is a turn-on delay caused by the MOSFET gate capacitance and gate drive resistance.

$$V_g = v_{gs\text{-}M} + R_gC_{gs\text{-}M}\frac{dv_{gs\text{-}M}}{dt} \tag{1}$$

$$t_{01} = -R_gC_{gs\text{-}M}\ln\left(1-\frac{V_{th\text{-}M}}{V_g}\right) \tag{2}$$

Turn-on Period 2 (t_{12}): From t_1 to t_2, MOSFET intends to conduct, but HEMT remains off until HEMT gate-source voltage hits the threshold, $v_{gs\text{-}H} = V_{th\text{-}H}$. During this period, MOSFET Miller capacitance $C_{gd\text{-}M}$ is charging and output capacitance $C_{ds\text{-}M}$ is discharging from $V_{dss\text{-}M}$ to $V_{th\text{-}H}$. A current is established within the MOSFET.

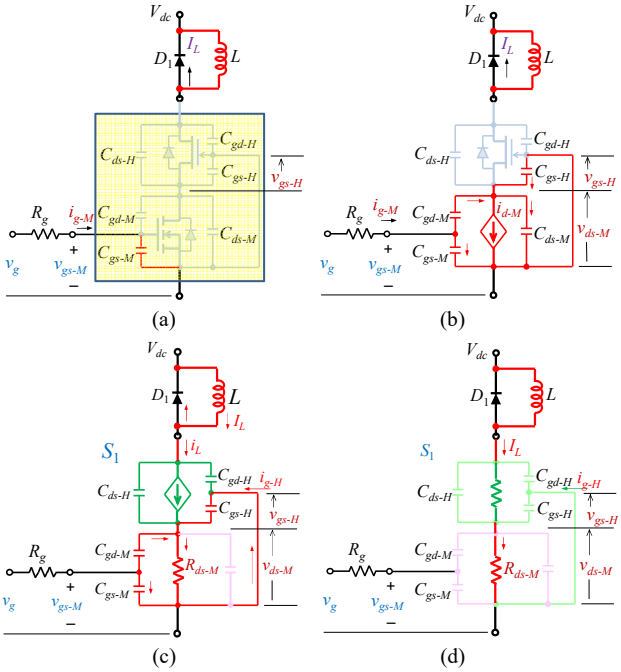


Fig. 4. Topological study during turn-on process: (a) turn-on period 1, (b) turn-on period 2, (c) turn-on period 3, and (d) turn-on period 4.

Turn-on Period 2 (t_{12}): From t_1 to t_2, MOSFET intends to conduct, but HEMT remains off until HEMT gate-source voltage hits the threshold, $v_{gs\text{-}H} = V_{th\text{-}H}$. During this period, MOSFET Miller capacitance $C_{gd\text{-}M}$ is charging and output capacitance $C_{ds\text{-}M}$ is discharging from $V_{dss\text{-}M}$ to $V_{th\text{-}H}$. A current is established within the MOSFET.

$$i_{g\text{-}M} = C_{gs\text{-}M}\frac{dv_{gs\text{-}M}}{dt} + C_{gd\text{-}M}\frac{dv_{gd\text{-}M}}{dt} \tag{3}$$

$$\begin{aligned} i_{d\text{-}M} &= g_m\left(v_{gs\text{-}M} - V_{th\text{-}M}\right) \\ &= C_{gd\text{-}M}\frac{d\left(v_{gd\text{-}M} - v_{ds\text{-}M}\right)}{dt} - \left(C_{ds\text{-}M} + C_{gs\text{-}H}\right)\frac{dv_{ds\text{-}M}}{dt} \end{aligned} \tag{4}$$

Turn-on Period 3 (t_{23}): From t_2 to t_3, this is the main switching transition period for the current to fully built-up. During this period, the load current I_L transitions from diode to the device with a time-varying component i_L. At t_2, the HEMT gate-source voltage $v_{gs\text{-}H}$ passes the threshold voltage $V_{th\text{-}H}$, a gate current $i_{g\text{-}H}$ is injected into the device with the magnitude related to gate-source and gate-drain charges, as shown in (5). Capacitances $C_{ds\text{-}H}$ and $C_{gd\text{-}H}$ are discharged by the partial load current i_L. The voltage difference between V_{dc} and $V_{ds\text{-}H}$ forces the current established in HEMT channel, and i_L is then transferred to drain $i_{d\text{-}H}$ as expressed in (6). Notice that the MOSFET is flowing with two current components. One is the HEMT current $i_{d\text{-}H}$, which is the current transitioning from the load current i_L, and the other one from the HEMT gating, $i_{g\text{-}H}$.

$$i_{g\text{-}H} = C_{gs\text{-}H}\frac{dv_{gs\text{-}H}}{dt} + C_{gd\text{-}H}\frac{dv_{gd\text{-}H}}{dt} \tag{5}$$

$$\begin{aligned} i_{d\text{-}H} &= g_{m\text{-}H}\left(v_{gs\text{-}H} - V_{th\text{-}H}\right) \\ &= C_{gd\text{-}H}\frac{d\left(v_{gd\text{-}H} - v_{ds\text{-}H}\right)}{dt} - C_{ds\text{-}H}\frac{dv_{ds\text{-}M}}{dt} + i_L \end{aligned} \tag{6}$$

$$v_{gs\text{-}H} + R_{ds\text{-}M}\left(i_{d\text{-}H} + i_{g\text{-}H}\right) = 0 \tag{7}$$

$$V_{dc} = v_{ds\text{-}H} + R_{ds\text{-}M}\left(i_{d\text{-}H} + i_{g\text{-}H}\right) = 0 \tag{8}$$

Turn-on Period 4 (t_{34}): From t_3 to t_4, both MOSFET and HEMT fully conduct the current, and $V_{ds\text{-}H}$ falls to zero. The freewheeling diode D_1 output capacitance C_j is charged with the current difference between i_L and i_{ds}, while the HEMT output capacitor $C_{ds\text{-}H}$ keeps discharging until the voltage falls to the conducting state. For a non-ideal diode, this period can be complicated with the diode reverse recovery.

b. Turn-off Transient Topological Study

The turn-off sequence is reversed, but without the freewheeling diode current turn-off issue, it is possible to make $R_g = 0$ to accelerate the transition. The entire turn-off transition can be explained with Fig. 3(b).

From t_5 to t_6, the MOSFET gate voltage is discharged to its threshold level, $v_{th\text{-}M}$, and the MOSFET starts to turn off. From t_6, the drain-source voltage $v_{ds\text{-}M}$ and thus the HEMT gate-source $v_{gs\text{-}H}$ starts rising.

At t_7, the source $v_{gs\text{-}H}$ passes the threshold $v_{th\text{-}H}$, the HEMT starts turn-off process with the load current I_L charges the drain-source capacitance. The charging period is load current dependent. In other words, the voltage slew rate $d_{vds\text{-}H}/dt$ or time period t_{78} is load dependent, and is not controllable by the gate resistance, which only controls the time period t_{56}.

At t_8, the current starts transferring from the device to the freewheeling diode. At t_9, the current is fully turn-off.

c. MOSFET Output Capacitor Charging Issue

During turn-off process, the output capacitors of GaN HEMT and Si MOSFET get charged by the load current. As shown in Fig. 5, because the MOSFET drain-source capacitor $C_{ds\text{-}M}$ is in parallel with the HEMT gate-source capacitor $C_{gs\text{-}H}$, the drain-source capacitance charge is the sum of the two capacitors, or

$$Q_{ds\text{-}M} = (C_{gs\text{-}H} + C_{ds\text{-}M}) \cdot v_{ds\text{-}M} \qquad (9)$$

With two separate charging path, it is quite possible that $v_{ds\text{-}M}$ will be charged to exceed its blocking voltage and thus resulting in avalanche, which will cause additional turn-off loss. The voltage rating of MOSFET thus needs to be higher than the HEMT threshold voltage $v_{g\text{-}H}$ with sufficient safe margins. Adding an external capacitor across $C_{ds\text{-}M}$ can also help prevent avalanche, but it tends to increase the turn-on loss under hard-switching conditions. For soft-switching though, adding an external capacitor across the MOSFET is in fact desirable to ensure zero-voltage switching.

Rather than adding external capacitor across $C_{ds\text{-}M}$, it is also possible to over-design the MOSFET device by increasing the voltage rating and the size to prevent avalanche under hard switching condition and to ensure ZVS under soft switching condition.

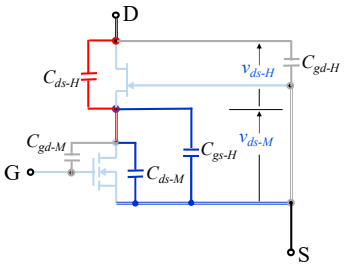
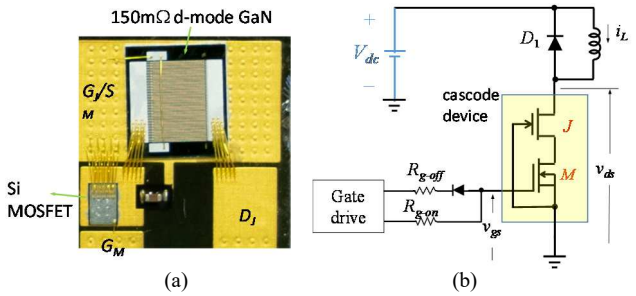


Fig. 5. Cascode device capacitor charging paths.



(a) (b)

Fig. 6. (a) Picture of the in-house developed cascade device, and (b) Power circuit for double-pulse testing.

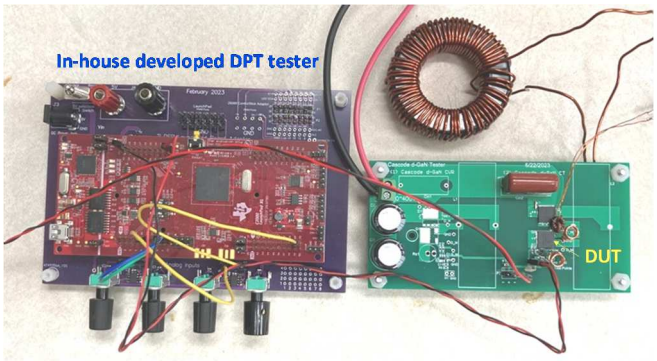


Fig. 7. Photograph of the double pulse testing controller and power circuits

III. Simulation and Experimental Verification

a. Simulation and Experimental Setup

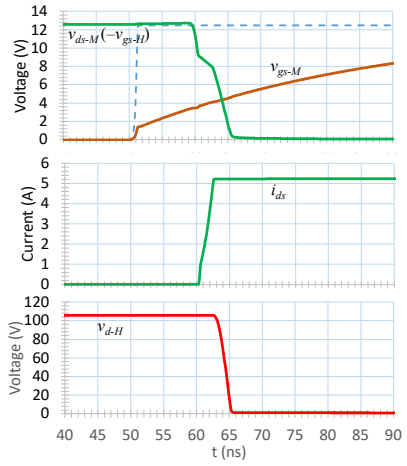
In order to verify the switching behavior and to provide the design guideline, a commercially available device TP65H150G4LS and an in-house developed device GSNTD63BD1 are simulated and tested with a double-pulse tester (DPT). Key parameters of the two cascode devices used in this study are listed in Table 1. The GaN HEMT devices are identically rated, but with different threshold voltage. For the Si MOSFET, GSNTD63BD1 adopts a much larger size MOSFET with a 2.7 times higher input capacitance C_{iss}. The MOSFET C_{oss} of TP65H150G4LS is not available, but we can expect that GSNTD63BD1 would have a much larger C_{oss}.

Table 1: Key parameters of two cascode devices used in this study

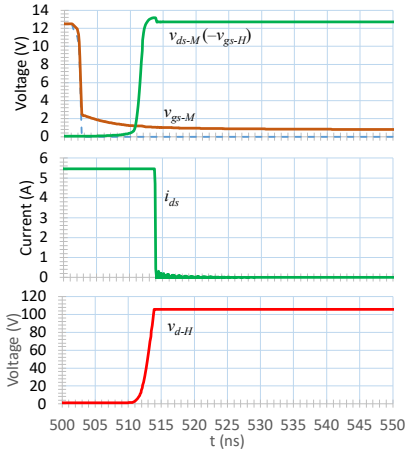
	TP65H150G4LS	GSNTD63BD1
Breakdown voltage V_{BV}	650 V	650 V
On-drop resistance $R_{ds\text{-}on}$	150 mΩ	150 mΩ
MOSFET $C_{iss\text{-}M}$ at 0 V	598 pF	1.62nF
MOSFET $C_{oss\text{-}M}$ at 0 V	n.a.	275 pF
Nominal HEMT $V_{th\text{-}H}$	–22 V	–10 V
Nominal MOSFET V_{th}	2.5 V	4 V

Fig. 6(a) shows the picture of the in-house developed cascade device GSNTD63BD1, which has a comparable conduction and voltage blocking capabilities as that of TP65H150G4LS. The package is also the same, with the back side pinouts compatible each other. Fig. 6(b) depicts the power circuit for double-pulse testing.

Fig. 7 shows the test setup with a photograph showing an in-house developed double pulse testing controller using TI DSP 320F28079D. The pulse widths are controlled with analog inputs through ADC ports. The power circuit consists of local capacitors for testing voltage up to 450 V. The freewheeling diode is a SiC Schottky diode IDL04G65C5XUMA2, rated 650 V, 4 A.



(a)



(b)

Fig. 8. (a) Simulated turn-on waveforms, (b) simulated turn-off waveforms.

To verify the topological study, GSNTD63BD1 is first simulated under low-voltage (100 V) condition. Fig. 8(a) and 8(b) depict the simulation results under (a) turn-on and (b) turn-off switching transient conditions. Both results indicate a clear agreement with those obtained from the analytical waveforms as described in the previous section.

b. Effects of $C_{gs\text{-}M}$ and $V_{th\text{-}H}$

Eqs. (1) and (2) indicate that the turn-on delay is affected by both time constant $R_g \cdot C_{gs\text{-}M}$ and the threshold voltage of MOSFET $V_{th\text{-}M}$. In fact, it is also quite clearly that these two parameters will affect the turn-off delay as well. The impact of HEMT threshold voltage $V_{th\text{-}H}$, however, has never been discussed in the literature. In this study, we discovered that both $C_{gs\text{-}M}$ and $V_{th\text{-}H}$ significantly affect the switching noise.

In both simulation and experimental studies, the gate resistances for both devices are set to be the same with $R_{g\text{-}on}$ = 10 Ω and, $R_{g\text{-}off}$ = 4.7 Ω. Fig. 9 shows the simulation results comparing the two devices in terms of (1) MOSFET gate-source voltage $v_{gs\text{-}M}$, (2) cascade device drain-to-source voltage v_{ds}, and (3) HEMT gate current, $i_{g\text{-}H}$. The $v_{gs\text{-}M}$ waveforms clearly indicate that the in-house device is much cleaner due to the combination of a larger $C_{gs\text{-}M}$ and a lower $V_{th\text{-}H}$. A large $C_{gs\text{-}M}$ increases t_{01}, and thus delaying the HEMT gating, which then allows the device current built-up before a sharp gating current occurs. A lower $V_{th\text{-}H}$ level also reduces the peak gating current $i_{g\text{-}H}$ for the HEMT, and thus avoiding the noises presenting on the gate voltage.

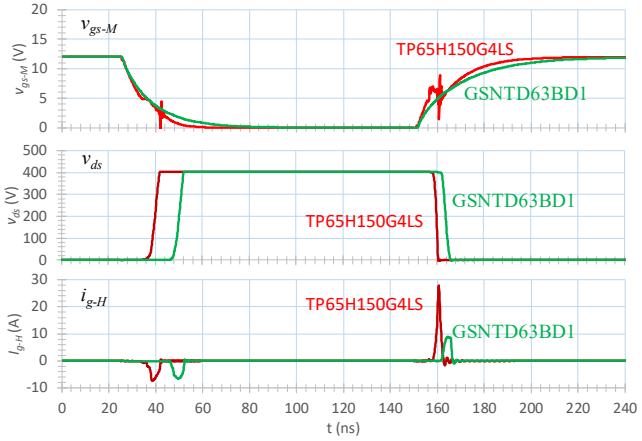


Fig. 9. Simulation comparison between two cascade devices, showing the effects of $C_{iss\text{-}M}$ and $V_{th\text{-}H}$.

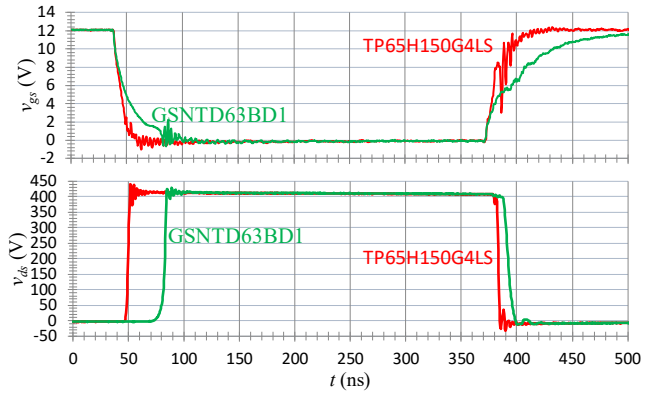
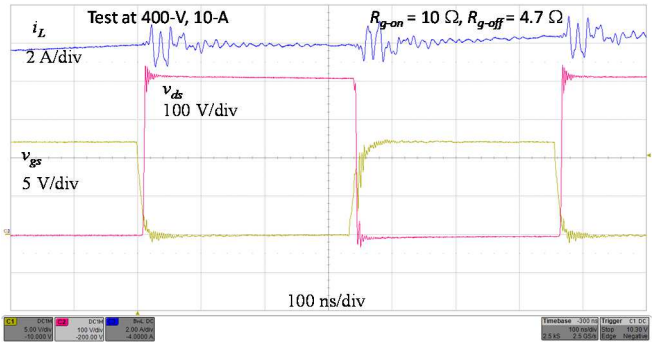


Fig. 10. Experimental verification and comparison of the $C_{gs\text{-}M}$ and $V_{th\text{-}H}$ effects between two cascade devices.

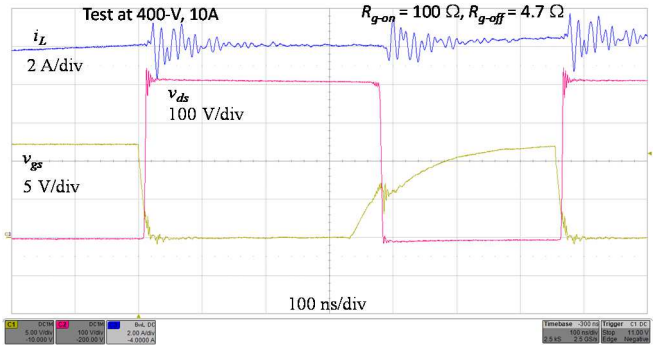
The concepts of switching delay and gate-voltage noise due to gate-source capacitance of MOSFET $C_{gs\text{-}M}$ and threshold voltage of HEMT $V_{th\text{-}H}$ are further verified with experiments. Fig. 10 shows the experimental verification and comparison with the same conditions used in the simulation study. During turn-off, due to a larger $C_{gs\text{-}M}$ and a lower $V_{th\text{-}M}$, the in-house device GSNTD63BD1 shows additional >25 ns delay as compared to that of TP65H150G4LS. During turn-on, similar delay occurs but is only about 10-ns slower. The gate drive waveform is a lot cleaner with GSNTD63BD1. The experimental gate signal is considered pretty clean even with unavoidable parasitic inductances in printed-circuit-board (PCB) traces.

The biggest advantage with clear gating waveform is to avoid false triggers when the opposite-side is a switching device. The false trigger can cause shoot-through or short circuit failure. The only concern with slowing gating for clean switching waveforms is possible impact for the pulse-width-modulation (PWM) duty cycle change when the converter needs to operate at a very high switching frequency. In this example study, the turn-off duty with slower gating is reduced by 15-20 ns, which accounts to up to 2% duty change under 1-MHz operating condition. However, such a duty change can be easily corrected in a closed-loop control system.

Both simulation and experimental studies clearly indicate that the selection of MOSFET and the threshold voltage level in a cascade device is nontrivial and requires some design tradeoffs. A slower but clear approach is indeed more desirable from the circuit level reliability point of view.



(a)



(b)

Fig. 11. Experimental results comparison using TP65H150G4LS under (a) $R_{g\text{-}on}$ = 10 Ω and (b) $R_{g\text{-}on}$ = 100 Ω conditions.

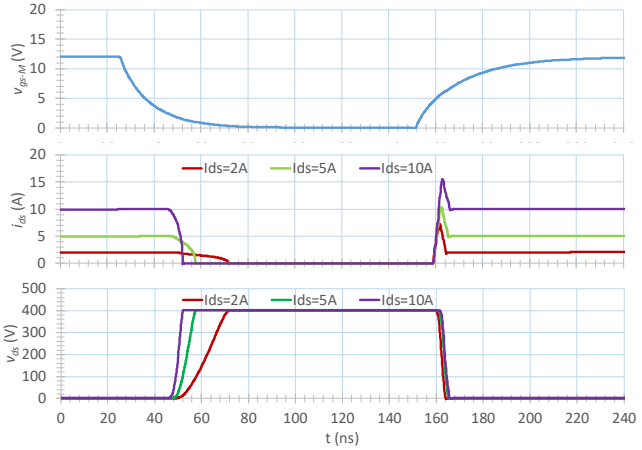
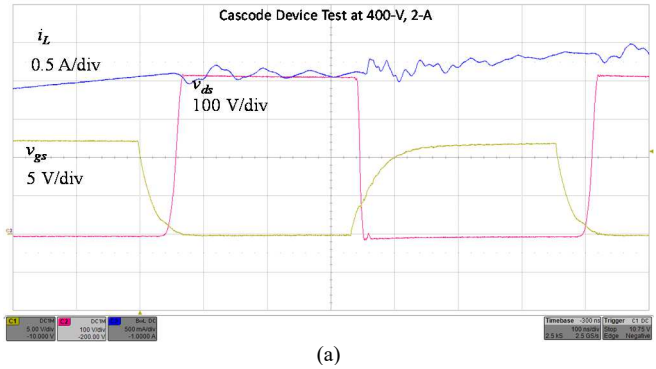


Fig. 12. Simulation comparison of voltage slew rates using GSNTD63BD1 under different load conditions.

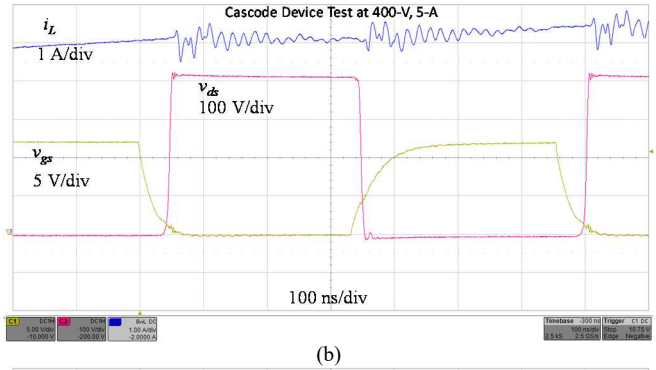
When dealing with the commercially available devices which have unchangeable $C_{gs\text{-}M}$ and $V_{th\text{-}H}$, can one design the gate drive circuit with a large $R_{g\text{-}on}$ to avoid the switching noise? The answer is clearly "no" because $R_{g\text{-}on}$ can only delay the turn on but not slow down the current slew rate. Fig. 11 compares the test results using TP65H150G4LS under (a) $R_{g\text{-}on}$ = 10 Ω and (b) $R_{g\text{-}on}$ = 100 Ω conditions.

c. Turn-off Slew Rate as a Function of Load Current

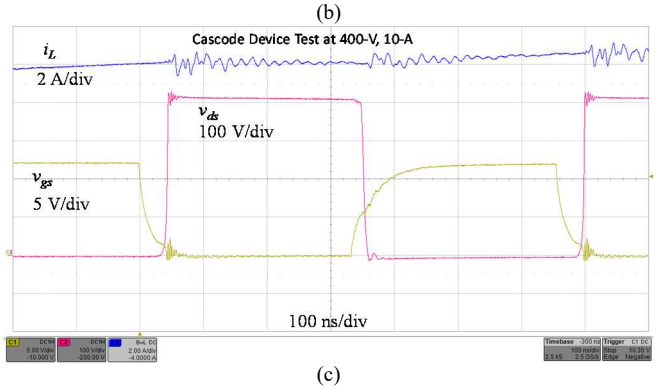
As described in the topological study, the turn-off delay is caused by the MOSFET gate-source capacitance discharge time constant, or $R_{g\text{-}off}C_{iss\text{-}M}$, but the turn-off voltage slew rate dv_{ds}/dt is a function of the load current. Simulation results in Fig. 12 compare the device voltage and current waveforms three load conditions under the same bus voltage and gating setup for the in-house device GSNTD63BD1. Under turn-off condition, the device voltage slew rates are 12.5 V/ns at 2 A, 38.2 V/ns at 5 A, and 79.6 V/ns at 10 A.



(a)



(b)



(c)

Fig. 13. Experimental verification for voltage slew rate under different load conditions: (a) 400 V, 2 A, (b) 400 V, 5 A, and (c) 400 V, 10 A.

Fig. 13 shows experimental verification for the voltage slew rate using the in-house device GSNTD63BD under different load conditions: (a) 400 V, 2 A, (b) 400 V, 5 A, and (c) 400 V, 10 A. The results clearly indicate the difference of slew rates under different load conditions. The inductor current i_L in both commercial device and in-house device testing all present noticeable ripples, which are not part of the device current, as they do not appear in the simulation results. The inductor ripple during device turn-off varies among different load conditions. Its magnitude tends to increase as load current or dv/dt increases.

Similar to the DPT test set up, for a voltage-source converter, the output load is typically inductive. The main reason for the output-side inductor current ripple to occur is due to the parasitic capacitance of the inductor that interacts with high dv/dt and results in such a noticeable current ripple. As the GaN device chip size continues to shrink with better designs, the device capacitances will proportionally reduce, which in principle will increase dv/dt, and the output-side inductor current ripple due to parasitic capacitance will be more prevalent.

IV. Conclusion

Despite the added Si MOSFET tend to impact the switching speed and potentially increases the switching loss, the structure of GaN HEMT and Si MOSFET cascode devices is relatively simple and easy to substitute the devices in the existing designs that have been dominated by the conventional silicon devices. However, the d-mode GaN HEMT devices are not commercially available, and thus the converter circuit designers always face significant challenges due to the noisy switching behavior of the off-the-shelf cascode devices. This paper's study clearly indicates opportunities for optimizing cascode device design, particularly concerning the GaN HEMT threshold voltage level and Si MOSFET selection.

Using a GaN HEMT fabricated in-house, we were able to identify the key design issues of cascode devices. This paper begins with the topological circuit analysis and verifies the switching behaviors through SPICE circuit simulation and hardware experiments. Key findings of the study are summarized as follows.

- The gate-source capacitance of the Si MOSFET should be sufficiently large to delay the current rise, which often leads to noisy gating signals.
- A relatively large or over-designed Si MOSFET can prevent avalanche during hard switching and ensure zero voltage switching (ZVS) under soft switching conditions.
- Lowering the GaN HEMT threshold voltage reduces the peak gating current.
- The gate drive resistance can only delay switching but cannot reduce the slew rate or associated noise.
- The turn-off voltage slew rate depends on the load current and the device output capacitance and is not influenced by the gate resistance.

Our in-house cascode device demonstrated significant reduction in switching noise by using a relatively large MOSFET gate-source capacitance and a relatively small GaN threshold voltage level. However, the overall study in this paper concludes that further optimization is necessary for enhancing the device's switching performance through GaN HEMT design and Si MOSFET selection.

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