POWERING THE FUTURE

2021 ANNUAL REPORT

CPES Center for Power Electronics Systems | VIRGINIA TECH

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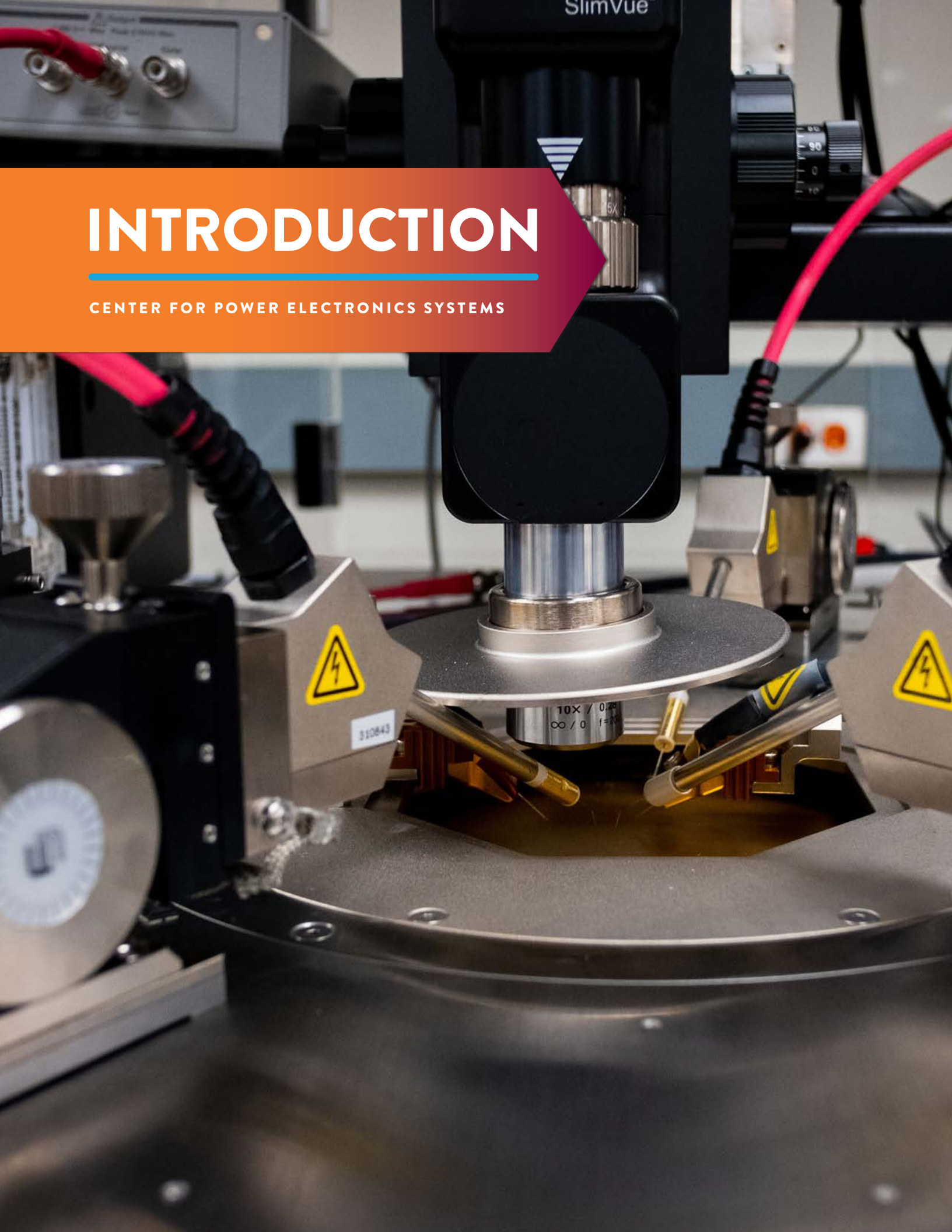
Table of Contents



INTRODUCTION

CENTER FOR POWER ELECTRONICS SYSTEMS

Powerfully Resilient

2020 was one of the most challenging years in history. Even now, well into 2021, the world continues to grapple with health, economic, and social issues that intensified last year. In the face of difficulty, however, the brightest innovation can and must shine through. It is with this sentiment that the Center for Power Electronics Systems (CPES) focused its efforts on building success over the course of a year that looked to hinder it.

The genesis of CPES was more than 40 years ago, when Professor Fred. C. Lee began the power electronics program at Virginia Tech. The mission is to provide leadership through global collaborative research and education in creating advanced electric power processing systems of the highest value to society. In today's environment specifically, CPES is dedicated to improving electrical power processing and distribution that affect systems of all sizes – from regional and national electrical distribution systems to battery operated electronics and vehicles too.

This vision, combined with tireless efforts from faculty, students, and staff, has resulted in an academic research center that is among the largest and most renowned in the world. Keeping the center's mission in mind provided clear guidance and a fundamental goal to turn to in the uncertainty of the past year. In the face of unprecedented challenges, CPES not only continued training the best students in the field and researching cutting-edge power electronics solutions, but also adapted to encourage future success.

This book is a comprehensive record of the center's accomplishments during the year 2020. In addition to copious research project summaries and results (see Sponsored Research and Research Nuggets), one can learn more about the world-class Facilities and People necessary for these achievements. Research outputs, like Intellectual Property and Publications, are detailed as well.

These accomplishments are framed by the articles in the Features section. We describe how, early in the pandemic, CPES adroitly navigated constantly evolving health guidelines to continue the center's trademark experimental work. CPES faculty are shown upholding the tradition of leading the world in developing new technologies for the benefit of humankind. And our newer faculty are already being recognized for their exceptional impact. The many critical contributions of our students are also captured in these pages. Finally, we celebrate the success of our completely reimagined annual conference, the preeminent opportunity to engage with and showcase technical achievements for our industry members and sponsors.

We are keenly aware that these triumphs and more would not be possible without your interest and support. In fact, CPES would not exist without the support of our many collaborators and sponsors and we offer heartfelt thanks to all.

The many accomplishments in this book display the devoted efforts of an institution which, in a time of great struggle, never lost focus of its main mission. Through sustained innovation, in the face of dire difficulty, CPES is still powering the future.

FEATURES

A YEAR OF BREAKTHROUGHS

Powering Through the Pandemic

The COVID-19 pandemic greatly affected the way humanity interacts on a personal and professional level. Through the dedication of faculty, students, and staff, and with the strong support of our industry members and sponsors, CPES was able to quickly adapt to a rapidly changing environment and continue to execute on our mission of training future power electronics engineers and delivering cutting-edge technical solutions.

In organizations where personal interactions are so crucial to success, transitioning to a workplace in a quarantined environment is inherently a difficult task. A large part of what makes CPES a leading research institution is not only faculty and student access to world-class facilities but also constant interaction with top minds in power electronics from around the world. Research success is built off a strong collaborative effort of the whole. However, in-person collaboration was suddenly brought to a halt, disrupting this integral part of the CPES experience.

In April 2020, Virginia Tech followed the actions of many other research institutions by moving most university functions off campus. For classes, spring semester was concluded online. Nonessential personnel were instructed to work from home in the wake of the virus outbreak. CPES followed university safety precautions by immediately restricting access to all facilities and enabling faculty, students, and staff to work from home. As a result, the lab activity in Blacksburg is still far from its usual bustle. More than 70 workbenches, ready to accommodate the research of students and visiting scholars, are now sparsely populated.

Following this severe change, CPES was tasked with quickly finding an effective way to continue operation. CPES had to find the optimal solution to continue progress and therefore uphold the organization's values of education and research, with an added focus on the safety of all involved.

Faculty and staff immediately began working through possible solutions to maintain productivity, while adhering to new university guidelines. Student Council representatives greatly aided in this process by providing an influx of student ideas, opinions, and potential ways forward.

As a result of this full-team effort, CPES was able to continue all research activities, even experimental work on hardware. University protocol was followed with writing, advising, meetings, reviews, and simulations fully transitioned to an accessible online format.

Many students continued their progress without visiting the lab thanks to Lab@Home, which made available CPES equipment for low-power research. The loaning of CPES lab equipment has provided an alternate way for students to complete testing work that they would otherwise need lab access to conduct. Tools and equipment that could be easily transported were identified for student use. If a student needed certain items, they simply reached out for approval to their major professors and CPES Director Dushan Boroyevich. After approval, CPES Lab Manager David Gilham worked with the student to provide the necessary equipment and track the loaned items.

> *"The COVID pandemic forced us to ask more of our faculty, students, and staff than ever before. And everyone responded exceptionally well. I am proud that we've upheld the tradition of excellence to which CPES has always aspired."*
>
> *Dushan Boroyevich, CPES Director*

With the proper equipment, much of the building and testing of student projects is now done at home with residential low power supply. Third-year CPES student

Yu Rong, who works on communications between large-scale power electronics building blocks (PEBB), commented, "There have been no problems for me with taking home lab equipment. Being able to have all of the equipment at home is exciting." Rong continued saying that, "While I am missing some things that are available in the lab, my productivity has remained very similar to what I was able to do previously." Also at home, students are writing their papers, patents, theses, and dissertations, and progressing towards their degrees uninterrupted.

However, there is a limitation to what work can be completed in a home environment. For instance, many current CPES projects require a higher power supply than what is residentially available and special testing equipment, which requires lab access.

To address this necessity for some students, CPES Webmaster Matthew Scanland used input from Student Council representatives to design and implement an online solution to manage highly restricted lab access. Students who must use the lab log-on to the program and reserve time slots in advance. David Gilham manages how many students are in the lab at any given time in order to keep the lab from becoming over-crowded, therefore minimizing student exposure to others. Once in the lab, students wear masks and adhere to social distancing guidelines. As an added health measure, full disinfection is provided between shifts, and all surfaces of the lab, including door handles, are sanitized multiple times per day by staff. The Student Council organizes and monitors student sanitation efforts in the evenings and on weekends.

Zhengrong Huang, a recent CPES graduate, is one of the students who was regularly doing work in the lab under the new restrictions. His work on 3 phase ac-dc power conversion for EV charging or solar installations required him to go into the lab to test hardware efficiency. Huang described some of his lab experience: "Progress was admittedly a bit slower due to limited hours but I was able to continue my project. I had no concerns about safety. The steps taken were effective and made the lab a safe place for all students."

While progress has continued, it is clear that there is one main aspect of work at CPES that students miss dearly. Chien-An Chen, another recent graduate, shared that he missed most the, "social interaction, talking to my colleagues, and the instant collaboration that is made possible by being in the normal lab environment."

Despite these challenges, students have taken the changes in stride and are once again showing their dedication and hard work by continuing their projects and processes towards degrees.

In a year of unprecedented difficulty, CPES adroitly problem solved in order to continue training the next generation of power electronics engineers and providing the high-level research that members and sponsors expect.

Boroyevich commended the efforts of the institution as a whole, saying that, "The COVID pandemic forced us to ask more of our faculty, students, and staff than ever before. And everyone responded exceptionally well. I am proud that we've upheld the tradition of excellence to which CPES has always aspired."

Takahide Tanaka Home Setup

CPES Technical Director Igor Cvetković with Urban Alliance interns Elhadji Gueye and Kionn Coates.

Outreach: Engaging Future Talent

URBAN ALLIANCE
Employing Youth. Inspiring Excellence.

For the second consecutive year, CPES partnered with the Urban Alliance in their efforts to empower under-resourced, under-served young people of color by providing job skills training and mentorship in a professional environment. Urban Alliance has been very successful in building a diverse next-generation workforce through paid internships, creating opportunities to collaborate with schools, nonprofits, government, and other partners. All Urban Alliance interns participate in professional development workshops, six weeks of pre-employment job skills training followed by weekly post-high school planning, and job and life skills workshops. CPES is proud to be one of over 200 employers supporting the development of diverse talent pipelines and preventing disconnection from school or the workforce.

CPES's first Urban Alliance intern, Phillip Wince, started in 2019 with CPES in Arlington, and supported faculty, staff, and students in daily operations and lab organization–from electronic components to 3D printing and installation of computers and lab equipment. While interning in CPES, Phillip conducted research on state-of-the-art photovoltaic (PV) technologies and performed a feasibility study on using PV panels in the Sahara Desert to satisfy worldwide consumption of electric energy. Despite the global pandemic hitting hard in early 2020, Phillip continued working remotely with CPES until the end of July. Phillip is now a freshman at Florida Institute of Technology, studying astrobiology.

CPES is proud to continue working with Urban Alliance again this year, and just a few weeks ago welcomed two new interns, Elhadji Gueye and Kionn Coates. Elhadji and Kionn will support CPES faculty, students, and staff at the Arlington location through their work on new equipment installation, commissioning, testing, and maintenance, and be able to help students with their use when needed. They will additionally work on developing an inventory program that will help locate the desired type of electronic component by entering keywords in the program, and help maintain that inventory log by adding new components, equipment, and tools as they are purchased. Elhadji and Kionn will also continue research started by their colleague, Phillip, learning about power electronics, and coming up with creative ideas on utilizing this important field to help provide electrical energy to billions of people who do not have access to it.

CPES Conference Reimagined

The 2020 CPES & PEC Conferences were highly innovative and shattered previous participation records. The preeminent event for engaging our members and sponsors, CPES faced the significant challenge of completely reimagining the in-person conference. The results exceeded expectations and served as a template for future conferences.

Success was due in equal parts to the guidance from the Industry Advisory Board (IAB) and the effective implementation by CPES students, led by the Student Organizing Committee.

The 2020 conference showcased strong collaborative efforts between world leading groups. With CPES, Virginia Tech's Power and Energy Center and Tsinghua University are working to bridge the ever-decreasing gap between power systems and power electronics and leverage their combined potential to bring about the benefits of the future power grid. The conference featured presentations and keynotes from all three groups.

The format of the conference was unlike any held before. Completely online August 31 through September 4, and open to all CPES Members, the five days featured more than 70 hours of keynotes, technical presentations, and panels. Much of the conference was repeated–once during the daytime in Blacksburg and once throughout the night–in order to provide an added degree of convenience for our members around the world.

This conference saw 3,600+ attendees across all sessions. More than 65% of all CPES Member companies, including over 80% of both Principal Plus and Principal companies, had employees in attendance.

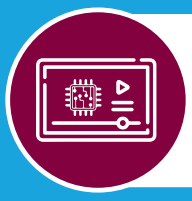
Figures at-a-Glance

470 Participants

127 Companies and Organizations

55 CPES Member Companies Represented

99 Papers and Research Updates



50 Technical Videos

Non-member organizations also responded en masse. More than 50 companies joined representatives from 20 academic and government groups. This dramatic increase in non-members affords a rich opportunity to establish contacts for recruitment and strengthen collaboration.

The IAB provided invaluable input on the format and the scheduling of the event. Their aid in reflecting and incorporating the collective will of members was key to such high industry involvement.

However, good ideas are worth little if not implemented effectively. The Student Organizing Committee gave an impressive effort to organize the conference in a completely new way. While there are admittedly limits to an online conference, students used the positives of this format to maximize the technical information conveyed and provide opportunities for interaction between industry and students. For the first time, students both starred in and directed their own "movies;" i.e., technical presentations. For almost five straight days, students were working around the clock. They were available at all hours for live Q&A sessions following their presentation recordings and also managed the delivery of the content.

The exceptional online participation means we will continue to incorporate the best of both online and in-person formats for future conferences.

The 2020 conference control room.

Future Power Electronics Leaders

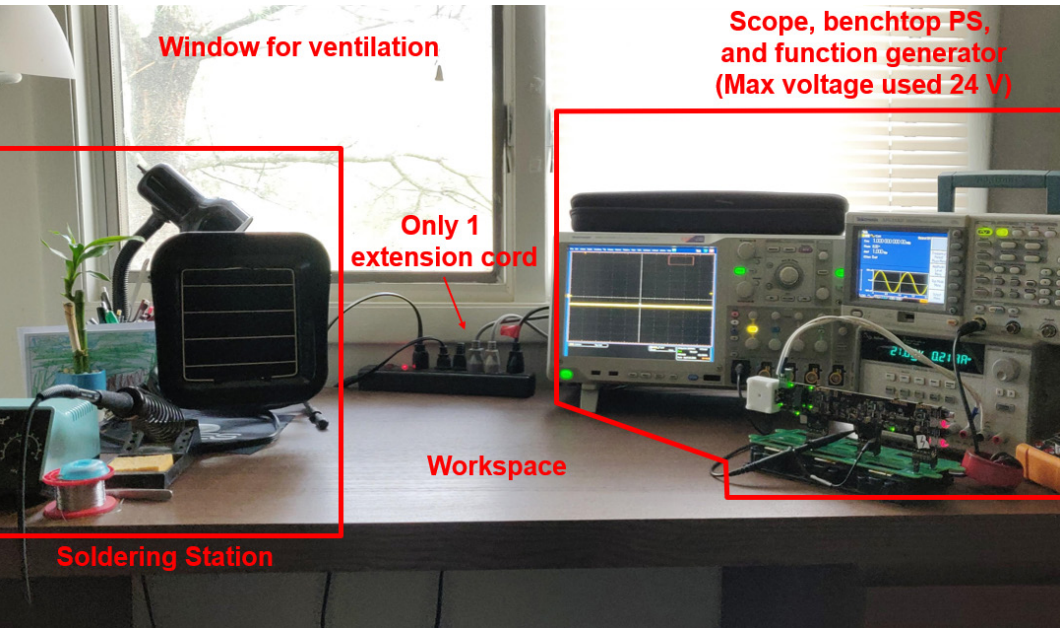
Students are integral to the functioning of CPES. Not only do they conduct much of the research while working towards their degrees, but they also serve in many other critical capacities. "We rely so heavily on students and all that they do. There could not be a CPES without them," says CPES Director Dushan Boroyevich.

Students are highly organized through the Student and Visiting Scholar Council and the Conference Organizing Committee.

In typical years, the Student and Visiting Scholar Council focuses on hosting exciting social activities to build camaraderie and provide opportunity for students to have new and interesting experiences outside the lab. Of course, 2020 was not typical, and social gatherings were not possible. However, the council was quite busy with another priority–representing students' interests in research matters.

Over the past year, the council played a key role as CPES transitioned to COVID-safe practices, enabling lab activities to continue with minimal disruption. From the design and implementation of Lab@Home to the online solution governing lab access to after-hours sanitation, the Student Council has organized and led their fellow students, ensuring member and sponsor research goals were met and progress towards graduation continued.

The Student and Visiting Scholar Council also organizes two seminar series, work that continued unabated in 2020. The CPES Weekly Student Seminar provides a different student each week the opportunity to present their current research through a 45-minute presentation to their fellow



students, as well as CPES faculty, staff, and visiting scholars. Due to the large gathering size of this event, the Weekly Seminar evolved to an online meeting platform to ensure this opportunity for valuable feedback continued. The Weekly Seminar was also expanded to include a section for general discussion before the presentation, to make sure the CPES family stays connected and is always up to date.

The monthly CPES Industry Webinars provide members the opportunity to learn about cutting-edge power electronics advancements and engage directly with future employees and colleagues. Students give 30-minute presentations on topics selected to represent the breadth of research at CPES, followed by Q&A with members. In 2020, more than 800 people participated in these webinars!

> *"We rely so heavily on students and all that they do. There could not be a CPES without them."*
>
> *Dushan Boroyevich, CPES Director*

Joshua Stewart, student council president, offered this statement of appreciation, "The council would like to thank all of the volunteers, staff, faculty, and alumni for their time and effort supporting the CPES family in the past year."

Another critical student group was the Conference Organizing Committee. Always requiring a herculean effort to organize and run, the pandemic added a significant degree of difficulty to hosting the center's premier event for members. Reimaging the usually in-person conference as a completely online event necessitated starting from scratch in planning and execution.

The Conference Organizing Committee worked closely with faculty and students to create high-quality recorded technical presentations, featuring the hardware built by students and resulting waveforms. "All the students did a great job adapting to the new requirements, especially on their recorded presentations," says Slavko Mocevic, general CPES & PEC conference chair.

Additionally, the conference sessions played around the clock, twice a day for almost five days. Students took shifts, managing the online sessions in the background. The result was a pioneering and incredibly successful conference that provides the foundation for future conference formats.

The Student Council and Conference Organizing Committee, and all CPES students, found new ways to succeed in 2020 in the face of tremendous challenge. The future of power electronics is truly bright!

Creativity, Collectivity and Continuity

The Center for Power Electronics Systems at Virginia Tech is today among the largest and possibly the most renowned academic research centers in the world. Almost 100 professors, graduate students, visiting scholars, and staff are working "24/7" in Blacksburg and Arlington, Virginia, to fulfill the CPES mission of providing leadership through global collaborative research and education in creating advanced electric power processing systems of the highest value to society. Specifically, CPES is dedicated to improving electrical energy processing and distribution that affect systems of all sizes—from battery-operated portable electronics to vehicles, to regional, national, and global electrical energy transmission systems.

This has been achieved through a long evolution that started over 40 years ago with the ambition of a young professor at Virginia Tech, Fred Lee, to develop a world-class graduate education program in the then emerging field of power electronics, focused on advanced engineering research. Since Fred's announcement to retire four years ago, we have been exploring how to assure continuing prosperity of this unique global resource of talent and ideas.

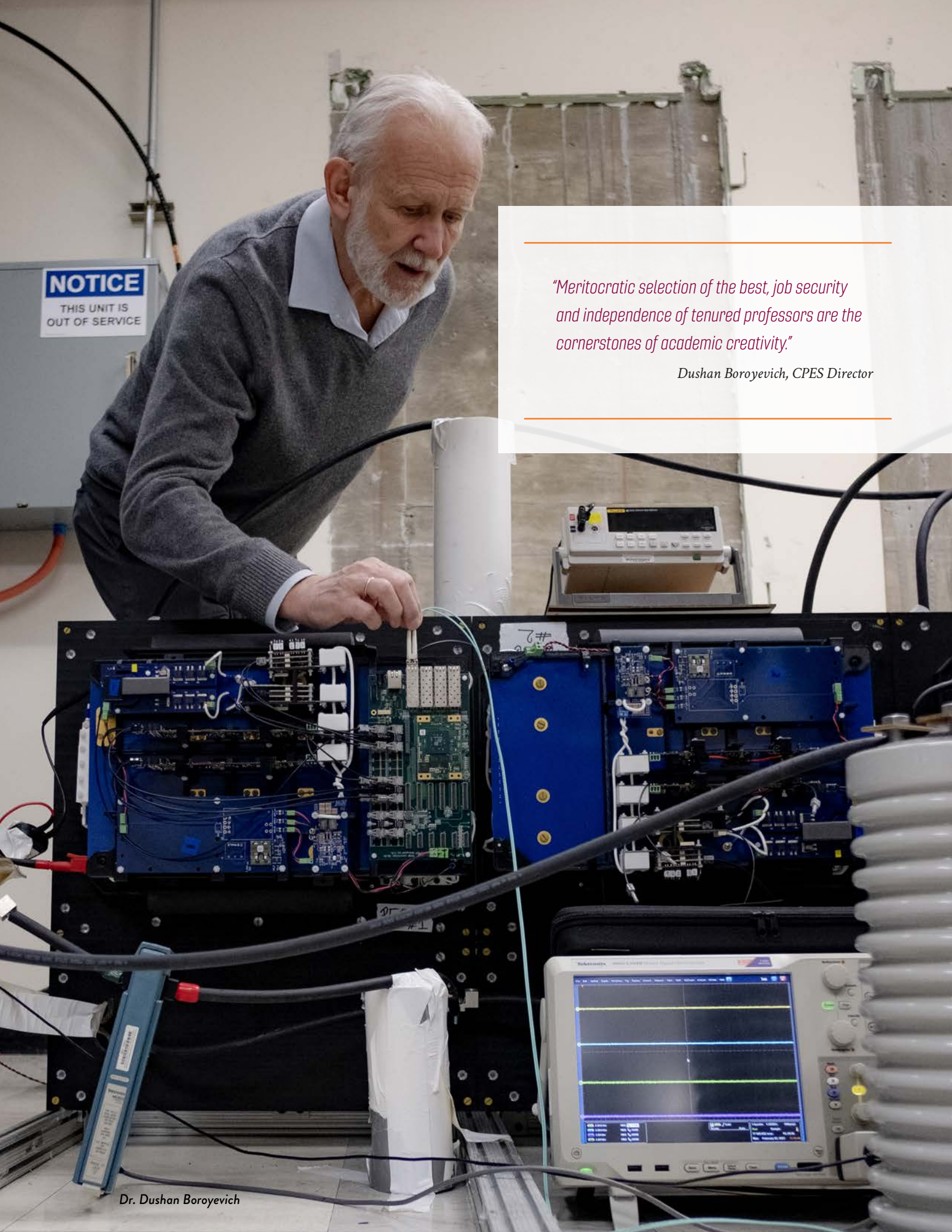
From the beginning, Dr. Lee intuitively focused on building a collaborative research group infused with the following fundamental values:

- Pursuit of global intellectual excellence and creativity
- Uncompromising scholarly integrity
- Constant engineering prototyping for full-scale experimental validation
- Clear industrial relevance (Engineering innovation must be possible to manufacture and scale-up for use in products needed/desired by people.)
- Agility and flexibility in exploring changing technology horizons (Don't have a solution, keep looking for new challenges.)
- Continuous, open and competitive sharing of ideas (Always share all your ideas; you are not allowed to steal other peoples' ideas, but you are encouraged to have a better idea.)

Meritocratic selection of the best, job security, and independence of tenured professors are the cornerstones of academic creativity. But too often these can lead to proliferation of minor contributions obtained with minimized resources, especially in the experimental disciplines that require major research infrastructure. To avoid the latter, many power electronics researchers at Virginia Tech collaborated under Dr. Lee's leadership to find the right balance between creative individuality and collective pooling of shared resources. Over the last decade, the CPES organizational structure coalesced around several key features.

CPES is a voluntary partnership between teaching and research faculty at Virginia Tech, who are primarily focused on power electronics research and education, and who have a long-term commitment of conducting all of their research activities within the partnership. The main objective of the enterprise is to excel engineering research and graduate education in collaboration with industry by:

- Growing and maintaining world-class laboratory facilities and information and communications technology (ICT) infrastructure
- Providing comprehensive and highly effective administrative support



"Meritocratic selection of the best, job security and independence of tenured professors are the cornerstones of academic creativity."

Dushan Boroyevich, CPES Director

Dr. Dushan Boroyevich

- Institutionalizing permanent engagement with industry through a consortium
- Facilitating interactions with other organizational units in Virginia Tech, and with external individuals, companies, governmental and professional organizations
- Maintaining a pleasant, open, inclusive, collaborative, industrious, and intellectually stimulating work environment

These operations are overseen by the Executive Board, consisting of all tenured CPES faculty, who select a Director for efficient internal management and external representation. Within the university, the CPES Director is administratively at the level of department head and reports to the Dean of the College of Engineering.

It would be impossible to assure continuing prosperity of CPES without this collective trust and commitment of support by industry partners, government funding agencies, CPES researchers, and Virginia Tech.

To stimulate creative freedom and increase personal responsibility, all CPES faculty–individually or as a part of ad-hoc teams of co-principal investigators (co-PIs) within or outside CPES–are expected to continuously seek external funding to support their research activities and their graduate students. Co-PIs (not CPES) are responsible for the successful technical and financial performance and completion of the research contracts. CPES faculty are also individually responsible for recruiting, advising, and supervising their graduate students, as well as other researchers (visiting scholars, postdocs, fixed-term research associates, etc.). Furthermore, teaching faculty do not report to the CPES Director, but their performance evaluation, reward, promotion, and tenure are conducted through the regular academic review processes of Virginia Tech, independent of CPES.

Fundamental support for CPES operations comes from the university: academic year salaries of teaching faculty, buildings and space for shared laboratories and offices, and a significant part of administrative and compliance costs. However, direct financial support of research and graduate education (e.g., salary, wage, or stipend funding for all researchers, tuition, administrative and engineering staff support, equipment, laboratory, and ICT infrastructure operations, materials and supplies, travel, outside services, research reporting and dissemination, publicity and outreach) must be secured by CPES faculty from competitive extramural research funding opportunities. Sponsored research funding is primarily used to fulfill grant or contract obligations and to reimburse CPES and the university for the use of shared resources. All investments in hardware and software are incorporated into the "CPES commons," after project completion. Similarly, equipment and software grants and donations are equally available to all CPES researchers, regardless of the sources of funding and how it was secured.

The equitable sharing of common resources enables huge efficiency gains in utilization of the physical and human infrastructure, which in itself is a major motivation and justification for choosing to be a part of CPES. However, the most distinguishing feature of the CPES enterprise is its industry partnership program, which engages much of the global power electronics industry in supporting and guiding pre-competitive research and education in exchange for non-exclusive access to the generated intellectual property and talent. Through the nominal annual gifts from over 80 companies – proportional to their levels of engagement – the industry consortium provides over one third of the direct financial support for research and graduate education in CPES.

CPES baseline support from the university and the industry consortium provides long-term security and thus enables the open and sharing team culture between all participants. The faculty think: "This patent will not make me rich, but it will be used by many companies to make useful products, and in return I will have even more opportunities to come up with better patents!" Graduate students and visiting scholars are inspired by the open sharing of ideas between themselves, faculty, staff, industry partners, and the professional community. They enjoy the open laboratory spaces filled with top-notch equipment, and are motivated to work ever

harder by e-mails from CPES faculty and staff that come at 5 AM, noon, and 11 PM. These young researchers feel they are an integral part of the CPES mission due to their major organizational responsibilities, beyond the core focus on academic progress; e.g., lab operations, annual conference, monthly webinars, weekly seminars, and the community-building activities organized by the Student and Visiting Scholar Council. CPES outstanding staff, although relatively small, are aware of and appreciated by everyone for their special role as the "mortar" that fills all the gaps between the "bricks" in order to prevent the CPES "building" from crumbling! Finally, our friends from industry partners and sponsors, program managers in government agencies, and professional colleagues everywhere, came to value the predictable output of the world-class research results and talent coming from CPES over the last 40 years. This creative productivity and its longevity, coupled with uncompromising scholarly integrity, has resulted in the global recognition and trust of the "CPES brand."

It would be impossible to assure the continuing prosperity of CPES without this collective trust and commitment of support by industry partners, government funding agencies, CPES researchers, and Virginia Tech. CPES faculty, led by the Executive Board, will continue exploring how to keep the organizational structure of CPES flexible and adaptive to the changing circumstances and developing interests of all our members, while preserving our fundamental values and key features, and continuously enhancing the CPES brand. This will guide the "change of generations," which started with Fred's retirement and will be completed in a couple of years with the expected promotions of new faculty and the upcoming retirements of Dushan Boroyevich and Khai Ngo. We, the CPES faculty, pledge to continue having fun in power electronics research and education, and to keep enjoying the friendships with our numerous colleagues around the world.

U.S. Department of Energy and CPES: A Powerful Collaboration

CPES, as a former National Science Foundation (NSF) Engineering Research Center (ERC), has a successful and long-standing collaboration record with the U.S. government, attained by working jointly with several of its agencies to advance power electronics technology. Starting from 1977 with National Aeronautics and Space Administration (NASA)-sponsored programs led by Dr. Fred Lee, who addressed several fundamental aspects of the integration of power converters in dc distribution systems for space applications, to the successful collaboration with the Office of Naval Research (ONR) led by Dr. Dushan Boroyevich, where CPES played a key role in the development of the Power Electronics Building Block (PEBB) concept, and posteriorly in the integrated power module (IPM) under NSF, to numerous other programs sponsored by the Air Force Research Laboratory (AFRL), the Army Research Laboratory (ARL), and the Defense Advanced Research Projects Agency (DARPA), CPES has been at the forefront of power electronics.

Dr. Rolando Burgos

The collaboration with the U.S. Department of Energy (DOE), however, did not materialize for CPES until 2010, where under the back-then nascent Advanced Research Projects Agency–Energy (ARPA-E), Drs. Lee, Boroyevich and Ngo led multiple projects under the Agile Delivery of Electrical Power Technology (ADEPT) program, cementing the foundations of what has become a strong partnership. This represented a significant turn of events, not just for CPES but for DOE, which with the creation of ARPA-E was responding to the 2007 National Academies report "Rising Above the Gathering Storm: Energizing and Employing America for a Brighter Economic Future" that had been tasked by Congress to *"identify the most urgent challenges the U.S. faces in maintaining leadership in key areas of science and technology."*[1] In 2010 DOE also created the

[1] *https://www.nap.edu/catalog/11463/rising-above-the-gathering-storm-energizing-and-employing-america-for*

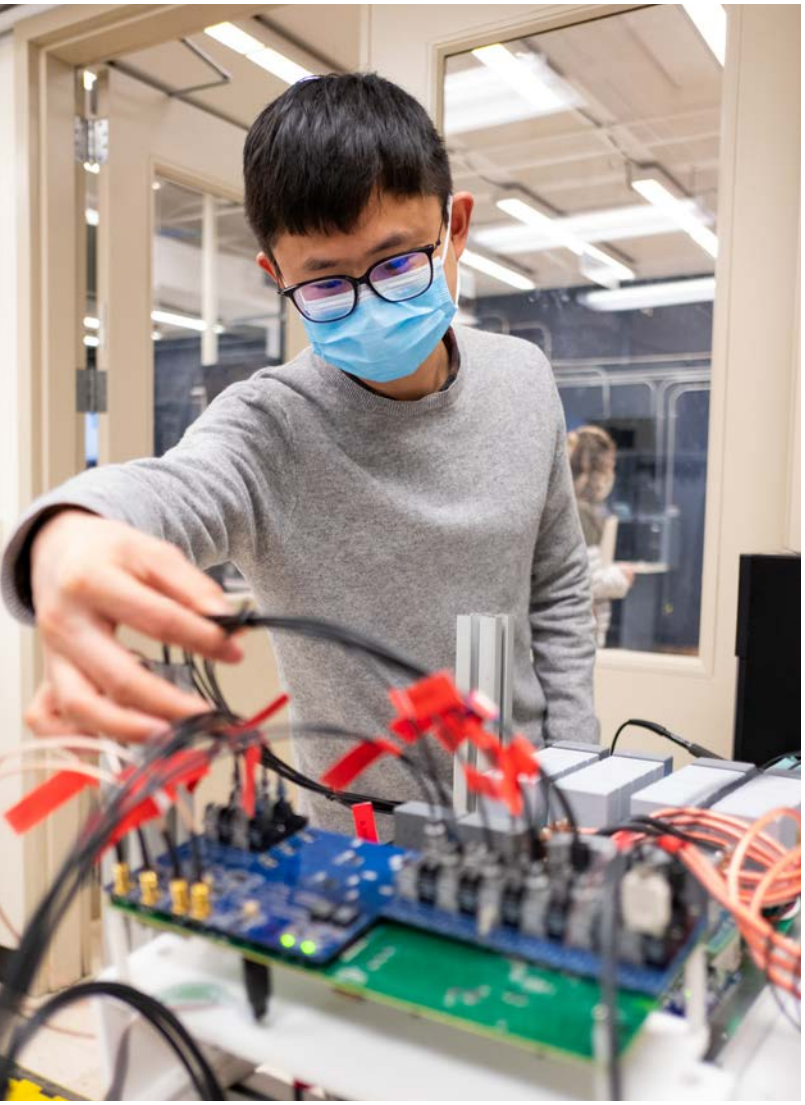
Regional University Alliance (RUA) partnership under the leadership of the National Energy Technology Laboratory (NETL), which, formed by Carnegie Mellon University, Pennsylvania State University, University of Pittsburgh, Virginia Tech, and West Virginia University, sought to advance energy science and technology in grid applications. CPES specifically took a leading role in the NETL-RUA Grid Technologies Collaborative, which had as its mission to "advance grid-scale power electronics and systems," and allowed the center to delve for the first time into the dynamic impact of grid-tied power converters.

The above energy-efficiency-led policy shift at DOE rapidly elevated power electronics to national prominence, which led to the multifaceted development of this critical technology building on top of the fundamental advancements that had been spearheaded by the U.S. Department of Defense (DOD), especially in regard to wide-bandgap (WBG) power semiconductors. As such, CPES played a key role in the formulation of the PowerAmerica Institute led by North Carolina State University, and participated actively throughout the five years of this DOE Advanced Manufacturing Office (AMO)-sponsored program, working jointly with multiple CPES industry members in the advancement of gallium nitride (GaN) and silicon carbide (SiC)-based power conversion technology. This included GaN-based ultra-high-power density converters for power adaptors, commercial, and aerospace applications, SiC-based onboard battery chargers, new electromagnetic interference (EMI) mitigation and suppression strategies for SiC-based UPS, extreme efficiency SiC-based commercial- and utility-scale photovoltaic inverters, and SiC-based aircraft generator-rectifier units qualified for 50,000 ft. operations.

DOE has also prioritized educational programs seeking to develop the future U.S. power engineering workforce, and CPES has had the opportunity to participate in this effort thanks to its AMO-sponsored traineeship entitled "Wide Bandgap Generation (WBGen): Developing the Future Wide Bandgap Power Electronics Engineering Workforce." This graduate-level fellowship program set forth as its main objective to train the next generation of U.S. citizen power engineers with WBG power semiconductor expertise, broadening the range of WBG-based power electronics by conducting research on high-efficiency grid apparatus and high-efficiency electrical power systems, enhancing the power engineering curriculum formalizing WBG-oriented design procedures for power electronics components and systems that can effectively integrate the inherent, challenging material characteristics of these devices, which have rendered design procedures for silicon-based power electronics obsolete. Kicked off in 2016, the WBGen program will have graduated 18 M.S. and 3 Ph.D. students by the end of its tenure in December 2021.

The increased participation in DOE-sponsored programs, supported with the center's own initiative under its mini-consortia on "WBG high-power converters and systems" (WBG-HPCS), "High-Density Integration" (HDI), and "Power Management Consortium" (PMC), has exposed CPES increasingly to higher power and higher voltage power electronics applications, allowing it to attract new funding contributing strongly to this field.

The WBGen program contributed significantly to the strengthening of the collaboration with DOE, allowing CPES to support multiple DOE, DOD, and industry sponsored projects with the participation of its fellows. This became an effective symbiosis supporting existent and new programs secured since its inception, including CPES's effort under the SWITCHES ARPA-E program developing vertical GaN transistors in collaboration with HRL Laboratories, as well as in the DOE Office of Energy Efficiency and Renewable Energy (EERE)-sponsored program "High-Efficiency High-Density GaN-Based 6.6 kW Bidirectional On-board Charger for PEVs" in collaboration with Delta Products Co., in the vehicular technologies office (VTO)-sponsored program "Highly integrated WBG power module for next-generation plug-in vehicles" in collaboration with General Motors, and in the AMO-sponsored program "Next Generation Electric Machines" in collaboration with General Electric.

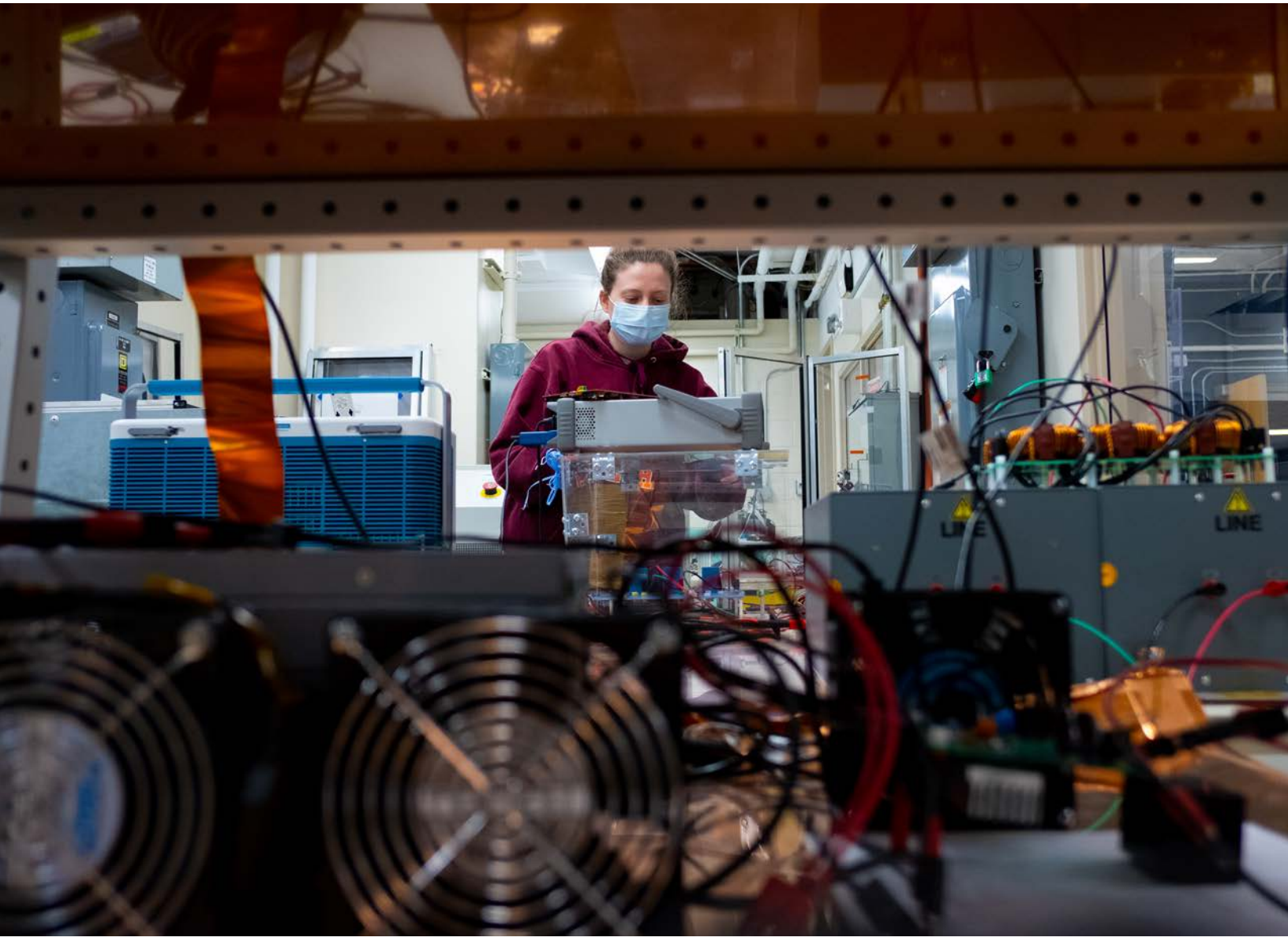


The increased participation in DOE-sponsored programs, supported with the center's own initiative under its mini-consortia on "WBG high-power converters and systems" (WBG-HPCS), "High-Density Integration" (HDI), and "Power Management Consortium" (PMC), has exposed CPES increasingly to higher power and higher voltage power electronics applications, allowing it to attract new funding contributing strongly to this field. This includes the ARPA-E CIRCUITS programs developing SiC-based matrix converters for aerospace applications in collaboration with Raytheon Technologies, and SiC-based modular multilevel converters for medium-voltage grid-applications using 10 kV SiC MOSFET devices, projects conducted in collaboration with ABB and Wolfspeed. More recently, CPES has partnered with Delta Products in the development of high-efficiency, medium-voltage, solid-state transformer-based fast-chargers for electric vehicles under EERE sponsorship, and with Siemens in the development of high-efficiency modular SiC-based power converters for flexible combined heat and power (CHP) systems featuring stability-enhanced grid-support functions to compensate for the impact of renewable energy sources, exploring, too, the advantages of grid-forming controls.

More recently, the CPES collaboration with DOE has continued strengthening, encompassing multiple new research programs sponsored by ARPA-E; namely OPEN "20 kV GaN Switch Technology Demonstrated in High-Efficiency Medium-Voltage Building Block;" BREAKERS "Ultra-Efficient Intelligent MVDC Hybrid Circuit Breaker" in collaboration with Eaton; and ASCEND "Ultra-Light, Integrated, Reliable, Aviation-class, Co-Optimized Motor and Power Converter with Advanced Cooling Technology" in collaboration with Raytheon Technologies. It also features new DOE programs, including VTO "Low-Cost Rare-Earth Free Electric Drivetrain Enabled by Novel Permanent Magnets, Inverter, Integrated Design and Advanced Thermal Management" in collaboration with

Marquette University and General Motors; Solar Energy Technologies Office (SETO) "Power Electronics Based Self-Monitoring and Diagnosing for Photovoltaic Systems," and the most recent AMO "High-Manufacturability 13.8 kV Grid-Interface Power Conditioning Converter with MVAC and MVDC Ports for Flexible Manufacturing Plants," conducted in collaboration with Siemens.

The above programs are the reflection of the unquestionable societal awareness that power electronics has gained over the past decade, which has played a key catalyst role in furthering its development and in positioning it as a critical enabling technology for the U.S. and for the world. CPES has responded opportunely to this challenge, and as such has become fully engaged working with DOE and with several government agencies, as well as with many of its industrial partners, in the advancement of this exciting technical field. The outlook of power electronics is unquestionably promising.



Dr. Yuhao Zhang

Advances in Power Electronic Devices

For the past 10 years, Dr. Yuhao Zhang has been working on wide-bandgap (WBG) technology, researching materials and devices to create smaller, faster, and more efficient power electronic components.

This WBG technology is front and center at CPES. In just the few years that Zhang has been at CPES, he and his colleagues have made huge advancements in the field that have caught worldwide attention.

Last year, Zhang had a remarkable three papers chosen and presented at the Institute of Electrical and Electronics Engineers' (IEEE) annual International Electron Devices Meeting (IEDM), the world's leading forum for reporting technological breakthroughs in the areas of semiconductor and electronic device technology, design, manufacturing, physics, and modeling. Usually only about 20 papers on power devices are accepted by the conference–out of hundreds of submissions from all over the world. Of the 20 accepted papers in 2020, three were submitted by Zhang.

One paper in particular was chosen as the highlight of the 2020 conference, earning the highest score in the power devices section. The paper focused on research Zhang and his colleagues are doing using gallium nitride (GaN) in rectifiers to provide high switching speeds and withstand high-voltage, high-power operations. These are used in electrical power systems that are found in transport, power distribution, and a range of consumer and industrial applications.

Traditionally, these rectifiers have used silicon. But with WBG semiconductor technology, the devices operate at a 10-times higher frequency. A higher frequency means that entire power electronic converters and systems can be smaller and lighter, while at the same time have higher efficiency. These products are then used in practical applications such as on-board chargers for electric vehicles and laptop chargers.

"The ultimate goal is for the devices to conduct high current with low resistance and switch at high speed with very low energy losses," said Zhang.

Zhang's goal is simple: To advance power electronics technology. At CPES, he and his team make devices spanning a wide range of voltage classes, from those with several volts used in consumer electronics such as phones; to those that can block hundreds of volts, like electric vehicles and solar panels to those that block thousands of volts, like on an electrical grid.

Innovations in the WBG field focus on current, voltage, the switching capability, and energy loss, as well as the materials that go into making the structures or devices.

"We have many creative ideas," Zhang said. "We want to make the devices so the power electronics are really light, fast and efficient, and the power loss is really small. It saves so much energy."

Zhang began his work on WBG devices when he was at MIT working on his Ph.D. and later brought his knowledge to Virginia Tech, where he's been an assistant professor in electrical and computer engineering since 2018. In 2019, he was among a group of researchers who won the prestigious George E. Smith Award, which recognized a paper published by the IEEE Electron Devices Society. The paper, titled "Large-Area 1.2-kV GaN Vertical Power FinFETs With a Record Switching Figure of Merit," was written while Zhang was at Virginia Tech, based on work started at MIT.

Zhang said he sees a rosy future for WBG technology, from devices that help increase the charging capacity for electric vehicles–for example, getting 1,000 miles versus 400 miles out of a single charge–to making the chargers for laptop computers smaller. In the future, laptops might not even need an adaptor–just a wire that plugs into the wall.

While his emphasis isn't on commercializing his work–his joy, he says, comes from inventing the technology–Zhang does hope to make an impact in the lives of others with technological advances that can change the world, one semiconductor at a time.

Electric Vehicles get a Boost

The first electric cars date back to the 1800s, when inventors around the world began toying with the concept of a battery-powered vehicle, creating prototypes that were a marvel to the world of horse-drawn carriages.

In 1890, an Iowa chemist introduced the first successful electric car in the United States. It only went 14 miles per hour, but sparked an interest in electric vehicles that continued to grow. By 1900, electric cars made up a third of all vehicles on the road, and prosperous Americans loved them.

But gasoline-fueled cars arrived on the scene as well, and while smellier and noisier, they were also cheaper. By the time WWII ended, so did the early quest for electric vehicles, edged out by gas cars that were cheaper to make and easier to sell. Later years occasionally produced electric-vehicle contenders, but it wasn't until around the start of the 21st century that the race to create the ideal electric vehicle really began. First, there was GM's EV1, which gained a cult following but was discontinued in 2001 because of high production costs, then the Toyota Prius, which became the first mass-produced hybrid electric vehicle, and then the luxury Tesla.

Since then, there's been a push to make the electric vehicle (EV)–and the components that go into it–better, faster and more efficient. It's far from an easy task, but researchers at the Center for Power Electronics Systems at Virginia Tech have risen to that challenge. Their work with the charging systems that make electrical vehicles run have made huge strides in recent years.

An electrical vehicle requires an on-board charger, which is the system built into the car to recharge the battery from the electrical grid while the vehicle is parked. This on-board charger manages the flow of electricity, converting ac power into dc power, which is stored in the battery so the vehicle can travel distances.

Dr. Qiang Li

The challenge faced by EV researchers involves creating an on-board charger that isn't too large or too heavy, so as not to increase the overall weight of the vehicle. Additionally, that charger needs to be able to charge the vehicle quickly, to reduce the waiting time for drivers.

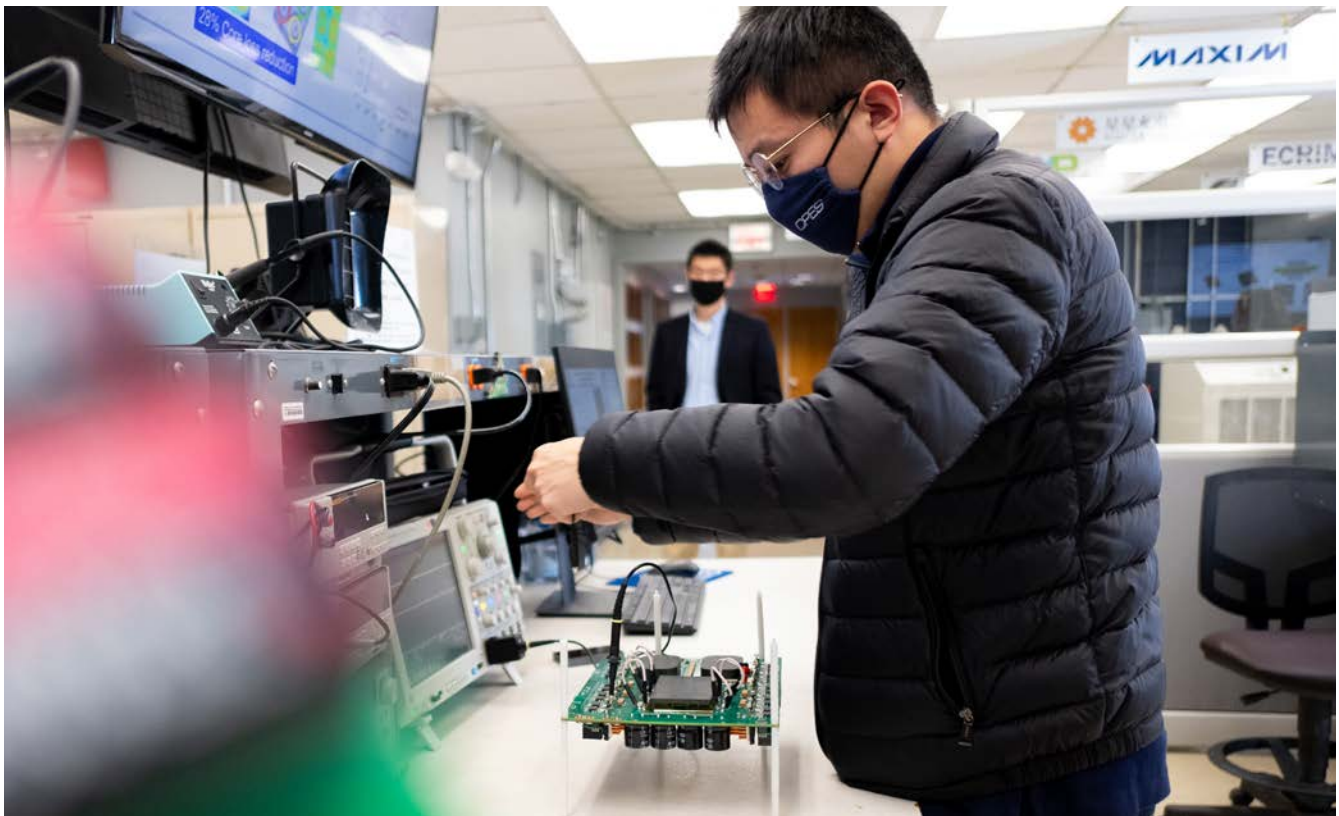
The challenge faced by EV researchers involves creating an on-board charger that isn't too large or too heavy, so as not to increase the overall weight of the vehicle.

"It sounds like an impossible mission," said Dr. Qiang Li, an associate professor in the Bradley Department of Electrical and Computer Engineering (ECE) at Virginia Tech.

But by using wide-bandgap (WBG) technology, Li and his colleagues at CPES have made strides in making a better on-board charger that is more efficient than current models. WBG semiconductors allow devices to operate at much higher frequencies and temperatures than conventional silicon semiconductors, which can help to improve the converter's power level, efficiency, and power density at the same time.

Li and Dr. Fred Lee, a Virginia Tech distinguished professor emeritus, have developed a two-stage, bidirectional, on-board charger (OBC) structure with WBG semiconductor devices. The first stage is an interleaved totem-pole ac-dc working in critical conduction mode with > 300 kHz switching frequency per phase. All the fast switches can achieve zero-voltage switching (ZVS), resulting in small switching loss. The second stage is a 500 kHz CLLC resonant converter featuring a symmetrical resonant tank. In order to deal with the wide battery voltage range, a variable dc-link voltage structure is used. By allowing the dc-link voltage to track the battery voltage, the gain range of the resonant converter is reduced significantly.

Because the switching frequency range is kept narrow, the best efficiency is maintained within the entire battery voltage range. In addition, all the magnetic components are implemented using PCB winding, including the transformer and inductor, for the resonant converter and the coupled inductor for the PFC stage. As a result, manufacturing automation and good parasitic control can be achieved. The PCB-integrated magnetic components also can help to reduce EMI noise when designed with shielding and balance techniques.



Li and Lee have successfully demonstrated several bi-directional on-board chargers, at 6.6 kW and 11 kW. Both of them can achieve 96% efficiency over the very wide battery voltage range and ~3.5 kW/L density. This is, Li said, far beyond the current industry practice.

> *"We hope a lot of the technology we work on will advance electrical technology and help create a more sustainable future."*
>
> *Christina DiMarino, CPES Assistant Professor (ECE)*

Getting the full benefit of WBG devices also requires great care in how they are packaged. They need to be protected from shock and vibration as well as from temperature. Semiconductors generate heat, and if the heat isn't removed, the device will overheat and fail. Recently, researchers have found success with printed circuit board (PCB) technology to tackle the power density, weight, and efficiency issues by embedding the WBG devices right into the circuit board used in the power converter. This also allows for better thermal performance because the device can be cooled from both sides, which enables a higher power output.

"The result is better efficiency and a longer lifetime," said Dr. Christina DiMarino, an assistant ECE professor who is working on advanced packaging technologies for WBG devices. She's also CPES's assistant director, located in the Virginia Tech Research Center in Arlington, VA.

DiMarino and Li are currently working with AT&S, a high-end PCB technology and manufacturing company based in Austria to design, build, and demonstrate a 22 kW power converter with PCB-embedded WBG devices as well as PCB-integrated magnetic components that will be used in on-board chargers for electric vehicles.

None of the on-board chargers currently on the market use this particular PCB-embedding of WBG technology, which will take on-board battery chargers to the next level, DiMarino said. The three-year research project with AT&S began in May 2020, with the team planning to demonstrate a final working prototype by the end of that period. The goal, after research, design-tweaking, modeling and testing, is to have an on-board charger that will be manufactured into a product that will end up in the hands of customers.

If the CPES research continues on its path, that charger will be lighter, more powerful, cut down charging times, and, perhaps most important to consumers, be more cost-effective. The PCB-embedding design actually takes a step out of the manufacturing process.

"This is unique, because we not only reduce the size and weight [of the chargers], we reduce the cost," Li said. "In the long-term, it could be a lot less to manufacture and bring the cost of the vehicles down."

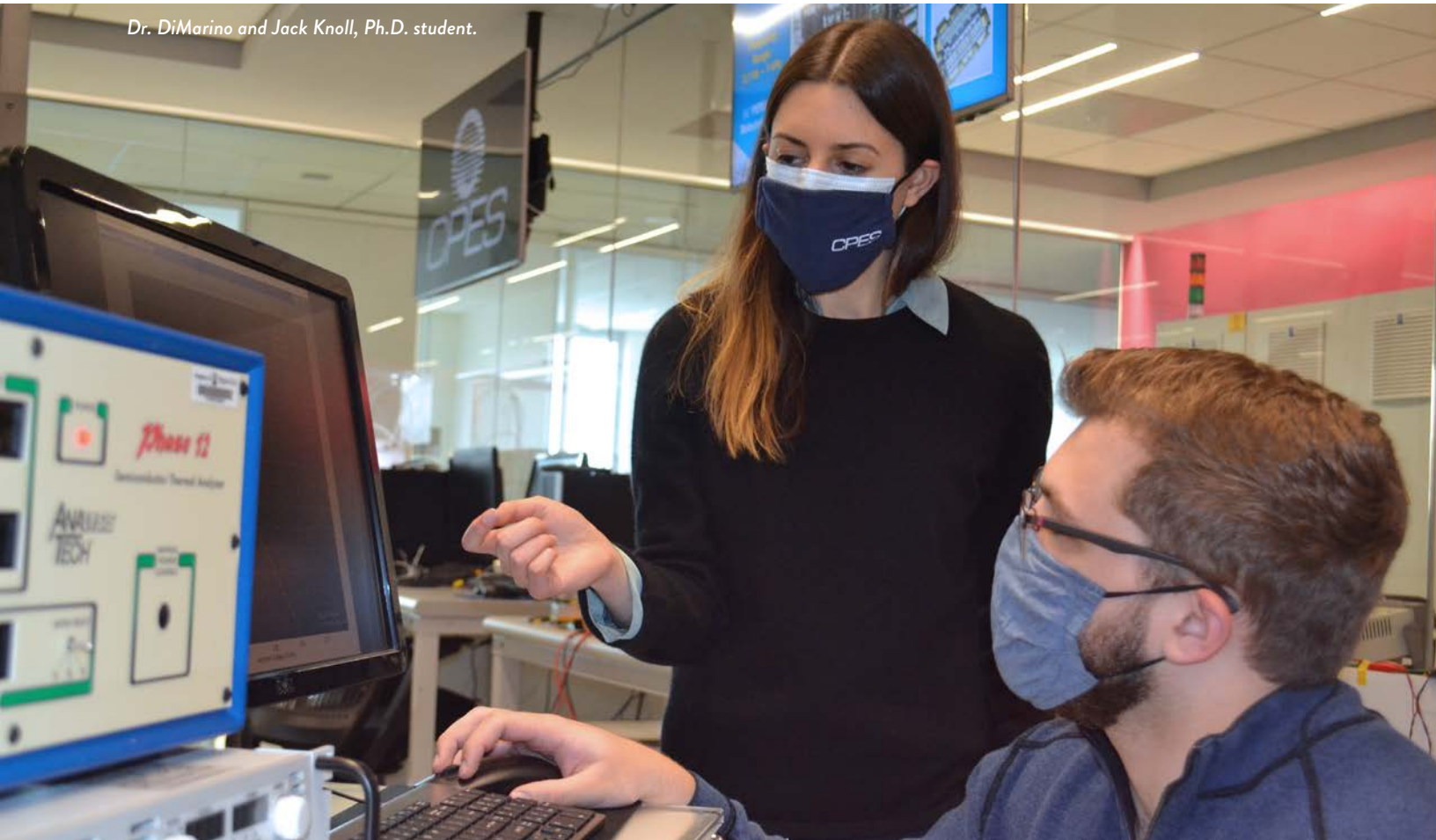
Right now, batteries make up about 40% of the cost of an electric vehicle, but improvements in the power capacity as well as increases in government initiatives for the development of EV infrastructure, such as charging stations, are expected to drive growth for the chargers.

Worldwide, there are more than 5.6 million electric vehicles on the roads – a number projected to grow as consumers adopt a more environmentally friendly mode of transportation over traditional fossil-fuel cars. By 2040, 58% of global passenger vehicles sales are projected to come from electric vehicles, according to Bloomberg New Energy Finance.

CPES also has ongoing research involving off-board fast chargers–the ones that remain at charging stations, where electric vehicles power up. The goal for those is to increase the power output to charge electric vehicles much faster than currently, say, in 10-15 minutes versus an hour or more.

The technologies that CPES has developed for on-board chargers, such as high-frequency soft switching control, integrated magnetic components, EMI-noise reduction with balance concept, and advanced WBG device packages can also be extended to off-board chargers, according to Li. This greatly helps increase their efficiency and power density.

"This is exciting stuff," DiMarino said. "We hope a lot of the technology we work on will advance electrical technology and help create a more sustainable future."



Dr. DiMarino and Jack Knoll, Ph.D. student.

LEADING THE WAY

CUTTING-EDGE ADVANCEMENTS

500 kHz Design Techniques Enabling 5x Power Density and 99% Efficiency for Front-End Converter

The new generation of processors for CPU, GPU, and AI demand a significantly higher current level at 500 A-1000 A. To accommodate this much-increased power demand, the data center server rack must deliver 25-30 kW to server processors with a 48 V backplane power bus instead of a 12 V bus. This change marks the convergence between the telecom power structure and data center infrastructures. With this high rate of electricity consumption, data centers have consumed about 1% of all electricity consumed in 2020 worldwide, which placed great emphasis on efficient power density and cost. The state-of-the-art silicon-based power module is demonstrated at 96% efficiency and power density around 40-50 W/in^3. In this work, a WBG-based LLC converter is demonstrated with significantly improved efficiency and power density. Operating at 500 kHz switching frequency, the circuit topology and design practice is not without significant departure from the current practice as shown in Fig. 1. (a). For example, a complicated transformer structure is broken down into three simple transformer structures that can be easily implemented using a form of 4-layer PCB. Furthermore, these magnetic components are integrated into a compact structure easily manufacturable as shown in Fig. 1. (b). By adding two additional shielding layers into the 4-layer PCB, a superior EMI performance can be achieved over the entire frequency spectrum of interest, from 150 kHz up to 30 MHz. A 3 kW 400/48 V dc-dc converter is demonstrated with a peak efficiency of 99% and a power density of 450 W/in^3 (28 kW/L), as shown in Fig. 2., which is 1.5% higher efficiency and 5 times higher power density than the state-of-the-art at a reduced cost due to its high manufacturability.

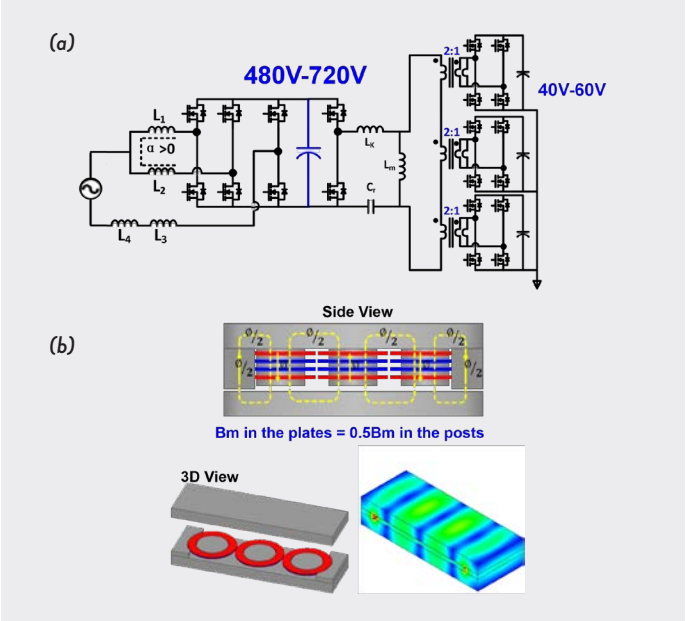


Fig. 1. Proposed structure, (a) proposed circuit diagram, (b) magnetic integration of 3-transformers for LLC converter.

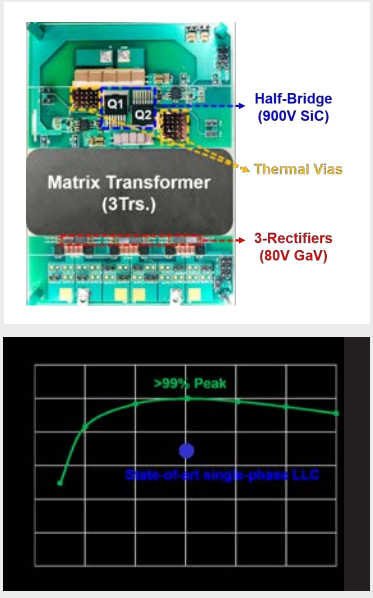


Fig. 2. DC-DC stage prototype and tested efficiency.

High-Frequency Medium-Voltage DC-DC Module Enabling EV Charger to Achieve 3C Rate

To achieve 3C or higher charging rate for an electric vehicle (EV), which means a 180-mile charge within 10 minutes, a solid state transformer (SST)-based 400 kW extreme fast charger (XFC) is proposed. It consists of two main function blocks: an SST and a charge converter, as shown in Fig. 1. Compared to a conventional line frequency transformer (LFT), the SST-based technology can reduce the size and weight, and increase the scalability and flexibility.

The dc-dc stage for medium-voltage isolation is the key of the SST. As shown in Fig. 2., the proposed dc-dc power cell employs a multilevel LLC resonant converter to reduce the number of cells, as well as the number of high-frequency medium voltage transformers. Each dc-dc power cell that is rated 15 kW takes 1.6 kV and converts it to a regulated 1.1 kV intermediate bus voltage. Compared with a traditional dc-dc converter, insulation requirement brings additional significant volume to handle medium voltage. Switching frequency becomes the essential design parameter for high-efficiency and high-power density requirements. A vigorous tool for transformer design is put forward for dealing with complicated multiple design parameters, including transformer turns number, core loss density, and switching frequency and for optimizing multiple objectives, including core loss, winding loss, and transformer volume. In addition, the transformer structure and materials are carefully designed to pass an applied voltage test and partial discharge test.

This work will provide an efficient, compact, and scalable SST based 400 kW XFC, which will accelerate the EV market penetration and promote renewable energy usage.

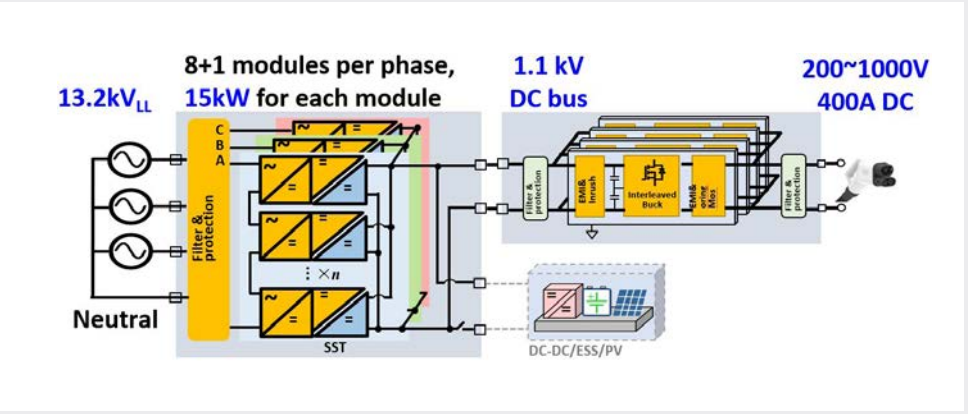


Fig. 1. SST-based 400 kW XFC.

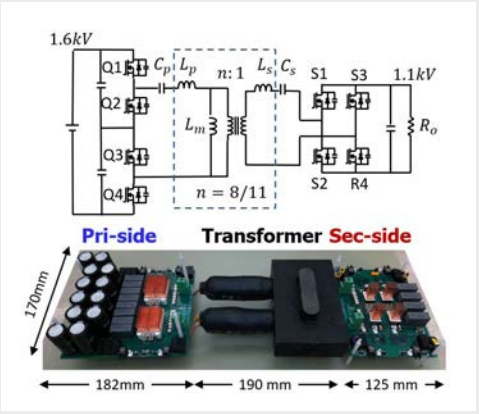


Fig. 2. DC-DC cell: 15 kW multilevel LLC resonant converter.

176 W/in^3 Power Density, 98.4% Peak Efficiency Three-Phase Soft-Switching Bidirectional AC-DC Converter with PCB Winding Coupled Inductor

Three-phase bidirectional ac-dc converters are widely used in grid-tied applications such as the electric vehicle charging stations and the photovoltaic systems. For the commercial products, the system power density is around 10-15 W/in^3 limited by large passive components due to low switching frequency below 20 kHz with silicon (Si) power devices.

Silicon carbide (SiC) power devices featuring much smaller turn-on energy and negligible turn-off energy compared to the Si counterpart help increase the frequency. Especially, critical conduction mode (CRM) operation can maximize the benefit of the SiC devices by eliminating the turn-on loss. In CPES, a 25 kW three-phase bidirectional ac-dc converter is developed with the CRM-based soft-switching modulation. In this method, zero voltage switching or valley switching turn-on is achieved for the whole line cycle so that the frequency can be pushed above 300 kHz.

Besides, to reduce common mode (CM) noise generated by high dv/dt over system parasitic capacitance, the balance technique is used with PCB winding coupled inductors. To make the circuit balance, a return path is added from the ac-dc side and additional inductors are placed in the path, which are coupled with original inductors in the main circuit as shown in Fig. 1. (a). The PCB winding coupled inductors shown in Fig. 1. (b) have the advantages of low profile and easy control on parasitic parameters. By means of the soft-switching technique with the PCB-coupled inductor, 176 W/in^3 power density and 98.4% peak efficiency are achieved as shown in Fig. 2. (a). The balance technique is effective from 300 kHz to 20 MHz reducing CM noise by 16-20 dB as shown in Fig. 2. (b).

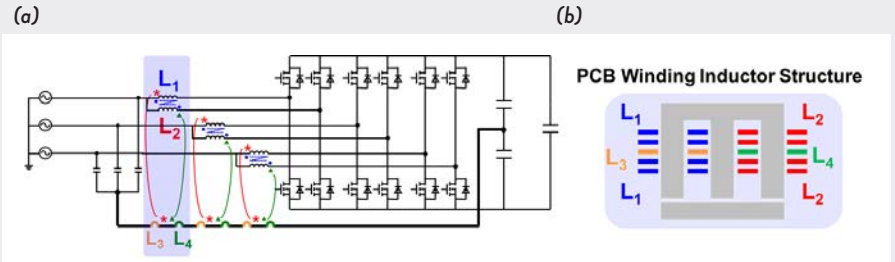


Fig. 1. (a) Circuit topology for two-channel interleaved three-phase ac-dc converter with balance technique (b) Structure of PCB winding coupled inductor.

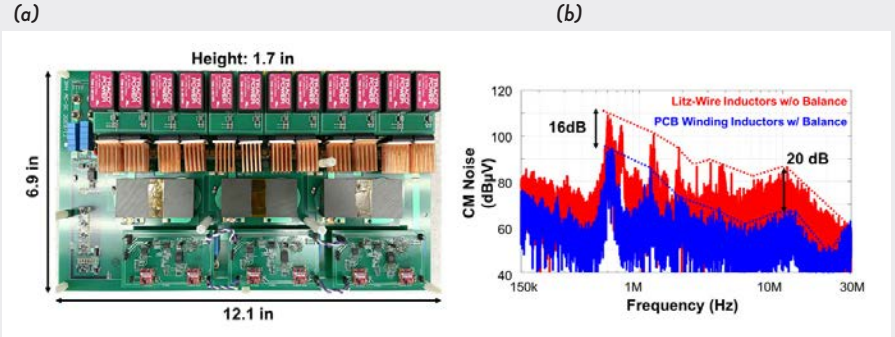


Fig. 2. (a) 25 kW three-phase ac-dc converter prototype (b) CM noise measurement.

A Universal DC-DC Module for Battery Charging Applications

Achieving zero emissions by 2050 in most major cities worldwide is widely acknowledged by countries all over the world. The electric vehicle (EV) can play an important role due to its fewer greenhouse gas emissions. To make the EV compatible with a traditional gasoline-driven car, larger battery pack and fast-charging technology are both essential. The fast-growing EV market brings great opportunities to the fast-charging infrastructures. In the state-of-the-art EVs, the 400 V Lithium battery design is the mainstream. Some EV manufacturers are considering 800 V Lithium battery design to improve the performance of EVs. Considering current and future prospects, it is worthwhile for investors to look into developing a battery charger with wide output voltage range from 200 V to 800 V (or higher) to serve all the mainstream EVs.

This work demonstrates a two stage dc-dc module, which consists of a three-phase CLLC converter and four-phase interleaving buck converter to meet the wide output voltage range with features such as modular design, isolation, bi-directional energy transfer, high efficiency, and high power density as shown in Fig. 1. With SiC devices, the proposed converter can run at high switching frequency so that the resonant inductors and transformers of three phases can be integrated into one six-leg core and built with PCB windings. The four-phase buck converters use negative coupling inductors with PCB winding structure. The peak efficiency of the proposed converter shown in Fig. 2. can be up to 97.7% and its power density is up to 100 W/in^3. This dc-dc module has very wide applications. It could be the second stage for an on-board charger with three-phase ac input. It also could be the final stage of an off-board charger with 850 V dc link as its distribution bus.

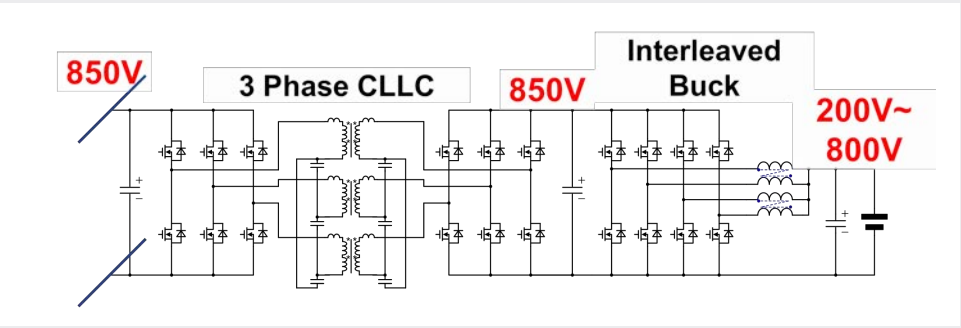


Fig. 1. Topology of proposed converter.

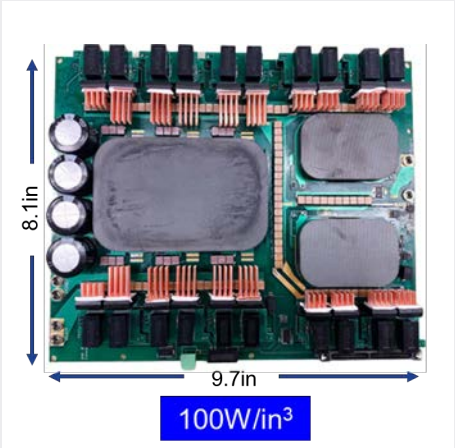


Fig. 2. Prototype of proposed converter.

Fast Transient Response, High Efficiency 48 V/1 V Sigma Converter for High Current CPU Application

As U.S. data centers' power demands increase, it is imperative that more efficient power conversion solutions with higher power density be developed. This can be accomplished using a one-stage quasi-parallel power architecture known as the Sigma converter. The proposed power delivery architecture shares the power between two converters connected in series from the input side and parallel connected from the output side. As opposed to well-established two-stage solutions, higher conversion efficiency is always obtained with the Sigma converter. A variable-controlled gain LLC converter with novel magnetic integration is utilized in the Sigma converter architecture powering the CPU, as shown in Fig. 1. This enables efficient wide voltage range operation. A converter prototype has been built that meets Intel's VR specifications; the converter can provide a maximum output current of 120 A, while achieving maximum efficiency of 95% and power density of 700 W/in^3.

In addition, a control method has been proposed for the Sigma converter to meet Intel VR13 transient specifications. Simulation and hardware results show the Sigma converter with the control method can achieve adaptive voltage positioning (AVP) and very fast transient response. With the high-efficiency, high-power density and fast transient response, it is verified that the Sigma converter has great potential in data center applications.

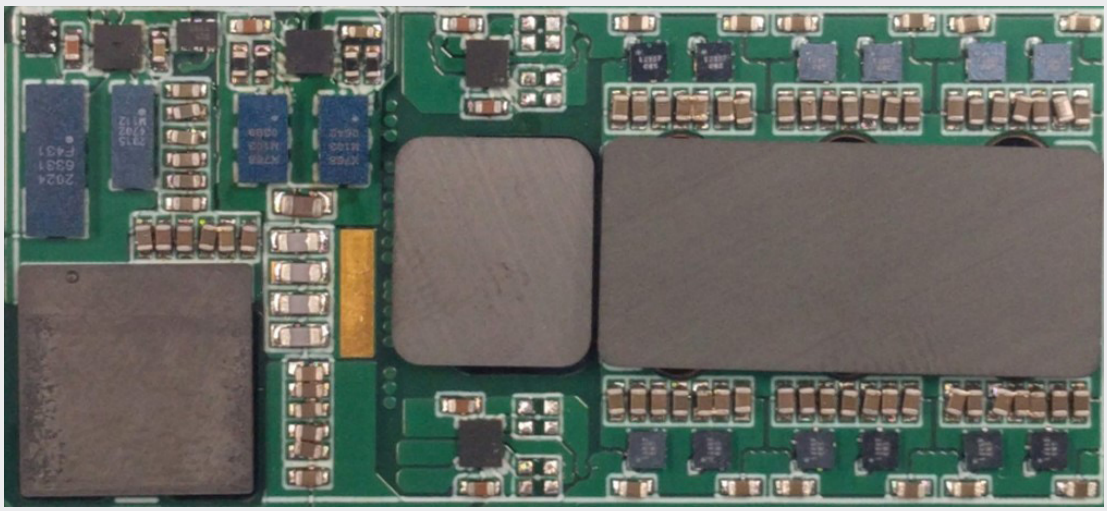


Fig. 1. Wide voltage range Sigma converter prototype.

Multi-Kilovolts Gallium Nitride Power Rectifier Exceeding the Silicon Carbide Limit

Kilovolts power rectifiers are widely used in medium-voltage power electronic applications such as electricity grids, industrial motor drives, and renewable energy processing. Bipolar silicon (Si) p-n diodes dominate today's multi-kilovolts rectifier market, but they suffer from a very poor reverse recovery. Unipolar silicon carbide (SiC) Schottky barrier diodes (SBDs) and junction barrier Schottky (JBS) diodes have been recently available up to 10 kV and commercialized at 3.3 kV.

Gallium nitride (GaN) has superior physical properties as compared to Si and SiC. AlGaN/GaN high electron mobility transistors (HEMTs) based on the two-dimensional electron gas (2DEG) channel have been commercialized to 650 V. Recently, large-area AlGaN/GaN wafers with multiple vertically-stacked 2DEG channels are available, which enables much higher current (and power) handling capabilities and lower specific on-resistance as compared to a single 2DEG channel. The multi-channel wafer opens a new door for developing multi-kilovolts power rectifiers.

This work demonstrates 5 kV AlGaN/GaN SBDs on a four-inch, five-channel, low-cost GaN-on-sapphire wafer. The device highlights a novel three-dimensional anode structure with p-n junctions wrapping around multiple fin-shaped 2DEG channels shown in Fig. 1. This structure enables good electric field management and control of leakage current. The devices have a low on-resistance of 13.5 mΩ cm^2 and a high breakdown voltage up to 5.2 kV. The device's figure-of-merit in Fig. 2. exceeds the 1-D SiC unipolar limit. Large-area multi-channel SBDs are demonstrated for the first time, with a 1.5 A current, a 4.8 kV BV with ~μA leakage current, and a 13 nC total charge. These results show the great potential of AlGaN/GaN multi-channel devices for medium-voltage power applications.

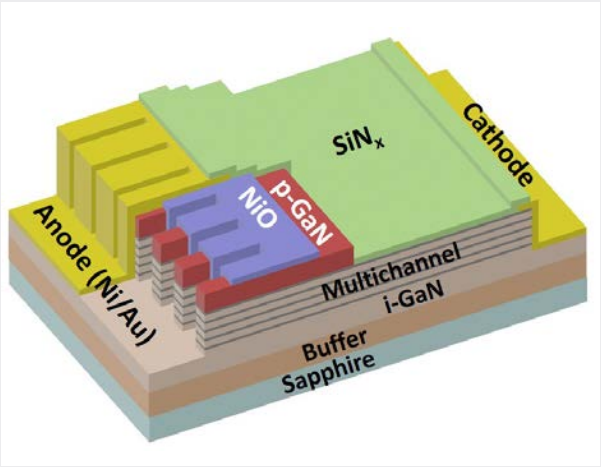


Fig. 1. Schematic structure of the multi-channel AlGaN/GaN Schottky rectifiers.

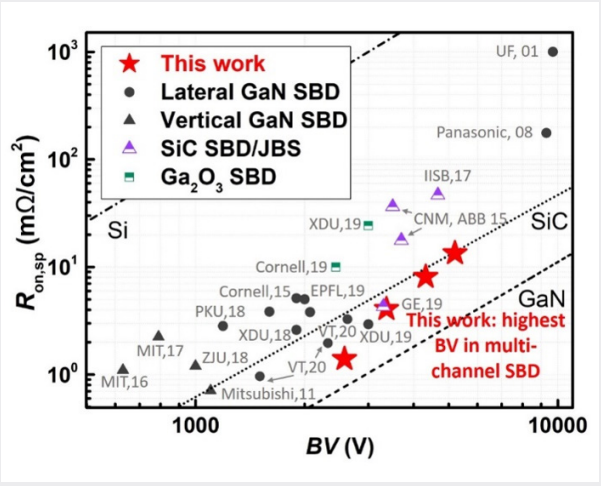


Fig. 2. Specific on-resistance versus breakdown voltage of our multi-channel AlGaN/GaN rectifiers and other state-of-the-art medium-voltage Schottky rectifiers.

Enhancing Surge Ruggedness with Ultra-Wide-Bandgap Semiconductors

The surge current value is listed in the datasheet of any power diode. In power electronic applications, the power diode must be able to temporarily carry a current intensity noticeably higher than its rated current; i.e., the current that it can sustain in steady state conditions. The surge current ruggedness has become a concern for many wide-bandgap (WBG) semiconductor devices, due to the smaller die size. In silicon carbide, bipolar currents are thereby introduced to boost the surge current capability, but they would compromise the device switching speed.

Ultra-wide-bandgap (UWBG) semiconductors can potentially allow a higher thermal stability than WBG materials. The temperature coefficient of electron mobility in UWBG materials is usually smaller than that in WBG materials, making the device's on-resistance more stable and therefore reduce the risk for thermal runaway. Among the major UWBG semiconductors, gallium oxide (Ga_2O_3) provides the availability of large-diameter wafers growing from the melt; i.e., the growth method similar to Si that can potentially result in low material cost.

This work presents the first experimental demonstrations of the packaged large-area Ga_2O_3 Schottky barrier diodes (SBDs), and, for the first time, reports the surge current capabilities of UWBG devices. To overcome the low thermal conductivity of Ga_2O_3, a double-side-cooling package is employed. These packaged diodes with a 3×3 mm^2 contact area can sustain a peak surge current over 60 A (Fig. 1.), with a ratio between the peak surge current and the rated current superior to that of similarly-rated SiC SBDs (Table 1.). These results show the great potential of UWBG devices for fault protection applications in power electronics systems.

TABLE 1

Comparison of the Surge Current Capability of SiC and Ga_2O_3 Schottky Barrier Diodes.

Device	Rated Current (A)	Max Surge Current (A)	Max surge current over rated current
SiC SBD (CSD01060A)	4	20.3	5.1
SiC SBD (CSD02060A)	8	26.9	3.36
SiC SBD (CSD03060A)	11	31.8	2.89
Bottom-side-cooled Ga_2O_3 SBD	6.2	37.5	6.05
Double-side-cooled Ga_2O_3 SBD	9.2	68	7.4

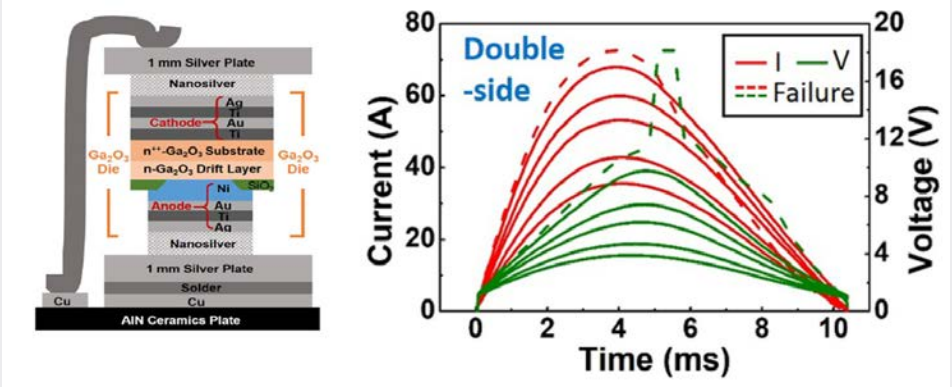


Fig. 1. Schematic of the double-side-cooled Ga_2O_3 Schottky diodes packaging (left) and their surge test results (right).

Closing the Gap Between High-Density and High-Voltage in Multi-Die Power Modules with 10 kV SiC MOSFETs

Silicon carbide (SiC) MOSFETs have the potential to drastically improve the size and efficiency of high-voltage power systems due to their improved blocking voltage, lower on-state losses, and faster switching speeds when compared to conventional silicon IGBTs. However, present power module packages are limiting the performance of these unique devices. Asymmetric device layout and bulky system interfaces cause high commutation inductance, limiting switching speed and increasing loss. As the rated voltage of multi-die power modules increases, these shortcomings are exacerbated due to the need to adhere to strict creepage and clearance requirements between the terminals, which inherently increase trace length inside and outside the package, further increasing commutation loop inductance and decreasing power density.

This work demonstrates an innovative 10 kV package concept (Fig. 1.) that employs a fully enclosed, spring-pin termination style that voids the need to adhere to creepage and clearance standards (Fig. 2.). Guard ring design techniques used in the fabrication of high-voltage dies are borrowed and reimagined in the form of PCB-embedded guard rings to aid in the electric field crowding around the terminals. Leveraging these technologies, a PCB-integrated bus bar is proposed, which allows for the integration of the bus bar and the gate drivers into a single PCB, and allows for a terminal spacing of 6 mm compared to an industry standard 40 mm terminal spacing on 10 kV-rated power modules. The decreased terminal spacing enables the high-power density of the module, which measures only 83 mm x 68 mm x 16 mm and is rated for 80 A continuous at 10 kV, as well as the 4 nH commutation loop inductance. The result is a voltage and current scalable module capable of switching speeds > 140 V/ns without compromising on long-term reliability, insulation performance, or power density.

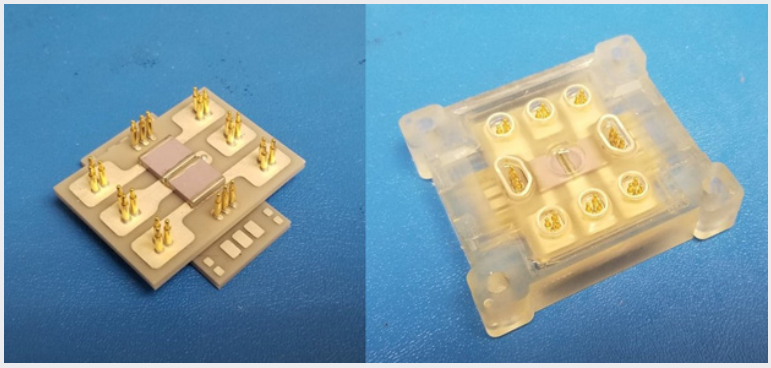


Fig. 1. Wirebond-less 10 kV 20 A SiC MOSFET phase-leg power module with 6mm terminal-to-terminal spacing without encapsulation (left) and with encapsulation (right).

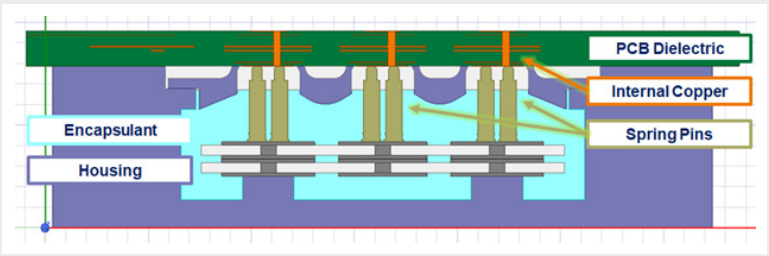


Fig. 2. Cross section of wirebond-less SiC power module showing the fully enclosed spring pin terminations enabling the high-density form factor.

Rethinking High-Density Power Converter Design Using Advanced Substrate Technology

A 250 kW, SiC-based integrated power electronics building block (iPEBB) is being explored for high-frequency, high-power density applications. This converter seeks to be the building block for future power systems with its light-weight, high manufacturability design, as shown in Fig. 1. (a). The iPEBB's unique topology enables flexible (dc-dc, dc-ac, ac-dc), galvanically-isolated, bidirectional power conversion, illustrated in Fig. 1. (b). The iPEBB uses state-of-the-art substrates like multi-layer silicon nitride (Si_3N_4) and organic direct bonded copper (ODBC) to achieve a high-density design (15 kW/L). These substrates play a vital role in the thermal, electrical, and mechanical performance, as well as the weight and reliability of the converter. The proposed iPEBB structure enables the SiC bridges to have smaller power loop inductance (3 nH), improved heat dissipation,and lower EMI, while meeting strict weight limitations (< 16 kg). A portion of the SiC bridges, referred to as a switching-cell, consists of a phase-leg with two paralleled 1.7 kV SiC MOSFET devices, detailed in Fig. 1. (c). The improved electrical and thermal design allows for fast switching (250-500 kHz), which reduces the size of the transformer and other passive components. Furthermore, the primary and secondary sides of the iPEBB have identical layouts, which simplifies manufacturing and reduces cost. To validate the design, the high-frequency transformer and the switching-cell have been packaged and prototyped for testing (Fig. 2.). The iPEBB's usage of advanced substrate technology will allow for reduced cost, size, weight, and design complexity of electrical systems.

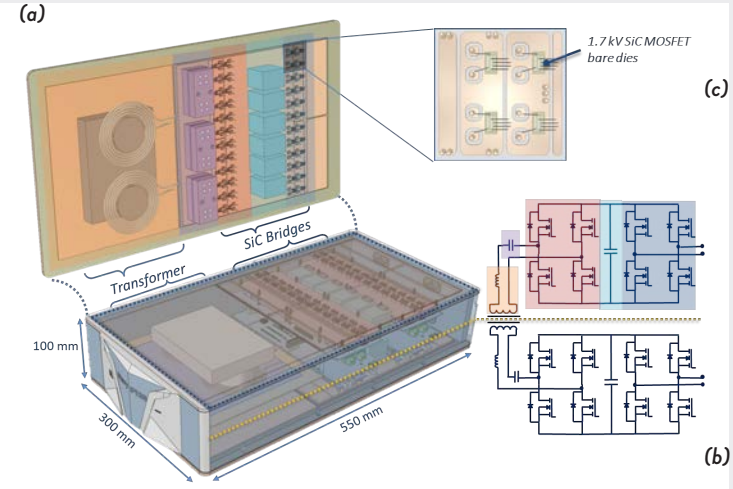


Fig. 1. (a) iPEBB design with a top view of the primary side, (b) iPEBB topology, (c) switching-cell portion of the SiC bridges.

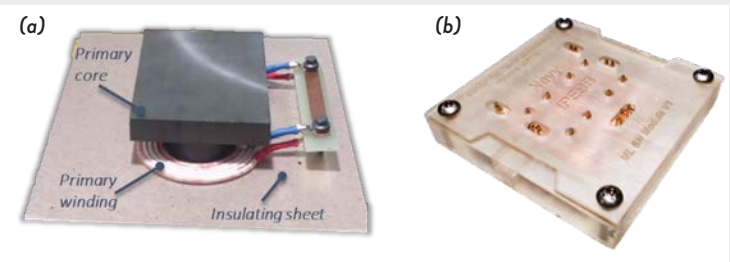


Fig. 2. (a) iPEBB high-frequency transformer V1 from FastWatt, (b) packaged iPEBB 1.7 kV SiC MOSFET switching-cell.

High-Frequency Multi-Channel Auxiliary Power Supply with Ultra-Low Coupling Capacitance for SiC-based Medium Voltage Systems

As many emerging medium voltage (MV) applications desire high-power density, high efficiency, and small footprint power converter, 10 kV SiC MOSFETs becomes an attractive solution for such MV applications due to their high breakdown voltage, fast switching speed (> 50 V/ns), and low switching loss. However, to energize the device safely, a high-performance isolated auxiliary power supply (APS) is required. High insulation capability (> 20 kV), low common-mode coupling capacitance (< 5 pF), and small footprint are the main design criteria in the APS design. Additionally, considering the lifetime of the APS's insulation system, no partial discharge (PD) under normal operating voltage is another critical design factor. Furthermore, since the APS needs to power many circuit components such as gate drivers, sensors, and controllers, multi-channel outputs with regulated output is preferred.

This work presents a high-density auxiliary power supply design with galvanic insulation enabled by a 1 MHz current-fed single-turn transformer. The current transformer is optimized based on the proposed design method that allows the transformer to achieve high partial-discharge inception voltage (PDIV), low coupling capacitance, and high output power. LCCL-LC resonant topology is adopted in the APS to create a constant current source on the output of sending side shown in Fig. 1., so the multi-channel output is achieved. A design procedure of resonant components is proposed to achieve a consistent soft-switching operation under a random number of output channels and installation set-ups. Furthermore, a regulation network is added, so the APS can operate under varied load conditions including faulty load conditions. Finally, two versions of APS shown in Fig. 2. based on air and silicon dielectric materials are built, achieving PDIV of 6 kV and 17 kV respectively, and the corresponding coupling capacitances are 1.86 and 3.6 pF.

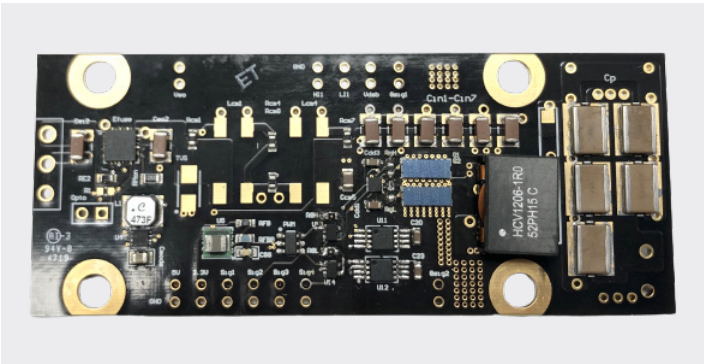


Fig. 1. Hardware prototype of APS's sending side circuitry.

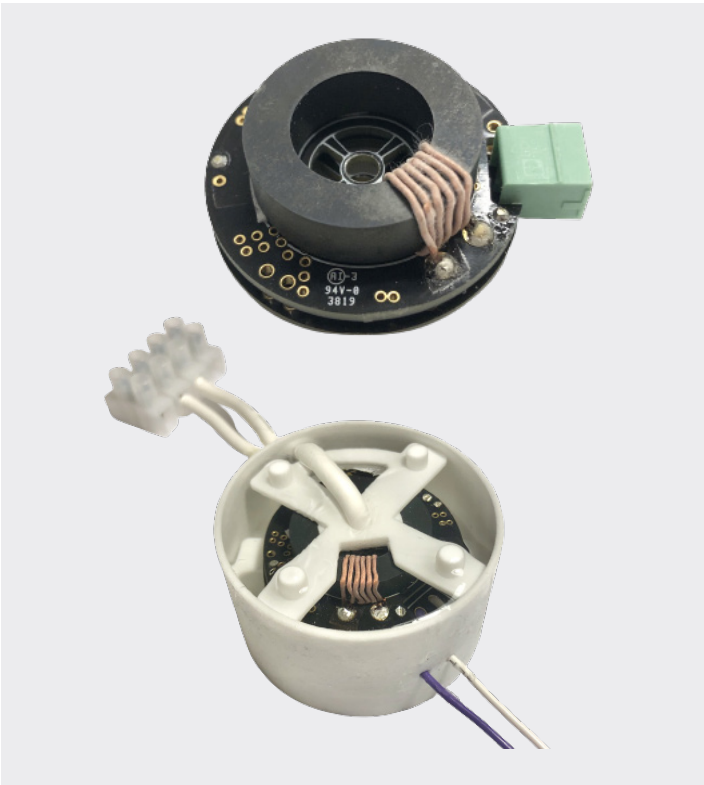


Fig. 2. Hardware prototypes of APS's receiving side circuitries with air-insulated design (top) and silicone-insulated design (bottom).

An 18 kW, 142 W/in^3, 500 kHz, 98.8% Isolated Bidirectional Partial Power Converter with 2-D Flux Cancelation Layout and Intra-Leaved Transformer

The demand for high-density, high-efficiency bidirectional battery chargers is driven by the fast development of energy storage systems in renewable energy system, micro-grid, and transportation electrification. The isolated dc-dc converter that interfaces a battery with a dc bus is one of the critical components. As shown in Fig. 1. (a), input-parallel output-series (IPOS) partial power (PP) converter is considered a promising high-efficiency, high-density solution because only a fraction of power is processed via multi-stage converters to regulate the output voltage.

To explore the limits of power density, the switching frequency was pushed to 500 kHz, which is at least 10 times higher than the current commercial product. Benefiting from increasing frequency, the size of the 18 kW high-frequency (HF) transformer can shrink dramatically. To optimize the loop inductance of a CLLC-type dc transformer, a 2-directions (2-D) flux cancelation layout and Intra-leaved method are proposed for full bridge circuit and transformer, respectively. As shown in Fig. 1. (b), with the adoption of 1.2 kV silicon carbide (SiC) and 650/150 V gallium nitrate (GaN) on the primary and secondary sides, the prototype peak efficiency and total power density (including heatsink, fan, and controller) were achieved at 98.8% and 142 kW/in^3. The corresponding steady-state waveforms at full load is shown in Fig. 2.

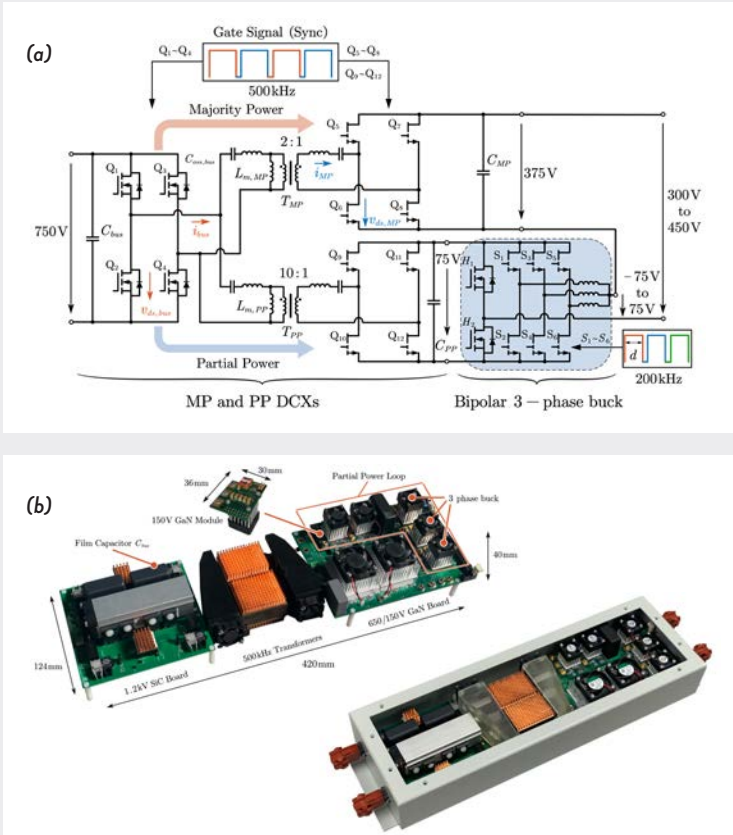


Fig. 1. (a) Circuit diagram of IPOS PP converter (b) 18 kW PP converter prototype operated in 500 kHz.

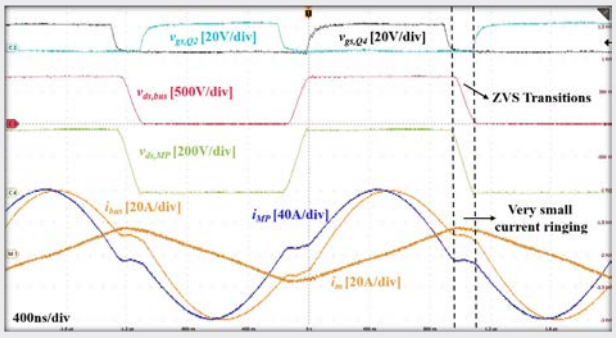


Fig. 2. Steady-state waveforms at 18 kW.

Assessment Methodology to Exceed 30 kV Partial Discharge Inception Voltage in Compact Converters

During the development of SiC-based medium voltage (MV) converters, compact and reliable insulation is required. Due to the high-power density requirement and the fast-switching transient, the size of a highly overdesigned insulation system is not acceptable. Therefore, insulation design for individual components and their coordination inside a single power cell, as well as among multiple converters in the system, is one of the major design aspects for future SiC-based MV converters. A well-designed insulation system that remains partial discharge (PD)-free during normal operation not only helps to reach an expected insulation lifetime and enhance the converter system's electrical performance, but also prevents cascaded failure that may be initialized by significant discharges.

With the established testbed in CPES (Fig. 1.), we have the capability to measure PD under 60 Hz sinusoidal or square excitation with varied parameters. Different types of PD sensors can be applied depending on the application. With our state-of-the-art PD detection system (< 10 pC sensitivity), the phase resolved partial discharge (PRPD) pattern can be captured and analyzed; this helps determine the type and severity of discharge. By implementing visual detectors, the location of corona discharge and flashover points can be identified as shown in Fig. 2. Therefore, different insulation design and realization ideas can be experimentally compared and verified. As demonstrated in several CPES papers, insulation design and assessment concepts are applied for all MV projects. With proper material, processing and electric field management, required minimum insulation size can be reduced up to 70% with improved PD performance.

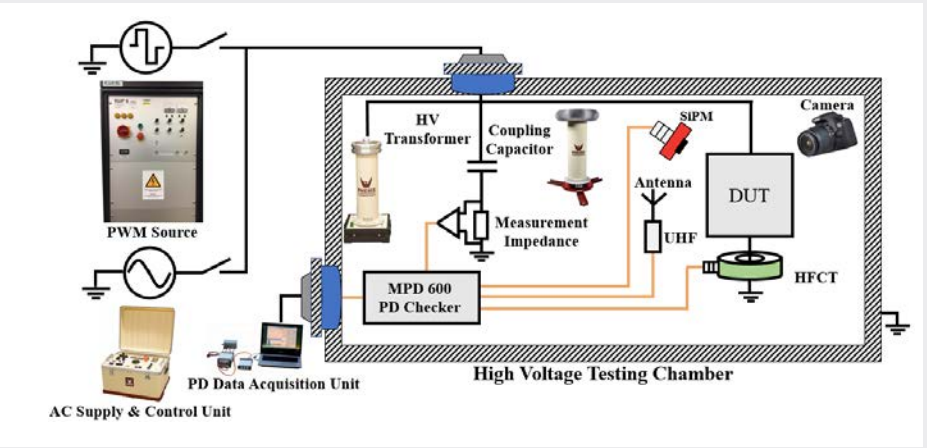


Fig. 1. High-voltage testbed for partial discharge and insulation system analysis.

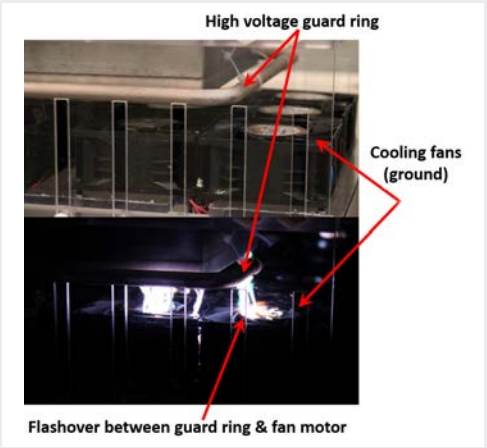


Fig. 2. Flashover between high-voltage guard ring and earth-grounded fans.

Auxiliary Power Network Architecture for Medium/High Voltage Power Converters

SiC devices have been widely explored in different applications thanks to their characteristic superiority. Among these applications, a medium-voltage (MV) power electronics building blocks (PEBB)-based modular multilevel converter (MMC) becomes an attractive topic because of its voltage and current scalability. However, the complex electromagnetic environment caused by the high-speed transient behavior, the limited space-caused compact design requirement, and higher power consumption caused by a more intelligent system all bring challenges for building a reliable auxiliary power supply network (APSN) for gate drivers, sensors, and controllers. A two-stage solution as shown in Fig. 1. is proposed to enable an APSN with high reliability, high efficiency and power density, high insulation capability, and low EMI susceptibility.

As shown in Fig. 1., for the first stage, auxiliary power supplies (APS) powered from three different sources i.e., external grounded low voltage source, PEBB dc-link capacitor, and battery, can make sure the MV system has auxiliary power in different operation conditions including start-up, normal operation, shutdown, or fault condition. Type I APS utilizes wireless-power-transfer technology providing a stable, mechanically flexible, independent source with 30 kV insulation capability, and 3 pF isolation capacitor. However, when more and more PEBBs are connected in series, type II APS, which is a soft-switching switched capacitor converter, is required so that the power can be fed inside the power cell directly stepping down voltage from 6 kV dc-link to break the limitation caused by insulation capability of the type I APS. Type III APS is a battery-based uninterruptible power supply, which is used to "fill the gap" during fault conditions. The output ports of the first stage APS are connected in parallel to an auxiliary power supply bus. For the second stage, a single-input-multiple-output current-transformer resonant converter is proposed to provide regulated output voltage for different isolated loads with 6 kV insulation capability, and 1.8 pF isolation capacitor. Fig. 2. shows the aforementioned converter prototypes in the auxiliary power network.

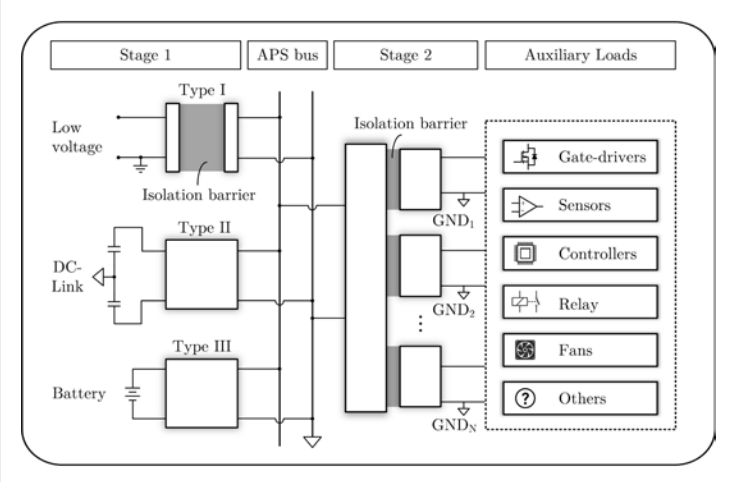


Fig. 1. Auxiliary power network architecture.

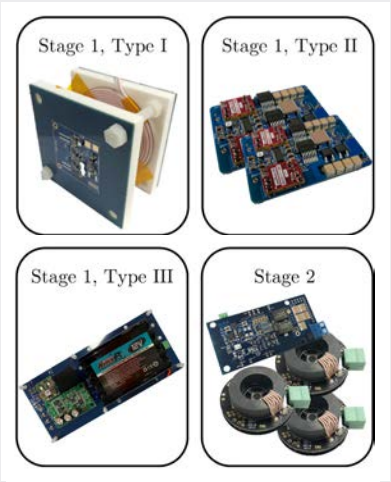


Fig. 2. Converter prototypes in the auxiliary power network.

Control Method of ICBT Cells Enabling High-Power Density, Modular Medium-Voltage Converters

In medium-voltage (MV) systems such as MV high-speed motor drives and ship-to-shore converters, it is often required to build power converters of higher voltage ratings with semiconductor devices of lower voltage ratings. The traditional solutions include using serial-connected devices, which brings the challenge of dealing with voltage unbalance among the devices, and employing multilevel converter topologies, which usually requires bulky capacitors and therefore low-power density. Converters having integrated capacitor-blocked transistor (ICBT) cells, as shown in Fig. 1., provide a new method. In this study, the control method of ICBT-based converters is explored in detail to ensure the safe operation and to fully exploit the advantages.

Each ICBT cell is controlled to operate as a single switching device, and the cells in the same arm are controlled to operate synchronously and behave as a high-voltage device. Each device only needs to block the corresponding cell capacitor voltage. Voltage balance among devices is achieved when cell capacitor voltage balance is achieved, which is ensured by a proposed closed-loop method. Based on sampled cell capacitor voltages and arm currents, delays are added to gate signals of devices to adjust cell capacitor voltages. With the proposed control method, ICBT-based converters enable direct power flow from input to output, do not require large cell capacitors and therefore have high-power density. Converters also have the modularity and voltage scalability. In addition, ICBT cells can be used to build converters with different topologies.

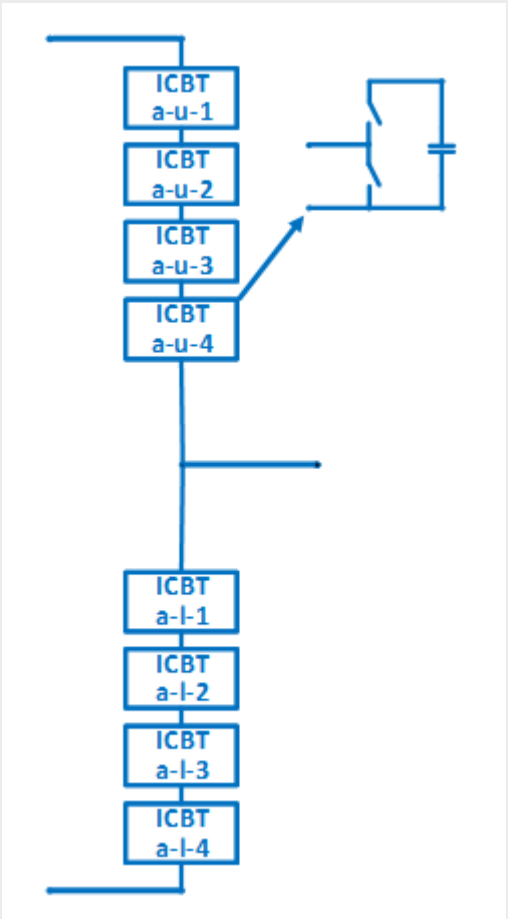


Fig. 1. An ICBT-based phase leg with four cells per arm.

Distributed Communication and Control System with Sub-ns Synchronization Accuracy for Fast Switching Modular Medium-Voltage Power Converters

The modular power electronics building block (PEBB)-based converter has been proven promising in medium-voltage applications due to its modularity and scalability. For conventional centralized control architecture, the cable connections become bulky and complicated with a large number of PEBBs. In contrast, in a distributed control and communication network, each node contains a PEBB controller that communicates with the power stage (enhanced gate driver). This way, the control is distributed between the main controller, local controllers, and gate drivers, which increases the modularity of the system.

For the whole system operation, PEBB controllers are connected using a specific topology that significantly reduces communication interfaces. However, the synchronization accuracy becomes a factor that requires careful design. A customized PEBB controller with Xilinx Zynq-7030 SoC module is designed to realize the sub-ns synchronization accuracy. The closed-loop PLL, implemented on the controller, combined with the precision time protocol (PTP), regulates the voltage-controlled crystal oscillator (VCXO) so that clocks of all controllers in the network are syntonized and timers synchronized. On the other hand, a physically shared clock between the local controller and gate drivers inside PEBB allows timer synchronization at the same sub-ns accuracy. Very tight synchronization allows the execution of an action/command on every node (controller or gate driver) in the network at the exact predefined moment.

The distributed communication and control system enables the operation of modular, SiC-based, fast switching PEBB converters. For synchronization between controllers, a state-of-the-art "White Rabbit" (WR) protocol is implemented, and sub-ns synchronization accuracy achieved. Enhanced gate drivers equipped with powerful FPGAs, communication interfaces, and current (Ids) sensors, allow that part of the control algorithm is executed on them, allowing control to be distributed not only among controllers in the network but among the gate drivers, too. The communication network that consists of one main and three local PEBB controllers connected in linear daisy chain topology (Fig. 1.) shows synchronization performance. The clock jitter at each node is ~1 ns.

Fig. 1. Synchronization accuracy measurement.

CENTER OVERVIEW

2020 DASHBOARD

Research

$6.5M
Research Expenditures

46
New Sponsored Research Projects

Scholars

185
Total
Since 1977

7 Ph.D. Degrees Awarded

194
Total
Since 1977

3 Master's Degrees Awarded

21 Visiting Scholars from Seven Countries

Leading with Distinction

2

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Dushan Boroyevich
Fred C. Lee

Election to National Academy of Engineering membership is one of the highest professional honors accorded an engineer.

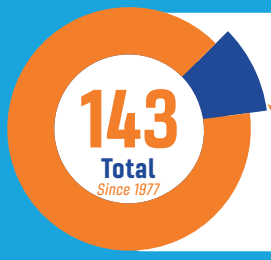
4

IEEE Fellows

Dushan Boroyevich
Guo-Quan Lu
Fred C. Lee
Khai Ngo

IEEE Fellow is a distinction reserved for select members who have demonstrated extraordinary accomplishments in their field.

Intellectual Property



6 U.S. Patents Awarded

15 U.S. Patent Applications Filed

IP Sharing Expenses

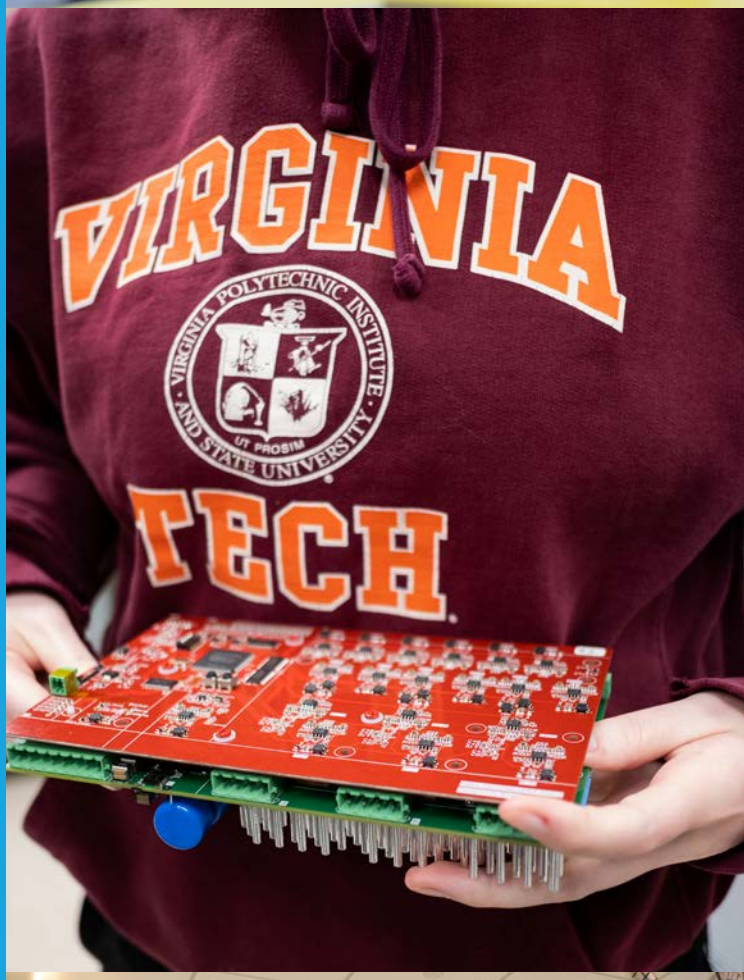
$157K

Industry Consortium

Consortium Value

$2.4M

90 Consortium Members



CPES Industry Consortium

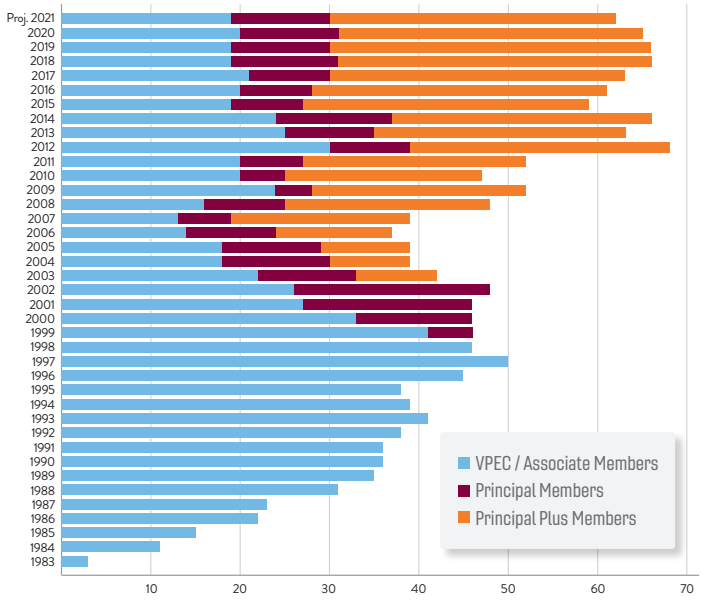
The CPES industrial consortium is designed to cultivate connectivity among researchers in academia and industry, as well as create synergy within the network of industry members.

The CPES connection provides the competitive edge to industry members via:

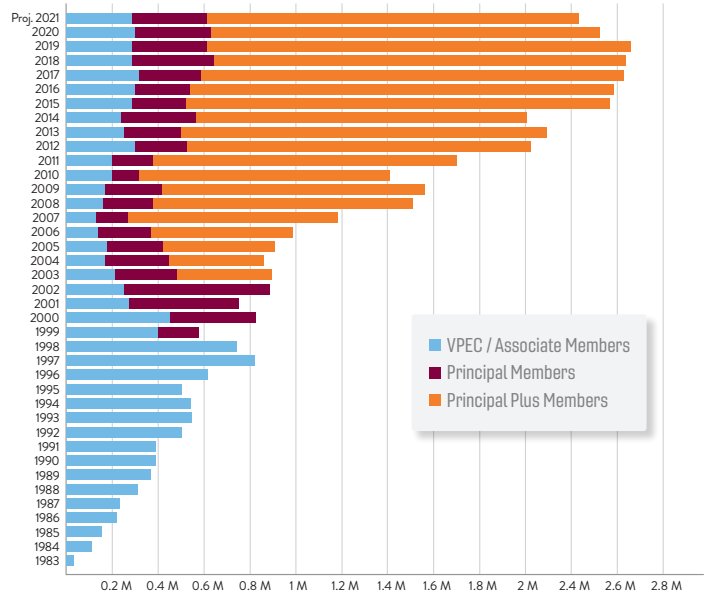
- Complimentary registration for CPES Annual Conference
- Access to state-of-the-art facilities, faculty expertise, top-notch students
- Leveraged research funding of more than $6 million per year
- Industry influence via Industry Advisory Board
- Early access to intellectual properties for Principal Plus and Principal members via CPES IP Sharing Program
- Technology transfer made possible via special access to the center's multidisciplinary team of researchers, and resulting publications, presentations, and intellectual properties
- Continuing education opportunities via professional short courses offered at a significant discount
- Option to send engineers to work with CPES researchers on campus via the Industry Residence Program

The CPES industrial consortium offers the ideal forum for networking with leading-edge companies and top-notch researchers and provides the best mechanism to stay abreast of technological developments in power electronics.

CPES Membership Company Growth



Industry Membership Funding Growth



Membership Structure

Principal Plus Members

Annual Contribution $50,000

Principal Plus Members gain tangible benefits via research collaboration with CPES as a member of one of the mini-consortia on focused research—PMC (Power Management Consortium), HDI (High Density Integration), or WBG-HPCS (Wide Bandgap High-Power Converters & Systems). Companies interested in more than one focused research area may join another mini-consortium for an additional annual contribution of $50,000 each. In addition to all the benefits offered to Principal and Associate Members, Principal Plus Members have easy access to cutting-edge IP via the CPES IP Sharing Program, as well as interactive opportunities with CPES researchers via designated student contacts and mini-consortium reviews.

Principal Members

Annual Contribution $30,000

Principal Members are well positioned to influence and guide CPES as Industry Advisory Board (IAB) members. Principal Members also have cutting-edge IP advantage via automatic IP Sharing Program membership, in addition to all the benefits offered to Associate Members.

Associate Members

Annual Contribution $15,000

Associate Members gain a competitive edge, not only through easy access to CPES research results, researchers, and state-of-the-art facilities, but also opportunities for technical exchanges via the Industry Residence Program and continuing education via CPES short courses to stay abreast of new technologies. Companies participating in the Industry Residence Program must be actively engaged in collaborative research with the center in technical areas that are of mutual interest, to be determined jointly with CPES faculty host.

Affiliate Members

Annual In-Kind Donations Equal to or Less Than $15,000

Affiliate Members make in-kind hardware/software donations to CPES equivalent to or less than $15,000 per year. Their contributions must be relevant to CPES research. Membership participation at this level requires approval of the center director.

Intellectual Property Sharing Program

For 20 years, CPES's unique IP Sharing Program has transitioned cutting-edge advances from the laboratory into myriad products of the highest value to society. Envisioned and brought to reality by CPES Founder Fred C. Lee, the IP Sharing Program has numerous benefits for industry partners as outlined here.

Leverage Research Dollars

- Intellectual Property (IP) development and prosecution funded collectively by the industry consortium
- IP resulting from federally-funded research often available for IP Sharing

Included with Principal Plus and Principal Memberships

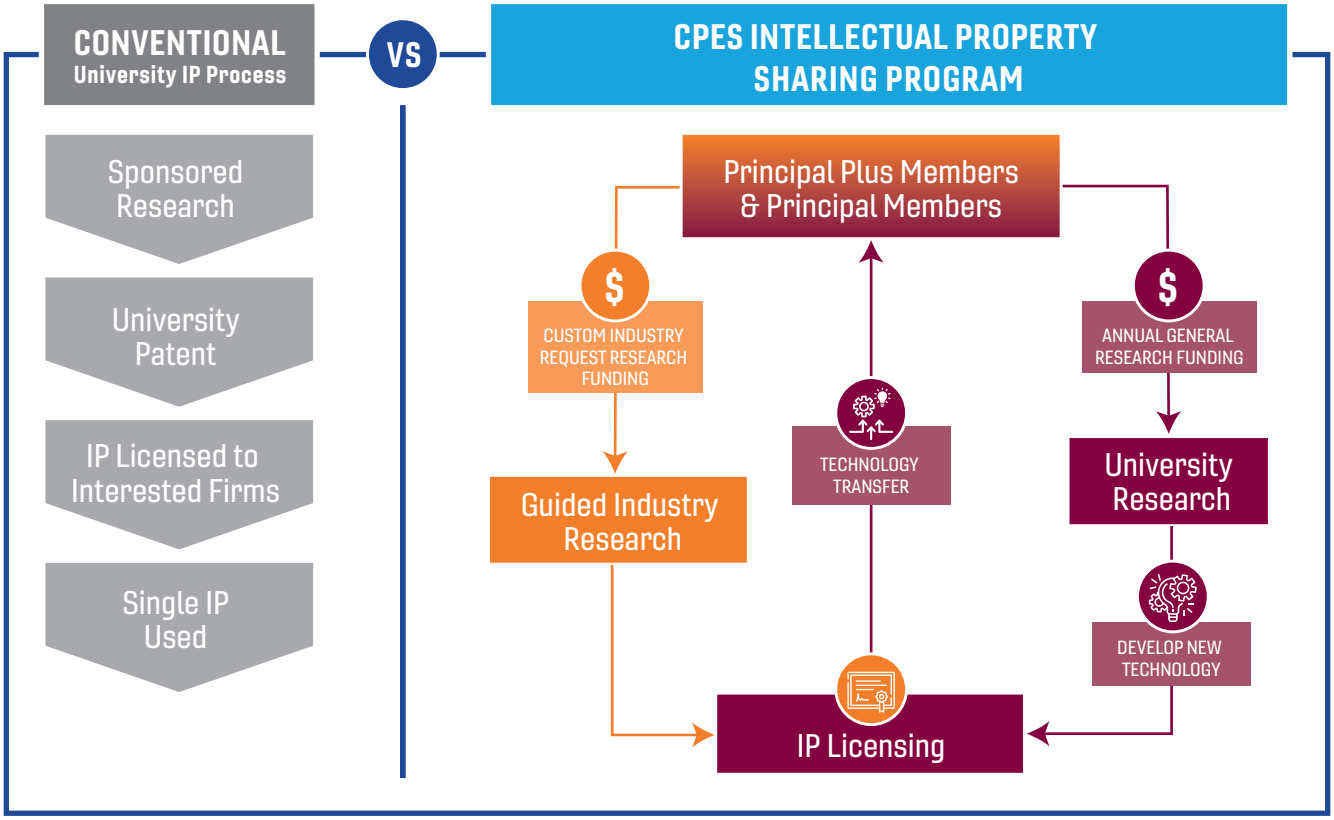
- Principal Plus Members have enhanced opportunity to guide research and future IP through the mini-consortia

Protection From Competitors

- Members are granted royalty-free, non-exclusive, non-transferable license

Active Role in Selecting Technology to Protect

- Members meet regularly with inventors to review and jointly decide which technologies to protect



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Jiangsu Wanbang Dehe New Energy Technology Co., Ltd.
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AcBel Polytech Inc.
Cummins Inc.
Fuji Electric Co., Ltd.
General Motors
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Johnson Controls Inc.
Kohler Company
Maxim Integrated
Northrop Grumman Corporation
NuVolta Technologies
Richtek Technology Corporation
Robert Bosch GmbH
Safran
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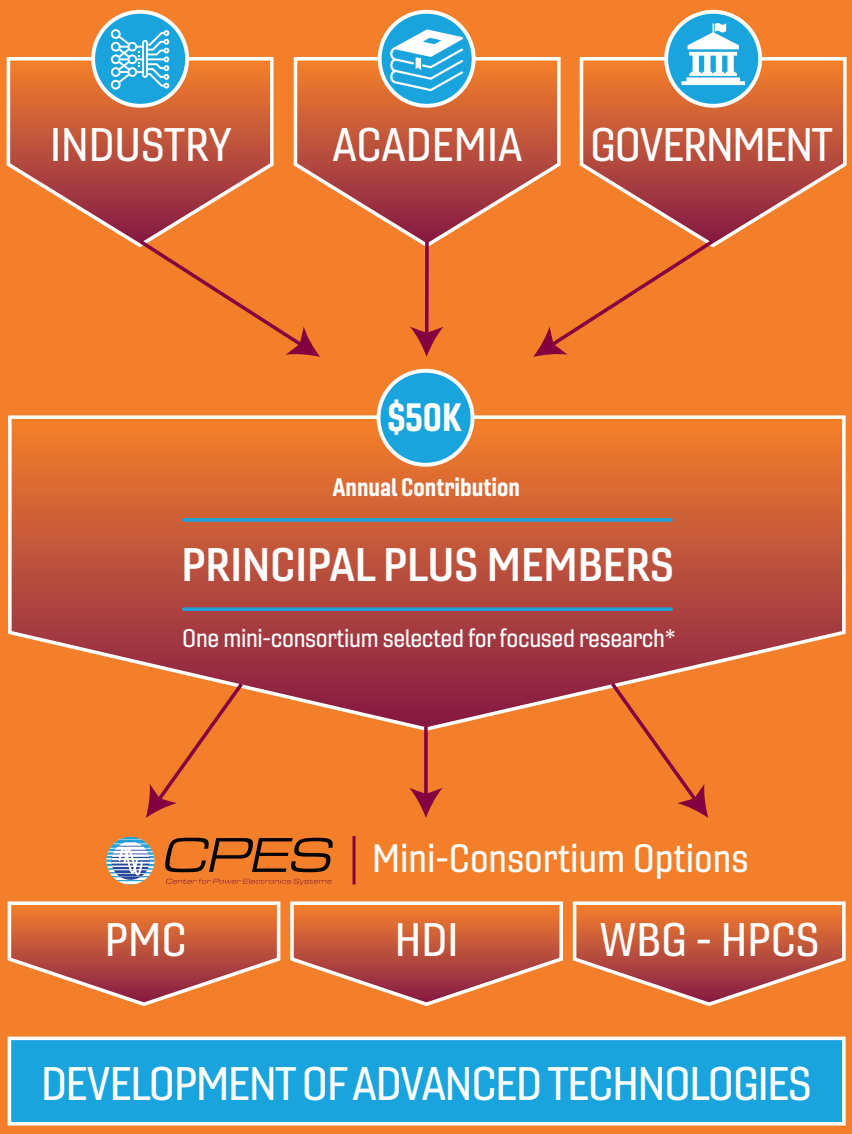
Sumitomo Electric Industries, Ltd.
Suzhou Inovance Technology Co., Ltd.
TBEA Xi'an Electric Technology Co., Ltd.
TDK-Lambda Corporation
Tesla Motors
Toyota Motor Corporation
United Silicon Carbide Inc.
Valeo

Affiliate Members

ANSYS Inc.
AT & S
Chicony Power Technology Co., Ltd.
Cissoid
Dowa Metaltech Co., Ltd.
Efficient Power Conversion
Egston Power Electronics GmbH
Electronic Concepts Inc.
Hitachi Metals
Mentor Graphics Corporation
Novel Crystal Technology
OPAL-RT Technologies
Plexim GmbH
Powersim Inc.
Silvaco
Simplis Technologies Inc.
Synopsys Inc.
Taiyo Yuden Co. Ltd.
Tektronix Inc.
Tokin Corporation
Transphorm Inc.
VPT Inc.

Mini-Consortium Program



*Companies interested in more than one focused research area may join another mini-consortium for an additional annual contribution of $50,000 each.

The CPES mini-consortium program provides a unique forum for creating synergy among industries and defining new research directions to meet future industry needs. The formation of the mini-consortium allows CPES to pool resources and focus on developing precompetitive technologies to address common challenges, and share the research results among mini-consortium members. Companies also benefit from enhanced opportunities to engage regularly and directly with CPES faculty and students through quarterly reviews.

Mini-consortium members are enrolled in CPES as Principal Plus Members, with annual contributions of $50,000. They gain tangible benefits via research collaboration with CPES as a member of one of the mini-consortia on focused research:

- PMC (Power Management Consortium)
- HDI (High Density Integration)
- WBG-HPCS (Wide Bandgap High Power Converters and Systems)

Companies interested in more than one focused research area may join another mini-consortium for an additional annual contribution of $50,000 each.

Power Management Consortium (PMC)

With ever-increasing current consumption and clock frequency, today's microprocessors are operating at very low voltage and continuously switching between the "sleep-mode" and "wake-up mode" up to tens of megahertz in order to conserve energy. This imposes a significant challenge to the power delivery and management and was perceived as a road block for further processor development.

In 1997, at the request of Intel, CPES established a voltage regulator module (VRM) mini-consortium to address the issue of power management for the next generation of Pentium processors. The CPES team developed a multi-phase voltage regulator (VR) module architecture and implementation and it was immediately adopted by industry. The scope of VRM research encompasses power delivery architecture, modularity and scalability, control and sensing, current sharing, integrated magnetics, advanced packaging, and integration. In these respects, over 30 U.S. patents were awarded. The developed power architecture is easily scalable to meet ever-increasing current consumption, clock rate, and stringent voltage regulation requirements. Today, every computer and server microprocessor in the world is powered with this multi-phase VR. These technologies have been further extended to high-performance graphical processors, AI, chipset, and memory devices, and used in all forms of mobile electronics, networks products, and telecommunications. The impacts are fundamental and span multiple industries worldwide.

The Power Management Consortium (PMC) is an outgrowth of the early VRM mini-consortium initiated in 1997, with a much expanded research scope and with a focus on developing precompetitive technologies for a wide range of applications. The current scope of research encompasses power architecture and management for computer and communication equipment, all forms of mobile devices, data centers, and network products, automotive electronics, EV charger, solid-state lighting, PV inverters, and industrial and consumer electronics. R&D emphasis includes such key issues as efficiency, power density, cost, power quality, EMI mitigation, and manufacturability.

Since its inception, the PMC program has been supported by more than 50 major global enterprises, and with wealth of knowledge generated, including over 75 U.S. patents, over 650 technical papers, and more than 80 Ph.D./M.S. students who are playing key leadership roles in various industry sectors.

With recent advances in wide-bandgap (WBG) power semiconductor devices, namely SiC and GaN, we have witnessed significant improvements in efficiency and power density while operating at an order of magnitude higher frequency than the current practice using silicon counterparts. With this dramatically increased operating frequency, current design practices are challenged. Design trade off previously inconceivable or deemed impractical can be realized not only with significant gain in efficiency and power density, but also drastic improvement of EMI/EMC, manufacturability, and cost.

This potential paradigm shift has been one of our major research activities. A number of demonstrations were developed to illustrate the performance improvements and ease of manufacturability, including:

- Point of Load 48/1.8 V @ 160 A voltage regulator with 95% efficiency and 1100 W/in^3 power density
- 1 kW 400/12 V unregulated LLC converter operating at 1 MHz with PCB-based integrated inductors and transformers while achieving 900 W/in^3 power density and 98% efficiency with much improved EMI performance
- 3 kW 400/48 V unregulated LLC at 500 kHz, with above 99% efficiency and 470 W/in^3 power density
- 3 kW 400/48 V regulated LLC at 1 MHz with above 98% efficiency and 700 W/in^3 power density
- 6.6 kW bidirectional on-board charger at 500 KHz for plug-in electric vehicles, using PCB-based integrated inductors and transformers while achieving 96% efficiency and 58 W/in^3 power density

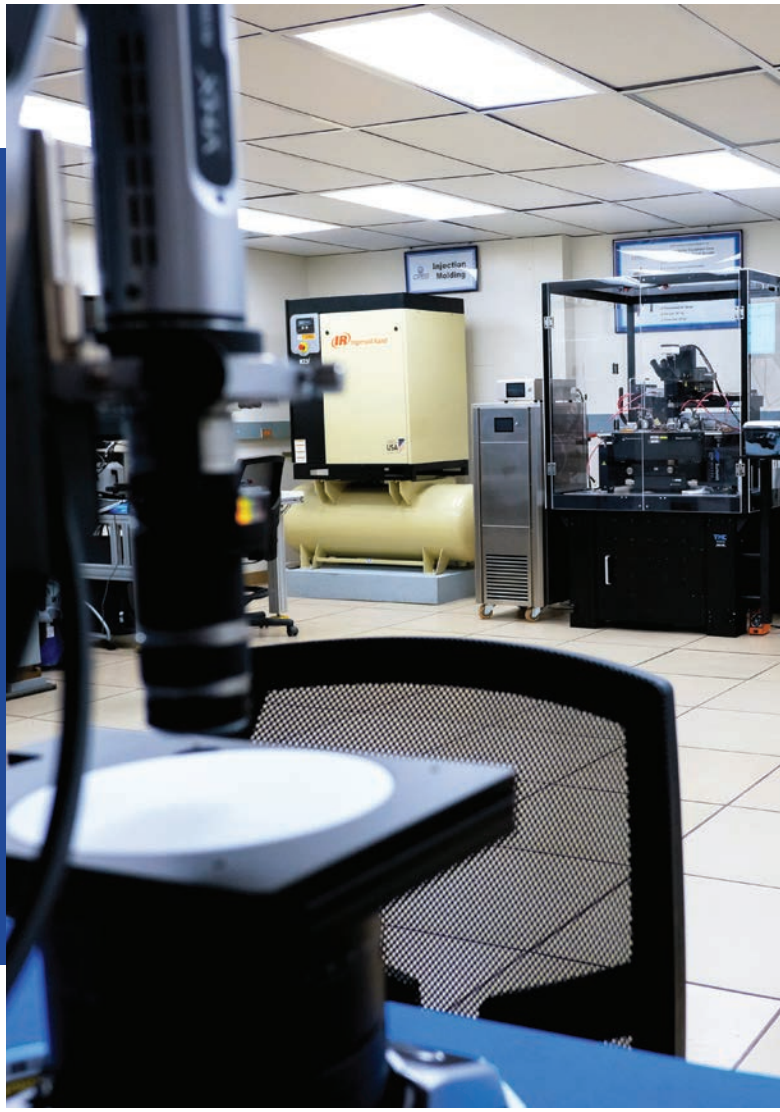
- 25 kW 3-phase inverter/rectifier module with PCB-based integrated inductors with 98.5% efficiency and 176 W/in^3 power density

With the recent recruitment of Professor Yuhao Zhang, PMC also established full-stack capabilities for power device research, including device design, simulation, cleanroom fabrication, small-scale process development, device characterization, as well as reliability and robustness studies. Current PMC device research includes the design and fabrication of novel GaN power devices beyond the commercial voltage range (15-650 V), development of p-channel GaN devices and "CMOS"-type GaN ICs, as well as the reliability and robustness studies of commercial GaN power devices under switching conditions and a variety of mission profiles. Below is some on-going device research.

- New GaN power transistors allow multi-megahertz switching at 5 V to 50 V
- New GaN lateral and vertical devices with a voltage class of 650 V to 3300 V with superior performance and low cost
- Single-event and repetitive avalanche and short-circuit robustness testing platform for WBG power devices

Work Scope of PMC

- High-performance VRM/POL converters with integrated magnetics
- Power architectures and management for servers and data center, PV system, EV charger/charging station
- High-frequency magnetics characterization and integration
- High-efficiency and high-power density power supplies using WBG power devices
- Wide-bandgap power device design and its reliability study
- Modeling and control
- Digital control
- EMI mitigation
- Solid-state lighting



Participants

PMC Members

PMC currently has 17 member companies. In 2020, NexGen Power Systems and OPPO joined as new members while Vertiv upgraded their membership to PMC from Principal level.

Analog Devices Inc.
CRRC Zhuzhou Institute Co., Ltd.
Delta Electronics Inc.
East China Research Institute of Microelectronics
Infineon Technologies AG
Innoscience (Zhuhai) Technology Co., Ltd.
Jiangsu Wanbang Dehe New Energy Technology Co., Ltd.
Lite-On Technology Corporation
Lockheed Martin Corporation
Murata Manufacturing Co., Ltd.
NexGen Power Systems
NXP Semiconductors N.V.
ON Semiconductor
OPPO
Panasonic Corporation
Powerland Technology Inc.
Silergy Corporation
Texas Instruments
Vertiv

Research Team

Faculty

Fred C. Lee
Qiang Li
Yuhao Zhang

Graduate Students

Xingyu Chen
Junjie Feng
Rimon Gadelrab
Yi-Hsun Hsieh
Zhengrong Huang
Virginia Li
Zheqing Li
Jingcun Liu
Xin Lou
Yunwei Ma
Ahmed Nabih
Pranav Prakash
Owen Ruan
Gibong Son
Tianlong Yuan
Chunyang Zhao
Feiyang Zhu

Visiting Scholars

Hieu Pham
Ming Xiao

Leveraged with Government Funding from

National Science Foundation (NSF)
PowerAmerica
U.S. Department of Energy (DOE)

High-Density Integration (HDI)

HDI was created in 2011 as a mechanism for CPES and industry members to address emerging and long-term challenges in power electronic integration. While it is supported primarily by CPES membership, it also leverages sponsored research with major industries such as Delta, Dowa, GE, GM, Group Safran, Lockheed Martin, MKS, Nissan, Raytheon, Rolls-Royce, TI, Toyota, and UTRC, as well as with government agencies including the U.S. Department of Energy (ARPA-E), U.S. Department of Defense (DARPA, ONR, Army and Air Force), and National Science Foundation. The tradeoffs among reliability, efficiency, cost, electromagnetic compatibility, power density, and speed are explored as new materials, components, circuits, and applications emerge.

The commercialization of wide-bandgap semiconductor devices such as silicon carbide (SiC) and gallium nitride (GaN) has shifted switching frequency beyond tens of megahertz, power rating beyond megawatts, and junction temperature beyond 250° C. Ancillaries, characterization metrology, modeling method, packaging process, and manufacturing paradigm need to be transformed.

Unique high-temperature packaging technology is an example of CPES fulfillment of these critical needs to the future power electronics industry. HDI developed die-attach materials that can be processed at low temperatures, yet are reliable at the temperature of the wide-bandgap junction. Processes were developed to encapsulate ultra-thin planar packages with a polymer having high glass transition temperature and dielectric strength.

Magnetic materials with low core loss-density were synthesized from magnetic metals for additive manufacturing of high-frequency magnetic components. Inductors were fabricated from heterogeneous magnetic composites to shape the EMI spectrum. Over-molding magnetic materials have been synthesized for integrating energy storage and protection functions.

Techniques to decouple the noise loops have been identified to enable high dv/dt commutation in wide-bandgap switches. Design methodologies have been documented for high-temperature capacitors, power buses, protection, sensing, digital control, etc. New breeds of gate drivers, sensors, active filters, and passive filters have been demonstrated in a wide range of products, from power adapters to power electronic building blocks. Significant improvements in power density, efficiency, and signal integrity are expected thanks to the adoption of technological advances. HDI tasks are scoped to advance wide-bandgap systems, magnetic components, and module integration.

This current scope of work includes the following topics:

Wide-Bandgap Systems

- Reliability study of failure mechanisms of GaN and SiC MOSFETs
- High-voltage high-temperature gallium oxide diode
- Characterization of wide-bandgap semiconductor switches up to highest voltage and temperature
- Short circuit protection design for paralleled GaN module high-density laptop adaptor
- High-frequency, low loss soft-switched converters
- Insulation coordination study for high-voltage high-power density converter design
- Wireless charging

Magnetic Components

- Swinging and coupled inductors with heterogeneous magnetic cores
- Magnetic structures with high-energy density
- Over-molding of encapsulating magnetics
- Low profile magnetic substrate

- Weakly coupled coils with a low stray field for wireless power
- Integration of and field interaction in common-mode and differential-mode filters
- Integrated multi-phase inductor for a voltage regulator for small portables
- PCB-integrated magnetics for high-efficiency, high-density front-end power supply
- Characterization of high-power inductors and materials
- High-frequency magnetic integration

Module Integration

- Large-area substrate-to-substrate bonding by silver sintering
- Reliability evaluation of module interconnects
- Current sensor integrated with SiC MOSFET module
- High-voltage SiC module packaging
- Integration of magnetic dice into the power module
- Electromagnetic interference (EMI)

Work Scope

- Wide-bandgap devices
- Material and component characterization
- Active module integration
- High-frequency magnetic integration
- Converter integration
- Wide power range (10 W – 100 kW)
- High frequency (100 kHz – 10 MHz)
- High temperature ≥ 250° C

Participants

HDI Members

Delta Electronics Inc.
Ford Motor Company
GE Global Research
GE Aviation
Hyundai Mobis
Komatsu Ltd.
Lockheed Martin Corporation
Moog Inc.
Nissan Motor Co., Ltd.
Texas Instruments
VisIC Technologies
Würth Elektronik

Research Team

Faculty

Dushan Boroyevich
Rolando Burgos
Christina DiMarino
Dong Dong
Mona Ghassemi
Fred C. Lee
Qiang Li
Guo-Quan Lu
Khai Ngo
Yuhao Zhang

Research Faculty

Igor Cvetkovic
Jun Wang

Graduate Students

Chao Ding
Jack Knoll
Joseph Kozak
Bo Li
Shengchang Lu
Ahmed Nabih
Tam Nguyen
Mina Shawky
Joshua Stewart
Maryam Tousi
Boyan Wang
Le Wang
Shuo Wang
Yue Xu
Lujie Zhang
Ruizhe Zhang
Tianyu Zhao

Visiting Scholars

Cyril Buttay
Takashi Hirota
Toshihiro Kai
Sang Min Kim

Leveraged with Gifts from

ABB Inc.
LG Electronics
Raytheon Technologies

Leveraged with Government Funding from

Advanced Research Project Agency – Energy (ARPA-E)
Office of Naval Research (ONR)
PowerAmerica
U.S. Department of Energy (DOE)

Wide-Bandgap High-Power Converters and Systems (WBG-HPCS)

Over its 10 years of operations, this CPES mini-consortium program has provided a unique, open, and collaborative forum for the power industry to explore new and emerging power conversion technologies and applications, seeking to meet what are the ever-increasing energy demands of our modern society: WBG-HPCS looks at everything from power semiconductors, to gate drivers and ancillary circuitry, to converters, all the way to the impact that they have on electrical power systems.

As a mini-consortium, WBG-HPCS allows CPES to pool various resources seeking to develop the above pre-competitive technology. CPES is then able to address common industry challenges, and effectively share research results among its members. The program is strongly leveraged by CPES's vast expertise in WBG-based power conversion and its in-depth knowledge of electronic power systems, which it has accrued over the past 35 years working closely with the space, transportation, and IT industries. As a result, the WBG-HPCS mini-consortium has expanded its research scope successfully into high-power medium-voltage (MV) applications for grid, industrial, and transportation applications.

CPES has continued to support research activities within the WBG-HPCS mini-consortium by securing funding—at the basic research level—from several government agencies. The most prominent ones include the Office of Naval Research (ONR), the U.S. Department of Energy (DOE), DARPA, PowerAmerica, ARPA-E, and NASA. These agencies have been instrumental in developing key enabling technology presently used in WBG-based, high-power electronics applications, and as such represent ideal partners for CPES. Their collaboration over the past years has generated invaluable synergy within CPES aiding in the pursuit of the mini-consortium goals. From a funding standpoint, CPES has been able to effectively quadruple the research activity in this area thanks to their support, ultimately quadrupling too the results and technological advancements that are shared with its members.

The WBG-HPCS present research thrusts are the following:

High-Power WBG-Based Power Converters

- High-frequency control of modular multilevel converters in ac-dc and dc-dc mode

- Design of SiC-based modular multilevel converters with 1.7 kV, 3.3 kV, and 10 kV devices (package, gate-drive, PEBB, converter, system)

WBG-Based Power Electronics Technology

- Characterization of MV SiC and LV GaN devices
- Development of EMI containment and suppression strategies for power converters, modular converters, and electronic systems
- Formulation of electric-field constrained design methodologies for power components subject to high-frequency excitation and fast dv/dt transients
- Design of electric-field constrained power converters and components for high-altitude (30,000 – 60,000 ft.) aerospace applications
- Development of enhanced gate drivers, auxiliary power supplies, and sensors for harsh dv/dt and EMI environments, and MV and high-altitude applications with advanced control capabilities
- Development of PCB-based medium-voltage ac-dc capacitor arrays for ultra-high-power density applications

Stability and Dynamic Interactions

- Analysis of dynamic interactions between multiple STATCOM operating in proximity in HV transmission systems
- Stability assessment and interactions of utility-scale PV inverters in medium-voltage distribution systems
- Stability analysis in three-phase unbalanced systems and single-phase distribution systems
- Assessment of electromechanical dynamics and stability in generator-rectifier powertrains
- Grid-forming control schemes for grid-tied inverters
- SiC-based impedance measurement unit (IMU) for ac-dc LV and MV distributions systems
- Self-impedance-measurement-based stability monitoring in grid-tied inverters

Renewable Energy Integration

- Design of high-efficiency SiC-based grid-tied PV inverters for MV and LV applications
- Design of high-efficiency GaN-based grid-tied inverters for residential PV applications
- Dynamic impact of PV inverters in MV distribution systems
- Grid-forming controls dynamic impact in MV distribution systems under grid-connected and islanded conditions
- Protection system operation under high penetration of PV inverters in MV distribution grid

Work Scope

- High-power WBG-based power converters
- WBG-based power electronics technology
- Stability and dynamic interactions in power converter systems
- Renewable energy integration

Participants

WBG-HPCS Members

ABB Inc.
Aurora Flight Sciences
Delta Electronics
EnerSys
GE Grid Solutions
Rockwell Automation
Siemens Corporate Technology
TMEIC Corporation

Research Team

Faculty

Dushan Boroyevich
Rolando Burgos
Dong Dong
Fred C. Lee
Qiang Li

Research Faculty

Igor Cvetkovic
Bo Wen

Graduate Students

Victoria Baker
Yuliang Cao
Yugal Gupta
Nidhi Haryani
Yi-Hsun Hsieh
Jiewen Hu
Qian Li
Zheqing Li
Qing Lin
Xiang Lin
Jian Liu
Slavko Mocevic
Minh Ngo
Lakshmi Ravi
Yu Rong
Rebecca Rye
He Song
Matthias Spieler
Joshua Stewart
Keyao Sun
Ye Tang
Ning Yan
Jianghui Yu
Biqi Wang

Visiting Scholars

Boran Fan
Takahide Tanaka
Sizhan Zhou

Leveraged with Gifts from

ABB Inc.
Dominion Energy
Raytheon Technologies

Leveraged with Government Funding from

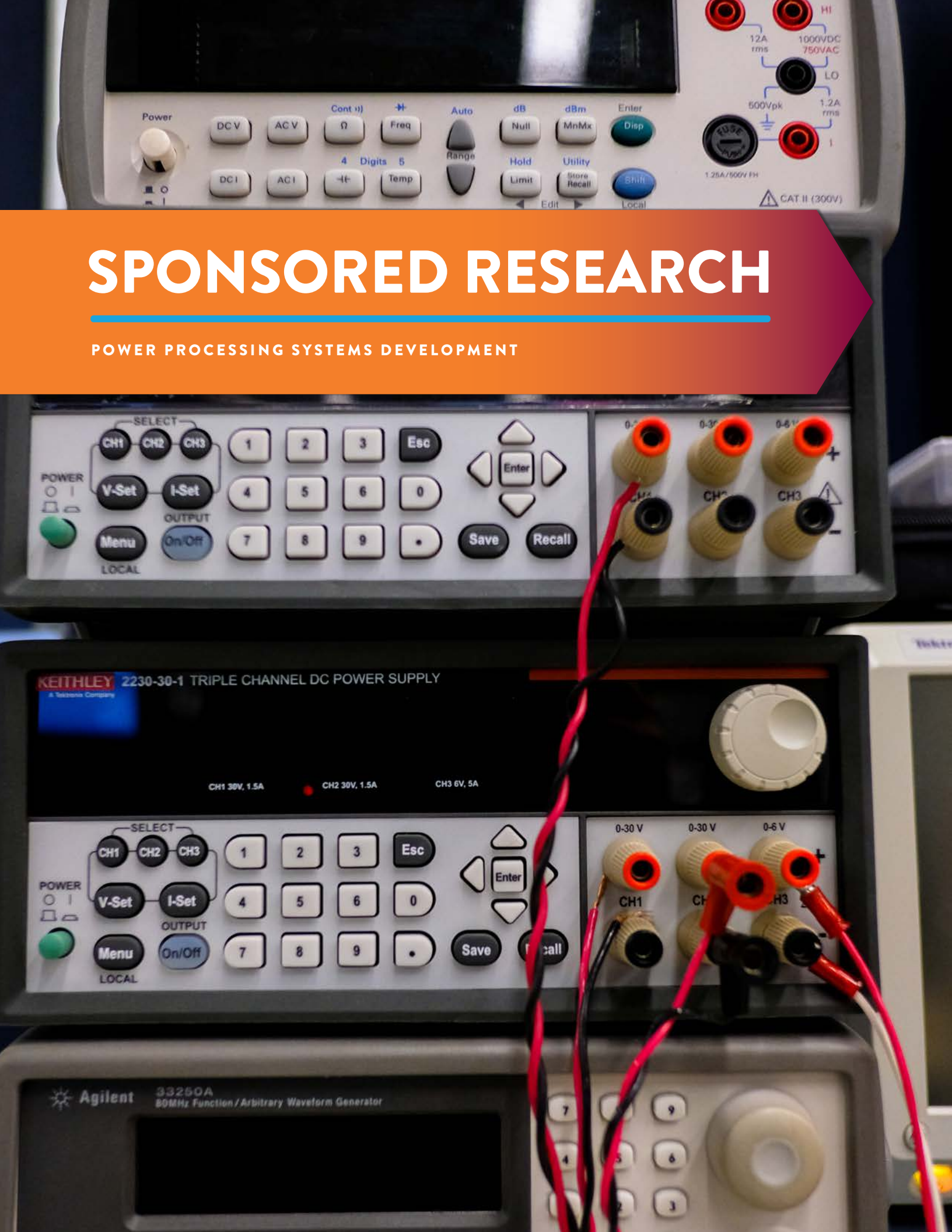
Advanced Research Project Agency – Energy (ARPA-E)

National Aeronautics and Space Administration (NASA)

Office of Naval Research (ONR)

PowerAmerica

U.S. Department of Energy (DOE)



SPONSORED RESEARCH

POWER PROCESSING SYSTEMS DEVELOPMENT

In its effort to develop power processing systems to take electricity to the next step, CPES has cultivated research expertise encompassing six technology areas:

1) Power conversion technologies and architectures
2) Power electronics components
3) Modeling and control
4) EMI and power quality
5) High-density integration
6) High-power high-voltage converters

These technology areas target applications that include:

1) Power management for information and communications technology
2) Point-of-load conversion for power supplies
3) Vehicular power converter systems
4) Sustainable and distributed electronic energy systems

In 2020, CPES-sponsored research totaled approximately $3.5 million. The following abstracts provide a quick insight to the current research efforts.

ABB Fellowship

This fellowship program was originally established to investigate the capabilities of wide-bandgap power semiconductors. Although the first year concentrated on the evaluation of gate-driver circuitry for silicon carbide (SiC) 1.7 kV and 10 kV MOSFET devices, the following years were fully devoted to the evaluation and assessment of the high-power handling capability of gallium nitride (GaN) power semiconductors. The effort concluded in 2020 with the development of a packaging solution for the latest generation of 10 mΩ GaN 650 V dies from GaN Systems, for which a ceramic substrate module with PCB interposer was built and successfully demonstrated in both single and half-bridge module configurations. A parallel effort explored the impact of the dynamic RDS(on) effect on the design of GaN-based power converters. In 2020, the fellowship direction returned once again to SiC devices, and specifically to the evaluation of SiC MOSFET devices as a viable power semiconductor for solid-state circuit breaker (SSCB) applications. Specifically, the work conducted developed a design methodology for SiC-MOSFET-based SSCB, focusing on the design and breaking capabilities of MOSFETs and the companion MOV devices used. While the current rating capability was expanded by connecting devices in parallel, the effort to investigate the series-connection of SiC devices was initiated seeking to expand the operating capacity of this technology.

Dominion Energy Fellowship

This fellowship program was originally established to investigate the dynamic interactions that can arise when multiple static synchronous compensator (STATCOM) units operate in proximity to transmission systems (200–500 kV ac lines). The results obtained demonstrated a strong dependence on the ac voltage and current controllers of the STATCOMs, which were shown to induce voltage oscillations with potentially damaging effects in the case proper precautions are not taken. A CPES-developed impedance measurement unit (IMU) was used to validate all theoretical findings using two STATCOM prototypes and a synchronous machine to emulate the power grid.

Extending the findings on the STATCOMs, the fellowship continued exploring the impact that utility-scale photovoltaic (PV) inverters have in medium-voltage (MV) distribution grids; especially in the case that these units are complying with the new voltage and frequency compensation requirements of the IEEE Std 1547. The results obtained showed the severe impact on dynamic interactions and stability that the various control modes dictated in this standard can have, specifically showing how the preferred control scheme from a static standpoint is the most challenging from a dynamic standpoint. This phenomenon was shown to effectively limit the amount of active power that can be generated when operating in these control modes. Similar effects were observed when operating multiple PV inverters within an MV distribution grid, where again the same IEEE 1547 compliant control schemes were shown to easily induce interactions among the inverter units.

In 2019, the fellowship work concentrated on exploring the stability in unbalanced MV grids, where a new stability assessment theory and approach were developed and validated experimentally. This new approach is based on the use of multiple synchronous d-q frames attached to the individual phases in a system, allowing for expanded impedances to be defined in order to create a fictitious quiescent operating point. The latter can then be readily used to conduct stability analysis using conventional multivariable linear control theory, overcoming a limitation of the conventional impedance-based stability assessment approach and a technical and theoretical challenge that CPES had pursued for more than 15 years.

Over the last year, the fellowship continued expanding the breadth of the analysis conducted to determine the impact that PV inverters can have on the protection coordination of distribution grids. Specifically, on identifying the increase or decrease of short-circuit currents throughout the distribution grid when increasing amounts and distributed PV inverter generation is present in the system. Additionally, the fellowship is targeting the quantification of the advantages and disadvantages that grid-forming controls of PV inverters can have on the protection system, as opposed to the effect of traditional grid-following PV inverter controls.

Raytheon Technologies Research Center Fellowship

This fellowship program was originally established by United Technologies Research Center (UTRC), now Raytheon Technologies Research Center (RTRC), to develop multi-objective design optimization methodologies for power electronics converters, taking into consideration parametric and model-form uncertainties. The design techniques developed have built on CPES's previous efforts designing high-power density and extreme efficiency power converters. The quantification of these uncertainties has been essential to achieve a robust optimum design accounting for the errors introduced naturally by parametric tolerances and by the inherent accuracy of the numerous electromagnetic and mechanical models used in the optimization process. Results obtained on a three-phase Vienna-type rectifier have been successfully used to validate the theoretical findings.

In its second phase, the fellowship sponsored by RTRC sought to evaluate and explore the possibility of developing 1.2 kV SiC MOSFET power modules for aerospace applications operating in ambient temperature conditions of up to 250° C. In 2019 CPES investigated several encapsulant materials and opted to evaluate alternative glass formulations seeking to use it as module encapsulant up to temperatures of 300° C. Some of the key results obtained indicated the persistent cracking of the encapsulant and its interface with the ceramic substrate that degraded its insulation rating leading to an increasingly reduced partial discharge inception voltage. A parallel effort investigated the capability of SiC MOSFET to operate at temperatures of up to 300° C. These semiconductors were characterized statically and dynamically, effectively showing a good performance; however, high temperature reverse bias and gate-bias reliability tests showed that these devices could not operate at 250° C beyond 100 hrs. New materials and semiconductors devices may hence be required to operate at high temperatures reaching 300° C.

In its third phase, the fellowship sponsored by RTRC has sought to develop ultra-high-power density, extreme efficiency, three-phase inverters for aerospace applications, where its main effort has been in exploring alternative topological solutions to maximize the figures of merit in question using either GaN or SiC power semiconductors for a 1 kV fed dc-ac three-phase inverter for a high-speed motor rated at 50 kW. The plan moving forward is to select the best performer topology and demonstrate the prototype that is targeting a power density of 40 kW/l and an efficiency greater than 99%.

Design, Evaluation, and Demonstration of an Embedded SiC Power Module for Electric Vehicle On-Board Charger

Sponsor: AT & S

May 2020 — December 2022

Embedding power semiconductors using PCB manufacturing processes can enable automated, flexible, low-cost, high-volume production of power electronic converters, while offering improved performance and reduced system size and weight. This is especially desirable for the electric vehicle industry due to the increasing needs

for greater manufacturing throughput, improved cost competitiveness, and better performance and power density. This work aims to design and evaluate the first fully-PCB-integrated 22 kW power converters with embedded 1.2 kV silicon carbide (SiC) MOSFETs, magnetics with PCB winding, and integrated gate driver, sensors, and control. The developed PCB-integrated converters will be used to demonstrate an 800 V, 22 kW on-board charger (OBC) system. The electrical, thermal, and thermomechanical performance of the PCB-embedded SiC half-bridge will first be evaluated using an ac-dc converter testbed, thermal impedance measurement platform, and power cycling system. The knowledge gained from the PCB-embedded SiC half-bridge evaluation will then inform the design and development of high-density PCB-integrated converters with embedded SiC MOSFETs for a 22 kW OBC application.

Evaluation of Electromagnetic Interference Mitigation Strategies for High-Voltage Wide-Bandgap Power Modules

Sponsor: Army Research Laboratory

September 2020 — September 2021

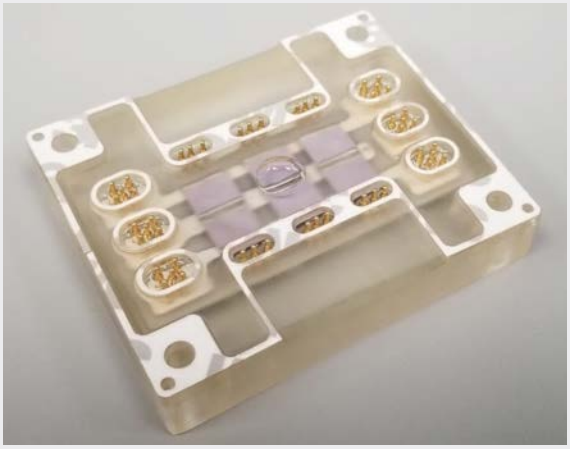
Wide-bandgap (WBG) power devices with voltage ratings exceeding 10 kV have the potential to revolutionize medium- and high-voltage systems due to their high operating voltage and high-speed switching. However, the benefits of these unique switches are also their main barriers to adoption. In particular, the high switching speed can cause significant electromagnetic interference (EMI), voltage overshoot, and ringing. While it has been shown that the latter can be mitigated by low-inductance packaging, the former remains a major challenge. Current EMI mitigation solutions involve adding common-mode (CM) chokes and EMI filters at the converter and system levels. To reduce these external filtering requirements, CPES has demonstrated a 10 kV silicon carbide (SiC) power module with an integrated screen, which reduces the CM current that is generated by the fast voltage transients, while simultaneously increasing the partial discharge inception voltage by more than 50%. Through systematic experimentation, a better understanding of how to design packages to mitigate EMI effects on the system can be achieved. Techniques that will be evaluated in this work include: 1) balancing the positive and negative bus parasitic capacitances and inductances, and 2) integrated screening. Other EMI mitigation techniques will also be reviewed, and strategies for implementing promising techniques at the package level will be explored. The knowledge that will be gained from this work will contribute to new design criteria for low-EMI WBG packages. Reducing the negative impacts of high-speed switching on the system is essential to mitigating the risk of high-voltage WBG devices without sacrificing performance.

Prototyping and Evaluation of High-Speed 10 kV SiC MOSFET Power Modules with High Scalability and System-Integration Solutions

Sponsor: U.S. Department of Energy through PowerAmerica

January 2020 – January 2021

Wide-bandgap (WBG) power devices with voltage ratings exceeding 10 kV have the potential to revolutionize medium- and high-voltage systems due to their high-speed switching and lower on-state losses. However, present power module packages are limiting the performance of these unique switches. A high-density package for 10 kV silicon carbide (SiC) power MOSFETs has been proposed that achieves low and balanced parasitic inductances, resulting in a fast switching speed of 140 V/ns with



10 kV, 100 mΩ SiC MOSFET module with dimensions of 80 x 70 x 15 mm.

negligible ringing and voltage overshoot. The objective of this work is to evaluate the scalability, system integration, and reliability of the proposed 10 kV SiC power module. Power modules with multiple 10 kV die in parallel will be prototyped and tested to evaluate the current scalability of the proposed design. A compact system interfacing solution between the module and the gate driver and bus bar that enables high-density, 10 kV-SiC-based power converters will be prototyped and undergo partial discharge testing. Accelerated testing will be employed to understand the failure mechanisms of the proposed 10 kV power module. Understanding these failure mechanisms will enable improved designs for use in high-reliability applications.

Commonwealth Cyber Initiative (CCI) SWVA Node Research Funding

Sponsor: Commonwealth Cyber Initiative

July 2019 – June 2021

In an effort to support positioning Virginia as a global center of excellence at the intersection of security, autonomous systems, and data, CPES started a study on deployment of 5G network within electronic power systems that can provide advanced communication capabilities and enhance operation of electrical systems in nanogrids and microgrids. Special emphasis will be put on real-time clock synchronization between system nodes at a microsecond accuracy, enabling network transfer of time-stamped, addressed variables with a millisecond latency. CPES's initial focus has been use of a White Rabbit precision time protocol (PTP) over 5G network to synchronize clocks in the all-power-electronics systems that could potentially eliminate phase-locked loops in the converter control. This concept also has promising advantages for protection coordination, which will be explored later in the project.

Development of the iPEBB 1000, a 1.7 kV SiC MOSFET-based Integrated Power Electronics Building Block

Sponsor: Office of Naval Research

January 2019 – December 2020

The power processing capabilities of 1.7 kV silicon carbide (SiC) high-current devices have been successfully demonstrated under the Office of Naval Research (ONR) SiC-PEBB program and the Electric Ship Research and Development Consortium (ESRDC). Embodied by the PEBB 1000 developed at the Center for Power Electronics Systems (CPES), Virginia Tech, this unit rated at 100 kW, 1 kV and 100 kHz, demonstrated a power density of 5 kW/l and has become an extremely valuable source of information regarding the design and operation of SiC-based power converters and systems. Propelling this concept for its adoption in future Navy ships, this project proposes to develop a fully integrated PEBB module designed for automated manufacturing, namely iPEBB 1000, featuring an ac-dc-dc circuit topology with high-frequency galvanic isolation for maximum power flexibility, and a 5 times higher power density (> 25 kW/l) attained by adopting an integrated metal substrate as host platform to all SiC dies and electromagnetic components, using embedded gate-drivers and sensors, having a multilayer structure integrating the cooling system baseplate, the electromagnetic interference (EMI) shield, and multi-turn planar windings for all magnetic components. Further, the iPEBB 1000 will be designed with fully controlled internal electric fields, achieving a 0 V enclosure potential, which will enhance its operational safety by allowing the direct handling and servicing of the unit.

Electric Ship Research and Development Consortium (ESRDC) Undergraduate Student Support

Sponsor: Office of Naval Research

January 2020 – April 2022

ONR has provided funding to engage undergraduate students in the significant ESRDC effort at CPES/VT. This support will make a great impact on undergraduate education providing immensely valuable hands-on training with research currently ongoing at CPES/VT under the ESRDC program. Undergraduate students selected to receive these funds will work directly with top graduate students and faculty in multiple research, hardware, and software development tasks.

Electric Ship Research and Development Consortium

Sponsor: Office of Naval Research

August 2016 – December 2020

CPES will continue supporting the Office of Naval Research (ONR) mission by participating as a member of the Electric Ship Research and Development Consortium (ESRDC), a multi-university consortium led by Florida State University. Within this framework, CPES is working on the demonstration of PEBB 1000 (power electronics building block)-based power converters and systems, for which it has developed an updated version of the PEBB 1000 unit built with 1.7 kV SiC MOSFET devices. It will continue working on the impedance measurement unit (IMU) previously developed for ONR using 10 kV SiC MOSFET devices and a multi-megawatt converter capable of operating from 4,160 V ac and 6,000 V dc networks, to measure the terminal impedances at interfaces of interest, with the purpose of assessing the stability conditions of the electrical system. The focus of this work will be to improve its electromagnetic compatibility (EMC), necessary to operate with the fast-switching 10 kV devices in place. Lastly, CPES will support the electric ship design, modeling, and simulation effort within ESRDC by integrating the modeling of power electronics systems, taking into consideration parametric and model-form uncertainties during the process, with which improved and optimum designs will become feasible using the PEBB models developed.

Resiliency Enhancement of Cyber-Microgrids and Microgrid Building Blocks

Sponsor: U.S. Department of Energy, Sub-Awardee of Pacific Northwest National Laboratory

April 2020 – March 2021

In close collaboration with the Power and Energy Center (PEC) at VT, CPES has been conducting a conceptual study of a Microgrid Building Block (MBB) – a bidirectional power electronics converter serving as a main tie between a microgrid and a utility. The microgrid example resembling the existing Virginia Tech Electric Service Power Plant is modeled and simulated to demonstrate the functionality enhancement achieved with the addition of a bidirectional power electronics converter named a microgrid building block - cyber-physical system, which features standardized power, control, and communication interfaces. This concept significantly simplifies (and standardizes) microgrid nesting, while providing dynamic decoupling from the utility. It further enables multiple microgrids to operate independently and coordinate operation even when the main grid is not present, thus enhancing the resiliency. Not only that MBB-interfaced microgrid can operate in an islanded mode for a given time determined by available power from the local energy generation and storage, but it also brings an advanced protection, black-start capability, fast resynchronization, low-voltage ride-through, and a sub-millisecond response functionality. Additionally, the concept of a Microgrid Building Block is important toward modularization of microgrids for wide deployment in the power grid. The VT team involved in this project will also study a broader set of cyber system events and their impact on the resiliency of the microgrid system.

High-Efficiency Multiport Power Conversion for an All-Electric Transportation Refrigeration Unit

Sponsor: U.S. Department of Energy through PowerAmerica

July 2019 – June 2020

Partnered with UTRC, CPES developed a high-power density (> 100 W/in^3) and high-efficiency (> 98.8%) 20 kW bidirectional onboard dc-dc isolated converter for battery charging and bus-interface applications using SiC and GaN power semiconductors. The operating frequency is 500 kHz in order to minimize the isolation transformer. The project will adopt a new circuit topology using partial power processing to reduce the total device kVA rating and improve the efficiency. The solution adopted in the project will also provide a fast and precise current and voltage regulation for pulse power applications.

The solution is considered an advanced technology insertion for next-generation battery chargers and bus-tie converter/breaker systems for future hybrid electric propulsion system. The CLLC-type bidirectional resonant converter will be adopted to achieve zero voltage switching (ZVS) throughout the complete operating range.

High-Density High-Altitude High-Voltage High-Speed Motor Control Unit (MCU) for Aviation Electric Propulsion

Sponsor: Airbus

July 2020 – December 2023

Airbus, one of the leading airspace and defense solution providers, partnered with CPES to investigate power conversion solutions for high-altitude, liquid-cooled high-speed motor control unit (MCU) systems. The goal is to attain high power density and high efficiency by profiting from new advanced power conversion and integration technologies in 200 kW applications.

Low-Cost Rare-Earth-Free Electric Drivetrain Enabled by Novel Permanent Magnets, Inverter, Integrated Design and Advanced Thermal Management

Sponsor: U.S. Department of Energy, Sub-awardee of Marquette University

October 2020 – December 2023

To achieve significant EV market penetration, e.g., 10 percent by 2025 and 35 percent by 2040, electric propulsion drive system cost and size will need to be reduced even further in addition to continued reduction in energy storage costs. This will in turn allow for easier integration of electric traction drive systems and favorable economics, resulting in a greater number of both passenger and light truck EVs.

Using GM's commercial Bolt™ light-weight EV IGBT-based traction drive system as the benchmark and demonstration platform, this project seeks to demonstrate a liquid-cooled, 200 kW, three-phase, highly integrated, full SiC high-speed electric propulsion drive, with 800 V operating dc-voltage, and a minimum of 20 kHz switching-frequency. The proposed solution will adopt the heavy-duty bus-bar embedded printed-circuit board (PCB) with integrated digital gate-driver, embedded current sensing, and PCB EMI filters solution to significantly reduce the OEM component count, which simplifies the mechanical structure and assembly process, as well as leverage low-cost electronics components. The power density target is 30 kW/L, almost twice the number of the 2025 U.S. Department of Energy target, and the peak power efficiency target is >98.5%. The cost savings are driven by overall mechanical and integration platform cost reduction thanks to high power density, hydraulic system and heat-exchanger reduction due to high efficiency, more automated assembly and component savings by highly-integrated multi-functional heavy copper PCB bus solution.

Modeling and Design of Solid-State Circuit Breaker

Sponsor: Naval Postgraduate School

September 2020 – September 2022

CPES will investigate the design trade-off of the energy dissipation circuit (EDC) used for a modular bi-directional solid-state based circuit breaker. The work includes survey and comparison of several EDC configurations in terms of density and voltage clamping profile control, reliability and scalability as well as modeling and design of critical EDC components like metal oxide varistor (MOV).

Modeling, Analysis and Simulation of Large-Scale Power Electronics-Based Power Grids

Sponsor: Oak Ridge National Laboratory

March 2020 – February 2021

Oak Ridge National Lab is partnering with the Center for Power Electronics Systems (CPES) to investigate system modeling and simulation and stability analysis of a new power electronics-based power system architecture, namely resilient all power electronics grid (APEG). The goal of the program is to explore a new modeling and simulation approach, which can provide significantly better simulation speed and accuracy than state-of-the-art EMT-based simulation software used in the power system community.

SiC Three-Level Hybrid Modular Multilevel Converter (THMMC) for Medium-Voltage Power Conversion Applications

Sponsor: National Science Foundation

September 2020 – August 2023

Accessing renewable energy and energy storage from the grid; e.g., solar, wind, and batteries, inevitably requires high-efficiency solid-state power conversion solutions. The industry is moving toward medium voltage (MV)

solutions, which can directly access the MV grid, to reduce bulky transformers, cables and cost/kVA of the converters. First published in 2003, the modular multilevel converter (MMC) technology immediately gained in popularity and became a de-facto benchmark system in MV to HV voltage-source converters (VSC). However, MMC still has many limitations. This work explores a new family of modular-oriented MV multi-level converters, namely a hybrid modular multilevel converters (HMMC). The proposed concept leads to important topology variations. For instance, the diode-based HMMC (DHMMC) rectifier provides a significant cost and total system size savings and efficiency improvement. SiC devices can be used in the proposed solutions to synthesize high-fidelity ac output. This NSF funding will support the PIs to perform detailed fundamental research on this family of solutions and to develop a set of fundamental modeling, control, and design solutions, paving the path for industry adoption as well as train students in medium-voltage power electronics and modular multilevel converter systems.

Ultra-Efficient Intelligent MVDC Hybrid Circuit Breaker

Sponsor: Department of Energy, sub-awardee of Eaton Corporation

October 2019 – September 2022

DC power provides numerous benefits at low (< 1kV), medium (1 kV – 100 kV), and high (> 100 kV) voltage levels. Both low-voltage dc (LVDC) and high-voltage dc (HVDC) markets are maturing. MVDC markets, comparatively, are still in the early phases of development. Currently, MVDC is primarily used in rail, with voltages up to 3 kV; however, MVDC benefits extend to a variety of potential markets, including distribution networks (e.g., conversion of existing ac lines to dc), distributed energy resources (DERs), and integrated renewable energy. One of the main difficulties preventing the growth of dc markets is a lack of reliable hardware protection against faults (e.g., short circuit and overload faults). Circuit breakers, current limiters, and fault detection mechanisms are essential to grid resiliency in a number of ways: sectioning the grid during a fault; preventing damage to wiring, power electronics, and other important assets; and restoring power to the grid after a fault is cleared.

In this program, CPES will work with Eaton Corporation and the Illinois Institute of Technology to develop an ultra-fast, ultra-efficient, intelligent, MVDC hybrid circuit breaker. The main objective of the program is to achieve 6 kV dc operating voltage, 200 A rated current, < 500 μs active interruption time, and > 99.99% efficiency and < 0.064 m^3 form factor. The technology to be developed in the program is ultra-fast vacuum switch, novel transient commutation current injector, and MV electronic interrupter, as well as system integration and intelligent switching operation.

20 kV GaN Switch Technology Demonstrated in High-Efficiency Medium-Voltage Building Block

Sponsor: Advanced Research Projects Agency-Energy (ARPA-E)

September 2019 – February 2021

One goal for the next performance period is to focus the packaging technologies on the demonstration of chip-to-megawatt power scaling using wide-bandgap switches. A 20 kV/60 A diode module and a 6.5 kV/25 A phase legs will be demonstrated with features advancing state-of-the-art numbers, such as > 50% improvement in power density.

The second goal is to develop field-grade materials for managing the electric field to ease the trade-offs among electromagnetic and thermo-mechanical stresses internal and external to a high-density power module. A field-grade coating will be developed to reduce the electrical field stress at the triple point and improve the module the partial-discharge inception voltage by 50% over commercial products. The materials will be showcased in the aforementioned 20 kV/60 A Diode Module. The height of the module could be as low as 3 cm with the coating material.

Finally, the project will develop GaN single- and multiple-channel super heterojunction diodes for 10 kV-class applications. Packaging processes and materials will be engineered for these lateral diodes.

Heterogeneous Integration Technologies for High-Temperature, High-Density, Low-Profile Power Modules of Wide-Bandgap Devices in Electric Drive Applications

Sponsor: U.S. Department of Energy

April 2019 – March 2024

The program is to develop a gate driver and power supply integrated into a low-profile SiC power module with 250° C junction temperature. A constant-current class-e dc-dc converter with air-core transformer is designed. Air-core transformer is used due to the unavailability of magnetic core above 200° C. To reduce the footprint required by the transformer, a class-e dc-dc converter is designed at 6.78 MHz. A 600 nH self-inductance and a 340 nH mutual inductance are realized with a 5 mm circular area. Zero-voltage-switching (ZVS) is achieved within a wide load range. The up-to-date prototype achieves a 78% peak efficiency and the output current keeps constant with load variation.

Future work will include efficiency, power density improvement, and control. The transformer will be optimized for a 50% loss reduction to boost the efficiency above 80%. A stack structure of the transformer and converter circuits will be designed for the integration. The impact of the transformer's stray field on the circuits will be investigated and minimized. On-off control will be designed for output voltage regulation.

Series-Resonator Buck (SRB) Converter for 48 V-54 V Power Delivery

Sponsor: Texas Instruments

November 2018 – October 2021

The fellowship program is established to support research in power delivery for data centers. As the current requirement exceeds 200 A, the 12 V architecture for power delivery incurs excessive loss. A voltage regulator module with 48 V bus voltage is introduced as a candidate to achieve high efficiency and high-power density for datacenter applications.

A Series-Resonator Buck (SRB) converter is proposed for a two-stage architecture for 48 V – 1 V power delivery with high efficiency, high-power density, and low noise. Compared with Series Capacitor Buck (SCB) converter, it achieves soft-switching with a wide and variable gain range. The solution is evaluated as the front end of the two-stage solution.

A high-frequency high-current-stress resonant inductor enables soft-switching in the SRB converter. Fringing loss effect, skinning effect loss, and core loss hinder efforts to reduce size via increasing switching frequency. The winding area is redesigned for balancing winding loss and core loss. The new design will be demonstrated in a 200 W SRB converter.

CAREER Award: High-Frequency Integrated Voltage Regulator to Support Dynamic Voltage and Frequency Scaling for Mobile Devices

Sponsor: National Science Foundation

February 2017 – January 2022

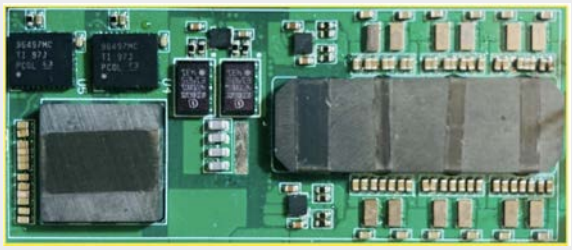
Voltage regulators have been widely used in computing systems to deliver power from energy sources such as batteries to microprocessors. Today's voltage regulator is usually constructed using discrete components and assembled on the motherboard. Discrete passive components such as inductors and capacitors are bulky and occupy a considerable footprint on the motherboard. Furthermore, the power delivery path from the voltage regulators to the microprocessors is relatively long. Recently there has been great demand for a very high-frequency integrated voltage regulator that can be placed very close to the microprocessor to support dynamic voltage and frequency scaling, which is a very effective power consumption reduction technique for microprocessors. This enables the supply voltage, to change dynamically according to the microprocessor workload (decreased workload leads to a lower supply voltage and a lower supply voltage also leads to a lower clock frequency). As a result, both the dynamic and static power consumption of the microprocessor can be greatly reduced. However, the traditional discrete voltage regulators are not able to realize the full potential of dynamic voltage and frequency scaling since they are not able to modulate the supply voltage fast enough, due to the high parasitic interconnect impedance between the voltage regulators and the microprocessors. This project focuses on developing a 20–50 MHz, three-

dimensional integrated voltage regulator for mobile devices, such as the smartphone. The proposed research will have a significant impact on power management solutions for smartphones as well as other mobile applications. It will help make the integrated voltage regulator a feasible approach to significantly reduce mobile device power consumption, which will greatly extend battery life and reduce electricity consumption. Proposed education activities also include outreach to K–12 and underrepresented groups to increase the attractiveness of power electronics.

High-Power Density, High-Efficiency, and Wide Range GaN-Based 48 V-1 V, 300 A Single-Stage Converter

Sponsor: U.S. Department of Energy through PowerAmerica, Sub-awardee of ABB

July 2019 – December 2020



160 A 48 V/1.8 V converter with 95% efficiency and 1100 W/in^3 power density.

The objective of this project is to demonstrate an efficient GaN-based single-stage 48 V to processor point of load (POL) converter that occupies less than half the board space occupied by equivalent solutions today. The outcome of the project is a technical demonstrator that supports high-current CPU processors of a data center. The proposed system can provide more than 1000 W/in^3 power density and 94.9% peak efficiency. With high-power density and efficiency, the proposed Sigma converter minimizes conversion and conduction loss, showing great potential for data center applications. In addition, a control method for the Sigma converter is proposed and verified through simulation and experiment. Results show that under wide input (40-60 V) and output (1.3-2.0 V) voltage ranges, the fast transient response can be achieved to meet VR13 transient response specifications.

High-Frequency Three-Phase Inverter

Sponsor: CRRC Zhuzhou Institute Co., Ltd.

November 2019 – November 2021

This project focuses on a high-frequency, high-density, frequency isolated, three-phase inverter module with wide input voltage range. A two-stage solution is used to provide isolation and accommodate wide input voltage range. Soft switching techniques and integrated magnetic solutions are used to improve the efficiency and power density for the proposed system. The targeted power level and efficiency are 20- 30 kW and 95-97%.

High-Density AC-DC

Sponsor: Jiangsu Wanbang Dehe New Energy Technology Co., Ltd.

November 2019 – February 2021

The objective of this project is to develop a high-density, high-efficiency, single phase ac-dc converter. The critical-mode operation is employed in order to achieve both high frequency and high efficiency. Several high-frequency design considerations are demonstrated, including zero-voltage-switching operation for the entire line cycle, and interleaving control for ripple current cancellation. At the same time, magnetic components are integrated with PCB windings for better density, manufacturability, and EMI performance. A 2.2 kW dual-phase interleaved totem-pole PFC rectifier running at ~500 kHz switching frequency is demonstrated. The peak efficiency reaches 98.6 %, and power density is 120 W/in^3.

High-Efficiency, Medium-Voltage-Input, Solid-State-Transformer-Based 400 kW/1000 V/400 A Extreme Fast Charger for Electric Vehicles

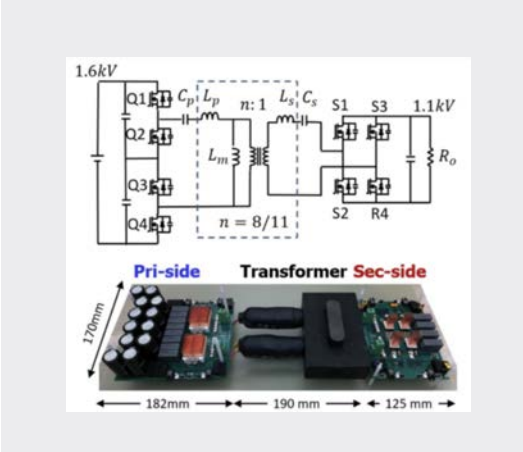
Sponsor: U.S. Department of Energy, Sub-awardee of Delta Products Corporation

July 2018 – November 2021

CPES is working with Delta Products Corporation, General Motors, DTE Energy, Next Energy, Michigan State Energy Office, and the City of Detroit Sustainability Office to deliver a novel, efficient, compact, and scalable Solid-State Transformer (SST)-based 400 kW Extreme Fast Charger


DANGER
ENERGIZED
KEYSIGHT
E36312A
Triple Output Programmable DC Power Supply
6V, 5A / 25V, 1A / 25V, 1A
LXI
1 2wire OFF
0.001 V
0.008 mA
Set 0.000 V 5.000 A
2 2wire OFF
0.001 V
-0.003 mA
Set 0.000 V 1.000 A
3 2wire OFF
0.000 V
-0.009 mA
Set 0.000 V 1.000 A
Source Settings
Output Settings
Output LIST
Data Logger
Utilities
Lock Unlock
Voltage
Current
Meter View
Tracking
Store/ Recall
Enter
All On/Off
On
On
On

(XFC). The proposed system will also provide a user-friendly dc interface to renewable energy generation systems (e.g. PV) and Energy Storage Systems (ESS), resulting in less disturbance to the existing grid. It is the enabling technology for large-scale XFC deployment. It will also accelerate the electric vehicle (EV) market penetration and promote renewable energy usage.



15 kW dc-dc building block with 99% efficiency for 13.2 kV Solid State Transformer (SST) system.

The proposed 400 kW/1000 V/400 A XFC consists of two main function blocks: a SST and a Charger Converter. The SST takes a 13.2 kV ac medium-voltage (line-to-line) and converts into a 1 kV intermediate dc bus voltage. The Charger Converter converts the 1 kV dc bus into the controllable dc-output voltage to charge an EV. The 1 kV intermediate dc bus is designed to interface with external renewable energy generation system (e.g. PV) and Energy Storage System (ESS) for load shaving and minimizing the demand charge. The bulky line frequency transformer (LFT) is eliminated in the proposed SST-based XFC system.

Ultra-High-Density 48 V-to-1 V Non-Isolated DC-DC Module

Sponsor: Powerland Technology Inc.

April 2019 – July 2021

In this project, an integrated magnetic structure and fast load transient control for a two-stage 48 V/1 V converter is studied. The proposed system has the potential to reach greater than 300 A output current with greater than 1000 W/in^3 power density.

13.8 kV Grid-Interface Power Conditioning Converter with AC and DC Microgrid Ports for Dispatchable and Resilient Manufacturing Facilities

Sponsor: U.S. Department of Energy

September 2020 – August 2023

CPES, in partnership with Siemens, will demonstrate a 13.8 kV medium-voltage (MV) power conditioning system (PCS) for flexible manufacturing plants, rated at 1.1 MVA (1 MW, 450 kVAr), with accessible 22 kV (MVDC) dc ports, using 10 kV Silicon-Carbide (SiC) MOSFET modules and a back-to-back, ac-dc-ac 5-level 'multi-cell' power converter topology. The converter system will be designed with the following targets per each three-phase ac-dc building-block:

- 99.7% peak efficiency
- a volume of 0.2 m^3 per MVA (power density = 5 kW/l)
- manufacturing costs without SiC devices of 13.6 $/kW
- a service lifetime > 10 years

To show the scalability of the proposed converter up to 3.3 MVA, the project will also demonstrate a phase-leg (ac-dc building-block) with threefold power rating using a CPES-developed triple-output gate-driver and force-paralleled 10 kV SiC modules that will triple the number of SiC dies per switch position. This higher power configuration will greatly simplify the PCS architecture for applications of up to 10 MVA (3 x 3.3 MVA).

100 kW SiC-Based Generator Rectifier Unit for Variable Frequency Airborne Applications

Sponsor: U.S. Department of Energy through PowerAmerica

July 2019 – Jan 2021

CPES, in partnership with Raytheon and GE Aviation, is developing a full SiC-based generator rectifier unit (GRU) rated at 100 kW and 600 V dc, designed to operate at an altitude of 50,000 ft., from a 200 V rms line-to-neutral, and 400–900 Hz VFG. The GRU targets a peak efficiency of 99% and a power density of 120 W/in^3 (without accounting for electromagnetic interference (EMI) filters), and will seek to displace a Si-IGBT-based GRU rated at 85 kW, 600 V dc, with a 20 kHz switching frequency, and featuring

a peak efficiency of 97% and a power density of 80 W/in^3. The GRU will use SiC MOSFET devices from GE Aviation rated for 200° C junction temperature operation, and packaged using GE's power-overlay technology. It will be liquid-cooled, operating at nominal power with a coolant temperature of 50° C, and de-rated to 50% with a coolant temperature of 75° C. Its switching frequency will be equivalent to 70 kHz or higher, allowing for a 3.5-times higher output voltage regulation bandwidth compared to the state-of-the-art unit. This increase in switching frequency will allow too for the reduction in the number of dc bus capacitors needed, further improving power density. A key design challenge is the high altitude requirement that affects both the insulation design of the inverter unit and its ancillary systems as well as the cooling systems due to the thin air constraints.

DC-DC Converter for Electrocaloric Air-Conditioning Systems

Sponsor: Carrier Corporation

September 2020 – August 2021

The objectives of this project are:

- to characterize the static and dynamic behavior of new electrical films with electrocaloric properties
- to develop a suitable model of the device and to conduct simulations to improve the understanding of the properties and capabilities of this device
- to devise a dc-dc power conversion solution and its control system
- to design and build this new power converter using capacitors instead of the electrocaloric material in order to demonstrate the converter operation and its pump action in a 1 kW unit

Developing the Future of Wide-Bandgap Power Electronics Engineering Workforce – Wide-Bandgap Generation (WBGen) Fellowship Program

Sponsor: U.S. Department of Energy

January 2016 – December 2021

The goals of the Wide-Bandgap Generation (WBGen) fellowship program sponsored by the U.S. Department of Energy (DOE) are:

- to train the next generation of U.S. citizen power engineers with wide-bandgap (WBG) power semiconductor expertise aiding in fulfilling future workforce needs in this field
- to broaden the range of WBG-based power electronics by conducting research and development on high-efficiency grid apparatus and high-efficiency electrical power systems
- enhance the power engineering curriculum by formalizing WBG-oriented design procedures for power electronics components and systems that can effectively integrate the inherent, challenging material characteristics of these devices, which have effectively rendered design procedures for silicon-based power electronics obsolete.

The WBGen fellowship has funded a total of 24 fellows since its inception in January 2016, of which 2 Ph.D. students have transitioned into other CPES programs, and 10 MS students have joined industry so far. 2021 should see 7 more MS students successfully graduate from the program. This has had an immense impact on the success of the WBG research programs at Virginia Tech, and is already having measurable positive effects on the power engineering workforce in the U.S. Furthermore, DOE laboratories and numerous CPES industrial partners have also benefited significantly from the interaction with the participating graduate students, cementing what are already strong relationships between the partners and CPES, and creating a solid network of power engineering training, research, and development. These partnerships have involved ABB Inc., General Motors (GM), United Technologies Aerospace Systems (UTAS), United Technologies Research Center (UTRC), Raytheon Technologies Research Center, HRL Laboratories, National Renewable Energy Laboratory (NREL), Oak Ridge National Laboratory (ORNL), Dominion Energy, Rockwell Collins, General Electric, Synopsys, Otis, Lockheed Martin, Newport News Shipbuilding (NNS), Nissan, the Office of Naval Research (ONR), VPT, EGSTON, Carrier, and the PowerAmerica Institute.

Development of a P-HIL System Emulator for Aerospace Electrical Systems

Sponsor: EGSTON Power Electronics GmbH

December 2018 – May 2020

This project develops a system simulation platform for aerospace electrical systems using the EGSTON COMPISO System Unit (CSU) CSU200-6AMP P-HIL that is currently in the CPES laboratory at the Virginia Tech Arlington campus. The goal was to implement the components and system models of a number of test scenarios that have been previously defined by EGSTON in collaboration with the aerospace industry, seeking to demonstrate the capabilities of the CSU to perform power hardware-in-the-loop (P-HIL) simulations in these environments. The objectives of this project were to develop the necessary models to demonstrate the CSU capability to simulate, in P-HIL mode, components and electrical systems in aerospace applications. The main emphasis of the project was to emulate three-phase induction motors.

Development of Impedance Measurement Unit for 1 kV DC and 800 V AC Systems

Sponsor: Newport News Shipbuilding

August 2017 – March 2020

Newport News Shipbuilding (NNS) approached CPES with the purpose of developing two medium-voltage (MV) impedance measurement units (IMU) for three-phase ac and dc electrical systems. NNS engineers worked jointly with the team at CPES to ensure an expedient technology and knowledge transfer for the project. Phase I was executed seeking to develop a new IMU rated at 1 kV dc, 800 V ac, with an injection capacity of 200 kW and an impedance measurement bandwidth spanning from 10 Hz to 1 kHz. The main measurement and operating modes under consideration were shunt and series operation. The IMU topology selected was a module-based single-phase configuration that CPES pioneered to develop for Office of Naval Research, the first IMU capable of operating from medium-voltage feeders using 10 kV SiC MOSFET devices. The project also set out to expand the stability theory and develop methods to assess stability in three-phase unbalanced networks, which was successfully achieved through this program after more than a decade of pursuing such development. In its second year of execution the IMU operation was successfully tested and demonstrated in both shunt and series injection modes operating from ac and dc grids. The IMU was delivered to the sponsor in early 2020.

Development of the PEBB 6000 Using Gen3 10 kV, 240 A SiC MOSFET Modules in Full-Bridge Configuration

Sponsor: Office of Naval Research

December 2017 – July 2021

After many years of sustained support from the U.S. Department of Defense, especially the Office of Naval Research (ONR), a revolutionary new silicon carbide (SiC) power semiconductor device was developed by Wolfspeed (formerly Cree), currently under production in 10 kV, 240 A SiC MOSFET half-bridge modules. As such, for the first time in history, a fully qualified, properly packaged, megawatt-scale semiconductor device capable of switching at frequencies above 20 kHz, with very high efficiency, is available. This event, coupled with new developments in modular multi-cell power converters, is expected to completely transform the world of medium-voltage (MV) high-power electronics.

Under the sponsorship of ONR, CPES has developed and demonstrated the operation of the first SiC-based PEBB rated at 6 kV, utilizing the second generation 10 kV, 120 A, SiC MOSFET half-bridge modules from Cree/Powerex/GE. More recently, CPES has developed too an advanced gate-driver for these modules with enhanced functionality and EMC capabilities. In addition, CPES has recently completed the initial development of the SiC-based PEBB 1000, based on 1.7 kV SiC power modules from Wolfspeed. Utilizing the knowledge from these three efforts, this new project has sought to demonstrate for the first time a full-bridge, self-contained, SiC-based least replaceable unit (LRU) rated at 1 MW, 6 kV and 20 kHz. Dubbed the PEBB 6000, this unit will feature a power density of 10 MW/m^3, 99% efficiency, zero conducted EMI emissions, a 30 kV partial discharge inception voltage, and a 0 V enclosure potential. The proposed program will demonstrate two PEBB 6000 units, formulating the high-power density design methodology to achieve the set targets, evaluating its electrothermal

performance, and assessing the impact of their operation in PEBB-based power converters and systems.

High-Power Density 10 kV SiC-MOSFET-Based Modular, Scalable Power Converters for Medium-Voltage Applications

Sponsor: Advanced Research Projects Agency-Energy

February 2018 – August 2021

The nearly ideal material properties of silicon carbide (SiC) are transforming the design and manufacturing paradigm of power electronics. Specifically, pervasive dv/dt and di/dt rates, augmented electromagnetic interference (EMI) emissions, higher operating voltages and switching frequencies, and junction temperatures greater than 200° C, have made apparent the need for the reformulation of design procedures developed for Silicon (Si)-based power electronics, as well as for the materials, packaging, and integration, and manufacturing technologies used. More so, the adequacy of existent circuit topologies is under scrutiny now, as their Si-optimized operation may impede the exploitation of the capabilities offered by SiC.

The last point is of special interest in medium-voltage (MV) and high-voltage (HV) applications, where multilevel converters and modular multilevel converters (MMC) have been developed to overcome the limitations of Si in terms of breakdown voltage, switching frequency, and efficiency. Expectedly, the use of SiC in these Si-optimized converters would yield minor gains, for which simpler two-level topologies have been pursued so far for 10 kV SiC MOSFETs. The latter promise direct connection to 4,160 V ac busses and increased power density by switching at 20–40 kHz, in what is a glimpse of the potential offered by SiC.

Addressing the above, this project proposed the development of modular power converters for MV applications optimized for SiC devices capable of achieving:

- power density greater than 10 kW/L
- efficiency greater than 99%
- specific power greater than 10 kW/kg
- unrestricted current and voltage scaling
- operation in both ac and dc power conversion modes

Such flexibility can be attained by adopting an MMC-type circuit, but using previously untapped topological states of this converter. Two unique circuit operating modes are unveiled in this way, one enabling the switching-cycle control of the power-cell voltages, which effectively eliminates their line-frequency dependence, and one that inverts their operating mode allowing for the direct power flow between the converter input and output terminals without having to transiently store energy in the power-cells. Both concepts have been extensively tested through simulations in applications of up to 120 power-cells, but have yet to be demonstrated experimentally. This constitutes the main objective of the project that targets the development of 5 mW, 20 kV modular ac-dc and dc-dc power converters.

During 2019, CPES successfully demonstrated two power-cells rated at 6 kV dc, 84 A rms, switching at 10 kHz, operating in a circulating power scheme and processing 250 kW at an exceedingly high 99.3% power conversion efficiency. The power-cell building-blocks in question also demonstrated the effective use of PCB technology to realize 6 kV dc planar dc bus structures featuring partial-discharge-free operation at 6 kV. The program has also successfully demonstrated auxiliary power supplies with insulation ratings of up to 30 kV, and input-output capacitances in the 2–3 pF range, which are necessary to effectively suppress the propagation of conducted EMI through the power-cells. The project has also made effective use of the electric-field constrained design methodologies developed within the project, and also in leveraging efforts funded by the Office of Naval Research (ONR) and the U.S. Department of Energy.

In 2020, the project devoted itself to the revision of the power-cell design which had as its main task and goal the methodic design of its insulation system to achieve partial-discharge (PD)-free operation up to 30 kV. This was successfully demonstrated in the final prototype of the power-cell, which was used to create a manufacturing line that so far has produced 8 of the 16 total units that are needed. In conjunction with the ONR project developing the PEBB 6000, and the CPES mini-consortium on wide-bandgap high-power converters and systems (WBG-HPCS), the project also concentrated on the development of a highly-synchronized digital communication and control network that achieved a sub-nanosecond synchronization

accuracy. This control network is used to establish all communications between power-cells, which are hence fully isolated over the associated high-speed optical network. Similarly, an optical tightly-synchronized communication and control network was developed to establish all communications within the power-cells, including the main controller, enhanced gate-drivers, and sensors. Lastly, the project developed the digital control architecture and also reduced to practice the digital control algorithms to implement the two novel fast-switching control schemes under evaluation in the project; namely the integrated capacitor-blocked transistor (ICBT) concept, and the CPES-developed switching cycle control (SCC). The complete modular converter rated at 24 kV and 2 mW is expected to be tested early in 2021.

High-Efficiency SiC-based Flexible-CHP Interface-Converter with Advanced Grid-Support Functions

Sponsor: U.S. Department of Energy

October 2018 – December 2021

This project proposes to develop a modular, scalable MV power converter featuring stability-enhanced grid-support functions for future F-CHP systems operating in small- to mid-size U.S. manufacturing plants being fully compliant with the IEEE Std 1547 and IEEE Std 2030.7. To this end, a modular circuit topology will be adopted based on 10 kV SiC MOSFET devices, achieving an efficiency greater than 98%, and a power density greater than 10 kW/L. As such, the proposed converter will not just profit from the high blocking voltage capability of these devices, but also from their inherent high efficiency and from their high switching frequency capacity. The latter will be enabled by a control scheme developed at CPES that can balance the converter capacitor voltages on a switching-cycle basis. Further, the voltage and current scalable capacity of the proposed converter will render it an appropriate solution for 1–20 MWe F-CHP systems, which typically operate in the 2–13.8 kV voltage range.

For demonstration purposes, a scaled-down modular power converter based on 1.7 kV SiC MOSFET devices, and rated at 480 V ac, 60 Hz, 200 kW, and 150 kVAr (±0.8 power factor), will be used to evaluate the converter operation and key performance metrics. These will be extrapolated to the MV solution using the ongoing work at CPES on the development of 10 kV SiC MOSFET-based modular power converters for MV grid applications. The converter prototype will be evaluated using an Egston P-HIL test bed rated at 480 V and 250 kW, which will emulate both the CHP generator and the microgrid environment for the F-CHP. A Siemens SICAM A8000 microgrid controller will be connected to the P-HIL unit and to the converter prototype, and will be used to direct the operation of the emulated microgrid and to demonstrate the grid-support functionality of the converter in compliance with the IEEE standards in question.

The proposed converter and control system will be able to measure the grid and its own terminal impedance, which will allow it to implement the stability-enhanced grid support functions. Accordingly, the converter will be able to:

- operate in over-excited and under-excited reactive power generation mode
- participate in voltage regulation under constant power factor, voltage-reactive power, active power-reactive power, and constant reactive power modes, and also by adjusting its active power generation as a function of voltage
- respond to abnormal conditions
- participate in frequency regulation
- operate in and detect both unintentional and intentional islanding conditions
- monitor the grid stability conditions
- use grid-forming controls
- monitor the microgrid with the GPS-synchronized integral μPMU module

Highly-Integrated Modular CM-DM Filters for Interleaved and Parallel SiC Converters

Sponsor: Siemens AG

September 2018 – December 2020

This project develops new modular and scalable filters, namely filter building blocks (FBB), for common-mode (CM) and differential-mode (DM) electromagnetic

interference (EMI) noise suppression, power quality control, and circulating current suppression in parallel Silicon-Carbide (SiC)-based converter systems. Key aspects of the desired modular filter solution were that it should allow the parallel operation of any number of filters, and that it should block the circulation of current between converters operating synchronously or in PWM interleaved mode. In addition, high-power density and efficiency were also desired objectives.

The power converter units to be connected in parallel, from common ac to dc buses, were three-level three-phase ac-dc voltage-source converters implemented with SiC 1.2 kV MOSFET devices and hence operating in the 40–100 kHz range. The prototype units built, for testing and demonstration purposes, were three-level, three-phase, ac-dc voltage-source converters implemented with SiC 1.2 kV MOSFET devices and switching at 40 kHz, and rated for 380 V ac, 800 V dc, and 15 kW. A total of three (3) converter units were built to demonstrate the modular, scalable FBB structure developed.

While in 2019 CPES successfully developed a novel modular FBB concept that could effectively limit DM and CM harmonic components, ensure power quality, and suppress the circulating current between the directly paralleled converter building blocks, in 2020 the project devoted itself fully to the experimental demonstration and evaluation of the modular filters. To this end, the three-converter prototype test bed was used extensively to assess the effectiveness and modularity of the FBB developed, characterizing the suppression of circulating currents, EMI emissions, power quality, and the efficiency of the units. Special emphasis was given to the secondary power loop used to interconnect the FBBs between converter units, which effectively suppresses circulating currents while providing DM-mode "boost" inductance to their operation.

Intelligent Power Stages (IPS)

Sponsor: Oak Ridge National Lab

July 2020 – June 2022

Supporting Oak Ridge National Laboratory's (ORNL) effort to develop future solid-state transformers by building and demonstrating their building-blocks, namely Intelligent Power Stages (IPSs) featuring advanced power conversion and control functionalities, CPES is developing a three-phase ac-dc-dc IPS unit rated at 50 kW and 75 kVAr (75 kVA), utilizing SiC devices to achieve an efficiency > 98%, and a power density > 10 kW/l. The proposed IPS topology has a three-phase ac-dc input terminal and a dc-dc output stage using a three-level buck-boost dc-dc converter for minimized electromagnetic interference (EMI) emissions. In addition, the IPS will demonstrate: Interoperability, grid and fault monitoring capacity, integrated modular filter-building-blocks (FBB), operational diagnostics and prognostics, electromagnetic compatibility (EMC), enhanced intelligent gate-driving with integrated sensors, EMC-enhanced intelligent sensors, EMC-enhanced auxiliary power supply network, and fiberoptic-based control, sensor, and communication networks.

Power Conversion Through a Novel Current Source Matrix Converter (PCTMXC)

Sponsor: Advanced Research Projects Agency-Energy (ARPA-E), Sub-Awardee of Raytheon Technologies Research Center

May 2018 – April 2021

Raytheon Technologies Research Center (RTRC), formerly United Technologies Research Center (UTRC), proposed a novel solution of a Matrix Converter (MxC), with voltage boost capability as a response to ARPA-E SWITCHES program. The proposed solution enables operation above 86.6% of input voltage and thus overcomes limitations of traditional MxC. Accordingly, the proposed MxC operates in "boost" Current Control Mode (CCM) in contrast to the traditional Voltage Control Mode (VCM). The concept is applicable to the broad range of systems where the source is an electrical generator. CPES has supported this effort by developing two hardware prototype demonstrators of the MxC, rated at 380 V ac, 60 Hz, and 15 kW, with a 1-min overload capacity of 25 kW, using 1.2 kV Silicon-Carbide (SiC) MOSFET devices.

The first-generation prototype used a modular per-phase PCB-based structure and through-hole discrete SiC MOSFETs packaged in 4-pin To-247, successfully demonstrating the boost current-mode operation of the MxC while also achieving a power density of 10 kW/l. The

second generation, improved prototype, adopted surface-mount devices to improve the switching performance and manufacturability of the unit, and used instead a single PCB-based design with Aluminum-Nitride ceramic inserts to minimize the thermal impedance from the device packages to the bottom-side mounted heatsink. The full three-phase implementation of the MxC on a single PCB was further exploited by designing an optimized physical layout, which minimized and balanced the parasitic inductances for the three commutation paths per switching pole. This resulted in an improved switching performance and reduced EMI, which helped counteract the main tradeoff of adopting surface-mount devices; namely the increased parasitic capacitance to ground. With these significant improvements, the second-generation MxC achieved a power density of 15 kW/l, an efficiency of 98.5%, and a 1 minute 25 kW overload capacity.

Small-Signal Modeling and Stability Specification of a Hybrid Propulsion System for Aircraft

Sponsor: National Aeronautics and Space Administration

January 2020 – January 2021

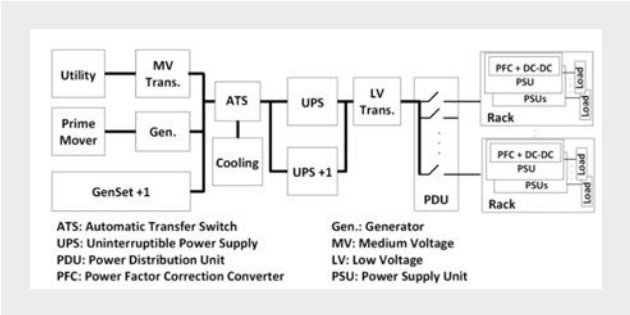
This project will develop models and stability specifications for the electric propulsion system of the Single-aisle Turboelectric Aircraft with an Aft Boundary Layer propulsor (STARC-ABL), which features tightly coupled electrical and mechanical dynamics. Specifically, the project has set out to model the STARC-ABL electric propulsion system, including the drivetrain, synchronous generator, commercial power supply for the testbed, rectifier, battery energy storage converter, housekeeping load, inverter, and the motor to drive the tailfan. The ultimate goal is to develop small-signal stability criteria accounting for both the electric and electro-mechanical systems in the associated gas turbine-generator powertrain.

Small-Signal Stability Analysis in Data Centers with Unbalanced PFC Loads

Sponsor: Google

March 2020 – June 2022

Google has approached the Center for Power Electronics Systems (CPES) at Virginia Tech to investigate the stability and dynamic interactions in data center distribution systems with multiple single-phase power factor correction (PFC) loads. The objective of this project is to analyze the small-signal stability in three-phase, four-wire datacenter distribution systems with multiple PFC loads, with the intent to formulate an analysis methodology and a test procedure capable of predicting the occurrence of dynamic interactions, having as the ultimate goal the reduction in the number of field tests during the construction and commissioning of data centers.



Data Center Power System.

To this end, CPES will expand on its recently developed stability analysis methods for three-phase unbalanced networks, developing the corresponding models to study the above system in both time and frequency domains, and building a test bed to verify the methods to be developed. The latter will employ both Google PFC loads, and CPES-developed PFC loads given the expected need to have full knowledge of the PFC operation and controls in the formulation of the methods in question. An electronic power supply, and a 30 kVA synchronous generator, will be used as sources. Lastly, CPES will make use of its low-voltage impedance measurement unit (IMU) to extract the synchronous d-q frame, small-signal impedances seen at the points of interest.

USB Type-C Power Delivery: Charger Development

Sponsor: Collins Aerospace

November 2020 – July 2021

The objectives of this project are to develop an integrated, highly compact USB Type-C PD charger targeting low cost and high efficiency, seeking to demonstrate a TRL 3 single-output prototype, including both single-phase PFC ac-dc

and high-frequency isolated dc-dc stages, with the following specifications: 100 W, 115 V, 360–800 Hz input, 5, 9, 15, and 20 V dc output. The project will specifically target: power density > 50 W/in^3, nominal power efficiency > 90%, 10% load efficiency > 80%, and 15 mW of standby power consumption. The proposed converter will use commercial-off-the-shelf (COTS) units as benchmark. The charger will encompass the power stage, electromagnetic interference (EMI) filters, and use available integrated-circuit (IC)-based controls, allowing the project to hone in on the performance and integration aspects of the unit. The main challenge at hand will be the design optimization of the ac-dc-dc powertrain to satisfy the wide output voltage range of the USC-C type charge specifications.

Machine Learning Enhanced Material-Device Co-Design for Power Electronics

Sponsor: The Thomas F & Kate Miller Jeffress Memorial Trust

August 2020 – July 2021

Power devices based on wide-bandgap (WBG) materials have demonstrated unprecedented performances and seen early applications by companies like Tesla, Google, and Amazon. However, their performance is still far from the theoretical limits. Their design practices mostly rely on empirical experiences, which often lead to non-optimum designs. While machine learning (ML) could efficiently traverse the material/device design spaces, it is prohibitively costly and time-consuming to obtain large experimental data for ML training. This project aims to develop a novel and computationally efficient framework, which comprises advanced ML models and a data-generation scheme that utilizes Technology Computer-Aided Design (TCAD) simulations to augment the experimental data. The calibrated TCAD simulations will be used as a 'low cost' tool to generate extra device data (10-to-100- fold larger than experimental data). Reservoir computing (RC), a recent ML paradigm with enhanced performance but significantly lower size and power budgets, will be used to construct deep learning models. The TCAD-ML framework will be explored to correlate the material/device designs to the device performance metrics in both forward process and inverse process. A highly interdisciplinary team with the leading experts in WBG materials and devices, power electronics, TCAD simulation, ML, has been assembled. Silvaco, a global leading EDA/TCAD company, will collaborate with the team. This project also highlights unique and interdisciplinary undergraduate research training on materials, devices, data science, TCAD, and ML.

Surge Energy Robustness of GaN Power Devices and Modules: Application-Driven Evaluation and Physics-of-Failure Modeling

Sponsor: U.S. Department of Energy through PowerAmerica

January 2020 – January 2021

This project aims to evaluate the surge energy robustness of commercial GaN power transistors and modules, through a combination of experimental characterization, failure analysis, and physics-based modeling. The outcomes of this project include:

- understanding how the GaN power transistor, a device without avalanche capability, withstands the surge energy, as well as the key determining factors for the withstand capability under single event and repetitive tests
- unbiased evaluation of surge-energy robustness of commercial GaN devices based on different enhancement-mode (E-mode) technologies
- evaluation of surge energy robustness of GaN devices under surge-energy switching events based on application-specific mission profiles

The test platform developed in this project will be made available to all PowerAmerica members after the project.

Ultra-Wide-Bandgap Electronics for High-Temperature Energy Applications

Sponsor: Southeastern Center for Electrical Engineering Education

July 2019 – July 2020

The global high-temperature electronics market is projected to reach $15 billion by 2023. A critical problem of today's high-temperature systems is the need for expensive, complicated and bulky cooling systems to protect silicon-based electronics. The ultimate goal of this project is to

develop next-generation electronics that can directly operate in extreme high-temperature environments (over 300° C), through the use of emerging ultra-wide-bandgap (UWBG) semiconductors, which have significantly superior thermal stability compared to silicon. The proposed work will boost innovation in both materials and devices. This seed grant will support one student with the goal to demonstrate the experimental prototype for the high-temperature UWBG devices. The intellectual products of this project are highly transportable with high impact in electrical engineering and material science. This project will also open up a wide range of external funding opportunities and therefore provide key momentum for the PI's career development.

INTELLECTUAL PROPERTY

INNOVATIONS SHARED

U.S. Patents Awarded

All patents awarded available to IP Sharing, unless otherwise noted.

VTIP 19-022

Bidirectional Three-Phase Direct Current DC-DC Converters

Hao Xue, Bin Li, Qiang Li, Fred C. Lee
U.S. PATENT 10,873,265
Issued December 22, 2020

VTIP 18-089

Interleaved Converters with Integrated Magnetics

Chao Fei, Bin Li, Fred C. Lee, Qiang Li, Hongfei Wu
U.S. PATENT 10,770,081
Issued September 29, 2020

VTIP 16-029

DC-DC Power Converter

Shigeharu Yamagami, Khai Doan The Ngo
U.S. PATENT 10,778,110 (Sponsored by Nissan)
Issued September 15, 2020
Not available to IP Sharing

VTIP 16-022

Non-Linear Droop Control

Fang Chen, Rolando Burgos, Dushan Boroyevich
U.S. PATENT 10,770,988
Issued September 8, 2020

VTIP 15-067

Inverse Charge Current Mode (IQCM) Control for Power Converter

Syed Bari, Fred C. Lee, Qiang Li
U.S. PATENT 10,673,328
Issued June 2, 2020

VTIP 18-113

Switched Capacitor Converters with Multi Resonant Frequencies

Owen Jong, Qiang Li, Fred C. Lee
U.S. PATENT 10,658,928
Issued May 19, 2020

U.S. Patents Filed

All pending patent applications available to IP Sharing, unless otherwise noted.

VTIP 20-018

Soft-Switched Series Capacitor Buck Converter

Cong Tu, Khai Ngo, Ting Ge, Rengang Chen
(Texas Instruments)
Nonprovisional application in process

VTIP 20-086

Short Pulse Gate Signal Voltage Balancing in Series-Connected MOSFETs

Xiang Lin, Dong Dong, Rolando Burgos
U.S. Serial No. 17/064,080
Filed October 6, 2020

VTIP 20-085

Core Loss Characterization and Measurement

Yuliang Cao, Minh Ngo, Dong Dong, Rolando Burgos
U.S. Serial No. 17/006,058
Filed August 28, 2020

VTIP 20-058

Medium Voltage Planar DC Bus with Distributed Capacitor Array

Lakshmi Ravi, Joshua Stewart, Dong Dong, Rolando Burgos
U.S. Serial No. 16/939,914
Filed July 27, 2020

VTIP 20-051

Bidirectional Architectures with Partial Energy Processing for DC-DC Converters

Yuliang Cao, Minh Ngo, Ning Yan, Dong Dong, Rolando Burgos
U.S. Serial No. 17/008,893
Filed September 1, 2020

VTIP 20-027

Control of Power Converters Having Integrated Capacitor Blocked Transistor Cells

Jianghui Yu, Rolando Burgos
U.S. Serial No. 16/844,514
Filed April 9, 2020

VTIP 20-026

Series/Series Resonant Topology for Wireless Power Transfer

Keyao Sun, Jun Wang, Rolando Burgos, Dushan Boroyevich
U.S. Serial No. 16/913,066
Filed June 26, 2020

VTIP 20-023

High-Density Single-Turn Inductor

He Song, Jun Wang, Rolando Burgos, Dushan Boroyevich
U.S. Serial No. 16/854,730
Filed May 4, 2020

VTIP 20-015

Gallium Oxide Vertical Schottky Barrier Diode

Yuhao Zhang, Kohei Sasaki
U.S. Serial No. 63/057,115 (Sponsored by Novel Crystal)
Filed July 27, 2020
Not available to IP Sharing

VTIP 19-134

Low Impedance Multi-Conductor Layered Bus Structure with Shielding

Jun Wang, Rolando Burgos, Dushan Boroyevich, Joshua Stewart, Yue Xu
U.S. Serial No. 16/879,078
Filed May 20, 2020

VTIP 19-133

Hybrid-Current Mode Switching-Cycle Control
Jun Wang, Rolando Burgos, Dushan Boroyevich
U.S. Serial No. 15/931,795
Filed May 14, 2020

VTIP 19-117

Magnetic Integration of Matrix Transformer with Controllable Leakage Inductance
Ahmed Nabih, Qiang Li, Fred C. Lee
U.S. Serial No. 16/864,868
Filed May 1, 2020

VTIP 19-116

Efficient Wide Voltage Range Quasi-Parallel Voltage Regulator
Mohamed Ahmed, Fred C. Lee, Qiang Li
U.S. Serial No. 16/865,236
Filed May 1, 2020

VTIP 19-114

High Electron Mobility Transistors with Charge Compensation
Yuhao Zhang
U.S. Serial No. 16/881,846
Filed May 22, 2020

VTIP 18-123

Three-Phase, Three-Level Inverters and Methods for Performing Soft Switching with Phase Synchronization
Nidhi Haryani, Sungjae Ohn, Rolando Burgos, Dushan Boroyevich
U.S. Serial No. 16/416,915
Filed May 29, 2019

VTIP 18-072

Integrated Parallel Matrix Transformer and Inductor
Mohamed Ahmed, Fred C. Lee, Qiang Li
U.S. Serial No. 16/899,053
Filed June 11, 2020

VTIP 17-108

Interleaved Converters with Integrated Magnetics
Chao Fei, Bin Li, Fred C. Lee, Qiang Li
U.S. Serial No. 16/006,117
Filed June 12, 2018

VTIP 16-109

Matrix Transformer and the Winding Structure
Chao Fei, Fred C. Lee, Qiang Li
U.S. Serial No. 15/656,198
Filed July 21, 2017

VTIP 14-075DIV

Compact Inductor Employing Redistributed Magnetic Flux
Khai Ngo, Han Cui
U.S. Serial No. 17/025,777
Filed September 18, 2020

VTIP 14-075

Compact Inductor Employing Redistributed Magnetic Flux
Khai Ngo, Han Cui
U.S. Serial No. 14/675,653
Filed March 31, 2015

FACILITIES

WORLD-CLASS INFRASTRUCTURE

The Center headquarters are located at Virginia Tech, occupying office and lab facilities encompassing more than 20,000 square feet of space in one building. Research space at CPES-VT includes an electrical research lab, an integrated packaging lab, and a computer lab. In addition to the headquarters labs and offices, a large conference room with voice and video conferencing capabilities supporting remote site course instruction, as well as interaction among CPES collaborators, is maintained. Interactive collaboration is routinely facilitated through conference calls, GoToMeeting and Zoom online conferencing, student and faculty exchanges, and face-to-face research project review meetings.

National Capital Region Laboratory

CPES's expansion into Northern Virginia includes state-of-the-art power electronics and packaging laboratories that are well-suited to continue building upon CPES's internationally-recognized expertise in developing groundbreaking power electronics technologies. The power electronics lab opened for the spring semester of 2019, and is located on the fourth floor of the Virginia Tech Research Center in Arlington, Virginia, occupying more than 1,800 square feet of space. Equipped with the latest testing and measurement equipment capable of achieving several hundreds of kilowatts of power, the lab provides an environment for unparalleled hands-on experience for graduate students and visiting scholars. The packaging laboratory is equipped with state-of-the-art equipment for designing, building, characterizing, and testing advanced power electronics packages. These new labs contribute to Virginia Tech's expanding presence in Northern Virginia.

Electrical Research Laboratory

The electrical research laboratory is equipped with state-of-the-art tools and equipment for development of power electronic circuits and systems of all sizes, from sub-volts, sub-watts to 6 kV, 1 MW. It also includes PWB manufacturing equipment, an EMI chamber, a clean room, and a mechanical shop. Each student bench is equipped with Dell computers with up to 32 GB of RAM for running complex simulations.

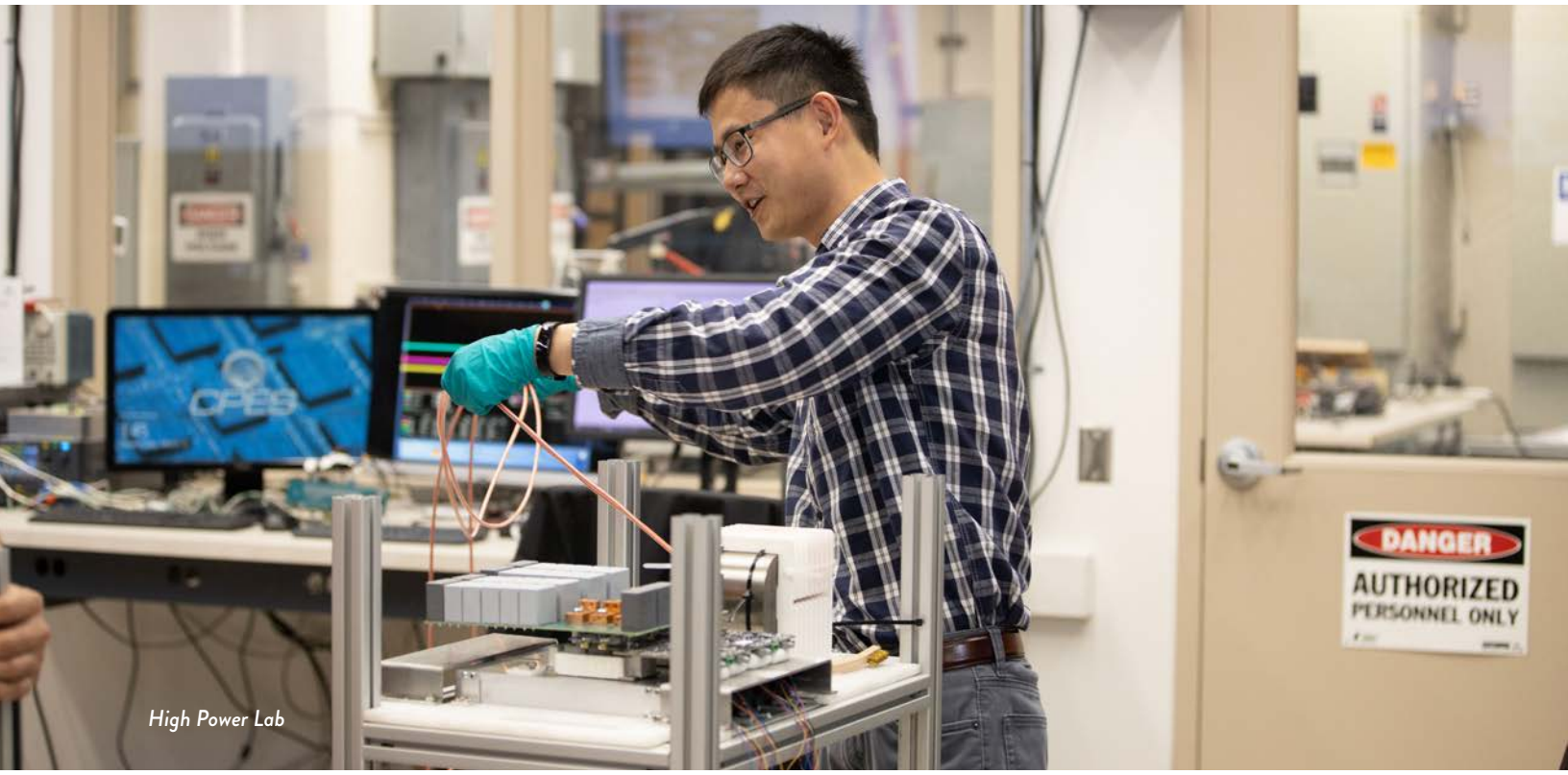
Standard instrumentation includes GHz oscilloscopes, multi-channel function generators, electronic loads, low- and high-voltage passive and differential probes, network, spectrum, impedance, logic, and power analyzers, thermal sensors, and ac-dc bench supplies of all sizes. Specialized test room equipment includes thermal imaging, a Hi-Pot tester, a 3D magnetic field scanner, an EMI/EMC analyzer, large and small dynamometers, automatic circuit board routing equipment, magnetic core loss testing, programmable and variable loads, and a liquid-cooled heat exchanger.

Integrated Packaging Lab

The Integrated Packaging (IP) Lab supports all CPES students, faculty, visiting scholars, and sponsors for their advanced needs in power electronics packaging research. The lab was established to create and evaluate alternative approaches to the design and manufacture of Integrated Power Electronics Modules (IPEMs) and provide state-of-the-art electronic manufacturing and assembly equipment. The IP lab itself has installed a sealed ceiling and HEPA filtration to create over 1,600 square feet of class 10,000

National Capital Region Laboratory


Integrated Packaging Lab



High Power Lab

cleanroom space. It has the capability to produce FR4, DBC, and thick film hybrid substrates, perform metallization using RF sputtering thin film deposition and electro- and electroless plating, and develop substrate patterns by virtue of laser ablation machining, chemical metal etching, and screen printing. New this year is a chamber for high altitude testing.

The IP lab also has the ability to mount bare dies and SMT components using a high-precision pick-n-place machine, a solder reflow belt furnace, and a convection reflow oven. The vacuum solder reflow system provides another technical solution for die-attachment in a flux-less, void-less process. Device attachment reliability is tested with the Dage 4000 Die shear equipment.

State-of-the-art device characterization equipment can also be found in the IP lab. This includes a Keysight B1505A curve tracer that is rated at 10 kV and 1500 A, a Form Factor probe station with a gold thermal chuck, and ATT system's thermal controller/chiller to give the ability to test bare die from -30° C to 300° C. The thermal chiller runs solely on air, which is provided by a 7.5 hp Ingersoll Rand air compressor.

The wire bonding machines equipped in the IP lab provide interconnect options of heavy aluminum wire bonding, gold wire ball bonding, and aluminum/gold ribbon bonding for manufacturing IPEMs. For accurate and controlled dispensing of adhesives and encapsulants, an automated precision dispensing system is in the lab. In addition, the IP lab has full capability for low temperature, co-fired ceramic (LTCC) processing from tape cutting, via drilling, screen printing, laminating, to co-firing. The components and module-level test and evaluation of electrical, thermal, and reliability performance for the assembled IPEMs are also available in the IP lab. Thermal performance evaluation can be made by the setup of thermo-couples, optic- fiber sensors, IR imaging, and the thermal diffusivity test system. Reliability analysis is performed using multi-purpose bond tester on as-made modules and ones after certain numbers of temperature/humidity cycling.

High-Power Lab

High-power, high-voltage power conversion technologies are attracting increasing attention in academia as well as industry in response to a need for more emerging power electronics applications, including alternative energy and power conversion such as wind power generations, fuel cells, hybrid electric vehicles, and all-electric ships. Enabled by a 2002 award of $839,337 from the Defense University Research Instrumentation Program (DURIP) paired with CPES cost-sharing of more than $250,000 for renovations, the electrical research lab area at Virginia Tech has been renovated and upfitted to accommodate medium-voltage, megawatts power capability. The facility has two medium voltage 1 MVA reconfigurable transformers, corresponding reactors, capacitors, switchgears, and controllers. The complete set-up is capable of testing power converters in various active and reactive operation modes continuously at 1 MVA, 4,160 V level. The unique installation distinguishes Virginia Tech as one of a few universities in the nation with this capability and enhances its position as a leader in power electronics research well beyond the NSF ERC life expectancy.

CPES also has the ability to test at 1 kV/100 A, 2 kV/50 A, and 3 kV/33 A with Magna dc Power Supplies along with 400 V/45 kVA/30 kVA ac-dc at various frequencies using the California Instruments MX-45 and MX-30. The high power lab has also added a TDK-Lambda 30 kV/3.3 A supply. Partial Discharge testing is being done with a Phenix 50 kV Hipot tester.

Software Support

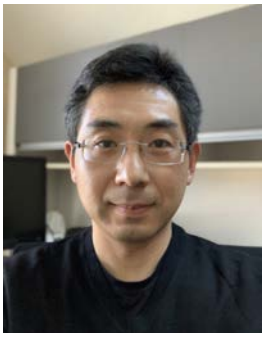
CPES supports all major software used in power electronics design, including SPICE, Saber, Simplis, PowerSim, Code Composer, Math products—Matlab and Mathcad, Ansys Products—Workbench and Mechanical, Ansys Electromagnetics—Maxwell, Electronics Desktop (Q3D, HFSS), Simplorer, SIWave, PLECS, and Altium Designer.

Computer Lab

SPOTLIGHT ON ALUMNI

TOGETHER WE LEAD

Rengang "Roger" Chen



Affiliation
Texas Instruments

Position Title
Business Lead, multiphase products, BMC/MCS

Last Degree from Virginia Tech
Ph.D.

Year
2005

Career Highlights

2005 – 2010	System Apps Manager, International Rectifier
2010 – 2018	System Apps Manager, NexFET products, Texas Instruments
2018 – 2019	System Architect/technologist, multiphase product line, Texas Instruments
2019 – present	Business Lead, multiphase products, Texas Instruments

"Time flies. I still remember very clearly the time I first flew to the U.S. and joined CPES, Virginia Tech 22 years ago. It feels like yesterday. The first semester was definitely not easy, especially when I took the Power Electronics course from Dr. B and the Power Converter Modeling and Control course from Dr. Lee at the same time. But I was so fortunate and grateful that we had the best faculties, staff members, and senior students in CPES. They helped and supported me (and other new students) in numerous ways to have the transitions as smooth and fast as possible. I quickly become a true CPES member and started to help junior students as well. This is one of the best things I liked in CPES. CPES also has great academic environment. I remembered those tough questions and debates in group meetings, in-depth papers and presentations in the CPES annual conferences, and especially the guidance I received from my advisor Dr. Van Wyk, during the weekly 1-on-1 meetings we had in his office. All of the valuable experience in CPES not only helped me achieve the graduate degree, but also helped develop my career in the power semiconductor industry in the past years, and for the years to come."

Heath Kouns

Affiliation
Moog, Inc.

Position Title
Electronics Engineering Manager and Innovation Team Lead

Last Degree from Virginia Tech
MSEE

Year
2000

Career Highlights
Heath started at Moog as a Project Engineer and has held numerous roles for the company ranging from Engineering Manager to Global Product Line Manager. He is an accomplished team leader with 6 Sigma Leadership and Program Management certifications. Throughout his career, he has excelled at innovative problem solving and has multiple patents to his credit.

Heath and Penny and their 5 kids reside on a small farm in the New River Valley.

"Thinking back on my time at CPES, I remember it being a period of tremendous personal growth. The environment provided the opportunity to develop independent critical analysis and thinking skills in the context of world leading research. The camaraderie of the CPES students, faculty, and staff was second to none and yielded a collaborative atmosphere in which to try new ideas and generate breakthrough technologies. I remember that everyone was committed to doing their best even when it required long hours. Based on my current view of the research, this commitment to quality is still present at CPES."

Yong "Perry" Li

Affiliation
Dialog Semiconductor

Position Title
Senior Director, Systems and Applications

Last Degree from Virginia Tech
Ph.D.

Year
2002

Career Highlights

2002 to 2007 – Senior Design Engineer, International Rectifier (IR), Los Angeles. Contributed to the development of the IRMCF300 series digital control ICs and iMOTION design platform

2007 to 2013 – Joined iWatt in 2007, a start-up specializing in digital power at Silicon Valley. Started as a Principal System Engineer, and progressed to Vice President, ACDC Systems and Applications. Served as the chief inventor, system architect and IC design team lead for most of iWatt's ACDC digital control ICs, which were widely adopted by world-class electronics device manufacturers on smart phones, networking equipment, and solid-state lighting, with multi-billion units of shipment. While working full time at iWatt, completed the VLSI Engineering Certificate Program at University of California at Santa Cruz in 2009.

2013 to Present – Joined Dialog Semiconductor through its acquisition of iWatt in 2013. As Senior Director, Systems and Applications, continues to lead the team to develop advanced power conversion controllers and system solutions, including those for the latest intelligent high-power-density fast charging for smart phones and note-book PCs.

- Holds more than 30 U.S. patents

"It's been 19 years since I graduated from CPES, but I still feel the tremendous impact it had on me on a daily basis. I am always grateful for the great opportunity to study under the best in the power electronics world, including my endlessly inspiring advisor Dr. Lee, and to learn from and grow with fellow students who became my lifelong friends. CPES provided me with not only technical skills to succeed in my career, but also a creative and collaborative spirit that has benefitted all aspects of my life. I hope that the next generations of talented CPESers will continue to flourish."

Juan Sabate

Affiliation
GE Global Research Center

Position Title
Senior Principal Engineer

Last Degree from Virginia Tech
Ph.D.

Year
1994

Career Highlights

2000-Present Senior Principal Engineer for GE Research Center, Niskayuna, NY

1997-2000 Senior Member of Research Staff for Philips Research, Briarcliff, NY

1994-1997 R&D Engineer for Hewlett Packard, Barcelona, Spain

1994-1997 Associate Professor at Ramon Llull University, Barcelona, Spain

"I am extremely proud of my work with CPES. My formation in the center set the foundation of my career learning from the top experts on power electronics and contributing to industrial partners' research projects. When I started, CPES (then VPEC) was already one of the best power electronics groups emerging in the U.S.. The center has continued growing and consolidated top-level contributions in the power electronics field. CPES accomplishments are a reference for power electronics research and people educated in CPES are part of the best power electronics teams in companies and universities all over the world."

Wei Tang

Affiliation
Delta Electronics, Inc.

Position Title
Director of R&D

Last Degree from Virginia Tech
Ph.D.

Year
1993

Career Highlights

- Developed and coded a general optimization program, which passed government certification and has been used by many graduate students, while studying as a master's student at Tsinghua University
- Developed the small-signal model for Charge Control and Average Current-Mode Control, and was the first person to apply Charge Control to CC mode Flyback PFC circuits while studying as a Ph.D. student at CPES
- Worked on very high density and integrated power supplies while working at Bell Labs
- Co-developed the world's first 1/16 brick dc-dc converter at Synqor
- Helped to establish Delta's first business unit in mainland China, which reached one hundred million U.S. dollars in annual revenue, while working as R&D Director for Delta dc-dc business unit
- Published 18 journal and conference papers, obtained 2 U.S. patents
- Translated sixteen English literature books as an English-Chinese language translator which, combined, have sold over 500,000 copies up to now

"I joined CPES (then VPEC) in April 1988 as a Ph.D. student, and spent the best five and a half years of my life at Virginia Tech. I am so fortunate to have had Dr. Lee as my advisor. Not only did his teachings guide my graduate studies, they are still helping my professional career to this day. During my studies at Virginia Tech, I had the opportunity to work with many of the best minds in the field of power electronics. I also met and married my dear wife there, and Dr. and Mrs. Lee were kind enough to host our wedding at their home."

Zhuxian "Nicole" Xu

Affiliation
Ford Motor Company

Position Title
Research Engineer

Last Degree from Virginia Tech
M.Sc.

Year
2010

Career Highlights

2013 Graduated from CURENT, the University of Tennessee, Knoxville with a Ph.D. degree

2014 Joined Ford Motor Company as power electronics research engineer. Led R&D projects to make electrified vehicles more efficient, more sustainable, and more intelligent. Led collaboration efforts between Ford and universities to develop disruptive technologies and to transform university researches into industry business needs and competitive advantages. Invented 25 patents.

2019 Served as CPES Industry Advisory Board member

2020 Served as Associate Editor for IEEE transactions on Transportation Electrification

" Two years at CPES is not long, but the knowledge, teamwork, critical thinking, and innovative spirit that I learned here have a profound impact on my life and lay the foundation for my further academic and professional advancement. As both a former CPES student presenting my research ideas to the industry and an industry member seeking for innovative solutions and cutting-edge technologies from CPES team, I truly appreciate the CPES industry consortium that bridges the university research and industry applications."

Sam Ye

Affiliation
LiteOn Technology Corporation

Position Title
Associate VP of Technical Sales and Marketing

Last Degree from Virginia Tech
Ph.D.

Year
2000

Career Highlights

- Senior R&D Engineer and Project Leader in GE Global Research Center
- Director of China R&D Center, LITEON Power Group, a worldwide #2 Power Supply Company.
- Associate VP of Engineering Organization, LITEON High Power BU
- Associate VP of Technical Sales and Marketing, LITEON USA

"Looking back on my career advancements, I'm always thankful for the CPES unique trainings, including power electronics courses, 5244, 5254, 5274. They are so unique, so classical, and prepared so many world-class power designers; Leadership training, such as serving in student council, organizing annual seminar, etc. As one of the world's largest industry consortia in a research lab, CPES really prepared us to have a good start and great professional networking in the industry from day one."

Jinfa "Alpha" Zhang

Affiliation
Delta Electronics (Shanghai) Design Center

Position Title
Director

Title at Virginia Tech
Visiting Professor

Year
1995, 1998

Career Highlights

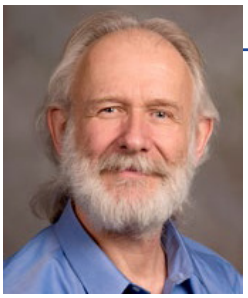
1991	Graduated and received PH.D. Degree from Zhejiang University
1991-1998	Associate Professor in Electrical Engineering Department of Zhejiang University, as vice director of Power Electronics Institute at Zhejiang University and vice director of State Key Lab on Power Electronics
1995 & 1998	Visiting professor in CPES/Virginia Tech
1999-2001	Assistant Director of Delta Power Electronics Center
2002-Now	Founder and Director of Delta Shanghai Design Center
2007-Now	Founder and Director of Delta Hangzhou Design Center
2011-2018	Vice-President of China Power Supply Society
2018-Now	Chief Supervisor of China Power Supply Society

"My staying and the experience in CPES is invaluable to my professional career, and it gave me an opportunity to learn the comprehensive knowledge of advanced power electronics, cutting-edge technology researches, as well as how to achieve challenging goals. The extensive industry collaboration at CPES had inspired me to change my career from academics to industry for technology advance and design innovation in the area of power electronics."

THE CPES TEAM

POWERED BY OUR PEOPLE

Faculty



Dushan Boroyevich

CPES Director

University Distinguished Professor

Associate Vice President for Research and Innovation in Energy Systems

Dushan Boroyevich received a Dipl.Ing. degree from the University of Belgrade in 1976 and a M.S. degree from the University of Novi Sad in 1982, in what used to be Yugoslavia. He received a Ph.D. degree in 1986 from Virginia Tech. From 1986 to 1990, he was an assistant professor and director of the Power and Industrial Electronics Research Program at the University of Novi Sad. Since 1990, he has been with the Bradley Department of Electrical and Computer Engineering at Virginia Tech.

Prof. Boroyevich is a member of the US National Academy of Engineering and is the recipient of 4 honorary professorships and numerous other awards. His research interests include electronic power distribution systems, multi-phase power conversion, power electronics systems modeling and control, and integrated design of power converters. He has graduated almost 50 Ph.D. and 50 M.S. students, and has co-authored with them around 1,000 technical publications and 20 patents.

Rolando Burgos

Professor

Rolando Burgos received the B.S. on Electronics Engineering, the Electronics Engineering Professional Degree, and the M.S. and Ph.D. degrees in Electrical Engineering from the University of Concepción, Chile, in 1995, 1997, 1999, and 2002 respectively. In 2002, he joined CPES as Postdoctoral Fellow, becoming Research Scientist in 2003 and Research Assistant Professor in 2005. In 2009, he joined ABB Corporate Research in Raleigh, NC, where he was Scientist (2009–2010), and Principal Scientist (2010–2012). In 2010, he was appointed Adjunct Associate Professor in the Electrical and Computer Engineering Department at North Carolina State University at the Future Renewable Electric Energy Delivery and Management (FREEDM) Systems Center. In 2012, he returned to Virginia Tech as associate professor, earning an early-decision tenure in 2017, and being promoted to professor in 2020. His research interests include high-power density wide-bandgap semiconductor-based power conversion, packaging and integration, electromagnetic interference (EMI) and electromagnetic compatibility (EMC), multi-phase multi-level power converters, modeling and control, grid power electronics systems, and the stability of ac and dc power grids.

Christina DiMarino

Assistant Professor

Christina DiMarino received her M.S. and Ph.D. degrees in electrical engineering from Virginia Tech in 2014 and 2018, respectively. She was a Webber Fellow from 2012 to 2015, and a Rolls-Royce Graduate Fellow from 2016 to 2017. She has been an assistant professor in the ECE department at Virginia Tech since 2019. She is located in the Virginia Tech Research Center in Arlington, VA, where she helped establish and manage two new CPES laboratories. Her research interests include power electronics packaging, high-density integration, medium-voltage power modules, and wide-bandgap power semiconductors.

Dong Dong

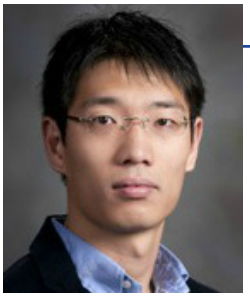
Assistant Professor

Dong Dong received a Bachelor of Science in 2007 from Tsinghua University in China and a Ph.D. in 2012 from Virginia Tech. Before joining CPES in 2018, he worked with GE's global research center for over five years on various power electronics and power system-related technologies. His research interests include high-frequency high-power conversion, application of wide-bandgap-based power electronics, power conversion systems for renewable energy systems, electric grids, and transportation applications.

Mona Ghassemi

Assistant Professor (Affiliate Faculty)

Mona Ghassemi received her M.S. and Ph.D. from the University of Tehran in 2007 and 2012, respectively. She was a postdoctoral fellow at NSERC/Hydro-Quebec/UQac from 2013 to 2015, and at the Electrical Insulation Research Center (EIRC) of the Institute of Materials Science (IMS) at the University of Connecticut from 2015 to 2017. Her research interests include dielectrics and electrical insulation materials and systems containing those in power electronics modules and systems, high-voltage technology, multiphysics modeling, plasma science, electromagnetic transients in power systems, and power system modeling.



Qiang Li

Associate Professor

Qiang Li received his B.S. in 2003 and M.S. in 2006 from Zhejiang University. Then in 2011, he received his Ph.D. from Virginia Tech. He started at Virginia Tech as a Research Assistant Professor in 2011 and was promoted to Assistant Professor in 2012. His research interests include high-density electronics packaging and integration, high-frequency magnetic components, high-frequency power conversion, distributed power systems, and renewable energy.

Guo-Quan Lu

Professor (Affiliate Faculty)

Guo-Quan Lu received a double-major B.S. in physics and materials science and engineering from Carnegie Mellon University in 1984, and a Ph.D. in applied physics from Harvard University in 1990. He then worked at Alcoa Technical Center for two years before joining Virginia Tech. Since 2003, Lu has been a professor in both the MSE and ECE departments. Lu's research activities and interests include packaging materials and assembly process development for interconnect, insulation, and magnetics of power electronics modules and converters.

Khai Ngo

Professor

Khai Ngo received his B.S. from California State Polytechnic University, Pomona, in 1979, and his M.S. and Ph.D. from the California Institute of Technology, Pasadena, in 1980 and 1984, respectively, all in electrical and electronics engineering. At CPES, he pursues technologies for reclamation and integration of renewal energy. He also coordinates CPES's outreach activities and the Consortium for High-Density Integration.

Yuhao Zhang

Assistant Professor

Yuhao Zhang studied physics at Peking University in China, where he received a B.S. in 2011. He went on to study electrical engineering at Massachusetts Institute of Technology in the United States, earning his M.S. in 2013 and his Ph.D. in 2017. He received the 2017 MIT Microsystems Technology Laboratories Doctoral Dissertation Seminar Award, the 2019 IEEE George E. Smith Award, and the 2021 NSF CAREER Award. His research interest is at the intersection of power electronics, micro/nano-electronic devices and advanced semiconductor materials, and the energy applications for data centers, electric vehicles, photovoltaics, and mobile applications, as well as the energy-related applications in extremely harsh environments.

Research Faculty

Igor Cvetkovic

Research Scientist and Technical Director

Igor Cvetkovic received a Dipl. Ing. Degree from University of Belgrade, Serbia in 2004. After working several years for the Electric Power Industry of Serbia, Igor joined the Center for Power Electronics Systems at Virginia Tech where he completed his M.S and Ph.D. degrees in 2010 and 2017, respectively. Igor is now a research scientist and technical director at CPES, and his research interests include electronic power distribution systems design and stability, as well as system-level modeling and control. Igor participated in numerous sponsored projects at CPES including Boeing, Newport News Shipbuilding, U.S. Department of Energy, and Office of Naval Research.

David Gilham

Lab Operations Director

David was born and raised in Southern California. He moved with his wife to Virginia in 2003 to pursue his B.S. degree in Electrical Engineering from Virginia Tech. Soon after graduation in 2007, he began as a staff researcher under the guidance of Dr. Fred Lee at CPES. In 2010 he was promoted to research faculty and began his M.S. study with concentration on packaging of POL converters using ceramic substrates and WBG devices. In 2012, David was promoted to Lab Operations Director and also graduated with his M.S. degree that same year.

Yi-Hsun Hsieh

Research Associate

Yi-Hsun (Eric) Hsieh received his B.S. and M.S. degrees in electrical engineering from the National Cheng Kung University in Taiwan in 2011 and 2013, respectively. He joined CPES as a Ph.D. student in 2014 and worked with Dr. Fred C. Lee. After receiving his Ph.D. degree in 2020, he continues working in CPES as a research associate.

Yi-Hsun Hsieh's research interests include resonant converter modeling, solid-state transformer, and modular multilevel converter. He holds one U.S. patent, and has published two journal papers and 18 conference papers.

Fred C. Lee

CPES Director Emeritus

University Distinguished Professor Emeritus

Fred C. Lee received his B.S. Degree in electrical engineering from the National Cheng Kung University in Taiwan in 1968, and his M.S. and Ph.D. degrees in electrical engineering for Duke University in 1972 and 1974, respectively. He has been Founder and Director of VPEC/CPES since 1983. His research interests include high-frequency power conversion, magnetics and EMI, distributed power systems, renewable energy, power quality, high-density electronics packaging and integration, and modeling and control.

Jun Wang

Research Assistant Professor

Jun Wang received his M.S. degree from Zhejiang University in 2007 and his Ph.D. degree from Virginia Tech in 2017. He won the Will Portnoy Prize Paper Award from IEEE Industrial Application Society in 2018. He was previously an electrical engineer with GE Power Conversion before joining CPES.

His research interests include wide-band gap power electronics, medium-voltage dc (MVDC) power distribution and protection systems, heavy duty transportation electrification, semiconductor fault prognostics and diagnostics, and biomedical power electronics.

Bo Wen

Research Assistant Professor

Bo Wen received his B.S. degree from Xi'an Jiaotong University, China, M.S. and Ph.D. degrees from Virginia Tech, USA, in 2006, 2011, and 2014 all in electrical engineering. He was a Research Associate with the University of Cambridge, Cambridge, and a Lecturer with the School of Electrical and Electronic Engineering, the University of Manchester, Manchester, U.K. Dr. Wen is currently a Research Assistant Professor at CPES. He received the 2017 Prize Paper Award in the IEEE Transactions on Power Electronics and the 2019 Outstanding Reviewer Award from the same journal. His current research interests include power conversion, power electronics systems modeling, and integration.

Staff

Audri Cunningham
Executive Assistant

Neil Croy
Lab Operations Associate

Angela Diamon
Intellectual Property Specialist

Dennis Grove
Industry Program Director

Na Ren
Business Director

Teresa (Trish) Rose
Procurement Officer

Matthew Scanland
Webmaster & Digital Content Specialist

Yan Sun
Accounting & Fiscal Associate

Visiting Scholars

Arthur Boutry
Ph.D. Student
INSA Lyon

Cyril Buttay
Centre National de la Recherche Scientifique Researcher
INSA Lyon

Chen Chen
Ph.D. Student
National Taiwan University of Science and Technology

Shih-Ming "Orion" Chen
Visiting Engineer
Lite-On Technology Corporation

Li Cheng
Lecturer
Chongqing University

Boran Fan
Post Doc
Tsinghua University

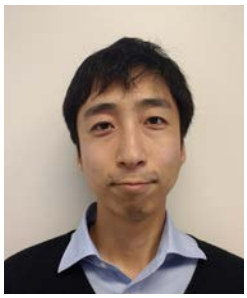
Takashi Hirota
Visiting Engineer
Komatsu Ltd.

Toshihiro Kai
Visiting Engineer
The Nissan Motor Company, Ltd.

Sang Min Kim
Visiting Engineer
Hyundai Mobis

Fei Li
Ph.D. Candidate
Xi'an Jiaotong University

Jingcun Liu
Ph.D. Candidate
Xi'an Jiaotong University



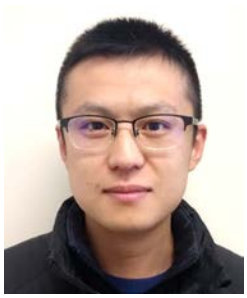
Takeya Okuno
Visiting Engineer
Panasonic Corporation

Phu Hieu Pham
Ph.D. Student
National Taiwan University of Science and Technology

Hans Hoffman Sathler
Ph.D. Student
IRT Saint Exupery

Takahide Tanaka
Visiting Engineer
Fuji Electric Co., Ltd

Chuanyun Wang
Visiting Engineer
Powerland Technology Inc.



Jizhe Wang
Ph.D. Student
Nagasaki University

Ming Xiao
Post Doc
Xidian University

Jiayu Xu
Ph.D. Student
North China Electric Power University

Zhichang Yuan
Professor
Tsinghua University

Sizhan Zhou
Post Doc
Xi'an Jiaotong University

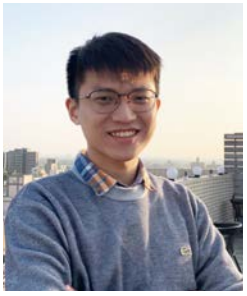
Graduate Students

Yijie Bai

Victoria Baker

Mark Cairnie

Yuliang Cao



Che-Wei Chang

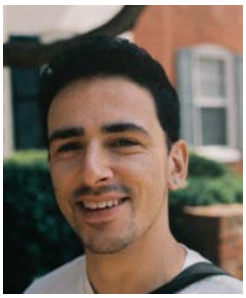
Xingyu Chen

Chao Ding

Ibrahim Eshera

Rimon Gadelrab

Md Abdul Gaffar



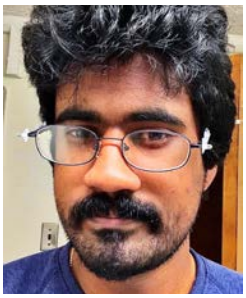
Jacob Gersh

Yugal Gupta

Jiewen Hu

Bhavin Jain

Feng Jin



Matthew Kallicharran

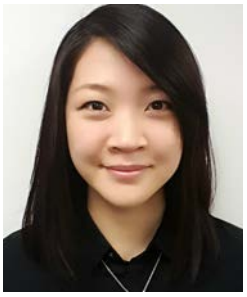
Daniel Knapp

Jack Knoll

Joseph Kozak

Bo Li


Qian Li


Virginia Li

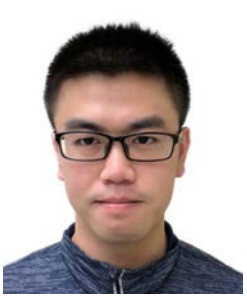

Zheqing Li

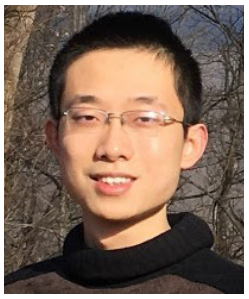

Qing Lin


Xiang Lin


Jian Liu


Xin Lou


Shengchang Lu


Yunwei Ma


Vladimir Mitrovic


Taha Moaz

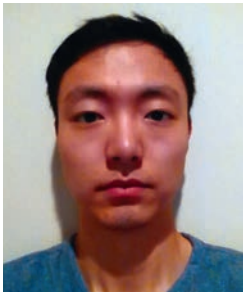

Slavko Mocevic


Jayesh Motwani


Paul Mourges


Sri Naga Vinay Mutyala


Ahmed Nabih


David Nam


Adhistira Naradhipa


Arash Nazari


Minh Ngo


Tam Nguyen


Carl Nicholas


Sungjae Ohn


Ripunjoy Phukan


Pranav Raj Prakash


Narayanan Rajagopal


Lakshmi Ravi

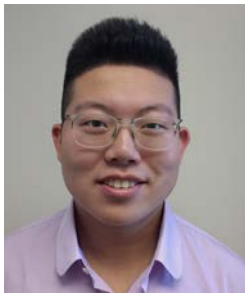

Moein Razavi


Yu Rong

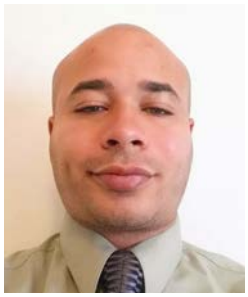

Keyue Shan


Gibong Son


He Song


Qihao Song


Matthias Spieler


Joshua Stewart


Keyao Sun


Maryam Tousi


Cong Tu


Biqi Wang


Boyan Wang

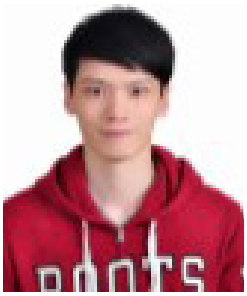

Le Wang


Shuo Wang


Sunbo Wang


Yue Xu


Ning Yan

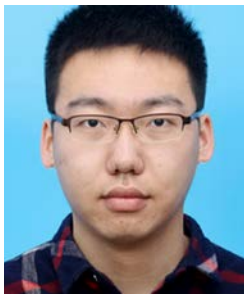

Sheng-Hung Yen


Jianghui Yu

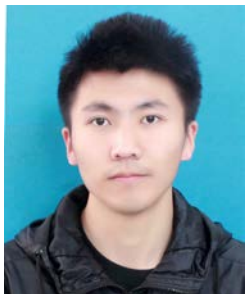

Tianlong Yuan


Ruizhe Zhang


Zichen Zhang


Chunyang Zhao


Tianyu Zhao

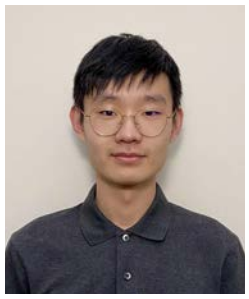

Xinchen Zhao


Feiyang Zhu

Undergraduate Students


Benjamin Alden


Ankit Bhardwaj


Junming Liang


Yizhi Ruan


Mina Shawky


Shashwat Singh


Zhengrui Wang

2020 Graduates

Chien-An Chen
Vicor Corporation

Junjie Feng
Monolithic Power Systems, Inc.

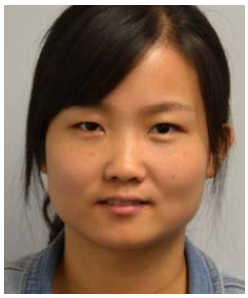
Yi-Hsun Hsieh
Virginia Tech

Zhengrong Huang
Analog Devices, Inc.

Lanbing Liu
Ansys, Inc.

John Noon
Moog Inc.

Rebecca Rye
Dominion Energy, Inc.



Ye Tang
Analog Devices, Inc.

Ning Yan
Virginia Tech

Lujie Zhang
Dialog Semiconductor PLC

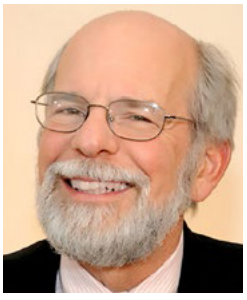
Advisory Boards

Scientific Advisory Board (SAB)

The CPES SAB is a critical part of the governing structure providing key insights on the technological direction of the center. Consisting of leading global researchers and managers of research programs in areas related to power electronics, these experts observe the status of CPES research and education programs and provide critical feedback to CPES leadership.

Anant Agarwal
Ohio State University

Johan Enslin
Clemson University



John Kassakian
Massachusetts Institute of Technology

Leo Lorenz
European Center for Power Electronics

Robert Steigerwald
GE Global Research (retired)

Industry Advisory Board (IAB)

The primary role of the IAB is to represent the interests of Industry Members in the CPES research programs as well as advise the CPES director and faculty members on industry trends, key challenges, and programmatic matters.

Pietro Cairoli
ABB, Inc.

Henry Zhang
Analog Devices, Inc.

Kevin Rhatigan
Aurora Flight Sciences

Ismail Agirman
Carrier Corporation

Shengli (Catherine) Huang
CRRC Zhuzhou Institute Co., Ltd.

Peter Barbosa, IAB Chair
Delta Electronic

Hongrae Kim
Eaton

Rui Zhou
EnerSys

Peter Xu
Flextronics

Chingchi Chen
Ford Motor Company

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GE Aviation

Satish Prabhakaran
GE Global Research

Colin Davidson
GE Grid Solutions

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David Zhou
Innoscience (Zhuhai) Technology

Gary Hua
Inventronics (Hangzhou), Inc.

Qiuyan Huang
Jiangsu Wanbang Dehe New Energy Technology Co. Ltd.

Sam Ye
LITE-ON Technology

Thomas Byrd
Lockheed Martin Corporation

Cory Arnold
Maxim Integrated Products

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Heath Kouns
Moog, Inc.

Alex Yang
Murata Manufacturing Co., Ltd.

Gene Sheridan
Navitas Semiconductor

Dinesh Ramanathan
NexGen Power Systems

Yasuaki Hayami
Nissan Motor Co., Ltd.

Zhenxia Shao
NR Electric, Ltd.

Kevin Kemp
NXP Semiconductors

Jaume Roig Guitart
ON Semiconductor

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OPPO

Robert Galli
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Ming Xu
Powerland Technology, Inc.

Sriram Chandrasekaran
Raytheon Technologies

Thomas Plum
Robert Bosch GmbH

Navid Zargari
Rockwell Automation

Anurag Jivanani
Schneider Electric IT Corporation

Arturo Pizano
Siemens Corporate Technology

Issac Chen
Silergy Corporation

Laszlo Balogh
Texas Instruments

Thomas Tainer
TMEIC Corporation

Kazuto Takao
Toshiba Corporation

Jian Li
Vertiv

Tamara Baksht
VisIC Technologies

Dheeraj (DJ) Jain
Würth Elektronik

Jianping Zhou
ZTE Corporation

HONORS & ACHIEVEMENTS

CELEBRATING TRANSFORMATION & MOMENTUM

National and International Honors

Dushan Boroyevich

Advisory Board for Journal of Power Electronics at The Korean Institute of Power Electronics

Editorial Board Member for Chinese Journal of Electrical Engineering, Beijing, China

Panelist on High-Power Density SiC-Based Modular Power Converters for Medium Voltage Applications, eGRID 2020, Aachen, Germany

Honorary Professorship, Tsinghua University, Beijing, China

Steering Committee, Power Electronics for Distributed Generation Systems Conference, Dubrovnik, Croatia, June 8-11, 2020

Steering Committee, eGrid Conference, Aachen, Germany, November 2-4, 2020

Rolando Burgos

Dean's Award for Excellence in Research, Virginia Tech

Chair, Technical Committee on Power and Control Core Technologies, IEEE Power Electronics Society

Administrative Committee Member, IEEE Power Electronics Society

Technical Committee Member of IEEE "Electric Ship Technologies Symposium," 2021

Christina DiMarino

Member-at-Large, IEEE Power Electronics Society Administrative Committee, 2020

Member, Power Conversion and Intelligent Motion Europe Conference Advisory Board, 2020

Topic Chair, IEEE Energy Conversion Congress and Exposition, 2020

Fred C. Lee

Chairman, IEEE Edison Medal Committee, 2020

Bo Wen

Outstanding Reviewer, IEEE Transactions on Power Electronics, 2020

Session Chair, IEEE Energy Conversion Congress and Exposition, 2020

Yuhao Zhang

Guest Editor, Semiconductor Science and Technology, Special Issue on GaN Technology for Next Generation Power Devices

Keynote Addresses

Fred C. Lee

"Next Generation of Switching Power Supplies," Chinese Electrotechnology Society Power Electronics Conference, August 21-23, 2020

"EV Charge Station," Xumishan Mobile Energy Grids Conference, Ningxia, China, September 22-23, 2020

"WBG-Based Magnetic Integration and EMI Mitigation," International Power Electronics and Motion Control, Energy Conversion Congress and Exposition-Asia, Nanjing, China, November 29-December 2, 2020

Invited Talks

Dushan Boroyevich

"Recent CPES Research Activity as Power Electronics Engineering Research Center," New-Generation PE Symposium, Tokyo, Japan, January 29, 2020

"Future Electronic Energy Systems," Faculty of Electrical Engineering and Computer, University of Zagreb, Zagreb, Croatia, February 11, 2020

"Research on High-Power-Density SiC-Based Modular Power Converters for High-Voltage Applications," HVDC Technologies Evolving for Future Systems, Xi'an, Shaanxi, China, November 6-9, 2020

Rolando Burgos

"A 16 kV PV Inverter Using Series-Connected 10 kV SiC MOSFET Devices," Invited Paper at IEEE International Electron Devices Meeting, December 2020

Christina DiMarino

"CPES Packaging Research," Army Research Laboratory, Adelphi, MD, January 2020

"CPES Packaging Research," University of Maryland, College Park, MD, January 2020

Dong Dong

"Modular High-Frequency SiC Power Conversion in High Power Applications," IEEE Power System Conference, Clemson University, March 11, 2020

"Modular High-Frequency SiC Power Conversion in High Power Applications," Forum on Power Electronics Technologies and Their Grid Applications, IEEE Industrial Electronics Society Nanjing Chapter, Southeast University, July 19, 2020

"Design of High-Frequency SiC Converter for Medium-Voltage High-Power Applications," Tutorial at the Energy Conversion Congress and Exposition-Asia, November 28, 2020

"High-Frequency SiC Converter for Medium Voltage High-Power Applications," Special Session at the Energy Congress and Exposition-Asia, November 30, 2020

"A Modular SiC-based High-Frequency Three-Phase Inverter System for MV Applications," Joint workshop of IEEE Power Electronics Society Beijing SBCs, December 7, 2020

Fred C. Lee

"Sustainable Energy and Power Electronics," ETH Zurich, Switzerland, January 24, 2020

"Next Generation of Power Supplies – from Design to Manufacturing," 3-hour Seminar, Asian Ph.D. Program, Xi'an, China, August 20, 2020

Qiang Li

"Integrated Planar Magnetic Components for High-Frequency Resonant Converters," European Center for Power Electronics Workshop on 'Magnetic Components in Power Electronics', Grenoble, France, February 19-20, 2020

"Common Mode Noise Reduction for High-Frequency PFC with Integrated PCB Winding Inductor," European Center for Power Electronics Workshop on 'Magnetic Components in Power Electronics', Grenoble, France, February 19-20, 2020

Yuhao Zhang

"Ruggedness of SiC and GaN Power Transistors in Switching Based Tests," Joint Symposium: State-of-the-Art Program in Compound Semiconductors, Electrochemical Society, Fall 2020 PRiME Meeting, October 2020

"Emerging WBG/UWBG Power Semiconductor Devices: Silvaco TCAD Enabled Designs and Applications," Silvaco UseRs Global Events, October 2020

"Emerging (Ultra-) Wide-Bandgap Power Devices on the Horizon," PowerAmerica Summer Wide-Bandgap Workshop, August 2020

"Emerging (Ultra-) Wide-Bandgap Power Devices on the Horizon," IEEE Power Electronics Society Young Professional Webinar, July 2020

"(Ultra-) Wide-Bandgap Materials and Devices: Reshaping the Power Electronics Landscape," IEEE Electron Device Society Silicon Valley/San Francisco Chapter Seminar, June 2020

Prize Paper Awards

Sungjae Ohn, Jianghui Yu, Paul Rankin, Bingyao Sun, Rolando Burgos, Dushan Boroyevich, Harish Suryanarayana, and Christopher Belcastro

"Three-Terminal Common-Mode EMI Model for EMI Generation, Propagation, and Mitigation in a Full-SiC Three-Phase UPS Module," IEEE Transactions on Power Electronics, Vol. 34, No. 9, pp. 8599-8612, September 2019

Shuo Wang, Hongfei Wu, Fred Lee, Qiang Li

William Portnoy Award Prize Paper Award, "Integrated Matrix Transformer with Optimized PCB Winding for High-Efficiency High-Power-Density LLC Resonant Converter," 2019 IEEE Energy Conversion Congress and Exposition, Baltimore, MD, pp. 6621-6627, September 29-October 3, 2019

Ahmed Nabih, Qiang Li, Fred. C. Lee

Best Paper Award, "3 kW Power Supply Design with Easy Manufacturability for 48 V Bus Power Architecture," IEEE Power Electronics Society 2020 Virtual Open Computer Project Future Technologies Symposium, May 15, 2020

Dong Dong, Ravieskhar Raju, Govardhan Ganireddy, Mohammed Agamy

"A Rotational Control in Medium-Voltage Modular Solid-State Transformer Based Converter Systems," IEEE Transactions on Industry Applications, 2019

Jian Liu, Dong Dong, Di Zhang

"Control of Hybrid Modular Multilevel Converter and its Capacitor Voltage Balancing," IEEE International Power Electronics and Motion Control Conference (Energy Conversion Congress and Exposition-Asia), 2020

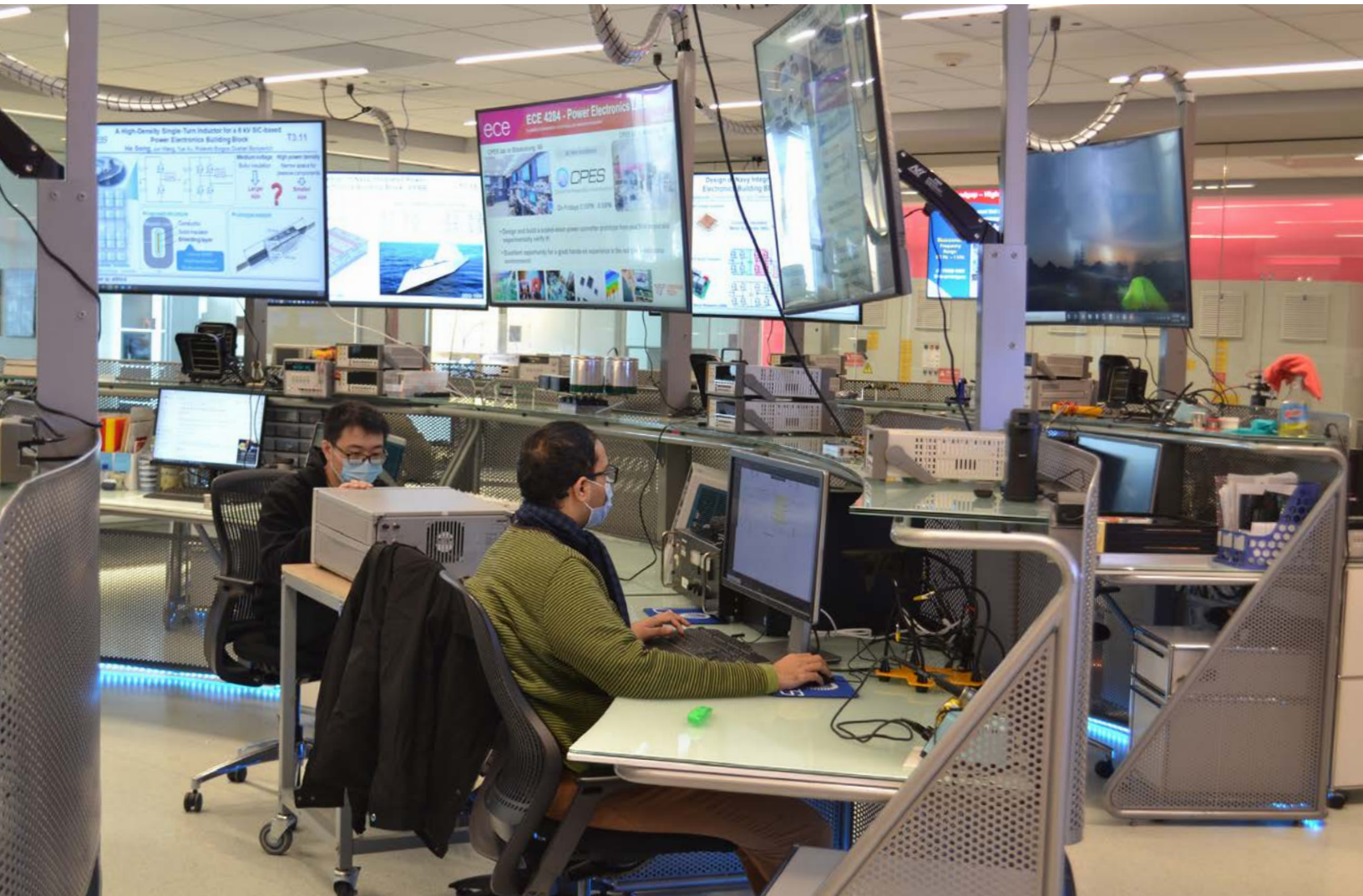
Yuhao Zhang, Min Sun, Josh Perozek, Zhihong Liu, Ahmad Zubair, Daniel Piedra, Nadim Chowdhury, Xiang Gao, Kenneth Shepard, Tomas Palacios

George Smith Award, "Large-Area 1.2 kV GaN Vertical Power FinFETs With a Record Switching Figure of Merit," 2019 IEEE Electron Devices Society, IEEE Electron Device Letters, Vol. 40, No. 1, pp. 75-78, January 2019

Student Awards and Achievements

Joseph Kozak

Virginia Tech Graduate Student of the Year Award, Electrical and Computer Engineering Department, Virginia Tech



PUBLICATIONS

WORKING TOWARDS TOMORROW

Transactions Papers

A Novel Filter Structure to Suppress Circulating Currents Based on the Sequence of Sideband Harmonics for High-Power Interleaved Motor-Drive Systems

Sungjae Ohn, Hyun-Sam Jung, Dushan Boroyevich, Seung-Ki Sui

IEEE Transactions on Power Electronics, Vol. 35, Issue 1, January 2020, pp. 853-866

Single-Stage High-Efficiency 48/1 V Sigma Converter with Integrated Magnetics

Mohamed Ahmed, Chao Fei, Fred Lee, Qiang Li

IEEE Transactions on Power Electronics, Vol. 67, Issue 1, January 2020, pp. 192-202

Small-Signal Modeling and Stability Prediction of Parallel Droop-Controlled Inverters Based on Terminal Characteristics of Individual Inverters

Zeng Liu, Jinjun Liu, Dushan Boroyevich, Rolando Burgos

IEEE Transactions on Power Electronics, Vol. 35, Issue 1, January 2020, pp. 1045-1063

Superjunction Power Transistors with Interface Charges: A Case Study for GaN

Yunwei Ma, Ming Xiao, Ruizhe Zhang, Han Wang, Yuhao Zhang

IEEE Journal of the Electron Devices Society, Vol. 8, January 2020, pp. 42-48

A GaN-Based DC-DC Module for Railway Applications: Design Consideration and High-Frequency Digital Control

Minfan Fu, Chao Fei, Yuchen Yang, Qiang Li, Fred Lee

IEEE Transactions on Industrial Electronics, Vol. 67, Issue 2, February 2020, pp. 1638-1647

Additive Manufacturing of Spiral Windings for a Pot-Core Constant-Flux Inductor

Chao Ding, Shengchang Lu, Jim Moss, Joyce Mullenix, Yunhui Mei, Khai Ngo, Guo Lu

IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 8, Issue 1, March 2020, pp. 618-625

An Analytical Model for Predicting Turn-ON Overshoot in Normally-OFF GaN HEMTs

Joseph P. Kozak, Ansel Barchowsky, Michael Hontz, Naga Babu Koganti, William Stanchina, Gregory Reed, Zhi-Hong Mao, Raghav Khanna

IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 8, Issue 1, March 2020, pp. 99-110

Design and Experimental Validation of a Wire-Bond-Less 10 kV SiC MOSFET Power Module

Christina DiMarino, Bassem Mouawad, Mark Johnson, Meiyu Wang, Dushan Boroyevich, Rolando Burgos

IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 8, Issue 1, March 2020, pp. 381-394

Design, Analysis, and Discussion of Short Circuit and Overload Gate-Driver Dual-Protection Scheme for 1.2 kV, 400 A SiC MOSFET Modules

Keyao Sun, Jun Wang, Rolando Burgos, Dushan Boroyevich

IEEE Transactions on Power Electronics, Vol. 35, Issue 3, March 2020, pp. 3054-3068

Low-Loss Integrated Inductor and Transformer Structure and Application in Regulated LLC Converter for 48 V Bus Converter

Mohamed Ahmed, Ahmed Nabih, Fred Lee, Qiang Li

IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 8, Issue 1, March 2020, pp. 589-600

Optimal Design of MHz LLC Converter for 48 V Bus Converter Application

Yinsong Cai, Mohamed H. Ahmed, Qiang Li, Fred C. Lee

IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 8, No. 1, March 2020, pp. 495-505

State-Trajectory Control With Single-Cycle Response for Point-of-Load Converters

Virginia Li, Qiang Li, Fred Lee, Pei-Hsin Liu

IEEE Transactions on Industrial Electronics, Vol. 67, No. 4, April 2020, pp. 3157-3166

Comparison and Discussion on Shortcircuit Protections for Silicon-Carbide MOSFET Modules: Desaturation Versus Rogowski Switch-Current Sensor

Slavko Mocevic, Jun Wang, Rolando Burgos, Dushan Boroyevich, Marko Jaksic, Constantin Stancu, Brian Peaslee

IEEE Transactions on Industry Applications, Vol. 56, Issue 3, May 2020, pp. 2880-2893

10 kV SiC MOSFET Power Module with Reduced Common-Mode Noise and Electric Field

Christina DiMarino, Mark Johnson, Dushan Boroyevich, Rolando Burgos

IEEE Transactions on Power Electronics, Vol. 35, Issue 6, June 2020, pp. 6050-6060

Critical-Conduction-Mode-Based Soft-Switching Modulation for Three-Phase PV Inverters with Reactive Power Transfer Capability

Zhengrong Huang, Qiang Li, Fred Lee

IEEE Transactions on Power Electronics, Vol. 35, Issue 6, June 2020, pp. 5702-5713

Reduced Common-Mode Voltage PWM Scheme for Full-SiC Three-Level Uninterruptible Power Supply with Small DC-Link Capacitors

Jianghui Yu, Rolando Burgos, Dushan Boroyevich, Harish Suryanarayana

IEEE Transactions on Power Electronics, Vol. 35, Issue 8, August 2020, pp. 8638-8651

Improvement of TCAD Augmented Machine Learning Using Autoencoder for Semiconductor Variation Identification and Inverse Design

Kashyap Mehta, Sophia Raju, Ming Xiao, Boyan Wang, Yuhao Zhang, Hiu Yung Wong

IEEE Access, Vol. 8, August 2020, pp. 143519-143529

Equivalent Circuit Modeling of LLC Resonant Converter

Shuilin Tian, Fred Lee, Qiang Li

IEEE Transactions on Power Electronics, Vol 35, No. 8, August 2020, pp. 8833-8845

High-Density Current-Transformer-Based Gate-Drive Power Supply with Reinforced Isolation for 10 kV SiC MOSFET Modules

Jiewen Hu, Jun Wang, Rolando Burgos, Bo Wen, Dushan Boroyevich

IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 8, Issue 3, September 2020, pp. 2217-2226

Trap-Mediated Avalanche in Large-Area 1.2 kV Vertical GaN p-n Diodes

Jingcun Liu, Ming Xiao, Ruizhe Zhang, Subhash Pidaparthi, Cliff Drowley, Lek Baubutr, Andrew Edwards, Hao Cui, Charles Coles, Yuhao Zhang

IEEE Electron Device Letters, Vol. 41, Issue 9, September 2020, pp. 1328-1331

(Ultra)Wide-Bandgap Vertical Power FinFETs

Yuhao Zhang, Tomas Palacios

IEEE Transactions on Electron Devices, Vol. 67, Issue 10, October 2020, pp. 3960-3971

Heteromagnetic Swinging Inductor and its Application for Power Factor Correction Converters

Shengchang Lu, Chao Ding, Lanbing Liu, Yunhui Mei, Khai Ngo, Guo Lu

IEEE Transactions on Industry Applications, Vol. 56, Issue 5, October 2020, pp. 5292-5298

High-Scalability Enhanced Gate Drivers for SiC MOSFET Modules With Transient Immunity Beyond 100 V/ns

Jun Wang, Slavko Mocevic, Rolando Burgos, Dushan Boroyevich

IEEE Transactions on Power Electronics, Vol. 35, Issue 10, October 2020, pp. 10180-10199

DC-DC Converter Synthesis: An Inverse Problem

Ramanuja Panigrahi, Santanu Mishra, Avinash Joshi, Khai Ngo

IEEE Transactions on Power Electronics, Vol. 35, Issue 12, December 2020, pp. 12633-12638

Design and Assessment of External Insulation for Critical Components in a Medium-Voltage SiC-Based Converter via Optical Method

Chongxing Zhang, Yue Xu, Ming Dong, Rolando Burgos, Ming Ren, Dushan Boroyevich

IEEE Transactions on Power Electronics, Vol. 35, Issue 12, December 2020, pp. 12887-12897

Reducing Migration of Sintered Ag for Power Devices Operating at High Temperature

Dan Li, Yunhui Mei, Yunchang Xin, Zhiqiao Li, Paul K. Chu, Changsheng Ma, Guo-Quan Lu

IEEE Transactions on Power Electronics, Vol. 35, Issue 12, December 2020, pp. 12646-12650

Surge-Energy and Overvoltage Ruggedness of P-Gate GaN HEMTs

Ruizhe Zhang, Joseph Kozak, Ming Xiao, Jingcun Liu, Yuhao Zhang

IEEE Transactions on Power Electronics, Vol. 35, Issue 12, December 2020, pp. 13409-13419

Conference Papers

A General Carrier-Based Modulation and Capacitor-Voltage Balancing Method for Multilevel Matrix Converters (AC-AC Stacked Multicell Converters)

Boran Fan, Vladimir Blasko, Rolando Burgos, Dushan Boroyevich

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 1230-1235

The Optimal Design of a High-Temperature PCB-Embedded Transformer GaN-Based Gate-Drive Power Supply with a Wide-Input Range

Jiewen Hu, Bo Wen, Rolando Burgos, Dushan Boroyevich, Yonghan Kang, Hossein Dadkhah

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 1382-1389

20 MHz, Two-Phase Negative Coupled Inductor Design for Integrated Voltage Regulator in Smartphone Applications

Feiyang Zhu, Qiang Li, Fred Lee

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 181-187

A High-Density Single-Turn Inductor for a 6 kV SiC-based Power Electronics Building Block

He Song, Jun Wang, Yue Xu, Rolando Burgos, Dushan Boroyevich

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 1127-1134

A Power Hardware-in-the-Loop Testbench for Aerospace Applications

John Noon, He Song, Bo Wen, Rolando Burgos, Igor Cvetkovic, Dushan Boroyevich, Gernot Pammer

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 2884-2891

Active Voltage Balancing Embedded Digital Gate Driver for Series-Connected 10 kV SiC MOSFETs

Xiang Lin, Lakshmi Ravi, Slavko Mocevic, Dong Dong, Rolando Burgos

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 1611-1616

Analysis of Parastic Capacitors' Impact on Voltage Sharing of Series-Connected SiC MOSFETs and Body-Diodes

Xiang Lin, Lakshmi Ravi, Yuhao Zhang, Dong Dong, Rolando Burgos

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 208-215

Comprehensive Analysis of Models and Operational Characteristics of Piezoelectric Transformers

Le Wang, Rolando Burgos

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 1422-1429

Critical Conduction Mode-Based High-Frequency Single-Phase Transformerless PV Inverter

Gibong Son, Zhengrong Huang, Qiang Li, Fred Lee

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 3232-3237

Design Analysis for Current-Transformer Based High-Frequency Auxiliary Power Supply for SiC-Based Medium-Voltage Converter Systems

Ning Yan, Jiewen Hu, Jun Wang, Dong Dong, Rolando Burgos

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 1390-1397

Design and Analysis of Tunable Piezoelectric Transformer Based DC-DC Converter with AC Output Inductor

Le Wang, Rolando Burgos, Alfredo Carazo

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 1398-1403

Design and Test of a 6 kV Phase-Leg Using Four Stacked 1.7 kV SiC MOSFET High-Current Modules

Emma Raszmann, Keyao Sun, Rolando Burgos, Igor Cvetkovic, Jun Wang, Dong Dong, Dushan Boroyevich

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 1604-1610

Design-Oriented Equivalent Circuit Model for Resonant Converters

Yi-Hsun Hsieh, Fred Lee

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 91-97

Evaluation of Active Capacitor Bank for Floating H-Bridge Power Modules

Tam Nguyen, Bo Wen, Rolando Burgos, Dushan Boroyevich, Jacob Verhulst, David Vrtachnik, Mohamed Belkhayat

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 2014-2020

Improved V^2 Constant On-time Control with State Trajectory Control

Virginia Li, Qiang Li, Fred Lee

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 3031-3038

Operation and Control of a Matrix Converter in Current Control Mode with Voltage Boost Capability

Vladimir Blasko, Boran Fan, Mahmoud Chamie, Warren Chen, Rolando Burgos

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 3049-3059

Series-Capacitor Buck Converter with Soft Turn-On

Cong Tu, Rengang Chen, Khai Ngo

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 41-47

Single Stage EMI Filter for Server Power Supply

Shuo Wang, Yuchen Yang, Fred Lee, Qiang Li

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 2384-2391

Three-Phase Interleaved LLC Resonant Converter with Integrated Planar Magnetics for Telecom and Server Application

Rimon Gadelrab, Fred Lee, Qiang Li

2020 IEEE Applied Power Electronics Conference and Exposition (APEC), New Orleans, LA, USA, March 15-19, 2020, pp. 512-519

Control of Hybrid Modular Multilevel Converter and its Capacitor Voltage Balancing

Jian Liu, Dong Dong, Di Zhang

2020 IEEE Energy Conversion Congress and Exposition – Asia, August 17, 2020

Generalized Behavioral Models of Three-Phase Converters and Electric Machines for System-Level Study and Stability Assessment

Igor Cvetkovic, Dushan Boroyevich, Rolando Burgos

2020 IEEE 11th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Dubrovnik, Croatia, September 28-October 1, 2020, pp. 291-296

3D Commutation-Loop Design Methodology for a Silicon-Carbide Based 15 kW, 380:480 V Matrix Converter with PCB Aluminum Nitride Cooling Inlay

Victoria Baker, Boran Fan, Rolando Burgos, Vladimir Blasko, Warren Chen

2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, October 11-15, 2020, pp. 233-238

A 16 kV PCB-Based DC-Bus Distributed Capacitor Array with Integrated Power-AC-Terminal for 10 kV SiC MOSFET Modules in Medium-Voltage Inverter Applications

Lakshmi Ravi, Xiang Lin, Dong Dong, Rolando Burgos

2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, October 11-15, 2020, pp. 3998-4005

A Synchronous Distributed Control and Communication Network for SiC-Based Scalable Impedance Measurement Unit

Yu Rong, Jun Wang, Zhiyu Shen, Sizhan Zhou, Bo Wen, Rolando Burgos, Dushan Boroyevich

2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, October 11-15, 2020, pp. 5085-5090

AC Impedance Characterization of a PV Inverter with Grid-Forming Control

Rebecca Rye, Rolando Burgos, Ye Tang, Qing Lin, Dushan Boroyevich

2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, October 11-15, 2020, pp. 6179-6184

An 11 kV AC, 16 kV DC, 200 kW Direct-to-Line Inverter Building-Block Using Series-Connected 10 kV SiC MOSFETs

Lakshmi Ravi, Xiang Lin, Dong Dong, Rolando Burgos

2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, October 11-15, 2020, pp. 362-369

Control Technique for High-Frequency Soft-Switching Three-Phase Inverter Under Grid Fault Condition

Gibong Son, Zhengrong Huang, Qiang Li, Fred Lee

2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, October 11-15, 2020, pp. 5000-5006

Design and Evaluation of a Power Hardware-in-the-Loop Machine Emulator

John Noon, He Song, Bo Wen, Igor Cvetkovic, Gernot Pammer, Rolando Burgos

2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, October 11-15, 2020, pp. 2013-2019

Design of Insulation System in High-Frequency Auxiliary Power Supply for Medium-Voltage Applications

Rolando Burgos, Qin Chen, Ning Yan, Dong Dong

2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, October 11-15, 2020, pp. 3492-3499

Gate-Driver Integrated Junction Temperature Estimation of SiC MOSFET Modules

Slavko Mocevic, Vladimir Mitrovic, Jun Wang,
Rolando Burgos, Dushan Boroyevich, Marko Jaksic, Mehrdad Teimor

2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, October 11-15, 2020, pp. 3761-3768

Hard-Switched Overvoltage Robustness of p-Gate GaN HEMTs at Increasing Temperatures

Joseph P. Kozak, Ruizhe Zhang, Jingcun Liu, Qihao Song, Ming Xiao, Yuhao Zhang

2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, October 11-15, 2020, pp. 677-682

Hybrid Voltage Balancing Approach for Series-Connected 10 kV SiC MOSFETs for DC-AC Medium-Voltage Power Conversion Applications

Xiang Lin, Lakshmi Ravi, Dong Dong, Rolando Burgos

2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, October 11-15, 2020, pp. 3769-3775

Modular Filter Building Block for Modular full-SiC AC-DC Converters by an Arrangement of Coupled Inductors

Sungjae Ohn, Ripun Phukan, Dong Dong, Rolando Burgos, Dushan Boroyevich, Gopal Mondal, Sebastian Nielebock

2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, October 11-15, 2020, pp. 4130-4136

Operation and Control of Converters Having Integrated Capacitor Blocked Transistor Cells

Jianghui Yu, Rolando Burgos

2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, October 11-15, 2020, pp. 2625-2632

Pre-Charge, Discharge, and Mini-UPS Circuits in Auxiliary Power Network Architecture for 10 kV SiC-Based Power Electronics Building Block

Keyao Sun, Jun Wang, Xiang Lin, Rolando Burgos, Dushan Boroyevich

2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, October 11-15, 2020, pp. 950-954

Small-Signal Dynamic and High-Bandwidth Design of LLC Resonant Converters

Yi-Hsun Hsieh, Fred Lee

2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, October 11-15, 2020, pp. 6136-6143

High-Frequency Transformer Design with High-Voltage Insulation for Modular Power Conversion from Medium-Voltage AC to 400 V DC

Zheqing Li, Yi-Hsun Hsieh, Qiang Li, Fred C. Lee, Mohamed H. Ahmed

2020 IEEE Energy Conversion Congress and Exposition (ECCE), Detroit, MI, USA, October 11-15, 2020, pp. 5053-5060

Analysis of Impacts of Compensation Networks on Characteristics of Piezoelectric Transformers

Le Wang, Rolando Burgos

2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL), Aalborg, Denmark, November 9-12, 2020, pp. 1-7

Impact of Parasitic Capacitors on Cell Capacitor Voltage Balance in Power Converters Having Integrated Capacitor Blocked Transistor Cells

Jianghui Yu, Rolando Burgos

2020 IEEE 21st Workshop on Control and Modeling for Power Electronics (COMPEL), Aalborg, Denmark, November 9-12, 2020, pp. 1-6

Theses and Dissertations

Design and Evaluation of a Photovoltaic Inverter with Grid-Tracking and Grid-Forming Controls

Rebecca Rye

Thesis, February 20, 2020

Load-Indepedent Class-E Power Conversion

Lujie Zhang

Dissertation, February 21, 2020

Design and Processing of Ferrite Paste Feedstock for Additive Manufacturing of Power Magnetic Components

Lanbing Liu

Dissertation, May 13, 2020

Model, Design, and Control for Power Conversion in Wave Energy Converter System

Chien-An Chen

Dissertation, May 13, 2020

Development of a Power Hardware-in-the-Loop Testbench for Electric Machine and Drive Emulation

John Noon

Thesis, July 24, 2020

Accurate Small-Signal Modeling for Resonant Converters

Yi-Hsun Hsieh

Dissertation, September 21, 2020

SiC-Based High-Frequency Soft-Switching Three-Phase Rectifiers/Inverters

Zhengrong Huang

Dissertation, September 24, 2020

6.78 MHz Omnidirectional Wireless Power Transfer System for Portable Devices Application

Junjie Feng

Dissertation, November 9, 2020

High-Frequency Current-Transformer Based Auxiliary Power Supply for SiC-Based Medium Voltage Converter Systems

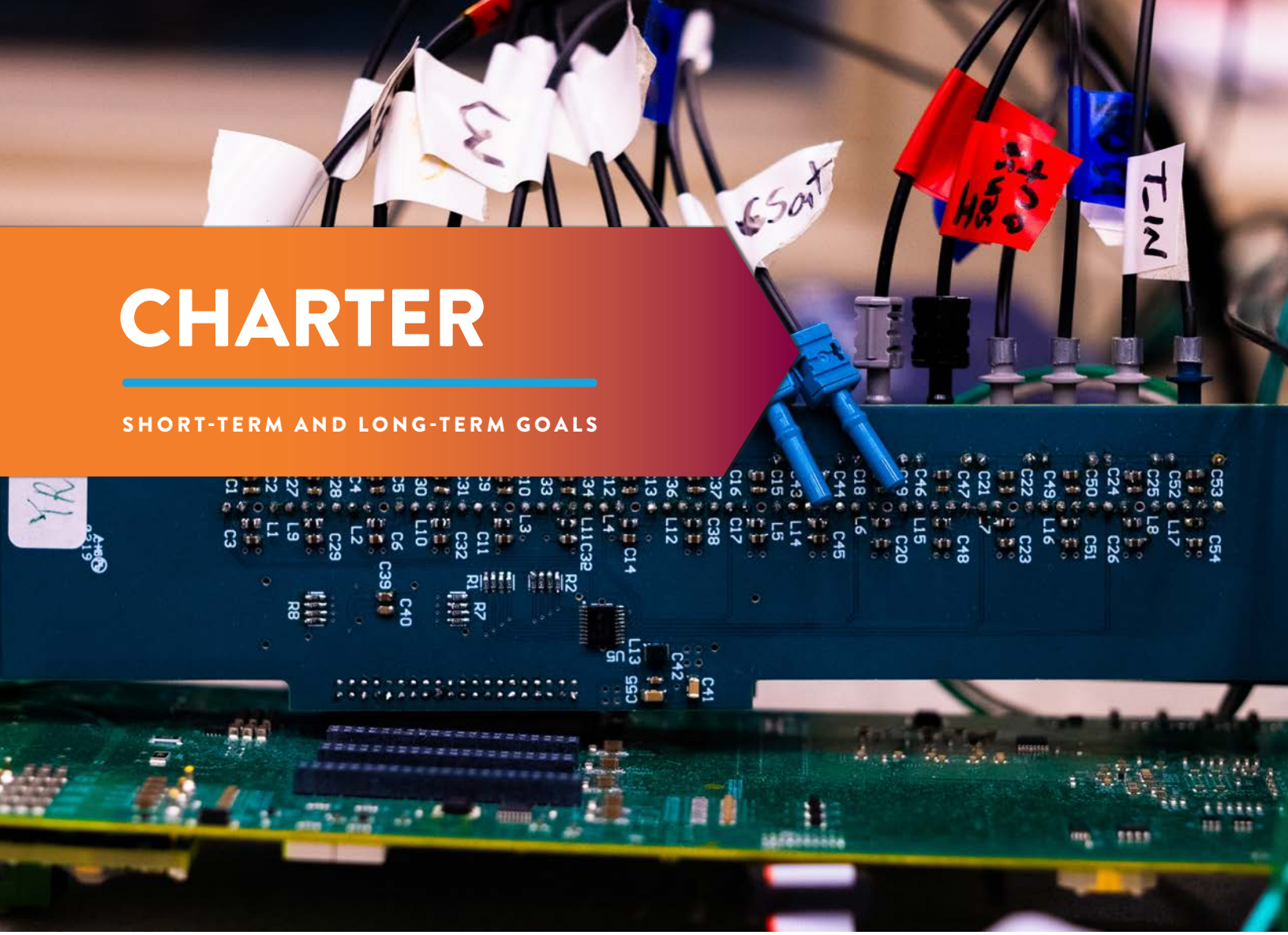
Ning Yan

Thesis, September 1, 2020

D-Q Frame Impedance Based Small-Signal Stability Analysis of PV Inverters in Distribution Grids

Ye Tang

Dissertion, December 14, 2020



CHARTER

SHORT-TERM AND LONG-TERM GOALS

Organization Charter

Short-Term and Long-Term Goals

Over the past four decades, CPES has developed promising new power electronics technologies, including new types of power semiconductor devices, high-frequency magnetics, soft-switching technologies that significantly reduce switching losses and electromagnetic interference (EMI), advanced materials and packaging technologies with planar interconnect processes, integrated sensors, and thermomechanical integration. These technologies collectively serve as the mainstay for the successful integration of modular building blocks into power electronics.

Industry adoption of the integrated power electronic module (IPEM) approach began in earnest in the early 2000s for applications such as power management solutions for the new generation of microprocessors, power supplies for the IT industry, electric/hybrid vehicles, and photovoltaic inverters, as well as variable-speed motor drives for applications ranging from industry automation and process control to home appliances. These core technologies offer the promise of higher performance at a lower cost with improved reliability. CPES is poised to extend these core competencies to a wide range of new and emerging applications.

We expect the emergence of wide-bandgap semiconductors to make it possible to operate converters at significantly higher switching frequencies, efficiency, and power density, and to operate at elevated temperatures. This new generation of wide-bandgap devices is poised to make a significant impact on the marketplace currently dominated by silicon power devices. These high-frequency and higher-temperature devices require advanced packaging technologies, together with high-temperature interface materials, passive components, and improved thermal management. CPES has unique strengths in these areas, and is a member of the "PowerAmerica" Institute led by North Carolina State University. This institute has been established as an alliance of eighteen corporations, five universities and two government labs. This program was initiated in early 2015 with a total budget of $140 million over five years aimed at developing wide-bandgap power services and associated system applications.

As the new generation of devices operate at significantly higher switching frequencies, power quality and electromagnetic interference and compatibility (EMI/EMC) have become increasingly important. CPES has pioneered a number of innovative technologies leading to significant improvements in power quality and EMI/EMC performance, and we plan to integrate these features directly into the next generation of power conversion systems. CPES researchers are well positioned to play a leading role in helping industry and government agencies find high-performance, cost-effective solutions.

With ever-increasing current consumption and clock frequencies, today's microprocessors are operating at very low voltages (one volt or less) and continuously switching between "sleep mode" and "wake-up mode" to conserve energy. This imposes a significant challenge to power delivery and management. Over the past 15 years, with the steady support of over 20 corporations, CPES developed a multi-phase voltage regulator (VR) module to power new generations of Intel microprocessors. This research project generated more than 30 U.S. patents, covering such areas as power delivery architecture; modularity and scalability; control and sensing; current sharing; integrated magnetics; and advanced packaging and integration. Today, every PC and server microprocessor in the world is powered with this multi-phase VR.

These technologies have been further extended to high-performance graphical processors, server chipsets and memory devices, networks, telecommunications, and all forms of mobile electronics, including smartphones. This research is structured as the Power Management Consortium (PMC) within the Center's Industry Consortium Program, which has over 80 participating members. The research scope of this mini-consortium has expanded in recent years to include power architecture and the management of data centers, telecommunications equipment, LED lighting, and PV converter/inverters.

Following the success of the PMC, CPES built upon its core strengths and launched two new mini-consortia in 2011; namely the mini-consortium on High-Density Integration (HDI), and the mini-consortium on Renewable Energy and Nanogrids (REN). HDI evolved as an extension of the early work supported under the NSF-ERC years to further develop IPEMs and system integration technology based on the new generation of wide-bandgap power semiconductors that were emerging. This research leverages the availability of wide-bandgap power semiconductors, as well as high-temperature passive components and ancillary functions. The switching frequency is pushed as high as component technologies, thermal management, and reliability permit. At the same time, the maximum component temperatures are pushed as high as component technologies, thermal management, and reliability permit.

REN on the other hand was created with the intent to consolidate the steady growth that CPES had in high-power applications, focusing on high-power and medium-voltage power conversion technologies to facilitate the integration of renewable energy sources, such as offshore wind farms, PV farms, and energy storage systems into the existing electrical grid. Later, due to the strong focus on the adoption of WBG devices in higher power applications, REN was relaunched as the Wide-Bandgap High-Power Converters and Systems (WBG-HPCS) mini-consortium to better reflect the expanded scope of work. Under this new

name, WBG-HPCS aims at consolidating and furthering the Center's strength surrounding WBG-based modular, multilevel power converters and high-power density, high-power converters for grid, industrial, and transportation applications. It continues to strengthen and grow expertise on electronic power systems—defined as electrical systems with a high penetration of power converters. CPES continues to lead investigations on the dynamic impact these converters have on power systems, targeting ac-dc low-voltage and medium-voltage distribution systems, up to high-voltage transmission systems.

CPES has established one of the largest university/industry partnership programs in the U.S. and has developed an innovative process for moving technology and intellectual property out of academic laboratories and into the marketplace. This process enables critical technologies developed by the center to permeate all forms of power electronics equipment and systems, and has profoundly affected the design and manufacturing process of the industry. With an increasing level of industry participation, more than 42 industry-funded graduate fellowships are made available to CPES students annually, with industry members serving as mentors in the students' research. This unique industry/university collaboration was cited by the NSF as a model ERC for its education/outreach program, industry collaboration, and technology transfer program. This program has continued to flourish since CPES graduated from the NSF ERC in 2008.

Resource Needs and Funding

CPES is a long-standing center, originally established in 1983 as VPEC (Virginia Power Electronics Center). Its continued support is expected to be consistent with the present sources of funding. The center is supported by both sponsored research, presently making up about $2.5 million/year, and industry member support, presently equal to an additional $6 million/year. Returned overhead is an additional source of support.

CPES has a Memorandum of Agreement (MOU) for the distribution of overhead. This agreement is reviewed periodically as new opportunities arise. The last MOU was signed by all parties in 2014.

Participation and Governance

CPES is made up of the highest level of faculty in the area of power electronics and power electronics systems. Top-caliber students from electrical engineering programs worldwide pursue their masters and doctorate degrees at CPES-Virginia Tech, and in turn are heavily recruited after graduation, many by our industry partners.

CPES is administratively established as a sub-organization under the College of Engineering. The Center Director, Dr. Dushan Boroyevich reports to the Dean, and together they identify initiatives to enhance the position and contributions of the center within the university, industry, and the world.

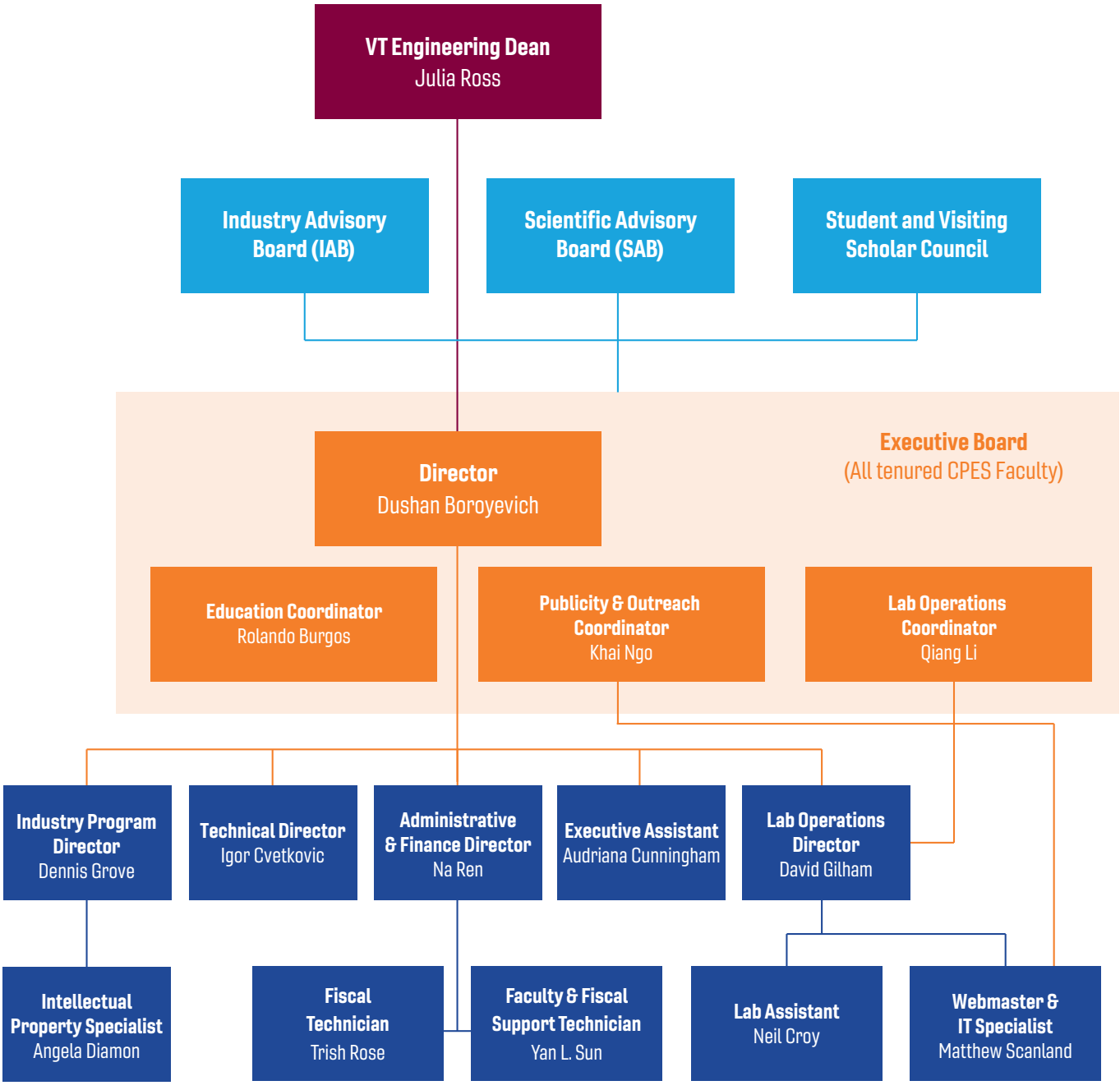
Director Dr. Dushan Boroyevich is supported in his role by Director Emeritus, Dr. Fred Lee. For daily operations of the center, Dr. Dushan Boroyevich is assisted by an executive board comprised of tenured faculty within CPES. Each faculty member plays a role as coordinator of one of four areas: Industry Consortium, Education, Publicity and Outreach and Lab Operations.

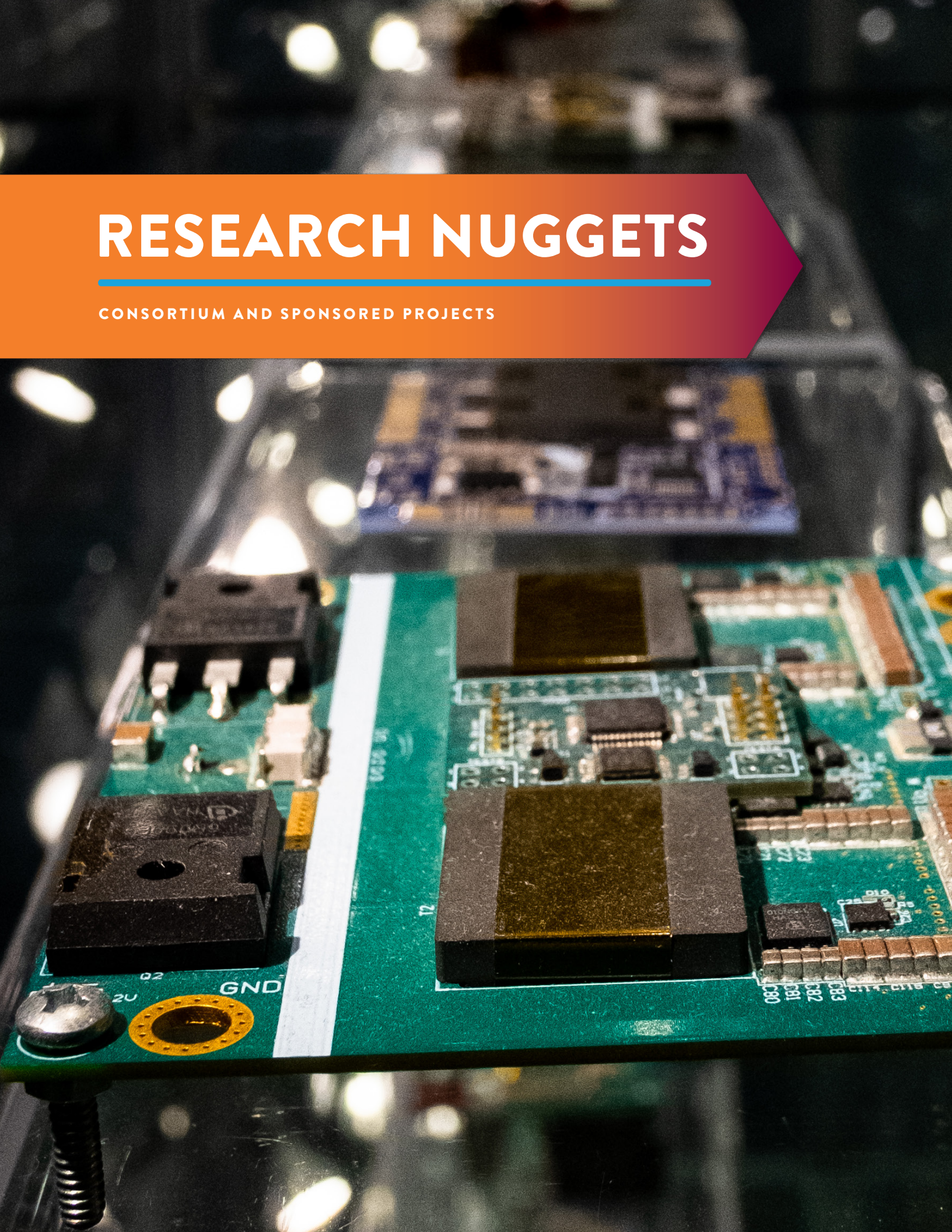
For long-term strategies, Dr. Boroyevich and Dr. Lee receive counsel from the CPES Industry Advisory Board (IAB) and the CPES Scientific Advisory Board (SAB).

The Industry Advisory Board represents industry interests and advises the CPES Director on programmatic matters. The board is made up of an elected chair and co-chair, representatives from all Principal Plus and Principal Members, and Associate Member representation equal to 20% of the total number of Associate Members, or one less than the total number of Principal-level Members.

The Scientific Advisory Board reviews the center's vision and strategic research plan, and offers critiques and guidance regarding the research vision and its programmatic approach to ensure that the center's research program maintains a focus on its long-term goals.

CPES Management Structure





RESEARCH NUGGETS

CONSORTIUM AND SPONSORED PROJECTS

High-Density Integration (HDI) Nuggets

High-Power Density Medium-Voltage Converter Integration via Active Electric Field Management

During the construction of a 6 kV Power Electronics Building Block (PEBB 6000), reliable and compact insulation design and realization is one of the important considerations. A good insulation system that can achieve PD free during normal operation not only helps to achieve an expected insulation lifetime and enhances the electric performance of the converter system, but also avoids any cascaded failure that may be initialized by some significant discharges. In Modular Multilevel Converter (MMC) topology, as we plan to stack four PEBBs up and thus hold a 24 kV system voltage, a widely used double-enclosure insulation strategy is applied for each of the PEBB units, as shown in Fig. 1. By connecting the inner enclosure with the local ground of each PEBB unit, there is only up to a 6 kV differential voltage between any adjacent components in the same PEBB. The remaining part of the system level voltage (up to 27 kV) is then pushed into the area between the inner and outer enclosures. Therefore, the insulation design can be decoupled into two levels (individual PEBB and system integration level), which leads to a more modular, flexible, and compact PEBB architecture. However, the area between the two enclosures needs some careful analysis and insulation design due to the 27 kV.

Focusing on the area between the two enclosures, two critical regions can be identified as shown in Fig. 2. As there are several uncontrolled sharp edges and corners in the heatsink on the bottom and along the small ICs of the PCBs on top, the insulation distance in air for these two regions must be very large (around 100 mm) in order to avoid discharges under 27 kV. Thus, the active Electric Field (E-field) management method, basically speaking the E-field-shielding technology, must be applied, in order to make the E-field distribution uniform and shrink the required minimum insulation distance in air. In this paper, the design methodology of shielding plate in MV power converters is proposed. Then fabrication of shielding plate and its experimental verification are demonstrated. With proper E-field shielding, the minimum insulation distance can be 30 mm, which leads to more than 50% volume reduction.

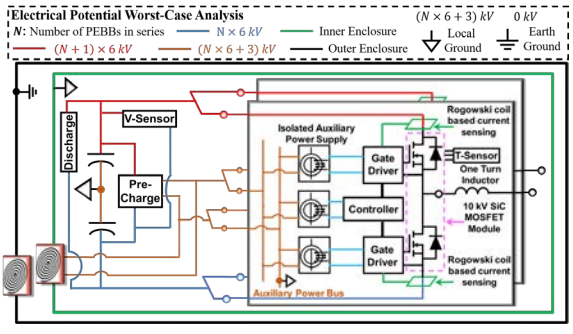


Fig. 1. Double-enclosure insulation system of a self-designed medium-voltage modular converter equipped with 10 kV SiC MOSFET.

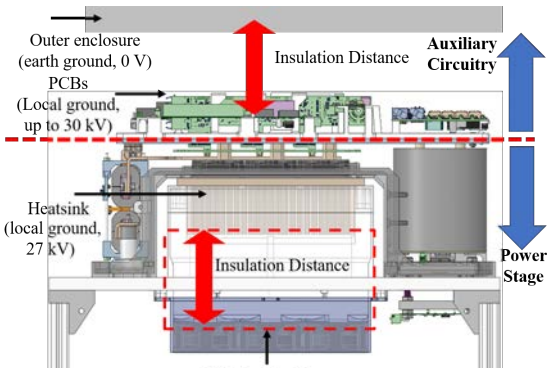


Fig. 2. Critical regions between two enclosures for insulation design.

Piezoelectric Transformer-Based High Step-Down Voltage-Ratio DC-DC Converter

In many medium- or high-voltage systems, such as the power electronic building blocks and some renewable energy applications, auxiliary power supplies are needed to provide the power for function blocks such as gate drivers, controllers, sensors, etc. For auxiliary power supplies fed from the dc bus, high-input voltage is faced. High step-down voltage ratio is needed to provide low output voltages. Wide input range is another requirement since a low startup voltage for the system is desired. The state-of-the-art commercial products are based on magnetic transformers, where bulky transformers with a large number of winding turns are needed. The height of the unit is limited by the high turns-ratio magnetic transformer.

By contrast, the piezoelectric transformer (PT), an electromechanical coupled transformer, whose equivalent circuit can be represented by the integration of a resonant tank and an ideal transformer, may provide an alternative solution. Among many types of PTs, the high-voltage Rosen-type PT features natural mechanisms for high-voltage insulation, high-transform ratio in a compact planar form, no coil winding, and no EMI source, providing an alternative solution for dc bus-fed, high step-down voltage-ratio auxiliary power supplies in medium- or high-voltage systems.

Fig. 1. presents the topology of the proposed converter. A full bridge is used to generate the ac voltage for the PT and to provide wider input regulation range compared to the half bridge. Since the PT steps down the voltage, a 1:1 planar magnetic transformer is used afterwards to provide the isolation since current commercial high-voltage PT is non-isolated, where the magnetizing inductance is utilized to improve the efficiency as well as provide load-independent voltage gain. A regulated buck-boost ac-dc stage is used to provide line-regulated output voltage. The control loop sits at the low-voltage side without crossing the high-voltage barrier.

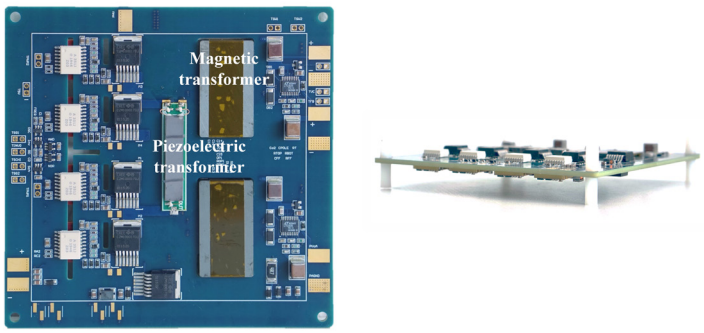


Fig. 2. shows the test board (10 cm × 10 cm × 1 cm), whose height is no longer limited by the transformers. Maximum output power is 5 W. Output voltage is regulated at 5 V for bus voltage ranging from 200 V to 1000 V.

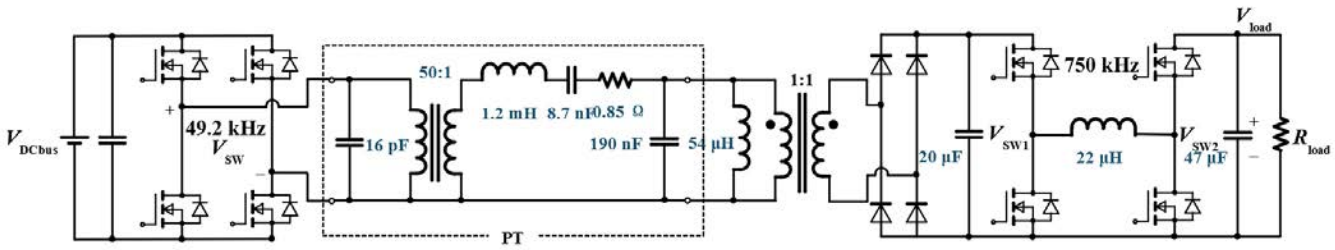


Fig. 1. Proposed PT-based high step-down voltage-ratio dc-dc converter.

Coupled Inductor Design for Multi-Phase PFC Converter

With recent advances in wide-bandgap (WBG) power semiconductor devices, namely SiC and GaN, we have witnessed significant improvements in efficiency and power density compared to the current practice of using silicon counterparts. Furthermore, with significant higher operating frequency, the integration of magnetic components with embedded windings in the printed circuit board (PCB) is feasible for coupled inductor. Design trade-offs, previously considered neither practical nor conceivable, can be realized, not only with significant gain in power density, but also with drastic improvements of EMI/EMC and manufacturability.

This research focuses on the design of PCB winding-based coupled inductor for multi-phase critical mode (CRM) PFC converter. First, the coupling coefficient is optimized by a trade-off of magnetic flux dc bias and switching frequency range. A higher coupling coefficient leads to a higher dc bias in the outer leg, which results in an increased core loss if an EI core structure is considered. As a contradictory point, the coupling coefficient should not be too small in order to avoid a large switching frequency range for CRM PFC converter. A coupling coefficient α=0.3 is selected based on minimizing the dc bias and switching frequency range in outer legs.

Second, improving common mode (CM) EMI noise reduction by balance technique is another highlight. A new PCB winding structure is proposed as shown in Fig. 1. CM noise is expected to be uniformly reduced in the frequency range of 150 kHz to 30 MHz.

Third, an improved coupled inductor design process is presented. The finite element analysis (FEA)-based Equivalent Elliptical Loop (EEL) model is employed for core loss calculation. Trade-offs of inductor loss and footprint are performed.

A positive coupled inductor for a 6.8 kW electric vehicle (EV) on-board charger is designed as an example. Fig. 2. shows the loss breakdown of the coupled inductor. The PFC converter is expected to have a peak efficiency over 98% and a power density of 2.7 kW/L. At the same time, CM noise is expected to be uniformly reduced with the proposed integrated coupled inductor.

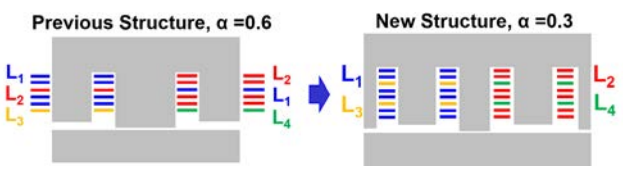


Fig. 1. Proposed PCB winding coupled inductor with PQ core structure.

Fig. 2. PCB winding coupled inductor loss breakdown.

High-Power Density 1 MHz 3 kW 400 V-48 V LLC Converter for Data Centers with improved Core Loss and Termination Loss

Power consumption of data centers has been increasing rapidly over recent years. Recently, 48 V power architecture has attracted more interest in data centers as it offers more efficient architecture. This paper focuses on the implementation of the dc-dc stage of a 3 kW power supply unit. Single-phase LLC topology is chosen as it can achieve soft switching, giving us the opportunity to push the switching frequency and increase the power density. This paper focuses on the magnetic design of the PCB-based transformer and resonant inductor of the LLC converter. The dimensional effects on core loss are discussed and evaluated. A matrix of two transformers implemented on UI core with rectangular core shape is proposed to minimize the eddy core loss of the transformer core. The termination of the secondary full-bridge rectifier is also optimized to reduce the conduction loss of the transformer.

Using a matrix transformer helps to reduce the conduction loss of the secondary winding and SR but also increases the core loss since all elemental transformers are subject to the same volt-sec. Hence, there is a trade-off between the conduction loss and core loss when it comes to designing a matrix transformer. Three candidates of Matrix transformer have been considered: a single transformer, two transformers, and four transformers. The three candidates are evaluated based on the total winding and core loss vs. footprint. The two-transformer solution was deemed better. The two elemental transformers are then integrated in a UI core structure. However, at 1 MHz and single secondary turn winding (High Volt-sec per turn). The transformer core suffers from dimensional effects like non-uniform flux and increased eddy core loss. In order to limit the eddy core loss, the transformer core is designed using a thin rectangular core instead of a round shape core. This method reduces the core loss by around 4 W.

The converter is implemented on 6-Layer PCB, 2 oz. copper. 35 mΩ-600 V GaN devices are used for the primary half-bridge, and 4 mΩ, 80 V GaN devices are used for the secondary center-tap rectifiers. Fig 1. shows the implemented PCB including primary and secondary devices and gate drivers and magnetics. The converter 11 mm profile has a power density of 700 W/in^3. Fig. 2. shows the tested efficiency of 98% at 54 output voltage

In summary, in this paper, the impact and importance of dimensional effects on core loss for a high-power transformer running at high frequency is discussed. Different candidates of matrix transformers are evaluated. a matrix of two transformers implemented on UI core with elongated core shape to reduce core's eddy loss. Prototype of the proposed converter is demonstrated. In the final paper, another part will be added to discuss the termination loss of SR and how to reduce it with optimized device layout.

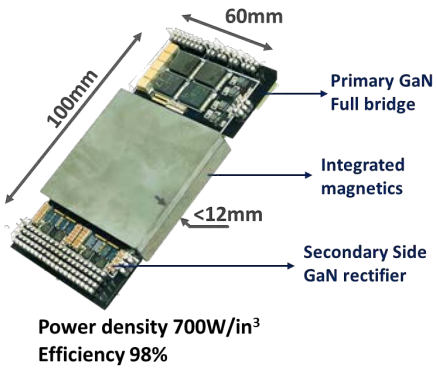


Fig. 1. Implemented 1 MHz 3 kW LLC.

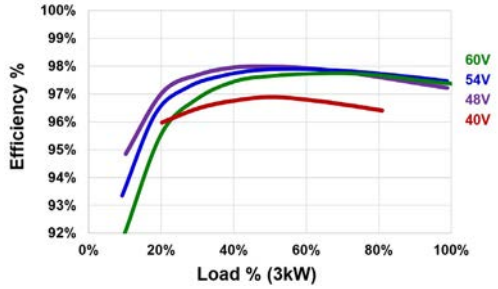


Fig. 2. Tested efficiency.

Packaging and High-Temperature Characterization of a 650 V, 150 A eGaN HEMT

Power devices based on wide-bandgap (WBG) semiconductor materials such as gallium nitride (GaN) present a significant growth opportunity for the power electronics industry because of the materials' high dielectric breakdown strengths, high electron mobilities, and good thermal conductivities. One way to further improve the metrics of power converters is to take advantage of the potential high-temperature capability of the wide-bandgap devices. However, there are few studies reported on the high-temperature capability of packaged GaN HEMTs.

In this work, a commercial 650 V, 150 A enchancement mode GaN (eGaN) HEMT from GaN Systems was packaged and characterized for its static properties at temperatures up to 250° C. The eGaN HEMTs studied in this work were purchased from GaN Systems with the part number of GS-065-150-1-D rated at 650 V, 150 A. Copper was the surface finish on all the gate, source, and drain pads, and the backside of the chip was finished with silver. Fig. 1. is a cross-sectional view of the package design. Silver sintering was used for attaching the device chip on direct-bond-copper substrate, and gold wire-bonding for interconnections. Fig. 2. shows the fabrication process of the high-temperature package.

The packaged device was tested at temperatures up to 250° C to determine the effects of temperature on its static characteristics. It survived multiple heating/cooling cycles between room temperature and 250° C as it underwent static testing on a curve tracer. Compared to the characteristics at room temperature, at 250° C, the threshold voltage was reduced by about 30%, the saturation current was down below 45% of the rated current, and the leakage current was increased by tens of times.

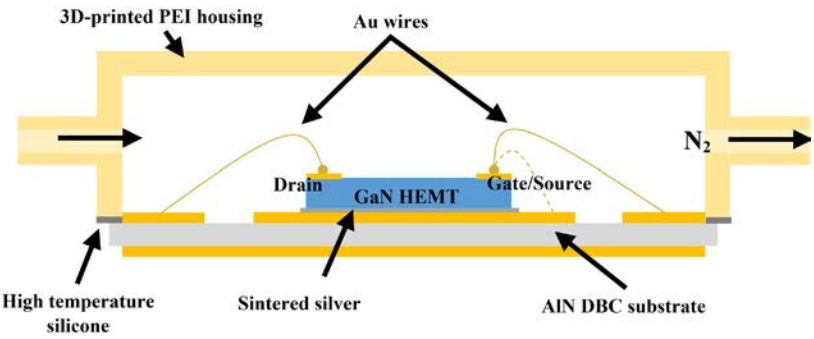


Fig. 1. Cross-sectional schematic of the high-temperature package for interconnecting and enclosing the eGaN HEMT.

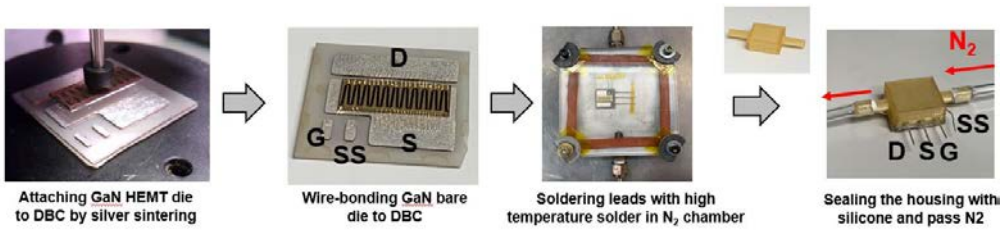


Fig. 2. Fabrication steps of the high-temperature package.

Dynamic Breakdown Voltage and Overvoltage Ruggedness of 600 V/650 V Commercial p-gate GaN HEMTs

This work develops a new method to measure the transient breakdown voltage (BV) of a non-avalanche device in ultra-short pulses, based on the unclamped inductive switching (UIS) setup. For the first time, the transient BVs of two types of 600/650 V enhancement-mode p-gate GaN high-electron-mobility transistors (HEMTs) are measured across the pulse duration from 25 ns (dv/dt > 100 V/ns) to 2 s. The BV is found to increase with the decreased pulse width up to 500 V higher than the static BV. This behavior is explained by the reduced buffer trapping and the resulted lower peak electric field in shorter pulses. Slightly different BV dependences on pulse width are observed in the two types of devices and the mechanisms are unveiled. Repetitive UIS tests are also conducted, revealing that this newly-found "dynamic BV" can provide GaN HEMTs additional overvoltage and surge energy margin in many power applications. These findings provide important new insights on the BV physics and ruggedness of GaN power HEMTs.

Two types of commercial p-gate GaN HEMTs with similar ratings are tested in this work, including the 650 V, 30 A-rated Schottky-type p-gate HEMT (SP-HEMT) and the 600 V, 31 A-rated hybrid-drain-embedded gate injection transistor (HD-GIT). The transient BV of the DUTs were measured in a pulse duration down to 25 ns for the first time based on the UIS test circuit Fig. 1. (a). Fig. 1. (b) shows the box plots of the BV vs. pulse width (from 25 ns to 2 s) at 25-125° C of the SP-HEMT, showing a consistent BV decrease from 1480±10 V to 950±10 V across 8 orders of magnitude in the pulse width at 25-125° C. Fig. 1. (c) shows the box plots of the BV vs. pulse-width at different temperatures of HD-GIT. The BV of the HD-GIT shows a much smaller variation compared to SP-HEMTs, dropping from 1180±5 V to 1095±5 V for the pulse width of 25 ns to 5 ms and remaining unchanged in longer pulses.

The "dynamic BV" can be explained by the dynamic filling of buffer traps. At zero bias, the acceptor-like buffer traps are partially filled. The high VDS will inject electrons into the buffer from the source or from the Si-substrate/transition-layer interface, inducing acceptor trap filling (Fig. 2. (a)). The ionized acceptor trap brings higher peak E-field locates at the drain side, resulting in smaller BV. The smaller "dynamic BV" range in the HD-GIT suggests less buffer electron trapping, which can be explained by the hole injection from p-gate and hybrid drain Fig. 2. (b).

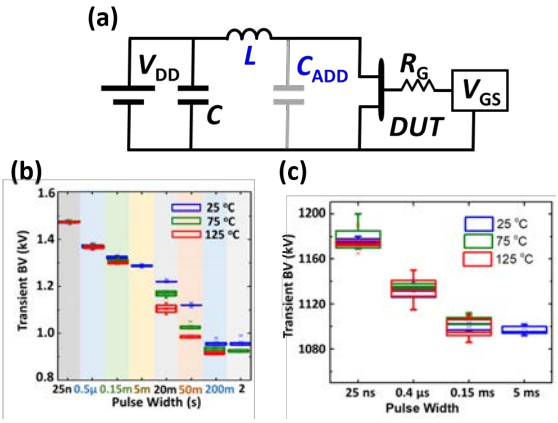


Fig. 1. (a) Test circuit & (b) and (c) BV spectrum vs pulse width.

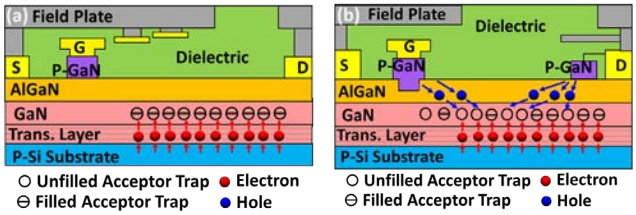


Fig. 2. Illustration of (a) SP-HEMT & (b) GIT.

Packaged Ga_2O_3 Schottky Rectifiers with Over 60 A Surge Current Capability

Ultra-wide-bandgap gallium oxide (Ga_2O_3) devices have recently emerged as the promising candidates for power electronics. However, the low thermal conductivity (kT) of Ga_2O_3 causes serious concerns on the electrothermal ruggedness of Ga_2O_3 devices. This work presents the first experimental demonstrations of the large-area Ga_2O_3 Schottky barrier diodes (SBDs) packaged in the bottom-side cooling and double-side cooling configurations, and for the first time, characterizes the surge current capabilities of these packaged Ga_2O_3 SBDs. Contrary to popular belief, Ga_2O_3 SBDs with proper packaging show high surge current capabilities. The double-side cooled Ga_2O_3 SBDs with a 3×3 mm^2 Schottky contact area can sustain a peak surge current over 60 A, as shown in Fig. 2., with the ratio between the peak surge current and the rated current comparable or even superior to that of commercial SiC SBDs. The key enabling mechanisms for this high surge current are the small temperature dependence of on-resistance, which strongly reduces the thermal runaway, and the double-side cooled packaging, which allows the heat extraction directly from the Schottky junction without the need for going through the low-kT bulk Ga_2O_3 chip. These results have removed some crucial concerns on the electrothermal ruggedness of Ga_2O_3 power devices and manifest the significance of their die-level thermal management.

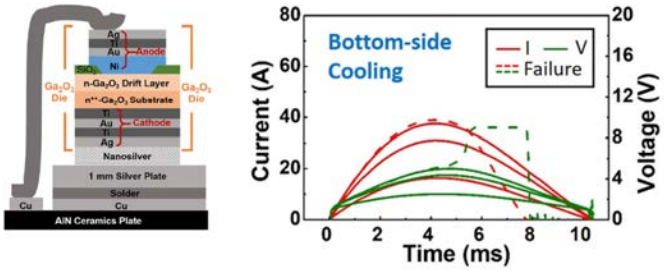


Fig. 1. Bottom-side cooling Ga_2O_3 Schottky diodes packaging & surge test result.

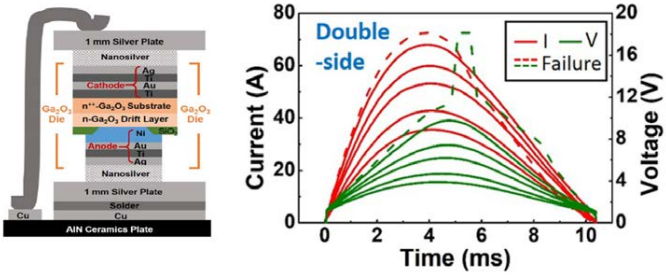


Fig. 2. Double-side cooling Ga_2O_3 Schottky diodes packaging & surge test result.

A Double-Side Cooled SiC MOSFET Power Module with Sintered-Silver Interposers

Planar, double-side cooled power modules are emerging in electric-drive inverters because of their low profile, better heat extraction, and lower package parasitic inductances. In a double-side cooled module, interposers are necessary for device top-side interconnections for routing and heat dissipation. The most commonly used material for interposers is solid copper (Cu). However, due to the high elastic modulus of copper and the coefficient of thermal expansion (CTE) mismatch between the copper and semiconductor materials, thermo-mechanical stresses are introduced under temperature cycling conditions, thus leading to a concern about the reliability of the double-side cooled modules. Molybdenum (Mo) has been proposed as an alternative solution to Cu thanks to a less CTE mismatch. However, Mo also has high elastic modulus and requires additional coatings to be compatible with soldering or sintering.

In this work, a porous interposer made of low-temperature sintered-silver (Ag) is introduced to reduce the thermo-mechanical stresses in the module. A double-side cooled half-bridge module consisting of two 1200 V, 149 A SiC MOSFETs shown in Fig. 1. was designed, fabricated, and characterized. The appearance and microstructure of sintered-Ag interposers are shown in Fig. 2. By using the sintered-Ag instead of solid Cu interposers, our simulation results showed that at a total power loss of 200 W, the thermo-mechanical stress at the most vulnerable interfaces (interposer-attach layer) was reduced by 42% and in the SiC MOSFET by 50% with a trade-off of only 3.6% increase in junction temperature. The sintered-Ag interposers were readily fabricated into desired dimensions without post-machining and did not require any surface finishing for die-bonding and substrate interconnection by silver sintering. The porous interposers were also deformable under a low force or pressure, which helped to accommodate chip thickness and/or substrate-to-substrate gap variations in the planar module structure, thus simplifying module fabrication. Experimental results on the electrical performance of the fabricated SiC modules validated the fabrication of a module design that employs the sintered-Ag interposers and all sintered-Ag joints for making high power-density converters with reliable operations at high junction temperatures.

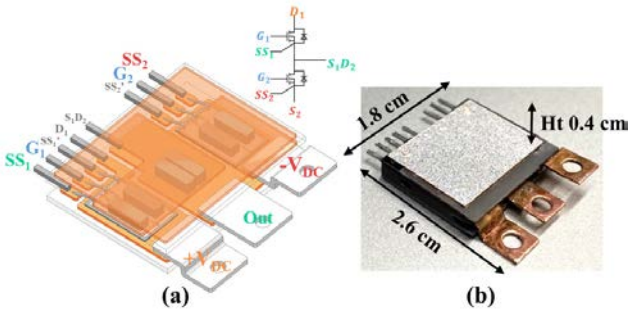


Fig. 1. (a) Layout design of the 1.2 kV, 149 A SiC MOSFET double-side cooled half-bridge module, and (b) the as-fabricated module.

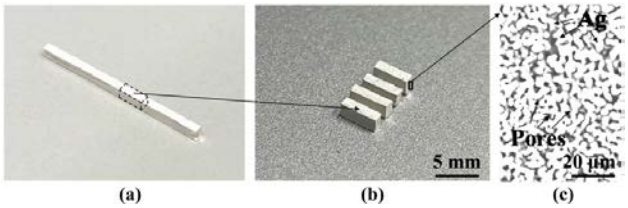


Fig. 2. (a) Sintered-Ag bar, (b) a few pieces of the cut interposers, and (c) a scanning electron microscope image showing the porous microstructure of sintered-Ag interposer.

Power Management Consortium (PMC) Nuggets

A WBG-Based 400/48 V LLC Converter with 99% Efficiency

The new generation of processors for CPU, GPU, and AI demand a significantly higher current level at 500 A-1000 A. To accommodate this much-increased power demand, the data center server rack must deliver 25-30 kW to server processors with a 48 V backplane power bus. The state-of-the-art, silicon-based power module is demonstrated at 96% efficiency and power density around 40-50W/in^3. In this paper, a WBG-based LLC converter is demonstrated with significantly improved efficiency and power density. Operating at 500 kHz switching frequency, the circuit topology and design practice is not without significant departure from the current practice. For example, a complicated transformer structure is broken down into three simple transformer structures that can easily be implemented using a form of 4-layer PCB. Furthermore, these magnetic components are integrated into a compact structure that is easy to manufacture. By adding two additional shielding layers into the 4-layer PCB, a 20 db reduction of common-mode noises is realized in the entire frequency spectrum of interest, from 150 KHz up to 30 MHz. A 3 kW 400/48 V dc-dc converter is demonstrated with a peak efficiency of 99% and a power density of 450 W/in^3 (28 kW/L) as shown in Fig. 1.

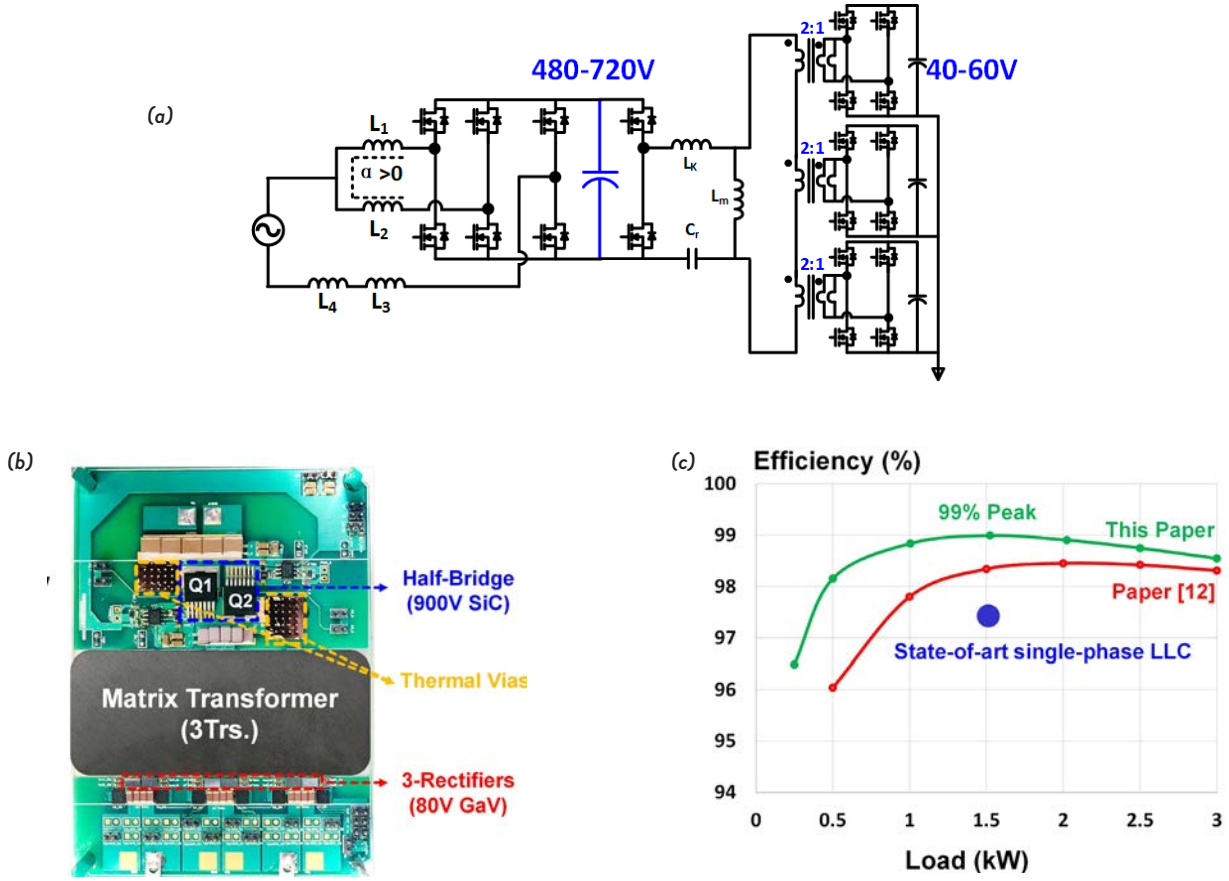


Fig. 1. (a) Circuit (b) Hardware prototype (c) Tested efficiency.

High-Frequency Transformer Design with High-Voltage Insulation for Solid-State Transformer (SST)

Due to the increasing use of cloud computing and big data, the power consumption of the data centers alone reached 10% of the total electrical power consumption in the world by the year 2020. Considering such a booming data center load development, high copper cost and conduction loss due to low voltage (480 V ac) power distribution outside the server hall need to be solved.

In the proposed system, medium-voltage SST is used as the distribution voltage in the data center to convert medium-voltage ac directly to 400 V dc inside each server hall, as shown in Fig. 1. This system can eliminate line frequency bulky transformer, reduce front-end conduction cable costs, and save conduction loss. Each system block consists of ac-dc H-bridge converters together with high-frequency isolated dc-dc converters. In total, five cascaded submodules are employed to convert 4160 VAC directly into 400 V DC The inputs of ac-dc H-bridges are in series and the outputs of the dc-dc stages are connected in parallel.

In this work, a high-frequency, high-efficiency isolated CLLC resonant converter is proposed for a next generation dc data center. The medium-voltage high-frequency transformer is the most crucial component in terms of insulation and power density. A novel UU core with sectionalized winding structure is chosen to enhance insulation capability, restrict leakage inductance, and reduce magnetic loss at the same time. Transformer insulation parameters are calculated based on the IEEE Std. C57.12.01 requirements. An additional conductive shielding layer is applied to restrain the electric field inside the insulation and ensure no electric field in air. A stress grading layer is utilized at termination to spread out equal potential line and thus reduces the E-field around termination. The winding arrangement is optimized based on the smallest insulation volume.

The transformer turns number is determined based on the transformer loss volume trade-off and core loss winding loss trade-off. Different working frequency and different core loss density impact on transformer design is also analyzed based on a similar method. 200 kHz is found to be the best working frequency for ML27D material from Hitachi in this application. A 15 kW/200 kHz converter prototype is developed shown in Fig. 2. Experiment results are also presented with 98.7% peak efficiency and 61W/in^3 power density.

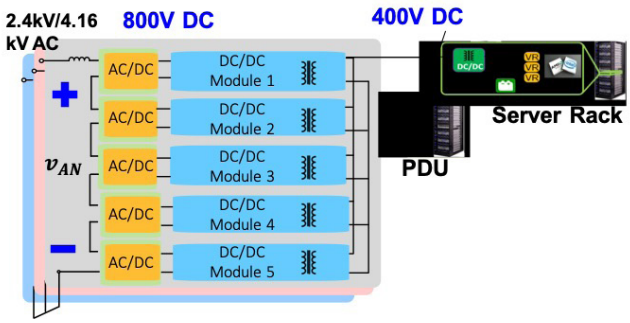


Fig. 1. Proposed medium voltage to SST for data center.

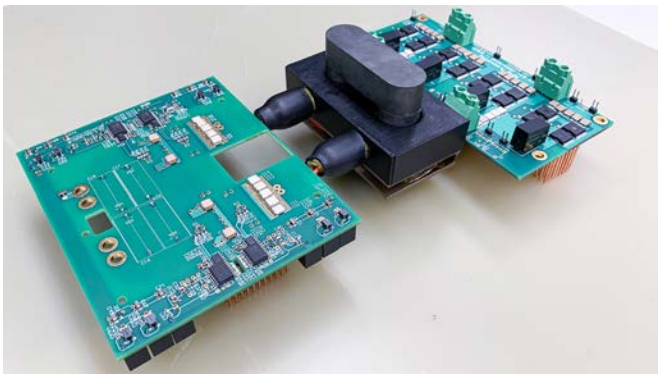


Fig. 2. 15 kW 200 kHz CLLC resonant converter prototype.

PCB-Embedded Integrated Coupled Inductor Design for Integrated VR in Smartphone Application

As the number of cores in microprocessors and power demand increase in mobile applications, power management is crucial to the whole system. Due to low-frequency operation of voltage regulators in today's smartphone products, passive components occupy lots of space on the motherboard. On the other hand, dynamic voltage and frequency scaling (DVFS) can help reduce power consumption of processors. However, traditional voltage regulators cannot support this function due to low-frequency operation and long power delivery path. In order to provide a compact and efficient power solution for high-performance processors, a three-dimensional integrated voltage regulator (IVR) operating at ultra-high frequency (> 10MHz) is proposed shown in Fig. 1. The multi-phase inductor is just underneath the processor to shorten the power delivery path. One of the most challenging parts of IVR design is integrated magnetic design with small volume and loss.

In this paper, a novel, four-phase integrated coupled inductor structure is proposed shown in Fig. 2. (a). Due to negative coupling, the dc flux in the core and inductor footprint are reduced. By integrating four inductors into one magnetic core, the inductor footprint is further reduced by flux cancellation without increasing inductor loss. By optimizing this new inductor structure with the help of a finite element tool, 70% inductor loss reduction and 40% footprint and thickness reduction are realized compared with previous inductor design. Furthermore, to demonstrate the feasibility of integrating active components with proposed inductor structure, the inductor samples are fabricated and embedded into PCB as shown in Fig. 2(b). By using PCB-compatible magnetic material, the inductor performance is not impacted by PCB integration. Finally, a very small footprint(< 14 mm^2) and low profile(0.6 mm) are achieved by this four-phase PCB-embedded, integrated coupled inductor.

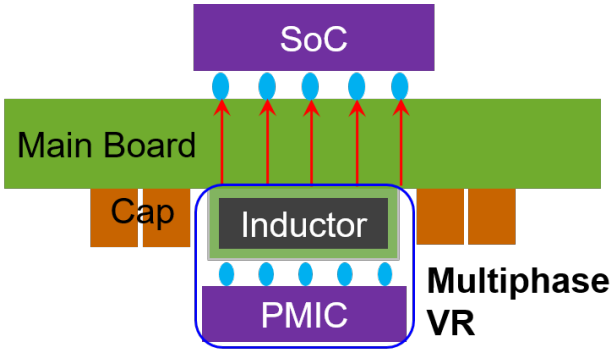


Fig. 1. Three-dimensional IVR structure.

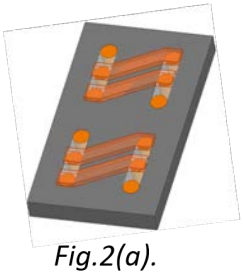


Fig.2(a).

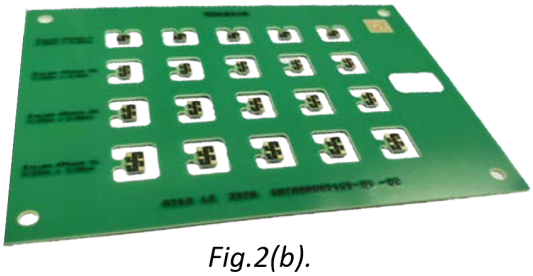


Fig.2(b).

Fig. 2. Four-phase PCB-embedded integrated coupled inductor structure.

Multi-Phase Coupled Inductor Analysis for Multi-Phase Voltage Regulators

As the performance of CPU and GPU continuously grows over the years, multi-phase voltage regulators with faster transient response are necessary to meet such high power demands and load transient requirements. Compared with non-coupled inductors in multi-phase voltage regulators, a negative-coupled inductor can realize small-current ripple and fast transient speed at the same time, as well as smaller inductor size due to flux cancellation in the magnetic core. However, a traditional-coupled inductor structure has difficulty in achieving symmetrical coupling when the phase number is larger than two. Unsymmetrical coupling becomes more severe with larger phase numbers, resulting in phase current difference and larger output voltage ripple and is not preferred.

To solve this issue, an indirect-coupled inductor structure was proposed by CPES to achieve symmetrical coupling as shown in Fig. 1. Furthermore, a hybrid-coupled inductor structure was proposed by Google recently, shown in Fig. 2., which combines both benefits of traditional-coupled and indirect-coupled inductor structures. However, the detailed analysis of these two structures is lacking in the literature and the benefits and limitations are not clear. In this paper, these two structures are analyzed in detail. The equivalent circuits are derived and extended for general case regardless of phase number. Based on the derived equivalent circuit and flux distribution analysis in the inductors, it is found that due to symmetrical coupling, indirect-coupled inductor structure has better circuit performance than that of a traditional-coupled inductor when the phase number is large. However, its flux distribution is similar to that of non-coupled inductors and there is no dc flux cancellation effect. By combining magnetic coupling from a traditional-coupled inductor and indirect coupling from an indirect-coupled inductor, a hybrid-coupled inductor can achieve good circuit performance and dc flux cancellation at the same time. However, careful design is required for the trade-off between circuit performance and inductor size for a hybrid-coupled inductor.

In summary, indirect-coupled inductor and hybrid-coupled inductor structures are analyzed thoroughly in this paper. The benefits and limitations of these two structures are clearly identified, which provide the opportunity to give design guidelines and further improve these two structures.

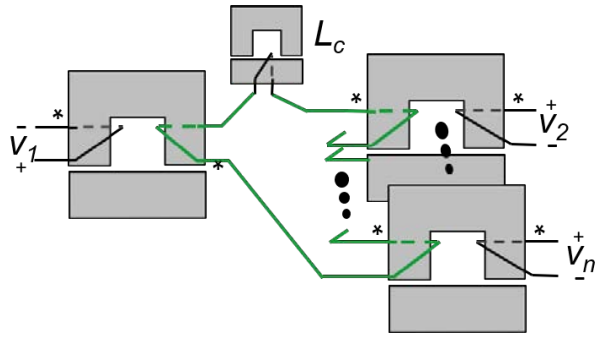


Fig. 1. Indirect-coupled inductor structure.

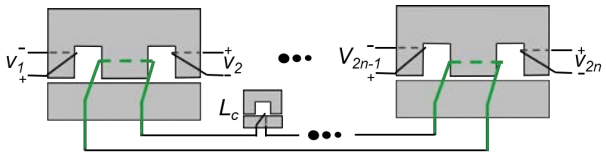


Fig. 2. Hybrid coupled inductor structure.

Solid-State Transformer (SST)-Based 400 kW EV Fast Charger

To shorten the charging time, increase the efficiency, and reduce the volume of an electric vehicle charger, the key research is to replace the bulky line-frequency, medium-voltage (MV) transformer cascaded by a low-voltage rectifier with a high-frequency MV ac-dc solid-state transformer (SST).

Fig. 1. shows the whole fast charger system with medium voltage (13.2 kV), input voltage, and 1.1 kV output voltage and a three-level CLLC resonant converter circuit of cascaded submodule. This resonant converter is a dc to dc conversion component respectively connected in SST. It converts 15 kW from ac-dc PFC output 1.6 kVDC to 1.1 kVDC dc bus then to a fast charger module.

Devices for both primary side and secondary side are selected based on device loss evaluation. Magnetizing inductance Lm and deadtime td are selected based on the requirement of zero voltage switching (ZVS). Transformer core material candidates are evaluated using the specialized core-loss measurement techniques developed at CPES and the core material is selected based on the switching frequency. Litz wire is also selected based on the switching frequency. Considering the insulation requirement, the insulation materials and winding structures are evaluated and selected to minimize the transformer volume. The transformer loss is then calculated using the magnetic core loss model and litz wire winding loss model developed in CPES. Finally, all the transformer design parameters, such as number of turns, core loss density, and switching frequency are optimized based on the trade-off between the volume and converter total loss, as well as winding loss and core loss. A prototype is built according to the optimized design, as shown in Fig. 2.

The CLLC resonant converter operation principals are analyzed and verified through experimental results. The efficiency of one sub-module is tested and compared to the design result. In addition, the insulation capability of the medium-voltage, high-frequency, solid-state transformer is also studied and discussed in the paper, especially its performance on the partial discharge test.

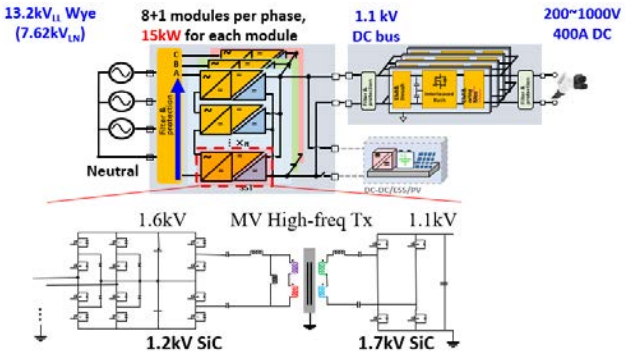


Fig. 1. System structure and one sub-module.

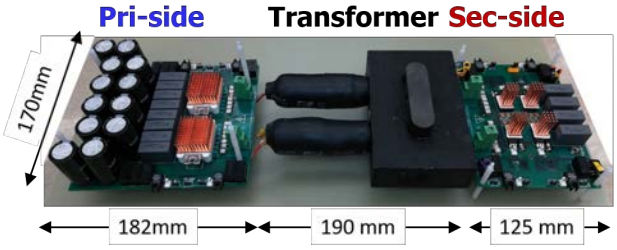


Fig. 2. Three level CLLC resonant converter prototype.

Phase Shedding Control and Circulating Current Analysis of Two-Channel Paralleled Soft-Switching Three-Phase Inverter

To develop a high-power density and efficiency inverter for grid-tied application, a novel CRM-based soft-switching modulation was introduced in which one phase is clamped to dc bus for DPMW, and two other phases operate in CRM and DCM at high frequency. With the soft-switching method, by paralleling two inverters and interleaving them, 98.9% peak efficiency and 127 W/in^3 were achieved above 300 kHz switching frequency for 25 kW inverter.

However, light load efficiency of the inverter is relatively low and decreases abruptly as output power goes down. The current handled by each channel becomes smaller at light load and the switching frequency of the inverter increases dramatically due to its CRM-based operation as shown in Fig. 1. (a). This brings about high switching-related loss. As shown in Fig. 1. (b), at 20% load, the switching-related loss is not only high, but also dominant. Minimization of the switching-related loss is the key to improve the light load efficiency.

The main concept of the proposed control for light load efficiency improvement is to lower the switching frequency by increasing the current that is handled in the first channel (CH1). No gate signals are given for the entire switches in channel 2 (CH2), so-called "phase shedding." With the phase shedding, the switching frequency drops significantly because of the increased current in CH1. Another benefit is the number of switches running at high frequency halves due to the no switching action in CH2. This also greatly reduces the switching-related loss.

By the way, despite no gate signals given in CH2, some current flows through CH2 during the clamping mode. The current does not deliver any energy to the output. It only circulates between CH1 and CH2 rendering the rms value of the inductor current in CH1 larger. When one phase is clamped, the corresponding switch's body diode in CH2 is forward-biased. Switching status in CH1 affects inverter output voltage in CH2 because two channels share the zero-sequence voltage.

The solution for the issue is to enable the clamping mode phase in CH2. In Fig. 2. (a), the gate signal is given in phase A in CH2 the same as CH1 and only the gate signals in CRM and DCM phases (phase B and C) in CH2 are not given. In this way, the currents in CH1 and CH2 converge to each other after entering clamping mode as shown in Fig. 2. (b). Eventually, the circulating current is removed and currents in both channels deliver power to the output. This control method improves light load efficiency by 0.8% -2.4%.

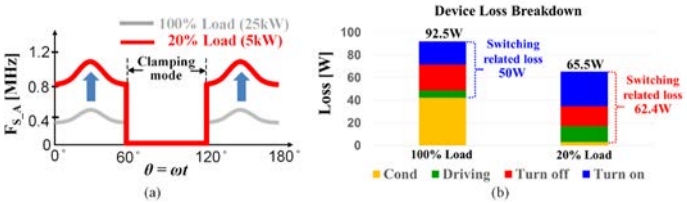


Fig. 1. (a) Phase A switching frequency (b) Device loss breakdown under full and 20% load conditions.

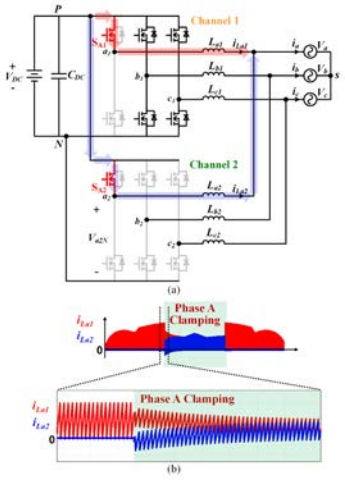


Fig. 2. (a) New phase shedding method (b) Removal of the circulating current.

Control Technique for CRM-Based High-Frequency Soft-Switching Three-Phase Inverter under Grid Fault Condition

To develop high-power density and efficiency inverter for grid-tied application, critical conduction mode (CRM)-based, soft-switching modulation (DPWM + CRM + DCM) for three-phase two-level inverter was developed. In this modulation scheme, one phase is clamped to DC-rail such that the other two phases operate at high frequency as CRM and DCM. In this soft-switching method, the turn-on instant of DCM phase is synchronized with CRM phase to reduce wide-switching frequency range. Although it was proven that the modulation method is a reasonable solution for high-frequency operation with high efficiency, previous studies only focused on ideal grid conditions such as balanced and rated voltage. For practicality, studies on non-ideal grid conditions like fault conditions need to be conducted.

Voltage sag is one of the most frequently happening grid faults. Under this condition, the magnitude of 3-phase voltage drops and imbalance appears. This could cause oscillation in the active power at the output side which is reflected to the dc-link capacitor as a larger voltage ripple. The voltage ripple across the dc-link capacitor may lead to over-voltage protection and stop inverter operation. To avoid such situations, constant active power should be delivered to the grid. For constant active power delivery, the output current to the grid becomes unbalanced as shown in Fig.1.

The challenge is to maintain the soft-switching during the grid fault. However, CCM operation occurs where DCM operation is intended. As a result, turn-on loss of the inverter increases substantially. Due to the unbalanced grid voltage and the ac current reference, the CRM phase current reference is smaller than DCM phase current reference in some region, which never happens under balanced grid conditions. In this case, since the CRM phase determines the turn-on instant, the DCM phase is turned on before the DCM phase inductor current reaches zero losing volt-sec balance.

To prevent the CCM operation and reduce the turn-on loss, off-time extension is used in the CRM phase as illustrated in Fig. 2. By comparing zero current detection (ZCD) signals of CRM phase and DCM phase, decision-making for off-time is made. In this control technique, CRM phase off-time is extended until DCM phase current reaches zero. Consequently, the concentrated turn-on loss in CCM operation region diminishes significantly.

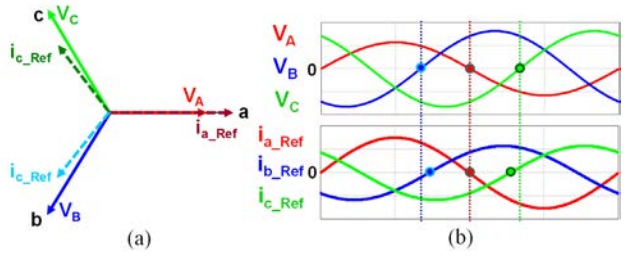


Fig. 1. Grid voltage and ac current reference under type B voltage sag for constant active power delivery (a) phasor diagram (solid: the grid voltage, dotted: the ac current reference), (b) time-domain waveforms.

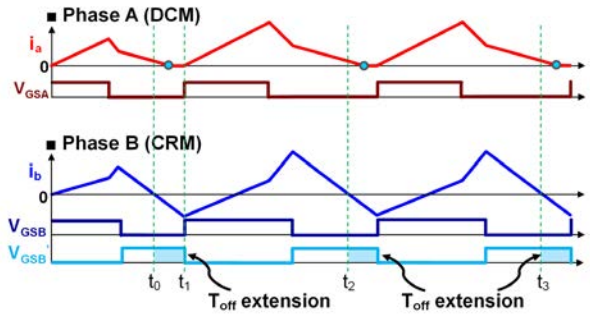


Fig. 2. Concept of the control scheme for the soft-switching three-phase inverter under grid fault condition: Off-time extension in CRM phase.

Tri-Gate GaN Junction High-Electron-Mobility Transistors

The tri-gate technology allows GaN HEMTs to realize enhancement-mode operation, superior gate control, and low leakage current. This work presents a GaN tri-gate transistor concept, the tri-gate GaN junction high-electron-mobility transistor (JHEMT), which comprises p-n junctions wrapping the AlGaN/GaN fins in the gate region. This tri-gate JHEMT differs from all the existing GaN FinFETs or tri-gate HEMTs, as they use the metal-insulator-semiconductor (MIS) gate stack. The p-n junction can offer stronger depletion than the MIS owing to a larger built-in potential (Vbi) and the obviation of voltage drop in the insulating dielectrics, thereby making it easier to realize the E-mode and prevent the punch-through.

A self-aligned process is used to deposit the NiO and gate metal in the same lithography step. The NiO is deposited in a magnetron sputtering system using the NiO target. Fig. 1. shows the scanning electron microscopy (SEM) images of the GaN fins before and after NiO sputtering, verifying the conformal NiO coverage. A hole concentration and mobility of 5×1019 cm^{-3} and 0.7 cm^2/Vs, respectively, are extracted for the sputtered p-NiO. For the tri-gate MISHEMTs.

Fig. 2. (a) shows the double-sweep transfer characteristics (VDS = 5 V, saturation region) of the tri-gate JHEMTs and MISHEMTs with 60 nm WFin. The tri-gate JHEMT has a VTH of 0.45 V (extracted at 1 μA/mm drain current) and a hysteresis below 0.1 V, while the tri-gate MISHEMTs show a negative VTH and ~0.6 V hysteresis. The close-to-60 mV/decade SS and small hysteresis in tri-gate JHEMTs suggest very small interface states in NiO-based junction gate. The tri-gate JHEMT faces larger gate leakage current when NiO/2DEG diode turns on. Fig. 2. (b) shows the output characteristics of the 60-nm tri-gate JHEMTs and 40-nm tri-gate MISHEMTs with a similar VTH. The higher current density in the tri-gate JHEMT is mainly due to the larger portion of the gate for current conduction.

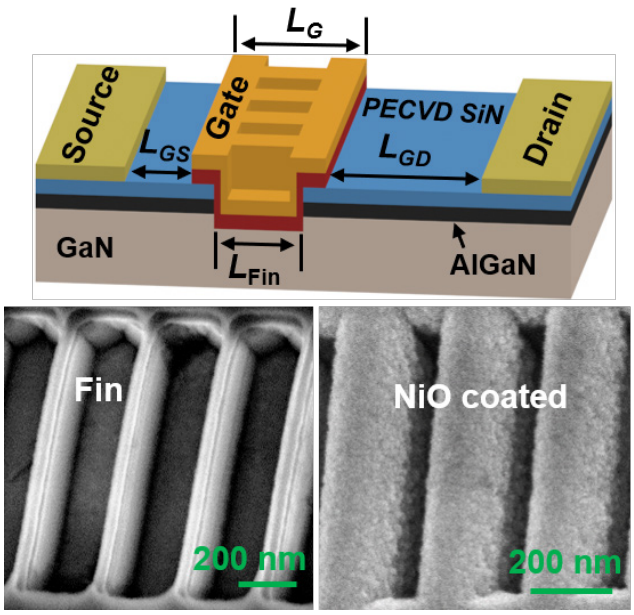


Fig. 1. (top) Diagram of tri-gate junction HEMT, the fins can be seen in gate region, wrapped by NiO and gate metal. (bottom) SEM image of fin before and after NiO coating.

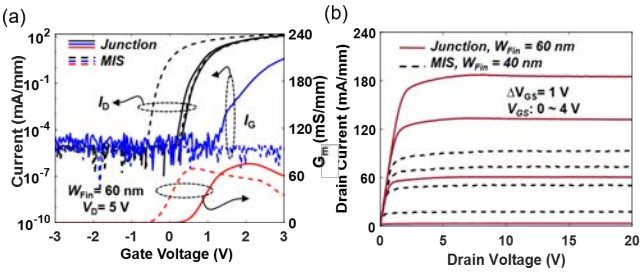


Fig. 2. Transfer and output characteristics of tri-gate JHEMT and MISHEMT. (a) compares transfer of junction and MIS trigate with same fin width Wfin= 60 nm. (b) compares output of junction and MIS trigate with same VTH.

Modeling and Control for 48 V/1V Sigma Converter

48 V voltage regulator modules (VRMs) are critical for telecom power supplies, and are becoming popular for future data centers. By using a novel sigma converter topology, outstanding performances in terms of efficiency (95.2%) and power density (700 W/in^3) have been demonstrated. Both the efficiency and power density are much higher than state-of-the-art solutions. However, both modeling and control of the Sigma Converter are challenging due to the quasi-parallel structure and have not been resolved properly yet. The small-signal model of current mode and V2 control are provided and compared with voltage mode control. The V2 control with active droop control is chosen for high bandwidth and constant load line design.

Fig. 1. shows the bode plot of constant-on-time current mode and enhanced V2 control, as well as the comparison with voltage mode control, where Vin=54V, Vo=1.4V, D=0.07, n=12, Lr=440nH, L=210nH, Cin=10uF, Co=2mF. From Fig. 1., voltage mode has a low frequency double pole and COT current mode has a low frequency RHP pole (gain decreases and phase increases). As a result, both voltage mode and COT current mode are not suitable for high-bandwidth design and enhanced V2 control is chosen.

It is well known that CPU VR must achieve adaptive voltage positioning (AVP) to meet Intel load line specification. In order to meet the AVP requirement, the active droop control scheme is adopted as shown in Fig. 2. With this method, constant load line is achieved at all operating regions.

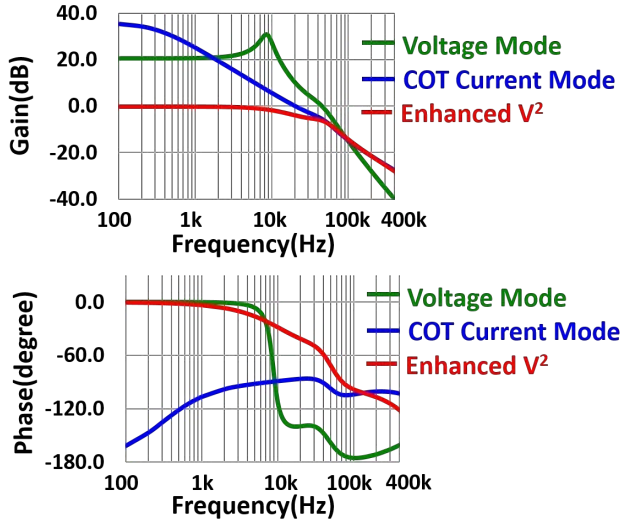


Fig. 1. Bode Plot of Control to Output Transfer Function with Different Control Methods.

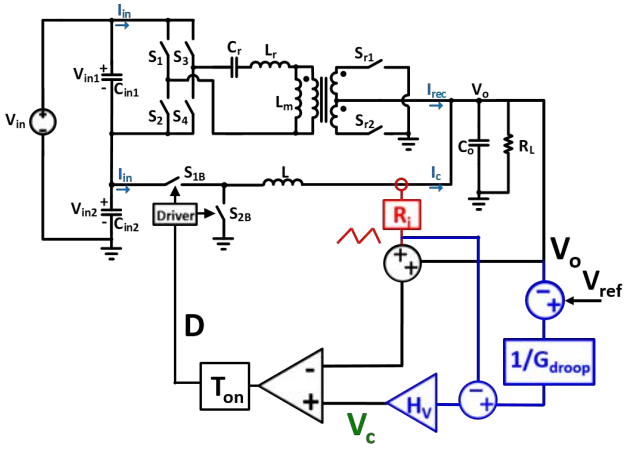
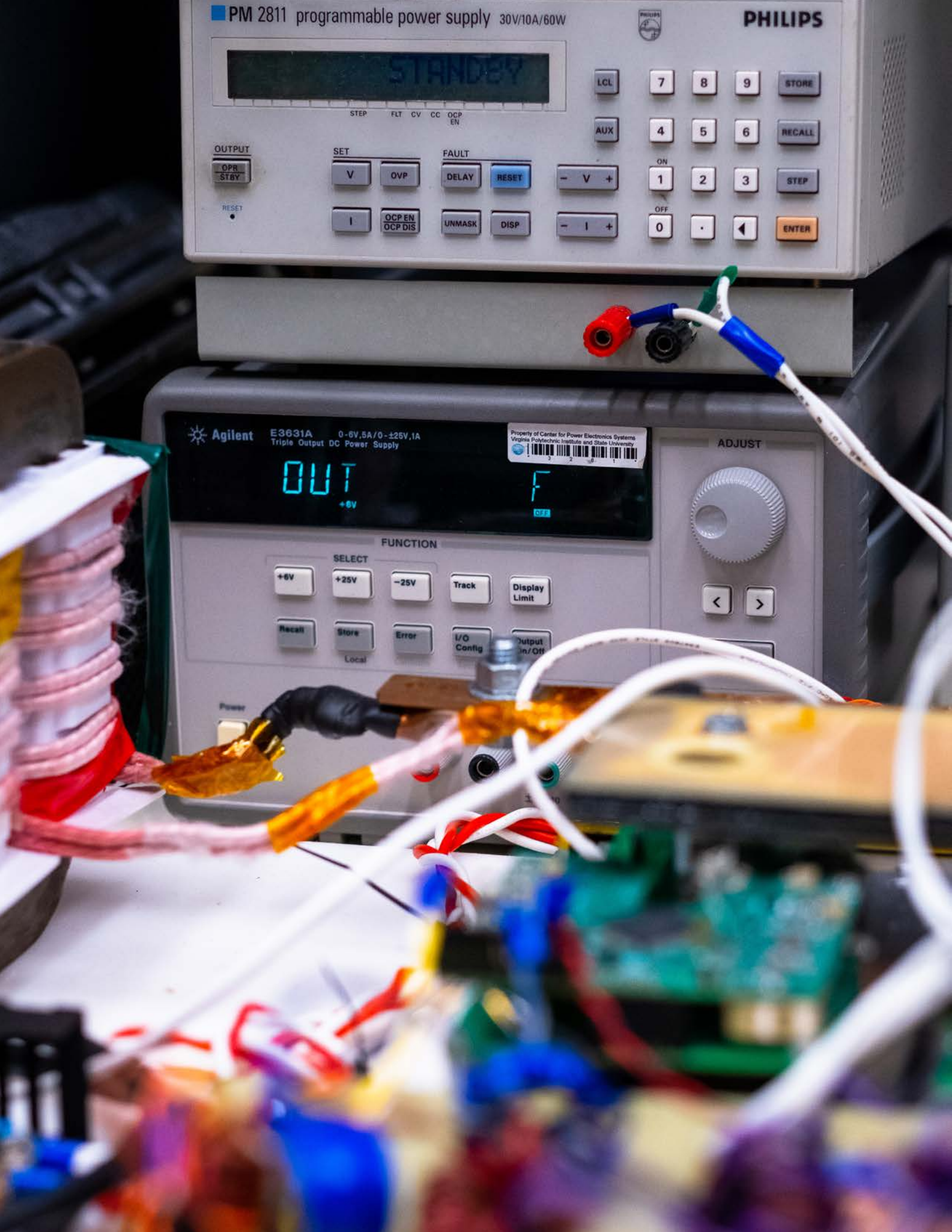


Fig. 2. Proposed Active Droop Control Scheme.


PM 2811 programmable power supply 30V/10A/60W
PHILIPS
STANDBY
STEP FLT CV CC OCP EN
LCL
7
8
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STORE
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RECALL
OUTPUT
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V
OVP
FAULT
DELAY
RESET
ON
1
2
3
STEP
RESET
I
OCP EN OCP DIS
UNMASK
DISP
OFF
0
ENTER
Agilent
E3631A
0-6V,5A/0-±25V,1A
Triple Output DC Power Supply
Property of Center for Power Electronics Systems
Virginia Polytechnic Institute and State University
OUT
+6V
OFF
ADJUST
FUNCTION
SELECT
+6V
+25V
-25V
Track
Display Limit
Recall
Store
Error
I/O Config
Local
Power

11 kW Bidirectional On-Board Battery Charger

Nowadays, electric vehicles (EV) are becoming more and more popular. Consumers are greatly interested in the on-board battery chargers (OBC) with higher power capability for faster charging time. The typical system structure of OBC is a front-end ac-dc stage, followed by a step-down dc-dc converter, as shown in Fig. 1. In this paper, the design considerations of the two-stage on-board charger are introduced, including the optimization of PCB-based magnetic design and the control strategy between stages. A 11 kW on-board charger prototype with 57W/in^3 power density is demonstrated and the efficiency of the system is above 96% over the whole battery voltage range, as shown in Fig. 2.

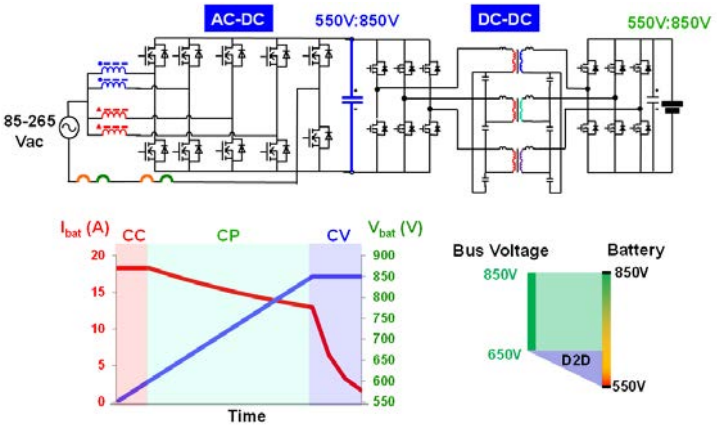


Fig. 1. The system structure of 11 kW on-board charger (a) and battery charging profile (b).

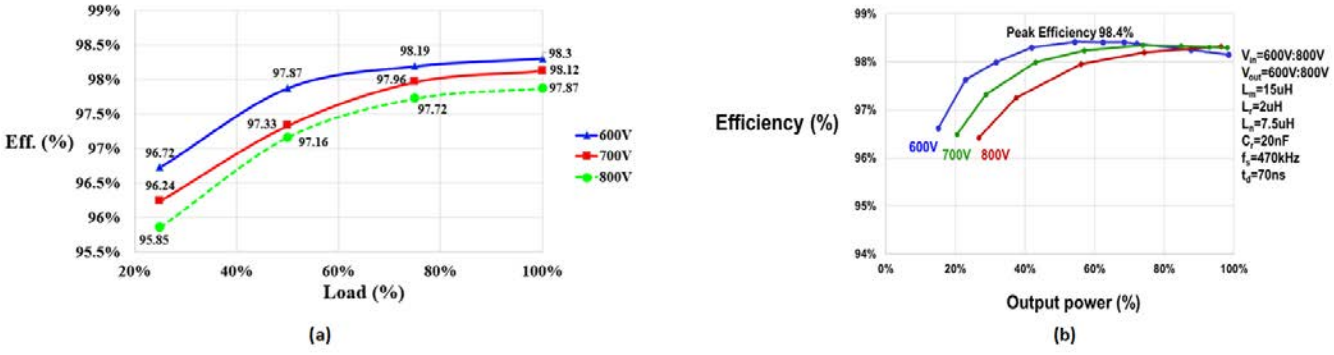


Fig. 2. The overall efficiency of the system: (a) ac-dc stage and (b) dc/dc stage.

A Three-Phase CLLC Converter with Improved Planar Integrated Transformer for Fast Charger Applications

Fast charging technology is a key feature that could attract customers to purchase an electrical vehicle instead of a gasoline-driven car. Solid-state-transformer (SST)-based charging stations have increasingly drawn attention. They require a high-efficiency, high-power density dc-dc stage to provide universal charging for all EVs no matter if their battery voltage is 400 V or 800 V. A two-stage dc-dc converter consisting of a three-phase CLLC converter and four-phase interleaving buck converters could meet the wide output voltage range as shown in Fig. 1.

The three-phase CLLC dc-dc converter can run at a high switching frequency so that the resonant inductors and transformers of three phases can be integrated into one six-leg core and built with PCB windings with the benefits from SiC devices as shown in structure 1 of Fig. 2. However, the core loss on the plate is still large since the flux on the plate is not evenly distributed. A novel core structure based on the six-leg integrated transformer will be proposed to reduce the core loss of core plate by adopting additional legs without sacrificing the footprint of core as shown in structure 2 of Fig. 2. Detailed analysis of the new core structure and comparison will be shown in the final paper. The peak efficiency of the proposed converter can be expected to be 98.3% and its power density is up to 150 W/in^3. The detailed experiment results will be provided in the full paper.

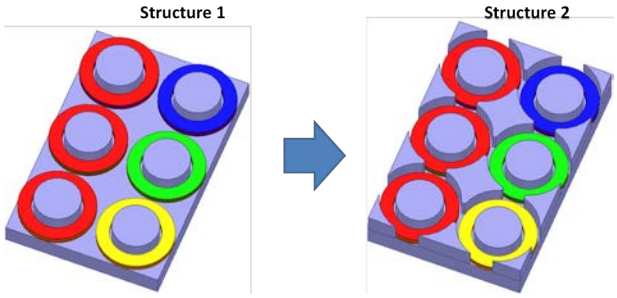


Fig. 2. Structure Comparison.

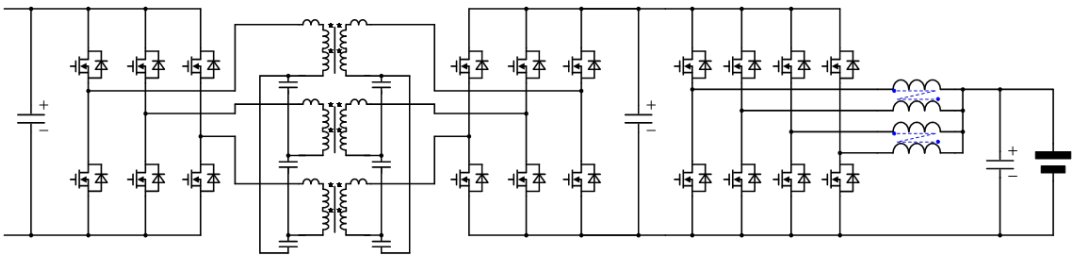


Fig. 1. Topology of proposed dc-dc converter.

A GaN-Based 2.2 kW Totem-Pole PFC Rectifier for Electric Vehicle Applications

Totem-pole PFC is well known as the simplest topology among bridgeless boost PFC structures. With the emergence of high-voltage Gallium-Nitride (GaN) high-electron-mobility transistor (HEMT), totem-pole structure is becoming increasingly popular for PFC rectifier. GaN HEMT has comparatively high turn-on loss and extremely small turn-off loss, which makes CRM soft switching operation very suitable to reduce switching loss by achieving zero-voltage switch (ZVS) during turn-on process. Two-phase interleaving is implemented to reduce DM noise and balance technique is introduced to this system to reduce CM noise. By pushing to high switching frequency, boost inductor value can be reduced, and together with balance technique, the boost inductor can be integrated to PCB winding inductor. The system is shown in Fig. 1.

A double loop control strategy is proposed to control this totem-pole PFC system, as shown in Fig. 2. Inner average current loop controls the average current to track the desired sinusoidal reference. The Toff calculation based on Iref, Vin and Vo guarantees the system works in CRM to achieve ZVS. Also, Ton is extended at line voltage zero-crossing area by the average current loop to improve the THD performance. Open-loop interleaving control is implemented to control the phase shift between the leading phase and following phase. The output voltage loop controls the output voltage. All control functions are implemented in a single digital signal processor.

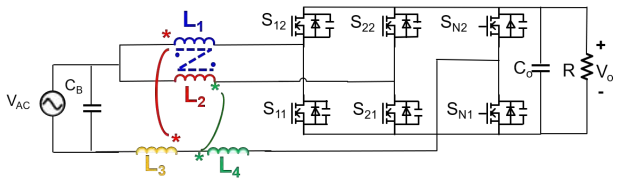


Fig. 1. 2-phase interleaved totem-pole PFC.

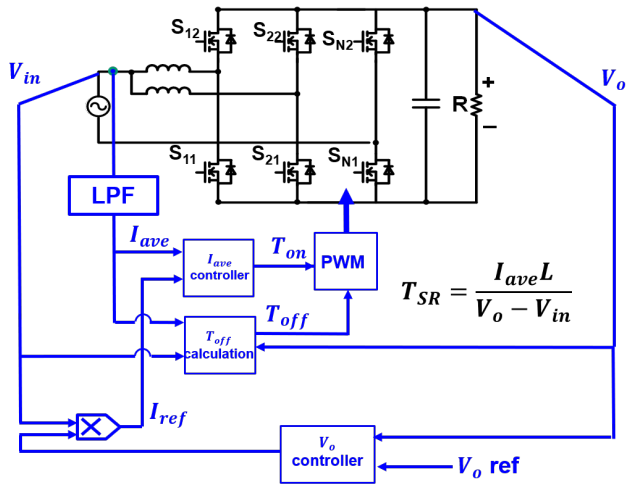


Fig. 2. Control strategy of 2-phase interleaved totem-pole PFC.

High-Power Transformer Design with Controllable Leakage Inductance for LLC Resonant Converter

With the electrification of railways, more power density and a more efficient auxiliary power converter used for lighting, fan, and compressor are in great demand. A 30 kW converter transferring a 500-1000 V dc voltage to a three-phase 380 V ac voltage with 150% overload is proposed. The topology is illustrated in Fig. 1. consisting of one dc/dc stage and one dc-ac stage. The dc/dc stage will transfer a 500-1000 V voltage to 600-800 V and serial half bridge resonant LLC converter is adopted because it can stand high voltage for primary side.

This paper focuses on the transformer design for the dc/dc stage. The transformer turns ratio is selected to be 0.563 based on the input and output voltage range. UI Core is selected based on needed leakage inductance. Different winding structures' impact on leakage inductance is analyzed and finally leakage inductance is achieved by properly breaking the interleaved winding structure without sacrificing too much winding loss.

The transformer turns number is determined based on the transformer loss volume trade-off and core loss winding loss trade-off. Different core loss density's impact on transformer design is also analyzed based on a similar method.

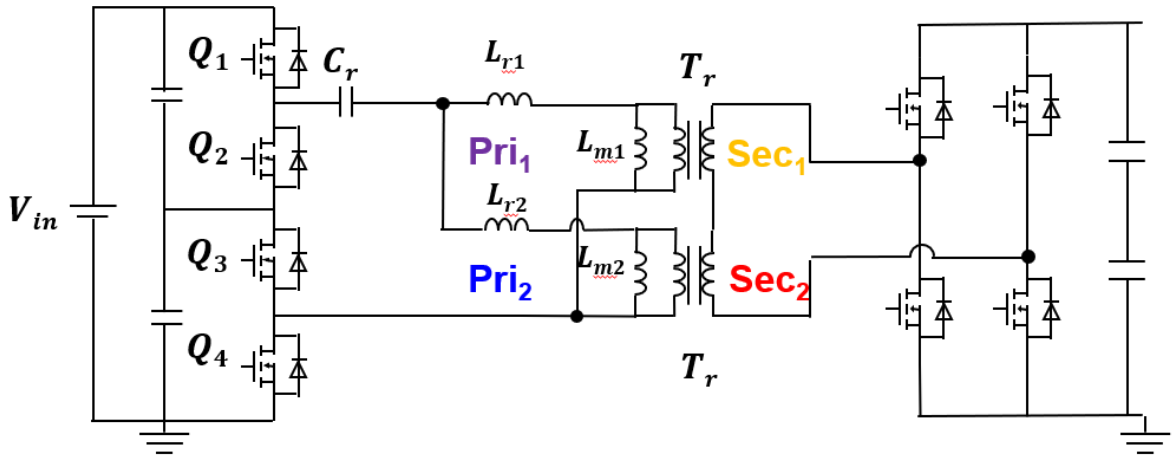


Fig. 1. Topology for the auxiliary power converter.

Surge Energy and Overvoltage Robustness of Cascode GaN HEMTs

Surge energy robustness of power devices is desired in many applications such as automotive motor inverters and powerlines. GaN high-electron-mobility transistors (HEMTs) have no intrinsic avalanche capability; p-gate GaN HEMTs were recently shown to withstand surge energy with their overvoltage capability. This work, for the first time, studies the surge-energy robustness and failure mechanisms of 650 V-rated cascode GaN HEMTs in the unclamped inductive switching (UIS) tests, which were found to be different from the ones of p-gate GaN HEMTs. The cascode GaN HEMT initially withstands the surge energy through capacitive charging, until VDS of the cascode device reaches ~150V350V, where the Si MOSFET begins to avalanche. Subsequently, two failure modes are observed, both occurring in the GaN HEMT. The first mode is electric-field (E-field) induced when the peak overvoltage reaches the HEMT breakdown voltage (BV ~2kV) Fig. 2. (a), featured by a short between the HEMT gate and drain (cascode source and drain) Fig. 2. (b). In the second mode, the cascode fails at a voltage much lower than the HEMT BV Fig. 2. (c), featured by a short between the HEMT source and drain Fig. 2. (d). The failed DUT can block voltage and avalanches like a low-voltage Si MOSFET Fig. 2. (e). These results provide critical insights on the cascode GaN HEMT ruggedness in surge-energy and overvoltage conditions.

The device under test (DUT) is a commercial 650 V, 50 mΩ rated cascode GaN HEMT Fig. 1. (a). Fig. 1. (b) shows the schematic of the UIS set-up. The typical DUT safe-withstanding waveform in the UIS test with a 20 μH inductor is shown in Fig. 1. (c). Five distinct phases have been identified: (a) Phase I: The DUT is turned ON, the inductor is charged by VDD. (b) Phase II: The Si MOSFET is first turned OFF, then the HEMT is turned off. (c) Phase III: cascode output capacitance (Coss) resonates with the load inductor (L) Fig. 1. (d). (d) Phase IV: Si MOSFET avalanches; the inductor energy is resonantly charging the HEMT CDS and resistively dissipated in Si avalanche simultaneously Fig. 1. (e). (e) Phase V: repeat phase III. (f) Phase VI: The DUT is turned on in its 3rd quadrant and the inductor and is gradually discharged by the power supply.

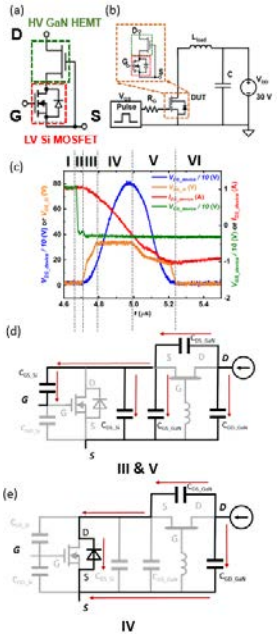


Fig. 1.

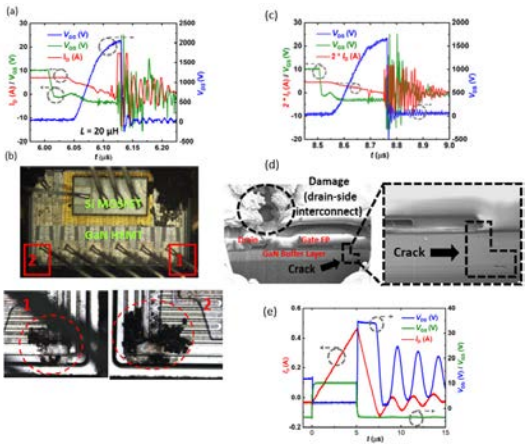


Fig. 2.

Medium-Voltage Multi-Channel AlGaN/GaN Power Schottky Barrier Diodes

This work demonstrates multi-kilovolt AlGaN/GaN Schottky barrier diodes (SBDs) on a 4-inch, 5-channel, low-cost GaN-on-sapphire wafer. Our device highlights a new 3-D anode architecture, in which the p-n junction wraps around the multi-2DEG-channel fins. Fig. 1. (a) and (b) show the device structure diagram and equivalent circuit model of this Junction-Fin-anode (JFA) SBD, respectively. This junction-fin structure differs from all existing tri-anode and tri-gate structures, which employ a Schottky or a metal-insulator-semiconductor (MIS) stack at the fin sidewalls. Our junction-fin structure is realized with regrown p-GaN on the top of the fin and p-type NiOx at the fin sidewalls. Thanks to the strong charge depletion, this structure allows an over 10-fold reduction in device leakage current. The top p-GaN further extends towards the cathode, which shields the fin-anode region from the high electric field. Our SBDs show a breakdown voltage (BV) from 300 V to 5.2 kV with a leakage current of 1.4 μA/mm at 90% BV, as well as super-low on-resistance (Ron), rending a Baliga's figure of merit (FOM) exceeding the SiC 1-D unipolar limit and among the highest in all kilovolts power SBDs. The projected VF•QC (forward voltage times reverse charges) metrics is also superior over commercial SiC devices at multi-kilovolt levels. Large-area, multi-channel AlGaN/GaN SBDs are demonstrated for the first time, with a 1.5 A current, a 4.8 kV BV with ~μA leakage current, and a 13 nC total charge. Fig. 2 benchmarks the specific differential Ron vs. BV of our multi-channel AlGaN/GaN JFA-SBDs, compared to the state-of-the-art lateral GaN, vertical GaN, SiC, and Ga2O3 SBDs. As our device is the first large-area multi-kilovolts AlGaN/GaN SBD. These results show the great potential of AlGaN/GaN multi-channel devices for medium-voltage power applications.

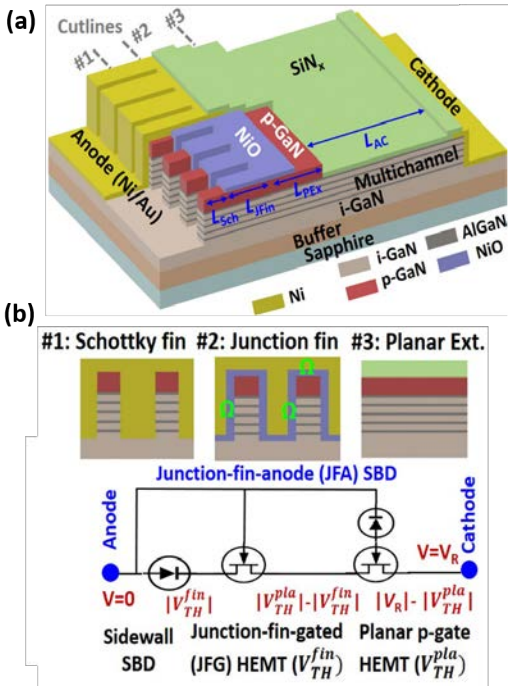


Fig. 1. (a) Junction-Fin-anode (JFA) SBD structure and (b) equivalent circuit model.

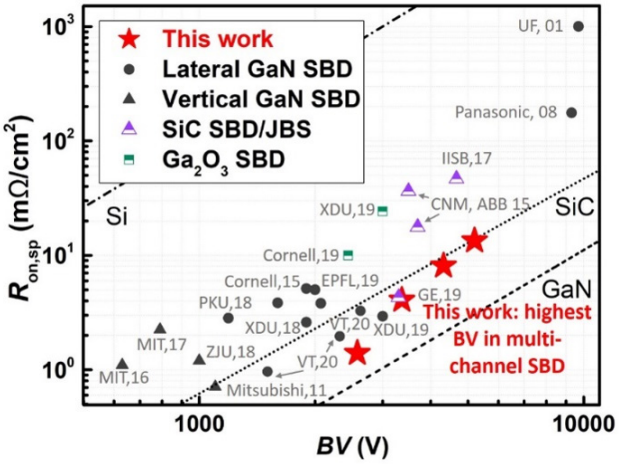


Fig. 2. Specific RON vs. BV of our multi-channel AlGaN/GaN JFA-SBDs.

Design Optimizations of the PCB Winding Matrix Transformer for LLC Converters

Of all the power supplies for industrial applications, those for the data center servers are among the most performance-driven, energy- and cost-conscious due to the large electricity consumption. Moreover, with the rapid increase in cloud computing and big data, the demand for higher performance in power delivery is sought after. Different power architectures for data centers have been explored in the past, and recently an architecture with a 400 V bus with an on-board 400 V/12 V converter has gained interest due to its potentially higher efficiency due to lower bus losses.

CPES designed a 400 V/12 V half-bridge LLC dc-dc converter with a planar matrix transformer and center-tap secondary rectifiers running at 1 MHz with a peak efficiency of 97.6% and a full load efficiency of 97.2%. To further improve the efficiency while maintaining the same power density, the switching frequency of the converter was swept from 200 kHz to 1.6 MHz and the transformer loss was evaluated versus magnetic footprint. It was found that the transformer loss is similar from 600 kHz to 1 MHz, but since the device switching losses increase with switching frequency, the lower frequency of 600 kHz has better overall converter efficiency. Subsequently, the 400 V/12 V LLC converter was redesigned for switching frequency of 600 kHz and a peak efficiency of 98.05% and a full-load efficiency of 97.2% was obtained, as shown in Fig. 1.

Upon closely examining the thermal performance of the converter it was observed that the temperatures of the secondary devices were not uniform, as shown in Fig. 2. This indicated that there are current-sharing issues between the four parallel secondary windings that conduct together in one switching cycle. This was reiterated by comparing the drain-source voltages of the parallel SRs, where it could be seen that the body diodes of the SRs stop conducting at different times, indicating different currents flowing through each device. A few factors causing this issue have been discussed in detail in this paper, such as proximity of the winding to the air gap of the transformer and the proximity of the conducting secondary layer to the conducting shield layer. A possible solution will also be presented.

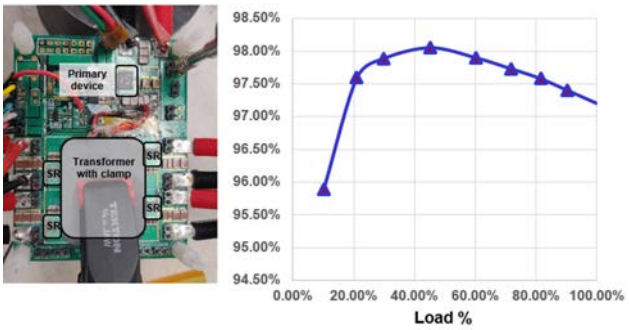


Fig. 1. Test hardware and converter efficiency.

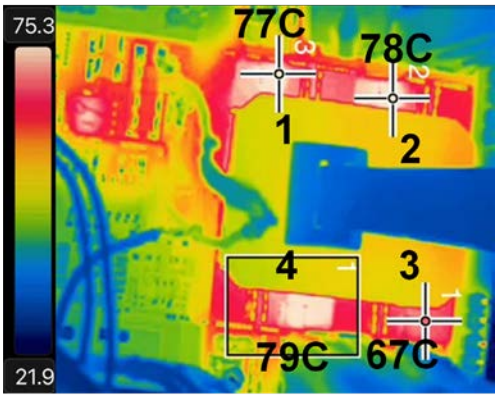


Fig. 2. Temperatures of SRs when converter running at full load.

Wide-Bandgap High-Power Converters & Systems (WBG-HPCS) Nuggets

Small-Signal Stability Impact of Utility PV with Reactive Power Control on the Medium-Voltage Distributed Systems

With an increasing number of photovoltaic (PV) inverters in the distribution system, their impact is no longer negligible, especially in the aspect of dynamic interaction. Accordingly, a comparison is done among PV inverters of different reactive power control modes, to determine their impact on the system voltage profile, power loss and small-signal stability. Generalized Nyquist Criteria (GNC) based on impedances in DQ frames is used for stability assessment, which is validated by time domain simulation results and also system eigenvalues calculation results from MATLAB. From these, guidelines are formulated to manage PV inverter reactive power control strategies. Reactive power control mode of volt-var Q = f (V) is preferred to other reactive power modes to avoid a voltage profile problem and reduce power loss, but will induce small-signal instability and cause PV terminal voltage oscillations. There's tradeoff between static influence and dynamic impact in choosing the local reactive power control strategies.

A known broad statement is that active power injected by PV inverters increases the system voltage. In what regards the reactive power compensation capability of PV inverters, this paper showed that the reactive power control mode Volt-var droop mode of Q = f (V) is preferred over other reactive power control modes after the static analysis of voltage regulation effect and the impact on grid power loss.

The terminal impedances in DQ frame are derived of utility-scale PV farm based on small signal model of PV inverters as shown in Fig.1. A comparison is done among impedances of PV inverters under 5 different reactive power control modes, based on which GNC is used to assess the grid-PV connection stability as shown in Fig. 2. The volt-var control mode changes PV terminal impedance signs and magnitudes significantly and may cause unstable connection to the grid. The stability assessment is proved by time domain simulation and also eigenvalues acquisition from the state space model of the whole system with PV generators.

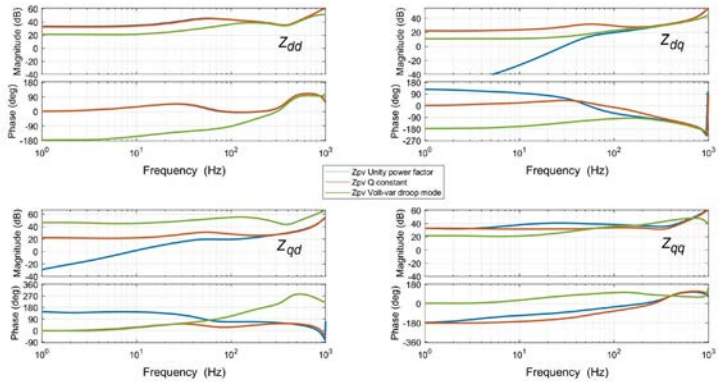


Fig. 1. PV impedances under different Q control modes.

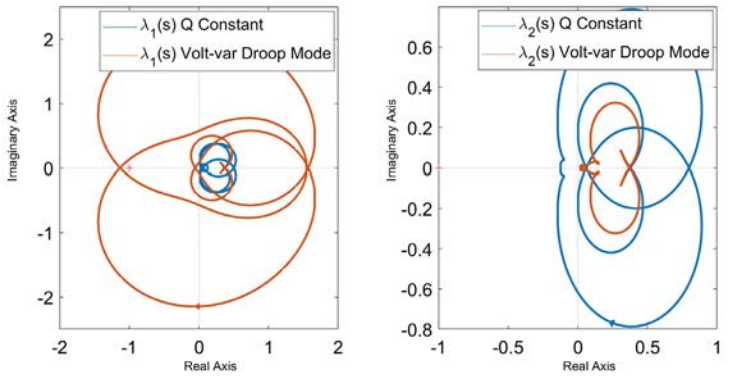


Fig. 2. Characteristic loci of PV connection to the grid.

Control of Converters Having Integrated Capacitor-Blocked Transistor Cells

Converters having Integrated Capacitor-Blocked Transistor (ICBT) cells provide a new method to transfer high power in medium voltage systems. Each ICBT cell includes a pair of switching devices and a cell capacitor. An ICBT-based phase leg has two converter arms, each of which includes one or more series-connected ICBT cells. An ICBT-based phase leg with two cells per arm is shown in Fig. 1. Each ICBT cell operates as a single switching device and an ICBT-based converter arm operates as a high-voltage device. In this way, ICBT-based converters enable direct power flow from input to output, are capable of both dc and ac operation modes, have little additional losses and do not require high cell capacitance values.

All the switching devices in the same phase leg are controlled together to operate collaboratively. The two switching devices in each cell operate complimentarily. Then, the ICBT cells in the same arm operate synchronously and the cells in opposite arms operate complimentarily. In each ICBT cell, a deadtime is applied to the pair of top switchs and bottom switchs to avoid shoot-through in the cell. Meanwhile, a deadtime is also required between the cells in the upper arm and the cells in the lower arm to avoid shoot-through in the phase leg. In addition, all cells in both arms cannot be off together, otherwise all the cell capacitors in a phase leg will be connected in series and to the converter bus and lead to shoot-through in the phase leg. All three types of deadtimes need to be long enough to ensure safe operation. Different deadtime values also affect the switching transients of an ICBT-based phase leg. It is discovered that when the phase leg deadtime is shorter than the cell deadtime, cell capacitors have less voltage ripples and the phase leg has less total switching loss.

For medium-voltage, high-power, modular converters like ICBT-based converters, the energy internally stored in cell capacitors needs to be carefully dealt with. A state machine is defined for the converter, in addition to the control algorithm during ICBT operation, to ensure the safe operation and correct functions of the converter. The converter is in the off state at the beginning of a test. The converter will transit to the pre-charge state to charge the cell capacitors. Then the converter will transit to the normal operation state through a buffer state called the idle state. After the desired test is conducted, the converter will transit to the discharge state through the idle state, to discharge the cell capacitors. The converter will finally transit to the off state if all the cell capacitors are fully discharged. The converter is de-energized other than the low-voltage auxiliary circuits. Various fault detections are implemented to detect any failures or malfunctions in the converter. The converter may enter fault state from any other states if any kind of fault is detected in the system.

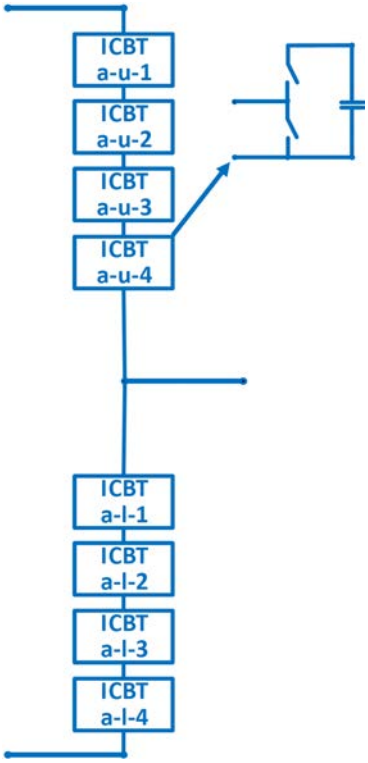


Fig. 1. An ICBT-based phase leg with two cells per arm.

SiC MOSFET Characterization, Packaging, and Reliability at 300° C

Though significant progress has been made in the semiconductor industry for SiC MOSFET fabrication, there remains a lack of research in pushing the high temperature operation and reliability to 300° C for the newest generation of SiC MOSFETs available. This work provides the groundwork for developing a power module capable of reliable operation at ambient temperatures of 250° C. Since device self-heating will cause the junction temperatures to be greater than 250° C, testing was performed at 300° C. To do so, reliability tests are conducted on SiC MOSFETs.

The HTRB test stresses the blocking capability of the MOSFET. A high voltage is placed on the drain to source potential of the MOSFET, which results in edge termination breakdown, gate oxide breakdown, and MOSFET drift region breakdown. Precursors for failure during HTRB include a shifted VAV, increased IDLEAK, as well as VTH shift or gate oxide breakdown.

The HTGB test stresses the gate oxide layer of the MOSFET. A high voltage is placed on the gate to source potential of the MOSFET, which results in a drift in the VTH or gate oxide breakdown.

Fig. 1. shows the experimental test setup for the HTGB and HTRB tests. 16 samples (8 for HTRB and 8 for HTGB) are tested. The samples are placed on a hotplate. Device junction temperature is kept at 300° C. Every 100 hours, the devices are cooled to room temperature and removed from the test fixture. Each device has static characterization performed and is replaced back in the test fixture. The temperature is taken back up to 300° C. These tests were designed in accordance with standards listed in JEDEC's A108C and Automotive Electronics Council's (AEC) Q101 forms.

Incremental static characterization is performed on the devices during the test. Every 100 hours, the devices are measured on the Agilent B1505A curve tracer. Failure is defined to be any characteristic outside of nominal datasheet values.

Fig. 2. shows the results from the HTGB and HTRB tests. As shown, all devices failed within 300 hours. For the HTRB test, 6 of the 8 samples catastrophically failed within 100 hours. Catastrophic failure is defined to be a short exhibited across the drain to source or gate to source of the MOSFET. For the HTGB, 2 of the 6 samples failed catastrophically within 100 hours.

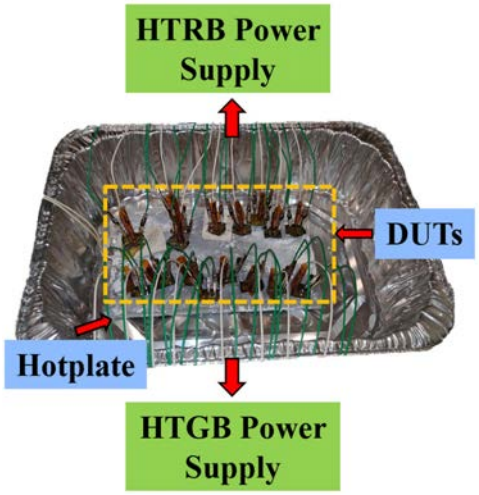


Fig. 1. HTRB and HTGB test setup.

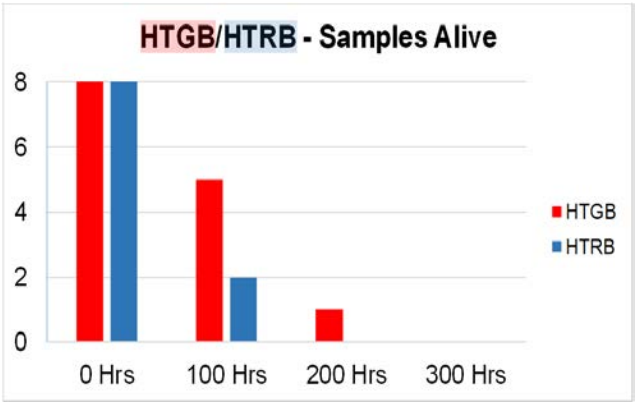


Fig. 2. HTRB and HTGB reliability test results.

Short Circuit Capability of a Medium-Voltage PCB-Based Planar Power Bus

To fully utilize the higher switching speed offered by medium-voltage wide-bandgap (WBG) devices, parasitic inductance must be minimized to limit voltage overshoot at switching transitions. A planar power bus structure can reduce the loop inductance by using larger conductor planes with antiparallel current conduction paths and conductors with minimal spacing. The traditional laminated power bus uses thicker conductors providing a high current capability, but fabrication limitations leave a relatively poor insulation quality due to internal defects such as small air voids. Although the solid dielectric can withstand a higher electric field (E-field) intensity, localized breakdown, or partial discharge (PD), occurs within voids at a much lower intensity leading to premature insulation failure. The partial discharge inception voltage (PDIV) can be increased by increasing the conductor spacing, but this is counterproductive to the goal of parasitic inductance reduction.

A PCB-based bus was implemented utilizing geometric techniques for a well-controlled E-field. The manufacturing process provides less defects allowing the bus thickness to be reduced by approximately 75% compared to the traditional laminated while increasing the PDIV from 5.6 kV to 10.5 kV. Multiple parallel layers were used for +dc and –dc to allow a current handling capability of at least 85 A.

During short circuit (SC) fault events, a high peak current can create a large force on the conductors, especially in high current density areas. This force can effectively peel the copper from the dielectric; thus, voids are introduced and the PDIV is decreased. A SC testbed has been constructed to allow SC testing up to 4500 Apk; see Fig. 1. A new bus is used to determine the initial PDIV and the phase resolved PD pattern (PRPD) is recorded as shown in Fig. 2. Repetitive SC events are generated with 20 seconds between pulses to allow capacitor recharging and ensure no degradation is caused from copper self-heating. Every 20 SC events, the PDIV is checked and PRPD recorded to aid in identifying insulation degradation. This work will be used to further improve the layout of PCB-based buses to ensure the long-term reliability.

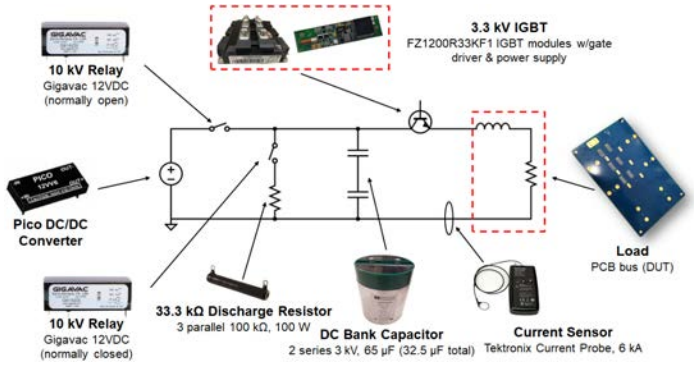


Fig. 1. Short circuit test setup for PCB bus.

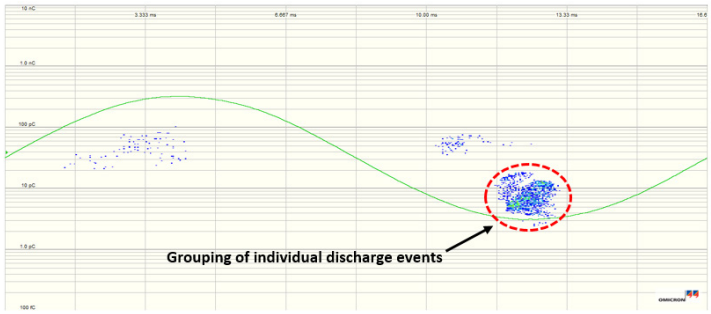


Fig. 2. Phase resolved partial discharge pattern for bus before short circuit testing; PDIV=10.5 kV, QIEC=9.4 pC.

Design of Three-Level Flying-Capacitor Commutation Cells with Four Paralleled 650 V/60 A GaN HEMTs

Increasing power density is one of the most important challenges in power electronics applications in transportation. A Flying capacitor (FC) multilevel inverter is one of the promising topologies for More Electric Aircraft (MEA) power drive system. This paper presents two improved solutions (Vertical and Horizontal commutation cells) for three-level flying-capacitor topologies with four 650 V/60 A (25 mΩ) GS66516T Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) in parallel per switch intended to be used in a 540 V/70 kVA power drive system. These two solutions are optimized considering both topology characteristics and the design of paralleling GaN devices. Both solutions were built and experimentally tested, as a buck converter, under different current levels and the switching performances are compared.

Each leg of the three-level FC inverter is composed of 16 semiconductors as shown in Fig. 1. Different PCB designs were considered using simulation in Ansys Q3D Extractor to define the solutions with lowest power loop inductances given layer symmetry, differential mode (CDM) capacitors, and FC (CFC and CFC'/CFC") ceramic capacitors positioning. In both versions, gate driver circuit, power connector, and the four paralleled GaN HEMTs have the same disposition: two transistors on top layer and two on bottom layer. Beyond the PCB layers routing, ceramic capacitors positioning is the key point to optimize power loop stray inductances, especially for CFC that influences both external and internal power loops shown in Fig. 1. Fig. 2. presents the side view of the power loop of different versions. Vertical version presents more symmetry disposition of layers (6 layers) and 6.4 nH and 5.7 nH of external and internal power loop inductances, respectively. The Horizontal version presents a dissymmetry regarding top and bottom paralleled devices and PCB layers. It has 8 layers but has only 4.4 nH and 3.6 nH for external and internal loop stray inductances. This inductance reduction compared to the Vertical version is due to CFC" (which is an extra CFC). The Horizontal version routing allows an easy way to cascade flying-capacitors cells in series to increase inverter output voltage levels. The Horizontal version presents lower loop inductances at the expense of thicker PCB layers and asymmetry between top and bottom paralleled devices. From the test results of the Vertical version, overvoltage of both internal and external loops are below 10%.

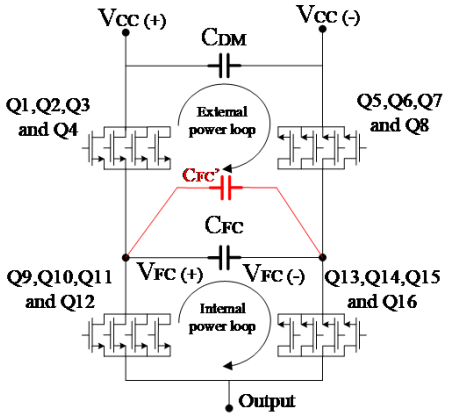


Fig. 1. Three level FC commutation cell with four 650 V GaN HEMTs (GS66516T).

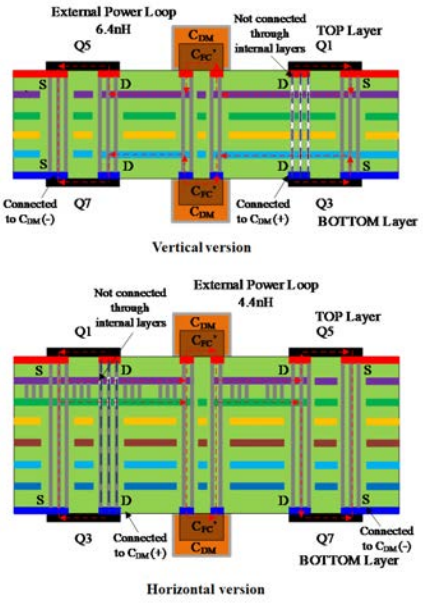


Fig. 2. Side view of the power loop of different versions.

Interpretation of Control Strategies for Modular Multilevel Converter Based on Proposed Decoupled Equivalent Circuit Model

In MMC, due to complicated power flow and coupling between upper and lower arm state variables, the generally accepted control framework proposed by Akagi et al. is difficult to rationalize in an intuitive and simplified manner. Recently, a CPES graduated student, Yi-Hsun Hsieh, proposed a decoupled equivalent circuit model based on state trajectory analysis and coordinate transformation. Unlike the conventional circuit, the proposed equivalent circuit model uses decoupled state variables, which, consequently, can be directly regulated. Fig. 1. shows the generally accepted control framework proposed by Akagi et al. under the decoupled equivalent circuit model. With the help of the circuit model, each detail of control framework is unveiled with a physical understanding, otherwise hidden behind the rigorous mathematics.

Moreover, from the equivalent circuit, two kinds of circulating energies related to v_Σ and v_Δ are identified. The circulating energy related to v_Σ exchanges between input and output while the circulating energy related to v_Δ merely swaps between the upper and lower arms in MMC. Further, two "ideal" control laws, $d_{in}i_{in}=d_oi_o$ and $2d_oi_{in}=0.5d_{in}i_o$ are established to make the circulating energies related to v_Σ and v_Δ zero, respectively. Using these control laws, the control strategies so far existing in the literature to reduce the circulating energies are easily interpreted.

Furthermore, to quantitively visualize the existing circulating energies in each control strategy, the state plane between arm current and arm capacitor voltage (i^u-Nv_c^u) is drawn where the area enclosed by the state trajectory is related to the circulating energy. Furthermore, the state plane between upper and lower arm capacitor voltages is drawn to quantify the circulating energy related to v_Σ and v_Δ separately. Fig. 2. shows the state planes for (a) Akagi's control, (b) improvement based on 2nd harmonic current injection, (c) Voltage gain control, and (d) 2nd harmonic current injection together with voltage gain control. From the state planes, the improvement in terms of the circulating energies can be easily observed.

Therefore, with the help of proposed circuit and state planes, the generally accepted control framework as well as various control strategies to reduce the circulating energies are easily interpreted.

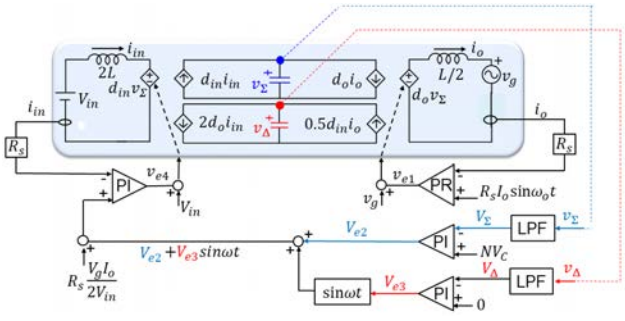


Fig. 1. Interpretation of Control Implementation Proposed by Akagi et al. using Decoupled Equivalent Circuit Model.

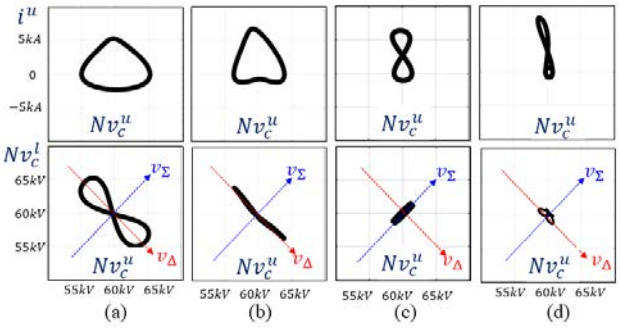
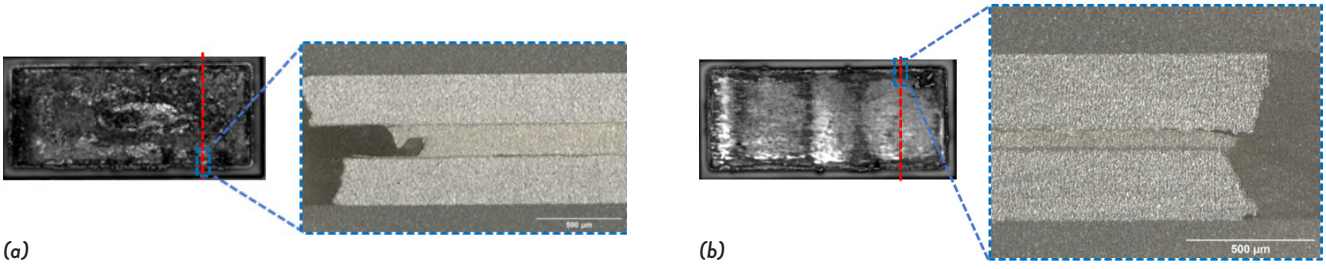


Fig. 2. State planes in various control strategies.

Evaluation of Low-Pressure-Sintered Multi-Layer Substrates for Medium-Voltage SiC Power Modules

Direct-bonded aluminum (DBA) multi-layer substrates have been fabricated using low-pressure silver sintering. AlN DBAs are used instead of DBCs and silver sintering instead of solder to improve the reliability of the multi-layer structure. These multi-layer substrates can be used to reduce the peak electric field strength, screen common-mode noise, and improve mutual inductance cancellation. These benefits are particularly important for medium-voltage (MV) silicon carbide (SiC) MOSFETs due to their high operating voltages, and fast switching speeds. The voiding content and defect density of the sintered bond is critical to the thermal performance and reliability of the power module. Scanning acoustic microscopy (C-SAM) images were used to examine the uniformity and quality of the sintered bond of the fabricated multi-layer substrates. Two large-area silver sintering methods were evaluated: 1) screen-printed nano-silver paste, and 2) stamp-transferred nano-silver preform.

The reliability of the multi-layer structure was evaluated through thermal cycling tests from –40 °C to 200 °C. Fifteen substrate stacks were fabricated for reliability testing. Four samples were bonded with nano-silver paste using 1 MPa pressure, and eleven samples were fabricated with nano-silver preform and either 1 MPa or 3 MPa pressure. The nano-silver preform sintering time is 90 seconds, while the nano-silver paste must be sintered for one hour. The samples fabricated with the nano-silver preform and 3 MPa sintering pressure were the most uniform of the population, according to the C-SAM images. Fig. 1. shows the location of cross-sections taken on samples after 300 thermal cycles. The C-SAM image Fig. 1. (a) suggests voids in the silver bond line for the nano-silver paste sample. The nano-silver preform sample imaged in Fig. 1. (b) showed more uniformity, and no abnormalities are present in the C-SAM image after 300 thermal cycles. The samples shown in Fig. 1. were cross-sectioned, polished, and imaged with a digital microscope. No obvious failure in the bond layer of either sample is shown in either cross-section. However, as shown in Fig. 1. (a), small cracks are observed at the edges of the bond of the nano-silver paste sample. Cross-sections of additional nano-silver paste and preform samples will be imaged after 300, 400, and 500 thermal cycles to better identify the onset and propagation of voids and cracks.



(a) *(b)*

Fig. 1. C-SAM images of (a) nano-silver paste sample before (left) and after (right) 300 thermal cycles from –40 °C to 200°C, and (b) a nano-silver preform sample before (left) and after (right) 300 cycles. Cross-sections are cut and imaged at the dotted red lines after 300 thermal cycles.

Common-Source Inductance-Induced Voltage Overshoot and Self-Sustained Oscillation in Active Bidirectional Switches

Common-source inductance (CSI) is proven to be problematic for high-speed switching. It can slow down switching speed and increase switching losses. Recent research also demonstrated a self-turn-on phenomenon during a device turn-off transient in a simple buck converter. Yet almost no literature investigated the impact of CSI in bidirectional switches. Using a matrix converter phase-leg as an example, this paper aims to first demonstrate and then reveal the mechanism of a unique voltage overshoot and oscillation phenomenon in converters using active bidirectional switches.

Shown in Fig. 1. is a typical commutation phase-leg which consists of two bidirectional devices. The phase current is being commutated from the top branch, S1 and S2, to the bottom branch, S3 and S4. Assuming that VDC > 0 and phase current flows out of the phase-leg, S1 and S3 act as the active and synchronous devices respectively. S2 should be in an off state and S4 in an on state, assuming a current-based commutation strategy is adopted. The LT-Spice simulation results in the top left of Fig. 1. show the voltage across S1 during the turn-off transient. As the CSI increases, a giant overshoot voltage occurs. The phenomenon is also observed in experiments as shown by the bottom graph in Fig. 1.

The CSI in S4 is found to be the major cause of this unusual overshoot voltage. In the S1 turn-off transient, the current slew rate, di/dt, turns the CSI into a voltage source, realizing releasing the gate charge of S4. The voltage across the CSI is proportional to the inductance value, Ls, and the output current squared. It is also highly dependent on the nonlinearity of the device output capacitance, as shown in Fig. 2. With the increase of the drain-source current and the drop of the gate-source voltage, it is possible that S4 is dragged into saturation. If that occurs, S4 becomes a Vgs-controlled current source and the entire commutation phase-leg resembles a three-point oscillator. If the Barkhausen criterion, open loop gain equal to 1, is met, the circuit becomes unstable and can result in a giant voltage overshoot as shown in Fig. 1., or even constant self-sustained oscillation.

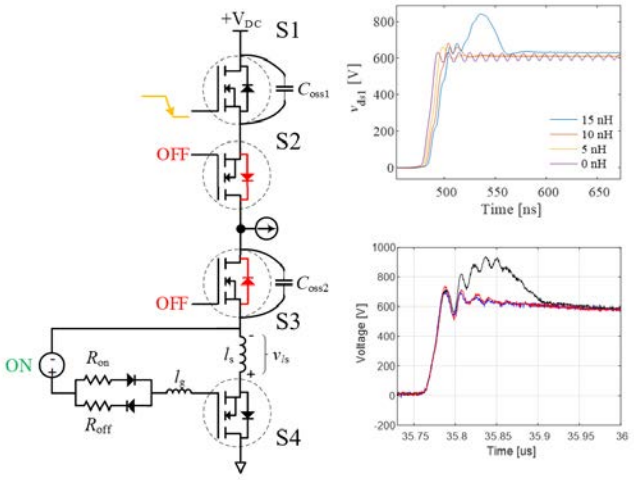


Fig. 1. Commutation phase-leg consists of two bidirectional devices. Top left: Vds1 in LT-spice simulation. Bottom left: Vds1 in experiment.

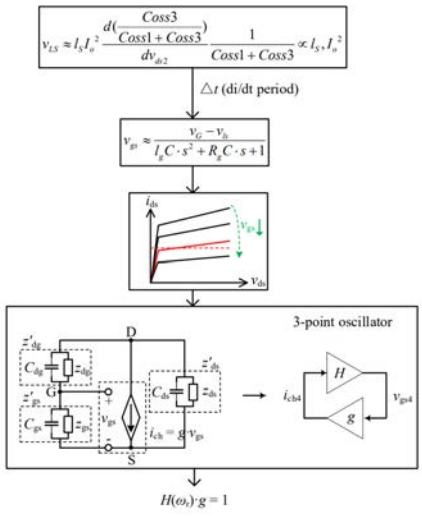


Fig. 2. Mechanism of the CSI-induced voltage overshoot and oscillation.

Characterization of 4.5 kV Charge-Balanced SiC MOSFETs

This work demonstrates a novel charge-balanced (CB) silicon carbide (SiC) MOSFET that boasts a specific on-resistance of 10 mΩ·cm^2 at 4.5 kV breakdown voltage, surpassing the 1-D SiC unipolar limit. This is achieved through buried p-doped regions inside the drift layers (Fig. 1.), which are more easily scalable to higher voltages compared to the p-doped pillars used in super-junction devices. Medium-voltage CB SiC MOSFETs with different p-doped bus widths and pitches designed and fabricated by GE were characterized in this work. The unique microstructure of these devices causes interesting macro-scale characteristics, such as distinctive steps in the capacitance–voltage curves and a turn-on voltage tail that reduces with increased temperature.

A Keysight B1505A curve tracer was used to characterize the CB SiC MOSFETs. The devices with the wide and large pitch bus design (WL) have the lowest on-resistance, while the devices with the wide and small pitch bus design (WS) have the highest on-resistance. Distinct steps in the output and Miller capacitance–voltage curves are caused by a rapid increase in depletion width as the individual depletion boundaries surrounding a single JFET or CB region meet.

A double-pulse inductive switching test (DPT) was used to evaluate the dynamic performance of the CB SiC MOSFETs up to 3 kV. These devices experience a turn-on voltage tail at room temperature caused by the slow transition to conduction of the depleted N-epi layer. The turn-on voltage tail of the devices was found to be dependent on temperature (Fig. 2.), blocking voltage, drain current, and p-bus structure. The turn-on tail is lowest for the type WS devices because they have the highest amount of p-doped bus per unit volume. Operating the SiC CB MOSFETs at higher temperatures reduces the voltage fall time by nearly four times. Above 100° C, the voltage tail becomes essentially negligible.

A 4.5 kV silicon IGBT (IXYX40N450HV) was evaluated using the same DPT setup. At 150° C, the total turn-on energy of the type WS CB SiC MOSFET is more than twelve times lower than that of the silicon IGBT. SiC CB MOSFETs hence offer advantages over silicon IGBTs in higher frequency applications due to their superior switching performance at common operating junction temperatures. The low switching loss at high temperatures, superior relationship between specific on-resistance and breakdown voltage, and simplified fabrication processes of SiC CB MOSFETs makes them uniquely qualified for medium-voltage applications.

Acknowledgement: The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DEAR0000674 advised by Program Director Isik Kizilyalli. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

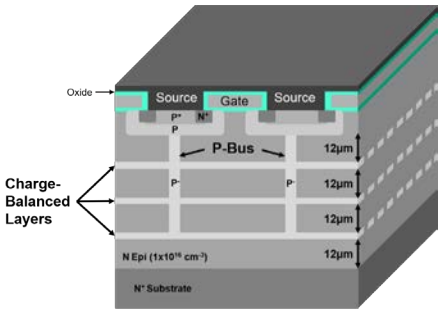


Fig. 1. 4.5 kV SiC CB MOSFET.

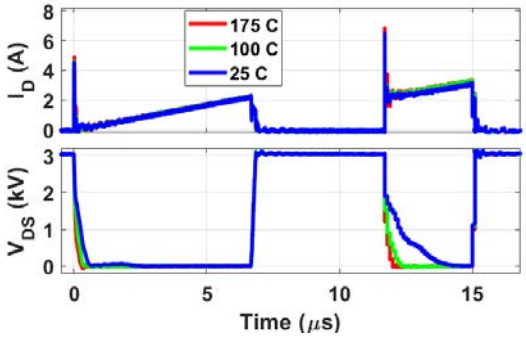


Fig. 2. Switching waveforms at 25° C, 100° C, and 175° C for device type WS.

Design and Analysis of a PCB-Embedded 1.2 kV SiC Half-Bridge Module

This work presents a printed circuit board (PCB)-embedded 1.2 kV silicon carbide (SiC) MOSFET half-bridge module that shows marked improvement over a conventional wire-bonded power semiconductor package in terms of electrical and thermal performance, and manufacturability. The 1.2 kV SiC MOSFET die are embedded in FR4 using embedding technology developed by AT&S. The die electrical connections and thermal paths are created using copper-filled microvias. Embedding the die allows for short conduction paths and small gate and power loops. Steady-state thermal simulations verify that large copper planes in the embedded module allow for increased heat spreading and lower junction temperature compared to a conventional TO-247 package under similar conditions.

The design of this module (Fig. 1.) is based on maximizing the benefits and understanding the trade-offs of the die PCB-embedding technique. The two die are kept far enough apart to minimize thermal coupling, while also maintaining a small power loop. The gate drive circuitry is included in the module to ensure a small gate loop. Copper-filled microvias are used to thermally connect the inner and outer copper layers between the die and the solder mask openings. Copper planes that are electrically connected to the die are designed to maximize power density, while allowing for sufficient heat spreading.

Thermal and electrical FEA simulations were performed on the module. The power and gate loop inductances are 1.8 nH and 2.0 nH, respectively. The double-sided thermal resistance of the embedded half-bridge module is 0.27° C/W. As seen in Fig. 2., the PCB-embedded module has a lower junction temperature than a conventional TO-247 wire-bonded package under similar conditions.

The PCB-embedded, half-bridge module presented here is expected to outperform industry-standard packages both thermally and electrically. Future experimental work includes thermal impedance measurement and analysis, power cycling tests, failure analysis, and converter testing to further explore the benefits and trade-offs of the PCB-embedded 1.2 kV SiC power module.

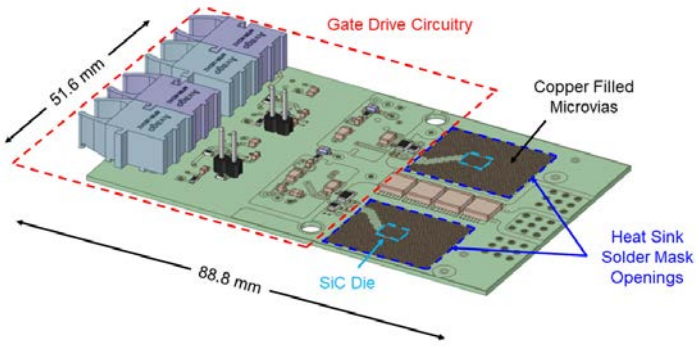


Fig. 1. PCB-embedded SiC MOSFET half-bridge module.

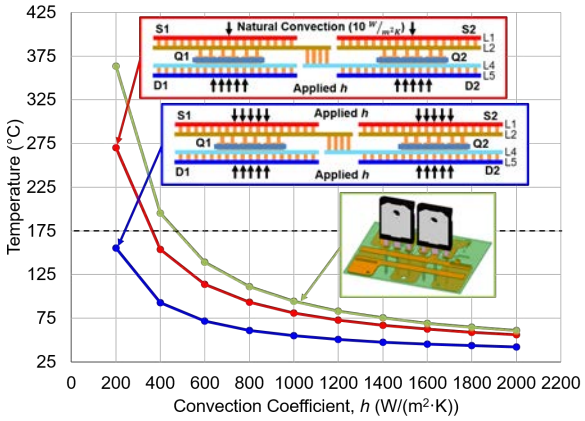


Fig. 2. Simulated junction temperature vs. convection coefficient for the PCB-embedded module with single (red) and double (blue) sided cooling, and a TO-247 package (green).

Sponsored Research Nuggets

Hierarchical Optimization Design of Medium-Voltage Modular Converter-Based Energy Management Systems

Modular converter-based systems become popular options for medium-voltage energy management and power-conditioning systems, which drive major improvements in system development and reductions in system design, inventory, and maintenance cost.

In this paper, a medium-voltage modular converter-based energy management system, as shown in Fig. 1., is constructed to conduct power conditioning from the dc distribution bus to the loads. A pulsed load, which has its loading profile defined, is used as the example to show the hierarchical design and optimization procedure of the energy management of minimized system weight. In this energy management system, a medium-voltage modular converter-based front-end subsystem generates an internal dc bus. A load subsystem that serves the pulsed load is then fed from this dc bus. To filter the pulsed power from the load, a battery bank-based energy storage subsystem is placed in parallel with the front-end subsystem and is connected to the same internal dc bus.

In the hierarchical optimization process of this system, a Morris Method-based sensitivity analysis procedure is embedded in each design hierarchy to rank the design variables based on their importance regarding both the design objectives and design constraints. Genetic Algorithm (GA) is applied in each design level to improve both the design efficiency and effectiveness during the optimization process. In this paper, we will also have a discussion of the terminal dc bus voltage's influence on the system weight and the modular converter's specifications, which result in the optimal system design. Finally, the impact from the system-level design constraints including both the system small-signal stability and the transient response across different dc terminals are taken into account in the system-level design and optimization process. The optimized system weight as a function of terminal design constraints will be shown and discussed for the first time in this paper.

This work was supported by the Office of Naval Research (ONR) under the grant number N00014-16-1-2956.

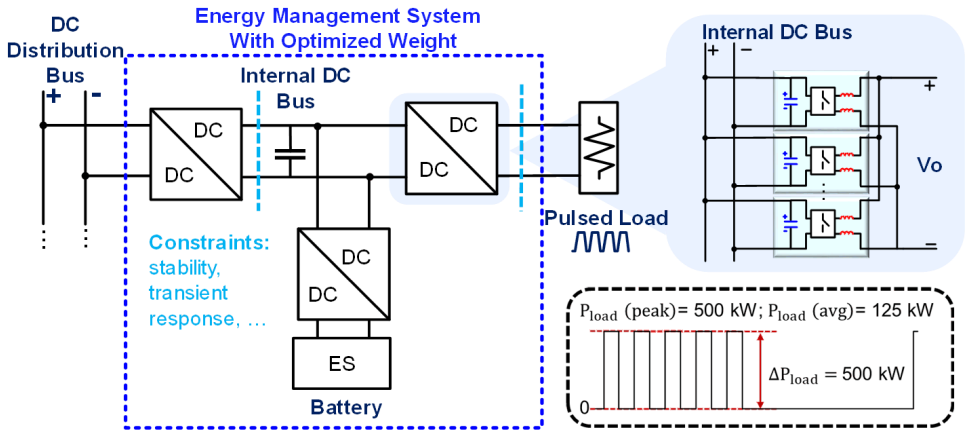


Fig. 1. Schematic of the Medium-Voltage Modular Converter-Based Energy Management System Understudy.

Hard-Switched Overvoltage Robustness of p-Gate GaN HEMTs at Increasing Temperature

An essential ruggedness characteristic of power devices is the capability to withstand the transient overvoltage in power electronic applications. As the newly commercialized GaN HEMTs can switch faster under higher voltage biases, it is important to identify their true overvoltage limitations in transient switching events. This work characterizes the transient overvoltage capability and failure mechanisms of GaN HEMTs under hard-switched, turn-off conditions at increasing temperatures, by using a clamped inductive switching circuit with a variable parasitic inductance as shown in Fig. 1. (a). This test method allows flexible control over both the magnitude and the dV/dt of the transient overvoltage. The overvoltage robustness of two commercial enhancement-mode (E-mode) p-gate HEMTs was extensively studied: one with the Ohmic-type gate (HD-GIT) and the other with the Schottky-type gate (SP-HEMT). The experimental motherboard-daughtercard system is shown in Fig. 1. (b).

Tests were conducted with varying parasitic inductance (L_D) values and increasing current values to measure the overvoltage magnitude. The failure of the two devices was found to be determined by the overvoltage magnitude rather than the dV/dt. Tests were then repeated with L_D = 130 nH but at increasing temperatures (100° C and 150° C). The failures of both devices were consistent with room temperature results and results are shown in Fig. 2. Overall, this work shows the robustness of two commercially available p-Gate GaN HEMTs under overvoltage switching stresses and increasing ambient temperatures.

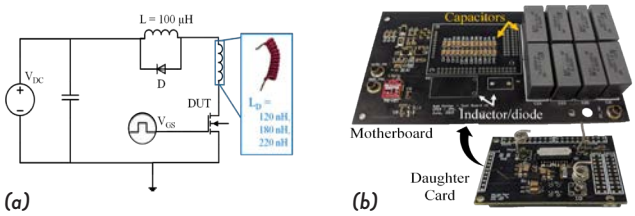


Fig. 1. Clamped inductive switching circuit schematic and external parasitic inductance (a), the experimental test circuit that includes the motherboard for the primary power loop and the daughter cards for the minimized gate driver loop and sensing circuitry (b).

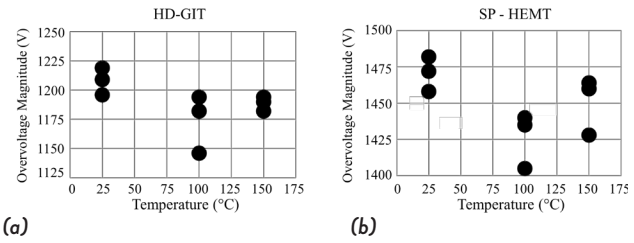


Fig. 2. Overvoltage failure magnitudes measured at different temperatures for the HD-GIT (a) and SP-HEMT (b).

Gate-Driver Integrated Junction Temperature Estimation of SiC MOSFET Modules

SiC MOSFET power modules are becoming a global solution in environment-harsh systems due to the benefits of higher power density and efficiency. Intelligence on the gate driver can lead to significant improvement of both short-term and long-term reliability by providing insight on real-time behavior of relevant switch information. Device switch-current Id can be used for short-circuit detection assessing the short-term reliability. In combination with V ds,on, the on-state resistance R ds,on and thus online junction temperature (Tj) estimation is possible. This enables monitoring the status of the SiC MOSFET device such as state of health, remaining useful life, maintenance scheduling, etc., tackling the long-term reliability aspect.

Intelligent gate driver is developed containing described measurements and is shown on Fig. 1. Rogowski coils are utilized for switch current measurement exhibiting high bandwidth and accuracy while not imposing on power density. So-called two diode circuit is utilized as an on-state voltage measurement sensor due to benefits such as high blocking capability, no offset problem, temperature independency, low losses, great accuracy, and sensitivity. Online junction temperature estimation will be performed with the aid of Field Programmable Gate Array (FPGA), that will sample current and voltage information at the same time. Based on the calibration results of the device stored in the Flash memory (temperature look-up table) on the gate driver, FPGA will assess and compare voltages and currents, thus returning estimated junction temperature. Fig. 2. shows temperature estimation results during double pulse test with pre-set to temperature of 100° C. Accuracy of the method throughout the whole tested temperature range (30-135° C) is higher than 96%, with absolute repeatability of 1.5° C showing great promise. Furthermore, a generalized junction temperature monitoring procedure is proposed, avoiding often complicated calibration procedures. The accuracy of this approach is relatively high, improving on and avoiding tremendous errors that would occur by implementing datasheet extracted thermal map and relying on temperature estimation by datasheet.

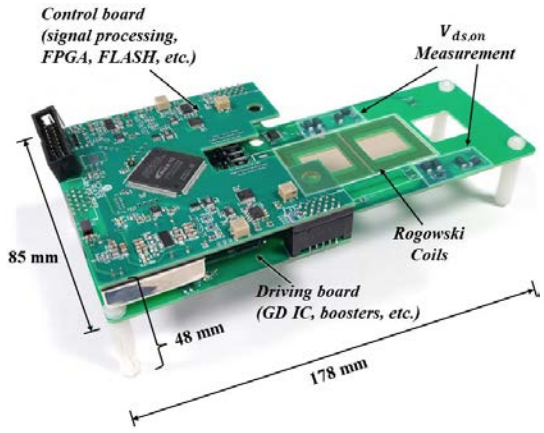


Fig. 1. Intelligent gate driver capable of measuring switch currents, voltages and temperature estimation.

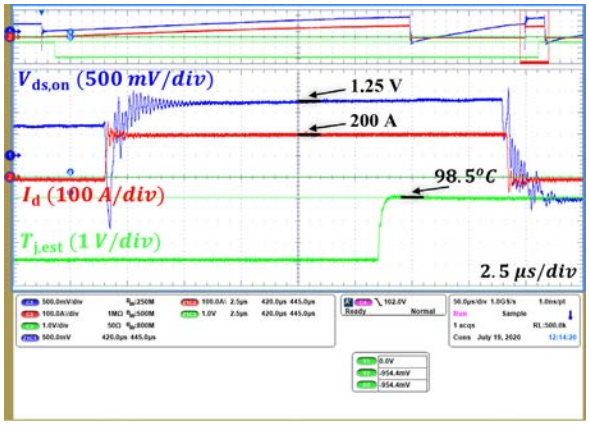


Fig. 2. Double-pulse test verification at 100° C. Ch1 (blue) is on-state voltage, Ch2 (red) is switch current, and Ch3 (red) is estimated junction temperature.

Rogowski Switch-Current Sensor Self-Calibration on Enhanced Gate Driver for 10 kV SiC MOSFETs

Modular multilevel converters (MMC) are increasingly considered in medium-voltage (MV) applications due to features such as modularity, voltage scalability, and transformer-less operation. If the power cell's kernel piece is SiC MOSFET, the design will be able to meet high-density and efficiency. The pinnacle of SiC technology is the 240 A, 10 kV SiC MOSFET XHV-6 module. For switching cycle control of MMC requirement is accurate analog information. Thus, a high-bandwidth, Rogowski current sensor (RSCS) is developed and integrated on the enhanced gate driver (eGD) to serve as peak-current-mode control sensor, short-circuit detector, and as a phase-current sensor by sampling the switch current (prototype shown in Fig. 1.). Each switch position requires 3 RSCSs.

Due to known non-idealities of the OpAmp integrator circuit such as input offset voltage and input bias current, an offset calibration circuit is necessary for successful integrator use. Mechanical potentiometer is not ideal due to temperature swings and mechanical parts that reduce usable lifetime. Generally, electrical parts are more reliable and have longer lifetime. Therefore, digital potentiometer instead of analog is proposed. Calibration circuit with ADC, FPGA, and DPOT is implemented during start-up, shown on Fig. 2. (a)., for one out of three RSCS. SRST sequence is first initiated. Due to existence of non-idealities, we will see ramp increasing until the reset occurs. Towards the end of the SRST enable, FPGA will initiate ADC to sample. If sampled value is higher than maximum allowable error, FPGA will reconfigure the digital potentiometer (DPOT), thus reducing the influence of non-idealities in the next cycle. This process will be repeated until the error becomes satisfactory. Verification of the implemented algorithm is shown at Fig. 2. (b). Good resolution of the system is achieved, with maximum error of the system of ± 2.5 A. Self-calibration process is finished relatively quickly during start up, within 12.4 ms maximum.

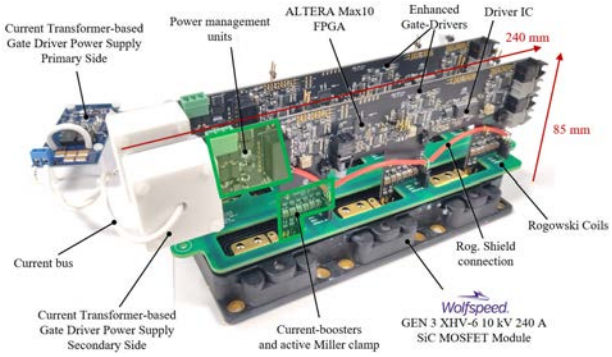


Fig. 1. 10 kV SiC MOSFET enhanced gate driver with indicated constitutive parts.

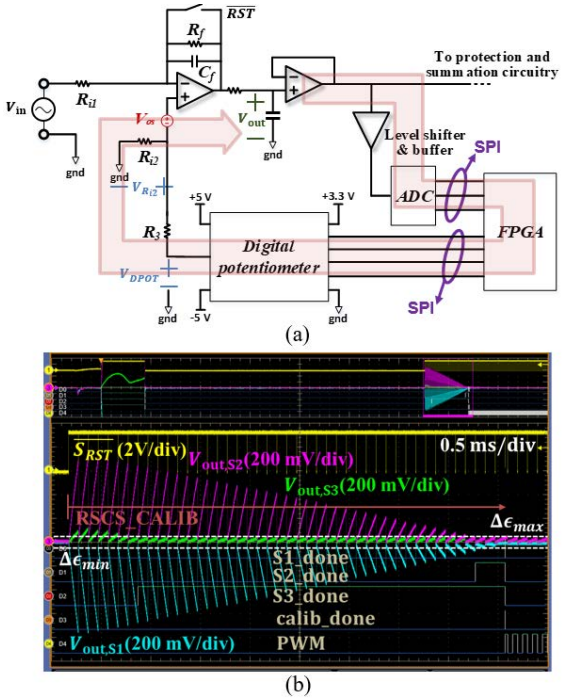


Fig. 2. (a) Rogowski switch-current sensor fundamentals and digital offset calibration, (b) Self-calibration experimental results at startup of GD.

Insulation Design of Wireless Auxiliary Power Supply for Medium-Voltage Converters

Auxiliary power supply (APS) that provides reliable power and voltage for gate drivers, controllers, and sensors is a critical component in a medium-voltage (MV) converter. Compared to being fed from the power-cell dc-link, APS fed from an external earthed system has its own benefits. However, with the power-cell number scaled up, the insulation design of the externally-fed APS becomes a significant challenge. Partial discharge (PD) can cause accumulative irreversible damages of insulation, which further lead to auxiliary power circuit fault and eventually cascaded failures of the whole converter system. Therefore, a PD-free APS system ensuring the reliability of MV converter is required. Among different technologies for building APS, wireless power transfer (WPT) becomes an attractive method because of its mechanical design flexibility and inborn insulation capability. In this paper, in order to design a PD-free WPT converter, insulation design criterion and electric field distribution under different coil geometries are analyzed, compared, and tested. Subsequently, a comprehensive insulation design including the influence of ferrite shielding layer is shown. Finally, an optimized WPT prototype with 120 W output power, 92.78% full-power efficiency, 2.76 pF isolation capacitance, and 27 kV insulation capability is validated experimentally. Fig. 1. shows the FEA simulation resulf of the maximum E-field intensity of the coil pair with different outer radius ro, distance between two coil d, and coil winding thickness rw. Fig. 2. shows the test bed designed to verify the insulation design of the coil pair.

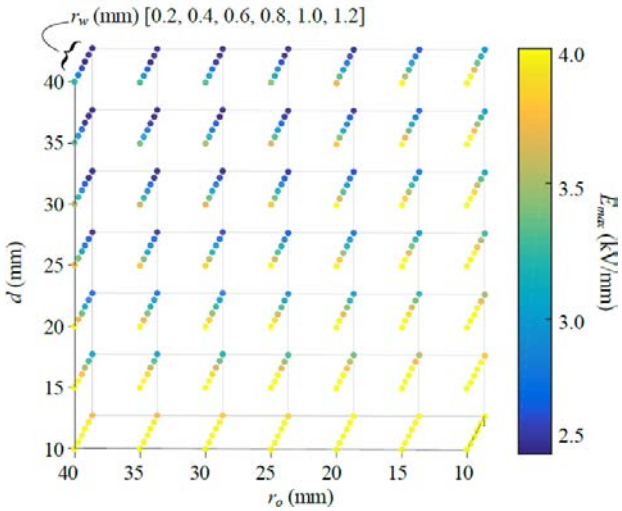


Fig. 1. FEA simulation result of maximum E-field intensity in air with different geometrical parameters of coils.

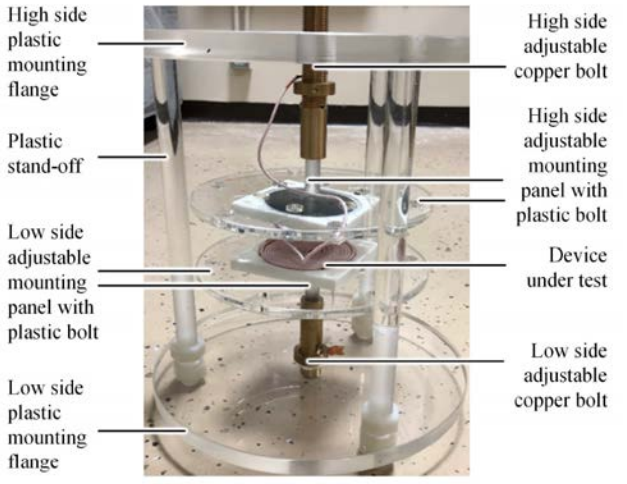


Fig. 2. Test bed for insulation verification.

Enhanced Gate Driver Design for SiC-Based Generator Rectifier Unit for Airborne Applications

Wide-bandgap (WBG) semiconductor devices, such as silicon carbide (SiC) MOSFETs, have emerged increasingly as a viable alternative to silicon (Si) IGBTs in airborne applications. The gate driver, as the adjacent electronic unit to SiC MOSFET modules and the essential interface between control system and power stage, is facing significant challenges. The move to higher voltages and the more compact packages of WBG semiconductor devices challenge the insulation design. In particular, the low-pressure working condition of the aircrafts degrades gas dielectric strength, which leads to an increased risk of partial discharges. To avoid discharges, a safe clearance distance should be maintained; however, only one standard, IEC 60664-1, provides an altitude correction factor of 6.67 at 50,000 ft., which might lead to overdesign that reduces the system power density. Instead of adding oversized correction factor of standard, insulation coordination is defined utilizing Paschen curve. The breakdown E-field Ebk converted from Paschen curve is shown in Fig. 1., where d is the distance between two conductors. As seen, Ebk decreases and infinitely approaches 600 V/mm as d increases. A safety margin of 50% is added to account for intensified fields. Therefore, the targeted peak E-field Epk in the proposed gate driver is below 300 V/mm.

Printed circuit boards (PCBs), with advantages of low profile, low cost, and perfect fit for automated manufacturing and mass production, have been widely used as carriers of electronic components. As solid insulators, they have a much higher dielectric strength (> 40 kV/mm) compared to dry air (3.3 kV/mm). With this feature, electric-field (E-field) management is applied to the layout design. By properly designing the field control plates, the peak E-field was shifted from the air to the PCB dielectric, effectively reducing the field strength along the surface of the PCB in air.

In this work, a gate driver for SiC-based GRUs for variable frequency airborne applications is designed. The hardware assembly is shown in Fig. 2. The size of the gate driver is 133 mm x 62 mm 23.8 mm. Rogowski switch current sensor (RSCS) is implemented in this gate driver to provide a fast and reliable fault detection mechanism that meets the narrow and inconsistent short-circuit withstand time requirement of the SiC MOSFETs.

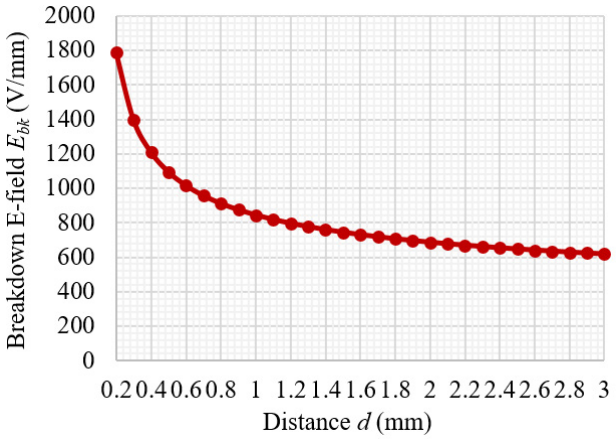


Fig. 1. Breakdown electric field Ebk versus distance.

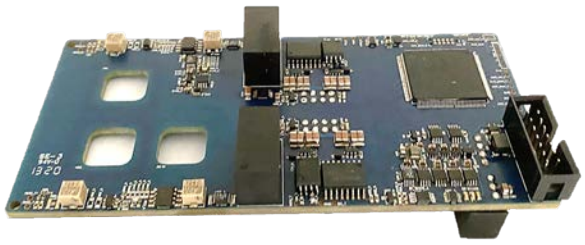


Fig. 2. Enhanced gate driver for airborne application.

Series-Resonator Buck Converter for Data Centers and Automotive Power Distribution Systems

Interleaved multiphase buck converters have been adopted for point-of-load regulation below 3.3 V and above 10 A from input voltage exceeding 12 V. The Series-Capacitor Buck (SCB) converter was synthesized by adding a series capacitor in a two-phase buck converter to reduce voltage stresses under steady state. Side benefits include doubling of the duty cycle, reduction of the switching loss, and equalization of the phase currents. Hard switching has hindered efforts to reduce volume via increasing the switching frequency, although a monolithically integrated SCB converter has boosted current density exceeding 60 A/cm^3. The efficiency dropped by 5%, owing to the switching loss, as the frequency increased from 1 MHz to 3 MHz.

The Series Resonator Buck (SRB) converter is synthesized by adding a parallel resonant tank next to the series-capacitor Cs, as demonstrated in Fig. 1. All switches turn on into zero-voltage (ZVOn), and low-side switches turn off from zero-current (ZCOff). No snubber is needed to keep the switches' stresses within the input voltage. A 2 MHz prototype with 48 V at the input, and 7 V, 20 A at the output, was built to verify the design.

The peak efficiency of the RSCB prototype is 98.5%, and the full load efficiency is 97.3%, as shown in Fig. 2. The measured drain-source voltages of all switches at nominal condition are shown. All switches turn on into zero-voltage.

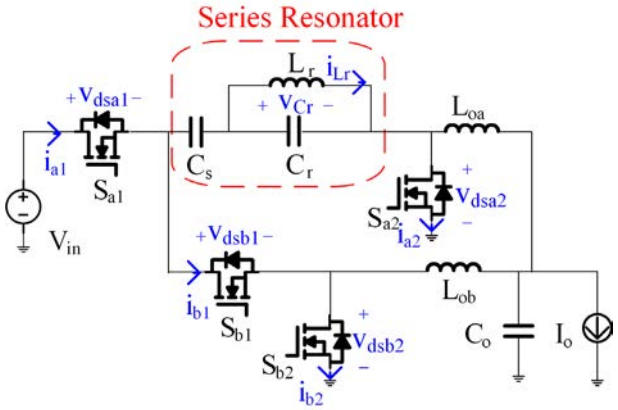


Fig. 1. Series-Resonator Buck (SRB) converter.

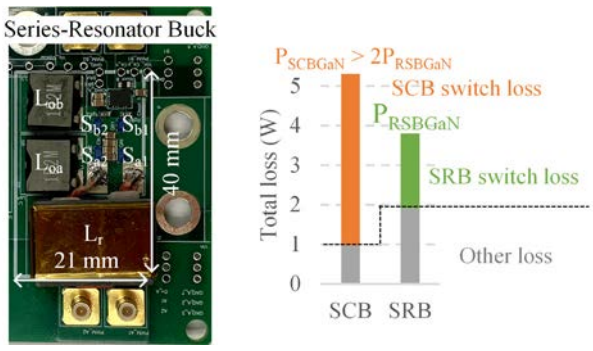


Fig. 2. Prototype and loss reduction compared with a conventional SCB converter.

Switching Current Measurement Based on Power Module Parasitics

Current and voltage sensors play important roles in electric drive systems. Switching current sensors help protect the power MOSFET module from a short-circuit event. Thus, good sensor design increases the reliability of the overall electric drive system.

In recent years, some advanced techniques, which are suitable for high-power MOSFET modules, have been developed. In some research works, the Rogowski coil is integrated into the gate driver for both short-circuit protection and current reconstruction. However, the PCB design of the on-board Rogowski coil is complex, and the coil also consumes a large space in the circuit. The current sensing for short-circuit protection based on parasitic inductances of the power MOSFET module is one of the simple yet effective methods. Although a good protection can be achieved, the current waveforms cannot be recovered due to the high-pass filter characteristic that rejects all low-frequency components in the measurement current.

This paper proposes a current sensor design based on the power module's parasitics. The experiment setup of the double-pulse test using the designed current sensor is presented in Fig. 1. Besides the simplicity in the configuration, the method provides a good switching current sensing, as shown in Fig. 2.

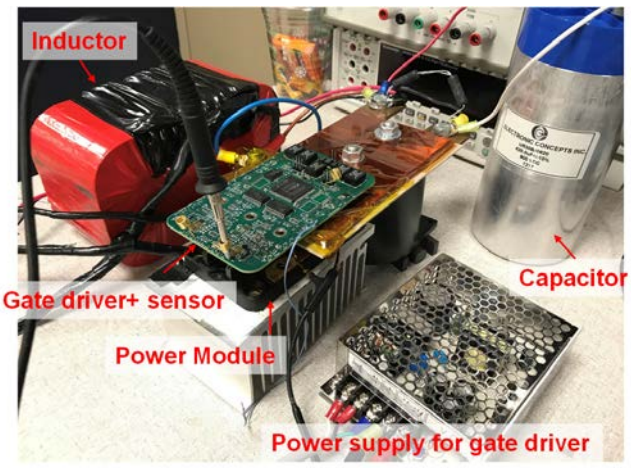


Fig. 1. Experiment setup of the double-pulse test using the proposed current sensor.

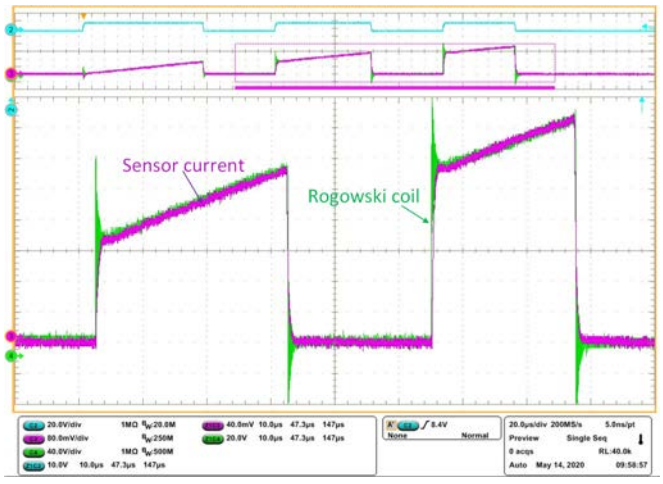


Fig. 2. Measured switching current waveform with the designed current sensor.

A Distributed Communication and Control System for Modular Power Converters with Sub-ns Synchronization Accuracy

The distributed control architecture shows an advantage over the centralized control architecture in large-scale, multi-node power electronics applications owing to its modularity. In the distributed control and communication network, PWM signals are modulated in each PEBB controller based on its own FPGA. Due to the uncontrollable latency among different PEBB controllers, the synchronization becomes a critical issue. It is necessary to ensure the synchronous operation to follow the desired modulation scheme. With the high switching frequency in SiC-based modular converters, the high synchronization accuracy (nanosecond range) is required. In this paper, a White Rabbit (WR)-based digital controller is developed, and the synchronization performance is evaluated in a four-node communication network with sub-ns synchronization accuracy.

A synchronization diagram is shown in Fig. 1. based on the WR protocol. Considering a master node and a slave node connected in a bidirectional optical fiber link, the synchronization logic is implemented in each node for the timestamping of t1, t2, t3, and t4. The phase detector in the master node measures the phase difference between master reference clock and recovered clock, phase M. With phaseM embedded in the packet and received by the slave node, the slave node adjusts the frequency of a voltage-controlled crystal oscillator (VCXO) within the closed-loop PLL, and generates a local clock synchronized with the master reference clock. The closed-loop PLL mainly consists of software-based phase detector and PI controller, and hardware chips including DAC, VCXO, and clock multiplier.

A communication network including one master and three slave PEBB controllers in a linear daisy chain topology is built in order to verify the synchronization performance. The controllers are connected through SFP transceivers running at 5 Gbps. The FPGA local clock frequency on each controller is set to be 125 MHz, and a local time counter is generated based on its own clock, which is utilized to coordinate the synchronous operation of different controllers. A square wave based on the local time counter is utilized to measure the synchronization accuracy among different controllers. The synchronization performance for four nodes is shown in Fig. 2. Keeping the system running for around 2 hours, the jitter (peak to peak) of 1 ns is observed. The total sampling points is 182,280 samples.

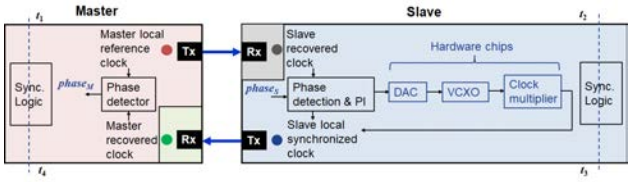


Fig. 1. Synchronization diagram between the master and slave node.

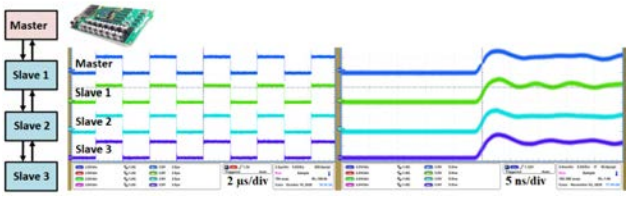


Fig. 2. Synchronization accuracy measurement.

A Constant-Current ZVS Class-E DC-DC Converter with a Loosely Coupled Transformer with PCB Windings

Current source is used in gate drivers, battery chargers, and wireless power transfer. A Class-E converter is a good candidate for the application because only one switch is required and ZVS is achieved. This work proposed an isolated class-e dc-dc converter with constant-current (CC) output and ZVS over a wide load range with finite input inductance. An air-core transformer is used for the isolation stage for lower profile and elimination of core loss. The air-core transformer with PCB winding has two planar layers. The radius is 5 mm. The drawing of the air core transformer and the hardware is shown in Fig. 1.

The converter can be separated with a Class-E inverter and a compensation network. The Class-E inverter can be equivalized with a voltage source in series with a capacitor. The fundamental output voltage can be constant if the capacitor is compensated at a certain switching frequency and the load is resistive. The CC output is realized by adding a CLC network to the Class-E inverter. Capacitor C1 and C2 compensate the self-inductance at the primary side and secondary side to realize a resistive load. For duty ratio (D) equal to 0.5, the switching frequency needs to be 1.29 of the resonant frequency of Lin and Cin. The leakage inductances Ll1 and Ll2 need to be large enough to suppress high-order harmonics. In this work, the self-inductance is 600 nH and mutual-inductance is 360 nH. The switching frequency is 6.78 MHz and the output current is 700 mA.

Fig. 2. shows the testing results with 10 V input and different load-resistances. ZVS is always maintained within the load range and output voltage increases linearly with the load-resistance, which is the characteristics of CC output. The peak efficiency of the converter is 80%.

In summary, this work demonstrated the principle of realizing CC output on the Class-E dc-dc converter with an air-core transformer. The work can be a good candidate for high-temperature and low-profile applications with the elimination of magnetic cores. The efficiency can be further improved by optimizing the air-core transformer and will be discussed in the future.

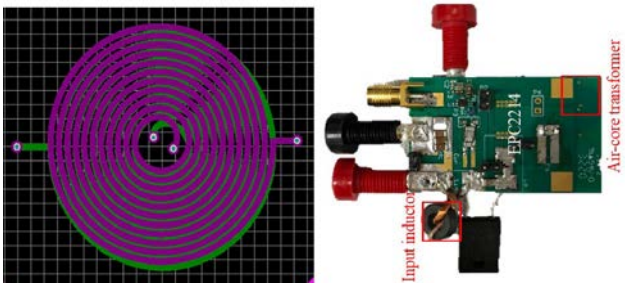


Fig. 1. The drawing of the air-core transformer and the hardware.

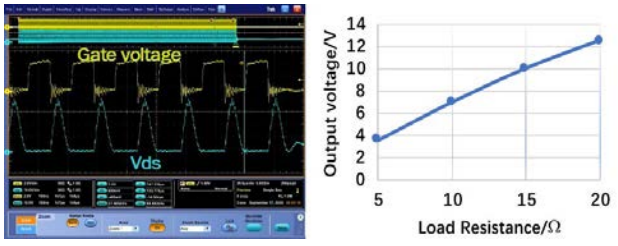


Fig. 2. Testing waveforms and outptut characteristic of the converter.

Real-Time Network Protocol for Gate Driver Communication and Control

The conventional approach for a controller to control gate drivers in a power electronics system is to send pulse width modulation (PWM) pulses from the controller to the gate drivers (usually two, four, or six are connected to one controller) and to do ADC conversion of signals from sensors as feedback to apply control. This is not a modular nor flexible approach since the controller usually has a limited number of inputs for sensors and a limited number of outputs for gate drivers. Additionally, modern gate driver modules have voltage, current, and temperature sensors for protection purposes, and a fault signal is sent as a signal to the gate driver. The main idea is to have a distributed system so that each sensor and gate driver can communicate with the controller and between them using some communication network and protocol. This time gate driver (GD) should be "smart" enough to receive commands from the controller and that some parts of control happen inside the GD itself. This way, the number of sensors could be reduced because gate drivers' sensors could be utilized for control purposes. Also, flexibility and modularity could be significantly increased. Control could be divided and distributed so that low-level control could be done in the gate driver.

Fig. 1. shows the internal structure of one power cell. As could be seen, it consists of two gate drivers for top and bottom devices, voltage, temperature sensors, and the local controller. Power cells could be combined to achieve the desired topology. Clock for synchronization purposes is not regenerated from communication, but it is physically distributed between the local controller and GDs. This approach brings good synchronization using relatively inexpensive communication hardware.

The key element of a system like this is synchronization between GDs and controller(s) (nodes of the system). Synchronization is tightly coupled with communication. The synchronization of timers in nodes is based on PTP (Precision Time Protocol – IEEE 1588). Synchronous timers allow us to "tell" GD or controller to execute some action at the exact moment with nanosecond precision. Fig. 2. shows the 8th bit of timers. It could be seen how well timers on the controller and both gate drivers are synchronized. It could be seen that the jitter is very small (~ 1 ns), and that the latency is in the two ns range.

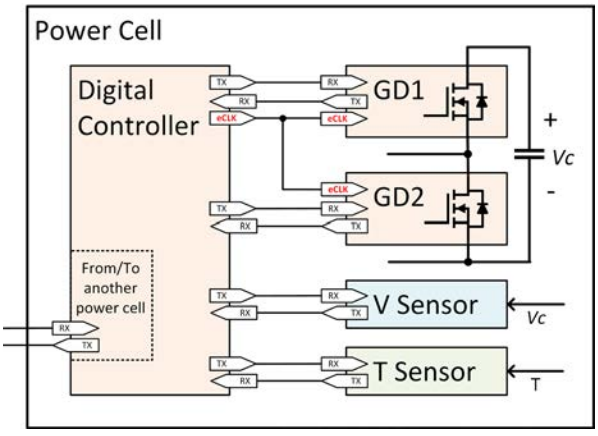


Fig. 1. Structure of the power cell.

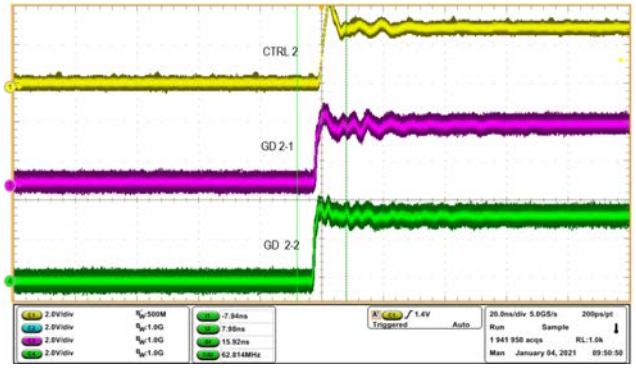


Fig. 2. Timers synchronization.

Design of Insulation System in High-Frequency Auxiliary Power Supply for Medium-Voltage Applications

10 kV SiC MOSFETs enable high-frequency power conversion solution in medium-voltage applications as it leads to a smaller converter size and better performance. However, as a consequence, the auxiliary power supply (APS) design becomes more challenging. To ensure the device's safe operation, it requires the APS to achieve a high isolation level, low coupling capacitance (Ccm), and small footprint. Since these three requirements are difficult to achieve at the same time, design balances exist in the APS design.

This work first presents the circuit design of a 1 MHz current-fed APS using LCCL-LC resonate topology with a single-turn transformer to reduce the overall size and realize multi-load driving ability. Then, based on the designed APS, eight insulation schemes using different dielectric materials and electric-field (E-field) stress control techniques are introduced. In the analysis, FEM and Q3D simulations are performed to evaluate the E-field distribution and Ccm value for each solution. Considering insulation capability, manufacturability, and Ccm values, as shown in Fig. 1., two designs using air and silicone as insulation materials are selected and evaluated by hardware experiment.

As shown in Fig. 2., with a threshold discharge value of 10 pC, the air-insulated design can achieve PD free of 5.8 kV with measured Ccm value of 1.25 pF. Due to higher dielectric strength, the silicone-insulated design achieves a higher partial discharge inception voltage of 16.4 kV with Ccm value of 3.9 pF. Both designs are able to drive a maximum power of 20 W without any thermal issues. Although in this work, only two solutions are built, all proposed insulation schemes can be applied to other APS system designs.

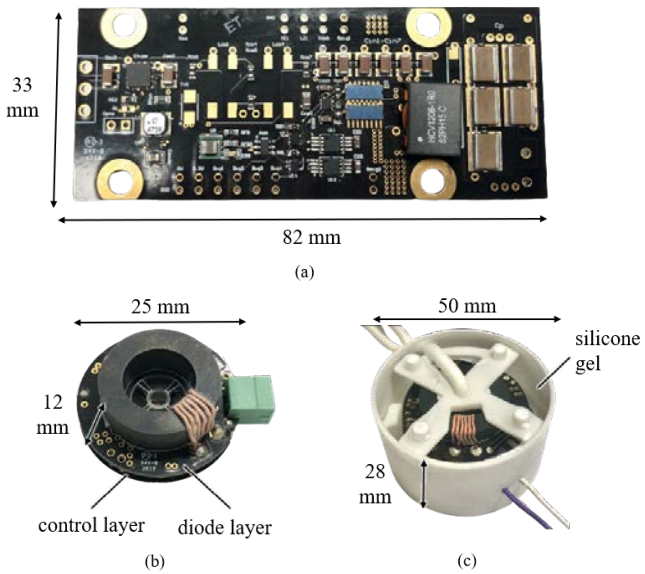


Fig. 1. Hardware prototypes of (a) sending side circuitry (b) air-insulated receiving side circuitry and (c) silicone-insulated receiving side circuitry.

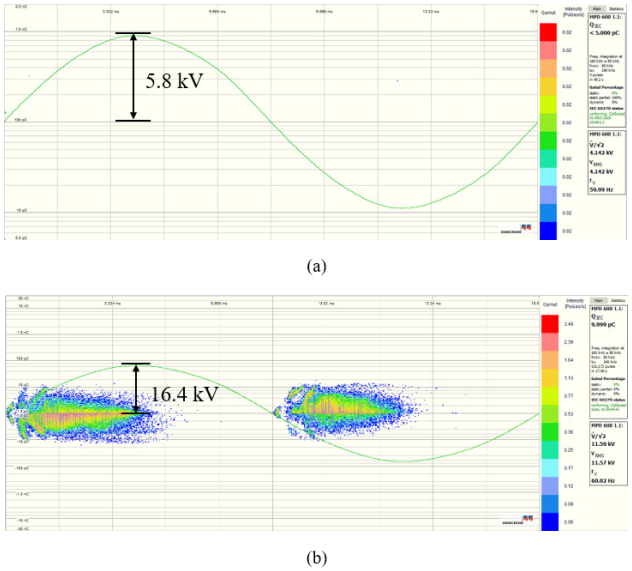


Fig. 2. PD test results for (a) air-insulated design (b) silicone insulated design.

15 kW Step-up Mode SiC Matrix Converter Design with 3D Commutation-loop Layout and PCB Aluminum Nitride Cooling Inlay

Matrix converter (MxC) is a direct frequency changer where bidirectional switches are used to directly interface two ac systems. It features low switching loss, small electromagnetic interference (EMI) filter, and potentials for achieving high-power density. By employing a current control mode (CCM) operation, MxC can work in step-up mode, thus extending the operation of MxC for power generation and distribution applications. This article aims to demonstrate a 15 kW 380:460 V step-up mode SiC MxC prototype.

First, as a key component of MxC, bidirectional device configuration is selected based on the trade-off between digital controller and powerline electromagnetic emissions. It is found that the common-source configuration for the bidirectional switch exhibits reduced noise emission at the controller side while the common-drain configuration benefits the power-line noise reduction. Second, as surface-mount device features low manufacturing cost, compact package, and low stray inductance, surface-mount instead of through-hole SiC MOSFETs are adopted. To solve the concern on the heat dissipation, a thorough evaluation on surface-mount device cooling approaches is provided. Thermal via, metal-core PCB and aluminum nitride inlay cooling approaches are considered. The PCB aluminum nitride cooling inlay stands out to be an effective cooling approach which can handle high per-device loss (24 W) with very limited impact on PCB layout flexibility. 3D vertical commutation-loop methodology is then employed to achieve small and symmetrical loop inductance for the 3 coupled commutation loops in a MxC phase-leg. Clean and symmetrical switching transient test results are provided to verify the 3D loop design. A highly integrated 15 kW MxC prototype is eventually demonstrated with a power density of 15 kW/l and 20 kW/kg, as shown in Fig. 1.

The prototype exhibits a full-load efficiency of 99% and is compliant with DO-160G standard. The CCM operation is experimentally verified on the prototype where the 380 V generator voltage is boosted by the MxC to establish a 480 V three-phase ac bus, as shown in Fig. 2.

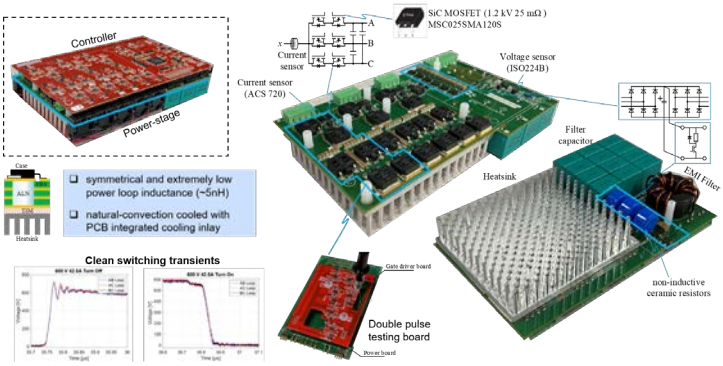


Fig. 1. SiC matrix converter power stage design.

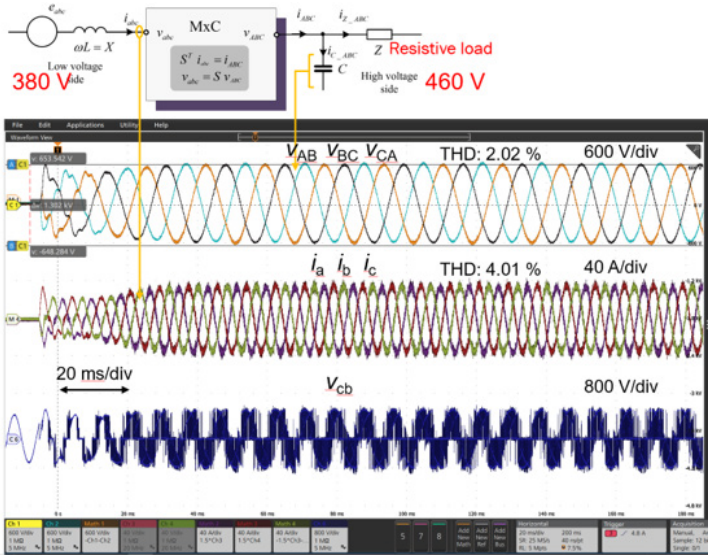


Fig. 2. Matrix converter step-up mode operation. The 380 V generator voltage is boosted to 460 V to establish a three-phase AC system.

Digital Implementation of the Multi-Cell Switching Cycle Control for Modular Multilevel Converters

A modular multilevel converter (MMC) features modular design, scalability, high power quality, and tolerance of failures. However, a conventional MMC suffers large-cell voltage ripple especially at low-frequency output. Switching cycle control (SCC) effectively eliminates this voltage line-frequency dependence, even enables the dc-dc mode operation of MMC benefiting a more than 100 times shrinking on required cell capacitance. Using 2-cell per-arm MMC as an instance, Fig. 1. demonstrates the typical working principle of the multi-cell SCC in dc-dc mode. To ensure the switching cycle capacitor voltage balancing, the top and bottom arm currents (iu and iL) are intentionally shaped to ensure the charge balancing of capacitor voltages (vcu1, vcu2, vcL1 and vcL2). Peak-current mode (PCM) modulation combined with on-line calculated current boundaries are adopted to precisely shape the arm currents, which is paramount for the SCC. As shown in Fig. 1., assuming the phase current flows out of the MMC phase-leg, the cell connection signals of the upper arm and lower arm (Su1, Su2, SL1 and SL2) are determined by average current mode and PCM modulation, respectively.

For MMCs, distributed control with a high degree of flexibility and scalability is obviously preferred. Yet the segmented arm current shaping in SCC demands nano-second synchronization accuracy among different controllers, which poses great challenges on digital implementations. In this article, based on the timing scale and accuracy, the SCC is separated into 3 control layers: naming the application control, converter control, and switching & hardware control layers. Control layer features are carefully investigated and mapped to custom-build distributed controller clusters with sub-nano-second synchronization accuracy, as shown in Fig. 2. The switching & hardware control layers are implemented with dedicated CPU cores, while the other two control layers are implemented by a cloud of high-end controllers with reconfigurable CPU functions to enable a high degree of flexibility and reliability. Communication, task tables, and a scheduler mechanism are designed to coordinate the controller cloud. A detailed timing chart is also provided to help demonstrate and minimize possible digital delays in the system. The digital implementation is verified on a 4-cell per arm 2 MW 24 kV MMC in both dc-dc and dc-ac operations.

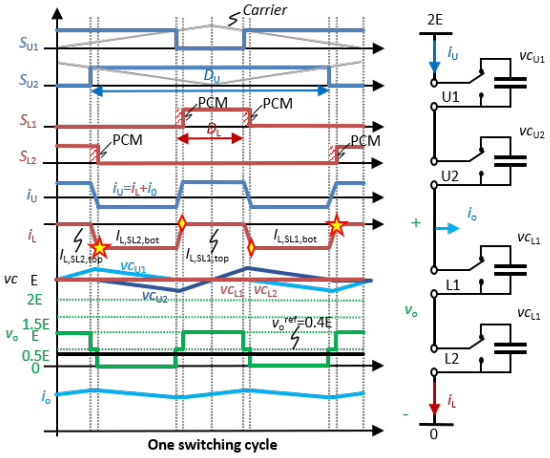


Fig. 1. Working principle of multi-cell switching-cycle control (2-cell per arm as an instance).

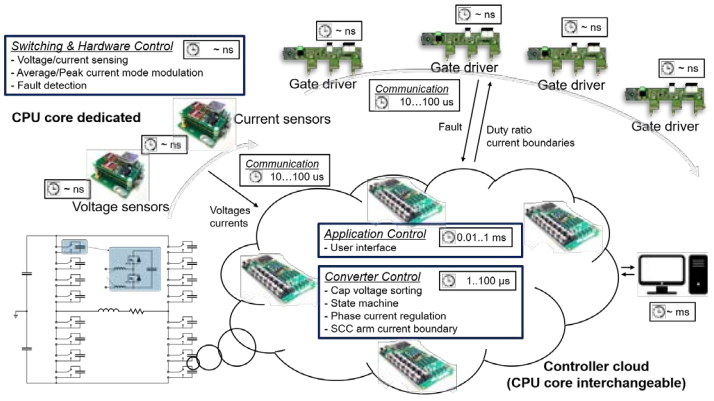
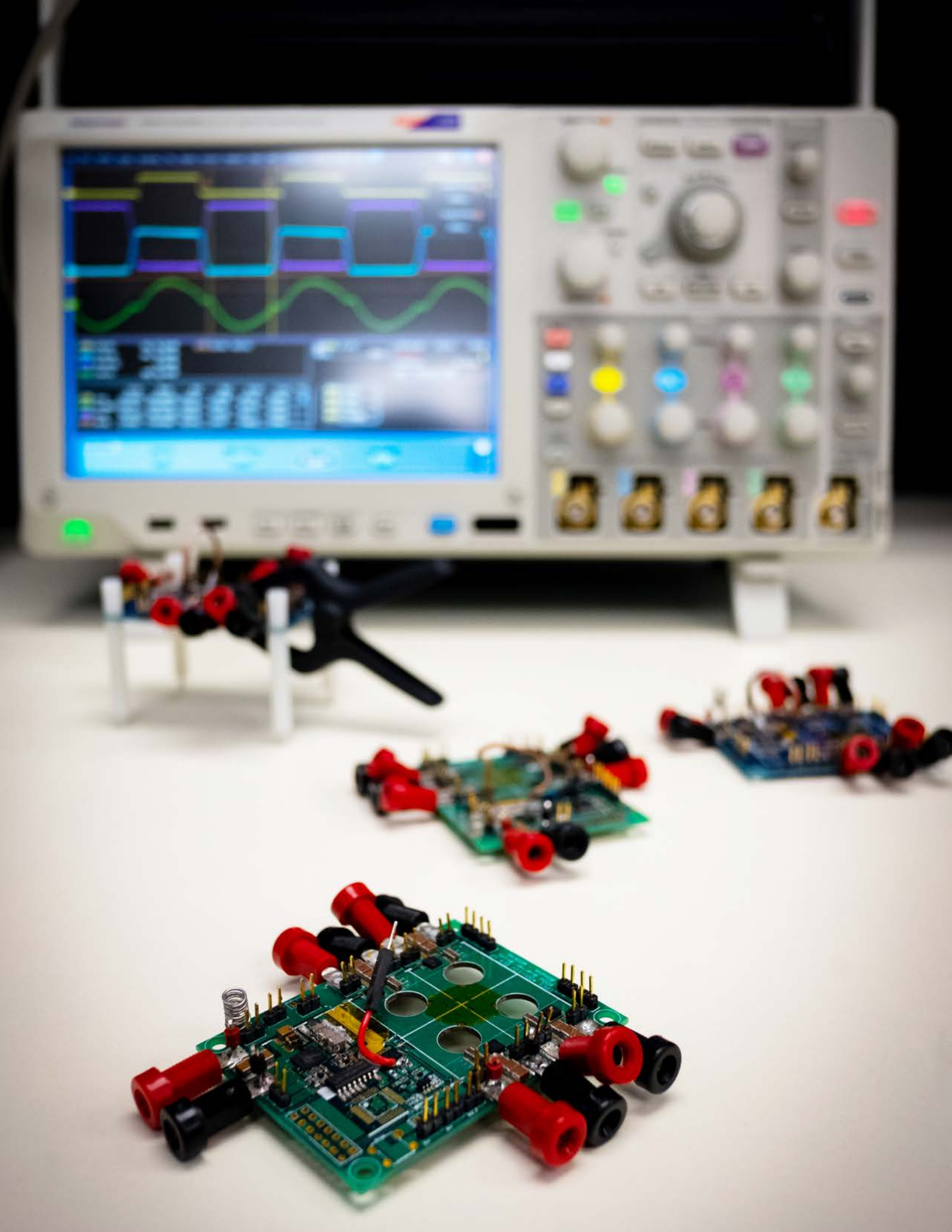


Fig. 2. Distributed controller cluster and control layer mapping.



Hybrid Voltage Balancing Approach for Series-Connected 10 kV SiC MOSFETs for DC-AC Medium-Voltage Power Conversion

To further push the device operating voltage for applications beyond 10 kV, series connection of 10 kV SiC MOSFETs is a cost-effective solution. However, a severe voltage-sharing issue exists among series-connected devices under higher switching speed conditions because of the difference in the parasitic capacitors and gate signals of different devices. The voltage balancing is required for series-connected SiC MOSFETs.

In this work, the delay time control is first evaluated to mitigate the voltage unbalance caused by parasitic capacitors. The analysis shows that active voltage balancing control has a limitation to adjust delay time accurately under a wide range of load current and cannot solve the voltage unbalance of body diodes. To mitigate the impact of a parasitic capacitor, the unbalanced parasitic capacitor from the package is first measured and compensated with the external capacitor. The value of added compensation capacitor is less than 100 pF and has slight impact on the total switching loss.

In the meantime, close-loop delay time adjustment also includes to mitigate the possible mismatch of gate signal. Body-diode turn-off detection also investigates with local drain-source voltage measurement circuit on the gate driver, so the delay time adjustment will be suspended during body-diode turn-off period. Fig. 1. shows the experiment result with the proposed hybrid voltage-balancing approach, which demonstrates a well-balanced voltage sharing for both MOSFET period and body-diode period.

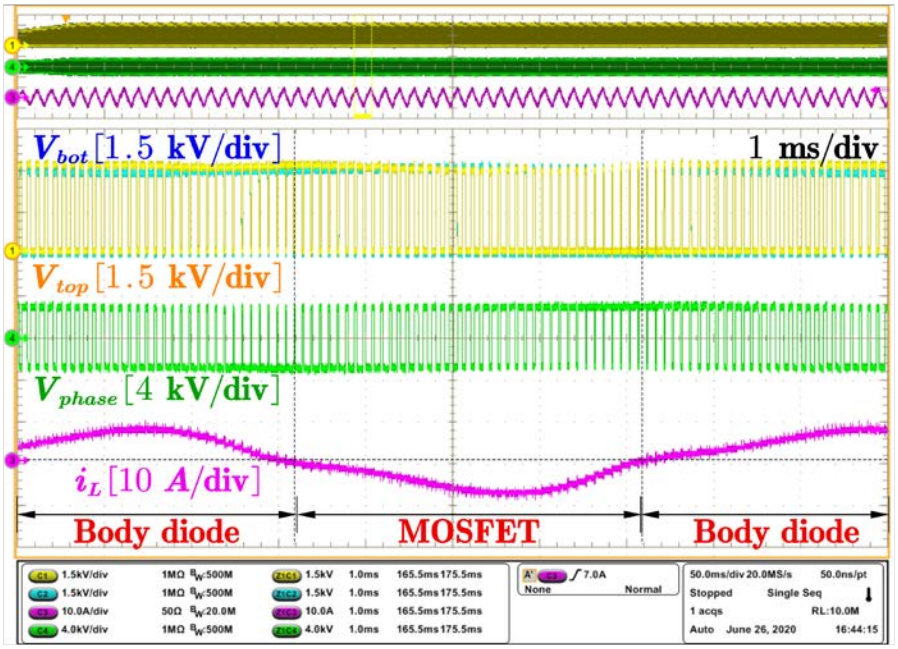


Fig. 1. Voltage sharing of series-connected SiC MOSFETs with proposed voltage balancing method.

Analysis of Voltage Sharing of Series-Connected SiC MOSFETs and Body-Diodes

Parasitic components, particularly the parasitic capacitors, surrounding the devices and gate-drivers introduce different voltage unbalance of series-connected SiC MOSFETs under different conditions. The impact of parasitic capacitors needs a detailed investigation. The understanding of such impacts will help design engineers select the proper devices, gate-drivers, and packaging solutions to enable sufficient voltage safety margins when operating the series-connected devices under high-speed switching operations. In this work, the impact of the parasitic capacitor, especially the gate parasitic capacitor, is further analyzed and more experiments are conducted to verify the analysis.

The gate parasitic capacitor will result in an extra gate current and affect the turn-off miller plateau during the transient. The analysis indicates that the voltage difference will be increased with a higher gate resistor or higher turn-off current. As shown in Fig. 1., voltage sharing of series-connected 10 kV SiC MOSFETs with different gate resistor is measured to verify the analysis.

On the other hand, the analysis also investigates the impact of drain/source parasitic capacitors on voltage sharing under different conditions. The analysis shows that the drain/source parasitic capacitor has similar impact on voltage sharing of both MOSFETs and body-diodes. Fig. 2. shows the voltage sharing of series-connected 10 kV SiC MOSFETs under ac load current condition. The voltage sharing during the body-diode period is similar to the MOSFET period, which also verifies the analysis.

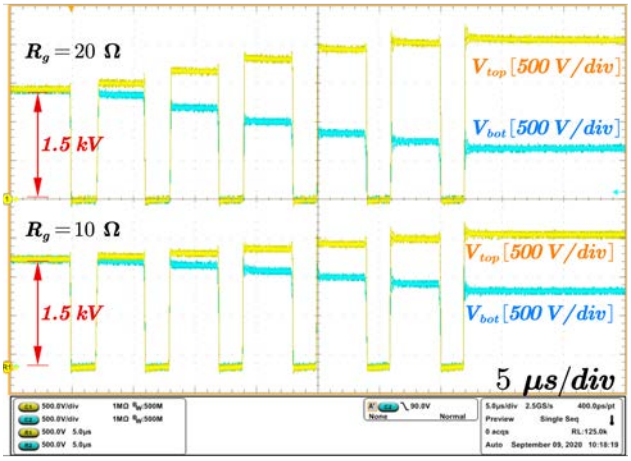


Fig. 1. Voltage sharing of series-connected 10 kV SiC MOSFETs with different gate resistor.

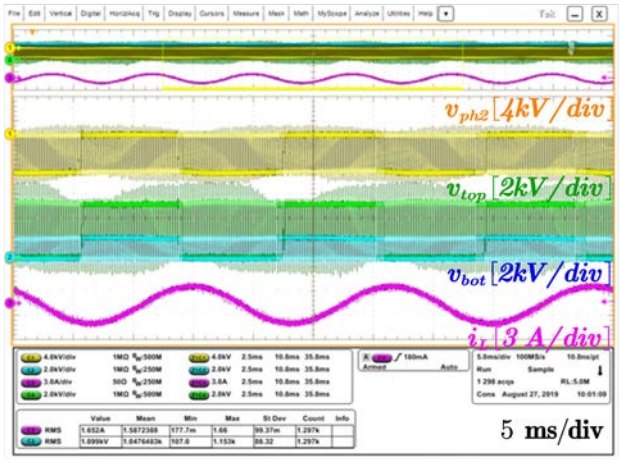


Fig. 2. Voltage sharing of series-connected 10 kV SiC MOSFETs under ac load current.

Evaluation of SiC MOSFETs for Solid State Circuit Breakers in DC Distribution Applications

DC distribution systems are currently used to facilitate the integration of distributed energy resources, energy storage elements, and other present-day loads in electric ships, aircraft, and data centers. The absence of natural zero current crossing and the high fault currents in dc systems present challenges for fault protection. Once a fault is detected, the primary function of the dc circuit breaker is to safely and quickly interrupt the fault current dissipating the energy stored in the system inductance (dependent on the fault location).

A fast reaction time is an important requirement in dc systems making the solid state circut breaker (SSCB) an ideal candidate. Combining the benefits of SiC technology, it is possible to further improve the SSCB response time and its efficiency (low conduction loss) while potentially increasing its power density, too (low cooling requirements). Therefore, it is advisable to evaluate the SiC MOSFET to understand its capabilities and limitations as it applies to this application, doing so in conjunction with its voltage-clamping circuit based on metal-oxide varistors (MOV), which combined embody the basic building block of the SSCB topology under consideration in this paper as shown in Fig. 1.

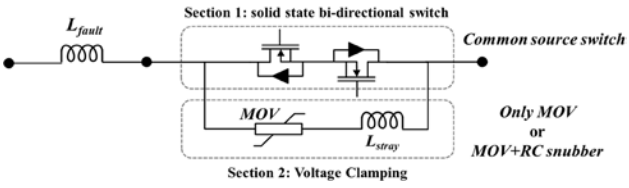


Fig. 1. Typical bidirectional SSCB used in dc distribution applications.

The evaluation was carried out with the help of a hardware prototype rated at 1.2 kV and 300 A, showing the inherent advantages of SiC devices in terms of efficiency and its capacity to attain snubberless operation. The results obtained also provided valuable insight into the SSCB switching transient behavior, which helped formulate the intrinsic dependence between gate-driver and MOV—the lower the MOSFET turn-off di/dt, the lower the MOV peak clamping voltage. Between the SiC MOSFET turn-off losses and the MOV knee voltage—the lower the knee voltage, the lower the turn-off losses compared to hard-switched events. And between system impedance and SSCB energy dissipation—the larger the impedance (and lower the di/dt), the larger the MOSFET and MOV energy dissipated. A complete set of design guidelines are formulated for the SiC-based SSCB configuration in question (Fig. 2.).

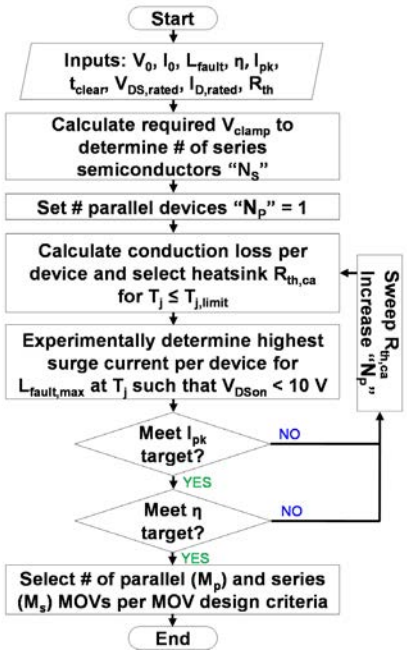


Fig. 2. SiC based SSCB design guideline.

Highly Integrated Monolithic Filter Building Block (FBB) for Silicon Carbide-Based Three-Phase Interleaved Converters

Three-phase interleaved converters provide lower harmonic content due to multi-level output voltage generation at the point of common coupling (PCC) at the expense of circulating current. Magnetic interphase coupling between converters is a well-known technique to mitigate the problem of inter-channel circulation due to interleaved carriers.

But such magnetically coupled inductors contribute to additional volume and loss. Since interleaving does not cancel the Nth order harmonics, where N is the number of parallel converters, consequently an additional boost inductor is added after the PCC to meet the power quality standards. In conjunction, the total filter volume defeats the purpose of interleaving. Thanks to the use of SiC devices, the switching frequency barrier can be extended, and the size of magnetics can be reduced dramatically. Herein lies the benefit of using a magnetically coupled structure with an integrated boost inductor as per Fig. 1.

A hybrid core structure as shown in Fig. 2. using a combination of amorphous and nanocrystalline materials has been proposed to maximize the power density of a Monolithic Filter Building Block (M-FBB) compared to a conventional Si-Steel counterpart for IGBT applications. A complete experimental evaluation using a 45 kW 3 L NPC converter is presented for a comprehensive design verification.

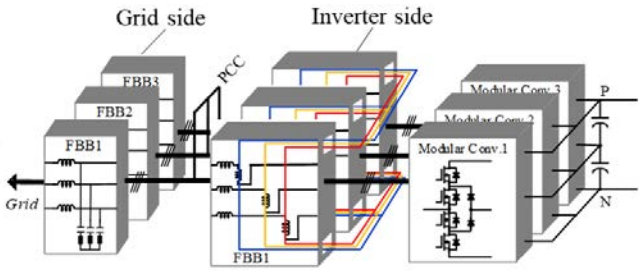


Fig. 1. System Schematic.

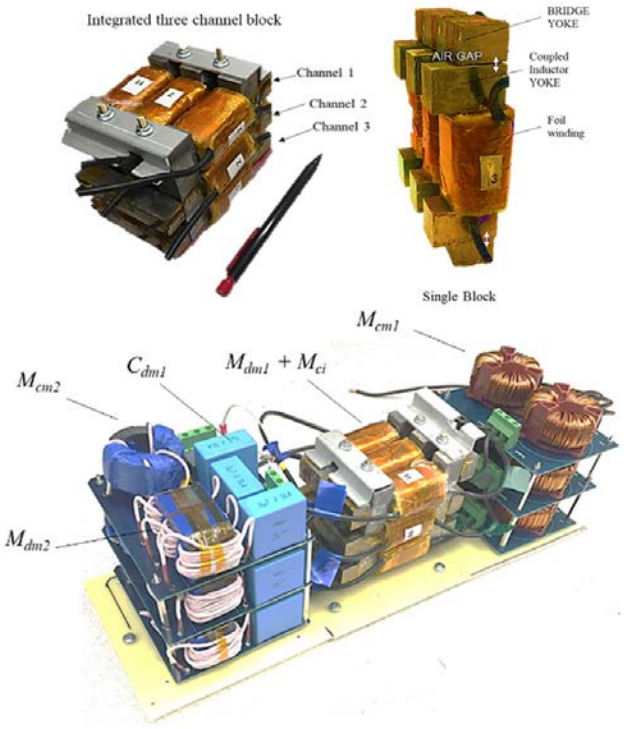


Fig. 2. Monolithic block and system assembly.

Development and Evaluation of a Power Hardware-in-the-Loop (P-HIL) Emulator Testbench for Aerospace Applications

As aerospace industries are progressing towards the More Electric Aircraft (MEA) concept, the need for complex electrical system testing is urgently increasing. Power Hardware-in-the-Loop (P-HIL) allows for a variety of electrical system tests without any hardware changes, thereby reducing the development time and cost, enabling concurrent development and fault modes testing.

In this work, the development of a P-HIL emulator testbench (Fig. 1.) using EGSTON Power Electronics, COMPISO System Unit (CSU) CSU200-1GAMP6, and external hardware (Rockwell Automation PowerFlex 753 drive inverter) is explained. First, the testbench was evaluated by characterizing an accuracy region and showed satisfactory accuracy to follow the setpoints. The power circulating operation mode was configured and several applications (induction machine, active front end, and ATRU) were tested and compared with offline simulation. Most importantly, the P-HIL emulated an induction machine working with a 30 kW PowerFlex 753 drive under various working conditions (no-load, constant-load, step-load transient, start-up transient), and the results were compared to the real-world tests as shown in Fig. 2. It showed that the P-HIL emulator has excellent accuracy and flexibility, thus can significantly facilitate the future aerospace electrical system development.

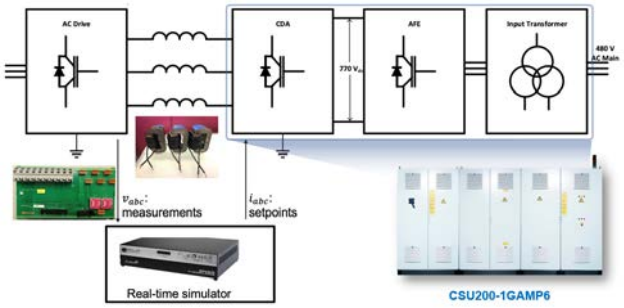


Fig. 1. System setup of the P-HIL emulator testbench with external hardware.

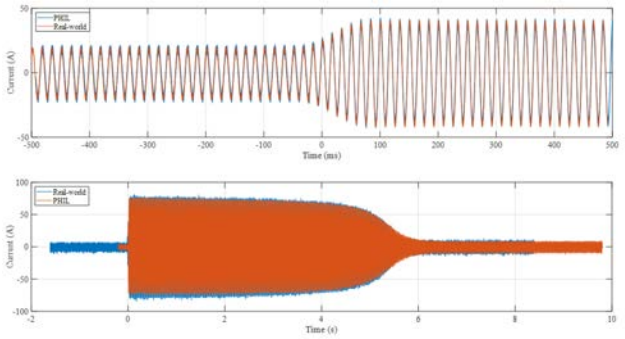


Fig. 2. Test result comparison between the P-HIL emulation and real-world motor. (Top: step-load transient. Bottom: start-up transient.)

A Compact High-Power Single-Turn Inductor for 6 kV SiC-based Power Electronics Building Blocks

In this study, a pair of differential-mode inductors was designed for placement inside the Power Electronics Building Block (PEBB) to achieve switching-cycle control (SCC) and to mitigate the harsh switching transient at the PEBB terminals. When it comes to high-power, medium-voltage applications, the bulky size of the passive components is always a hurdle towards achieving a higher power density.

This work presents the design, construction, evaluation, and testing of a single-turn inductor for a 6 kV PEBB using 10 kV SiC MOSFET modules. Among all the design solution candidates, the single-turn magnetic core structure with shielded solid insulation is selected to be the most suitable solution for the given specifications. The U-shape winding was proposed to better coordinate with the overall PEBB structure. A grounded shielding layer is applied on the solid insulator surface to achieve high compactness, and issues arising from the shielding layer were comprehensively addressed. The grounding path of the shield was designed so that the displacement current has minimum impact to the PEBB (loss, EMI, etc.). Fig. 1. shows the overall inductor prototype.

When fabricating the inductor winding, two methods (resin rich and epoxy encapsulation) were used and compared. The resin rich method uses the resin bonded mica tape to wrap on the copper bar, which is followed by hot press and oven curing. The encapsulation method, as a contrast, requires a particularly designed and 3D-printed mold for fabrication. An epoxy encapsulant with proper properties was selected. It was found that the encapsulation method takes significantly less fabrication time while achieving the similar PDIV to the resin rich method.

The performance is experimentally demonstrated. The PDIV of the inductor is measured to be 5.16 kV under a 60 Hz excitation. The measured common-mode and differential-mode impedances match the simulation beyond 10 MHz. The converter level tests were done after the inductor was integrated to a 6 kV PEBB prototype. Fig. 2. shows the current and loss on the grounding network with varying dv/dt levels, demonstrating the effectiveness of the proposed grounding strategy.

This work also evaluates the application with higher current requirements.

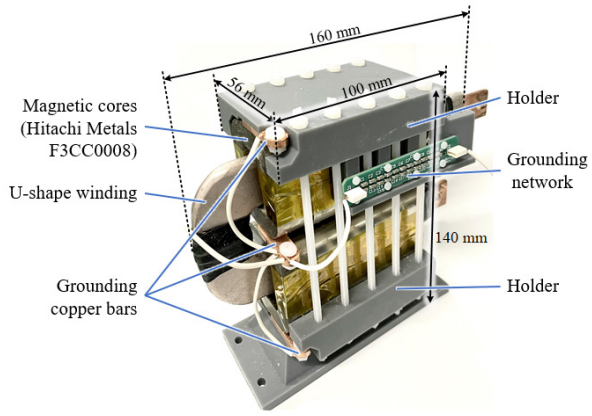


Fig. 1. Structure of the single-turn inductor.

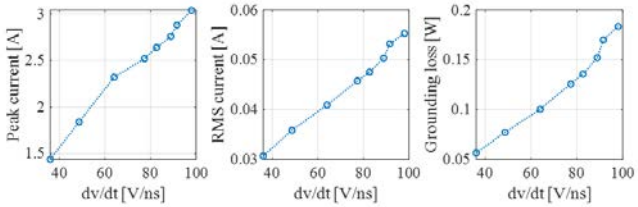


Fig. 2. Test results of grounding current and grounding loss with varying dv/dt.

Computational Fluid Dynamic Analysis and Design of an Air Duct Cooling System for 18 kW, 500 kHz Planar Transformers

Power converter designers have adopted high-frequency planar transformers to increase system power density. However, shrinking transformer size increases thermal stress and cooling system size. This work presents an air duct cooling system that was designed using computational fluid dynamics for two parallel (8:4 and 10:1) 18 kW, 500 kHz planar transformers. A 1U low profile forced air cooling duct with converging geometry and integrated turbulators is presented to increase free stream air velocity, which lowers winding temperature.

Cooling duct design was constrained by three criteria: 1) cooling system power consumption < 5 W, 2) complies with 1 U height requirement, and 3) peak internal winding temperature < 120° C. The 18 kW battery charger with 3D printed cooling duct system is shown in Fig. 1. Turbulators were added to the 30 mm x 30 mm (inlet area) duct to improve air velocity and better deposit airflow onto the winding surfaces as shown in Fig. 2. The addition of turbulators increased average simulated air velocity from 6 m/s to 17 m/s.

The system was constructed and tested to thermal steady state at 10 kW, 15 kW, and 18 kW (full load). At full load power, peak internal winding temperature was only 118° C after steady state was reached. Total cooling system power consumption was only 4 W and the transformer height including the cooling system was only 43 mm. The cooling duct and analytical insights are applicable to future high-power, high-density planar transformers.

Fig. 1. 18 kW battery charger with cooling ducts.

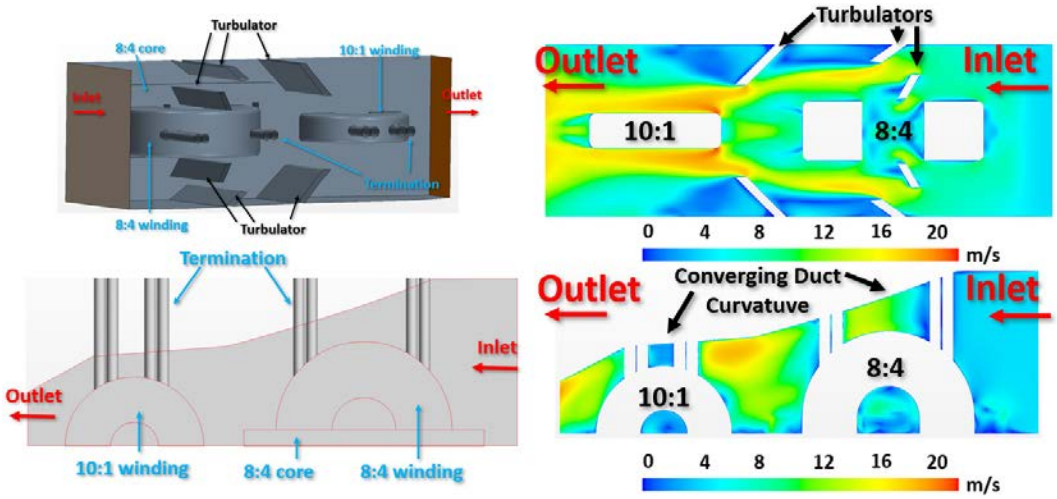


Fig. 2. 30 mm duct with turbulators to improve air velocity and deposit of air flow.

Magnetic Design and Validation of a 500 kHz, 18 kW "Intra-Leaved" Litz Wire Transformer for Battery Charging Applications

This paper presents the design and fabrication process of a high-density 500 kHz 18 kW litz wire, air-cooled transformer that achieves low leakage inductance and high efficiency for a bidirectional resonant dc-dc converter system. The transformer design procedure analyzes the trade-offs between standard E cores and planar E cores with a focus on low leakage inductance, high efficiency, high-power density, and even current sharing among parallel windings. A planar E core with a primary-secondary-primary-secondary (PSPS) configuration is chosen as the final design. Transformer efficiency is 99.61% at full load power (18 kW) and power density is 4277 W/in^3. Leakage inductance is 764 nH and 128 nH for the primary and secondary sides, respectively. The transformer winding is potted in thermal epoxy to improve heat spreading and reduce peak internal winding temperature. A simple-to-use potting mold is developed to pot the transformer winding and remove air bubbles from the winding bundle.

The secondary side is split into parallel secondaries S1 and S2 to handle full-load current (56 ARMS) while still using small diameter litz wire to achieve a high window fill factor. Due to the high operating frequency of 500 kHz, any mismatch in winding leakage inductance will result in unequal current sharing among parallel windings. An "Intra-leaved" winding structure is proposed as shown in Fig. 1. With "Intra-leaving," the winding impedance of S1 and S2 are well matched resulting in improved current sharing over the non-"Intra-leaved" case. Current sharing results are shown in Fig. 2., which validates the impact of the proposed winding strategy. Without "Intra-leaving" S1 takes 53 APeak and S2 takes 27 APeak. With "Intra-leaving" S1 takes 42 APeak and S2 takes 38 APeak, an almost perfect current split between the parallel windings S1 and S2. The proposed winding method, potting method, and analytical insights are applicable to future high-power, high-density planar transformers.

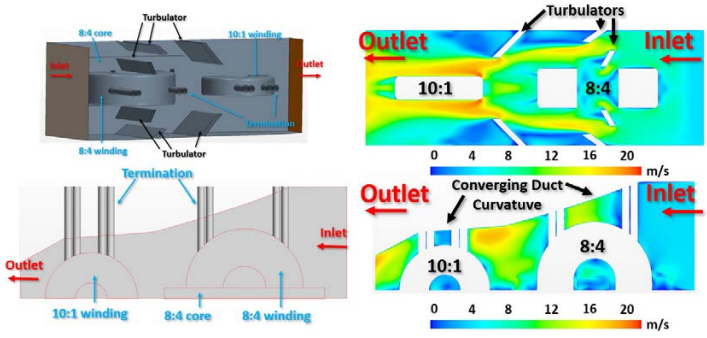


Fig. 1. "Intra-leaved" PSPS planar E core.

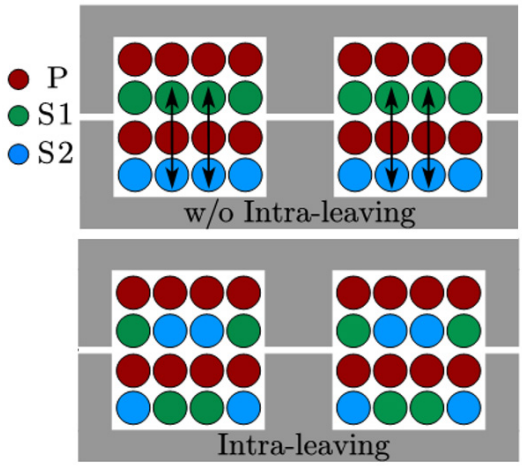


Fig. 2. Current sharing results with and without "Intra-leaving."

Design of a SiC-Based High-Density Integrated Power Electronics Building Block (iPEBB)

A 250-kW, SiC-based integrated power electronics building block (iPEBB) is being explored for applications requiring high-power density. The integrated design features a common substrate, which plays a vital role in the thermal, electrical, and mechanical performance, as well as the weight and reliability of the iPEBB. Silicon nitride (Si_3N_4) and organic direct bonded copper (ODBC) materials are explored to see their impact on these characteristics and identify key trade-offs. The high-density design is achieved through integrating SiC bridges using 1.7 kV SiC MOSFETs on a common multilayer substrate, which also connects to the high-frequency transformer and other passive components. Compared to employing multiple power modules on a baseplate, the proposed integrated SiC bridges enable smaller power-loop inductance (~3 nH per half-bridge), improved heat dissipation, and lower EMI, while meeting strict weight limitations (<16 kg).
Fig. 1. (a) shows the iPEBB topology, which enables flexible (dc-dc, dc-ac, ac-dc), galvanically-isolated, bidirectional power conversion. Fig. 1. (b) shows the iPEBB primary side components on the common substrate.

The primary and secondary side of the iPEBB have an identical common substrate, which simplifies manufacturing and reduces cost. This will allow the iPEBB to be mass produced and serve as the backbone of the power distribution system on future electric ships. The iPEBB is intended to be inserted into a rack, which will provide cooling to the top and bottom substrates, and hence the components mounted to them. Thermal, mechanical, and electromagnetic finite element analysis (FEA) simulations were performed to identify suitable substrate materials, dimensions, and layouts, while also minimizing the weight.

To verify the design, 1.7 kV SiC MOSFET half-bridges with Si_3N_4 and ODBC substrates have been packaged as shown in Fig. 2. (a) and 2. (b). The half-bridges will be tested in a quasi-square wave, zero-voltage switching (QSW-ZVS) buck testbed shown in Fig. 2. (c). ZVS reduces the switching losses, enabling the 1.7 kV half-bridges to operate in the hundreds of kilohertz range. The testbed was designed to enable thermal imaging of the SiC MOSFET die during operation. These temperature measurements will be used to verify the thermal models. The proposed design and state-of-the-art substrate materials aid in the realization of the iPEBB, which will advance future electric transportation systems.

This work was supported by the Office of Naval Research (ONR) with the grant number N00014-16-1-2956.

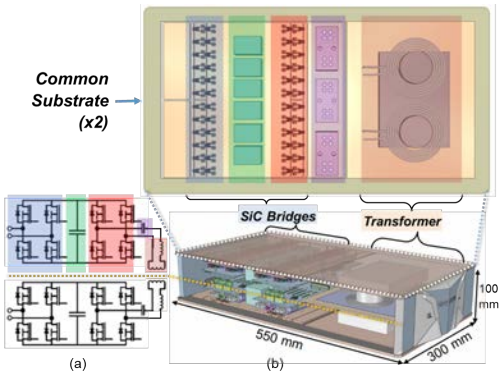


Fig. 1. (a) CLLC-based topology for iPEBB, (b) iPEBB design with a top view of the common substrate for the primary side.

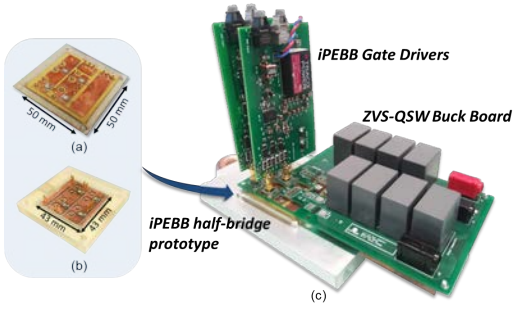


Fig. 2. (a) ODBC and (b) Si_3N_4 1.7 kV SiC MOSFET half-bridges, (c) QSW-ZVS buck testbed.

EMI Evaluation of a 1.7 kV SiC MOSFET Module with Organic DBC Substrate

This work evaluates the electromagnetic interference (EMI) of a silicon carbide (SiC) MOSFET power module with emerging organic direct bonded copper (ODBC) substrates. The thin, ductile organic insulator in ODBC substrates enables thick copper (Cu) to be used. The thick Cu enables higher current capacity, improved heat spreading, and can eliminate the need for a baseplate. However, the thin dielectric of the ODBC increases the electrical coupling within the power module. In particular, the ODBC-based module has increased capacitive coupling between the module terminals and the mounting structure (i.e. ground network) compared to a conventional ceramic-DBC-based module. Capacitive coupling between the power module terminals and the ground network is known to be a significant contributor to the propagation of common mode (CM) currents in high-power converter systems. Therefore, as part of this work, a detailed analysis of the CM implications of the module design presented herein was conducted.

A 1.7 kV SiC MOSFET half-bridge module was fabricated using a 50 mm × 50 mm ODBC substrate as shown in Fig. 1. (c). The layout of the module is shown in Fig. 1. (a). The Cu pads are color coded to correspond to the nodes in the schematic shown in Fig. 1. (b). The half-bridge was designed to minimize CM noise by reducing the S1D2 area to be less than 30% of the total substrate area. The ODBC module was simulated in a custom inverter testbed, where the input and output impedance of the system are equal (Zin = Zout). This allows for a simplified common-mode equivalent model (CEM) of the testbed.

The ratio of the S1D2 capacitance (Cag) to the total module capacitance to ground (Cbp) can be manipulated to minimize or cancel the leakage current through the baseplate. The testbed and model were previously verified with a Cree BM2 SiC MOSFET power module. As shown in Fig. 2., the baseplate leakage current of the ODBC module is reduced by nearly 20 dB across a wide frequency range, and by 30 dB at 5-10 MHz. This evaluation is valuable because it demonstrates that proper application of a suitable CM model can be employed to reduce emissions in a deterministic fashion, even without the introduction of CM filters.

This work was supported by the Office of Naval Research (ONR) with the grant number N00014-16-1-2956.

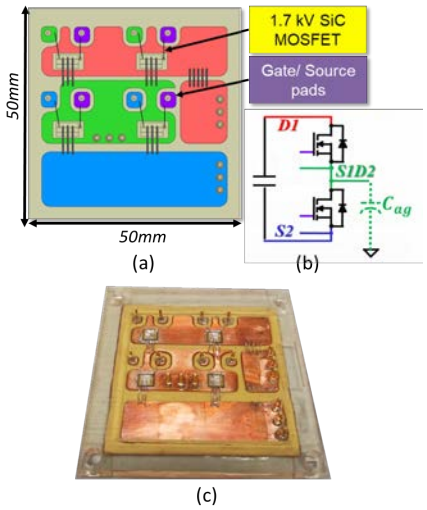


Fig. 1. (a) ODBC-based half-bridge layout, (b) Half-bridge schematic, and (c) ODBC module prototype.

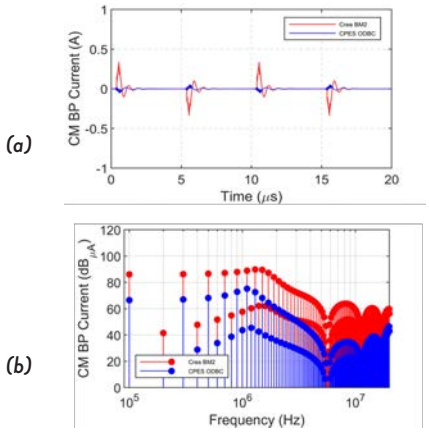


Fig. 2. Predicted leakage current through module baseplate in (a) time-domain, (b) frequency-domain for practical configuration of EMI testbed with commercial module (red) and ODBC module (blue).

Modeling and Impedance Analysis of a Turbine-Generator-Rectifier System with Electromechanical Dynamic Interactions in More Electric Aircraft

More electric aircraft concept has been a trend in the aircraft industry to tackle the challenge of reducing cost and weight, reducing environmental emissions, and increasing fuel efficiency. This increase in onboard electric power installation has brought challenges in the design and operation of aircraft electrical power systems. Onboard electrical power is generated by turbofan-driven generators and transferred to multiple loads through a dc distribution system. Since the electrical system is tightly coupled with the mechanical system through the generators, it is an interesting question as to whether the generators would transfer disturbances from mechanical to electrical domain. To ensure electrical system normal operation during the whole flying profile, it is important to consider shaft dynamics' impact on the electrical system stability in the system design. By examining generator output impedance, this paper found that the impact of the shaft dynamics on the electrical power system stability is masked by the generator rectifier.

In this paper, an onboard HVDC system is studied, as shown in Fig. 1. The permanent magnet synchronous generator is rated at 1 MW, the dc bus voltage is rated at 1 kV. A dual-loop control strategy is applied to the generator, where the outer loop regulates dc bus voltage with a PI controller and provides the reference for iq, and the reference of id is set as 0 to achieve unity power factor control. The turbofan shaft is emulated using the open-source AGTF30 advanced geared turbofan engine system model. Multiple loads are connected to the dc bus through power electronics interface, which can be modeled as constant power loads.

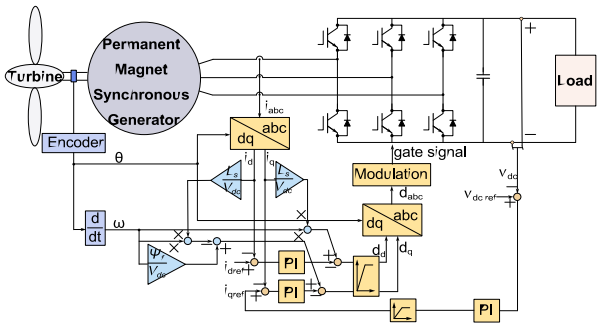


Fig. 1. Onboard DC distribution system.

Here the impedance-based stability criterion is used to access the stability condition of the dc distribution system. Therefore, to access the turbofan shaft dynamics' impact on system stability, it is necessary to derive the small-signal impedance of the source subsystem. The small signal model is shown in Fig. 2. It is found that the difference of the closed-loop output impedance in the case where shaft dynamics is considered and ignored lie in the three terms, GdeωGTe, GvωGTe, and GiωGTe, which are found to be so small that the difference is negligible. It is also found that when the generator power ratio to the total turbofan power increases, the turbofan shaft dynamics have more impact, though still small, on the output impedance below 10 Hz, at which the source subsystem seldom has dynamic interactions with the load subsystem.

This paper provides a detailed analysis of the shaft dynamics of the turbofan's impact on the small-signal stability of the aircraft dc distribution system and reveals the masking effect of the rectifier for the following reasons: the speed perturbation has small impact on the dc bus voltage and stator current; the turbine dynamics is small with the current speed controller; the decoupling terms in the current controller attenuates the speed perturbation impact; and the dc voltage control reduces the impedance gain at low frequency, which further reduces the potential stability impact from mechanical dynamics.

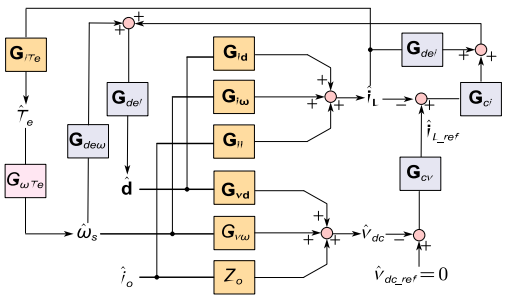


Fig. 2. Small signal model of the system.

Optimization of Electric-Field Grading Plates in a PCB-Integrated Bus Bar for a High-Density 10 kV SiC MOSFET Power Module

High-voltage SiC MOSFETs have the potential to drastically improve the size and efficiency of power systems due to their higher operating voltages and faster switching speeds. To realize this potential, a 10 kV high-density (4 W/mm^2) package with low parasitic inductance (4.4 nH) was developed. The high-density design is enabled by minimal (6 mm) spacing between the terminals of the module. This is nearly six times closer than the terminals of the CREE XHV-9 10 kV SiC module, which has a terminal spacing of 37 mm. The reduction in terminal spacing is made possible by fully enclosing the terminals, which circumvents the creepage and clearance distance requirements (Fig. 1.).

To reduce the electric field strength in the air surrounding the interface, copper traces inside the PCB are used as field-grading plates that shift the peak electric field from the air to the FR4 dielectric, which has a higher breakdown field strength than air. The geometry and location of the field-grading plates is critical to their effectiveness. To design the geometry, a numerical optimization technique is used in conjunction with finite element analysis (FEA). The system is first decomposed into critical 2D design regions, which are then parameterized, and the locations of field crowding are identified. A weighted cost function is formulated using the breakdown strength of the materials and optimized using an interior-point algorithm with finite difference derivatives.

One of these optimized cross-sections is shown in Fig. 2. The optimization results in copper conductor shapes that contain the high electric field strength in the FR4 dielectric, where the field can be supported without partial discharge. Meanwhile, the electric field in air is kept below the breakdown strength of air, resulting in safe, reliable, partial-discharge-free operation. The optimized laminate bus bar and optimized module housing were built and experimentally demonstrated a partial discharge inception voltage of 11.6 kV rms (16.4 kV peak) under 60 Hz sinusoidal excitation.

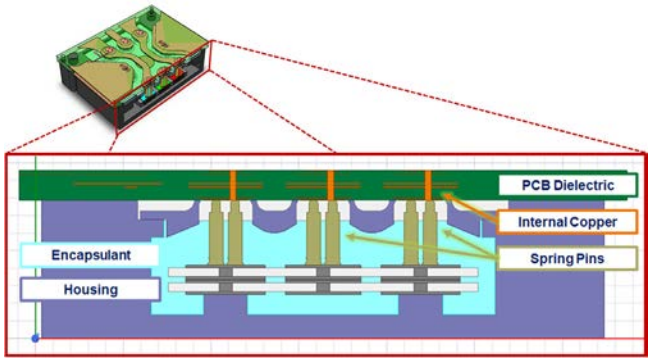


Fig. 1. SiC 10 kV power module cross-section

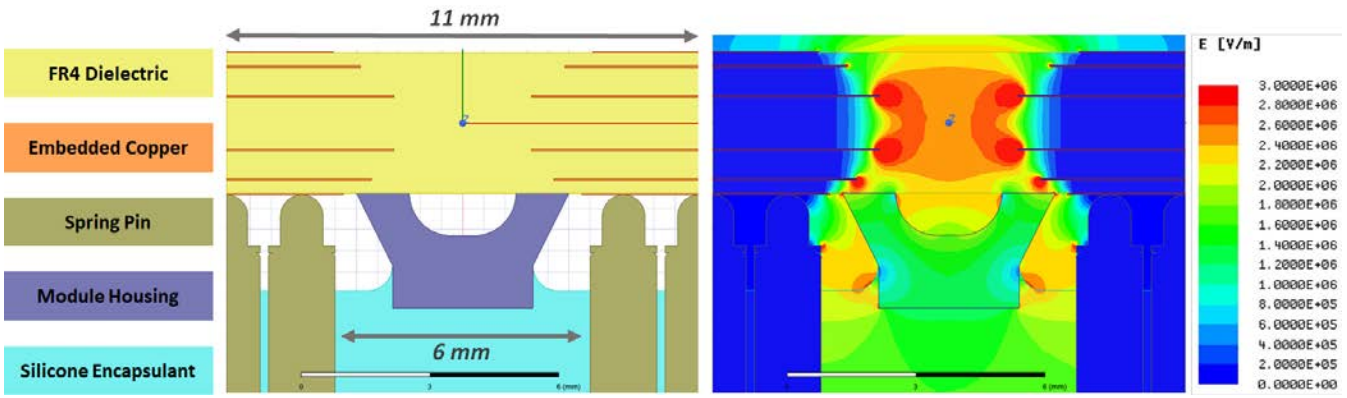


Fig. 2. Optimized cross-section supports 10 kV bus voltage without exceeding the breakdown strength of air.

High-Power Density Design of Power Electronic Interrupter in Medium-Voltage Hybrid DC Circuit Breaker

Circuit protection is a key enabler for future medium-voltage direct-current (MVDC) distribution systems. Hybrid dc circuit breaker (HCB) offers low conduction losses and reasonably fast response times but suffers from large size. In this paper, a high-power density, power electronic interrupter design is introduced for the HCB as shown in Fig. 1. The device selection and trade-off analysis of voltage clamping circuit are investigated.

For the blocking voltage requirement, single IGBT is far from meeting the demand of 12kV, so series device is required. Traditional power electronic interrupter (PEI) usually adopts series device parallel with a concentrated voltage clamping circuit for energy absorption. Then additional voltage balancing circuits such as a passive snubber or an active gate driver are designed to protect each device from exceeding withstand voltage. However, in dc circuit breaker, the function of the voltage clamping circuit overlaps with the voltage-balancing design. So the voltage clamping component can be divided into small components and paralleled with each device, which can be regarded as one module. In this way, the consistency requirements for devices are low and higher voltage could be achieved by the series of more modules. Besides, if one module is damaged during operation, the other module will not be exposed to higher voltage so that the cascading damage could be avoided. The modular design procedure was shown in Fig. 2.

According to this procedure, a small-sized module with two parallel 1.7 kV discrete IGBTs are selected as main switches. The RC snubber and MOVs are carefully designed to guarantee no tail current bump and sufficient turn-off voltage margin. Different methods are also utilized to suppress the current bumps to avoid device failure. In the module integration stage, the power supply structure and staged turn-off strategy are investigated to improve the power density and breaking time. Experimental results at 12 kV and 1 kA are provided to verify the operation of the prototype.

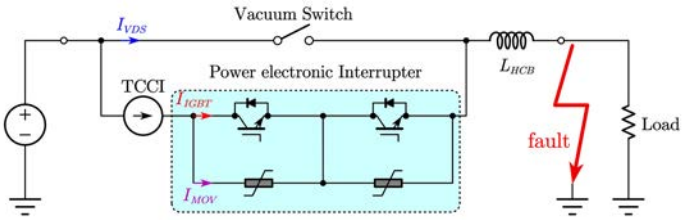


Fig. 1. Hybrid circuit breaker structure.

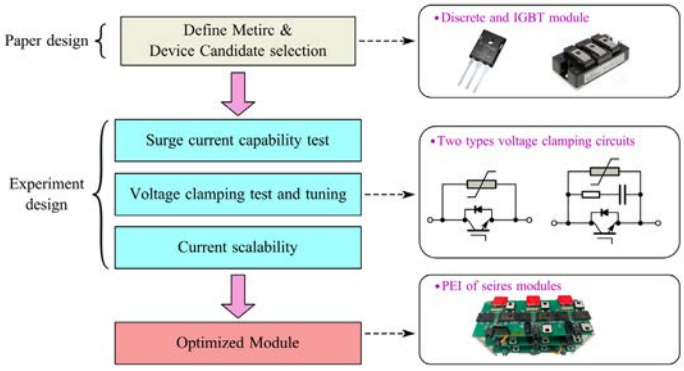


Fig. 2. Modular Design procedure.

Design and Implementation of an 18 kW 500 kHz 98.8% Efficiency High-Density Charger with Partial Power Processing

The demand for high-density, high-efficiency bidirectional battery chargers is driven by the fast development of an energy storage system in renewable energy system, micro-grid, and transportation electrification. An isolated dc-dc converter that interfaces a battery with a variable voltage range is one of the critical components. An input-parallel output-series (IPOS) partial power (PP) converter is considered a promising high-efficiency, high density solution because only a fraction of power is processed via multi-stage converters to regulate output voltage. However, due to the tight coupling between two dc transformers (DCXs), the design of the PP converter is complicated. To solve this issue, an overall design procedure for a bi-directional soft-switching resonant type PP converter is proposed. In the parameters design part, a decoupled design method is proposed to simplify the DCXs design. With this method, two DCXs can be designed separately and a typical optimization method can be easily applied. As for the hardware design part, to minimize the ac loop inductance and resistance, a 2-directions (2-D) flux cancellation method and an "intra-leaving" winding structure are proposed for circuit layout and HF transformer to obtain high operation efficiency and power density. Finally, the whole design procedure is verified by an 18 kW rated, 25 kW peak, prototype operating at 500 kHz. The realized PP converter features a peak efficiency of 98. 8% and a power density of 142 W/in^3 as shown in Fig. 1.

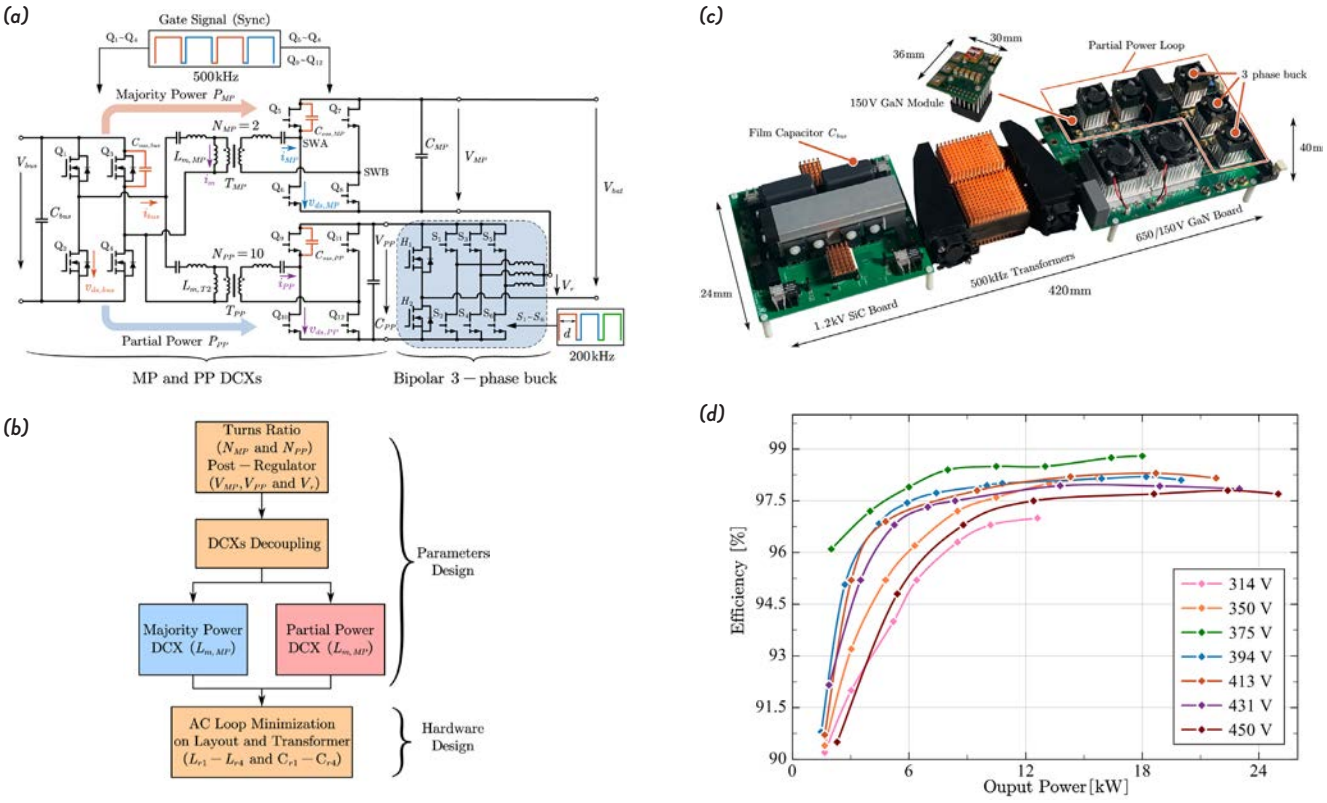
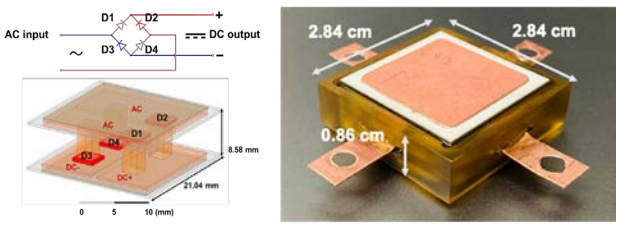


Fig. 1. (a) Circuit Diagram (b) Design Procedure (c) 18 kW Prototype (d) Total Efficiency.

Double-Side Cooled Medium-Voltage Power Module with Sintered-Silver Joints Demonstrated in an 8 kV Silicon Carbide Diode Module

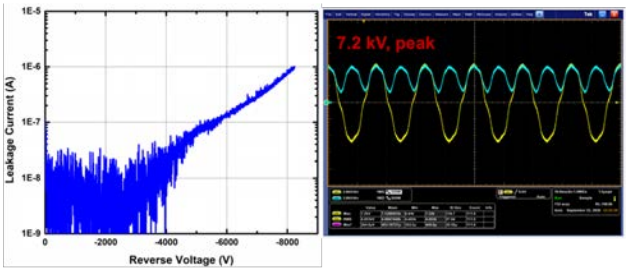
The power-handling capability of a packaged power semiconductor device is limited by the heat extraction ability. The heat extraction pathway involves conduction from junction to case, and the heat transfer from case to the coolant. A unique challenge for packaging MV power modules is the trade-off between the heat extraction and the insulation. Two packaging innovations that can improve heat extraction without compromising insulation, thus expanding the safe operating area of the device and reducing the number of devices needed for a specific application, are (1) double-side cooling, and (2) sintered-Ag bonding. The first is realized by using short metal posts, rather than long and thin wire bonds for device interconnection, to form a low-profile package with devices sandwiched between two insulated metal substrates. The second enables the devices to function reliably at device junction temperatures over 250° C, which is higher than that of the state-of-the-art soldered power devices. The latter innovation is especially significant for packaging wide-bandgap devices since these devices theoretically can function at much higher temperatures than silicon devices.

In this work, we implemented the two packaging innovations for the design and fabrication of an 8kV SiC full-bridge diode rectifier module. Fig. 1.(a). is a schematic of the module layout. The device chips were sandwiched between two patterned direct-bond-copper (DBC) substrates. Die-attach and metal-post bonding were done by silver sintering. Steady-state thermal simulations were run to verify the benefit of double-side cooling. Electrical and electric field simulations and analyses were performed to minimize the loop inductances and guide the insulation design. The packaging concept was implemented in assembling an 8 kV SiC diode full-wave rectifier shown in Fig. 1. (b). The electrical testing results of the module shown in Fig. 2., validated the package design and fabrication.



(a) (b)

Fig. 1. (a) Schematic of the double-side cooled 8 kV SiC diode full-wave module and its equivalent circuit. (b) Prototype of the 8 kV SiC diode full-wave rectifier module.



(a) (b)

Fig. 2. (a) Reverse I-V characteristics of Diode 4 (labeled in Fig. 1(a). as D4) after packaging. (b) Output dc waveform (blue) under 60 Hz sinusoidal ac input (yellow) with a 7.2 kV peak value.

Fault Characteristic Analysis in 56 Bus Distribution System with Penetration of Utility-Scale PV Generation

The increasing penetration level of distributed energy resources (DERs) in electrical power systems has led to revisions of criteria and requirements for DER interconnection, as IEEE Standard 1547-2018 published. These revisions are likely to cause some major changes of distribution system fault characteristics, which might defeat the traditional protective relay schemes. To achieve the effective integration of DERs into existing distribution systems and avoid the negative impact on system reliability, it is necessary to study the fault characteristics changes and undesirable problems in system protection caused by DER interconnection. This paper focuses on the impacts from high-level penetration of utility-scale PV generation.

A 56-bus, light-loaded radial distribution system connected with a utility-scale PV farm as shown in Fig.1. was simulated in PLECS for fault analysis. The PV inverters control schemes are designed according to requirements stated in IEEE Standard 1547-2018. PV inverter fault performance and distribution system fault response are analyzed for both three-phase and single-phase short circuit faults, under different fault resistance and at different locations. After a short circuit fault happens in the distribution system, the PV inverter output current will only have a small increase because the reactive power control loop and dc voltage control loop both lose their effect. The current reference values on d and q axis will both hit their saturation limits while the current loop is still able to track the reference values, as it shows in Fig. 2. During a three-phase fault at PV upstream, most part of the PV output current will flow from the PV farm to fault, the relay at fault downstream and closest to the fault might incorrectly operate since its operation time could be set smaller than its upstream relays. The smaller the fault resistor is (or the closer the fault location is to the PV farm), the higher the fault downstream current will be. For single phase fault at PV farm upstream, the PV output current and the fault downstream current at faulted phase is higher compared to three-phase fault case, which is more likely to cause the incorrect operation of fault downstream relay.

Based on simulations implemented on PLECS platform, this paper studies the impact of inverter-based solar photovoltaic (PV) source to a 56-bus distribution system and analyzes the distribution system characteristics under various different short-circuit fault conditions. The potential issues in system protective relays caused by DER penetration are also presented.

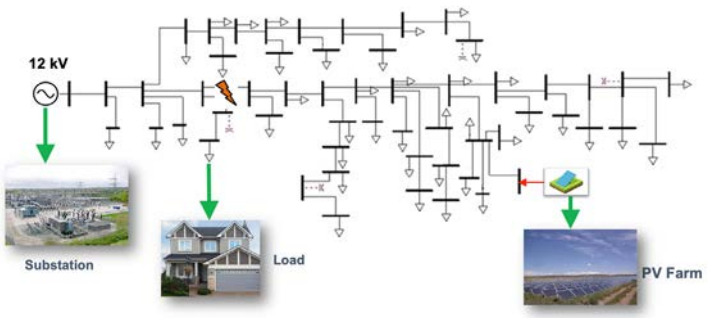


Fig. 1. Topology of 56-bus distribution system.

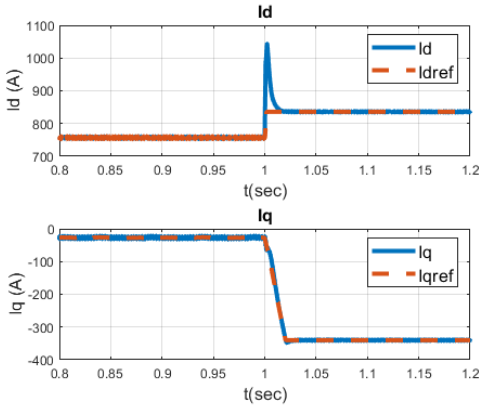


Fig. 2. PV inverter output current on d-q frame.

Design of a PCB-Based Planar Common-Mode EMI Filter of a 100 kW SiC Inverter for High-Altitude Application

Silicon-Carbide (SiC) devices are more and more commonly used for high-power traction inverters due to the higher junction temperature limit, lower conductive resistance, and higher switching speed. However, the higher switching frequency and higher switching speed of SiC inverters bring more challenges to the EMI filter. For aerial applications, the high altitude increases the risk of partial discharge (PD) and breakdown of conventional EMI filters. According to the Paschen curve, the breakdown voltage is 600 V/mm at the altitude of 50,000 ft., which is much lower than the breakdown voltage at sea level (3000 V/mm). Therefore, 300 V/mm is defined as the limit of the electric-field (E-field) intensity at the altitude of 50,000 ft. The heat dissipation is also more challenging at higher altitudes compared to that at sea level. The thermal resistance of natural convection at the altitude of 50,000 ft. is more than twice that at sea level. The E-field and heat dissipation should be considered carefully in the optimal design of the CM choke at the altitude of 50,000 ft.

Cables and toroidal cores are always used in the traditional common-mode (CM) chokes. However, the E-field is difficult to be controlled using the convection material and structure. Also, the inefficient heat dissipation and the bulky size prevent the application of the convectional CM choke. The planar core and PCB-based CM choke is good for the control of the E-field and heat dissipation.

In this work, a PCB-based planar CM EMI filter of a 100 kW SiC inverter for high-altitude application is designed, as shown in Fig. 1. The CM model of the inverter system is analyzed, and a LC CM filter is designed based on the model. The dimensions of the core of CM choke are optimized to minimize the volume with the constraint of the E-field and heat dissipation at the altitude of 50,000 ft. To reduce the profile of the CM choke and control the electric field effectively, the PCB windings are adopted for the CM choke. The electric field of the CM choke is analyzed, and the PCB windings are designed to avoid PD at high altitude. Some grounded shielding traces are inserted into the PCB windings to reduce the risk of PD. The CM choke is tested in the 100 kW SiC inverter system and the PD test is conducted in the low-pressure chamber. The tests show that the CM EMI noise is reduced effectively with the CM choke and no PD occurs in the CM choke even at an altitude of 50,000 ft. The partial discharge inception voltage (PDIV) at different altitudes are measured, as shown in Fig. 2. The PDIV decreases as the altitude increases and PD does not occur even at the altitude of 50,000 ft.

Fig. 1. The CM Choke for High-Altitude Application.

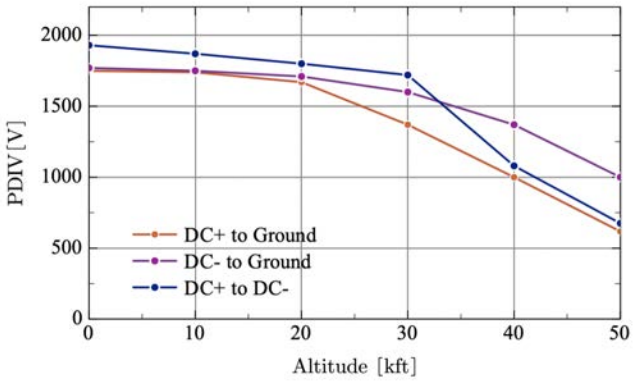


Fig. 2. The PDIV at Different Altitudes.

Integrated Power Electronics Building Block Circuit Design and Analysis

The concept of the integrated power electronics building block (iPEBB) is to develop a least-replaceable unit that will increase power density, functionality, and reliability, while decreasing cost, weight, and maintenance, of medium-voltage, MW-scale applications, such as electric ships. To achieve universal functionality, a bidirectional, flexible, high-efficiency, and galvanically-isolated topology is required. To realize this, a CLLC-based resonant topology is selected (Fig. 1.). It enables bidirectional dc-dc, dc-ac, and ac-dc power conversion, features a high-frequency transformer, and can achieve zero-voltage switching (ZVS) to allow for high efficiency at high switching frequency. With this topology and 1.7 kV SiC MOSFETs, the iPEBB will have a 1 kV dc bus voltage and operate in the hundreds of kW and hundreds of kHz range.

A 500 kHz, 250 kW dc-dc CLLC resonant converter was simulated in this work. The magnetizing inductance, and the primary and secondary side leakage inductances of a 500 kHz transformer were extracted using FEA simulations. Nine 1.7 kV SiC MOSFETs are used in parallel to achieve 98.5% efficiency. The simulated conduction, switching, and transformer losses were found to be 2.13 kW, 0.75 kW, and 1.15 kW, respectively. The deadtime was calculated such that the output capacitance of the MOSFETs have sufficient time to discharge/charge to reduce switching loss. Fig. 2. shows the simulated waveforms of the CLLC converter operating in ZVS.

A high-frequency ZVS-buck converter was also designed and simulated. This converter will be used to test the high-frequency capability of a custom 1.7 kV SiC MOSFET module and verify the ZVS operation and simulated losses. These test results will be used to inform the CLLC converter loss and ZVS operation.

This work was supported by the Office of Naval Research (ONR) with the grant number N00014-16-1-2956.

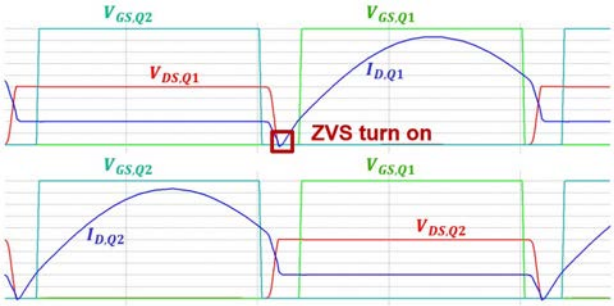


Fig. 2. Waveform of CLLC converter in ZVS. condition.

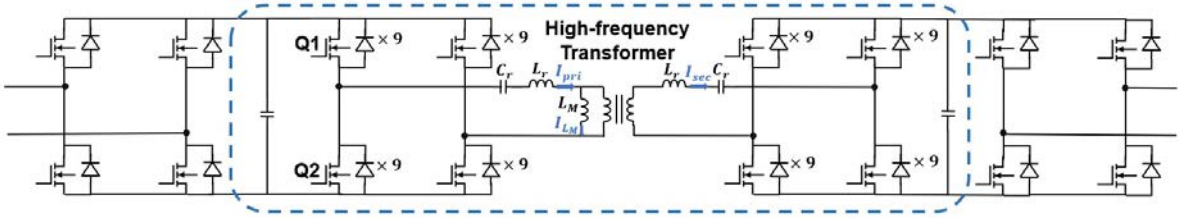
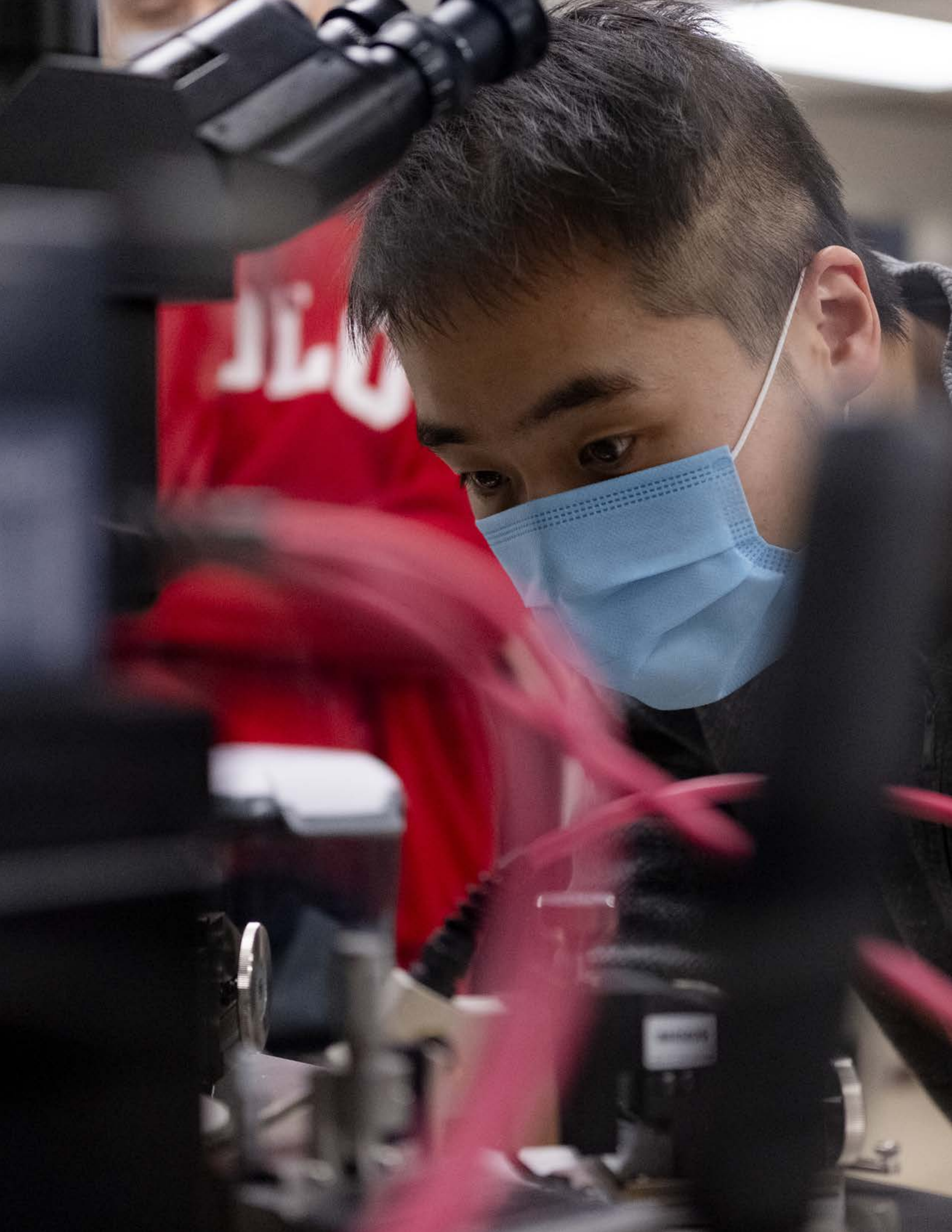


Fig. 1. CLLC resonant converter in dc-dc mode.



BLACKSBURG

1185 PERRY STREET
655 WHITTEMORE HALL
BLACKSBURG, VA 24061

NATIONAL CAPITAL REGION

900 N. GLEBE ROAD
ARLINGTON, VA 22203

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