Control, Analysis, and Design of SiC-Based High-Frequency Soft-Switching Three-Phase Inverter/Rectifier

Gibong Son

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Qiang Li
Fred C. Lee
Rolando Burgos
Virgilio Centeno
Steve Southward

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Abstract

This dissertation presents control, analysis, and design of silicon carbide (SiC)-based critical conduction mode (CRM) high-frequency soft-switching three-phase ac-dc converters (inverter and rectifier). The soft-switching technique with SiC devices grounded in CRM makes the operation of the ac-dc converter at hundreds of kHz possible while maintaining high efficiency with high power density. This is beneficial for rapidly growing fields such as electric vehicle charging, photovoltaic (PV) systems, and uninterruptable power supplies, etc. However, for the soft-switching technique to be practically adopted to real products in the markets, there are a lot of challenges to overcome. In this dissertation, four types of the challenges are carefully studied and discussed to address them.

First, the grid-tied inverters used for distributed energy resources, such as PV systems, must continue operating to deliver power to the grid, when it faces flawed grid conditions such as voltage drop and voltage rise. During abnormal grid conditions, delivering constant active power from the inverter to the grid is essential to avoid large voltage ripples on the dc side because it could trigger over-voltage protection or harm the circuitries, eventually shutting down the inverter. Hence, in such cases, unbalanced ac currents need to be injected into the grid. When the grid voltages and the ac currents are not balanced, there is a chance for the CRM soft-switching inverter

to lose its soft-switching capability. Continuous conduction mode operation emerges, causing hard-switching where discontinuous conduction mode (DCM) operation is expected. This leads to huge turn-on loss and high dv/dt noise at the active switch's turn-on moment. To eradicate the hard-switching problem, two improved modulation schemes are developed; one with off-time extension in the CRM phase, the other by skipping switching pulses in the DCM phase. The DCM pulse skipping is applied for a variety of grid imbalance cases, and it is proven that it can be a generalized solution for any kinds of unbalanced grid conditions.

Second, the CRM soft-switching scheme with 2-channel interleaving achieves high efficiency at heavy load. Nevertheless, the efficiency plunges as the output load is reduced. This is not suitable for PV inverters, which take account of light load efficiency in terms of "weighted efficiency". Small inductor currents at light load cause the switching frequency to soar because of its CRM-based operation characteristic, causing large switching loss. To increase the inductor current dealt with by the first channel, a phase shedding control is proposed. Gate signals for the second channel are not excited, increasing the first channel's inductor current, thus cutting down the first channel's switching frequency. To prevent the unwanted circulating current formed by shared zero-sequence voltage in the paralleled structure, only two phases in the second channel working in high frequency are shed. The proposed phase shedding control achieves a 0.5 to 3.9 % efficiency improvement with light loads.

Third, due to the usage of SiC devices, high dv/dt generated at switching nodes over the system parasitic capacitance causes substantial common mode (CM) noise compared to that with Si devices. In this case, a balance technique with PCB winding inductors can effectively reduce the CM noise. First, winding interleaving structure is selected to minimize the eddy current loss in the windings. But the interwinding capacitance caused by the winding interleaving structure

aggravates the CM noise. Impact of the interwinding capacitance on the CM noise is analyzed with a new inductor model containing the interwinding capacitance. Then, finally, a novel inductor structure is proposed to remove the interwinding capacitance and to improve the CM noise reduction performance. The soft-switching ac-dc converter built with the final PCB magnetics features almost similar efficiency compared to that with litz-wire inductor and 14 to 18 dB CM noise reduction up to 15 MHz.

Lastly, the soft-switching technique is extended to inverters in standalone mode. To meet tight ac voltage total harmonic distortion requirements, a current control in dq-frame is introduced. As for the ac voltage regulation at no-load, on top of the improved phase shedding control, a frequency limiting with fixed frequency DCM method is applied to prevent excessive increase in the switching frequency. Then, how to deal with short-circuit at the output load is investigated. Since the soft-switching modulation violates inductor voltage-second balance during the short-circuit, the modulation method is switched to a conventional sinusoidal PWM at fixed frequency. It is concluded that all the additional requirements for the standalone inverters can be satisfied by the introduced control strategies.

Control, Analysis, and Design of SiC-Based High-Frequency Soft-Switching Three-Phase Inverter/Rectifier

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General Audience Abstract

The world is facing an unprecedented weather crisis. Global warming is getting more severe because of excessive amount of carbon emission. In an effort to overcome this crisis, paradigm of energy and lifestyle of people have changed. Penetration of distributed energy resources (DERs) such as wind turbines, and photovoltaic systems has been dramatically increased. Instead of internal combustion engine vehicles (EVs), electric vehicles hit the mainstream. In these changes, power electronics plays a critical role as the key element of the systems. Especially, three-phase inverter/rectifiers are essential parts in such applications.

Most important aspects of the three-phase inverter/rectifier are efficiency and power density. In the past decades, Silicon (Si) power devices were mostly used for the systems and the technology based on Si has almost reached to its physical limits. The switching frequency of Si-based inverter/rectifier is limited below 20 – 30 kHz to reduce switching loss. This impedes high power density due to bulky passive components such as inductors and capacitors.

Nowadays, the advent of wideband gap such as Silicon Carbide (SiC) and Gallium Nitride (GaN) power devices gives us a great opportunity to improve the efficiency and the power density with its high switching speed capability, low switching energy and low on-resistance. The SiC power devices are more suitable for DERs and EVs due to higher voltage rating. Using SiC power

devices allows to increase inverter/rectifier' switching frequency about five times to have similar efficiency with those based on Si power devices, making the power density high. However, there is still room to push the switching frequency even higher to hundreds of kHz with soft-switching.

In this sense, studies on soft-switching techniques for three-phase inverter/rectifier have been intensively conducted. Particularly, soft-switching techniques based on critical conduction mode (CRM) are regarded as the most promising solutions because it does not have any additional circuits to achieve the soft-switching, keeping the system as straightforward as possible. However, most of the studies for the CRM-based soft-switching three-phase inverter/rectifier mainly focus on limited occasions such as ideal operation conditions. For this technique to be widely used and adopted in industry, more practical cases for the systems need to be studied.

In this dissertation, the soft-switching three-phase inverter/rectifier under diverse situations are investigated in depth. First, behavior of the soft-switching inverter/rectifier under unbalanced grid conditions are analyzed and control methods are developed to maintain its soft-switching capability. Second, how to improve light load efficiency is explored. Circulating current issue for the light load efficiency improvement is analyzed and a control method is proposed to eliminate the circulating current. Third, a design methodology and considerations of inductors based on PCB magnetics are discussed to reduce electromagnetic noise and improve system efficiency. Lastly, the soft-switching technique is extended to standalone mode applications dealing with strict voltage regulation, no-load operation, and output short-circuit.

To My Family

My Parents: Gildon Son, Namhee Kim

My Parents in Law: Jooil Youn, Youngae Kwon

My Wife and Daughter: Haney Youn, Jieul Son

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Chapter 1 Introduction

1.1 Three-Phase AC-DC Converter Applications and Its Limits

With dramatically increasing demands on sustainable energy to achieve carbon neutrality, there are a lot of applications in which three-phase ac-dc converters play a pivotal role. The ac-dc converters are widely used for grid-tied applications such as electric vehicle (EV) charging, photovoltaic (PV) systems, and uninterruptable power supplies (UPS) 0-[3]. For EV charging, the ac-dc converter works as a rectifier to charge batteries. For PV systems, the ac-dc converter works as an inverter to deliver power to the grid. In UPS, there are two ac-dc converters, one works as a rectifier charging back up batteries, and the other works as an inverter supplying power to loads when the grid is not stable. It is also commonly used for the power supplies for three-phase loads in transportation, such as locomotives and aircrafts. These systems consist of two parts, as shown in Fig. 1-2: three-phase ac-dc stage and dc-dc stage. As the needs of the applications grow rapidly, they have drawn attention to how to improve the efficiency and power density of the ac-dc converter.

Fig. 1-1. Applications of three-phase ac-dc converters.

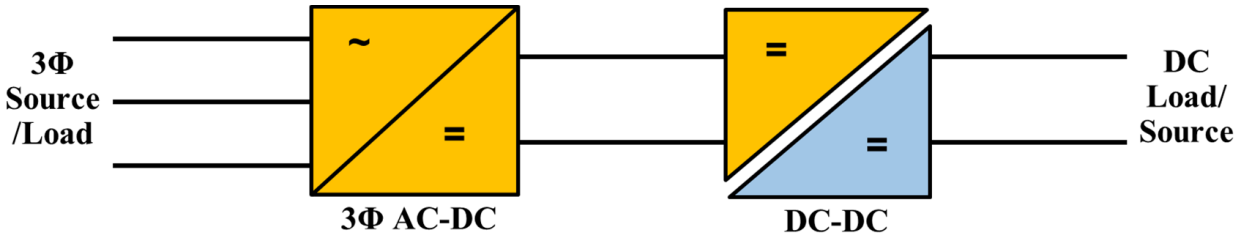


Fig. 1-2. Three-phase ac-dc converter configuration: ac-dc stage + dc-dc stage.

Fig. 1-3 illustrates commercial ac-dc converter products in the market, especially converter modules in the EV charging system. Even though efficiency of the converter modules is above 95%, power density is lower than 40 W/in^3, which is very low [4]-[7]. The reason behind it is that these products use silicon (Si) power devices, such as Si insulated gate bipolar transistors (IGBTs) or Si metal oxide semiconductor field effect transistors (MOSFETs). Then the switching frequency of the converter is limited to below 20 to 30 kHz to reduce switching loss. This makes passive components in the converters bulky, impeding high power density because the passive components generally take up more than 30 % of the converter's real estate. Basically, it is a tradeoff between efficiency and power density. With the matured technology for the Si devices, these have been pushed to the limit.

However, advent of wide band gap (WBG) power devices, such as silicon carbide (SiC), provides a new paradigm for design and control methods of the ac-dc converters. Its superb characteristics compared to its counterparts lead us to a new phase. Recently, the research goal in CPES has been to develop high efficiency and high power density three-phase ac-dc converters by using SiC power devices and pushing the switching frequency to several hundreds of kHz specifically, with a unique soft-switching technique based on critical conduction mode operation.

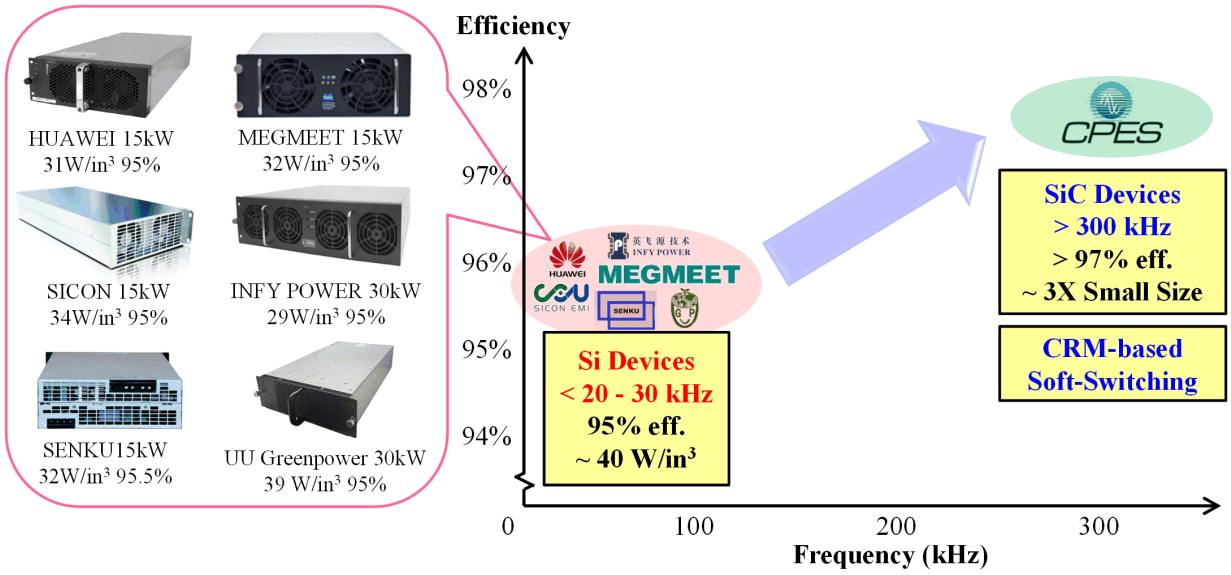


Fig. 1-3. Commercial products of EV charging modules in the market and research goal in CPES.

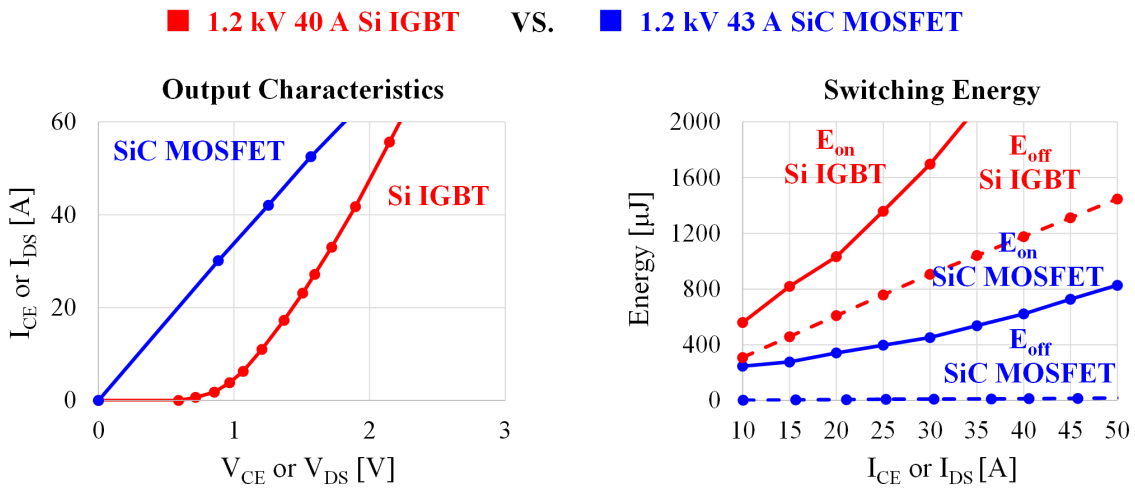


Fig. 1-4. Comparison of characteristics between Si IGBT and SiC MOSFET.

1.2 Benefits of SiC Devices

Recent developments in SiC MOSFETs provide a big opportunity to increase the switching frequency of the converter. Fig. 1-4 shows two superior characteristics of a SiC MOSFET (rated

voltage: 1200 V, rated current: 43 A) compared to its Si counterpart (rated voltage: 1200 V, rated current: 40 A). For the same breakdown voltage, SiC MOSFETs feature much lower on-resistance because of their higher doping concentration. On top of that, SiC MOSFETs have much lower switching energy, greatly smaller turn-on energy, and very little turn-off energy due to their fast switching speed with small reverse recovery charge, small gate charge, and small junction capacitance [8]-[10].

Fig. 1-5 represents the benefits of SiC MOSFETs over Si IGBTs on system performance based on the data shown in Fig. 1-4. A 4 kW continuous conduction mode (CCM) boost converter is taken as an example for the device loss estimation. When the two converters are operating at the same switching frequency (20 kHz), the SiC-based converter's conduction loss is much lower than that of an Si-based converter with the help of low on-resistance. Furthermore, the switching loss is also very small due to the low switching energy. One thing to note is that the turn-off loss reduction is the most noticeable among the switching related loss (turn-on, turn-off, and driving loss).

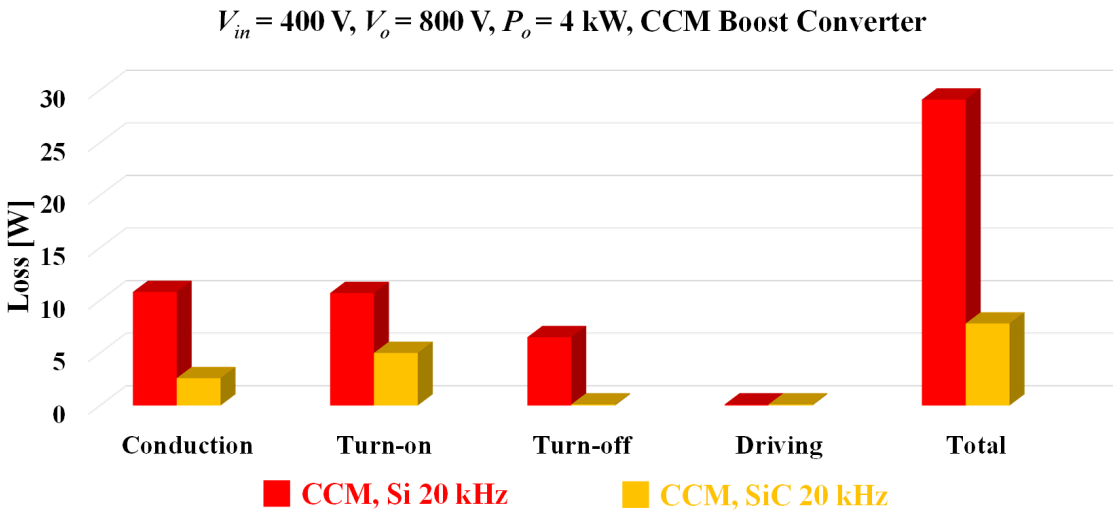


Fig. 1-5. Device loss comparison to show benefit of SiC MOSFETs over Si IGBTs on system performance.

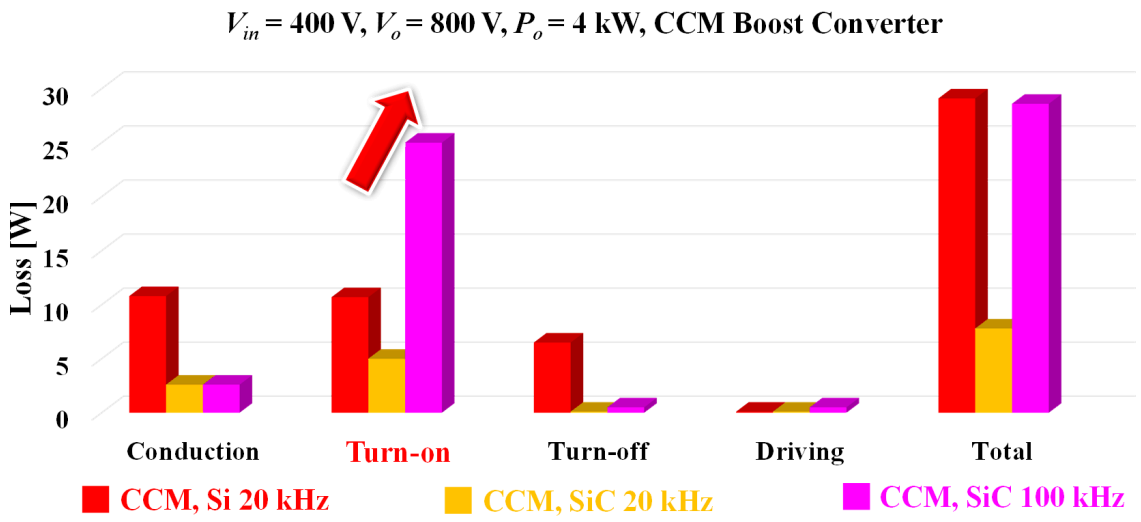


Fig. 1-6. Device loss comparison to show limit of SiC MOSFETs to push above hundreds of kHz.

The switching frequency of the SiC-based converter can be increased to about 5 times higher (100 kHz) to have a similar loss level with the Si-based converter at 20 kHz as shown in Fig. 1-6. In this case, because of the non-negligible turn-on energy of the SiC MOSFETs, the turn-on loss increases significantly and becomes dominant. This means that there is still limitation for increasing the switching frequency even with the SiC MOSFETs. Therefore, to further push the switching frequency up to several hundreds of kHz, zero voltage switching (ZVS) is essential.

1.3 Soft-Switching Three-Phase AC-DC Converters

1.3.1 Zero Voltage Switching (ZVS) with Auxiliary Circuits

There has been a lot of research to achieve ZVS for three-phase ac-dc converters. In early days, auxiliary circuits, called resonant tanks, were utilized for ZVS. In general, there are two main approaches with the auxiliary circuits. The first approach is to place an auxiliary circuit between the switch network and the dc side, as shown in Fig. 1-7(a) [11]-[14]. The auxiliary circuit is

comprised of an inductor, a switch, and a capacitor. The inductor in the additional circuit is in charge of achieving ZVS for all switches. The switch and capacitor are used to control the resonant current of the inductor for ZVS and clamp the voltage across the main switches to reduce the voltage stress. The second approach is to connect auxiliary circuits to the switching node of each phase leg as shown in Fig. 1-7(b) [15]-[17]. Unlike the first case, the auxiliary network in each phase leg is in charge of achieving ZVS for the corresponding phase. Even though these methods fulfill ZVS, the additional components increase cost and complexity of the system which render the approaches less appealing. Hence, these methods have been mostly studied in academia, but barely used in real products.

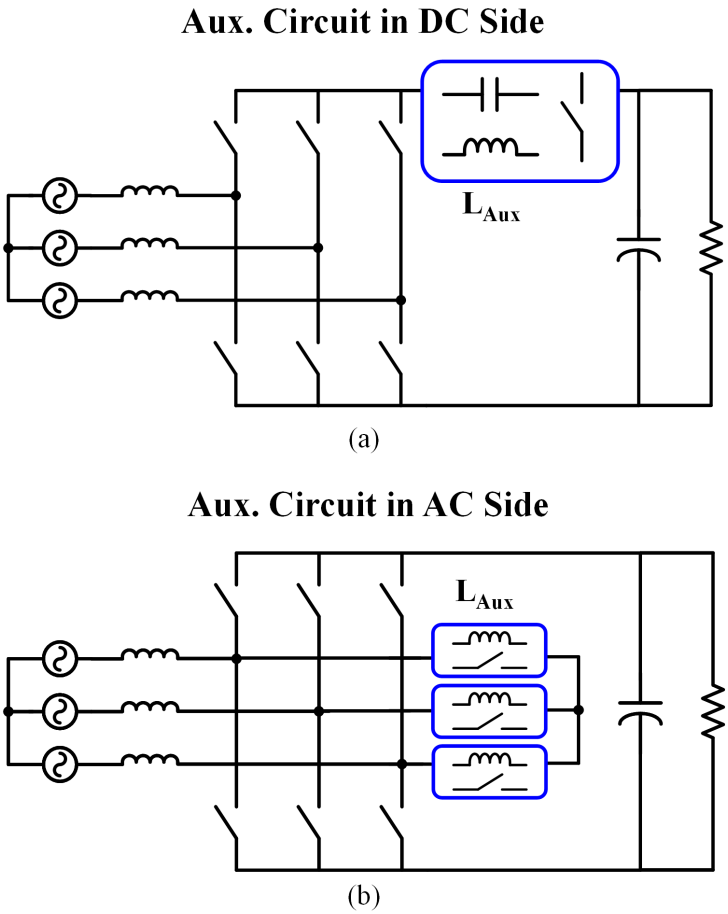


Fig. 1-7. Soft-switching three-phase ac-dc converters with an auxiliary circuit (a) at dc side and (b) at ac side.

1.3.2 Critical Conduction Mode (CRM) and Constraint in Three-Phase Systems

Critical conduction mode is one of the most straightforward means to achieve ZVS without any additional circuits. Take a boost converter, shown in Fig. 1-8, as an example. When the inductor current touches zero at t_1, the synchronous rectifier (SR), Q_2, is turned off. Then, the inductor and the output capacitors of the switches start to resonate. During the resonant period, the drain-to-source voltage of the active switch, Q_1, goes down to zero at t_2 and ZVS can be fulfilled. The energy stored in the inductor itself is employed for the soft-switching. Despite the increased turn-off current for Q_1 owing to the enlarged current ripple, SiC MOSFETs' diminutive turn-off energy, depicted in Fig. 1-4, renders the increase in the turn-off loss not so severe. Also, the large current ripple increases conduction loss, but it is relatively small compared to Si IGBT due to smaller on-resistance. The gain from the soft-switching turn-on by CRM outweighs the cons. That is to say, CRM can maximize SiC devices' superiority. Fig. 1-9 shows the system benefit of CRM with SiC MOSFETs. When the switching frequency of the SiC-based CRM converter is pushed to 300 kHz, the device loss level is analogous to the SiC-based CCM converter at 20 kHz. This clearly indicates that CRM with SiC allows us to increase switching frequency by up to hundreds of kHz.

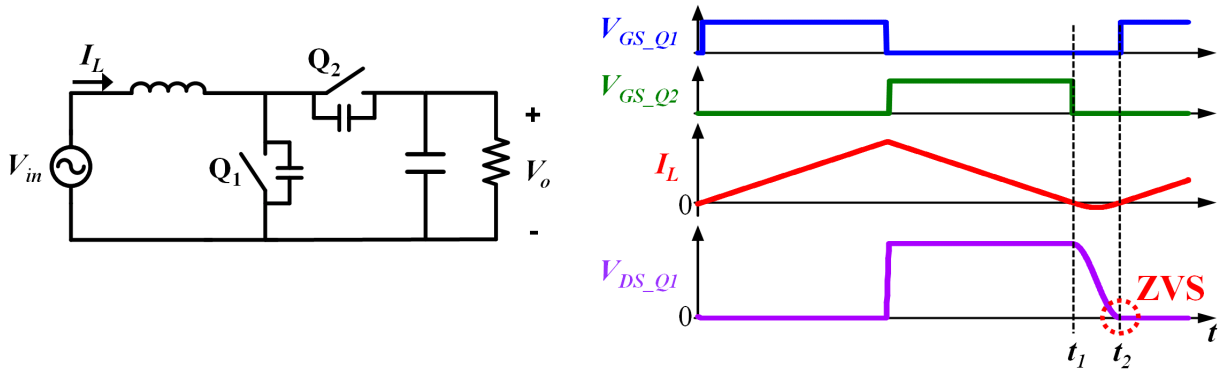


Fig. 1-8. CRM boost converter. (a) Circuit diagram and waveforms. (b) Equivalent circuit model of CM noise.

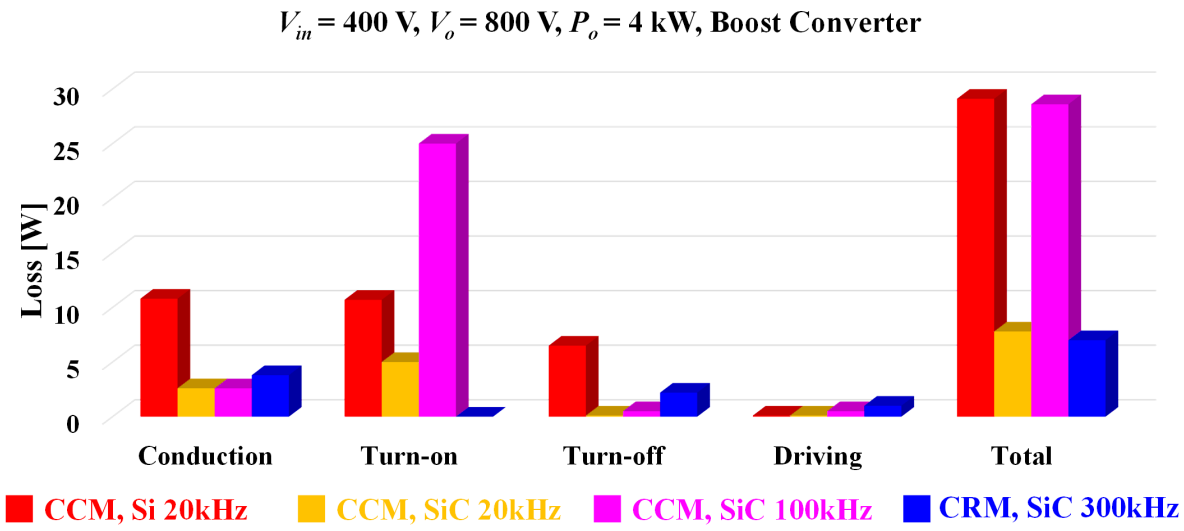


Fig. 1-9. Device loss comparison to show the benefit of CRM with SiC MOSFETs at hundreds of kHz

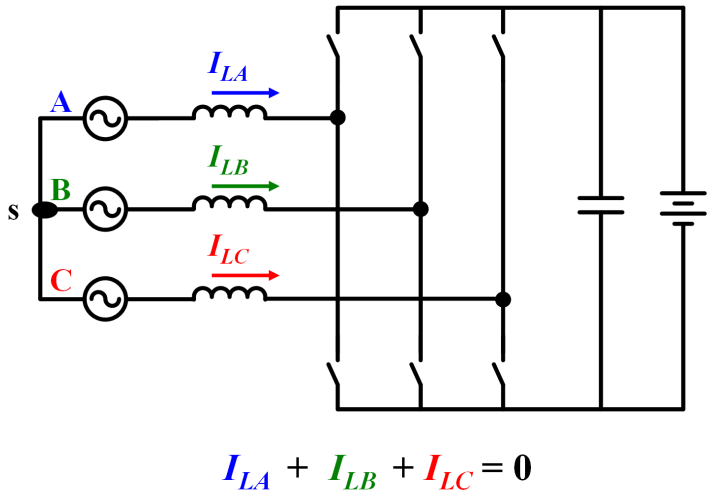


Fig. 1-10. Two control freedom in three-phase three-wire system.

Research on how to extend CRM to a three-phase system has been actively conducted. However, in the three-phase three-wire configuration exhibited in Fig. 1-10, all phases are coupled together via the neutral point, s, at the ac side and summation of the three-phase currents must be equal to zero. One phase current is determined by the other two-phase currents. This denotes that

there is only two control freedom in this structure. Because of the inherent limitation, controlling all phases as CRM independently is hard to achieve, as it is the key for CRM to control turn-on instant of active switches in each phase independently at a right timing for ZVS.

1.3.3 ZVS with CRM in Three-Phase Four-Wire Configuration

To avoid this constraint, [18] and [19] use three-phase four-wire configuration. The 4th wire links the ac side's neutral point and the dc capacitor's middle point, as shown in Fig. 1-11(a). This decouples the three phases so that it can be treated as three single-phase converters. As a result, each phase can be controlled as CRM independently. However, the switching frequency range over the line cycle is extremely wide as shown in Fig. 1-11(b). This increases the switching related loss substantially and causes a burden on control.

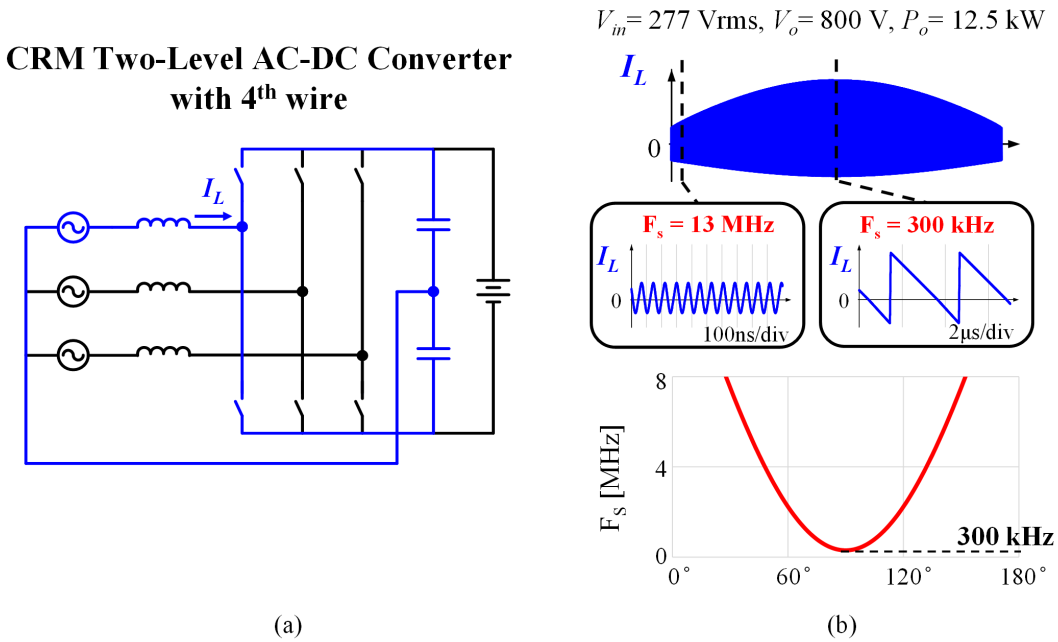


Fig. 1-11. CRM-based two-level three-phase ac-dc converter with 4th wire: (a) circuit diagram and (b) frequency distribution.

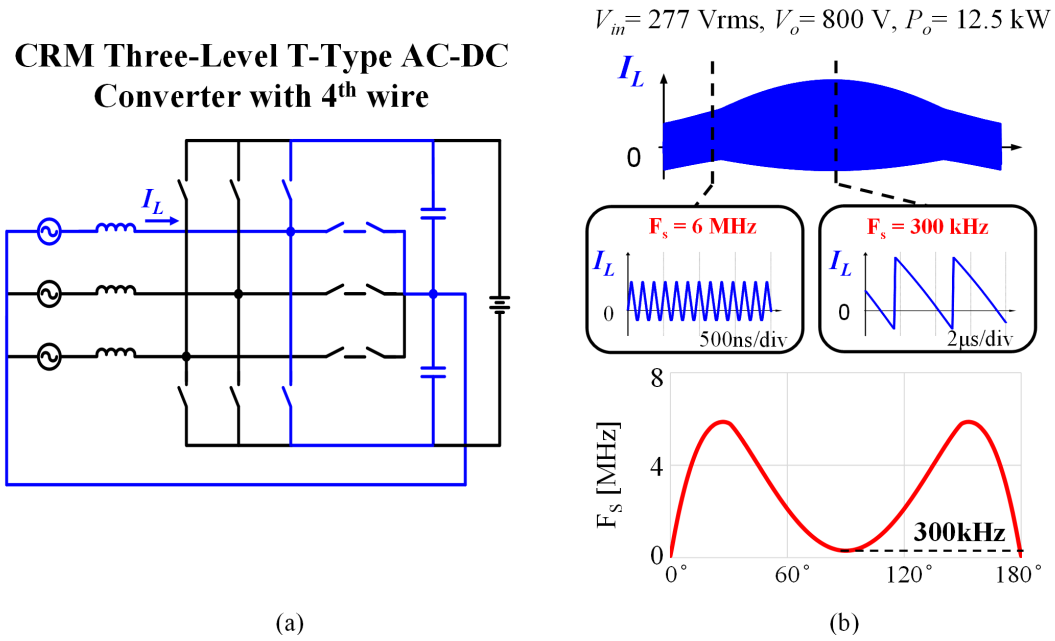


Fig. 1-12. CRM-based three-level T-type three-phase ac-dc converter with 4th wire: (a) circuit diagram and (b) frequency distribution.

In Fig. 1-12, the same concept is used for three-level T-type topology [20]. In this configuration, three-phases are also decoupled by adding the 4th wire, and each phase is controlled as CRM independently. Although the frequency range is reduced by means of lower voltage across the inductor during the turn-off interval ($V_{in} - V_o/2$) compared to the previous case ($V_{in} - V_o$), which makes active switch turn-off time longer, though it is still very wide. It is obvious that the main challenge here is the extremely wide frequency range with CRM in the three-phase systems.

1.3.4 ZVS with CRM in Three-Phase Three-Wire Configuration

To cope with the constraint, [21]-[23] propose an innovative soft-switching modulation on the basis of CRM for the three-phase three-wire system. The key concept of this modulation is to fix switching status of one phase and let two phases operate at CRM freely. This is realized by adapting discontinuous pulse width modulation (DPWM), which is frequently used in conventional CCM-

based modulation method to reduce switching loss. In DPWM, one phase does not have any high frequency switching action. Instead, it is clamped to the dc-rail. In this manner, separate CRM control for the other two phases can be conducted as shown in Fig. 1-13(a). The clamping mode is assigned to the phase that has the highest instantaneous ac voltage, as shown in Fig. 1-13(b). The other two phases have a dedicated current controller to realize independent CRM.

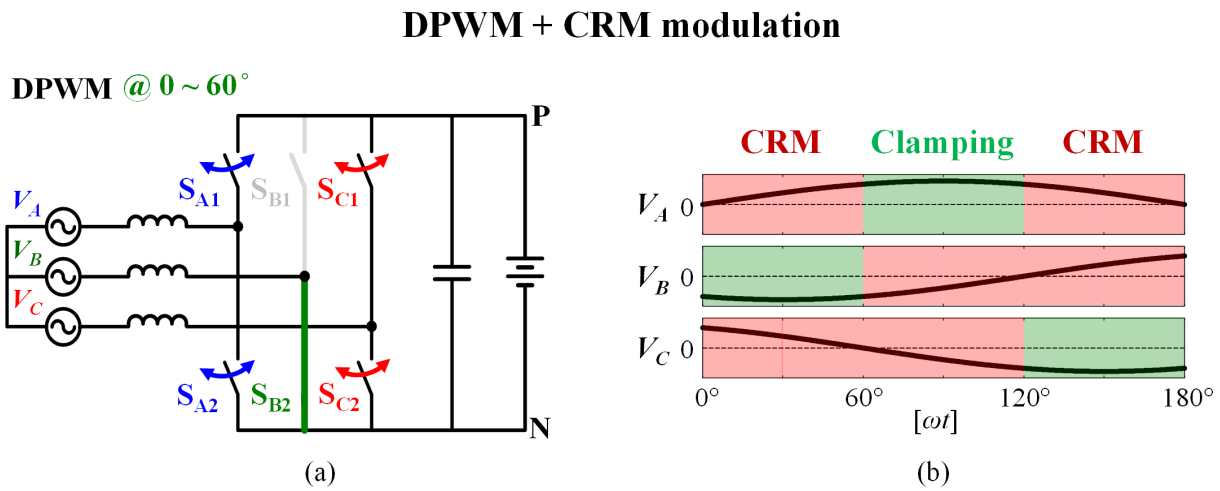


Fig. 1-13. DPWM + CRM modulation. (a) Switching status at 0 to 60°. (b) Operation mode of each phase.

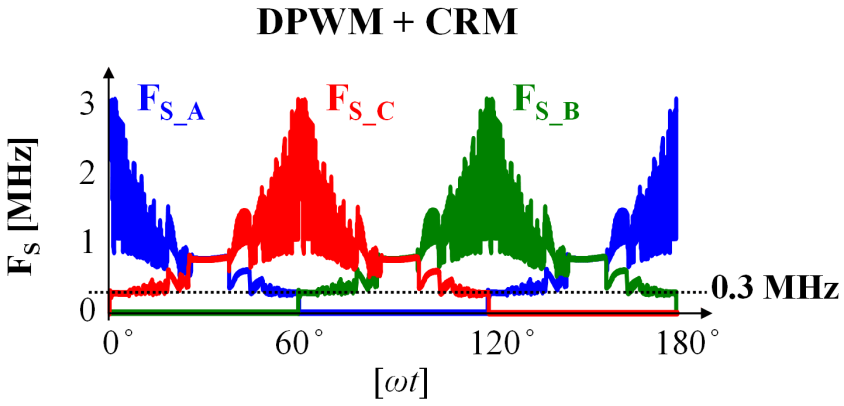


Fig. 1-14. Switching frequency range of three-phase ac-dc converter with DPWM + CRM modulation in [23].

The “DPWM + CRM” modulation method makes the frequency range much narrower than those methods with the 4th wire approaches, but it is still quite wide along the line cycle. Fig. 1-14 illustrates switching frequency distribution for all phases under a specific working condition (V_{AC} = 277 Vrms, V_o = 800 V, Po = 12.5 kW) at the minimum frequency 300 kHz [23]. Minimum frequency to maximum frequency ratio is around 1:10. This is still not satisfying because of the high switching loss and the control burden.

To further shrink the frequency variation, a frequency synchronization is proposed [23]. In this concept the two phases’ frequencies, excluding the clamping mode phase, are synchronized. The basic principle of the frequency synchronization is to make the frequency of one phase that has higher switching frequency equal to that of the other phase. For instance, the first 30 degrees in Fig. 1-14, phase A frequency (blue) is higher than that of phase C (red). Then, the frequency of phase A is synchronized with phase C. How to realize this is 1) Operate phase A at DCM rather than CRM, and, 2) Align the timing of the phase A turn-on with that of phase C, as depicted in Fig. 1-15. i_{LA} is phase A inductor current and i_{LC} is phase C inductor current. I_{A_Ref} is phase A ac current reference and I_{C_Ref} is phase C ac current reference. V_{GS_A} and V_{GS_C} are phase A and phase C active switch gate-to-source voltage. In a unity power factor case, the CRM phase ac current is consistently larger than that of the DCM phase, so i_{LA} first crosses zero at t_0. Later, i_{LC} reaches zero at t_1. The turn-on of the active switch in the CRM phase is done at t_2, after some delay is given for phase C to participate in LC resonance for ZVS. At this moment, the turn-on of the active switch in the DCM phase is carried out for the synchronization. Now that the CRM phase determines the switching frequency, the CRM phase is the leader phase, and the DCM phase is the follower phase.

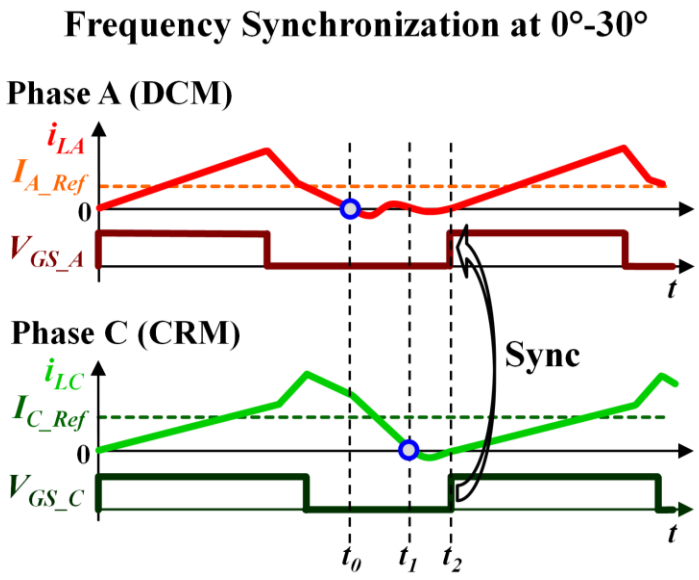


Fig. 1-15. Frequency synchronization concept.

Synchronization of two phases' frequency is conducted over the whole line cycle in the same sense (e.g., phase C synchronized to phase A during 30°-60°). After all, the operation mode in one phase rotates at clamping mode, CRM, and DCM. Selection of the operation mode can be easily done by comparing the instantaneous ac voltage among three phases as represented in Fig. 1-16. The phase with the largest ac voltage works in clamping mode. Another phase with the smallest ac voltage becomes the DCM phase and the remaining phase becomes the CRM phase. The frequency range over the line cycle shrinks considerably, as illustrated in Fig. 1-17 (gray: DPWM + CRM, blue/red/green: DWPM + CRM + frequency synchronization). Eventually the minimum to maximum frequency ratio is reduced to be lower than 1:2.

Through the soft-switching technique, a 25 kW bidirectional three-phase ac-dc converter is developed [23]. The main features of the converter are 1) The switching frequency is pushed above 300 kHz with SiC MOSFETs, and 2) To cope with high power and cancel out the large inductor current ripple, two converter modules are paralleled and 180-degrees interleaved in a switching

cycle, called 2-channel interleaving. Through this, 98.9 % peak efficiency and 127 W/in^3 power density are fulfilled. This accomplishment validates that the soft-switching technique is a very attractive solution for high efficiency and high power density three-phase ac-dc converters.

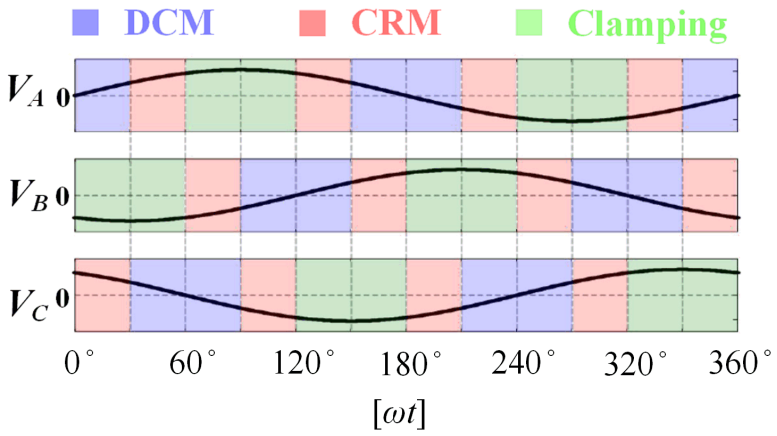


Fig. 1-16. Operation mode of DPWM + CRM + Frequency synchronization.

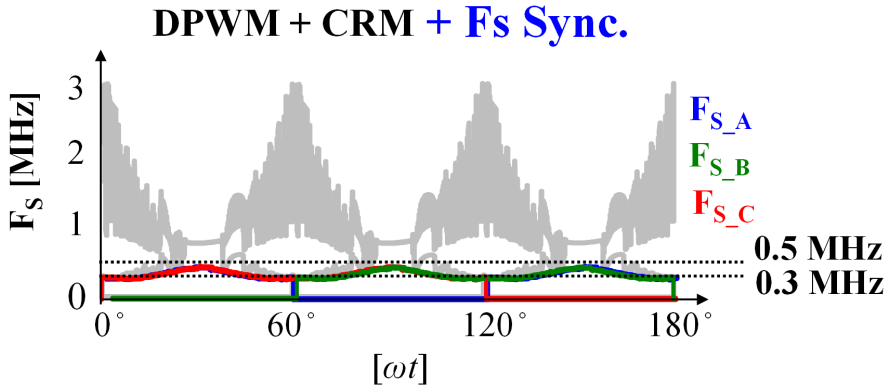


Fig. 1-17. Frequency range comparison: DPWM + CRM vs. DPWM + CRM + Frequency synchronization.

Similar soft-switching methods adopting DPWM have been introduced in [24]-[30] and show relatively narrow frequency range compared to those with 4th wire. [24]-[27] use the same frequency synchronization concept, but different synchronization timing. These run one phase

triangular current mode (TCM) instead of CRM. [28]-[30] use TCM for two phases running at high frequency. In these literatures, how to use space vector modulation for required switching period instead of detecting the zero current of the inductors. In this dissertation, the soft-switching method in [23] is focused on and studied carefully.

1.4 Challenges in CRM-Based Soft-Switching Three-Phase AC-DC Converter

1.4.1 Challenge in Maintaining Soft-Switching Capability at Unbalanced Grids

The first challenge is to deal with unbalanced grid conditions. During a grid imbalance, an unbalanced ac current reference is required for the grid-tied inverters to deliver constant active power to the grid. The question is if the high-frequency soft-switching inverter can maintain its soft-switching capability. The accomplishments of high efficiency and high power density at several hundreds of kHz frequency is attributable to an inverter's soft-switching ability. But if it lost this ability, it would become a double-edged sword. As the inverter runs at very high-frequency, drastic switching loss increase is anticipated. Additionally, a noise issue might arise on account of high dv/dt at switching nodes, due to hard-switching. This might give rise to a false turn-on and a shoot-through, eventually, an over-current problem.

1.4.2 Challenges in Light Load Efficiency Improvement

Even though the CRM-based soft-switching inverter has a very good performance from an efficiency point of view at heavy load, the efficiency decrease is quite rapid as the output power becomes lighter. At light loads, the inductor current in each channel is smaller, bringing about a sharp increase in the switching frequency due to its CRM-based operation. In accordance with this,

switching loss escalates. In PV systems, the efficiency at light loads is regarded as crucial as that at heavy loads because the power generated by PV panels varies depending on weather conditions like irradiation and ambient temperature. Then the term "weighted efficiency" is an important aspect to grade the performance of PV inverters, which takes into consideration for efficiency at different loads. Therefore, the light load efficiency of the soft-switching inverter must be improved.

1.4.3 Challenges in Common Mode Noise Reduction with Low Inductor Loss

The third challenge is to reduce common mode (CM) electromagnetic interference (EMI) noise with minimized inductor loss. Owing to the fast-switching characteristic of SiC devices, the dv/dt at the switching node of the converter is much higher than that with Si devices. The high dv/dt over parasitic capacitance, which exists between the power circuit and the earth ground, forms a substantial amount of CM noise. In order to abide by electromagnetic compatibility (EMC) standards, a large CM filter is needed between the ac side and the converter, thus depreciating the benefit from using SiC devices with CRM at high frequency (size reduction for inductors in the power stage and overall DM filter). A balance technique with PCB-based magnetics efficiently alleviates the CM noise of the ac-dc converter up to 10-20 MHz. However, it is very difficult to have both good CM noise reduction performance and low inductor loss at the same time. Therefore, the PCB winding inductor for balance technique needs to be carefully designed.

1.4.4 Challenges in Extension of Soft-Switching Technique to Standalone Mode

The last challenge is to extend the soft-switching technique to a standalone mode inverter, since the inverter in standalone mode must satisfy several requirements that are not necessary in grid-connected applications. To be specific, the output ac voltage total harmonic distortion (THD)

regulation is very tight in some applications because it becomes the power source for electric loads. Also, the output ac voltage needs to be regulated even under no-load conditions for standby, wherein the inductor current becomes extremely small, leading to excessively high switching frequency. On top of that, the inverter needs to be capable of handling output short-circuit. It must be guaranteed that the soft-switching inverter can deal with all of these requirements.

1.5 Dissertation Outline

Chapter 1 discusses the background of the SiC-based high-frequency soft-switching three-phase ac-dc converters. Prior arts of soft-switching three-phase are introduced, and remaining challenges are identified.

Chapter 2 investigates the CRM-based high-frequency soft-switching inverter at grid imbalance. Current control strategies for imperfect grids, specifically voltage drop, are discussed, and the ramifications of the unbalanced grid on the soft-switching inverter are analyzed. Control methods to overcome unexpected hard-switching issues led by non-ideal grid conditions are proposed and verified for a variety of voltage sags.

Chapter 3 proposes two phase shedding controls to ameliorate the light load efficiency. The principle of the phase shedding is elaborated. Then an issue in regard with an undesired circulating current is analyzed in depth. In an effort of avoiding the circulating current, an improved phase shedding is proposed. Both phase shedding methods are compared from efficiency perspective and the improved phase shedding control is verified experimentally.

Chapter 4 presents in-depth study on design considerations for the PCB winding coupled inductor for the balance technique in a three-phase ac-dc converter. Diverse inductor structures

with different winding arrangement, coupling between inductors are investigated to comprehend its implications on converter efficiency and CM noise reduction performance. Finally, a novel inductor structure is selected to reduce CM noise and achieve high converter efficiency.

Chapter 5 investigates a variety of control strategies for a soft-switching inverter in standalone mode. An average current control structure in dq-frame for the soft-switching to achieve low THD, a frequency limiting method to reduce switching loss for no-load condition, and a control scheme to cope with the output short-circuit are discussed.

Chapter 6 concludes the dissertation and discusses the future work.

Chapter 2 Control Techniques for Soft-Switching Three-Phase Inverter/Rectifier Under Unbalanced Grid Conditions

2.1 Introduction

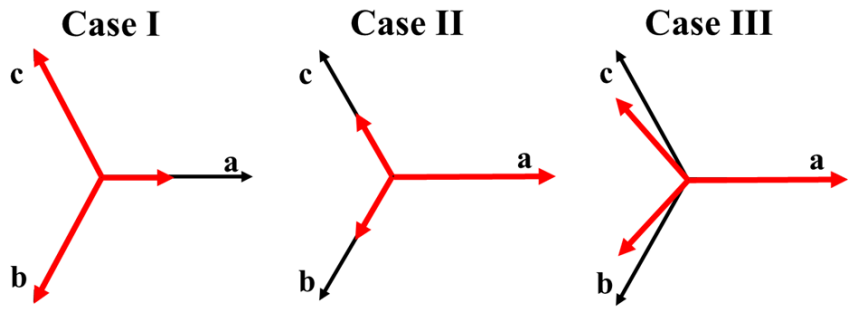


Fig. 2-1. Phasor diagrams for voltage sags.

Three-phase ac-dc converters for the grid-tied applications commonly encounter abnormal grid conditions. Short-circuit at any point connected to the grid brings about voltage sag. This is one of the most recurrent grid faults, resulting in either voltage decrease or shifted angle between phases, or both phenomena. Fig. 2-1 describes classic grid imbalances of voltage sag in phasor diagrams. In Case I, one phase and the ground are shorted, and the shorted phase has voltage drop. Case II shows voltage drop in two phases, but no angle shift. This takes place when two phases are shorted with the ground. Case III arises when two phases are shorted to each other causing phase shift between the two phases as well as voltage drop in the two phases. It should be mentioned that there are more kinds of grid imbalances seen to users because the form of grid imbalance can be transformed by penetrating different types of transformers. But, here only the

three cases in Fig. 2-1 will be covered as representatives. The level of the decrease in voltage and the angle change is contingent on the entire grid's characteristics, such as the source impedance at the point-of-common coupling (PCC) and the impedance between the PCC and the fault [31].

The most challenging parts to control the inverter at such grid cases are the following: The first challenge is whether the inverter is able to remain connected to the grid without stopping its operation. This is called fault ride through (FRT), more particularly low voltage ride through (LVRT) in the cases of voltage drop. In the past, the grid-connected inverters for distributed energy resources (DERs) shown in Fig. 2-2 were expected to terminate their work over the abnormal grids because DERs were regarded as unwelcome guests to the grid, due to the possibility of bringing hidden disturbances [32]. However, as time goes by, the penetration of DERs has soared. The power generated by DERs has increased more and more, and finally it begins to play an important role in the grid. Now the tendency is changing in a way that the inverters are asked to support the grid through stable power provision during the imbalance [33].

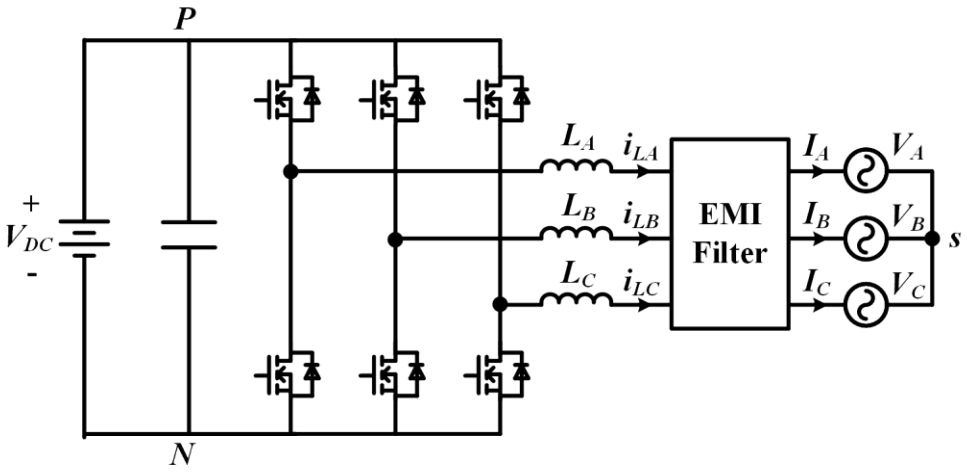


Fig. 2-2. Grid-tied three-phase two-level inverter.

When the grid becomes unbalanced, if balanced ac currents are injected to the grid by the inverter, the output active power oscillation in twice the line frequency happens [34]. The active power oscillation is reflected to the inverter's dc side, giving rise to excessive voltage ripple, shutting down the inverter. This is depicted in Fig. 2-3 in detail. For example, if there is one phase voltage drop, and if the balanced ac currents are injected to the grid as the normal grid condition, the instantaneous active power at the output has the double line cycle oscillation as illustrated in Fig. 2-3(b). This low frequency oscillation is directly seen at the dc bus voltage (for two stage systems) or at the dc input of the system (for one stage systems) in terms of the large voltage ripple in Fig. 2-3(a). This is not desirable because it could lead to shutdown of the inverter operation by over-voltage protection or even damage the circuit. In this sense, constant active power delivery is necessary. In [35]-[39], a lot of studies on forming proper ac current reference at grid imbalances have been done to steer clear of the active power oscillation.

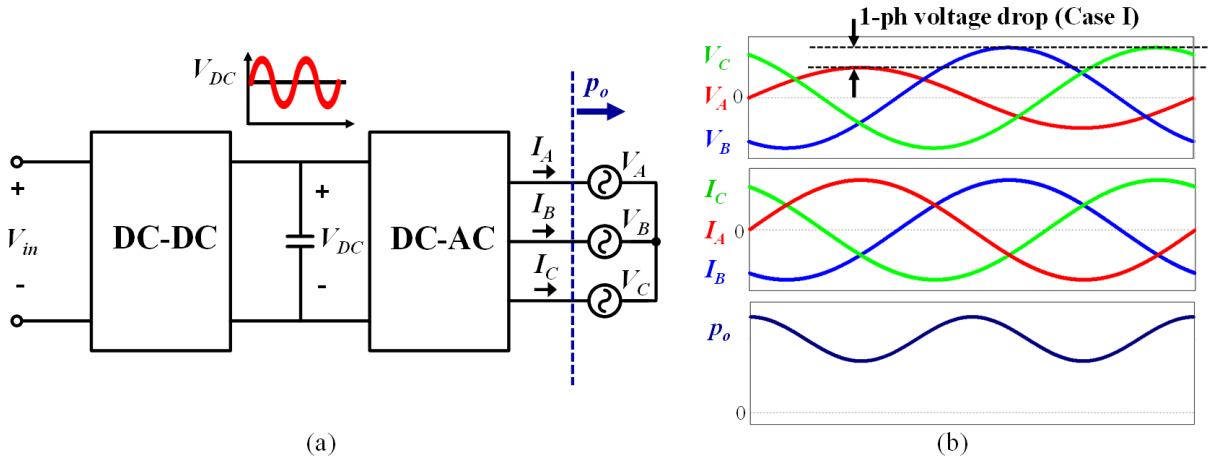


Fig. 2-3. Double line frequency oscillation by unbalanced grid.

The next challenge is to retain the inverter's soft-switching capability. The fulfillments of the high-frequency soft-switching inverter is attributable to its soft-switching. Yet, if the soft-switching capability is lost, the high switching frequency operation itself points a sword at the

inverter because the switching loss escalates significantly. Furthermore, hard-switching might cause severe noise in the circuit, which can be a source of false triggering of switches. Then an over-current problem arises, or even critical damage on the circuit could occur [40], [41]. Research related to the first hurdle have been conducted massively, thus, in this chapter the second hurdle is primarily focused on.

2.2 Implication of Grid Imbalance on High-Frequency Soft-Switching Three-Phase Inverter Control

2.2.1 Current Control for Constant Active Power Delivery

To avoid the double line frequency power oscillation, constant active power needs to be delivered. This requires modification of the ac currents during the abnormal grid. Some articles [35]-[39] explain diverse methods to form the appropriate ac current reference for constant active power when the grid has imbalances. The expression for the instantaneous output active power is as follows:

$$p_o = \mathbf{v} \cdot \mathbf{i} = \mathbf{v}^+ \cdot \mathbf{i}^+ + \mathbf{v}^- \cdot \mathbf{i}^- + \mathbf{v}^+ \cdot \mathbf{i}^- + \mathbf{v}^- \cdot \mathbf{i}^+ \tag{2-1}$$

where $\mathbf{v} = [V_A\ V_B\ V_C]$ is a vector for the ac voltage and $\mathbf{i} = [I_A\ I_B\ I_C]$ is a vector for the ac current. The superscripts added to these vectors denote the positive sequence ("+") element and the negative sequence ("–") element. It can be observed from equation (2-1) that there exist countless combinations to create the current reference for the constant active power. In [35], five representative combinations are introduced, but the positive-negative sequence compensation (PNSC) method in which the ac current does not include harmonic components is dealt with in the following discussion, as this method brings less contamination to the grid compared to others. In this method, the ac currents

provided to the grid are merely comprised of positive and negative sequence components in a sinusoidal form. This is achieved by the equations below.

$$\mathbf{v}^{+} \cdot \mathbf{i}^{+} + \mathbf{v}^{-} \cdot \mathbf{i}^{-} = P_o \tag{2-2a}$$

$$\mathbf{v}^{+} \cdot \mathbf{i}^{-} + \mathbf{v}^{-} \cdot \mathbf{i}^{+} = 0 . \tag{2-2b}$$

P_o is the dc value of the instantaneous active power. Multiplying $\mathbf{v}^{+}$ both sides in (2-2b) yields $\mathbf{i}^{-}$ as

$$\mathbf{i}^{-} = -\frac{\mathbf{v}^{-} \cdot \mathbf{i}^{+}}{\left|\mathbf{v}^{+}\right|^2} \mathbf{v}^{+} . \tag{2-3}$$

After multiplying $\mathbf{v}^{+}$ at both sides in (2-2a) as

$$(\mathbf{v}^{+} \cdot \mathbf{i}^{+} + \mathbf{v}^{-} \cdot \mathbf{i}^{-})\mathbf{v}^{+} = P_o \mathbf{v}^{+} \tag{2-4a}$$

(2-3) is substituted into (2-4a). This derives $\mathbf{i}^{+}$, which is expressed as

$$\mathbf{i}^{+} = \frac{P_o}{\left|\mathbf{v}^{+}\right|^2 - \left|\mathbf{v}^{-}\right|^2} \mathbf{v}^{+} . \tag{2-4b}$$

Lastly, the summation of (2-3) and (2-4b) gives the ac current reference, $\mathbf{i}_{Ref}$, as follows [35]:

$$\mathbf{i}_{Ref} = \frac{P_o}{\left|\mathbf{v}^{+}\right|^2 - \left|\mathbf{v}^{-}\right|^2} \mathbf{v}^{+} - \frac{P_o}{\left|\mathbf{v}^{+}\right|^2 - \left|\mathbf{v}^{-}\right|^2} \mathbf{v}^{-} . \tag{2-5}$$

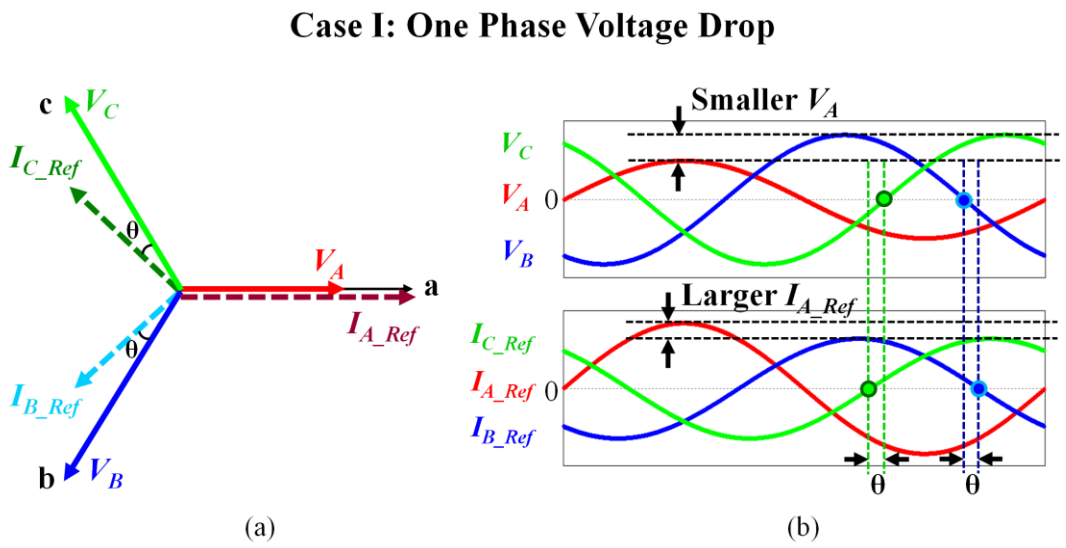


Fig. 2-4. Grid voltage under Case I voltage sag and ac current reference for constant active power.

Fig. 2-4 illustrates an example of Case I voltage sag. Phase A has a voltage drop, and phase B and phase C voltages are normal. The required ac current reference is calculated from (2-5). The voltage and the ac current reference are drawn in a phasor diagram in Fig. 2-4(a) and as time-domain waveforms in Fig. 2-4(b), respectively. As phase A has smaller voltage than other phases, phase A ac current is enlarged. Then, the angle of phase B and phase C currents are shifted, indicated as θ, from the corresponding phase voltage so that all three-phase currents' summation can be equal to zero. In other words, the ac currents become unbalanced as well. Then, the question is whether the soft-switching inverter can inject the unbalanced ac currents into the grid properly.

2.2.2 Unbalanced AC Voltage and Current Reference's Impact on Soft-Switching

When the soft-switching modulation proposed in [23] is applied to the grid imbalance without any modification, the inverter's operation mode changes, as the mode selection is decided by the instantaneous value of the ac voltage. Fig. 2-5 shows the operation mode comparison between the normal grid and Case I voltage sag with 30 % voltage drop in phase A. For the normal grid, the

tendency for the operation mode is perfectly symmetrical, repeating rotation of each phase's mode at every 30 degrees. On the other hand, the operation mode in an unbalanced case becomes asymmetrical. It is also worthwhile to mention that the current refence in the CRM phase is not always larger than that in the DCM phase. This never happens with the balanced grid. The CRM phase current reference is higher than the DCM phase current reference all the time during the balanced grid since the ac current reference is in phase with and proportional to the ac voltage as illustrated in Fig. 2-5.

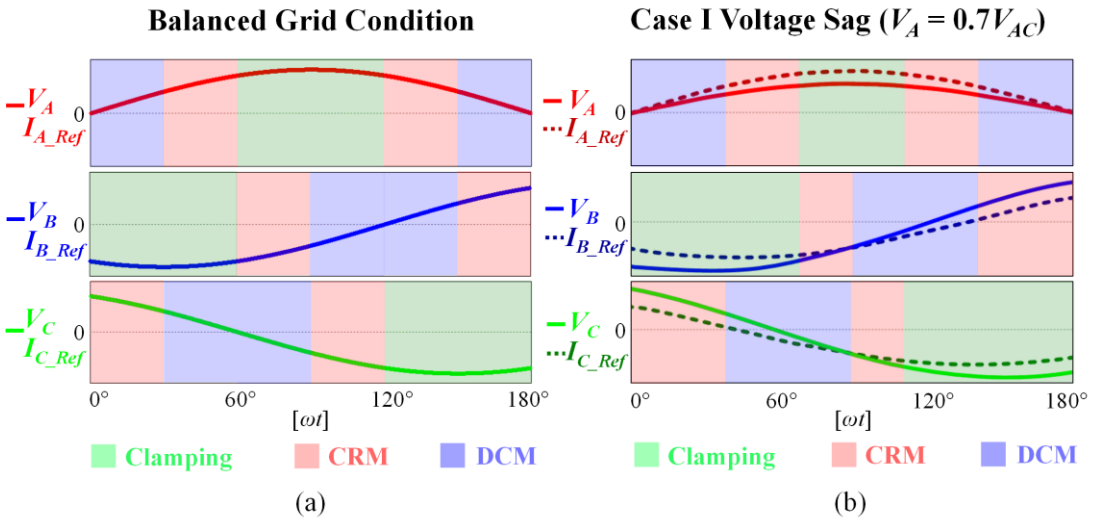


Fig. 2-5. Comparison for operation mode and ac current references: (a) balanced grid and (b) unbalanced grid with Case I voltage sag.

Simulation results for the soft-switching inverter at a specific operating condition under Case I voltage sag mode (V_{DC} = 800 V, V_{AC} = 277/480 V_{rms}, $V_A = 0.7V_{AC}$, P_o = 12.5 kW) are represented in Fig. 2-6. In Fig. 2-6(a), the inductor current (i_{LA}, i_{LB}, i_{LC}), the ac current reference (I_{A_Ref}, I_{B_Ref}, I_{C_Ref}), and the output active power (P_o) in the line cycle are shown. The output active power is free from double line frequency oscillation because the inductor currents are controlled well to track the unbalanced ac current references. This indicates that there is no issue from the line cycle point of view. By the way, when taking at a close look at the switching cycle waveforms in Fig. 2-6(b), which shows

zoomed-in waveforms for the yellow shaded region, an unexpected phenomenon is observed. In this region, DCM operation, clamping mode, and CRM operation are assigned to phase A, phase B, and phase C, respectively. It seems that around 15°, phase A operates at DCM and phase C operates at CRM adequately as intended. Turn-on synchronization for phase A is conducted at the phase C turn-on instant. The same thing appears around 25°. However, at 32°, even though phase A turn-on is still synchronized at the phase C turn-on instant, the phase A inductor current has not reached zero yet by the synchronization instant. As a result, phase A operates at CCM, instead of DCM differing from what is intended. This means the inverter loses soft-switching.

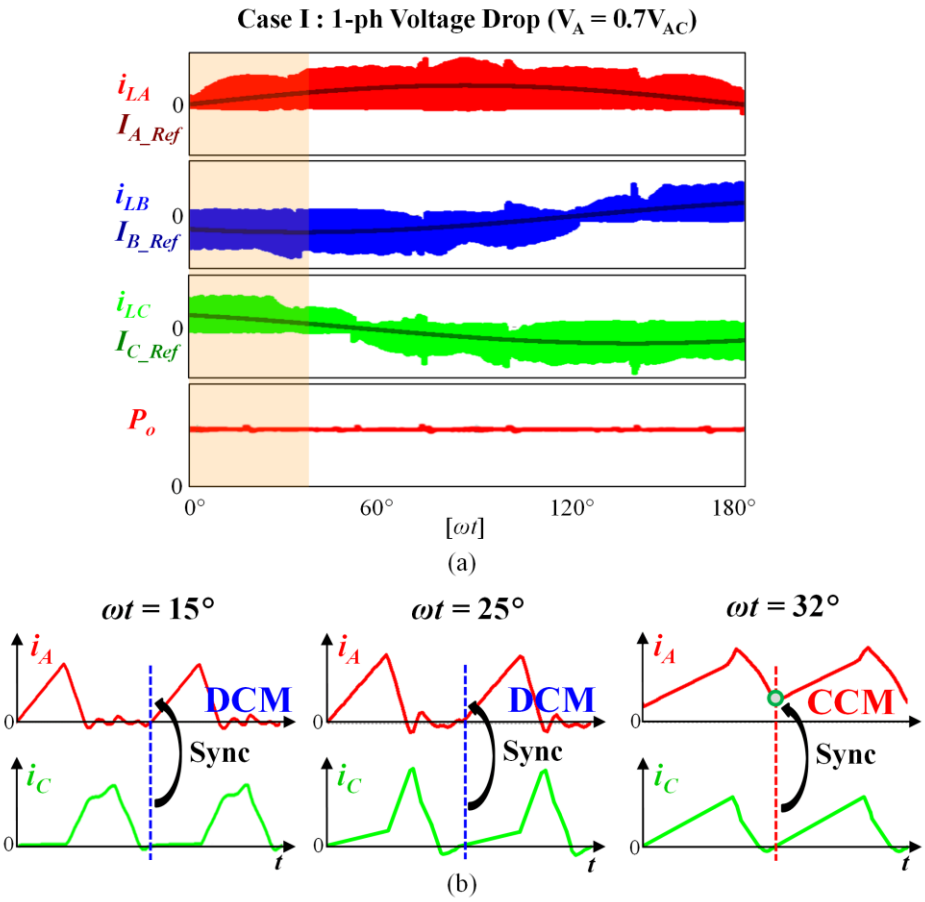


Fig. 2-6. Simulated waveforms of soft-switching inverter under Case I voltage sag: (a) line cycle and (b) switching cycles.

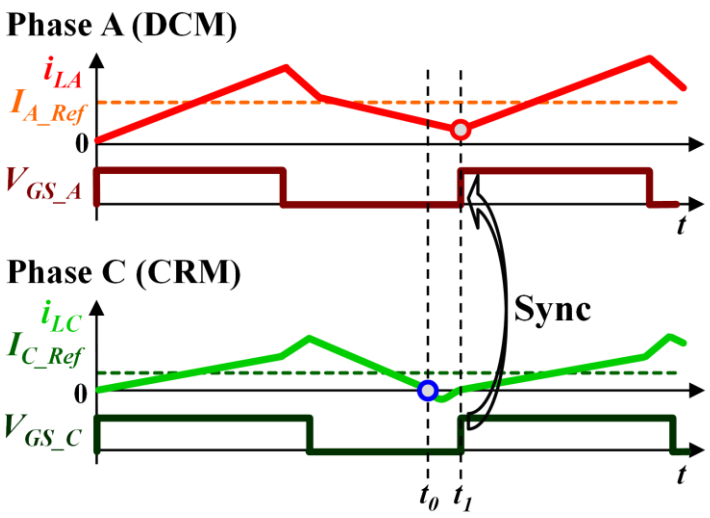


Fig. 2-7. Switching cycle waveforms where CCM occurs in DCM phase.

Fig. 2-7 exhibits the detailed switching cycle waveforms of phase A and phase C in the yellow shaded region, specifically at the point where CCM starts to arise. The reason why the CCM problem takes place at which DCM is expected is elaborated on this figure. Opposed to that shown in Fig. 1-15, CRM phase's inductor current, i_{LC}, hits zero first at t_0. Afterward, CRM phase's active switch is turned on at t_1. At this point, the DCM phase active switch is turned on, according to the frequency synchronization concept. But the DCM phase inductor current has not crossed zero yet by the synchronizing action. It is worth noting that the DCM phase inductor current's final value differs from the initial value in this switching cycle, denoting that the DCM phase fails to discharge energy stored in the inductor and violates the inductor voltage-second balance.

In Fig. 2-7, it is represented that the current reference in phase C (CRM phase) is much smaller than the current reference in phase A (DCM phase). This happens because of the unbalanced ac current reference with the non-symmetrical operation mode as mentioned in Fig. 2-5. The small current reference in the CRM phase renders the phase's switching period too short. On the other hand, it takes longer for the DCM phase inductor current to reach zero with the bigger current reference.

Consequently, the CRM phase switching period finishes early, forcing the DCM phase active switch turn-on before the inductor current crosses zero.

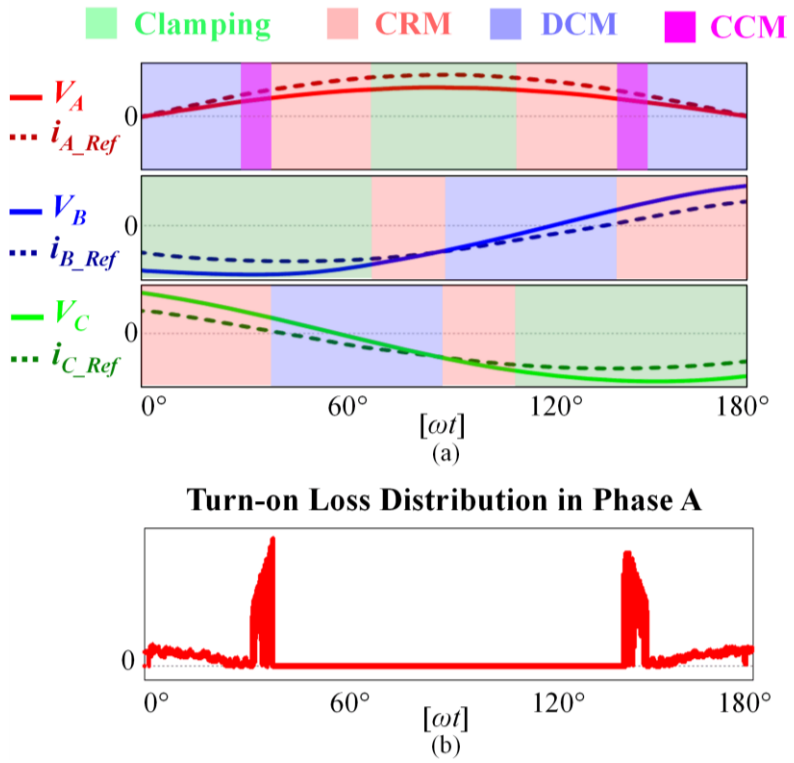


Fig. 2-8. Influence of Case I voltage sag: (a) operation mode and (b) turn-on loss distribution.

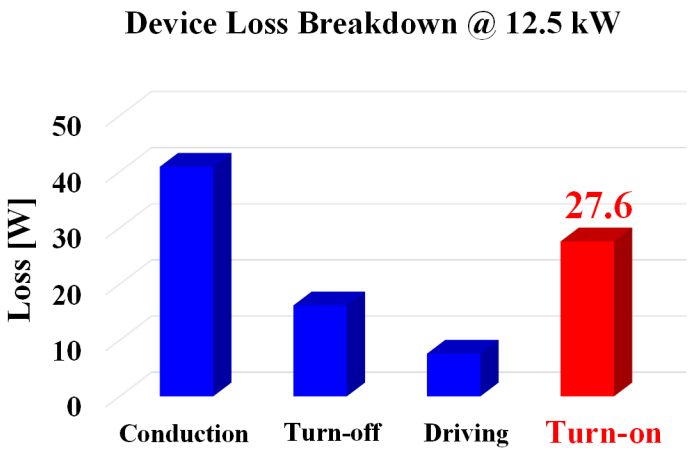


Fig. 2-9. Device loss breakdown for Case I voltage sag.

The problematic phenomenon (CCM) only comes out where DCM is expected as represented in Fig. 2-8(a). When phase A voltage decreases, the CCM operation is observed solely in phase A marked as purple zones. As stated, the ac current reference is much higher in the DCM phase. As a result of the hard-switching by CCM, the turn-on loss is mostly focused in the CCM area as depicted in Fig. 2-8(b). It gives rise to a considerable rise in phase A turn-on loss, as exhibited in Fig. 2-9, especially owing to very high switching frequency of the inverter. Moreover, there exists a chance for noise issues caused by the hard-switching, particularly for SiC power devices [40], [41]. High dv/dt at the switching node of each phase leg is spread out to the gate driver's primary side. This could trigger an unwanted false turn-on of the switches and lead to detrimental shoot-through. This critically threatens the inverter reliability, thus the hard-switching must be shunned.

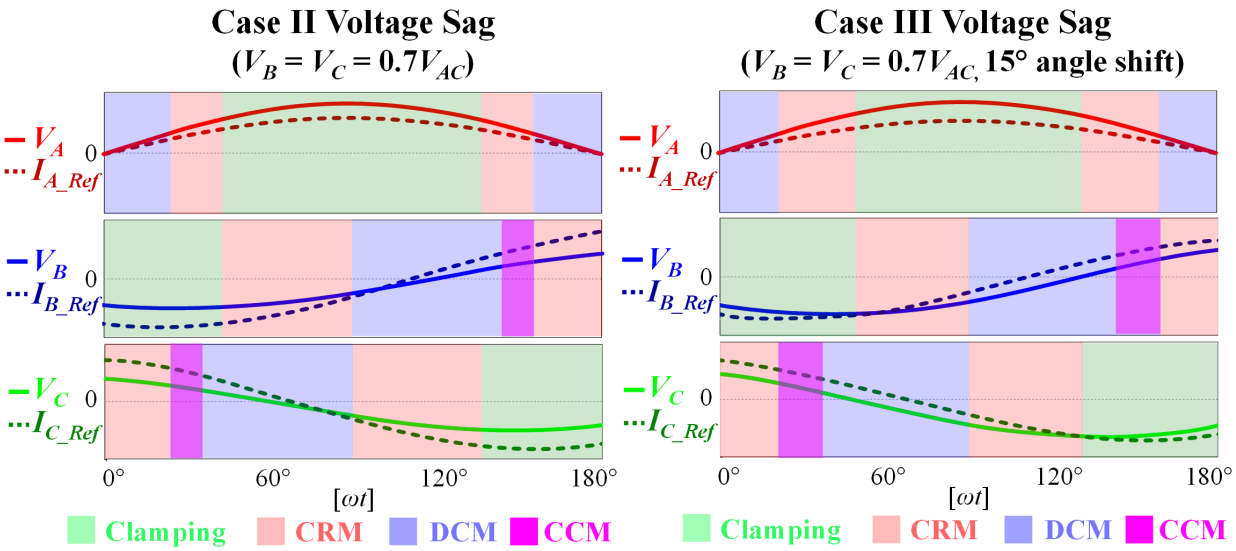


Fig. 2-10. Influence of different voltage sags on operation mode.

The same issue about CCM is present in other kinds of grid imbalances. Fig 2-10 shows the operation mode of the soft-switching inverter under Case II voltage sag (voltage drop in both phase B and phase C), and Case III voltage sag (voltage drop in both phase B and phase + 15 degrees shift),

and where the CCM operation arises for each case. As elaborated, the operation mode becomes asymmetrical due to the imbalance and the unbalanced ac current needs to be injected for constant active power delivery. One obtrusive thing is that Case III voltage sag suffers from CCM most among the three cases assuming that the voltage drop is identical, since the extent of abnormality is the most serious with the angle shift. It can be deduced that there is more adversity related to the CCM issue as the voltage decreases and angle shift gets severe.

2.3 Improved CRM-Based Soft-Switching Technique for Grid Imbalance

Two control techniques are proposed to improve the CRM-based soft-switching modulation to resolve the CCM problem. The key feature of these control methods is to avoid the violation of the inductor voltage-second balance by letting the inductor current in the DCM phase to reach zero. This can be realized by manipulating switching actions of either the CRM phase or the DCM phase.

2.3.1 Off-Time Extension in CRM Phase

The first approach (Approach 1) proposed in [42] is represented in Fig. 2-11. For the sake of brevity, the resonant period by the switches' output capacitance and the inductors are neglected. In Fig. 2-11, i_{LC}, crosses zero first at t_0, just like what is shown in Fig. 2-7. At this moment, i_{LA}, has not yet touched zero. Then, additional conduction time for the synchronous rectifier (SR), V_{GS_C}' is given in the CRM phase and lasts until i_{LA} crosses zero. Since the active switch's off-time is elongated, this is called "off-time extension". When i_{LA} hits zero at t_1, the SR is turned off. The active switches in both CRM and DCM phases are turned on at this time. In the next switching period, during the t_2 - t_3 time interval, the off-time extension is carried out again. In consequence, the inductor in the DCM phase is now able to fully release the stored energy, and obey voltage-second

balance. It needs to be pointed out that "off-time extension" is normally utilized either to store additional energy in an inductor for ZVS [22], or to make the resonant time shorter to alleviate CM noise sources [43], [44]. On the other hand, it is employed to evade the inductor voltage-second balance violation in this control method, resulting in the removal of the CCM issue.

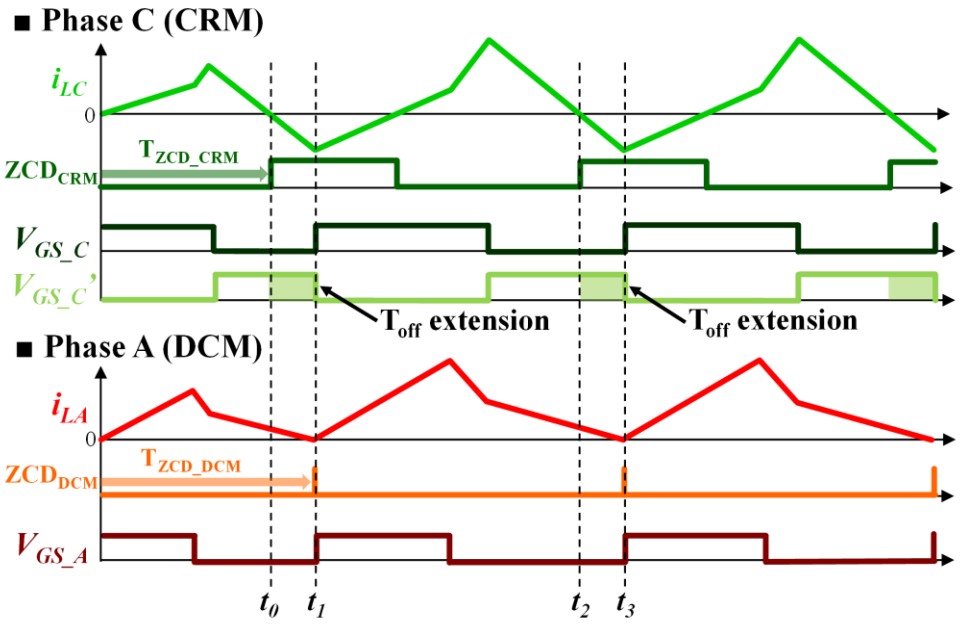


Fig. 2-11. Approach I: Off-time extension in CRM phase.

Implementation of Approach I in digital control is easily done by watching the CRM phase and DCM phase ZCD signals, ZCD_{CRM} and ZCD_{DCM}. eCAP modules in a microcontroller (MCU) can separately capture T_{ZCD_DCM} and T_{ZCD_CRM} which are the time required for the DCM phase and CRM phase to reach zero current. The demanded off-time for the CRM phase active switch is yielded by subtracting T_{ZCD_CRM} from T_{ZCD_DCM}. This approach is analyzed and verified in [42], so that it soothes the appearance of CCM and significantly lowers the switching loss. One drawback of this method is that the extended off-time is renewed based on MCU's update time or interrupt time, normally at a few switching cycles and not every switching cycle, as the inverter switching period is much shorter than

the available update time in the MCU. Because of this, although CCM can be thoroughly eliminated theoretically, there remains a chance for the CCM operation to appear.

2.3.2 Pulse Skipping in DCM Phase

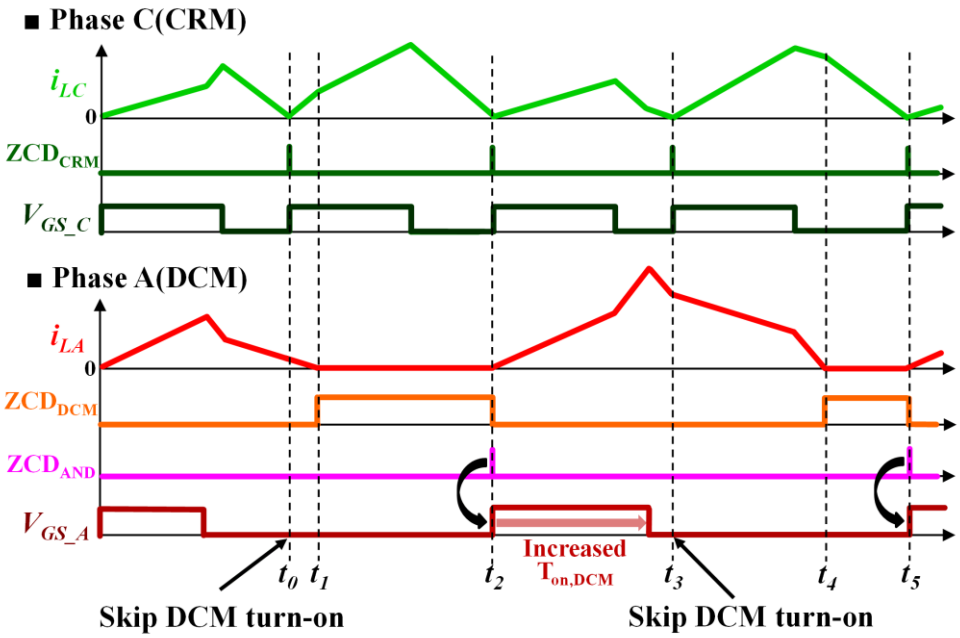


Fig. 2-12. Approach II: Pulse skipping in DCM phase.

Fig. 2-12 shows the second approach proposed in [45]. The switches' output capacitance is also omitted, and LC resonance is ignored as well. In Fig. 2-12, i_{LC} first hits zero at t_0 just like what is shown in Fig. 2-7 and Fig. 2-11. At that time, i_{LA} has not touched zero. In Approach II, instead of manipulating the CRM phase switch, one switching action in the DCM phase is intentionally skipped to enable the DCM phase inductor current to cross zero. But the CRM phase works as usual, turning on the active switch according to ZCD_{CRM} signal. Then i_{LA} continues to decrease and finally becomes zero at t_1. At t_2, a new switching cycle starts for the CRM phase because i_{LC} becomes zero again. Now that the DCM phase current is zero, the DCM phase turn-on is synchronized with

the CRM phase turn-on. One thing to note is that the DCM phase on-time is adjusted by a current controller, and is slightly increased after one switching period is skipped to compensate for the skip. In this manner, the DCM phase inductor current is able to touch zero all the time, and the CCM operation disappears.

The pulse skipping can be simply realized by mixing analog circuits and the digital control. First an AND logic gate is needed to generate ZCD_{AND} signal from ZCD_{DCM} and ZCD_{CRM}. Then the ZCD_{CRM} signal triggers the CRM phase and ZCD_{AND} signal triggers the DCM phase. The upside of this approach is its instantaneous execution by the help of the additional analog circuit, opposite to the first approach. Though the nature of the approaches is identical, Approach II resolves the CCM issue better and is more practical in the digital control. Thus, Approach II is focused more in the ensuing discussion within this chapter.

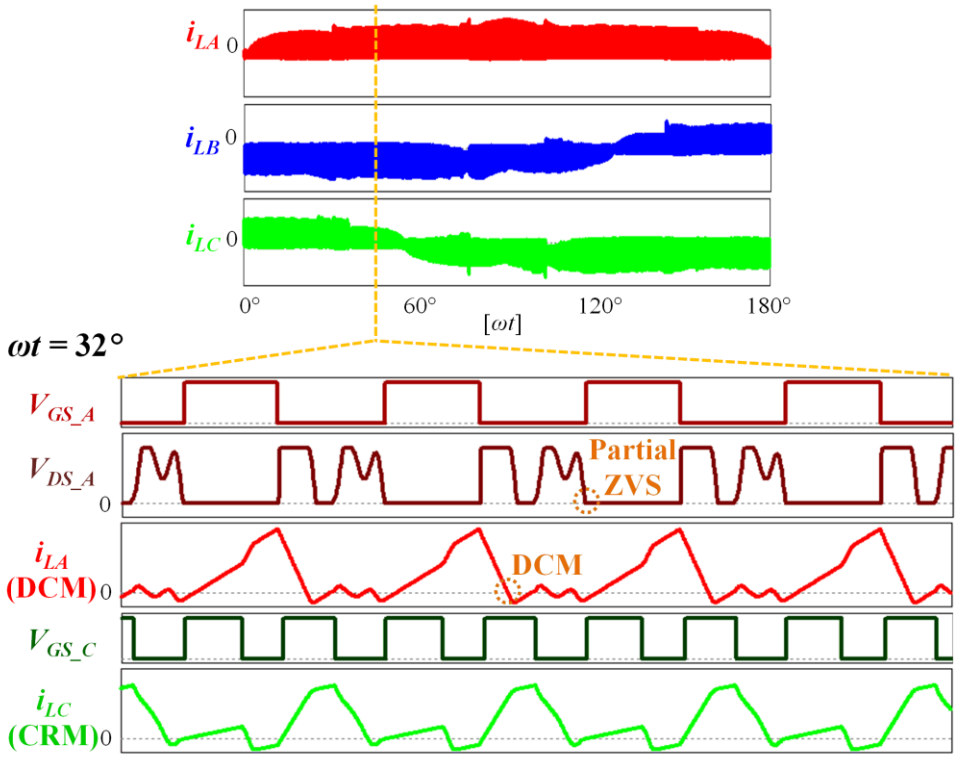


Fig. 2-13. DCM pulse skipping method under Case I voltage sag.

The proposed control method is applied to the previously described Case I voltage sag, and the simulation results are represented in Fig. 2-13. On the top, half line cycle inductor currents are shown. At the bottom, phase A active switch's gate-to-source and drain-to-source voltages, and the inductor current, as well as those for phase C are shown. At 32°, at which previously the CCM issue would exist, the pulse skipping is conducted in phase A and, thereafter, the phase A inductor current is able to reach zero. It is witnessed that the hard-switching turn-on is removed. Additionally, ZVS or partial ZVS is achieved in the DCM phase. This reduces the switching loss substantially. The in-depth analysis of the partial ZVS will be covered in the next section.

Fig. 2-14 makes comparisons between one with and one without the DCM pulse skipping. Turn-on loss distribution in phase A is plotted, and the corresponding device loss breakdown is shown. In Fig. 2-14 (a), the extreme concentration of turn-on loss in phase A by the hard switching, marked as the gray line, is nearly gone when the pulse skipping method is carried out, marked as the red line. The improved control slightly reduces driving loss because of the half or one-third switching frequency by the skipped pulses. But the increased rms and peak inductor current in the DCM phases leads to larger turn-off and conduction losses. Nonetheless, the total device loss given in fig. 2-14(b) is reduced remarkably as the saved turn-on loss outweighs the increased losses.

Fig. 2-15 makes the same comparisons for Case II voltage sag and Case III voltage sag. The extent of the voltage sag is described in the figures. Overall, the effectiveness of the improved control is similar. It is most effective and shows the most dramatic improvement for Case III voltage sag. The hard-switching in this case is the most prominent and widely spread out along the line cycle because of the severe imbalance, as shown in Fig. 2-10. Consequently, it can be concluded that the proposed pulse skipping method is efficacious to any type of abnormal grid. In other words, it is a generalized solution for unbalanced grid conditions.

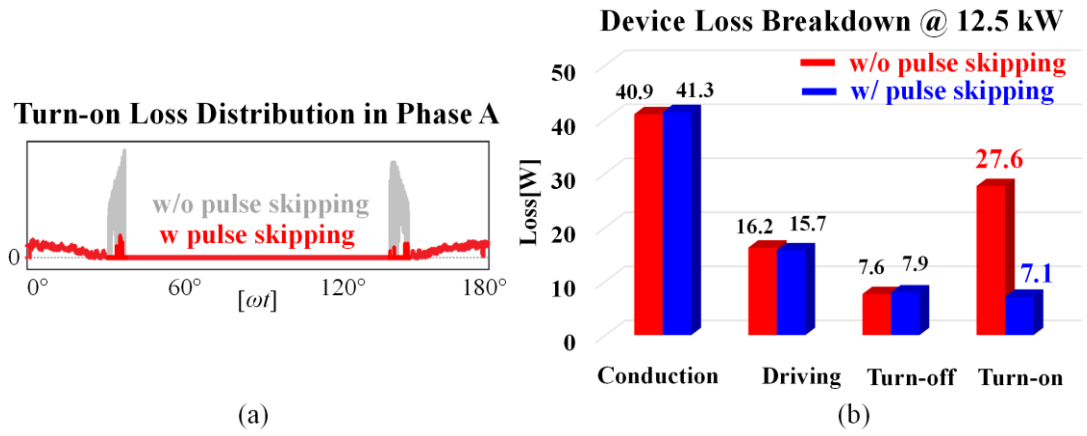


Fig. 2-14. Phase A turn-on loss distribution and device loss breakdown comparison for Case I voltage sag.

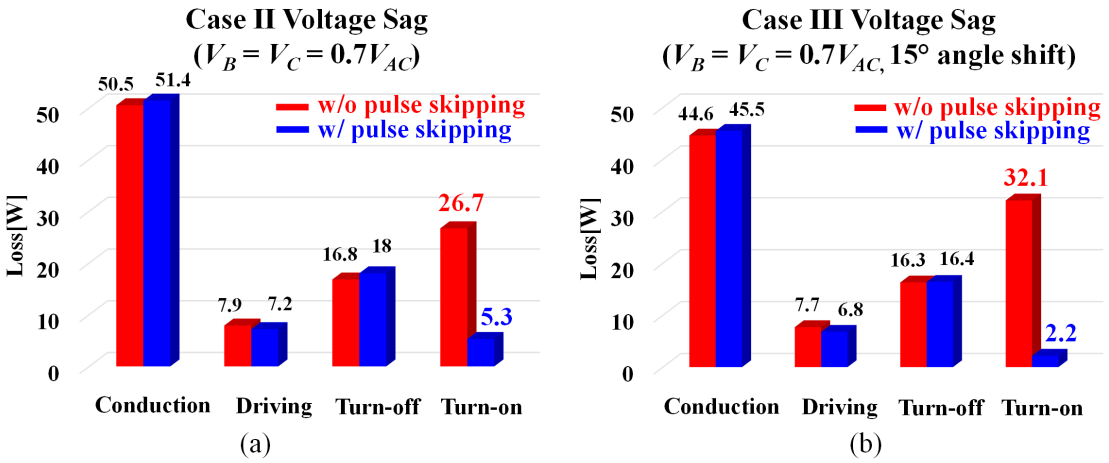


Fig. 2-15. Device loss breakdown comparison: (a) Case II voltage sag and (b) Case III voltage sag.

2.3.3 Partial ZVS in DCM Phase with Pulse Skipping

As mentioned in the previous section, pulse skipping can accomplish the partial ZVS for the switches in the DCM phase. Detailed analysis of the mechanism is presented in Fig. 2-16. Fig. 2-16(a) features the zoomed-in waveforms of Fig. 2-13. This highlights the region in which phase B is in clamping mode, phase A works as DCM, and phase C works at CRM. In particular, three time

intervals from t_0 to t_3 are emphasized. Accordingly, the state-plane trajectory of phase A during the intervals is drawn in 2-16(b). i_{LA} is the phase A inductor current, V_{DS_A} is phase A active switch's drain-to-source voltage, and Z_n is the inverter's characteristic impedance. L is the inverter inductor and C_{oss} is the switch's output capacitor, assuming that all three phase inductors and output capacitors are exactly the same. The equivalent circuits during the time intervals are shown in Fig. 2-17. For conciseness, the input capacitor and the EMI filter of the inverter are left out.

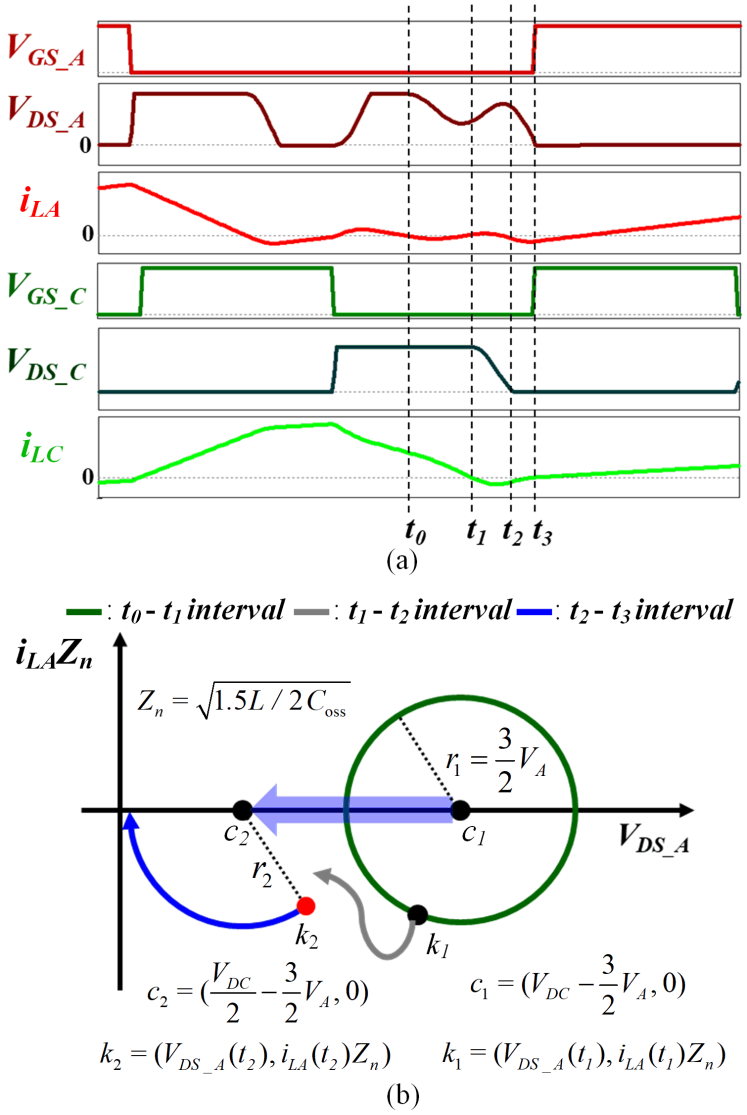


Fig. 2-16. Partial ZVS mechanism in DCM phase: (a) switching cycle waveforms and (b) phase A state-plane trajectory.

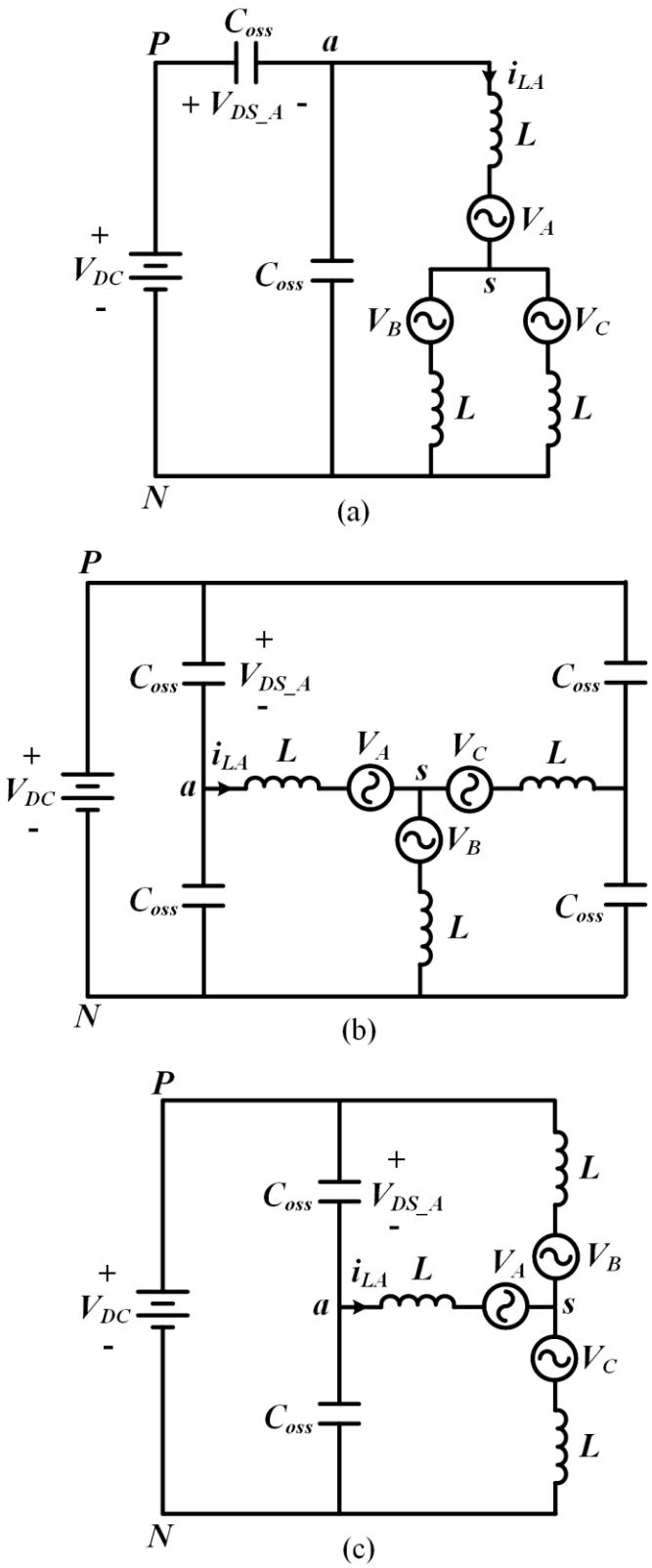


Fig. 2-17. Equivalent circuits during (a) t_0-t_1 interval (b) t_1-t_2 interval (c) t_2-t_3 interval.

Stage I [t_0-t_1 interval]: Phase A's top switch and bottom switch are in off-status because i_{LA} has already reached zero before t_0. On the other hand, the bottom switches in phase B and phase C are in on-status because phase B is clamped to *N* node and the phase C inductor current is being discharged. During this interval, phase A's top and bottom switches output capacitors and all phase inductors participate in LC resonance. Then a 2nd order LC resonant circuit is formed, as depicted in Fig. 2-17(a). The initial value of V_{DS_A} is V_{DC}, and the initial value of i_{LA} is zero, respectively. According to Kirchhoff's Current Law (KCL) at the node *a*, the following equation is yielded:

$$\frac{V_{DC}-V_{DS\_A}(s)-V_A-V_{sN}(s)}{sL}=\frac{V_{DS\_A}(s)}{1/sC_{oss}}-\frac{V_{DC}-V_{DS\_A}(s)}{1/sC_{oss}} \tag{2-6a}$$

wherein V_{sN} is the zero-sequence or common-mode voltage. During this interval, expressed as

$$V_{sN}(s)=\frac{V_{DC}-V_{DS\_A}(s)}{3} \tag{2-6b}$$

solving (2-6a) and (2-6b) with the given initial values acquires V_{DS_A} and i_{LA} as follows:

$$V_{DS\_A}(t)=\frac{3}{2}V_A\cos\omega_0 t+V_{DC}-\frac{3}{2}V_A \tag{2-7a}$$

$$i_{LA}(t)=-\frac{3}{2}\frac{V_A}{Z_n}\sin\omega_0 t\,. \tag{2-7b}$$

The resonant frequency of the inverter is $\omega_0=\sqrt{3LC_{oss}}$. Then, the state-plane trajectory expression is obtained by summing (2-7a) and (2-7b) after powering both sides of the equations, which is

$$(Z_n i_{LA})^2+(V_{DS\_A}-V_{DC}+\frac{3}{2}V_A)^2=(\frac{3}{2}V_A)^2\,. \tag{2-8}$$

In Fig. 2-16(b), the green line represents the corresponding state-plane trajectory during this interval where c_1 and r_1 mean the trajectory's center and radius, respectively. This stage lasts until i_{LC} hits zero at t_1. It should be mentioned that t_1 varies depending on the operation conditions of the inverter (e.g., input voltage, output voltage, power level, and the extent of voltage sag). This makes it difficult to predict or calculate the variables' value at the end of Stage I (the Stage II initial value), k_1, even though the values are definitely on the green trajectory.

Stage II [interval t_1-t_2]: At t_1, i_{LC} is zero and the phase C bottom switch is turned off. After that, phase C switches' output capacitors join the LC resonance. The order of LC resonance increases by two and a 4th order resonant circuit is built as depicted in Fig. 2-17(b). Even though phase A and phase C variables' initial values are required to solve the 4th order differential equation for the LC resonance, as stated, phase A variables' initial values are unknown. Therefore, during this interval, it is not feasible to anticipate the exact trajectory depicted as the gray line in Fig. 2-16(b). This stage ends when phase C active switch drain-to-source, V_{DS_C}, reaches zero. To say nothing of that, the last values of the phase A in Stage II, k_2, are vague.

Stage III [interval t_2-t_3]: Once V_{DS_C} reaches zero, the phase C active switch is turned on. Then, the order of LC resonance decreases by two turning the 4th order LC resonant circuit back to the 2nd order as illustrated in in Fig. 2-17(c). By doing KCL at node *a* to solve the resonant circuit, the following equations are obtained:

$$\frac{V_{DC}-V_{DS\_A}(s)-V_A-V_{sN}(s)}{sL}=\frac{V_{DS\_A}(s)}{1/sC_{oss}}-\frac{V_{DC}-V_{DS\_A}(s)}{1/sC_{oss}} \tag{2-9a}$$

$$V_{sN}(s)=\frac{2V_{DC}-V_{DS\_A}(s)}{3}. \tag{2-9b}$$

The corresponding state-plane trajectory of Stage III is shown as the blue line in Fig. 2-16(b). The expression for this stage is given by

$$(Z_n i_{LA})^2 + (V_{DS\_A} - \frac{V_{DC}}{2} + \frac{3}{2}V_A)^2 = (r_2)^2 . \tag{2-10}$$

Here, r_2 is the trajectory's radius and is a function of c_2, the trajectory's center, and the initial values of phase A and phase C variables in Stage III, k_2. Now that k_2 is unknown, it is not ensured that the DCM phase will accomplish ZVS. Despite this, the center of the trajectory moves closer to the origin compared to Stage I, from c_1 to c_2. There is a higher possibility for the DCM phase to achieve ZVS as phase A voltage increases because the center moves closer to the origin. Eventually, the DCM phase can partially achieve ZVS.

2.4 Experimental Results

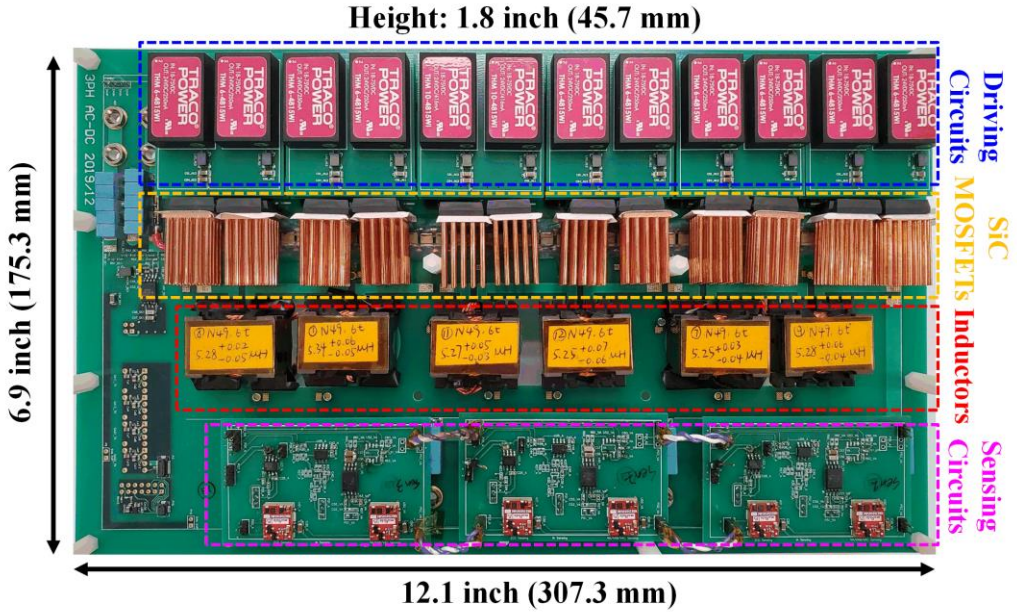


Fig. 2-18. SiC-based soft-switching three-phase inverter prototype.

TABLE 1 THE PROTOTYPE SPECIFICATION

Description	Value
Output Power (P_o)	12.5 kW
Input DC Voltage (V_{DC})	800 V
Output AC Voltage (V_{AC})	277/480 Vrms at 60 Hz
Unbalance Grid Condition	Case I Voltage Sag (30 % drop at phase A)
-	Case II Voltage Sag (30 % drop at phase B & C)
-	Case III Voltage Sag (30 % drop + 15° angle shift at phase B & C)
Output Inductor (L)	3.5 µH
SiC MOSFETs	C3M0021120K
Minimum Switching Frequency (F_{S_Min})	300 kHz

The proposed control strategy is digitally implemented on an SiC-based three-phase inverter, as shown in Fig. 2-18, to evaluate its performance. The prototype consists of the gate drivers (blue box), the SiC power devices (yellow box), the output inductors (red box), and the sensing circuits (pink box). The MCU is placed outside of the prototype and is connected to it externally. It is responsible for the current control and PWM generation for the soft-switching. The PWM signals are transmitted to the inverter prototype via fiber optic cables for noise immunity. It is worth mentioning that originally the prototype was developed for a 25 kW two-channel interleaved bidirectional three-phase ac-dc converter, yet only one channel is operated (12.5 kW) to validate the proposed control. The prototype specification is presented in TABLE 1.

For the current control under unbalanced grid conditions, the current reference generation becomes a bit more complicated compared to that under normal grid conditions. Fig. 2-19 exhibits

how to obtain the ac current reference for the constant active power delivery. First, the instantaneous ac voltage is sensed. Second, it is transformed into αβ-frame (the stationary reference frame). The ac voltage in αβ-frame is decomposed into the positive and negative sequence elements via a calculation block. This ac voltage decomposition block uses the double second-order generalized integrator discussed in [46]. After extracting the positive and negative elements, the ac current reference in αβ-frame is calculated according to the output power for the PNSC method [35]. Based on (2-5), the current reference generation equations are expressed as

$$I_{\alpha\_Ref} = \frac{P_o}{\left|\mathbf{v}^+\right|^2 - \left|\mathbf{v}^-\right|^2}(V_\alpha^+ - V_\alpha^-) \tag{2-11a}$$

$$I_{\beta\_Ref} = \frac{P_o}{\left|\mathbf{v}^+\right|^2 - \left|\mathbf{v}^-\right|^2}(V_\beta^+ - V_\beta^-). \tag{2-11b}$$

Then the ac current reference in αβ-frame is either directly used for current control if the controller is designed in αβ-frame, or transformed back to abc-frame if the controller is designed in abc-frame.

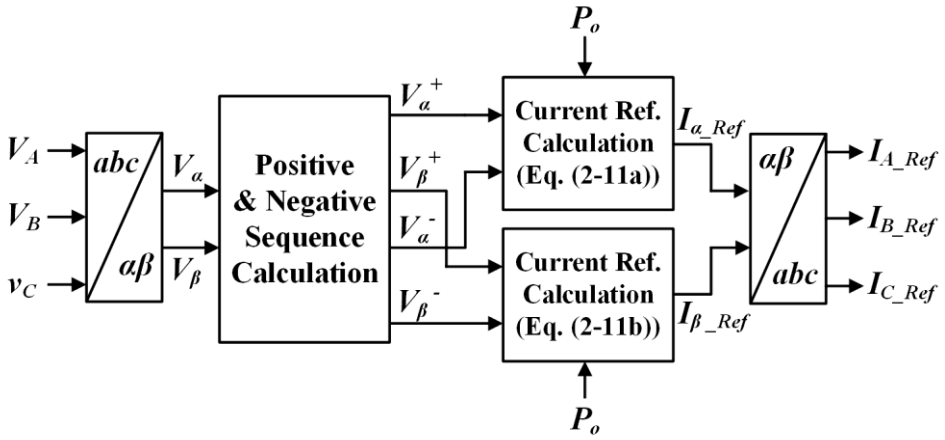


Fig. 2-19. Unbalanced ac current reference generation block.

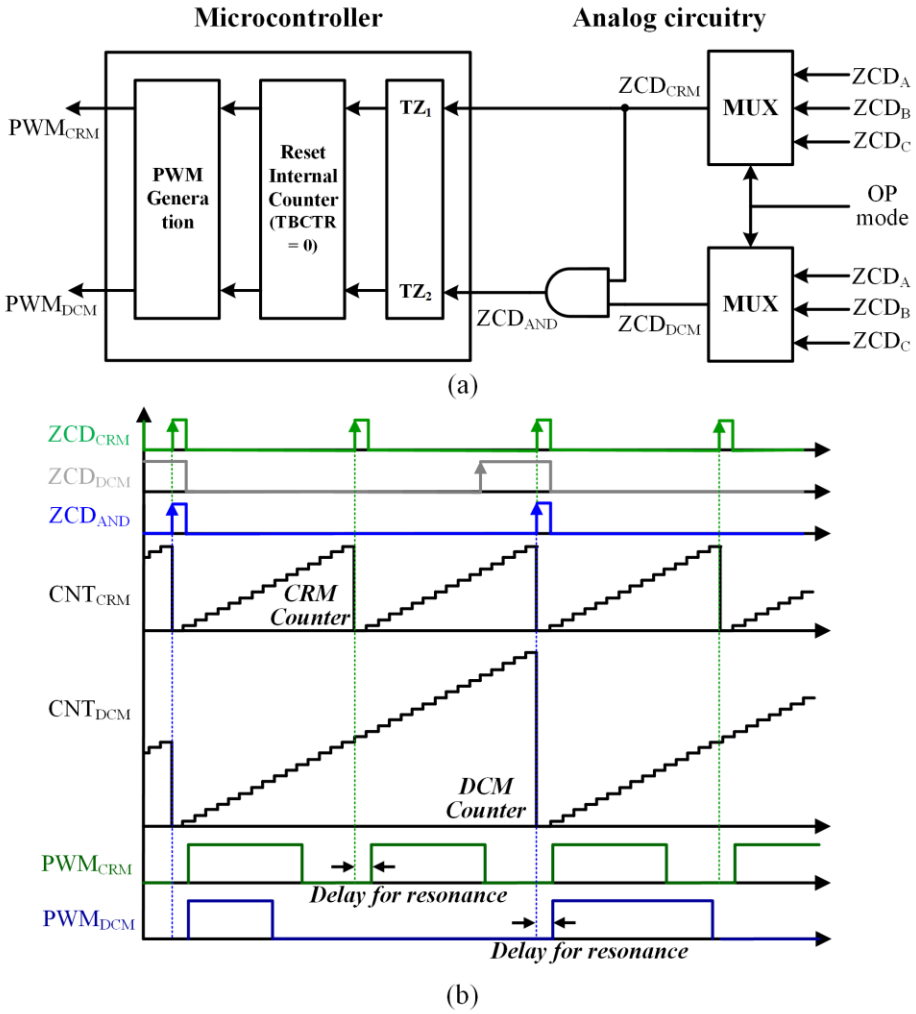


Fig. 2-20. Pulse skipping control implementation. (a) Overall structure. (b) Execution of the DCM pulse skipping in microcontroller.

As for the key element of the proposed control, DCM phase pulse skipping, Fig. 2-20(a) shows how it is realized. It requires simple analog circuits and several digital signals from the MCU. The operation mode indicator (OP mode), which includes the information on which phase operates at CRM or DCM, is sent to the multiplexers to distinguish ZCD signals for the CRM phase, ZCD_{CRM}, and the DCM phase, ZCD_{DCM}. An AND logic gate outputs ZCD_{AND} by monitoring ZCD_{CRM} and ZCD_{DCM}. After that, ZCD_{CRM} and ZCD_{AND} are fed to the trip-zone (TZ) ports in the MCU

(ZCD_{CRM} to TZ1, ZCD_{AND} to TZ2). These signals play a pivotal role for the soft-switching and reset MCU's internal time-based counter (CNT). As illustrated in Fig. 2-20(b), once ZCD_{CRM} sets high, the CRM phase internal counter, CNT_{CRM}, is reset to be zero. Similarly, once ZCD_{AND} sets high, the DCM phase internal counter, CNT_{DCM}, is reset to be zero. This is the difference between the original soft-switching method and the proposed control method. In the original method, ZCD_{CRM} resets both CNT_{CRM} and CNT_{DCM} for the frequency synchronization, but in the improved control with the DCM pulse skipping, CNT_{DCM} is not reset by ZCD_{CRM}, but by ZCD_{AND} taking the status of both CRM and DCM phases' ZCD signals into account. The way to trigger the DCM phase turn-on makes the inverter's operating principle under normal grid conditions unchanged because ZCD_{CRM} and ZCD_{AND} sets high at the same time in such a case. Basically, the pulse skipping is carried out only during the grid imbalances.

By the way, it must be mentioned that the ZCD circuits for the three phases (ZCD_A, ZCD_B, and ZCD_C) in Fig. 2-20 must be designed in a very robust manner, as all the techniques explained by far utterly count on the reliability of the ZCD signals. The ZCD circuit is built on the basis of the circuit proposed in [47] except for Zener diodes at the comparator input. A 25mΩ shunt resistor (ten of 250 mΩ in parallel) is placed in series with the inductor. The voltage potential between two nodes of the resistor is fed to a comparator with a hysteresis function (ADCMP601). The comparator judges the inductor current's polarity. The output of the comparator is sent to a digital isolator (AduM1100) for noise immunity and isolation between the signal sensing circuit and the power stage. Finally, this information is used in the MCU.

When it comes to the delay for resonance shown in Fig. 2-20, after the inductor current touches zero, several delays in the circuit need to be considered. First, the ZCD circuit itself has a delay which is measured to be about 100 ns. Then, for the MCU to recognize the ZCD signal, it takes 15

ns (3 system clock in the MCU). In total, the inductor zero current to the internal counter reset has a 115 ns delay. Basically, by the time the MCU is aware of the ZCD signal, the LC resonance has already started. Therefore, the PWM signal generation must be selected based on the delay. For example, if the time required for ZVS after the inductor current touches zero is 200 ns, the required minimum delay until the PWM signal generation is 85 ns. But there is also a delay between the PWM signal and the gate signal which is measured to be 110 ns. Once the LC resonance finishes, the body diode of the active switch is conducted with a negative inductor current. If the time for the body diode conduction is 200 ns, the PWM signal sets high within 90 ns after the end of the LC resonance so that the active switch is turned on before the inductor goes back to zero. Consequently, the PWM signal should be generated between 85 ns and 175 ns after the ZCD high is recognized by the MCU.

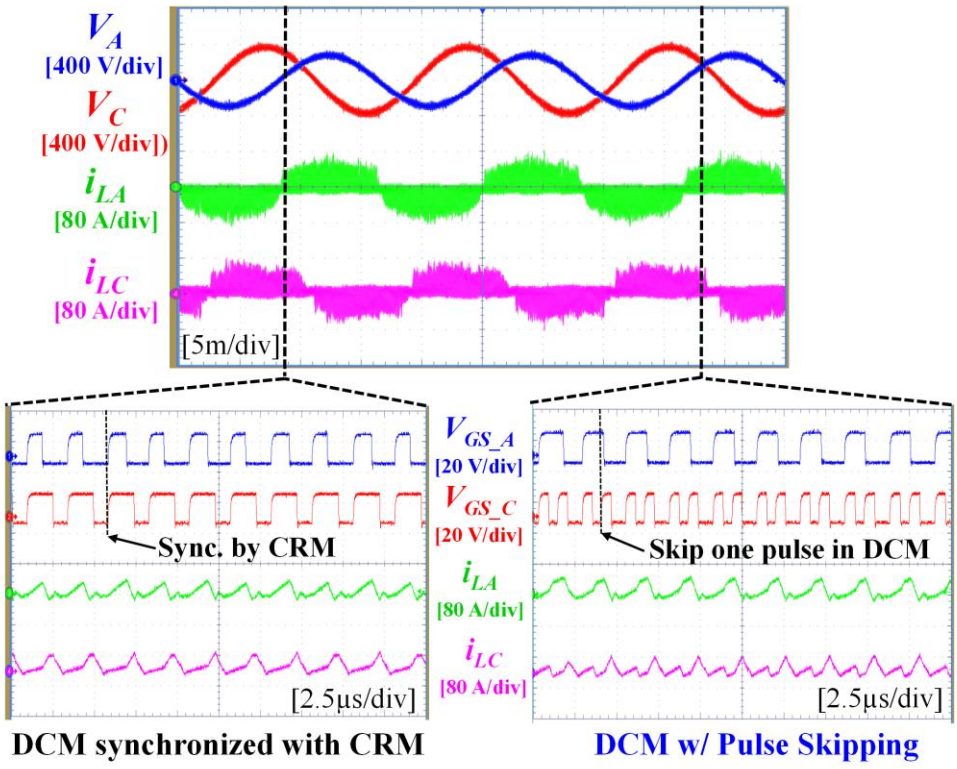


Fig. 2-21. Experimental waveforms of the proposed control method under Case I voltage sag.

Fig. 2-21 shows the experimental results of the proposed DCM pulse skipping under Case I voltage sag. To imitate the ac grid, the California Instruments' MX45 ac power source is utilized. It features a regenerative mode, which can absorb power from the inverter and behave like the ac grid. In addition, it is capable of emulating unbalanced grid voltages, such as voltage decrease as well as angle shift between each phase. Regarding the experimental waveforms at the bottom left, when the inductor current in the DCM phase reaches zero before the inductor current in CRM phase crosses zero, the DCM phase turn-on is aligned with that in the CRM phase. Conversely, at bottom right, the DCM pulse skipping is executed. Due to the skipped pulses, the DCM phase's switching period is twice that of the CRM phase. It should be noted that multiple pulses can be skipped contingent on how bad the ac voltage's abnormality is.

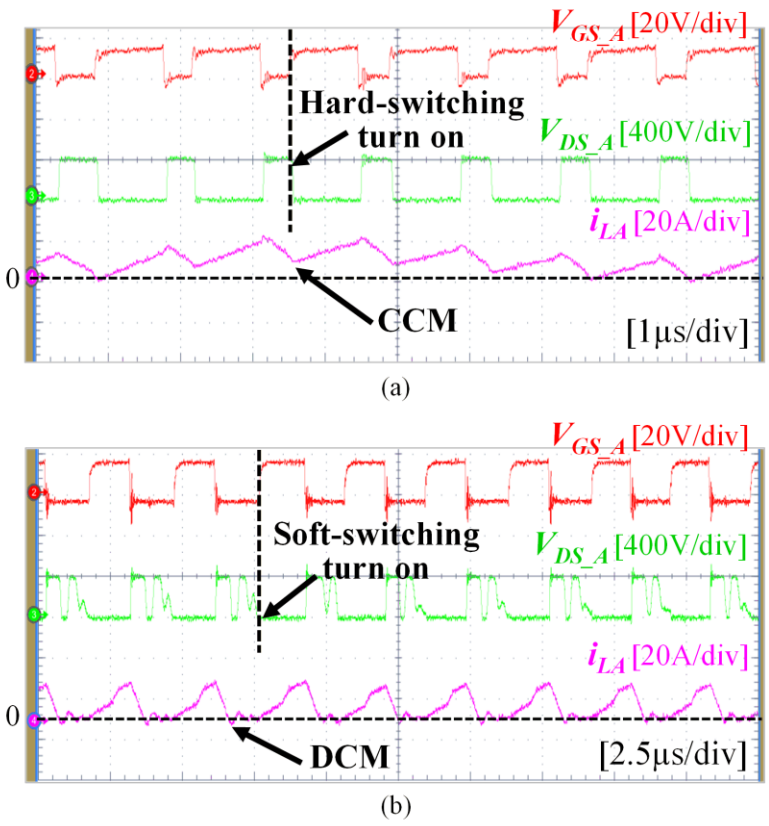


Fig. 2-22. Comparison between original and improved controls at switching cycle: (a) original control without DCM pulse skipping and (b) improved control with DCM pulse skipping

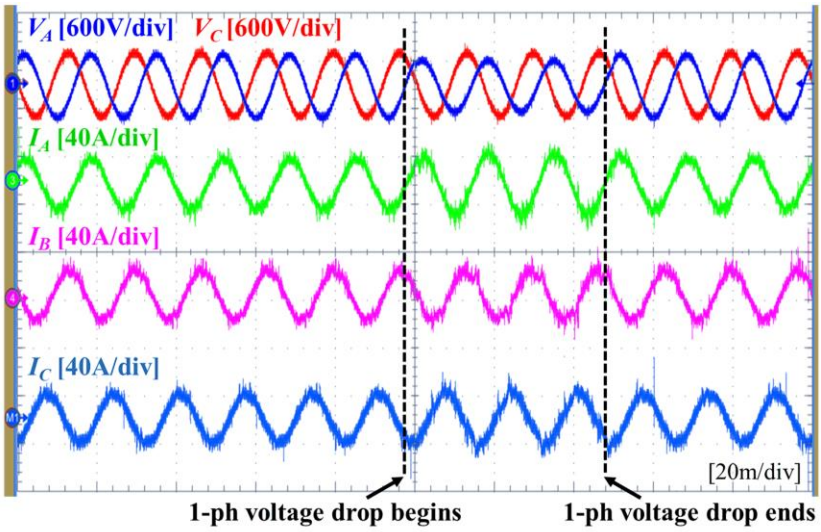


Fig. 2-23. Grid transient from normal to Case I voltage sag and vice versa.

A comparison for the switching behaviors between the original control and the improved control schemes is made in Fig. 2-22. The hard-switching by the CCM operation is observed in the DCM phase (phase A) in Fig. 2-22(a). The inductor current in the DCM phase, phase A, does not touch zero. On the contrary, the DCM pulse skipping control eliminates the hard-switching and guarantee that the DCM phase inductor current reaches zero. Moreover, it achieves soft-switching as shown in Fig. 2-22(b). As expected, it is seen that ZVS is not always achieved, but partial ZVS can be achieved.

With the proposed control method, the grid transient is tested and the result is given in Fig. 2-23. In this experiment, the ac voltage is manipulated to vary from the normal grid to the Case I voltage sag and back to the normal grid. Right after V_A decreases, the ac current becomes unbalanced. Particularly, it is clear that the phase A current is larger than the other phase currents. When the grid recovers, the ac current becomes balanced again. The experimental result shows that the transition from the normal grid to the voltage sag and vice versa is very smooth. It turns out that the inverter with the proposed control can deal with FRT with soft-switching capability.

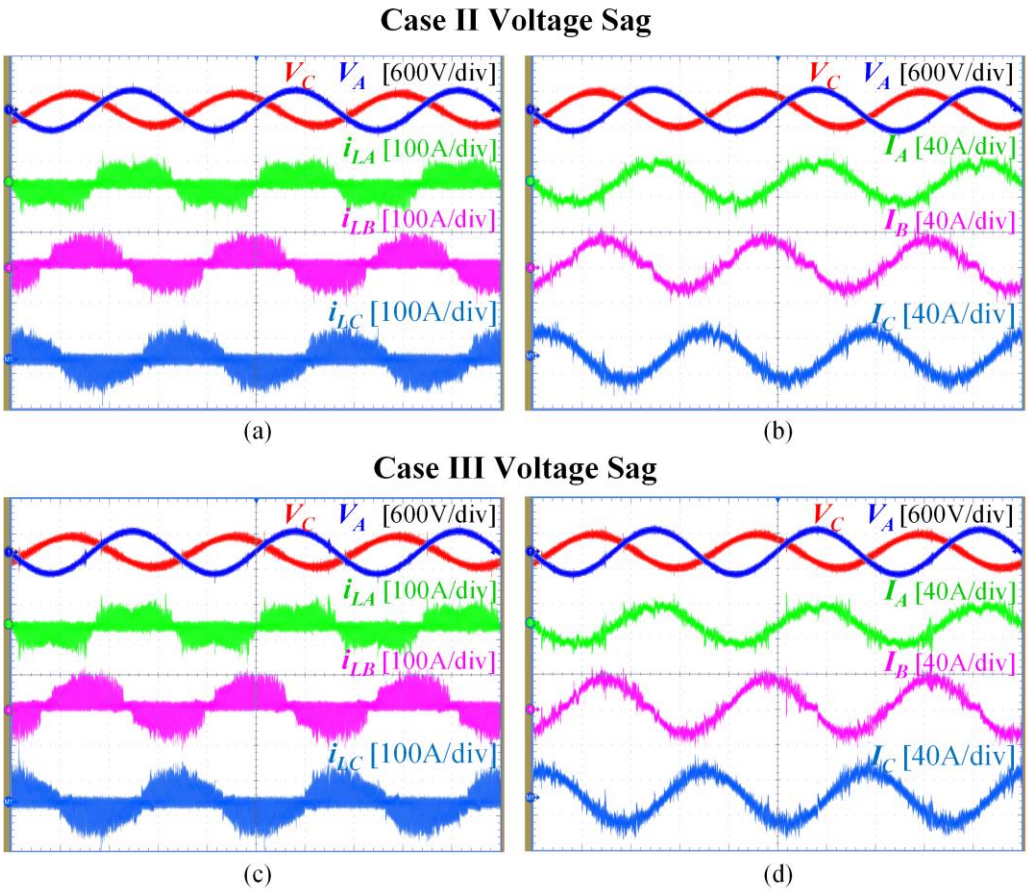


Fig. 2-24. Case II voltage sag and Case III voltage sag with the proposed DCM pulse skipping.

Experimental results in Fig. 2-24 show the line cycle waveforms of the soft-switching inverter under different types of voltage sag. Fig. 2-24(a) and Fig. 2-24(b) are for Case II voltage sag; 30% of phase B and phase C is dropped. Fig 2-24(c) and Fig. 2-24(d) are for Case III voltage sag; 30% of phase B and phase C is dropped, as well as 15° angle shifted. With the DCM pulse skipping control, the inductor current and the output ac current are well controlled. It is proven from all the results above that this control method can be a generalized solution for all kinds of unbalanced grid conditions.

Measured efficiencies at various load conditions under the Case I, Case II, and Case III voltage sag are shown in Fig. 2-25, Fig. 2-26, and Fig. 2-27. The extent of the voltage sags in these figures is as

stated in TABLE 1. The proposed control method improves the inverter efficiency from 0.2 % to 1.1 % in Case I, 0.1 % to 0.9% in Case II, and 0.3 % to 1.1 % in Case III. To be specific, as the inverter output power is smaller, the efficiency improvement is higher. This is because the switching frequency becomes higher at lighter loads, due to its CRM-based operation, suffering more from the higher turn-on loss by CCM. Consequentially, the improvement of inverter efficiency is more dramatic at lighter loads.

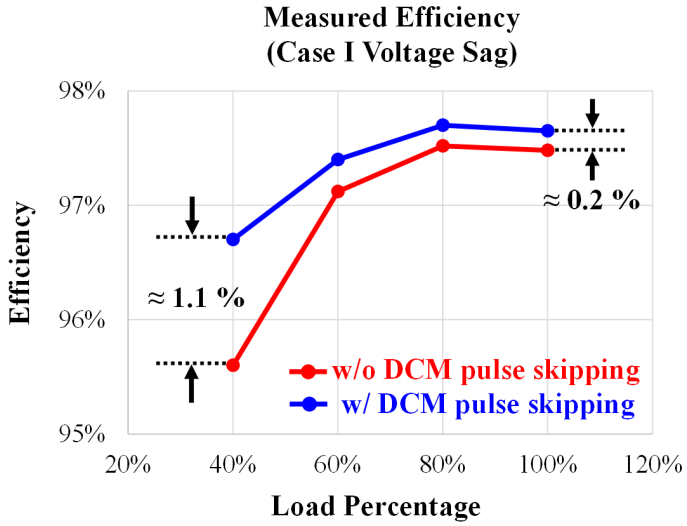


Fig. 2-25. Measured efficiency at various load conditions under Case I voltage sag.

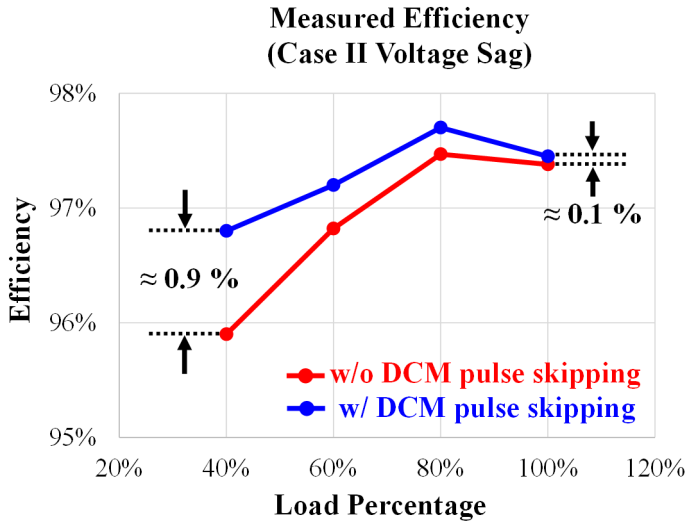


Fig. 2-26. Measured efficiency at various load conditions under Case II voltage sag.

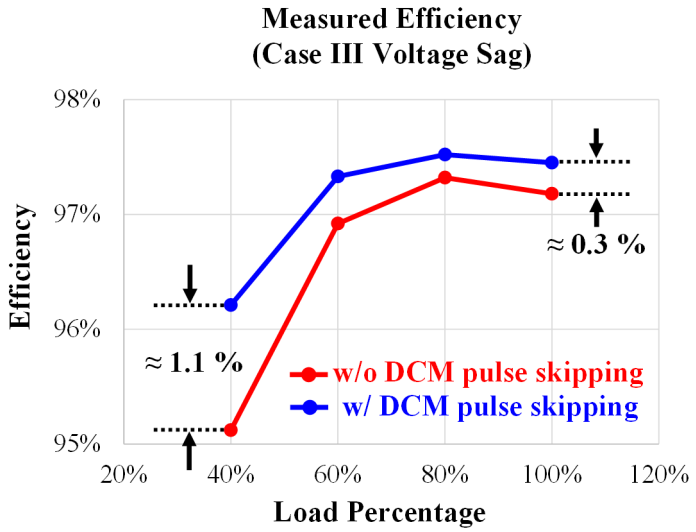


Fig. 2-27. Measured efficiency at various load conditions under Case III voltage sag.

2.5 Conclusions

In this chapter, control techniques for the CRM-based high-frequency soft-switching three-phase inverter at grid imbalances are studied. An unbalanced ac current needs to be injected to deliver constant active power when the grid stays unbalanced. This causes the unexpected hard-switching by CCM operation in the soft-switching inverter. Control methods to allow the DCM phase inductor current to cross zero are proposed to eliminate the hard-switching, called "CRM off-time extension" and "DCM pulse skipping". Especially, the pulse skipping control is analyzed and evaluated carefully. It fulfills partial ZVS, resulting in a huge reduction in the turn-on loss, and lessens the chance of the noise issue. The proposed control is applied to the representative cases of voltage sags and it is validated that the control method improves inverter efficiency at assorted load conditions and has capability to deal with FRT.

Chapter 3 Light Load Efficiency Improvement for Soft-Switching Three-Phase Inverter/Rectifier

3.1 Introduction

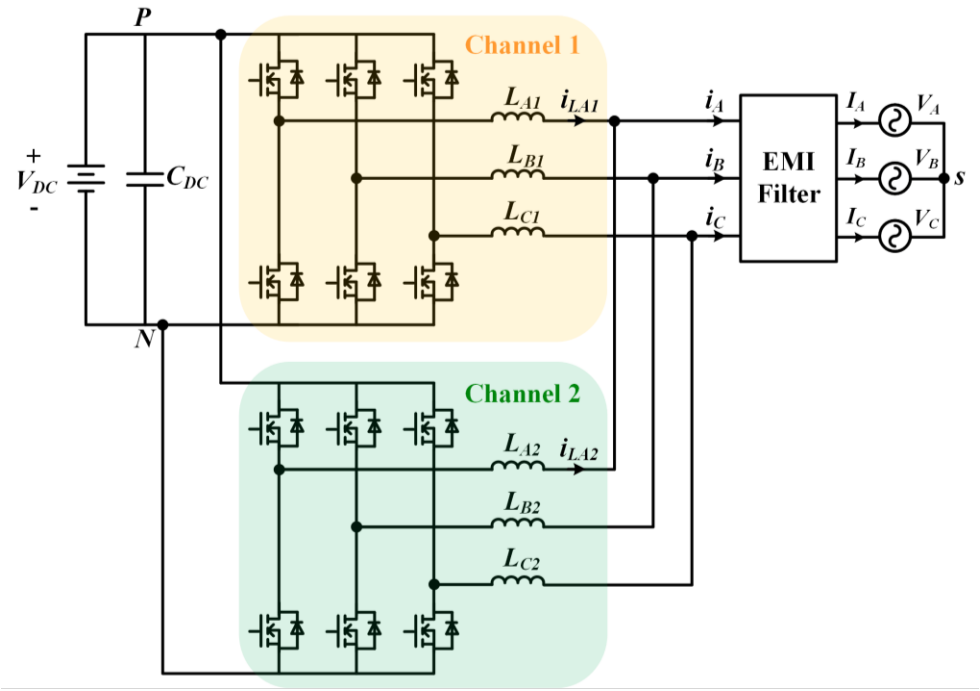


Fig. 3-1. Two-channel paralleled grid-tied three-phase inverter.

Fig. 3-1 shows a two-channel paralleled grid-connected three-phase inverter. When the CRM-based soft-switching technique [23] is adapted for the three-phase inverter, high efficiency and high power density can be accomplished at the same time. Despite this, soft-switching inverter efficiency plunges when the output power decreases, as shown in Fig. 3-2. For PV applications, the inverter efficiency at light load is regarded as an important factor, as much as that at heavy load on account of the term called "weighted efficiency" [48], [49]. This term was introduced to reflect the real operating profile of PV inverters in accordance with surrounding environments such as irradiation and

ambient temperature. Weighting factor is applied to different load conditions, emphasizing the importance of the light load efficiency. To PV inverter manufacturers, improving the light load efficiency is of great interest to attract customers.

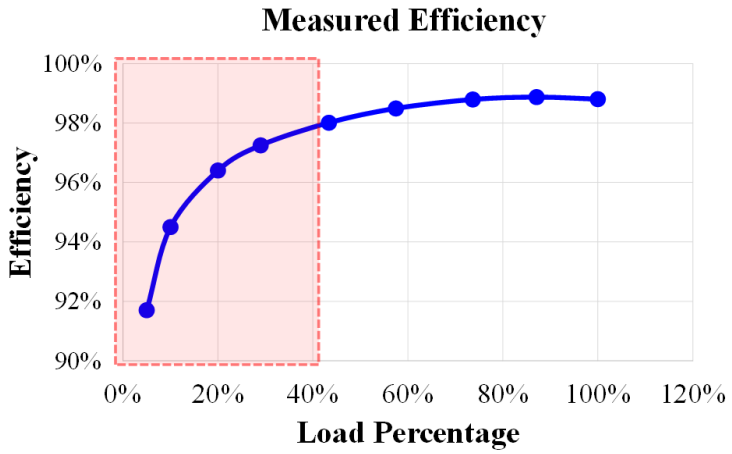


Fig. 3-2. Soft-switching inverter efficiency in [23].

A lot of research has been conducted to figure out how to improve the light load efficiency of several applications. First, in voltage regulator (VR) applications, multiple channels of low voltage dc-dc converters are placed in parallel because of the high output current. Although these converters must handle very high current above several hundreds of amperes at full load, they work at a very light load most of the time. Therefore, the light load efficiency has been studied extensively in this application [50]-[52]. Second, multi-channel single-phase power factor correction (PFC) in front-end converters [53]-[55] also need high light load efficiency because of the similar reason for the VR applications, but not high output current; instead, high input current. On the other hand, it is quite difficult to find literature that digs into the light load efficiency improvement for three-phase inverter/rectifier. The research on this topic has not been actively done. In [56], a phase skipping control for the inverter is discussed. It mainly focuses on the four-wire structure instead of three-wire. [57] proposes a pulse skipping method applied to a two-stage PV system, consisting of not only a three-phase inverter, but

also dc-dc stage. None of these schemes can be immediately applicable to the target inverter in this dissertation because the inverter has the coupled phases in the three-wire configuration and does not have the dc-dc stage.

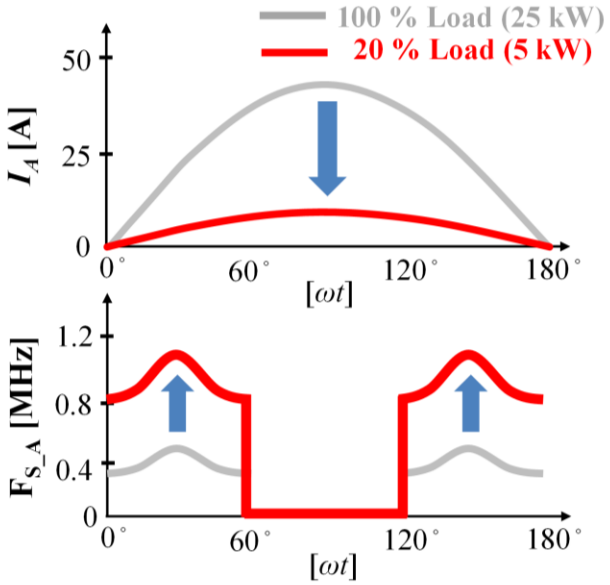


Fig. 3-3. Frequency range in phase A according to load conditions.

The reason for the rapid efficiency drop at light load is associated with dramatic rise in the switching frequency when the inverter encounters such a situation. Fig. 3-3 presents a comparison between two different load cases from frequency range perspective. It shows the switching cycle averaged output ac current in phase A, I_A, as well as the switching frequency range in phase A, F_{S_A}. Here, the rated output power is set to be 25 kW. When the load is reduced to 20 %, I_A becomes one-fifth of that at 100 % load. Of course, the inductor current in channel 1and channel 2 becomes one-fifth of that at 100 % load. Due to the nature of CRM operation, the small inductor current at 20 % brings about a significant surge in the switching frequency. It is clearly seen from Fig. 3-3 that the switching frequency increases by 500- 600 kHz at 20 % load. It even exceeds 1 MHz, which is too extreme. In spite of this inverter's soft-switching ability, this high switching frequency can be huge burden to the inverter.

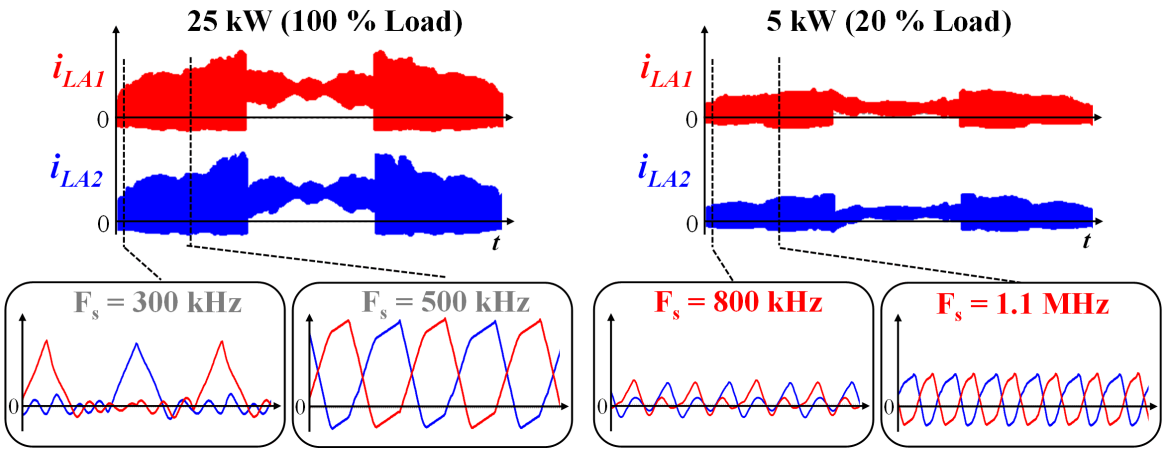


Fig. 3-4. Inductor currents waveform at 100 % load and 20 % load.

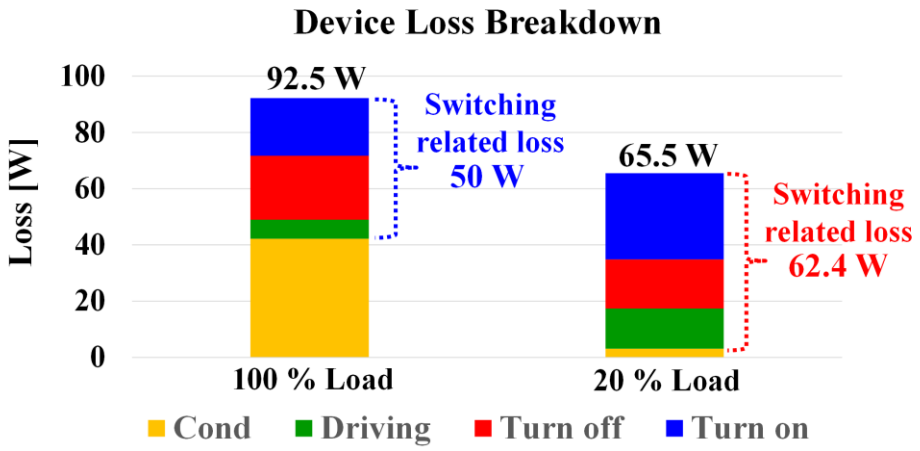


Fig. 3-5. Device loss breakdown comparison for full load and 20 % load.

Fig. 3-4 helps to see this issue more intuitively with the detail inductor current waveforms. It illustrates simulated waveforms of the inverter at both 100 % and 20 % load conditions in a half-line cycle and switching cycles. At 20 % load, channel 1 and channel 2 inductor currents in phase A, i_{LA1} and i_{LA2}, are much smaller than those of 100 % load resulting in the high frequency operation. The problem is that the radical increase in the switching frequency produces skyrocketed switching loss. Device losses are estimated for the two conditions and the loss breakdowns are shown in Fig. 3-5. For the device loss estimation, a 21mΩ SiC MOSFET with a Kalvin source by CREE (C3M0021120K

[58]) is selected. At the full load, the conduction loss is 42.5 W and the switching loss is 50 W. The portion of the switching loss is somewhat higher than the conduction loss, roughly 55% of the total device loss, but it remains very close. However, at 20 % load, the switching loss is 62.4 W. This is more than 95 % of the total device loss. The switching loss is not only high, but also dominant at the light load. This provides an inference that switching loss minimization is the key to improve the light load efficiency.

3.2 Phase Shedding for CRM-Based Soft-Switching Three-Phase Inverter

3.2.1 Phase Shedding Control Concept

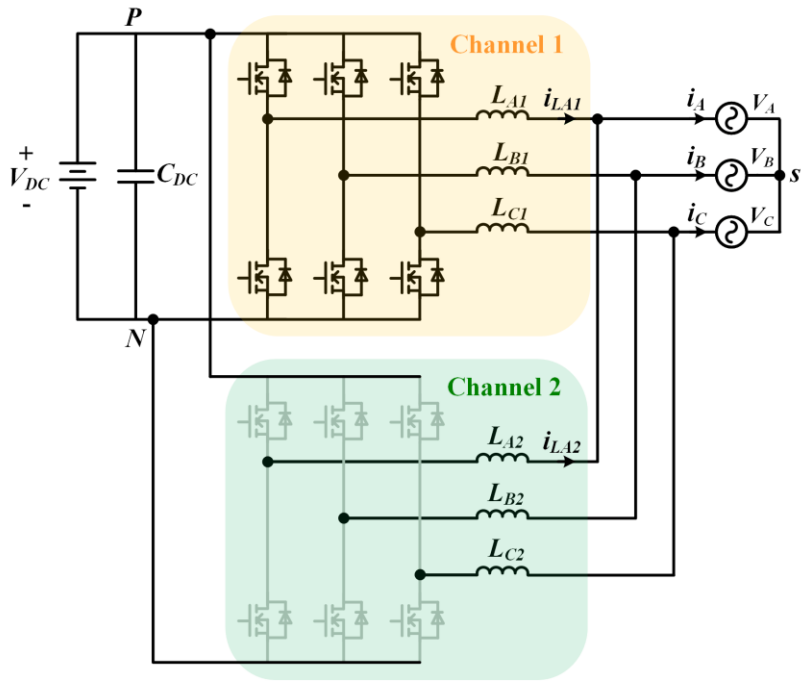


Fig. 3-6. Phase shedding for the entire CH2 in two-channel paralleled three-phase inverter.

The basic idea of the phase shedding control is to reduce the switching frequency by making CH1 manage more power and have a larger inductor current. Fig. 3-6 displays the phase shedding strategy where gate signals are not given for the whole CH2; every switch in CH2 is drawn as the gray

line. In this figure, the EMI filter is omitted for simplicity. Conceptually, the output ac current, i_A, is supposed to flow through CH1 thoroughly through the phase shedding. Then, due to the increased inductor current in CH1, CH1 switching frequency is reduced. Not to mention that the phase shedding does not affect the switching frequency of the clamping mode.

Fig. 3-7 shows a switching frequency reduction at 20 % load when the phase shedding is carried out, compared with the two-channel interleaving case. The frequency drops by roughly 300 kHz. It is expected that the frequency decrease cuts down the switching loss remarkably. Moreover, the number of switches running at high frequency becomes a half from eight to four, due to the no switching action in CH2. This also helps to reduce the switching loss substantially. It should be pointed out that the phase shedding has been commonly used for multi-channel low voltage VRs [52] and multi-channel single-phase PFCs [53], but it is hardly studied for the two-channel paralleled three-phase ac-dc inverter. One difference is that, for those applications, the prime advantage comes from the lowered number of switches running at high frequency. But for the CRM-based soft-switching inverter, the switching frequency itself is brought down and the number of switches running at high frequency is reduced.

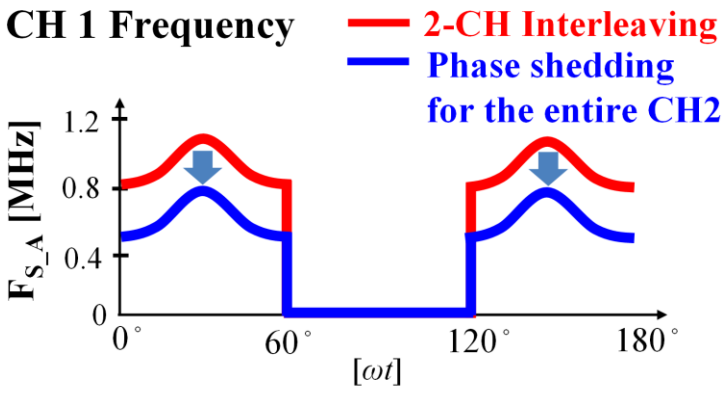


Fig. 3-7. Phase A switching frequency with the two-channel interleaving (red) and with the phase shedding (blue) at 20 % load.

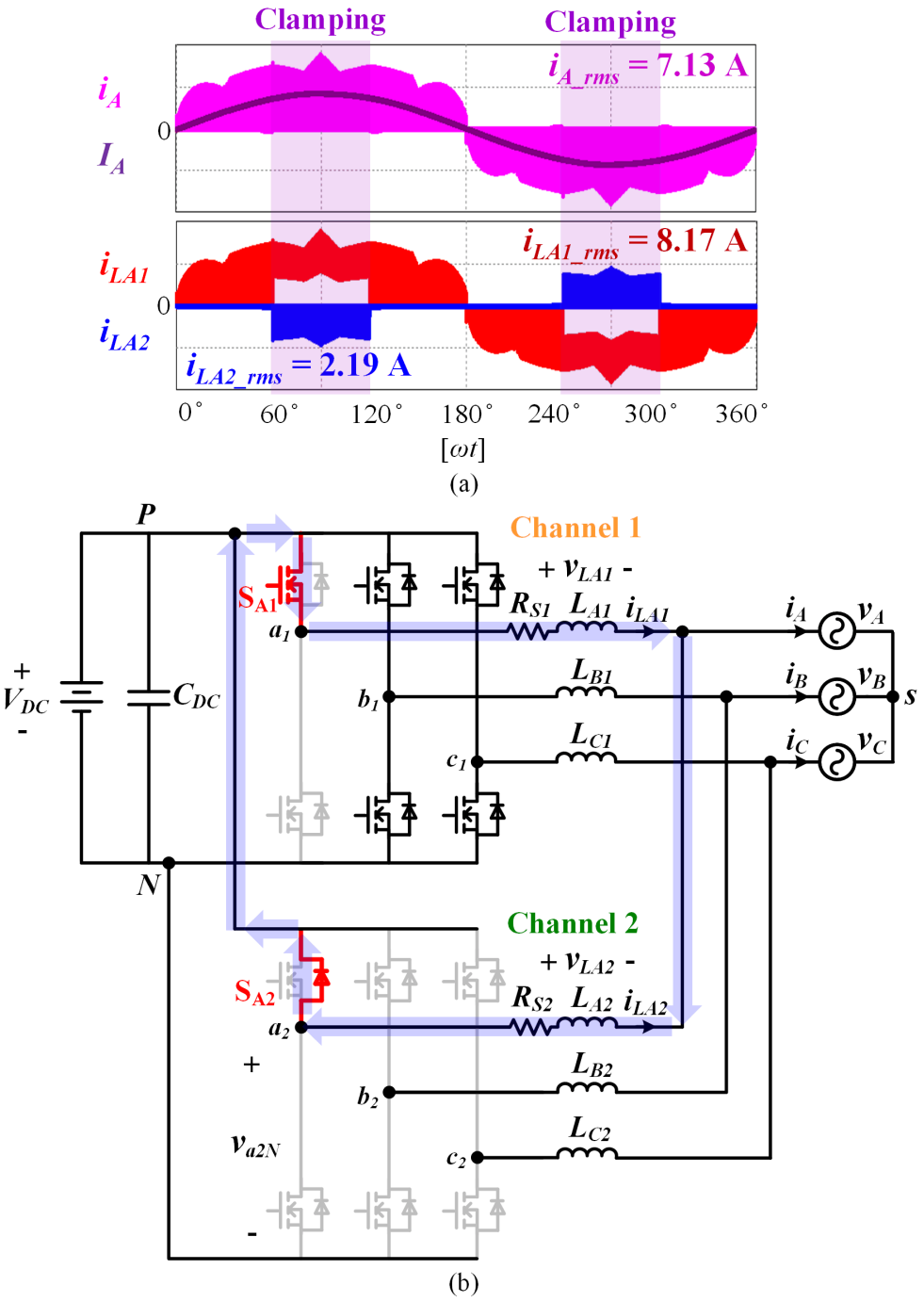


Fig. 3-8. Circulating current issue. (a) Simulation waveforms of phase A output ac current (pink), average output ac current (purple), inductor currents in CH1 (red) and CH2 (blue) with phase shedding for the entire CH2 at 20 % load. (b) Circulating current path during 60° to 120° in the inverter circuit.

By the way, unlike what is expected and in spite of having no gate signals applied to the switches in CH2, some current flows in CH2 during clamping mode, as shown in Fig. 3-8(a). For instance, during 60° to 120° where phase A is clamped to *P* node, phase A inductor current in CH2 is not zero, but exists as a negative value. This negative current does not transfer any energy to the ac side. It only circulates between CH1 and CH2 having the rms value of CH1 inductor current larger than the output ac current (i_{A_rms} = 7.13 A, and i_{LA1_rms} = 8.17 A in Fig. 3-8(a)). This is undesirable as it causes an additional conduction loss. Fig. 3-8(b) depicts how the undesired current circulates in the circuit. When phase A is clamped to *P* node by keeping the top switch in CH1 (S_{A1}) on, the corresponding switch's body diode in CH2 (phase A top switch in CH2, S_{A2}) is conducted. Then, the circulating current path denoted by the blue arrows is created. To fully comprehend the reason why the body diode in CH2 becomes forward-biased, the phase A inverter output voltage in CH2, v_{a2N}, needs to be investigated at the transition from CRM to clamping mode. It must be made clear that the same phenomenon is also observed for phase B and C when these phases are in clamping mode.

3.2.2 Circulating Current Analysis During Phase Shedding

First, to acquire v_{a2N}, we need to make an assumption that all switches in CH2 are open and the inductor currents in CH2 are zero because we do not know the status of the switches in CH2 at the beginning as shown in Fig. 3-9(a). Then, each inductor voltage in CH2 is zero, and the inverter output voltage is expressed as

$$v_{a2N} = V_A + v_{sN} \tag{3-1}$$

where V_A is phase A ac voltage, and v_{sN} is the zero-sequence voltage, which is also called common-mode or offset voltage. The zero-sequence voltage in the two-channel paralleled inverter is presented as

$$v_{sN} = \frac{(v_{a1N} + v_{b1N} + v_{c1N} + v_{a2N} + v_{b2N} + v_{c2N})}{6}. \tag{3-2}$$

Here, v_{x1N} and v_{x2N} (x = a, b, and c) are the inverter output voltage (voltage potential between the switching node of each phase leg a_1, b_1, c_1, a_2, b_2, c_2 and N node) in CH1 and CH2. Under another assumption that all inductors in the inverter are identical and the ac voltages are balanced, (3-2) can be simplified as follows:

$$v_{sN} = \frac{(v_{a1N} + v_{b1N} + v_{c1N})}{3}. \tag{3-3}$$

Equation (3-1) and (3-3) represent that the inverter output voltage in CH2 could be influenced by the switching status in CH1, although no gate signal is applied to CH2 switches, through the zero-sequence voltage. This is because the two channels share the dc side and the neutral point at the ac side in the paralleled structure. The following step is to obtain v_{a2N} at the mode transition from CRM to clamping mode. Fig. 3-10 displays the switching status of CH1switches at the instant of the mode transition when phase A enters clamping mode from CRM. S_{x1} and S_{x1}' (x = A, B, and C) are the switching statuses of the top and bottom switches in CH1, respectively. Both phase A and phase B top switches in CH1 are turned on at t_0 as shown in Fig. 3-9(b). In phase C, neither the top switch nor the bottom switch is turned on as phase C ac voltage and output ac current are almost zero at the transition instant. The inverter output voltages in CH1 at t_0 are expressed as

$$v_{a1N}(t_0) = V_{DC} \tag{3-4a}$$

$$v_{b1N}(t_0) = V_{DC} \tag{3-4b}$$

$$v_{c1N}(t_0) = V_C(t_0) + v_{sN}(t_0). \tag{3-4c}$$

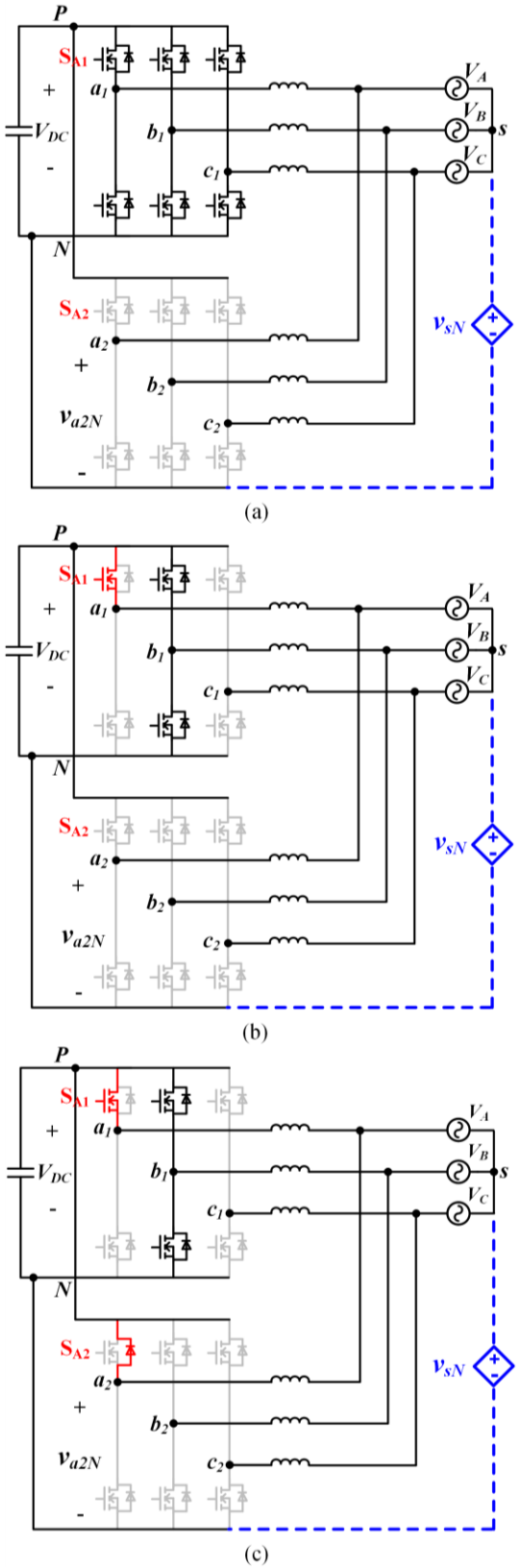


Fig. 3-9. Analysis of circulating current path formation.

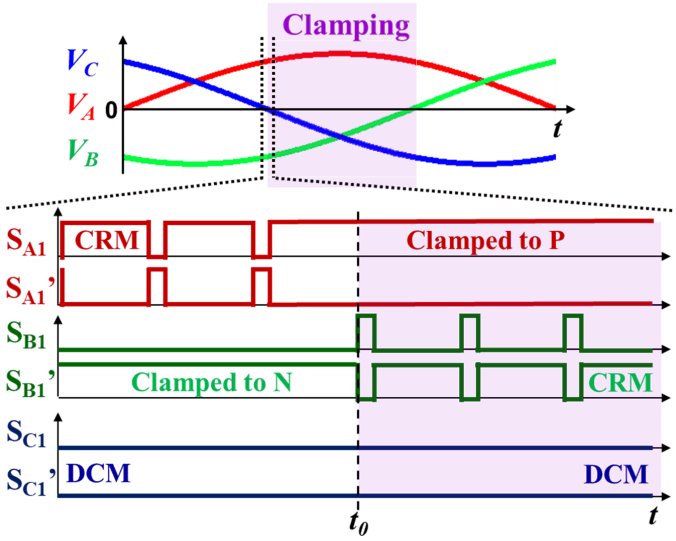


Fig. 3-10. Switching status of all switches in CH1 at the mode transition of phase A from critical conduction mode to clamping mode.

Equation (3-5) is obtained by substituting (3-4) into (3-3) as:

$$v_{sN}(t_0) = \frac{1}{2} V_C(t_0) + V_{DC} \approx V_{DC} . \tag{3-5}$$

As mentioned, V_C at t_0 is almost zero, and v_{sN} can be approximated to V_{DC}. Eventually, the combining (3-5) with (3-1) yields

$$v_{a2N}(t_0) = V_A(t_0) + v_{sN}(t_0) \approx V_A(t_0) + V_{DC} . \tag{3-6}$$

Since V_A is a positive value at t_0 and V_{DC} is the input voltage, v_{a2N} is much larger than V_{DC} at t_0. As a result, v_{a2N} is clamped to V_{DC}, and phase A top switch S_{A2} must be conducted through the body diode as shown in Fig. 3-9(c). This is how the CH2 body diode in clamping mode starts to be forward-biased.

Fig. 3-11 minutely illustrates the simulation waveforms relevant to the circulating current to show how it is formed and acts after S_{A2}'s body diode is conducted. v_{LA1} is the voltage across the

phase A inductor in CH1, L_{A1}, and v_{LA2} is the voltage across the phase A inductor in CH2, L_{A2}, respectively. It should be pointed out that the mode transition from CRM to clamping mode for phase A can take place anytime between t_0' and t_1 in Fig. 3-11, but for the sake of brevity, the case where the event happens at t_0 is chosen for the ensuing discussions.

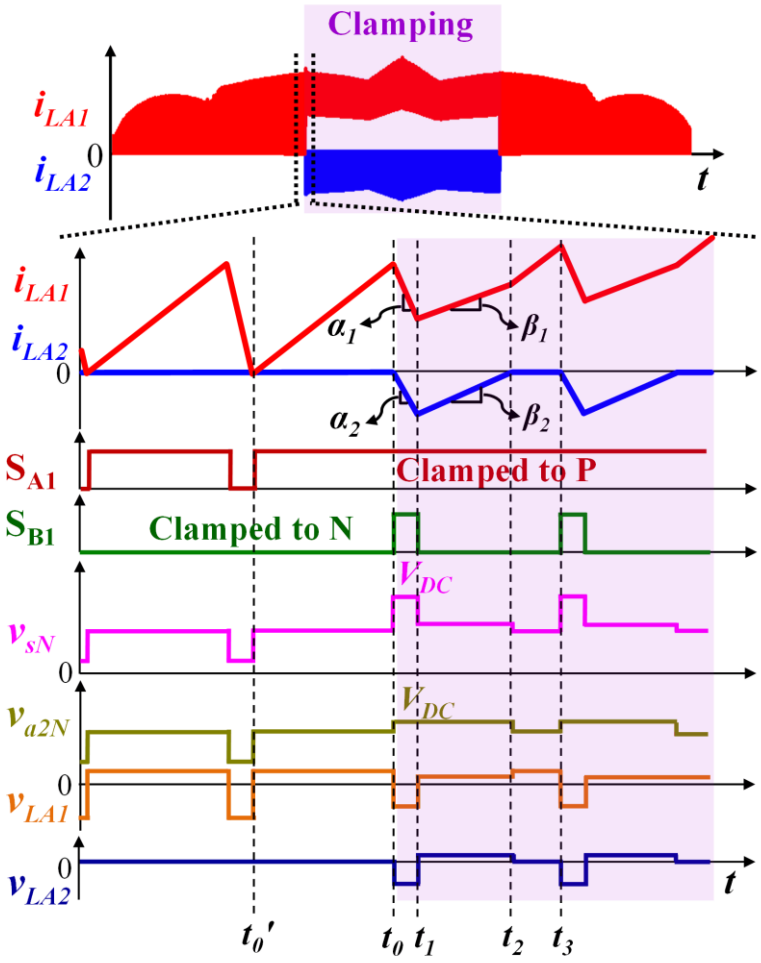


Fig. 3-11. Simulation waveforms of phase A inductor currents (i_{LA1}, i_{LA2}), CH1 top switch gate signals in phase A and phase B (S_{A1}, S_{B1}), zero-sequence voltage(v_{sN}), phase A inverter output voltage in CH2 (v_{a2N}), and phase A inductor voltages (v_{LA1}, v_{LA2}) at the transition from CRM to clamping.

1) *Interval t_0-t_1*: At t_0, phase A gets into clamping mode and phase B starts to operate at CRM. Once S_{B1} is turned on, v_{a2N} increases to V_{DC}, and S_{A2}'s body diode is conducted as explained in (3-4) to (3-6). The voltage across L_{A1} and L_{A2} are expressed as:

$$v_{LA1} = V_{DC} - V_A - v_{sN} - R_{S1} i_{LA1} = -V_A - R_{S1} i_{LA1} \tag{3-7a}$$

$$v_{LA2} = V_{DC} - V_A - v_{sN} - R_{S2} i_{LA2} = -V_A - R_{S2} i_{LA2} \tag{3-7b}$$

where R_{S1} and R_{S2} are series resistance in the loop including the on-resistance of the switches and parasitic resistance of the trace in CH1 and CH2, respectively, as shown in Fig. 3-8(b). During this interval, the voltage excitations for L_{A1} and L_{A2} are less than zero. In turn, the inductor currents begin to decrease. Since the initial value of i_{LA2} in this interval is zero, it goes down to a negative value. This negative current is the circulating current. It is noteworthy to mention that the voltage across the inductors in (3-7a) and (3-7b) is very similar, but slightly different due to the last term in the equations. Because i_{LA1} is a positive value and i_{LA2} is a negative value, the polarity of the voltage drop for the resistors are the opposite. Thus, the slope of i_{LA1}, $|\alpha_1|$, is slightly steeper than that of i_{LA2}, $|\alpha_2|$ in Fig. 3-11.

2) *Interval t_1-t_2*: When S_{B1} is turned off and S_{B1}' is turned on (ignoring the dead-time between S_{B1} and S_{B1}' for simplicity), the zero-sequence voltage varies. Regardless of the zero-sequence voltage change, the body diode of S_{A2} still stays conducted during this interval, since i_{LA2} is a negative value and must have a path to flow. Now, we need to use (3-2) to obtain v_{sN} instead of (3-3), as the assumption that all switches in CH2 are open is no longer valid. It is re-calculated as below:

$$v_{sN}(t_1) = \frac{1}{3} V_B(t_1) + \frac{2}{3} V_C(t_1) + \frac{2}{3} V_{DC} \approx \frac{1}{3} V_B(t_1) + \frac{2}{3} V_{DC}\,. \tag{3-8}$$

The equation for v_{LA1} and v_{LA2} are the same as (3-7), but the positive values due to different v_{sN}. So the inductor currents increase during this interval. Here, the slope of i_{LA1}, $|\beta_1|$ is smaller than that of i_{LA2}, $|\beta_2|$. This stage ends once i_{LA2} reaches zero.

3) *Interval* t_2-t_3: At t_2, i_{LA2} becomes zero. Then the body diode becomes reverse-biased. There is no current flowing through the body diode of S_{A2}, and the zero-sequence voltage changes given by

$$v_{sN}(t_2) = \frac{1}{2}V_C(t_1) + \frac{1}{2}V_{DC} \approx \frac{1}{2}V_{DC} . \tag{3-9}$$

During this interval, the voltage across L_{A1} and L_{A2} are yielded as

$$v_{LA1} = V_{DC} - V_A - v_{sN} - R_{S1}i_{LA1} = \frac{1}{2}V_{DC} - V_A - R_{S1}i_{LA1} \tag{3-10a}$$

$$v_{LA2} = 0 . \tag{3-10b}$$

i_{LA1} still increases, but i_{LA2} remains at zero. Eventually, the circulating current loop does not exist anymore. This continues until S_{B1} is turned on at t_3 at which the zero-sequence voltage is built up to V_{DC}, creating the circulating loop again. Then, the unwanted circulating current resurfaces.

3.3 Improved Phase Shedding Control

3.3.1 Improved Phase Shedding to Eliminate Circulating Current

The solution to steer clear of the circulating current is to activate the clamping mode phase in CH2 [59]. For example, in Fig. 3-12(a), phase A is in clamping mode and CH1 is clamped to the *P* node through S_{A1}. Then the gate signal for phase A in CH2 (S_{A2}) is also forced to be turned on. Basically, phase A in CH2 is also clamped to the *P* node. But the gate signals for the CRM phase

and the DCM phase (phase B and phase C) in CH2 are still not given. In other words, the phase shedding is conducted only for the CRM phase and the DCM phase in CH2.

In this way, i_{LA2} can flow through S_{A2} in both positive and negative directions although the same loop exists between CH1 and CH2. When phase A gets into clamping mode, i_{LA2} goes to a negative value like the original phase shedding method, but now i_{LA2} can be a positive value and seems to converge to i_{LA1}, as shown in Fig. 3-12(b). The main difference from the original phase shedding method is the capability of bidirectional current flow through the activated S_{A2}. This results in the disappearance of the time interval t_2-t_3 in Fig. 3-10. Instead, i_{LA2} continues to increase until S_{B1} is turned on, and becomes a positive value in the end.

In the convergence process of i_{LA1} and i_{LA2}, R_{S1} and R_{S2} play critical roles as damping factors (25 mΩ for each). At the starting point of the clamping mode, i_{LA1} is larger than i_{LA2}. Thus, the voltage drop across R_{S1} is larger than that across R_{S2}. This results in larger voltage excitation across L_{A2}, v_{LA2} than L_{A1}, v_{LA1}. Then, i_{LA1} increases and i_{LA2} decreases. Now that the clamping mode phase in CH2 is activated, i_{LA2} can be a positive value which would not be possible in the original phase shedding. As time goes by, i_{LA1} keeps decreasing and i_{LA2} keeps increasing, and finally these two currents become identical. As i_{LA2} becomes a positive current completely at last, it is not the circulating current anymore. Both CH1 and CH2 convey power to the ac side and share half of the output current. In summary, by the phase shedding for only the CRM phase and DCM phase in CH2, the circulating current is removed with the help of the bidirectional current flow via S_{A2} and the damping elements in the loop. The same method is applied when the other phases enter clamping mode along the whole line cycle. For instance, when phase B is in clamping mode and clamped to *N* node in CH1, phase B bottom switch in CH2 is also turned on, but the other phases (phase A and phase C) in CH2 do not have any gate signals.

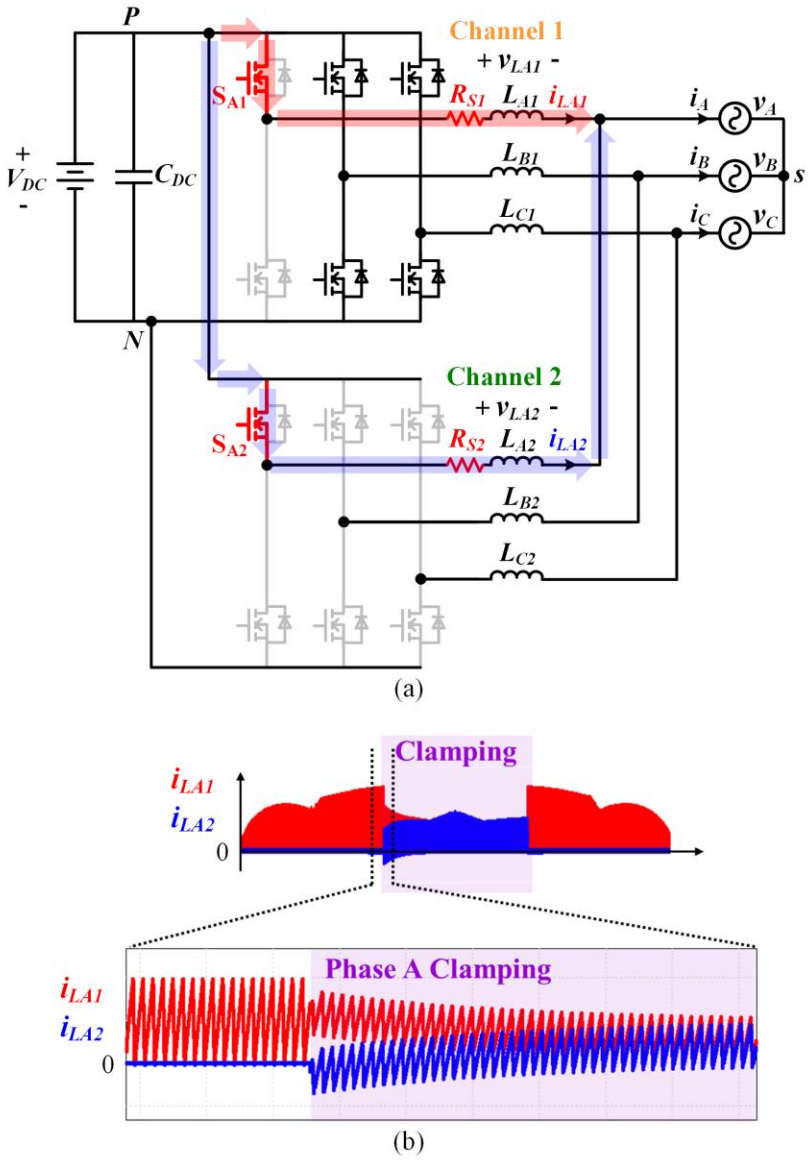


Fig. 3-12. Improved phase shedding control. (a) Activating clamping mode phase in CH2. (b) Convergence of i_{LA1} and i_{LA2} and elimination of the circulating current.

Fig. 3-13 presents the simulation waveforms of the phase A output ac current, and the inductor currents in CH1 and CH2 with the improved phase shedding control. During the clamping modes marked as purple shaded areas, CH1 and CH2 inductor currents are different at first but become the same at the end. The rms value of phase A inductor current in CH1 is reduced significantly compared to that in Fig. 3-8(a), but the rms value of that in CH2 is somewhat increased.

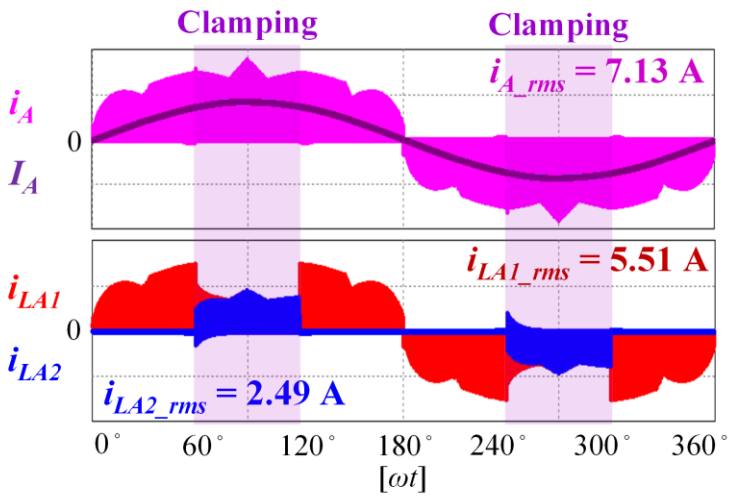


Fig. 3-13. Simulation waveforms of phase A output ac current (purple), CH1 inductor current (red) and CH2 inductor current (blue) with the improved phase shedding at 20 % load.

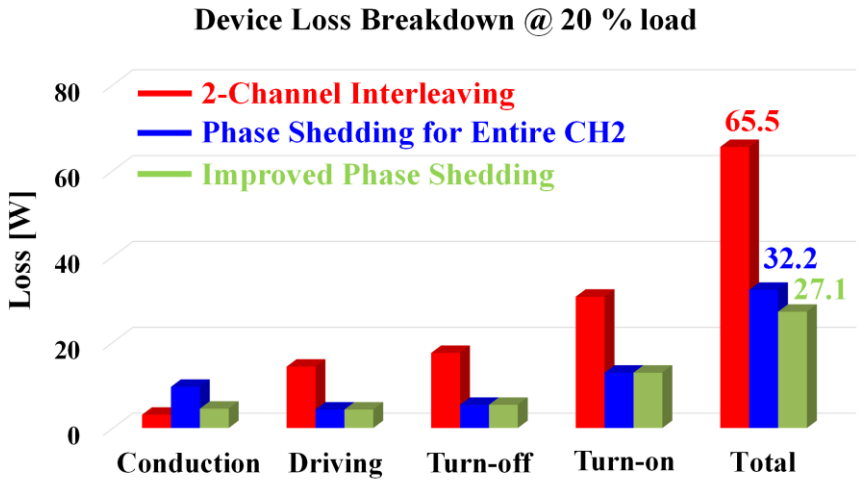


Fig. 3-14. Device loss breakdown comparison for three different control methods at 20 % load.

Fig. 3-14 compares the device loss breakdown for the three control methods. By simply applying the phase shedding, the switching loss decreases enormously. Besides, the improved phase shedding helps to even reduce the conduction loss by eliminating the undesired circulating current between CH1 and CH2. In consequence, the device loss with the improved phase shedding becomes even lower than a half, almost one-third of that with the two-channel interleaving. It should be noted that the fruit of the improved phase shedding might not look very noticeable based

on the results in Fig. 3-14 because of the SiC MOSFETs with small on-resistance (21 mΩ), but it could be more striking if other types of SiC MOSFETs were used which have higher on-resistance.

3.3.2 Extension of Improved Phase Shedding to Convention PWM modulation

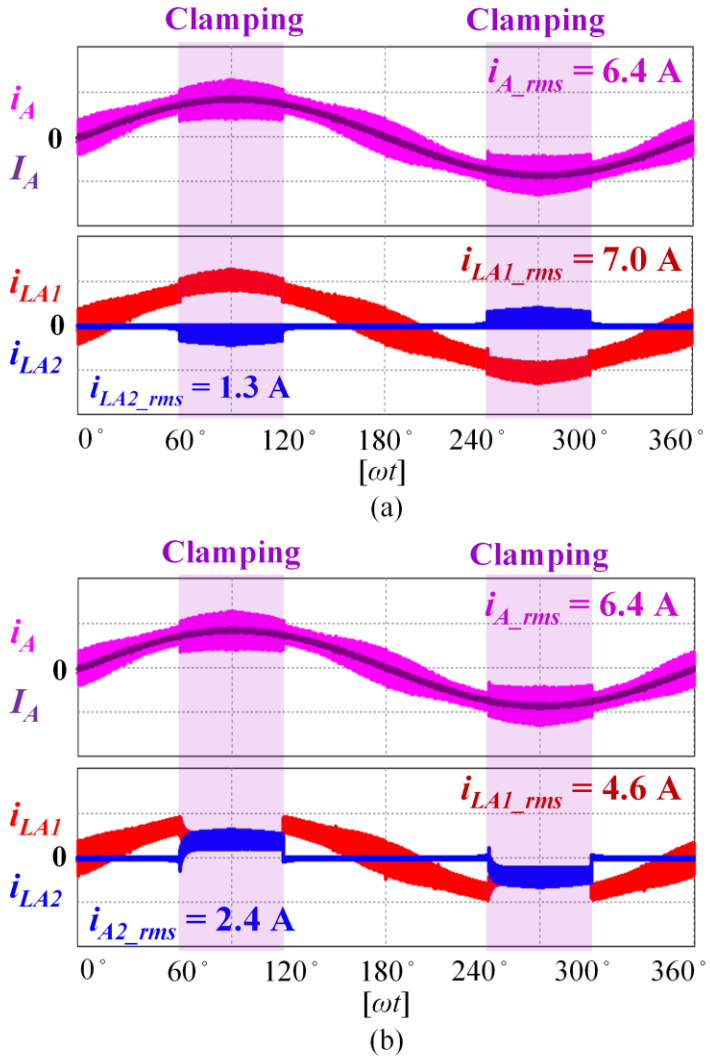


Fig. 3-15. Simulation results of two-channel paralleled DPWM-based three-phase inverter operating at CCM with (a) original phase shedding method and (b) improved phase shedding method.

One thing to note is that the proposed phase shedding control can also be applicable to conventional two-channel paralleled DPWM-based three-phase inverters operating at fixed frequency continuous conduction mode (CCM) [60]. Fig. 3-15 represents the simulation results of the inverter

with both the original phase shedding and the improved phase shedding. Operating conditions such as input voltage, output voltage, and output power are the same as those in Fig. 3-8 and Fig. 3-13. The output inductors (50 μH) and the switching frequency (500 kHz) are chosen so that the inverter operates at CCM. What appears with the original phase shedding is that the circulating current issue in CH2 still exists, as shown in Fig. 3-15(a), even though the inverter operates at CCM with the fixed switching frequency. Likewise, the circulating current is eliminated with the improved phase shedding as shown in Fig. 3-15(b). Based on these observations, it can be inferred that the existence of the circulating current during clamping mode with the original phase shedding has nothing to do with the modulation methods, but rather is a matter of the two-channel paralleled inverter structure in which CH1 and CH2 share the zero-sequence voltage.

3.3.3 Control Structure of Improved Phase Shedding

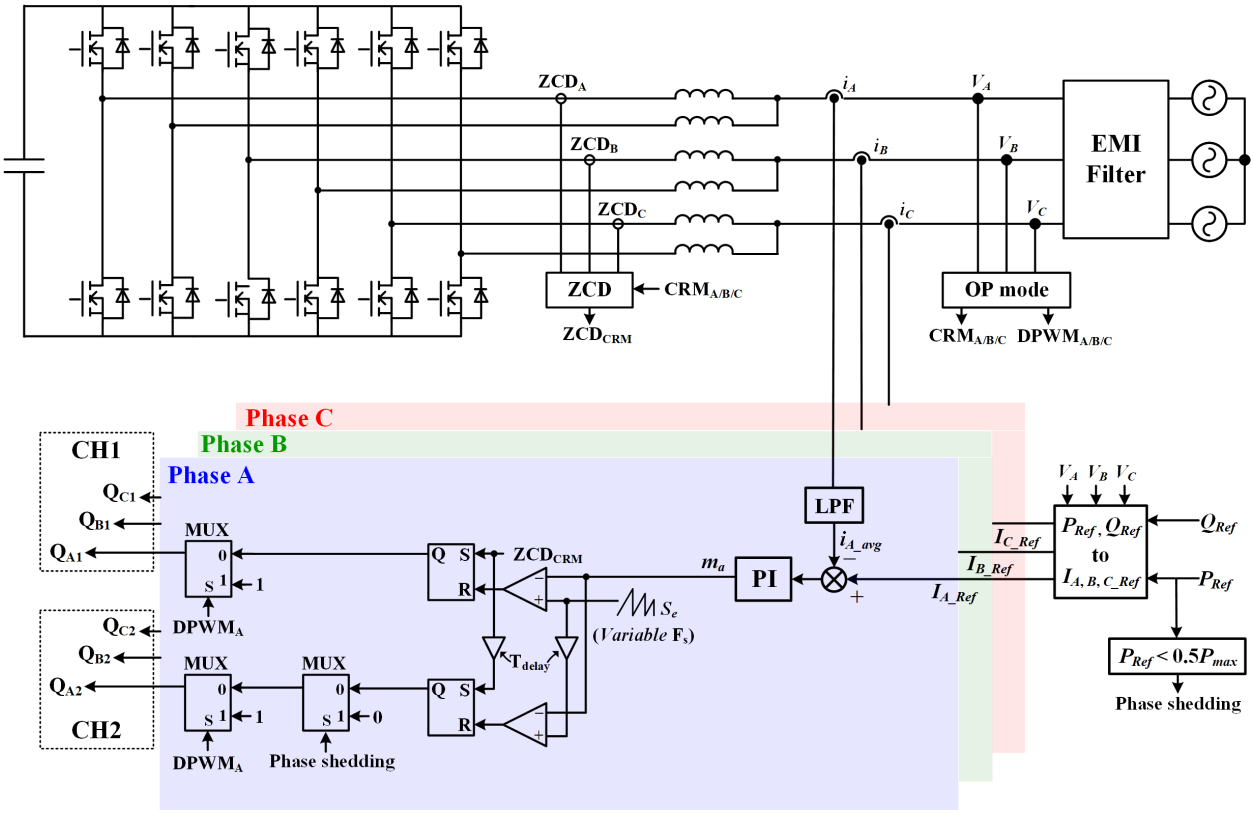


Fig. 3-16. Control structure of the soft-switching three-phase inverter with the improved phase shedding.

Fig. 3-16 shows the overview of the soft-switching inverter control with the improved phase shedding. For brevity, the LC filter on the ac side for the current ripple attenuation is expressed as an EMI filter block. The output ac currents (i_A, i_B, i_C) before the EMI filter, the ac voltages (V_A, V_B, V_C), and the CH1 inductor zero current detection (ZCD_A, ZCD_B, ZCD_C) signals are required to sense. The ac current references (I_{A_Ref}, I_{B_Ref}, I_{C_Ref}) are calculated from the power reference information (P_{Ref}, Q_{Ref}), and the operation mode of each phase is decided by the ac voltages; for example, what phase is in CRM and clamping mode ($CRM_{A/B/C}$, $DPWM_{A/B/C}$). Based on the $CRM_{A/B/C}$ indicator, which phase ZCD signal is utilized as the CRM phase ZCD signal, ZCD_{CRM}.

The sensed output ac currents penetrate an either analog or digital low-pass filter (possibly both) to attenuate the current ripple and generate averaged currents signals (i_{A_avg}, i_{B_avg}, i_{C_avg}) since the current ripple is still large even when 2-channel interleaving is conducted. Then the average currents are controlled to track the current references. The current compensators output the control signals (m_a, m_b, m_c). It is worth mentioning that the current controller can be realized in many ways. In this chapter, abc-frame is used, and in each phase average currents are controlled independently. Other methods will be discussed later in Chapter 5. These signals include turn-off instant information from the active switches and are compared to the sawtooth signals (internal counter in digital control), S_e. On the other hand, the turn-on of the active switches is triggered by ZCD_{CRM}. To realize the open-loop control for two-channel interleaving [61], ZCD_{CRM} and S_e are 180-degree phase-shifted by the time delay, T_{delay}. The time delay is half of the switching period of the previous switching cycle which is captured by an eCAP function in a digital controller. Then, based on the operation mode of each phase, the PWM signal is processed by the final multiplexer to be either the one coming from the Set/Reset latch or the high signal for DPWM. When the output power reference is smaller than 50% of the rated output power, P_{max}, the proposed phase shedding

control is carried out. The PWM signals in CH2 are forced to be the low signal. Finally, only the clamping mode phase in CH2 is activated and set to be high at the final stage.

3.4 Experimental Results

TABLE 2 SPECTIFICATIONS OF THE PROTOTYPE FOR PHASE SHEDDING

Condition	Value
Rated Output Power (P_{o_rated})	25 kW
Input Voltage (V_{DC})	800 V
Output AC Voltage (V_{AC})	277/480 Vrms at 60 Hz
Inductor (L_{A1}, L_{A2}, L_{B1}, L_{B2}, L_{C1}, L_{C2})	5.28 µH
Minimum Switching Frequency (F_{S_Min})	300 kHz
LC Filter Cutoff Frequency (F_{Cutoff_LC})	67 kHz
SiC MOSFETs	C3M0021120K

A 25 kW SiC-based three-phase inverter prototype based on Fig. 3-1 was built to validate the performance of the proposed phase shedding control, as shown in Fig. 2-18. The specifications of the inverter prototype are enumerated in TABLE 2.

Fig. 3-17 and Fig. 3-18 display the experimental waveforms of the CRM-based soft-switching three-phase inverter with the improved phase shedding control at different loads. In Fig. 3-17, the average output ac currents, I_A, I_B, and I_C (three waveforms on the top), phase A inductor current in CH1 and the inductor current in CH2 at 40 % load (10 kW) are illustrated. In Fig. 3-18, those at 20 % load (5 kW) are depicted. Firstly, the average output ac currents are properly regulated as sinusoidal with the proposed phase shedding control. Furthermore, CH1 and CH2 inductor currents come to be identical during the clamping mode such that no circulating current is existent. At the

beginning of the clamping mode, the CH1 inductor current and the CH2 inductor current are slightly different, but they converge to each other swiftly as discussed in Fig. 3-12(b). Apart from the clamping mode regions, the average inductor current in CH2 remains zero. It should be mentioned that the CH2 inductor current is not perfectly zero in the waveforms. The reason is that the inductors in CH2 resonate with output capacitors of some switches in CH1 and CH2, although the CH2 switches are all turned off except for the clamping mode phase.

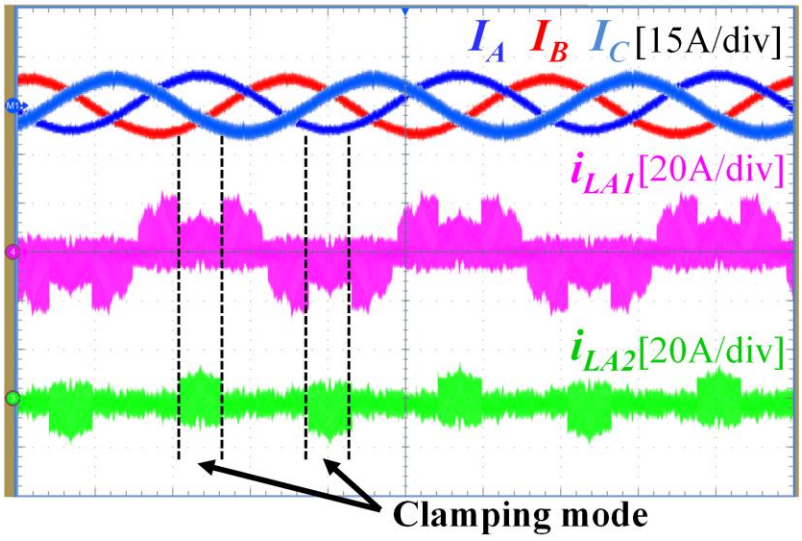


Fig. 3-17. Experimental waveforms of the improved phase shedding control at 40 % load.

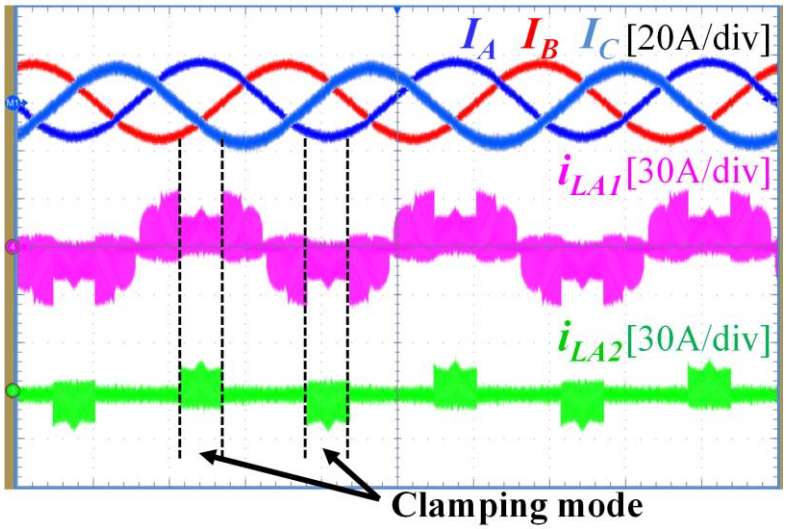


Fig. 3-18. Experimental waveforms of the improved phase shedding control at 20 % load.

Load transient experimental waveforms are shown in Fig. 3-19 with the average output ac currents, and the inductor currents in phase A. Fig. 3-19(a) shows the load transient from 60 % load (2-CH interleaving) load to 30 % load (improved phase shedding). At 30 % load, as all current flows through CH1 during CRM and DCM operation modes, the peak value of CH1 current is close to that at 60 % load. Fig. 3-19(b) is the load transient from 30 % load (phase shedding) to 60 % load (2-CH interleaving). It is observed that the transition from 2-CH interleaving to phase shedding is very smooth without any glitch.

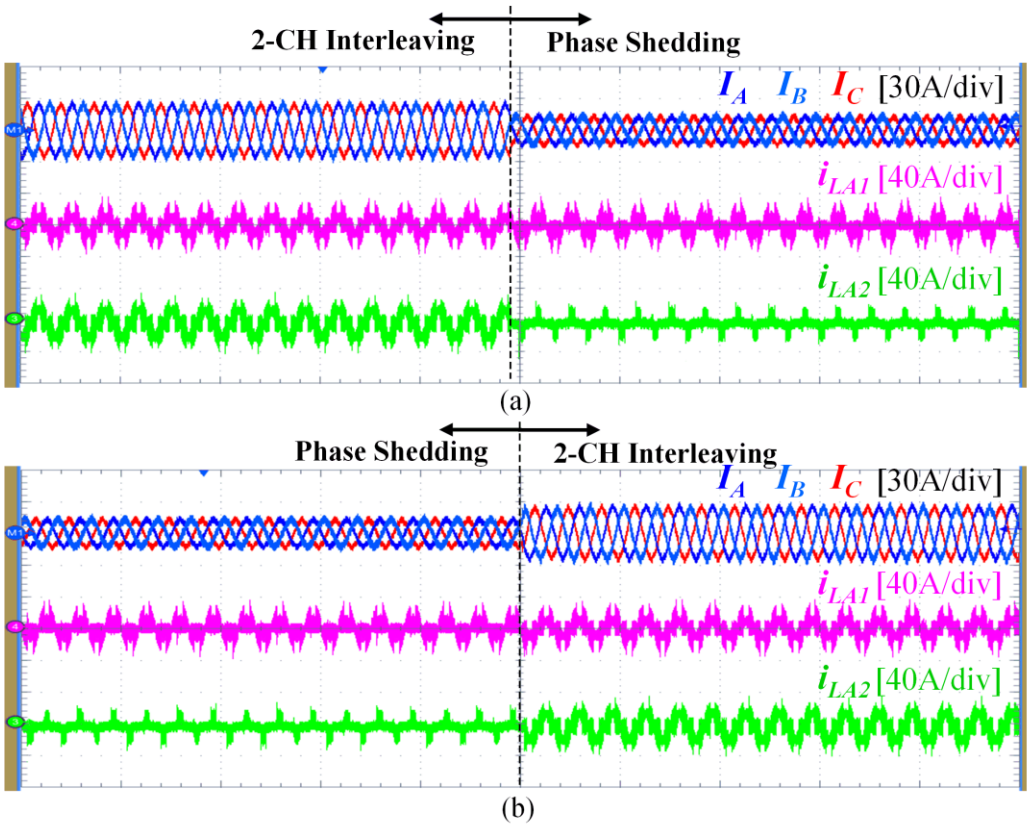


Fig. 3-19. Experimental waveforms of the improved phase shedding control at 20 % load.

Fig. 3-20 presents the measured inverter efficiency comparison for two different control methods under assorted load conditions (two-channel interleaving vs. improved phase shedding). It proves the effectiveness of the improved phase shedding scheme for light load efficiency. It is substantially

improved by 0.5 to 3.9 % at different loads. Specifically, the efficiency improvement is more appreciable at lighter load. Most losses come from the switching loss at light load due to high switching frequency and the conduction loss is comparatively small, as explained in Fig. 3-5. Above 20 % load, the efficiency is always higher than 98 %. The efficiency data in Fig. 3-20 is collected by a PA2203A power analyzer.

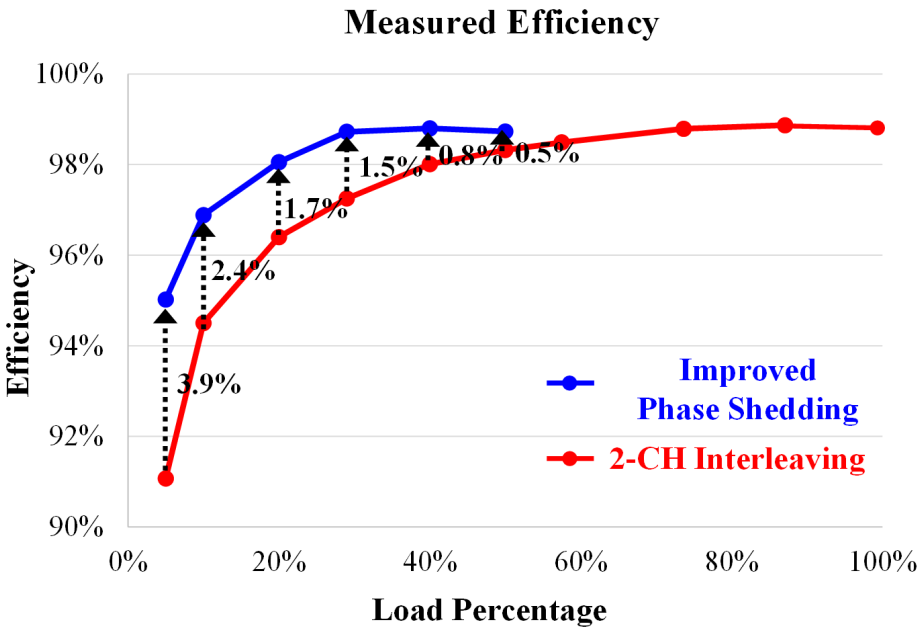


Fig. 3-20. Tested efficiency comparison: 2-CH interleaving, the improved phase shedding.

As a result, the weighted efficiency is also improved considerably. TABLE 3 and TABLE 4 show how beneficial the improved phase shedding control is on PV systems by comparing the two different weighted efficiencies (CEC and EURO) between the 2-CH interleaving control and the proposed control method. The CEC efficiency is enhanced by 0.46 %, and EURO efficiency is enhanced by 0.81 % for the 25 kW three-phase inverter, respectively. Since EURO efficiency put more weight on the light load efficiency, the effect of the phase shedding is more recognizable in this case.

TABLE 3 Weighted Efficiency Comparison (CEC)

Method	Efficiency @ various load condition						**CEC** Eff.
	10%	20%	30%	50%	75%	100%	
2-CH Interleaving	94.5 %	96.4 %	97.3 %	98.3 %	98.9 %	98.8 %	**98.27 %**
Improved Phase Shedding	96.7 %	98.1 %	98.7 %	98.7 %	98.9 %	98.8 %	**98.71 %**

TABLE 4 Weighted Efficiency Comparison (Euro)

Method	Efficiency @ various load condition						**Euro** Eff.
	5%	10%	20%	30%	50%	100%	
2-CH Interleaving	91.1 %	94.5 %	96.4 %	97.3 %	98.3 %	98.8 %	**97.61 %**
Improved Phase Shedding	95.0 %	96.7 %	98.1 %	98.7 %	98.7 %	98.8 %	**98.42 %**

Lastly, the tested total rated-current distortion (TRD) for the two control schemes is shown in Fig. 3-21. Now that the target applications for the inverter are the DERs, TRD is measured rather than total harmonic distortion (THD), on the basis of the IEEE standard 1547-2018 [62]. The two-channel interleaving method boasts lower TRD because the switching frequency is the highest among the three methods, so the ripple at the sensed average current is attenuated more than that of the phase shedding method. In digital control, the small current ripple at the sensed average current provides MCU with very accurate sampled information, the current control accuracy is improved. The phase shedding helps improve light load efficiency by decreasing switching frequency, but this is not advantageous to attenuating the current ripple. Moreover, a current ripple cancellation effect by the two-channel interleaving does not exist any longer. This adversely affects TRD and make it higher compared to the two-channel interleaving case. However, the proposed control method still meets the requirement (5%) with enough margin.

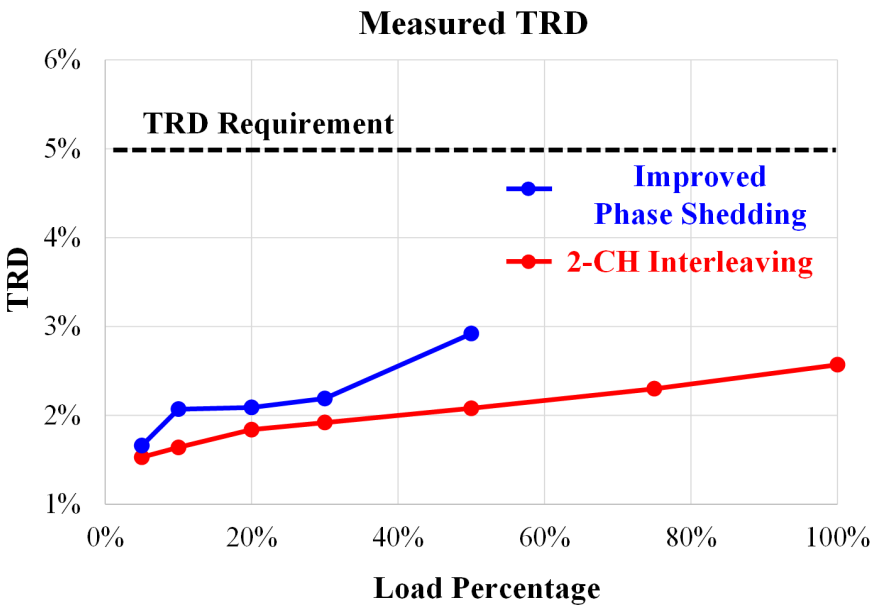


Fig. 3-21. TRD comparison: 2-CH interleaving, the improved phase shedding.

3.5 Conclusion

In this chapter, phase shedding control methods for a two-channel paralleled CRM-based soft-switching three-phase inverter are proposed to improve light load efficiency. First, the phase shedding is applied to the entire CH2. However, the shared zero-sequence voltage in the parallel inverter structure drives clamping mode's body diode in CH2 to be conducted, thus unwanted circulating current is generated. To suppress the circulating current, the phase shedding for only the CRM phase and DCM phase in CH2 is applied by activating the clamping mode phase in CH2. Experiments with the proposed controls, both steady-date and transient response, verify that considerable light load efficiency improvement is accomplished, leading to enhanced weighted efficiency.

Chapter 4 PCB Winding Coupled Inductor Design and CM EMI Noise Reduction

4.1 Introduction

For CRM-based soft-switching ac-dc converter with SiC devices, one of the major concerns is conducted electromagnetic interference (EMI) noise. Owing to the fast-switching characteristic of SiC devices, the dv/dt at the switching node of the converter is much higher than that with Si devices [63]. The high dv/dt over parasitic capacitance between the power circuit and the ground generates substantial common mode (CM) EMI noise, as shown in Fig. 4-1. In order to comply with electromagnetic compatibility (EMC) requirements, a large CM filter is necessary between the converter and the ac source, thus depreciating the benefit from the use of SiC devices with CRM at high frequency (small size inductors for the power stage and the small DM filter).

A balance technique can effectively lessen the CM noise of the ac-dc converter [64]-[66]. The power stage is modified in the way that CM equivalent circuits meet the balance condition in the Wheatstone bridge configuration. This helps the power stage share the burden of the CM filter so that the EMI filter size can be reduced. Hence, the balance technique for the three-phase ac-dc rectifier/inverter is studied in this chapter discussing how to design PCB winding coupled inductor.

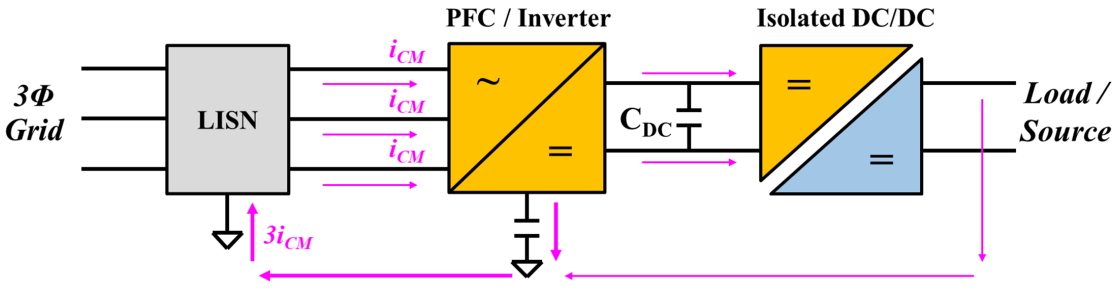


Fig. 4-1. CM noise in three-phase rectifiers/inverters.

4.2 Balance Technique for Two-Channel Interleaved Three-Phase Rectifier /Inverter

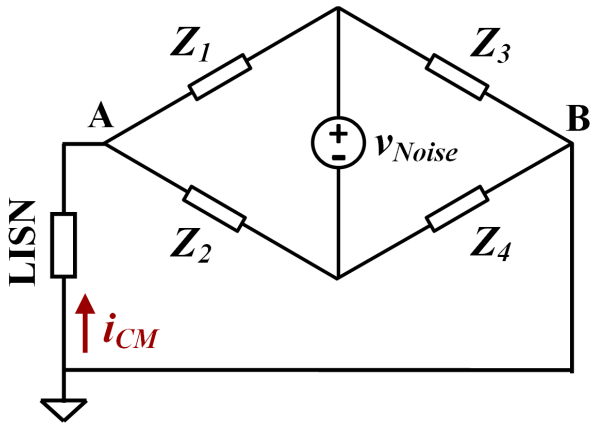


Fig. 4-2. Wheatstone bridge structure for common mode noise.

The balance technique is to balance the impedance ratio of the CM equivalent circuit model in the Wheatstone bridge structure, as depicted in Fig. 4-2 [64]. If the voltage level at node A and node B are identical, no matter how large the noise source, v_{Noise}, is, the current flowing through the LISN, i_{CM}, is zero. This is achieved by the balance condition expressed as:

$$\frac{Z_1}{Z_2} = \frac{Z_3}{Z_4} \tag{4-1}$$

In a single-phase two-channel interleaved totem-pole power factor correction (PFC) converter [66], [67], additional inductors are added in the return path, such that there is a chance to meet the balance condition. These inductors are coupled with the main inductors to fulfill better EMI noise reduction performance at high frequency.

Fig. 4-3 illustrates the two-channel interleaved three-phase ac-dc converter with the balance technique [68]. In this literature, the inductors are implemented by PCB windings to make the

balance technique effective at high frequency up to 10 - 20 MHz. Although the balance concept in the three-phase ac-dc converter is first applied in [69], the result of the balance technique is not very impressive at high frequency beyond 2 MHz. The inductors in this literature are implemented with litz-wire on toroidal cores which make difficult to control parasitic components at tens of MHz level.

In [68], unlike the circuit topology introduced in the previous chapters, a return path is added, connecting the middle point of the dc capacitors, *m*, to the neutral point of the ac filter capacitors, *n*. In the return path, additional inductors are placed to form a balanced structure. The inductors on the return path are coupled with the inductors in the main circuit for better balance at high frequency. L_{A1} and L_{A2} are phase A main inductors inversely coupled with each other, and L_{A3} and L_{A4} are the additional inductors in phase A, coupled to the main inductors. The same sets of inductors are used for phase B and phase C. The detailed operation principle of the soft-switching ac-dc converter and the impact of the additional inductors is elaborated in [70].

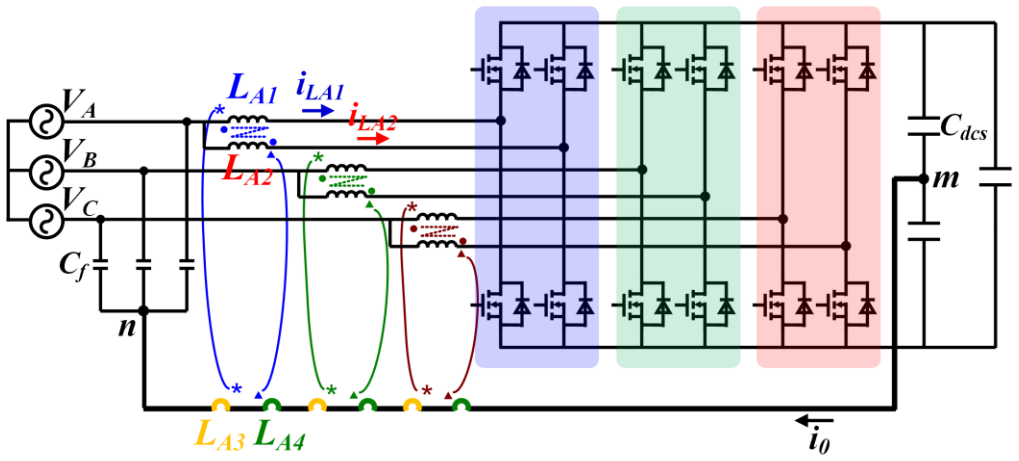


Fig. 4-3. Circuit topology for two-channel interleaved three-phase ac-dc converter with balance technique.

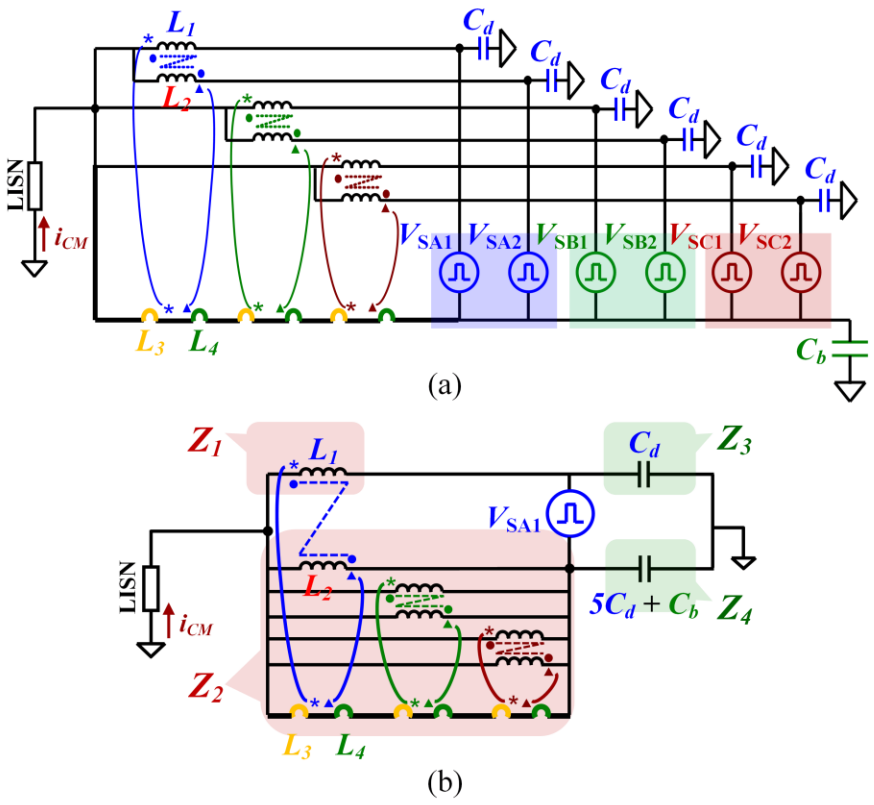


Fig. 4-4. (a) CM equivalent circuit model for two-channel interleaved three-phase ac-dc converter. (b) Simplified equivalent circuit model for V_{SA1} by using the superposition theorem.

Fig. 4-4(a) represents the CM equivalent circuit model with parasitic capacitances. C_d is the capacitance between the switching node (the drain of the bottom switch) of each phase leg and the ground. C_b is the capacitance between the dc bus and the ground. It should be noted that the phase information for the inductors is dropped for the sake of simplicity in Fig. 4-4. According to the EMI circuit modeling method introduced in [64], which is based on the substitution theorem, the dv/dt of each phase leg is replaced with an independent noise source in the form of pulsating voltage, V_{Sxy} (x = A, B, and C representing phase A, B, and C; y = 1 and 2 representing Channel 1 and Channel 2). It should be noted that, in the circuit model, other CM noise sources at the ac filter capacitors, the top switches, and the dc capacitors are omitted, assuming that these sources have relatively minor influence on the CM noise in comparison with the pulsating voltage sources. If

the pulsating voltage sources are the same as the real waveforms at each switching node, the equivalent circuit becomes linear. Then, by applying the superposition theorem, the equivalent circuit is further simplified as the Wheatstone bridge structure shown in Fig. 4-4(b), where only the impact of the noise source of phase A in CH1, V_{SA1}, is presented. When the impedance ratio of Z_1 to Z_2 is equal to Z_3 to Z_4 as in (4-1), the balance condition is achieved, and no CM current by V_{SA1} flows through LISN.

On the assumptions that 1) Parasitic components in the coupled inductors are negligible and 2) The main and extra inductors are perfectly coupled, the ratio of Z_1 to Z_2 is given by:

$$\frac{Z_1}{Z_2} = \frac{N_{12} + 5N_{34}}{N_{34}} \tag{4-2}$$

where N_{12} is the turns number of the main inductors, and N_2 is the turns number of the return path inductors. The ratio of Z_3 to Z_4 is expressed in terms of the parasitic capacitance as:

$$\frac{Z_3}{Z_4} = \frac{C_b + 5C_d}{C_d} \tag{4-3a}$$

$$\frac{Z_3}{Z_4} = \frac{C_b + 5C_d + C_{add1} + 5C_{add2}}{C_d + C_{add2}} \,. \tag{4-3b}$$

Based on (4-2) and (4-3a), the impedance ratio of Z_1 to Z_2 (turns number of the inductors) must be selected by the values of C_b and C_d to satisfy the balance condition, which restricts the design freedom for the inductors. By adding extra capacitance in parallel with the system parasitic capacitance C_b and C_d, C_{add1} and C_{add2}, respectively, the impedance ratio of Z_3 to Z_4 is no longer a fixed value as expressed in (4-3b), allowing flexibility for the balance condition and the inductor design. By substituting (4-2) and (4-3b) into (4-1), the balance condition is obtained by:

$$\frac{N_{12}}{N_{34}} = \frac{C_b + C_{add1}}{C_d + C_{add2}} \,. \tag{4-4}$$

For the rest of the noise sources in Fig. 4-4(a), from V_{SA2} to V_{SC2}, the superposition theorem can be also applied. Accordingly, the simplified equivalent model for the sources similar to Fig. 4-4(b) can be derived. Equation (4-4) is applicable to the other noise sources as well.

It must be mentioned that, in a real implementation, parasitic components of the coupled inductor, specifically EPC, definitely exist and dominate at high frequency around tens of MHz. As a result, (4-2) is no longer constant and varies in accordance with the parasitic elements. Thus, the coupling between the main inductor and the extra inductor, L_1 and L_3, and L_2 and L_4 (phase information is omitted in the subscript as all the inductors in phase A, B, and C are intended to be identical), need to be as close as unity. With this strong coupling, the parasitic elements in the main inductor and the extra inductor are reflected to each other, such that the impedance ratio of Z_1 to Z_2 remains almost constant, even if the parasitic components become predominant. In this way, the balance condition is still valid even at the high frequency [71].

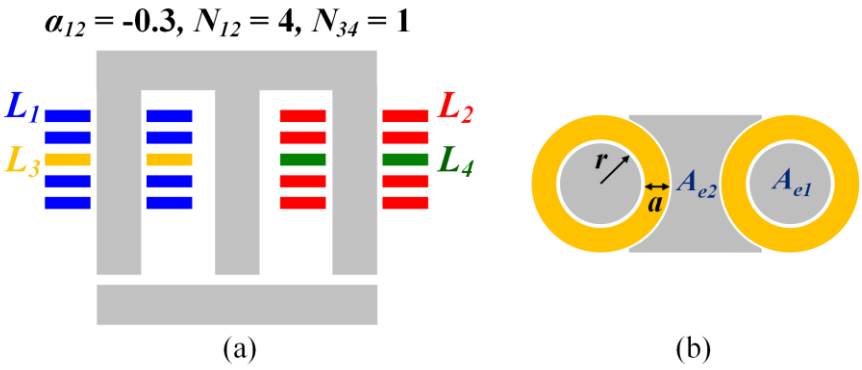


Fig. 4-5. PCB winding coupled inductor designed in [68]. (a) Side view of conceptual inductor drawing, and (b) cross-sectional view of the inductor.

Fig. 4-5 shows the PCB winding coupled inductor built in [69]. Four inductors from L_1 to L_4 are coupled and integrated in one core. Again, note that the phase information is omitted in the notation for the inductors. In Fig. 4-5(a), to simply illustrate the arrangement of the windings, the sideview of the inductor is conceptually expressed where α_{12} is the coupling coefficient between L_1 and L_2. As illustrated, the center leg of the core is a simple bar shape instead of its pot-like shape in the real implementation, as shown in Fig. 4-5(b), where r is the outer leg core radius, a is the winding width, A_{e1} is the outer leg cross-sectional area, and A_{e2} is the center leg cross-sectional area. The pot-like shape is chosen because it can fully utilize the space between the two outer legs, resulting in a shorter distance between the outer legs compared to a rectangular shape. One turn for the return path is placed in the middle layer so that the coupling between L_1 and L_3, and L_2 and L_4 is very strong.

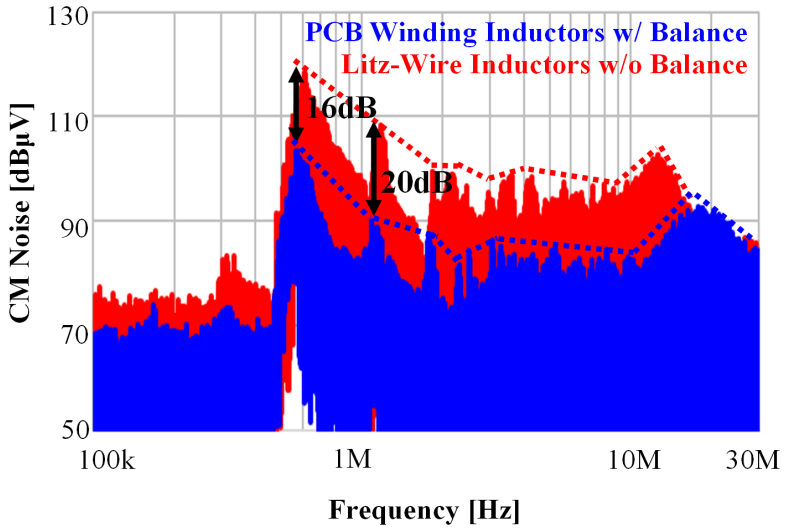


Fig. 4-6. CM noise comparison for a 25 kW ac-dc converter: litz-wire inductor without balance technique (red) and PCB winding inductor with balance technique (blue) [68].

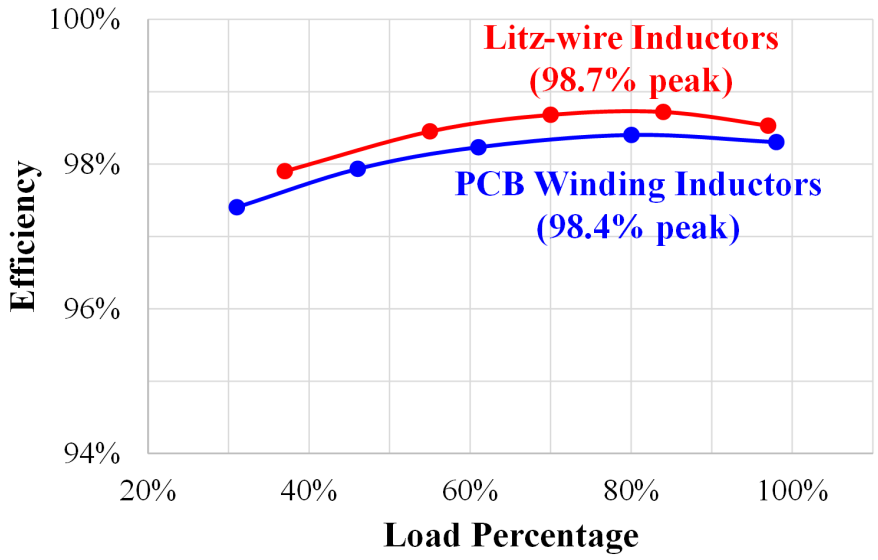


Fig. 4-7. Efficiency comparison for a 25 kW ac-dc converter: litz-wire inductor without balance technique (red) and PCB winding inductor with balance technique (blue) [68].

Fig. 4-6 and Fig. 4-7 represent the comparisons of measured CM noise and efficiency for a 25 kW ac-dc converter: one based on litz-wire inductors without the balance technique, and the other based on the PCB winding coupled inductors with the balance technique presented in [68]. It is obviously seen that the balance technique realized with the PCB winding coupled inductor effectively reduces CM noise to 15 MHz. Yet, the efficiency drops by 0.3 to 0.4 % in comparison with the litz-wire inductor version. It should be pointed out that the measured CM noise in Fig. 4-6 is slightly different from those in [68] even though the same hardware is verified. This is because the EMI test setup is not perfectly the same, resulting in the discrepancy, which is particularly at high frequency regions. This efficiency drop could make the balance technique less attractive for the three-phase system, despite its very good CM noise reduction performance.

The main reason for this is the large inductor loss. In the three-phase ac-dc converter shown in Fig. 4-3, unlike the single-phase PFC converter with the balance technique in [67], the current

in the return path, i_0, contains only small ripples, but no dc bias, so the inductor structure shown in Fig. 4-5(a) has almost no winding interleaving effect. As a result, high magnetomotive forces (MMFs) across windings are established and the winding loss becomes very large. Hence, the objectives of the work in this chapter are as follows: 1) Minimize the winding loss of the PCB winding coupled inductor and make it a similar level to the litz-wire version, and 2) Optimize the inductor design by considering not only the inductor loss, but also the system level benefit of enhancing the converter efficiency while maintaining good CM noise reduction capability.

4.3 Design Considerations for PCB Winding Coupled Inductor for Efficiency Improvement

4.3.1 Inductor Winding Structure

The first consideration is the inductor winding structure. L_1 and L_2 winding interleaving helps to minimize winding loss by reducing MMFs across the windings. Fig. 4-8(b) and Fig. 4-8(c) illustrate the different types of winding structures (without and with the winding interleaving) and the corresponding MMFs at a certain operating point, t_1, in Fig. 4-8(a), where the line cycle and switching cycle waveforms of L_1 current, i_{L1}, L_2 current, i_{L2}, and the return path current, i_0, are shown. It can be inferred from Fig. 4-8(b) that the winding loss is substantial due to the large MMF, especially for the windings at the bottom. In contrast, the MMF of the inductor in Fig. 4-8(c) decreases with the help of one turn from the other inductor. One turn of L_2 is placed in the left leg, and one turn of L_1 is placed in the right leg. This results in smaller winding loss because the smaller MMF reduces the eddy current loss caused by the skin effect and the proximity effect.

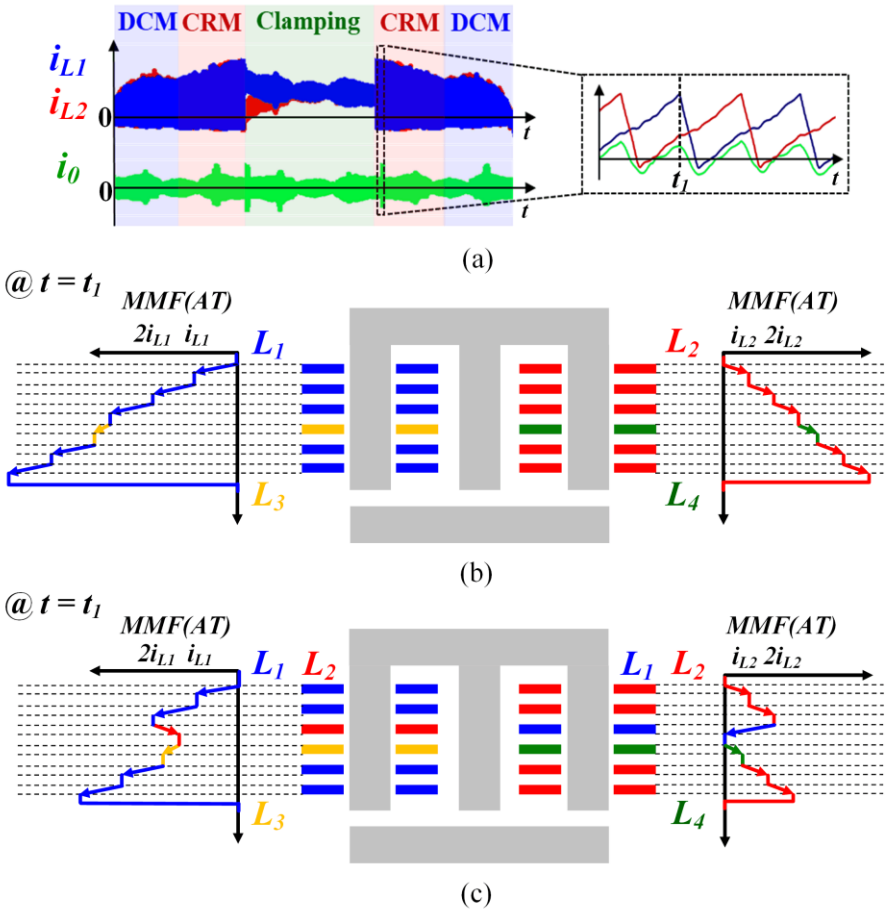


Fig. 4-8. Effect of winding interleaving on MMFs across windings: (a) Indutor current waveforms over the half line cycle. (b) MMFs of non-interleaving winding structure at t_1 instant. (c) MMFs of interleaving winding structure at t_1 instant.

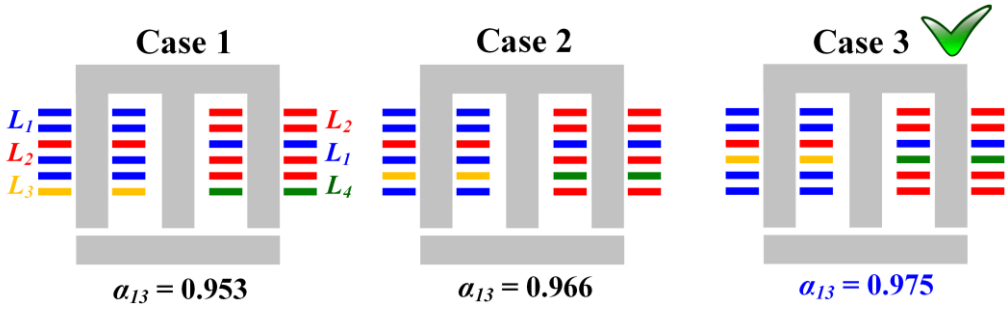


Fig. 4-9. Different winding arrangements of L_3 and L_4 for winding interleaving between L_1 and L_2.

Fig. 4-9 exhibits the diverse options for the L_3 and L_4 winding arrangement for the winding interleaving structure. This determines the coupling coefficient between L_1 and L_3 (or L_2 and L_4), α_{13}. Based on 3D finite element analysis (FEA) simulation, the following is discovered: As L_3 and L_4 windings are placed closer to the middle layer, the coupling becomes stronger, due to less leakage flux generated by L_3 and L_4. Among the candidates in Fig. 4-9, Case 3 is selected for the following design process. As already mentioned, the strong coupling between the main inductors and the extra inductors in the return path is advantageous in terms of better balance for the CM noise reduction, specifically at the MHz level, by alleviating the adverse impact of parasitic components formed between the winding layers.

4.3.2 Coupling Coefficient Selection for L_1 and L_2, α_{12}

The second consideration is the selection of the coupling coefficient between L_1 and L_2, α_{12}. First and foremost, the coupling has an influence on the switching frequency range of the converter, because of the non-linear characteristics of the inductors due to the coupling. Fig. 4-10(a) illustrates the simulated phase A switching frequency over the half line cycle according to different coupling coefficients. As the coupling becomes stronger, the frequency range becomes narrower. This leads to lower average switching frequency over the line cycle, in turn, brings about a decrease in the total device loss of the converter, as shown in Fig. 4-10(b).

One thing to note is that beyond α_{12} = -0.5, the benefit (smaller device loss) of the coupling diminishes, so the choice of coupling coefficient can be narrowed down. This is because the inductor current ripple becomes larger as the coupling becomes stronger which enlarges the conduction loss and the loss across ZCD shunt resistors. Therefore, the selection of the coupling coefficient is restricted between -0.6 and -0.8 from the device loss perspective.

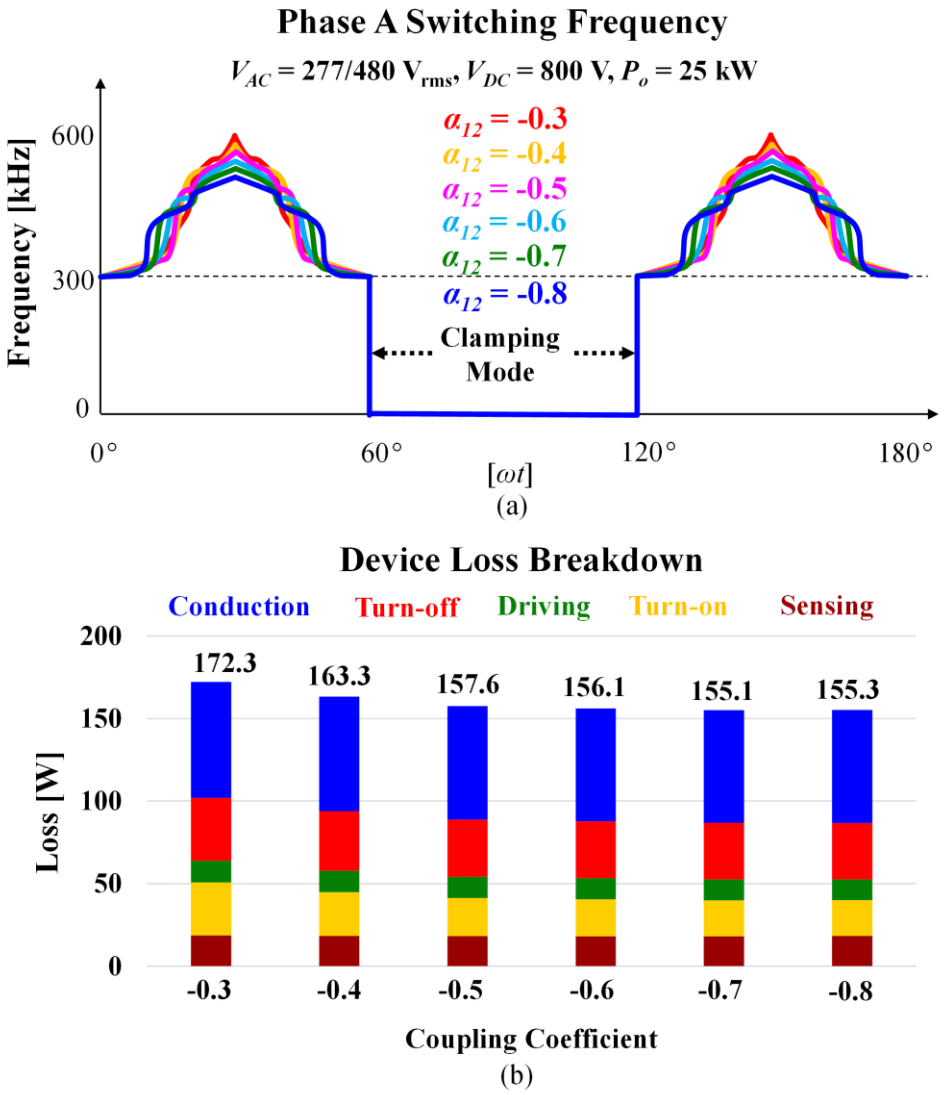


Fig. 4-10. Impact of α12. (a) Switching frequency range. (b) Device loss + ZCD sensing loss.

Another impact of the coupling is the dc magnetic flux in the core legs. Fig. 4-11 shows the reluctance model of the PCB winding coupled inductor and the magnetic flux in each core leg for different coupling coefficients at the operation mode transitions instantly from clamping mode to CRM. This is the zoomed-in area in Fig. 4-8(a), where the flux is the highest over the line cycle. l_{g1} and l_{g2} are the air-gap lengths, R_{g1} and R_{g2} are the reluctances, and A_{e1} and A_{e2} are the cross-sectional areas of the outer and center leg, respectively. The equations for the flux in the outer leg and the center leg are given by:

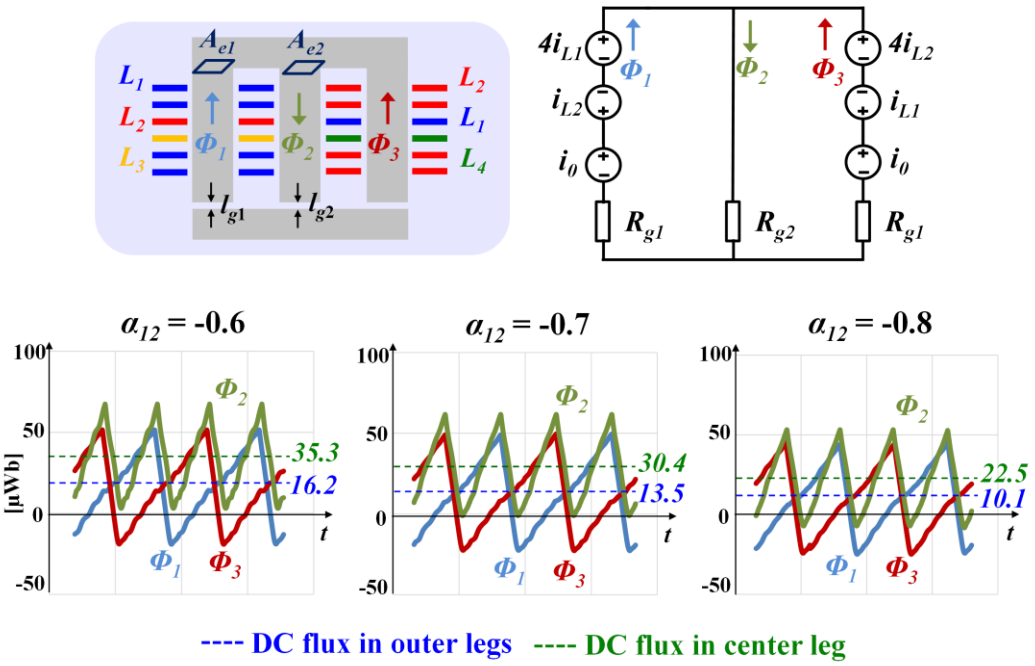


Fig. 4-11. Magnetic circuit and flux in the PCB winding coupled inductor for different coupling coefficients.

$$\Phi_1 = \frac{4i_{L1} - i_{L2} + i_0}{R_{g1} + \frac{R_{g1} \cdot R_{g2}}{R_{g1} + R_{g2}}} - \frac{4i_{L2} - i_{L1} + i_0}{R_{g1} + \frac{R_{g1} \cdot R_{g2}}{R_{g1} + R_{g2}}} \cdot \frac{R_{g2}}{R_{g1} + R_{g2}} \tag{4-5a}$$

$$\Phi_2 = \frac{3i_{L1} + 3i_{L2} + 2i_0}{R_{g1} + \frac{R_{g1} \cdot R_{g2}}{R_{g1} + R_{g2}}} \cdot \frac{R_{g1}}{R_{g1} + R_{g2}} \tag{4-5b}$$

$$\Phi_3 = \frac{4i_{L2} - i_{L1} + i_0}{R_{g1} + \frac{R_{g1} \cdot R_{g2}}{R_{g1} + R_{g2}}} - \frac{4i_{L1} - i_{L2} + i_0}{R_{g1} + \frac{R_{g1} \cdot R_{g2}}{R_{g1} + R_{g2}}} \cdot \frac{R_{g2}}{R_{g1} + R_{g2}} . \tag{4-5c}$$

As the inductors are inversely coupled, the average value of the magnetic flux in one switching cycle (dc magnetic flux) created in each outer leg is cancelled by the one from the other leg. In Fig. 4-11, as the coupling gets stronger, more dc magnetic flux in the outer legs is cancelled out, giving rise to lower dc magnetic flux. On top of that, less dc magnetic flux flows into the center

leg with stronger coupling due to higher reluctance in the center leg. These two factors allow the inference that, with stronger coupling, the core loss can be reduced for the same core volume, because of smaller core loss density by smaller dc magnetic flux. It is worth noting that the ac magnetic flux in each leg remains similar for different coupling coefficients.

Based on the observations so far, it appears it would be better to couple L_1 and L_2 more strongly; however, the choice of the coupling coefficient is restricted by the air-gap length of the core. In the reluctance model in Fig. 4-11, the ratio of R_{g2} to R_{g1} (R_{g2}/R_{g1}) needs to be larger to realize stronger coupling, thus more flux is linked between the outer legs. This gives rise to a larger air-gap in the center leg, l_{g1}, compared to those in the outer legs, l_{g2}, which are expressed as

$$l_{g1} = \mu_0 A_{e1} R_{g1} \tag{4-6a}$$

$$l_{g2} = \mu_0 A_{e2} R_{g2} \tag{4-6b}$$

where μ_0 is the permeability of free space.

Fig. 4-12(a) represents a comparison of the core shapes with different coupling coefficients. It should be noted that the cross-sectional area of the outer leg and the center leg in Fig. 4-12(a) is selected, such that all legs have the same core loss density at the transition instant from clamping mode to CRM. It is worth mentioning that from (4-6) it is possible to have similar air-gap lengths for the outer leg and the center leg by adjusting A_{e1} and A_{e2}, but it could lead to huge discrepancy of the entire core size between different coupling coefficients, making it hard to compare them fairly. It is obvious that the center leg air-gap is too large for α_{12} = -0.8. This is undesirable, as the flux in the center leg air-gap penetrates the windings near the air-gap, as shown in Fig. 4-12(b). Compared to the other two cases, for α_{12} = -0.8, the magnetic flux around the windings close to

the center leg air-gap is very crowded. This fringing effect induces additional eddy current in the windings and causes extra winding loss. For α_{12} = -0.6, although the windings are far away from the air-gap (meaning that it is free from the fringing effect), it could be mechanically less stable compared to the other cases. Thus, α_{12} = -0.7 is preferred and selected for the first round of the design. In the end, the other cases are also studied and compared in terms of inductor loss in the following sub-chapters.

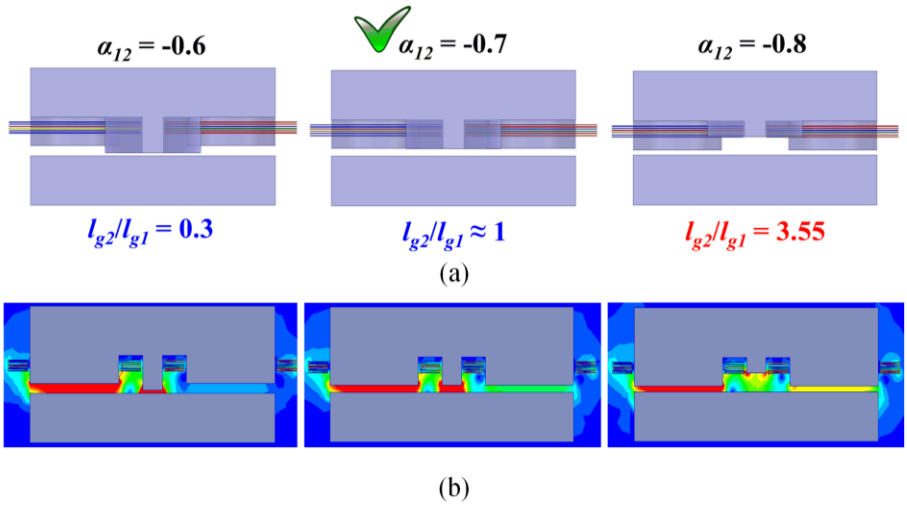


Fig. 4-12. Different winding arrangements of L_3 and L_4 for winding interleaving between L_1 and L_2.

4.3.3 PCB Winding Coupled Inductor Design Process

With the selected inductor winding structure and coupling coefficient, the turns number for L_1 and L_2, N_{12}, needs to be selected. Based on [65], one turn is preferred for better efficacy of the balance technique to reduce the noise source in the CM equivalent circuit. N_{12} is directly related to the winding loss and the core loss. As N_{12} becomes higher, the winding loss becomes higher and dominant, as does the core loss as it becomes lower. Thus, an arbitrary turns number should be chosen for the first round of the design, and the turns number must be swept for the optimal inductor design that has the winding loss and the core loss balanced. Here, N_{12} = 5 is chosen first.

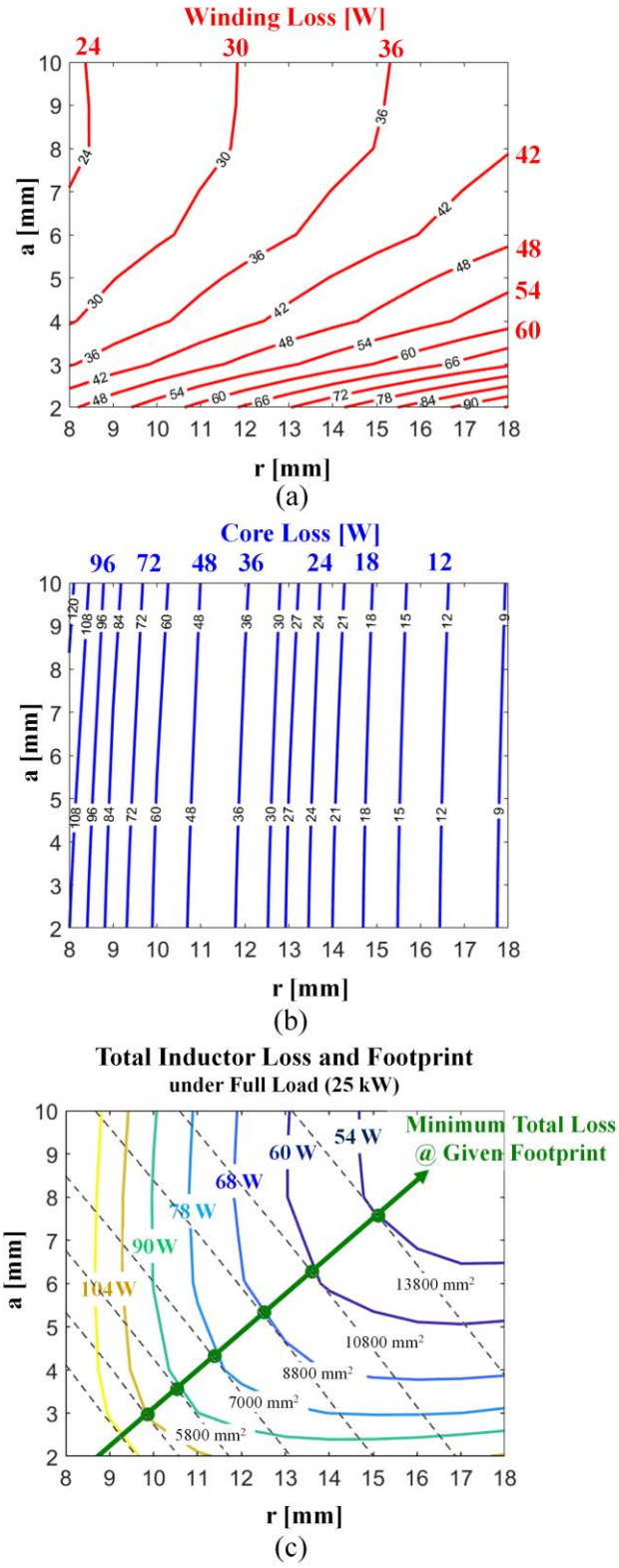


Fig. 4-13. Inductor loss by sweeping the design variables. (a) Wining loss. (b) Core loss. (c) Total loss at 25 kW load condition.

Then, following the design methodology introduced in [70] and [72], the outer leg core radius, *r*, and the winding width, *a*, in Fig. 4-5(a) are selected as independent design variables. Hitachi Metal's ML95S (Mn-Zn soft-ferrite) is used for the core and 3oz copper is used for the windings. By sweeping *r* value and *a* value, the winding loss and the core loss corresponding to each pair of *r* and *a* can be acquired as illustrated in Fig. 4-13(a) and Fig. 4-13(b). The winding loss is obtained by 2D FEA simulation (Ansys Maxwell), and the core loss is calculated based on the equivalent elliptical loop (EEL) method [73], considering the dc bias of each leg's flux. By summing these losses, the total loss contour is plotted in Fig. 4-13(c) with the corresponding footprint. The tangential points of each curve for total loss are connected as the green line to indicate the minimum total loss at the given footprint.

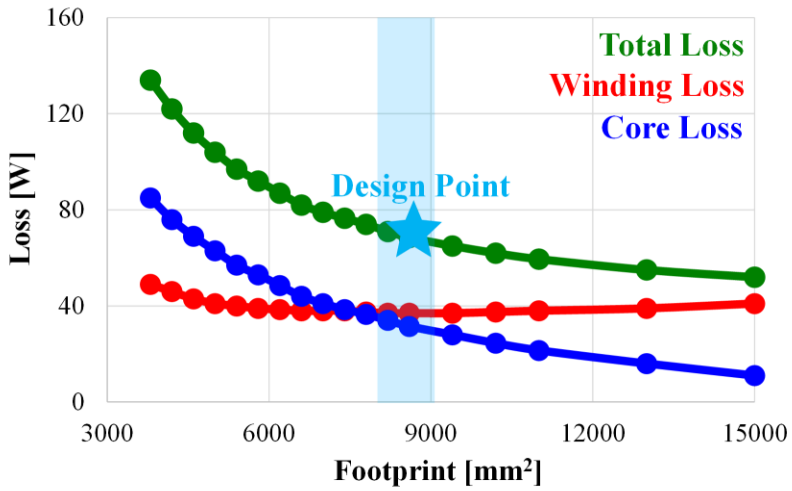


Fig. 4-14. Loss vs. footprint with munimum total loss plot.

In Fig. 4-14, the green line in Fig. 4-13(c) is re-plotted in a loss versus footprint graph. This graph also includes the winding loss and the core loss separately at different footprints. The blue shaded area is the area of interest for the design where the winding loss shows the knee point, and the benefit of a larger footprint (smaller total loss) starts to diminish after this area. In order to

make sure that the first arbitrary choice for α_{12} is the best, the same process for different coupling cases is repeated. In Fig. 4-15, the solid line is the total loss, the dotted line is the winding loss, and the dashed line is the core loss. It can be seen that, in the area of interest, the α_{12} = -0.7 case has the lowest total loss. Finally, a = 5.5 mm and r = 12.5 mm (Footprint = 8600 mm^2) with α_{12} = -0.7 is selected to be the final design point.

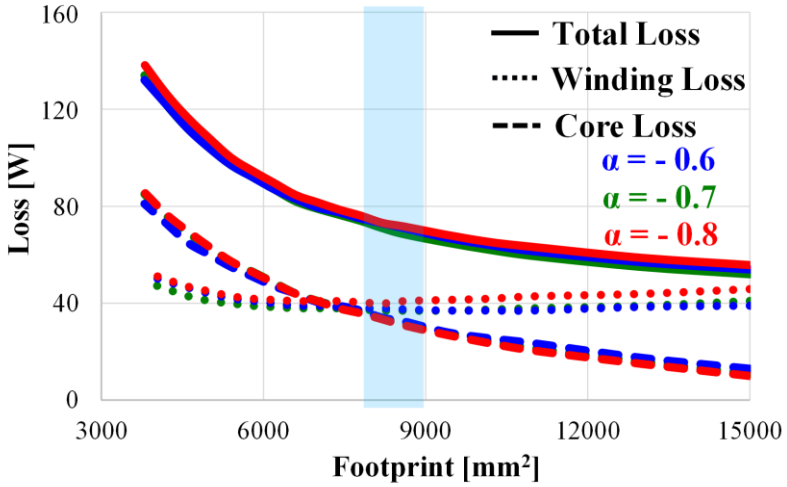
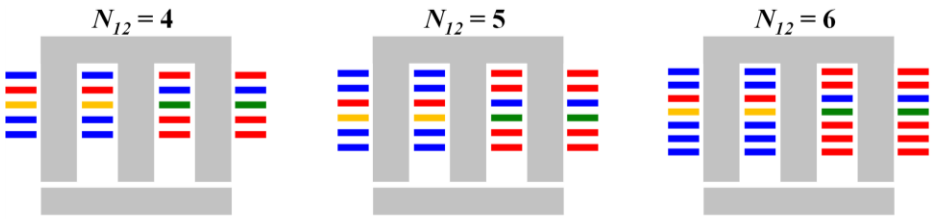


Fig. 4-15. Loss comparison at given footprint for different coupling coefficeints.

The aforementioned design process is repeated for different turns numbers for L_1 and L_2. Fig. 4-16 represents the winding configurations and the inductor loss for three cases (N_{12} = 4, 5, and 6). As the turns number increases, the winding loss increases, and the core loss decreases, and vice versa. Even though the N_{12} = 5 and N_{12} = 6 cases have similar total loss, the latter is not preferable for the PCB winding inductor because it is difficult to dissipate heat from the PCB windings. For the N_{12} = 4 case, the winding loss is very small, but the total loss is too large compared to the other cases, due to the extremely large core loss. Eventually, the N_{12} = 5 case is chosen, as its winding loss and core loss are well balanced.



N_{12}	Winding Loss	Core Loss	Total Loss
4	25 W	76 W	101 W
5	38 W	32 W	70 W
6	52 W	20 W	72 W

Fig. 4-16. Inductor structure and loss breakdown with different turns numbers.

4.3.4 Experimental Results

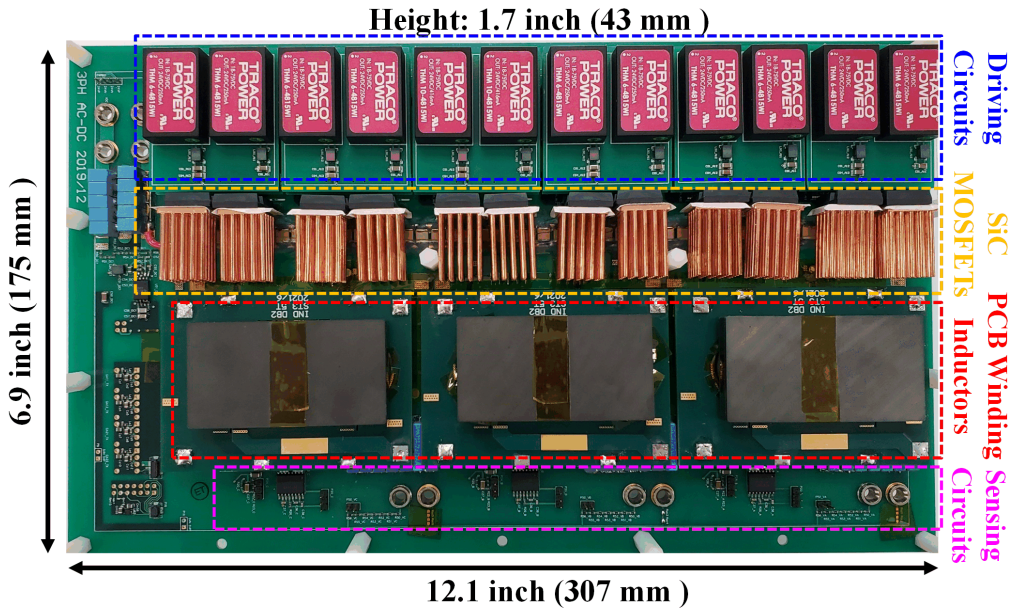


Fig. 4-17. 25 kW bidirectional three-phase ac-dc converter prototype with balace technique implemented with PCB winding coupled inductors.

An SiC-based 25 kW three-phase ac-dc converter prototype is built to verify the performance of the newly designed PCB winding inductor [72]. Fig. 4-17 shows the photograph of the hardware. The power density of the converter power stage is 176 W/in^3. The specifications of the prototype

are organized in TABLE 5. The inductor parameters in TABLE 5 are measured by the Keysight E4990A impedance analyzer.

TABLE 5 SPECTIFICATIONS OF THE PROTOTYPE WITH PCB MAGNETICS

Condition	Value
Maximum Output Power (P_{out})	25 kW
DC Voltage (V_{DC})	800 V
AC Voltage (V_A, V_B, V_C)	277/480 Vrms at 60 Hz
Self-Inductance of Main Inductor (L_1, L_2)	8.64 µH
Inductance of Additional Inductor (L_3, L_4)	0.43 µH
Coupling Coefficient between L_1 and L_2 (α_{12})	-0.7
AC Filter Capacitor (C_f)	1.2 µF
DC Split Capacitor (C_{dcs})	0.1 µF
Minimum Switching Frequency (Fs_min)	300 kHz
SiC MOSFETs	C3M0021120K

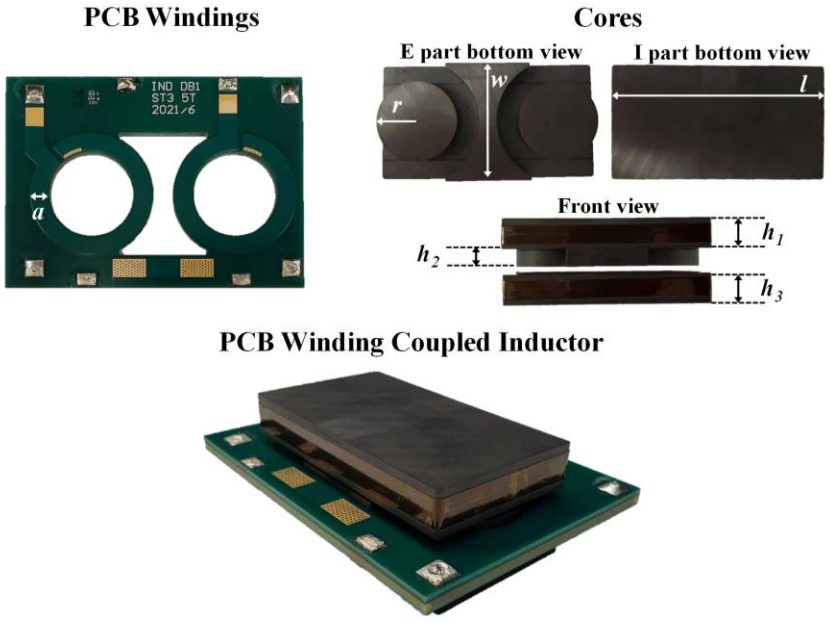


Fig. 4-18. PCB winding coupled inductor teardown and assembled item.

For the PCB winding inductor shown in Fig. 4-18, even though the total number of required layers is six, eight-layer PCBs (two sets of four-layer PCBs) are used, on account of its complicated realization; out of the eight layers, seven layers are utilized. The inductor can be either separately implemented from the converter motherboard or integrated into the motherboard. The dimensional information for the inductor is organized in TABLE 6. One thing to consider for the inductor implementation is to ensure that there is enough distance between the core and the PCB windings to avoid insulation failure and undesired conduction. A 1 mm gap is applied to the inductors (0.5 mm from the winding edge to the PCB cutout, 0.5 mm from the PCB cutout to the core).

TABLE 6 SPECTIFICATIONS OF THE PROTOTYPE WITH PCB MAGNETICS

r	a	w	l	$h_1/h_2/h_3$	Footprint
12.5 mm	5.5 mm	37 mm	68.68 mm	10/5.76/10 mm	2867 mm^2

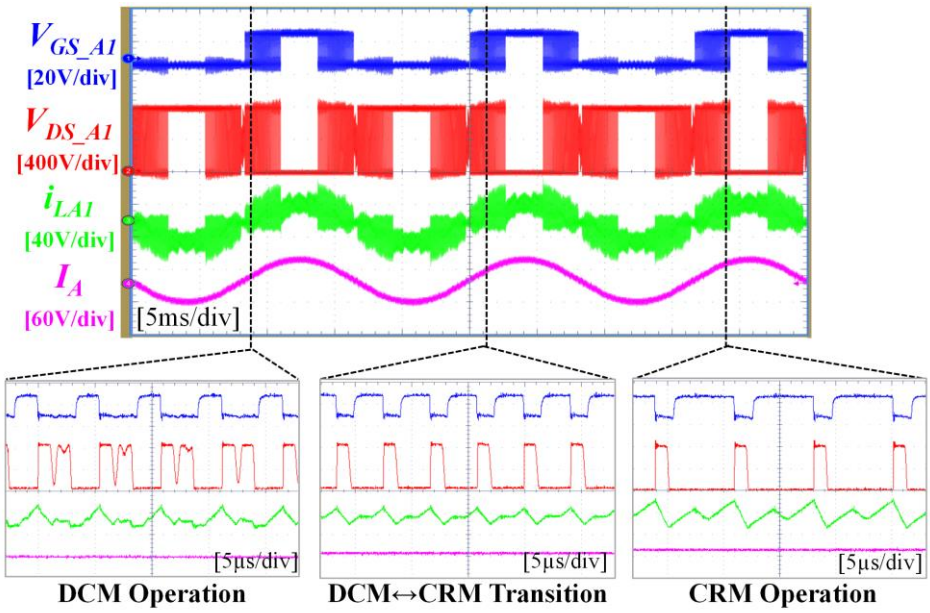


Fig. 4-19. Line cycle and switching cycle waveforms of CRM-based softswitching ac-dc converter with balance technique implemented with PCB winding coupled inductors [72].

The experimental waveforms for the soft-switching three-phase ac-dc converter at 25 kW output power are shown in Fig. 4-19. The figure illustrates phase A top gate-to-source voltage in CH1, V_{GS_A1}, phase A top drain-to-source voltage in CH1, V_{DS_A1}, phase A inductor current in CH1, i_{LA1}, and phase A ac current, I_A. The zoomed-in waveforms at the bottom show the detailed switching cycle behavior. There are three different operation mode: 1) the DCM operation, 2) the CRM operation, and 3) the transition between DCM and CRM. It is observed that ZVS is achieved in the CRM region and the transition instant, and partial ZVS or valley switching is achieved in the DCM region.

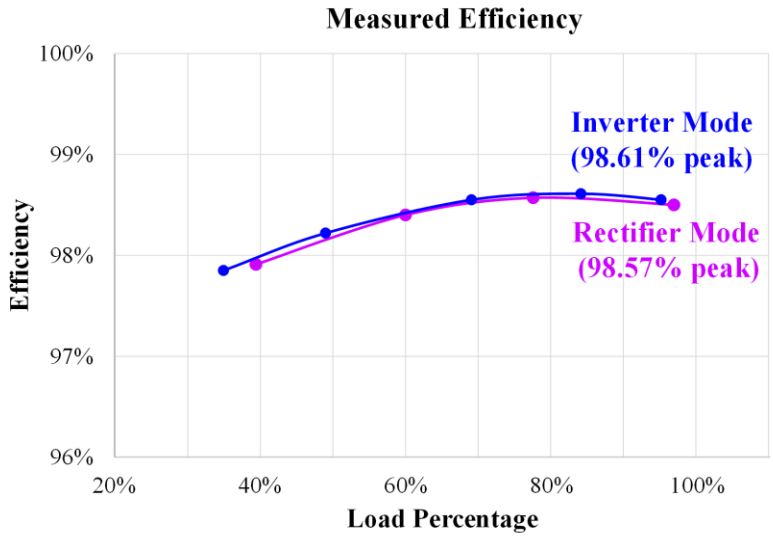


Fig. 4-20. Measured efficiency of the ac-dc converter in inverter mode (blue) and rectifier mode (purple).

Fig. 4-20 shows the measured efficiency of the three-phase ac-dc converter with the PCB winding coupled inductors for the balance technique in inverter mode and rectifier mode. The efficiency in inverter mode is slightly higher than that in rectifier mode. This is because rectifier mode requires extra negative current to fully achieve ZVS, which makes the rms and peak value of the inductor current larger.

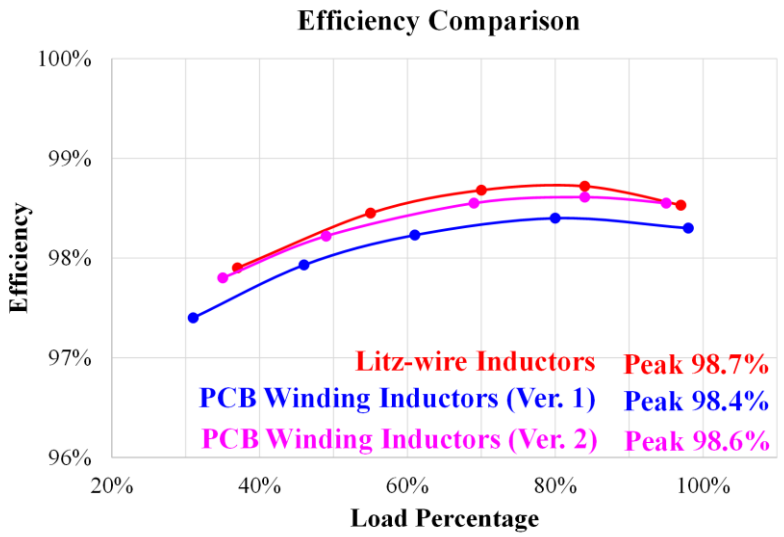


Fig. 4-21. Efficiency comparison with litz-wire inductors (red) and the PCB winding inductors (Ver.1: blue [68] and Ver. 2: pink [72]).

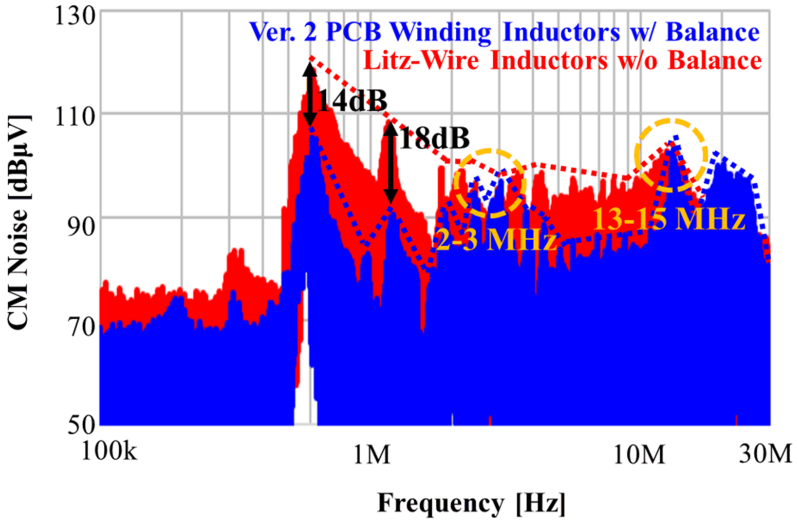


Fig. 4-22. CM noise comparison for a 25 kW ac-dc converter: litz-wire inductor without balance technique (red) and Ver. 2 PCB winding inductor with balance technique (blue) [72].

In Fig. 4-21, the efficiency of the ac-dc converter with the newly designed PCB winding inductors (Ver. 2) is added to the efficiency curves shown in Fig. 4-7 (litz-wire inductors and the PCB winding inductors designed in [68] (Ver. 1)). It is observed that Ver. 2 PCB winding inductors have similar efficiency or slightly lower peak efficiency by approximately 0.1 % compared to the

litz-wire inductor version under assorted load conditions. In comparison with Ver. 1 PCB winding inductors, the efficiency is improved by 0.2 to 0.3 %. However, there is a sacrifice on the CM noise reduction performance. Fig. 4-22 illustrates the measured CM noise with Ver. 2 PCB winding inductors. It is effective up to 10 MHz and reduces CM noise by 14 to 18 dB, but it seems like the new inductors generate more CM noise, especially around 2 to 3 MHz and 13 to 15 MHz in comparison with the CM noise result in Fig. 4-6. It should be mentioned that based on the C_b and C_d value of the EMI test setup, 3.5 pF is used for C_{add1}, but none are used for C_{add2} in order to satisfy the balance condition.

4.4 Impact of Interwinding Capacitance by Winding Interleaving Structure and Improved PCB Winding Coupled Inductor

4.4.1 Observation of Intervention between L_1 and L_2

In order to analyze the root cause of the increased CM noise at those problematic area, experimental results of Ver. 1 inductor and Ver. 2 are carefully scrutinized. Fig. 4-23 compares the switching cycle waveforms between Ver. 1 PCB inductors and Ver. 2 PCB inductors when operating at CRM. The blue one is phase A top switch gate-to-source signal in CH1 and the red one is the corresponding drain-to-source voltage, and the green one is phase A inductor current in CH1. A noticeable difference is that in Ver. 2 high frequency ringings are observed which is not seen in Ver. 1. The frequency of this ringing is around 14 MHz. This coincides exactly with the poor CM noise area shown in Fig. 4-22. More specifically, this ringing happens at switching instants.

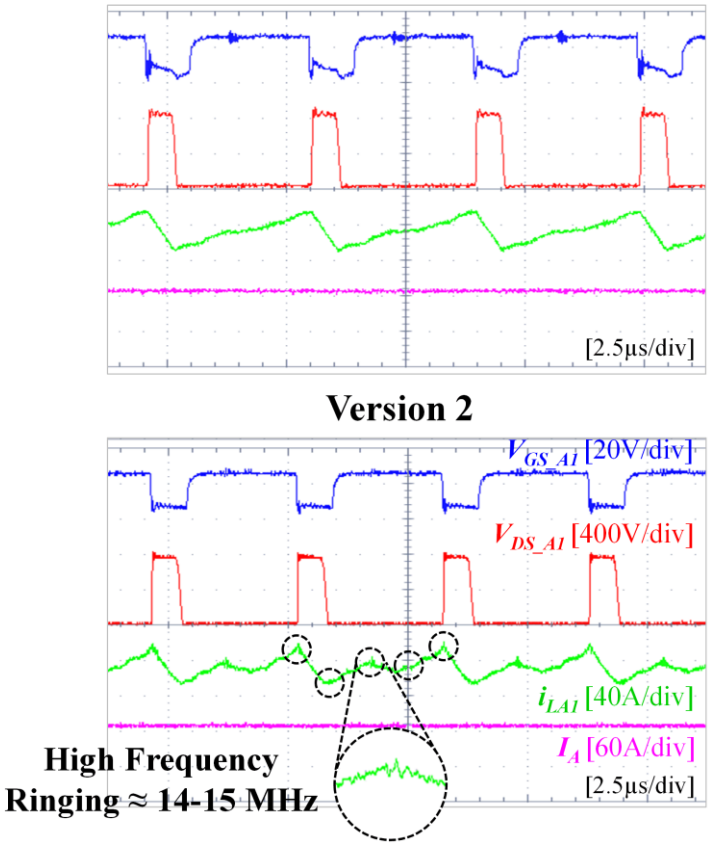


Fig. 4-23. Switching cycle experimental waveforms of Ver. 1 (top) and Ver. 2 (bottom) PCB inductors.

Fig. 4-24 illustrates phase A information (CH1 gate signal, V_{GS_A1}, CH2 gate signal, V_{GS_A2}, and CH1 inductor current, i_{LA1}) and phase C information (CH1 gate signal, V_{GS_C1}, CH2 gate signal, V_{GS_C2}, and CH1 inductor current, i_{LC1}) while phase A operates at CRM and phase C operates at DCM. The high frequency ringing, which is exaggerated in this figure for easier understanding, appear on the CH1 inductor current when the CH1 switch is turned on and off. Interestingly, when the CH2 switch is turned on and off, the ringing appears on the CH1 inductor current as well. This is caused by the interwinding capacitance between L_1 and L_2, C_{12}, brought on by the winding interleaving structure, as depicted in Fig. 4-25. The high frequency ringing in each phase is summed up at the point of LISN and is denoted as $I_{Ringing}$ in Fig. 4-24. These ringing arises six times in one switching cycle (two times at CRM phase turn-off, and two times at DCM phase turn-

off, two times at CRM and DCM phase turn-on due to the synchronized turn-on instant between two phases [23]). Then the frequency of the repetitive ringing is 1.8 to 3 MHz, since the switching frequency at 25 kW output power is from 300 to 500 kHz. This perfectly matches with another poor CM noise area in Fig. 4-22. It can be inferred from these observations that the interwinding capacitance C_{12} is the culprit of the CM noise at both 2 to 3 MHz and 13 to 15 MHz.

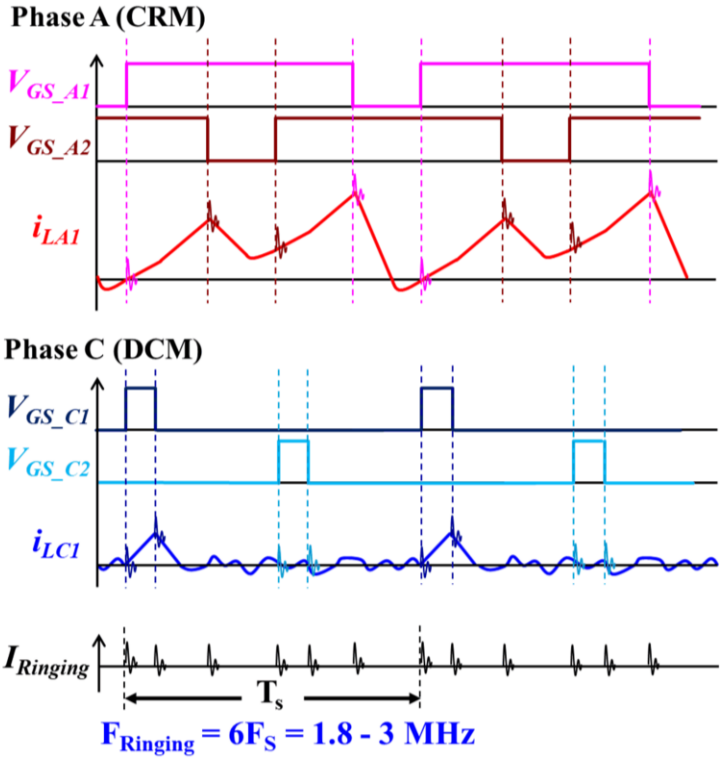


Fig. 4-24. High frequency ringing at switching instants and intervention between L_1 & L_2.

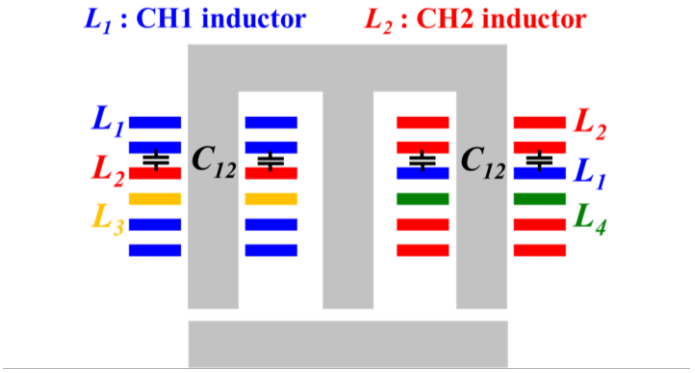


Fig. 4-25. Ver. 2 PCB winding coupled inductor including interwinding capacitance.

4.4.2 Verification of Interwinding Capacitance's Impact

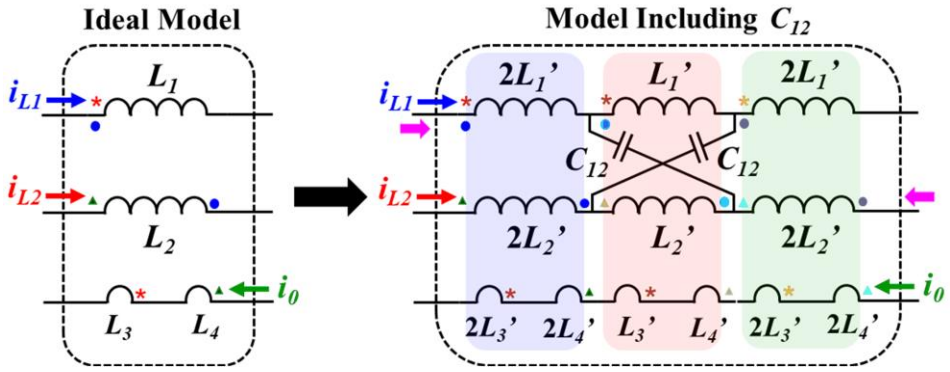


Fig. 4-26. PCB winding coupled inductor models: ideal (left), one including C12 (right).

Based on the observations so far, it is necessary to analyze the impact of the parasitic capacitances on CM noise with an appropriate inductor model [73]. To verify how the interwinding capacitance C_{12} affects the high frequency ringing at the switching instants, a new inductor model including C_{12} is developed. Fig. 4-26 represents the ideal inductor model of the PCB winding coupled inductor (left) and the new inductor model including C_{12} (right). The ideal inductor model, $\boldsymbol{L}$, consists of self-inductances and mutual-inductances as given by

$$\boldsymbol{L} = \begin{bmatrix} L_1 & M_{12} & M_{13} & M_{14} \\ M_{12} & L_2 & M_{14} & M_{13} \\ M_{13} & M_{14} & L_3 & M_{34} \\ M_{14} & M_{13} & M_{34} & L_4 \end{bmatrix} \tag{4-7}$$

where L_1, L_2, L_3, and L_4 are the self-inductances of each inductor, and M_{12}, M_{13}, M_{14}, and M_{34} are the mutual-inductances between the inductors. The subscript indicates the relationship between the inductors; for instance, M_{13} is the mutual inductance between L_1 and L_3. Coupling between the inductors is marked as dots, stars, and triangles in the model. The ideal inductor is split into three parts (blue, red, and green shaded boxes) to locate the interwinding capacitance. The blue box represents the upper two layers (two turns for L_1 and L_2) of the PCB winding coupled inductor in

Fig. 4-25. The red box represents the third layer (interleaving turn for L_1 and L_2). The green box represents the bottom two layers (two turns for L_1 and L_2). The new inductance matrix, $\boldsymbol{L}'$, in this model is expressed as:

$$\boldsymbol{L}' = \begin{bmatrix} L_1' & M_{12}' & M_{13}' & M_{14}' \\ M_{12}' & L_2' & M_{23}' & M_{24}' \\ M_{13}' & M_{23}' & L_3' & M_{34}' \\ M_{14}' & M_{24}' & M_{34}' & L_4' \end{bmatrix} = \frac{1}{5}\boldsymbol{L}. \tag{4-8}$$

Then, one C_{12} is placed between the second layer of L_1 and the third layer of L_2, and the other C_{12} is placed between the second layer of L_2 and the third layer of L_1, based on the physical structure of the PCB winding coupled inductor.

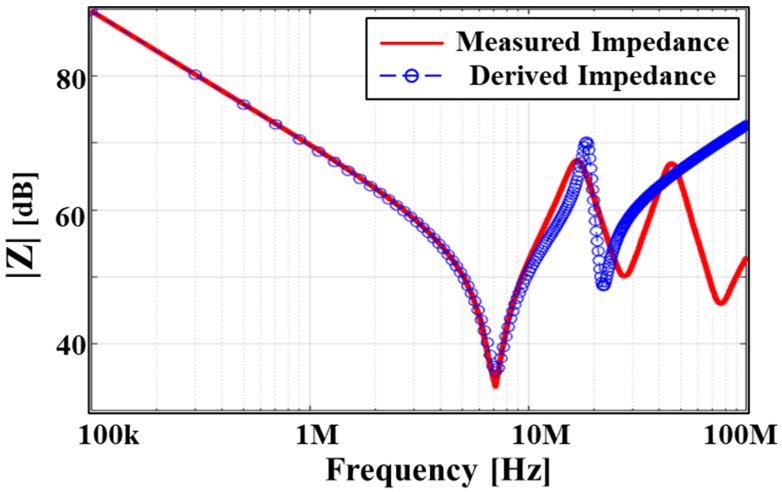


Fig. 4-27. Measured impedance vs. derived impedance.

To evaluate the validity of the new inductor model, the inductor's impedance between the two nodes, indicated as pink arrows in Fig. 4-26 is derived. In this impedance path, all C_{12} in the model are included and it is expressed as:

$$Z(s) = \frac{1}{s(2C_{12} + (2C_{12}^{\,2}L_{12}' - 2C_{12}^{\,2}M_{12}')s^2)} + 4L_{12}'s + \frac{(L_{12}' - M_{12}')s}{1 + (C_{12}L_{12}' - C_{12}M_{12}')s^2} \tag{4-9}$$

where L_{12}' is equivalent to L_1' and L_2' on the assumption that L_1' and L_2' are identical. The derived impedance is compared with the measured impedance in Fig. 4-27. The comparison shows that the derived impedance is completely matched below 10 MHz, and has a very similar characteristic up to 40 MHz with the measured impedance. It should be noted that the new inductor model does not reflect the coupling between L_1 and L_3, and L_2 and L_4 perfectly because L_3 and L_4 are made of one layer in the real implementation. The prime focus of this work is to scrutinize how C_{12} plays a role as a medium of the intervention between L_1 and L_2; thus, the complete coupling aspect of L_3 and L_4 is not discussed.

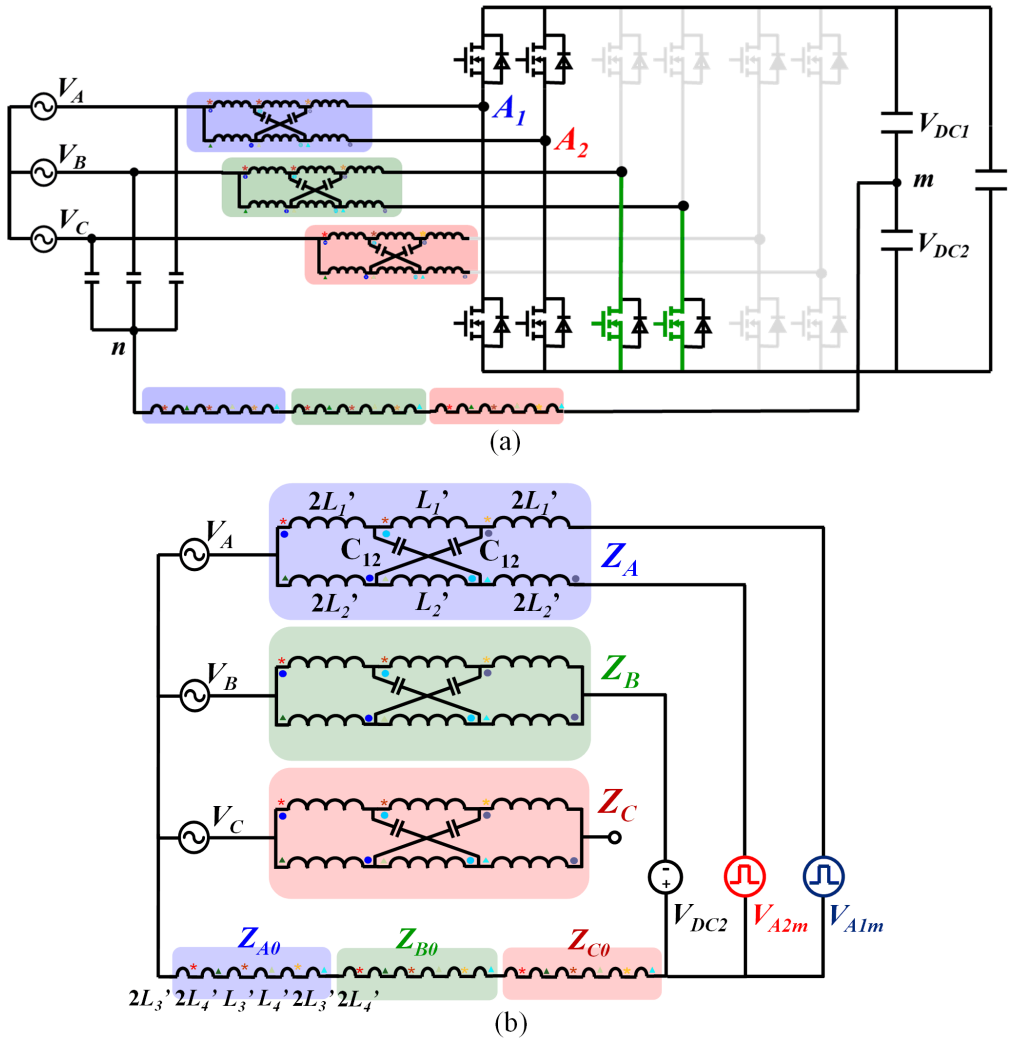


Fig. 4-28. Equivalent circuits with proposed inductor model.

Fig. 4-28(a) shows the CRM-based soft-switching three-phase ac-dc converter with the new inductor models (phase A: blue, phase B: green, phase C: red) at 60° over the line cycle where phase A is at CRM, phase B is in clamping mode, and phase C is at DCM. Phase B is clamped to the negative dc rail. There are no switching actions in phase C, since phase C ac voltage and current are almost zero at this operating point. Now that only phase A switches are running, voltages across the switching nodes in phase A, A_1 and A_2, and the mid-point of the dc capacitors, m, are pulsating according to the phase A switching status. These pulsating voltages can be replaced with high frequency voltage sources, V_{A1m} and V_{A2m}. In this way, the circuit in Fig. 4-28(a) is simplified to that shown in Fig. 4-28(b). The dc split capacitors are also replaced with constant voltage sources. By analyzing this circuit, the frequency of the ringing at the switching instants can be predicted. This is helpful to adjust the frequency of the ringing by controlling C_{12} in the inductor design and move it far beyond 30 MHz, where no EMC standards are applied.

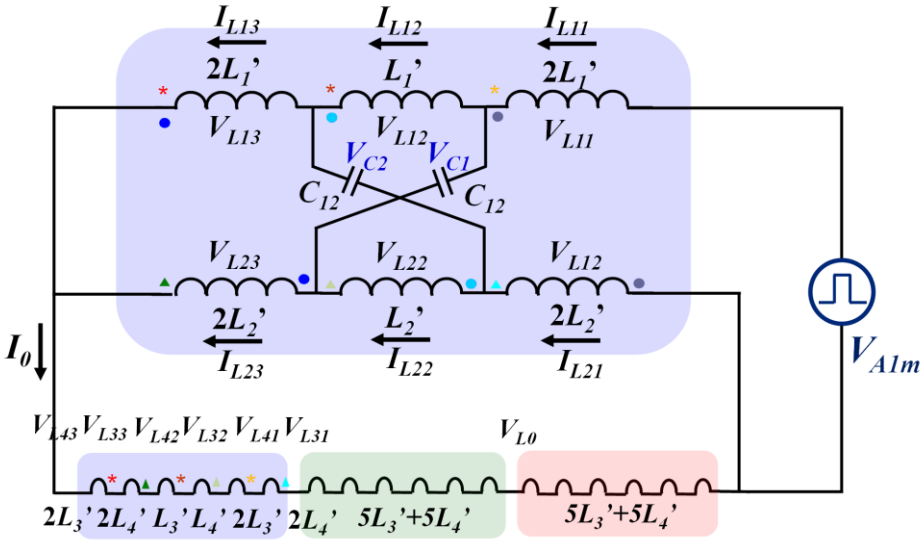


Fig. 4-29. Simplified equvalent circuit with only V_{A1m}.

Fig. 4-28(b) can be further simplified by the following steps. First, all the low frequency and DC voltage sources (V_A, V_B, V_C, and V_{DC2}) are shorted. The inductor branch in phase C, Z_C, is

ignored as it is an open circuit. Now that Z_C is ignored, the coupling between Z_C and Z_{C0} is invalid. Then, only the self-inductance in Z_{C0} is left. The next step is to short the pulsating voltage source in CH2, V_{A2m}, to see only the impact of V_{A1m}. Finally, Z_B is ignored because the impedance of Z_B is much higher than the sum of Z_{A0}, Z_{B0}, and Z_{C0} in the return path. The coupling between Z_B and Z_{B0} is no longer valid as well, and only self-inductance in Z_{B0} remains. Fig. 4-29 is the final equivalent circuit only with V_{A1m}. To imitate the ac-dc converter's switching actions of phase A in CH1, V_{A1m} is excited as a square-wave with 50 % duty cycle.

The simplified equivalent circuit in Fig. 4-29 can be solved by the equations below with Kirchhoff's Voltage and Current Laws:

$$V_{A1m} = V_{L11} + V_{L12} + V_{L13} + V_{L0} + V_{L43} + V_{L33} + V_{L42} + V_{L32} + V_{L41} + V_{L31}. \quad (4\text{-}10)$$

$$0 = V_{L21} + V_{L22} + V_{L23} + V_{L0} + V_{L43} + V_{L33} + V_{L42} + V_{L32} + V_{L41} + V_{L31}. \quad (4\text{-}11)$$

$$V_{C1} = V_{L12} + V_{L13} - V_{L23} \quad (4\text{-}12a)$$

$$V_{C1} = V_{L12} + V_{L13} + V_{L0} + V_{L43} + V_{L33} + V_{L42} + V_{L32} + V_{L41} + V_{L31} + V_{L21} + V_{L22} \quad (4\text{-}12b)$$

$$V_{C1} = I_{C1} / (C_{12} s). \quad (4\text{-}12c)$$

$$V_{C2} = V_{L13} - V_{L32} - V_{L22}. \quad (4\text{-}13a)$$

$$V_{C2} = V_{L13} + V_{L0} + V_{L43} + V_{L33} + V_{L42} + V_{L32} + V_{L41} + V_{L31} + V_{L21} \quad (4\text{-}13b)$$

$$V_{C1} = I_{C2} / (C_{12} s). \quad (4\text{-}13c)$$

$$I_{C1} = I_{L11} - I_{L12}. \quad (4\text{-}14)$$

$$I_{C2} = I_{L12} - I_{L13} = I_{L22} - I_{L21}. \quad (4\text{-}15)$$

$$I_0 = I_{L13} + I_{L23} = I_{L11} + I_{L21}. \quad (4\text{-}16)$$

The terms of inductor voltage appear in (4-10) to (4-13) are expresses as

$$V_{L11} = 2L_1'sI_{L11} + 2M_{12}'sI_{L21} + 2(M_{13}' + M_{14}')sI_0 . \quad (4\text{-}17)$$

$$V_{L21} = 2L_2'sI_{L21} + 2M_{12}'sI_{L11} + 2(M_{13}' + M_{14}')sI_0 . \quad (4\text{-}18)$$

$$V_{L12} = L_1'sI_{L12} + M_{12}'sI_{L22} + (M_{13}' + M_{14}')sI_0 . \quad (4\text{-}19)$$

$$V_{L22} = L_2'sI_{L22} + M_{12}'sI_{L12} + (M_{13}' + M_{14}')sI_0 . \quad (4\text{-}20)$$

$$V_{L13} = L_1'sI_{L13} + M_{12}'sI_{L23} + (M_{13}' + M_{14}')sI_0 . \quad (4\text{-}21)$$

$$V_{L23} = L_2'sI_{L23} + M_{12}'sI_{L13} + (M_{13}' + M_{14}')sI_0 . \quad (4\text{-}22)$$

$$V_{L23} = L_2'sI_{L23} + M_{12}'sI_{L13} + (M_{13}' + M_{14}')sI_0 . \quad (4\text{-}23)$$

$$V_{L31} = 2(L_3'sI_0 + M_{13}'sI_{L11} + M_{14}'sI_{L21} + M_{34}'sI_0) . \quad (4\text{-}24)$$

$$V_{L41} = 2(L_4'sI_0 + M_{14}'sI_{L11} + M_{13}'sI_{L21} + M_{34}'sI_0) . \quad (4\text{-}25)$$

$$V_{L32} = L_3'sI_0 + M_{13}'sI_{L12} + M_{14}'sI_{L22} + M_{34}'sI_0 . \quad (4\text{-}26)$$

$$V_{L42} = L_4'sI_0 + M_{13}'sI_{L12} + M_{14}'sI_{L22} + M_{34}'sI_0 . \quad (4\text{-}27)$$

$$V_{L33} = 2(L_3'sI_0 + M_{13}'sI_{L13} + M_{14}'sI_{L23} + M_{34}'sI_0) . \quad (4\text{-}28)$$

$$V_{L43} = 2(L_4'sI_0 + M_{14}'sI_{L13} + M_{13}'sI_{L23} + M_{34}'sI_0) . \quad (4\text{-}29)$$

$$V_{L0} = 10L_3'sI_0 + 10L_4'sI_0 . \quad (4\text{-}30)$$

By substituting (4-17) to (4-30) into (4-10) to (4-16), the characteristic equation for I_{L11} and V_{C1} is found to be

$$k_5 s^5 + k_3 s^3 + k_1 s = ks(s^2 + \omega_1^2)(s^2 + \omega_2^2) = 0 \,. \tag{4-31}$$

The two double roots in (4-31) represent the resonant frequencies of the circuit. Fig. 4-30 is the simulation waveforms of V_{A1m}, an inductor current, I_{L11}, and an interwinding capacitor voltage, V_{C1}. It is clearly seen that there is high frequency ringing at the inductor current and the capacitor voltage. The frequency of the ringing is very similar to that observed in the experiment. The double roots in (4-31) are also observed in the frequency spectrum of V_{C1} in Fig. 4-30. Therefore, based on the analysis, it can be concluded that the interwinding capacitance, C_{12}, causes the high frequency ringing at the switching instants and the intervention between L_1 and L_2.

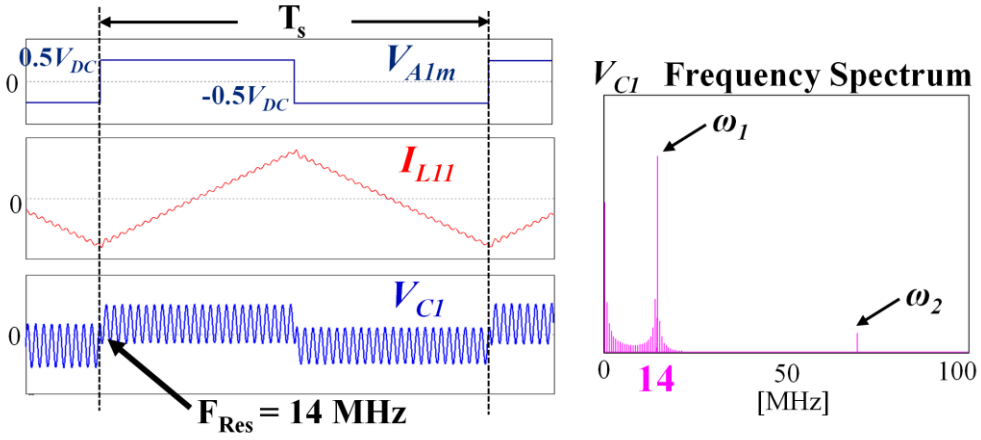


Fig. 4-30. Simulation results of the simplified equivalent circuit with only V_{A1m}: creation of high frequency ringing in inductoro current and C_{12} at switching instant.

4.4.3 Improved PCB Winding Coupled Inductor

The solution to tackle the high frequency ringing issue is to reduce the interwinding capacitance. An improved PCB winding coupled inductor (Ver. 3) is introduced in Fig. 4-31 [74].

One more layer for the return path is inserted between L_1 and L_2. Then, the return path layers are connected in parallel to keep one turn. In this way, the winding interleaving layer is surrounded by the return path layers, leading to almost zero C_{12}. Meanwhile, this structure still maintains the winding interleaving to minimize the MMFs and the winding loss. Theoretically, the turns number for L_1, L_2, L_3, and L_4 in the improved inductor design does not change, so the inductor parameters are supposed to be the same as that of the Ver. 2 PCB inductor.

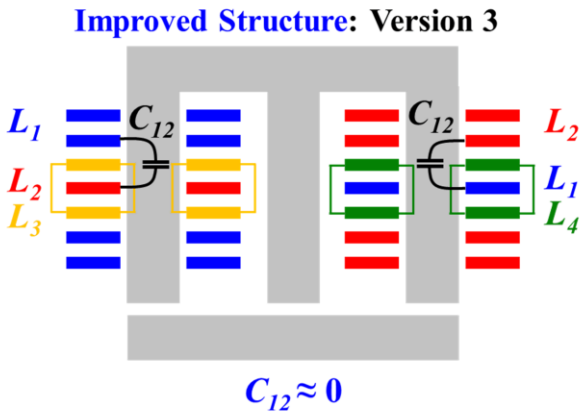


Fig. 4-31. Improved PCB winding coupled inductor minimizing C_{12}.

To evaluate the performance of the improved inductor, Ver. 3 PCB inductors are built and installed in the prototype, shown in Fig. 4-17. For fair comparison, the remaining parts of the prototype are kept the same. Regarding the inductor implementation, the eight-layer PCBs (two sets of four-layer PCBs) are still used, which are the same as the Ver. 2 PCB inductor. Unlike the Ver. 2 PCB inductor, all the layers are utilized because one more layer is inserted in the Ver. 3 PCB inductor. Since the thickness of the PCB winding remains equal, the core used for the Ver. 2 PCB inductor can also be used directly. TABLE 7 shows the measured parameters of the Ver. 3 PCB inductor. The difference in the parameters between Ver. 2 and Ver. 3 is negligible.

TABLE 7 MEASURED INDUCTANCE OF IMPROVED INDUCTOR (VERISON 3)

Parameters	Value
Self-Inductance of Main Inductor (L_1, L_2)	8.61 µH
Inductance of Additional Inductor (L_3, L_4)	0.44 µH
Mutual Inductance between L_1 and L_2 (M_{12})	-6.0 µH
Mutual Inductance between L_1 and L_3 (M_{13})	1.9 µH
Mutual Inductance between L_3 and L_4 (M_{34})	-0.13 µH

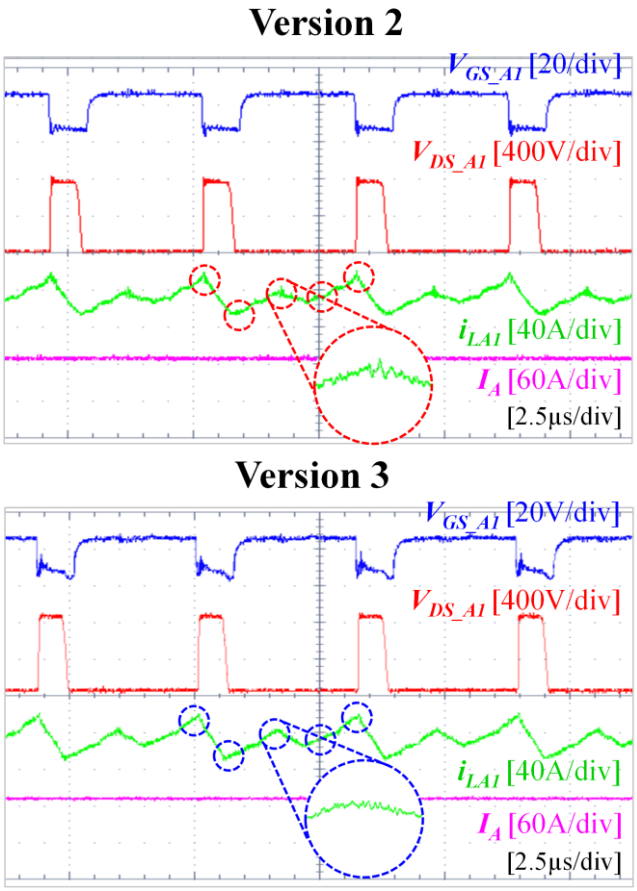


Fig. 4-32. Comparison of switching cycle experimental waveforms of Ver. 2 (top) and Ver. 3 (bottom) inductors: suppresion of high frequency ringings.

Fig. 4-32 compares switching cycle experimental waveforms between the Ver. 2 PCB inductors and Ver. 3 PCB inductors when operating at CRM. With the improved inductor structure,

the high frequency ringing at switching instants are suppressed substantially. Additionally, the frequency of the ringing moves beyond 40 MHz, which is not considered in the EMC requirements.

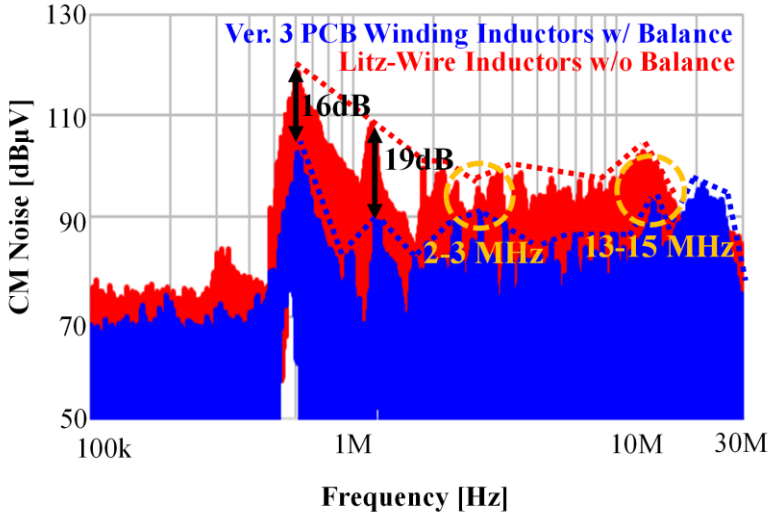


Fig. 4-33. CM noise comparison for a 25-kW ac–dc converter: litz-wire inductor without balance technique (red) and Ver. 3 PCB winding inductor with balance technique (blue).

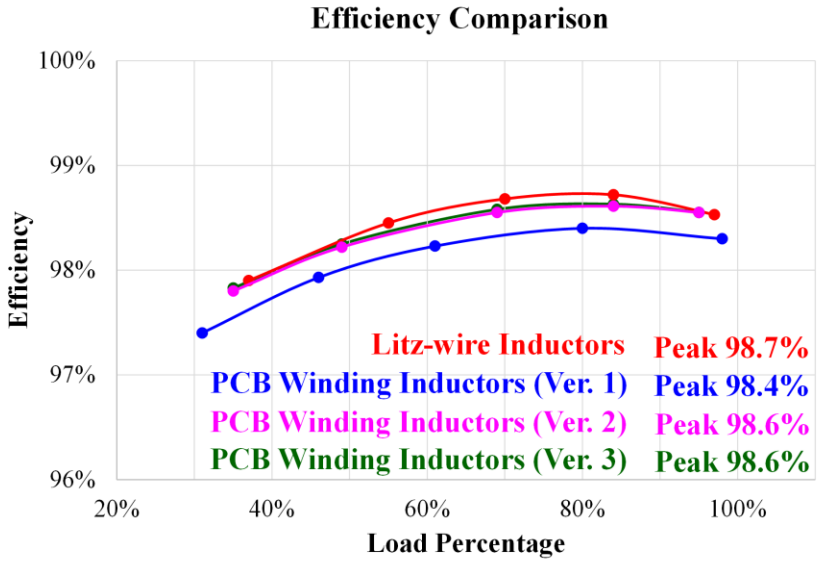


Fig. 4-34. Efficiency comparison with litz-wire inductors (blue) and the PCB winding inductors (Ver.1: blue[68], Ver. 2: pink[72], and Ver. 3: Green[74]).

The reduced ringing improves the CM noise performance of the converter, as shown in Fig. 4-33. The CM noise peaking at the problematic areas with the Ver. 2 inductors, 2 to 3 MHz and 13 to 15 MHz, is reduced by 6 to 9 dB. The efficiency of the ac-dc converter using Ver. 3 PCB inductors is similar to using Ver. 2 PCB inductors. It is somewhat higher, as illustrated in Fig. 4-34, but the difference is insignificant.

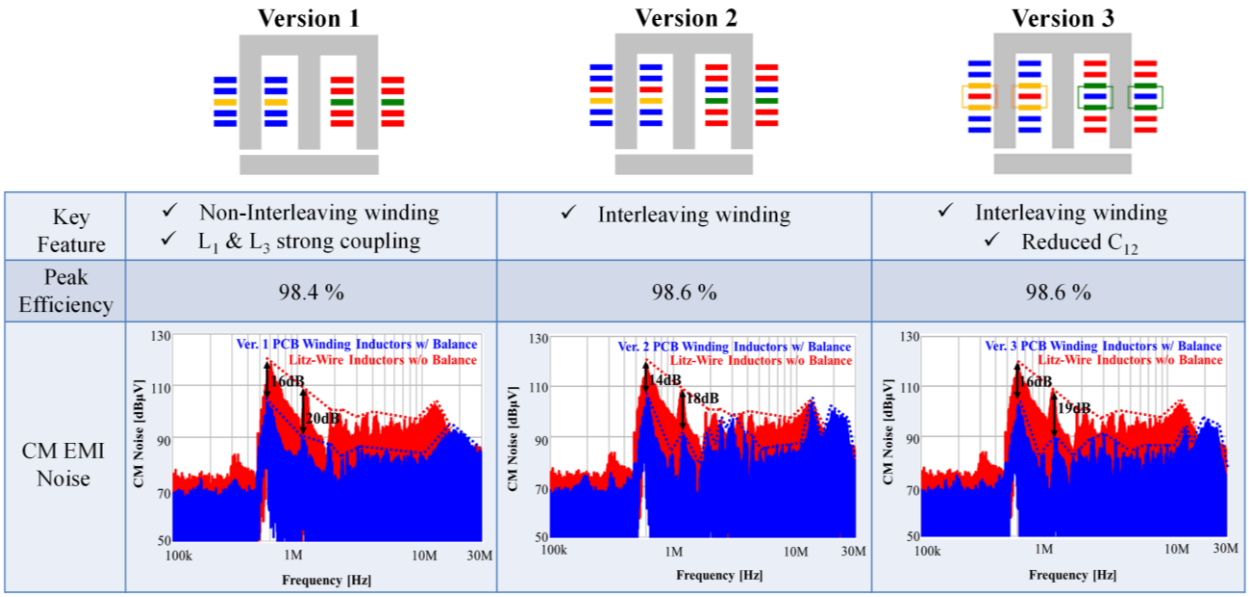


Fig. 4-35. Summary of studies on PCB winding coupled inductor design for soft-switching three-phase ac-dc converter with balance technique.

To summarize, different types of PCB winding coupled inductors for a three-phase ac-dc converter with the balance technique are studied as shown in Fig. 4-35. The non-interleaving structure, Ver. 1 [68], features the best CM noise reduction performance with strong coupling between L_1 and L_3, but efficiency is a little low due to the large winding loss. The winding interleaving structure, Ver. 2 [72], enhances the efficiency, but creates more CM noise at certain frequencies owing to the interwinding capacitance, C_{12}. By reducing C_{12} [74], Ver. 3 has high efficiency, and good CM noise reduction is achieved. It is not as effective in noise redcution as Ver. 1, but it could be regarded as a reasonable compromise for higher efficiency. It is concluded

that the design of the PCB winding coupled inductor for a three-phase ac-dc converter with balance technique is a tradeoff between the CM noise reduction and efficiency.

4.4.4 EMI Filter Design

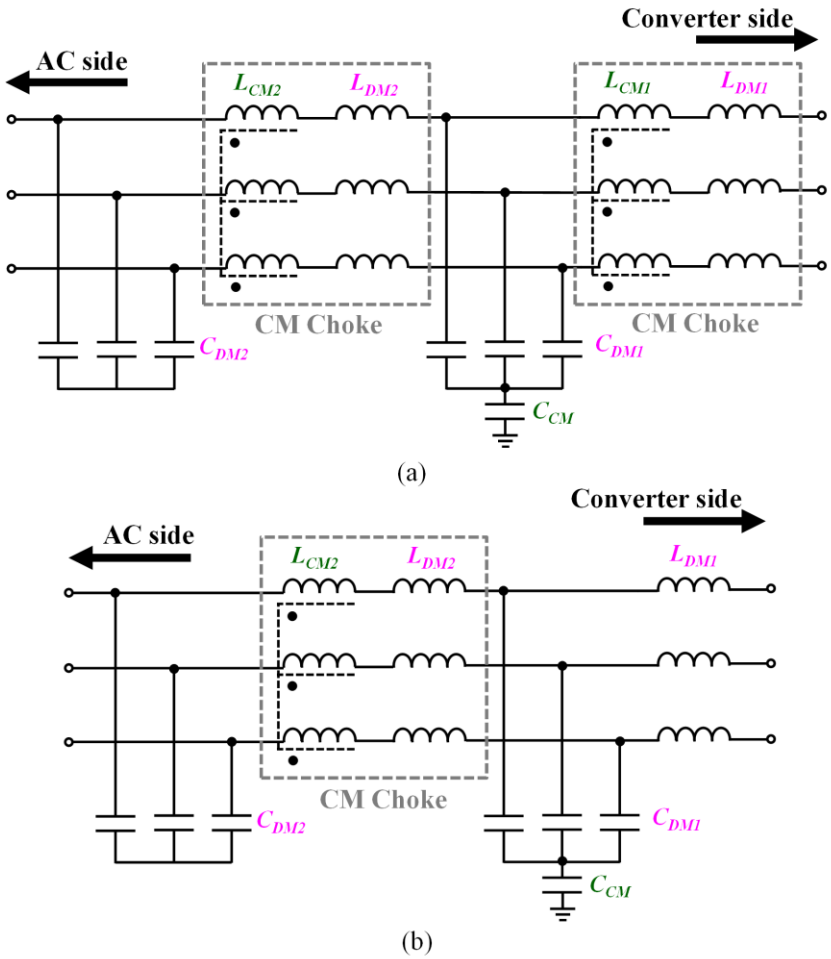


Fig. 4-36. EMI filter circuit diagram. (a) Litz-wire inductor version without balance technique. (b) PCB winding inductor version with balance technique.

Finally, EMI filters for the litz-wire inductor version and Ver. 3 PCB winding inductor version are built to satisfy the EMC requirement, and compared from the size point of view to see how much size reduction can be achievable with the balance technique. EMI filter design methodology introduced in [75], [76] was chosen as a design guideline. The target EMC requirement is FCC

Part 15 Class B, since the ac-dc converter was intended for industrial applications. The EMI filters are designed in the way that DM and CM noise element are suppressed to be at least 6 dB smaller than the requirement. In this way, the total EMI noise (DM + CM) level does not exceed the requirement. Fig. 4-36 presents the designed EMI filter structure. The parameters of the EMI filters are tabulated in TABLE 8.

TABLE 8 EMI FILTER PARAMETERS

Parameters	EMI filter in 4-36 (a)	EMI filter in 4-36 (b)
L_{DM1}	7 μH	6.8 μH
L_{CM1}	0.45 mH	-
C_{DM1}	1.2 μF	1.2 μF
C_{CM}	10 nF	15 nF
L_{DM2}	7 μH	7 μH
L_{CM2}	0.45 mH	0.45 mH
C_{DM2}	0.1 μF	0.1 μF

First, the EMI filter in Fig. 4-36(a) is designed. Based on the impedance mismatch concept [77], the filter's last stage impedance is chosen to be much smaller than LISN's side impedance. For example, the DM filter's last stage impedance is C_{DM2} at 600 kHz, where the noise peak appears is compared with the LISN's impedance as

$$\left|Z_{CDM2}\right| = \frac{1}{2\pi \cdot 600 \cdot 10^{3} \cdot 100 \cdot 10^{-9}} = 2.65\Omega \ll 50\Omega(\text{LISN}) . \tag{4-32}$$

Since (4-32) meets the impedance mismatch concept, the last stage of the DM filter is correctly designed. For the CM filter's last stage, if the C_{CM} was placed at the last stage, which is normally

in a range of 10 nF to 30 nF due to the earth leakage current requirement for safety, the impedance mismatch concept would not be satisfied as

$$|Z_{CCM}| = \frac{1}{2\pi \cdot 600 \cdot 10^{3} \cdot 10 \cdot 10^{-9}} = 26.5\Omega > \frac{50}{3}\Omega(\text{LISN}) . \tag{4-33}$$

Therefore, in order to make the last stage's impedance larger, an inductor is selected for the CM filter's last stage.

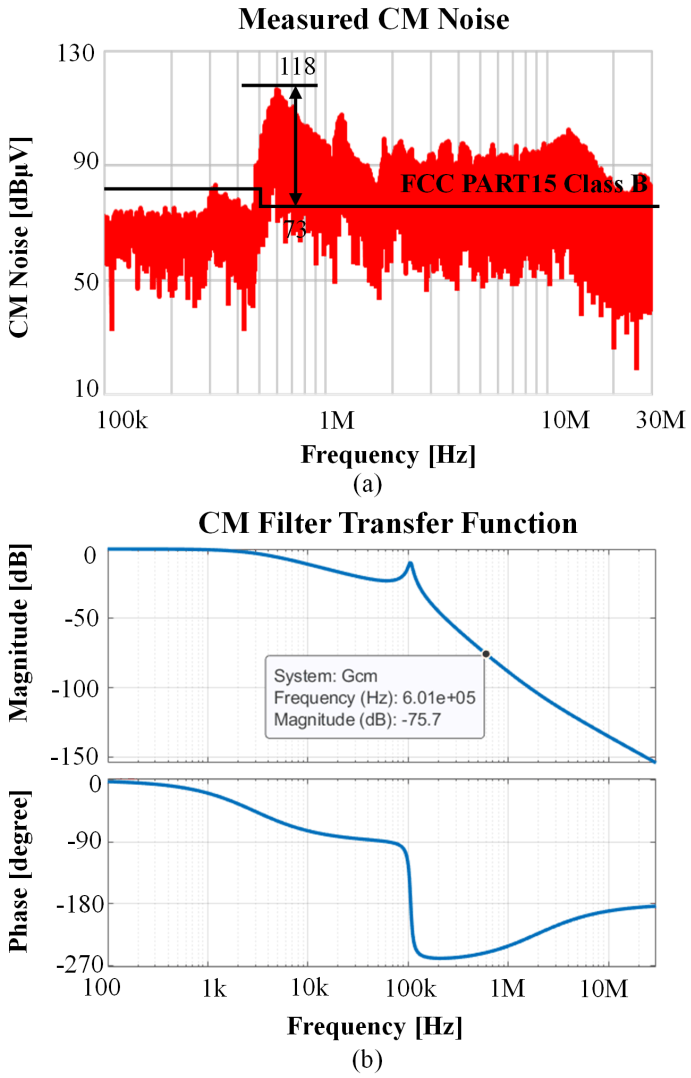


Fig. 4-37. CM EMI filter design process of Litz-wire inductor version without balance technique. (a) Measured CM noise and required attenuation. (b) Transfer function of CM EMI filter.

The next step is to check the required attenuation at the target frequency because the peak noise takes place at 600 kHz and the magnitude is 118 dBuV as shown in Fig. 4-37(a). The required attenuation is obtained as follows:

$$\text{Att\_CM} = 118\ \text{dB (peak noise)} - 73\ \text{dB (EMC standard)} - 6\ \text{dB(margin)} = 51\ \text{dB}. \quad (4\text{-}34)$$

Since the CM capacitor, C_{CM}, is chosen to be 10 nF, the CM inductors L_{CM1} and L_{CM2} are chosen to be 0.45 mH such that the CM filter can have sufficient gain to attenuate the CM noise as shown in Fig. 4.37(b). It should be noted that the same CM chokes are used for L_{CM1} and L_{CM2} in which the DM inductor is integrated in terms of leakage inductance. Then the DM filter is designed. Since the DM inductors are already decided by the choice of the CM choke, the DM capacitors are appropriately selected to have enough attenuation at the highest noise. However, one thing to note is that the DM filter needs to be chosen considering that the ac voltage does not have huge phase delay after passing the EMI filter to keep high power factor between the ac voltage and the ac current at the ac side. The EMI filter in 4-36(b) is designed in a similar way.

Even though both cases use a two stage structure, there is an evident difference. For the litz-wire inductor version without the balance technique, due to the necessity of huge CM noise reduction, two CM chokes are needed: one for the first stage, the other for the second stage. On the other hand, the PCB winding inductor version with the balance technique contains one CM choke for the second stage, but only DM inductors are placed for the first stage. Although the huge CM choke is eliminated with the help of the effective balance technique, the two stage DM filter is still needed because the balance technique has nothing to do with the DM noise reduction. As a result, the additional DM inductors are necessary and similar inductance value (6.8 uH) with the leakage inductance of the CM choke is selected.

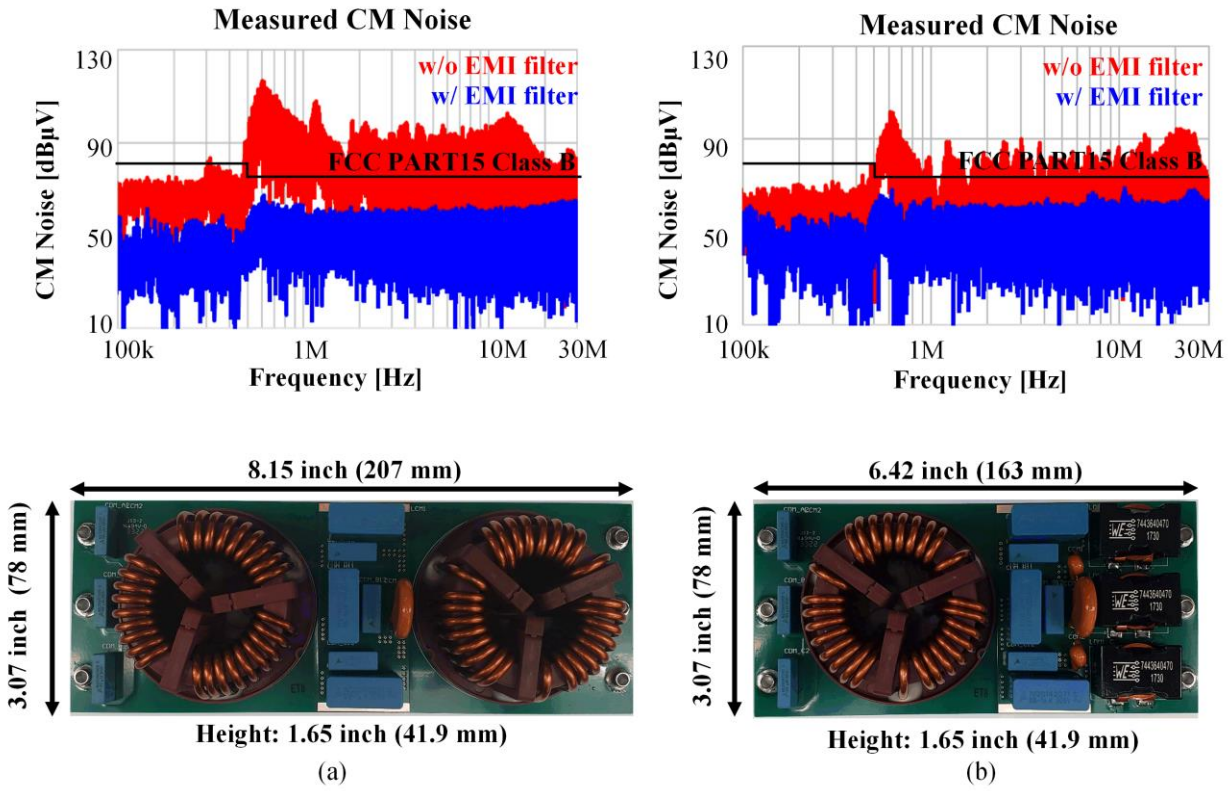


Fig. 4-38. Measured CM noise and designed EMI filter. (a) Litz-wire inductor version without balance technique. (b) PCB winding inductor version with balance technique.

Fig. 4-38 illustrates the CM noise results (top) with the designed EMI filter (bottom) for both cases. After connecting the EMI filters, both cases' CM noise is attenuated properly, and the noise level is brought down below the EMC standard. As mentioned, the CM noise level is at least 6 dB lower than the limit, from 150 kHz to 30 MHz. It turns out that a 21 % size reduction of the EMI filter is achieved by the PCB winding inductor version with balance technique.

4.5 Conclusion

In this chapter, a PCB winding coupled inductor design for a SiC-based two-channel interleaved soft-switching three-phase ac-dc converter with balance technique is investigated. The winding structure, coupling coefficient between the two main inductors, and turns number of the

inductors are carefully selected as design considerations to improve the efficiency of the converter. The impact of interwinding capacitance by the winding interleaving is deeply analyzed with a new inductor model including the parasitic capacitance and an improved inductor structure is proposed to cut down the interwinding capacitance. It is proven that the proposed PCB winding coupled inductor for the balance technique boasts a good CM noise reduction performance (up to 15 MHz), and has similar efficiency to the litz-wire inductor version without the balance technique. Lastly, EMI filters are designed to abide by the EMC standard and compared to show the benefit of the balance technique.

Chapter 5 Extension of Soft-Switching Technique to Standalone Mode Inverter

5.1 Introduction

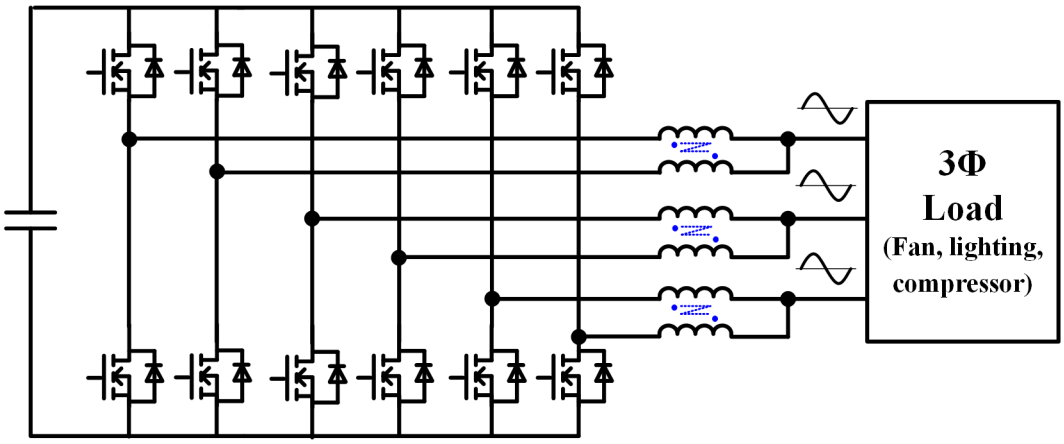


Fig. 5-1. Standalone inverter for locomotive application.

The soft-switching technique can be extended to standalone mode applications such as dc-ac inverters in locomotives, aircrafts, and off-grid PV systems. These applications also demand high efficiency and high power density because size, weight, and efficiency are directly associated with its performance. Fig. 5-1 illustrates a standalone inverter for the locomotive application. This differs from the grid-tied inverter in the sense that it regulates output ac voltage by itself to supply power electric loads such as fans, lighting, compressor, and so on.

Dissimilar to the grid-tied applications, standalone inverters have several additional requirements. First, the output ac voltage needs to be tightly regulated because it becomes the source of electric loads. As a result, the THD requirement (below 2%) is much stricter than that of the grid-tied applications (below 5%). Second, the output ac voltage has to be formed even at no-load condition as a standby. In this case, the output current is extremely small, so the switching

frequency skyrockets for the CRM-based soft-switching modulation which causes unnecessary power consumption and control burden. Lastly, the standalone mode inverter must be capable of the output short-circuit in case the electric loads are shorted externally. In general, the inverter output current is expected to be regulated 150% of the rated current in sinusoidal waveform during the output short-circuit.

In this chapter, the aforementioned aspects are investigated thoroughly. To keep the THD low, an average current control in dq-frame is proposed for the soft-switching modulation. For the no-load operation, a frequency limiting method is applied to minimize switching loss. Operation principle is analyzed, and a control strategy is introduced during the short-circuit.

5.2 Digital Implementation of Current Control for Tight THD Requirement

5.2.1 Digital Control Structure

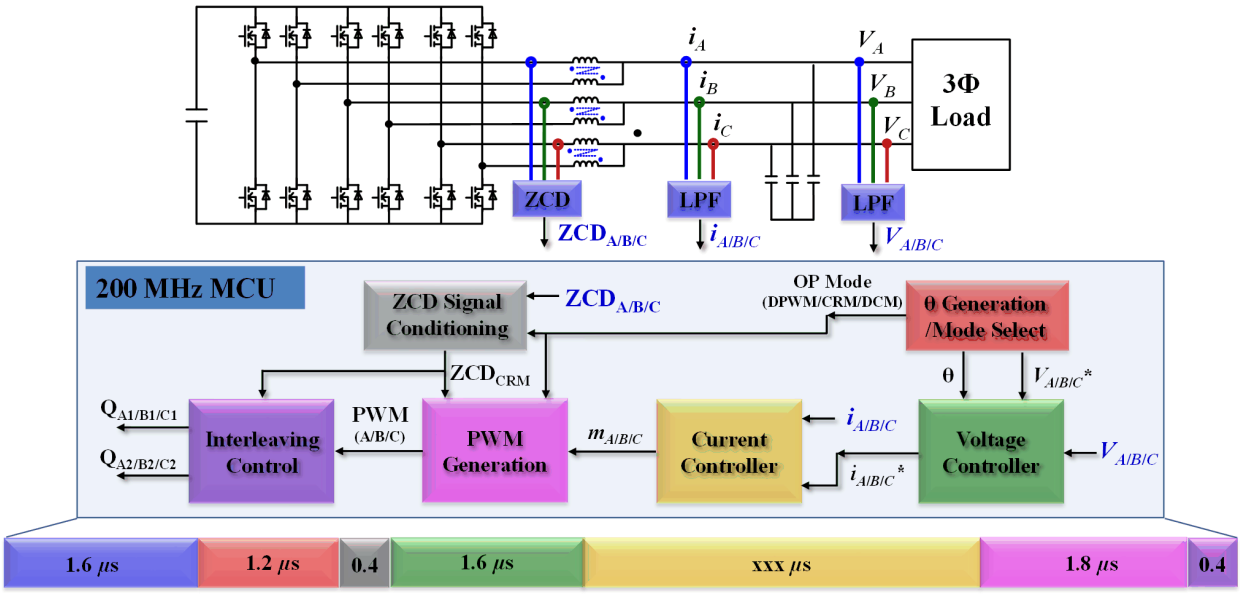


Fig. 5-2. Digital control structure of soft-switching inverter in standalone mode and execution time for funtion blocks with 200 MHz MCU.

Fig. 5-2 depicts the digital control structure of the soft-switching inverter in standalone mode and execution time (calculation time) for function blocks with a 200 MHz MCU. Three sets of signals are sensed, output ac voltage (V_A, V_B, V_C), ac current before ac filter capacitors (i_A, i_B, i_C), and inductor zero current detection (ZCD_A, ZCD_B, ZCD_C). First, the output ac voltage's angle information, θ, is generated according to the required line frequency. This information is used for dq-transformation for controllers, ac voltage reference, and the mode selection of each phase. For example, which phase operates in clamping mode, CRM, and DCM. The sensed ac voltage is regulated to follow the voltage reference and generates the current reference. The sensed current passes through a low pass filter, and this average current is controlled to track the current reference. The current controller generates the control signal (m_A, m_B, m_C). The control signal is used to generate PWM and determines turn-off instant. Turn-on instant is determined by ZCD signal in the CRM phase for frequency synchronization. Then, based on the operation mode of each phase, the final PWM is outputted. Lastly, PWM signals for CH1 and CH2 are created by the interleaving control function block.

With the 200 MHz MCU, each function blocks' execution times are measured in Fig. 5-2. Sensing signals including ADC conversion and low pass filtering take 1.6 us. Output ac voltage angle information generation and mode selection take 1.2 us. Then ZCD signals are processed to output ZCD_{CRM} which takes 0.4 us. The voltage control takes 1.6 us, assuming that it is conducted in dq-frame. For the PWM generation, since each phase changes its operation mode every 30 degrees, the total execution time is 1.8 us. When it comes to the interleaving control, the eCAP module is used to capture the previous switching period and giving 180-degree delay to CH2 switches taking 0.4 us. The remaining part is the current controller. The current control is critical for the output ac voltage regulation performance and plays an important role for the total execution

time because it takes the longest among all function blocks. Since the switching frequency of the soft-switching inverter is very high at several hundreds of kHz, and even higher at light load, the update time or the interrupt time of the MCU should be minimized to ensure best performance. Therefore, the current controller needs to be implemented optimally.

5.2.2 Implementation of Current Control in DQ-frame for Soft-Switching Modulation

In [26], one current control method for the soft-switching inverter is introduced as presented in Fig. 5-3. In this method, the current information in abc-frame is transformed into another domain which is defined as CRM (TCM)/DCM-frame. First, the current reference in abc-frame is rectified and transformed in CRM/DCM-frame. Then, the current references for the CRM phase and the DCM phase can be obtained. There are only two current compensators and the CRM phase current and DCM phase current are controlled separately. Lastly, the control signals in CRM/DCM-frame are transformed back into abc-frame.

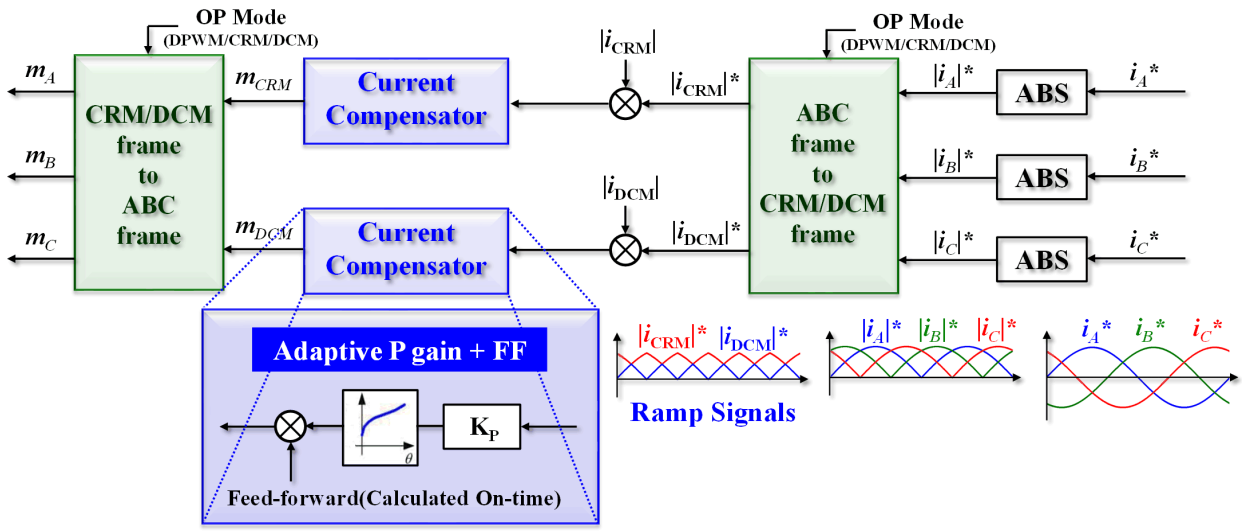


Fig. 5-3. Current control implementation in CRM/DCM-frame [26].

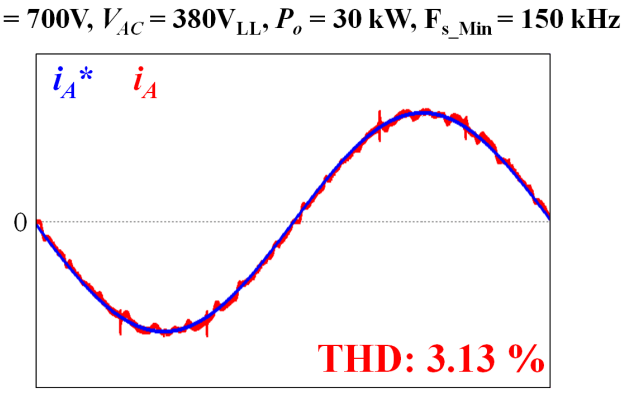


Fig. 5-4. Simulation result with current control in CRM/DCM-frame [26].

In this approach, the current information is in the form of ramp signals. So instead of a simple proportional-integral (PI) controller, an adaptive proportional controller with a feed-forward term is used for the current compensator. The feed-forward term is the key factor to deciding the performance of the current control and it takes long time to calculate. The total execution time for this method including the current reference generation and the current controller in the 200 MHz MCU is 7.7 us. Fig. 5-4 is the simulation result with the control scheme. The sampling time and update time are set to be 15 us because the total execution time is 14.7us. It is seen that the ac current THD exceeds the output ac voltage THD requirement, meaning that the control method is not suitable for the standalone mode inverter.

In [23], the current information in abc-frame is directly used as shown in Fig. 5-5. The rectified current in abc-frame is controlled to track the rectified current reference. There are three current compensators for phase A, B, and C, and their output control signals for each phase independently. A simple PI controller is employed in this current control scheme. The control structure is simple and the execution time for the current control is only 2.36 us, even though one more current compensator is needed compared to that in [26].

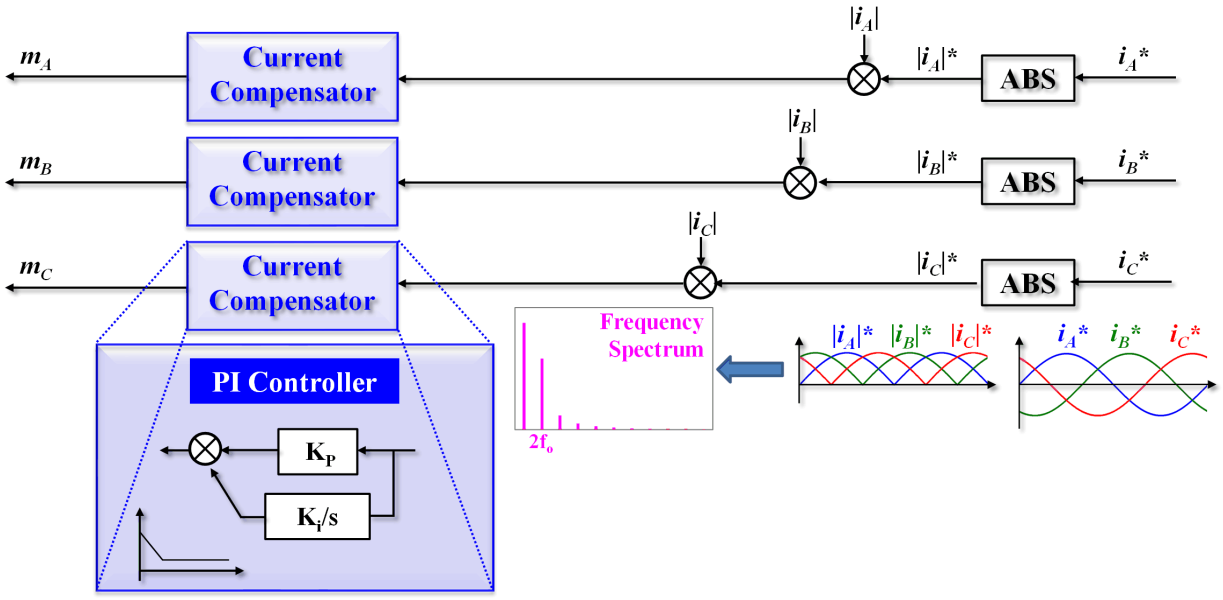


Fig. 5-5. Current control implementation in abc-frame [23].

V_{DC} = 700V, V_{AC} = 380V_{LL}, P_o = 30 kW, F_{s_Min} = 150 kHz

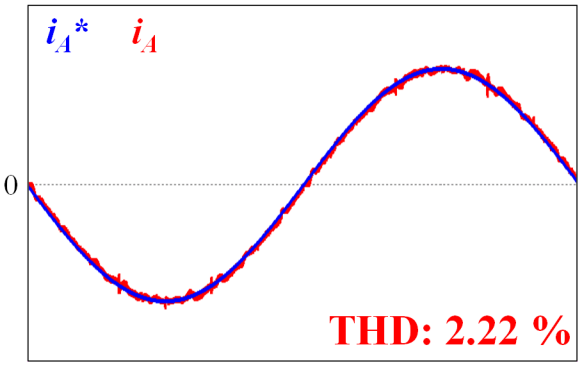


Fig. 5-6. Simulation result with current control in abc-frame [23].

However, due to the existence of the harmonics in the current reference and using the PI controller, which does not have high gain at the harmonic frequencies, there appears to be a steady state error between the current reference and the real current. Fig. 5-6 is the simulation result with the control scheme. The sampling time and update time are set to be 10 us because the total execution time is 9.4 us. Despite this, the current THD is 2.22 %, which does not meet the requirement. One way to improve THD is to increase the bandwidth of the current controller. In

this way, even though the PI controller is used for the compensator, the steady state error can be reduced with higher gain at the harmonic frequencies. However, this soft-switching modulation in digital control needs to have low bandwidth LPF for the current sensing to filter out the high frequency inductor ripple. For 150 kHz switching frequency, LPF's corner frequency should be lower than 15 kHz for sensing accuracy in the MCU. Basically, the dynamic of the current loop is mostly affected by the corner frequency of the LPF. This limits the bandwidth of the current controller below 2-3 kHz in this case.

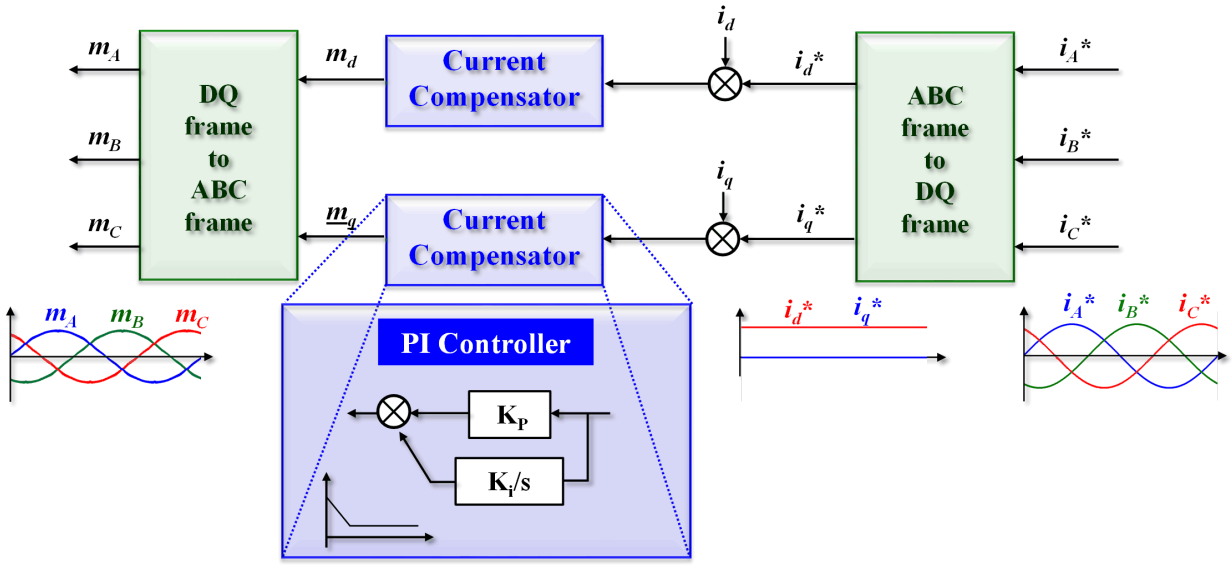


Fig. 5-7. Current control implementation in dq-frame.

To address this issue, a current control in dq-frame is proposed here as illustrated in Fig. 5-7. The current reference in abc-frame is transformed into dq-frame. Then, the current in dq-frame, i_d and i_q, are independently controlled to track the reference. As the current information in dq-frame is in a form of dc value, simple PI controller can be used. Theoretically, there should be no steady state error. This control scheme is the same as one already widely used control method for the conventional CCM-based three-phase inverter. But for the soft-switching three phase inverter, the control signals in abc-frame, which are transformed back from the control signals in dq-frame,

cannot be utilized to generate PWM signals in the MCU. The reason is related to its variable frequency operation.

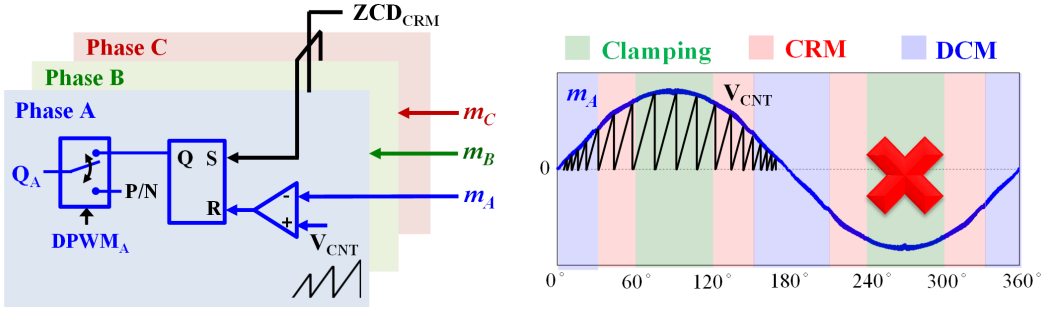


Fig. 5-8. Digital control implementation issue in dq-frame.

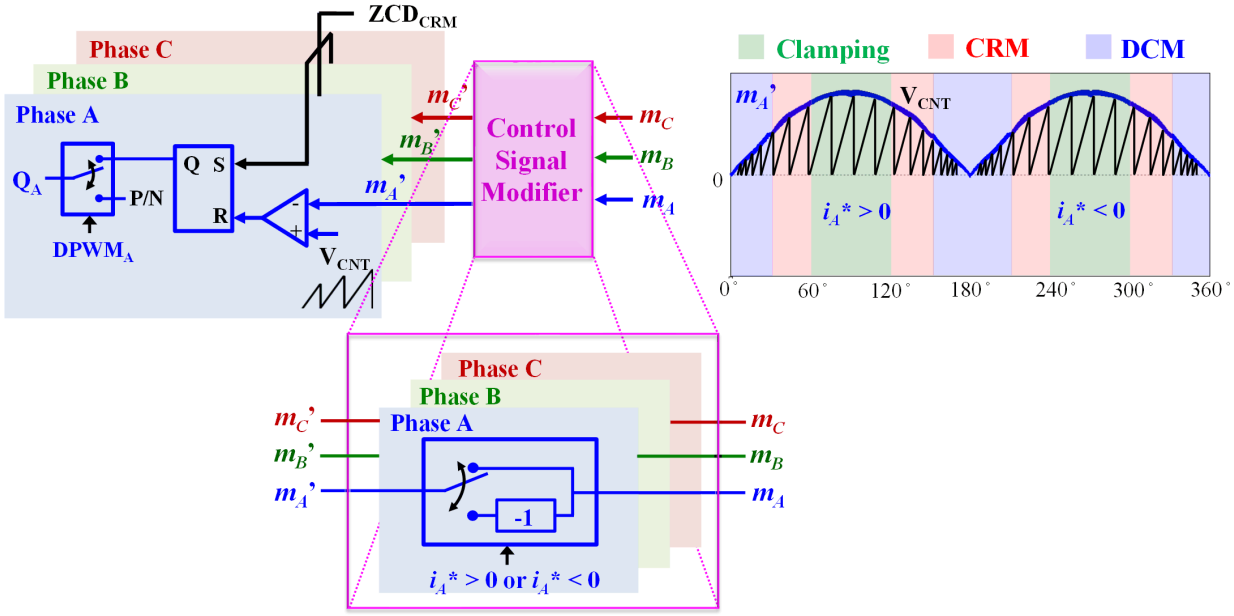


Fig. 5-9. Digital implementation for current control in dq-frame with control signal modifier.

Fig. 5-8 represents how the PWM signal is generated in the MCU. The CRM phase ZCD signal determines the turn-on instant. The turn-off instant is determined by comparing the control signal and internal counter of the MCU, V_{CNT}. Because of the variable switching frequency in CRM, the triangular carrier signal, which needs the switching frequency information in advance, cannot be used for V_{CNT}, and only the sawtooth signal can be used. With the sawtooth signal, when

the control signal is positive, it works fine, but it cannot handle a negative value. Thus, a control signal modifier is needed as shown in Fig. 5-9. Based on the polarity of each phase current reference, the control needs to be rectified. Now the PWM signal can be generated by the sawtooth signal over the whole line cycle. The total execution time for the current control in dq-frame is 3.6 us. It takes a little longer time than the current control in abc-frame due to the abc to dq and dq to abc transformations although it has one fewer current compensator.

Fig. 5-10 is the simulation result with the control scheme. The sampling time and update time are set to be 12.5 us because the total execution time is 10.6 us. Now that the currents are only dc values and the compensator has infinite gain at dc, the ac current THD is 1.56 % and the ac voltage THD requirement is satisfied (assuming the loads are resistive meaning that the ac current THD is equal to ac voltage THD) even with slower update time in the MCU.

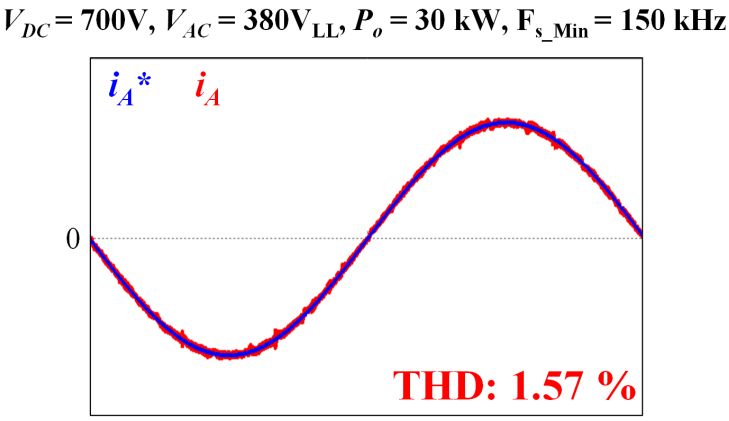


Fig. 5-10. Simulation result with current control in dq-frame.

5.2.3 Experimental Results

In order to verify the control method, a SiC-based 30 kW soft-switching three-phase inverter in standalone mode prototype is built as shown in Fig. 5-11. Contrary to other prototypes built in

other chapters in this dissertation, the MCU is also integrated in the inverter. Also, litz-wire based inversely coupled inductors are made instead of PCB winding inductors, since the inverter has a requirement for 150% overload condition (45 kW). Therefore, its high current makes the PCB winding inductors not appealing for the system. The specifications are tabulated in TABLE 9.

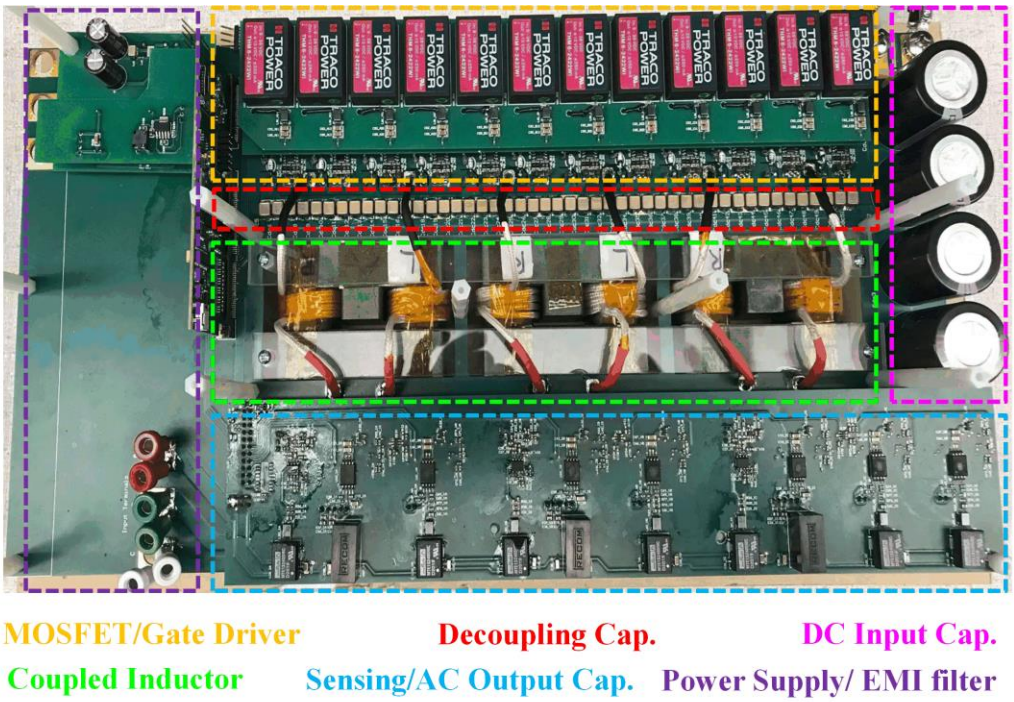


Fig. 5-11. 30 kW three-phase inverter prototype in standalone mode.

TABLE 9 SPECTIFICATIONS OF THE PROTOTYPE IN STANDALONE MODE

Condition	Value
Rated Output Power (P_{o_rated})	30 kW
Input Voltage (V_{DC})	600 - 800 V
Output AC Voltage (V_{AC})	220/380 Vrms at 50 Hz
Self-Inductance (L_{A1}, L_{A2}, L_{B1}, L_{B2}, L_{C1}, L_{C2})	8.4 µH
Mutual-Inductance (M_{12})	-3.7 µH
SiC MOSFETs	C3M0016120K

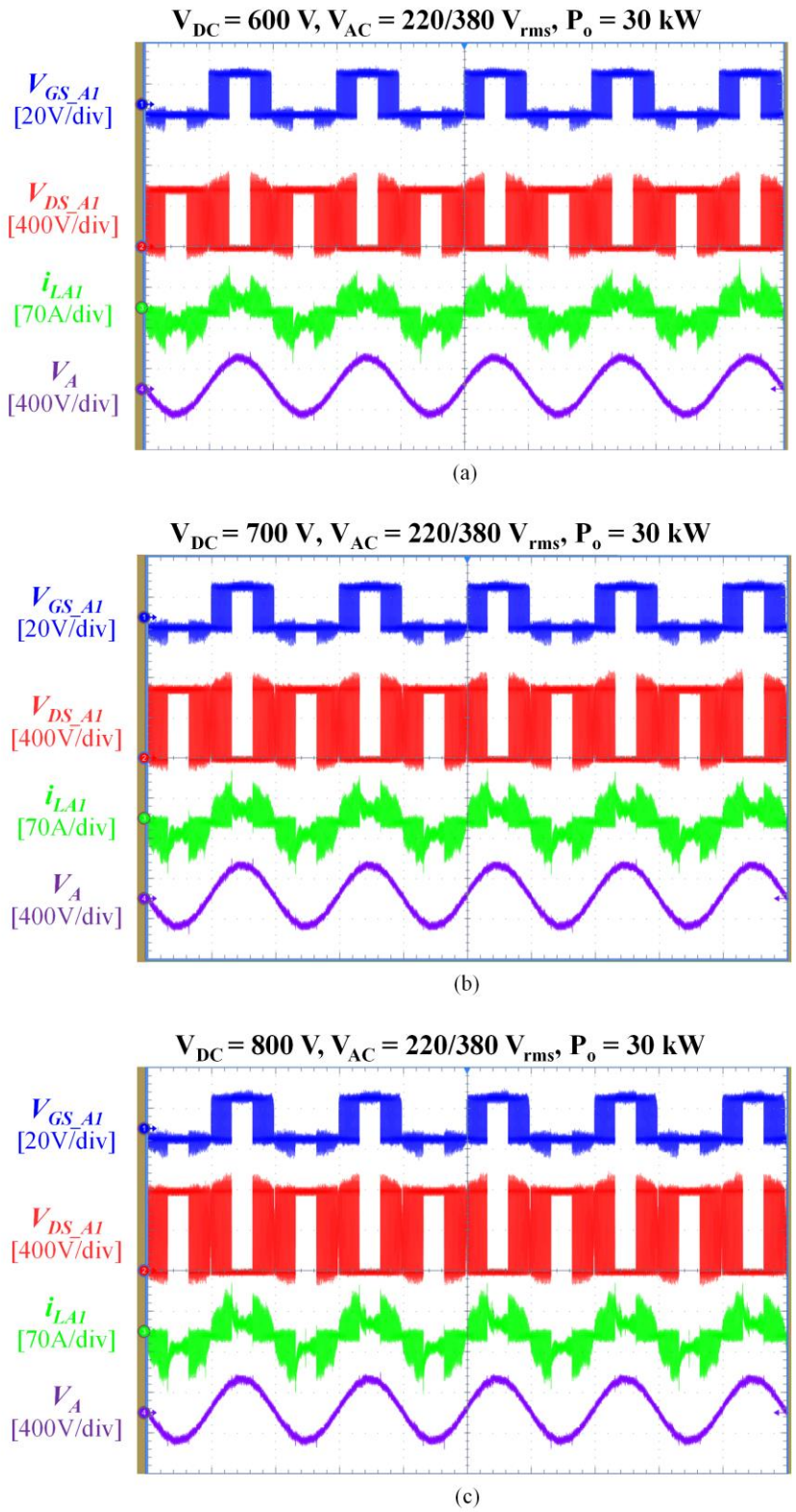


Fig. 5-12. Experimental waveforms of the standalone mode soft-switching three-phase inverter with proposed current control in dq-frame (a) V_{DC} = 600 V, (b) V_{DC} = 700 V, V_{DC}= 800 V.

Experimental waveforms for the standalone mode soft-switching three-phase inverter with the current control in dq-frame according to different input dc voltage are shown in Fig. 5-12. The gate-to-source voltage, the drain-to-source voltage, inductor current of phase A in CH1, and phase A output ac voltage are presented. The output THD is measured to be 1.93 %, 1.96 %, 1.81 % considering up to 40th harmonic components. This validates that the proposed current control implementation method is appropriate for the application which demands very tight output ac voltage regulation.

5.3 Frequency Limiting for No-Load Operation

5.3.1 Extreme switching frequency at no-load

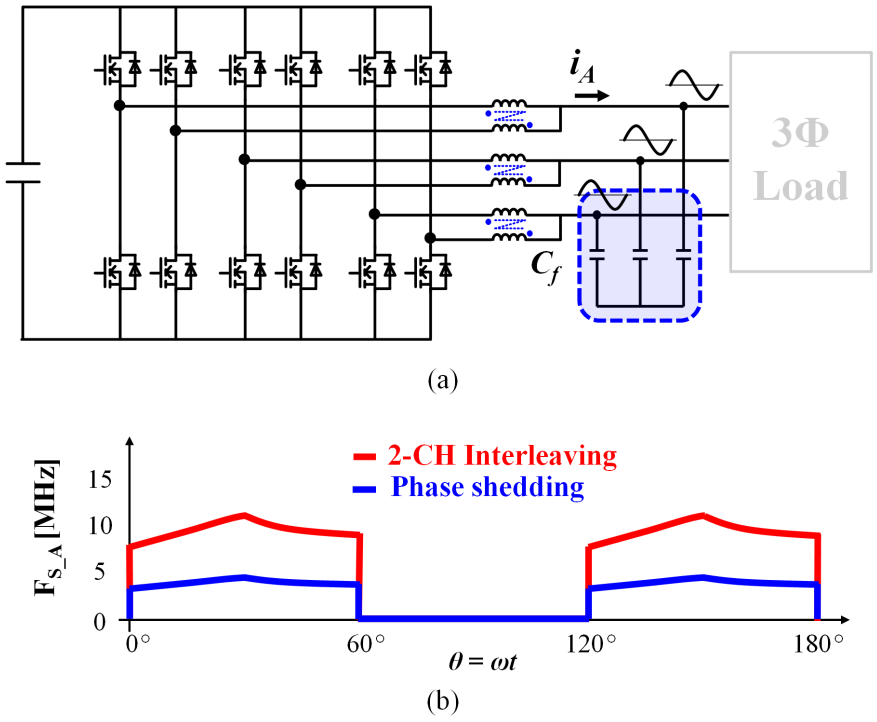


Fig. 5-13. No-load operation for standalone mode inverter. (a) Circuit diagram. (b) Switching frequency range with 2-CH interleaving and with phase shedding.

The standalone inverter needs to be capable of regulating the output ac voltage at even no-load. Now that there is nothing connected to the inverter at the output, the only load to the inverter is its output ac capacitors, as represented in Fig. 5-13(a). This brings about a huge increase in switching frequency. Even if the phase shedding control proposed in Chapter 3 is applied, MHz switching frequency arises, as shown in Fig. 5-13(b). This is not desirable because the power consumption at no-load condition is delivered nowhere and wasted. Thus, the switching frequency should be limited to a lower frequency.

5.3.2 Frequency limiting method at fixed switching frequency

There are two candidates to limit the switching frequency with a fixed value [78]: making the inverter operate at either quasi-square wave (QSW) mode (also called triangular current mode) or at DCM mode. Detailed waveforms for the methods at no-load with a switching frequency at 400 kHz are presented in Fig. 5-14 ((a) QSW case, (b) DCM case), where the phase A inductor current in CH1 and CH2, and the phase A output ac voltage are presented. Both frequency limiting methods can accomplish the proper output ac voltage regulation. It also should be mentioned that the improved phase shedding is still applied for both cases.

The two cases deliver the same output ac current, but the characteristics are totally different. The benefit of the QSW case is that it can achieve ZVS and minimize the turn-on loss; however, the conduction loss and the turn-off loss are very large due to its enlarged current ripple. Also, the active switches and the synchronous rectifiers (SRs) run in one switching cycle, and that gives rise to doubled driving loss compared with the DCM case. The advantage of the DCM case is that the current ripple is smaller than that of the QSW case, so the conduction loss and the turn-off loss are much smaller. Besides, it is optional to run the SRs, so the driving loss can be saved. Yet, DCM

cannot guarantee ZVS leading to a larger turn-on loss. Basically, the selection of a frequency limiting method is a tradeoff between conduction/turn-off/driving loss and turn-on loss.

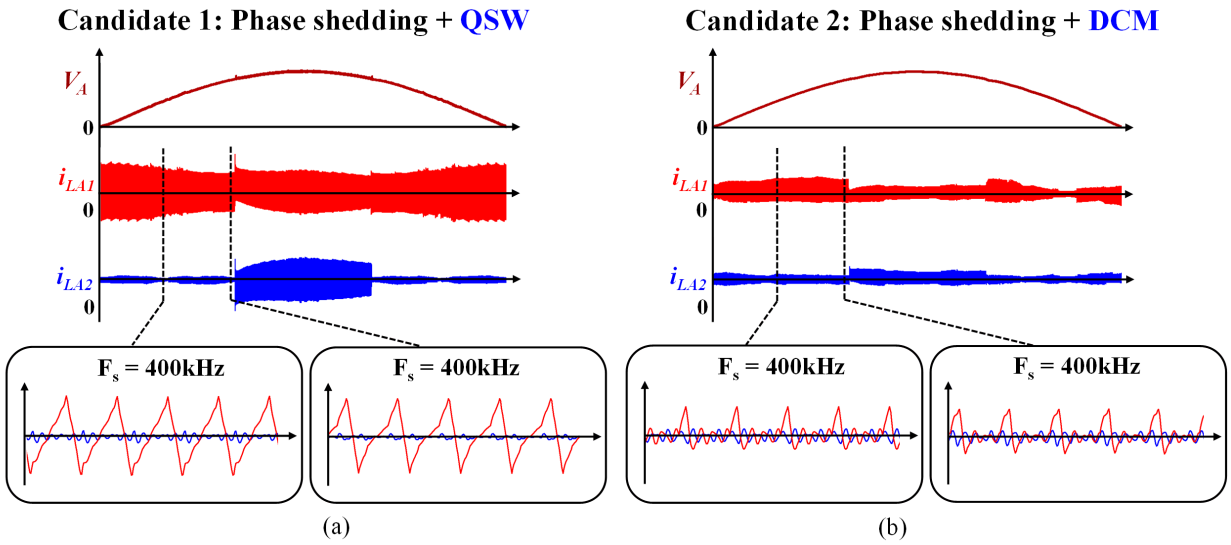


Fig. 5-14. Detailed waveforms of phase A inductor currents at no-load with (a) QSW + phase shedding and (b) DCM + phase shedding.

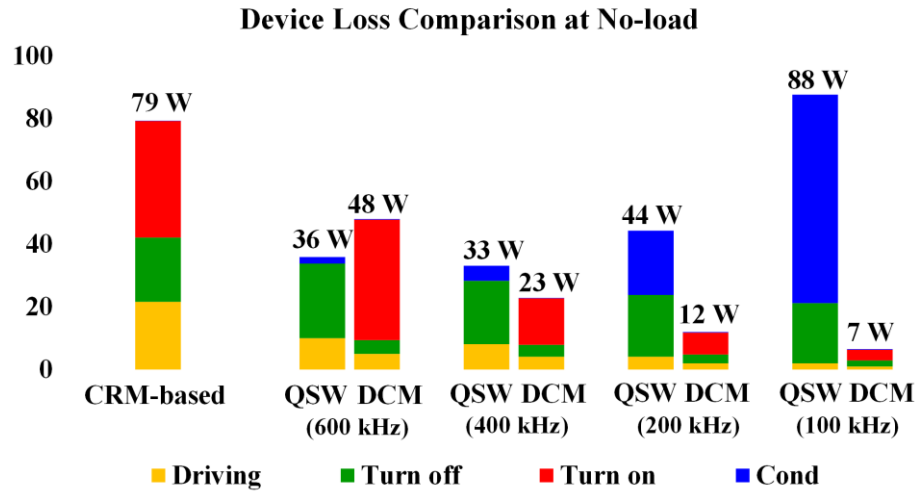


Fig. 5-15. Device loss breakdown comparison for CRM-based, QSW, and DCM modulations at no-load.

To find the more suitable frequency limiting method for the system, the device loss breakdowns based on Cree's C3M0016120K devices are compared in Fig. 5-15, according to

different switching frequencies with different modulation methods. It turns out that the QSW case shows huge conduction loss as the switching frequency becomes lower. The DCM case features smaller total device loss with lower frequency, and the loss is smaller than the CRM-based modulation. Therefore, the DCM method is selected to limit the switching frequency under no-load conditions. It should be noted that this conclusion may be the opposite if other SiC power devices are used to the comparison.

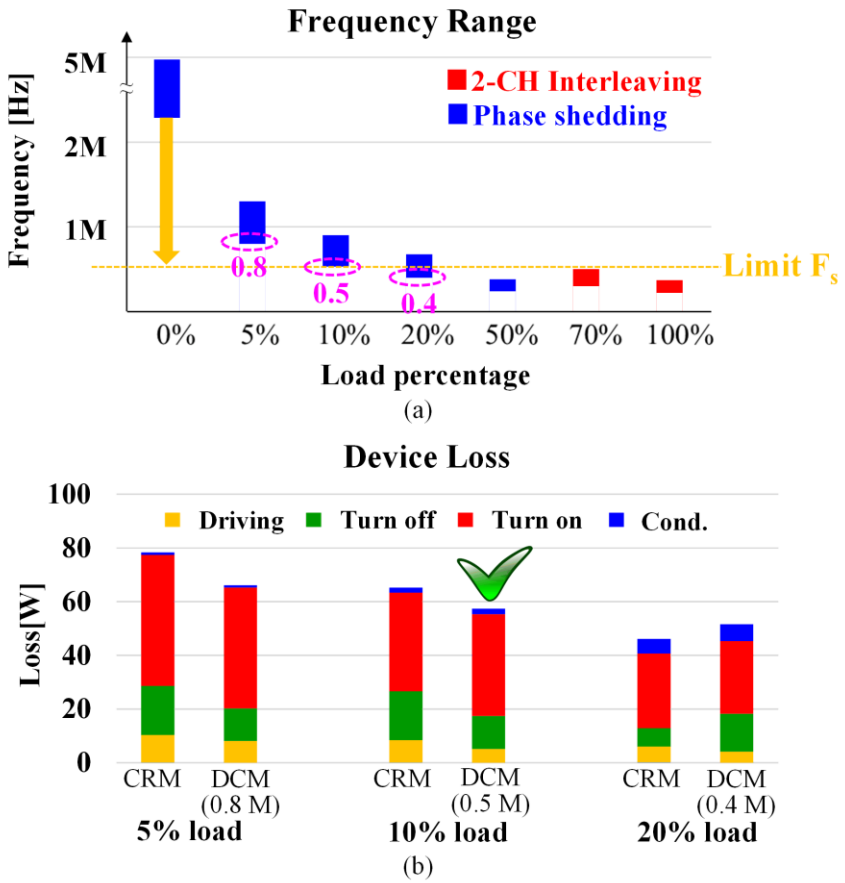


Fig. 5-16. Device loss breakdown comparison for CRM-based, QSW, and DCM modulations at no-load.

The next point is from which load condition this frequency limiting begins and at what switching frequency it should operate. In Fig. 5.16, the device loss of CRM-based soft-switching at light loads (5 %, 10 %, and 20 %) is compared with that of DCM frequency limiting. The

frequency of each case for the DCM method is selected to be the minim frequency of the CRM-based soft-switching in Fig. 5-16(a) to seamless transition from the CRM modulation to the DCM modulation. It is seen that at 20 % load the frequency limiting with DCM shows higher loss, but at 10 % load, it shows a smaller loss. So it is decided that the DCM frequency limiting starts when the load becomes lower than 10 % at 500 kHz.

5.3.3 Experimental results

Fig. 5-17 is experimental waveforms for the frequency limiting with DCM at no-load condition (V_{DC} = 700 V). The output ac voltage in phase A is well regulated as sinusoidal. On top of that, the measured THD is very low, 1.72 %.

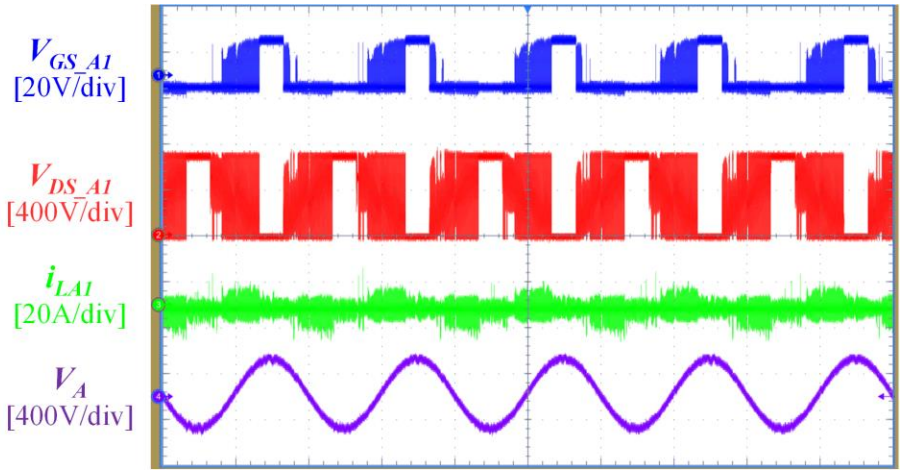


Fig. 5-17. Experimental waveforms of frequency limting with DCM at steady state.

Experimental waveforms of transient response from no-load to 30 kW, and from 30 kW to no-load are shown in Fig. 5-18 and Fig. 5-19. The output of the inverter is connected to the resistor bank for 30 kW through mechanical switches (Panasonic HE1AN-W-DC24V). At the load change instant, the mechanical switches are on or off so that there is a step load change. Despite the step load change, the transient is done seamlessly. In these experiments, the DC source's voltage also

drops when the load steps up and rises when the load steps down, which cause a small delay for the inverter to reach the steady state. However, after the load step change, the output ac voltage is regulated in the form of sinusoidal waveform within a half line cycle.

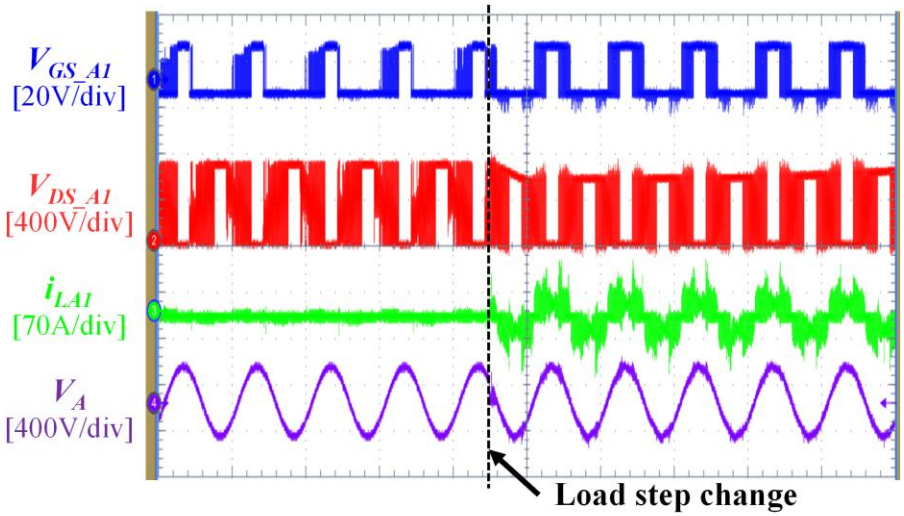


Fig. 5-18. Experimental waveforms of load transient from no-load to 30 kW.

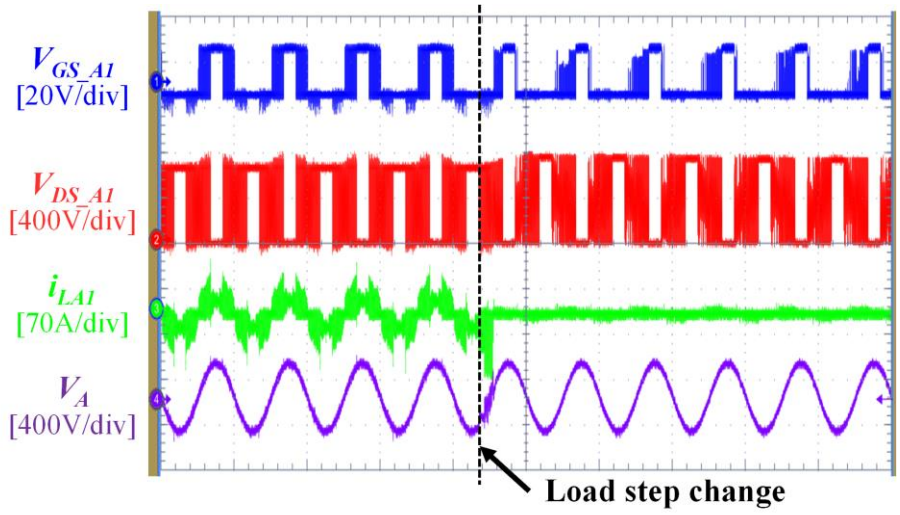


Fig. 5-19. Experimental waveforms of load transient from 30 kW to no-load.

5.4 Control Strategy for Output Short-Circuit

5.4.1 Output short-circuit in standalone mode inverter

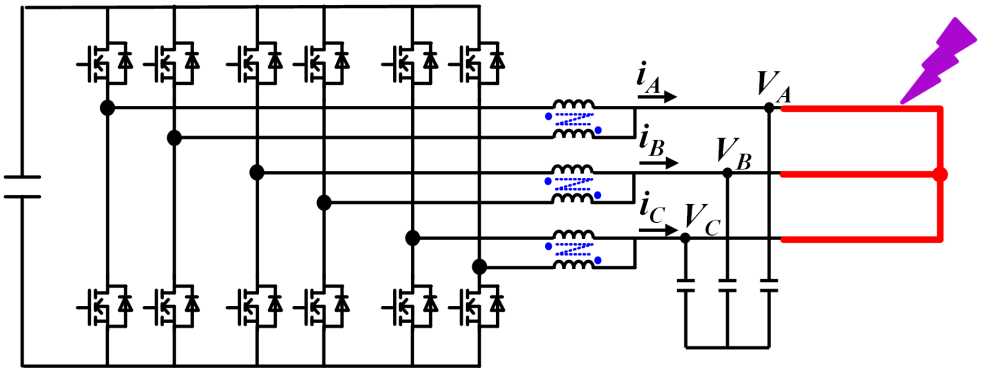


Fig. 5-20. Standalone mode inverter at output short-circuit.

The standalone mode inverter has a unique requirement regarding output short-circuit, as there is a possibility that some loads can be shorted due to an electric failure or a human error, as shown in Fig. 5-20. In this sense, the requirement demands safe operation of the inverter under such a condition. The inverter is expected to control the output ac current to be 150% of the rated value given as

$$\begin{cases} I_{A\_Ref} = 1.5 \cdot \sqrt{2} I_{rated} \sin(\omega t) \\ I_{B\_Ref} = 1.5 \cdot \sqrt{2} I_{rated} \sin(\omega t - 2\pi / 3) \\ I_{C\_Ref} = 1.5 \cdot \sqrt{2} I_{rated} \sin(\omega t + 2\pi / 3) \end{cases} \quad (5\text{-}1)$$

where I_{rated} is the rms ac current value at rated power, and ω is the angular frequency of the inverter. Similarly, when two phases are shorted and only one phase is connected to the load correctly, for example, phase A and B are shorted, the currents in each phase are expected to be controlled as:

$$\begin{cases} I_{A\_Ref} = 1.5 \cdot \sqrt{2} I_{rated} \sin(\omega t) \\ I_{B\_Ref} = -1.5 \cdot \sqrt{2} I_{rated} \sin(\omega t) \\ I_{C\_Ref} = 0 \end{cases} \quad (5\text{-}2)$$

A couple of articles have discussed how to deal with the output short-circuit for inverters, but these are hard to apply to the soft-switching three-phase inverter because these studies were done based on the conventional CCM-based modulation method [79], [80]. Therefore, a dedicated control strategy needs to be developed for the soft-switching inverter. When the short-circuit occurs on the soft-switching inverter, it turns out from a preliminary simulation result that the inverter cannot regulate the output current. This is illustrated in Fig. 5-21. Output ac voltage (V_A, V_B, V_C), phase A inductor currents (i_{LA1}, i_{LA2}), averaged output ac current (I_A), and phase A ac current reference (I_{A_Ref}) are shown. In Fig. 5-21, when the short-circuit for all phases arises at t_1, the ac current reference is modified to 150% rated current immediately. However, the inductor currents are not controlled properly. The inductor current in CH1 increases rapidly, and almost no current flows in CH2 inductor.

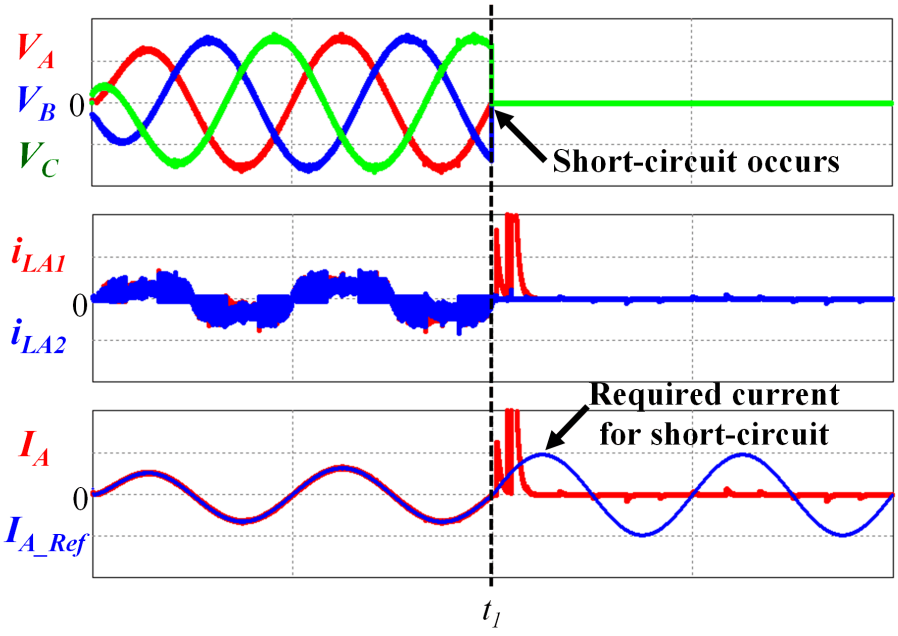
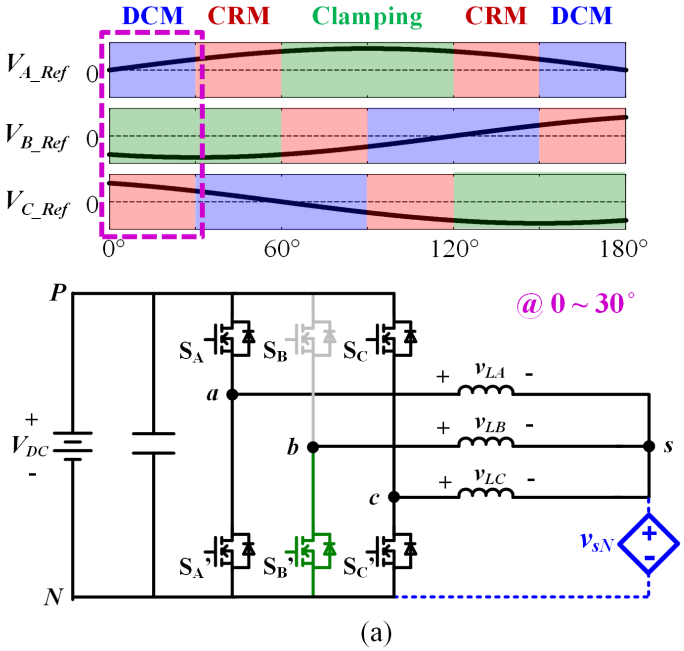


Fig. 5-21. Simulated waveforms of soft-switching inverter at output short-circuit.

The reason why the inductor currents are not controlled appropriately is because of a violation of the inductor voltage-second balance in clamping mode during the short-circuit. For the sake of

simplicity, a non-interleaved CRM-based soft-switching three-phase inverter during the short-circuit is analyzed in Fig. 5-22. Take the first 30° in Fig. 5-22(a) as an instance. Phase B is in clamping mode and clamped to *P* node. Then the phase A and phase C switches are turned on and off. All possible combinations of switching status in the three phases are enumerated in Fig. 5-22(b).



(a)

Phase A (DCM)		Phase B (Clamp)		Phase C (CRM)		v_{sN}	v_{LA}	v_{LB}	v_{LC}
S_A	S_A'	S_B	S_B'	S_C	S_C'	-	-	-	-
1	0	0	**1**	1	0	$2V_{DC}/3$	$V_{DC}/3$	$\mathbf{-2V_{DC}/3}$	$V_{DC}/3$
0	1	0	**1**	1	0	$V_{DC}/3$	$2V_{DC}/3$	$\mathbf{-V_{DC}/3}$	$-V_{DC}/3$
0	1	0	**1**	0	1	0	0	**0**	0
0	0	0	**1**	0	1	$V_{DC}/6$	$-V_{DC}/6$	$\mathbf{-V_{DC}/6}$	$V_{DC}/3$
0	0	0	**1**	0	0	$V_{DC}/3$	$V_{DC}/3$	$\mathbf{-V_{DC}/3}$	$V_{DC}/3$

(b)

Fig. 5-22. Violation of inductor voltage-second balance in clamping mode phase during short-circuit. (a) inverter circuit operation at 0° - 30°. (b) Switching status and inductor voltages.

Also, voltages across the inductors in accordance with the switching status are presented in Fig. 5-22(b), which are expressed as:

$$\begin{cases} v_{LA} = v_{aN} - v_{sN} \\ v_{LB} = v_{bN} - v_{sN} \\ v_{LC} = v_{cN} - v_{sN} \end{cases} \tag{5-3}$$

where v_{aN}, v_{bN}, v_{cN} are the inverter output voltage at each leg, and v_{sN} is the zero-sequence voltage. Even though the ac output is shorted, v_{sN} is expressed as the same as that in the normal operation given by:

$$v_{sN} = \frac{v_{aN} + v_{bN} + v_{cN}}{3} . \tag{5-4}$$

During the short-circuit, the zero-sequence voltage plays a really critical role because it becomes the only voltage source which can discharge the inductor in each phase. The output ac voltage in each phase becomes zero and the inductors rely on the inverter output voltage and the zero-sequence voltage to charge and discharge energy in the inductor. By considering all possible switching statuses, Fig. 5-22(b) reveals that phase B, the clamping mode phase, violates the inductor voltage-second balance. It is seen that the sign for phase B inductor is only negative in one switching period during such an occasion. Basically, in the CRM-based soft-switching modulation, there is no chance for the clamping mode phase to achieve the inductor voltage-second balance. The same principle is applicable to the two-channel interleaved three-phase inverter. In conclusion, with the CRM-based soft-switching modulation, there is no way to handle the output short-circuit. This problem is not only for the soft-switching modulation, but also for the general DPWM. We cannot use DPWM during the output short-circuit.

5.4.2 Control strategy for short-circuit in standalone

Fig. 5-23 exhibits a control strategy for the short-circuit for the soft-switching inverter in standalone mode. As mentioned, the CRM-based modulation cannot be used. Therefore, the modulation itself must be replaced with another one. In Fig. 5-23, a fixed frequency operation is selected. Once the output short-circuit is detected, the modulation method is switched to the fixed frequency sinusoidal PWM as shown in the enlarged function block in Fig. 5-23.

In this case, the current control can be shared for normal operation and short-circuit. But when the short-circuit is detected by monitoring the output ac voltage and the voltage controller (when the output of the voltage controller is saturated, but the ac voltage value remains zero [78]), the modulation is switched. The control signals (m_A, m_B, m_C) are compared with a fixed frequency carrier signal as shown in Fig. 5-23. One distinction is that the control signals are not modified, as explained in Fig. 5-9, for the CRM-based soft-switching modulation. It is because a triangular carrier signal can be used for the PWM generation due to its fixed frequency operation.

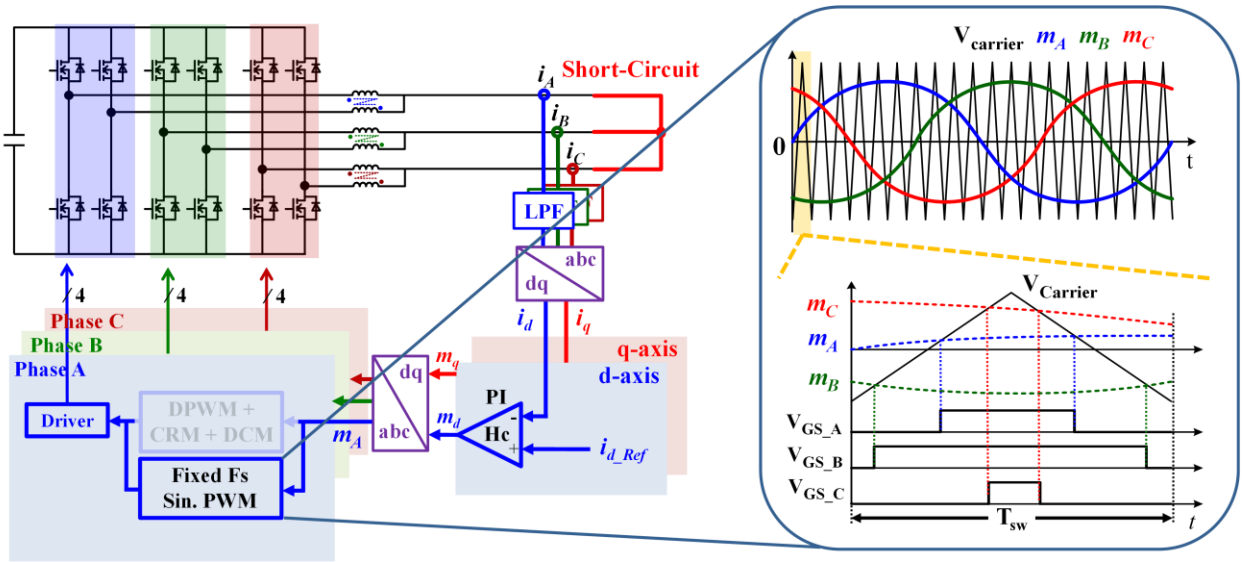


Fig. 5-23. Short-circuit control strategy for the soft-switching inverter in standalone mode.

The next step is to decide the switching frequency during the short-circuit. According to the switching frequency the characteristic of the inverter becomes totally different. Fig. 5-24 depicts simulation results of two different cases. One is for F_s = 100 kHz and the other is for F_s = 300 kHz. In Case 1, the zoomed-in waveform shows that the inductor current crosses zero and becomes negative. This is called quasi-square wave mode (QSW) or TCM. Therefore, ZVS can be achieved. The con of this method is the large current ripple resulting in high conduction loss. On the other hand, Case 2 has smaller current ripple, but QSW is not guaranteed as the current ripple becomes smaller having high turn-on loss with partial CCM. Basically, the choice of the switching frequency is a tradeoff between conduction loss and turn-on loss. Fig. 5-25 represents the device loss comparison for the different switching frequencies. The total device loss is broken down into conduction loss and switching loss. The final selection is 200 kHz because it shows the lowest total loss.

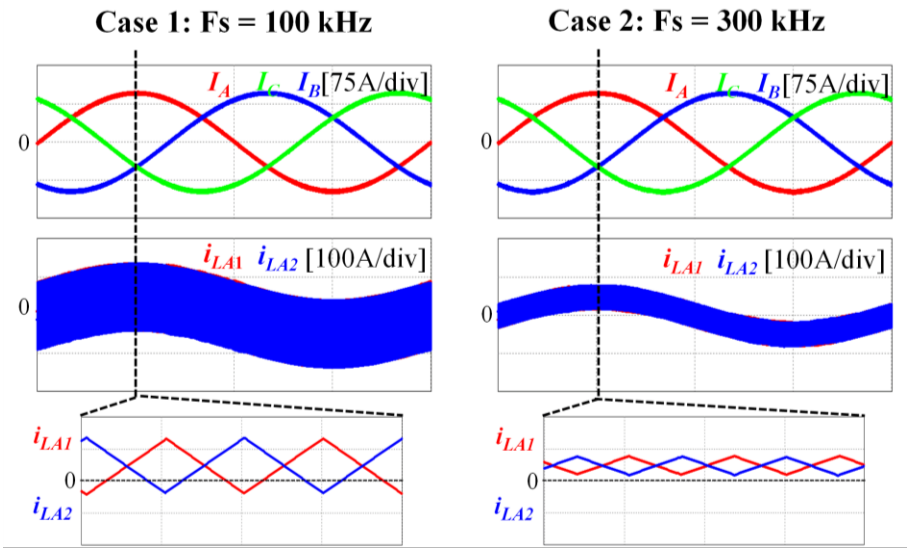


Fig. 5-24. Fixed frequency SPWM during short-circuit at different switching frequencies.

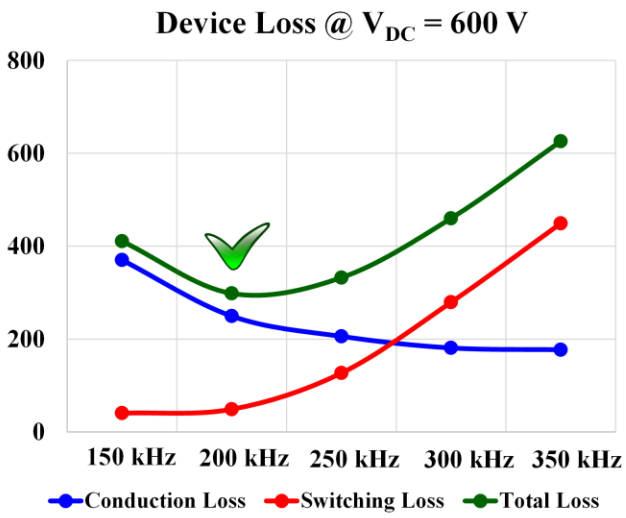


Fig. 5-25. Fixed frequency SPWM during short-circuit at different switching frequencies.

5.4.3 Experimental results

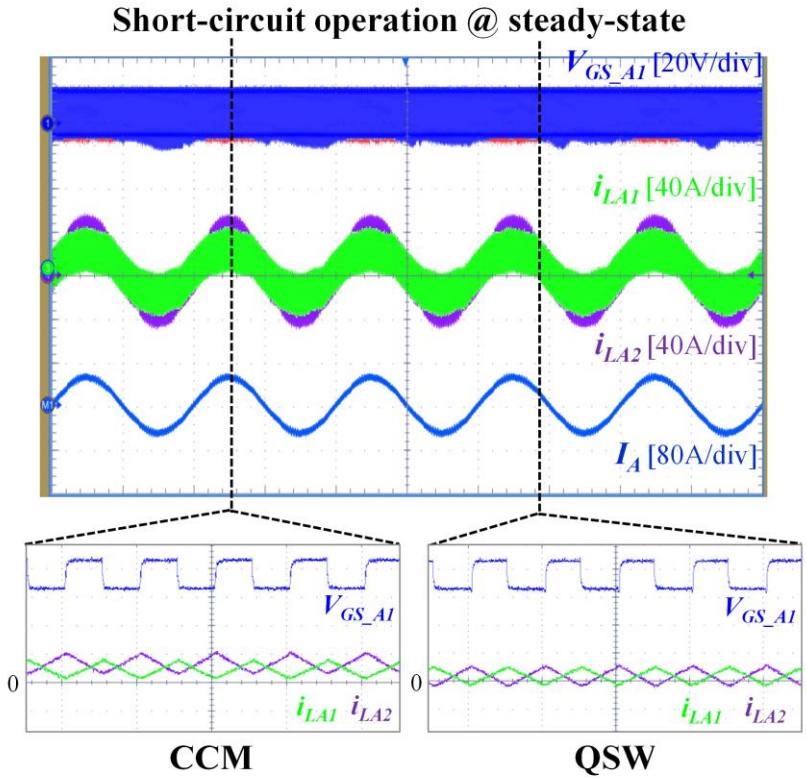


Fig. 5-26. Short-circuit opration at steady state.

Fig. 5-26 illustrates the experimental waveforms for the three-phase short-circuit operation at steady state. In Fig. 5-26, phase A CH1 top switch gate-to-source voltage, V_{GS_A1}, phase A inductor currents, i_{LA1}, i_{LA2}, and phase A output current, i_A, are shown. The ac current is well controlled as sinusoidal during the short-circuit. It should be mentioned that CH1 inductor current is smaller than that of CH2. This arises because the shunt resistor for ZCD sensing is only placed in series with CH1 inductor and generates some voltage drop across it. Then, the voltage excitation across CH1 and CH2 inductor becomes non-identical. For the switching cycle waveforms at the bottom, as expected, not only QSW, but also CCM exits over the line cycle at 200 kHz.

Fig. 5-27 and Fig. 5-28 depict the transient response from the normal operation to the three-phase short-circuit operation, three-phase short-circuit and two-phase short-circuit, respectively. Both cases can control the output ac current properly. What is distinct is that the ac currents in Fig. 5-27 show a 120 degree shift from each phase, but two of those in Fig. 5-28 show a 180 degree shift and the other is zero as mentioned in (5-1) and (5-2). It is validated that, with the control strategy, the transition between two modulation methods is seamless without any glitches.

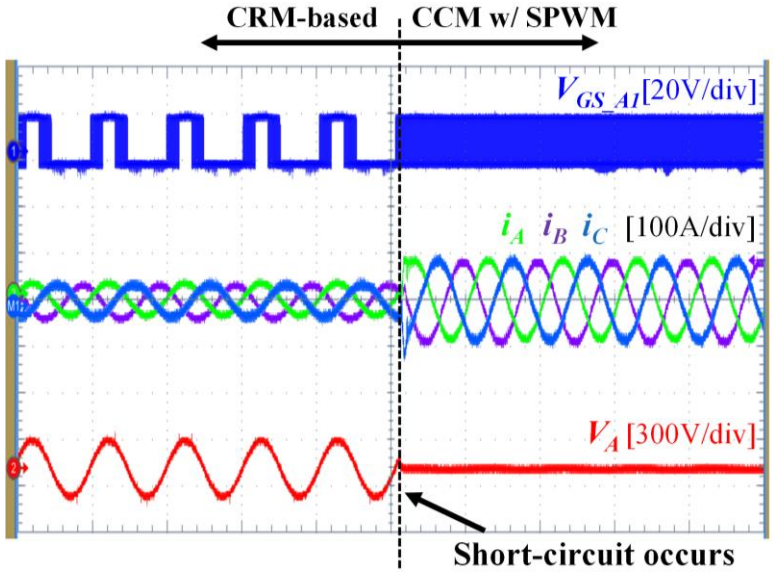


Fig. 5-27. Transient response from normal operation to three-phase short-circuit operation.

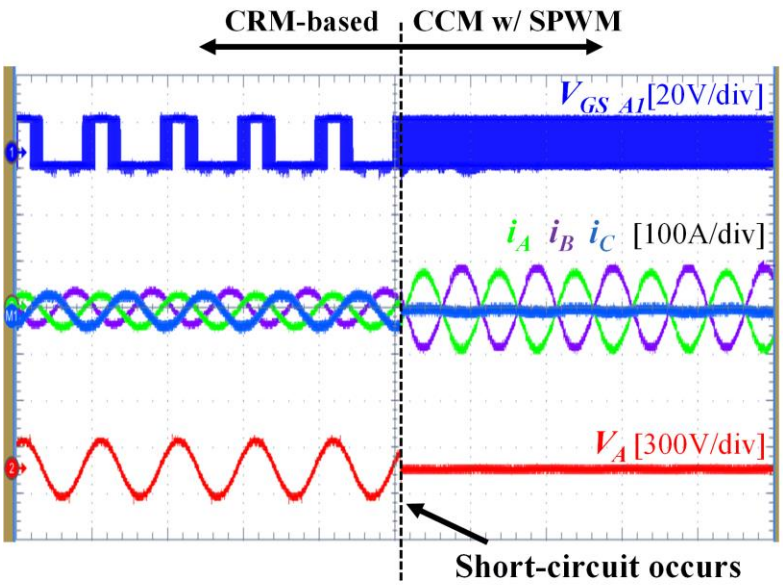


Fig. 5-28. Transient response from normal operation to two-phase short-circuit operation.

5.5 Conclusion

In this chapter, extension of the CRM-based soft-switching technique to standalone mode is explored. Three main subjects are covered. First, the digital control implementation for the current control in dq-frame to meet the tight requirement for the high output ac voltage. Second, the frequency limiting with fixed frequency DCM is proposed to minimize the enormous switching frequency increase at no-load condition. Lastly, how to deal with the output short-circuit is discussed. Since the CRM-based soft-switching modulation cannot satisfy the inductor voltage-second balance, it was replaced with the conventional SPWM at fixed frequency CCM during the short-circuit. All of these studies with experimental verification prove that the soft-switching technique can be a very appealing solution not only for grid-tied applications, but also for standalone mode applications.

Chapter 6 Conclusions and Future Work

In this dissertation, control, analysis, and design of SiC-based soft-switching three-phase ac-dc converters are deeply analyzed. For high efficiency, high power density soft-switching ac-dc converters to be more widely accepted in real products in the market, the author covers practical issues based on target application requirements.

First, how to deal with unbalanced grid conditions is explored. Unbalanced ac current needs to be injected to deliver constant active power when the grid stays unbalanced. This causes the unexpected hard-switching by CCM operation in the soft-switching inverter. Control methods to allow the DCM phase inductor current to cross zero are proposed to eliminate the hard-switching, called “CRM off-time extension” and “DCM pulse skipping”. Especially, the pulse skipping control is analyzed and evaluated carefully. It fulfills partial ZVS, resulting in huge reduction in the turn-on loss, and lessens the chance of a noise issue. The proposed control is applied to the representative cases of voltage sags. With the proposed control, the CRM-based soft-switching technique is proven to be a more attractive solution for DERs, which require high power density, high efficiency, and capability of stable operation under unbalanced grid conditions.

Second, a new phase shedding control for two-channel paralleled soft-switching three-phase inverters is studied. To improve light load efficiency, phase shedding is first applied to the entire CH2. However, an unwanted circulating current is generated because of body diode conduction in CH2 during the clamping mode, which gives rise to increased conduction loss. Detailed analysis of the circulating current shows that the switching status in CH1 effects the inverter output voltage in CH2 via the shared zero-sequence voltage. To address this issue, phase shedding for only the CRM phase and the DCM phase in CH2 is executed by activating the clamping mode phase in

CH2. Consequently, the circulating current is eliminated. The proposed control is experimentally verified and substantial efficiency improvement is achieved.

Third, a PCB winding coupled inductor design for soft-switching three-phase ac-dc converter with balance technique is investigated. The winding structure, coupling coefficient between the two main inductors, and turns number of the inductors are carefully selected as design considerations to improve the efficiency of the converter. The impact of interwinding capacitance by the winding interleaving is deeply analyzed and an improved inductor structure is proposed to cut down the interwinding capacitance. It is proven that the proposed PCB winding coupled inductor for the balance technique boasts a good CM noise reduction performance (up to 15 MHz), and has similar efficiency to the litz-wire inductor version without the balance technique.

Lastly, how to extend the soft-switching technique to standalone mode inverter is investigated. The current control in dq-frame enables the inverter to regulate the output voltage with very small THD. The frequency limiting with DCM dramatically reduces switching loss. During output short-circuit, the conventional SPWM replaces the CRM-based modulation to obey the inductor volt. -second balance resulting in capability to regulate the ac current.

However, there must still be a lot of effort put in for the soft-switching ac-dc converter to be accepted in the real market, since the soft-switching technique solely relies on the ZCD signal to achieve CRM. This requires more studies on how to increase reliability of the circuit realization. Another issue could be thermal management of the PCB winding inductor. Although the inductor is designed to minimize the winding loss, effective cooling method for the inductor is necessary. Also, how the soft-switching technique can be used in multi-level ac-dc converters and studying the pros and cons could be an interesting research topic.

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