SiC-Based High-Frequency Soft-Switching Three-Phase Rectifiers/Inverters

Zhengrong Huang

Dissertation submitted to the faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Electrical Engineering

Qiang Li, Chair
Fred C. Lee
Dong Dong
Virgilio Centeno
Alfred L. Wicks

September 24th, 2020
Blacksburg, Virginia

Keywords: Critical conduction mode, digital control, high frequency, silicon carbide, soft switching, three-phase rectifiers/inverters.

SiC-Based High-Frequency Soft-Switching Three-Phase Rectifiers/Inverters

Zhengrong Huang

Abstract

Three-phase rectifiers/inverters are widely used in grid-tied applications. Take the electric vehicle (EV) charging systems as an example. Within a certain space designated for the chargers, quick charging yet high efficiency are demanded. According to the current industry practice, with a power rating between 10 and 30 kW, the power density are limited by silicon (Si) power semiconductor devices, which make the systems operate at only up to around 30 kHz.

The emerging wide bandgap (WBG) power semiconductor devices are considered as game changing devices to exceed the limits brought by their Si counterparts. Much higher switching frequency, higher power density and higher system efficiency are expected to be achieved with WBG power semiconductor devices. Among different types of WBG power semiconductor devices, Silicon Carbide Metal-Oxide-Semiconductor Field-Effect Transistors (SiC MOSFETs) are more popular in current research conducted for tens of kW power converter applications. However, the commonly adopted hard switching operation in this application still leads to significant switching loss at high frequency operation even for SiC-based systems.

With the unique feature that the turn-off energy is almost negligible compared with the turn-on energy, critical conduction mode (CRM) based zero voltage soft switching turn-on operation is preferred for the SiC MOSFETs to eliminate the turn-on loss with small penalty on the conduction

loss and on the turn-off loss. With this soft switching operation, switching frequency of SiC-based systems is able to be pushed to more than ten times higher than Si-based systems, and therefore higher power density yet even higher system efficiency can be achieved.

The CRM-based soft switching is applied to three-phase rectifiers/inverters under the unity power factor operating condition first. Decoupled CRM-based control is enabled, and the inherent drawback of wide switching frequency variation range at CRM-based operation is overcome by the proposed novel modulation technique. It is the first time that CRM-based soft switching modulation is demonstrated in the most conventional three-phase H-bridge ac–dc converter, and more than three-time size reduction compared with current industry practice yet 99.0% peak efficiency are achieved at above 300 kHz switching frequency operation.

Then this proposed soft switching modulation technique is extended to non-unity power factor operating conditions especially for grid-tied inverter system applications. With several improvements on the modulation, a generalized CRM-based soft switching modulation technique is proposed, which is applicable to both the unity and non-unity power factor conditions. With the power factor down to 0.8 lagging or leading according to commercial products, above 98.0% peak efficiency is achieved with the generalized soft switching modulation technique at above 300 kHz switching frequency operation.

Furthermore from the aspect of electromagnetic interference (EMI), compared with the traditional Si-based design, CRM operation brings higher differential-mode (DM) EMI noise, and higher dv/dt with SiC MOSFETs brings higher common-mode (CM) EMI noise. What's more, hundreds of kHz switching frequency operation makes the main components of the system EMI spectrum located within the frequency range related to the EMI standard (150 kHz – 30 MHz). Therefore, several methods are adopted for the reduction of EMI noise. The total inductor current

ripple is reduced with multi-channel interleaving control in order to reduce DM EMI noise. The balance technique is applied in order to reduce CM EMI noise. With PCB winding coupled inductors, the well-controlled parasitic parameters make the balance technique able to be effective for a uniform reduction of CM EMI noise from 150 kHz to above 20 MHz. In addition, PCB winding based magnetic designs are beneficial to achieving manufacture automation and reducing the labor cost.

SiC-Based High-Frequency Soft-Switching Three-Phase Rectifiers/Inverters

Zhengrong Huang

General Audience Abstract

Power electronics and power conversion are crucial to many applications related to electricity, such as consumer electronics, domestic and commercial appliances, automobiles, data centers, utilities and infrastructure. In today's market, quality and reliability are usually considered as a given; high efficiency (low loss), high power density (small size and weight) and low cost are the main focuses in the design of power electronics products.

In the past several decades, significant achievements in power electronics have been witnessed thanks to the silicon (Si) semiconductor technology, especially the Si power semiconductor devices. Nowadays, the development of Si power semiconductor devices is already close to the theoretical limits of the material itself. Therefore, in order to meet the increasing demands from customers in different applications, wide bandgap (WBG) based power semiconductor devices, namely Gallium Nitride (GaN) and Silicon Carbide (SiC), are becoming attractive because of its great potential compared with their Si counterparts.

In literature, great contributions have already been made to understanding the WBG based power semiconductor devices. It is exciting and encouraging that some of the GaN-based power electronics products featuring high efficiency, high power density and low cost have been

commercialized in consumer electronics applications. However, when pursuing these objectives, previous literature has not shown any applications of high frequency soft switching technology into the high power ac–dc conversion (usually three-phase ac–dc) in a simple way as the low power ac–dc conversion (usually single-phase ac–dc) in consumer electronics products.

The key to achieving high efficiency, high power density and low cost is the high frequency soft switching operation. For single-phase ac–dc systems, the research on the realization of soft switching by control strategies instead of additional physical complexity has been intensively conducted, and this technology has also been adopted in the current industry practice. Therefore, the major achievement of this work is the development of a generalized soft switching control strategy for three-phase ac–dc systems, without adding any physical complexity, which is applicable to the simplest and most conventional three-phase ac-dc circuit topology. The proposed soft switching control strategy features bidirectional (rectifiers/inverters) power conversion, active/reactive power transfer, grid-tied/stand-alone modes, and scalability to multi-channel interleaved operation. Furthermore, with high frequency, the integration of magnetic components with embedded windings in the printed circuit board (PCB) becomes feasible, which is also beneficial to achieving electromagnetic compatibility (EMC) and manufacture automation. Based on the proposed control strategy and design methodology, a SiC-based 25-kW three-phase high frequency soft switching rectifier/inverter is developed for various applications such as electric vehicle (EV) charging stations, uninterruptible power supplies (UPS) and renewable energy based utilities.

To My Family

My parents: Zhiping Huang and Liqun Du

My wife: Zhiting Zhou

Acknowledgments

First and foremost I would like to express my sincerest gratitude to my advisors, Dr. Qiang Li and Dr. Fred C. Lee, for supporting and encouraging me during the past six years. Dr. Li has taught me fundamental knowledge of power electronics, guided me to find research topics, and provided insightful discussions about research problems. Dr. Lee is well known for his rich knowledge in power electronics and rigorous attitude on doing research, from which I have benefited a lot. His passion on academic and challenging spirit on the research have always motivated me to work harder and improve myself.

Joining Center for Power Electronics Systems (CPES) is one of the most important decisions I have made in my life. The six years of my Ph.D. experience has allowed me to better understand the culture of CPES, that is exploring the unknown and pursuing the cutting-edge, and finally shaped me into the researcher I am today.

I would like to thank my committee members, Dr. Dong Dong, Dr. Virgilio Centeno, and Dr. Alfred L. Wicks for their valuable comments and suggestions on my dissertation. I would appreciate all my committee giving me the chance to defend my Ph.D. dissertation on Zoom, which for sure is a unique experience in my life.

I would like to express special thanks to Dr. Zhengyang Liu. I feel so lucky to work with him for the first three years in CPES. He is a responsible mentor, reliable colleague, and great friend. When I came to CPES, he taught me patiently about the software and hardware in power electronics design from the very basics. It is always great pleasure to discuss research problems with him, where I can get a lot of inspirations and suggestions. The beginning of the Ph.D. life is always very challenging. Thanks to Zhengyang, I can get through all these situations.

My special thanks also go to my colleagues, Dr. Furong Xiao and Gibong Son. I used to work with them for one year and two years, respectively. They helped a lot with the development and the validation of key ideas in this work. Without their contributions, it is impossible to achieve so much.

I appreciate the suggestions and supports from CPES faculty and research scientists: Dr. Dushan Boroyevich, Dr. Khai Ngo, Dr. Rolando Burgos, Dr. Guo-Quan Lu, Dr. Yuhao Zhang, Dr. Christina DiMarino, Dr. Mingkai Mu, Dr. Jun Wang, and Dr. Bo Wen.

It is great pleasure to study and work at CPES. I would like to thank all my colleagues in the Power Management Consortium (PMC) group: Dr. Shuilin Tian, Dr. Dongbin Hou, Dr. Xiucheng Huang, Dr. Yang Jiao, Dr. Yuchen Yang, Dr. Syed Bari, Dr. Chao Fei, Xuebing Chen, Dr. Bin Li, Shishuo Zhao, Tao Liu, Virginia Li, Dr. Mohamed Ahmed, Dr. Yi-Hsun Hsieh, Yadong Lyu, Junjie Feng, Rimon Gadelrab, Shuo Wang, Yinsong Cai, Ahmed Nabih, Feiyang Zhu. Owen Jong, Hao Xue, Chunyang Zhao, Zheqing Li, Xin Lou, Feng Jin, Xingyu Chen, Tianlong Yuan, Yugal Gupta, Pranav Raj Prakash, Yizhi Ruan, Dr. Weijing Du, Dr. Yan-Cun Li, Dr. Li Wang, Dr. Kenichiro Tanaka, Dr. Minfan Fu, Dr. Guo Xu, Dr. Rong Xu, Dr. Dong Liu, Dr. Wei Qin, Dr. Shaoliang An, Dr. Hongfei Wu, Dr. Orion Chen, Dr. Hieu Phu Pham, Dr. Guoen Cao and Dr. Zhichang Yuan.

My thanks also go to many other students and visiting scholars I have met in CPES: Dr. Lingxiao Xue, Dr. Zhemin Zhang, Dr. Han Cui, Dr. Fang Chen, Dr. Ming Lu, Dr. Qiong Wang, Dr. Chi Li, Dr. Yincan Mao, Dr. Niloofar Rashidi, Dr. Zichen Miao, Dr. Alinaghi Marzoughi, Dr. Ting Ge, Dr. Bingyao Sun, Dr. Chien-An Chen, Dr. Lujie Zhang, Ye Tang, Ye Fan, Jianghui Yu, Dr. Sungjae Ohn, Yue Xu, Qian Li, Alex Chu, Jiewen Hu, Joseph Kozak, Slavko Mocevic, Victor Turriate, Keyao Sun, Shengchang Lu, Tam Nguyen, Le Wang, Bo Li, Emma Raszmann, Watt

Grace, David Nam, Chris Salvo, Cong Tu, Yu Rong, Ripun Phukan, Lakshmi Ravi, Xiang Lin, Tianyu Zhao, Ning Yan, Ruizhe Zhang, Yuliang Cao, Jian Liu, Minh Ngo, Jack Knoll, Dr. Zeng Liu, Dr. Xiaolong Yue, Dr. Bo Sun, Dr. Benjamin Cheong, Dr. Sizhan Zhou, Dr. Boran Fan, Dr. Cyril Buttay, and too many others to name.

The wonderful staff have made my life and work in CPES more efficient. I sincerely thank Ms. Teresa Shaw, Mr. David Gilham, Ms. Teresa Rose, Ms. Marianne Hawthorne, Ms. Linda Long, Ms. Lauren Shutt, Mr. Dennis Drove, Ms. Na Ren, Ms. Yan Sun, Ms. Audri Cunningham, Mr. Matthew Scanland and Mr. Neil Croy.

During these six years, there are also many friends who have ever helped me in my study and in my life, including but not limited to: Dr. Xiangyu Zhang, Dr. Xiaonan Zhao, Jiaji He, Weizhen Sun and Yudong Xu. I take this chance to thank all of them.

My thanks also go to Power Management Consortium (PMC) in CPES, Virginia Tech, for funding my research in the past six years.

The year 2020 is special due to the widespread pandemic. The working hours and the access to the lab becomes quite different. I would like to thank the administration of CPES for making the lab a safe place for everyone, and ensuring the on-site research progress uninterrupted. I would also like to thank all the people who have coordinated time shifts and shared testing equipment with me in the high power bay B-2. Without your support, my testing cannot be finished so quickly.

If there is one good thing from the pandemic, I would say there is more time that I can spend with my family. I would like to thank my wife, Zhiting Zhou. Thank you for coming into my life and making it special. Every moment I have spent with you is pure joy and happiness. It is your support and encouragement that let me move forward for all these years.

Finally, I am sincerely grateful to my parents and my parents-in-law as well. Thank you for your endless love, support, and encouragement.

Table of Contents

Chapter 1 Introduction 1

1.1 Applications and Challenges of Three-Phase Rectifiers/Inverters 1

1.2 SiC vs. Si: Benefits and Limitations 3

1.3 Critical Conduction Mode (CRM) Soft Switching for SiC 4

1.4 Challenges in Three-Phase CRM 7

1.5 Dissertation Outline 9

Chapter 2 Soft-Switching Technique for Three-Phase Rectifiers/Inverters under Unity Power Factor 12

2.1 Introduction 12

2.2 Proposed Soft Switching Modulation for Three-Phase Rectifiers/Inverters 12

2.3 Quantification of Switching Frequency Variation Range: Its Dependency on Inductance and Device Parasitic Capacitance 21

2.4 Experimental Verifications 28

2.5 Conclusions 34

Chapter 3 Soft Switching Technique under Non-Unity Power Factor for Three-Phase Grid-Tied Inverters 36

3.1 Introduction 36

3.2 Hard Switching Related Issues of the Original Soft Switching Modulation under Non-Unity Power Factor Conditions 37

3.3 Proposed Generalized Soft Switching Modulation Technique for Both Unity and Non-Unity Power Factor Conditions 46

3.4 Experimental Verifications 56

3.5 Conclusions 61

Chapter 4 Interleaving Control and Balance Technique for EMI Noise Reduction . 63

4.1 Introduction 63

4.2 Reduction of DM Noise with Interleaving Control 65

4.2.1 Negative Coupled Inductors for Stability in Interleaved Converters 68

4.2.2 Impact of Interleaving and Negative Coupled Inductors on Switching Frequency Variation Range 74

4.3 Reduction of CM Noise with Balance Technique 82

4.3.1 Review of Balance Technique in Single-Phase Systems and Three-Phase Non-Interleaved Systems 82

4.3.2 Derivation of CM Noise Model for Balance Technique Applied in Three-Phase Interleaved Rectifiers/Inverters 87

4.4 PCB Winding Coupled Inductor Design and Optimization 92

4.4.1 Impact of Balance Technique on Switching Frequency Variation Range 92

4.4.2 PCB Winding Coupled Inductor Design and Optimization Process 101

4.5 Experimental Verifications 114

4.6 Conclusions 120

Chapter 5 Conclusions and Future Work 122

5.1 Conclusions 122

5.2 Future Work 123

Appendix A. Characterization of Time-Domain Switching Waveforms for Minimizing Switching Loss 126

References 146

List of Figures

Fig. 1-1. Commercial product of a 20-kW string PV inverter system. 2

Fig. 1-2. Comparison between a typical Si IGBT device and a typical SiC MOSFET device in terms of: (a) output characteristics; (b) switching energy. 3

Fig. 1-3. Switching frequency distribution under different modulation index conditions with (a) decoupled two-level H-bridge structure [32]. (b) decoupled three-level T-type structure [33]. 9

Fig. 2-1. AC current based DPWM clamping strategy over a whole line cycle. 13

Fig. 2-2. "DPWM + CRM" modulation in the first 60° line-cycle interval. (a) Control diagram for both inverter and rectifier modes. (b) Switching-cycle waveforms in the inverter mode in phase A and phase C with the definitions in (a). 14

Fig. 2-3. With "DPWM + CRM" modulation. (a) Switching frequency distribution in all three phases over a half-line cycle. (b) Switching-cycle waveforms. 16

Fig. 2-4. Typical switching-cycle waveforms with "DPWM + CRM + Fs sync" modulation. 18

Fig. 2-5. Line-cycle operation mode distribution with "DPWM + CRM + Fs sync" modulation under the unity power factor condition. 19

Fig. 2-6. Comparison between switching frequency distributions in phase A over a half-line cycle without and with the synchronization of switching frequency. 20

Fig. 2-7. System operation at the 60 °operating point without the parasitic capacitance of devices: (a) Simulated switching-cycle waveforms in phase A; (b) Circuit operation diagram during on-time; (c) Circuit operation diagram during off-time. 23

Fig. 2-8. System operation during the LC resonance stage at the 60 ° operating point: (a) Circuit operation diagram; (b) Simulated waveforms in phase A; (c) State-plane trajectory. 25

Fig. 2-9. Prototype of the 25 kW SiC-based three-phase bi-directional ac–dc converter. 29

Fig. 2-10. Line-cycle experimental results at full power in the inverter mode. (a) Experimental waveforms of three-phase ac voltages and three-phase grid currents. (b) FFT analysis result of phase A grid current. 30

Fig. 2-11. Switching-cycle experimental waveforms in the inverter mode at the following operating points. (a) Around 5 ° during the CRM. (b) Around 15 ° during the CRM. (c) Around 25 ° during the CRM. (d) Around 5 ° during the DCM. (e) Around 15 ° during the DCM. (f) Around 25 ° during the DCM. 31

Fig. 2-12. Line-cycle experimental results at 85% of full power in the rectifier mode. (a) Experimental waveforms of three-phase ac voltages and three-phase grid currents. (b) FFT analysis result of phase A grid current. 32

Fig. 2-13. Switching-cycle experimental waveforms in the rectifier mode at the following operating points. (a) Around 5 ° during the CRM. (b) Around 15 ° during the CRM. (c) Around 25 ° during the CRM. (d) Around 5 ° during the DCM. (e) Around 15 ° during the DCM. (f) Around 25 ° during the DCM. 33

Fig. 2-14. Simulated loss breakdown with the proposed modulation. 34

Fig. 2-15. Tested efficiency under different load conditions with the proposed modulation at above 300 kHz.34

Fig. 3-1. Line-cycle operation mode with DPWM clamping based on ac reference current under PF = 0.9 (ψ = 26 °) condition; the 1st type hard switching turn-on exists during the intervals 1, 2, and 3 over this half line-cycle (v_A, v_B, and v_C are ac line-to-neutral voltages in phases A, B, and C, respectively; $i_{ref,A}$, $i_{ref,B}$, and $i_{ref,C}$ are ac reference currents in phases A, B, and C, respectively). 38

Fig. 3-2. Switching-cycle waveforms around 70 ° operating point with conventional DPWM clamping under PF = 0.9 (ψ = 26 °) condition; DCM hard switching turn-on occurs in phase C at t_2 instant. (a) Simulation results based on ideal switches. (b) Experiment results for verification (v_{GSA} and v_{GSC} are control switch gate signals in phases A and C, respectively; i_{LA} and i_{LC} are inductor currents in phases A and C, respectively; v_{DSC} is the control switch drain–source voltage in phase C). 39

Fig. 3-3. Equivalent circuit diagram during the DCM dead-time interval (t_0–t_2 in Fig. 3-2) in phase A at around 70 ° operating point under PF = 0.9 (ψ = 26 °) condition. (a) t_0–t_1 interval. (b) t_1–t_2 interval. 40

Fig. 3-4. Simulated switching-cycle waveforms at (a) 40 ° operating point with stable operation; (b) 45 ° operating point with the CRM/DCM transition angle θ_T = 56 ° under PF=0.9 (ψ =26 °) condition; unstable CCM operation occurs (i_{LA} and i_{LC} are inductor currents in phases A and C, respectively). 42

Fig. 3-5. Experiment waveforms around 45 ° operating point with the CRM/DCM transition angle θ_T = 56 ° under PF = 0.9 (ψ = 26 °) condition to verify unstable CCM operation in phase A (v_{GSA} and v_{GSC} are

control switch gate signals in phases A and C, respectively; i_{LA} and i_{LC} are inductor currents in phases A and C). 43

Fig. 3-6. Line-cycle operation mode with DPWM clamping based on ac reference current under PF = 0.9 (ψ = 26 °) condition; the 2nd type hard switching turn-on exists during the intervals 4, 5, and 6 over this half line-cycle (v_A, v_B, and v_C are ac line-to-neutral voltages in phases A, B, and C, respectively; $i_{ref,A}$, $i_{ref,B}$, and $i_{ref,C}$ are ac reference currents in phases A, B, and C, respectively). 44

Fig. 3-7. (a) Equivalent circuit during the DCM dead-time interval after the control switch is turned off and the SR is turned on in phase B. (b) Simulated switching-cycle waveforms around 70 ° operating point with modified DPWM clamping under PF = 0.9 (ψ = 26 °) condition to indicate that DCM hard-switching turn-on is avoided, especially $t_1 - t_2$ is corresponding to panel (a) (V_{dc} is the dc bus voltage; v_C is the ac line-to-neutral voltage in phase C; v_{GSB} and v_{GSC} are the control switch gate signals in phases B and C, respectively; i_{LB} and i_{LC} are inductor currents in phases B and C, respectively). 47

Fig. 3-8. (a) Comparison of simulated DCM turn-on loss between current-based DPWM clamping (without improvement) and voltage-based DPWM clamping (with improvement) at different PF values. (b) Tested loss reduction from current-based DPWM clamping to voltage-based DPWM clamping at different PF values. 48

Fig. 3-9. Simulated switching-cycle inductor current waveforms at three example line-cycle operating points: (a) θ_1, (b) θ_2, and (c) θ_3 ($0 < \theta_1 < \theta_2 < \theta_3 < 60$ °; PF = 0.9 (ψ = 26 °). The optimal DCM/CRM transition angle $\theta_T^* = \theta_2$ because of the simultaneous inductor current zero crossings and i_{LA} and i_{LC} are the inductor currents in phases A and C, respectively). 50

Fig. 3-10. Comparison between simulated and calculated optimal CRM/DCM transition angles θ_T^* under different PF operating conditions. 50

Fig. 3-11. (a) Simulated CCM turn-on loss with different CRM/DCM transition angles θ_T under PF = 0.9 (ψ = 26 °) condition. (b) Tested additional loss with different CRM/DCM transition angles θ_T when compared with $\theta_T = \theta_T^* = 40$ ° under PF = 0.9 (ψ = 26 °) condition. 51

Fig. 3-12. Operation mode with the generalized DPWM + CRM + Fs sync modulation concept under PF=0.9 ($\psi = \pm 26$ °) conditions to show operational symmetry. 53

Fig. 3-13. Switching frequency variation over a half line-cycle under different PF conditions. 54

Fig. 3-14. Simulated device loss breakdown under different PF operating conditions. 56

Fig. 3-15. Line-cycle experimental results at PF = 0.9. (a) Lagging condition. (b) Leading condition. (v_A, v_B, and v_C are three-phase ac line-to-neutral voltages; i_{gA}, i_{gB}, and i_{gC} are three-phase grid currents; hereinafter the same). 57

Fig. 3-16. Switching-cycle experimental waveforms under PF = 0.9 (lagging) condition at the following operating points. (a) Around 10 °in phase A. (b) Around 30 °in phase A. (c) Around 50 °in phase A. (d) Around 10 °in phase C. (e) Around 30 °in phase C. (f) Around 50 °in phase C. (In each figure, v_{GS} is the control switch gate signal; v_{DS} is the control switch drain–source voltage; i_g is the grid current; i_L is the inductor current; hereinafter the same). 58

Fig. 3-17. Line-cycle experimental results at PF = 0.8. (a) Lagging condition. (b) Leading condition. 59

Fig. 3-18. Switching-cycle experimental waveforms under PF = 0.8 (lagging) condition at the following operating points. (a) Around 10 °in phase A. (b) Around 30 °in phase A. (c) Around 50 °in phase A. (d) Around 10 °in phase C. (e) Around 30 °in phase C. (f) Around 50 °in phase C. 60

Fig. 3-19. Tested efficiency at 12.5 kVA power under different PF values with the original and proposed improved modulation at above 300 kHz. 61

Fig. 4-1. Propagation path of the conducted EMI noise. 64

Fig. 4-2. Circuit diagram of the two-channel interleaved three-phase ac-dc converter. 66

Fig. 4-3. Line-cycle simulation waveforms of total inductor current in phase A: (a) without interleaving (b) with two-channel interleaving. 67

Fig. 4-4. Switching-cycle simulation waveforms of total and individual inductor current in each phase: (a) without interleaving (b) with two-channel interleaving. 68

Fig. 4-5. Line-cycle simulation waveforms of individual inductor current in phase A: (a) without interleaving (b) with two-channel interleaving 69

Fig. 4-6. Line-cycle and switching-cycle inductor current waveforms in rectifier mode operation of the two-channel interleaved three-phase ac-dc converter. 69

Fig. 4-7. Variation of inductor current slew rate prior to zero crossing over the first 30 ° line-cycle interval: comparison between interleaved inverter mode and interleaved rectifier mode. 71

Fig. 4-8. Typical switching-cycle inductor current waveforms under (a) Sequence 1: DCM dead-time is short than half of switching period; (b) Sequence 2: DCM dead-time is longer than half of switching period. 71

Fig. 4-9. Two-channel interleaved three-phase ac-dc converter with negative coupled inductors. 72

Fig. 4-10. Variation of inductor current slew rate prior to zero crossing over the first 30 °line-cycle interval at interleaved rectifier mode: comparison between negative coupled case (-0.5 coupling coefficient) and non-coupled case. 73

Fig. 4-11. Switching-cycle inductor current waveforms in the rectifier mode operation of two-channel interleaved three-phase converter under different coupling coefficient (α): (a) α = 0; (b) α = -0.4; (c) α = -0.5. 74

Fig. 4-12. Switching frequency variation under different coupling coefficient values (α). 75

Fig. 4-13. System operation in phase A at the 60 °operating point without the parasitic capacitance of devices (a) Simulated switching-cycle waveforms; (b) Circuit diagram showing the operation during Stage I (on-time). 76

Fig. 4-14. Circuit diagram during the LC resonance stage at the 60 °operating point. 78

Fig. 4-15. Equivalent transformation from a coupled inductor to non-coupled inductors. 79

Fig. 4-16. Wheatstone bridge structure for illustrating balance concept. 83

Fig. 4-17. Equivalent CM EMI noise model for original circuit topology. 84

Fig. 4-18. Equivalent sub circuit from Fig. 4-17 for original circuit topology. 85

Fig. 4-19. Modified circuit topology with additional inductors L_3 and L_4 85

Fig. 4-20. Equivalent sub circuit for modified circuit topology. 86

Fig. 4-21. Balance technique applied into a three-phase non-interleaved NPC inverter. 87

Fig. 4-22. Interleaved three-phase ac–dc converter topology with balance technique applied. 88

Fig. 4-23. Equivalent CM EMI noise model for the topology in Fig. 4-22. 88

Fig. 4-24. Equivalent sub circuit of the model in Fig. 4-23. 89

Fig. 4-25. Switching frequency variation in phase A over a line cycle with balance. 93

Fig. 4-26. System operation in phase A at the 60 °operating point without the parasitic capacitance of devices (a) Simulated switching-cycle waveforms; (b) Circuit diagram showing the operation during Stage I (on-time). 94

Fig. 4-27. Definition of the self inductance and the mutual inductance in phase A. 96

Fig. 4-28. Circuit diagram during the LC resonance stage at the 60 °operating point. 97

Fig. 4-29. Simplified circuit diagram during the LC resonance stage at the 60 °operating point. 98

Fig. 4-30. Equivalent circuit diagram during the LC resonance stage at the 60 °operating point. 98

Fig. 4-31. PCB winding coupled inductor structure for each phase. 102

Fig. 4-32. The required value of self inductance under different coupling coefficient values to achieve 300-kHz minimum switching frequency. 103

Fig. 4-33. Magnetic circuit of the PCB winding coupled inductor structure in Fig. 4-31. 103

Fig. 4-34. The calculated half-line-cycle and zoomed in switching-cycle flux in the left leg and the center leg of the inductor structure in Fig. 4-31. 105

Fig. 4-35. Cross section view of the PCB winding coupled inductor. 106

Fig. 4-36. An example of finite element analysis (FEA) simulations in Ansys Maxwell: (a) meshes in the PCB windings and the magnetic cores; (b) simulated flux density distribution in the magnetic cores at a certain instant. 107

Fig. 4-37. Core loss density tested results under sinusoidal excitations with different core materials under (a) 300 kHz; (b) 500 kHz; (c) 1 MHz. (red: ML27D, Hitachi Metal; black: 3F36, Ferroxcube; blue: DMR51, DMEGC; green: ML95S, Hitachi Metal) 110

Fig. 4-38. Core loss density tested results under sinusoidal excitations with different ac flux density magnitude and with different dc bias values at (a) 300 kHz; (b) 500 kHz; (c) 1 MHz. 111

Fig. 4-39. *B*-*H* curve of ML95S. 112

Fig. 4-40. Calculated inductor loss and footprint under different pairs of (*r*, *a*). (a) inductor winding loss; (b) inductor core loss; (c) inductor total loss and inductor footprint. 113

Fig. 4-41. Plot of inductor loss vs. inductor footprint with minimum inductor loss for each footprint. 114

Fig. 4-42. Line-cycle and switching-cycle experiment waveforms of individual and total inductor current in phase A in two-channel interleaved rectifier mode operation. 115

Fig. 4-43. Comparison of DM EMI noise testing results between non-interleaved operation and two-channel interleaved operation under the same power. 115

Fig. 4-44. : Generation #2 of 25-kW SiC-based three-phase ac-dc converter prototype featuring PCB winding coupled inductors 116

Fig. 4-45. Switching-cycle experimental waveforms in phase A tested on Generation #2 hardware prototype at the following operating points: (a) Around 10 °at DCM in rectifier mode. (b) Around 30 °at boundary of DCM/CRM in rectifier mode. (c) Around 50 °at CRM in rectifier mode. (d) Around 10 °at DCM in inverter mode. (e) Around 30 °at boundary of DCM/CRM in inverter mode. (f) Around 50 °at CRM in inverter mode. 118

Fig. 4-46. Comparison of CM EMI noise testing results on Generation #2 hardware prototype: using litz-wire inductors (without balance) vs. using PCB winding inductors (with balance). 119

Fig. 4-47. Tested efficiency of Generation #2 hardware prototype: comparison between using PCB winding inductors and using litz-wire inductors. 120

Fig. A- 1. Circuit diagram of three-phase ac–dc structure for operation analysis in the inverter mode. 127

Fig. A- 2. Typical switching-cycle waveforms in phase A and phase C during the first 30 °line-cycle interval in the inverter mode. 128

Fig. A- 3. State-plane trajectory between v_{DSA1} and i_{LA} right before t_1 instant in Fig. A- 2. 129

Fig. A- 4. Time-domain calculated results of v_{DSC1} (control switch drain–source voltage in phase C) values during t_1−t_2 interval in Fig. A- 2, with fixed θ = 15 °but with different φ values as an example. (a) With four different φ values. (b) With all the possible φ values. 131

Fig. A- 5. State-plane trajectory between v_{DSA1} and i_{LA} right after t_2 instant in Fig. A- 2. 132

Fig. A- 6. Circuit diagram of the three-phase ac–dc structure for operation analysis in the rectifier mode. ..133

Fig. A- 7. Typical switching-cycle waveforms in phase A and phase C during the first 30 °line-cycle interval in the rectifier mode. (a)Without off-time extension. (b) With off-time extension. 134

Fig. A- 8. (a) 3-D distribution of the worst-case valley point value of v_{DSC2} (v_M), during the fourth − order LC resonance period in the rectifier mode, at different operating points (θ, from 0 to 30°) and with different negative current values at t_1 instant $i_{LC}(t_1)$. (b) Contour of (a). 137

Fig. A- 9. Fourth-order equivalent LC resonance circuit during the first 60° line-cycle interval. 139

Fig. A- 10. Distribution of the line-to-neutral voltage in the phase with DCM (v_{DCM}) and that in the phase with CRM (v_{CRM}) during the first 60° line-cycle interval. (a) Under PF = 1 condition. (b) Under PF = 0.9 (ψ = 26°) condition.....140

Fig. A- 11. Switching-cycle waveforms in the phase operating at DCM (phase A), under PF = 0.9 (ψ = 26°) condition, at (a) 10° operating point with valley drain–source voltage turn-on; (b) 35° operating point with ZVS turn-on (v_{GS} is the gate signal of the control switch; i_L is the inductor current; v_{DS} is the drain–source voltage of the control switch). 143

Fig. A- 12. Switching-cycle waveforms in the phase operating at CRM, under PF = 0.8 (ψ = 37°) condition, at 44° operating point at (a) full-load condition with non-ZVS; (b) 75% load condition with ZVS (v_{GS} is the gate signal of the control switch; i_L is the inductor current; v_{DS} is the drain–source voltage of the control switch). 144

Fig. A- 13. Distribution of the minimum required negative current (i_{neg_req}) between the 40° and the 45° operating point for achieving ZVS turn-on under any load condition (initial condition angle φ). 145

List of Tables

Table 2-1 Verification of Proposed Analytical Model 27

Table 2-2 Parameters of the Prototype 30

Table 4-1 Verification of Proposed Analytical Model for Interleaved Operation 80

Table 4-2 Verification of Proposed Analytical Model for Interleaved Operation with Balance 101

Table 4-3 Selected Design Point of PCB Winding Coupled Inductors 114

Table 4-4 Parameters of the Generation #2 Prototype 117

Chapter 1 Introduction

1.1 Applications and Challenges of Three-Phase Rectifiers/Inverters

Electrical energy is becoming more and more important for human life all over the world, and three-phase rectifiers/inverters are widely used in grid-tied applications, such as the chargers in electric vehicle (EV) charging systems, power factor correction (PFC) converters in the uninterruptible power supplies (UPS) or data centers, for storage and utilization of electrical energy from power grids, and the photovoltaic (PV) inverters in solar energy systems for harvesting electrical energy and the interface with power grids. These converters are also seen in stand-alone applications such as the auxiliary converters in the locomotives in order to supply the power for cooling fans, compressors and motor blowers on trains.

Take the EV charging systems as an example. Modular approach is widely adopted in this application in order to construct a higher power EV charging systems for quicker charging. In Tesla's 145-kW super chargers, there are 12 modules in parallel, with each module handling about 12 kW power [1], [2]. Therefore, several tens of kW is an attractive power level in this application. Typically a two-stage structure is used in this application, including one three-phase ac–dc stage as a front-end PFC converter and one dc–dc stage for isolation and regulation. The research in this dissertation is mainly focused on the three-phase ac–dc stage.

In this application, within a certain limited space designated for the chargers, quick charging is always desired in order to shorten the charging time. Meanwhile, the high system efficiency is also required since it saves the energy. According to the current industry practice, with a power rating between 10 and 30 kW, the power density is around 30 W/in^3 and the system efficiency is around 95% [3] – [6]. It is very hard to further improve the power density since these systems are

designed based on silicon (Si) power semiconductor devices and the operating switching frequency is usually up to 30 kHz, which has been close to the frequency limit of this type of power semiconductor devices in order to maintain relatively high efficiency and low switching loss.

For PV inverter systems, several tens of kW power level is attractive in commercial applications such as the rooftop PV systems for garages and supermarkets. According to current industry practice, with a power rating between 10 and 50 kW, the system efficiency is around 98% while the power density is below 15 W/in^3 [7] – [10], which is also due to the Si power semiconductor devices with limited operating switching frequency.

The reason of the limited power density is that low switching frequency operation makes the passive components, especially the magnetic components bulky. Fig. 1-1 shows a picture of a commercial 20-kW string PV inverter system. The magnetic components highlighted in the yellow boxes, including the chokes in the EMI filters, inductors and transformers in the two power stages, occupy around 30 – 40% of the total system volume.

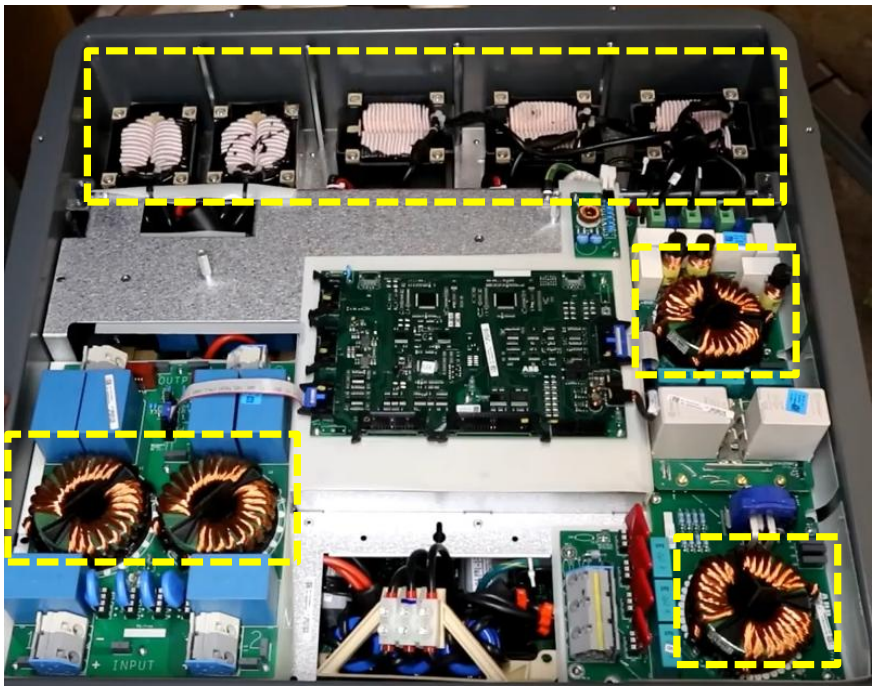
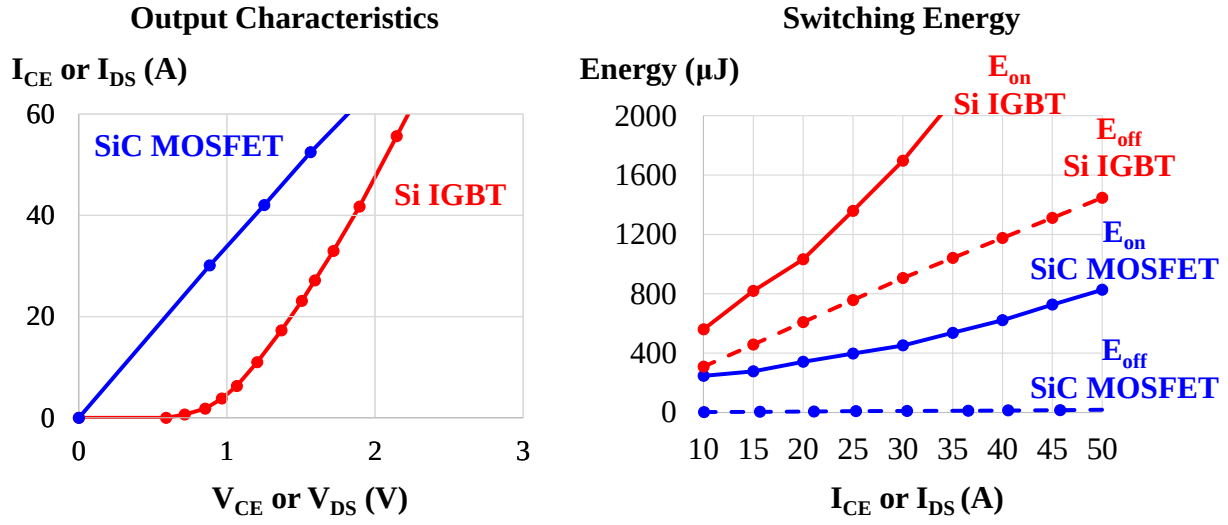


Fig. 1-1. Commercial product of a 20-kW string PV inverter system.

In addition, in the current industry practice, the magnetic components are usually wound by hands using litz wire or copper wires, which indicates a labor-intensive manufacture process and contributes to high labor cost.

1.2 SiC vs. Si: Benefits and Limitations

The recently emerging wide-band-gap (WBG) power semiconductor devices, including gallium nitride (GaN) and silicon carbide (SiC), are expected to be promising candidates for high frequency power converter design. Compared with their Si counterparts, WBG power semiconductor devices have lower specific on-state-resistance, faster switching speed and lower switching energy. Fig. 1-2 (a) and (b) show the comparison between a typical Si IGBT and a typical SiC MOSFET, with the same breakdown voltage (1.2 kV) and similar current rating (around 40 A at 100 ℃), from output characteristics and switching energy points of view, respectively.



(a) (b)

Fig. 1-2. Comparison between a typical Si IGBT device and a typical SiC MOSFET device in terms of: (a) output characteristics; (b) switching energy.

Therefore, it is expected that with WBG power semiconductor devices, systems can operate at higher switching frequency to achieve higher power density due to the size reduction of filters made up of passive components, and even higher system efficiency. Between GaN and SiC, the latter one is more popular in current research conducted for tens of kW power converter applications.

In order to develop SiC-based three-phase ac–dc converters, direct substitution of SiC devices for traditional Si devices is a common practice reported in the literature [11]–[15]. In [11], SiC JFETs are used instead of traditional Si devices and up to 98.8% peak efficiency is achieved. However, the benefit of SiC devices is not fully utilized if devices are still operating at relatively low switching frequency, which makes the system power density almost the same as vast majority of commercial products, but with an increased system cost because of SiC devices. In [13], a 60 kW three-phase two-stage all-SiC PV inverter system is developed. With 75 kHz switching frequency at the dc–dc stage and 50 kHz switching frequency at the dc–ac stage, 27 W/in^3 power density is achieved, which is two to three times of commercial Si-based products. However, on the other hand, at high switching frequency operation, the increased switching loss becomes a main challenge for high efficiency with continuous conduction mode (CCM) hard switching operation. In [15], hard switching operation makes the system peak efficiency drop from 99% at 16 kHz switching frequency to 97% at 160 kHz switching frequency, which is a significant sacrifice on system performance.

1.3 Critical Conduction Mode (CRM) Soft Switching for SiC

According to the above discussion, CCM hard switching operation brings high switching loss, which is a main drawback of pushing the switching frequency to several hundreds of kHz for SiC-

based systems. Therefore, soft switching is necessary to achieve high efficiency at high-frequency operation.

In the past, various soft-switching techniques for three-phase rectifiers/inverters have been studied. The resonant dc link (RDCL) inverter and the active clamped resonant dc link (ACRDCL) inverter are the well-known dc-side soft-switching topologies [16], [17]. However, they suffer from severe voltage stress (> 2.5 times the dc-bus voltage for the RDCL and 1.3 – 1.4 times the dc-bus voltage for the ACRDCL) across the devices. The Auxiliary Resonant Commutated Pole inverter is an important achievement in ac-side soft-switching inverter and has extended its applications into three-level topology [18], [19]. However, the count of the devices is doubled with this kind of ac-side soft-switching topologies. Most recently, based on the RDCL and ACRDCL soft switching concepts, a series of more simplified soft-switching topologies and related modulation based on traditional sinusoidal pulse width modulation (SPWM), space vector modulation (SVM) etc. for three-phase rectifiers/inverters are developed by Dr. Xu *et al*. [20] – [24]. In [23], the soft switching technique is achieved in a SiC-based three-phase three-wire inverter. The tested peak efficiency of the inverter is 98.7% with 300 kHz switching frequency. In [24], similar technique is applied into a SiC-based three-phase four-wire topology and the tested peak efficiency is 98.3% with 150 kHz switching frequency. However, additional components including an inductor, seven capacitors and an active switch are still required, which add to the complexity and cost of the whole system, and also bring additional loss and make the efficiency decrease by around 0.3 – 0.4% in both cases. In addition, with additional components, the critical decoupling power loop for each phase leg becomes larger. This leads to extra parasitic inductance and contributes to severe voltage ringing across the devices at switching instants, which is an inherent drawback for this kind of dc-side soft switching topologies. Although in [23] a customized

7-in-1 SiC module is well developed and proved to be able to reduce the voltage ringing across the devices by at least 50%, the limitation lies in the lack of flexibility compared with using discrete power semiconductor devices and standard packages.

For SiC MOSFET power semiconductor devices, the per-switching-cycle turn-off energy is almost negligible compared with the relatively high per-switching-cycle turn-on energy [25]–[27], which is also evident in Fig. 1-2. Therefore, this unique feature makes zero-voltage-switching (ZVS) soft switching turn-on preferable because the dominant turn-on switching loss at high switching frequency operation is able to be eliminated completely, while only the very small portion of turn-off switching loss is left even at high switching frequency operation. In order to realize the ZVS soft switching turn-on, critical conduction mode (CRM), that is, the boundary mode between CCM and discontinuous conduction mode (DCM), becomes more attractive for SiC-based systems due to its simplicity without bringing any additional physical complexity into the entire system [28], [29]. In CRM, the inductor current is controlled so as to be able to reach zero in each switching cycle. After the inductor current reaches zero, all the device channels and body diodes are open and LC resonance occurs between the inductor and the device output capacitance. During this LC resonance period, there are chances for the drain-to-source voltage of the active switch to go down to zero and ZVS is achievable, indicating the turn-on loss is eliminated. When compared with the CCM hard switching operation, although there is an increase in the turn-off loss and in the conduction loss at CRM operation due to the increased inductor current ripple, the significant reduction in turn-on loss makes up for the penalty. With this ZVS soft switching, the switching loss of the devices becomes small and thus high efficiency is still achievable, even when the system is operating at hundreds of kHz high switching frequency.

Therefore, ZVS soft switching is the key factor for SiC-based systems to achieve high efficiency at high switching frequency operation, and CRM operation is the simplest way to achieve this soft switching and becomes the preferred operation mode.

In [27], [30], [31], high-frequency CRM control combined with average current regulation is proposed to achieve ZVS soft switching and good power factor on a 6.6 kW single-phase bi-directional ac–dc converter. Experiment results show that with this high-frequency CRM control, 98.5% peak efficiency is achieved with switching frequency above 300 kHz. Therefore, the CRM soft switching is very promising for achieving both the high efficiency and high power density, and is to be extended to three-phase ac–dc systems for higher power applications.

1.4 Challenges in Three-Phase CRM

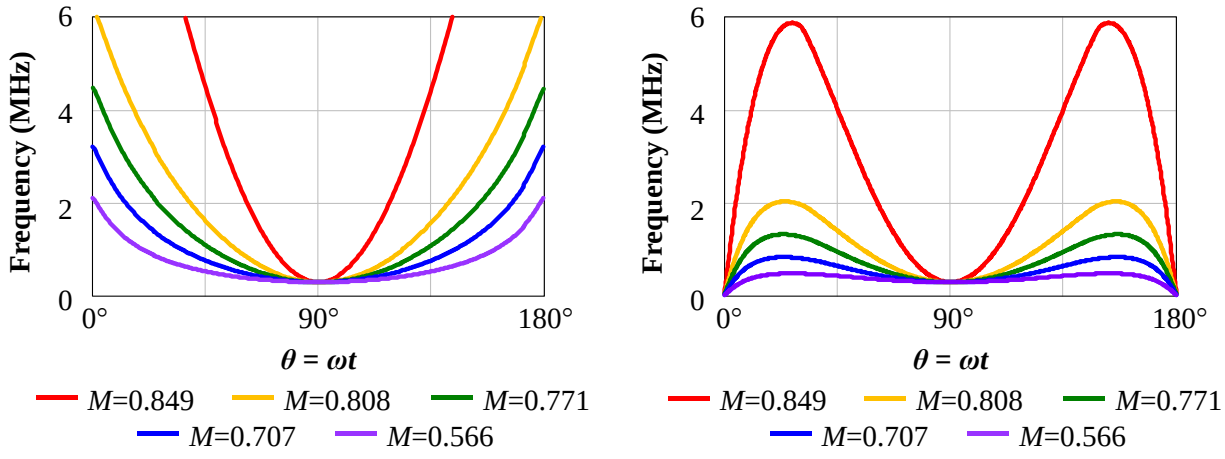
For typical three-phase ac–dc systems, there are only two control freedoms for ac currents due to the fact that the summation of ac currents in all three phases is always zero. Therefore, it is in conflict with the requirement that all three phases need to be independently controlled for the system to operate at CRM, which is the main challenge for extending the CRM control from single phase systems to three-phase ac–dc systems. In order to avoid this constraint, one method reported in the literature is to add a third control freedom by using split capacitors at the dc side and connecting the dc side midpoint of the split capacitor branch to the ac side neutral point. This method is able to be applied into different topologies such as the two-level H-bridge structure [32] and the three-level T-type structure [33]. With this connection, three phases are able to be decoupled so that each phase runs independently at CRM operation. In other words, it becomes a three-phase four-wire systems. Bidirectional operation is still allowed in these three-phase four-wire systems.

This method works well at low modulation index conditions with tens of kHz switching frequency as shown in [32] and [33], where the modulation index is defined as the ratio of the ac line-to-line peak voltage value to the dc voltage value (hereinafter "*M*"). However, when this method is applied into high modulation index conditions with hundreds of kHz high switching frequency operation, it shows an extremely wide switching frequency variation range. Under a typical operating condition (the dc voltage V_{dc} = 800 V, the ac line-to-line RMS voltage $V_{ac,\ L\text{-}L}$ = 480 V, M = 0.849, power factor PF = 1), if the minimum switching frequency with highest current ripple (the middle of each half line cycle) is 300 kHz, the maximum switching frequency in a half line cycle reaches around 13 MHz with the decoupled two-level H-bridge structure and around 6 MHz with the decoupled three-level T-type structure.

Under different modulation index conditions, the simulated switching frequency variation over a half line cycle with these two topologies are shown in Fig. 1-3. Here in order to more clearly identify or specify different operating points in one line cycle, $\theta = \omega t$ is used and defined as the line-cycle phase angle with the unit of degree. (Different θ values indicate different line-cycle operating points; θ = 0 is defined as the negative-to-positive zero crossing point of ac line-to-neutral voltage in phase A; hereinafter the same) The switching frequency variation is the same no matter if it is at inverter mode operation or it is at rectifier mode operation. In the simulation, practical power semiconductor devices are selected based on the capability of handling tens of kW system power and the output capacitance of devices is considered. Here the inductance value is properly designed to make sure the minimum switching frequency is 300 kHz in each case for a fair comparison. It can be seen that the switching frequency variation range becomes wider as the modulation index goes higher, and it becomes extremely sensitive to the modulation index value when the value is above 0.8 with these two topologies. Although the CRM ac–dc converter systems

intrinsically feature the line-cycle time-variant switching frequency, a wide switching frequency variation range leads to high switching-related loss and difficulty in system design.

In addition, with proper modulation, typical three-phase ac–dc systems are able to operate normally up to the unity modulation index, which is beneficial to lowering the dc side voltage as well as the voltage stress of devices at a given ac side voltage. However, for the aforementioned decoupled CRM three-phase four-wire topologies, normal operation cannot be achieved if the modulation index is above 0.866, which is limited by the fact that the equivalent dc voltage should be always no lower than the equivalent ac voltage for the equivalent decoupled single-phase topology. In summary, there are some limitations for the abovementioned decoupled CRM three-phase four-wire topologies to be applied into high modulation index operating conditions.



(a) (b)

Fig. 1-3. Switching frequency distribution under different modulation index conditions with (a) decoupled two-level H-bridge structure [32]. (b) decoupled three-level T-type structure [33].

1.5 Dissertation Outline

In Chapter 1, the research background is introduced and the challenges are identified. Due to the significant advantages over Si power semiconductor devices, SiC power semiconductor

devices are to be used for developing high-frequency three-phase rectifier/inverter systems. According to the feature of switching performance of SiC power semiconductor devices, ZVS soft switching turn on is desired. After compared with other soft switching techniques, CRM is preferred since the soft switching is achieved purely by control without adding any physical complexity into the system. The state-of-the-art three-phase CRM control and the limitations are introduced in this chapter.

In Chapter 2, the CRM-based soft switching modulation technique is proposed for three-phase rectifiers/inverters, which overcomes the limitations mentioned in Chapter 1. Decoupled CRM-based control and narrow switching frequency variation range are achieved with the proposed soft switching modulation technique. The switching frequency variation range is quantified and its dependency on the inductance and on the device parasitic capacitance is derived. The benefits from the proposed soft switching modulation technique is experimentally verified.

In Chapter 3, the above CRM-based soft switching modulation technique is improved for non-unity power factor conditions in order to achieve soft switching for grid-tied inverter related applications, and a generalized modulation concept is summarized for both the unity and non-unity power factor conditions. Similarly the experimental verifications are provided.

In Chapter 4, in order to overcome the high EMI noise brought by the CRM operation and by the fast switching of SiC devices, two-channel interleaving is applied in order to reduce the DM EMI noise, and balance technique is applied in order to reduce the CM noise. In order to achieve effective CM noise reduction with balance, PCB winding coupled inductors are designed and optimized. The reduction of EMI noise is experimentally validated.

In Chapter 5, the dissertation is summarized and concluded, and some research topics are provided as the future work.

The analysis of circuit operation and the characterization of time-domain waveforms for minimizing the switching loss is included in the Appendix, for both the unity power factor and non-unity power factor operating conditions.

Chapter 2 Soft-Switching Technique for Three-Phase Rectifiers/Inverters under Unity Power Factor*

2.1 Introduction

The CRM-based soft switching modulation technique is proposed in this chapter for the unity power factor condition. First, the process of exploring and developing the soft-switching modulation technique is presented step by step. Then, under the CRM-based operation, the dependence of switching frequency variation range on the inductance and on the device parasitic capacitance is quantified for the design of system parameters. Finally, the experimental verifications are provided. Due to the complex mathematical derivations and for the sake of brevity, in the Appendix, the operational principles are analyzed and the time-domain switching waveforms are quantitatively characterized during the LC resonance period, which is key to achieving soft switching and to minimizing the switching loss.

2.2 Proposed Soft Switching Modulation for Three-Phase Rectifiers/Inverters

According to the literature, discontinuous pulse width modulation (DPWM) has been commonly used in three-phase three-wire systems [34], [35]. With DPWM, at any operating point during the whole line cycle, switching actions only occur in two phases every switching cycle, while either the top or the bottom switch in the third phase is always on. In order words, one phase is clamped to either the positive or negative dc bus, while the other two phases operate at high-frequency pulse width modulation (PWM). Although there are many different DPWM clamping

strategies as summarized in [35] considering different design targets, under the unity power factor condition, the most commonly adopted strategy is to clamp the phase with the highest amplitude of ac reference current (i_{ref}), which avoids the switching actions at relatively high current over each line cycle and thus features the reduction of switching loss. Whether this phase is clamped to the positive or the negative dc bus is determined by the polarity of the ac reference current. This clamping strategy over a whole line cycle is shown in Fig. 2-1. Taking the first 60 ° line-cycle interval as an example, phase B is clamped to the negative dc bus, which is denoted as "B → N".

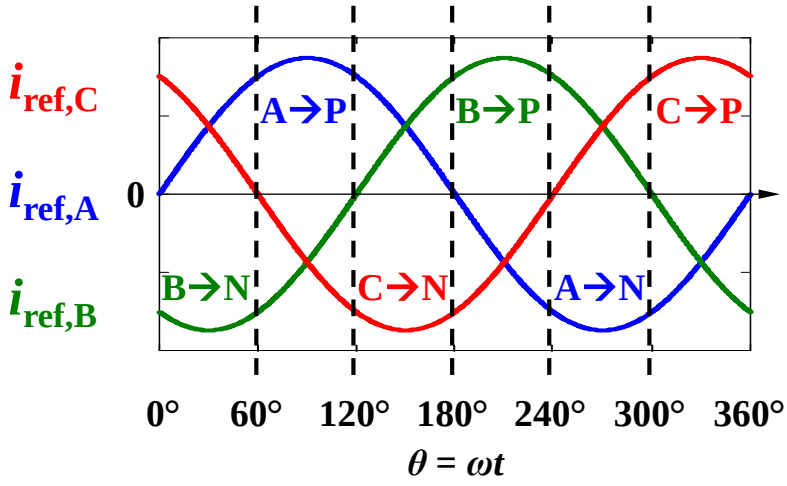
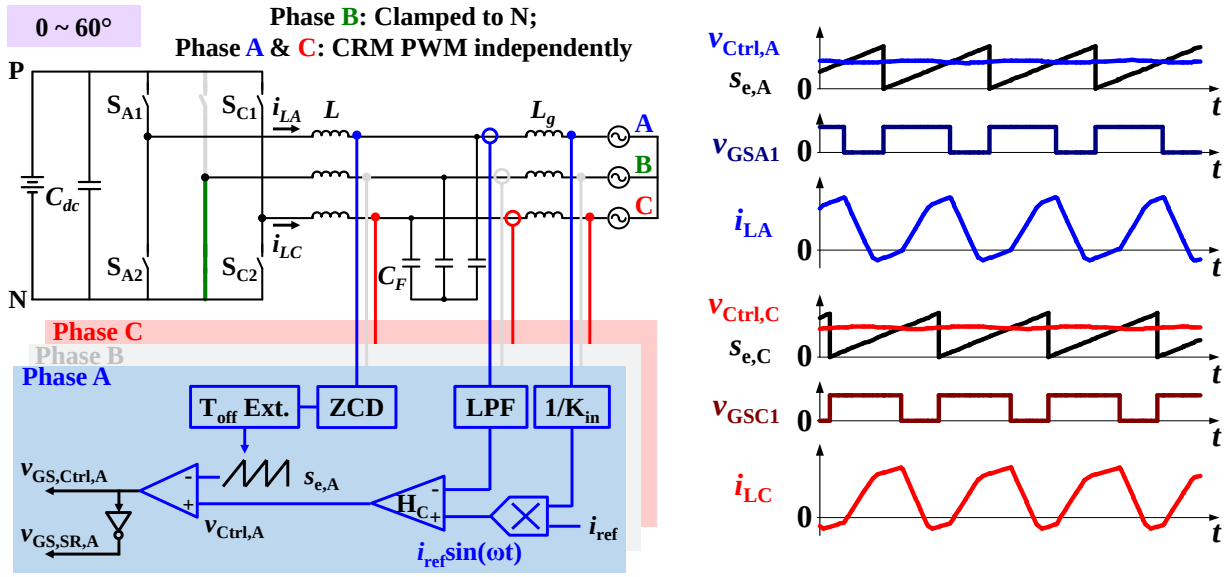


Fig. 2-1. AC current based DPWM clamping strategy over a whole line cycle.

In this application, besides the more obvious benefits of the reduction in switching loss, the more important point to mention is that DPWM provides the opportunity to decouple three phases from the control point of view. Since the phase operating at the clamping mode is uncontrolled, the two control freedoms in the three-phase three-wire ac–dc systems are able to be shared by the other two phases, and independent control in these two phases becomes achievable. Therefore, by utilizing the concept of DPWM clamping to decouple the control of the three-phase systems, making two phases independently controlled at CRM operation (hereinafter "DPWM + CRM"), ZVS soft-switching turn-on can be achieved in these two phases.

With the "DPWM + CRM" modulation, the operation repeats itself every 60° line-cycle interval, except that the operation mode exchanges among all three phases depending on the DPWM clamping strategy. Therefore, here take the first 60 ° line-cycle interval as an example to illustrate the concept of this control. The corresponding control diagram is shown in Fig. 2-2(a) based on the three-phase two-level H-bridge structure with an LCL-type harmonic filter to interface with the grid. There is an individual control block for each phase to determine high-frequency switching actions, as shown in the rectangular shaded area below the circuit diagram. All three control blocks are identical to each other. However, since phase B is clamped, the control block for phase B is temporarily inactive (with the color gray), while phase A and phase C are controlled at the CRM independently according to the individual control block.



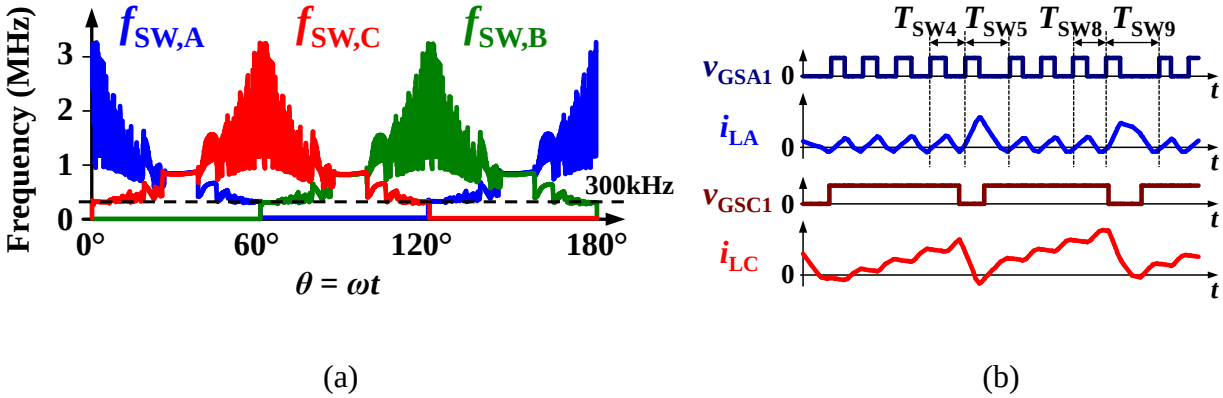
(a) (b)

Fig. 2-2. "DPWM + CRM" modulation in the first 60° line-cycle interval. (a) Control diagram for both inverter and rectifier modes. (b) Switching-cycle waveforms in the inverter mode in phase A and phase C with the definitions in (a).

The detailed parts in each control block is referred from [27]. In the control blocks for phase A and phase C, the zero crossing detector (ZCD) senses the inductor current zero crossing point, and the off-time extender (T_{off} Ext.) provides extra conduction time for the synchronous rectifier (SR) switch (S_{A2}, S_{C2} in the inverter mode, while S_{A1}, S_{C1} in the rectifier mode) after the inductor current zero crossing occurs to provide some amount of negative inductor current when necessary, and thus, ZVS turn-on of the control switch (S_{A1} , S_{C1} in the inverter mode, while S_{A2}, S_{C2} in the rectifier mode) is achievable. The constant-slope sawtooth signal s_e is reset to zero once every switching cycle after the inductor current zero crossing is sensed by the ZCD and extra off-time is applied by the off-time extender. Meanwhile, the control signal v_{Ctrl} is generated from the average current loop compensator H_C. The intersections between s_e and v_{Ctrl} determine the switching instants of the control switch, and when v_{Ctrl} is higher than s_e, the control switch is during the on state. The gate signal of the SR switch ($v_{GS,SR}$) is complementary to that of the control switch ($v_{GS,Ctrl}$) when ignoring the dead-time. Phase A and phase C are controlled independently according to the above-mentioned control concept of the CRM with average current regulation. Fundamentally, in each of the two phases independently controlled at the CRM, for the control switch, the ZCD and off-time extender determine the turn-on instant to achieve ZVS, and the average current controller determines the turn-off instant to achieve sinusoidal ac average current. The switching-cycle waveforms in the inverter mode during the first 60 ° line-cycle interval are shown in Fig. 2-2(b).

As shown in Fig. 2-3(a), with "DPWM + CRM" modulation and 300 kHz minimum switching frequency, peak switching frequency is around 3 MHz. Although the switching frequency variation range with this modulation is narrower than the one with decoupled CRM control on the structures in [32] and [33] under the aforementioned high modulation index condition (V_{dc} = 800 V, $V_{ac,\ L\text{-}L}$

= 480 V, M = 0.849, PF = 1), the switching frequency variation range is still wide. Additionally, high-frequency oscillation exists in Fig. 2-3(a), which is caused by the asynchronous switching frequencies in the two phases operating at the CRM and the interaction between these two phases.



(a) (b)

Fig. 2-3. With "DPWM + CRM" modulation. (a) Switching frequency distribution in all three phases over a half-line cycle. (b) Switching-cycle waveforms.

Switching-cycle waveforms in phase A and phase C at θ = 10 °are shown in Fig. 2-3(b). Since each of these two phases is independently controlled as the CRM, switching frequencies in these two phases may be different. In addition, in this two-level H-bridge structure, the inductor current slew rate in each phase is dependent not only on the switching state in this phase but also on the switching states in other phases. Therefore, as shown in Fig. 2-3(b), switching frequency in phase A is higher than in phase C. Over ten adjacent switching cycles in phase A, the operations are not all the same since the switching state in phase C is not the same in every switching cycle of phase A. More specifically, phase C is at the off state during most of the fifth and the ninth cycle in phase A, while phase C is at the on state during all the other cycles in phase A. Therefore, the inductor current slew rate at the on state in phase A has a sudden change during the fifth and the ninth cycle when compared with the previous cycle, and so does the slew rate at the off state in phase A. The

switching period in the fifth and the ninth cycle also has a sudden change when compared with the previous cycle, which indicates the oscillation in switching frequency.

According to the previous analysis, one simple method for limiting the switching frequency variation range and for eliminating the oscillation is synchronizing the switching frequencies in the two phases operating at high-frequency PWM. For a better understanding, consider the first 30 °line-cycle interval as an example. According to Fig. 2-3(a), switching frequency in phase A is higher than switching frequency in phase C. Therefore, switching frequency in phase A needs to be synchronized to that in phase C. The way to implement this concept of synchronization of switching frequency (Fs sync) is to change the operation mode in phase A from CRM to DCM, while phase C still operates at the CRM. The turn-on instant in phase C is determined by the inductor current zero crossing point in phase C, while the turn-on instant in phase A is determined by the information from phase C in every switching cycle to keep switching frequencies in these two phases synchronized. For simplicity of control, the turn-on instant in phase A is controlled to be synchronized to the turn-on instant in phase C, which means the turn-on instant in both phase A and phase C is determined by the inductor current zero crossing point in phase C. Typical switching-cycle waveforms of gate signals and inductor currents in phase A and phase C with switching frequency synchronization are shown in Fig. 2-4 for better illustration.

More generally speaking, due to the dependence of switching frequency on the average inductor current (ac reference current) under CRM operation, asynchronous switching frequency variation exists between the two phases operating at CRM, leading to wide switching frequency variation over a whole line cycle. In order to limit the switching frequency, between the two phases operating at high-frequency PWM, the one originally operating at higher frequency is controlled to follow the one originally operating at lower frequency. This can also be understood from the

concept of master and slave. Between those two phases operating at high-frequency PWM, the slave phase (originally operating at higher frequency) is controlled to follow the master phase (originally operating at lower frequency) in order to achieve the synchronization of switching frequency variation and to limit the switching frequency variation range.

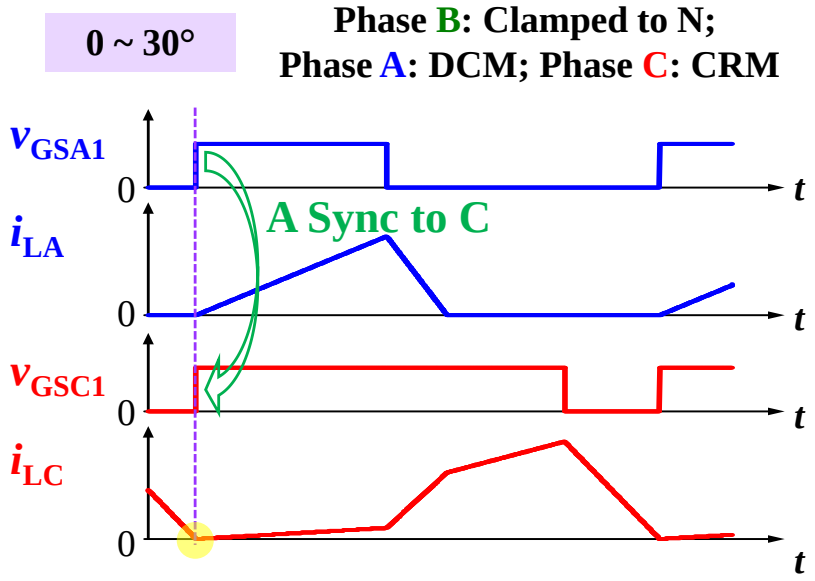


Fig. 2-4. Typical switching-cycle waveforms with “DPWM + CRM + Fs sync” modulation.

All the analyses mentioned above are applicable to the whole line cycle, and the same control strategy is applicable to both inverter and rectifier modes. The operation mode distribution with the above-mentioned modulation (hereinafter “DPWM + CRM + Fs sync”) for three-phase bidirectional ac–dc converters over the whole line cycle is shown in Fig. 2-5. As shown, ac reference currents are used to represent three phases. The transition between clamping mode and CRM occurs every 60 ° according to the amplitude of the ac reference current in all three phases. The transition between CRM and DCM occurs at the midpoint of two adjacent clamping/CRM transition points, since at this midpoint, the two phases operating at high-frequency PWM are at the same operating point.

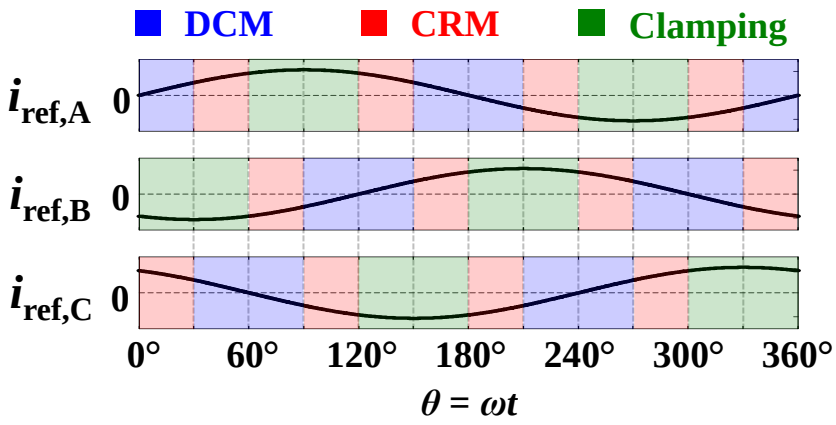


Fig. 2-5. Line-cycle operation mode distribution with "DPWM + CRM + Fs sync" modulation under the unity power factor condition.

The control diagram with the proposed "DPWM + CRM + Fs sync" modulation is similar to what is shown in Fig. 2-2(a) with the only difference found in the ZCD part. A multiplexer is combined with the ZCD part, which is responsible for selecting the phase operating at CRM according to Fig. 2-5 and allowing the information of the inductor current zero crossing in this phase (for example, phase C during the first 30 ° line-cycle interval) to pass through, and then to become the global decision point to reset s_e and then to turn on the control switches in both phases operating at high-frequency PWM, instead of the individual inductor current zero crossing point in each phase as the decision point.

With the synchronization of switching frequency, there is significant reduction in the switching frequency variation range over the whole line cycle. Comparison between switching frequency distributions in phase A over a half-line cycle without and with the synchronization of switching frequency is shown in Fig. 2-6. With the minimum switching frequency at 300 kHz, the peak switching frequency is only around 530 kHz instead of 3 MHz, which significantly reduces the switching-related loss and the difficulty in control, even under this high modulation index condition (V_{dc} = 800 V, $V_{ac,\ L\text{-}L}$ = 480 V, M = 0.849).

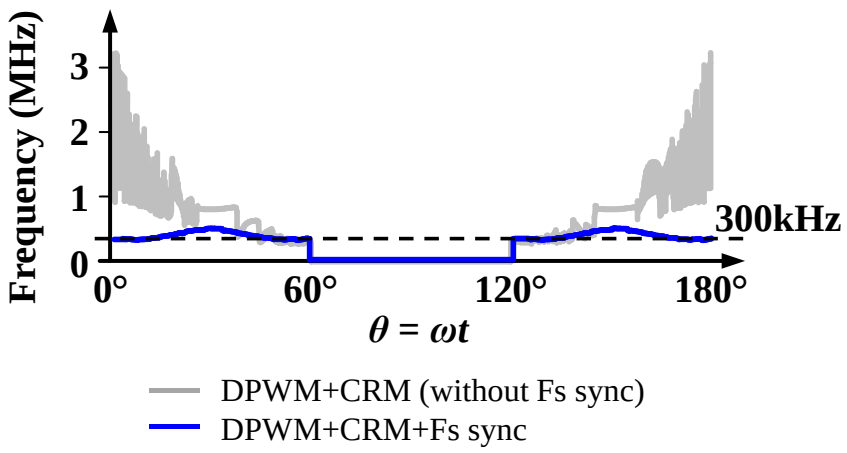


Fig. 2-6. Comparison between switching frequency distributions in phase A over a half-line cycle without and with the synchronization of switching frequency.

Furthermore, the switching frequency variation range is still narrow, with only 2:1 (the ratio of maximum to minimum switching frequency) over a line cycle even when the modulation index is 0.9, although this range becomes wider as the modulation index goes higher. What is more, with this modulation concept the system can still work at the condition when the ac line-to-neutral voltage is higher than half of the dc voltage ($M > 0.866$). Therefore, the aforementioned limitations under the high modulation index conditions do not exist in this proposed modulation.

It is important to note several points as this section concludes. First, switching frequency distributions in this section are all the simulation results in the inverter mode, while in the rectifier mode, switching frequency distributions are similar.

Next, the turn-on instant in the phase operating at the DCM can be determined by any information from the phase operating at the CRM, as long as switching frequencies in these two phases are synchronized. Besides the simplicity of control, another reason for the synchronization of the turn-on instants in these two phases is the relatively narrow switching frequency variation range over a line cycle. However, the method to control the turn-on instant in the phase operating at the DCM should not be restricted to this way.

After that, with the proposed “DPWM + CRM + Fs sync” modulation, further quantitative analysis about the time-domain switching waveforms shows that the CRM ZVS turn-on is able to be naturally achieved under inverter mode operation, while additional negative inductor current by off-time extension [27], [36]–[39] is necessary for achieving CRM ZVS turn-on under rectifier mode operation. During DCM, for both inverter mode and rectifier mode operation, valley switching turn-on is able to be achieved by a turn-on delay compared with the turn-on instant in the phase operating at CRM. The detailed analysis is illustrated in the Appendix.

Finally, the proposed “DPWM + CRM + Fs sync” modulation concept is also applicable to other three-phase ac–dc structures, such as the three-level T-type structure and the three-level neutral-point-clamped structure. Since this dissertation is focused on the modulation concept itself, the two-level H-bridge structure is selected for analysis due to its simplicity.

2.3 Quantification of Switching Frequency Variation Range: Its Dependency on Inductance and Device Parasitic Capacitance

For CRM-based ac–dc converters, the minimum switching frequency is a key design target since it is a critical parameter to determine the corner frequency in the EMI filter design.

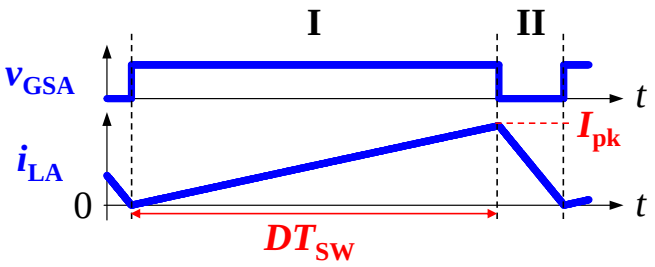
In CCM operation mode, the switching frequency is usually fixed, and the inductance value determines the inductor current ripple. In contrast, in CRM-based operation mode, the inductor current ripple is given; the inductance value determines the switching frequency. Furthermore, at high-frequency high-power applications, as the current rating of power semiconductor devices increases, there is usually an increase in the parasitic capacitance of devices, which makes the LC resonance period in each switching cycle not negligible any more. Therefore, it is important to know the quantitative dependence of switching frequency variation, especially of the minimum switching frequency, on the inductance value and the device parasitic capacitance value.

Fig. 2-6 shows that under the proposed "DPWM + CRM + Fs sync." soft-switching modulation, the minimum switching frequency occurs at the 0°, 60°, 120° … (multiples of 60°) operating points. The reason is that at these operating points, the ac reference current value in the phase under CRM operation reaches the peak over the whole line cycle. Since the system frequency is determined by the phase under CRM operation, and under CRM operation the inductor current ripple is approximately two times as the ac reference current, intuitively the minimum switching frequency would occur at these operating points.

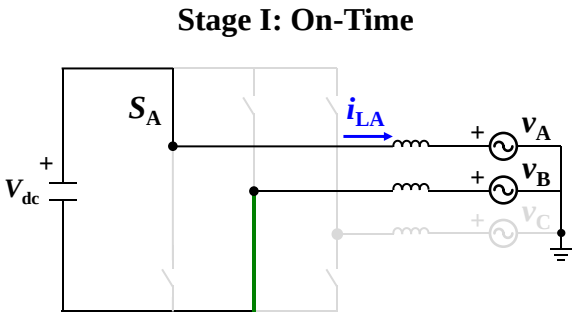
In order to achieve 300 kHz minimum switching frequency, the 60 °operating point is selected as an example and the switching frequency dependence on the inductance and the device parasitic capacitance is to be quantified. At this operating point before the DPWM clamping option changes, phase A, B, and C operates at CRM, clamping mode, and DCM, respectively.

In order to make the illustration more clearly, the parasitic capacitance of all the power semiconductor devices is neglected first to simplify the analysis procedure. The impact of the parasitic capacitance is to be included later.

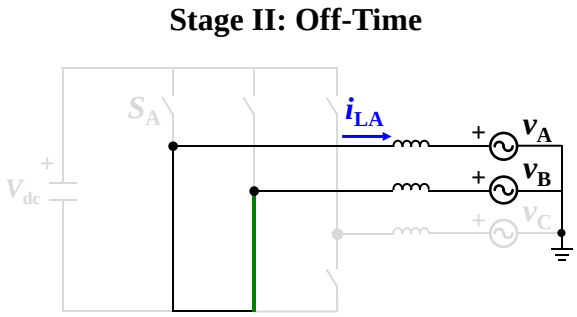
Fig. 2-7 (a) shows the simulated switching-cycle waveforms under inverter mode operation in phase A at the 60 ° operating point without the parasitic capacitance of devices, including the gate signal of the active switch and the inductor current. Fig. 2-7 (b) and (c) show the circuit operation during on-time and during off-time, respectively. It should be noted that the 60 ° operating point is the line-frequency zero crossing point of the ac line-to-neutral voltage (also the ac reference current) in phase C. Therefore, the on-time in phase C is almost zero at this operating point. Here an approximation is made that phase C is disconnected with the system.



(a)



(b)



(c)

Fig. 2-7. System operation at the 60 °operating point without the parasitic capacitance of devices: (a) Simulated switching-cycle waveforms in phase A; (b) Circuit operation diagram during on-time; (c) Circuit operation diagram during off-time.

Based on the volt-second balance of the inductor in phase A, the duty cycle is calculated as below. It is noted that at the 60 ° operating point, the line-to-neutral voltage value in phase A is approximately the opposite of that in phase B (hereinafter the same unless otherwise specified). It is also noted that the upper case letter "*V*" (V_A, V_B, etc.) here is used for representing the ac voltage at a specific line-cycle operating point, which is assumed a fixed value over several switching cycles, while the lower case letter "*v*" (v_A, v_B, etc.) is used for representing the time-domain ac voltage waveforms or expressions (hereinafter the same unless otherwise specified and applicable to other physical quantities, e.g. ac reference current).

$$\frac{V_{dc}-V_A+V_B}{2}D-V_A(1-D)\approx\frac{V_{dc}-2V_A}{2}D-V_A(1-D)=0\Rightarrow D=\frac{2V_A}{V_{dc}} \tag{2-1}$$

Therefore, the switching frequency dependence on the inductance value at this operating point is able to be derived according to the following relation between the inductor voltage and the inductor current ripple during on-time (I_{ac} is the RMS value of the ac reference current).

$$\frac{V_{dc}-V_A+V_B}{2}\cdot\frac{DT_{SW}}{L}\approx\frac{V_{dc}-2V_A}{2}\cdot\frac{DT_{SW}}{L}=I_{pk}=\sqrt{6}I_{ac} \tag{2-2}$$

Then the next part is to derive this dependency when the parasitic capacitance of devices is included. In this case, it is necessary to consider the LC resonance stage before the turn-on instant of the active switch. The corresponding circuit operation diagram is shown in Fig. 2-8 (a), and the simulated switching-cycle waveforms are shown in Fig. 2-8 (b), including the gate signal of the active switch, the inductor current, and the drain-source voltage of the active switch. The LC resonance period is highlighted. Since this is a 2nd-order LC resonance circuit, the state-plane trajectory analysis is applicable and the trajectory is shown in Fig. 2-8 (c) during this resonance period.

It is clear that at this operating point, the valley of the switching-cycle inductor current, I_{valley}, is determined by the following equation.

$$-I_{valley}Z_n=V_A-V_B\approx 2V_A \tag{2-3}$$

The characteristic impedance Z_n at this operating point is determined by the inductance and the device parasitic capacitance (time-related output capacitance at the dc voltage) as below. Here the C_{OSS} is the output capacitance of each power semiconductor devices, and the time-related device output capacitance value at $v_{DS} = V_{dc}$ is used here (hereinafter the same).

$$Z_n=\sqrt{\frac{L}{C_{OSS}}} \tag{2-4}$$

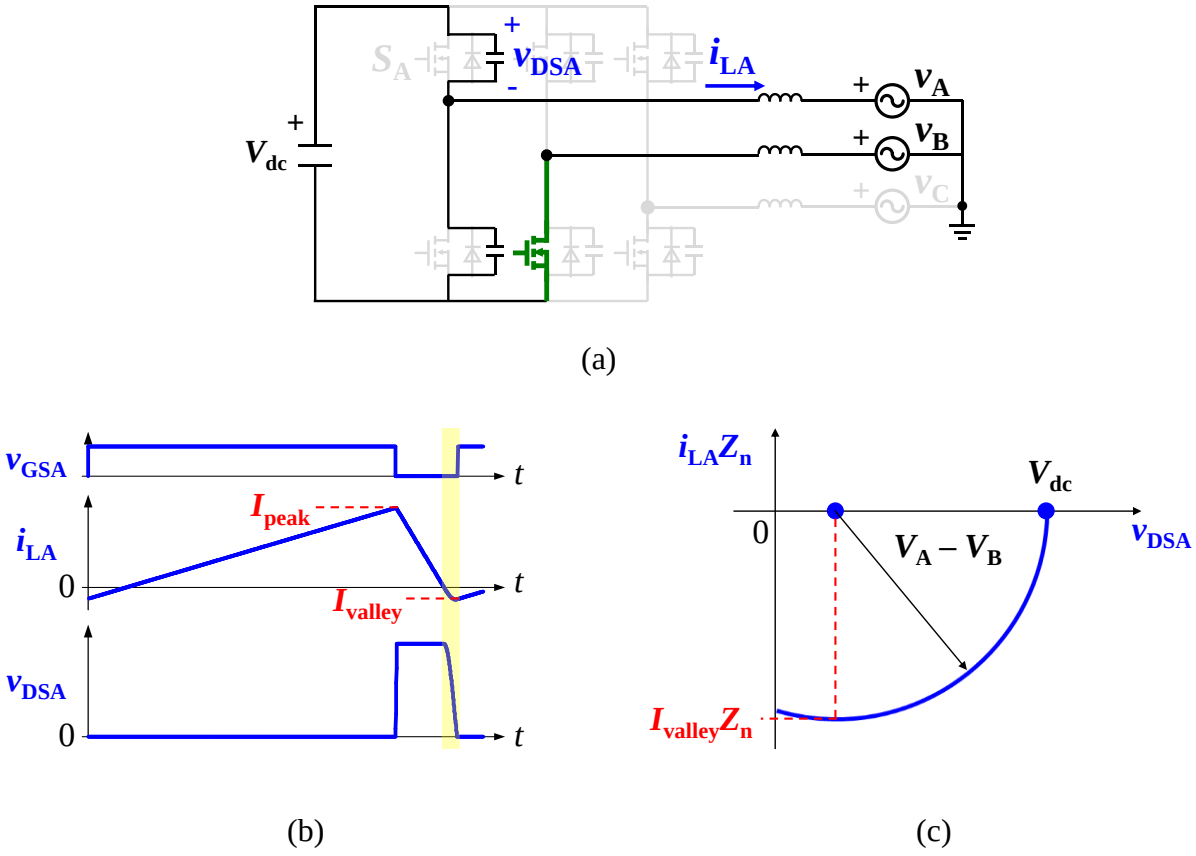


Fig. 2-8. System operation during the LC resonance stage at the 60 °operating point: (a) Circuit operation diagram; (b) Simulated waveforms in phase A; (c) State-plane trajectory.

Then, similar to [39], it is assumed that the switching-cycle inductor current waveform has a triangular shape, and therefore the peak of the switching-cycle inductor current, I_{peak}, is determined by the following equation.

$$\frac{I_{peak}+I_{valley}}{2}=I_{ref}=\frac{\sqrt{6}}{2}I_{ac}\Rightarrow I_{peak}=\sqrt{6}I_{ac}-I_{valley} \tag{2-5}$$

After that, similar to Equation (2-2), based on Equations (2-1), (2-3), (2-4), and (2-5), the dependence of switching frequency at this operating point on the inductance and on the device parasitic capacitance is shown as the following equation.

$$\frac{V_{dc}-2V_A}{2}\cdot\frac{2V_A}{V_{dc}}\cdot\frac{T_{SW}}{L}=I_{peak}-I_{valley}=\sqrt{6}I_{ac}+4V_A\sqrt{\frac{C_{OSS}}{L}} \tag{2-6}$$

Therefore, in order to achieve a certain minimum switching frequency, the analytical solution of the desired inductance L is as below.

$$L = \left[\frac{-4V_A\sqrt{C_{OSS}} + \sqrt{16V_A^2 C_{OSS} + 4\sqrt{6} I_{ac} T_{SW} \frac{V_A(V_{dc} - 2V_A)}{V_{dc}}}}{2\sqrt{6} I_{ac}} \right]^2 \tag{2-7}$$

Equation (2-7) indicates the dependence of the minimum switching frequency (the maximum switching period T_{SW}) on the inductance value L (or vice versa), under a certain system dc/ac voltage, a certain system power and a certain parasitic capacitance of power semiconductor devices.

Take 800-V dc voltage, 277/480-V ac voltage, 12.5-kW power, 300-pF device parasitic capacitance as an example. Under three arbitrarily selected inductance values, the calculated minimum switching frequency based on Equation (2-7), the simulated minimum switching frequency, and the error between them are shown in Table 2-1. It shows high accuracy when the desired minimum system switching frequency is lower than 500 kHz, which is sufficient for the application in this dissertation. The reason of the more and more evident inaccuracy as the inductance goes smaller is due to the more and more dominant LC resonance period in one switching period, since the switching period is approximately proportional to the inductance value, while the LC resonance period is proportional to the square root of the inductance value. Therefore, the approximation of triangular switching-cycle inductor current waveform becomes less accurate.

The dependence of the maximum switching frequency on the inductance value and on the device parasitic capacitance can be quantified in a similar way. Take the 30 °operating point as an example. For sake of brevity, only the key equations are shown in the following parts.

Table 2-1 Verification of Proposed Analytical Model

Inductance (μH)	Calculated Min. Switching Freq. (kHz)	Simulated Min. Switching Freq. (kHz)	Error (Δ/Simulated Value)
2.0	481.8	465.3	3.55%
3.0	340.6	338.2	0.71%
4.0	265.0	264.7	0.11%

At this operating point, the operations in phase A and in phase C are identical at CRM. Similar to Fig. 2-7 and Equation (2-1), when the device parasitic capacitance is ignored, the duty cycle is derived as below.

$$\left(\frac{1}{3}V_{dc}-V_A\right)D-V_A(1-D)=0\Rightarrow D=\frac{3V_A}{V_{dc}} \tag{2-8}$$

After considering the device parasitic capacitance, the valley of the switching-cycle inductor current, I_{valley}, is determined by the following equation.

$$-I_{valley}Z_n=3V_A \tag{2-9}$$

The characteristic impedance Z_{n} at this operating point is determined by the inductance and the device parasitic capacitance (time-related output capacitance at the dc voltage) as below.

$$Z_n=\sqrt{\frac{3L}{2C_{OSS}}} \tag{2-10}$$

Then after assuming the triangular inductor current waveform in each switching cycle, the peak of the switching-cycle inductor current, I_{peak}, is determined by the following equation.

$$\frac{I_{peak}+I_{valley}}{2}=I_{ref}=\frac{\sqrt{2}}{2}I_{ac}\Rightarrow I_{peak}=\sqrt{2}I_{ac}-I_{valley} \tag{2-11}$$

Finally, the dependence of the switching frequency at this operating point on the inductance and on the device parasitic capacitance is shown as the following equation.

$$\left(\frac{1}{3}V_{dc}-V_A\right)\cdot\frac{3V_A}{V_{dc}}\cdot\frac{T_{SW}}{L}=I_{peak}-I_{valley}=\sqrt{2}I_{ac}+6V_A\sqrt{\frac{2C_{OSS}}{3L}} \tag{2-12}$$

Under the given dc/ac voltage, system total power, device parasitic capacitance and the selected inductance according to Equation (2-7), the calculated maximum switching frequency based on Equation (2-12) is around 500 kHz, which has been verified from simulation in the previous section in this chapter.

Furthermore, by comparing Equation (2-12) with Equation (2-6), the switching frequency variation range is able to be derived as well.

For the rectifier mode operation, the aforementioned method is applicable to derive the relation between the desired inductance and the target minimum switching frequency. Furthermore, it can be proved that at the 60 °operating point, duality exists in the operation between the inverter mode and the rectifier mode, when the off-time extension is included in the rectifier mode. Therefore, the proposed analytical model, especially Equation (2-7) is also applicable to the rectifier mode operation for the inductance design.

2.4 Experimental Verifications

Based on the two-level H-bridge structure, a 25 kW three-phase bidirectional ac–dc converter prototype is built with SiC MOSFETs, which is shown in Fig. 2-9. The power density of this prototype is 127 W/in^3, including heat sinks, dc-link capacitors, three-phase LCL harmonic filters, devices, gate drivers, and all other sensing ICs. This power density is at least three times higher than commercial products according to the survey.

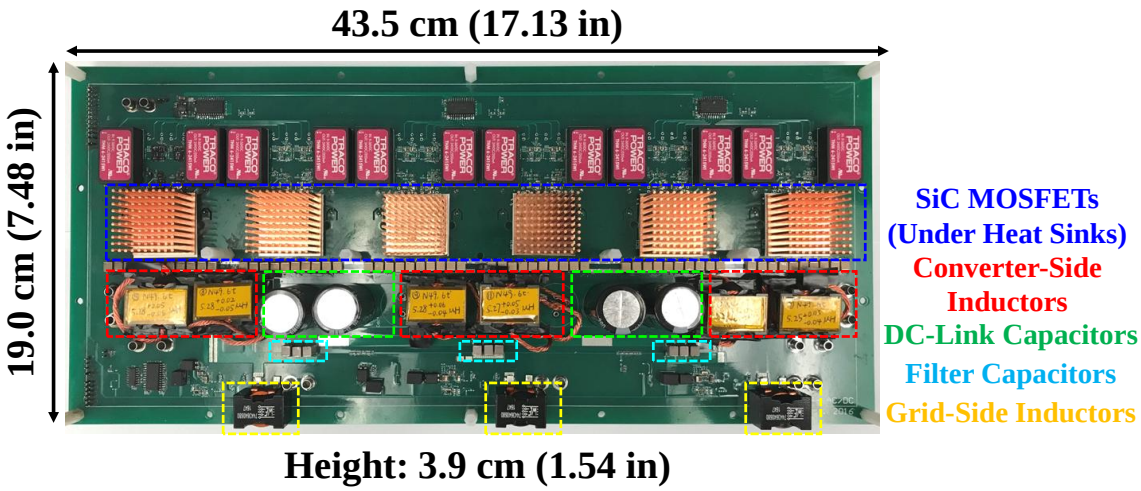


Fig. 2-9. Prototype of the 25 kW SiC-based three-phase bi-directional ac–dc converter.

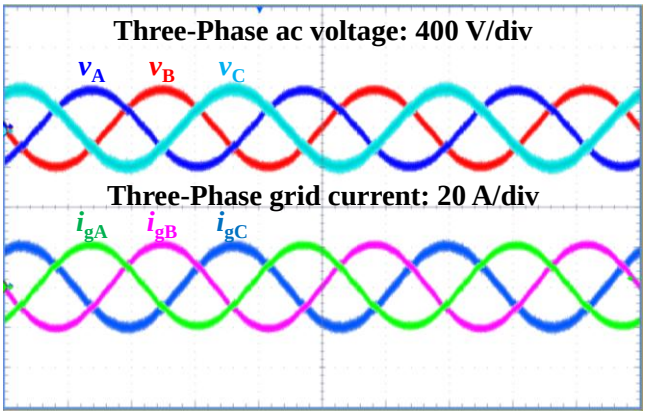
The design parameters of the converter are listed in Table 2-2. In this converter prototype, altogether there are six phase legs and 12 SiC MOSFETs, with two phase legs and four SiC MOSFETs in each phase. Compared with the topology in Fig. 2-2(a), the additional half of them are for the purpose of the future application of two-channel interleaving control, which is to be discussed in later chapters. Therefore, the experimental verification of the proposed modulation in this chapter is based on three phase legs, and thus, in this case, the full power is 12.5 kW.

The converter side inductor is designed with 3.5 μH, which is calculated based on Equation (2-7), to achieve 300 kHz minimum switching frequency. N49 from EPCOS/TDK is used as the magnetic core material. The core shape is PQ32/20 and the turns number of each inductor winding is 4.

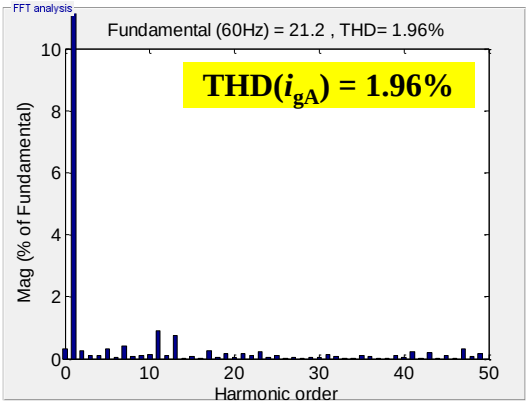
Fig. 2-10(a) shows three-phase line-cycle experimental waveforms of ac line-to-neutral voltages and grid-side currents in the inverter mode under full load. The waveforms in phase A and phase B are measured, while the waveforms in phase C are calculated based on waveforms in the first two phases. Fig. 2-10(b) shows the total harmonic distortion (THD%) of the grid-side current based on phase A. The grid-side currents are well controlled as sinusoidal shapes.

Table 2-2 Parameters of the Prototype

Description		Value
Nominal output power (P_O)		25 kW (6 phase legs)
DC voltage (V_{dc})		800 V
AC grid voltage (V_{ac})		277/480 V, 60 Hz
Switching frequency (F_{SW})		Above 300 kHz
Converter-side inductance (L)		3.55 μH
Filter capacitance (C_F)		1.2 μF
Grid-side inductance (L_g)		6.8 μH
DC-link capacitance (C_{dc})		220 μF
SiC MOSFET	Part No.	GE12N025RF-3
	Voltage rating (V_{DSS})	1200 V
	On-resistance (R_{DSon})	25 mΩ (25 ℃)
	Package	DE-150
Microcontroller (MCU)	Part No.	TMS320F28075
	Clock frequency (F_{CLK})	120 MHz
	Control cycle (T_{ISR})	3 μs



(a)



(b)

Fig. 2-10. Line-cycle experimental results at full power in the inverter mode. (a) Experimental waveforms of three-phase ac voltages and three-phase grid currents. (b) FFT analysis result of phase A grid current.

Fig. 2-11(a)–(c) shows switching-cycle experimental waveforms at three operating points around 5°, 15°, and 25° in phase C (CRM) in the inverter mode. At each operating point, the

control switch is turned on at zero drain–source voltage. Similarly, Fig. 2-11(d)–(f) shows switching-cycle experimental waveforms at the same three operating points in phase A (DCM) in the inverter mode. At each operating point, the control switch is turned on at the valley point (near zero voltage), which is guaranteed by the strategy introduced in the Appendix.

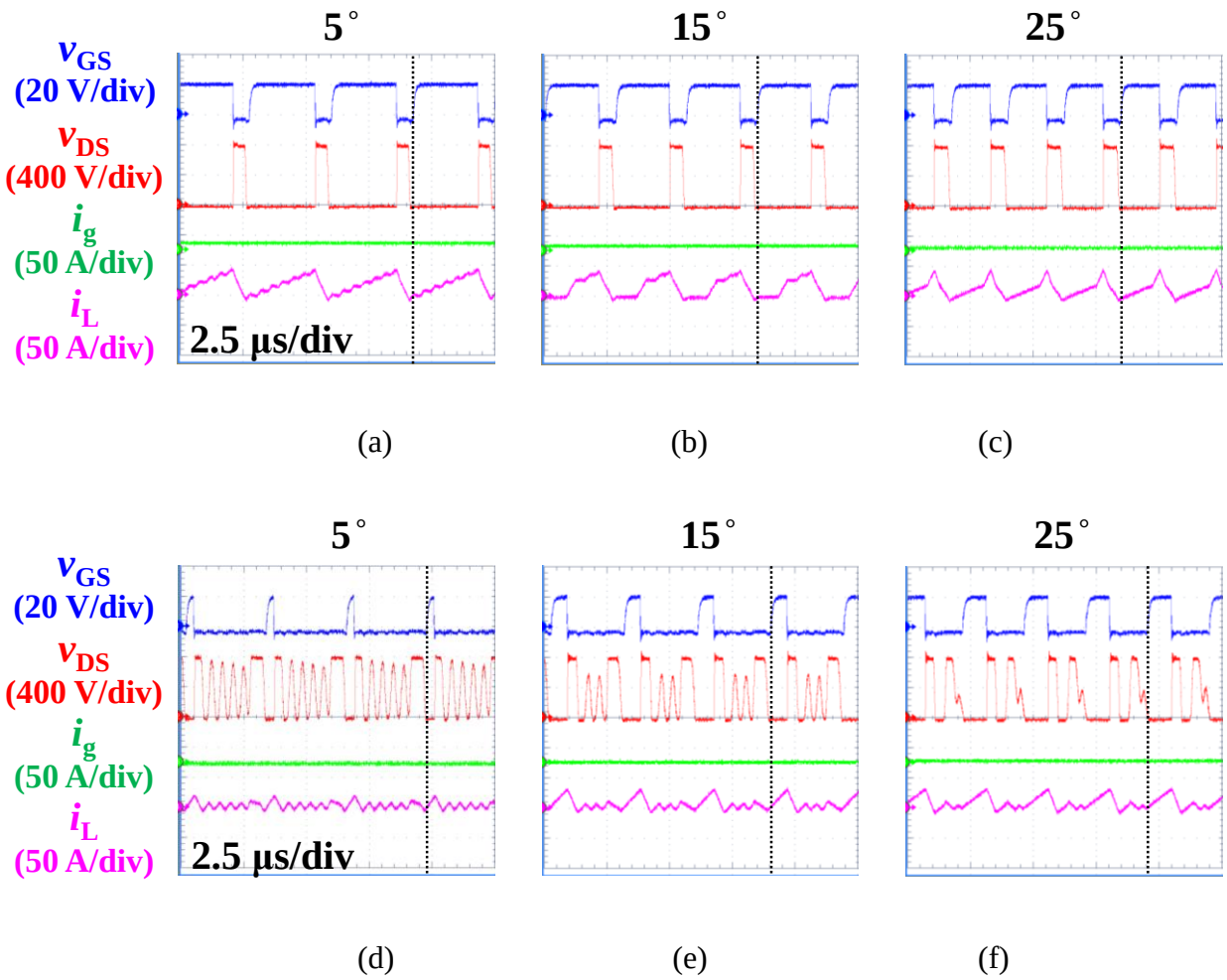
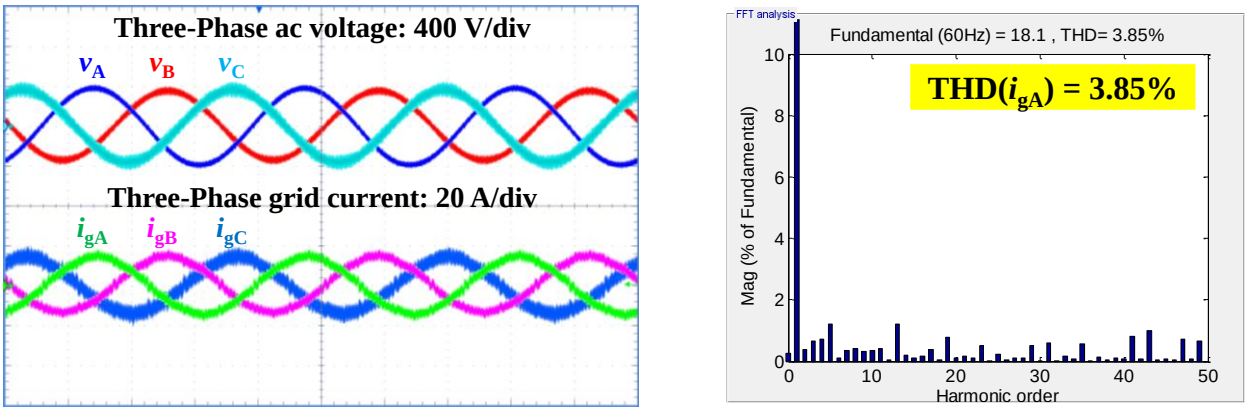


Fig. 2-11. Switching-cycle experimental waveforms in the inverter mode at the following operating points. (a) Around 5 °during the CRM. (b) Around 15 °during the CRM. (c) Around 25 °during the CRM. (d) Around 5 °during the DCM. (e) Around 15 °during the DCM. (f) Around 25 °during the DCM.

Fig. 2-12(a) shows three-phase line-cycle experimental waveforms of ac line-to-neutral voltages and grid-side currents in the rectifier mode at 85% of full power. The waveforms in phase

C are calculated based on measured waveforms in phase A and phase B. The THD% of the grid-side current based on phase A is shown in Fig. 2-12(b), which indicates well-controlled grid currents.



(a) (b)

Fig. 2-12. Line-cycle experimental results at 85% of full power in the rectifier mode. (a) Experimental waveforms of three-phase ac voltages and three-phase grid currents. (b) FFT analysis result of phase A grid current.

Fig. 2-13(a)–(c) shows switching-cycle experimental waveforms at the same three operating points in phase C (CRM) in the rectifier mode, and Fig. 2-13(d)–(f) shows switching-cycle experimental waveforms at the same three operating points in phase A (DCM) in the rectifier mode. At each operating point, the control switch is turned on at zero drain–source voltage during CRM and at the valley point during DCM operation.

With the proposed modulation, the simulated loss breakdown is shown in Fig. 2-14 for both inverter and rectifier modes. Generally, the loss breakdown in inverter and rectifier mode is similar. The slightly higher conduction loss, inductor loss, and shunt-based ZCD sensing loss in the rectifier mode are due to a slightly higher RMS current caused by the off-time extension with some margin.

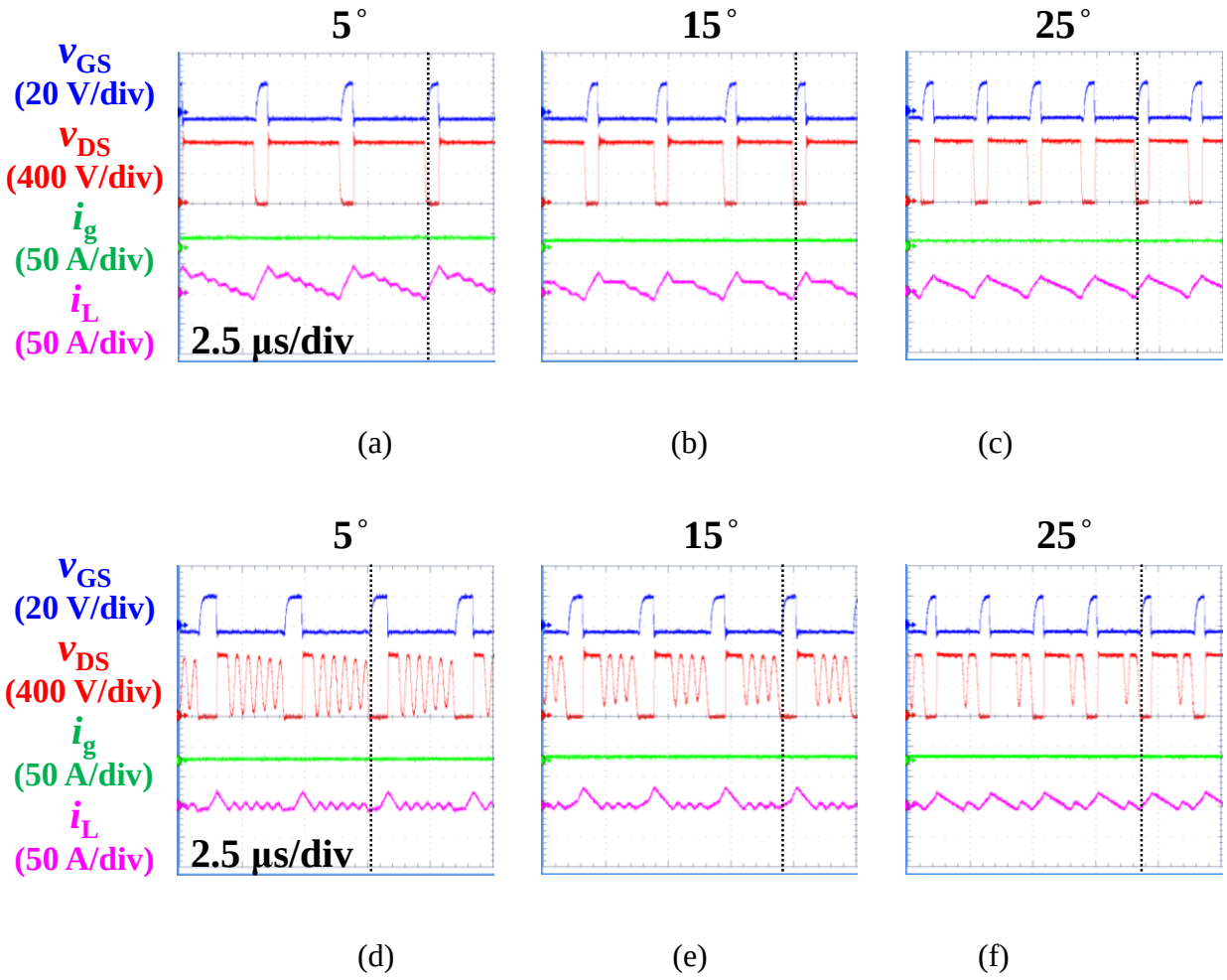


Fig. 2-13. Switching-cycle experimental waveforms in the rectifier mode at the following operating points. (a) Around 5 °during the CRM. (b) Around 15 °during the CRM. (c) Around 25 °during the CRM. (d) Around 5 °during the DCM. (e) Around 15 °during the DCM. (f) Around 25 °during the DCM.

With the proposed modulation operating at above 300 kHz switching frequency, the system efficiency is tested in inverter and rectifier mode, as shown in Fig. 2-15. The peak efficiency is close to 99.0%, which verifies the proposed modulation is a high-efficiency solution, even when the operating switching frequency is above 300 kHz.

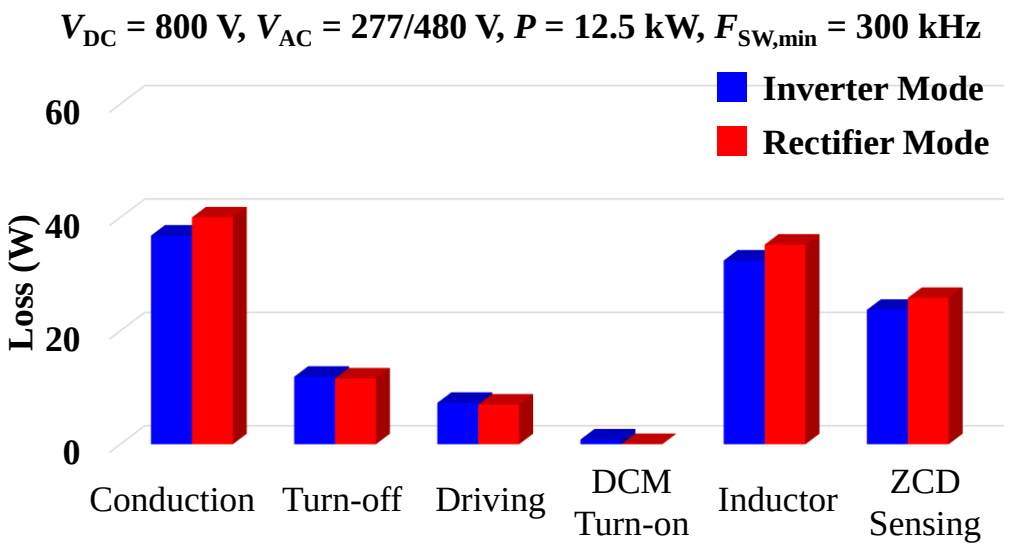


Fig. 2-14. Simulated loss breakdown with the proposed modulation.

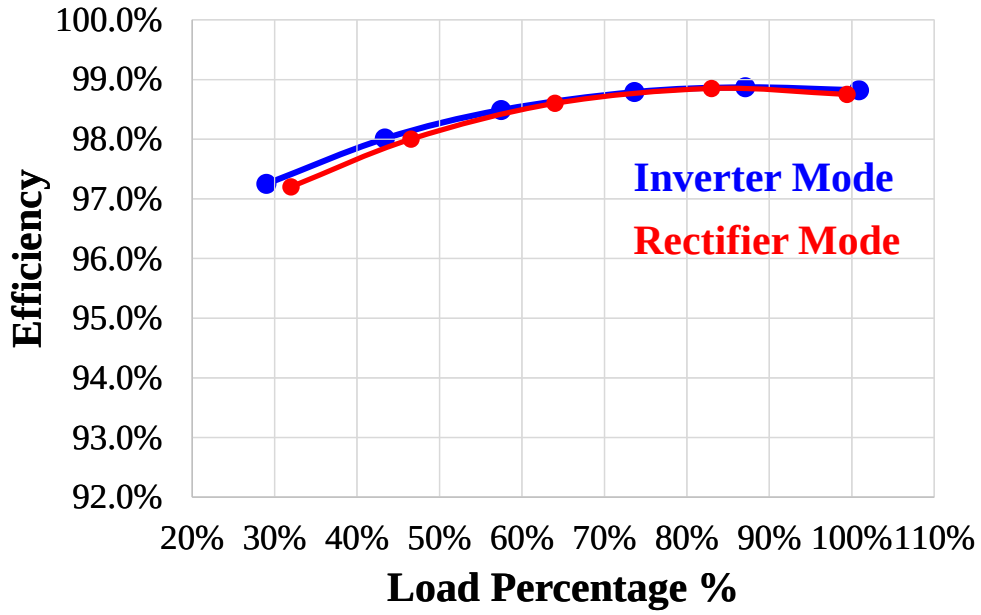


Fig. 2-15. Tested efficiency under different load conditions with the proposed modulation at above 300 kHz.

2.5 Conclusions

According to Chapter 1, for SiC MOSFET power semiconductor devices, CRM ZVS soft switching was the key to achieving both high power density and high efficiency at high switching

frequency operation. In this chapter, a novel CRM-based soft-switching modulation (DPWM + CRM + Fs sync.) was proposed for three-phase bidirectional ac–dc converters under the unity power factor condition, without adding any physical complexity to the three-phase system. With the proposed soft-switching modulation, for both inverter and rectifier mode operations, the switching frequency variation range shrank, ZVS soft switching was achieved, and thus, switching related loss was reduced. All the control functions were implemented and benefits of the proposed modulation were experimentally verified on a 25 kW SiC-based high-frequency three-phase bidirectional ac–dc prototype with a power density of 127 W/in^3. The tested peak efficiency of the prototype was around 99.0% in both inverter and rectifier mode operations even above 300 kHz high switching frequency operation.

Chapter 3 Soft Switching Technique under Non-Unity Power Factor for Three-Phase Grid-Tied Inverters[†]

3.1 Introduction

The CRM-based soft switching modulation technique proposed in the last chapter is suitable for the unity power factor operating conditions. However, when it is directly applied into non-unity power factor operating conditions, there are several hard switching related issues which cause the increase in switching loss. Therefore, in this chapter, these issues are introduced, the corresponding reasons are analyzed, and the solutions are provided. Then, a generalized soft switching modulation technique is proposed for both the unity and non-unity power factor conditions. Finally, the benefits are experimentally verified. The similar method for minimizing the switching loss mentioned in the last chapter is applied in the non-unity power factor operating conditions, which is also presented in the Appendix.

For better illustration of the concepts in this chapter, ideal power semiconductor devices are used unless otherwise specified. In addition, for each phase, define ψ as the phase-shift angle from the ac line-to-neutral voltage to the ac reference current. Specifically, taking phase A as an example, the ac line-to-neutral voltage v_{A} and the ac reference current $i_{\mathrm{ref,A}}$, along with the line-cycle phase angle θ, are defined as follows:

$$\begin{cases} \theta = \omega t \\ v_A(\theta,\psi) = \sqrt{2}V_{ac}\sin\theta \\ i_{ref,A}(\theta,\psi) = \sqrt{2}I_{ac}\sin(\theta-\psi) \end{cases} \tag{3-1}$$

[†] © 2020 IEEE. Reprinted, with permission, from [69] Z. Huang, Q. Li and F. C. Lee, "Critical-Conduction-Mode-Based Soft-Switching Modulation for Three-Phase PV Inverters with Reactive Power Transfer Capability," in *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5702-5713, June 2020.

3.2 Hard Switching Related Issues of the Original Soft Switching Modulation under Non-Unity Power Factor Conditions

When the original soft switching modulation technique proposed in Chapter 2 is applied for reactive power transfer, hard switching related issues occur in the phase which is intended to operate in DCM. More specifically, the features of zero current turn-on and of partial zero voltage turn-on are lost, leading to higher turn-on switching loss. There are two types of hard-switching turn-on, and the reasons for each type of hard-switching turn-on are analyzed in details in this section.

Under non-unity power factor conditions, the DPWM clamping based on the ac reference current is already well established. According to the conventional wisdom [34], [35], when the displacement angle between ac grid line-to-neutral voltage and ac reference current is less than 30 °, the DPWM clamping is applied to the phase with the highest ac reference current amplitude; otherwise, the DPWM clamping zones lags or leads by 30 ° when compared with the DPWM clamping zones under the unity power factor condition. This DPWM clamping option, according to the ac reference current, is widely adopted in the conventional modulations.

When the original "DPWM+CRM+Fs sync" modulation technique proposed in the last chapter is used for reactive power transfer, the operation mode over a half line-cycle is shown in Fig. 3-1, under an example of PF = 0.9 (ψ = 26 °) condition. The line-cycle intervals for each operation mode are shifted by 26 °when compared with that under the unity power factor condition shown in Fig. 2-5.

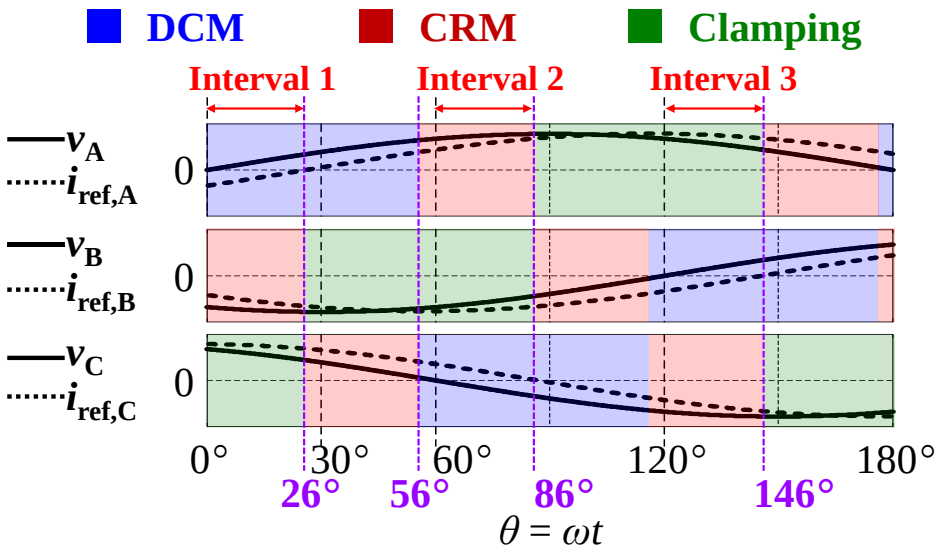
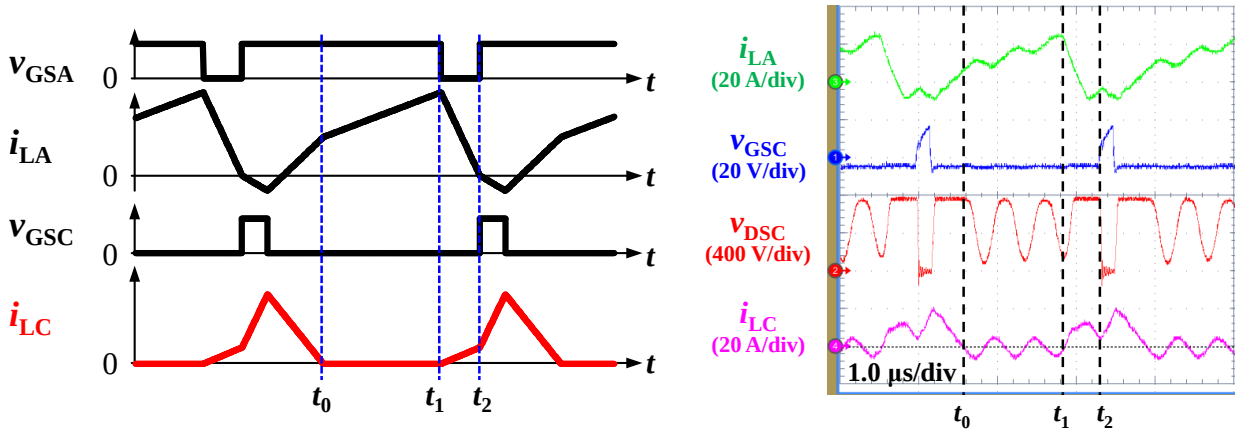


Fig. 3-1. Line-cycle operation mode with DPWM clamping based on ac reference current under PF = 0.9 (ψ = 26 °) condition; the 1st type hard switching turn-on exists during the intervals 1, 2, and 3 over this half line-cycle (v_A, v_B, and v_C are ac line-to-neutral voltages in phases A, B, and C, respectively; $i_{ref,A}$, $i_{ref,B}$, and $i_{ref,C}$ are ac reference currents in phases A, B, and C, respectively).

However, with the operation mode shown in Fig. 3-1 under the non-unity power factor condition, the first type of hard-switching turn-on at positive drain–source current is observed at some operating points in the phase operating at DCM.

An example of switching-cycle waveforms at 70 ° operating point is shown in Fig. 3-2 (a), with the operation mode shown in Fig. 3-1. The reference direction for currents is defined from the dc side to the ac side, unless otherwise specified. As shown in Fig. 3-2 (a), during the DCM dead-time interval ($t_0 - t_2$), after the control switch in phase A is turned off at t_1 instant, the inductor current in phase C starts to increase even before the control switch in phase C is turned on at t_2 instant. The operation in phase C is still DCM but the turn-on current becomes positive, which is different from the conventional DCM operation in which zero-current-switching (ZCS) turn-on is

achieved but is similar to that in the CCM hard-switching operation from the point of view of turn-on instant. The experimental switching cycle waveforms are shown in Fig. 3-2 (b), which verifies the hard switching turn-on in phase C. Although the inductor current in phase C drops toward zero before t_2 instant due to the impact of the LC resonance after the inductor current zero crossing occurs in phase A, the turn-on current in phase C is still positive.

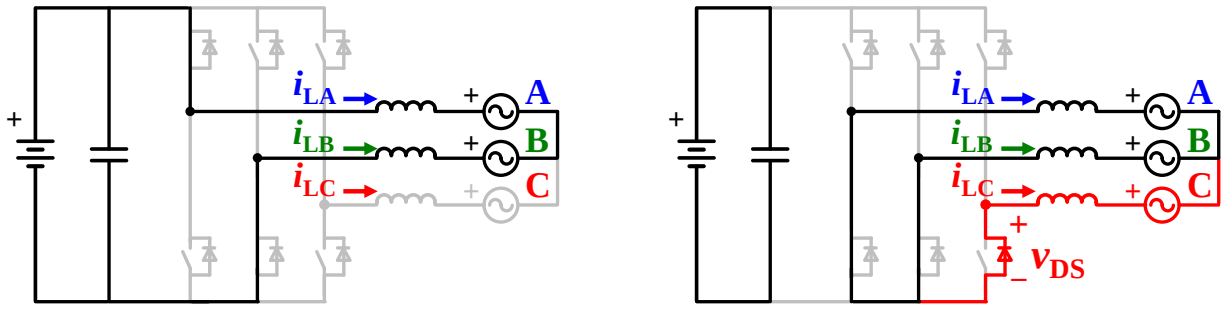


(a) (b)

Fig. 3-2. Switching-cycle waveforms around 70 °operating point with conventional DPWM clamping under PF = 0.9 (ψ = 26 °) condition; DCM hard switching turn-on occurs in phase C at t_2 instant. (a) Simulation results based on ideal switches. (b) Experiment results for verification (v_{GSA} and v_{GSC} are control switch gate signals in phases A and C, respectively; i_{LA} and i_{LC} are inductor currents in phases A and C, respectively; v_{DSC} is the control switch drain–source voltage in phase C).

Based on the 70 °operating point, the reason for this type of hard-switching turn-on is analyzed as here. In both phase A and phase C, the positive ac reference current indicates the top switch acts as the control switch whereas the bottom switch acts as the synchronous rectifier (SR). During t_0–t_1 interval in Fig. 3-2 (a), phase C is already during DCM dead-time interval and therefore is disconnected with the system as shown in the equivalent circuit in Fig. 3-3 (a). However, after the control switch is turned off and the SR is turned on in phase A at t_1 instant, a negative drain–source

voltage is applied to the SR in phase C, which makes its body diode forward-biased, as shown in Fig. 3-3 (b). Therefore, the inductor current starts to increase, although neither the top switch nor the bottom switch is turned on in phase C. When the inductor current zero crossing occurs in phase A at t_2 instant, the control switch in phase C is hard-switching turned on at positive current. The drain–source voltage of the control switch in phase C is clamped to the dc voltage before t_2 instant, indicating the complete loss of ZVS turn-on, as shown in Fig. 3-2 (b). Both the loss of ZCS and the loss of ZVS contribute to the increase in DCM turn-on loss.



(a) (b)

Fig. 3-3. Equivalent circuit diagram during the DCM dead-time interval (t_0–t_2 in Fig. 3-2) in phase A at around 70 °operating point under PF = 0.9 (ψ = 26 °) condition. (a) t_0–t_1 interval. (b) t_1–t_2 interval.

This type of hard-switching turn-on occurs when the polarity of the ac line-to-neutral voltage is opposite to that of the ac reference current in this phase, which are marked as the three intervals in Fig. 3-1 over the half line-cycle. The lower the PF, the higher the DCM turn-on loss, since the duration of the interval with abovementioned opposite polarities in a line cycle becomes longer. Simulation results demonstrate that this part of the increased DCM turn-on loss at PF = 0.9 and PF = 0.8 contributes to 51% and 77% additional device loss, respectively, making the switching loss at least triple, which is unacceptable.

Therefore, the first type of hard-switching turn-on occurs during the line-cycle interval when the polarity of the ac line-to-neutral voltage is opposite to that of the ac reference current. The other type of hard-switching turn-on is analyzed as follows, which occurs around the line-cycle phase angle when the operation mode is swapped between CRM and DCM. Here, the same example of PF = 0.9 (ψ = 26 °) condition is used for the illustration of this type of hard-switching turn-on.

Define θ_T as the line-cycle phase angle at which the operation mode is swapped between CRM and DCM (hereinafter "CRM/DCM transition angle θ_T"). According to Fig. 3-1, the CRM/DCM transition angle θ_T = 56 °. From the 26 ° to the 56 ° operating point, phase A and phase C are expected to operate at DCM and CRM, respectively. During this 30 ° line-cycle interval, the inductor current zero crossing in phase C determines the turn-on instant of the active switch in both phase C and phase A.

However, as the simulated switching-cycle inductor current waveforms in phase A and phase C at the 40 °operating point, shown in Fig. 3-4 (a), the inductor current zero crossing occurs almost simultaneously in each switching cycle at this operating point for these two phases. With CRM/DCM transition angle θ_T = 56 °, CCM hard-switching operation occurs in phase A between the 40 ° and the 56 ° operating points, which is different from the expectation that phase A should operate at DCM. The simulated switching-cycle inductor current in phase A and phase C at the 45 ° operating point is shown in Fig. 3-4 (b) as an example. The experiment switching-cycle waveforms at the 45 °operating point are shown in Fig. 3-5 as validation. This type of hard-switching turn-on exists during the three intervals marked in Fig. 3-6 over the half line cycle, and especially interval 4 is used as the example in the above-mentioned discussion.

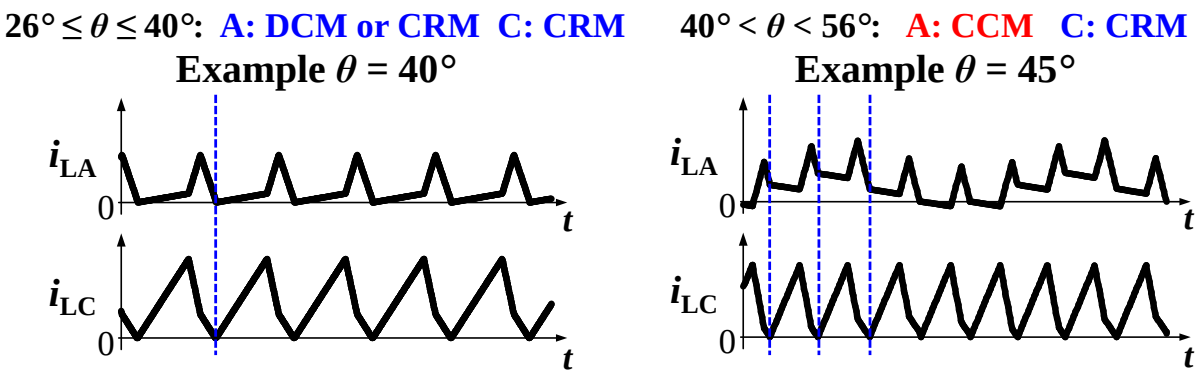


Fig. 3-4. Simulated switching-cycle waveforms at (a) 40 °operating point with stable operation; (b) 45 °operating point with the CRM/DCM transition angle θ_T = 56 °under PF=0.9 (ψ =26 °) condition; unstable CCM operation occurs (i_{LA} and i_{LC} are inductor currents in phases A and C, respectively).

Here, a comparison is made between the unity PF case and a non-unity PF case to analyze the impact of the PF on the CRM/DCM transition. The discussion is focused on the first 60 °line-cycle interval.

For the unity PF case, according to Fig. 2-5 and Equation (3-1), the CRM/DCM transition angle θ_T = 30 °. The ac line-to-neutral voltage is same in phase A and phase C at this operating point, and so is the ac reference current. Therefore, the switching-cycle operation is the same for these two phases at this operating point, and so is the inductor current zero crossing point.

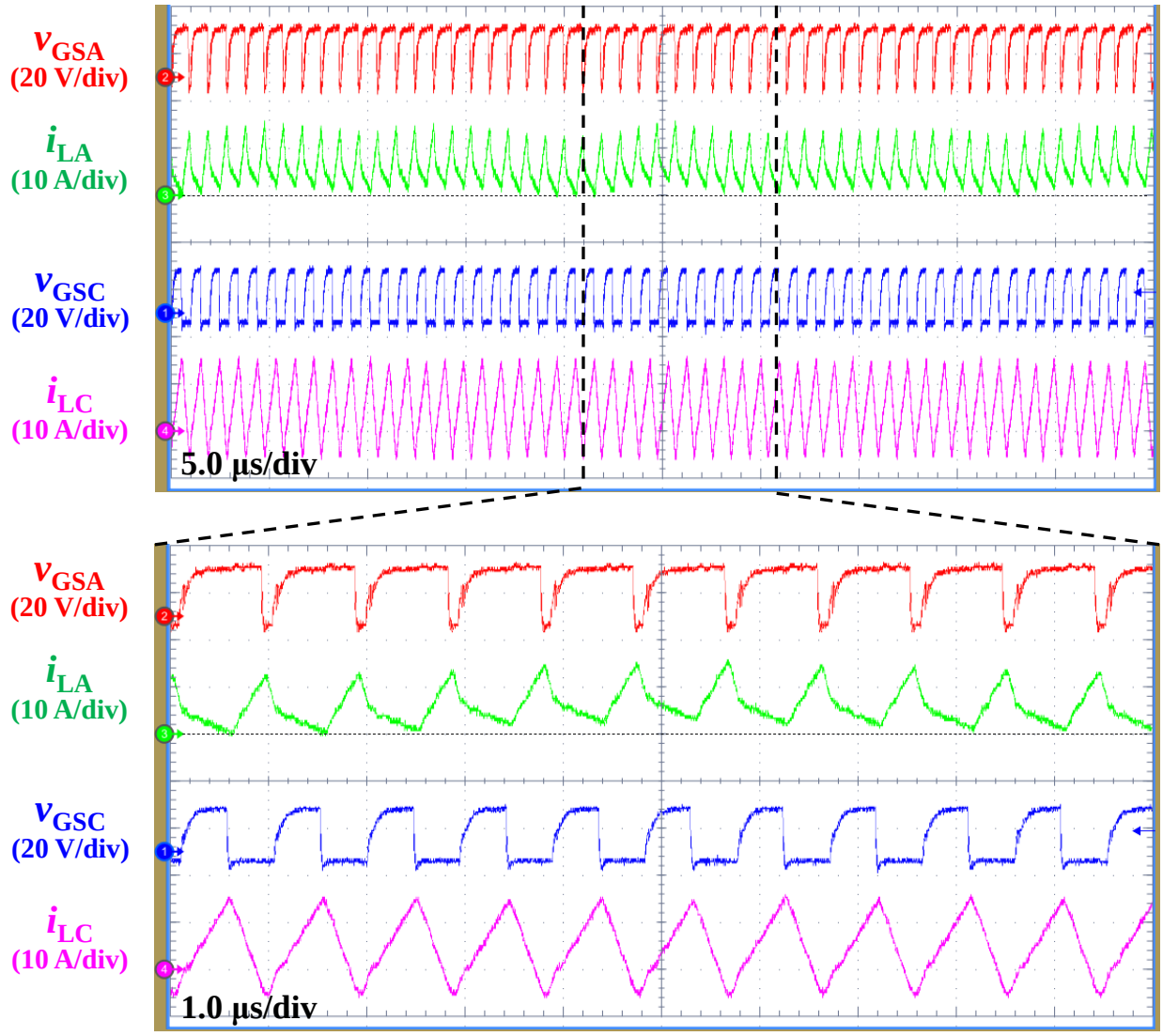


Fig. 3-5. Experiment waveforms around 45 °operating point with the CRM/DCM transition angle θ_T = 56 °under PF = 0.9 (ψ = 26 °) condition to verify unstable CCM operation in phase A (v_{GSA} and v_{GSC} are control switch gate signals in phases A and C, respectively; i_{LA} and i_{LC} are inductor currents in phases A and C).

However, for the non-unity PF condition, in phase A and phase C, the operating point with the same ac line-to-neutral voltage is different from the operating point with the same ac reference current. Take the PF = 0.9 (ψ = 26 °) case as an example. According to Fig. 3-6 and Equation (3-1), at the 30 °operating point, in phase A and phase C, the ac line-to-neutral voltage is the same

but phase A has lower ac reference current than phase C. Therefore, the inductor current zero crossing in phase A occurs earlier than phase C. At the 56 °operating point, in phase A and phase C, the ac reference current is the same but phase C has lower ac line-to-neutral voltage than phase A. Therefore, the inductor current zero crossing in phase C occurs earlier than phase A due to the higher inductor current slew rate during the on-time in phase C. Based on abovementioned analysis, it is concluded that there is a specific operating point between 30 °and 56 °, at which the inductor current zero crossing occurs simultaneously in switching cycles for these two phases. Simulation shows that this specific operating point is 40 °in the PF = 0.9 (ψ = 26 °) case, which is the starting point of the interval 4 in Fig. 3-6.

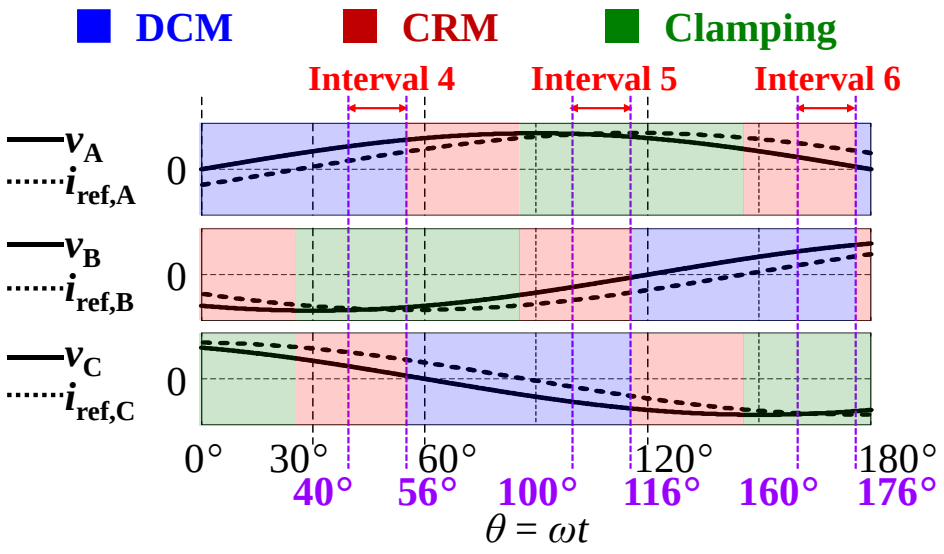


Fig. 3-6. Line-cycle operation mode with DPWM clamping based on ac reference current under PF = 0.9 (ψ = 26 °) condition; the 2nd type hard switching turn-on exists during the intervals 4, 5, and 6 over this half line-cycle (v_A, v_B, and v_C are ac line-to-neutral voltages in phases A, B, and C, respectively; $i_{ref,A}$, $i_{ref,B}$, and $i_{ref,C}$ are ac reference currents in phases A, B, and C, respectively).

With the CRM/DCM transition angle $\theta_T = 56°$, CCM operation appears in phase A, which is analyzed as follows. According to Fig. 3-1, starting from the 26 °operating point, phase A operates at DCM, and phase C operates at CRM. The DCM dead time in phase A gets shorter as it is approaching the 40 ° operating point. After the 40 ° operating point, the switching-cycle inductor current zero crossing occurs earlier in phase C than phase A. If the turn-on instant in these two phases is still determined by the inductor current zero crossing in phase C, then due to the per-switching-cycle volt-second unbalance, CCM hard-switching operation will occur in phase A, as shown in both Fig. 3-4 (b) and Fig. 3-5.

Besides, sub-harmonic oscillation occurs in CCM operation, which is explained as follows. First, assume that the CCM hard switching operation is stable in phase A. Then, on one hand, four independent constraints must be met for a stable operation: the per-switching-cycle volt-second balance and the average current control in both phase A and phase C. On the other hand, from the control point of view, there are only three independent variables in these two phases: the on-time in each phase and the switching period shared by these two phases (the off-time is determined by the on-time and the switching period). It is impossible to make three independent variables always meet four independent constraints, which is in conflict with the previous assumption. The sub-harmonic oscillation occurs due to the fact that not all of the four independent constraints are satisfied. This unstable operation does not exist when phase A operates at DCM, since there is one more independent variable in phase A: the dead-time period.

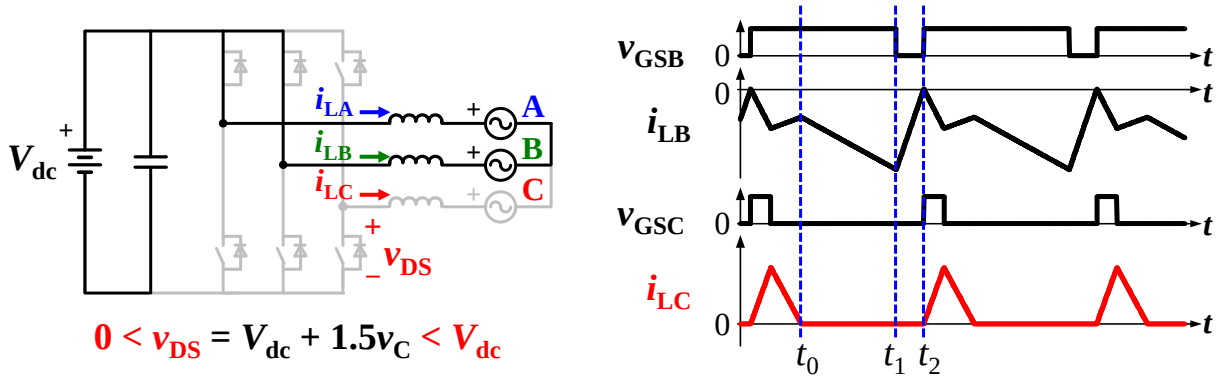
In summary, when the original CRM-based soft switching modulation strategy proposed in Chapter 2 is directly applied into non-unity power factor operating conditions, two types of hard-switching turn-on will show up. The first type is positive current turn-on during DCM operation, due to the undesired body diode conduction of the SR device before the turn-on instant of the

control switch. The second type is the CCM hard switching turn-on, due to the non-optimal CRM/DCM transition angle.

3.3 Proposed Generalized Soft Switching Modulation Technique for Both Unity and Non-Unity Power Factor Conditions

As for the first type of hard-switching turn-on, the proposed improvement is to modify the DPWM clamping option around 70 ° operating point by clamping phase A to the positive dc bus instead of clamping phase B to the negative dc bus. With this improvement, phase B operates at CRM, and phase C still operates at DCM. The negative ac reference current indicates the bottom switch acts as the control switch, whereas the top switch acts as the SR in phase B. After the control switch is turned off and the SR is turned on in phase B as the equivalent circuit shown in Fig. 3-7 (a), the drain–source voltage of the bottom switch in phase C is positive and lower than the dc bus voltage. This indicates that phase C is still kept disconnected with the system, and, thus, the undesired bottom switch (SR) body diode conduction is avoided. This modification of DPWM clamping is equivalent to applying DPWM clamping to the phase with highest ac line-to-neutral voltage amplitude.

Simulation verification with this improvement is shown in Fig. 3-7 (b), indicating no hard-switching positive current turn-on in phase C. The simulated DCM turn-on loss with the original current-based DPWM clamping and that with the proposed voltage-based DPWM clamping are shown in Fig. 3-8 (a). Also, the tested loss reduction from current-based DPWM clamping to voltage-based DPWM clamping is shown in Fig. 3-8 (b), which matches the difference of DCM turn-on loss between these two cases and verifies the benefits of the improvement.



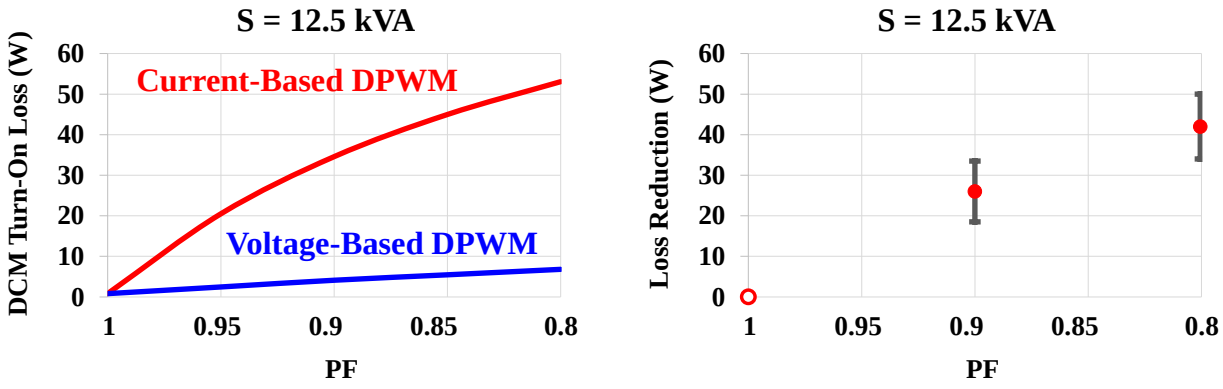
(a) (b)

Fig. 3-7. (a) Equivalent circuit during the DCM dead-time interval after the control switch is turned off and the SR is turned on in phase B. (b) Simulated switching-cycle waveforms around 70 °operating point with modified DPWM clamping under PF = 0.9 (ψ = 26 °) condition to indicate that DCM hard-switching turn-on is avoided, especially $t_1 - t_2$ is corresponding to panel (a) (V_{dc} is the dc bus voltage; v_C is the ac line-to-neutral voltage in phase C; v_{GSB} and v_{GSC} are the control switch gate signals in phases B and C, respectively; i_{LB} and i_{LC} are inductor currents in phases B and C, respectively).

With the voltage-based DPWM clamping, DCM turn-on loss is significantly reduced but still exists, which is because of the DCM valley switching turn-on and is to be discussed in the Appendix. Based on simulation results, the DCM turn-on loss after the improvement is 3.4% out of the total device loss (13.5% out of the switching loss) at PF = 0.9, and 5.3% out of the total device loss (19.3% out of the switching loss) at PF = 0.8, respectively. The detailed device loss breakdown with the improvement is shown later.

Also, it is concluded that the selection of the DPWM clamping option is fundamentally a tradeoff between the turn-on loss and the turn-off loss. The current-based DPWM clamping brings lower turn-off loss but higher turn-on loss, whereas the voltage-based DPWM clamping brings lower turn-on loss but higher turn-off loss. In the SiC-based systems, according to [27, Fig. 9], the

turn-off energy is no more than 10% when compared with the turn-on energy for SiC MOSFETs, and, therefore, the voltage-based DPWM clamping is more suitable.



(a) (b)

Fig. 3-8. (a) Comparison of simulated DCM turn-on loss between current-based DPWM clamping (without improvement) and voltage-based DPWM clamping (with improvement) at different PF values. (b) Tested loss reduction from current-based DPWM clamping to voltage-based DPWM clamping at different PF values.

For the second type of hard-switching turn-on and taking the first 60 °line-cycle interval as an example, the improvement is to make the CRM/DCM transition occur at the operating point when the switching-cycle inductor current zero crossing occurs simultaneously in phase A and phase C to avoid the CCM operation. Define this specific operating point as the optimal CRM/DCM transition angle θ_T^* (with a superscript "*").

To predict this optimal transition angle θ_T^*, a model is developed and is illustrated here. At steady-state operation, the switching-cycle volt-second is balanced in these two phases respectively. Meanwhile, it is assumed that the ac reference current value in one switching cycle is unchanged, and the per-switching-cycle average current is well controlled as the ac reference

current in these two phases respectively. Based on these aspects, key equations are derived as follows:

$$\begin{cases} \int_{t_0}^{t_0+T_{SW}} v_{LX}(t)dt = 0 \\ \dfrac{1}{T_{SW}} \int_{t_0}^{t_0+T_{SW}} i_{LX}(t)dt = I_{ref,X}(\theta,\psi) \end{cases} \tag{3-2}$$

Here, t_0 is the starting point of one switching cycle, T_{SW} is the switching period, V_{LX} is the inductor voltage in phase X, i_{LX} is the inductor current in phase X, and $I_{ref,X}$ is the ac reference current in phase X which is assumed to be constant around each specific line-cycle operating point ("X" represents "A" or "C").

Based on Equation (3-2), the values of the on-time and off-time in phase A and phase C at different operating points during the first $60°$ line-cycle interval are calculated. If at a specific operating point, the summations of on-time and off-time are identical in these two phases, then this operating point is the optimal CRM/DCM transition angle θ_T^*. This is illustrated in Fig. 3-9, using three specific operating points, θ_1, θ_2, and θ_3, as examples to show the sequence of inductor current zero crossing between these two phases (summation of on-time and off-time is marked as the interval between two red dash lines in each phase). It is clear that the optimal CRM/DCM transition angle $\theta_T^* = \theta_2$.

Due to the high order of Equation (3-2), it is hard to derive the analytical solutions for the optimal CRM/DCM transition angle θ_T^*. Therefore, the θ_T^* values are calculated numerically and are verified with simulation. Fig. 3-10 presents the calculated and simulated optimal transition angles θ_T^* at PF from 0.8 to 1 (V_{dc} = 800 V, V_{ac} = 277/480 V). The calculated and simulated results match well, which indicates that the numerical model has sufficient accuracy.

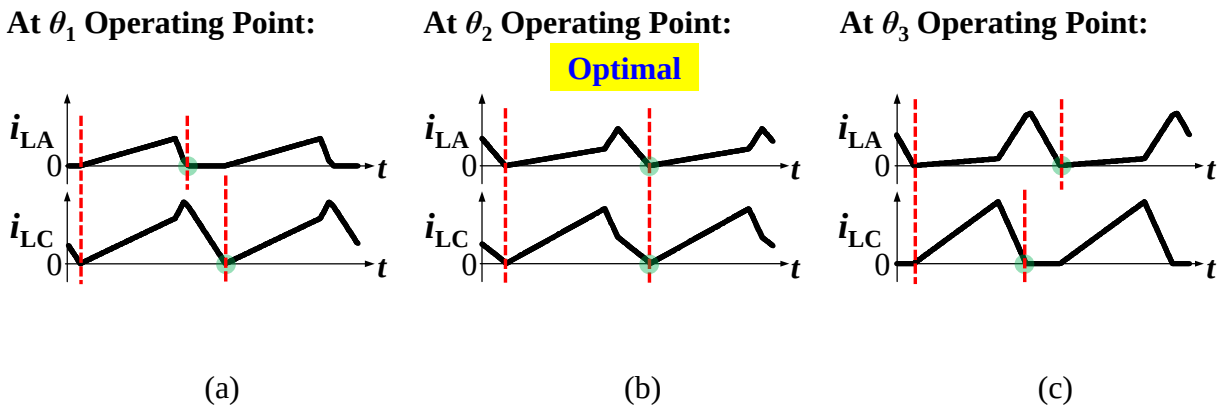


Fig. 3-9. Simulated switching-cycle inductor current waveforms at three example line-cycle operating points: (a) θ_1, (b) θ_2, and (c) θ_3 ($0 < \theta_1 < \theta_2 < \theta_3 < 60$°; PF = 0.9 ($\psi$ = 26°). The optimal DCM/CRM transition angle $\theta_T^* = \theta_2$ because of the simultaneous inductor current zero crossings and i_{LA} and i_{LC} are the inductor currents in phases A and C, respectively).

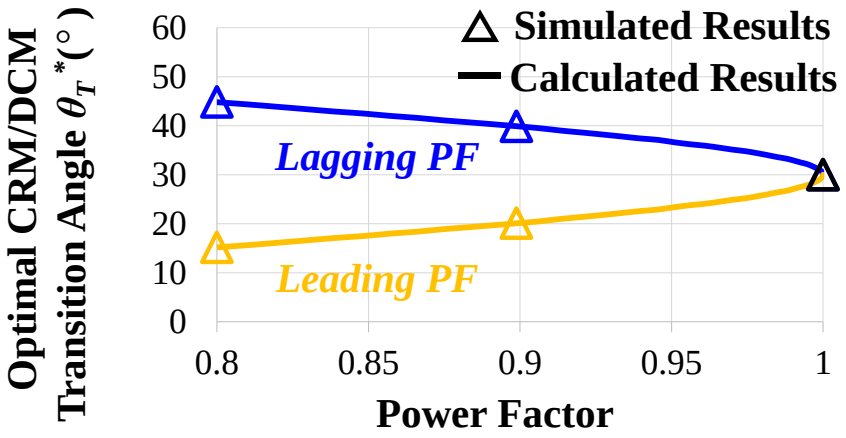
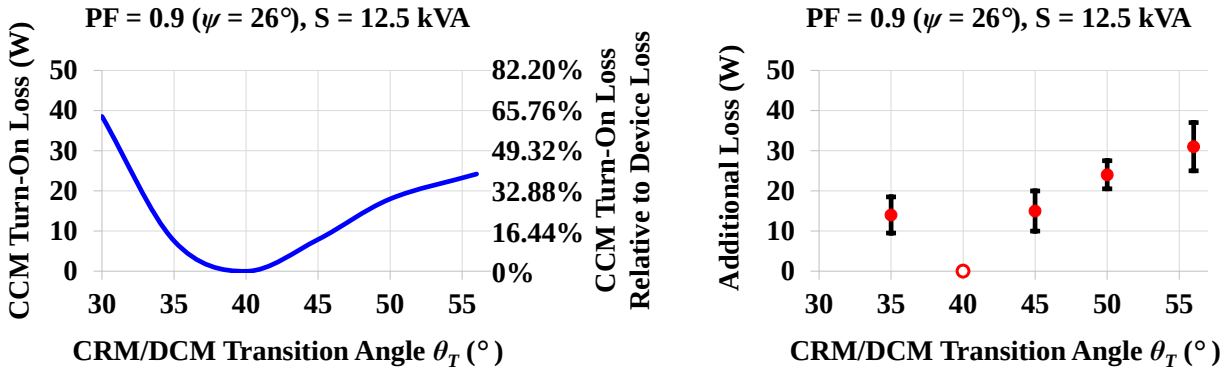


Fig. 3-10. Comparison between simulated and calculated optimal CRM/DCM transition angles θ_T^* under different PF operating conditions.

For digital implementation, the optimal CRM/DCM transition angles θ_T^* is pre-calculated under different PF conditions and loaded into a look-up-table.

It should be noted that some small errors are allowed for the calculation of the optimal CRM/DCM transition angle θ_T^*. Take the PF=0.9 (ψ = 26°) condition as an example. Fig. 3-11 (a)

shows the simulated CCM turn-on loss with different CRM/DCM transition angle θ_T values. There is no CCM turn-on loss when $\theta_T = \theta_T^* = 40$ °, whereas the CCM turn-on loss increases as θ_T goes away from the optimal value. Fig. 3-11 (b) shows tested additional loss at different θ_T values when compared with $\theta_T = \theta_T^* = 40$ °. The tested additional loss matches the simulated CCM turn-on loss, which verifies the benefit of the improvement and the above-mentioned sensitivity analysis.



(a) (b)

Fig. 3-11. (a) Simulated CCM turn-on loss with different CRM/DCM transition angles θ_T under PF = 0.9 (ψ = 26 °) condition. (b) Tested additional loss with different CRM/DCM transition angles θ_T when compared with $\theta_T = \theta_T^* = 40$ °under PF = 0.9 (ψ = 26 °) condition.

With the improvement and neglecting the error in the calculation of θ_T^*, the CCM turn-on loss that is equivalent to 40% of the device loss and 80% of the switching loss is avoided at PF = 0.9. At PF = 0.8, the avoided CCM turn-on loss is equivalent to 56% of the device loss and 103% of the switching loss.

It should be noted that the modulation index also has an impact on the optimal CRM/DCM transition angle θ_T^*. The abovementioned numerical model is applicable to other modulation index conditions to calculate the θ_T^* values. Load conditions do not have impact on the optimal CRM/DCM transition angle θ_T^*. The change of load conditions brings a proportional change in

the ac reference current at each operating point and consequently, a proportional change in the switching period. However, the operating point with the simultaneous inductor current zero crossing in each phase does not change.

According to the aforementioned solutions to each type of hard-switching turn-on related issues, it is obvious that with the proposed solutions, the modulation technique is still suitable for the unity PF condition. Therefore a generalized "DPWM + CRM + Fs sync" modulation concept is summarized, covering both unity and non-unity PF operating conditions with the PF value down to 0.8 ($\psi = \pm 37°$). First, the DPWM clamping is applied to the phase with the highest ac line-to-neutral voltage amplitude. Second, for the other two phases, the one in which the inductor current zero crossing first occurs should operate at DCM, whereas the other one should operate at CRM. The synchronization of turn-on instants still applies between these two phases.

Fig. 3-12 presents the operation mode over a half line-cycle under the aforementioned example modulation index condition at PF = 0.9 ($\psi = \pm 26°$). The DPWM clamping zone is not changed as the variation of the PF since the ac line-to-neutral voltage is used as the reference when defining the zero of the line-cycle phase angle. The optimal CRM/DCM transition angle θ_T^* varies under different PF conditions.

The operational symmetry between the lagging condition and the leading condition under the same PF value is also demonstrated in Fig. 3-12. Take the 40° operating point under PF = 0.9 ($\psi = 26°$) condition and the 20° operating point under PF = 0.9 ($\psi = -26°$) condition as examples. The V_B value and the $I_{ref,B}$ value at these two operating points are identical, respectively. The V_A value and the $I_{ref,A}$ value at the first operating point is the same as the V_C value and the $I_{ref,C}$ value at the second operating point, respectively, whereas the V_A value and the $I_{ref,A}$ value at the second operating point is the same as the V_C value and the $I_{ref,C}$ value at the first operating point,

respectively. Therefore, the operation in phase A, phase B, and phase C in the first operating point is exactly the same as the operation in phase C, phase B, and phase A in the second operating point, respectively.

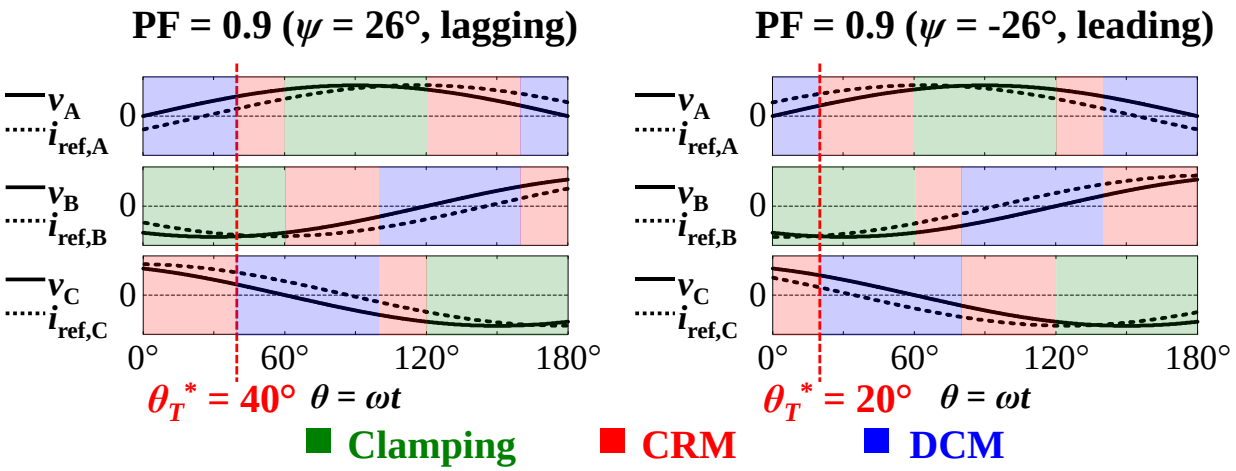


Fig. 3-12. Operation mode with the generalized DPWM + CRM + Fs sync modulation concept under PF=0.9 ($\psi = \pm 26°$) conditions to show operational symmetry.

Furthermore, it should be noted the 30 ° operating point is the axis of the above-mentioned operational symmetry during the first 60 ° line-cycle interval. Since the operation repeats itself every 60 °line-cycle interval, the abovementioned operational symmetry exists over the whole line cycle.

As for the proposed generalized "DPWM + CRM + Fs sync" modulation concept, when compared with the original modulation concept proposed in Chapter 2 under non-unity PF conditions, there is an increase in the inductor current RMS value, which brings consequential increase in the conduction loss. The increase in RMS current value is 4.1% at PF = 0.9 and 5.0% at PF = 0.8, which indicates the increase in the conduction loss is 8.4% and 10.3%, respectively. However, the increased conduction loss is less than 6% out of the total device loss. Therefore, the

price paid on the conduction loss is almost negligible when compared with the benefits from the soft switching with the two improvements.

With the proposed generalized "DPWM + CRM + Fs sync" modulation concept, Fig. 3-13 presents the switching frequency variation over a half line-cycle in phase A under different PF operating conditions, with 300 kHz minimum switching frequency under the unity PF condition. The switching frequency variation range is still relatively narrow at $0.8 \leq PF < 1$ operating condition. The axis of the operational symmetry is also clearly presented in Fig. 3-13.

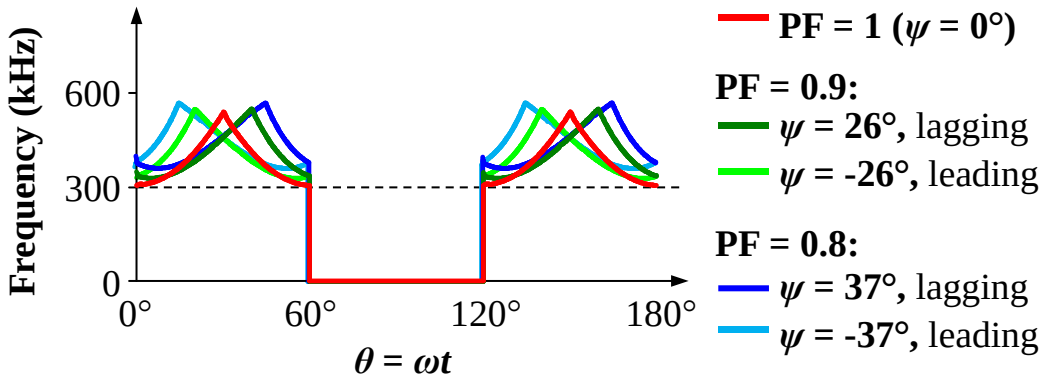


Fig. 3-13. Switching frequency variation over a half line-cycle under different PF conditions.

In sum, to solve the two hard-switching related issues, the original soft-switching modulation technique is improved and a generalized "DPWM + CRM + Fs sync" modulation technique is proposed. For both the unity and non-unity PF conditions, the DPWM clamping is applied to the phase with highest ac line-to-neutral voltage amplitude, and the optimal CRM/DCM transition angle is dependent on PF values, which is predicted by a developed numerical model and implemented by look-up-table in MCU.

Similar to Chapter 2, further quantitative analysis about the realization of CRM ZVS turn-on and DCM valley switching turn-on is shown in the Appendix. Under non-unity power factor conditions, as the PF value goes lower, at some operating points over a whole line cycle, off-time

extension becomes necessary for achieving CRM ZVS turn-on. In addition, as the PF value goes lower, the valley voltage at the DCM valley switching turn-on becomes higher.

With the generalized "DPWM+CRM+Fs sync" modulation technique and the aforementioned strategies to achieve soft switching and to reduce switching loss, Fig. 3-14 presents the simulated semiconductor device loss breakdown under different PF conditions. With the same PF value, the loss breakdown at the lagging condition is similar to that at the leading condition. Therefore, only the results at lagging conditions are shown here. It shows that with the proposed DPWM clamping options according to ac phase voltage, although the turn-off loss increases at a lower PF value, this increase is still negligible when compared with the system total power. Furthermore, the DCM turn-on loss is only 5.3% out of the total device loss (19.3% out of the switching loss) even at PF = 0.8. Therefore, the benefit on the system efficiency is clearly presented. The total device loss at non-unity PF conditions is similar to that under the unity PF condition, with 7.0% increase at PF = 0.9 and 13.9% increase at PF = 0.8, respectively. The aforementioned increase compared with the unity PF condition is mainly caused by increased turn-off current, increased switching frequency, and DCM valley switching turn-on.

It should be noted that all the analysis process is applicable to the leading PF conditions since at the same PF value, there is operational symmetry between the leading PF condition and the lagging PF condition, as analyzed in the last section. Also, all the analysis process is applicable to other modulation index conditions.

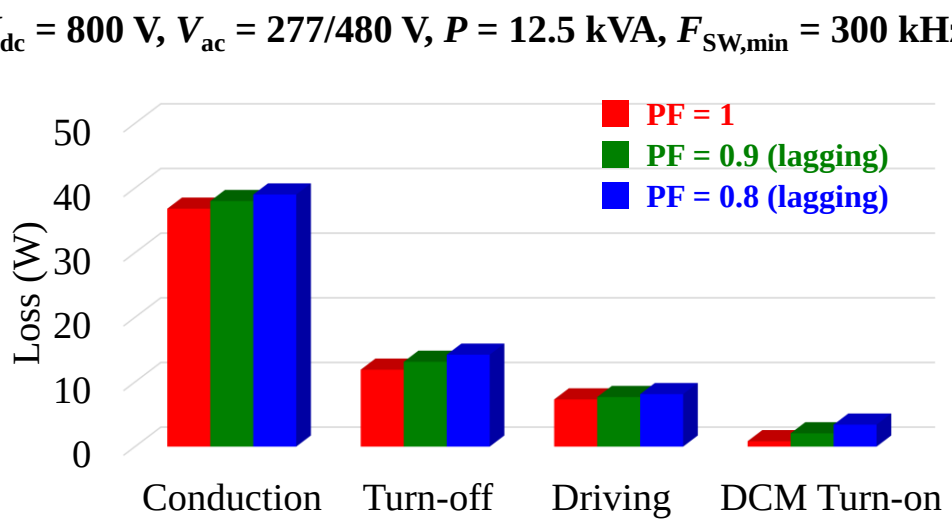
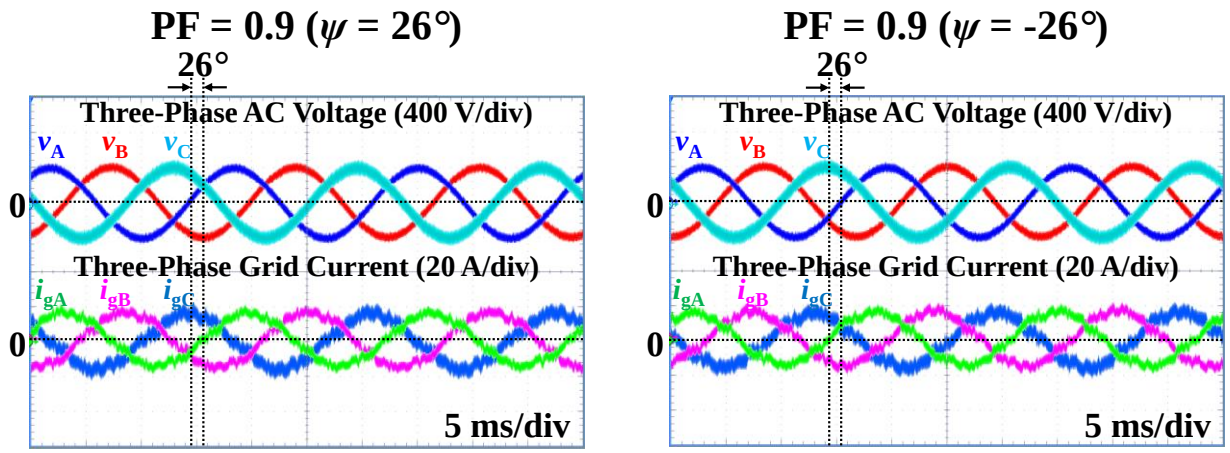


Fig. 3-14. Simulated device loss breakdown under different PF operating conditions.

3.4 Experimental Verifications

The above-mentioned modulation technique is digitally implemented with the same low-cost MCU and experimentally verified on the same 25-kVA SiC-based three-phase bidirectional ac–dc converter prototype as shown in Chapter 2. The detailed parameters of the prototype are shown in Table 2-2. In order to verify the effectiveness of the proposed modulation concept and further make a fair comparison with the test results in Chapter 2, similarly, the test here is focused on one 12.5-kVA module with the second 12.5-kVA module disabled.

Fig. 3-15 (a) and (b) presents three-phase line-cycle experimental waveforms of ac line-to-neutral voltages and grid-side currents at 12.5 kVA, under PF=0.9 (ψ = ±26°) conditions. The capability of reactive power transfer is verified for both the lagging condition and the leading condition.



(a) (b)

Fig. 3-15. Line-cycle experimental results at PF = 0.9. (a) Lagging condition. (b) Leading condition. (v_A, v_B, and v_C are three-phase ac line-to-neutral voltages; i_{gA}, i_{gB}, and i_{gC} are three-phase grid currents; hereinafter the same).

According to the aforementioned operational symmetry between the lagging condition and the leading condition with the same PF value, here only the switching-cycle waveforms under lagging PF conditions are shown. Fig. 3-16 (a)–(c) presents switching-cycle experimental waveforms at three operating points around 10 °, 30 °, and 50 ° in phase A under PF = 0.9 lagging condition, and Fig. 3-16 (d)–(f) presents switching-cycle experimental waveforms at the same three operating points in phase C under the same condition. At each operating point, the control switch is turned on at zero drain–source voltage during CRM and at the valley point during DCM operation.

Fig. 3-17 (a) and (b) presents three-phase line-cycle experimental waveforms of ac line-to-neutral voltages and grid-side currents at 12.5 kVA, under PF = 0.8 (ψ = ±37 °) conditions. The capability of reactive power transfer is verified for both the lagging condition and the leading condition.

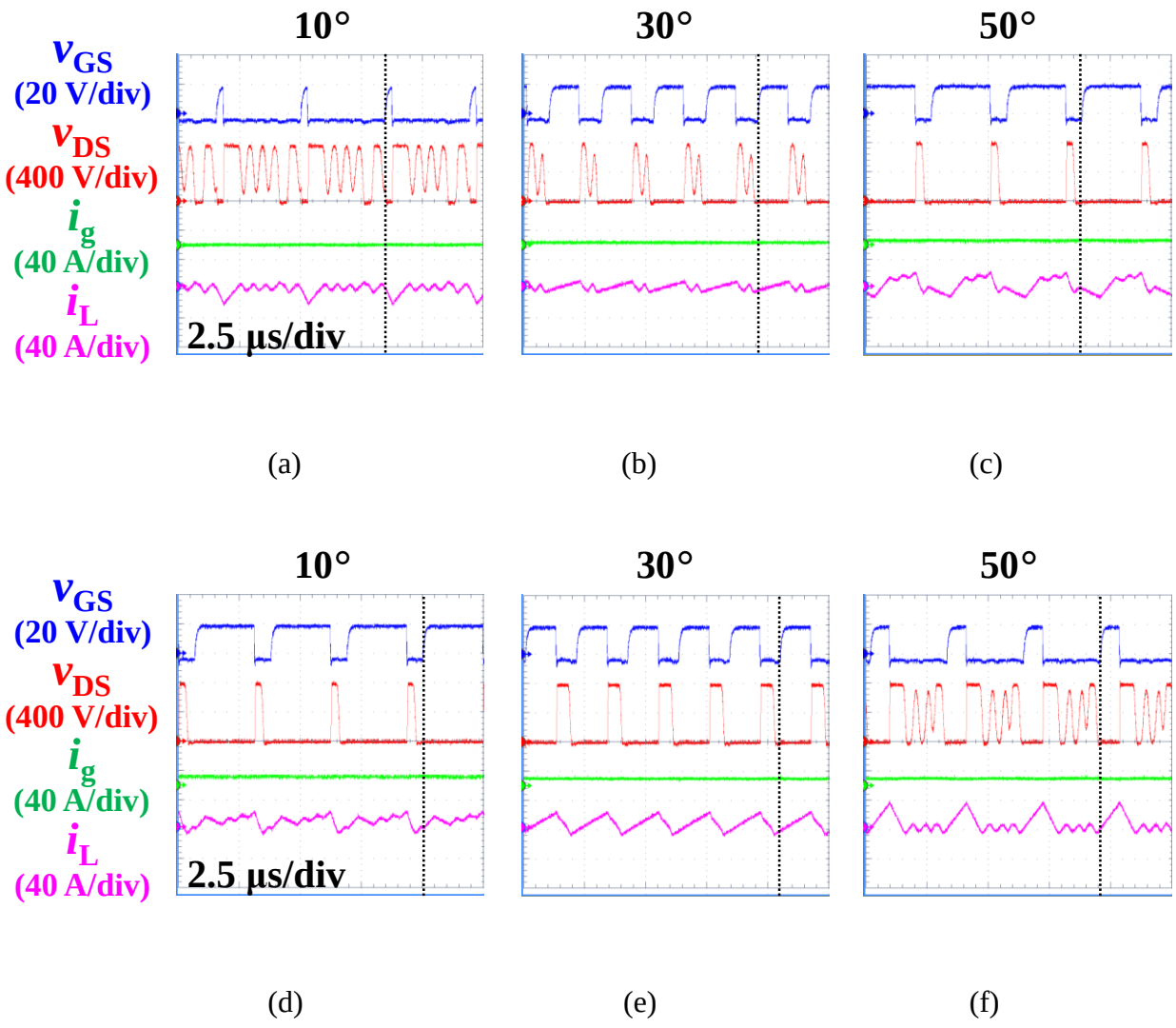
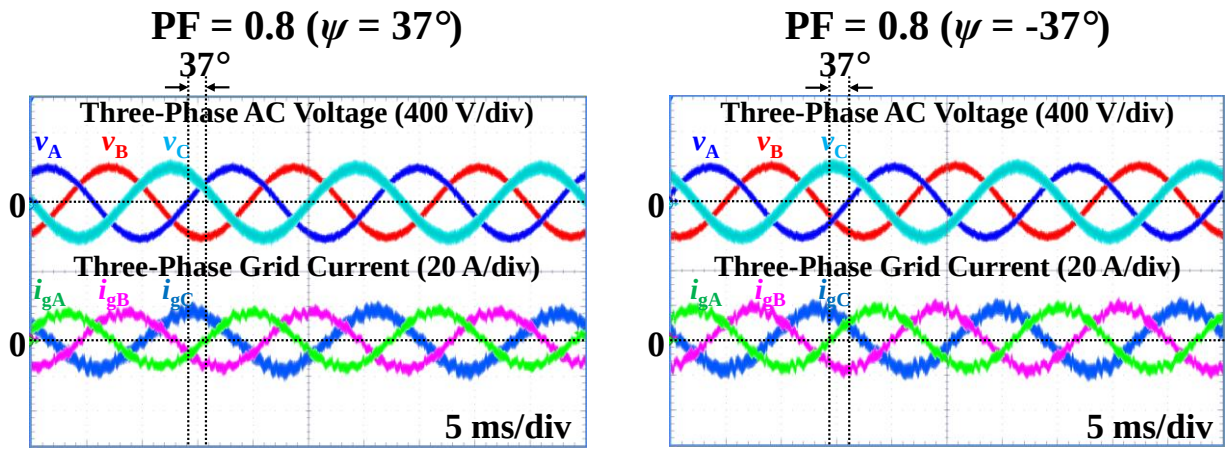


Fig. 3-16. Switching-cycle experimental waveforms under PF = 0.9 (lagging) condition at the following operating points. (a) Around 10 °in phase A. (b) Around 30 °in phase A. (c) Around 50 °in phase A. (d) Around 10 °in phase C. (e) Around 30 °in phase C. (f) Around 50 °in phase C. (In each figure, v_{GS} is the control switch gate signal; v_{DS} is the control switch drain–source voltage; i_g is the grid current; i_L is the inductor current; hereinafter the same).



(a) (b)

Fig. 3-17. Line-cycle experimental results at PF = 0.8. (a) Lagging condition. (b) Leading condition.

Fig. 3-18 (a)–(c) presents switching-cycle experimental waveforms at three operating points around 10°, 30°, and 50° in phase A under PF = 0.8 lagging condition, and Fig. 3-18 (d)–(f) presents switching-cycle experimental waveforms at the same three operating points in phase C under the same condition. At each operating point, the control switch is turned on at zero drain–source voltage during CRM and at the valley point during DCM operation.

With the proposed improved modulation operating at above 300 kHz switching frequency, the system efficiency is tested at 12.5 kVA power under different PF values, as shown in Fig. 3-19. The efficiency is tested with the power analyzer from YOKOGAWA with part number of PZ4000. The error is up to ±0.20% according to the tested results. With the two proposed improvements, 0.5% higher efficiency at PF = 0.9 and 0.9% higher efficiency at PF = 0.8 are achieved, which verifies the effectiveness of the two aforementioned improvements. The efficiency is above 98.0% at PF = 0.8 condition, even when the operating switching frequency is above 300 kHz.

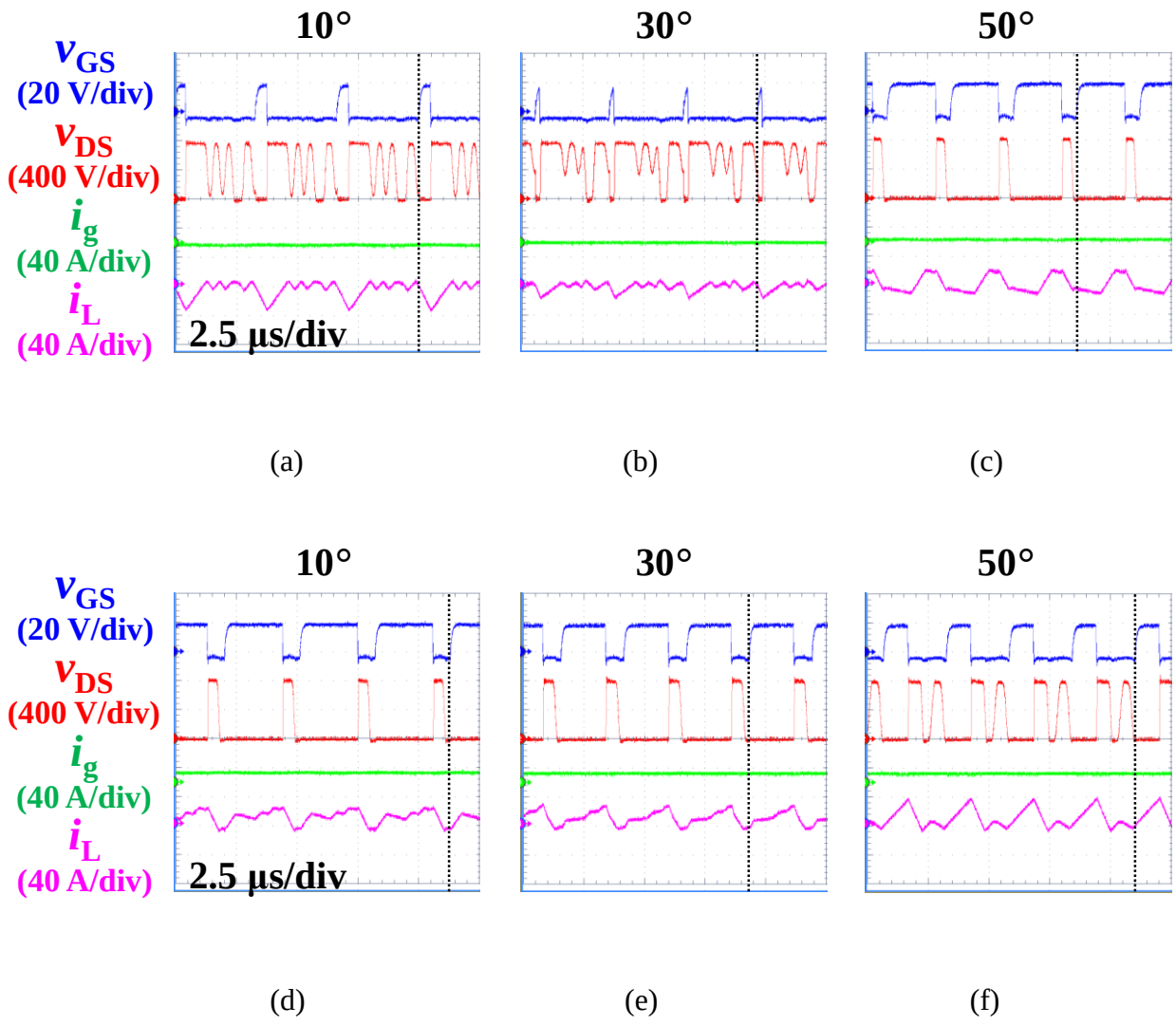


Fig. 3-18. Switching-cycle experimental waveforms under PF = 0.8 (lagging) condition at the following operating points. (a) Around 10 °in phase A. (b) Around 30 °in phase A. (c) Around 50 °in phase A. (d) Around 10 °in phase C. (e) Around 30 °in phase C. (f) Around 50 °in phase C.

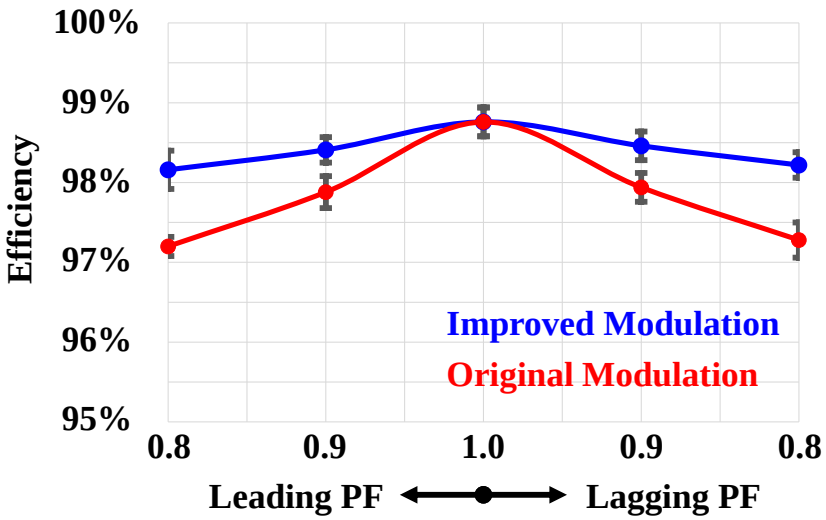


Fig. 3-19. Tested efficiency at 12.5 kVA power under different PF values with the original and proposed improved modulation at above 300 kHz.

3.5 Conclusions

In this chapter, a generalized "DPWM + CRM + Fs sync" modulation technique is proposed for three-phase grid-tied inverter applications, covering both unity and non-unity PF operating conditions (0.8 lagging–0.8 leading for typical PV applications), with the objective of reducing switching loss. DPWM clamping is applied to the phase with highest ac line-to-neutral voltage amplitude. Control switches in the other two phases are turned on in each switching cycle when the inductor current zero crossing occurs in both of these two phases, which determines the assignment of DCM and CRM operation modes in these two phases and the optimal CRM/DCM transition angle. This optimal transition angle is predictable according to the proposed numerical model with enough accuracy. With this generalized modulation concept, soft switching is achieved during CRM and DCM operation, which is beneficial for high efficiency at hundreds of kilohertz high-frequency operation with SiC MOSFETs. All the control functions are implemented with one low-cost MCU, and the capability of reactive power transfer and soft switching are verified on a

SiC-based high-frequency three-phase bidirectional ac–dc converter prototype with 98.9% peak efficiency at the unity PF condition and above 300 kHz switching frequency. Benefits from the proposed improvements are also experimentally validated, and the tested peak efficiency is above 98.0% within the typical PF range in PV applications.

Chapter 4 Interleaving Control and Balance Technique for EMI Noise Reduction

4.1 Introduction

In previous chapters, with the "DPWM + CRM + Fs sync." soft switching modulation, 98.9% high efficiency is achieved on a SiC-based three-phase ac-dc system even at above 300 kHz switching frequency operation, which indicates similar efficiency but at least three-time size reduction when compared with the industry practice at the time this research was conducted. However, the conducted electromagnetic interference (EMI) noise becomes a more serious concern when compared with the conventional Si-based systems at 20 – 30 kHz operating switching frequency.

Generally, there are two types of conducted EMI noise (hereinafter "EMI noise" unless otherwise specified): differential-mode (DM) EMI noise and common-mode (CM) EMI noise [40], [41]. Fig. 4-1 shows the propagation path of these two types of EMI noise in a typical two-stage structure based on the applications of this dissertation. A line impedance stabilization network (LISN) is connected between the three-phase ac grid and the converter to separate the noise on two sides when the EMI noise is measured. The DM EMI noise goes through and returns from the main power paths but not the earth, while the CM EMI noise goes through the main power paths and returns from the earth due to the existence of the parasitic capacitance between the systems and the earth. It can be seen that the DM EMI noise is dominated by the ac (inductor) current ripple in the ac-dc stage, while the CM EMI noise is generated by the voltage changing rate ($\mathrm{d}v/\mathrm{d}t$) across the parasitic capacitance between the system and the earth. Although EMI filters exist between the power converters and the ac grid in order to meet the corresponding EMI standard and prevent the

EMI noise from interfering other components, the higher raw EMI noise at the converter side diminishes the benefits brought by high-frequency operation on EMI filter size reduction.

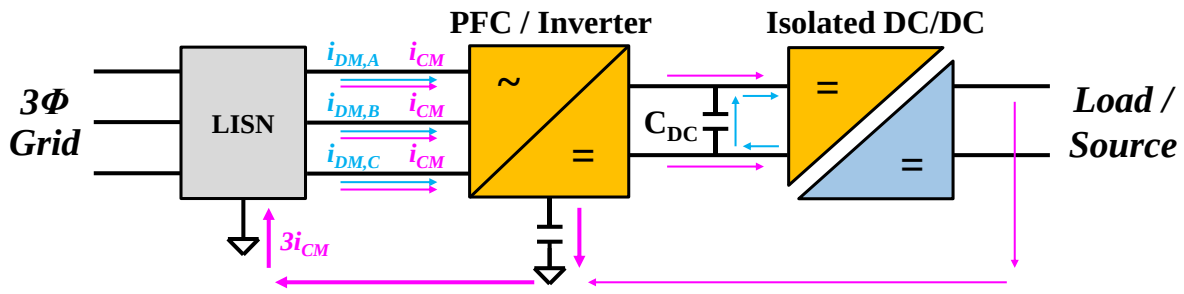


Fig. 4-1. Propagation path of the conducted EMI noise.

As for the DM EMI noise, the CRM and DCM operation in the soft switching modulation technique makes the inductor current ripple at least twice of the ac reference current value. In contrast, in the conventional Si-based design, the inductor current ripple is only around 20% of the ac reference current under CCM operation. Therefore, approximately ten-time higher DM EMI noise exists in the SiC-based high-frequency three-phase ac-dc system developed in the previous chapters. The multi-channel interleaving control [42], a relatively mature control technique in single-phase CRM ac-dc converters, is to be applied here to reduce the DM EMI noise.

As for the CM EMI noise, under the same voltage rating and similar current rating, SiC power semiconductor devices feature more than ten times higher switching speed, namely the dv/dt, especially during the turn-off transition period, when compared with their Si counterparts [43], [44]. Therefore, significantly higher CM EMI noise exists in the SiC-based high-frequency three-phase ac-dc system developed in the previous chapters. The balance technique is commonly used in the ac–dc systems in order to reduce the raw CM EMI noise at the converter side, for both single-phase systems [45], [46] and three-phase systems [47]. The similar balance technique is to be applied into the interleaved three-phase ac–dc systems here.

4.2 Reduction of DM Noise with Interleaving Control

As previously mentioned, the large inductor current ripple is a drawback of CRM and DCM operations, which brings high DM EMI noise and diminishes the benefits brought by the high switching frequency operation.

From the literature, multi-channel interleaving control is widely applied for the cancellation of the inductor current ripple. Theoretically with the perfect interleaving control, the fundamental switching frequency component can be eliminated, and the harmonic switching frequency components will be left, whose amplitudes are usually no higher than that of the fundamental component. Therefore, the harmonic components instead of the fundamental component become dominant and with the same structure of the DM EMI filter, the corner frequency of the DM EMI filter increases, which indicates the size reduction in the DM EMI filter.

The two-channel interleaving control is applied here to make the three-phase ac-dc system get benefits from the ripple cancellation effects but not become too complicated. Fig. 4-2 shows the circuit diagram of the two-channel interleaved three-phase ac-dc converter. The ac side filters are ignored here for better illustration of the raw noise source. There are totally 6 channels (phase legs) and 12 SiC MOSFETs power semiconductor devices in this structure. To facilitate the illustration in later sections, the 6 channels are named as "Channel A_1", "Channel A_2", and so on. The first channel (Channel A_1, etc.) in each phase is the master channel and the second channel (Channel A_2, etc.) is the slave channel. This is applicable to the entire dissertation unless otherwise specified.

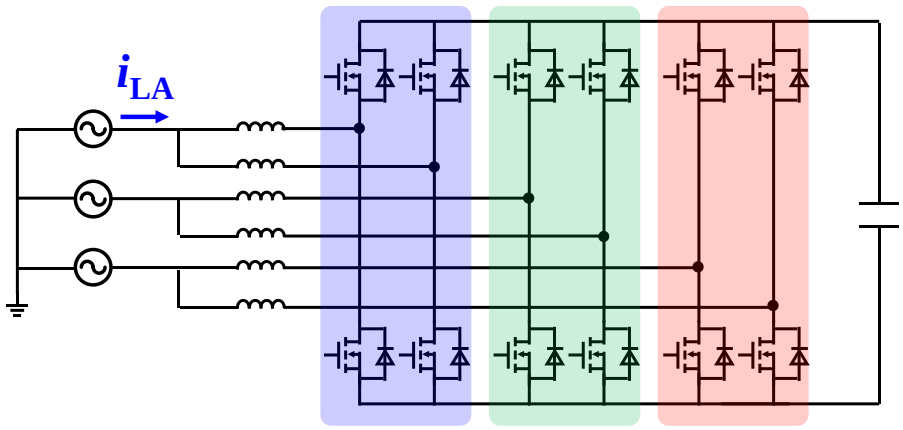
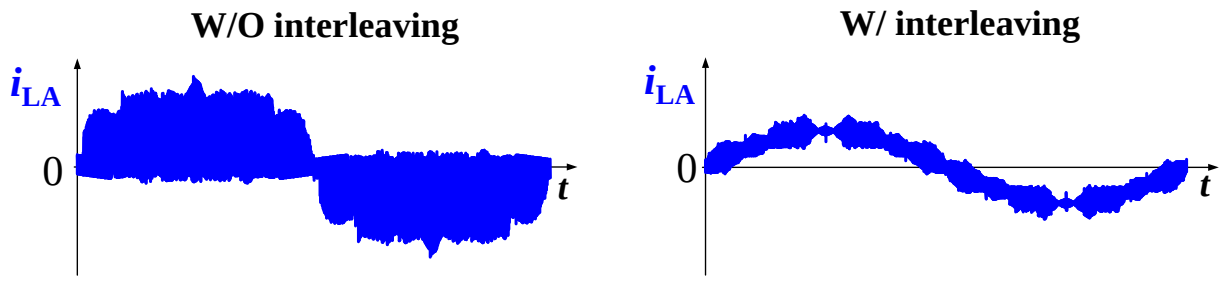


Fig. 4-2. Circuit diagram of the two-channel interleaved three-phase ac-dc converter.

As for methods of two-channel interleaving control, compared with PLL-based closed-loop interleaving control method [48] – [51], the master-slave-based open-loop interleaving control method [52] – [57] is more suitable in several hundreds of kHz to MHz high switching frequency and digital-control-based applications, which has been applied in single-phase CRM AC/DC converter in [27]. It is experimentally verified that with two-channel interleaving, the corner frequency of DM EMI filter has an eight-time increase, which indicates significant DM EMI filter size reduction [37] – [39], [42].

Therefore, the master-slave-based open-loop interleaving control method is selected for implementation in this work. Under the same power, taking the inverter mode operation as an example, the simulation waveforms of the total inductor current in phase A (denoted as "i_{LA}" in Fig. 4-2) over a line cycle without and with two-channel interleaving are shown in Fig. 4-3. It can be clearly seen the total inductor current ripple cancellation effect with two-channel interleaving.



(a) (b)

Fig. 4-3. Line-cycle simulation waveforms of total inductor current in phase A: (a) without interleaving (b) with two-channel interleaving.

In addition to the cancellation effect reflected in the total inductor current ripple, the individual inductor current ripple in each channel is reduced during the interval operating at clamping mode, which is another benefit of the application of two-channel interleaving with "DPWM + CRM + Fs sync." soft switching modulation. This benefit can be better illustrated using switching-cycle waveforms in Fig. 4-4, where the total inductor current is denoted as "i_{LX}" and the individual inductor current is denoted as "$i_{LX1/2}$" (X = A, B, C). Here the first 30 °line-cycle interval is taken as an example, when phase A is operating at DCM, phase C is operating at CRM, and phase B is operating at clamping mode. The total inductor current ripple in phase B is determined by the summation of total inductor current in the other two phases. Because of the cancellation in the total inductor current ripple brought by two-channel interleaving in phase A and in phase C, it can be seen that the total inductor current ripple in phase B is smaller compared with the case without interleaving. During the clamping mode operation, the individual inductor current ripple is equal to half of the total inductor current ripple in this phase. Therefore, with two-channel interleaving, the individual inductor current ripple is reduced during the clamping mode operation.

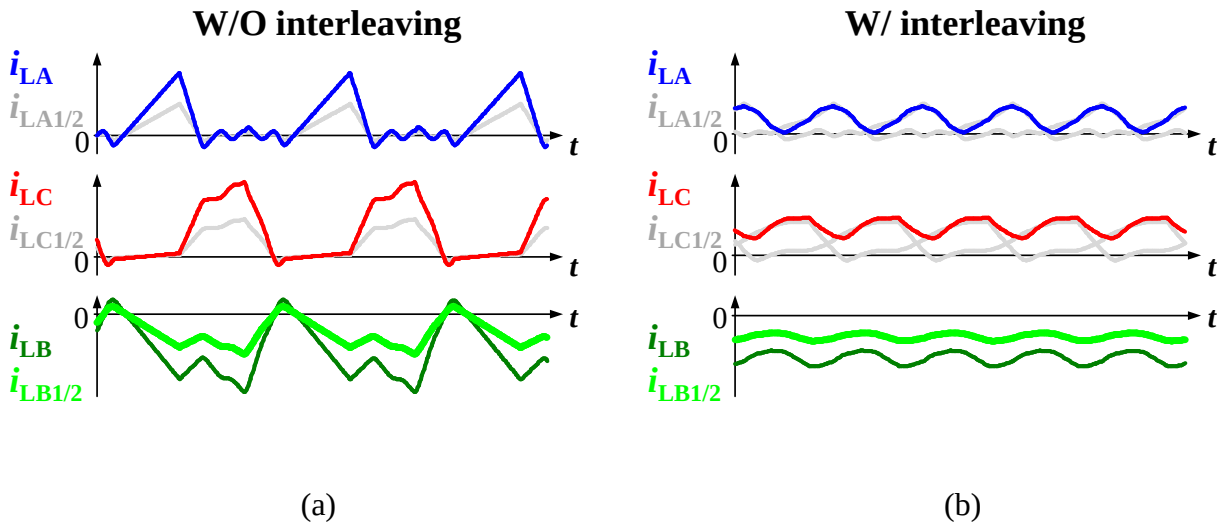


Fig. 4-4. Switching-cycle simulation waveforms of total and individual inductor current in each phase: (a) without interleaving (b) with two-channel interleaving.

Under the same power, the simulation waveforms of an individual inductor current in phase A, i_{LA1}, over a line cycle without and with two-channel interleaving are shown in Fig. 4-5. It can be clearly seen that the individual inductor current ripple is reduced during clamping mode operation with two-channel interleaving. According to simulation results based on the operating condition and system parameters shown in Table 2-2, about 20% conduction loss reduction is achieved due to this individual inductor current ripple reduction during clamping mode operation.

4.2.1 Negative Coupled Inductors for Stability in Interleaved Converters

In the rectifier mode operation, instability occurs with the two-channel interleaving, while the instability does not exist in the inverter mode operation. Fig. 4-6 shows the line-cycle and switching-cycle waveforms in two-channel interleaved rectifier mode operation, including the master-channel individual inductor current and the total inductor current in phase A. It can be clearly seen that there is sub-harmonic oscillation in the inductor current waveforms.

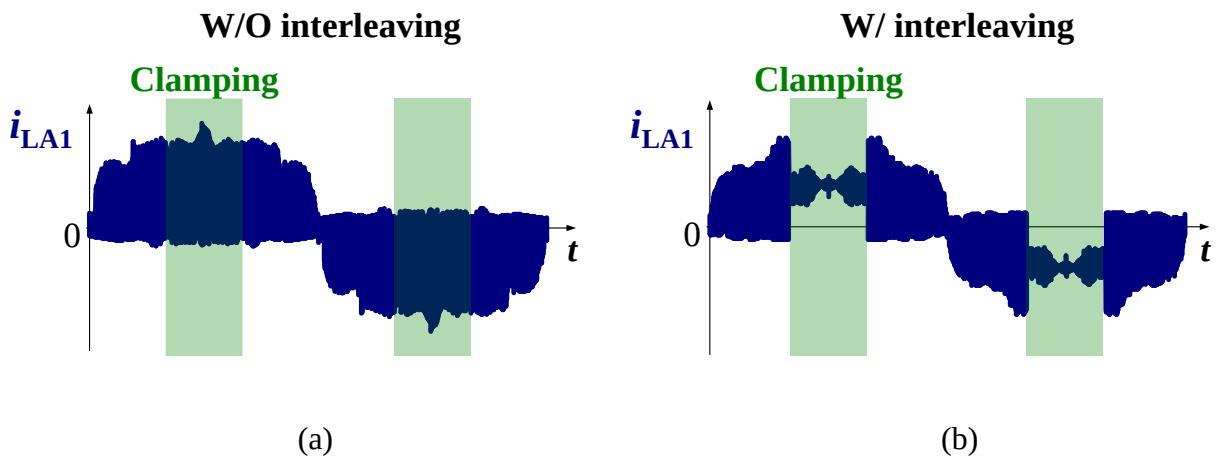


Fig. 4-5. Line-cycle simulation waveforms of individual inductor current in phase A: (a) without interleaving (b) with two-channel interleaving

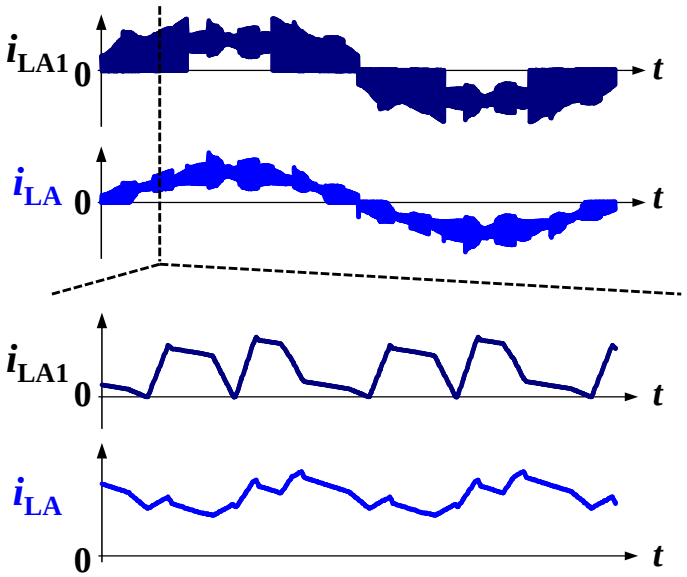


Fig. 4-6. Line-cycle and switching-cycle inductor current waveforms in rectifier mode operation of the two-channel interleaved three-phase ac-dc converter.

The reason of the instability is qualitatively explained as below. With CRM-based soft switching modulation, the switching frequency is time-variant during a whole line cycle. The variance of switching period in the master channel will cause phase error and impact the switching actions in the slave channel, because sometimes the interleaving control cannot be implemented

cycle-by-cycle but may be at least every two or three switching cycles. On the other hand, due to the existence of the ac side common node, all the 6 channels get influenced when a switching action occurs in one channel. Thus, the switching action in the slave channel will also impact the inductor volt-second, and thus the switching period in the master channel. Therefore, a new feedback loop related to the two-channel interleaving is formed. Instability issue exists when the phase margin of this feedback loop is insufficient.

The main reason of the instability in the two-channel-interleaved rectifier mode operation is that the current slew rate before the master channel inductor current (i_{LA1} in phase A) zero crossing point is very small, in contrast to the large current slew rate in the two-channel-interleaved inverter mode operation. This current slew rate at different operating points over the first 30 ° line-cycle interval at two-channel interleaved rectifier mode operation is shown in Fig. 4-7, as a comparison with that at interleaved inverter mode operation. This current slew rate is based on the 300 kHz minimum switching frequency.

Depending on whether the DCM dead time is longer than 50% of switching period or not, two different switching sequences exist during this 30 ° line-cycle interval, with the boundary at around the 15 ° operating point. The typical switching-cycle inductor current waveforms under these two sequences are shown in Fig. 4-8. The sudden change of the inductor current slew rate in Fig. 4-7 at around the 15 ° operating point is due to the change from one switching sequence to the other. The instability starts from around the 15 ° operating point, which is corresponding to the sudden drop of the inductor current slew rate prior to the zero crossing point. The small inductor current slew rate makes the small signal modulation gain and bandwidth of the aforementioned feedback loop high, and thus phase margin is insufficient to maintain stable operation when there is perturbation (time-variant switching frequency/period over the whole line cycle).

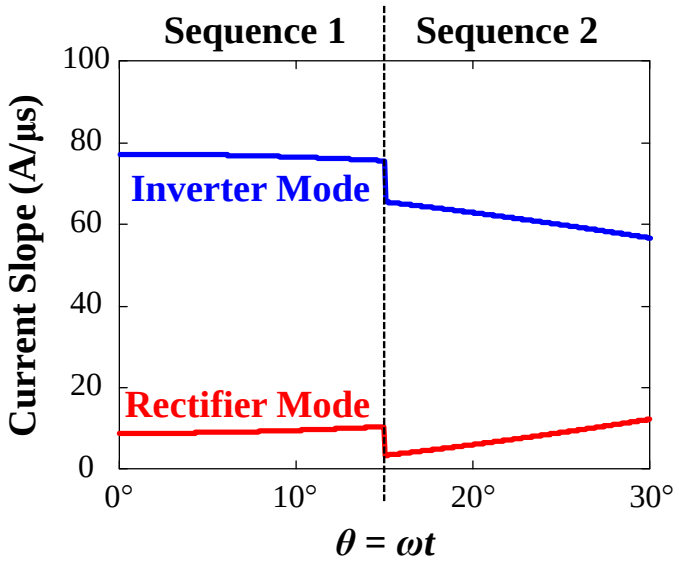


Fig. 4-7. Variation of inductor current slew rate prior to zero crossing over the first 30 °line-cycle interval: comparison between interleaved inverter mode and interleaved rectifier mode.

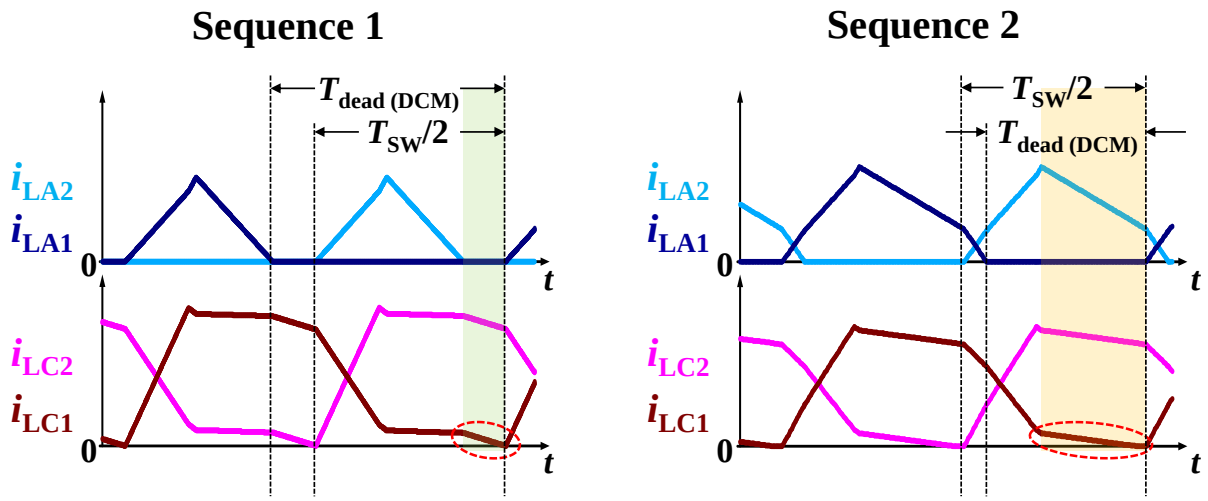


Fig. 4-8. Typical switching-cycle inductor current waveforms under (a) Sequence 1: DCM dead-time is short than half of switching period; (b) Sequence 2: DCM dead-time is longer than half of switching period.

In order to modify the inductor current slew rate and maintain the stable operation, negative coupled inductors are applied into the two-channel interleaved three-phase ac-dc converter. The circuit diagram with negative coupled inductors is shown in Fig. 4-9. Here the two individual inductors in each phase are inversely coupled with each other.

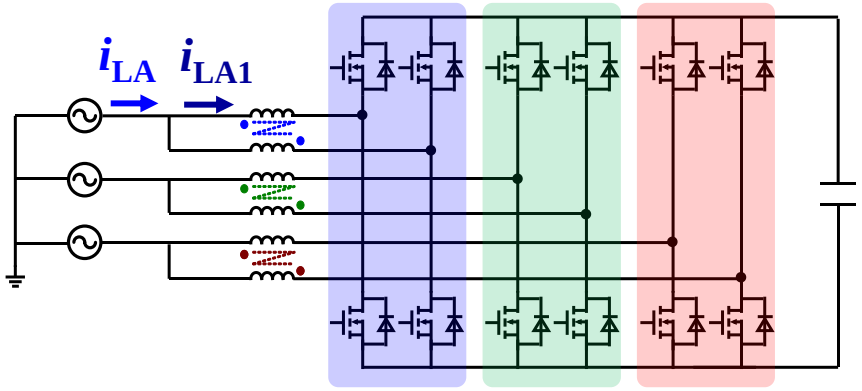


Fig. 4-9. Two-channel interleaved three-phase ac-dc converter with negative coupled inductors.

At the interleaved rectifier mode operation, for the Sequence 2 shown in Fig. 4-8, the inductor current slew rate prior to the zero crossing point is derived as the following Equation (4-1) to show its dependency on the coupling coefficient (α) values. Here V_A, V_C, V_{dc} and L are phase A line-to-neutral voltage, phase C line-to-neutral voltage, dc voltage and the self inductance, respectively.

$$\left|\frac{di_{L(CRM)}}{dt}\right|_{i_{L(CRM)}\to 0^+} = \frac{\left|\frac{1-\alpha}{5+\alpha}V_A + V_C - \frac{2}{5+\alpha}V_{dc}\right|}{L(1+\alpha)} \tag{4-1}$$

The variation of this inductor current slew rate over the first 30 °line-cycle under α = -0.5 is shown in Fig. 4-10, as a comparison with the non-coupled case. Both Equation (4-1) and Fig. 4-10 clearly show that negative coupling is beneficial to the increase in the inductor current slew rate prior to the zero crossing point.

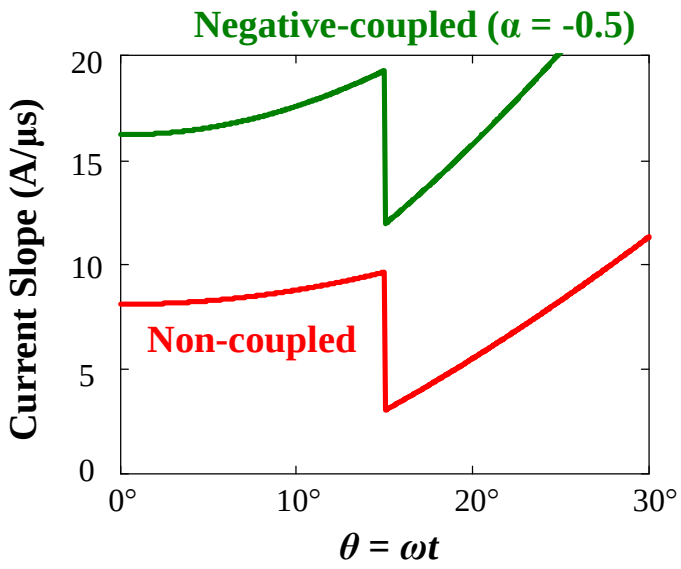


Fig. 4-10. Variation of inductor current slew rate prior to zero crossing over the first 30 °line-cycle interval at interleaved rectifier mode: comparison between negative coupled case (-0.5 coupling coefficient) and non-coupled case.

It should also be noted that the negative coupling effect should be strong enough to totally eliminate the instability (sub-harmonic oscillation). Fig. 4-11 shows the switching-cycle waveforms in two-channel interleaved rectifier mode operation under different coupling coefficient (α) values, including the master-channel individual inductor current (i_{LA1}) and the total inductor current (i_{LA}) in phase A. With α = -0.4, the sub-harmonic oscillation is alleviated but not fully eliminated. With α = -0.5, the sub-harmonic oscillation is totally eliminated.

According to simulations, the maximum coupling coefficient value to achieve stable operation is α = -0.45 under the operating condition in this dissertation (V_{dc} = 800 V, V_{ac} = 277/480 V). This maximum coupling coefficient value is related to the modulation index. Under the condition of realizing stable operation, the lower modulation index allows the coupling coefficient value closer to 0.

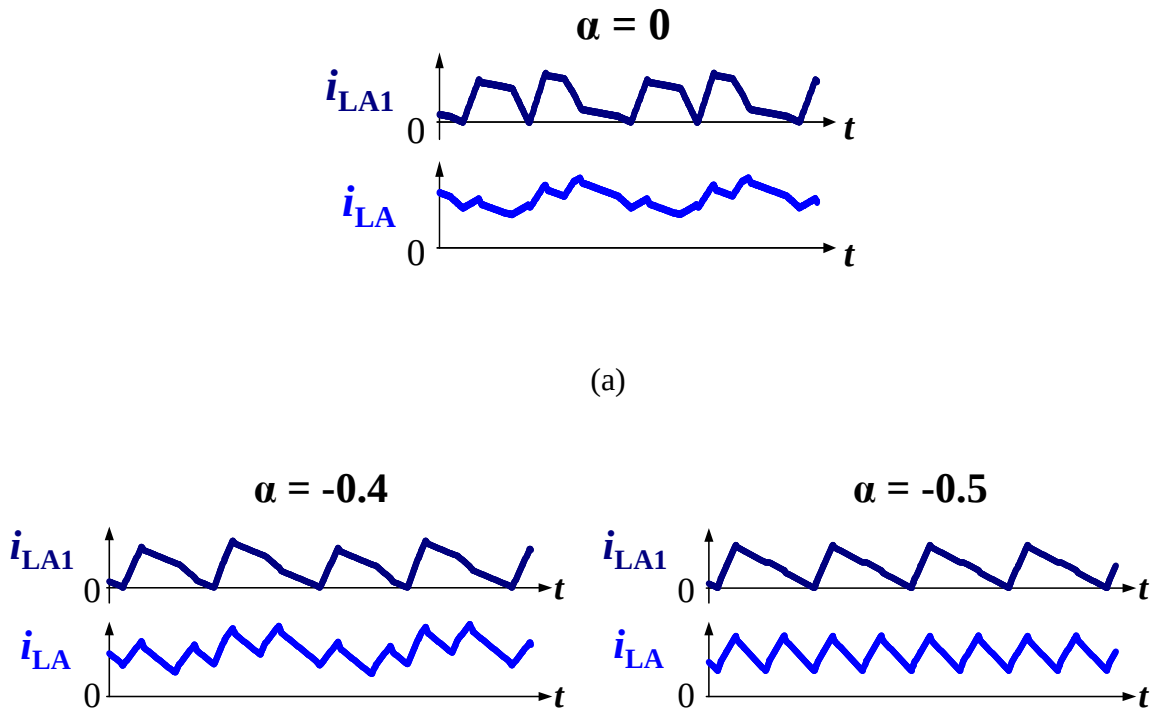


Fig. 4-11. Switching-cycle inductor current waveforms in the rectifier mode operation of two-channel interleaved three-phase converter under different coupling coefficient (α): (a) α = 0; (b) α = -0.4; (c) α = -0.5.

It should be noted that the boundary of the coupling coefficient for avoiding instability may also be changed with different electrical structures of coupled inductors.

4.2.2 Impact of Interleaving and Negative Coupled Inductors on Switching Frequency Variation Range

With two-channel interleaving, the switching frequency variation range becomes slightly wider. With minimum switching frequency at 300 kHz, the peak switching frequency is around 600 kHz, which makes the switching related loss has a little bit increase. According to simulation results based on the operating condition and system parameters shown in Table 2-2, there is around

20% increase in the average switching frequency over a line cycle. This is because the voltage excitation applied on the individual inductor changes and the inductor current slew rate also changes, which makes the switching frequency variation range become slightly wider.

However, after using negative coupled inductors, the switching frequency variation range shrinks over the whole line cycle, which makes up for the drawback brought by the two-channel interleaving in this aspect. Fig. 4-12 shows the switching frequency variation under different coupling coefficient values α. The switching frequency variation range shrinks as the coupling coefficient value goes smaller, which indicates lower switching related loss. It also shows diminishing return in the reduction of switching frequency variation range as $\alpha < -0.5$.

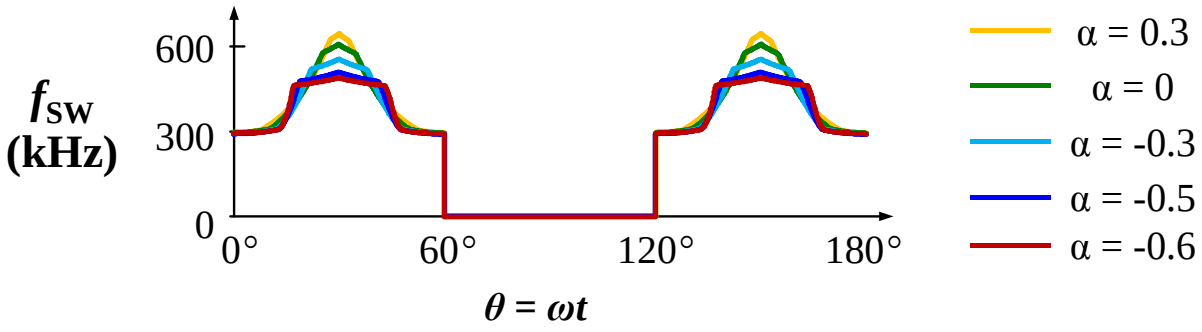
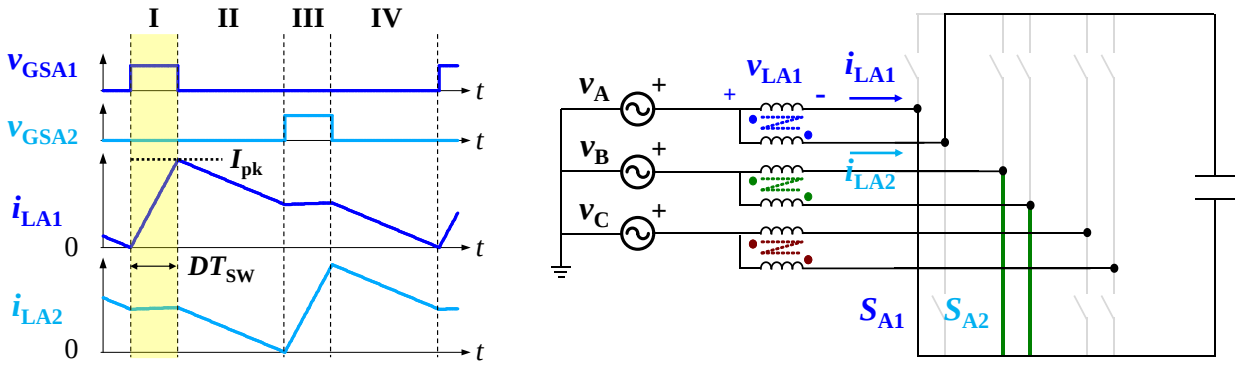


Fig. 4-12. Switching frequency variation under different coupling coefficient values (α).

Based on Fig. 4-12, it is clear that the two-channel interleaving and negative coupled inductors both have impacts on the switching frequency variation range over the whole line cycle. In order to design the self inductance properly and achieve the 300 kHz minimum switching frequency, the dependence of switching frequency variation range on the inductance and on the device parasitic capacitance needs to be quantified. Therefore, similar to Chapter 2, according to Fig. 4-12, the 60 ° operating point is selected as an example first to quantify the system's minimum switching frequency. The same approximation is made here to disconnect the phase at DCM operation (phase

C) from the system. Then the 30 °operating point is selected as an example first to quantify the system's maximum switching frequency.

The same procedure as Chapter 2 is followed here. The parasitic capacitance of all the power semiconductor devices are ignored first in order to illustrate the fundamental concept of the model, and then the parasitic capacitance is included into this model. Taking the two-channel interleaved rectifier mode operation with coupled inductors as an example, the switching cycle waveforms in phase A at this operating point are shown in Fig. 4-13 (a), including the gate signal of the active switch and the inductor current in two channels. According to the switching status of the two active switches, the entire switching cycle is divided into four stages. It is clear that the equivalent inductance of the channel A_1 in the Stage I represents the steady-state inductance, since the inductor current of the channel A_1 increases from the valley to the peak during this stage. Fig. 4-13 (b) shows the circuit diagram of the system operation during the Stage I.



(a) (b)

Fig. 4-13. System operation in phase A at the 60 °operating point without the parasitic capacitance of devices (a) Simulated switching-cycle waveforms; (b) Circuit diagram showing the operation during Stage I (on-time).

Based on the relation between the inductor voltage and the inductor current in the channel A_1, the steady-state inductance L_{SS} is derived as below, where D is the duty cycle; T_{SW} is the switching period; I_{pk} is the peak inductor current in the channel A_1; $V_{LA1(I)}$ is the inductor voltage in the channel A_1 during the Stage I; $L_{A1eq(I)}$ is the equivalent inductance in the channel A_1 during the Stage I.

$$L_{SS} = L_{A1eq(I)} = \frac{DT_{SW}}{I_{pk}} \cdot V_{LA1(I)} \tag{4-2}$$

In this equation, the T_{SW} and the I_{pk} are easy to identify as already shown in the Chapter 2. From Fig. 4-13 (b), the inductor voltage in the channel A_1 during the Stage I is as below.

$$V_{LA1(I)} = \frac{1}{4}V_{dc} + V_A \tag{4-3}$$

Similarly, the inductor voltage in the channel A_1 during the entire switching cycle can be derived and the duty cycle is calculated as below.

$$D = \frac{V_{dc} - 2V_A}{V_{dc}} \tag{4-4}$$

On the other hand, for a coupled inductor, the fundamental relation between the inductor voltages and the inductor currents is shown as below (taking phase A as an example, v_{LA2} is the inductor voltage in the channel A_2; L is the self inductance and $M = \alpha L$ is the mutual inductance).

$$\begin{cases} v_{LA1} = L\dfrac{di_{LA1}}{dt} + M\dfrac{di_{LA2}}{dt} \\ v_{LA2} = L\dfrac{di_{LA2}}{dt} + M\dfrac{di_{LA1}}{dt} \end{cases} \tag{4-5}$$

By eliminating the terms related to i_{LA2}, the equivalent inductance in the channel A_1 is shown in the following equation.

$$v_{LA1} = \frac{L^2 - M^2}{L - M\dfrac{v_{LA2}}{v_{LA1}}} \cdot \frac{di_{LA1}}{dt} \tag{4-6}$$

Based on the inductor voltage in Stage I, the equivalent inductance in the channel A_1 is further expressed as below.

$$L_{A1eq(I)} = \frac{L^2 - M^2}{L + M\dfrac{3V_{dc} - 4V_A}{V_{dc} + 4V_A}} \tag{4-7}$$

By comparing Equations (4-2) and (4-7), and noticing $M = \alpha L$, the dependence of the system's minimum switching frequency on the self inductance and on the coupling coefficient can be derived accordingly.

Then the parasitic capacitance of power semiconductor devices is included and the circuit diagram during the LC resonance stage before the turn-on instant of the active switch is shown in Fig. 4-14.

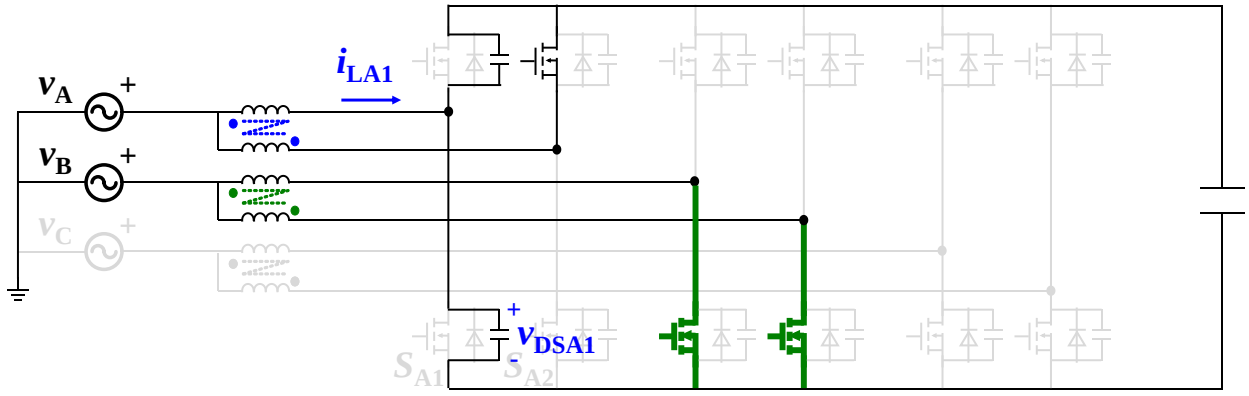


Fig. 4-14. Circuit diagram during the LC resonance stage at the 60 °operating point.

By using the equivalent transformation from a coupled inductor to non-coupled inductors in Fig. 4-15, the above circuit is simplified and the characteristic impedance Z_n of this 2nd-order LC resonance circuit is expressed as below.

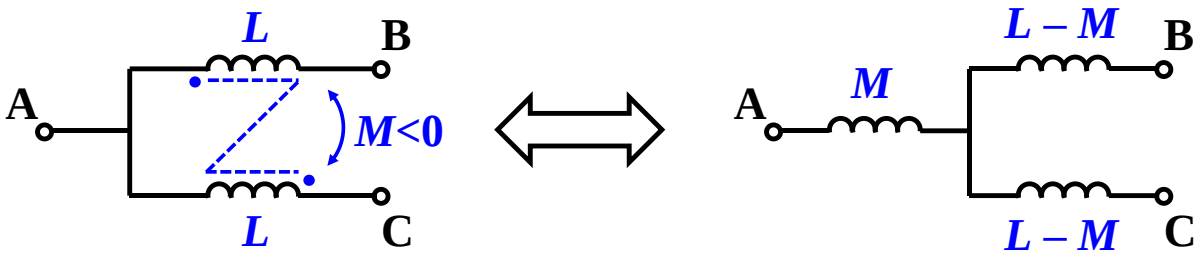


Fig. 4-15. Equivalent transformation from a coupled inductor to non-coupled inductors.

$$Z_n = \sqrt{\frac{4\left(L^2 - M^2\right)}{3L + M} \cdot \frac{1}{C_{OSS}}} \tag{4-8}$$

After that, similar to Equation (2-6), the dependence of system's minimum switching frequency on the self inductance, on the mutual inductance (coupling coefficient), and on the device parasitic capacitance is derived as below.

$$\frac{\frac{1}{4}V_{dc} + V_A}{\frac{L^2 - M^2}{L + M\frac{3V_{dc} - 4V_A}{V_{dc} + 4V_A}}} \cdot \frac{V_{dc} - 2V_A}{V_{dc}} T_{SW} = \sqrt{6} I_{ac} + 4V_A \sqrt{\frac{3L + M}{4\left(L^2 - M^2\right)} C_{OSS}} \tag{4-9}$$

To meet a specific system's minimum switching frequency, the analytical solution of the desired self inductance L with two-channel interleaving and coupled inductors is as below, with given coupling coefficient value α and given device parasitic capacitance C_{OSS}.

$$L = \left[\frac{-V_A\sqrt{\frac{(3+\alpha)C_{OSS}}{1-\alpha^2}} + \sqrt{V_A^2\frac{(3+\alpha)C_{OSS}}{1-\alpha^2} + \sqrt{6}I_{ac}\frac{V_{dc}-2V_A}{V_{dc}T_{SW}^{-1}}\cdot\frac{\frac{1}{4}V_{dc}+V_A}{\frac{1-\alpha^2}{1+\alpha\frac{3V_{dc}-4V_A}{V_{dc}+4V_A}}}}}{\sqrt{6}I_{ac}} \right]^2 \quad (4\text{-}10)$$

Take 800-V dc voltage, 277/480-V ac voltage, 25-kW power, 300-pF device parasitic capacitance as an example. Under three pairs of arbitrarily selected self inductance value and coupling coefficient value, the calculated minimum switching frequency based on Equation (4-10), the simulated minimum switching frequency, and the error between them are shown in Table 4-1. The lower simulated switching frequency compared with the calculated value is because of the margin reserved for the off-time extension. The inverter mode operation shares the same analytical model with the rectifier mode for the design of self inductance with given coupling coefficient value, for achieving a certain minimum switching frequency.

Table 4-1 Verification of Proposed Analytical Model for Interleaved Operation

Self Inductance (μH)	Coupling Coefficient (α)	Calculated Min. Switching Freq. (kHz)	Simulated Min. Switching Freq. (kHz)	Error (Δ/Simulated Value)
5.0	-0.5	356.6	333.7	6.86%
6.0	-0.6	328.1	301.8	8.02%
7.0	-0.7	327.9	294.3	11.42%

Then the dependence of the maximum switching frequency on the inductance value and on the device parasitic capacitance can be quantified in a similar way based on the 30 °operating point. For sake of brevity, only the key equations are shown in the following parts.

At this operating point, the operations in phase A and in phase C are identical at CRM. Similar to Fig. 4-13, when the device parasitic capacitance is ignored, the duty cycle is derived as below.

$$D = \frac{V_{dc} - 3V_A}{V_{dc}} \tag{4-11}$$

Based on Equation (4-5) and Equation (4-6), the equivalent inductance during on-time is expressed as below:

$$L_{A1eq(I)} = \frac{L^2 - M^2}{L + M\dfrac{V_{dc} - 3V_A}{V_{dc} + 3V_A}} \tag{4-12}$$

After considering the device parasitic capacitance, the valley of the switching-cycle inductor current, I_{valley}, is determined by the following equation.

$$-I_{valley}Z_n = 3V_A \tag{4-13}$$

The characteristic impedance Z_n at this operating point is determined by the self inductance, the mutual inductance (coupling coefficient), and the device parasitic capacitance (time-related output capacitance at the dc voltage) as below.

$$Z_n = \sqrt{\frac{3\left(L^2 - M^2\right)}{4L + 2M} \cdot \frac{1}{C_{OSS}}} \tag{4-14}$$

After that, the dependence of system's maximum switching frequency on the self inductance, on the mutual inductance (coupling coefficient), and on the device parasitic capacitance is derived as below.

$$\frac{\dfrac{1}{3}V_{dc} + V_A}{\dfrac{L^2 - M^2}{L + M\dfrac{V_{dc} - 3V_A}{V_{dc} + 3V_A}}} \cdot \frac{V_{dc} - 3V_A}{V_{dc}} T_{SW} = \sqrt{2}I_{ac} + 6V_A\sqrt{\frac{3\left(L^2 - M^2\right)}{4L + 2M} \cdot \frac{1}{C_{OSS}}} \tag{4-15}$$

Under the given dc/ac voltage, system total power, device parasitic capacitance and the selected inductance according to Equation (4-10), the calculated maximum switching frequency based on Equation (4-15) is around 530 kHz, with the coupling coefficient α = -0.5, which has been verified from simulation at the beginning of this part.

Furthermore, by comparing Equation (4-9) with Equation (4-15), the switching frequency variation range is able to be derived as well. It can be concluded that as negative coupling effect goes stronger, the switching frequency variation range becomes narrower.

For the interleaved inverter mode operation, similar conclusion is able to be drawn that the aforementioned method is applicable to derive the switching frequency variation range in order to design the proper inductance.

4.3 Reduction of CM Noise with Balance Technique

4.3.1 Review of Balance Technique in Single-Phase Systems and Three-Phase Non-Interleaved Systems

The basic concept of balance technique is shown as below. Fig. 4-16 shows a Wheatstone bridge structure. Z_1, Z_2, Z_3 and Z_4 are defined as the impedance which are directly connected with one terminal of the voltage excitation v_S shown in Fig. 4-16.

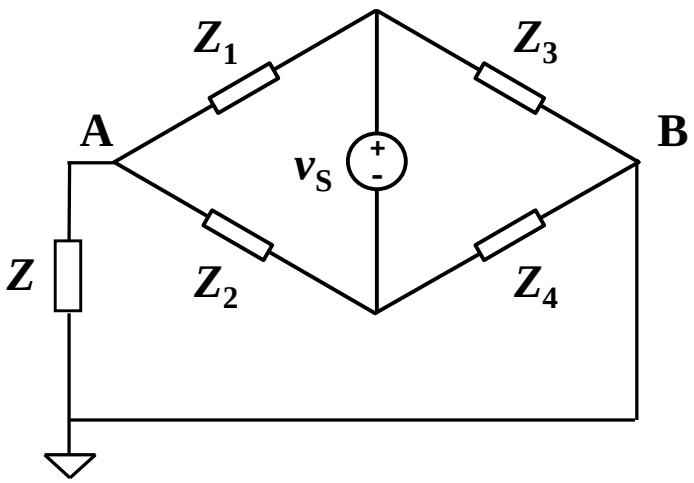


Fig. 4-16. Wheatstone bridge structure for illustrating balance concept.

As long as the impedance meets the relation in Equation (4-16), whatever the voltage excitation v_S is, the voltage potential of point A is always identical to that of point B. Therefore, there is no current flowing through the impedance Z which is directly connected between point A and point B shown in Fig. 4-16.

$$\frac{Z_1}{Z_2} = \frac{Z_3}{Z_4} \tag{4-16}$$

Take the balance technique applied into a two-channel interleaved single-phase totem-pole PFC rectifier in [46] as an example. When measuring the CM EMI noise, a line impedance stabilization network (LISN) is required to be connected between the ac side power source and the converter. Define the parasitic capacitance between the dc bus and the earth as C_b, and the parasitic capacitance between the switch node of each phase leg and the earth as C_d. After treating each high-frequency phase leg as an independent pulsating voltage source, an equivalent CM EMI noise model for the two-channel interleaved single-phase totem-pole PFC rectifier is derived and shown in Fig. 4-17.

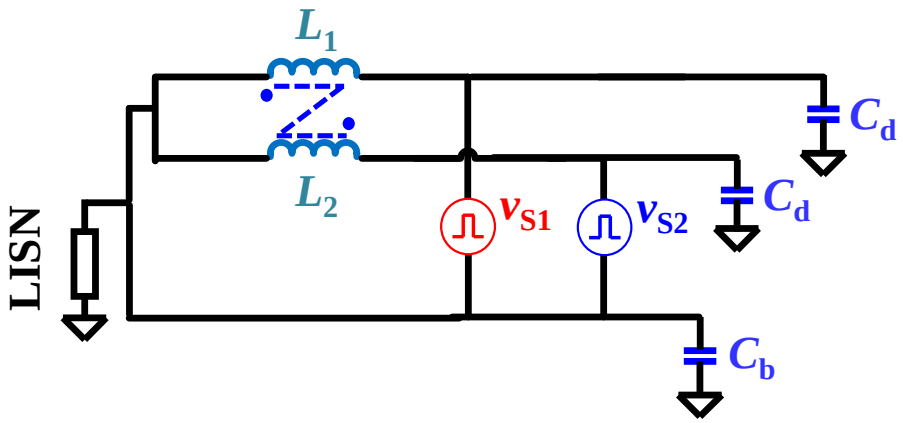


Fig. 4-17. Equivalent CM EMI noise model for original circuit topology.

Due to the equivalent transformation of each phase leg, the system becomes a linear system and then the superposition theory is applicable to analyze the impact of each independent source on the circuit. In this equivalent CM EMI noise model, there are totally two independent sources, v_{S1} and v_{S2}, representing the two phase legs respectively. No matter which source the superposition theory is applied on, the same equivalent sub circuit is derived and shown in Fig. 4-18. It can be seen that the sub circuit is a Wheatstone bridge circuit. According to the previous analysis, if Equation (4-16) is achieved for the four impedance in this structure and therefore it is a balanced Wheatstone bridge structure, there is no current flowing through the LISN no matter what the switching actions are, indicating there is no CM EMI noise. However, this Wheatstone bridge circuit is not a balanced structure since one of the four impedance defined in Fig. 4-16 is zero while the other three are non-zero.

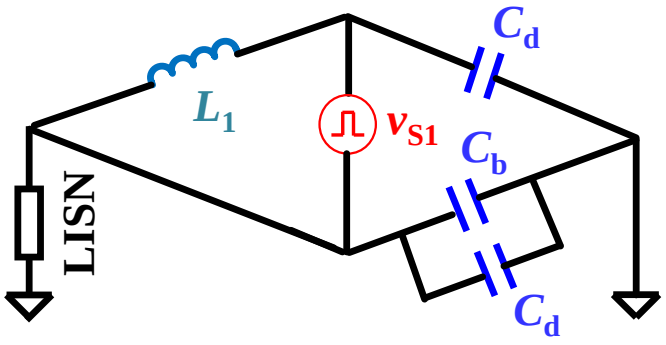


Fig. 4-18. Equivalent sub circuit from Fig. 4-17 for original circuit topology.

In order to achieve a balanced structure for the reduction of CM EMI noise, another two inductors, L_3 and L_4, are added in the return path of this totem-pole PFC rectifier and coupled with the two originally existing inductors, L_1 and L_2. The coupling between L_1 and L_3 is positive coupling and the coupling coefficient is close to unity, and the same for the coupling between L_2 and L_4. The circuit topology with this modification is shown in Fig. 4-19, and the corresponding equivalent sub circuit is shown in Fig. 4-20 for analysis of CM noise. Comparing Fig. 4-20 with Fig. 4-18, it is clear that now none of the four impedance around the voltage excitation is zero, and therefore with proper design, there is opportunity for achieving balanced Wheatstone bridge structure for the reduction of CM EMI noise.

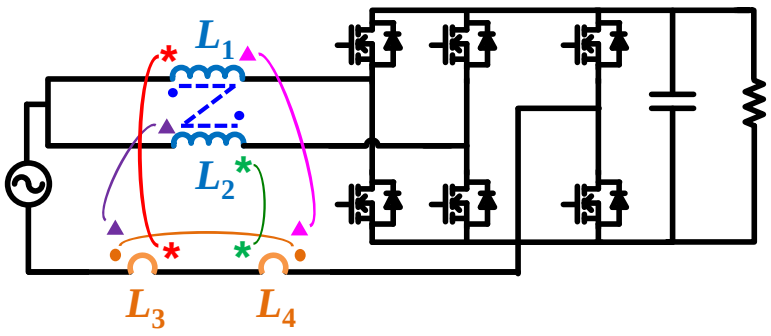


Fig. 4-19. Modified circuit topology with additional inductors L_3 and L_4.

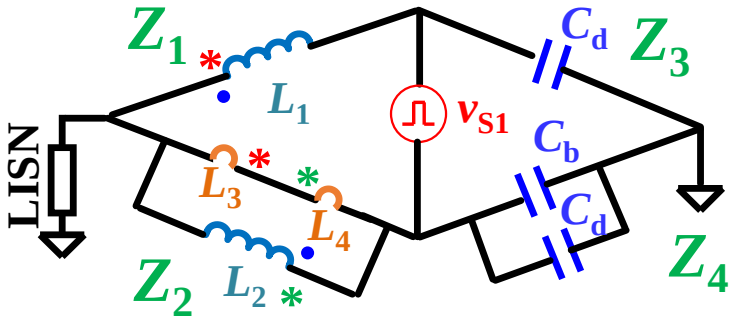


Fig. 4-20. Equivalent sub circuit for modified circuit topology.

The reason of coupling L_1 with L_3, and of coupling L_2 with L_4 is to make the impedance ratio of Z_1 to Z_2 constant over the entire frequency range stated in the EMI standard (150 kHz – 30 MHz). Starting from tens of MHz, the equivalent parallel capacitance (EPC) of the inductors dominates the impedance. Coupling between two inductors makes the parasitic parameters able to be reflected from one to the other, and therefore not only the impedance ratio contributed by the inductance, but also the impedance ratio contributed by the parasitic parameters, maintains at a constant value.

Similar concept is applied into a three-phase non-interleaved neutral-point-clamped (NPC) inverter system in [47]. This system is not a balanced structure from the CM EMI noise point of view, and there is no natural return path in three-phase three-wire systems. Therefore a split capacitor branch is added in the dc side, and a return path is created by connecting the midpoint of the dc split capacitor branch to the neutral point of the three-phase ac filter capacitors. Three inductors are added in this created return path and with proper design, opportunities exist to achieve the balanced structure.

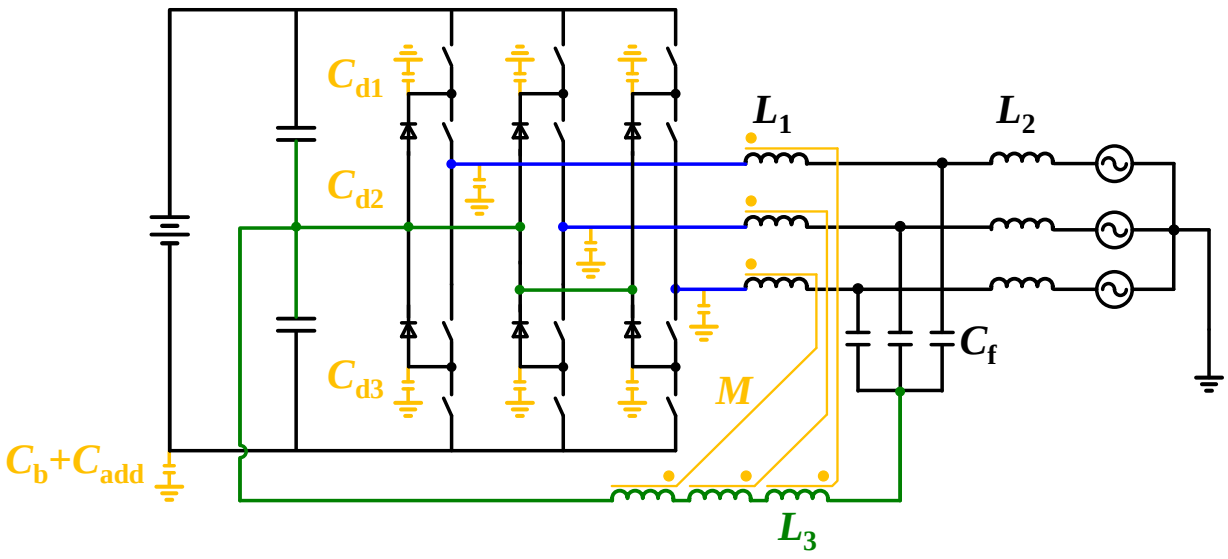


Fig. 4-21. Balance technique applied into a three-phase non-interleaved NPC inverter.

4.3.2 Derivation of CM Noise Model for Balance Technique Applied in Three-Phase Interleaved Rectifiers/Inverters

By referring to [46] and [47], the balance technique is applied into the two-channel interleaved three-phase ac–dc converter. The circuit diagram is shown in Fig. 4-22. Here the two capacitors C_{dcs} are the split capacitor branch added at the dc side. Six inductors are added on the created branch between the midpoint of the dc split capacitor branch and the neutral point of the three-phase ac filter capacitors. Here L_{A1} and L_{A2} are the two originally existing inductors in phase A; L_{A3} and L_{A4} are the two additional inductors in phase A. The same definition is for phase B and phase C.

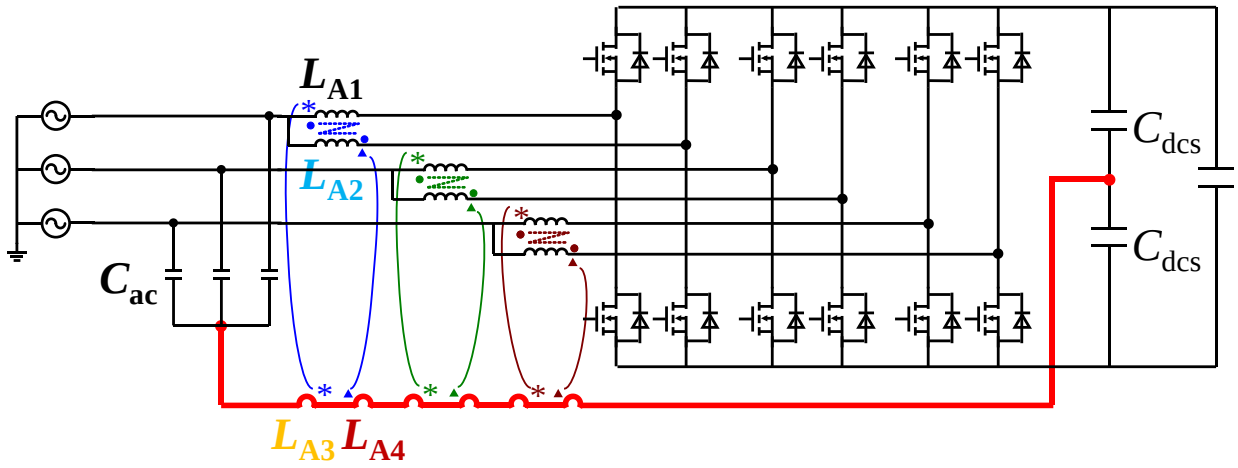


Fig. 4-22. Interleaved three-phase ac–dc converter topology with balance technique applied.

By replacing each phase leg with independent pulsating voltage source, and considering the parasitic capacitance C_b and C_d which are defined in the same way as the previous section, the equivalent CM EMI noise model is shown as Fig. 4-23. Here since the impedance of dc split capacitors and that of the ac filter capacitors are much lower compared with the parasitic capacitance C_b and C_d, and therefore it is assumed that the dc split capacitors and the ac filter capacitors are short circuit in the CM EMI noise model.

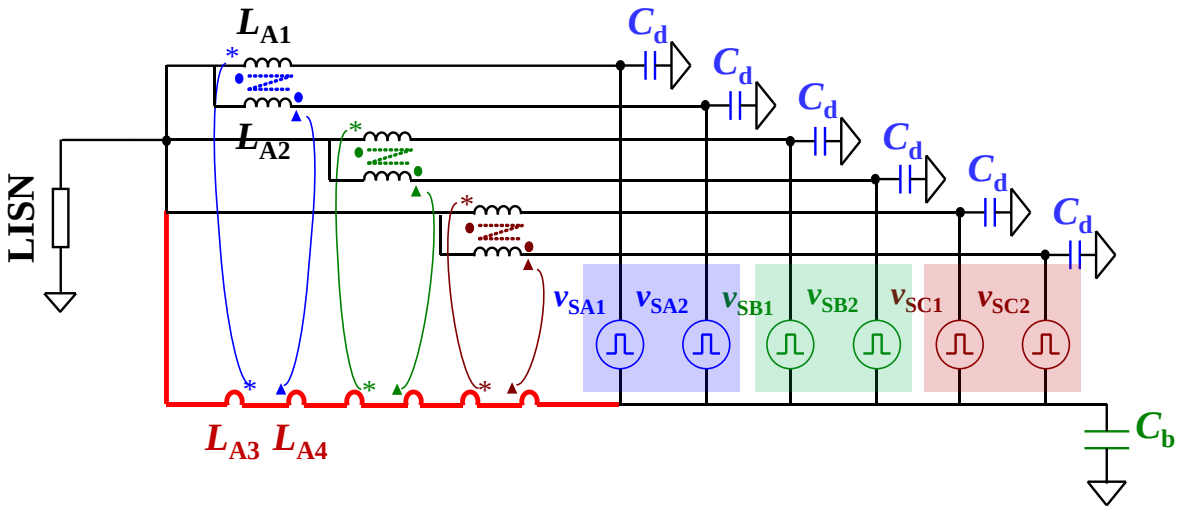


Fig. 4-23. Equivalent CM EMI noise model for the topology in Fig. 4-22.

After the superposition theory is applied on the equivalent CM EMI noise model, its equivalent sub circuit is shown in Fig. 4-24. It can be seen that this is a Wheatstone bridge structure. With the definition of the four impedance Z_1, Z_2, Z_3 and Z_4 shown in Fig. 4-24, as long as Equation (4-16) is satisfied, there is no current flowing through the LISN and therefore there is no CM EMI noise.

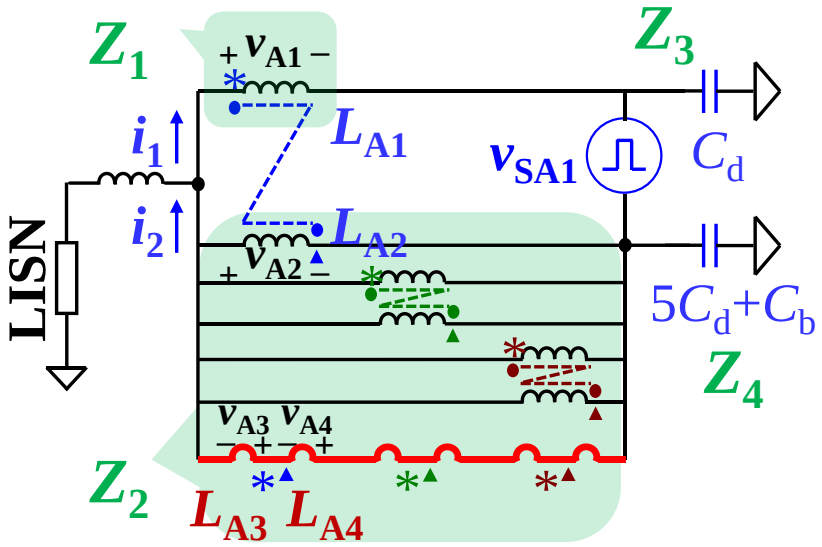


Fig. 4-24. Equivalent sub circuit of the model in Fig. 4-23.

Then the following part is about the derivation of the balance condition to meet Equation (4-16). Define the voltage across the inductor L_{A1}, L_{A2}, L_{A3} and L_{A4} as v_{A1}, v_{A2}, v_{A3} and v_{A4}. The same definition is applied to phase B and phase C. Then define the current flowing through the impedance Z_1 and Z_2 as i_1 and i_2. The reference directions of the defined voltage and current are shown in Fig. 4-24. Assume the positive coupling between L_1 and L_3, between L_2 and L_4 is unity in each phase, and that the parasitic parameters of all inductors are negligible. With N_{12} turns of L_1 and L_2, and N_{34} turns of L_3 and L_4 in each phase, the relation between inductor voltages and the inductor turns number is expressed as the following equations:

$$\frac{v_{A1}}{v_{A3}} = \frac{v_{A2}}{v_{A4}} = ... = \frac{v_{C1}}{v_{C3}} = \frac{v_{C2}}{v_{C4}} = \frac{N_{12}}{N_{34}} \tag{4-17}$$

Also, from Fig. 4-24, it is clear that:

$$v_{A3} + v_{A4} + ... + v_{C3} + v_{C4} = -v_{A2} = -v_{B1} = ... = -v_{C2} \tag{4-18}$$

According to Equations (4-17) and (4-18), the relation between the voltage across impedance Z_1 and the voltage across impedance Z_2 is as below, when v_{SA1} is applied as the excitation:

$$\frac{v_{A1}}{-v_{A2}} = \frac{N_{12} + 5N_{34}}{N_{34}} \tag{4-19}$$

With zero CM EMI noise, the relation between the current flowing through impedance Z_1 and the current flowing through the impedance Z_2 is as below:

$$i_1 = i_2 \tag{4-20}$$

According to Equations (4-19) and (4-20), the impedance ratio between Z_1 and Z_2 is as below, when v_{SA1} is applied as the excitation:

$$\frac{Z_1}{Z_2} = \frac{v_{A1}/i_1}{-v_{A2}/i_2} = \frac{N_{12} + 5N_{34}}{N_{34}} \tag{4-21}$$

On the other hand, the impedance ratio between Z_3 and Z_4 is as below:

$$\frac{Z_3}{Z_4} = \frac{C_b + 5C_d}{C_d} \tag{4-22}$$

Therefore, by comparing Equation (4-21) with Equation (4-22), it is clear that the balance condition for achieving Equation (4-16) is as follows:

$$\frac{N_{12}}{N_{34}} = \frac{C_b}{C_d} \tag{4-23}$$

It should be noted that the inductor turns number N_{12} and N_{34} are only able to be integers. Therefore, some additional capacitors can be added to either C_b or C_d, in order to more freely adjust

the capacitance ratio in Equation (4-23) and make it closer to that inductor turns ratio to achieve better balance effect.

It should also be noted that since the parasitic parameters of the inductors are ignored in this derivation process, only the balance at low frequency range (well below the self-resonance frequency of the inductors, where the impedance is dominated by the inductance rather than other parasitic parameters) can be guaranteed with Equation (4-23). The realization of balance at high frequency range up to 30 MHz relies on the strong coupling between the inductor L_1 and L_3 (between the inductor L_2 and L_4 as well). In spite of that, Equation (4-23) is still the most fundamental condition that needs to be met in order to achieve balance.

Sometimes between the inductor L_1 and L_2, it is preferred to make some turns of L_1 (and also of L_2) interleaved with the other inductor in order to reduce the ac winding loss, which is common in the applications with PCB winding based magnetic components [30][46]. In this case, the coupling between L_1 and L_3 (and that between L_2 and L_4) is not unity any more. Between the inductor L_1 and L_2, define that N_{12}' turns out of the total N_{12} turns of L_1 (and also of L_2) are interleaved with the other inductor. Therefore, with the interleaved inductor windings, the relation between inductor voltages and the inductor turns number is expressed as the following equations, taking phase A as an example:

$$\begin{cases} v_{A1} = v_{A3}\dfrac{N_{12}-N_{12}'}{N_{34}} - v_{A4}\dfrac{N_{12}'}{N_{34}} \\ v_{A2} = v_{A4}\dfrac{N_{12}-N_{12}'}{N_{34}} - v_{A3}\dfrac{N_{12}'}{N_{34}} \end{cases} \tag{4-24}$$

By applying Equation (4-24) to other two phases and summing up all these equations, it is clear that:

$$v_{A1}+v_{A2}+\ldots+v_{C2} = v_{A1}+5v_{A2} = \frac{N_{12}-2N_{12}'}{N_{34}}\left(v_{A3}+v_{A4}+\ldots+v_{C4}\right) = -\frac{N_{12}-2N_{12}'}{N_{34}}v_{A2} \tag{4-25}$$

Therefore, the relation between the voltage across impedance Z_1 and the voltage across impedance Z_2 is as below:

$$\frac{v_{A1}}{-v_{A2}} = \frac{N_{12} - 2N_{12}' + 5N_{34}}{N_{34}} \tag{4-26}$$

Similarly, the final balance condition for achieving Equation (4-16) with interleaved inductor windings is as follows:

$$\frac{N_{12} - 2N_{12}'}{N_{34}} = \frac{C_b}{C_d} \tag{4-27}$$

It can be seen that the Equation (4-27) is able to be reduced to Equation (4-23) when $N_{12}' = 0$, which indicates there are no interleaved inductor windings. Some external capacitors are also able to be added to either C_b or C_d to more freely fine tune the capacitance ratio.

It should also be noted that the analysis about the balance technique is also applicable to the inverter mode operation.

4.4 PCB Winding Coupled Inductor Design and Optimization

4.4.1 Impact of Balance Technique on Switching Frequency Variation Range

With the additional return path and the six inductors for the purpose of balance, the inductor voltage excitations could be different when compared with that shown in the previous sections, which could have impacts on the steady-state inductance and the switching frequency variation range. In order to design the steady-state inductance and achieve the 300 kHz minimum switching frequency, the steady-state inductance and the switching frequency variation range with balance technique applied are to be quantified in this part.

Fig. 4-25 shows the three-phase line-to-neutral voltage as well as the simulated switching frequency variation in phase A over a line cycle, under the same design objective of 300 kHz

minimum switching frequency as in Chapter 2. It is the same as Chapter 2 that the minimum switching frequency occurs at the 0°, 60°, 120° … (multiples of 60°) operating points, as highlighted with red circles in Fig. 4-25, and that the maximum switching frequency occurs at the 30°, 90°, 150° … operating points, as highlighted with blue circles in Fig. 4-25.

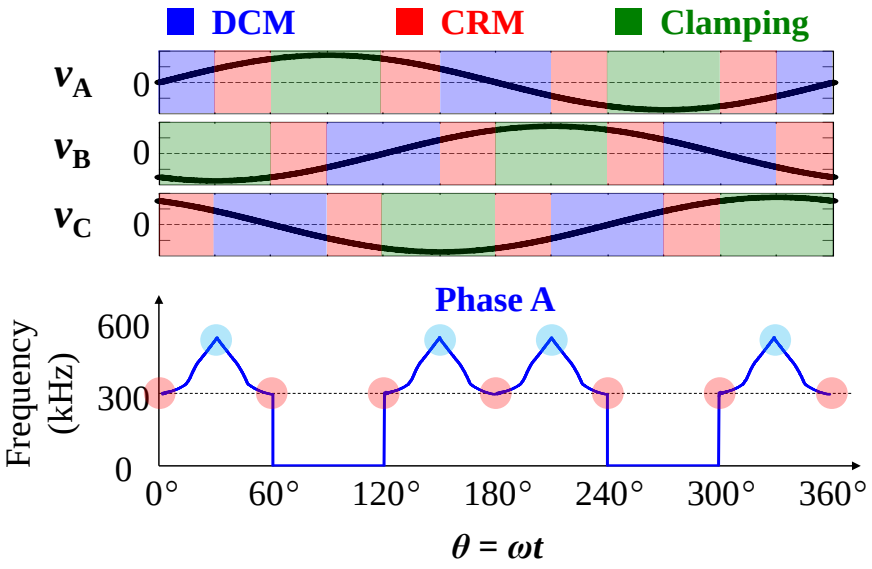
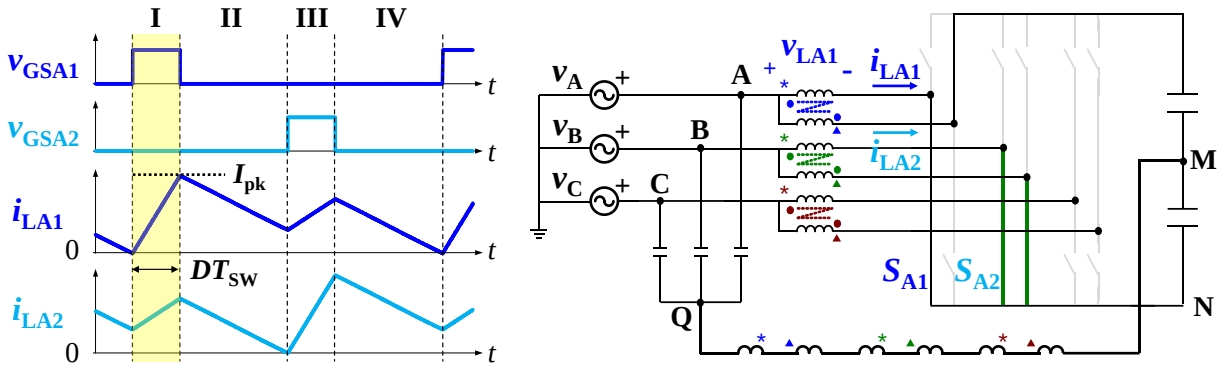


Fig. 4-25. Switching frequency variation in phase A over a line cycle with balance.

Similarly, the 60 °operating point is selected as an example and the dependence of minimum switching frequency on the inductance and on the device parasitic capacitance under this operating point with the balance technique applied. The parasitic capacitance of all the power semiconductor devices is neglected first to simplify the calculation procedure. The impact of the parasitic capacitance is to be included later.

Taking the rectifier mode operation as an example, Fig. 4-26 (a) shows the simulated switching-cycle waveforms in phase A at the 60 °operating point without the parasitic capacitance of devices, including the gate signals of the bottom switches (v_{GSA1}, v_{GSA2}, the active switches) and the inductor currents (i_{LA1}, i_{LA2}) of the two channels. If each switching cycle is divided into four

stages according to switching status, as shown in Fig. 4-26 (a), then the equivalent inductance of the channel A_1 in the Stage I represents the steady-state inductance, since the inductor current of the channel A_1 increases from the valley to the peak during this stage. Fig. 4-26 (b) shows the circuit diagram of the system operation during the Stage I. Here the same approximation is made that phase C is disconnected with the system.



(a) (b)

Fig. 4-26. System operation in phase A at the 60 °operating point without the parasitic capacitance of devices (a) Simulated switching-cycle waveforms; (b) Circuit diagram showing the operation during Stage I (on-time).

Based on the relation between the inductor voltage and the inductor current in the channel A_1, the steady-state inductance L_{SS} is derived as below, where D is the duty cycle; T_{SW} is the switching period; I_{pk} is the peak inductor current in the channel A_1; $V_{LA1(I)}$ is the inductor voltage in the channel A_1 during the Stage I; $L_{A1eq(I)}$ is the equivalent inductance in the channel A_1 during the Stage I.

$$L_{SS} = L_{A1eq(I)} = \frac{DT_{SW}}{I_{pk}} \cdot V_{LA1(I)} \tag{4-28}$$

In this equation, the T_{SW} and the I_{pk} are easy to identify as already shown in the Chapter 2 and Section 4.2. However, the existence of the return path with the six additional inductors makes the

derivation of the duty cycle and of the inductor voltage more complicated when compared with that in Chapter 2 and Section 4.2. Then the following part is mainly about the derivation of these two quantities.

For the duty cycle D in Equation (4-28), the volt-second balance of the inductor in the channel A_1 over one switching cycle indicates the following equation, where the subscript "(X)" is corresponding to the Stage X (hereinafter the same).

$$V_{LA1(I)}D+V_{LA1(II)}(0.5-D)+V_{LA1(III)}D+V_{LA1(IV)}(0.5-D)=0 \tag{4-29}$$

By assuming the voltages across the ac filter capacitors and that across the dc split capacitors are respectively constant during one switching cycle, Equation (4-29) is expanded as below.

$$\begin{aligned}&(V_{AQ}+V_{QM(I)}+V_{MN})D+(V_{AQ}+V_{QM(II)}+V_{MN}-V_{dc})(0.5-D)+\\&(V_{AQ}+V_{QM(III)}+V_{MN}-V_{dc})D+(V_{AQ}+V_{QM(IV)}+V_{MN}-V_{dc})(0.5-D)=0\end{aligned} \tag{4-30}$$

Due to the volt-second balance of the series of inductors between point Q and point M in Fig. 4-26 (b), Equation (4-30) is further simplified as below.

$$(V_{AQ}+V_{MN})D+(V_{AQ}+V_{MN}-V_{dc})(1-D)=0 \tag{4-31}$$

Then by simply applying the KVL, the duty cycle is calculated as below.

$$D=\frac{V_{dc}-V_{AQ}-V_{MN}}{V_{dc}}=\frac{V_{dc}-V_A+V_B}{V_{dc}}\approx\frac{V_{dc}-2V_A}{V_{dc}} \tag{4-32}$$

For the inductor voltage excitation $V_{LA1(I)}$, taking phase A as an example, define the self inductance and the mutual inductance as shown in Fig. 4-27. Then the relations between the inductor voltage and the inductor current in phase A are as below. Similar relations exist for phase B and phase C.

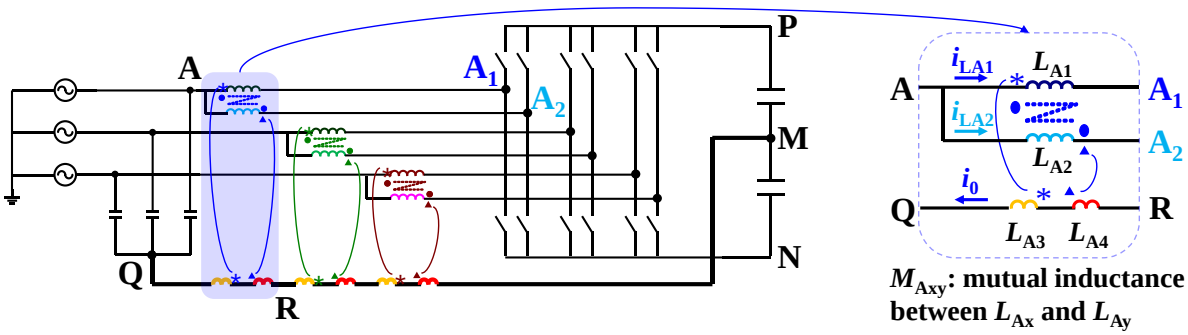


Fig. 4-27. Definition of the self inductance and the mutual inductance in phase A.

$$\begin{cases} V_{AA1} = L_{A1}\dfrac{di_{LA1}}{dt} + M_{A12}\dfrac{di_{LA2}}{dt} + \left(M_{A13} + M_{A14}\right)\dfrac{di_0}{dt} \\ V_{AA2} = L_{A2}\dfrac{di_{LA2}}{dt} + M_{A12}\dfrac{di_{LA1}}{dt} + \left(M_{A23} + M_{A24}\right)\dfrac{di_0}{dt} \\ V_{RQ} = \left(L_{A3} + M_{A34}\right)\dfrac{di_0}{dt} + M_{A13}\dfrac{di_{LA1}}{dt} + M_{A23}\dfrac{di_{LA2}}{dt} \\ \qquad + \left(L_{A4} + M_{A34}\right)\dfrac{di_0}{dt} + M_{A14}\dfrac{di_{LA1}}{dt} + M_{A24}\dfrac{di_{LA2}}{dt} \end{cases} \tag{4-33}$$

Furthermore, the following assumptions of symmetrical inductor structure and therefore of the identical inductance for each channel and among three phases are made.

$$\begin{cases} L_{A1} = L_{A2} = \ldots = L_{C1} = L_{C2} = L_1 \\ L_{A3} = L_{A4} = \ldots = L_{C3} = L_{C4} = L_3 \\ M_{A12} = M_{B12} = M_{C12} = M_{12} \\ M_{A13} = M_{A24} = \ldots = M_{C13} = M_{C24} = M_{13} \\ M_{A14} = M_{A23} = \ldots = M_{C14} = M_{C23} = M_{14} \\ M_{A34} = M_{B34} = M_{C34} = M_{34} \end{cases} \tag{4-34}$$

Based on Equation (4-33) and Equation (4-34), the inductor voltage excitation $V_{\mathrm{LA1(I)}}$ is derived and expressed as below.

$$V_{LA1(I)} = V_A - V_B - \frac{\left(2V_A - 2V_B - V_{dc}\right)\left(M_{13} + M_{14} + 6L_3 + 6M_{34}\right)}{L_1 + M_{12} + 8M_{13} + 8M_{14} + 24L_3 + 24M_{34}} \tag{4-35}$$

Meanwhile, the inductor current slew rate in the channel A_1 in Stage I is derived as below.

$$\frac{di_{LA1}}{dt}_{(I)} = \frac{V_A - V_B + \frac{(6L_3 + 6M_{34} + 2M_{13} + 2M_{14})(V_{dc} - 2V_A + 2V_B)}{L_1 + M_{12} + 8M_{13} + 8M_{14} + 24L_3 + 24M_{34}}}{L_1 + M_{12}} + \frac{M_{12}V_{dc}}{L_1^2 - M_{12}^2} \quad (4\text{-}36)$$

Therefore, to achieve the target minimum switching frequency, the following equation should be satisfied.

$$L_{SS} = L_{A1eq(I)} = \frac{DT_{SW}}{I_{pk}} \cdot V_{LA1(I)} = \frac{V_{LA1(I)}}{\frac{di_{LA1}}{dt}_{(I)}} \Leftrightarrow \frac{di_{LA1}}{dt}_{(I)} = \frac{I_{pk}}{DT_{SW}} \quad (4\text{-}37)$$

It should be noted that in Equations (4-35), (4-36) and (4-37), with the additional return path and six inductors, now the steady-state inductance, inductor voltage and inductor current slew rate are all dependent not only on the inductance L_1 and the mutual inductance M_{12}, but also on other inductance values (the inductor turns numbers N_{12} and N_{34}), which is never seen in the previous analysis. Therefore, for achieving the target minimum switching frequency, with different inductor turns number, even with the same coupling coefficient, the desired self inductance L_1 may be different.

When the parasitic capacitance of the power semiconductor devices is included, the circuit diagram during the LC resonance stage every switching cycle at the 60 °operating point is shown as Fig. 4-28.

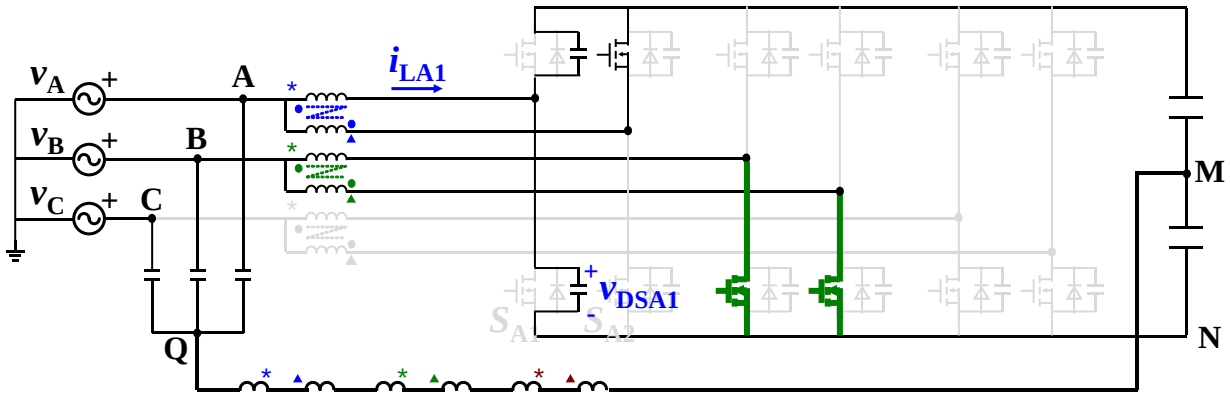


Fig. 4-28. Circuit diagram during the LC resonance stage at the 60 °operating point.

Similar procedure as in Section 4.2.2 will be applied here to derive the characteristic impedance of the 2nd-order LC resonance circuit, in order to calculate the negative inductor current amplitude and modify the inductor current ripple value. It should be noted that the dc side split capacitors and the ac side filter capacitors can be approximated as voltage sources and therefore treated as short circuit when deriving the characteristic impedance, since the capacitance of these capacitors is much larger than the output capacitance of devices,. Therefore, the circuit diagram in Fig. 4-28 is simplified to Fig. 4-29. The four points Q, A, B, and C in Fig. 4-28 is now combined into one point, highlighted in dark red.

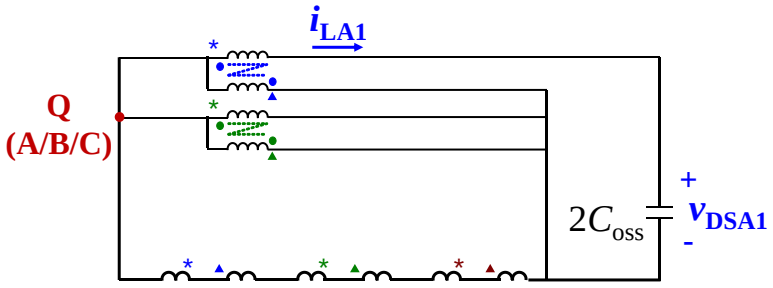


Fig. 4-29. Simplified circuit diagram during the LC resonance stage at the 60 °operating point.

By applying the equivalent transformation similar to Section 4.2.2, the equivalent circuit diagram of Fig. 4-29 is shown as Fig. 4-30 with all the inductors non-coupled.

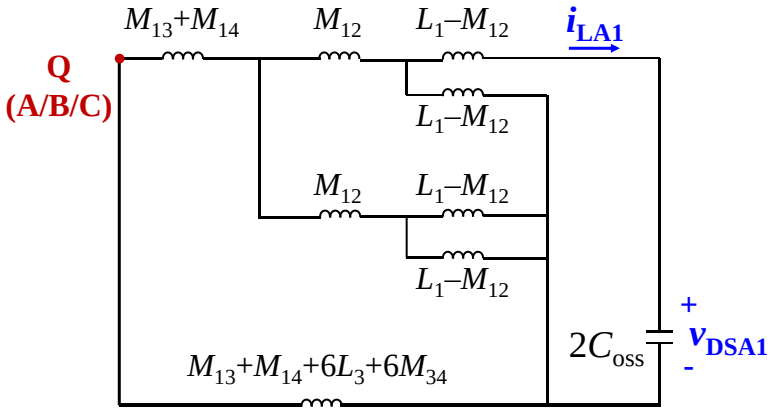


Fig. 4-30. Equivalent circuit diagram during the LC resonance stage at the 60 °operating point.

Therefore, according to Fig. 4-30, the characteristic impedance Z_n of the 2nd-order LC resonance circuit is expressed as below.

$$Z_n = \sqrt{\frac{(L_1 - M_{12})(2L_{EQ} + L_1 + M_{12})}{L_{EQ} + L_1} \cdot \frac{1}{C_{OSS}}} \tag{4-38}$$

In Equation (4-38), the L_{EQ} is expressed as follows.

$$L_{EQ} = \frac{\frac{1}{2}(L_1 + M_{12})[2(M_{13} + M_{14}) + 6(L_3 + M_{34})]}{\frac{1}{2}(L_1 + M_{12}) + 2(M_{13} + M_{14}) + 6(L_3 + M_{34})} \tag{4-39}$$

Therefore, the Equation (4-37) is modified as follows when the parasitic capacitance of devices is considered.

$$\frac{di_{LA1}}{dt}_{(I)} = \frac{1}{DT_{SW}}\left[\sqrt{6}I_{ac} + 2(V_A - V_B)\sqrt{\frac{L_{EQ} + L_1}{(L_1 - M_{12})(2L_{EQ} + L_1 + M_{12})}C_{OSS}}\right] \tag{4-40}$$

By comparing Equation (4-40) with Equation (4-36), the minimum switching frequency is able to be quantified with a given self inductance L_1, a given coupling coefficient (the coupling coefficient between L_1 and L_2, $\alpha_{12} = M_{12}/L_1$, hereinafter the same unless otherwise specified), a given inductor turns number N_{12} and N_{34}, and a given device output capacitance C_{OSS}. On the other hand, the self inductance L_1 can be calculated with a target minimum switching frequency, a given coupling coefficient value α_{12}, a given inductor turns number N_{12} and N_{34}, and a given device output capacitance C_{OSS}.

Then the dependence of the maximum switching frequency on the inductance value and on the device parasitic capacitance can be quantified in a similar way based on the 30 °operating point. For sake of brevity, only the key equations are shown in the following parts.

At this operating point, the operations in phase A and in phase C are identical at CRM. Similar to Fig. 4-26, when the device parasitic capacitance is ignored, the duty cycle is derived as below.

$$D = \frac{V_{dc} - 3V_A}{V_{dc}} \tag{4-41}$$

Meanwhile, the inductor current slew rate in the channel A_1 in Stage I is derived as below.

$$\frac{di_{LA1}}{dt}_{(I)} = \frac{V_A - V_B + \frac{(6L_3 + 6M_{34} + 2M_{13} + 2M_{14})(2V_{dc} + 6V_B)}{L_1 + M_{12} + 12M_{13} + 12M_{14} + 36L_3 + 36M_{34}}}{L_1 + M_{12}} + \frac{M_{12}V_{dc}}{L_1^2 - M_{12}^2} \tag{4-42}$$

After considering the device parasitic capacitance, similar to the derivation process shown in Fig. 4-28, Fig. 4-29, and Fig. 4-30, the characteristic impedance Z_n at this operating point is expressed as below.

$$Z_n = \sqrt{\frac{\left(\frac{1}{2}L_1 - \frac{1}{2}M_{12}\right)\left(2L_{EQ} + \frac{1}{2}L_1 + \frac{1}{2}M_{12}\right)}{L_{EQ} + \frac{1}{2}L_1} \cdot \frac{1}{C_{OSS}}} \tag{4-43}$$

In Equation (4-43), the L_{EQ} has the same definition as expressed in Equation (4-39).

After that, an equation similar to Equation (4-40) but applicable to the 30 °operating point is derived as follows.

$$\frac{di_{LA1}}{dt}_{(I)} = \frac{1}{DT_{SW}}\left[\sqrt{2}I_{ac} + 6V_A\sqrt{\frac{L_{EQ} + \frac{1}{2}L_1}{\left(\frac{1}{2}L_1 - \frac{1}{2}M_{12}\right)\left(2L_{EQ} + \frac{1}{2}L_1 + \frac{1}{2}M_{12}\right)}C_{OSS}}\right] \tag{4-44}$$

Then by comparing Equation (4-44) with Equation (4-42), the maximum switching frequency is able to be quantified with a given self inductance L_1, a given coupling coefficient α_{12}, a given inductor turns number N_{12} and N_{34}, and a given device output capacitance C_{OSS}.

Similarly, take 800-V dc voltage, 277/480-V ac voltage, 25-kW power, 300-pF device parasitic capacitance as an example. Assume the unity coupling between L_1 and L_3, between L_2 and L_4. Under three groups of arbitrarily selected turns number N_{12} and N_{34}, self inductance value

and coupling coefficient value α_{12}, the calculated minimum/maximum switching frequency based on Equations (4-40) and (4-44), the simulated minimum/maximum switching frequency, and the error between them are shown in Table 4-2. The small error indicates the high accuracy of the model.

Table 4-2 Verification of Proposed Analytical Model for Interleaved Operation with Balance

Turns Number N_{12} / N_{34}	Self Inductance (μH)	Coupling Coefficient (α_{12})	Calculated Min. / Max. Switching Freq. (kHz)	Simulated Min. / Max. Switching Freq. (kHz)	Error (Δ/Simulated Value)
4/1	5.0	-0.3	360.9/705.4	347.2/707.7	3.95%/0.32%
4/1	6.0	-0.4	314.8/599.0	301.6/593.1	4.38%/0.99%
4/1	7.0	-0.5	289.6/531.0	282.8/523.9	2.40%/1.36%

For the interleaved inverter mode operation, similar conclusion is able to be drawn that the aforementioned method is applicable to derive the switching frequency variation range in order to design the proper inductance.

4.4.2 PCB Winding Coupled Inductor Design and Optimization Process

According to [58], in order to make the balance technique effective in the entire EMI frequency range (150 kHz – 30 MHz), it is important to make the coupling as close to unity as possible between the inductor L_1 and the inductor L_3, and also between the inductor L_2 and the inductor L_4. The same is for phase B and phase C. Therefore, for each phase, the proposed PCB winding coupled inductor structure is shown in Fig. 4-31. The turns number of inductor L_1 and L_2, N_{12}, is preferred to be small for easier implementation with 4- or 6-layer PCB, and also avoiding the significant amount of winding loss. The turns number of inductor L_3 and L_4, N_{34}, is preferred to be 1 considering to make the ground loop resonance frequency as high as possible which is introduced in [45] and [58].

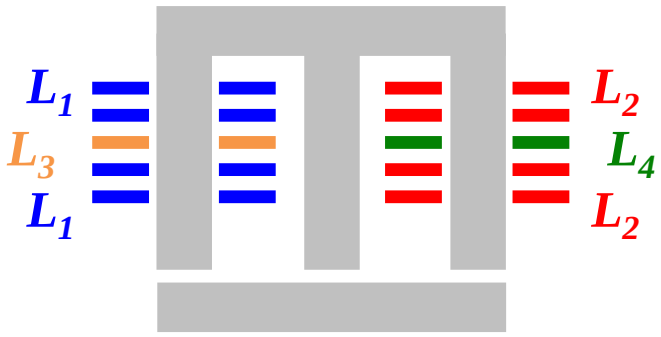


Fig. 4-31. PCB winding coupled inductor structure for each phase.

The first step of PCB winding coupled inductor design is to identify the required values of self inductance and coupling coefficient between inductor L_1 and inductor L_2, in order to achieve a certain minimum switching frequency over a line cycle. Based on Equation (4-40) and the winding structure in Fig. 4-31, Fig. 4-32 shows the calculated result of required self inductance value under different coupling coefficient values between inductor L_1 and inductor L_2 to achieve a minimum switching frequency of 300 kHz over a line cycle. For the coupled inductor structure shown in Fig. 4-31, it is very hard to design a coupling coefficient smaller than -0.5 considering the practically existing leakage flux in the air. On the other hand, for this coupled inductor structures with L_3 and L_4 for balance shown in Fig. 4-31, the boundary of coupling coefficient to avoid instability in rectifier mode becomes much higher than -0.5, due to the increase in the inductor current slew rate before zero crossing compared with what is presented in Section 4.2. Therefore, the coupling coefficient is selected as -0.3 as an example to illustrate the subsequent design process, and the corresponding required self inductance value is 6.1 μH. It has been verified with simulations that instability does not exist with this coupling coefficient.

The second step is to calculate the required air gap reluctance of the coupled inductor to achieve the aforementioned self inductance and coupling coefficient. For the inductor structure shown in Fig. 4-31, define the air gap reluctance of the outer leg and that of the center leg as R_{g1}

and R_{g2}, respectively, then the magnetic circuit of the coupled inductor is shown in Fig. 4-33. Define i_{L1} and i_{L2} as the current in L_1 and L_2, respectively; define i_0 as the current in L_3 and L_4. The flux in each leg is defined as Φ_1, Φ_2 and Φ_3, respectively.

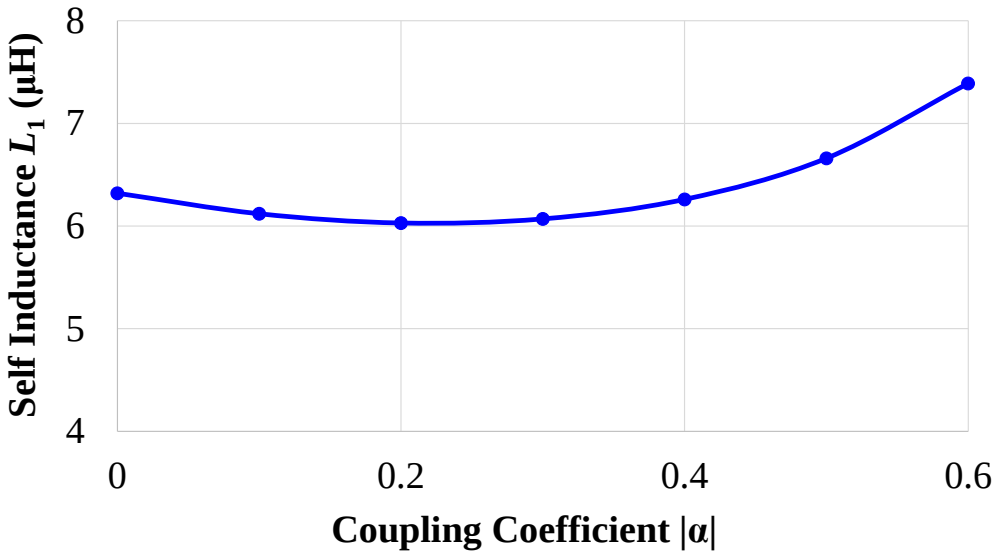


Fig. 4-32. The required value of self inductance under different coupling coefficient values to achieve 300-kHz minimum switching frequency.

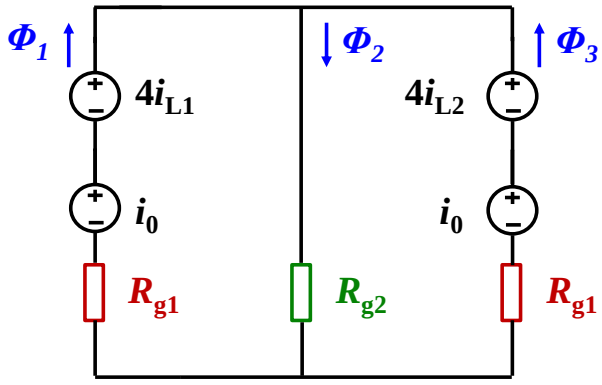


Fig. 4-33. Magnetic circuit of the PCB winding coupled inductor structure in Fig. 4-31.

Based on the magnetic circuit in Fig. 4-33 and the definition of self inductance and coupling coefficient, the following Equation (4-45) are derived in order to solve the required air gap reluctance to achieve 6.1-μH self inductance and -0.3 coupling coefficient. Here in this example,

the turns number of each inductor L_1 and L_2 is 4 (N_{12} = 4); the turns number of each inductor L_3 and L_4 is 1 (N_{34} = 1).

$$\begin{cases} L_1 = \dfrac{\Phi_1}{i_{L1}}\Big|_{i_{L2}=i_0=0} = \dfrac{16}{R_{g1} + \dfrac{R_{g1}R_{g2}}{R_{g1}+R_{g2}}} = 6.1\mu H \\ |\alpha_{12}| = \dfrac{|M_{12}|}{L_1}\Big|_{i_{L2}=i_0=0} = \dfrac{R_{g2}}{R_{g1}+R_{g2}} = 0.3 \end{cases} \tag{4-45}$$

The solved reluctance values R_{g1} and R_{g2} is as below:

$$\begin{cases} R_{g1} = 2.02\times10^6\, H^{-1} \\ R_{g2} = 0.86\times10^6\, H^{-1} \end{cases} \tag{4-46}$$

The third step is to calculate the flux in each leg according to the calculated reluctance values and the inductor currents, which is as below:

$$\begin{cases} \Phi_1 = \dfrac{4i_{L1}+i_0}{R_{g1}+\dfrac{R_{g1}R_{g2}}{R_{g1}+R_{g2}}} - \dfrac{4i_{L2}+i_0}{R_{g1}+\dfrac{R_{g1}R_{g2}}{R_{g1}+R_{g2}}} \cdot \dfrac{R_{g2}}{R_{g1}+R_{g2}} \\ \Phi_2 = \dfrac{4i_{L1}+4i_{L2}+2i_0}{R_{g1}+\dfrac{R_{g1}R_{g2}}{R_{g1}+R_{g2}}} \cdot \dfrac{R_{g1}}{R_{g1}+R_{g2}} \\ \Phi_3 = \dfrac{4i_{L2}+i_0}{R_{g1}+\dfrac{R_{g1}R_{g2}}{R_{g1}+R_{g2}}} - \dfrac{4i_{L1}+i_0}{R_{g1}+\dfrac{R_{g1}R_{g2}}{R_{g1}+R_{g2}}} \cdot \dfrac{R_{g2}}{R_{g1}+R_{g2}} \end{cases} \tag{4-47}$$

The calculated half-line-cycle flux waveforms in the left leg and the center leg of the coupled inductor is shown in Fig. 4-34. Here a zoomed in switching-cycle waveforms around the 60° operating point is also shown here. It can be seen that under this example condition (L_1 = 6.1 μH, α = -0.3, N_{12} = 4, N_{34} = 1), the maximum flux in the left leg is around 60 μWb, while the maximum flux in the center leg is around 67 μWb. It should be noted that the flux in the right leg has 180°

phase shift compared with that in the left leg from the switching cycle point of view, and therefore, the maximum flux in the right leg is the same as that in the left leg.

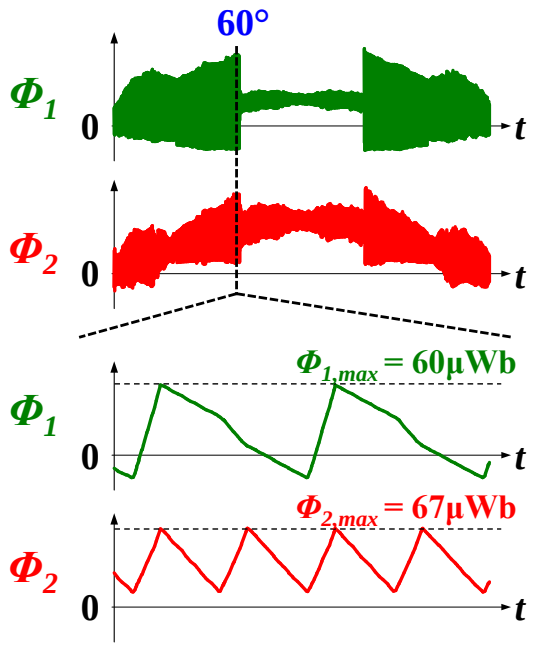


Fig. 4-34. The calculated half-line-cycle and zoomed in switching-cycle flux in the left leg and the center leg of the inductor structure in Fig. 4-31.

The fourth step is to identify the independent design variables for the PCB winding coupled inductor. The independent design variables are selected so that as long as all these independent design variables are given, the dimension of the PCB winding coupled inductor is determined. Fig. 4-35 shows the cross section view of the PCB winding coupled inductor. The circular cross section shape in the outer core leg is for minimizing the winding length under a specific cross section area; the curved cross section shape in the center leg is for fully utilizing the space. Two independent design variables are selected: the outer core leg cross section radius *r*, and the winding width *a*. For simplicity, the cross section area of the outer core leg and that of the center core leg is designed to be identical, considering the similar level of the maximum flux in these two legs over a line cycle as shown in Fig. 4-34. The air gap length of the outer core legs and that of the center core

leg become two dependent variables to be adjusted in order to realize the desired self inductance and coupling coefficient, at each given pair of (r, a). Therefore, it is clear that for each pair of the two independent variables r and a, the cross section area and the air gap length of each core leg are able determined for realizing the desired self inductance and coupling coefficient. In other words, as long as the two independent variables are given, the dimension of the inductor is determined.

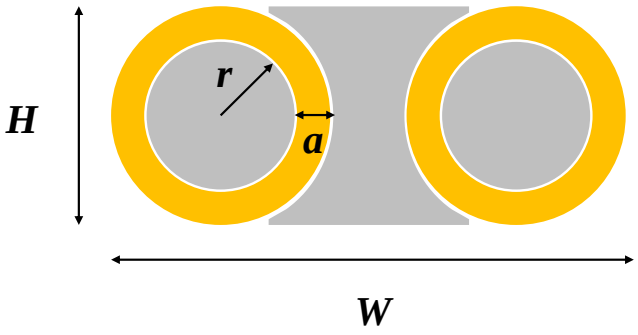


Fig. 4-35. Cross section view of the PCB winding coupled inductor.

The fifth step is to calculate the inductor footprint and the inductor loss. The inductor footprint is calculated according to Fig. 4-35, which is as below:

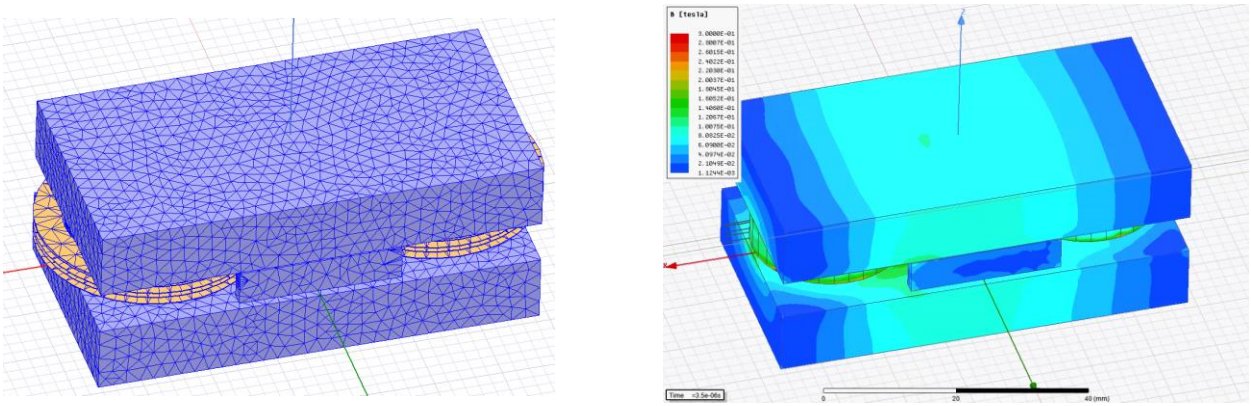
$$FP(r,a) = H \cdot W = 2(r+a)\left[4(r+a) + \frac{\pi r^2 - (4-\pi)(r+a)^2}{2(r+a)}\right] \tag{4-48}$$

The inductor loss is calculated by averaging the inductor loss at selected 13 evenly distributed operating points over a half line cycle (0°, 15°, 30°, …, 180°). The inductor loss can be more accurately calculated with more selected operating points for averaging but it will make the entire process more time-consuming.

The winding loss and the core loss are calculated separately and then summed up to be the inductor loss. Both the winding loss and the core loss are calculated based on finite element analysis (FEA) simulations using the Ansys Maxwell software. The switching-cycle inductor

current waveforms from SIMetrix/SIMPLIS circuit simulation at each operating point is used as the excitation for the FEA simulations.

In the FEA simulations, both the PCB windings and the magnetic cores are divided into many sufficiently small cells (meshes) as shown in Fig. 4-36 (a), so that the current density and the flux density inside each cell are approximately uniformly distributed, respectively. Take the flux density distribution in magnetic cores as an example. With the switching-cycle inductor current waveforms as the excitation, the time-domain flux density distribution for each cell of the magnetic cores is obtained through the transient simulation in Ansys Maxwell. Fig. 4-36 (b) shows an example flux density distribution of magnetic cores at a specific instant in the switching cycle. Similarly, the selection of the number of the small cells is based on the tradeoff between the simulation accuracy and simulation time consumption.



(a) (b)

Fig. 4-36. An example of finite element analysis (FEA) simulations in Ansys Maxwell: (a) meshes in the PCB windings and the magnetic cores; (b) simulated flux density distribution in the magnetic cores at a certain instant.

With the time-domain flux density information for each cell of magnetic cores, the core loss at each operating point is calculated based on the following equation:

$$P_{core}(r,a)=\sum \Delta V_{core}\cdot\frac{1}{T_{sw}}\int_0^{T_{sw}} P_v(r,a,t)dt \tag{4-49}$$

Here ΔV_{core} is the volume of each cell of the magnetic cores; the core loss density P_{v} is calculated based on the equivalent elliptical loop (EEL) model developed in [59] for each cell of magnetic cores based on the following equation:

$$P_v(t)=\left|\frac{C_m}{(2\pi)^{\alpha}\frac{2}{\pi}\int_0^{\frac{\pi}{2}}\cos^{\beta}(\theta)d\theta}\times\left(B_m\sqrt{1-\left[\frac{B(t)}{B_m}\right]^2}\right)^{\beta-\alpha}\right|\left|\frac{dB(t)}{dt}\right|^{\alpha} \tag{4-50}$$

In Equation (4-50) the C_{m}, α and β are empirical parameters obtained from experimental measurement under sinusoidal excitation applied on the core material under test, to calculate the core loss density in the following Steinmetz Equation [60]:

$$P_v=C_m f^{\alpha}B_m^{\beta} \tag{4-51}$$

B_{m} is one half of the peak-to-peak value of time domain flux density in each switching cycle. It should be noted that the $B(t)$ is only the ac part of the time domain flux density, which means $B(t)$ comes from the original flux density after removing the switching-cycle dc bias.

The impact of dc bias in the time domain flux density on core loss density is considered by multiplying the core loss density from Equation (4-50) by a coefficient $f(H_{\text{dc}})$ [61]. This coefficient is equal to the ratio of measured core loss density with dc bias and measured core loss density without dc bias. Both measurements are under sinusoidal excitation. It should be noted that this coefficient is dependent on the ac flux magnitude and on the switching frequency. The final expression to calculate the averaged core loss density per switching cycle is shown as below.

$$\overline{P_v}=f(H_{dc})\cdot\frac{1}{T_{SW}}\int_0^{T_{SW}} P_v(t)dt \tag{4-52}$$

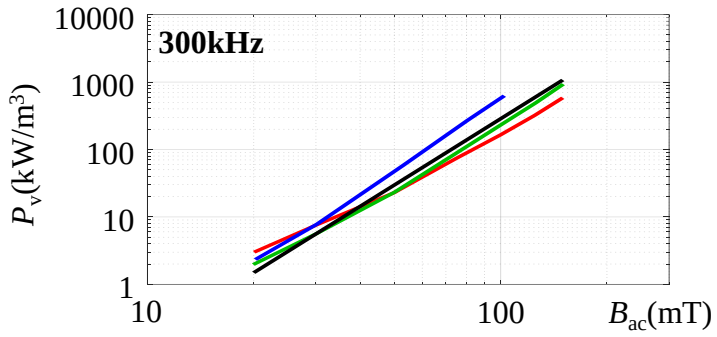
As for the winding loss, it is calculated based on simulated current density and the Ohm's Law for each cell of the PCB windings.

The last step is to sweep all the independent design variables of the PCB winding coupled inductors in order to find the optimal design point, considering the tradeoff among inductor footprint, inductor winding loss and inductor core loss. The detailed optimization process is shown in as follows.

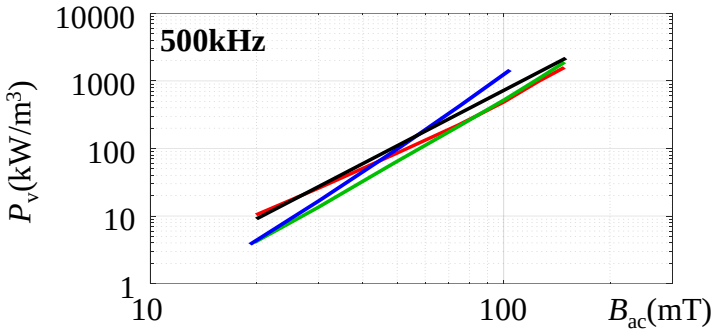
Before the optimization process, the core material needs to be selected. According to the core loss density test results shown in Fig. 4-37 for different core materials under several different frequency in interested switching frequency range, the ML95S from Hitachi Metal is selected for designing the PCB winding coupled inductor. The horizontal axis B_{ac} is half of the peak-to-peak amplitude of the sinusoidal flux density in the core.

The core loss density is also tested under different dc bias conditions in order to determine the aforementioned coefficient $f(H_{dc})$ in Equation (4-52), as shown in Fig. 4-38. The transformation between H_{dc} and B_{dc} can be realized based on the B-H curve of ML95S [62] shown in Fig. 4-39. Therefore, for any given time-domain switching-cycle flux density distribution in the cell of the magnetic cores, the switching frequency, ac flux density magnitude, and dc bias of flux density can be easily identified. Then the core loss density can be calculated simply based on Equation (4-52).

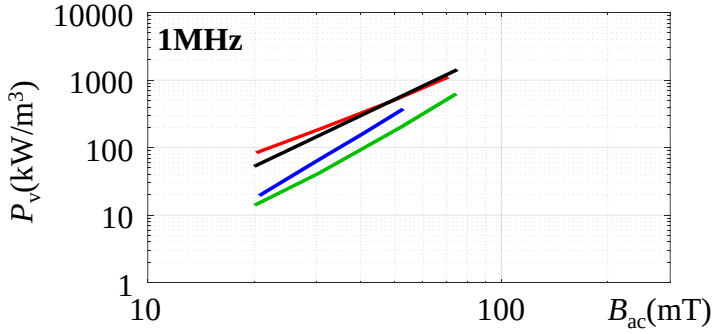
Based on the *B-H* curve of ML95S shown in Fig. 4-39, in order to avoid the core saturation with sufficient design margin, the peak flux density in the core is limited to be below 200 mT. To achieve the coupling coefficient of -0.3, according to the calculated flux shown in Fig. 4-34, as long as the outer leg radius r is designed to be larger than 10.3 mm, the peak flux density in the core is below 200 mT. Therefore, 10.3 mm is the lower limit of the outer leg core radius r.



(a)

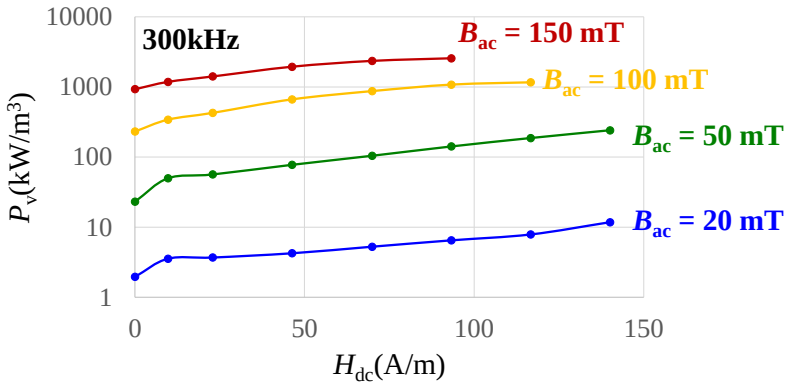


(b)

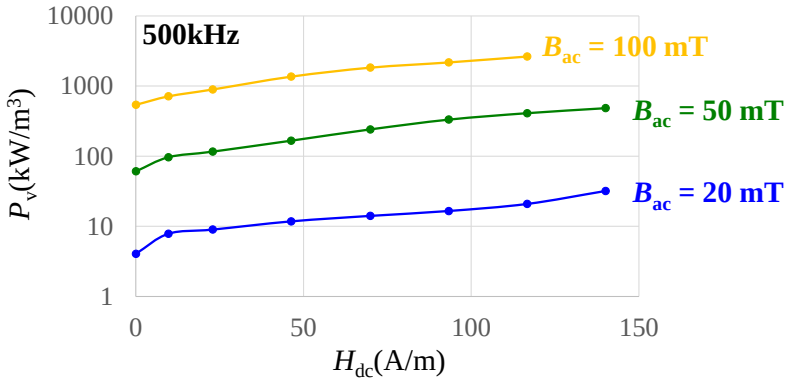


(c)

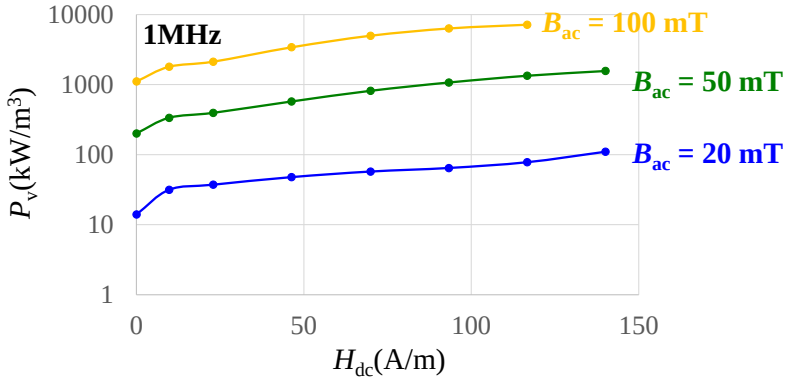
Fig. 4-37. Core loss density tested results under sinusoidal excitations with different core materials under (a) 300 kHz; (b) 500 kHz; (c) 1 MHz. (red: ML27D, Hitachi Metal; black: 3F36, Ferroxcube; blue: DMR51, DMEGC; green: ML95S, Hitachi Metal)



(a)



(b)



(c)

Fig. 4-38. Core loss density tested results under sinusoidal excitations with different ac flux density magnitude and with different dc bias values at (a) 300 kHz; (b) 500 kHz; (c) 1 MHz.

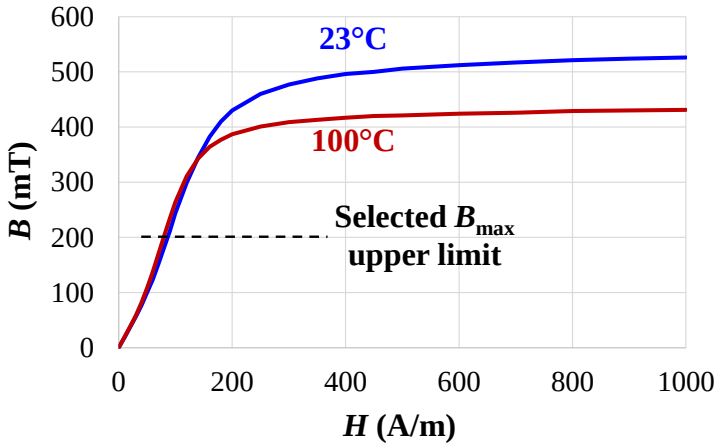
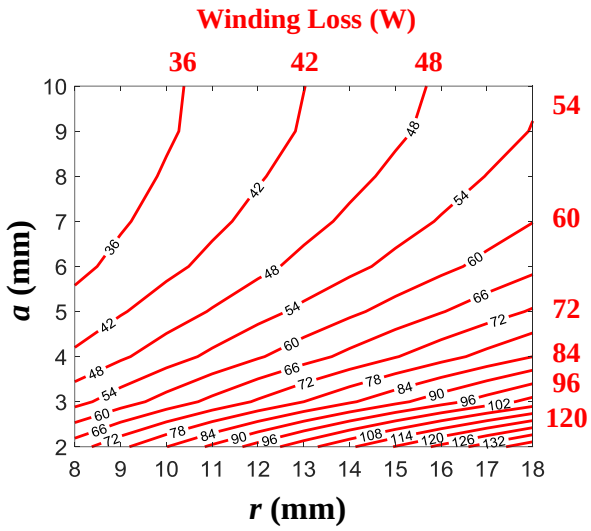


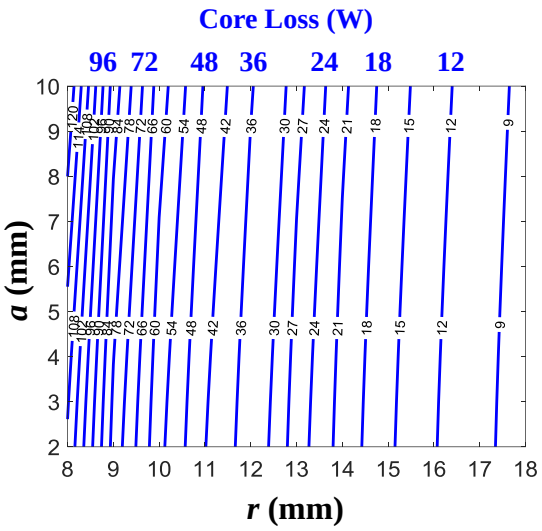
Fig. 4-39. *B*-*H* curve of ML95S.

The optimization process of the design of the PCB winding coupled inductors are shown as following parts, which is similar to the literature [63] – [67]. With a fixed inductor turns number N_{12} = 4, N_{34} = 1, sweep the inductor outer leg core radius *r* and the winding width *a*. With each pair of (*r*, *a*), the inductor winding loss, core loss and footprint are calculated and the contour is shown in Fig. 4-40. The winding loss and the core loss are shown in Fig. 4-40 (a) and (b), respectively. The inductor total loss and the inductor footprint are overlapped and shown in Fig. 4-40 (c). It can be seen that there is a minimum total inductor loss point with each given footprint, which is marked with green dots and connected by a green line in Fig. 4-40 (c). All these points on this green line are the optimal design points for each given inductor footprint.

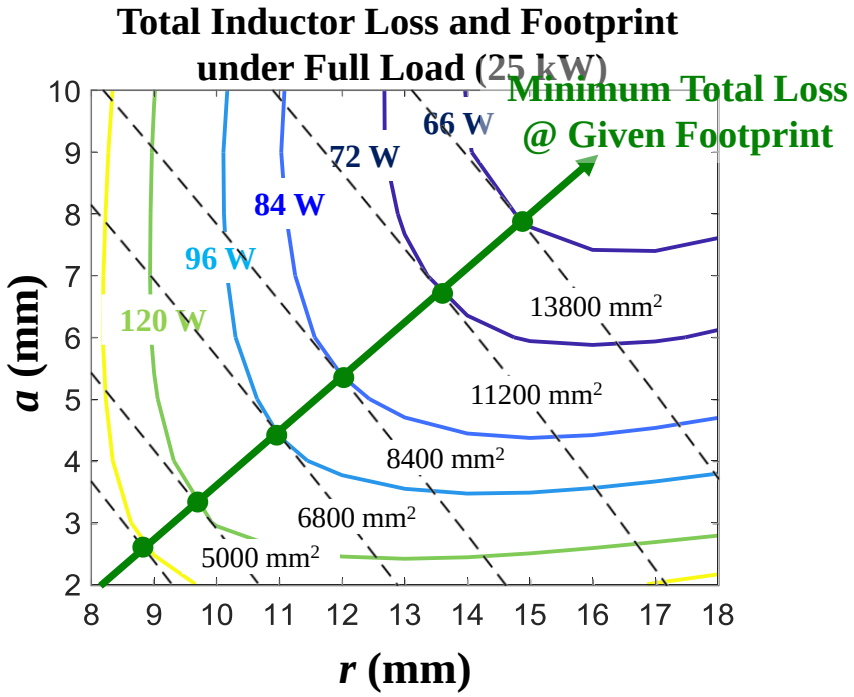
Then, all the design points on the green curve shown in Fig. 4-40 (c) is redrawn in the loss vs. footprint plot shown in Fig. 4-41. The inductor loss breakdown between the winding loss and the core loss is also shown in Fig. 4-41. The area of interest for design is highlighted with blue circle, which is around the knee area of the total loss curve. Finally, the values of the independent variables (*r*, *a*) and the loss breakdown of the selected design point is shown in Table 4-3.



(a)



(b)



(c)

Fig. 4-40. Calculated inductor loss and footprint under different pairs of (r, a). (a) inductor winding loss; (b) inductor core loss; (c) inductor total loss and inductor footprint.

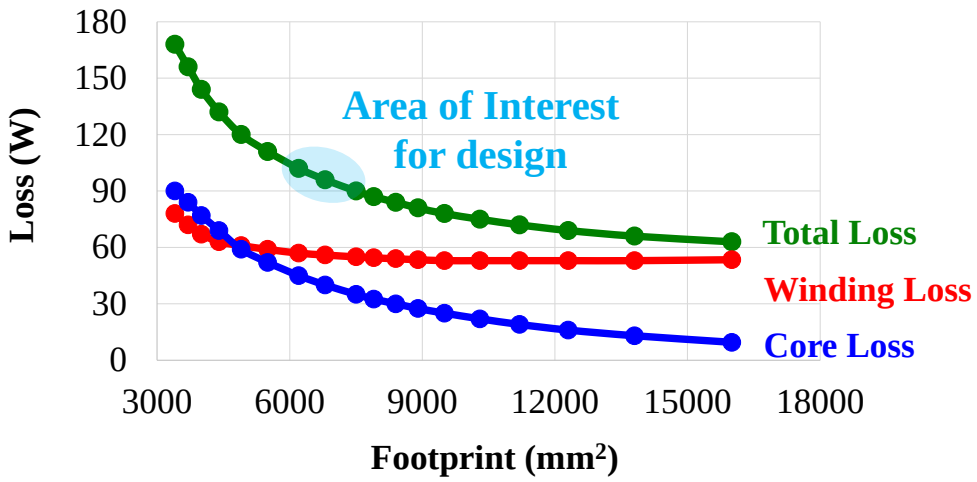


Fig. 4-41. Plot of inductor loss vs. inductor footprint with minimum inductor loss for each footprint.

Table 4-3 Selected Design Point of PCB Winding Coupled Inductors

r	*a*	Winding Loss	Core Loss	Total Loss
12 mm	4 mm	59 W	34 W	93 W

4.5 Experimental Verifications

The experiment verification of the reduction of DM EMI noise is conducted on the 25-kW SiC-based three-phase ac-dc converter prototype introduced in Chapter 2 and Chapter 3. Taking the rectifier mode operation as an example, Fig. 4-42 shows the experimental line-cycle and switching-cycle individual (i_{L1} and i_{L2}) and total (i_L) inductor current waveforms. With negative coupled inductors, stable operation is achieved over the whole line cycle.

The comparison of DM EMI noise testing results are shown in Fig. 4-43 between non-interleaved operation and two-channel interleaved operation under the same power. There is almost 40 dB reduction in the fundamental component at 300 kHz and the 2nd-order harmonic component at 600 kHz becomes dominant from the aspect of the DM EMI filter design.

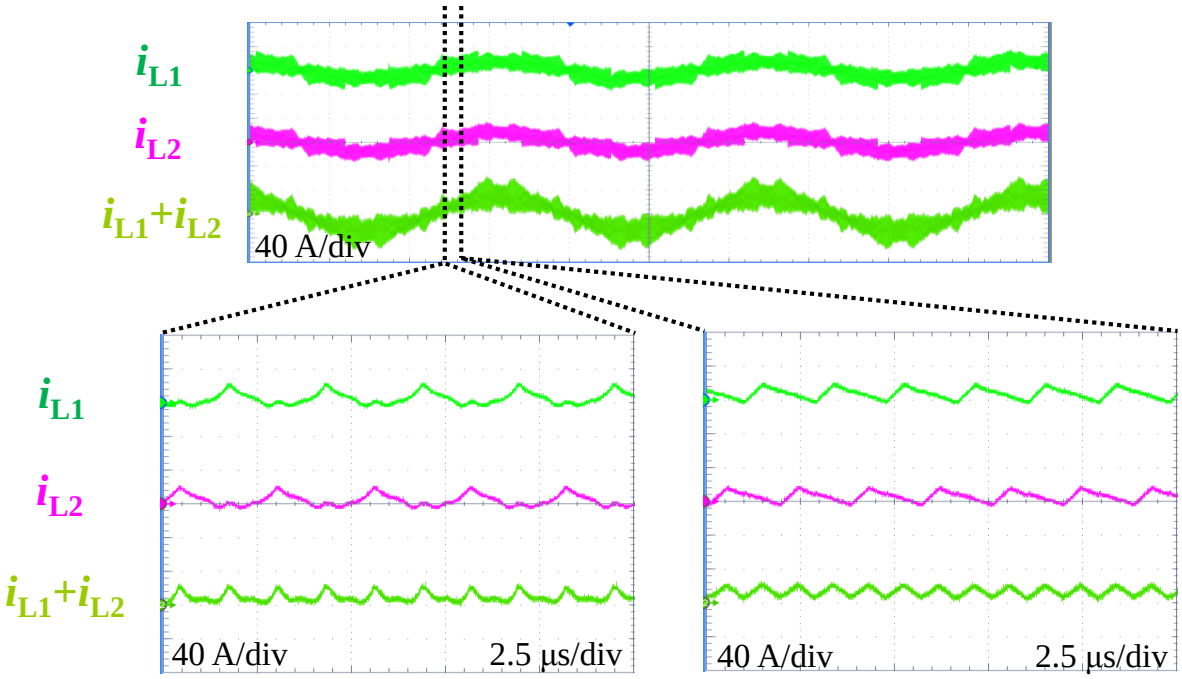


Fig. 4-42. Line-cycle and switching-cycle experiment waveforms of individual and total inductor current in phase A in two-channel interleaved rectifier mode operation.

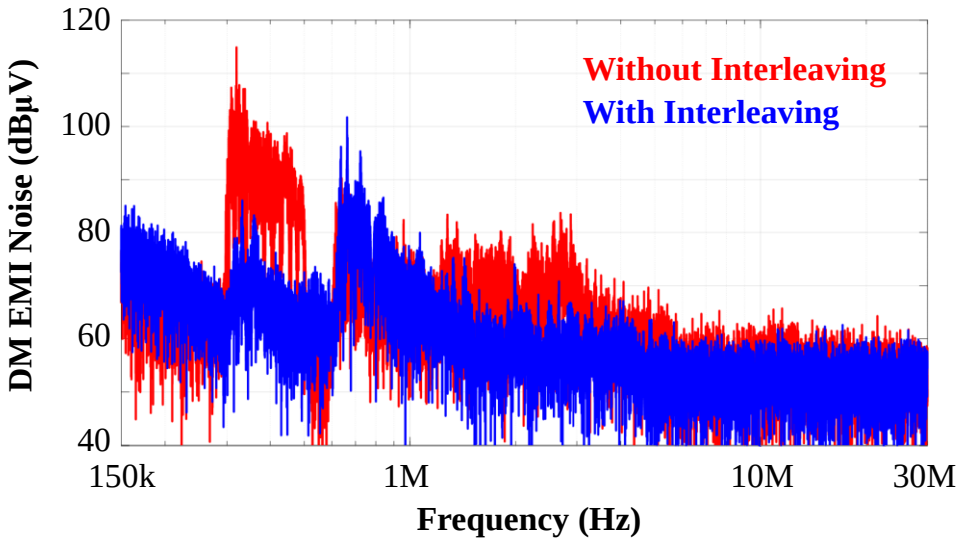


Fig. 4-43. Comparison of DM EMI noise testing results between non-interleaved operation and two-channel interleaved operation under the same power.

For the experimental verification of CM noise reduction, due to the application of balance technique and the utilization of PCB winding inductors, a new version (Generation #2) of hardware prototype is developed, as shown in Fig. 4-44. Compared with the hardware prototype introduced in previous chapters (Generation #1), the layout is improved by utilizing the structure of stacked daughter boards on the mother board, and the power density is 184 W/in^3, including heat sinks, dc side split capacitors, three-phase LCL harmonic filters, devices, gate drivers, and all other sensing ICs. On the left bottom corner, there is some space reserved for the controller.

The detailed design parameters of the converter are listed in Table 4-4. The SiC MOSFETs used in the Generation #1 hardware prototype are discontinued and therefore the SiC MOSFETs from Wolfspeed with similar on-resistance are used to develop the Generation #2 hardware prototype. Fiber optics are used in Generation #2 hardware for the transmission of gate signals and fault signals with excellent noise immunity.

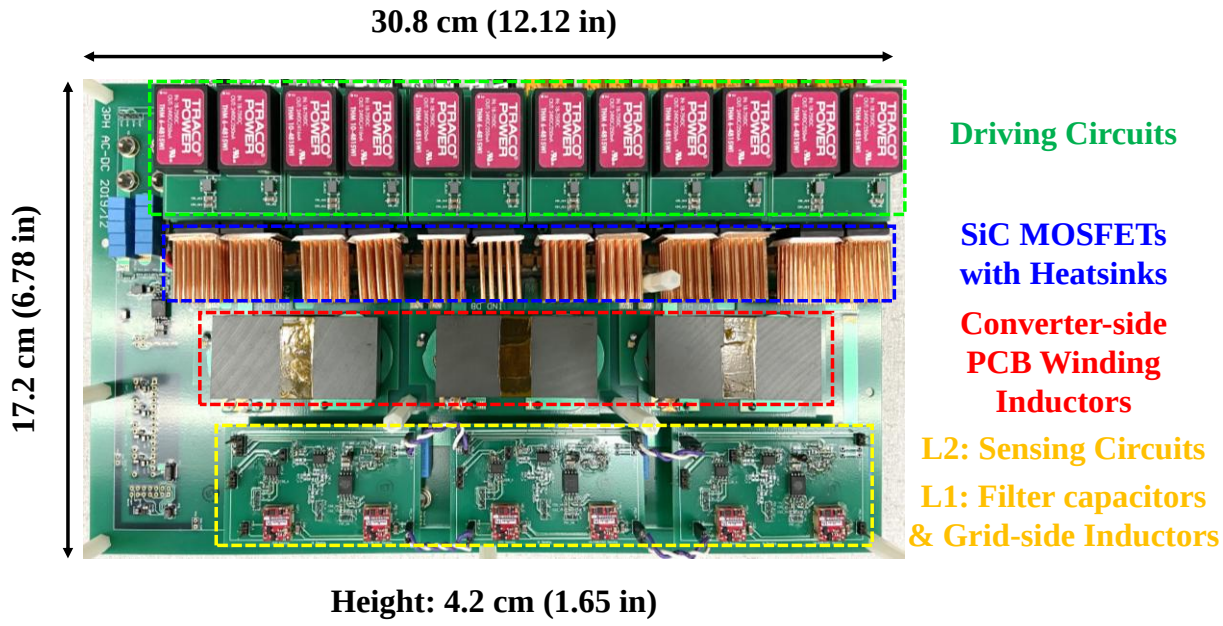


Fig. 4-44. : Generation #2 of 25-kW SiC-based three-phase ac-dc converter prototype featuring PCB winding coupled inductors

Table 4-4 Parameters of the Generation #2 Prototype

Description		Value
Nominal output power (P_O)		25 kW
DC voltage (V_{dc})		800 V
AC grid voltage (V_{ac})		277/480 V, 60 Hz
Switching frequency (F_{SW})		Above 300 kHz
Converter-side self inductance (L_1, L_2, L_3, L_4)		6.4 μH, 6.8 μH, 0.44 μH, 0.44 μH
Converter-side mutual inductance (M_{12}, M_{13}, M_{14}, M_{34})		-2.45 μH, 1.7 μH, -0.65 μH, -0.15 μH
Filter capacitance (C_F)		1.2 μF
Grid-side inductance (L_g)		6.8 μH
DC-side split capacitance (C_{dcs})		0.1 μF
SiC MOSFET	Part No.	C3M0021120K
	Voltage rating (V_{DSS})	1200 V
	On-resistance (R_{DSon})	21 mΩ (25 ℃)
	Package	TO247-4
Microcontroller (MCU)	Part No.	TMS320F28075
	Clock frequency (F_{CLK})	120 MHz
	Control cycle (T_{ISR})	3 μs

The coupling coefficient of the PCB winding inductors is selected based on the equal air gap length for all the magnetic core legs for easier manufacture process.

In this hardware prototype, each terminal of the PCB winding inductors is connected to other parts in the circuit through a short jumper wire. This is beneficial to testing with different inductors. If external inductors are tested, it is necessary to remove the jumper wires in order to bypass the PCB windings.

Fig. 4-45 shows switching-cycle experimental waveforms tested on Generation #2 hardware at different operating points under both rectifier mode (at 80% load condition) and inverter mode (at full load condition), including the gate signal of the control switch, drain-source voltage of the control switch, and the inductor current. ZVS turn-on is achieved at CRM operation for both rectifier mode and inverter mode. The existence of higher order LC resonance in the two-channel

interleaved converter structure makes the time-domain drain-source voltage hard to predict. Therefore the short turn-on delay is not applied during DCM operation, and the valley-switching turn-on at DCM operation cannot be realized in most cases.

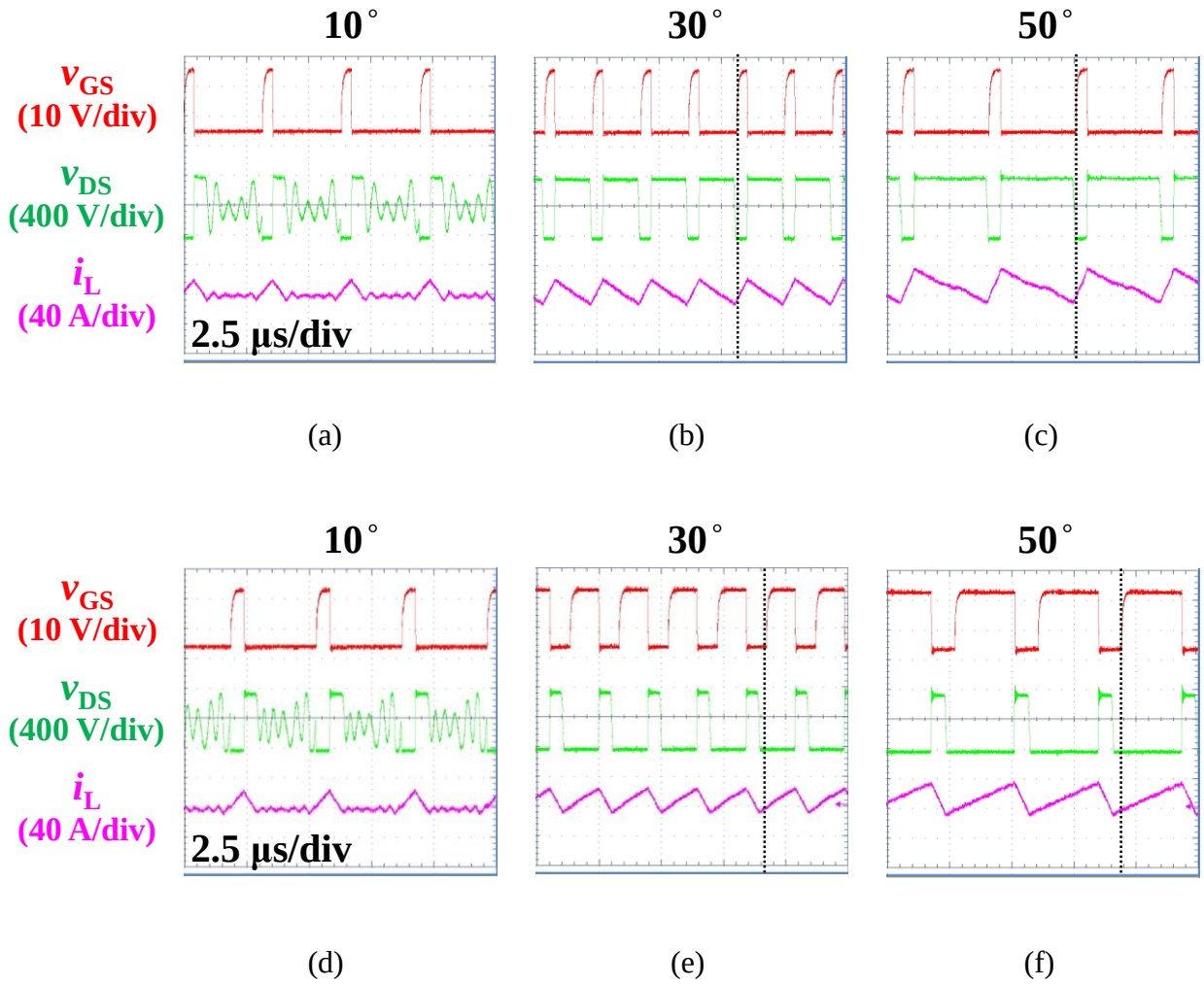


Fig. 4-45. Switching-cycle experimental waveforms in phase A tested on Generation #2 hardware prototype at the following operating points: (a) Around 10 °at DCM in rectifier mode. (b) Around 30 °at boundary of DCM/CRM in rectifier mode. (c) Around 50 °at CRM in rectifier mode. (d) Around 10 °at DCM in inverter mode. (e) Around 30 °at boundary of DCM/CRM in inverter mode. (f) Around 50 °at CRM in inverter mode.

Fig. 4-46 shows the testing results of CM EMI noise on Generation #2 hardware prototype using litz-wire inductors (without balance) and using PCB winding inductors (with balance), respectively. There is a uniform 16 dB – 20 dB reduction in CM EMI noise up to 20 MHz.

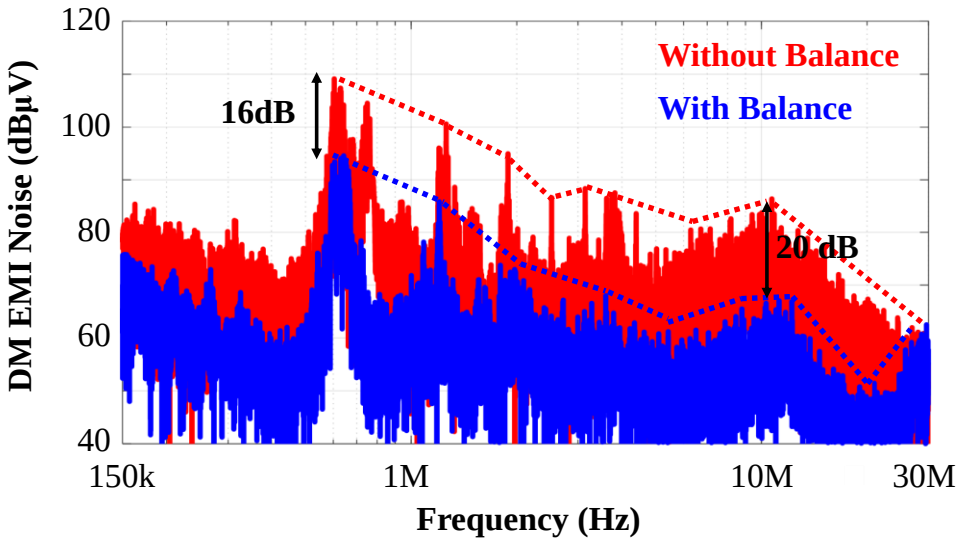


Fig. 4-46. Comparison of CM EMI noise testing results on Generation #2 hardware prototype: using litz-wire inductors (without balance) vs. using PCB winding inductors (with balance).

Fig. 4-47 shows the tested efficiency of Generation #2 hardware prototype, using PCB winding inductors and using litz-wire inductors, respectively. Despite the good CM noise reduction effect by using PCB winding inductors, 0.2% – 0.3% system efficiency is sacrificed by PCB winding inductors compared with the litz-wire inductors. The reason is that in order to pursue the good CM noise reduction effect starting from several MHz frequency range, the PCB winding interleaving is not adopted, which brings much higher ac winding loss compared with the litz-wire inductors. In addition, in three-phase systems, the current in the additional branch contains the information from all three phases. This current does not deliver any main power and it is much smaller compared with that in the main power path due to the cancellation effects among three phases, and therefore there is almost no winding interleaving effect between the L_3 inductor and

the L_1 inductor. This is different from the single-phase totem-pole ac–dc structure, where the L_3 inductor delivers power and it contains the information from the L_2 inductor, indicating that it can be served as the interleaved winding for the L_1 inductor. In sum, there is still room for improving the PCB winding inductor design for the better tradeoff between low CM noise and high efficiency.

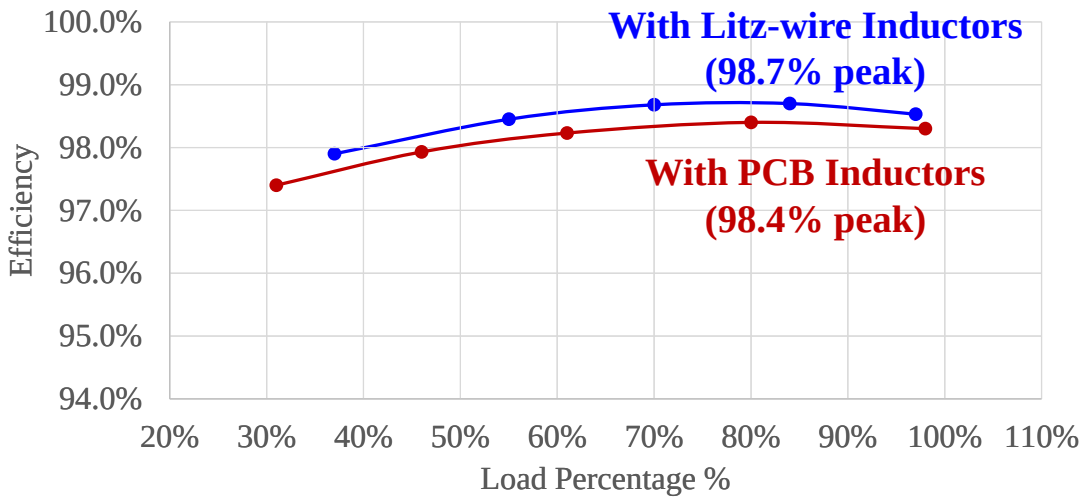


Fig. 4-47. Tested efficiency of Generation #2 hardware prototype: comparison between using PCB winding inductors and using litz-wire inductors.

4.6 Conclusions

In this chapter, methods are proposed for the reduction of conducted EMI noise in SiC-based high-frequency soft switching three-phase ac-dc converters under the "DPWM + CRM + Fs sync." modulation. As for the reduction of DM EMI noise, two-channel interleaving control is applied and the cancellation effect in the total inductor current ripple is achieved. In the two-channel interleaved structure, negative coupled inductors are necessary to avoid the instability in the rectifier mode operation, and meanwhile brings an extra bonus in the reduction of switching frequency variation range. Experiment results show there is a 40 dB reduction of the fundamental switching frequency component in the DM EMI noise. As for the reduction of CM EMI noise,

balance technique is applied by introducing a return path and six additional inductors coupled with the original inductors. The ratio of the parasitic capacitance in the converter needs to be equal to the inductor turns ratio to meet the balance condition and reduce the CM EMI noise, which is achieved by adding external capacitors into the circuit to modify the ratio freely. Experiment results show there is a 16 dB – 20 dB uniform reduction of CM EMI noise up to 20 MHz, while the price of 0.2% – 0.3% efficiency drop is paid with the PCB winding inductors. Further optimization of the PCB winding inductor design is still needed.

Chapter 5 Conclusions and Future Work

5.1 Conclusions

The emerging WBG power semiconductor devices have demonstrated significant improvements when compared with their Si counterparts. For several tens of kW high power applications such as EV charging stations and string PV inverter systems, traditional Si IGBT based design shows high efficiency but low power density due to the limitation in switching frequency. WBG devices, especially SiC MOSFETs in high power applications, are suitable for more than ten times higher switching frequency operation so that the system power density is significantly improved.

SiC MOSFETs, featuring high turn-on energy and low turn-off energy, renders CRM based soft switching operation promising in order to achieve high efficiency similar to the traditional design but at a significantly high operating switching frequency. By combining the DPWM for decoupled control and the DCM operation for shrinking the switching frequency variation range, a novel CRM-based soft switching modulation technique is proposed in this work and applied into three-phase three-wire ac-dc systems. This is the first time that soft switching operation is achieved in three-phase three-wire ac-dc systems, not with auxiliary circuits but purely by control with the help of CRM-based modulation technique. Operation principles are analyzed in order to achieve soft switching and minimize the switching loss during CRM and DCM operation. The proposed soft switching technique is further improved and generalized for both unity and non-unity power factor operating conditions. With the powerful microcontroller, all the proposed control concepts are implemented and the benefits are experimentally verified.

For WBG-based power converter systems with CRM-based soft switching operation, the conducted EMI noise is always a concern, which is caused by the large inductor current ripples and the fast switching of SiC MOSFETs especially at high turn-off currents. Solutions are proposed and the corresponding benefits of the EMI noise reduction are experimentally verified. In addition, PCB winding inductors are designed as part of the solutions to the reduction in CM EMI noise. This is the first time that PCB winding magnetic components are applied in several tens of kW high power three-phase ac-dc applications. Further optimization of the PCB winding inductor design is needed to do better tradeoff between CM noise reduction and high system efficiency.

5.2 Future Work

Design of a power electronics converter system can be divided into two main parts: the software and the hardware. The software part is related to the development of modulation strategy and the design of the control, while the hardware part includes driving and packaging of power semiconductor devices, magnetic components design, the EMI, thermal managements, fault protections, and etc.

This work puts half of the focus on the development of the CRM based soft switching modulation strategy. However, the research in this work is under the ideally balanced three-phase ac system. For grid-tied applications, unbalanced three-phase grid voltages and various grid fault conditions are not uncommon. For stand-alone applications, there is possibility for a three-phase ac-dc system to connect to unbalanced three-phase linear loads or even non-linear loads. These non-ideal conditions need to be considered for the performance optimization, meeting the corresponding standards, or at least the survival of the power converter systems, so that the developed CRM based soft switching modulation technique would be more complete.

Another half of the focus of this work is on the magnetic design mainly for the purpose of reduction in conducted CM EMI noise. With the PCB winding inductors designed in this work, there is a sacrifice in the system efficiency when compared with the litz-wire inductors. New design and optimization methodology for magnetic components at such high-frequency applications is necessary to expedite the application of WBG devices in power electronics systems and make the benefits of WBG devices more thoroughly utilized. In addition, the magnetic loss is also influenced by the temperature, which is closely related to the technology of thermal managements. Therefore, thermal managements are also necessary to be considered when designing the PCB winding inductors to avoid the additional loss to the whole system.

As for the reduction of CM EMI noise with balance technique, significant benefits show up to 20 MHz. It is believed that the ground loop resonance occurs at around 30 MHz and brings the diminishing benefits around that frequency, and therefore further optimization is necessary to extend the range of the effective CM noise reduction up to 30 MHz. Since the resonance frequency depends on the inductance and the parasitic capacitance, either the optimization in the PCB winding inductor or the optimization of PCB layout would be a possible solution to make the ground loop resonance occur above 30 MHz.

Furthermore, it would be promising to integrate the power semiconductor devices, drivers, phase leg decoupling capacitors and magnetic components into a building block, which is mainly beneficial to the minimization of the parasitic inductance in the critical driving/power loops and to the further improvement in system power density. For the three-phase ac-dc system built in this work, each phase is able to be integrated as a building block, including a full bridge and a PCB winding coupled inductors as the two key components. In this way, this building block is able to be flexibly constructed as many different power converter systems, such as dc–dc converters,

single phase rectifiers/inverters and three-phase rectifiers/inverters. Additionally, the capability of manufacture automation with PCB winding based magnetic components is able to reduce the total system cost.

In general, a major challenge existing nowadays is that the advance in WBG devices exceeds the advance in materials for magnetic components in such high-frequency applications. The characterization, driving, sensing and fault protection of SiC MOSFETs have already been relatively mature thanks to the previous generations of research work. For the magnetic design for a SiC-based high power system, probably there is still a long way to go in order to make the system-level performance optimized.

Appendix A. Characterization of Time-Domain Switching Waveforms for Minimizing Switching Loss

An important aspect of the performance with the proposed "DPWM + CRM + Fs sync." modulation is whether soft switching is achieved and whether the switching loss is minimized during a whole line cycle. Take the unity power factor condition and the first 30 °line-cycle interval as an example, where phase A operates at the DCM, phase C operates at the CRM, and phase B is clamped to the negative dc bus. Considering the device output capacitance (C_{OSS}), for both phase A and phase C, in each switching cycle after inductor current zero crossing happened, LC resonance between the converter side inductor (hereinafter "inductor" unless otherwise specified) and the device output capacitance occurs, which brings a small amount of negative inductor current and helps to discharge the control switch output capacitance (and thus the control switch drain–source voltage is reduced). However, before the control switches are turned on in phase A and in phase C, inductor currents have already touched zero and LC resonance occurs in these two phases make the equivalent circuit become a fourth − order LC resonance circuit at this instant, and therefore very complicated to derive analytical expressions of device drain–source voltage.

Consequently, the analysis of this fourth − order LC resonance period with the proposed modulation is done in a numerical way using state-space equations. The operation analysis related to ZVS with the proposed modulation on the two-level H-bridge structure is presented in the rest of this section under the unity-power-factor inverter mode, under the unity-power-factor rectifier mode, and non-unity-power-factor inverter mode, respectively. Analysis in this section is based on the first 60 °line-cycle interval under the aforementioned high modulation index condition (V_{dc} = 800 V, $V_{ac,\,L\text{-}L}$ = 480 V, M = 0.849) as an example. For the analysis in this section, the following

assumptions are made. First, the damping effect during LC resonance period is negligible. Second, in one switching cycle, the values of ac grid voltage and of ac reference current in each phase are considered constant, respectively. Third, the voltage drops on the grid-side inductors are negligible, and therefore, the grid-side inductors in the circuit diagram are ignored. Fourth, based on specific devices to be used, the time-related device output capacitance value at $v_{DS} = V_{dc}$ is used for analysis.

I. Minimization of Switching Loss in Inverter Mode under Unity Power Factor

The circuit diagram and definitions used in this part of analysis in the inverter mode under unity power factor are shown in Fig. A- 1, including the DPWM clamping in phase B and device output capacitances (C_{OSS}) in the other two phases. Under unity power factor, operational symmetry exists between 0 °– 30 °line-cycle interval and 30 °– 60 °line-cycle interval. Therefore, the first 30 °line-cycle interval is used for the analysis here. During this interval, S_{A1} and S_{C1} are the control switches in these two phases, respectively, while S_{A2} and S_{C2} are the SRs.

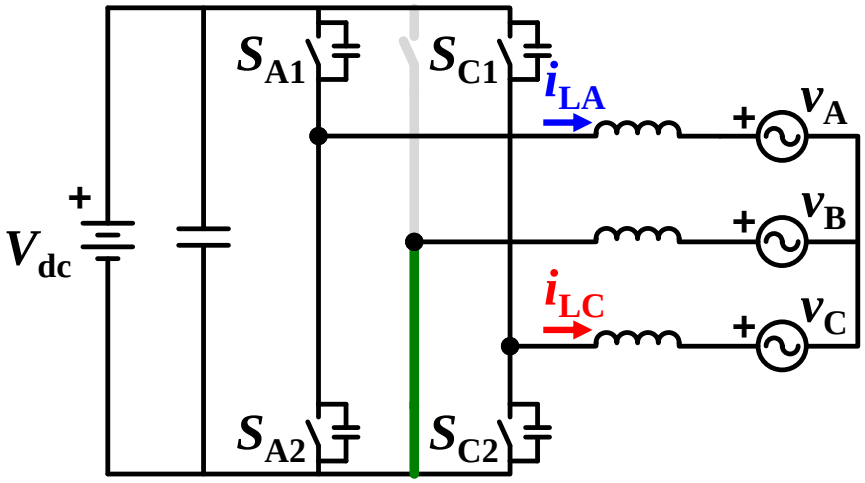


Fig. A- 1. Circuit diagram of three-phase ac–dc structure for operation analysis in the inverter mode.

Fig. A- 2 shows switching-cycle waveforms in phase A and phase C at an arbitrarily selected line-cycle operating point during the first 30 °line-cycle interval. At t_0 instant, the inductor current

zero crossing occurs in phase A. Since the operation before this instant is not related to ZVS, the analysis is only focused on the operation after this instant. Starting from t_0 instant, the LC resonance occurs between the device output capacitances in phase A and all three inductors. The ringing effects in i_{LA}, v_{DSA1}, and i_{LC} beginning from t_0 instant are the results of the LC resonance. Although five energy storage elements (three inductors and two capacitors) participate in this LC resonance, only two among them are independent, and thus, it is still a second − order LC resonance circuit before the inductor current zero crossing occurs in phase C at t_1 instant. Therefore, two independent state variables v_{DSA1} and i_{LA} are selected, and the state-plane trajectory between these two independent state variables right before t_1 instant is shown in Fig. A- 3.

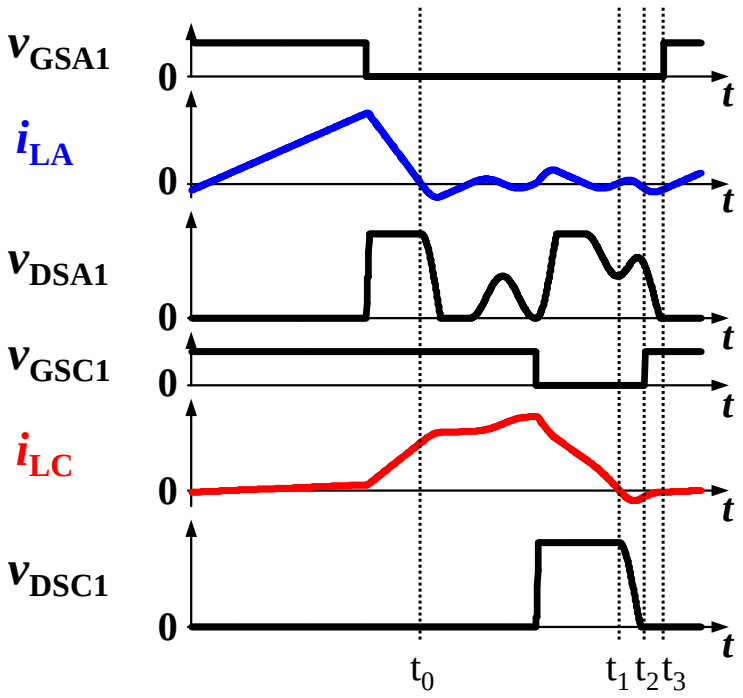


Fig. A- 2. Typical switching-cycle waveforms in phase A and phase C during the first 30 ° line-cycle interval in the inverter mode.

At t_1 instant, the inductor current zero crossing occurs in phase C and after that phase C together with phase A participates in the LC resonance, between the device output capacitances in

phase A, phase C, and the three inductors. Among the seven energy storage elements (three inductors and four capacitors), it is clear that four elements are independent, indicating a fourth − order LC circuit before the drain–source voltage in phase C reaches zero at t_2 instant. v_{DSA1}, v_{DSC1}, i_{LA}, and i_{LC} are selected as the four state variables, and the following state-space equations are derived (V_A and V_C are line-to-neutral voltage in phase A and phase C at a specific line-cycle operating point, which is assumed constant, respectively; V_{dc} is the dc voltage):

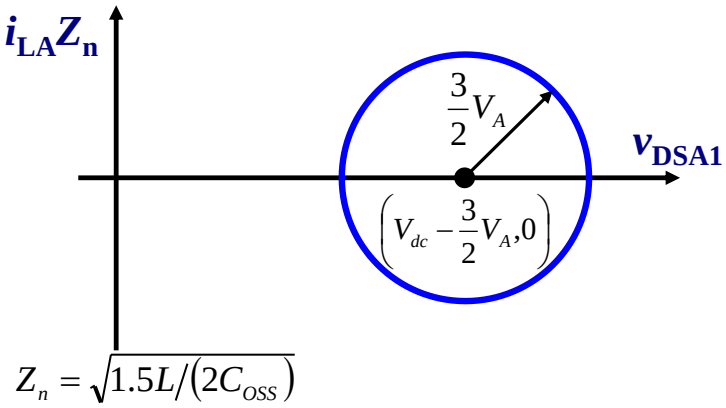


Fig. A- 3. State-plane trajectory between v_{DSA1} and i_{LA} right before t_1 instant in Fig. A- 2.

$$\frac{d}{dt}\begin{bmatrix} v_{DSC1}(t) \\ i_{LC}(t) \\ v_{DSA1}(t) \\ i_{LA}(t) \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{2C_{oss}} & 0 & 0 \\ -\frac{2}{3L} & 0 & \frac{1}{3L} & 0 \\ 0 & 0 & 0 & \frac{1}{2C_{oss}} \\ \frac{1}{3L} & 0 & -\frac{2}{3L} & 0 \end{bmatrix} \begin{bmatrix} v_{DSC1}(t) \\ i_{LC}(t) \\ v_{DSA1}(t) \\ i_{LA}(t) \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ -\frac{1}{L} & 0 & \frac{1}{3L} \\ 0 & 0 & 0 \\ 0 & -\frac{1}{L} & \frac{1}{3L} \end{bmatrix} \begin{bmatrix} V_C \\ V_A \\ V_{dc} \end{bmatrix} \quad \text{(A-1)}$$

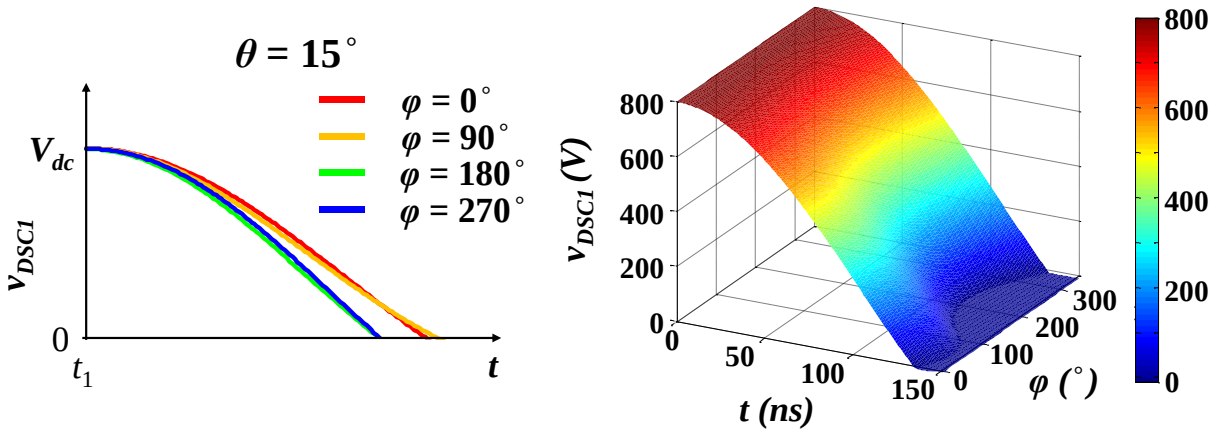
The initial conditions (values at t_1 instant) of all the state variables in Equation (A-1) are determined as follows. In phase C, it is evident $v_{DSC1}(t_1) = V_{dc}$ and $i_{LC}(t_1) = 0$. In phase A, since t_1 instant is the endpoint of the precedent second − order LC resonance period, the value combination of $v_{DSA1}(t_1)$ and $i_{LA}(t_1)$ is located on the circle shown in Fig. A- 3. Different load conditions result in different durations of DCM dead-time and thus different initial conditions in phase A. All the

possible value combinations of $v_{DSA1}(t_1)$ and $i_{LA}(t_1)$ are expressed in the following parametric form (Z_n is the characteristic impedance defined in Fig. A- 3; φ is a parameter ranging from 0 to 360 °):

$$\begin{cases} v_{DSA1}(t_1) = V_{dc} - \dfrac{3}{2}V_A + \dfrac{3}{2}V_A \cos\varphi \\ i_{LA}(t_1) = \dfrac{3}{2}V_A \dfrac{1}{Z_n}\sin\varphi \end{cases} \tag{A-2}$$

According to the state-space equations in Equation (A-1) and the initial conditions defined above, the time-domain values of v_{DSC1} during t_1–t_2 interval are solved numerically and the valley point of v_{DSC1} is found from the solution. However, it should be noted that Equations (A-1) and (A-2) are dependent on the line-cycle phase angle θ ($0 \le \theta \le 30$ °) and the initial condition parameter φ ($0 \le \varphi < 360$ °). For a comprehensive analysis, all possible value combinations of θ and φ should be considered.

The first step is to fix the value of θ and to sweep the value of φ from 0 to 360 °. Consider θ = 15 °as an example. The time-domain values of v_{DSC1} during t_1–t_2 interval are solved and shown in Fig. A- 4 (a) with four different example φ values. v_{DSC1} can reach zero in all these four cases during this LC resonance period, and the required time period for v_{DSC1} to drop from V_{dc} to zero is also calculated in each case. Furthermore, by sweeping φ from 0 to 360 °, the time-domain values of v_{DSC1} during t_1–t_2 interval are solved and shown as a three-dimensional (3-D) plot in Fig. A- 4 (b). In Fig. A- 4 (b), the zero instant in the time axis corresponds to the t_1 instant in Fig. A- 2. For all the possible initial conditions in phase A (all the φ values from 0 to 360 °), at this fixed line-cycle operating point of θ = 15 °, v_{DSC1} can reach zero during this fourth − order LC resonance period (after that the body diode of the control switch begins conduction), and thus, ZVS is naturally achieved in the inverter mode at this line-cycle operating point during CRM operation.



(a) (b)

Fig. A- 4. Time-domain calculated results of v_{DSC1} (control switch drain–source voltage in phase C) values during t_1–t_2 interval in Fig. A- 2, with fixed θ = 15 °but with different φ values as an example. (a) With four different φ values. (b) With all the possible φ values.

The second step is to sweep the value of θ from 0 to 30 °and repeat the first step process. It is found v_{DSC1} can always reach zero during this fourth − order LC resonance period at any line-cycle operating point for all possible initial conditions in phase A, which indicates ZVS is naturally achieved at any line-cycle operating point during CRM operation in the inverter mode.

It should be noted that the control switch needs to be turned on not only after the drain–source voltage reaches zero, but also before the inductor current returns to zero from a negative value in phase C. In other words, there is an optimal interval to turn on the control switch in phase C. For implementation, this turn-on instant is selected as the midpoint of the optimal interval.

As for phase A operating at the DCM, ZVS is not necessarily achieved since the turn-on instant is determined by phase C. However, it is still possible to minimize DCM turn-on loss by adding a short turn-on delay to phase A, which is shown as t_2–t_3 interval in Fig. A- 2. With this turn-on delay, the control switch in phase A is turned on at the valley drain–source voltage point.

The required turn-on delay in phase A is calculated based on state-plane trajectory. During t_2–t_3 interval, only phase A participates in the LC resonance, and thus, it is a second − order LC resonance circuit. v_{DSA1} and i_{LA} are selected as the two independent state variables. The center of this second − order LC resonance is shown in Fig. A- 5 on the horizontal axis. The initial condition of these two state variables during t_2–t_3 interval (values at the endpoint of precedent fourth − order LC resonance period during t_1–t_2 interval) is marked in Fig. A- 5 as the red point. Then, the trajectory will closely track the blue curve beginning at the red point. The instant the blue curve touches the horizontal axis indicates v_{DSA1} has reached the valley point. Thus, the required time period for v_{DSA1} to reach the valley point, which is the required turn-on delay in phase A, is expressed as follows:

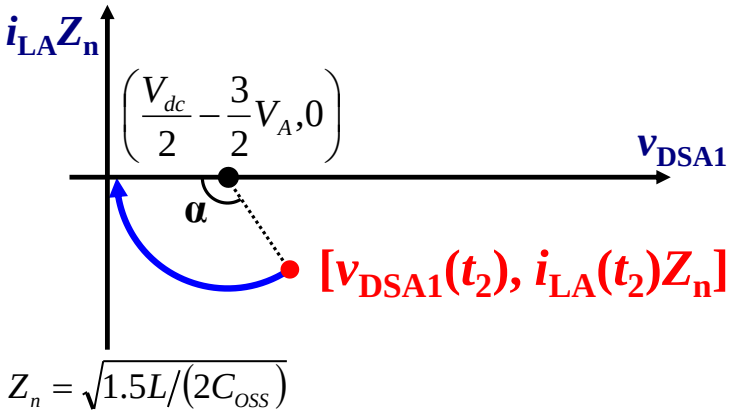


Fig. A- 5. State-plane trajectory between v_{DSA1} and i_{LA} right after t_2 instant in Fig. A- 2.

$$t_{delay}=\alpha\sqrt{1.5L\cdot 2C_{oss}}=\left(\pi-\arctan\left|\frac{i_{LA}(t_2)Z_n}{v_{DSA1}(t_2)-0.5V_{dc}+1.5V_A}\right|\right)\sqrt{1.5L\cdot 2C_{oss}} \qquad \text{(A-3)}$$

Based on Equation (A-3), by sweeping θ from 0 to 30 ° and sweeping φ from 0 to 360 °, the required turn-on delay in phase A is calculated for all the cases with different value combinations of θ and φ. For simplicity of implementation, at each line-cycle operating point, the required turn-

on delay is selected as the average of all the calculated values with φ ranging from 0 to 360 °. From the calculation, in most cases, it is found ZVS is also achieved in phase A with this turn-on delay.

In sum, in the inverter mode with V_{dc} = 800 V, V_{ac} = 277/480 V, and M = 0.849 condition, ZVS is naturally achieved at any line-cycle operating point during CRM operation, and valley point turn-on (ZVS turn-on in most cases) is achieved during DCM operation to minimize DCM turn-on loss. Similar operation analysis is applicable to other modulation index conditions.

II. Minimization of Switching Loss in Rectifier Mode under Unity Power Factor

The circuit diagram and definitions used in this part of analysis in the rectifier mode under unity power factor are shown in Fig. A- 6. Different from the inverter mode, here during the first 30 °line-cycle interval, S_{A2} and S_{C2} are the control switches in these two phases, respectively, while S_{A1} and S_{C1} are the SRs.

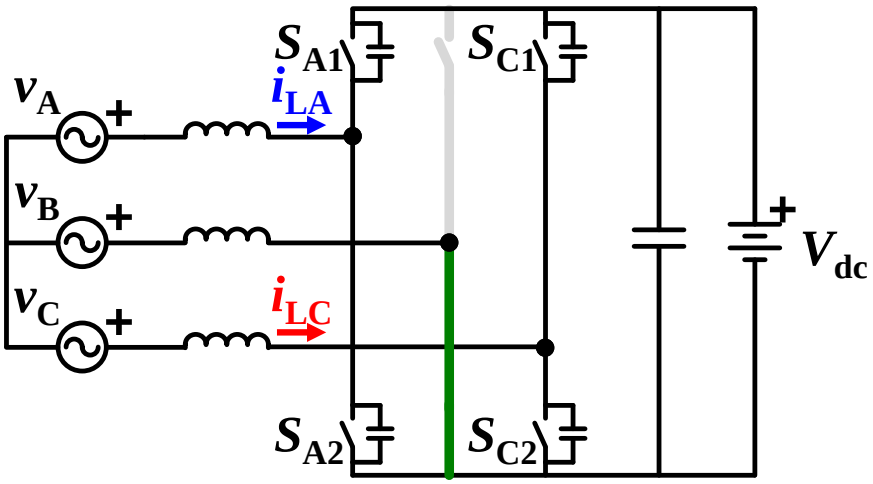
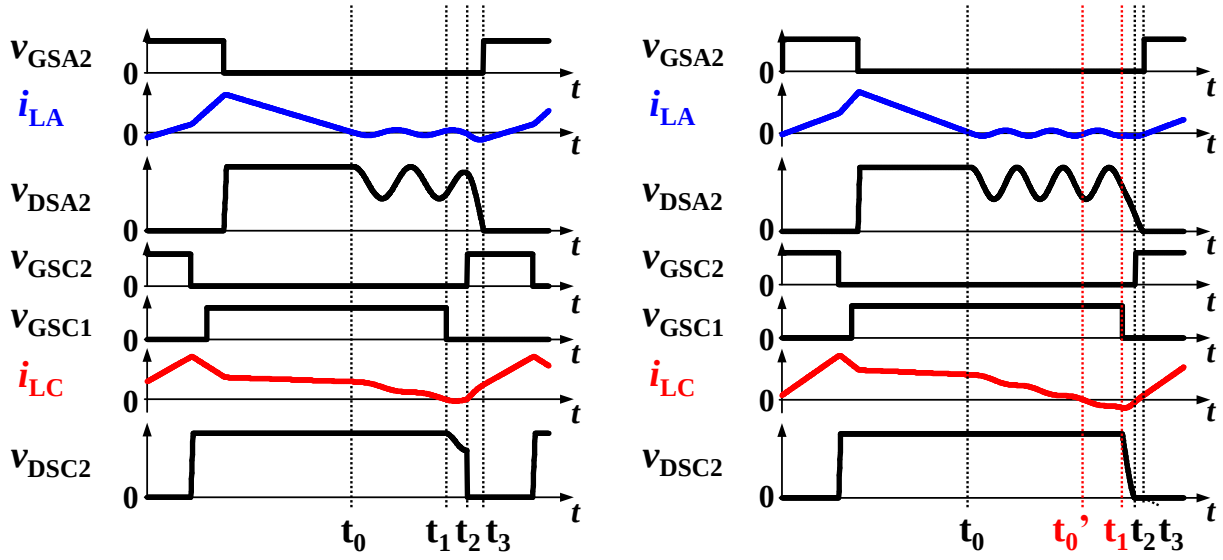


Fig. A- 6. Circuit diagram of the three-phase ac–dc structure for operation analysis in the rectifier mode.

Fundamentally, the operation analysis in the inverter mode in the previous part is applicable to the operation analysis in the rectifier mode. Fig. A- 7 (a) shows switching-cycle waveforms in

phase A and phase C at an arbitrarily selected line-cycle operating point during the first 30 °line-cycle interval.

As presented with the operation analysis in the inverter mode in the previous part, at t_0 instant, the inductor current zero crossing occurs in phase A. The second − order LC resonance starts from t_0 instant and ends at t_1 instant, when the inductor current zero crossing occurs and the SR is turned off in phase C.



(a) (b)

Fig. A- 7. Typical switching-cycle waveforms in phase A and phase C during the first 30 °line-cycle interval in the rectifier mode. (a)Without off-time extension. (b) With off-time extension.

After that, the fourth − order LC resonance begins. However, it is shown in Fig. A- 7 (a) v_{DSC2} cannot reach zero during this fourth − order LC resonance period, which indicates the control switch in phase C cannot be turned on at zero voltage, but rather at the valley point voltage. The valley point of v_{DSC2} happens at t_2 instant, when i_{LC} returns to zero from a negative value. Although the control switch in phase C is turned on optimally at t_2 instant with the minimum CRM non-ZVS

turn-on loss, this part of the loss has impact on the system efficiency, especially at high switching frequency operation.

The reason for CRM non-ZVS turn-on is insufficient negative current. To provide more negative current, after inductor current zero crossing occurs in phase C, off-time is extended by making the SR conduct for an extra period of time [27], [36]–[39]. Fig. A- 7 (b) shows switching-cycle waveforms with this off-time extension (t_0'−t_1 interval highlighted with the color red is the extended off-time period) at the same line-cycle operating point as in Fig. A- 7 (a). From Fig. A-7 (b), it is shown with off-time extension, v_{DSC2} reaches zero during the fourth − order LC resonance period at t_1−t_2 interval, which means ZVS is achieved. Thus, off-time extension is required for ZVS.

As for the operation analysis for every operating point during the first 30 °line-cycle interval in the rectifier mode, the process is similar to the analysis in the inverter mode in the previous part, except for the state space equations during the fourth − order LC resonance period (t_1−t_2 interval in Fig. A- 7) and corresponding initial conditions during this period. In the rectifier mode, v_{DSA2}, v_{DSC2}, i_{LA}, and i_{LC} are the four selected state variables during the fourth − order LC resonance period, and the corresponding state-space equations are as follows (V_A and V_C are line-to-neutral voltage in phase A and phase C at a specific operating point, which is assumed constant, respectively):

$$\frac{d}{dt}\begin{bmatrix} v_{DSC2} \\ i_{LC} \\ v_{DSA2} \\ i_{LA} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{2C_{oss}} & 0 & 0 \\ -\frac{2}{3L} & 0 & \frac{1}{3L} & 0 \\ 0 & 0 & 0 & \frac{1}{2C_{oss}} \\ \frac{1}{3L} & 0 & -\frac{2}{3L} & 0 \end{bmatrix} \begin{bmatrix} v_{DSC2} \\ i_{LC} \\ v_{DSA2} \\ i_{LA} \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ \frac{1}{L} & 0 \\ 0 & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} V_C \\ V_A \end{bmatrix} \tag{A-4}$$

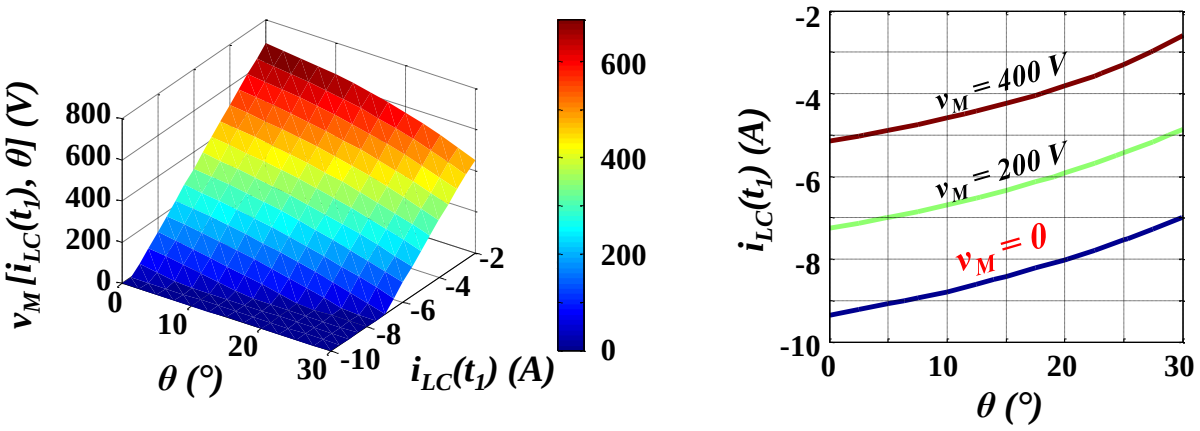
The initial conditions (the values at t_1 instant) of all the state variables in Equation (A-4) are determined as follows. In phase C and without off-time extension, it is evident $v_{DSC2}(t_1) = V_{dc}$ and $i_{LC}(t_1) = 0$. In phase A and similar to the inverter mode in the previous part, all the possible value combinations of $v_{DSA2}(t_1)$ and $i_{LA}(t_1)$ are located on a circular trajectory similar to Fig. A- 3, but with the center at $(0.5V_{dc} + 1.5V_A, 0)$ and the radius as $(0.5V_{dc} - 1.5V_A)$. Therefore, the combinations are expressed as the following parametric form (Z_n and φ have the same definition as in the previous part):

$$\begin{cases} v_{DSA2}(t_1) = \frac{1}{2}V_{DC} + \frac{3}{2}V_A + \left(\frac{1}{2}V_{DC} - \frac{3}{2}V_A\right)\cos\varphi \\ i_{LA}(t_1) = \left(\frac{1}{2}V_{DC} - \frac{3}{2}V_A\right)\frac{1}{Z_n}\sin\varphi \end{cases} \tag{A-5}$$

According to the state-space equations in Equation (A-4) and the initial conditions defined above, by sweeping θ from 0 to 30 °and sweeping φ from 0 to 360 °, the calculation of time-domain values of v_{DSC2} during t_1−t_2 interval shows the valley point value of v_{DSC2} is always higher than zero, which indicates ZVS cannot be achieved naturally at any line-cycle operating point with any initial condition in phase A during CRM operation in the rectifier mode (when M = 0.849). Thus, off-time extension is required at every operating point for ZVS.

The next step is to determine the minimum required extended off-time [Fig. A- 7 (b) t_0'−t_1 interval], which is also equivalent to the minimum required negative current value (hereinafter "i_{neg_req}") at t_1 instant when the SR is turned off in phase C. For ZVS at each line-cycle operating point, the required negative current value at t_1 instant should confirm the valley point value of v_{DSC2} during the fourth − order LC resonance period is no higher than zero, considering all the possible φ values ranging from 0 to 360 °.

Therefore, according to the state-space equations in Equation (A-4) and the defined initial conditions, with a fixed negative current value at t_1 instant: $i_{LC}(t_1)$ and a fixed operating point θ sweep φ from 0 to 360 ° and calculate the valley point value of v_{DSC2} in each case and find the maximum value. In other words, the worst case among all the valley point values of v_{DSC2} at different φ (define this worst case value as "v_M" and it is a function of $i_{LC}(t_1)$ and θ). Then, with different $i_{LC}(t_1)$ values and at different operating points during the first 30 °line-cycle interval, the 3-D surface of v_M [$i_{LC}(t_1)$, θ] is shown in Fig. A- 8 (a) and a corresponding contour map is shown in Fig. A- 8 (b). The v_M = 0 curve in Fig. A- 8 (b) indicates the required minimum negative current i_{neg_req} at different operating points during the first 30 °line-cycle interval for achieving ZVS turn-on, since giving the negative current $i_{LC}(t_1)$ located on the v_M = 0 curve, the valley point of v_{DSC2} will reach zero, considering all the possible φ values ranging from 0 to 360 °.



(a) (b)

Fig. A- 8. (a) 3-D distribution of the worst-case valley point value of v_{DSC2} (v_M), during the fourth − order LC resonance period in the rectifier mode, at different operating points (θ, from 0 to 30 °) and with different negative current values at t_1 instant $i_{LC}(t_1)$. (b) Contour of (a).

Based on the v_M = 0 curve shown in Fig. A- 8 (b) and the phase C inductor current slew rate at t_0'−t_1 interval shown in Fig. A- 7, the minimum required extended off-time is determined.

For phase A operating at the DCM in the rectifier mode, the similar turn-on delay is applied, which is shown in Fig. A- 7, as t_2−t_3 interval to achieve valley point turn-on of the control switch in phase A. The DCM turn-on loss in the rectifier mode is also minimized with this turn-on delay.

In sum, in the rectifier mode with V_{dc} = 800 V, V_{ac} = 277/480 V, and M = 0.849 condition, ZVS turn-on cannot be naturally achieved at any line-cycle operating point during CRM operation, and off-time extension is required for ZVS. Valley point turn-on (ZVS turn-on in most cases as well) is achieved during DCM operation to minimize DCM turn-on loss. Similar operation analysis is applicable to other modulation index conditions.

III. Minimization of Switching Loss in Inverter Mode under Non-Unity Power Factor

In previous parts, the complexity of the fourth-order equivalent LC resonance circuit redrawn in Fig. A- 9 for the operational analysis of the soft-switching capability with the original "DPWM + CRM + Fs sync" modulation technique is identified, and, therefore, a numerical method based on state-space equations is developed. The conclusion presented in previous parts is that for three-phase inverters under unity PF condition and the aforementioned modulation index condition, ZVS turn-on is naturally achieved during CRM operation and valley drain–source voltage turn-on (ZVS turn-on in most cases) is achieved during DCM operation. However, under non-unity PF conditions, the conclusion becomes different.

For each of the non-unity PF case, the operation mode repeats itself every one sixth of the line cycle, which is the same as the unity PF case. As for the operational symmetry, it exists in the unity PF case with 30 ° as the axis of symmetry. Therefore, the analysis of the soft-switching capability presented in previous parts is able to be simplified and only focused on the first 30 °line-cycle interval. However, for non-unity PF cases, the operational symmetry only exists between the lagging case and the leading case under the same PF value, but not for each case itself. Therefore,

the first 60 °line-cycle interval should be entirely considered. In addition, the optimal CRM/DCM transition angle changes with the PF value, which may cause different operation modes even at the same line-cycle phase angle θ.

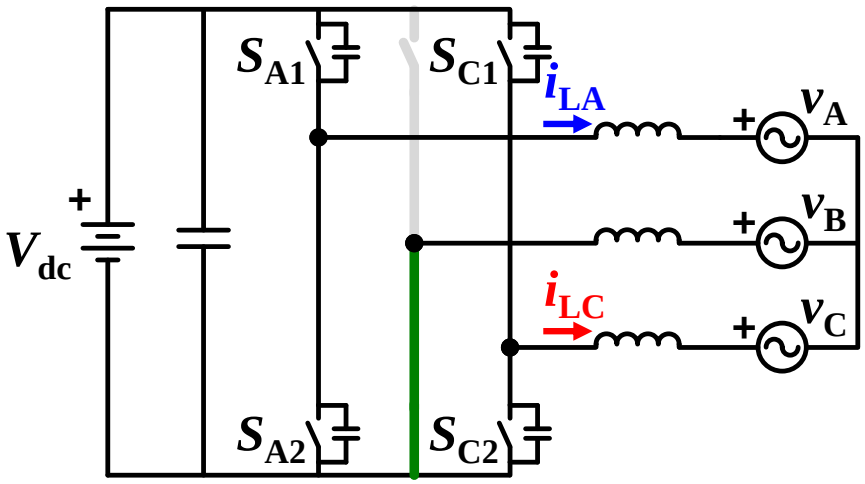


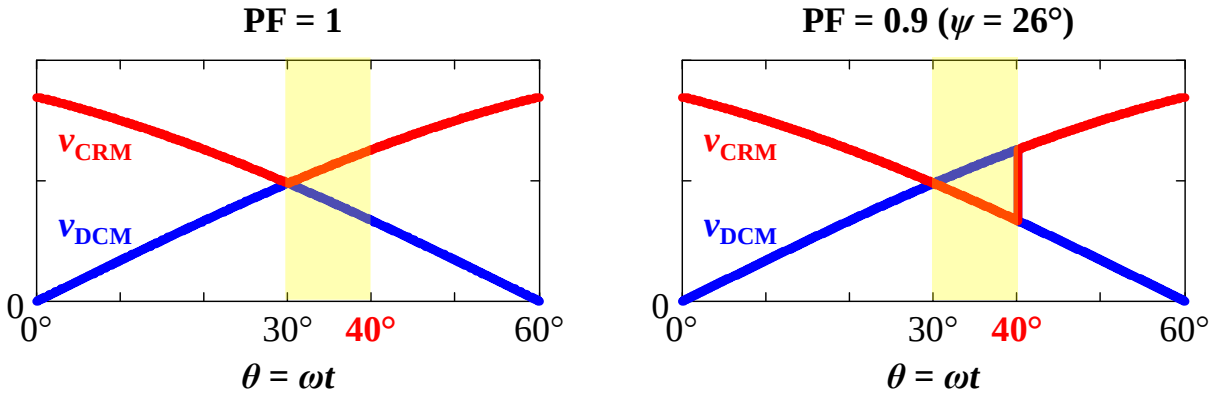
Fig. A- 9. Fourth-order equivalent LC resonance circuit during the first 60 °line-cycle interval.

Considering the abovementioned reasons, the numerical method developed in previous parts is modified here. The four state variables are still the inductor current and the control switch drain–source voltage in the two controlled phases (phase A and phase C) but are categorized based on the operation mode in each phase. Specifically, the modified state-space equation and the modified initial condition are given as follows:

$$\frac{d}{dt}\begin{bmatrix} v_{DSCRM}(t) \\ i_{LCRM}(t) \\ v_{DSDCM}(t) \\ i_{LDCM}(t) \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{2C_{oss}} & 0 & 0 \\ -\frac{2}{3L} & 0 & \frac{1}{3L} & 0 \\ 0 & 0 & 0 & \frac{1}{2C_{oss}} \\ \frac{1}{3L} & 0 & -\frac{2}{3L} & 0 \end{bmatrix} \begin{bmatrix} v_{DSCRM}(t) \\ i_{LCRM}(t) \\ v_{DSDCM}(t) \\ i_{LDCM}(t) \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ -\frac{1}{L} & 0 & \frac{1}{3L} \\ 0 & 0 & 0 \\ 0 & -\frac{1}{L} & \frac{1}{3L} \end{bmatrix} \begin{bmatrix} V_{CRM}(\theta,\psi) \\ V_{DCM}(\theta,\psi) \\ V_{dc} \end{bmatrix} \quad \text{(A-6)}$$

$$\begin{cases} v_{DSCRM}(0) = V_{dc} \\ i_{LCRM}(0) = 0 \\ v_{DSDCM}(0) = V_{dc} - \frac{3}{2}V_{DCM}(\theta,\psi) + \frac{3}{2}V_{DCM}(\theta,\psi)\cos\varphi \\ i_{LDCM}(0) = \frac{3}{2}V_{DCM}(\theta,\psi)\sqrt{\frac{3C_{oss}}{2L}}\sin\varphi \end{cases} \quad \text{(A-7)}$$

Here the subscript "CRM" represents the state variables or the inputs from the phase with CRM operation. The same definition applies to the subscript "DCM". φ is the initial condition angle ranging from 0 °to 360 °as defined in previous parts. With this modification, the information of the PF is also included, which is reflected in the ac line-to-neutral voltage in the two controlled phases, v_{CRM} and v_{DCM}. Take the PF = 1 case and the PF = 0.9 (ψ = 26 °) case as an example. Fig. A- 10 shows the distribution of these two voltages over the first 60 °line-cycle interval.



(a) (b)

Fig. A- 10. Distribution of the line-to-neutral voltage in the phase with DCM (v_{DCM}) and that in the phase with CRM (v_{CRM}) during the first 60 °line-cycle interval. (a) Under PF = 1 condition. (b) Under PF = 0.9 (ψ = 26 °) condition.

The state-space equation and the corresponding initial condition is based on each operating point θ and each PF angle ψ. This fourth-order LC resonance period starts when the inductor

current zero crossing occurs in both the two controlled phases and ends when the control switch is turned on in at least one of these two phases.

From Equations (A-6) and (A-7), when the dc voltage value and the ac voltage value change proportionally (the modulation index M is kept the same), the soft-switching capability does not change. When there are proportional changes in the dc voltage value and the ac voltage value, the input and the initial conditions also change proportionally, which only results in proportional change in the time-domain values of all the state variables. However, whether the drain–source voltage reaches zero during LC resonance period, and the required time period for it to reach zero do not change.

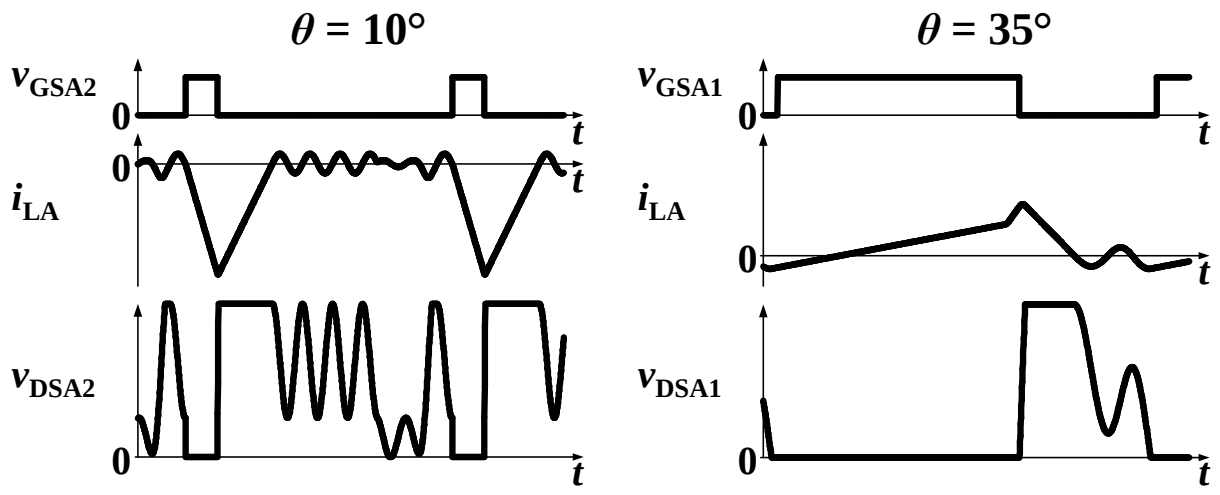
With the above-mentioned modified numerical model, the soft-switching capability of three-phase inverters with the generalized "DPWM + CRM + Fs sync" modulation technique under different non-unity PF conditions is analyzed. The analysis is based on the aforementioned example modulation index (V_{dc} = 800 V, V_{ac} = 277/480 V, M = 0.849) condition, but under two different PF conditions: PF = 0.9 (ψ = 26 °) and PF = 0.8 (ψ = 37 °) as examples. The similar analysis process is applicable to other modulation index conditions and leading PF conditions. In this part, the same assumptions as presented in previous parts are made for analysis.

For the first example of PF = 0.9 (ψ = 26 °), according to the operation modes shown in Fig. 3-12 and the polarity of ac reference currents, at any operating point, the top switch works as the control switch in the phase operating at CRM. Therefore, in each switching cycle after the inductor current zero crossing occurs in both phase A and phase C, the equivalent fourth-order LC circuit during this resonance period is the same as shown in Fig. A- 9, which has Equation (A-6) as the state-space equations and Equation (A-7) as the initial conditions.

From the previous discussion, the PF value has impact on v_{CRM} and v_{DCM}. By comparing Fig. A- 10 (a) and (b), the difference only exists between the 30 ° and the 40 ° operating points, which are the optimal CRM/DCM transition angle θ_T^* in these two cases, respectively. Therefore, the analysis only needs to be focused on this 10 ° line-cycle interval, since at any other operating point ZVS turn-on is naturally achieved in the phase operating at CRM at this PF condition, which is the same as under the unity PF condition and has been analyzed in previous parts.

Therefore, here by sweeping the line-cycle phase angle θ from 30 ° to 40 ° and the initial condition angle φ from 0 ° to 360 °, the numerical solutions of the control switch time-domain drain–source voltage waveform in the phase operating at CRM are derived. Considering all the possible initial condition angle φ, it is found that the natural ZVS turn-on is achieved at any operating point.

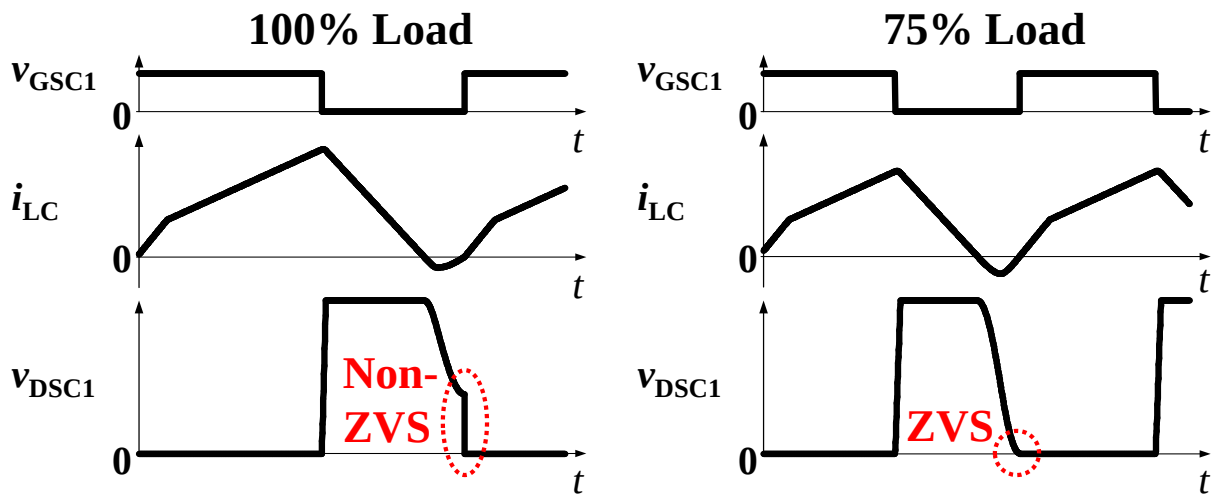
For the valley drain–source voltage turn-on in the phase operating at DCM, it is achievable by applying a short delay on the turn-on instant when compared with the turn-on instant in the phase operating at CRM as presented in previous parts. The difference is that before the 26 ° operating point when the polarities of the ac reference current are different in phase A and phase C, the valley drain–source voltage in the phase operating at DCM is usually not able to reach zero, making the DCM turn-on loss higher when compared with the unity PF condition. Example switching-cycle waveforms in this phase at 10 ° operating point and at 35 ° operating point are shown in Fig. A- 11.



(a) (b)

Fig. A- 11. Switching-cycle waveforms in the phase operating at DCM (phase A), under PF = 0.9 (ψ = 26 °) condition, at (a) 10 ° operating point with valley drain–source voltage turn-on; (b) 35 ° operating point with ZVS turn-on (v_{GS} is the gate signal of the control switch; i_L is the inductor current; v_{DS} is the drain–source voltage of the control switch).

For the other example of PF = 0.8 (ψ = 37 °), according to the optimal CRM/DCM transition angle in Fig. 3-10 and similar to the comparison shown in Fig. A- 10 for the example of PF = 0.9 (ψ = 26 °), it is clear that the analysis only needs to be focused on the 15 ° line-cycle interval between the 30 ° and the 45 ° operating points. Therefore, following the same process, it is found that after the 41 ° operating point, natural ZVS turn-on is not necessarily achieved. Example switching-cycle waveforms in the phase operating at CRM at the 44 ° operating point but under two different system load conditions (and therefore two different initial condition angle φ) are shown in Fig. A- 12.



(a) (b)

Fig. A- 12. Switching-cycle waveforms in the phase operating at CRM, under PF = 0.8 (ψ = 37 °) condition, at 44 ° operating point at (a) full-load condition with non-ZVS; (b) 75% load condition with ZVS (v_{GS} is the gate signal of the control switch; i_L is the inductor current; v_{DS} is the drain–source voltage of the control switch).

In order to achieve ZVS turn-on after the 41 ° operating point considering all the possible initial condition angle φ, the off-time extension strategy presented in [27], [36]–[39] is applied here. By making the SR in the phase operating at CRM conduct for an extra period of time after the inductor current zero crossing occurs in this phase, some amount of negative inductor current is provided to discharge the drain–source voltage of the control switch to zero and achieve ZVS turn-on. Again and according to the state-space equation, the minimum required negative current (i_{neg_req}) distribution between the 40 ° and the 45 ° operating points is shown as Fig. A- 13. Before the 40 ° operating point, the required negative current is zero, indicating off-time extension is not required during this period. It should be noted that this negative current is able to make the ZVS turn-on achieved for any load conditions (any initial condition angle φ).

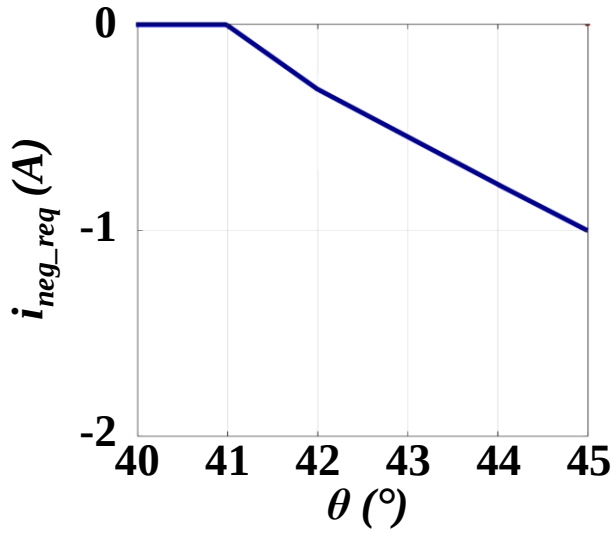


Fig. A- 13. Distribution of the minimum required negative current (i_{neg_req}) between the 40 °and the 45 °operating point for achieving ZVS turn-on under any load condition (initial condition angle φ).

As for the valley drain–source voltage turn-on in the phase operating at DCM, it is still achievable by applying a short turn-on delay when compared with the turn-on instant in the phase operating at CRM, which is similar to that at the unity PF condition in previous parts.

In summary, under the aforementioned example modulation index, for non-unity power factor inverter mode operation, under the condition with PF higher than 0.9, the natural ZVS turn-on is achieved at any operating point during CRM operation. As the PF goes lower than 0.9, the non-ZVS zone expands gradually, and, therefore, the off-time extension is required for achieving ZVS turn-on. During DCM operation, the slight turn-on delay is still helpful to achieve valley drain–source voltage turn-on in this phase. However, at the operating points when the polarity of the ac line-to-neutral voltage is opposite to that of the ac reference current, the DCM valley turn-on voltage becomes higher.

References

[1] Electrek, “Tesla quietly upgraded its Superchargers for faster charging, now capable of 145 kW,” [Online]. Available: https://electrek.co/2016/07/20/tesla-supercharger-capacity-increase-145-kw/

[2] TeslaTap, “Supercharger SuperGuide – Inside the V2 Supercharger,” [Online]. Available: https://teslatap.com/articles/supercharger-superguide/

[3] Huawei, “R75020G2 Charger User Manual V1.1,” Huawei, China. [Online]. Available: https://support.huawei.com/enterprise/en/doc/EDOC1000185247

[4] Megmeet, “Electric Vehicle Charging Module MR750-40H Series,” [Online]. Available: https://en.megmeet.com/product/lists/49/123.html.

[5] Sicon, “DPM EV Charger Module 15/20/30kW,” [Online]. Available: https://www.sicon-emi.com/dpm-ev-charger-module-15-20-30kw_p30.html.

[6] Infy Power, “30KW @1000V EV Charger Module REG1K0100G,” [Online] Available: https://www.infypower.com/30kw-1000v-ev-charger-module-reg1k0100g.html.

[7] SMA America, “Solar inverters,” SMA America, Niestetal, Germany. [Online]. Available: http://www.sma-america.com/products/solarinverters.html.

[8] Yaskawa Solectria Solar, “PV inverters,” Yaskawa Solectria Solar, Lawrence, MA, USA. [Online]. Available: https://solectria.com/pvinverters/

[9] ABB, “Solar inverters,” ABB, Zurich, Switzerland. [Online]. Available: http://new.abb.com/power-converters-inverters/solar.

[10] Sungrow, “PV inverters,” Sungrow, Hefei, China. [Online]. Available: https://www.sungrowpower.com/index.php/en/commercial.

[11] G. Deboy, R. Rupp, R. Mallwitz, and H. Ludwig, “New SiC JFET boost performance of solar inverters,” in *Proc. Power Electron. Eur.*, 2011, no. 4, pp. 29–33.

[12] J. Mookken, B. Agrawal, and J. Liu, “Efficient and compact 50 kW Gen2 SiC device based PV string inverter,” in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, Nuremberg, Germany, 2014, pp. 1–7.

[13] Y. Shi, L. Wang, R. Xie, Y. Shi, and H. Li, "A 60-kW 3-kW/kg five-level T-Type SiC PV inverter with 99.2% peak efficiency," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9144–9154, Nov. 2017.

[14] A. Anthon, Z. Zhang, M. A. E. Andersen, D. G. Holmes, B. McGrath, and C. A. Teixeira, "The benefits of SiC MOSFETs in a T-type inverter for grid-tie applications," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 2808–2821, Apr. 2017.

[15] E. Gurpinar and A. Castellazzi, "Single-phase T-type inverter performance benchmark using Si IGBTs, SiC MOSFETs, and GaN HEMTs," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7148–7160, Oct. 2016.

[16] D. M. Divan, "The resonant DC link converter—A new concept in static power conversion," *IEEE Trans. Ind. Appl.*, vol. 25, no. 2, pp. 317–325, Mar./Apr. 1989.

[17] D. M. Divan and G. Skibinski, "Zero-switching-loss inverters for highpower applications," *IEEE Trans. Ind. Appl.*, vol. 25, no. 4, pp. 634–643, Jul./Aug. 1989.

[18] R. W. De Doncker and J. P. Lyons, "The auxiliary commutated resonant pole converter," in *Proc. Conf. Record IEEE Ind. Appl. Soc. Annu. Meeting*, 1990, pp. 1228–1235.

[19] X. Yuan, G. Orglmeister, and I. Barbi, "ARCPI resonant snubber for the neutral-point-clamped inverter," *IEEE Trans. Ind. Appl.*, vol.36, no.2, pp. 586-595, Mar/Apr 2000.

[20] D. Xu, B. Feng, and R. Li, "A zero voltage switching SVM (ZVS–SVM) controlled three-phase boost rectifier," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 978–986, May 2007.

[21] Z. Ma, D. Xu, R. Li, C. Du and X. Zhang, "A Novel DC-Side Zero Voltage Switching (ZVS) Three-Phase Boost PWM Rectifier Controlled by an Improved SVM Method, " *IEEE Trans. Power Electron.*, vol.27, no.11, pp.4391-4408, Nov. 2012.

[22] R. Li and D. Xu, "A Zero-Voltage Switching Three-Phase Inverter," *IEEE Trans. Power Electron.*, vol.29, no.3, pp.1200-1210, March 2014.

[23] N. He, M. Chen, J. Wu, N. Zhu and D. Xu, "20-kW Zero-Voltage-Switching SiC-mosfet Grid Inverter With 300 kHz Switching Frequency," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5175-5190, June 2019.

[24] N. He, Y. Zhu, A. Zhao and D. Xu, "Zero-Voltage-Switching Sinusoidal Pulsewidth Modulation Method for Three-Phase Four-Wire Inverter," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7192-7205, Aug. 2019.

[25] C. DiMarino, Z. Chen, M. Danilovic, D. Boroyevich, R. Burgos, and P. Mattavelli, “High-temperature characterization and comparison of 1.2 kV SiC power MOSFETs,” in *Proc. IEEE Energy Convers. Congr. Expo.*, Denver, CO, USA, 2013, pp. 3235–3242.

[26] C. DiMarino, Z. Chen, D. Boroyevich, R. Burgos, and P. Mattavelli, “Characterization and comparison of 1.2 kV SiC power semiconductor devices,” in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Lille, France, 2013, pp. 1–10.

[27] Z. Liu, B. Li, F. C. Lee, and Q. Li, “High-efficiency high-density critical mode rectifier/inverter for WBG-device-based on-board charger,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9114–9123, Nov. 2017.

[28] J. -S. Lai and D. Chen, "Design consideration for power factor correction boost converter operating at the boundary of continuous conduction mode and discontinuous conduction mode," *Proceedings Eighth Annual Applied Power Electronics Conference and Exposition*, San Diego, CA, USA, 1993, pp. 267-273.

[29] J. Sebastian, J. A. Cobos, J. M. Lopera and U. Uceda, "The determination of the boundaries between continuous and discontinuous conduction modes in PWM DC-to-DC converters used as power factor preregulators," in *IEEE Transactions on Power Electronics*, vol. 10, no. 5, pp. 574-582, Sept. 1995.

[30] Y. Yang, Z. Liu, F. C. Lee, and Q. Li, “Multi-phase coupled and integrated inductors for critical conduction mode totem-pole PFC converter,” in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Tampa, FL, USA, 2017, pp. 1804–1809.

[31] B. Li, F. C. Lee, Q. Li, and Z. Liu, “Bi-directional on-board charger architecture and control for achieving ultra-high efficiency with wide battery voltage range,” in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Tampa, FL, USA, 2017, pp. 3688–3694.

[32] D. Zhang, Q. Zhang, H. Hu, A. Grishina, J. Shen, and I. Batarseh, “High efficiency current mode control for three-phase micro-inverters,” in *Proc. IEEE Energy Appl. Power Electron. Conf. Expo.*, Feb. 2012, pp. 892–897.

[33] D. Leuenberger, D. Christen, and J. Biela, “Triangular current mode operation of a three phase interleaved T-type inverter for photovoltaic systems,” in *Proc. Int. Conf., Power Electron., Intell. Motion Power Qual.*, Nuremberg, Germany, 2012, pp. 436–443.

[34] J. W. Kolar, H. Ertl, and F. C. Zach, “Influence of the modulation method on the conduction and switching losses of a PWM converter system,” *IEEE Trans. Ind. Appl.*, vol. 27, no. 6, pp. 1063–1075, Nov./Dec. 1991.

[35] A. M. Hava, R. J. Kerkman, and T. A. Lipo, “A high-performance generalized discontinuous PWM algorithm,” *IEEE Trans. Ind. Appl.*, vol. 34, no. 5, pp. 1059–1071, Sep./Oct. 1998.

[36] B. Su, J. Zhang, and Z. Lu, “Totem-pole boost bridgeless PFC rectifier with simple zero-current detection and full-range ZVS operating at the boundary of DCM/CCM,” *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 427–435, Feb. 2011.

[37] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, “Design of GaN-based MHz totem-pole PFC rectifier,” *IEEE J. Emerging Sel. Topics Power Electron.*, vol. 4, no. 3, pp. 799–807, Sep. 2016.

[38] Z. Liu, Z. Huang, F. C. Lee, Q. Li, and Y. Yang, “Operation analysis of digital control based MHz totem-pole PFC with GaN device,” in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl.*, Blacksburg, VA, USA, 2015, pp. 281–286.

[39] Z. Huang, Z. Liu, Q. Li, and F. C. Lee, “Microcontroller-based MHz totem-pole PFC with critical mode control,” in *Proc. IEEE Energy Convers. Congr. Expo.*, Milwaukee, WI, USA, 2016, pp. 1–8.

[40] S. Wang, “Characterization and cancellation of high-frequency parasitics for EMI filters and noise separators in power electronics applications,” Ph.D. dissertation, Virginia Polytechnic Institute and State University, Blacksburg, VA, 2005.

[41] K. Mainali and R. Oruganti, "Conducted EMI Mitigation Techniques for Switch-Mode Power Converters: A Survey," in *IEEE Transactions on Power Electronics*, vol. 25, no. 9, pp. 2344-2356, Sept. 2010.

[42] Z. Liu, Z. Huang, F. C. Lee and Q. Li, "Digital-Based Interleaving Control for GaN-Based MHz CRM Totem-Pole PFC," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 808-814, Sept. 2016.

[43] CREE Inc. “C3M0032120K *Datasheet*”, 2019. [Online]. Available: https://www.wolfspeed.com/media/downloads/1505/C3M0032120K.pdf

[44] Infineon Technologies AG, “IKW40N120H3 *Datasheet*”, 2014. [Online]. Available: https://www.infineon.com/dgdl/Infineon-IKW40N120H3-DS-v02_01-EN.pdf?fileId=db3a304325305e6d012591d4832f7032

[45] P. Kong, S. Wang, F. C. Lee and C. Wang, "Common-Mode EMI Study and Reduction Technique for the Interleaved Multichannel PFC Converter," in *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2576-2584, Sept. 2008.

[46] Y. Yang, M. Mu, Z. Liu, F. C. Lee and Q. Li, "Common mode EMI reduction technique for interleaved MHz critical mode PFC converter with coupled inductor," 2015 *IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015, pp. 233-239.

[47] H. Zhang, L. Yang, S. Wang and J. Puukko, "Common-Mode EMI Noise Modeling and Reduction With Balance Technique for Three-Level Neutral Point Clamped Topology," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 9, pp. 7563-7573, Sept. 2017.

[48] M. S. Elmore, "Input current ripple cancellation in synchronized, parallel connected critically continuous boost converters," in *Proc. IEEE Appl. Power Electron. Conf.*, 1996, pp. 152–158.

[49] M. S. Elmore and K. A. Wallace, "Zero voltage switching supplies connected in parallel." U.S. Patent 5 793 191, Aug. 11, 1998.

[50] X. Xu and A. Huang, "A novel closed loop interleaving strategy of multiphase critical mode boost PFC converters," in *Proc. IEEE Appl. Power Electron. Conf.*, 2008, pp. 1033–1038.

[51] L. Huber, B. T. Irving, and M. M. Jovanovic, "Review and stability analysis of PLL-Based interleaving control of DCM/CCM boundary boost PFC converters," in *IEEE Transactions on Power Electronics*, vol. 24, no. 8, pp. 1992–1999, Aug. 2009.

[52] J. W. Kolar, G. R. Kamath, N. Mohan, and F. C. Zach, "Self-adjusting input current ripple cancellation of coupled parallel connected hysteresis-controlled boost power factor correctors," in *Proc. IEEE Power Electron. Spec. Conf.*, 1995, pp. 164–173.

[53] T. Ishii and Y. Mizutani, "Power factor correction using interleaving technique for critical mode switching converters," in *Proc. IEEE Power Electron. Spec. Conf.*, 1998, pp. 905–910.

[54] T. Ishii and Y. Mizutani, "Variable frequency switching of synchronized interleaved switching converters," U.S. Patent 5 905 369, May 18, 1999.

[55] B. T. Irving, Y. Jang, and M. M. Jovanovic, "A comparative study of soft-switched CCM boost rectifiers and interleaved variable-frequency DCM boost rectifier," in *Proc. IEEE Appl. Power Electron. Conf.*, 2000, pp. 171–177.

[56] J. Zhang, J. Shao, P. Xu, F. C. Lee, and M. M. Jovanovic, “Evaluation of input current in the critical mode boost PFC converter for distributed power systems,” in *Proc. IEEE Appl. Power Electron Conf.*, 2001, pp. 130–136.

[57] L. Huber, B. T. Irving, and M. M. Jovanovic, “Open-loop control methods for interleaved DCM/CCM boundary boost PFC converters,” in *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1649–1657, Jul. 2008.

[58] F. C. Lee, S. Wang and Q. Li, "Next Generation of Power Supplies-Design for Manufacturability," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2020.3002857.

[59] D. Lin, P. Zhou, W. N. Fu, Z. Badics and Z. J. Cendes, "A dynamic core loss model for soft ferromagnetic and power ferrite materials in transient finite element analysis," in *IEEE Transactions on Magnetics*, vol. 40, no. 2, pp. 1318-1321, March 2004.

[60] C. P. Steinmetz, “On the law of hysteresis,” *AIEE Trans*., pp. 3–64, 1892. Reprinted under the title “A Steinmetz contribution to the ac power revolution,” introduction by J. E. Brittain, in *Proc. IEEE*, vol. 72, 196–221, Feb., 1984.

[61] Y. Su, Q. Li and F. C. Lee, "FEA modeling of the low profile coupled inductor with non-uniform flux distribution," *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2013, pp. 2416-2423.

[62] Hitachi Metal, Ltd. “Mn-Zn soft ferrite cores for high frequency power supplies MaDC-F^{TM}”, 2020. [Online]. Available: http://www.hitachi-metals.co.jp/products/elec/tel/pdf/madc-f.pdf.

[63] C. Fei, F. C. Lee and Q. Li, "A new design paradigm for GaN based LLC converter," 2017 *IEEE Southern Power Electronics Conference (SPEC)*, Puerto Varas, 2017, pp. 1-6.

[64] Y. Yang, “EMI Noise Reduction Techniques for High Frequency Power Converters,” Ph.D. dissertation, Virginia Polytechnic Institute and State University, Blacksburg, VA, 2018.

[65] B. Li, Q. Li and F. C. Lee, "A WBG based three phase 12.5 kW 500 kHz CLLC resonant converter with integrated PCB winding transformer," 2018 *IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, 2018, pp. 469-475.

[66] M. Fu, C. Fei, Y. Yang, Q. Li and F. C. Lee, "Optimal Design of Planar Magnetic Components for a Two-Stage GaN-Based DC–DC Converter," in *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3329-3338, April 2019.

[67] B. Li, Q. Li and F. C. Lee, "High-Frequency PCB Winding Transformer With Integrated Inductors for a Bi-Directional Resonant Converter," in *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6123-6135, July 2019.

[68] Z. Huang, Z. Liu, F. C. Lee and Q. Li, "Critical-Mode-Based Soft-Switching Modulation for High-Frequency Three-Phase Bidirectional AC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3888-3898, April 2019.

[69] Z. Huang, Q. Li and F. C. Lee, "Critical-Conduction-Mode-Based Soft-Switching Modulation for Three-Phase PV Inverters With Reactive Power Transfer Capability," in *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5702-5713, June 2020.