Design, Optimization, and Integration of a SiC-Based Traction Inverter with Enhanced Current Sharing for Paralleled Discrete Devices

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Dissertation submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Electrical Engineering

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August 11th, 2025
Blacksburg, Virginia

Keywords: Silicon Carbide, Traction Inverter, High-Density Integration, Paralleled Discrete Devices, TO-247 package, Current Sharing, Layout Optimization, Differential-Mode-Choke Gate Driver, Current Sensor, Active Gate Driver, Thermal Management

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Abstract

Electric vehicles (EVs) with hybrid or full electric traction drives have emerged as leading contenders for reducing exhaust emission. In the traction drive system, dc/ac inverters that spin the motor need to deliver high power, high efficiency, and high density. According to the U.S. Department of Energy (DOE) roadmap, the 2025 targets for traction inverters include achieving a power density of 100 kW/L, reducing inverter cost to $2.7/kW, reaching efficiency of 98 %, and supporting voltage of 800 V.

To meet these aggressive targets, this dissertation first investigates one of the critical challenges in high-power inverters: current sharing among paralleled devices. In Chapter 2, the current-sharing mechanisms are comprehensively analyzed, and mathematical models are developed to describe both dynamic and static sharing. These models enable clear identification of key impact parameters, providing practical layout guidelines for designers.

Building upon the current sharing analysis, Chapter 3 explores passive current-balancing methods to improve both static and dynamic current sharing. The layout for paralleled devices is first optimized by categorizing and comparing different layout types with a focus on minimizing parasitic loop inductance L_{loop} and overlapping capacitance C. Then, a novel distributed-block (DB) layout concept is proposed to improve current sharing by mitigating asymmetric parasitic among paralleled traces. Furthermore, the differential-mode-choke (DMC) gate driver is introduced to enhance the dynamic current sharing without impairing power loop and switching performance.

While passive methods are effective for layout-induced current imbalance, they remain limited when device mismatch is significant. To address this, Chapter 4 proposes an active gate driver

(AGD) solution. A low-cost and compact *di/dt*-RC current sensing technique is introduced, along with a novel R_K sensing structure to improve sensing accuracy. The proposed R_K sensing structure requires only three tiny components (2 resistors and 1 capacitor) per MOSFET and can be easily scaled for more paralleled devices, making it highly advantageous for industrial applications. Leveraging this sensing technique, the AGD is developed to balance dynamic currents among paralleled devices, offering a near-perfect balancing performance regardless of imbalance cause.

Beyond device-level current balancing, achieving high power density for traction inverters remains challenging in both academia and commercial EVs, and requires system-level circuit and mechanical integration. Chapter 5 proposes a systematic "single-board" integration strategy, and an all-in-one half-bridge (HB) printed circuit board (PCB) is built to demonstrate the proposed strategy. This design not only simplifies integration but also eliminates the constraints of conventional "sandwich" structures, achieving a power density of 101.7 kW/L. A comprehensive experimental evaluation of designed all-in-one HB PCB is also performed.

Finally, Chapter 6 addresses the thermal challenges of high-density inverters, which become more and more critical as both power and density increase. A systematic thermal design methodology is proposed for high-density inverters and is validated using two prototypes: a 200 kW multi-level inverter in harsh high-altitude environment and a 200 kW traction inverter using the all-in-one HB PCB. Results reveal that conventional sandwich structures create stagnating air spaces that degrade cooling performance and generate localized hot spots. By contrast, the proposed single-board approach eliminates these thermal bottlenecks and enables robust heat dissipation.

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General Audience Abstract

Electric vehicles (EVs) with hybrid or full electric traction drives have emerged as leading contenders for reducing exhaust emission. In the traction drive system, most important component is the traction inverter, a device that converts electricity from the battery into power for the motor. To make EVs more affordable, efficient, and compact, traction inverters need to deliver very high power in a small space while keeping costs low and performance reliable.

This dissertation focuses on designing and improving the high-power inverter to achieve smaller size and more efficient. In high-power inverters, paralleling devices is a necessary approach to increase the inverter power, and to ensure balanced current sharing among devices is a critical challenge. To solve this, Chapter 2 studies the mechanisms of current sharing behavior, identifies key impact parameters, and provides the practical layout guidelines for paralleled devices.

To balance the current, Chapter 3 and Chapter 4 explores and develops current-balancing solutions, including improved circuit layout, adding extra components, and smart control techniques. These methods significantly improve the current sharing performance of paralleled devices, thereby enhancing reliability and safety of the traction inverters.

Beyond component-level current balancing, this dissertation also proposes new ways to integrate the inverter system. Instead of using traditional “sandwich” structures, Chapter 5 proposes a “single-board” integration strategy which simplifies the construction, increases power density beyond the U.S. Department of Energy (DOE) 2025 target, and reduces thermal bottleneck.

Finally, Chapter 6 addresses the thermal challenges of high-density inverters, which become more

and more critical as both power and density increase. A systematic thermal design methodology is proposed to help traction inverters stay cool even when operating in a harsh environment. Moreover, the thermal designs of inverter prototypes are presented to demonstrate the effectiveness and feasibility of proposed methodology.

Together, these contributions make traction inverters more compact, efficient, and robust. The findings in this dissertation provide practical solutions that can help improve the range and performance of EVs.

Dedicated to My Family:

My parents, Tzu-Hsien Chang and Hsiu-Hua Chiu

父母：張次賢，邱秀華

My brother, Che-Kang Chang

兄弟：張哲綱

My wife, Woonjung Hong

妻子：홍운정（洪雲貞）

My baby girl, Yuna Chang

女兒：張瑜娜（장유나）

Acknowledgement

First and foremost, I would like to express my sincere gratitude to my advisor, Dr. Dong Dong, for his continuous guidance, patience, encouragement, and support throughout my research work and time at the Center for Power Electronics Systems (CPES). From him, I learned to think analytically, tackle new challenges, and become a qualified doctoral researcher. I truly value the weekly discussions with him, as his insightful suggestions and experiences have been invaluable to my project work, research, and life lessons.

I am also very grateful to my committee members: Dr. Rolando Burgos and Dr. Christina DiMarino for their guidance on projects and providing a great research environment at CPES, and to Dr. G.Q. Lu, and Dr. von Spakovsky for their thoughtful comments and valuable suggestions during the preliminary examination and final defense.

Looking back, I have enormous gratitude to Dr. Yaow-Ming Chen from National Taipei University, who introduced me to the field of power electronics and encouraged me to pursue a doctoral degree. I would also like to thank Dr. Ching-Jan Chen and Dr. Katherine Kim who helped make my journey at CPES possible.

I would like to thank other CPES faculty for their support in every aspect: Dr. Fred Lee, Dr. Dushan Boroyevich, Dr. Khai Ngo, Dr. Richard Zhang, Dr. Qiang Li, Dr. Yuhao Zhang, Dr. Boran Fan, Dr. Bo Wen, Dr. Yi-Hsun Hsieh, Dr. Liyan Zhu, and Dr. Vladimir Mitrovic. I am also grateful to the amazing staff in CPES: Ms. Yan Sun, Ms. Ling Li, Ms. Audri Cunningham, Mr. David Gilham, Mr. Neil Croy, Mr. Dennis Grove, Ms. Brandy Grim, Ms. Teresa Shaw, Ms. Trish Rose, Mr. Matthew Scanland, and Mr. Brad Welch. Their dedication makes CPES a lovely place to work.

I would like to thank all my friends and colleagues who helped me along the way: Dr. Jian Liu, Dr. Yuliang Cao, and Dr. Tianlong Yuan, for their priceless help and support in both research and life; Dr. Xingchen Zhao and Dr. Ripun Phukan for their wonderful leadership and precious teamwork spirit in the Airbus project; Mr. Matthias Spieler for his generous help and support in the General Motors project; Dr. Qing Lin, Ms. Ning Yan, Ms. Biqi Wang, Ms. Yan Liang, Mr.

Tien-Sheng Li, Mr. Che-An Cheng, Mr. Boping Jiang, Mr. Xipei Yu, Mr. Zhangwei Xiang, Mr. Yijie Bai, Mr. Keyue Shan, Mr. Junming Liang, Dr. Xiang Lin, Dr. Joshua Stewart, Mr. David Nam, Dr. Feng Jin, Mr. Minh Ngo, Dr. Lakshmi Ravi, Dr. Jayesh Kumar Motwani, Mr. Jeet Panchal, Mr. Abhinav Soni, Mr. Mingze Gao, Dr. Mark Cairnie, Dr. Gibong Son, Dr. Shuo Wang, Dr. Xin Lou, Dr. Zheqing Li, Mr. Yizhi Ruan, Mr. Pranav Raj Prakash, Mr. Adhistira Naradhipa, Mr. Arthur Mendes, Mr. Ashkan Barzkar, Mr. Qiuzhe Yang, Mr. Tyler McGrew, Dr. Slavko Mocevic, Dr. Joseph Koazk, Ms. Tianyu Zhao, Dr. Cong Tu, Dr. Ruizhe Zhang, Dr. Boyan Wang, Dr. Qihao Song, Dr. Yifan Wang, Ms. Bixuan Wang, Dr. Yu Chen, Dr. Cao Zhan, Dr. Jingcun Liu, and many others to name. I have learnt so much from all of you, and we have shared so many wonderful moments together. I feel so lucky to have you as my colleagues and friends.

Special thanks to Airbus, U.S. Department of Energy (DOE), General Motors, Cummins, and RCT Systems for funding my research.

There are no words to fully describe my deep deep deep gratitude to my parents, Mr. Tzu-Hsien Chang and Ms. Hsiu-Hua Chiu, for their endless love, support, trust, and encouragement, and to my brother, Mr. Che-Kang Chang, for his continuous help and care. This milestone is dedicated to them, as I wouldn't have accomplished it without them, thank you.

I would also like to thank my wife, Woonjung Hong, a Ph.D. candidate at CPES, for her continuous love and support. Meeting you has been the luckiest blessing of my life. Thank you for being by my side all the time, and for the most precious gift, our beautiful daughter, Yuna Chang.

Finally, thank you, Che-Wei, for not giving up.

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List of Abbreviations

2L	Two-level
3L	Three-level
AD	Air duct
AD-IV	AD with internal vanes
AD-IVB	AD with internal vanes and air blocks
AD-O	Original AD
AGD	Active gate driver
AMC	Active Miller clamp
AMR	anisotropic magnetoresistance
B2B	Back-to-back
CFD	Computational fluid dynamics
CGD	Conventional gate driver
CMC	Common-mode-choke
CS	Common source
D	Drain
DB	Distributed block
DBC	Direct bond copper
DMC	Differential-mode-choke
DOE	Department of Energy
DPT	Double pulse test
DUT	Device under test
EV	Electric vehicle
FEA	finite element analysis
G	Gate
GaN	Gallium nitride
GD	Gate driver
HB	Half-bridge

Hipot	High potential
HS	High-side
IC	Integrated circuit
IGBT	Insulated gate bipolar transistor
KS	Kelvin-source
LS	Low-side
MEA	More electric aircraft
MLC	Microchannel liquid cooling
MOSFET	Metal-oxide-semiconductor field-effect transistors
NTC	Negative temperature coefficient
PCB	Printed circuit board
PD	Partial discharge
PDIV	PD inception voltage
PTC	Positive temperature coefficient
PWM	pulse width modulation
S	Source
Si	Silicon
SiC	Silicon carbide
SMD	Surface mounted device
SPWM	Sinusoidal-PWM
TIM	Thermal interface material
TNPC	T-type neutral-point-clamp
VD	Volume density
VSI	Voltage source inverter
WBG	Wide-bandgap
WD	Weight density

Chapter 1

Introduction

1.1. Trend and Targets for Traction Inverters in Electric Vehicles (EVs)

Electric vehicles (EVs) with hybrid or full electric traction drives have emerged as leading contenders for reducing exhaust emissions [1]. Comparing to vehicles with conventional combustion engines, EVs are more environmentally friendly, have lower running costs, produce less noise pollution, and offer smoother operation. As shown in Fig. 1-1, a typical dc/ac traction system uses a traction inverter to convert dc voltage from the battery into ac current to power and spin the motor. For commercial EVs, these dc/ac traction inverters need to deliver high efficiency and high power density to save on system cost and space. The U.S. Department of Energy (DOE) roadmap outlines specific targets for traction inverter for 2025 [2], which includes:

- Supporting an 800 V dc-link voltage. A higher baseline dc-link voltage improves power transfer efficiency, allows lighter power cables, reduces heat generation, and enables more compact high-power designs.
- Achieving efficiency of 98 %. The efficiency goal can be met by implementing wide-bandgap (WBG) devices like silicon carbide (SiC) or gallium nitride (GaN) devices, offering smaller die, faster switching, lower losses, and better high-temperature performance when compared to conventional silicon (Si)-based counterparts, which ultimately enabling compact and cheaper inverters.
- Reaching a power density of at least 100 kW/L. This target necessitates integrating all major components within an inverter as shown in Fig. 1-1, such as dc-link capacitors, power devices, gate drivers, current sensors, and cold plate, into a smaller volume which improves EV range and performance.
- Reducing inverter cost to $2.7/kW, which makes the EVs more affordable for general consumers and further helps reduce global gas emissions.

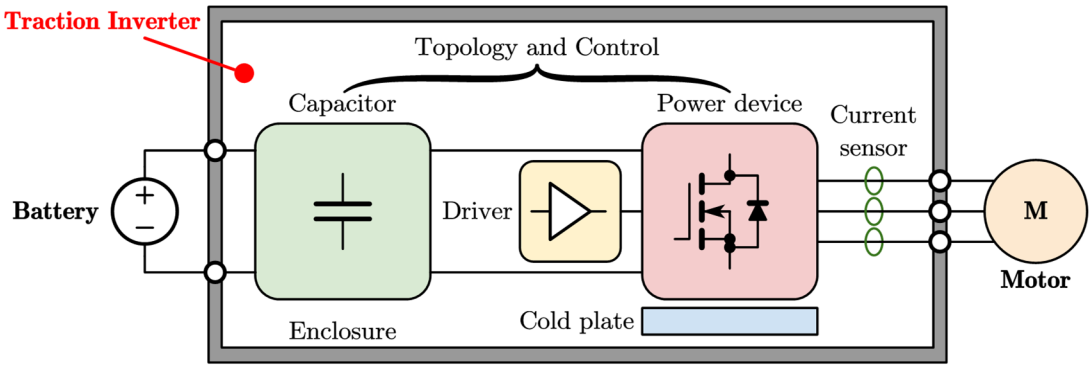


Fig. 1-1 The typical configuration of dc/ac traction system with major components within traction inverter.

These ambitious goals highlight the need for higher power capability, compact inverter designs, advanced semiconductor technologies, and efficient thermal management.

Recent trend in commercial traction inverters of EVs shows a clear shift toward these targets, as shown in Fig. 1-2 and summarized in Table 1-1. From 2010 to 2025, these traction inverters experience a rise in power rating from around 100 kW to 450 kW, an increase in dc-link voltage from 400 V to 800 V, a growth in power density from around 10 kW/L to 30 kW/L, as well as a shift from Si to SiC devices to meet the 2025 roadmap goals. Moreover, most EVs adopt the topology of two-level (2L) voltage source inverter (VSI) due to its low cost, less complexity, compact, and high reliability [3]. The hard-switching 2L VSI with switching frequency f_{sw} lower than 20 kHz dominates the commercial EV market [4].

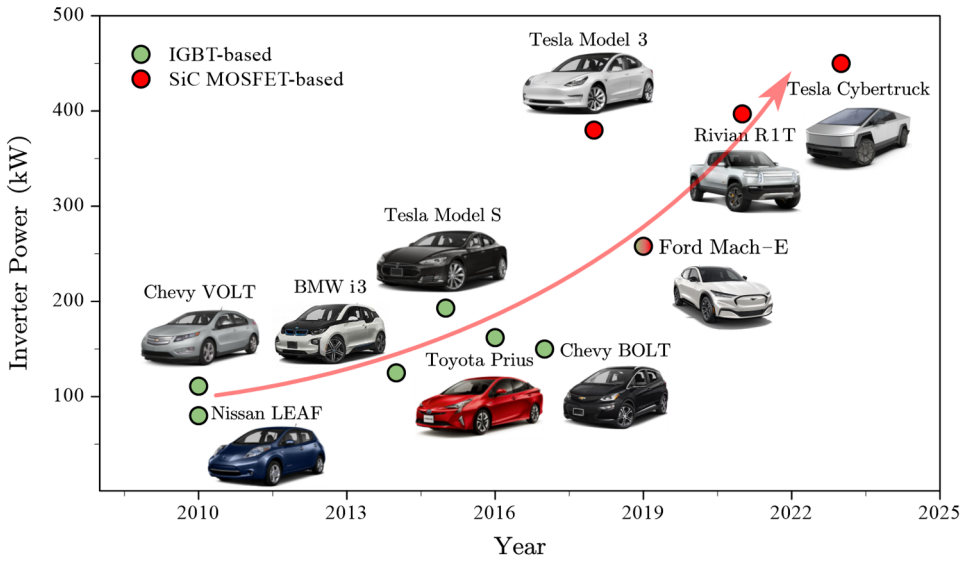


Fig. 1-2 From 2010 to 2025, trend in traction inverters of commercial EVs.

TABLE 1-1 COMPARISON OF TRACTION INVERTERS IN COMMERCIAL EVS

EV model	Topology	Rated Power	dc Voltage	Phase Current	Power Density	Power Devices
2010 Chevy VOLT [5, 6]	2L VSI	111 kW	360 V	150 Arms	10.7 kW/L	Si IGBT module
2010 Nissan LEAF [7]	2L VSI	80 kVA	240 V	340 Arms (max)	7.1 kW/L	Si IGBT module
2015 Tesla Model S [8-11]	2L VSI	193 kVA	350 V	-	30.1 kVA/L	Si IGBT discrete
2014 BMW i3 [2]	2L VSI	125 kW	360 V	210 Arms	18.5 kW/L	Si IGBT module
2016 Toyota Prius [1, 12, 13]	2L VSI	162 kVA	200 - 600 V	180 Arms	23.7 kVA/L	Si IGBT module
2017 Chevy BOLT [14-16]	2L VSI	150 kW	350 V	184 Arms	19.6 kW/L	Si IGBT module
2018 Tesla Model 3 [17, 18]	2L VSI	380 kW	400 V	-	27.4 kW/L	SiC MOSFET discrete
2019 Ford Mach-E [19]	2L VSI	258 kW	380 V	-	-	Si IGBT & SiC MOSFET modules
2021 Rivian R1T [20]	B2B 2L VSI	397 kW	440 V	-	-	SiC MOSFET module
2023 Tesla Cybertruck	2L VSI	450 kW	800 V	-	-	SiC MOSFET discrete

For the first target related to dc-link voltage, the EVs like 2019 Porsche Taycan, 2022 GMC Hummer EV, or 2023 Tesla Cybertruck, have implemented 800 V dc bus voltage platform to power their traction inverters. Moreover, several manufacturers, including Valeo [21], Eaton [22], BorgWarner [23], and Semikron Danfoss [24], have successfully demonstrated commercial inverters that support 800 V to 950 V dc-link voltage with power rating up to 500 kW. To date, the widespread adoption of 800 V system is in progress and being heavily invested in, and will become more common and accessible in the coming years.

The efficiency target can be achieved by using WBG devices like SiC or GaN semiconductors which offer promising performance for power electronics. Combining with advanced technologies of modulation schemes [25, 26], topologies [27-29], modeling and control [30-37], device packaging [38, 39], gate driver designs [40-42], sensors [43-46], thermal management [47, 48], and inductor technologies [49-60], the inverters can achieve compact and high-efficiency. In older EV models from 2010 to 2017, the Si-based insulated gate bipolar transistor (IGBT) devices have been widely adopted due to their low cost and robust performance. However, they suffer from high switching losses, low switching speed, and performance drop above 125 ^{o}C, which limit efficiency and increase cooling requirements especially when facing the rise in power rating of traction drive system. The 2018 Telsa Model 3 long-range variant became the first EV with full SiC traction inverter in mass production, using paralleled 650 V discrete SiC metal-oxide-semiconductor field-

effect transistors (MOSFET) from STMicroelectonics. The SiC MOSFET features faster switching, lower losses, and better thermal resistance, enabling more compact, lighter, and more efficient inverter design [61-63]. Moreover, the Tesla inverter is integrated with the gearbox and motor, eliminating the need for bulky power cables. Tesla Model 3 marked a shift toward compact and efficient inverters, followed by 2019 Ford Mach-E (rear inverter), 2021 Rivian R1T, and 2023 Tesla Cybertruck. In general, the peak efficiencies of SiC-based inverters are typically around 98 – 99 %. To further extend the efficiency boundary, GaN devices have been recently implemented in some inverters with power rating up to 100 kW [64-67], achieving efficiencies beyond 99 %. By employing WBG devices, the challenges associated with efficiency target are effectively addressed.

However, meeting the DOE's targets for low-cost, high-power, and high-density requires overcoming several key design challenges which can be described as follows.

1) **Device level**: While enjoying the benefits and superiorities of SiC MOSFETs to reach high efficiency, the active area of a single die is restricted by low yield rate, thereby limiting the current rating of a single device [68-70]. Therefore, as the demand for higher power ratings continues to rise, paralleling the SiC MOSFETs is a popular and cost-effective solution to enhance current-carrying capability, regardless of the device packages [71]. Fig. 1-3 shows examples in commercial applications. In Fig. 1-3(a), Tesla Model 3 inverter paralleled the SiC MOSFETs in discrete TO-247-like package. in Fig. 1-3(b), the Chevy BOLT inverter employed a six-pack power module with paralleled dies inside the module. In Fig. 1-3(c), Infineon demonstrated the paralleled power modules in their traction design. These examples highlight industry's reliance on paralleled devices, whether through discrete devices or integrated power modules. Paralleling devices is a practical approach for achieving the current capacity required in modern high-power traction inverters.

Despite being a practical solution, paralleling devices introduces a critical problem: unbalanced current sharing. Fig. 1-4 presents an experimental example waveform of current sharing among four paralleled SiC MOSFETs, where i_D is the channel or drain current of each device. Obviously, the currents are extremely unbalanced, especially during the switching turn-on transient. Such current sharing imbalance can lead to a range of problems, including uneven losses [72], current overshoot [73, 74], gate voltage oscillation [75], unequal junction temperatures, and in some severe

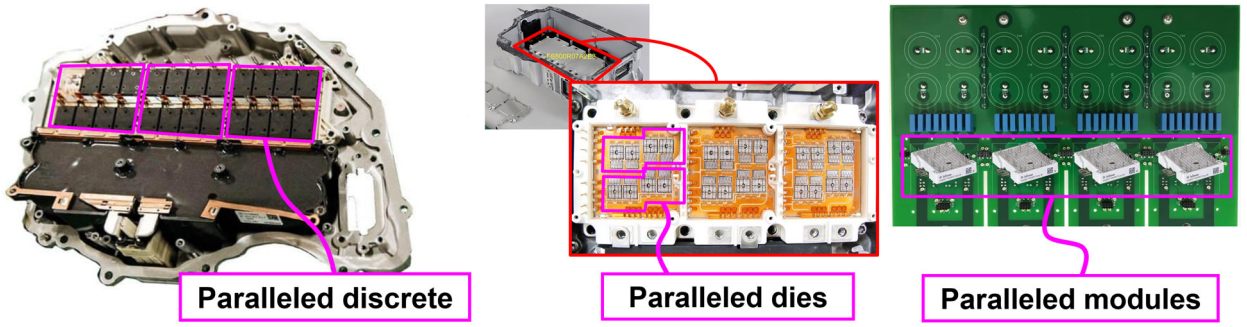


Fig. 1-3 Industry examples of paralleled devices (a) paralleled discrete devices in Tesla Model 3 traction inverter, (b) paralleled dies in power modules for Chevy BOLT traction inverter, and (c) paralleled power modules in Infineon's traction design.

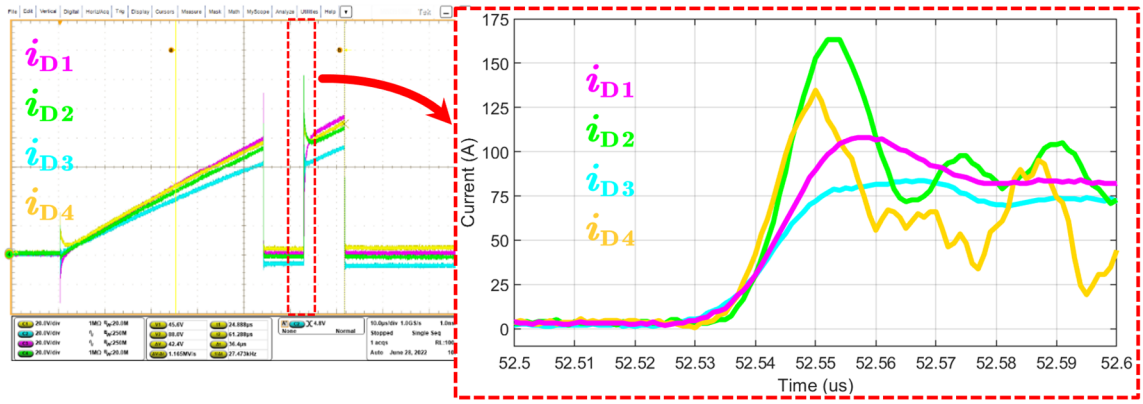


Fig. 1-4 Experimental waveform example of unbalanced current sharing among four paralleled devices.

cases, thermal runaway [76, 77], introducing reliability and performance concerns that must be carefully managed via current sharing analysis, current-balancing solutions, and circuit design.

2) **System level**: The drive to achieve a power density of 100 kW/L requires a highly compact inverter design. Compactness is not only necessary for meeting power density goal but also fundamentally reduces the total material cost. However, most inverter designs in both commercial EVs and academic literature struggle to meet power density target. As shown in Table 1-1, state-of-the-art commercial inverters rarely exceed 30 kW/L, underscoring the significant gap between current practices and DOE targets.

Moreover, the cost target must be achieved in tandem with power density target, as simply selecting the cheapest components is not an optimal solution here. Instead, the inverters can still achieve low total cost by incorporating advanced components and innovative technologies that enable reduced inverter volume, thereby reduces the material cost even if individual components are more expensive. These considerations highlight the importance of systematic integration

strategies that ensure economic viability while meeting the power density goal.

3) **Thermal management**: As inverter volume shrinks in pursuit of high power density, the resulting challenge of thermal management becomes more pronounced. The reduction in inverter volume directly increases the system heat flux which necessitates efficient and integrated cooling solutions. After all, optimal electrical design can only be achieved when supported by strong thermal performance, as excessive temperature rise impacts device efficiency, reliability, and component lifetime. Addressing thermal challenges is essential to fully realize the benefits of SiC-based traction inverters and to meet DOE's aggressive 2025 roadmap targets.

1.2. Challenges in High-Power High-Density Inverters with Paralleled Devices

1.2.1 Limitation of Existing Current Sharing Models and Layout Guidelines

Before addressing the issue of current imbalance among paralleled devices, it is crucial to first understand the current sharing mechanism and the key impact parameters. Previous works in the literature have primarily focused on experimental investigations to study current sharing behavior. For instance, work [74] studied dynamic current sharing through experiments, finding that the use of Kelvin-source (KS) can improve current sharing performance. In [76], the impact of parasitic on both static and dynamic current sharing were explored, providing some mathematical insights. It was concluded that dynamic current sharing is particularly vulnerable to the mismatched power source parasitic inductance, and the mechanism of dynamic current sharing was uncovered in [78]. The impact of mutual inductance on current sharing was further studied in [79].

Although the above research presented valuable contributions, their models remain qualitative, overly complex to interpret, and some conclusions for layout guidelines are misleading which require refinement. As a result, they provide limited utility for parasitic study or practical implementation. To enable quantitative comparison and more rigorous analysis, accurate mathematical models are needed. Such models can serve as a foundation for establishing layout guidelines and developing current-balancing solutions to improve current sharing performance.

1.2.2 Drawbacks of Existing Current-Balancing Solutions

Current-balancing solutions for paralleled devices are now an active research area. In general, approaches to balance the currents can be categorized into passive methods or active solutions.

Passive solutions like modifying the layout structure can enhance current sharing. For example, research [80] has indicated that the paralleling half-bridges (HB) is more effective in balancing dynamic currents compared to paralleling dies directly. Building on this concept, cutouts have been made on the printed circuit board (PCB) to facilitate better current sharing among paralleled discrete devices in TO-247 package [81]. However, such modifications come with a trade-off, resulting in increased commutation loop inductance L_{loop}. In power modules, [72] adjusted the length and location of power source bonding wires to compensate the mismatched inductances, though this technique is limited to the die level. Other studies introduced innovative layout structures, such as double-ended terminals [82] or common source compensation [73], but these approaches complicate gate-driving routing.

Another passive strategy involves adding extra components. In [83], ceramic decoupling capacitors are placed closer to the devices to achieve both balanced currents and small L_{loop}, though this approach requires meticulous design for the ceramic decoupling capacitors, and the devices must be arranged in a specific pattern to maintain clearance which inevitably increases the footprint area. Work [78] inserted a snubber circuit into the power loop to alleviate unbalanced currents. Yet, this solution demands complex frequency domain calculations and careful placement of the snubber circuit. In [84-86], differential mode chokes (DMC) were placed into the drain-source power loop to balance the currents. Similarly, a coupled inductor was added to the power source path to mitigate unbalanced dynamic currents [87]. However, these methods increase L_{loop} which causes high overshoot voltage on power devices. Moreover, the inductors must be capable of carrying power currents, inevitably yielding issues of cost, volume, and thermal challenge.

Active solutions actively control the switching of power devices to achieve balanced current. Recent research efforts have been focused on developing active gate driver (AGD) techniques. The AGD proposed in [88] adjusted both applied driving voltage and turn-on/off timings to balance the dynamic currents. However, this solution requires a dedicated controller and communication circuitry for each MOSFET which substantially increases the total cost and system

complexity. A study [89] introduced an alternative transistor-based AGD for dynamic current sharing. Two added circuits, facilitating gate current injection/extraction, were connected to the MOSFETs' gates and triggered by voltage drops across power source inductances. This method is particularly effective in scenarios where device mismatch occurs, however, even slight differences in power loop layout could degrade the AGD performance. In [90], a digital-based AGD design was presented to balance both static and dynamic currents. Yet, the signal-delay control is unable to compensate unbalanced dynamic currents entirely, and gate voltage control for static current balancing results in increased conduction losses.

A key challenge of active methods lies in dynamic current sensing during fast switching transients. Since AGD reacts according to the information provided by the current sensors, accuracy and bandwidth are critical. While these sensors need not restore the dynamic currents perfectly, they must provide correct information on current imbalances. In [90], dedicated current transformers were used to sense the currents in paralleled devices, requiring large magnetizing inductance and bulky transformer which makes it impractical for paralleled devices. Rogowski coils [43, 46, 91] offer high bandwidth but add cost, size, and design complexity. The conventional shunt resistor suffers from obvious disadvantages such as extra losses and higher L_{loop} [92]. In [93], an additional current sensing MOSFET was introduced in paralleled with the main power MOSFET. The main challenges with this approach include poor low-current accuracy and strong temperature dependence. Leveraging parasitic elements that in series with power current path for sensing provides low-cost integration since these elements are inherent in all conductive parts without needing extra sensors. In [94], both parasitic resistance and inductance were used to sense switching current. However, the complicated design and temperature-dependent parasitic resistance limit its applicability. Research [95] proposed an adaptive method to dynamically compensate the undesired effect of temperature-dependent parasitic resistance, achieving high accuracy in sensing both dynamic and static currents. The compensation circuit, though, can be costly when implementing it for paralleled devices.

In summary, the passive solutions proposed in the literature have drawbacks of increased L_{loop} and addition components into power loop, yielding reliability, thermal, and practicality concerns for high-power applications. On the other hand, existing AGDs face challenges of inefficient balancing strategies, dependence on multiple controllers, and complex current sensing techniques, ultimately increasing system size, cost, and design difficulty.

1.2.3 Barriers to Achieving High Power Density

As mentioned earlier, commercial EV traction inverters rarely exceed 30 kW/L, showing a significant gap between current practices and DOE's power density target. Similar bottleneck exists in the academia. Fig. 1-5 shows the state-of-the-art inverter designs reported in recent publications [27, 64, 96, 97], adopting different topologies, power devices, dc-link capacitors, PCB busbars, cooling techniques, and driver designs.

In [96], a compact SiC-based 2L inverter with heat pipe and microchannel liquid cooling (MLC) techniques was presented, achieving a power density of 34 kW/L. Papers [27] and [97] conducted weight-optimizations for propulsion inverters, and three-level (3L) T-type neutral-point-clamped (TNPC) and back-to-back (B2B) 2L are adopted to reduce EMI filters and dc-link capacitors weight. More recently, a GaN-based traction inverter was presented in [64], conducted volume-optimizations for power devices, capacitors, and cold plate. However, while these works presented high-quality trade-off analyses and component-level optimizations, none of them exceeded 100 kW/L. Even another work [98] reported a power density of 86 kVA/L (111 kVA/L if excluding enclosure), their inverter design did not evaluate the thermal performance. This omission raises concerns as their design should require larger and thicker component size and advanced cooling to manage heat, especially in high-current PCB-based busbars and regions with poor airflow beneath gate driver boards.

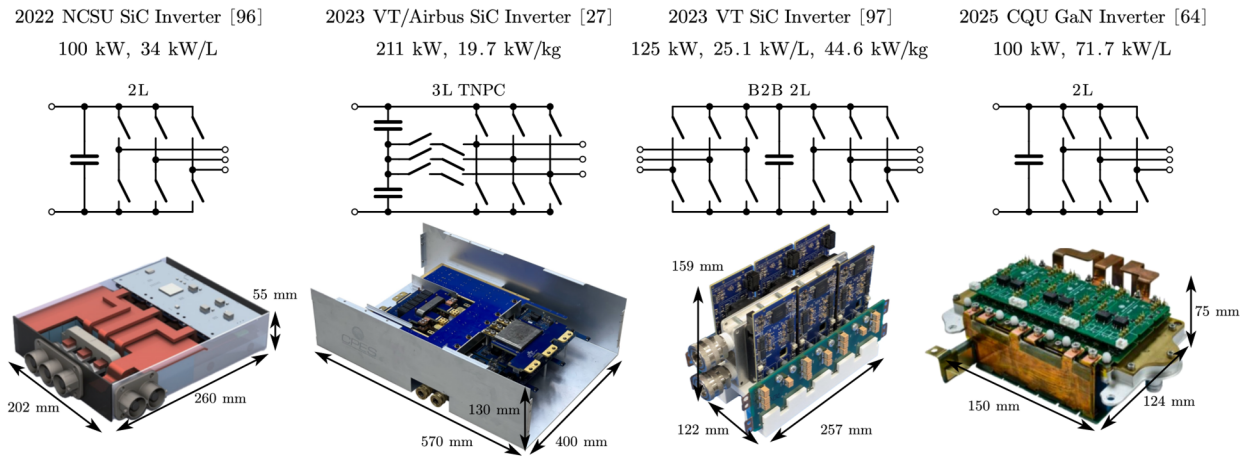


Fig. 1-5 State-of-the-art inverter designs in recent publications. Despite component-level optimizations have been conducted for these power inverters, their power densities are all lower than DOE's target of 100 kW/L.

1.2.4 Lack of Systematic Design Process for Thermal Management

Three decades ago, a common myth existed in industry was that the thermal design was usually an afterthought, addressed only when problems arose [99]. As power electronics technology has advanced over the years, this misconception has faded, and thermal design is usually prioritized due to its significant impact on system cost. Today, as high-power inverters are required to meet higher power density, thermal challenges increasingly arise due to sharply elevated heat flux. The thermal issues can lead to system failures like component cracks, solder joint fatigue, and wire lift-offs [100, 101]. Moreover, for inverters operating in harsh environments under high ambient temperature or high-altitude conditions, thermal management becomes more challenging because of stricter buffer for temperature rise and lower air density [102-105]. Additionally, as demonstrated by examples in Fig. 1-5, multi-board structures of power inverters often create localized hot-spots, leading to detrimental impact on lifetime and reliability. These challenges underscore the urgent need for a systematic thermal design methodology, which is currently absent in the literature.

1.3. Dissertation Outline

Chapter 1 introduces the research background and motivation, highlighting the main challenges in achieving low-cost, high-power, and high-density traction inverters.

Chapter 2 presents the modeling and analysis of current sharing among paralleled SiC MOSFETs, enabling quantitative comparisons. The derived models allow for more straightforward study of parameter impacts, guidelines of practical layout circuit design, and exploration of current-balancing solutions.

Chapter 3 investigates two low-cost passive current-balancing solutions guided by the models derived in Chapter 2. These solutions are demonstrated by paralleled discrete SiC MOSFETs in TO-247 packages. A novel distributed-block (DB) layout concept is first proposed to optimize electrical performance and improve current sharing. Then, the dynamic current sharing is further enhanced by implementing DMC gate driver.

Chapter 4 develops a single-controller AGD solution for near-perfect current balancing,

regardless of root causes of current imbalance. To accurately sense the dynamic currents, *di/dt*-RC sensing method with novel R_K sensing structure is proposed and implemented.

Chapter 5 reviews state-of-the-art inverter designs and proposes a systematic integration strategy to meet power density target of 100 kW/L. To demonstrate the proposed strategy, an all-in-one HB PCB is designed, incorporating the proposed passive current-balancing solutions to enhance current sharing among paralleled devices. Furthermore, a 200 kW three-phase inverter is built, verifying the proposed integration strategy.

Chapter 6 proposes a systematic methodology for thermal management to tackle the thermal challenges in high-power high-density inverters. Comprehensive thermal modeling, thermal mitigation strategies, cooling path configurations, optimization of cooling devices, and impact of stagnating air space are presented. To demonstrate the feasibility and thoroughness of proposed methodology, thermal designs are presented for a high-altitude multi-level SiC-based inverter, which poses more challenging thermal issues than a sea-level 2L traction inverter.

Chapter 7 concludes this dissertation and discusses future work.

Chapter 2

Current Sharing Analysis and Modeling

2.1. Introduction to Current Sharing: Factors and Regions

As introduced in Chapter 1, paralleling SiC MOSFETs is a popular and cost-effective method to augment the current-carrying capability regardless of device packages. Before exploring current-balancing solutions to address unbalanced currents, it is essential to first understand current sharing mechanisms and identifying key impact parameters. Fig. 2-1 illustrates a double pulse test (DPT) circuit with two paralleled SiC MOSFETs, LS1 and LS2, placed at the low-side (LS) switching position, and the typical switching waveforms of SiC MOSFET are shown in Fig. 2-2. In this specific circuit, the high-side (HS) devices can be substituted with diodes since they remain in off-state [106]. All relevant parameters are listed in Table 2-1.

Current sharing can be affected by two main factors, using Fig. 2-1 as an example:

- Asymmetric layout: The asymmetric layout parasitic resistances R or inductances L create unequal impedances between the paralleled device branches, resulting in current imbalance.
- Mismatched devices: The mismatched characteristics between paralleled devices, LS1 and LS2, can lead to unbalanced current sharing due to differences in turn-on/off timings and current rising/falling rates.

On the other hand, current sharing issue typically occurs in two main regions based on Fig. 2-2:

- Dynamic region: It refers to the switching transients when SiC MOSFET is turning on and start conducting i_D after gate-source voltage v_{GS} reaches threshold voltage V_{th}, or turning off as i_D start decreasing and reaches 0 A when v_{GS} reaches V_{th}.
- Static region: When SiC MOSFET conducts continuous steady-state current, the v_{GS}, i_D, and drain-source voltage v_{DS} remain nearly constant.

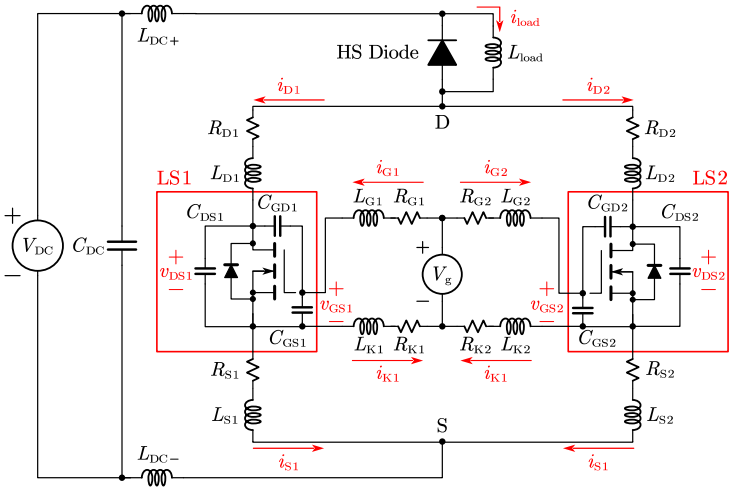


Fig. 2-1 DPT circuit of paralleled SiC MOSFETs at LS position.

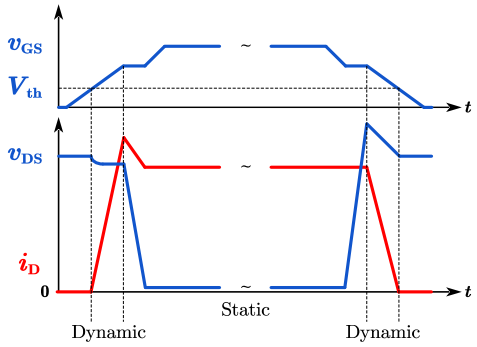


Fig. 2-2 Switching waveforms of SiC MOSFET.

TABLE 2-1 KEY PARAMETERS IN FIG. 2-1

Symbols	Parameters
V_{DC}	Dc-link voltage
C_{DC}	Dc-link capacitance
V_g	Gate driving voltage
R_{G1}, R_{G2}	Gate resistance
L_{DC+}, L_{DC-}	Parasitic inductance between C_{DC} and HB circuit
L_{load}	Load inductor
L_{D1}, L_{D2}	Drain parasitic inductance
L_{S1}, L_{S2}	Source parasitic inductance
L_{G1}, L_{G2}	Gate parasitic inductance
L_{K1}, L_{K2}	KS parasitic inductance
C_{DS1}, C_{DS2}	Drain-source capacitance
C_{GS1}, C_{GS2}	Gate-source capacitance
C_{GD1}, C_{GD2}	Gate-drain capacitance

It's worth noting that the SiC MOSFET's V_{th} displays a negative temperature coefficient (NTC) behavior [107], forcing the device with lower V_{th} to bear more dynamic current. During the continuous operation of SiC MOSFET, the positive temperature coefficient (PTC) of drain-source resistance $R_{DS,on}$ may help recover the V_{th} from getting lower and lower over cycles. However, it is found that the occurrence of thermal runaway depends on the switching frequency and current level [76, 77]. If the switching frequency is too high such that the PTC of $R_{DS,on}$ cannot offset the NTC of V_{th}, thermal runaway may occur. Furthermore, the decreasing V_{th} increases the likelihood of shoot-through event due to crosstalk. Eventually, the devices may fail earlier than expected lifetime and consequently reduce system stability. Since device consistency is largely determined by manufacturing capability and technology, it is necessary to characterize devices from different vendors to assess the degree of device variation.

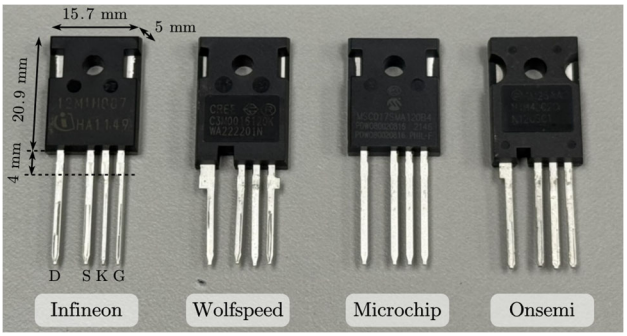


Fig. 2-3 Four SiC MOSFET candidates in TO-247 packages, candidates from left to right are (a) Infineon IMZA120R007M1H, (b) Wolfspeed C3M0016120K, (c) Microchip MSC017SMA120B4, and (d) Onsemi NTH4L020N120SC1.

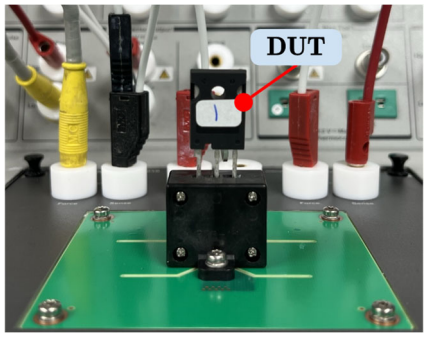


Fig. 2-4 Device characterization by using curve tracer.

Fig. 2-3 shows four selected SiC MOSFET candidates in discrete TO-247 package for device characterization. The TO-247 package is chosen because it allows simple characterizing process using a curve tracer. The four-pin configuration from left to right is drain, source, KS, and gate. This package with KS connection helps reduce the switching losses and improve switching speed [74, 108]. The thermal pad (or cooling surface) on the back side of the device is internally connected to the drain of SiC MOSFET. Fig. 2-4 shows the device under test (DUT) being characterized by curve tracer. For each candidate, multiple device samples from different batches purchased from distributors are tested.

The measured transfer characteristics (i_D to v_{GS}) are presented in Fig. 2-5. While some candidates exhibit obvious mismatches, the Infineon and Wolfspeed devices show a good consistency in transfer characteristics, indicating that they have consistent V_{th} and transconductance g_m (defined as the derivative of i_D over small change in v_{GS}) across individual devices. These results suggest a higher likelihood of consistent switching performance during operation of paralleled devices. Fig. 2-6 further characterizes the $R_{DS,on}$ of different candidates. Again, the Infineon devices show both the most consistent and lowest $R_{DS,on}$ among all candidates. In overall, both Fig. 2-5 and Fig. 2-6 prove that the device mismatch is a less critical challenge compared to asymmetric layout, as the dies/devices from Infineon and Wolfspeed provide relatively consistent performance for parallel operation. In contrast, it is challenging to ensure symmetric layout for paralleled devices, especially when paralleling more than two devices. Therefore, the remainder of this chapter focuses on modeling of current sharing caused by asymmetric layout.

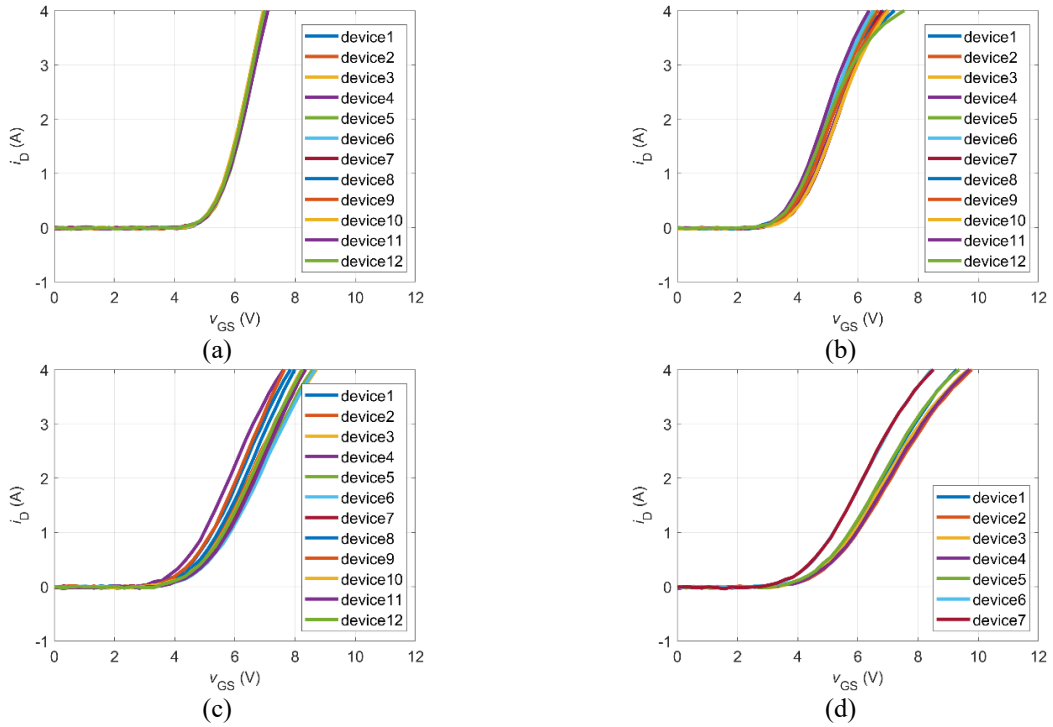


Fig. 2-5 The comparison of transfer characteristics (a) Infineon IMZA120R007M1H, (b) Wolfspeed C3M0016120K, (c) Microchip MSC017SMA120B4, and (d) Onsemi NTH4L020N120SC1.

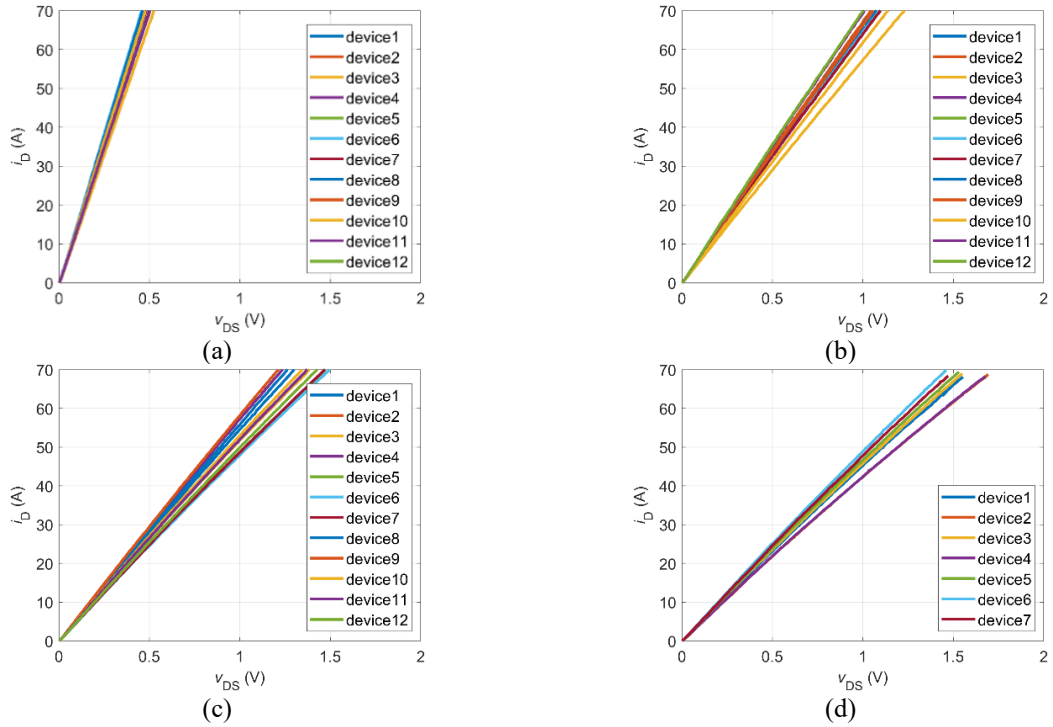


Fig. 2-6 The comparison of $R_{DS,on}$ (a) Infineon IMZA120R007M1H, (b) Wolfspeed C3M0016120K, (c) Microchip MSC017SMA120B4, and (d) Onsemi NTH4L020N120SC1.

2.2. Time-Domain Modeling for Current Sharing

2.2.1 Dynamic Current Sharing during Switching Transients

The mathematical model of dynamic current sharing is first derived in this section, and DPT circuit in Fig. 2-1 is used to derive current shared between paralleled devices LS1 and LS2. Individual currents on the drain, source, gate, and KS paths are denoted as i_D, i_S, i_G, and i_K, respectively. The total load current i_{load}, which is also the sum of i_{D1} and i_{D2}, flows into the drain node (D) and comes out from the source node (S). For the mathematically analysis of dynamic current sharing within the defined dynamic region shown in Fig. 2-2, several assumptions are made as follows [109, 110]:

- The V_{DC} is considered as a constant voltage source.
- During switching transient, the current i_{load} is considered as a constant.
- The SiC MOSFETs operate in saturation region and can be modeled as voltage-controlled current sources controlled by the v_{GS} across C_{GS}.
- Before reaching Miller plateau, i_G only charges the C_{GS}.
- Due to the nearly constant voltage of v_{DS}, the output capacitance $C_{oss} = C_{DG} + C_{DS}$ is omitted.
- The coupling effects between parasitic inductances are neglected.

Ideally, the i_D begins to increase after v_{GS} reaches V_{th}, and i_{load} is equally shared among paralleled devices. As shown in Fig. 2-2, due to the reverse recovery effect of the HS diode, the i_D continuous to rise until it reaches peak current value $i_{D,pk}$ which can serve as an indicator of whether the dynamic currents are balanced. Given these assumptions and descriptions, the L_D that in series with the current sources can be removed. Moreover, during dynamic switching transients, the impedances of parasitic inductances are much greater than that of parasitic resistances. Therefore, other than gate resistors R_G, the parasitic resistance can be neglected, and the circuit in Fig. 2-1 can be simplified as shown in Fig. 2-7 with emphasis on the paralleled LS devices. The circuit diagram shown in Fig. 2-7 valid only in the dynamic region and is used specifically for analyzing dynamic current sharing.

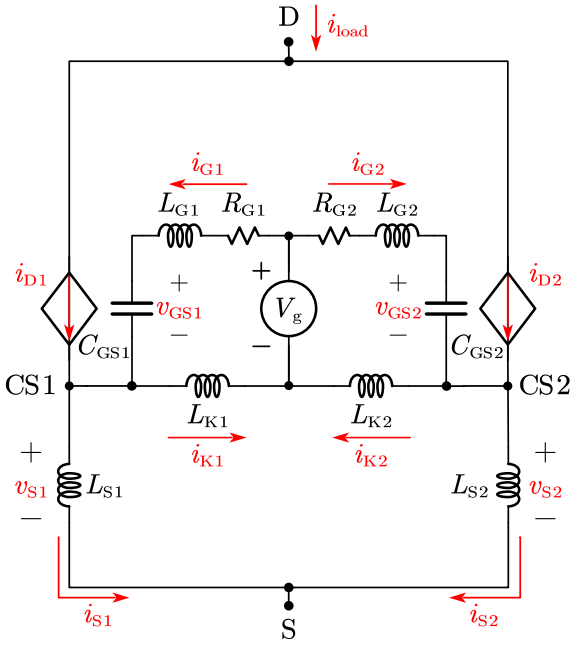


Fig. 2-7 Dynamic circuit diagram of paralleled SiC MOSFETs.

To simplify the derivation, the definitions in (2.1) are used in the following derivations:

$$\begin{cases} \Sigma x = x_1 + x_2 \\ \Delta x = x_1 - x_2 \end{cases} \tag{2.1}$$

The turn-on transient of SiC MOSFET is exemplified to analyze the dynamic current sharing. Given that the devices operate in the saturation region, channel currents i_{D1} and i_{D2} can be expressed as:

$$\begin{cases} i_{D1} = g_{m1}(v_{GS1} - V_{th1}), \ v_{GS1} > V_{th1} \\ i_{D2} = g_{m2}(v_{GS2} - V_{th2}), \ v_{GS2} > V_{th2} \end{cases} \tag{2.2}$$

The gate-source v_{GS1} and v_{GS2} during the dynamic region:

$$\begin{cases} v_{GS1} = \dfrac{1}{C_{GS1}} \displaystyle\int i_{G1} dt + V_{th1} \\ v_{GS2} = \dfrac{1}{C_{GS2}} \displaystyle\int i_{G2} dt + V_{th2} \end{cases} \tag{2.3}$$

Since this chapter mainly focuses on the unbalanced currents caused by asymmetric layout, the following assumptions are made for paralleled devices:

$$\begin{cases} V_{\mathrm{th}1} = V_{\mathrm{th}2} = V_{\mathrm{th}} \\ g_{\mathrm{m}1} = g_{\mathrm{m}2} = g_{\mathrm{m}} \\ C_{\mathrm{GS}1} = C_{\mathrm{GS}2} = C_{\mathrm{GS}} \end{cases} \tag{2.4}$$

Combining (2.1) to (2.4), relationships below can be obtained:

$$\begin{cases} \dfrac{d\,\Sigma i_{\mathrm{D}}}{dt} = \dfrac{di_{\mathrm{load}}}{dt} = \dfrac{g_{\mathrm{m}}}{C_{\mathrm{GS}}} \Sigma i_{\mathrm{G}} \\ \dfrac{d\,\Delta i_{\mathrm{D}}}{dt} = \dfrac{g_{\mathrm{m}}}{C_{\mathrm{GS}}} \Delta i_{\mathrm{G}} \end{cases} \tag{2.5}$$

By applying the KVL to gate driving loops in Fig. 2-7, the relationships can be written as:

$$\begin{cases} V_{\mathrm{g}} = R_{\mathrm{G}1} i_{\mathrm{G}1} + L_{\mathrm{G}1} \dfrac{di_{\mathrm{G}1}}{dt} + v_{\mathrm{GS}1} + L_{\mathrm{K}1} \dfrac{di_{\mathrm{K}1}}{dt} \\ V_{\mathrm{g}} = R_{\mathrm{G}2} i_{\mathrm{G}2} + L_{\mathrm{G}2} \dfrac{di_{\mathrm{G}2}}{dt} + v_{\mathrm{GS}2} + L_{\mathrm{K}2} \dfrac{di_{\mathrm{K}2}}{dt} \end{cases} \tag{2.6}$$

Since it is commercially available to select R_{G} with great tolerance (1% or less), and this article focuses on analyzing asymmetric layout, it is assumed that $\Delta R_{\mathrm{G}} = 0$. Another circuit relationship can be obtained by applying KVL to the bottom source-KS loop that includes L_{S} and L_{K}:

$$L_{\mathrm{S}1} \frac{di_{\mathrm{S}1}}{dt} - L_{\mathrm{K}1} \frac{di_{\mathrm{K}1}}{dt} = L_{\mathrm{S}2} \frac{di_{\mathrm{S}2}}{dt} - L_{\mathrm{K}2} \frac{di_{\mathrm{K}2}}{dt} \tag{2.7}$$

With the KCL to the power and gate loops, and at MOSFETs' common source (CS) nodes:

$$\begin{cases} \Sigma i_{\mathrm{D}} = \Sigma i_{\mathrm{S}} = i_{\mathrm{load}} \\ \Sigma i_{\mathrm{G}} = \Sigma i_{\mathrm{K}} \\ i_{\mathrm{D}1} + i_{\mathrm{G}1} = i_{\mathrm{S}1} + i_{\mathrm{K}1} \\ i_{\mathrm{D}2} + i_{\mathrm{G}2} = i_{\mathrm{S}2} + i_{\mathrm{K}2} \end{cases} \tag{2.8}$$

By substituting (2.5), (2.7), and (2.8) into (2.6), without performing Laplace transform, a time-domain mathematical model that describes the dynamic current sharing can be derived:

$$-v_{\mathrm{eq}} = R_{\mathrm{eq}} \Delta i_{\mathrm{G}} + L_{\mathrm{eq}} \frac{d\,\Delta i_{\mathrm{G}}}{dt} + \frac{1}{C_{\mathrm{eq}}} \int \Delta i_{\mathrm{G}}\, dt \tag{2.9}$$

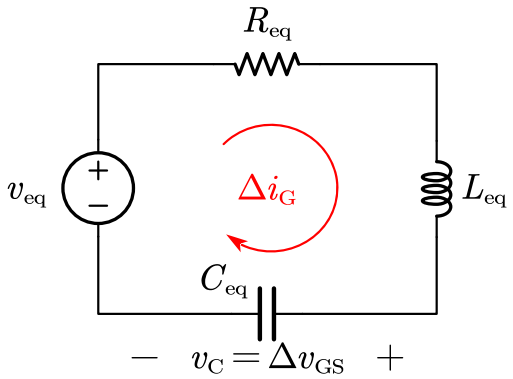


Fig. 2-8 Equivalent time-domain RLC circuit model that describes dynamic current sharing caused by asymmetric layout.

$$\begin{cases} v_{eq} = \Delta L_S \dfrac{di_{load}}{dt} + \left[\left(\dfrac{\Sigma L_S}{\Sigma L_K} + 1 \right) \Delta L_G + \dfrac{\Sigma L_S}{\Sigma L_K} \Delta L_K \right] \dfrac{d \Sigma i_G}{dt} \\ R_{eq} = \dfrac{\Sigma R_G (\Sigma L_S + \Sigma L_K)}{\Sigma L_K} + \dfrac{g_m \Sigma L_S}{C_{GS}} \\ L_{eq} = \dfrac{\Sigma L_G (\Sigma L_S + \Sigma L_K)}{\Sigma L_K} + \Sigma L_S \\ C_{eq} = \dfrac{C_{GS} \Sigma L_K}{2(\Sigma L_S + \Sigma L_K)} \end{cases} \tag{2.10}$$

Based on the derived (2.9) and (2.10), Fig. 2-8 illustrates the equivalent circuit model, suggesting that the process of dynamic current sharing can be modeled as an RLC circuit. It is observed that the equivalent voltage source v_{eq} causes the unbalanced gate current Δi_G, and the degree of Δi_G is determined by combination of equivalent resistance R_{eq}, equivalent inductance L_{eq}, and equivalent capacitance C_{eq}. The values of R_{eq}, L_{eq}, and C_{eq} are influenced by parasitic components and device's parameters.

For the source v_{eq} in (2.10), it can be generated by ΔL_S, ΔL_G, and ΔL_K. However, during the current rising period, the change in i_{load} (tens or hundreds of A level) is usually much greater than change in i_G (A level), implying that the v_{eq} is most sensitive to ΔL_S instead of ΔL_G or ΔL_K which aligns with previous works [76, 78]. Therefore, the v_{eq} can be simplified as:

$$v_{eq} = \Delta L_S \frac{di_{load}}{dt} \tag{2.11}$$

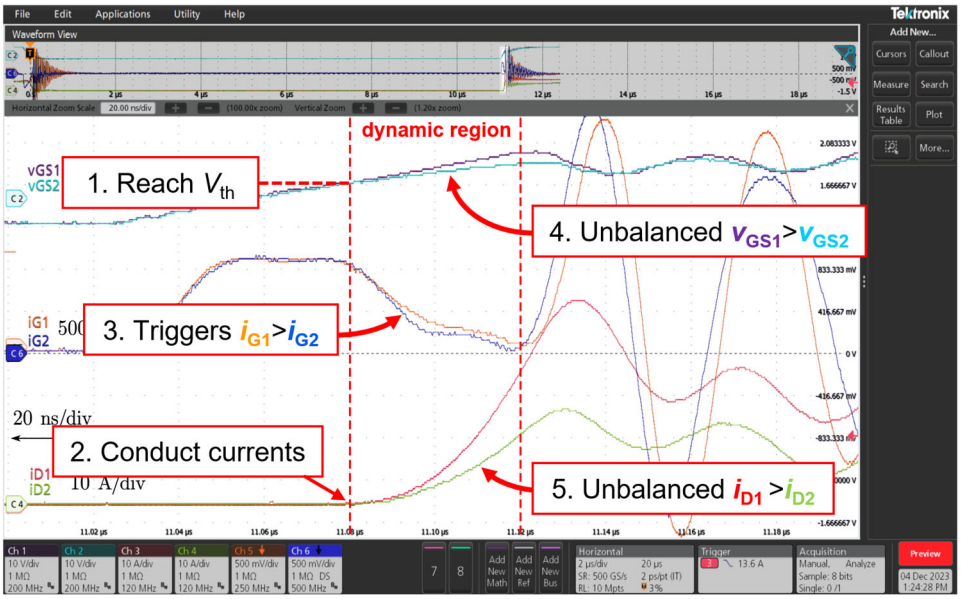


Fig. 2-9 Experimental waveforms to explain the mechanism of dynamic current sharing.

During dynamic region, the unbalanced Δi_G also determines the unbalanced channel currents Δi_D. Based on Fig. 2-8, the equivalent circuit impedance Z_{eq} is expressed as:

$$Z_{eq} = R_{eq} + j\omega L_{eq} + \frac{1}{j\omega C_{eq}} \tag{2.12}$$

where $\omega = 2\pi f$ and f is the specific frequency.

To explain the dynamic current sharing mechanism, Fig. 2-9 shows the experimental waveform example under asymmetric layout $L_{S2} > L_{S1}$. When both devices v_{GS} reach V_{th} and start conducting currents, v_{eq} in Fig. 2-8 becomes positive, creating the positive unbalanced gate current $\Delta i_G = i_{G1} - i_{G2} > 0$. Given that i_{G1} is larger than i_{G2}, the C_{GS1} is charged faster than the C_{GS2}, causing v_{GS1} to surpass v_{GS2}. During dynamic region, since the MOSFETs are controlled by v_{GS}, i_{D1} rises more rapidly than i_{D2} and results in unbalanced dynamic currents. Similarly, during the turn-off transient when L_{S2} is larger than L_{S1}, a larger turn-off current is drawn from LS1 to V_g. Consequently, the LS1 turns off faster and carries less turn-off current than LS2. The derived time-domain RLC model in this dissertation helps identify the key impact factors more straightforwardly and allows predicting the time-domain waveform of unbalanced Δi_G for quantitative comparison. The corresponding practical layout suggestions and verifications will be presented in later Section 2.3, Section 2.4, and Section 2.5.

2.2.2 Static Current Sharing

For the static regions in Fig. 2-2, the SiC MOSFET in Fig. 2-1 can be modeled as $R_{DS,on}$. Also, due to the low-frequency static currents, it is required to take parasitic resistance R into consideration. Fig. 2-10 shows the static circuit based on Fig. 2-1, emphasizing two paralleled devices at LS position. Due to the static circuit characteristic, the Laplace transform can be applied to analyze the circuit. In Fig. 2-10, impedance Z consists of both parasitic resistance R and inductance L from the PCB traces and the device internal package that are previously listed in Table 2-1:

$$Z = R + j\omega L \tag{2.13}$$

The device $R_{DS,on}$ is included in the combined Z_D due to series connection. By applying Δ-Y transformation, the circuit in Fig. 2-10(a) can be simplified to that in Fig. 2-10(b), where:

$$\begin{cases} Z_A = \dfrac{Z_K \cdot Z_{S1}}{Z_S + Z_K} \\ Z_B = \dfrac{Z_K \cdot Z_{S2}}{Z_S + Z_K} \\ Z_C = \dfrac{Z_{S1} \cdot Z_{S2}}{Z_S + Z_K} \end{cases} \tag{2.14}$$

According to Fig. 2-10(b), the difference of static current Δi_D in s-domain can be expressed by

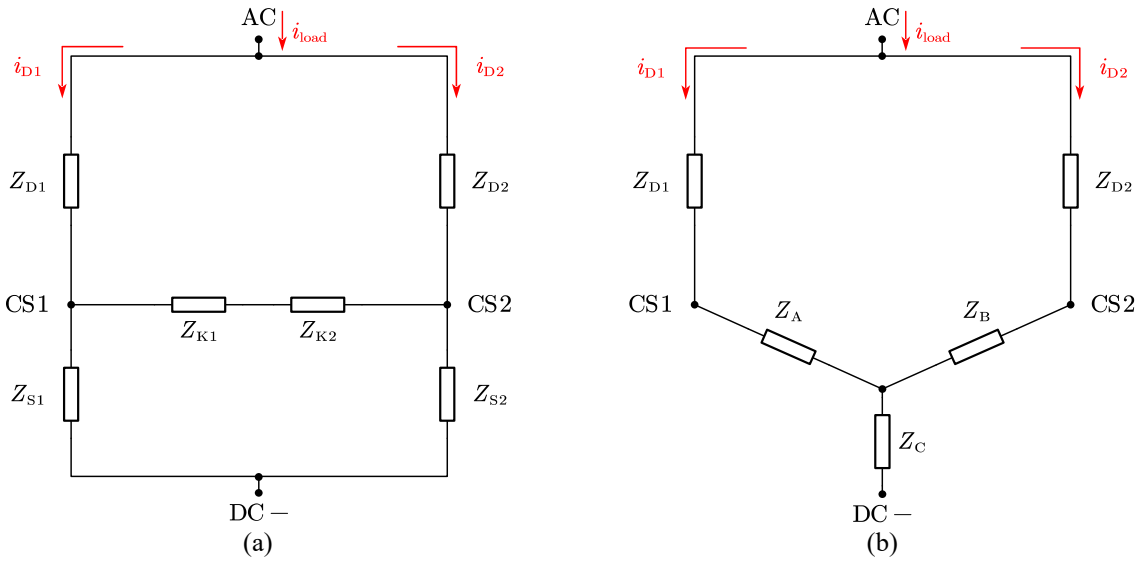


Fig. 2-10 Static circuit diagram of paralleled SiC MOSFETs (a) original circuit and (b) circuit after Δ-Y transformation.

applying KVL to the circuit:

$$\begin{aligned}&(Z_{\mathrm{D1}}+Z_{\mathrm{A}})\cdot i_{\mathrm{D1}}(s)-(Z_{\mathrm{D2}}+Z_{\mathrm{B}})\cdot i_{\mathrm{D2}}(s)=0\\&\Rightarrow \Delta i_{\mathrm{D}}(s)=-\frac{\Delta Z_{\mathrm{D}}+\frac{Z_{\mathrm{K}}}{Z_{\mathrm{S}}+Z_{\mathrm{K}}}\Delta Z_{\mathrm{S}}}{Z_{\mathrm{D}}+\frac{Z_{\mathrm{K}}}{Z_{\mathrm{S}}+Z_{\mathrm{K}}}Z_{\mathrm{S}}}\cdot i_{\mathrm{load}}\end{aligned}\tag{2.15}$$

When Δi_{D} reaches its maximum value $\Delta i_{\mathrm{D,max}}$, the *di/dt* in time-domain is 0. The $\Delta i_{\mathrm{D,max}}$ can therefore be derived by applying inverse Laplace transform to (2.15):

$$\begin{aligned}&\Delta i_{\mathrm{D,max}}=\\&-\left[\frac{(R_{\mathrm{S}}+R_{\mathrm{K}})}{R_{\mathrm{D}}(R_{\mathrm{S}}+R_{\mathrm{K}})}\frac{di_{\mathrm{load}}}{dt}\right]\Delta L_{\mathrm{D}}-\left[\frac{(L_{\mathrm{S}}+L_{\mathrm{K}})\frac{di_{\mathrm{load}}}{dt}+(R_{\mathrm{S}}+R_{\mathrm{K}})i_{\mathrm{load}}}{R_{\mathrm{D}}(R_{\mathrm{S}}+R_{\mathrm{K}})}\right]\Delta R_{\mathrm{D}}\\&-\left[\frac{R_{\mathrm{K}}}{R_{\mathrm{D}}(R_{\mathrm{S}}+R_{\mathrm{K}})}\frac{di_{\mathrm{load}}}{dt}\right]\Delta L_{\mathrm{S}}-\left[\frac{L_{\mathrm{K}}\frac{di_{\mathrm{load}}}{dt}+R_{\mathrm{K}}i_{\mathrm{load}}}{R_{\mathrm{D}}(R_{\mathrm{S}}+R_{\mathrm{K}})}\right]\Delta R_{\mathrm{S}}\end{aligned}\tag{2.16}$$

In (2.16), the static current difference $\Delta i_{\mathrm{D,max}}$ is affected by mismatches in parasitic resistance ΔR and parasitic inductance ΔL. The first two terms are from asymmetric drain parasitic (ΔL_{D} and ΔR_{D}), while the latter two are generated by mismatched source parasitic (ΔL_{S} and ΔR_{S}). Combining with the model derived for dynamic current sharing, several key practical layout suggestions are provided in the next section.

2.3. Practical Layout Suggestions

Based on the derived models, which are (2.9) to (2.12) for dynamic current sharing and (2.16) for static current sharing, practical layout suggestions are proposed in this section. Observing derived (2.9) to (2.12) for dynamic current sharing, it is evident that reducing R_{G} worsens the unbalanced dynamic currents. This is attributed to an increase in the switching speed in v_{eq} and a decrease in the value of R_{eq}. From the perspective of current sharing, the R_{G} significantly influences dynamic current sharing as it impacts both v_{eq} and Z_{eq} in the equivalent RLC circuit model. For parasitic inductances, it is seen that the unbalanced gate currents Δi_{G} can be zero or suppressed if one of the following three conditions is satisfied:

- The $\Delta L_S = 0$, indicating a perfect layout thus $v_{eq} = 0$, the unbalanced Δi_G vanished.
- The L_K is extremely small when v_{eq} is held at constant, creating significantly large Z_{eq} that helps suppress the Δi_G even if v_{eq} exists.
- When v_{eq} is held at constant, the ΣL_S should be as large as possible to suppress Δi_G.

For the first condition, it aligns with the existing conclusions given by [76, 78], therefore, will not be further discussed.

Contrary to the conclusion in [79] that the impact of L_K is negligible in the presence of ΔL_S, it is discovered that the unbalanced Δi_G is positively correlated with L_K. Based on the derived model in (2.10), increasing L_K results in a reduced Z_{eq}, which in turn leads to greater Δi_G and more unbalanced currents. As L_K increases further, its influence becomes less pronounced. Once L_K reaches a sufficiently large value and becomes comparable with ΣL_S, its effect saturates. Eventually, the change in Δi_G will be less noticeable which is exactly the scenarios studied in [79] where L_K was very large and comparable to ΣL_S. This discovery will be validated by simulation results in later sections. The conclusion given in this dissertation that L_K should be minimized can be beneficial for power module design. In practice, dies in a power module can be arranged to achieve a low L_K value through custom bonding, whereas the power devices with existing package have a non-zero L_K. However, dynamic current sharing can still be improved by minimizing the L_K in PCB layout for paralleled discrete devices which will be shown in experimental validations.

Additionally, the statement in [79] suggesting that ΣL_S should be significantly increased may be misleading. This aspect can be clarified by the derived model. While increasing ΣL_S does enhance Z_{eq}, it also reduces the di_{load}/dt in v_{eq} due to a larger L_{loop}. Since no time-domain waveforms were presented, the observed improvement in Δi_D in [79] could partially be attributed to a slower switching speed, similar to the effect caused by increasing R_G. According to the derived model, this dissertation offers a refined suggestion. For layout design, the commutation loop inductance L_{loop} should always be minimized as it affects the overshoot voltage of the device [111]. Both L_D and L_S are part of the entire L_{loop}. To further enhance the dynamic current sharing at the same switching speed, within L_{loop}, the proportion of ΣL_S should be maximized because Z_{eq} is positively proportional to ΣL_S. In contrast, increasing ΣL_D has no impact on dynamic current sharing.

The junction temperature T_j also affects the dynamic current sharing since it affects g_m of SiC

MOSFET. Because R_{eq} is positively related to g_m, the change in g_m has impact on Z_{eq} which further affects dynamic current sharing. Fig. 2-11 shows the transfer characteristic from datasheets of C3M0016120K from Wolfspeed [112]. Within the rated current, the i_D at 25 °C rises slightly faster than that at 175 °C, yielding a smaller g_m at higher T_j which can be fitted as:

$$\begin{cases} i_D = 42.1 \cdot v_{GS} - 233.7, T_j = 25^\circ C \\ i_D = 40.5 \cdot v_{GS} - 181.4, T_j = 175^\circ C \end{cases} \tag{2.17}$$

As a result, when paralleled devices are operating at a higher T_j, the Z_{eq} becomes smaller and worsens current sharing. The impact of T_j on dynamic current depends on the g_m characteristics of SiC MOSFET being chosen.

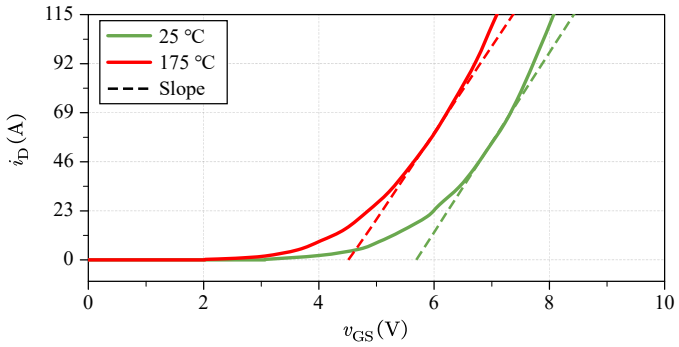


Fig. 2-11 The g_m characteristics of C3M0016120K.

For static current sharing from (2.16), it is more straightforward that asymmetric parasitic along both drain and source paths, namely ΔL_D, ΔR_D, ΔL_S, and ΔR_S, affects current sharing. The static $\Delta i_{D,max}$ is more sensitive to mismatches in drain parasitic than source parasitic, and to parasitic R than L. Moreover, the static current sharing is influenced by sum of KS parasitic R_K and L_K, while asymmetries in ΔR_K and ΔL_K have no impact. Additionally, the gate parasitic has no impact on static current sharing. Therefore, to achieve balanced static currents, effort should be put into minimizing asymmetries in drain and source paths.

2.4. Simulation Verifications

The derived models are verified by using LTspice. The verification of dynamic current sharing model is first conducted. In the simulations, the parameter studied can be easily adjusted without being affected by other external factors. Both DPT circuit in Fig. 2-1 and equivalent RLC circuit

model in Fig. 2-8 are built to study the impact of parameters. The DPT circuit is simulated under 600 V conditions. Two SiC MOSFETs are paralleled in LS position, and the SPICE model of C3M0016120K from Wolfspeed is employed as the switching devices and HS diode. The values of R_{eq}, L_{eq}, and C_{eq} in the RLC circuit model are calculated according to the parasitic and device parameters obtained from the datasheet or scaled result from the SPICE device model [112, 113].

Fig. 2-12 shows the impact of R_G on dynamic current sharing. The L_{S2} is set as 10 nH higher than L_{S1}, and R_G takes on values of 3 **Ω**, 10 **Ω**, and 15 **Ω**. The Δi_G in solid is the subtraction of two gate currents in DPT circuit, and that in dashed represents the measured current in the derived equivalent RLC circuit model. When the mismatched L_S is fixed, the currents become more balanced as the R_G increases. More importantly, focusing on Δi_G, the trend of measured model current aligns well with the subtraction of real currents.

The discrepancy between the simulated and modeled waveforms is due to the nonlinearity of g_m. In a real device, as i_D rises from 0 to load current, g_m gradually increases from low to high values. However, the obtained waveform is calculated assuming a constant g_m. Therefore, since Z_{eq} is positively proportional to g_m, the modeled Δi_G initially underestimates and later slightly overestimates compared to the real Δi_G during current rising period. The largest discrepancy occurs after i_D reaches $i_{D,pk}$ because the analyzed circuit can no longer accurately represent the real case due to changes in v_{DS}, implying that both C_{GD} and C_{DS} can no longer be neglected. Despite this, during the transient period, the modeled Δi_G is still close to real currents with small error.

Fig. 2-13 shows the simulation results when $L_{K1} = L_{K2}$ are 0.1 nH, 5nH, and 10 nH. In all three cases, the L_{S2} is 10 nH higher than L_{S1} and R_G is 10 **Ω**, indicating that the v_{eq} is fixed. In Fig. 2-13, apparently, the degree of unbalanced Δi_G is smallest when L_K is minimized, and the channel currents i_{D1} and i_{D2} are almost balanced accordingly. The currents become unbalanced as L_K increases. In addition, the impact of L_K becomes less pronounced when L_K is further increased, indicating that the effect of L_K will get saturate. The simulation results verify the refined suggestion proposed in this paper, showing that L_K should be minimized to help balance the currents.

Fig. 2-14(a) reveals the impact of ΣL_S when the L_{loop} is kept at constant to ensure the same switching speed. Three different cases present the waveforms when ΣL_S are 12 nH, 32 nH, and 52 nH. It is apparent that the degree of unbalanced Δi_G decreases as ΣL_S increases. On the other hand,

Fig. 2-14(b) shows the influence of ΣL_D. Increasing ΣL_D has a negligible impact on dynamic current sharing since the process is independent of L_D. The results align with the layout suggestion that within L_{loop}, the proportion of ΣL_S should be maximized and ΣL_D should be minimized.

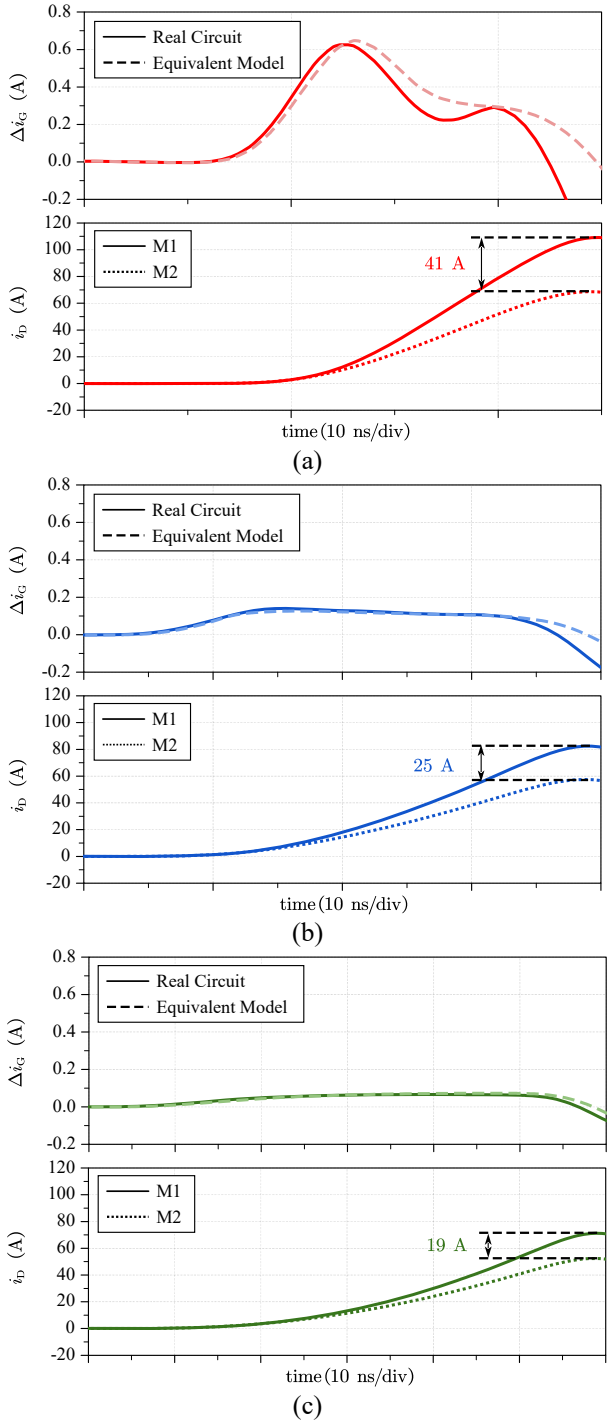


Fig. 2-12 Simulation results with fixed ΔL_S when (a) R_G = 3 Ω, (b) R_G = 10 Ω, and (c) R_G = 15 Ω.

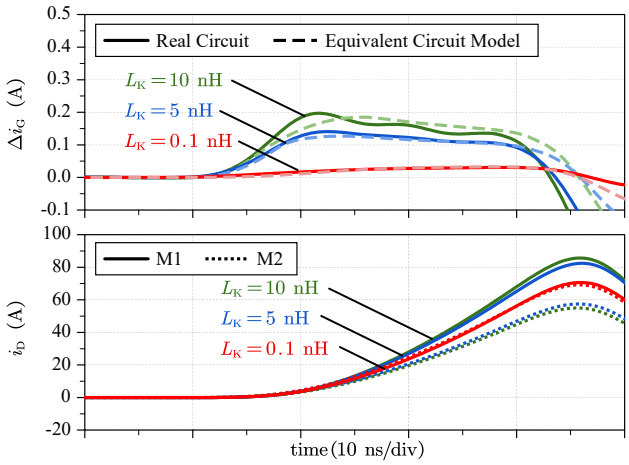


Fig. 2-13 Simulation results of different L_K values with fixed R_G and ΔL_S.

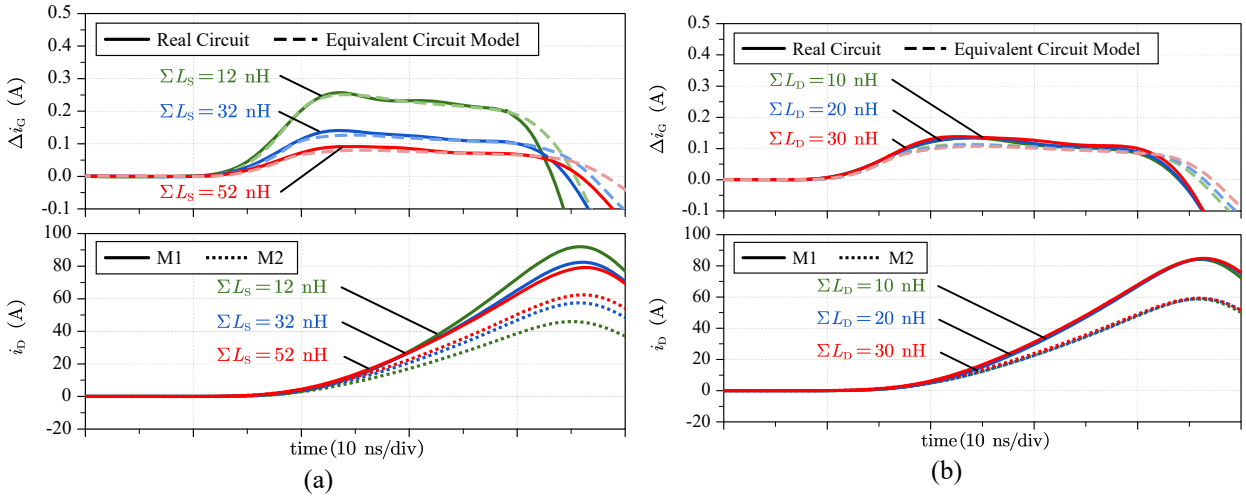


Fig. 2-14 Simulation results of (a) different ΣL_S values (b) different ΣL_D values. The R_G and ΔL_S are fixed.

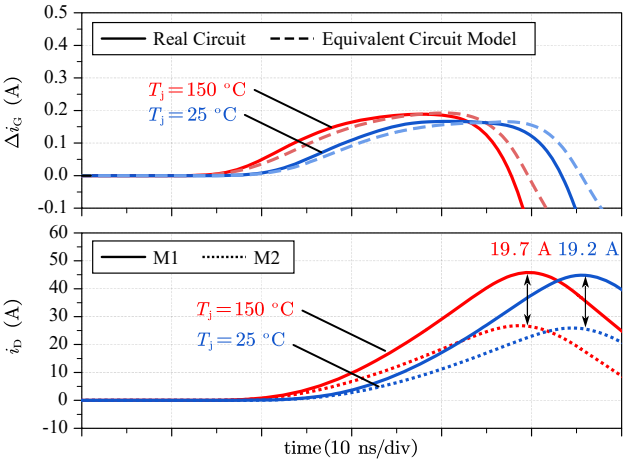


Fig. 2-15 Simulation results of different ΣL_S values with fixed R_G and ΔL_S.

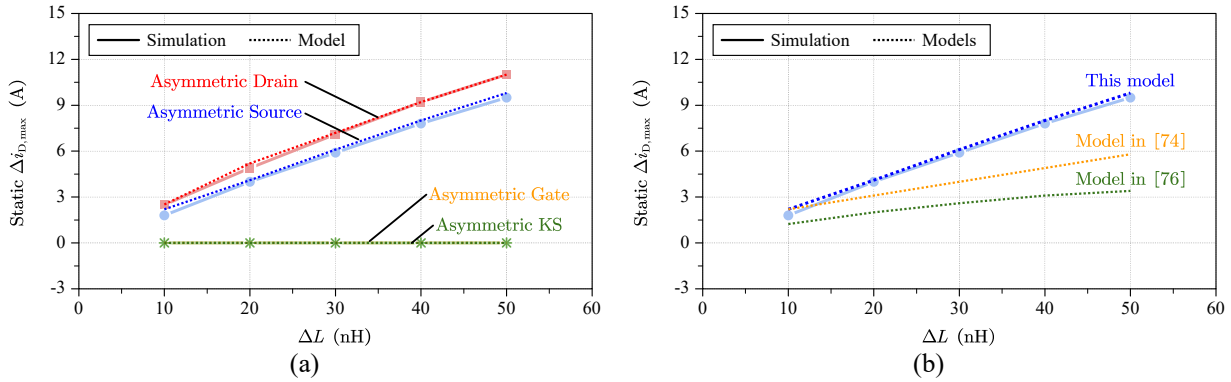


Fig. 2-16 Static $\Delta i_{D,max}$ comparisons between (a) derived model and circuit-level simulations (b) derived model and different models in the literature.

Lastly, the impact of T_j on current sharing is demonstrated in Fig. 2-15 by using C3M0016120K. The T_j slightly changes g_m based on (2.17). The $|\Delta L_S|$ and R_G are set as 10 nH and 10 Ω, respectively. Compared to the case with T_j of 25 ºC, the current sharing is slightly worse when paralleled devices are heated to T_j of 150 ºC because of a lower g_m at higher T_j. However, since the g_m is only slightly affected by T_j for this specific device, the impact of T_j on current sharing is not as significant as R_G or other parasitic inductances.

For static current sharing verification, Fig. 2-16(a) compares the static $\Delta i_{D,max}$ with different ΔL in different cases from circuit-level simulation and derived (2.16). Consistent with the summary in Section 2.2.2, the asymmetric drain has greater impact than asymmetric source, while asymmetries in gate and KS paths have negligible impact. Additionally, the static $\Delta i_{D,max}$ values predicted by the derived model well align with the values from simulation results, verifying the model's accuracy. Fig. 2-16(b) further compares the derived model with existing models from the literature [74, 76]. Obviously, the derived model accurately predicts static $\Delta i_{D,max}$ by incorporating both parasitic R and L in the circuit, outperforming other models [74, 76] that consider only parasitic L.

2.5. Experimental Validations

To verify the current sharing analysis and derived model. A DPT environment is established as shown in Fig. 2-17. In this section, the primary focus is to verify the dynamic current sharing analysis, as static current sharing is relatively more straightforward. Fig. 2-17(a) shows the circuit diagram of the test boards. The SiC MOSFETs C3M0016120K and SiC Schottky diode C4D40120D in TO-247 packages from Wolfspeed are employed as paralleled DUT and

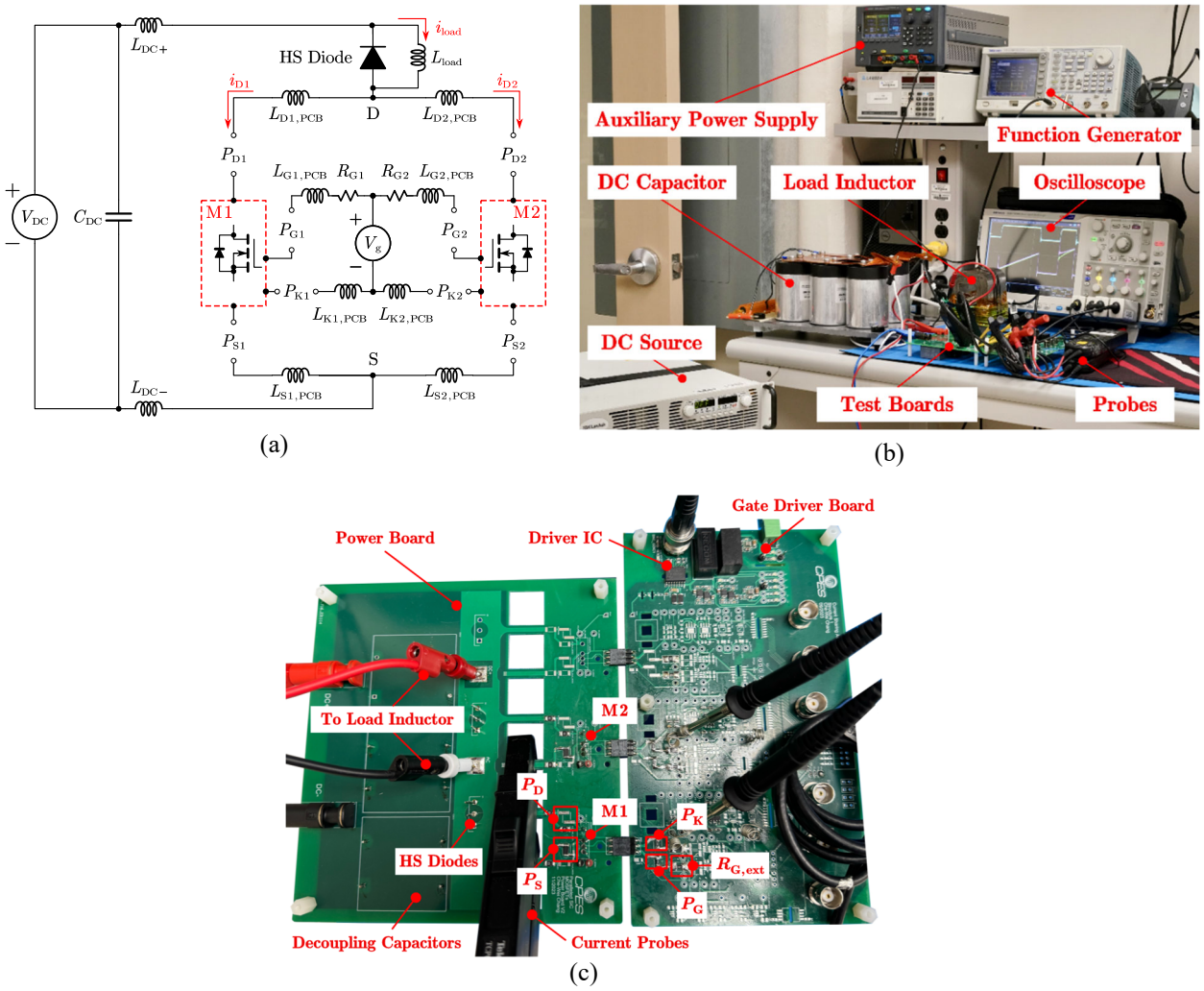


Fig. 2-17 The DPT setup for current sharing analysis (a) circuit diagram, (b) testing environment, and (c) top view of test boards.

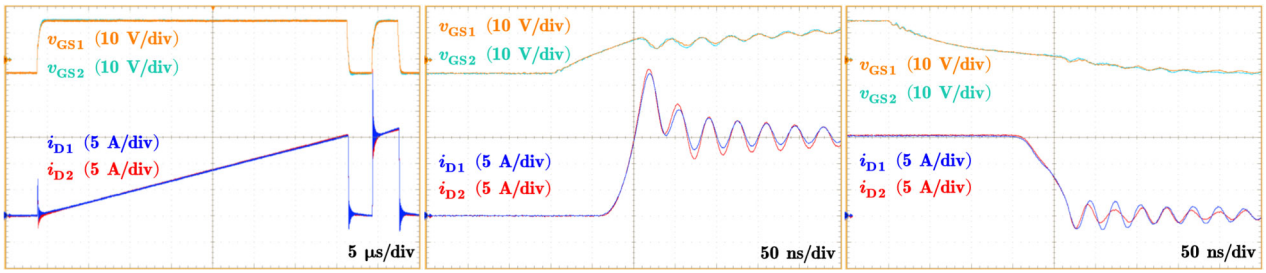
freewheeling diode, respectively. The layout of each MOSFET is identical to the other. The pads P_D, P_S, P_G, and P_K are left on the PCB, which can either be used to insert external parasitic inductance L_{ext} or be shorted by jumper depending on the testing need. Table 2-2 lists the testing conditions and parameters, including PCB parasitic L_{PCB} extracted from the Q3D and device's internal parasitic L_{int}. The parasitic inductance L on each path can be expressed as:

$$L = L_{PCB} + L_{ext} + L_{int} \tag{2.18}$$

Fig. 2-17(b) shows the testing environment where the function generator is used to generate the gate driving pulse. Fig. 2-17(c) offers a closer view of the test boards. The SiC MOSFETs M1 and M2, paralleled in LS position, are soldered on the power board. Both MOSFETs are driven

TABLE 2-2 EXPERIMENTAL TESTING CONDITIONS IN FIG. 2-17

SYMBOLS	VALUES
V_{DC}	600 V
V_g	15 V/-5 V
C_{DC}	286 μF
i_{load}	30 A
L_{load}	185 μH
Device internal gate resistance $R_{G,int}$	2.6 Ω
Device internal drain parasitic $L_{D,int}$	4.366 NH
Device internal source parasitic $L_{S,int}$	2.3 NH
Device internal gate parasitic $L_{G,int}$	7.7 NH
Device internal KS parasitic $L_{K,int}$	5.17 NH
Layout initial drain parasitic $L_{D1,PCB}/L_{D2,PCB}$	17.389 NH/ 17.421 NH
Layout initial source parasitic $L_{S1,PCB}/L_{S2,PCB}$	20.667 NH/ 20.591 NH
Layout initial gate parasitic $L_{G1,PCB}/L_{G2,PCB}$	15.71 NH/ 15.62 NH
Layout initial KS parasitic $L_{K1,PCB}/L_{K2,PCB}$	17.12 NH/ 17.38 NH



(a) (b) (c)

Fig. 2-18 Initial experimental waveforms with symmetric layout (a) overall, (b) turn-on transient, and (c) turn-off transient.

by gate driver IC mounted on the separated gate driver board. The drain currents i_D can be measured from the cutouts on the power board using current probes Tektronix TCP0030A [114]. The SMD air coil inductors from Wurth Elektronik ranging from 5 to 28 nH are utilized as L_{ext}. The SiC MOSFETs are prescreened by using curve tracer B1505A to select devices with similar electrical parameters, such as V_{th}, g_m, and $R_{DS,on}$. Fig. 2-18 shows the initial experimental waveforms without placing any L_{ext}. The i_{D2} rises slightly faster than i_{D1}. Overall, both v_{GS} and i_D of two DUTs are nearly identical.

Fig. 2-19 shows the experimental waveforms with a fixed mismatched L_S of 16.5 nH and varying external gate resistor $R_{G,ext}$. The gate currents i_{G1} and i_{G2} are measured by Rogowski coil current probe CWT06 (120 A/30 MHz). In Fig. 2-19, the mechanism is consistent with the theoretical circuit model. The degree of Δi_G diminishes as the $R_{G,ext}$ increases, consistent with the model's prediction that higher R_G results in greater impedance during dynamic region, decreasing the Δi_G. The bottom waveform of each case compares the unbalanced Δi_G obtained from experiment,

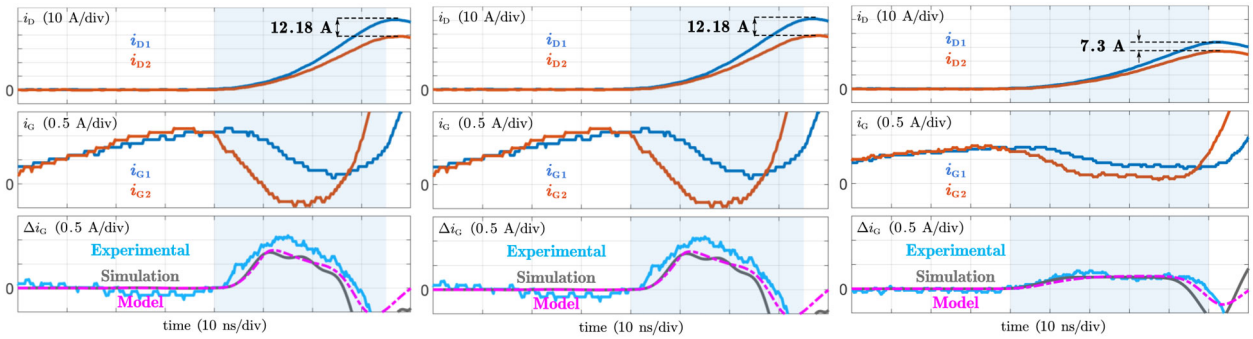


Fig. 2-19 Experimental waveforms with fixed ΔL_S when (a) $R_{G,ext}$ of 3.6 Ω (b) $R_{G,ext}$ of 10 Ω, and (c) $R_{G,ext}$ of 15 Ω.

simulation, and equivalent circuit model. In all cases, the experimental waveform is slightly higher than those obtained from simulation and circuit model. In addition, before the channels start conducting currents, the measured i_{G2} is slightly higher than i_{G1}. These differences may be caused by characteristics difference between DUTs or measuring errors. In overall, the experimental results correspond well with the model.

The experimental waveforms in Fig. 2-20 show the impact of L_K by inserting external $L_{K,ext}$ at position P_K. When L_{S2} is 16.5 nH larger than L_{S1} and $R_{G,ext}$ of 10 Ω, the i_{D1} and i_{D2} become more unbalanced as $L_{K,ext}$ increases. The peak current difference $\Delta i_{D,pk}$ are 8.3 A, 9.9 A, and 10.5 A when $L_{K,ext}$ are 0 nH, 11 nH, and 21.5 nH, respectively. Theoretically, currents should achieve perfect balance when L_K equals 0 nH. However, demonstrating such results with TO-247 devices is challenging due to the existing device's $L_{K,int}$ and layout $L_{K,PCB}$. According to the SPICE model, the device has a $L_{K,int}$ of 5.17 nH [113]. Despite that, the waveform trend validates the analysis, showing that increasing L_K deteriorates the unbalanced dynamic current sharing.

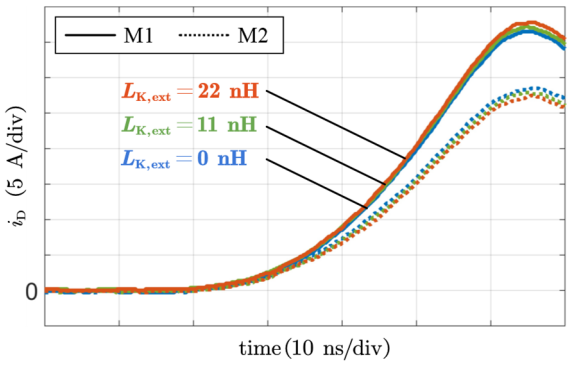


Fig. 2-20 Experimental waveforms of different $L_{K,ext}$ values with fixed $R_{G,ext}$ and ΔL_S.

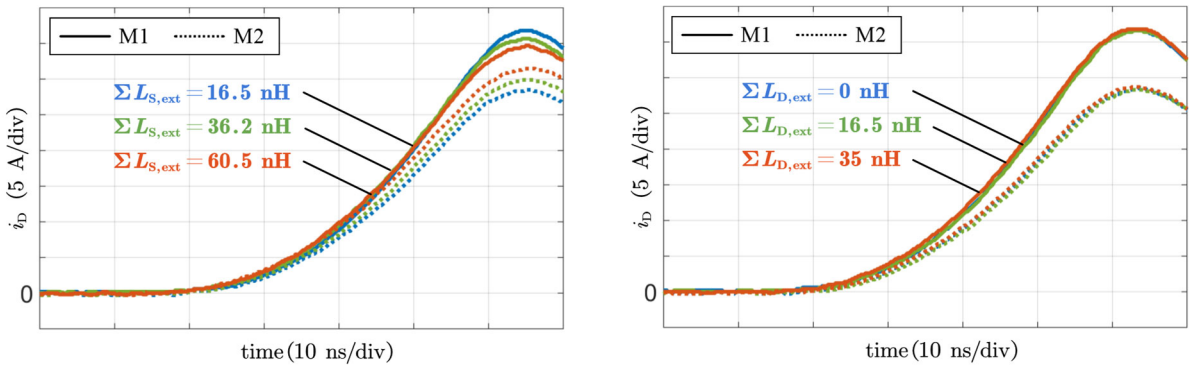


Fig. 2-21 Experimental waveforms of (a) different $\Sigma L_{S,ext}$ and (b) different $\Sigma L_{D,ext}$ values. The $R_{G,ext}$ and ΔL_S are fixed.

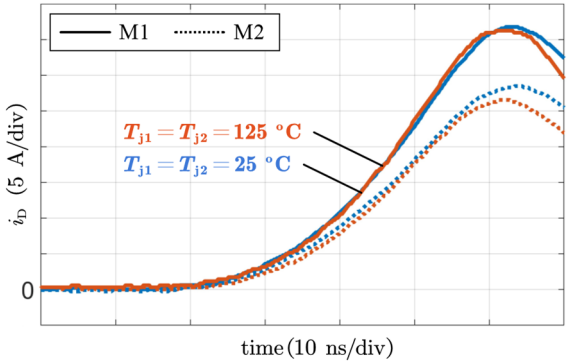


Fig. 2-22 Experimental waveforms at different T_j values with fixed $R_{G,ext}$ and ΔL_S.

The effect of ΣL_S is revealed in Fig. 2-21(a) where mismatched L_S is 16.5 nH and $R_{G,ext}$ is 10 Ω. Under the fixed L_{loop}, the $\Delta i_{D,pk}$ decreases from 8.3 A, 7.1 A, to 5.1 A as $\Sigma L_{S,ext}$ increases from 16.5 nH, 36.2 nH, to 60.5 nH, respectively. On the other hand, Fig. 2-21(b) shows the experimental waveforms under same conditions but with $\Sigma L_{D,ext}$ increased from 0 nH, 16.5 nH, to 35 nH. In these cases, the degree of unbalanced i_D remains nearly identical around 8.3 A, suggesting that unbalanced dynamic currents are independent of ΣL_D. The results in Fig. 2-21verify the conclusion that, while L_{loop} should always be minimized, increasing the proportion of ΣL_S in L_{loop} is more advantageous than increasing ΣL_D from the perspective of dynamic current sharing. The experimental results align with the analysis.

Fig. 2-22 depicts the experimental results when both DUTs are heated to 125 °C. The resistors MP9100 with TO-247 package are mounted on the backside of the DUTs to heat the devices. When T_j is elevated to 125 °C, the $\Delta i_{D,pk}$ increases from 8.3 A to 9.2 A though the peak currents are slightly lower than that of 25 °C. The result is consistent with the analysis that the dynamic currents become more unbalanced in high-temperature environments. However, for this specific device,

the impact of T_j is not as significant when compared to R_G or ΣL_S. These results in Fig. 2-19, Fig. 2-20, Fig. 2-21, and Fig. 2-22 verify the current sharing analysis.

2.6. Conclusion

This chapter comprehensively analyzes the current sharing mechanism among paralleled SiC MOSFETs in both dynamic and static regions. Device characterization results show that the device mismatch is a less critical challenge compared to asymmetric layout, as some device candidates provide a consistent performance among individual devices. Moreover, the entire dynamic current sharing process can be described by the derived time-domain equivalent RLC circuit model which allows straightforward quantitative comparisons. In addition to confirming previous findings that minimizing ΔL_S is crucial, more layout suggestions from literature for paralleled SiC MOSFETs should be refined as listed as follows:

- Parasitic inductance on KS paths (L_K) should be minimized as small as possible, contrary to the literature that the impact of L_K is negligible.
- The commutation loop inductance L_{loop} should always be minimized. However, within L_{loop}, the proportion of source inductances summation ΣL_S should be as high as possible, as increasing ΣL_S helps balance the dynamic currents. Increasing the proportion of drain inductances summation ΣL_D has no impact on dynamic current sharing.

On the other hand, the developed static current sharing model helps predict the peak current difference, and the accuracy outperforming other models in literature.

Chapter 3

Passive Current-Balancing Solutions

In Chapter 2, it is found that asymmetric layout poses a more critical challenge than mismatched devices, as some device candidates prove to have consistent characteristics across individual devices. Consequently, the current-balancing solutions should target current imbalance induced by asymmetric layout. For commercial applications, passive current-balancing solutions are very attractive due to the merits of low-cost, simple, high scalable, and easy to implement. Based on the current sharing analysis in Chapter 2, current sharing in both static and dynamic regions can be improved through two key approaches:

- Mitigating drain and source parasitic: Static current sharing is directly influenced by asymmetric drain and source parasitic. Furthermore, as indicated by the derived RLC circuit model in Fig. 2-8, dynamic current sharing can be improved if the equivalent voltage source $v_{eq} = 0$, which corresponds to balanced source parasitic.
- Introducing additional components: The RLC circuit model in Fig. 2-8 also suggests that dynamic current sharing can be enhanced by incorporating additional components that maximize the impedance Z_{eq} in the RLC circuit, thereby suppressing the Δi_G even if v_{eq} exists.

The first approach emphasizes the importance of layout strategy for paralleled devices, focusing on balanced layout of paralleled branches. The efforts should concentrate on balancing the drain and source power layout, as the models show that mismatched gate and KS layouts have negligible impact on both dynamic and static current sharing. In addition to improving current sharing, the adopted layout strategy must also ensure the best electrical performance, particularly in terms of minimizing L_{loop} and parasitic capacitances.

The second approach highlights the potential of adding extra components on the gate driver side to suppress Δi_G, since the induced Δi_G is the root cause of unbalanced dynamic current sharing. This solution should feature simple and cost-effective, enhancing current sharing with minimal

additional implementation effort.

In this chapter, the development process of passive current-balancing solutions is carried out through the following steps:

- Step 1: Optimize layout configuration and device arrangement. Various layout options for paralleled devices are evaluated to identify the combination that delivers the best electrical performance, with particular emphasis on minimizing L_{loop} and overlapping capacitances.
- Step 2: Building upon the optimal layout configuration, a novel distributed-block (DB) layout concept is proposed to mitigate drain and source parasitic, thereby improving both static and dynamic current sharing.
- Step 3: To further enhance dynamic current sharing, differential-mode-chokes (DMC) are added into the gate driver, suppressing the Δi_G and mitigating current imbalance.

3.1. Optimal Layout Design for Paralleled Devices

3.1.1 Layout Configurations and Device Arrangements

Fig. 3-1 illustrates an HB circuit consists of dc-link capacitor C_{DC} and switching positions of HS and LS. The HB circuit is connected to an external dc voltage source V_{DC}, and discrete SiC MOSFETs are paralleled in both HS and LS positions. The electrical performance of the HB is mainly influenced by two factors, the layout-generated L_{loop} and overlapping capacitances C (C_{HS} and C_{LS}). Disregard the device parasitic, the L_{loop} is the sum of the total parasitic inductances along the switching current path, including parasitic from layouts between C_{DC} and HS, HS and LS, LS and C_{DC}. During switching transients, the rapid change in current direction induces voltage across L_{loop}, resulting in additional voltage stress on the SiC MOSFETs. The voltage stress is positively related to L_{loop} and switching speed, and may exceed device's rated voltage [115]. Meanwhile, the C_{HS} and C_{LS} generated by overlapping layout layers in the PCB are equivalent to the output capacitance of switching positions. These parasitic capacitances introduce additional switching losses of SiC MOSFETs. Therefore, minimizing L_{loop}, C_{HS}, and C_{LS} help reducing voltage stress and switching losses, thereby enhancing electrical performance.

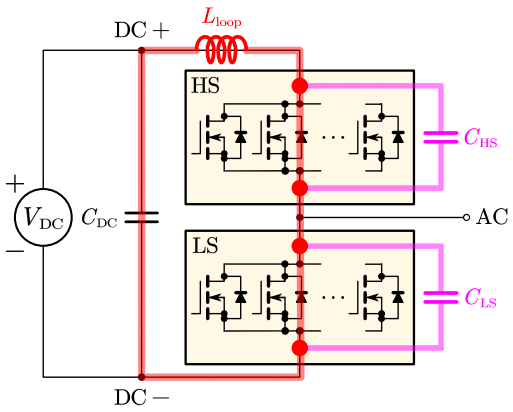


Fig. 3-1 The circuit diagram of a HB with parasitic L_{loop} and overlapping C.

To find the optimal layout combination that improves electrical performance, several layout types for paralleled discrete devices are shown in Fig. 3-2 based on the orientation of devices:

- Type 1 (T1): Device pin legs face inward toward the center of the PCB as shown in Fig. 3-2(a) [116].
- Type 2 (T2): Device pin legs face outward from the center of the PCB as shown in Fig. 3-2(b) [117].
- Type 3 (T3): Device pin legs face in the same direction as shown in Fig. 3-2(c) [17, 118].
- Type 4 (T4): Devices are arranged in a single-row configuration as shown in Fig. 3-2(d) [81, 119].

For fair comparison, the four layout types shown in Fig. 3-2 follow the same design rules. The discrete devices are closely placed with a minimum clearance sufficient for a V_{DC} of 800 V. The devices' pins are bent 90 degrees into the PCB, making the device bodies lie parallel to the PCB surface. Moreover, the C_{DC} is placed at in a fixed position (bottom of the figure) with a consistent distance from the devices in all types. Additionally, no decoupling capacitors are used. Conventional laminated layout technique is adopted in all layout types for comparison, in which pads are connected by large pieces of polygon.

In addition to layout types, as depicted in Fig. 3-3, the arrangement of paralleled discrete devices can be classified into two categories:

- Sequential (Seq): Devices from the same switching position are grouped together (e.g., …, HS, HS, LS, LS, …) as shown in Fig. 3-3(a).

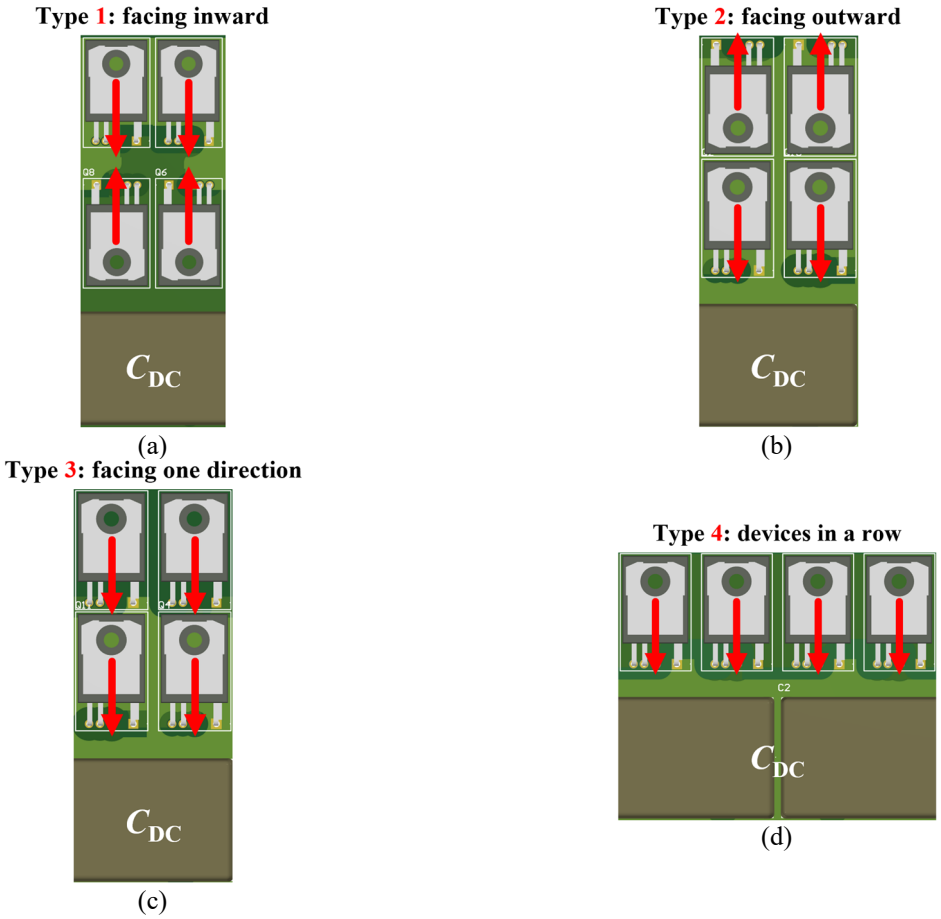


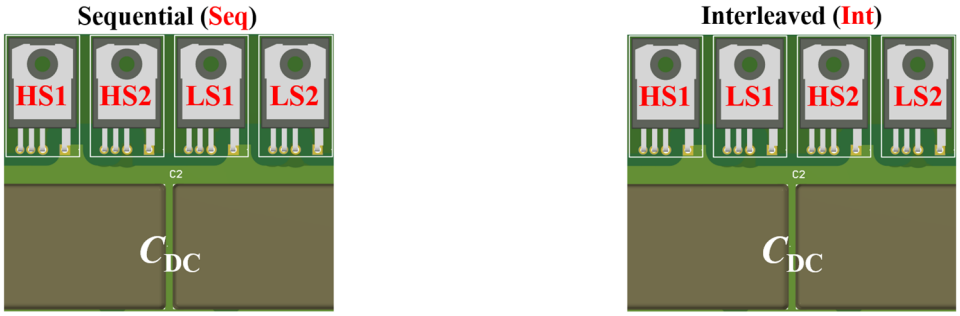
Fig. 3-2 Four layout types based on orientation of paralleled devices.

- Interleaved (Int): Devices from different switching positions are interleaved arranged (e.g., …, HS, LS, HS, LS, …) as shown in Fig. 3-3(b).

Furthermore, as shown in Fig. 3-4, the output node (which is AC node in Fig. 3-1) of a HB can be placed in two different positions:

- Centered (C): The AC connection is located at the center position as shown in Fig. 3-4(a).
- Sided (S): The AC connection is located at the side of the board as shown in Fig. 3-4(b).

In the following sections, layout combinations are abbreviated using the format of: Type–AC locations–Device arrangement. For example, the short of layout combination using Type 1, centered AC location, and interleaved arrangement is denoted as T1-C-Int.



(a) (b)

Fig. 3-3 Two arrangements of paralleled devices in (a) sequential arrangement and (b) interleaved arrangement.

(a) (b)

Fig. 3-4 Two positions of output AC terminal when placing (a) centered and (b) sided.

3.1.2 Comparisons of Parasitic L_{loop} and Overlapping Capacitances

To compare L_{loop}, Fig. 3-5 depicts the circuit diagram based on Fig. 3-1 with individual layout-generated parasitic, using two paralleled devices in each switching position as an example. During switching transients, the high-frequency commutation current tends to find the shortest conducting path to the C_{DC}, and the effective mitigation of L_{loop} relies on the direction of current flow. As presented in Fig. 3-6(a), when currents i_1 and i_2 flow through a pair of closely spaced, paralleled conductors, the generated fluxes reinforce each other, resulting in a positive mutual inductance M_{12} between two conductors. The equivalent inductance $L_{1,eq}$ and $L_{2,eq}$ of the conductors can be expressed as:

$$\begin{cases} L_{1,eq} = L_1 + M_{12} \\ L_{2,eq} = L_2 + M_{12} \end{cases} \tag{3.1}$$

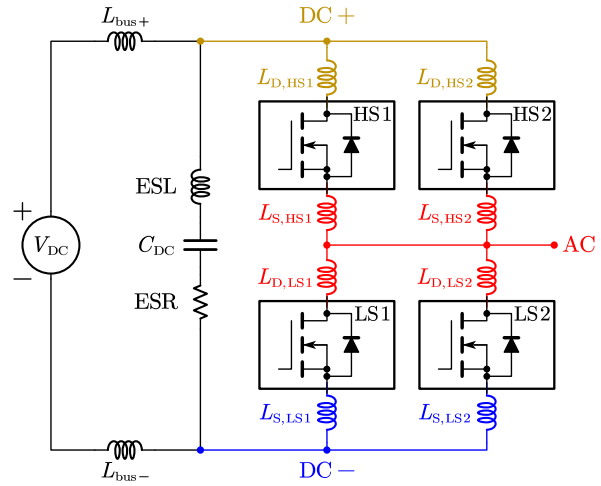


Fig. 3-5 HB circuit with individual parasitic inductances.

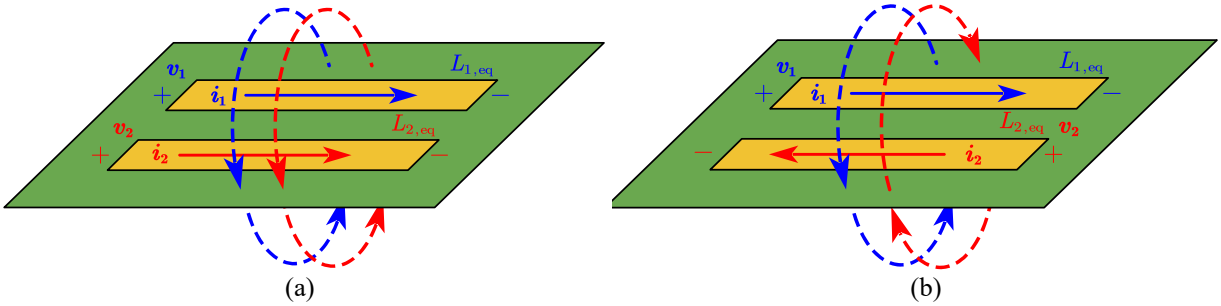


Fig. 3-6 Relationship between current direction and generated fluxes.

where L_1 and L_2 are the self-inductances. If the currents in the two conductors flow in opposite direction as illustrated in Fig. 3-6(b), the M_{12} becomes negative due to opposing fluxes generated. In this case, the equivalent $L_{1,eq}$ and $L_{2,eq}$ can be written as:

$$\begin{cases} L_{1,eq} = L_1 - M_{12} \\ L_{2,eq} = L_2 - M_{12} \end{cases} \tag{3.2}$$

Based on the above characteristics, the layout's L_{loop} is mainly influenced by the devices' arrangement. Fig. 3-7 shows two layout configurations: T1-C-Seq and T1-C-Int, showing both 3D views and internal structure layers. Both layouts follow the circuit in Fig. 3-5, using the same capacitor with a fixed distance from the power devices. In Fig. 3-7(a) and (b), the C_{DC} has the same distance to power devices, implying that the self-inductances from both DC+ (brown) and DC- (blue) layers are similar for two configurations. In addition, the adjacent laminated DC+ and DC- layers largely overlap, generating negative mutual inductance due to opposite current direction.

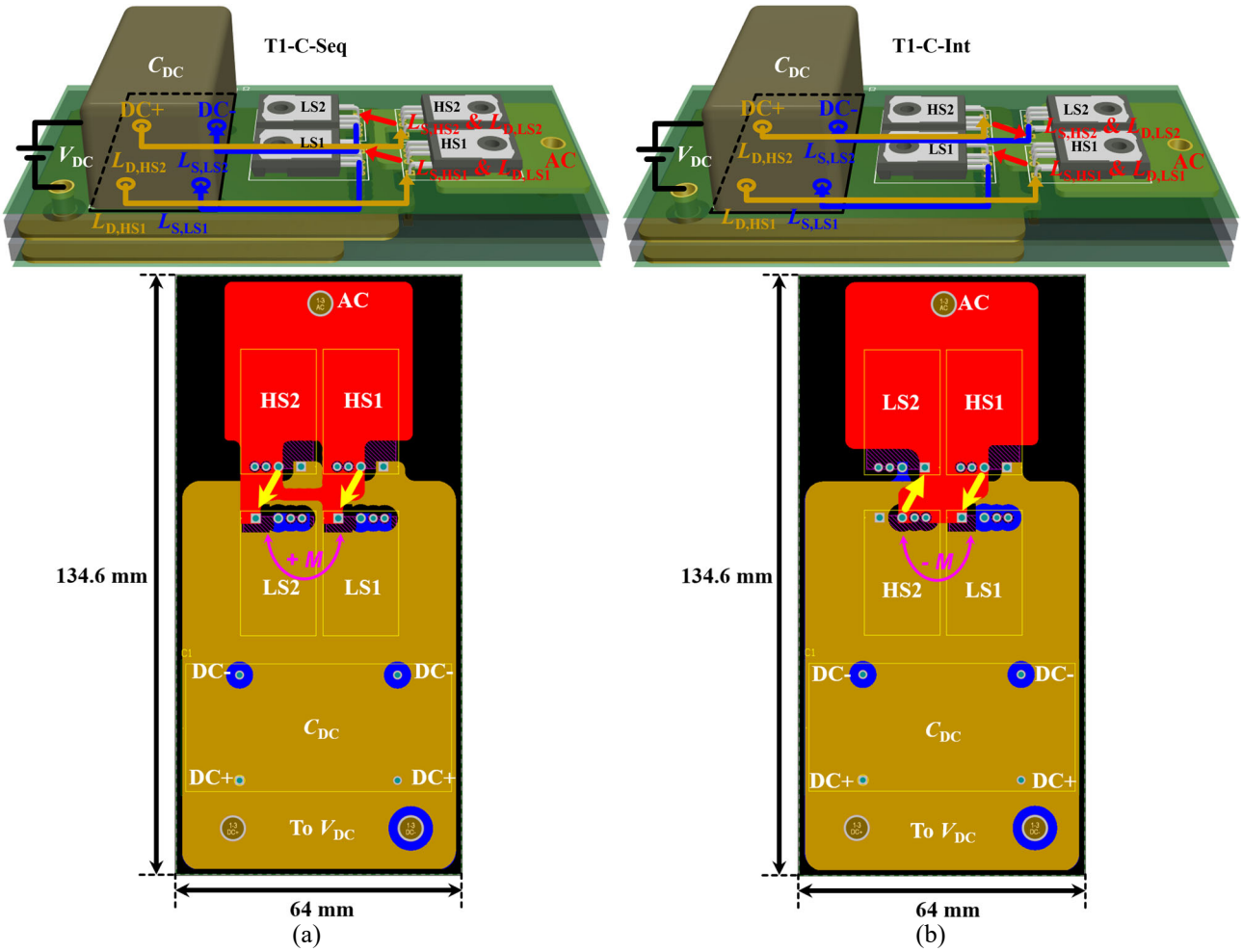


Fig. 3-7 For L_{loop} comparison, layout example of T1-C with (a) sequential arrangement (b) interleaved arrangement.

The key difference arises from the device arrangement. In Fig. 3-7(a), the sequential arrangement places HS and LS in separate groups, causing commutation currents from HS devices to LS devices to flow in the same direction. This lead to positive mutual inductance between paralleled AC branches ($L_{S,HS1}$ to $L_{D,LS1}$ and $L_{S,HS2}$ to $L_{D,LS2}$), increasing the total L_{loop}. Conversely, Fig. 3-7(b) adopts interleaved arrangement, where commutation currents in paralleled AC branches flow in opposite direction. This generate a negative mutual inductance, reducing L_{loop}.

Fig. 3-8 compares the L_{loop} from different layout combinations. Normalized values are presented to highlight relative relationships between cases, as absolute values depend on number of paralleled devices. The L_{loop} values are extracted from Q3D simulations. Obviously, for any given layout type, the interleaved arrangement always yields a lower L_{loop} than the sequential arrangement. Among different layout types, T4 exhibits the highest L_{loop} especially under

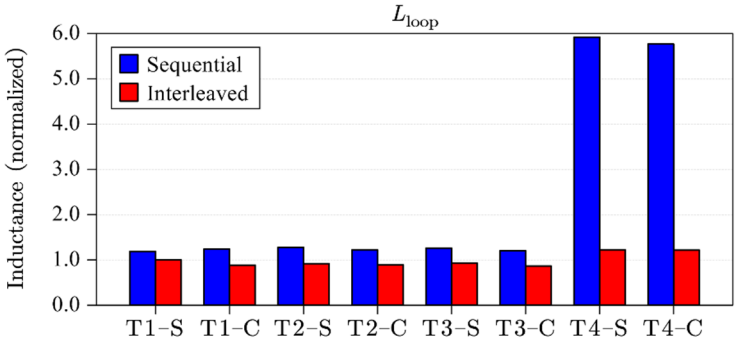


Fig. 3-8 Comparison of L_{loop} across different layout combinations.

sequential arrangement. In contrast, T1, T2, and T3 with interleaved arrangement yeild the lowest L_{loop} across all combinations. Moreover, the L_{loop} in centered terminal is slightly better than that of sided one due to slight shorter and more uniform distance to all paralleled devices, though the improvement is relatively marginal.

On the other hand, the layout-generated C_{HS} and C_{LS} should be minimized to prevent additional losses. The overlapping C between each pair of potential layers in the layout can be expressed as:

$$C = \frac{\varepsilon \cdot A}{d} \tag{3.3}$$

where ε is permittivity of the material, the A and d are the overlapping area and distance between layers, respectively. According to (3.3), the capacitance can be reduced by increasing distance d and decreasing overlapping A. In the PCB design, the distance d is typically fixed by board thickness and clearance requirements, making overlapping A the dominant factor that determines the overlapping C among various layout types.

Fig. 3-9 compares the overlapping A in four layout types. The ranking from highest to lowest is: T2 > T3 > T1 > T4. In T2 and T3, because the pin legs of different devices are positioned far apart from each other, large areas of polygons are required for connection and consequently creating great overlapping A. In T1, the overlapping A is mainly determined by the spacing between upper and lower rows of devices. By contrast, T4 has the smallest overlapping A since the pin legs are close to the C_{DC}, eliminating the need for DC layer polygons to extend into the middle of PCB.

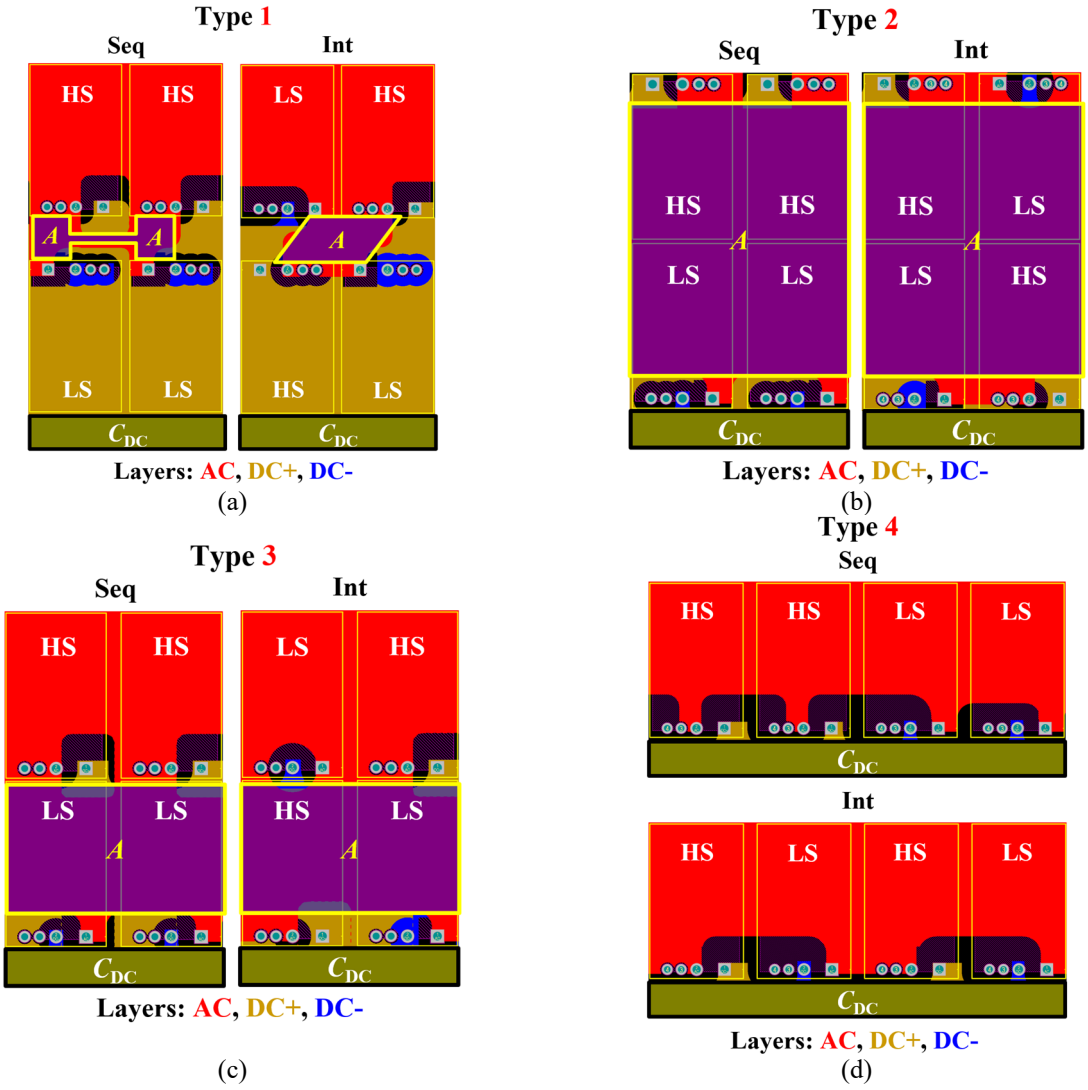


Fig. 3-9 For overlapping C comparison, the overlapping area between AC layer and DC layers in layout (a) Type 1, (b) Type 2, (c) Type 3, and (d) Type 4.

With the aid of Q3D simulations, the normalized overlapping C_{HS} and C_{LS} are presented in Fig. 3-10. The results align with the overlapping A shown in Fig. 3-9, where T1 and T4 have much smaller C_{HS} and C_{LS} than T2 and T3. In addition, the interleaved arrangement generally has higher overlapping C than the sequential arrangement, since in the sequential case only one of the DC+ or DC- layers overlaps with the AC layer.

By combining results from Fig. 3-8 and Fig. 3-10, the optimal combination for minimizing both L_{loop} and overlapping C is identified as T1-C-Int. Specifically, the interleaved arrangement reduces L_{loop} by 28.58 % compared with that of the typical sequential arrangement, while the overlapping C is suppressed by 93.3 % and 87.23 % relative to T2 and T3, respectively. Though the choice

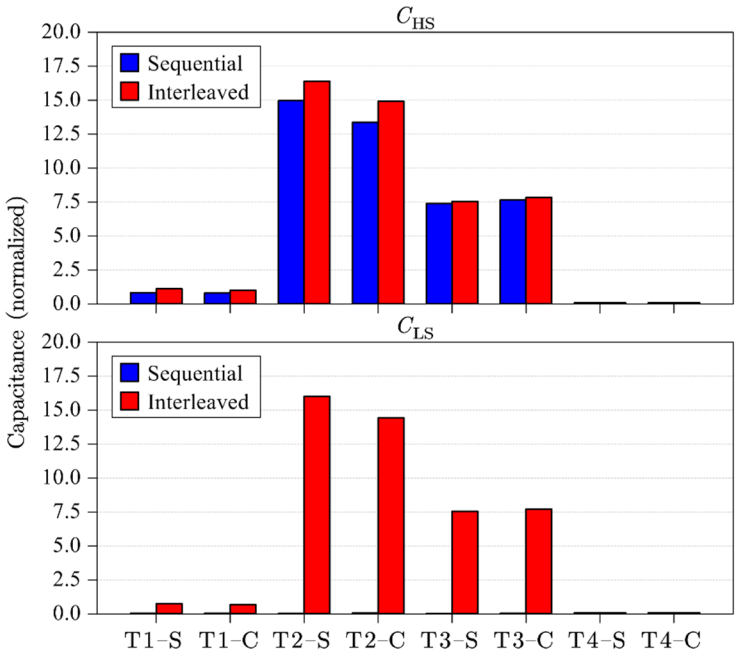


Fig. 3-10 Comparison of overlapping C across different layout combinations.

between centered or sided terminal has little impact on L_{loop} or overlapping C, the centered terminal is preferred due to the more uniform and slightly shorter distance to all paralleled devices.

The layout example of T1-C-Int is presented in Fig. 3-7(b), where the conventional laminated layout technique is employed, connecting all pads using large copper polygons. The equivalent circuit of this technique is previously presented in Fig. 3-5. However, it is evident that the conventional laminated layout technique introduces unbalanced parasitic among the parallel traces, especially devices in the interleaved arrangement. According to the current sharing analysis, the asymmetric drain and source in Fig. 3-7(b) can cause unbalanced current sharing in both static and dynamic regions.

3.2. Passive Solution I: Distributed-Block (DB) Layout

3.2.1 Concept of DB Layout

To mitigate the asymmetric parasitic, a novel distributed-block (DB) layout concept is proposed in this section. Fig. 3-11 shows the layout example of optimal T1-C-Int by implementing the proposed DB layout concept [120], and its equivalent circuit is depicted in Fig. 3-12. In the proposed layout concept, each node (AC, DC+, and DC- layers) first routes to the middle point

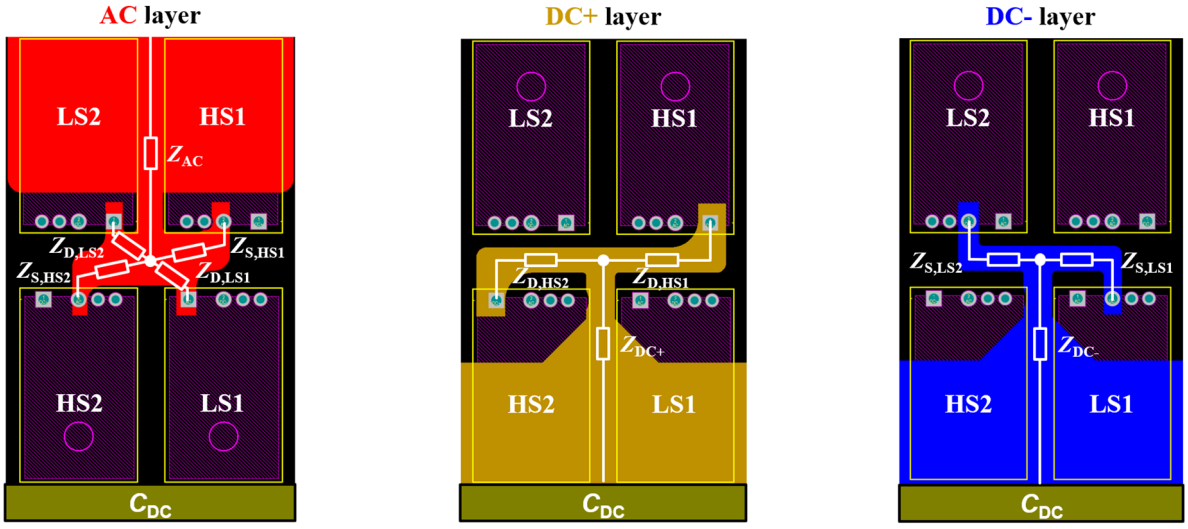


Fig. 3-11 Proposed distributed-block layout concept using T1C-C-Int as an example, internal layers of (a) AC, (b) DC+, and (c) DC-.

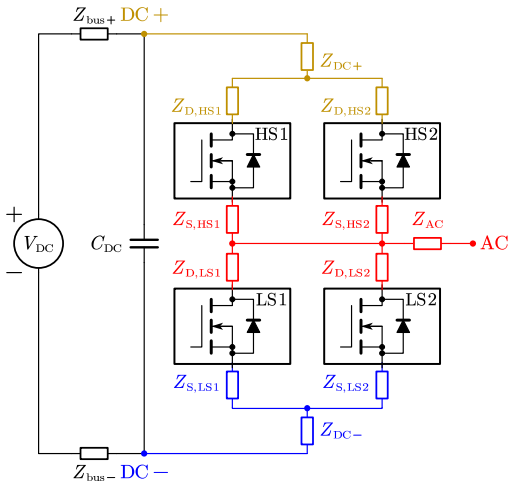
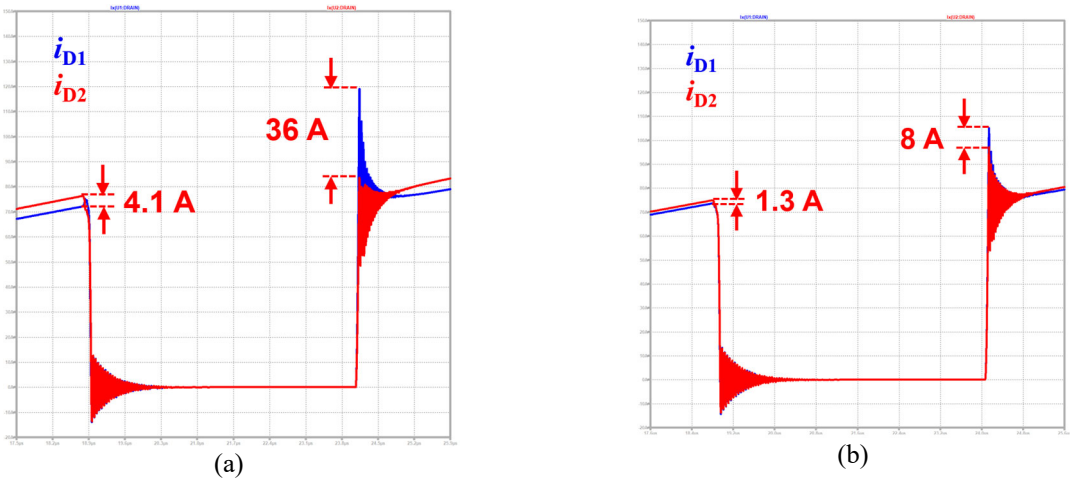


Fig. 3-12 Equivalent circuit diagram by using the proposed DB layout concept.

between paralleled devices, and then branches out to distribute current to each device individually. Compared to the circuit and layout using conventional laminated layout technique in Fig. 3-5 and Fig. 3-7(b), the proposed DB layout significantly minimizes mismatches in ΔZ_D and ΔZ_S, while maintaining optimal device arrangement to achieve minimal L_{loop} and overlapping C. According to Q3D simulations, Table 3-1 summarizes the normalized parasitic parameters of the proposed DB layout in Fig. 3-11, against the conventional layout in Fig. 3-7(b). Obviously, the mismatched parasitic in proposed layout concept are greatly reduced. Additionally, L_{loop} and overlapping C_{HS} and C_{LS} remain nearly unchanged. As a trade-off, the spacing between devices in the DB layout slightly increases by 16 % to accommodate the distributed routing traces.

TABLE 3-1 COMPARISON OF CONVENTIONAL LAYOUT AND PROPOSED LAYOUT

Parameters	Normalized values	
	Conventional Laminated Layout	Proposed DB Layout
ΔL_D	1 nH	0.596 nH
ΔR_D	1 mΩ	0.475 mΩ
ΔL_S	1 nH	0.195 nH
ΔR_S	1 mΩ	0.054 mΩ
L_{loop}	1 nH	0.984 nH
C_{HS}	1 pF	1.01 pF
C_{LS}	1 pF	0.98 pF
Footprint area	1 mm^2	1.16 mm^2



(a) (b)

Fig. 3-13 DPT waveforms from circuit-level simulations in LTspice based on the circuit parameters of (a) conventional laminated layout technique and (b) proposed DB layout concept

By implementing the parasitic parameters in Table 3-1 into LTspice, Fig. 3-13 shows the DPT waveforms of the proposed DB layout comparing to conventional laminated layout under the same conditions. The employed SiC MOSFETs are C3M0016120K from Wolfspeed, with i_{load} of 150 A (75 A/each MOSFET). Despite having identical $R_{DS,on}$ and threshold voltage V_{th} in the simulations, in Fig. 4-13(a), the peak current differences between paralleled devices are 4.1 A in static region and 36 A in the dynamic region. The result clearly demonstrates that parasitic mismatches introduced by the conventional laminated layout technique must be minimized. On the other hand, by adopting proposed DB layout in Fig. 3-13(b), the peak current differences greatly decreased to 1.3 A in static region and 8 A in dynamic region. The slight current imbalance remains due to mutual inductance effects. In overall, the circuit-level simulations verify the efficacy of the proposed DB layout concept, improving both static and dynamic current sharing by mitigating asymmetric drain and source parasitic.

3.2.2 Experimental Validation of DB Layout

To verify the current sharing improvement achieved by the proposed layout, two versions of HB PCBs are designed. The HB-base shown in Fig. 3-14 adopts the conventional laminated layout technique, serving as the baseline design for comparison. On the other hand, an all-in-one HB PCB is designed in Fig. 3-15, implementing the proposed DB layout concept.

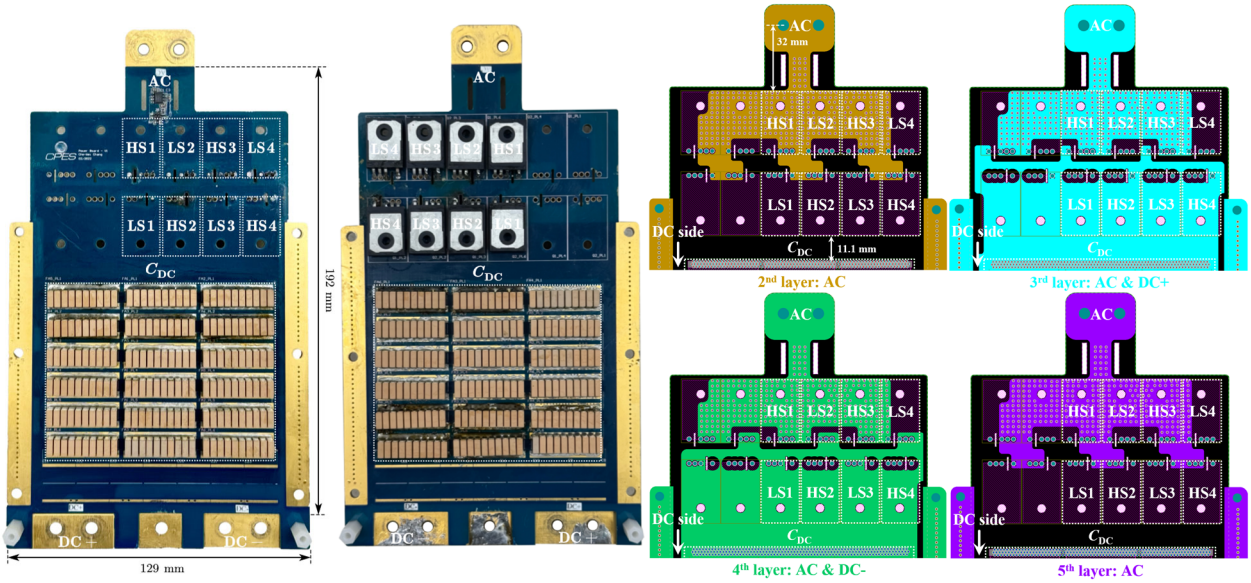


Fig. 3-14 Layout design of the baseline design HB-base which adopts the conventional laminated layout technique.

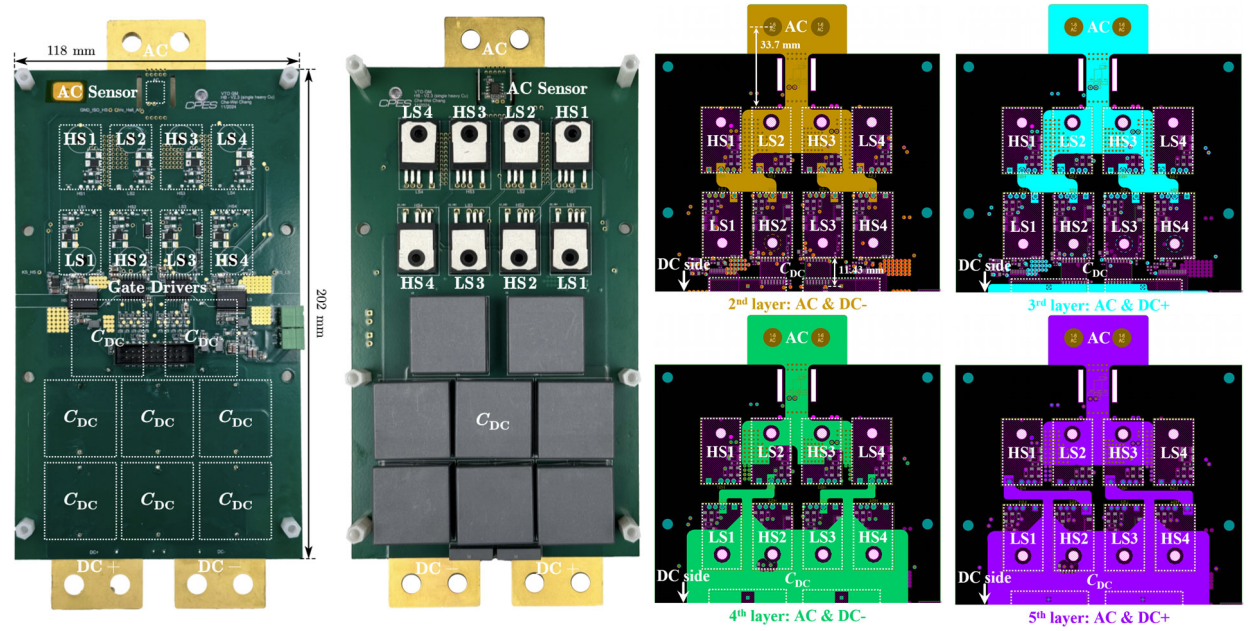


Fig. 3-15 Layout design of the all-in-one HB PCB which adopts the proposed DB layout concept for improving current sharing.

Both HB-base and all-in-one HB follow the HB circuit shown in Fig. 3-1, consisting of C_{DC}, four paralleled devices at both HS and LS positions, and copper busbars for DC+, DC-, and AC nodes. Both designs employ a 6-layer PCB structure, with 1 oz copper for the outer layers (top and bottom) and 16 oz copper for the four inner layers. The optimal T1-C-Int layout is adopted in both versions.

For HB-base in Fig. 3-14, the power devices are driven by a separate gate driver board mounted on top of the power PCB and soldered directly to the device pin legs. The vertical gap between the two boards is less than 1 mm, minimizing the gate driving loop. The CeraLink FA10 series capacitors are used as C_{DC}, mounted on both sides of the PCB. The distance from power devices to the nearest capacitor pad is around 11.1 mm, and the distance to the AC terminal is about 32 mm. For the layer stack-up, the top and bottom layers are thin copper for the exposed pads of C_{DC}, while the inner layers are heavy copper to carry high currents on DC+, DC-, and AC layers. In HB-base, it can be clearly seen that all pads and vias are connected by pouring large-area polygons, in line with the conventional laminated layout technique.

The all-in-one HB PCB shown in Fig. 3-15 adopts the proposed DB layout concept, with key polygon layers highlighted. The distances from the devices to the nearest capacitor pin and to AC terminal are similar to HB-base, approximately 11.43 mm and 33.7 mm, respectively. Like HB-base, the inner heavy copper layers are DC+, DC-, and AC high-current paths. However, rather than directly pouring large polygons, the routing in all-in-one HB PCB first reaches the midpoint between the paralleled devices, then distributes to each device individually. Compared to HB-base, the device spacing is slightly increased to accommodate the distributed routings. In all-in-one HB PCB, the gate driving components are integrated on the top surface of the PCB.

Although HB-base uses a separate gate driver board, its gate driver circuitry and layout are completely identical to those of all-in-one HB PCB. Moreover, as shown in Fig. 3-16, the distance between the gate driver board and HB-base is less than 1 mm, which barely has impact on current sharing performance. Furthermore, the distances from the power devices to the nearest dc-link capacitor pads are nearly identical in both HB-base and all-in-one HB PCB, despite difference capacitor packages being used. Since current sharing is primarily influenced by layout-induced parasitic mismatches, the choice of capacitor has minimal impact.

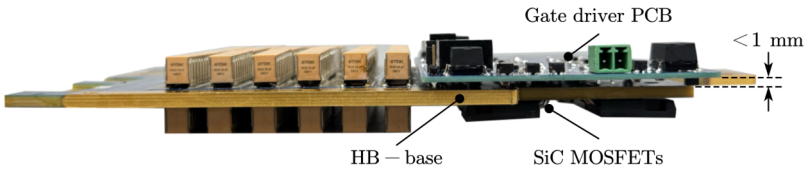
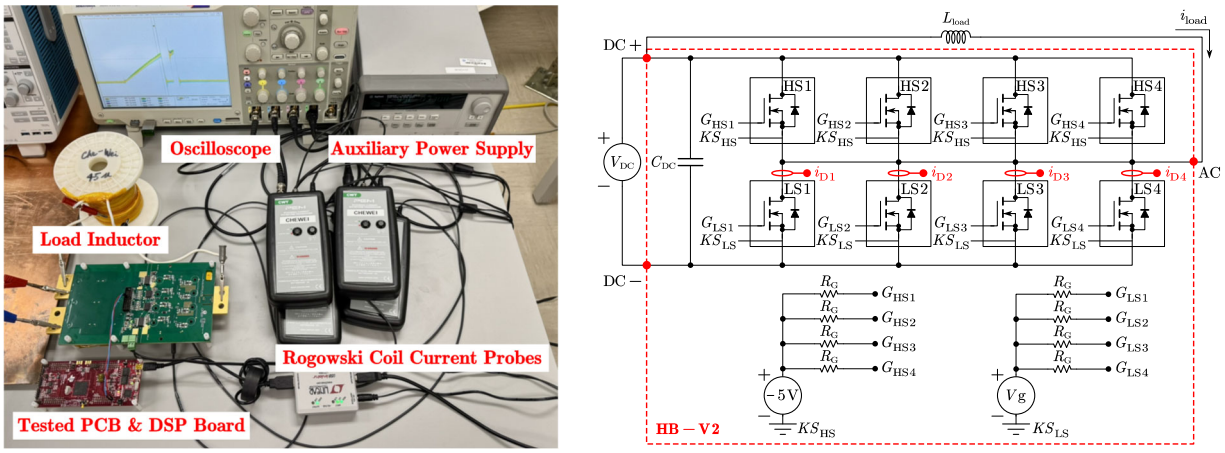


Fig. 3-16 Side view of HB-base driven by a separate gate driver board.

An 800-V DPT environment is established in Fig. 3-17. Both HB-base and all-in-one HB PCB are tested under the same testing conditions for current sharing comparison. All parameters are listed in Table 3-2. The SiC MOSFET IMZA120R007M1H from Infineon is employed as paralleled devices at both HS and LS positions. The HS devices are turned off by -5 V and act as freewheeling diodes, while the LS devices are driven by pulse gate voltage V_g. As previously shown in Fig. 2-5 and Fig. 2-6, the IMZA120R007M1H from Infineon demonstrates a good consistency among individual devices. Those devices with close $R_{DS,on}$ and V_{th} are employed on tested PCBs, eliminating the concern of mismatched devices. Each device has its own gate resistance R_G of 10 Ω. A load inductor L_{load} is connected between DC+ and AC terminals of the test PCB, supplying a total load current i_{load} of 300 A (75 A/device). Four Rogowski coil current probes CWTUM/3/B with bandwidth of 30 MHz are used to measure the i_D of four paralleled LS devices.



(a) (b)

Fig. 3-17 DPT (a) test setup (b) circuit diagram.

TABLE 3-2 EXPERIMENTAL TESTING CONDITIONS IN FIG. 3-17

Symbols	Values
V_{DC}	800 V
C_{DC}	108 µF
L_{load}	45 µH
i_{load}	300 A
SiC MOSFET	IMZA120R007M1H
V_g	18 V/-5 V
R_G	10 Ω

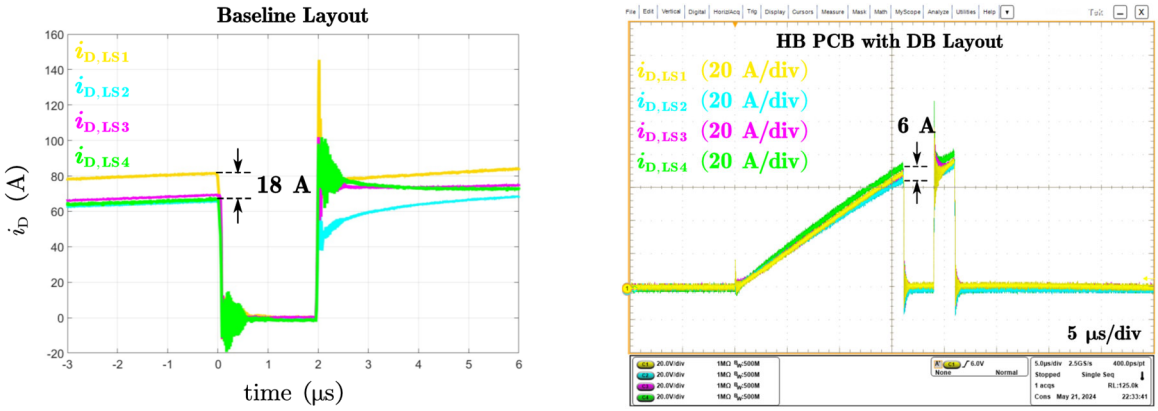


Fig. 3-18 Static current sharing of (a) HB-base using conventional laminated layout technique (b) all-in-one HB with proposed DB layout concept.

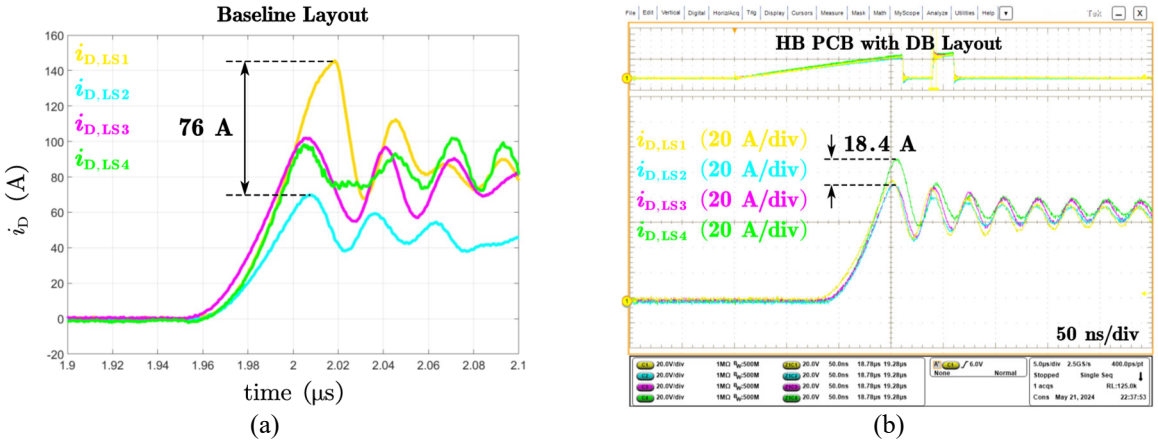


Fig. 3-19 Turn-on dynamic current sharing of (a) HB-base using conventional laminated layout technique (b) all-in-one HB with proposed DB layout concept.

Fig. 3-18 compares the static current sharing of two layouts. For HB-base, which uses conventional laminate layout technique, the peak static current difference Δi_D is 18 A. In contrast, the all-in-one HB PCB which adopts the proposed DB layout has a peak static Δi_D of only 6 A, attributed to the minimized drain and source parasitic.

Fig. 3-19 presents the dynamic current sharing during the turn-on transient. Due to the same operating conditions and R_G, the switching speeds of both cases are identical. The results show that all-in-one HB exhibits a peak dynamic Δi_D of 18.4 A, substantially lower than the 76 A observed in HB-base. This improvement is primarily due to balanced source parasitic, while the remaining current mismatch may be caused by mutual inductance effects and slight variations among paralleled devices.

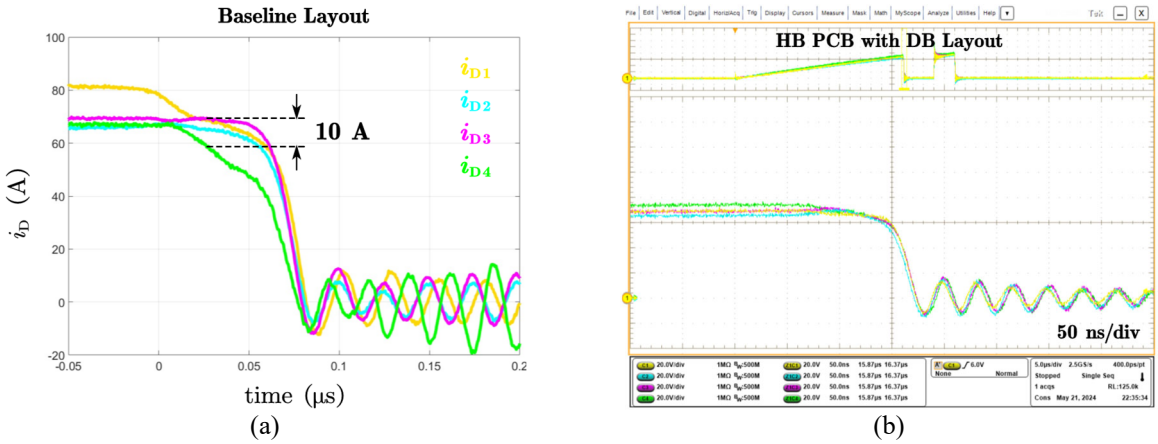


Fig. 3-20 Turn-off dynamic current sharing of (a) HB-base using conventional laminated layout technique (b) all-in-one HB with proposed DB layout concept.

Finally, Fig. 3-20 shows the dynamic current sharing during turn-off transient. Once again, in all-in-one HB, four turn-off currents are almost balanced with negligible difference. Conversely, HB-base has a peak Δi_D of approximately 10 A. The experimental results verify the effectiveness of the proposed DB layout concept in improving current sharing, while maintaining optimal layout configuration for minimal L_{loop} and overlapping C, with a slight penalty of 16 % larger footprint area as a trade-off.

Though the proposed DB layout concept significantly improves current sharing performance, slight asymmetric parasitic caused by mutual inductance still exists. To further enhance dynamic current sharing, a DMC gate driver is proposed in the next section to suppress Δi_G.

3.3. Passive Solution II: Differential-Mode-Choke (DMC) Gate Driver

Following the development process, the DMCs are integrated into the gate driver to suppress Δi_G. Instead of adding components into the power loop which affects L_{loop} and thermal performance [84], integrating chokes or coupled inductors into the gate driver can be an attractive solution. In [121], two common mode chokes (CMC) are added to the gate driver for two paralleled IGBTs to balance the dynamic collector currents. This approach has been extended to paralleled SiC MOSFETs to suppress voltage oscillation [122] and balance dynamic currents [123]. While effective for current balancing, the leakage inductance and winding resistance in the KS connection may weaken crosstalk protection for high-switching speed SiC MOSFETs. In [124], a

DMC is placed at the gate driving node for paralleled IGBTs to improve switching performances. Subsequently, [125] presents a comparison of DMC gate driver with various gate driving structures. In [126], the functionality of DMC gate driver is evaluated for paralleled SiC MOSFETs for the first time. However, due to the absence of mathematical model, the results in above studies can only be qualitative, and the magnetizing inductance of the DMC is immensely large. Moreover, a comprehensive analysis that aids engineers in implementing the method is still missing. Furthermore, the evaluation of DMC gate driver for multiple paralleled SiC MOSFETs remains unclear. This section endeavors to cover this gap, and a comprehensive analysis is presented.

3.3.1 Modeling of DMC Gate Driver

Based on the model in Fig. 2-8, the feedback mechanism from asymmetric layout to unbalanced Δi_G is the root cause of the unbalanced dynamic current sharing. To balance the gate currents, Fig. 3-21(a) depicts the DMC gate driver structure by inserting a DMC at the gate driving node [127]. When the gate currents are well-balanced, the magnetic flux of the DMC equals 0. If the gate charging currents become unbalanced due to mismatched layout, according to the dot convention, the induced voltages on parallel gate paths are opposite which help regulate the Δi_G. Once the gate charging currents are balanced, the channel currents are automatically balanced. This solution has no impact on the power loop and common-mode gate current components. The DMC provides impedance to suppress unbalanced Δi_G while the switching speed is still determined by the R_G.

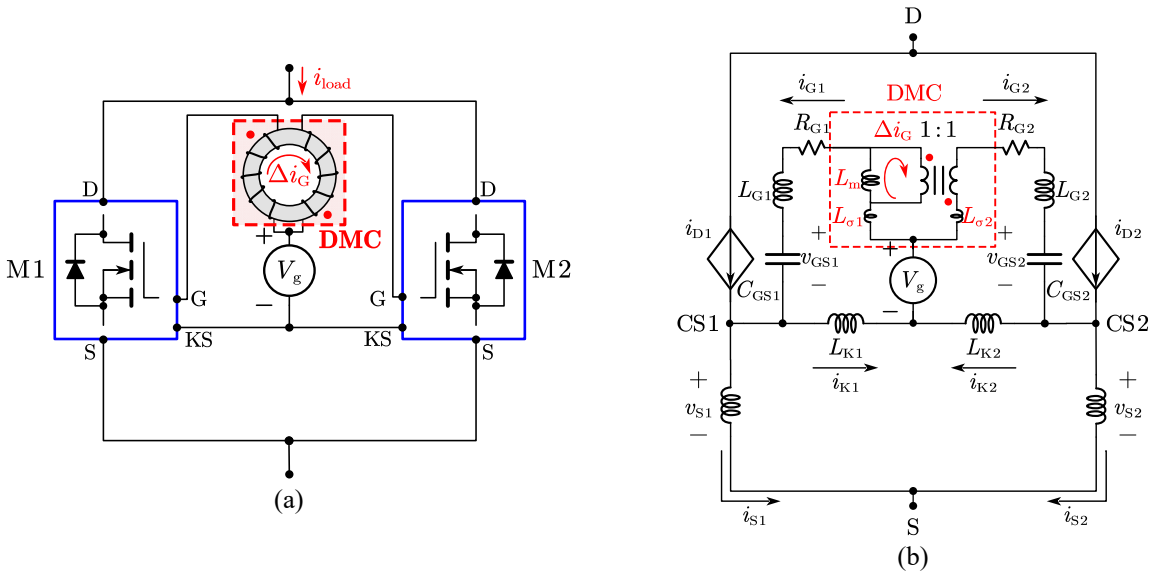


Fig. 3-21 The DMC gate driver (a) structure and (b) equivalent circuit diagram.

Fig. 3-21(b) shows the equivalent circuit diagram of the DMC gate driver. The L_{m} and L_{σ} are the magnetizing and leakage inductances, respectively. The mathematical expression in (2.1) is still used for mathematical derivations. Based on Fig. 3-21(b), the relationship of gate driving loops can be derived by applying KVL:

$$\begin{cases} V_{\mathrm{g}} = (L_{\sigma 1} + L_{\mathrm{G}1}) \dfrac{di_{\mathrm{G}1}}{dt} + L_{\mathrm{m}} \dfrac{d\,\Delta i_{\mathrm{G}}}{dt} + R_{\mathrm{G}1} i_{\mathrm{G}1} + v_{\mathrm{GS}1} + L_{\mathrm{K}1} \dfrac{di_{\mathrm{K}1}}{dt} \\ V_{\mathrm{g}} = (L_{\sigma 2} + L_{\mathrm{G}2}) \dfrac{di_{\mathrm{G}2}}{dt} - L_{\mathrm{m}} \dfrac{d\,\Delta i_{\mathrm{G}}}{dt} + R_{\mathrm{G}2} i_{\mathrm{G}2} + v_{\mathrm{GS}2} + L_{\mathrm{K}2} \dfrac{di_{\mathrm{K}2}}{dt} \end{cases} \tag{3.4}$$

By substituting (2.3) to (2.5) into (3.4) with additional assumption that $L_{\sigma 1} = L_{\sigma 2} = L_{\sigma}$, and combining (2.7) and (2.8) with (3.4), the equivalent circuit model for DMC gate driver:

$$-v_{\mathrm{eq}} = R_{\mathrm{eq}} \Delta i_{\mathrm{G}} + (L_{\mathrm{eq}} + L_{\mathrm{DMC,eq}}) \frac{d\,\Delta i_{\mathrm{G}}}{dt} + \frac{1}{C_{\mathrm{eq}}} \int \Delta i_{\mathrm{G}}\, dt \tag{3.5}$$

where the v_{eq}, R_{eq}, L_{eq}, and C_{eq} remain unchanged with those in equations (2.10). However, an additional term $L_{\mathrm{DMC,eq}}$ appears after adding the DMC into the circuit and can be expressed as:

$$L_{\mathrm{DMC,eq}} = \frac{2(L_{\sigma} + 2L_{\mathrm{m}})\,(\Sigma L_{\mathrm{S}} + \Sigma L_{\mathrm{K}})}{\Sigma L_{\mathrm{K}}} \tag{3.6}$$

The value of $L_{\mathrm{DMC,eq}}$ highly depends on L_{m}. Fig. 3-22 shows the equivalent RLC circuit model using the DMC gate driver based on (3.5) and (3.6). Comparing Fig. 3-22 with the original model in Fig. 2-8, the appearance of $L_{\mathrm{DMC,eq}}$ helps suppress the unbalanced Δi_{G} even when the asymmetric layout exists. Based on Fig. 3-22, the equivalent circuit impedance $Z_{\mathrm{DMC,eq}}$ can be expressed as:

$$Z_{\mathrm{DMC,eq}} = R_{\mathrm{eq}} + j\,\omega\,(L_{\mathrm{eq}} + L_{\mathrm{DMC,eq}}) + \frac{1}{j\,\omega C_{\mathrm{eq}}} \tag{3.7}$$

Fig. 3-23 plots the bode plot of Z_{eq} based on (2.12) in original model, and (3.7) after incorporating the DMC with different L_{m} values. The $L_{\mathrm{S}2}$ is 10 nH higher than $L_{\mathrm{S}1}$ and R_{G} are set as 10 **Ω**. In the original case without DMC, the bode plot behaves like a general RLC circuit, featuring one pole at 0 Hz and two zeros at higher frequencies. The impedance magnitude in the low-frequency range is dominated by the C_{eq}. The impedance magnitude begins to decrease in the mid-frequency range due to the existence of R_{eq}. Beyond the second zero, L_{eq} dominates.

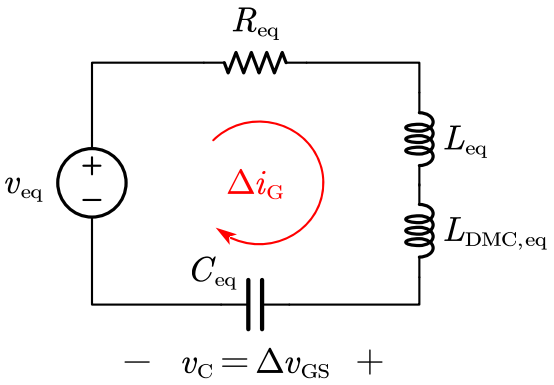


Fig. 3-22 Equivalent time-domain RLC circuit model when adopting the DMC gate driver.

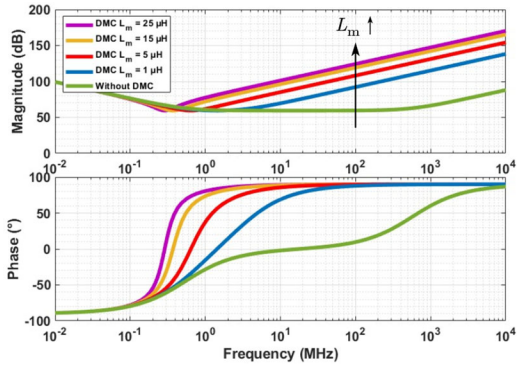


Fig. 3-23 Bode plot before and after adopting the DMC gate driver with different L_m values of DMC.

After adopting the DMC gate driver, in comparison to the original case without the DMC, the impedance magnitude significantly increases, especially in mid to high-frequency range. Both zeros of the system shift to the lower frequency range. Typically, the dynamic region spans only a few dozens of nanoseconds. During this period, the increased impedance magnitude generated by L_m helps suppress the unbalanced Δi_G which further balances the channel currents. The effect of the DMC is positively related to the L_m. The impact of L_m is most pronounced when it increases from 0 μH to 1 μH, whereas the effect is less noticeable when it increases from 15 μH to 25 μH.

The DMC helps balance the dynamic current sharing when inserted in the gate nodes. However, as shown in Fig. 3-24(a), it should avoid placing the DMC at the KS node though this node also belongs to part of the entire gate driving loop. When devices are paralleled, in addition to the gate currents, the currents on the KS paths also include the circulating current from one MOSFET's CS node to another's CS node [128]. The consequence of placing the DMC at KS node is analyzed. Fig. 3-24(b) shows the equivalent circuit diagram of Fig. 3-24(a), the relationships of the driving loops are:

$$\begin{cases} V_g = R_{G1} i_{G1} + L_{G1} \dfrac{di_{G1}}{dt} + v_{GS1} + L_{K1} \dfrac{di_{K1}}{dt} + L_m \dfrac{d\,\Delta i_K}{dt} + L_{\sigma 1} \dfrac{di_{K1}}{dt} \\ V_g = R_{G2} i_{G2} + L_{G2} \dfrac{di_{G2}}{dt} + v_{GS2} + L_{K2} \dfrac{di_{K2}}{dt} - L_m \dfrac{d\,\Delta i_K}{dt} + L_{\sigma 2} \dfrac{di_{K2}}{dt} \end{cases} \tag{3.8}$$

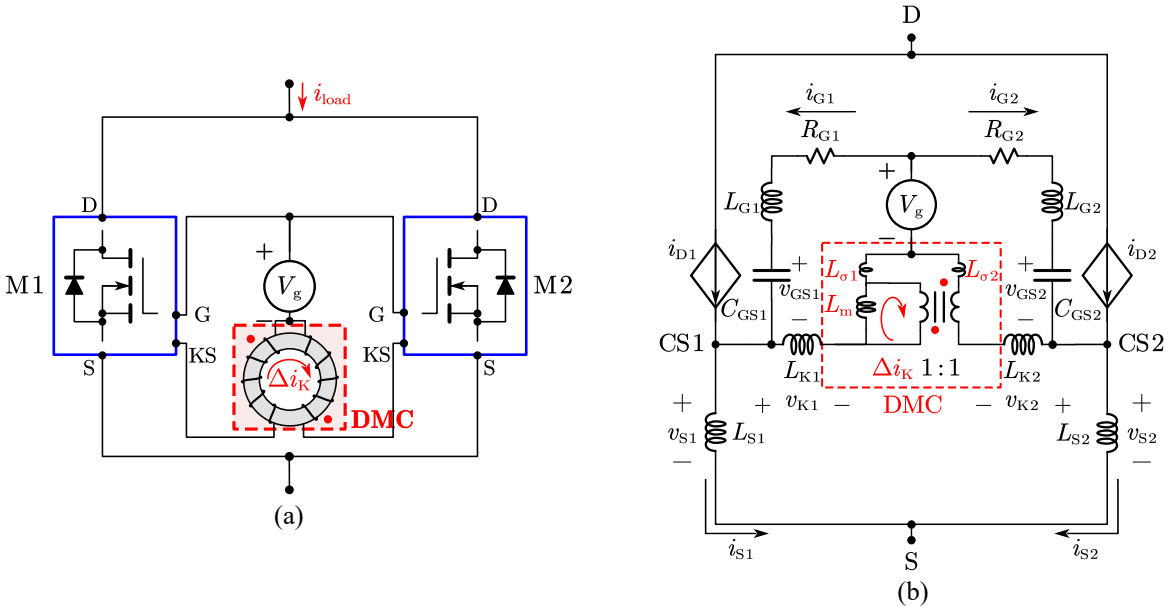


Fig. 3-24 When the DMC is placed at the KS node instead of gate node (a) structure and (b) circuit diagram.

In addition, the KVL of the bottom source-KS loop:

$$\begin{aligned} &L_{S1}\frac{di_{S1}}{dt}+L_{K2}\frac{di_{K2}}{dt}+L_{\sigma 2}\frac{di_{K2}}{dt}-L_m\frac{d\Delta i_K}{dt} \\ &=L_{S2}\frac{di_{S2}}{dt}+L_{K1}\frac{di_{K1}}{dt}+L_{\sigma 1}\frac{di_{K1}}{dt}+L_m\frac{d\Delta i_K}{dt} \end{aligned} \tag{3.9}$$

By following similar deriving process, with the facts that L_m is much larger than $L_{S1}+L_{S2}$ and i_{load} is much greater than i_G, the model when placing DMC at KS node:

$$-v_{DMCK,eq}=R_{DMCK,eq}\Delta i_G+L_{DMCK,eq}\frac{d\Delta i_G}{dt}+\frac{1}{C_{DMCK,eq}}\int\Delta i_G dt \tag{3.10}$$

$$\begin{cases} v_{DMCK,eq}=\Delta L_S\dfrac{di_{load}}{dt}+\left[\dfrac{\Sigma L_S}{\alpha}\Delta L_K+\left(\dfrac{\Sigma L_S}{\alpha}+1\right)\Delta L_G\right]\dfrac{d\Sigma i_G}{dt} \\ R_{DMCK,eq}=\dfrac{g_m\Sigma L_S}{C_{GS}}+(1+\dfrac{\Sigma L_S}{\alpha})2R_G \\ L_{DMCK,eq}=\Sigma L_S+\left(1+\dfrac{\Sigma L_S}{\alpha}\right)\Sigma L_G \\ C_{DMCK,eq}=\dfrac{\alpha C_{GS}}{2(\alpha+\Sigma L_S)} \\ \alpha=\Sigma L_K+4L_m+2L_\sigma \end{cases} \tag{3.11}$$

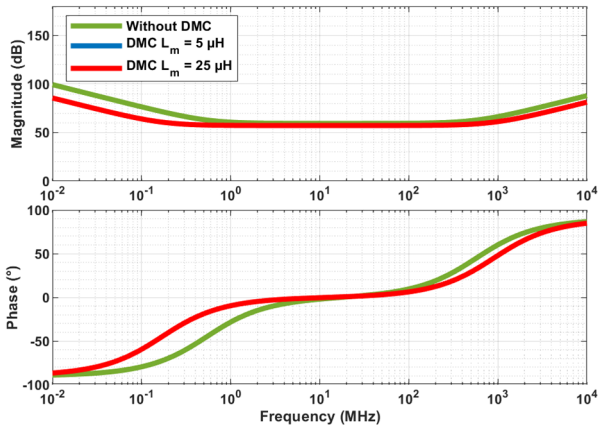


Fig. 3-25 The equivalent impedance bode plot when the DMC is placed at the KS node.

$$Z_{\mathrm{DMCK,eq}} = R_{\mathrm{DMCK,eq}} + j\omega L_{\mathrm{DMCK,eq}} + \frac{1}{j\omega C_{\mathrm{DMCK,eq}}} \tag{3.12}$$

From (3.11) and (3.12), an increase in L_{m} results in a decrease in circuit impedance $Z_{\mathrm{DMCK,eq}}$ which worsens dynamic current sharing. Fig. 3-25 shows the bode plot when the DMC is placed at KS node. The impedance magnitude becomes even lower when the DMC is placed at KS node. The curves when L_{m} equals to 5 μH and 25 μH nearly overlap. Clearly, the DMC should not be placed at the KS node to prevent worsening dynamic current sharing.

Fig. 3-26 presents the proof-of-concept simulation adopting the proposed current balancing gate driver. The L_{S2} is set to be 10 nH higher than L_{S1} and R_{G} is 10 Ω. The DMC with L_{m} of 5 μH and 25 μH are added into the circuit. As shown in Fig. 3-26, the dynamic currents are much more balanced after the DMC is added, with the Δi_{G} being effectively suppressed by DMC. The currents are even balanced when the L_{m} is increased to 25 μH.

Fig. 3-27(a) further compares the simulated and modeled Δi_{G} with difference L_{m} values. The waveform of the modeled Δi_{G} aligns perfectly with the real Δi_{G} during switching transient, verifying the accuracy of the derived model. Fig. 3-27(b) shows the degree of peak current difference γ under difference L_{m} values. The γ is defined as:

$$\gamma = \frac{|\Delta i_{\mathrm{D,pk,DMC}}|}{|\Delta i_{\mathrm{D,pk,no\ DMC}}|} \times 100 \tag{3.13}$$

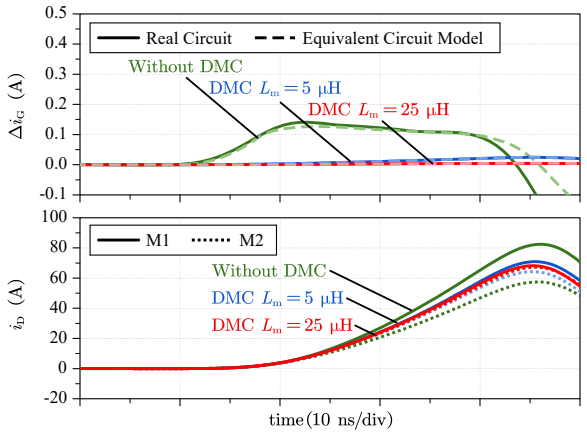


Fig. 3-26 Simulation results after utilizing the DMC gate driver with fixed R_G and ΔL_S.

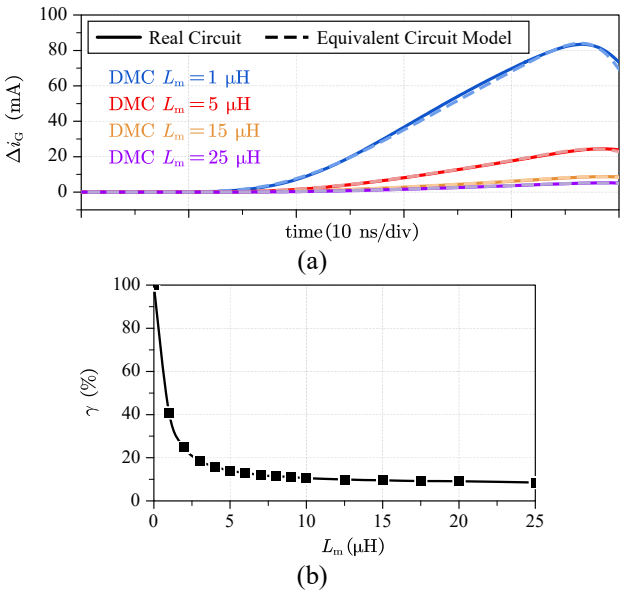


Fig. 3-27 The (a) time-domain comparison of simulated and modeled Δi_G with different L_m (b) degree of peak current difference after adopting DMC gate driver.

The result aligns with the analysis in Fig. 3-23 that the effect of DMC is less pronounced as L_m increases. The γ becomes relatively stable when L_m is larger 20 μH.

The DMC gate driver helps balance the currents from the mismatched layout. However, in real-world applications, mismatches in layout, device, or gate driving delay may occur simultaneously. Fig. 3-28 shows the simulation waveforms of possible worst-case scenario when L_{S1} is 5 nH smaller than L_{S2}, V_{th1} is 0.2 V smaller than V_{th2}, C_{GS1} is 200 pF smaller than C_{GS2}, and the gate driving signal arrives at M1 5 ns earlier than M2, implying that M1 will turn on sooner and faster than M2. After adding a 10 μH DMC, since the gate charging currents are forced to be balanced, M1 with a lower V_{th} still turns on earlier than M2. Nevertheless, during the current rise period, the DMC helps suppress the unbalanced currents caused by mismatched layout, reducing the degree of Δi_D by 46 % compared to the original waveforms. This result also suggests that, under the same switching frequency and operating conditions, the PTC of $R_{DS,on}$ has a higher probability of counteracting the NTC of V_{th}, thereby helping to prevent thermal runaway.

3.3.2 Experimental Validation of DMC Gate Driver

The DMC is soldered on the PCB as shown in Fig. 3-30 to verify the DMC gate driver, and the circuit and test environment are shown in Fig. 2-17(a) and (b). The paralleled devices at LS

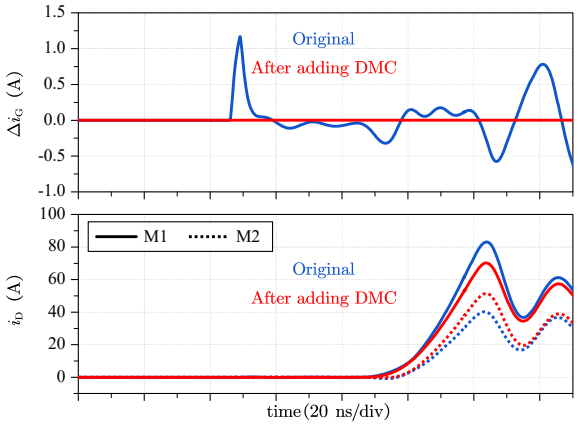


Fig. 3-28 Simulation results of possible worst-case scenario considering combined mismatches in layout, devices, and driving signals.

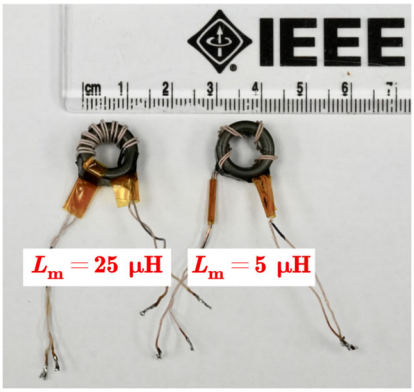


Fig. 3-29 The DMC with bifilar winding structure.

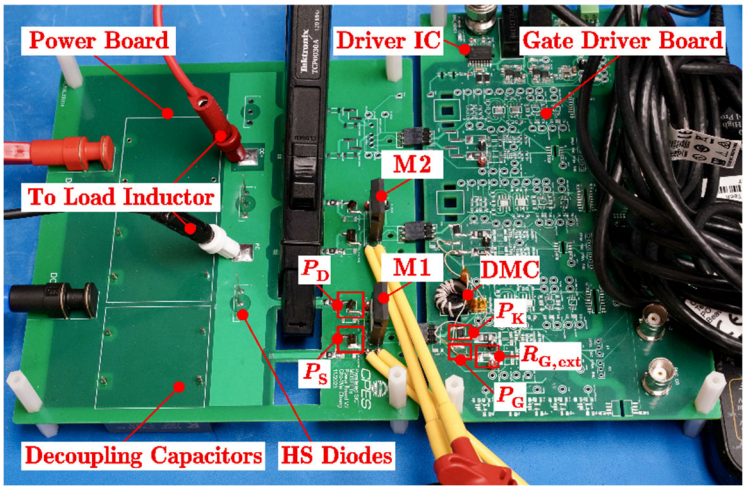
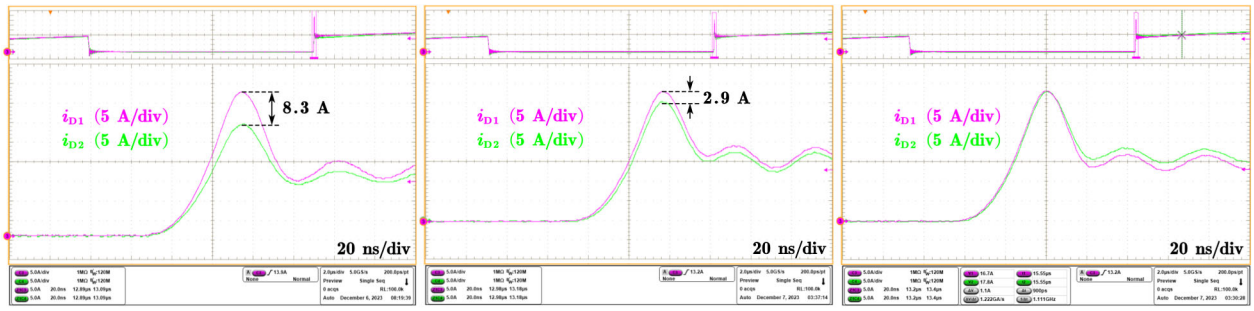


Fig. 3-30 The DMC gate driver under DPT.

position are labeled as M1 and M2 in these tests. The DMC can be soldered on P_G or P_K to verify the analysis of DMC gate driver. Fig. 3-29 shows the toroidal DMCs with two different L_m values, 5 μH and 25 μH. Ideally, the L_σ should be designed as small as possible since it remains present in the gate driving loop and may slow down the switching speed. The bifilar winding technique is adopted to minimize L_σ and equivalent parallel capacitance. In contrast to the balancing method in [84], the DMC winding's current capacity in this dissertation can be reduced due to the low gate current level, potentially help decrease the volume and footprint of the DMC. This dissertation focuses on the concept and feasibility of the proposed method; thus, the optimization of the DMC is beyond the scope and will not be further discussed.

Fig. 3-31 shows the experimental waveforms before and after adopting the DMC gate driver. The



(a) (b) (c)

Fig. 3-31 Experimental waveforms with fixed $R_{G,ext}$ and ΔL_S (a) without balancing method, (b) with DMC gate driver L_m = 5 µH, and (c) with DMC gate driver L_m = 25 µH.

Fig. 3-31(a) serves as the baseline waveforms without the DMC, showing a $\Delta i_{D,pk}$ of 8.3 A. After implementing the DMC with L_m of 5 µH in Fig. 3-31(b), the $\Delta i_{D,pk}$ is greatly suppressed down to 2.9 A. The dynamic current imbalance is 65.1 % smaller than the baseline waveforms using the DMC gate driver. Under the same condition, Fig. 3-31(c) further presents the waveforms when the L_m is increased to 25 µH. The measured current becomes almost balanced with difference less than 1 A. Moreover, being tested under same conditions, all three cases in Fig. 3-31 have similar rising time of the currents, indicating that the solution has negligible impact on the switching speed.

To demonstrate the capability of the DMC gate driver, Fig. 3-32 shows the experimental waveforms under fixed L_m of 5 µH with different $R_{G,ext}$ values. Corresponding baseline waveforms without the DMC can be found in Fig. 2-19. Compared to the baseline waveforms, the currents in Fig. 3-32 are much more balanced. When $R_{G,ext}$ equals to 15 **Ω**, the current difference almost vanishes. Similarly, the rising time of the currents are not affected by the DMC gate driver.

The switching energy is calculated by integrating the voltage and current during the dynamic periods. Table 3-3 summarizes the difference of switching energy ΔE between Fig. 2-19 and Fig. 3-32, and ΔE is defined as:

$$\Delta E = |E_{M1} - E_{M2}| \tag{3.14}$$

It can be seen that the unbalanced switching energy ΔE during both turn-on and turn-off transients are significantly reduced by the DMC gate driver.

Fig. 3-33 illustrates the waveforms of v_{GS} before and after implementing the DMC gate driver. With a 5 µH DMC, there is a slightly higher peak-to-peak voltage and longer oscillation appears

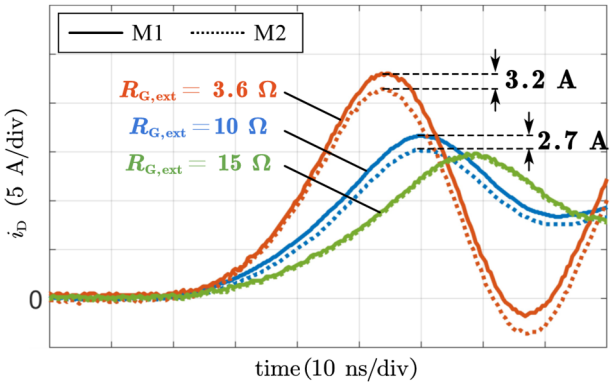


Fig. 3-32 Experimental waveforms of different $R_{G,ext}$ with DMC gate driver L_m = 5 µH. The baseline waveforms are presented in Fig. 3-16.

TABLE 3-3 COMPARISON OF SWITCHING ENERGIES USING DIFFERENT R_G

$R_{G,ext}$	Cases		M1	M2	$\Delta E/E_{avg}$
3.6 Ω	Original	Turn-on	278 µJ	215 µJ	25.6 %
		Turn-off	137 µJ	155 µJ	12.3 %
	With DMC	Turn-on	252 µJ	241 µJ	2.2 %
		Turn-off	145 µJ	146 µJ	0.7 %
10 Ω	Original	Turn-on	349 µJ	275 µJ	23.7 %
		Turn-off	204 µJ	226 µJ	10.2 %
	With DMC	Turn-on	320 µJ	305 µJ	4.8 %
		Turn-off	214 µJ	212 µJ	0.9 %
15 Ω	Original	Turn-on	421 µJ	336 µJ	22.5 %
		Turn-off	259 µJ	282 µJ	8.5 %
	With DMC	Turn-on	386 µJ	371 µJ	4 %
		Turn-off	271 µJ	267 µJ	1.5 %

during both turn-on and turn-off transients. Yet, the v_{GS} also become more balanced. While L_σ aids in suppressing the unbalanced Δi_G, it may slow down the switching speed and can introduce unwanted oscillation since L_σ remains present in the gate driving loop. Ideally, L_σ should be design as small as possible to minimize its impact on switching speed.

As analyzed in the previous session, the DMC should be inserted into the gate position P_G instead of P_K. Fig. 3-34 shows the experimental waveforms when the DMC with L_m = 5 µH is placed at P_K. Compared to the baseline waveform in Fig. 3-31(a), clearly, the current sharing becomes even worse when the DMC is placed at the KS node. The $\Delta i_{D,pk}$ increases from 8.3 A to 10.5 A. The waveforms emphasize the necessity of inserting DMC into right position at P_G.

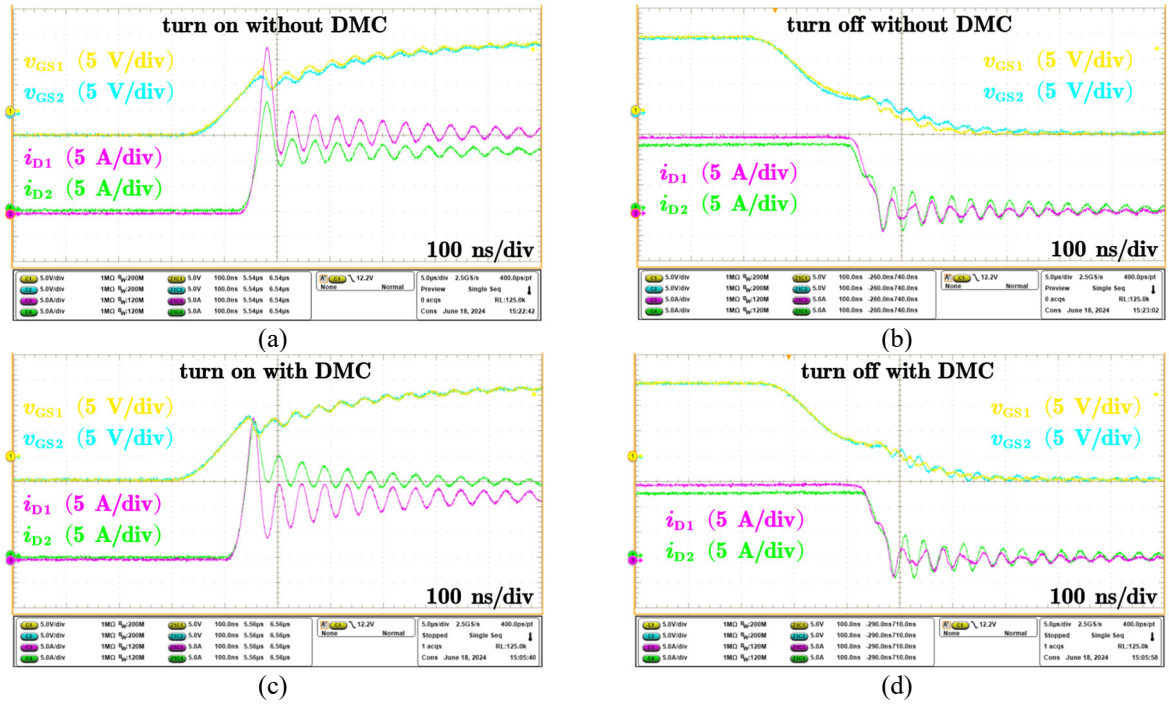


Fig. 3-33 Experimental waveforms of v_{GS}, before adding the DMC (a) turn-on (b) turn-off; after adding DMC (c) turn-on (d) turn-off.

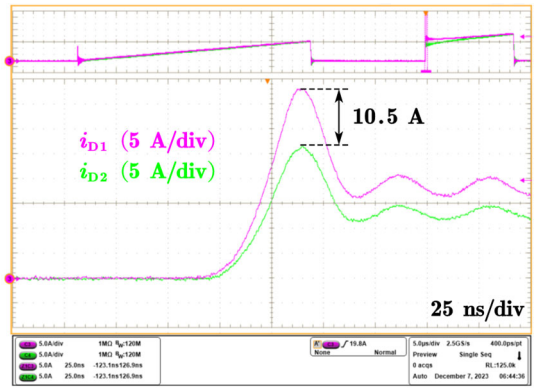


Fig. 3-34 Experimental waveforms after placing DMC with L_m = 5 μH at the location of P_K instead of P_G.

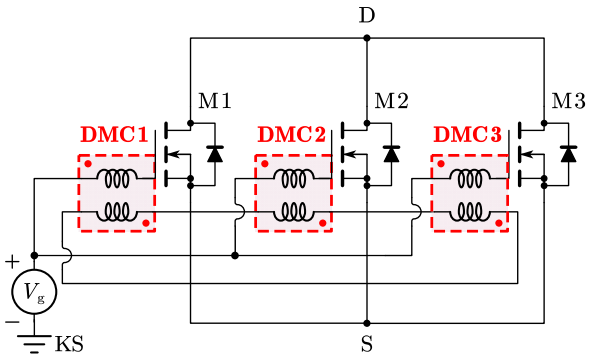
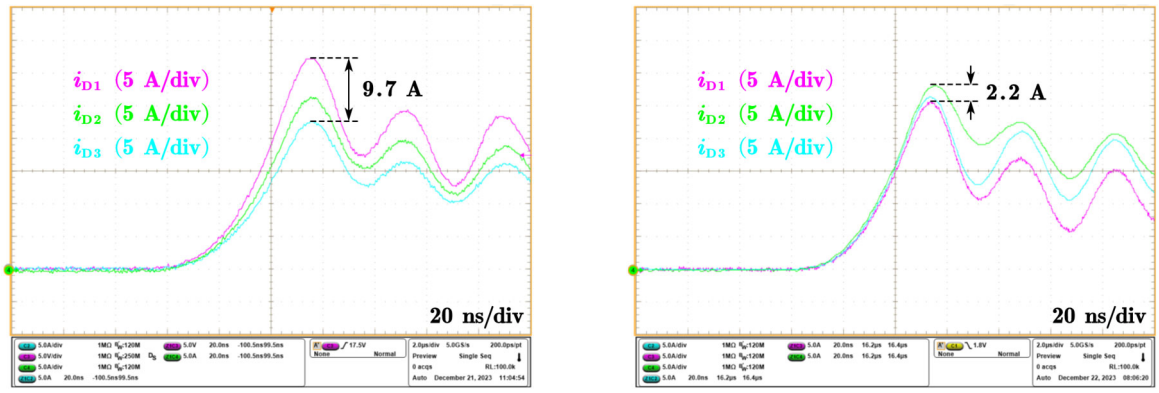


Fig. 3-35 The structure of DMC gate driver for multiple devices.

The DMC gate driver can be extended to applications involving more than two paralleled devices. An additional SiC MOSFET, labeled as M3, is soldered on the power board in Fig. 2-17. Likewise, the layout of M3 is symmetrical and identical to that of other devices. There are two different configurations of DMC for multiple devices [84]. Also, the required number of DMCs equals the total number of paralleled devices. For simplicity, structure as shown in Fig. 3-35 is chosen to demonstrate the effectiveness of the DMC method.



(a) (b)

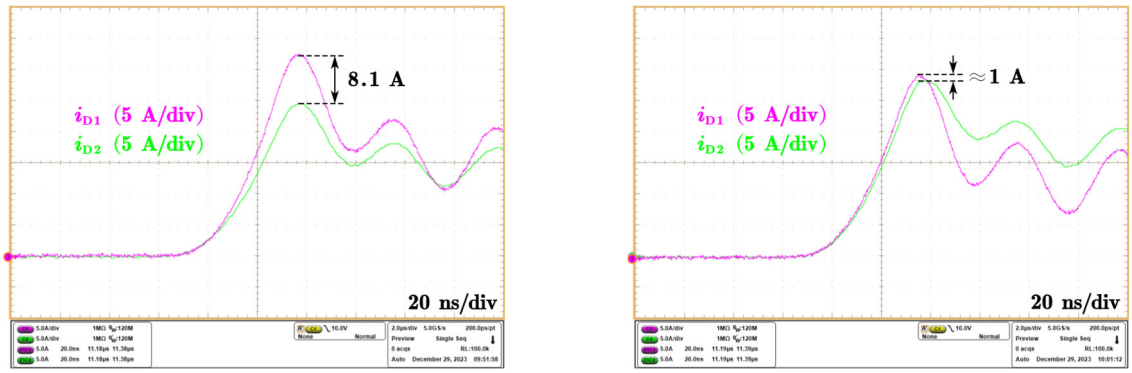
Fig. 3-36 Experimental waveforms when $L_{S3} > L_{S2} > L_{S1}$ (a) without balancing method and (b) with DMC gate driver.

TABLE 3-4 COMPARISON OF SWITCHING ENERGIES FOR MULTIPLE DEVICES IN FIG. 4-34

		M1	M2	M3	$\Delta E_{max}/E_{avg}$
Original	Turn-on	395 µJ	337 µJ	293 µJ	29.8 %
	Turn-off	254 µJ	239 µJ	280 µJ	10.1 %
With DMC	Turn-on	349 µJ	336 µJ	326 µJ	6.8 %
	Turn-off	270 µJ	267 µJ	263 µJ	2.6 %

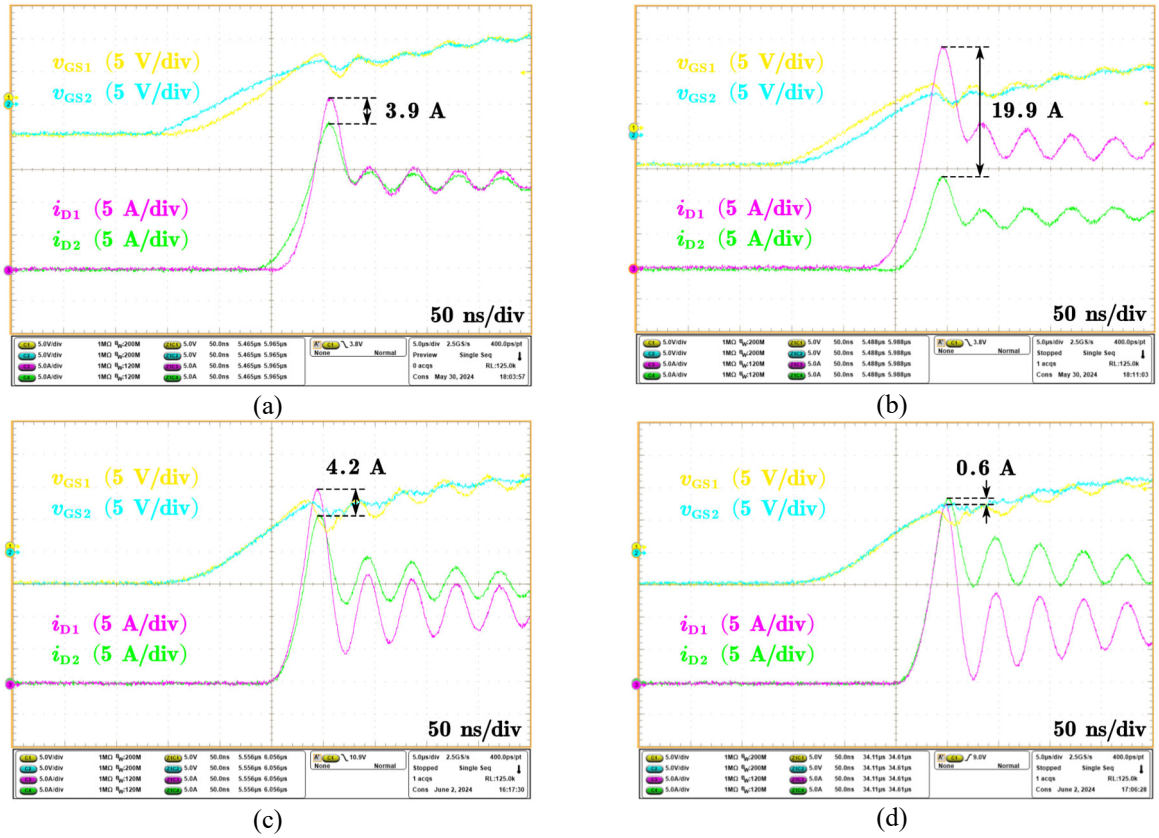
Fig. 3-36(a) shows the baseline waveforms when $L_{S3} > L_{S2} > L_{S1}$. The total i_{load} is increased to 45 A. Clearly, M1 carries the most turn-on current while M3 carries the least. In Fig. 3-36(b), the experimental waveforms after adopting the DMC gate driver are presented. Evidently, the dynamic currents are much more balanced when compared to the baseline waveforms. By using the DMC method, the $\Delta i_{D,pk}$ is reduced by 77.3 %. The switching energies are summarized in Table 3-4. As expected, the ΔE are much balanced after adopting the DMC gate driver. The test results verify the effectiveness of DMC gate driver with multiple paralleled SiC MOSFETs.

In Chapter 2, it is mathematically shown that the mismatched gate driving loops have negligible impact on dynamic current sharing. When L_{S2} is 16.5 nH higher than L_{S1} and $R_{G,ext}$ at 10 Ω, Fig. 3-37(a) shows the experimental waveforms with additional mismatches in gate loop where L_{G2} and L_{K2} are all 4.95 nH larger than L_{G1} and L_{K1}. It is seen that the $\Delta i_{D,pk}$ is similar to that of the baseline waveforms in Fig. 3-37(a). The DMC is later added under the same conditions, and the waveforms are shown in Fig. 3-37(b). Apparently, the DMC gate driver effectively balances the dynamic currents even with mismatched gate driving loops.



(a) (b)

Fig. 3-37 Experimental waveforms with fixed $R_{G,ext}$, ΔL_S, ΔL_G, and ΔL_K (a) without balancing method and (b) with DMC gate driver L_m = 25 µH.



(a) (b)

(c) (d)

Fig. 3-38 Experimental waveforms with fixed $R_{G,ext}$ and ΔL_S (a) driving signal of M1 is delayed (b) driving signal of M2 is delayed. While driving signal of M2 is still delayed (c) with DMC gate driver L_m = 5 µH (d) with DMC gate driver L_m = 25 µH.

In real-world applications, it is possible for paralleled devices having different driving signal delays [129]. This mismatch can be caused by unequal signal traces or differences among additional driving components, such as current boosters [40]. Fig. 3-38 shows the experimental waveforms when ΔL_S is fixed and $R_{G,ext}$ is 10 Ω. In Fig. 3-38(a), the gate driving signal of M1 is

delayed by around 20 ns. Therefore, the v_{GS2} is first charged and the M2 turns on prior to M1. Yet, after the M1 is turned on, the i_{D1} rises faster than i_{D2} due to layout mismatch. The currents are unbalanced during the rising period, and the $\Delta i_{D,pk}$ is around 3.9 A. Conversely, Fig. 3-38(b) shows the waveforms when driving signal of M2 is delayed by 20 ns. Under the combination of both driving and layout mismatches, the i_{D1} is much higher than i_{D2} with $\Delta i_{D,pk}$ of 19.9 A.

In Fig. 3-38(c), the DMC with L_m of 5 μH is added when driving signal of M2 is still delayed by 20 ns. When compared to Fig. 3-38(b), the $\Delta i_{D,pk}$ is greatly decreased from 19.9 A to 4.2 A. When L_m is further increased to 25 μH in Fig. 3-38, the currents are almost balanced with $\Delta i_{D,pk}$ less than 0.6 A. After the DMC is added, it is observed that the pre-turn-on time (before v_{GS} reaches V_{th}) is around 5 ns longer than those cases without DMC because the initial charging current for one device that has no delay is now equally shared by 2 devices. After the MOSFETs start conducting currents, the current rising speed is similar with cases without DMC. DMC gate driver can help balance the currents even when gate driving signals are mismatched. The experimental results validate the feasibility of DMC gate driver for paralleled discrete devices.

3.4. Conclusion

Guided by the current sharing models established in previous Chapter 2, two passive current-balancing solutions are comprehensively analyzed and evaluated. It is found that the layout configuration of T1-C-Int emerges as the optimal choice for paralleled devices, especially in minimizing the parasitic L_{loop} and overlapping C. However, the conventional laminated layout technique poses issue of asymmetric layout for paralleled devices, resulting in serious current sharing issues in both static and dynamic switching regions. To address this, the proposed DB layout concept mitigates the mismatched parasitic, proving the approach of eliminating the source v_{eq} that initiates the unbalanced current sharing mechanism. Furthermore, incorporating the DMC gate driver enhances dynamic current sharing by introducing extra impedance element $L_{DMC,eq}$ into the dynamic equivalent RLC circuit, thereby suppressing the unbalanced Δi_G.

Chapter 4
Active Current-Balancing Solutions with Dynamic Current Sensing

Although the passive current-balancing solutions in Chapter 3 significantly improve the current sharing, their effectiveness depends on the use of power devices with high consistency. In real world, however, this assumption may not always hold. Cost constraints or limited device characterization may necessitate the use of device candidates with lower consistency, where slight current imbalance, particularly in the dynamic region, can still occur even when adopting the proposed DB layout or DMC gate driver, like the case shown in Fig. 3-28.

To achieve current balancing under all conditions, this chapter proposes an AGD solution. The AGD consists of three primary functions, current sensing, signal processing, and gate driving. Among these, accurate current sensing is of great importance as the AGD reacts according to the information provided by the current sensors. Furthermore, to measure individual currents in paralleled devices, the current sensor must be low-cost, simple, and high scalable. Building on these requirements, this chapter first introduces a current sensing method for paralleled devices, followed by the design and implementation of the proposed AGD solution.

4.1. Dynamic Current Sensing for Paralleled Devices

Beyond the current sensing methods introduced in Section 1.2.2, which are largely impractical for paralleled devices, the *di/dt*-RC sensing method stands out as a cost-effective and simple solution with strong potential for paralleled devices applications. In [130, 131], the this method was adopted as overcurrent detection for single IGBT and SiC MOSFET. Research [132] extended this technique for load current sensing, providing comprehensive design guidelines. An improved sensing structure was proposed in [133], aiming to resolve triggering issue caused by different overcurrent scenarios [134]. The [135] implemented the *di/dt*-RC sensing to sense both dynamic

and static currents for single SiC MOSFET, along with compensation technique for parasitic resistance.

Although these studies present high-quality analyses, a thorough evaluation of *di/dt*-RC sensing for paralleled SiC MOSFETs remains lacking. In particular, while [88] introduced this technique for paralleled devices, the critical impact of circulating currents among devices has not been addressed. This gap motivates the present section, which investigates the applicability, limitations, and enhancements of *di/dt*-RC sensing for dynamic current sensing in paralleled SiC MOSFETs.

4.1.1 Operating Principles of *di/dt*-RC Sensing

Since the *di/dt*-RC sensing technique for single device has been extensively analyzed in [130-132], this article only provides necessary background. Fig. 4-1 shows when implementing *di/dt*-RC sensing for single device. A pair of RC filter R_f and C_f are directly connected to device's source and KS pins. It can be assumed that the drain current i_D equals to the source current i_S, and gate current i_G equals KS current i_K. During switching transients, the sensed voltage v_{sense} across C_f can be derived as:

$$v_{\text{sense}}(s) = \frac{i_{\text{S}}(s) \cdot sL_{\text{S,int}} - i_{\text{K}}(s) \cdot sL_{\text{K,int}}}{sR_{\text{f}}C_{\text{f}} + 1} \tag{4.1}$$

where L_{int} is internal parasitic inductance of device's package. Typically, the power current is much greater than driving current. Therefore, it is assumed that $i_S >> i_K$, then (4.1) can be rewritten with the focus on high-frequency range ($s \to \infty$):

$$\frac{v_{\text{sense}}(s)}{i_{\text{S}}(s)} = \frac{sL_{\text{S,int}}}{sR_{\text{f}}C_{\text{f}} + 1} \approx \frac{L_{\text{S,int}}}{R_{\text{f}}C_{\text{f}}} \tag{4.2}$$

where $s = j2\pi f$ is the Laplace operator, and f is the specific frequency. Based on (4.2), the transfer function from i_S to v_{sense} behaves like a high-pass filter with a cutoff frequency $f_c = 1/R_fC_f$. The value selection of R_f and C_f has been previously studied in [132]. To restore the switching current i_S, it is critical to determine $L_{S,int}$, which can be estimated by measuring the i_S and the voltage v_{SK} in double pulse test [130]. Fig. 4-2 shows the experimental result of *di/dt*-RC sensing for single device. Apparently, the v_{sense} effectively captures the high-frequency dynamic current i_S during the

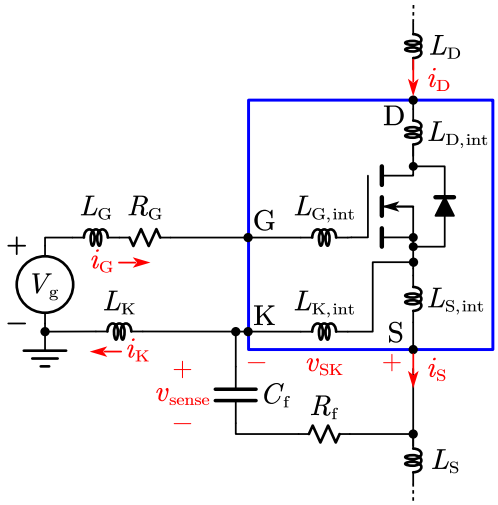


Fig. 4-1 The *di/dt*-RC sensing structure for single device.

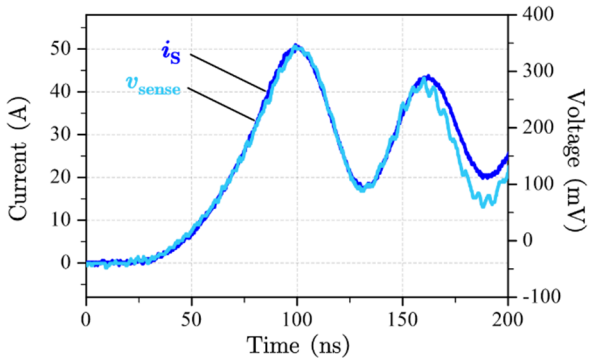


Fig. 4-2 Experimental example of *di/dt*-RC sensing for single device.

switching transient. After the second resonating current peak, the v_{sense} begins to decay due to the reduced gain at the lower frequency range below f_c.

4.1.2 Issue of Conventional Sensing Structure

For dynamic current monitoring or active current balancing solutions, it is crucial for Δv_{sense} between paralleled devices to provide correct information as it indicates which device is conducting higher/lower dynamic current. However, when using the conventional sensing structure which is shown in Fig. 4-3, the circulating current i_{cir} induced by asymmetric layout or mismatched devices results in sensing error.

In Fig. 4-3, the R_f and C_f are directly connected to the paralleled devices, M1 and M2. During switching transients, the power current i_S can induce a voltage drop v_S across the source parasitic L_S. Due to mismatches in either layout or paralleled devices, a difference between v_{S1} and v_{S2} arises, leads to a i_{cir} [128]. The i_{cir} can be pronounced depends on the degree of asymmetric layout or mismatched devices. According to Fig. 4-3, the v_{sense1} and v_{sense2} can be derived as:

$$\begin{cases} v_{sense1}(s) = \dfrac{sL_{S,int}i_{S1}(s) - sL_{K,int}i_{K1}(s)}{sR_fC_f + 1} \\ v_{sense2}(s) = \dfrac{sL_{S,int}i_{S2}(s) - sL_{K,int}i_{K2}(s)}{sR_fC_f + 1} \end{cases} \tag{4.3}$$

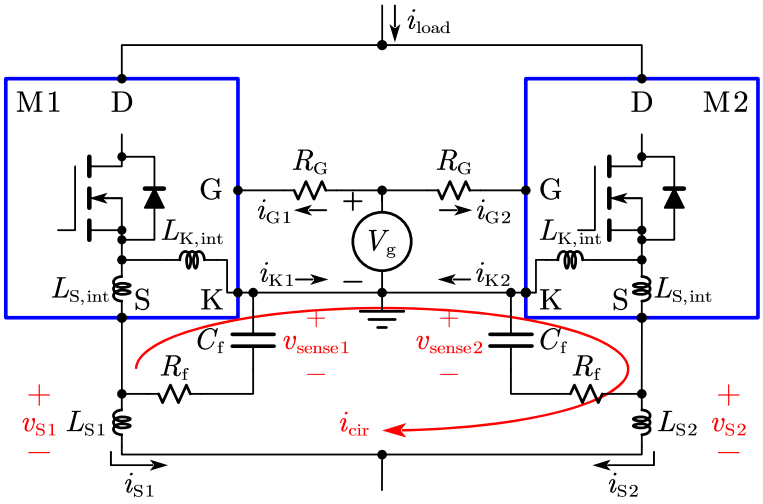


Fig. 4-3 Conventional sensing structure for paralleled devices with i_{cir} induced by unbalanced currents, regardless causes of asymmetric layout or mismatched devices.

where i_{K1} and i_{K2} are the KS currents of paralleled devices. It is assumed that both have the same base current i_K, with i_{cir} added to better illustrate the impact:

$$\begin{cases} i_{K1} = i_K + i_{cir} \\ i_{K2} = i_K - i_{cir} \end{cases} \tag{4.4}$$

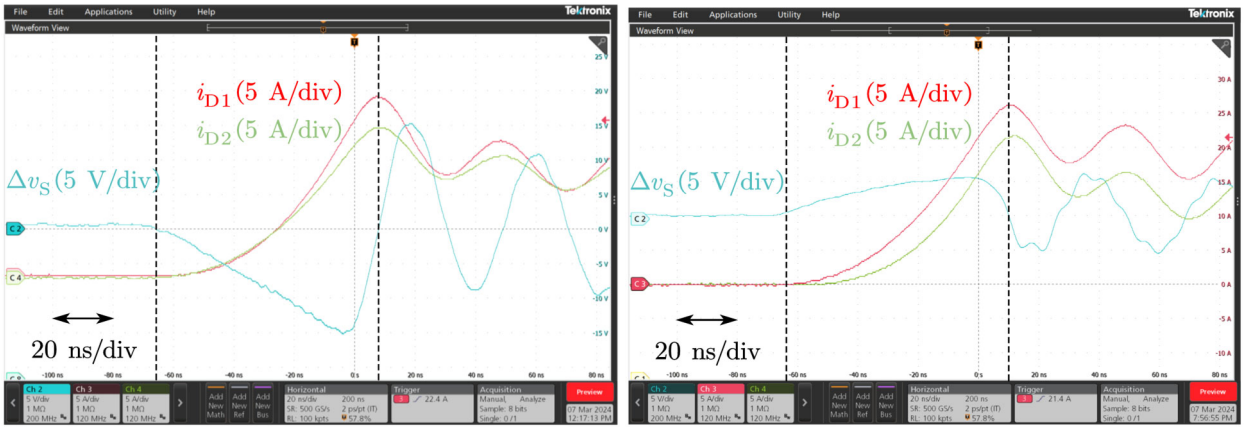
By combining (4.3) and (4.4) with focus in high-frequency range, and applying mathematical expression in (2.1), the Δv_{sense} can be derived as:

$$\Delta v_{sense} = \frac{L_{S,int}}{R_f C_f} \Delta i_S - \frac{2L_{K,int}}{R_f C_f} i_{cir} \tag{4.5}$$

It is found that i_{cir} affects the sensing accuracy. In (4.5), the Δv_{sense} is seen to consist of two components. The first component represents the ideal term, where Δv_{sense} reflects the unbalanced currents of $\Delta i_S = i_{S1} - i_{S2}$. However, the second component is the unwanted sensing error generated by i_{cir}. Additionally, it is observed that the direction of i_{cir} varies under different conditions.

In Section 2.1, it has been concluded that dynamic current sharing is mainly affected by mismatches in L_S or threshold voltage V_{th}. It is crucial to highlight the behavioral difference between two cases:

- Case 1: Asymmetric layout with identical devices: ($L_{S1} < L_{S2}$ and $V_{th1} = V_{th2}$).
- Case 2: Perfect layout but devices have mismatched V_{th} ($L_{S1} = L_{S2}$ and $V_{th1} < V_{th2}$).



(a) (b)

Fig. 4-4 Behavioral difference between (a) case 1 asymmetric layout with identical devices and (b) case 2 a perfect layout with mismatched devices.

Take the Δv_S in Fig. 4-3, which is the difference between the source voltage potentials Δv_S (voltage across source inductance), as an example, this polarity is employed to trigger the current balancing AGD proposed in [89]. However, while their method has proven to be effective for the second scenario, it may be invalid for the first scenario due to the behavioral difference, potentially resulting in even worse current balancing. Fig. 4-4 shows the experimental waveforms of both cases. In Fig. 4-4(a), the L_{S2} is 16 nH larger than L_{S1} with identical devices. The devices are prescreened by using curve tracer to pick those with identical V_{th}. On the other hand, the layout in Fig. 4-4(b) is matched but the selected devices exhibit V_{th} mismatch (V_{th1} is 0.7 V lower than V_{th2}). In both cases, the dynamic current i_{D1} is higher than i_{D2}. However, the potential of Δv_S is entirely in opposite direction. Therefore, if Δv_S is involved in the current sensing or triggering indication for current balancing technique, the polarity of Δv_S should be taken into consideration.

According to behavioral difference shown in Fig. 4-4, apparently, the directions of i_{cir}, which depends on polarity of Δv_S, in two cases are also reversed. For the case of asymmetric layout, the i_{cir} becomes negative. Conversely, when the paralleled devices exhibit mismatch in V_{th}, the i_{cir} becomes positive.

The influence of i_{cir} on measured v_{sense} is demonstrated in Fig. 4-5 obtained from circuit-level simulations in LTspice. In Fig. 4-5(a), when the unbalanced currents are caused by asymmetric layout, the negative i_{cir} exacerbates Δv_{sense} based on (4.5), amplifying Δv_{sense} beyond the actual unbalanced currents (assuming power current $\Delta i_D \approx \Delta i_S$). On the other hand, in Fig. 4-5(b), the positive i_{cir} generated by mismatched devices reduces Δv_{sense} than actual currents. If i_{cir} is large

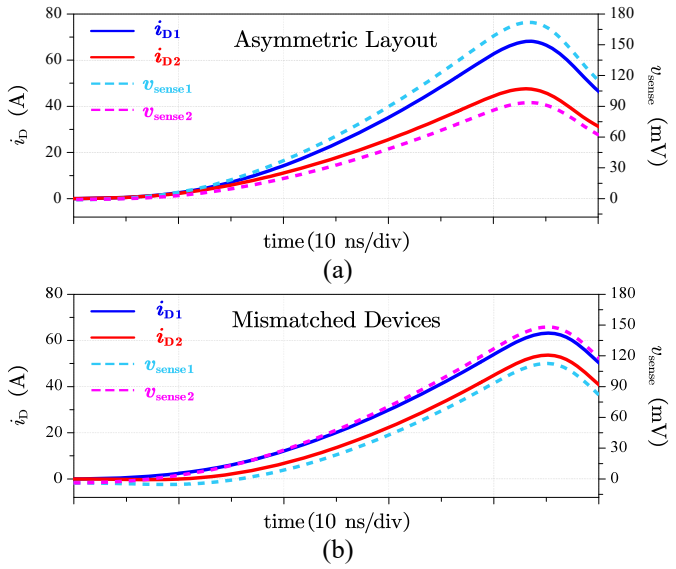


Fig. 4-5 Influence of i_{cir} on *di/dt*-RC sensing in conventional sensing structure when the unbalanced currents are caused by (a) asymmetric layout (b) mismatched devices.

enough, the Δv_{sense} may even become negative ($v_{sense1} < v_{sense2}$), despite the current i_{D1} being larger than i_{D2}. This can cause the signal processing circuit to receive erroneous information about the actual dynamic currents.

4.1.3 Proposed R_K Sensing Structure for Paralleled Devices

To address the undesirable impact of i_{cir} on *di/dt*-RC sensing, a novel sensing structure is proposed. Fig. 4-6 shows the proposed R_K sensing structure with necessary components, where additional KS resistors R_K are added on KS paths to suppress i_{cir}. The original single gate resistor R_G in Fig. 4-3 is divided into a smaller R_G with additional R_K so the total equivalent gate loop resistance remains unchanged. The proposed R_K sensing structure requires only three passive components (R_f, C_f, and R_K) for each MOSFET which is advantageous for industrial applications. To determine the value of R_K and its effect on i_{cir}, it is necessary to develop a mathematical model for i_{cir}.

According to the defined dynamic region and assumptions made in Section 2.2.1 for dynamic current analysis, Fig. 4-7 shows the dynamic circuit of Fig. 4-6. Since the RC sensing branches barely have current, they can be excluded to simplify the derivation. Given that the paralleled devices operate in the saturation region, by applying KVL to gate driving and bottom source-KS loops:

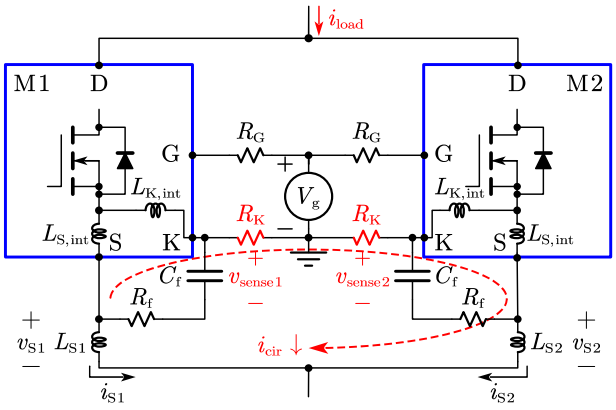


Fig. 4-6 Proposed R_K sensing structure to improve sensing accuracy.

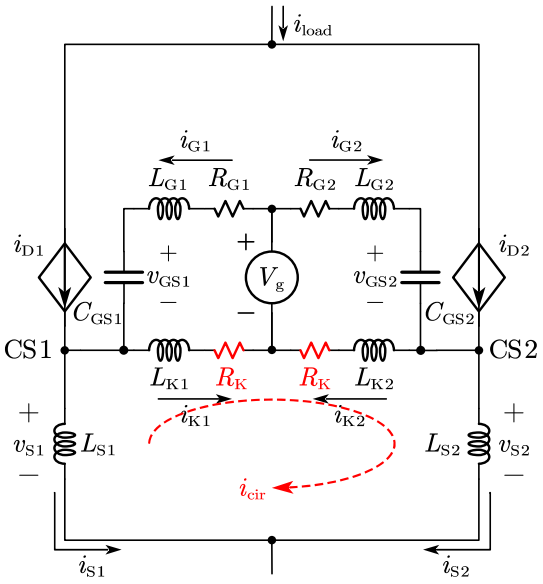


Fig. 4-7 Dynamic circuit based on Fig. 4-6.

$$\begin{cases} V_g = R_G i_{G1} + L_{G1}\dfrac{di_{G1}}{dt} + v_{GS1} + L_{K1}\dfrac{di_{K1}}{dt} + R_K i_{K1} \\ V_g = R_G i_{G2} + L_{G2}\dfrac{di_{G2}}{dt} + v_{GS2} + L_{K2}\dfrac{di_{K2}}{dt} + R_K i_{K2} \end{cases} \tag{4.6}$$

$$L_{S1}\frac{di_{S1}}{dt} - R_K i_{K1} - L_{K1}\frac{di_{K1}}{dt} = L_{S2}\frac{di_{S2}}{dt} - R_K i_{K2} - L_{K2}\frac{di_{K2}}{dt} \tag{4.7}$$

And assuming that during switching transient, the i_G charges C_{GS} and returns to V_g via KS path, the KCL relationships:

$$\begin{cases} \Sigma i_D = \Sigma i_S = i_{load} \\ \Sigma i_G = \Sigma i_K \\ i_{D1} = i_{S1} + i_{cir} \\ i_{D2} = i_{S2} - i_{cir} \\ i_{K1} = i_{G1} + i_{cir} \\ i_{K2} = i_{G2} - i_{cir} \end{cases} \tag{4.8}$$

1) Modeling for Asymmetric Layout

In this case, the paralleled devices are assumed to be identical. Since the dynamic current sharing is only sensitive to ΔL_S, the impacts from ΔL_G and ΔL_K are neglected [76, 127]. Also, it is assumed that $di_{cir}/dt >> di_G/dt$ because the di_G/dt is less pronounced once the MOSFETs begin conducting

current. Therefore, the following assumptions are made:

$$\begin{cases} V_{\mathrm{th}1} = V_{\mathrm{th}2} = V_{\mathrm{th}} \\ g_{\mathrm{m}1} = g_{\mathrm{m}2} = g_{\mathrm{m}} \\ C_{\mathrm{GS}1} = C_{\mathrm{GS}2} = C_{\mathrm{GS}} \\ L_{\mathrm{G}1} = L_{\mathrm{G}2} = L_{\mathrm{G}} \\ L_{\mathrm{K}1} = L_{\mathrm{K}2} = L_{\mathrm{K}} \\ \dfrac{di_{\mathrm{cir}}}{dt} \gg \dfrac{di_{\mathrm{G}}}{dt} \end{cases} \tag{4.9}$$

By combining (2.1) to (2.3), (2.5), (4.6) to (4.9), a time-domain mathematical model for i_{cir} can be derived without performing Laplace transform:

$$v_{\mathrm{eq}} = R_{\mathrm{eq}} i_{\mathrm{cir}} + L_{\mathrm{eq}} \frac{di_{\mathrm{cir}}}{dt} + \frac{1}{C_{\mathrm{eq}}} \int i_{\mathrm{cir}} dt \tag{4.10}$$

$$\begin{cases} v_{\mathrm{eq}}(\mathrm{V}) = \dfrac{\Delta L_{\mathrm{S}}}{2} \dfrac{di_{\mathrm{load}}}{dt} + \dfrac{\Delta L_{\mathrm{S}}}{2C_{\mathrm{GS}}(R_{\mathrm{G}} + R_{\mathrm{K}})} i_{\mathrm{load}} \\ R_{\mathrm{eq}}(\Omega) = \dfrac{2R_{\mathrm{K}}}{R_{\mathrm{G}} + R_{\mathrm{K}}} \left(\dfrac{g_{\mathrm{m}} \Sigma L_{\mathrm{S}}}{2C_{\mathrm{GS}}} - R_{\mathrm{K}} \right) + 2R_{\mathrm{K}} + \dfrac{\Sigma L_{\mathrm{S}} + 2L_{\mathrm{K}}}{C_{\mathrm{GS}}(R_{\mathrm{G}} + R_{\mathrm{K}})} \\ L_{\mathrm{eq}}(\mathrm{H}) = \dfrac{2L_{\mathrm{K}}}{R_{\mathrm{G}} + R_{\mathrm{K}}} \left(\dfrac{g_{\mathrm{m}} \Sigma L_{\mathrm{S}}}{2C_{\mathrm{GS}}} - R_{\mathrm{K}} \right) + \Sigma L_{\mathrm{S}} + 2L_{\mathrm{K}} \\ C_{\mathrm{eq}}(\mathrm{F}) = \dfrac{C_{\mathrm{GS}}(R_{\mathrm{G}} + R_{\mathrm{K}})}{2R_{\mathrm{K}}} \end{cases} \tag{4.11}$$

Based on the derived (4.10) and (4.11), the mechanism of i_{cir} induced by asymmetric layout ΔL_{S} can be modeled as an equivalent RLC circuit just like the one shown in Fig. 2-8. The equivalent voltage source v_{eq} generates i_{cir}, and the magnitude of i_{cir} is determined by the combination of R_{eq}, L_{eq}, and C_{eq}. The values of R_{eq}, L_{eq}, and C_{eq} are influenced by parasitic components and device parameters.

In the case of asymmetric layout, the v_{eq}, R_{eq}, L_{eq}, and C_{eq} are determined by (4.11) which suggests that, when $L_{\mathrm{S}1} < L_{\mathrm{S}2}$ and $i_{\mathrm{D}1} > i_{\mathrm{D}2}$, the i_{cir} is negative and flows from M2 to M1. Consequently, the $\Delta v_{\mathrm{S}} < 0$ which explains the experimental waveform shown in Fig. 4-4(a). To verify the derived model in (4.11) and effect of R_{K}, Fig. 4-8 compares the simulated i_{cir} based on circuit in Fig. 4-7, with the modeled i_{cir} extracted from RLC equivalent model. In Fig. 4-8(a), the R_{K} is first set as 0 **Ω**, showing the waveforms with different ΔL_{S}. It is evident that both Δi_{D} and i_{cir} increase as ΔL_{S}

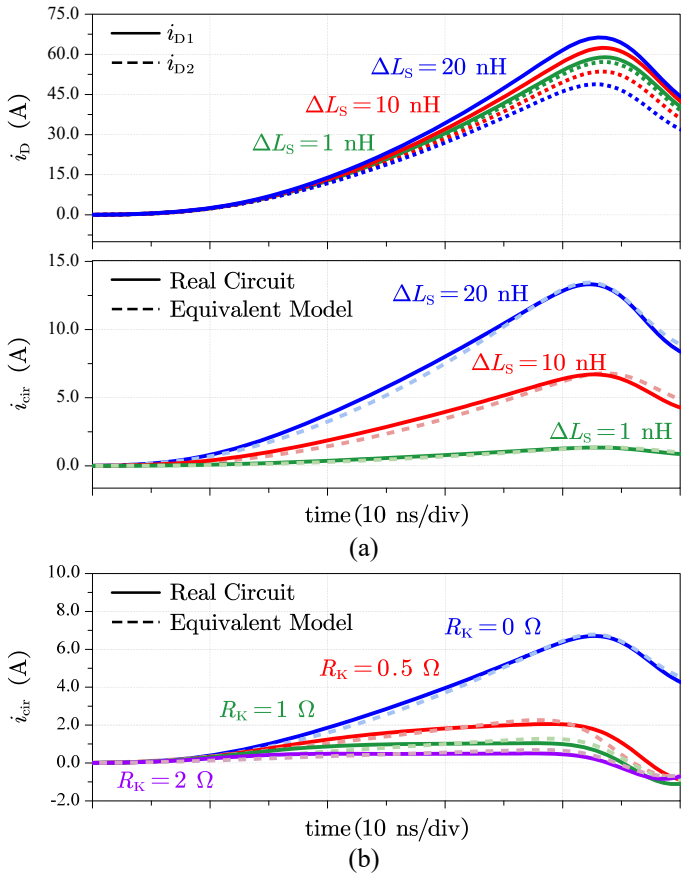


Fig. 4-8 Comparison of simulated and modeled i_{cir} under asymmetric layout condition (a) i_{cir} to different ΔL_S when R_K = 0 Ω (b) i_{cir} to different R_K when ΔL_S is fixed at 10 nH.

increases. Focusing on i_{cir}, the modeled i_{cir} from the equivalent model closely matches the simulated i_{cir} from circuit-level simulation, verifying the accuracy of the derived time-domain model. The effect of R_K on suppressing i_{cir} is demonstrated in Fig. 4-8(b). The i_{cir} is greatly reduced after adding R_K, while maintaining the total gate driving resistance $R_G + R_K$ as constant. More importantly, the modeled i_{cir} aligns well with the actual i_{cir}, further confirming the high accuracy of the derived time-domain model.

The suppressing rate γ_{layout} is defined in (4.12) as the ratio of peak $i_{cir,pk}$ with R_K to that without R_K under the same circuit condition:

$$\gamma_{layout}(\%) = \frac{|i_{cir,pk,with\ RK}|}{|i_{cir,pk,no\ RK}|} \times 100 \tag{4.12}$$

Fig. 4-9 further shows the γ_{layout} to R_K. The effect of R_K is most significant when R_K is smaller than

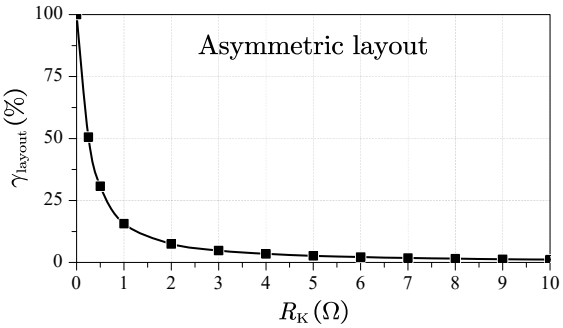


Fig. 4-9 Relationship between γ_{layout} and R_K in asymmetric layout case

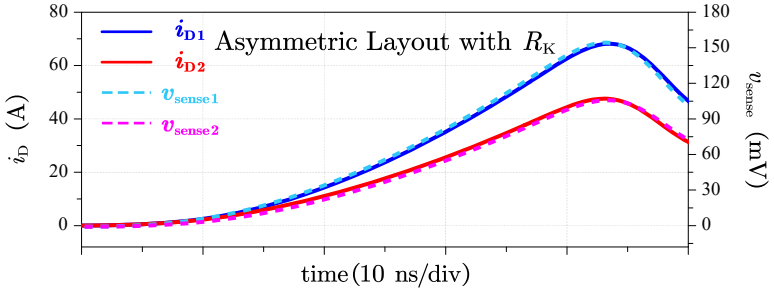


Fig. 4-10 Effect of proposed R_K sensing structure on *di/dt*-RC sensing under asymmetric layout condition.

3 Ω, implying that further increasing R_K beyond than 3 Ω offers limited benefits and may deteriorate crosstalk issue.

Fig. 4-10 shows the effectiveness of the proposed R_K sensing structure with R_K = 1.5 Ω. When compared to Fig. 4-5(a) in conventional structure, while maintaining the same gate driving resistance, the accuracy of the sensed v_{sense} in Fig. 4-10q is significantly improved and closely matches the actual currents.

2) Modeling for Mismatched Devices

The model of i_{cir} is derived when devices exhibit V_{th} mismatch. In this case, it is assumed that the layouts are symmetric. The assumptions are made under the conditions of:

$$\begin{cases} L_{S1} = L_{S2} = L_S \\ L_{G1} = L_{G2} = L_G \\ L_{K1} = L_{K2} = L_K \\ g_{m1} = g_{m2} = g_m \\ C_{GS1} = C_{GS2} = C_{GS} \\ \dfrac{di_{cir}}{dt} \gg \dfrac{di_G}{dt} \end{cases} \tag{4.13}$$

The derivation of mismatched devices can be separated into two parts, depending on the turn-on sequence of the paralleled devices. If the V_{th1} of M1 is lower than V_{th2} of M2, the first part covers the time interval when M1 reaches V_{th1} and begins conducting current prior than M2. The second part corresponds to the time interval when both M1 and M2 are turned on. Fig. 4-11 shows the dynamic circuit during the first interval.

Both i_{G1} and i_{G2} are charging the C_{GS}, while only M1 conducts current i_{D1}. In this case, the current relationships are:

$$\begin{cases} i_{\text{D1}} = i_{\text{load}} = g_{\text{m}}\left(v_{\text{GS1}} - V_{\text{th1}}\right) \\ i_{\text{D2}} = 0 \\ i_{\text{K1}} = i_{\text{G1}} + i_{\text{cir}} \\ i_{\text{K2}} = i_{\text{G2}} - i_{\text{cir}} \\ i_{\text{S1}} = i_{\text{D1}} - i_{\text{cir}} \\ i_{\text{S2}} = i_{\text{cir}} \end{cases} \tag{4.14}$$

By substituting (4.13) and (4.14) into (4.6) and (4.7), and following a similar derivation process as in previous part, the equivalent circuit model for the first interval can be derived as:

$$\begin{cases} v_{\text{eq}}(\text{V}) = L_{\text{S}}\dfrac{di_{\text{load}}}{dt} + \dfrac{L_{\text{S}}}{C_{\text{GS}}\left(R_{\text{G}} + R_{\text{K}}\right)} i_{\text{load}} + \dfrac{R_{\text{K}}}{R_{\text{G}} + R_{\text{K}}}\Delta V_{\text{th}} \\ R_{\text{eq}}(\Omega) = 2\left[\dfrac{L_{\text{S}} + L_{\text{K}} + C_{\text{GS}} R_{\text{G}} R_{\text{K}}}{C_{\text{GS}}\left(R_{\text{G}} + R_{\text{K}}\right)}\right] \\ L_{\text{eq}}(\text{H}) = 2\left(L_{\text{S}} + \dfrac{R_{\text{G}} L_{\text{K}}}{R_{\text{G}} + R_{\text{K}}}\right) \\ C_{\text{eq}}(\text{F}) = \dfrac{C_{\text{GS}}\left(R_{\text{G}} + R_{\text{K}}\right)}{2R_{\text{K}}} \end{cases} \tag{4.15}$$

The (4.15) has a similar form to (4.11) and can be described by (4.10). The (4.15) only reflects the circuit condition in Fig. 4-11 when M2 hasn't been turned on.

For the second interval, when both M1 and M2 are conducting currents, the dynamic circuit is the same as Fig. 4-7 with current relationship in (4.8). By substituting (4.8) and (4.6) into (4.7), the equivalent circuit model for the second interval can be expressed as:

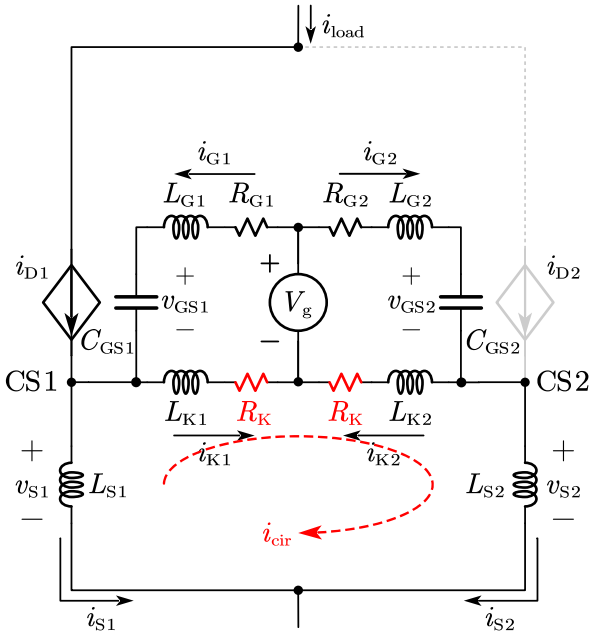


Fig. 4-11 Dynamic circuit when V_{th1}<V_{th2} and M1 is first conducting.

$$\begin{cases} v_{eq}(\mathrm{V}) = -\Delta V_{th} \\ R_{eq}(\Omega) = 2R_K + \dfrac{2R_K(R_G+R_K)}{\alpha} + \dfrac{2(L_S+L_K)}{\alpha C_{GS}} \\ L_{eq}(\mathrm{H}) = \dfrac{2(R_G+R_K)(L_S+L_K)}{\alpha} + 2L_K \\ C_{eq}(\mathrm{F}) = \dfrac{\alpha C_{GS}}{2R_K} \\ \alpha(\Omega) = \dfrac{L_S g_m}{C_{GS}} - R_K \end{cases} \tag{4.16}$$

where α is a positive constant (considering L_S is tens of nH, g_m is tens of S, C_{GS} is thousands of pF [112, 136]). For case of mismatched devices, the parameters in RLC circuit can be calculated by (4.15) and (4.16), depending on the turn-on sequence of paralleled devices. In the first interval, according to (4.15), the v_{eq} is primarily influenced by the positive load current i_{load}. Once the M2 turns on, as shown in (4.16), the v_{eq} becomes independent of i_{load}. Both intervals result in a positive i_{cir}. Therefore, when $V_{th1} < V_{th2}$, the i_{cir} flows from M1 to M2, aligning with the result of $\Delta v_S > 0$ in Fig. 4-4(b).

To verify the derived model, Fig. 4-12 shows the simulated i_{cir} from circuit-level simulation in Fig. 4-7, with the modeled i_{cir} based on (4.15) and (4.16). In Fig. 4-12(a), when R_K = 0 Ω, the i_{cir}

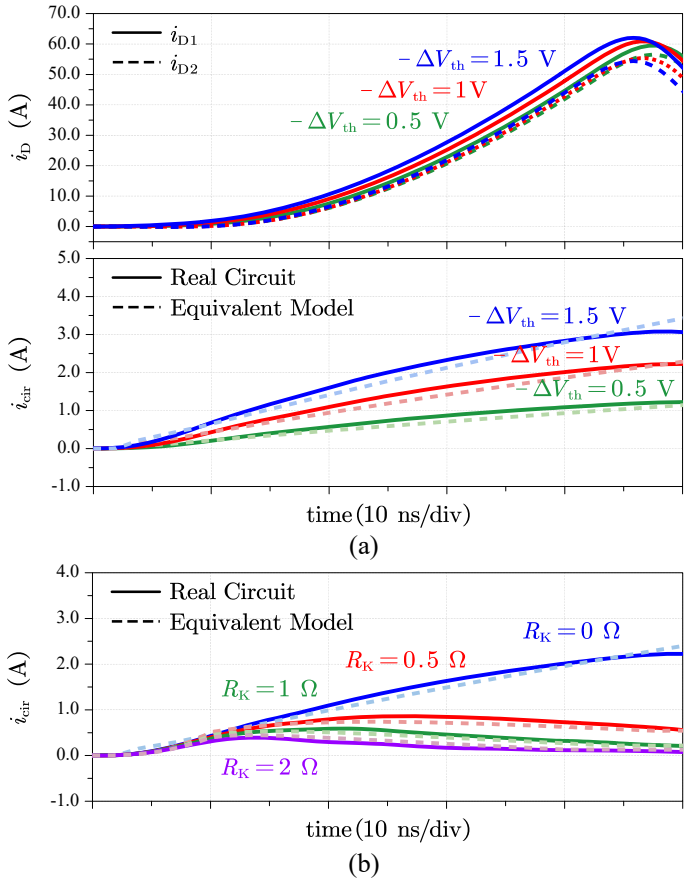


Fig. 4-12 Comparison of simulated and modeled i_{cir} under mismatched devices condition (a) i_{cir} to different ΔV_{th} when $R_K = 0\ \Omega$ (b) i_{cir} to different R_K when ΔV_{th} is fixed.

is positively related to ΔV_{th}, and the modeled i_{cir} well aligns with simulated i_{cir} during dynamic transient. Furthermore, Fig. 4-12(b) illustrates the effect of R_K under mismatched devices condition. As the R_K increases, the i_{cir} generated by mismatched devices is suppressed. The modeled i_{cir} also closely matches the simulated i_{cir}, verifying the accuracy of the derived model.

The γ_{device} has a similar definition with γ_{layout}:

$$\gamma_{device}(\%) = \frac{|i_{cir,pk,with\ RK}|}{|i_{cir,pk,no\ RK}|} \times 100 \tag{4.17}$$

For the mismatched devices, Fig. 4-13 shows the suppressing rate γ_{device} to R_K. The effect of R_K is significant when R_K is less than 2 Ω, and gradually diminishes as R_K increases higher than 2 Ω. The effectiveness of the proposed R_K sensing structure in the case of mismatched devices is depicted in Fig. 4-14 with R_K = 1.5 Ω. When compared to Fig. 4-5(b) without R_K, the sensing

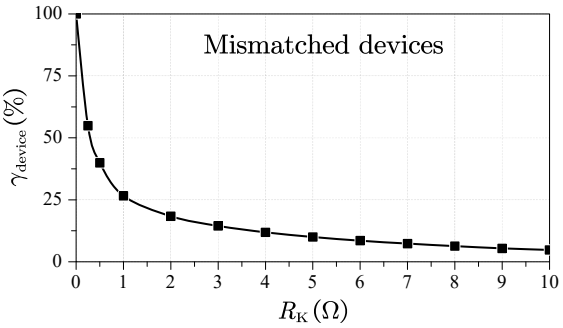


Fig. 4-13 Relationship between γ_{device} and R_K in mismatched devices case.

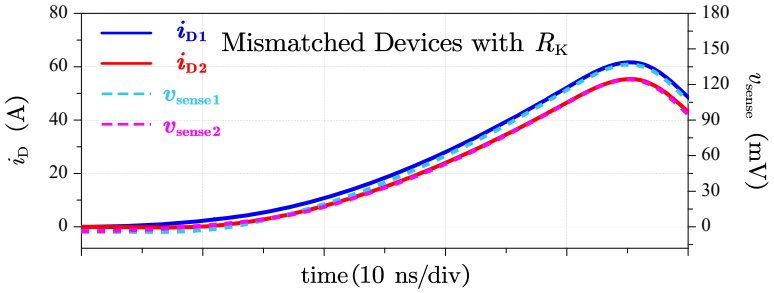


Fig. 4-14 Effect of proposed R_K sensing structure on *di/dt*-RC sensing under mismatched devices condition.

accuracy in Fig. 4-14 is greatly improved. Whether for cases of asymmetric layout or mismatched devices, the proposed R_K sensing structure enhances the accuracy of *di/dt*-RC sensing.

4.1.4 Parasitic Impact on *di/dt*-RC Sensing

In this section, the impact of parasitic as well as design considerations for *di/dt*-RC sensing are presented. In real world applications, parasitic inductance L_f exists in the sensing branch and is in series with R_f and C_f. Additionally, the L_{f1} and L_{f2} can be unequal due to poor layout, and the effect of ΔL_f is uncovered in this article. Two scenarios can happen when designing the circuit. In the first scenario shown in Fig. 4-15(a), both v_{sense1} and v_{sense2} are measured directly across the C_f. In contrast, Fig. 4-15(b) depicts the second scenario where v_{sense1} and v_{sense2} are measured across not only C_f but also L_f. Both scenarios are analyzed with consideration of unbalanced L_f. It is assumed that both power loop layouts and devices are identical, meaning the power currents are balanced $i_{S1} = i_{S2} = i_S$.

In the first scenario as shown in Fig. 4-15(a), the $v_{sense1}(s)$ and $v_{sense2}(s)$ in two branches can be expressed as:

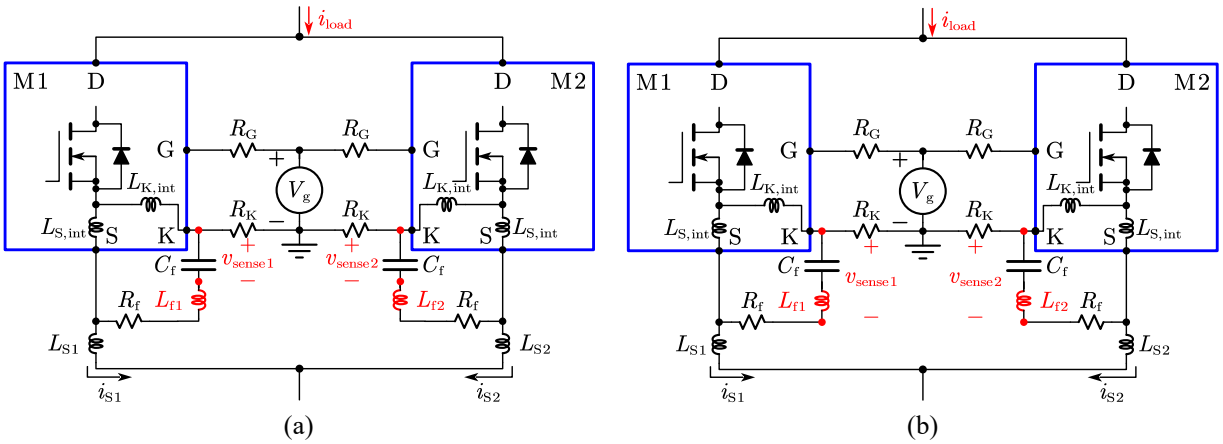


Fig. 4-15 Considering impact of ΔL_f (a) first scenario (b) second scenario.

$$\begin{cases} \dfrac{v_{sense1}(s)}{i_S(s)} \approx \dfrac{sL_{S,int}}{s^2 L_{f1} C_f + sR_f C_f + 1} \\ \dfrac{v_{sense2}(s)}{i_S(s)} \approx \dfrac{sL_{S,int}}{s^2 L_{f2} C_f + sR_f C_f + 1} \end{cases} \tag{4.18}$$

where the difference between $v_{sense1}(s)$ and $v_{sense2}(s)$ can be derived as:

$$\begin{aligned} \frac{\Delta v_{sense}(s)}{i_S(s)} &= \frac{v_{sense1}(s) - v_{sense2}(s)}{i_S(s)} \\ &= -\frac{s^3 C_f L_{S,int} \cdot \Delta L_f}{(s^2 L_{f1} C_f + sR_f C_f + 1)(s^2 L_{f2} C_f + sR_f C_f + 1)} \end{aligned} \tag{4.19}$$

Given the earlier assumption of balanced power currents, the $\Delta v_{sense}(s)$ in (4.19) should ideally be zero or close to zero. The presence of mismatched ΔL_f generates $\Delta v_{sense}(s)$, potentially resulting in sensing error.

Fig. 4-16 shows the magnitude-frequency plot of (4.18) and (4.19) where L_{f1} and L_{f2} are 20 nH and 10 nH, respectively. In the first scenario, when v_{sense} is measured directly across C_f, the magnitude of $\Delta v_{sense}(s)$ from 1 to 100 MHz is negligible. Typically, the current rising/falling period is a relatively slow RC charging/discharging state which usually lasts only tens of nanoseconds. This indicates that, in the first scenario, the ΔL_f has trivial impact within the frequency range of interest. Fig. 4-17 shows the simulation results based on circuit in Fig. 4-15(a) under balanced $i_{D1} = i_{D2}$ with $R_f = 1$ kΩ, $C_f = 1$ nF, and $\Delta L_f = 10$ nH. Clearly, the polarity of Δv_{sense} is opposite to that of ΔL_f which consistent with the negative sign in (4.19). However, during the current rising period, the magnitude of Δv_{sense} is extremely small, making it negligible when compared to the measured

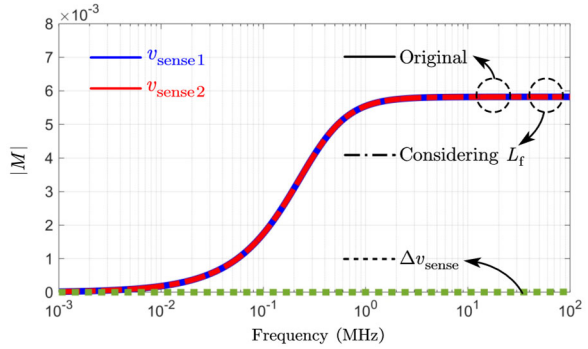


Fig. 4-16 Magnitude-frequency plot considering ΔL_f in the first scenario.

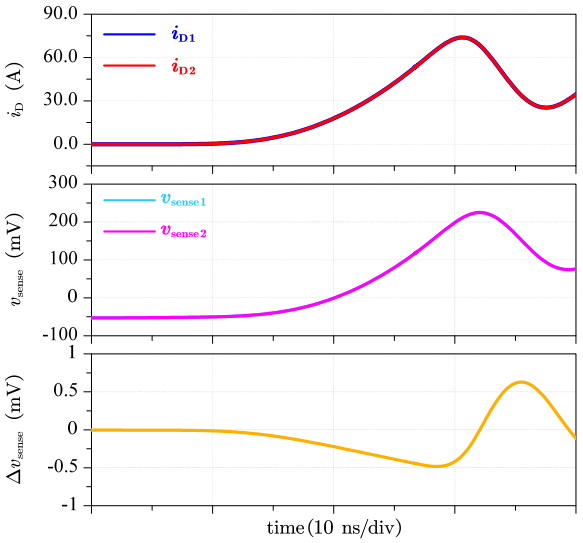


Fig. 4-17 Simulation waveforms in first scenario when $\Delta L_f = 10$ nH.

v_{sense1} and v_{sense2}. It can be concluded that, in first scenario, the impact of ΔL_f on v_{sense} is negligible. The outcome of second scenario shown in Fig. 4-15(b) is also analyzed, the v_{sense1}, v_{sense2}, and Δv_{sense} can be derived as:

$$\begin{cases} \dfrac{v_{sense1}(s)}{i_S(s)} \approx \dfrac{(s^2 L_{f1} C_f + 1) \cdot s L_{S,int}}{s^2 L_{f1} C_f + s R_f C_f + 1} \\ \dfrac{v_{sense2}(s)}{i_S(s)} \approx \dfrac{(s^2 L_{f2} C_f + 1) \cdot s L_{S,int}}{s^2 L_{f2} C_f + s R_f C_f + 1} \end{cases} \tag{4.20}$$

the difference between $v_{sense1}(s)$ and $v_{sense2}(s)$:

$$\begin{aligned} \frac{\Delta v_{sense}(s)}{i_S(s)} &= \frac{v_{sense1}(s) - v_{sense2}(s)}{i_S(s)} \\ &= \frac{s^3 R_f C_f^2 \cdot \Delta L_f}{(s^2 L_{f1} C_f + s R_f C_f + 1)(s^2 L_{f2} C_f + s R_f C_f + 1)} \end{aligned} \tag{4.21}$$

Fig. 4-18 presents the magnitude-frequency plot of (4.20) and (4.21). Unlike the first scenario, the ΔL_f in the second scenario has a significant impact within the frequency range of interest, affecting the sensing accuracy of v_{sense}. In addition, (4.21) shows that $\Delta v_{sense}(s)$ in second scenario is positively related to ΔL_f which contrasts with that in (4.19). Fig. 4-19 shows the simulation results for the circuit in Fig. 4-15(b) when $\Delta L_f = 10$ nH. During switching transient, the Δv_{sense} is much greater than that in Fig. 4-17, resulting in greater Δv_{sense} even when both i_{D1} and i_{D2} are balanced.

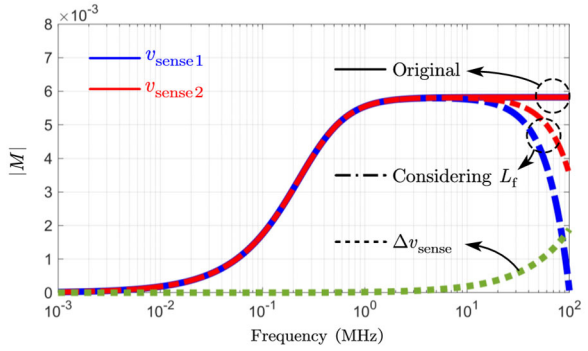


Fig. 4-18 Magnitude-frequency plot considering ΔL_f in the second scenario.

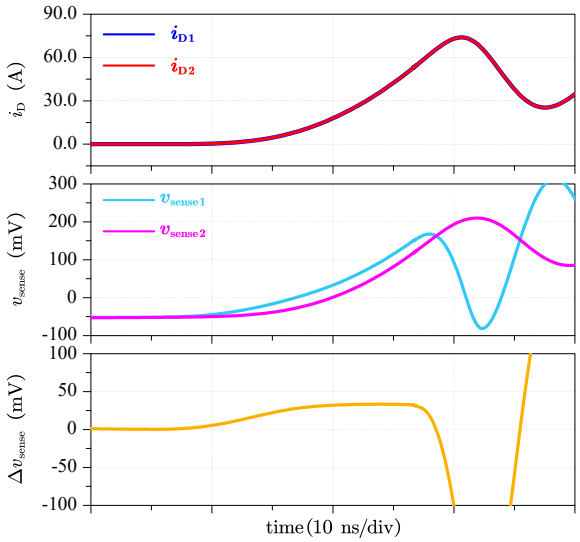


Fig. 4-19 Simulation waveforms in second scenario when ΔL_f = 10 nH.

Therefore, the layout design should avoid scenario like Fig. 5-14(b) to prevent sensing error.

Other than L_f, as shown in Fig. 4-20, the parasitic resistance R_S, which is in series with L_S, can also introduce sensing error in *di/dt*-RC sensing. Assuming that $i_S >> i_K$, the sensed signals for *di/dt*-RC sensing can be derived with consideration of R_S:

$$\begin{cases} \dfrac{v_{\text{sense1}}(s)}{i_S(s)} \approx \dfrac{sL_{S,\text{int}} + R_{S1}}{sR_fC_f + 1} \\ \dfrac{v_{\text{sense2}}(s)}{i_S(s)} \approx \dfrac{sL_{S,\text{int}} + R_{S2}}{sR_fC_f + 1} \end{cases} \tag{4.22}$$

Focusing first on a single device, Fig. 4-21 illustrates the magnitude-frequency plot based on (4.22) with different values of R_S. It is evident that the presence of R_S primarily affects the gain in the low-frequency range (below f_c). The magnitude is positively related to R_S. When comparing (4.22) to ideal case in (4.2), the position of the zero shifts from 0 to $R_{sense}/L_{S,int}$, while the system's pole remains at frequency $f_c = 1/R_fC_f$. Therefore, the gain above f_c remains unchanged. In other words, the dynamic current sensing is not affected by R_S when $R_{S1} = R_{S2}$.

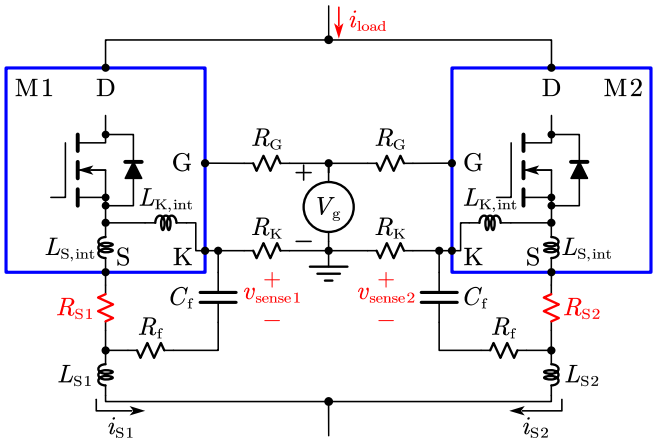


Fig. 4-20 The circuit considering the impact of parasitic R_S.

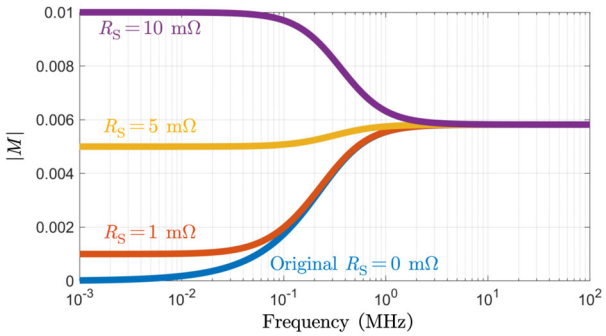


Fig. 4-21 Magnitude-frequency plot of v_{sense} with different R_S.

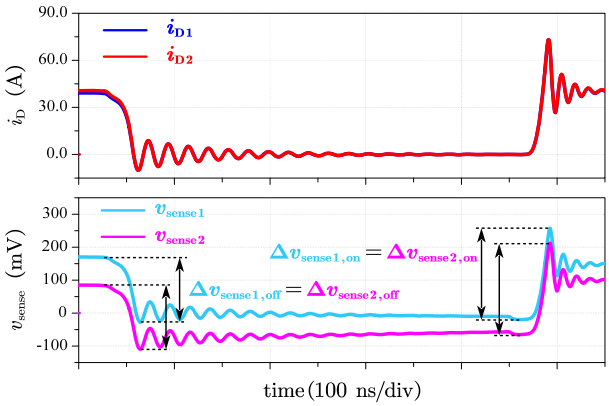


Fig. 4-22 Simulation waveforms when ΔR_S = 5 mΩ.

However, R_{S1} and R_{S2} can be different due to asymmetric layout, inconsistent device package, or unequal temperatures. According to Fig. 4-21, the value of R_S determines the gain at low-frequency range which affects the offset value of v_{sense} right before the dynamic transient. This aspect is demonstrated in Fig. 4-22, presenting the simulation waveforms when unbalanced ΔR_S = 5 mΩ occurs in the circuit. At the beginning of turn-off transient (which is the end of continuous conduction stage), since R_{S1} is higher than R_{S2}, the v_{sense1} rises to a higher initial value than v_{sense2}. During the current falling period, although the change in v_{sense1} is equal to that of v_{sense2} due to the equal gain in high-frequency range, the absolute values differ because of the different initial values. After the paralleled MOSFETs are turned off, both v_{sense1} and v_{sense2} begin to converge. However, if the devices are turned on again before v_{sense} reaches 0 V, the sensing error persists, even though the changes in v_{sense1} and v_{sense2} are equal.

4.1.5 Design Considerations for Paralleled Devices

According to the above analysis, when designing *di/dt*-RC sensing for paralleled devices, several layout suggestions are proposed:

- If v_{sense} is sensed directly across the C_f in Fig. 4-15(a), it is not necessary to create identical layout for RC sensing branches to achieve equal L_f.
- If v_{sense} is sensed across both C_f and L_f in Fig. 4-15(b), the layout for RC sensing branch must be symmetric.
- The power traces that include R_S and $L_{S,int}$ should be identical since both components separately affect low- and high-frequency gains.

It is important to note that temperature distribution can affect the values of R_S and results in sensing error. The equivalent R_S is the sum of parasitic resistance on bonding wire, device's pin, and PCB trace. For metallic materials, a temperature difference of several tens of degrees Celsius is typically required to cause a variation in the order of mΩ. Also, in closely spaced paralleled devices, the pins and PCB copper traces are interconnected, leading to similar changes in temperatures. In practice, it is unlikely to have dramatic temperature difference between paralleled devices.

For the sensing circuitry, the conventional structure shown in Fig. 4-3 should be avoided, as it adversely affects sensing accuracy, especially if the unbalanced currents are caused by mismatched devices. The conventional structure may provide erroneous information to the processing circuit. From the perspective of sensing accuracy, the proposed R_K sensing structure in Fig. 4-6 should be implemented to improve the sensing performance.

Regarding system integration, the components R_f and C_f can utilize surface-mounted devices (SMD) with small package since they are all grounded to the driving ground potential. In addition, the presence of RC branch has no impact on original current sharing conditions due to minimal current flows through these components [132].

On the other hand, the selection of R_K depends on circuit condition and the degree of i_{cir}. The value of R_K can be determined by referring to Fig. 4-9 and Fig. 4-13, and it should be large enough to suppress i_{cir} while remaining small enough to minimize additional power losses and prevent

crosstalk induced by Miller current [128]. The tolerance of R_K must also be considered, as R_K affects equivalent gate driving resistance. Similar to R_G, a mismatch in R_K can result in different switching speeds among paralleled devices. It should also be noted that the presence of R_K slightly affects the current sharing condition. As concluded in [127], for unbalanced currents caused by asymmetric layout, the impedance on KS path should be minimized to enhance current sharing. Conversely, for mismatched devices, R_K helps improve current sharing because the opposing direction of i_{cir} mitigates the difference in equivalent v_{GS} between paralleled devices [137]. However, in real applications, it is difficult to distinguish whether the unbalanced dynamic currents are caused by asymmetric layout, mismatched devices, or a combination of both factors.

4.1.6 Experimental Verifications

A DPT environment shown in Fig. 4-23 is used to verify the proposed R_K sensing structure, the circuit and testing environment are previously shown in Fig. 2-17(a) and (b). The testing parameters are listed in Table 4-1. The SiC MOSFETs M1 and M2 are soldered on the power board and driven by a single gate driver IC on the gate driver board. The sensing components R_f, C_f, and R_K, are all positioned on the gate driver board. The values of R_f and C_f are 357 Ω and 1 nF, respectively. Following the layout suggestions in Section 4.1.5, the layout of each MOSFET is identical to the others, indicating a symmetric R_S and L_f in paralleled branches. Also, v_{sense} is measured directly across the C_f on the measuring rings to ensure sensing accuracy. It should be noted that due to the low voltage level of v_{sense}, the measurement may be affected by noise. The measurement can be improved by adding chokes, adjusting oscilloscope's filter settings, or minimizing the probing loop.

To estimate the gain for *di/dt*-RC sensing, the $L_{S,int}$ of the device is extracted experimentally. Fig. 4-24 shows the experimental waveforms of v_{SK} and i_S. During the current-rise period, the $L_{S,int}$ can be calculated in (5.26) by averaging the results at different time points. It is estimated that the $L_{S,int}$ of C3M0016120K on the tested board is around 2.91 nH. According to (4.2), the gain at high-frequency range of the *di/dt*-RC sensing can be calculated as 8.15 mV/A.

$$v_{SK} = -L_{S,int}\frac{di_S}{dt} \Rightarrow \begin{cases} \text{A: } L_{S,int} = 2.93 \text{ nH} \\ \text{B: } L_{S,int} = 3.02 \text{ nH} \\ \text{C: } L_{S,int} = 2.78 \text{ nH} \end{cases} \tag{4.23}$$

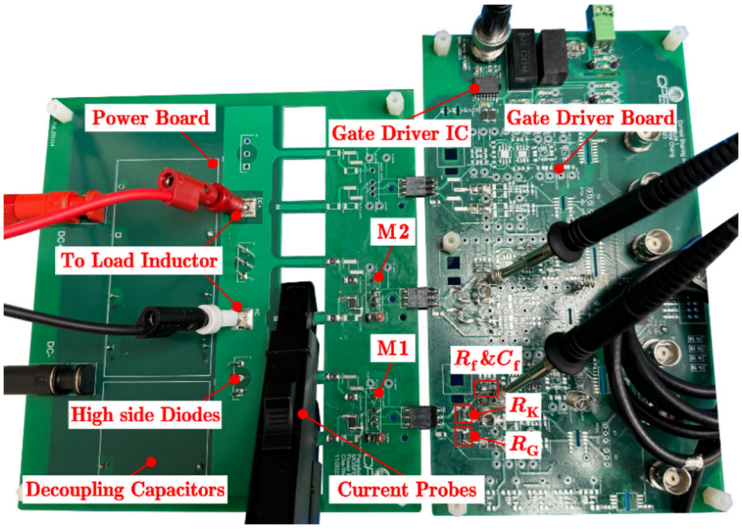


Fig. 4-23 The test boards to verify *di/dt*-RC sensing.

TABLE 4-1 EXPERIMENTAL TESTING CONDITIONS

Symbols	Values
V_{DC}	600 V
V_g	15 V/-5 V
C_{DC}	286 μF
C_{dec}	14.4 μF
i_{load}	30 A
L_{load}	185 μH
R_f	357 Ω
C_f	1 nF

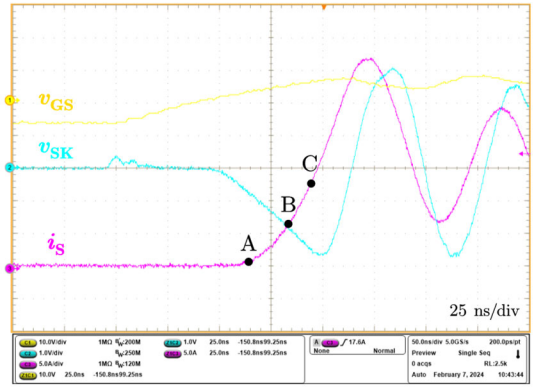


Fig. 4-24 Experimental waveforms of v_{SK} and i_S for estimating $L_{S,int}$.

1) Current Sensing under Asymmetric Layout

To exaggerate the impact of asymmetric layout, the L_{ext} is soldered on the PCB, making L_{S1} 16 nH smaller than L_{S2}. The paralleled devices are pre-screened by using curve tracer to select those with similar V_{th}. Fig. 4-25(a) shows the experimental waveform using conventional sensing

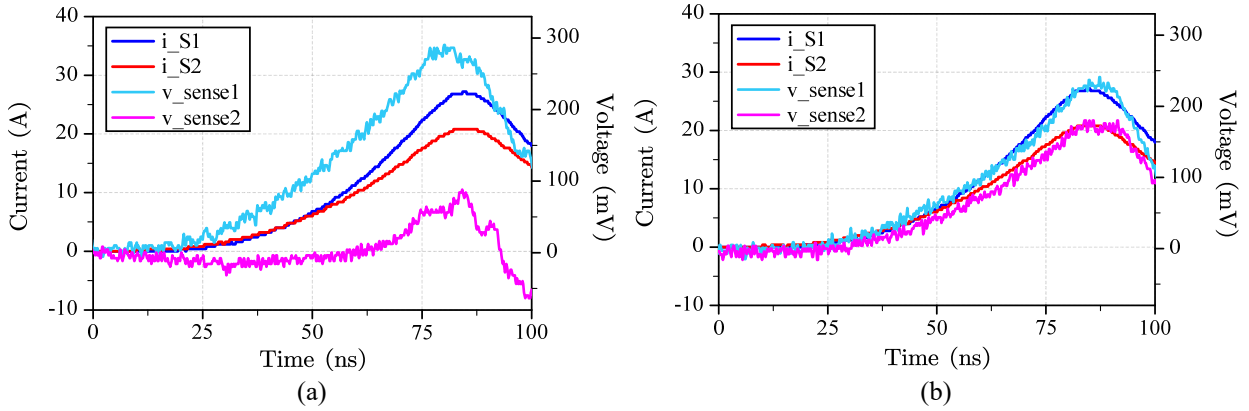


Fig. 4-25 Experimental waveforms of v_{sense} under asymmetric layout (a) conventional sensing structure (b) proposed R_K sensing structure.

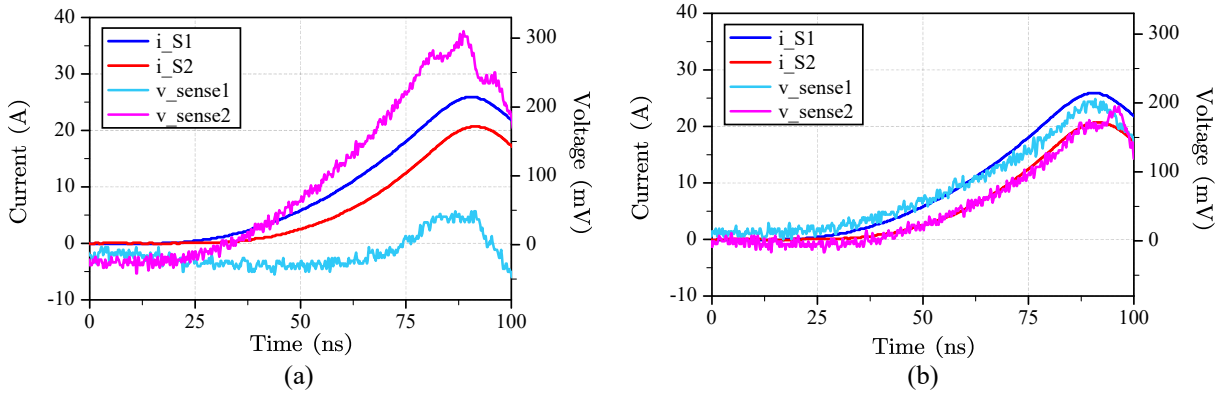


Fig. 4-26 Experimental waveforms of v_{sense} under mismatched devices (a) conventional sensing structure (b) proposed R_K sensing structure.

structure with R_G = 15 Ω and R_K = 0 Ω per device. Without R_K, obviously, the i_{cir} affects the sensing accuracy, causing the difference between v_{sense1} and v_{sense2} to be much larger than that between actual i_{S1} and i_{S2}. The result matches with performed analysis, which indicates that i_{cir} enlarges the Δv_{sense} in asymmetric layout case.

Fig. 4-25(b) demonstrates the effectiveness of the proposed R_K sensing structure. Based on the guidance in Fig. 4-9, the R_G and R_K are selected as 13.5 Ω and 1.5 Ω, respectively, to mitigate the degree of i_{cir} down to around 10 %. Since the equivalent gate driving resistance still equals to 15 Ω, the current rising time remains unchanged. Moreover, both v_{sense1} and v_{sense2} in Fig. 4-25(b) accurately capture the dynamic currents, significantly improving the accuracy compared to Fig. 4-25(a). By adopting the proposed R_K sensing structure, v_{sense} can provide correct information for signal processing circuit.

2) Current Sensing under Mismatched Devices

Similarly, Fig. 4-26 shows the experimental waveforms under mismatched devices $V_{th1} < V_{th2}$ while $L_{S1} = L_{S2}$. The devices are also pre-screened to select the devices with a ΔV_{th} of 0.7 V between them. Fig. 4-26(a) shows the waveforms when using conventional structure with R_G of 15 Ω and R_K of 0 Ω per device. Despite i_{S1} being greater than i_{S2}, the presence of i_{cir} results in the sensed v_{sense1} being much smaller than v_{sense2}. The trend aligns with previous analysis, potentially leading to erroneous information received by the signal processing circuit.

In Fig. 4-26(b), the proposed R_K sensing structure is implemented with R_G = 13.5 Ω and R_K = 1.5 Ω. Obviously, during the current-rise period, the sensed v_{sense1} and v_{sense2} accurately track the actual i_S. The v_{sense} or Δv_{sense} can effectively indicate the mismatched dynamic currents, enabling the processing circuit to determine which device is conducting a higher dynamic current. The experimental results validate the proposed R_K sensing structure for paralleled SiC MOSFETs.

3) Current Sensing for Three Paralleled Devices

The proposed R_K sensing structure can be easily extended to more than two paralleled devices. The SiC MOSFETs are Infineon IMZA120R007M1H. An additional device, labeled as M3, is soldered on the power board. All devices are randomly selected from a batch of purchased devices since it is impractical to screen all devices in real applications. By following a similar process, the $L_{S,int}$ of IMZA120R007M1H on the board is estimated as 2.26 nH, and the gain of the *di/dt*-RC sensing is calculated as 6.33 mV/A. Fig. 4-27(a) shows the baseline waveforms when $L_{S1} > L_{S2} > L_{S3}$ with R_G = 10 Ω and R_K = 0 Ω for each device. The turn-on sequence can be observed as i_{D3}, followed by i_{D2} and i_{D1}, leading to an inverse relationship of v_{sense} at the beginning of the turn-on transient. During the current-rise period, due to the asymmetric layout, the relationship of v_{sense} starts to correspond to the actual currents, with v_{sense3} rising faster than v_{sense2} than v_{sense1}. In overall, the accuracy of v_{sense} is not ideal for signal processing circuit.

Fig. 4-27(b) shows the experimental waveforms after adopting the proposed R_K sensing structure. The R_G and R_K are selected as 8.7 Ω and 1.3 Ω, respectively. Apparently, the tracking performance of v_{sense} is significantly improved compared to the conventional structure in Fig. 4-27(a), especially at the beginning of the turn-on transient. The relationship between v_{sense} signals reflects to the

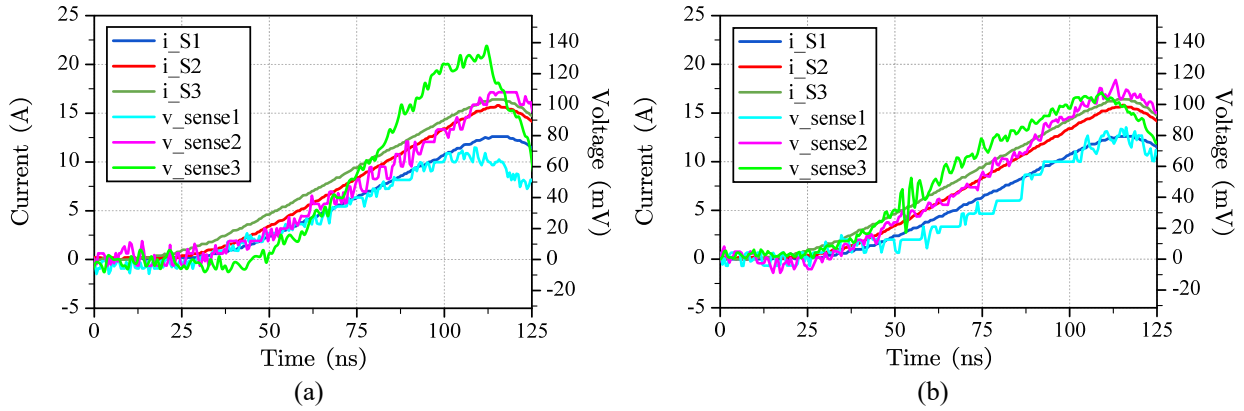


Fig. 4-27 Experimental waveforms of multiple devices (a) conventional sensing structure and (b) proposed R_K sensing structure.

actual unbalanced dynamic currents, providing correct information to signal processing circuit. The experimental results validate the proposed R_K sensing structure for multiple paralleled devices.

4.1.7 Extension and Discussion

1) *di/dt*-RC Sensing for SiC Power Modules

The proposed R_K sensing structure can also be used for paralleled power modules. However, due to the multi-die structure within the modules, the required gate current can be higher compared to single-die discrete devices under equal voltage rating. According to (4.1), assuming $i_G \approx i_K$, the measured v_{sense} may exhibit a pronounced negative offset right before the turn-on dynamic transient. Additionally, while the total power current flowing through the power module can be measured, it is not possible to measure the current for each individual die within the module. This limitation makes the di/dt-RC sensing less appealing for use in paralleled power modules.

2) KS Differential Mode Choke (KS-DMC) Sensing Structure

An alternative sensing structure can achieve similar purpose with R_K sensing structure. As shown in Fig. 4-28, a KS-DMC is placed on KS paths to balance i_K and suppress i_{cir}. When i_{K1} and i_{K2} are well-balanced, the magnetic flux of the KS-DMC equals 0. If the i_{cir} appears due to asymmetric layout or mismatched devices, according to the dot convention, the induced voltages on two windings are opposite which help suppress i_{cir}. The KS-DMC with magnetizing inductance L_m provides impedance to suppress unbalanced i_{cir} while the switching speed is still determined by

the R_G.

For KS-DMC, there are two potential locations. In Fig. 4-28(a), the first option places KS-DMC between the RC sensing branches and the driving ground. The second option, shown in Fig. 4-28(b), positions the KS-DMC between the RC sensing branches and devices' KS pins. Their differences in placement and their impact on di/dt-RC sensing are analyzed.

In Fig. 4-28(a), the KS-DMC does not affect the operation of di/dt-RC sensing. The v_{sense} and Δv_{sense} continue to adhere to the same equations in (4.3) and (4.5) but with a much smaller i_{cir}. Since the i_{cir} is greatly suppressed by L_m, Δv_{sense} reflects actual differences between the unbalanced dynamic currents like those in Fig. 4-10 and Fig. 4-14.

On the other hand, in Fig. 4-28(b), the KS-DMC affects the accuracy of v_{sense1} and v_{sense2} which can be expressed as:

$$\begin{cases} v_{\mathrm{sense1}}(s) = \dfrac{[sL_{\mathrm{S,int}}\, i_{\mathrm{S1}} - sL_{\mathrm{K,int}}\, i_{\mathrm{K1}}(s) - sL_{\mathrm{m}}\, i_{\mathrm{cir}}]}{sR_{\mathrm{f}}C_{\mathrm{f}} + 1} \\ v_{\mathrm{sense2}}(s) = \dfrac{[sL_{\mathrm{S,int}}\, i_{\mathrm{S2}} - sL_{\mathrm{K,int}}\, i_{\mathrm{K2}}(s) + sL_{\mathrm{m}}\, i_{\mathrm{cir}}]}{sR_{\mathrm{f}}C_{\mathrm{f}} + 1} \end{cases} \tag{4.24}$$

By substituting (4.4) into (4.24) with focus on high-frequency range, the Δv_{sense} can be obtained:

$$\Delta v_{\mathrm{sense}} = \frac{L_{\mathrm{S,int}}}{R_{\mathrm{f}}C_{\mathrm{f}}}\Delta i_{\mathrm{S}} - \frac{2(L_{\mathrm{K,int}} + L_{\mathrm{m}})}{R_{\mathrm{f}}C_{\mathrm{f}}}\, i_{\mathrm{cir}} \tag{4.25}$$

According to (4.25), even though the i_{cir} is suppressed by L_m, the Δv_{sense} is still affected by the product of L_m and i_{cir}, resulting in sensing error. The Δv_{sense} still behaves like that in (4.5) and Fig. 4-5: it is amplified in asymmetric layout case and is reduced or inverted when the devices exhibit V_{th} mismatch.

While the KS-DMC sensing structure in Fig. 4-28(a) helps improve sensing accuracy, the product of L_m and i_{cir} induces voltage ringing on DMC, which can further affect the v_{GS} of paralleled devices.

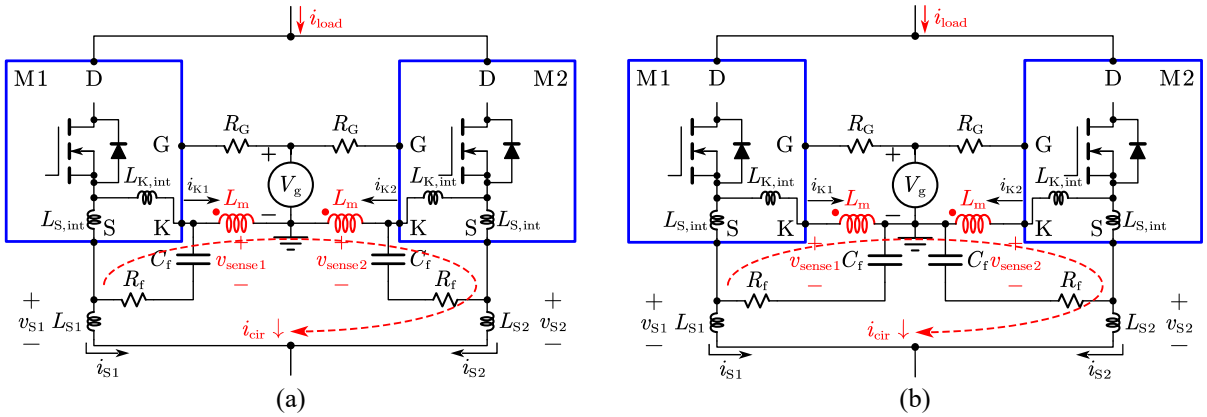


Fig. 4-28 Proposed KS-DMS sensing structure considering various locations for KS-DMC.

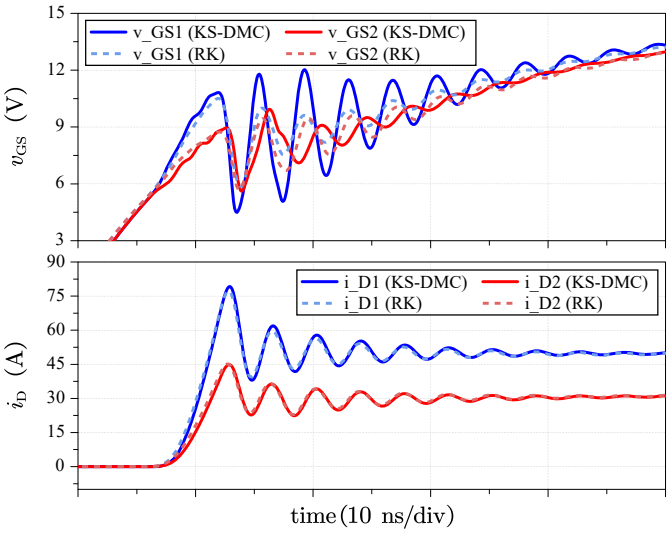


Fig. 4-29 Comparison of v_{GS} waveforms when using KS-DMC sensing structure and R_K sensing structure.

Fig. 4-29 illustrates the comparison of v_{GS} between R_K sensing structure and KS-DMC sensing structure. Both structures operate under the same conditions, resulting in the same unbalanced currents of i_D. In R_K sensing structure, v_{GS} stabilizes after the first current peak. In contrast, the KS-DMC sensing structure exhibits greater voltage oscillation in v_{GS}. Moreover, the leakage inductance of the DMC inevitably slows down the switching speed. Thus, when comparing the two, the R_K sensing structure emerges as a simpler and more convenient solution, especially when extended it to multiple devices.

Based on the analysis and experimental verifications in this section, to sense dynamic currents in paralleled devices, the *di/dt*-RC sensing with enhanced R_K sensing structure is the optimal method due to its low-cost and high scalability. The design of AGD is presented in the next section.

4.2. Active Gate Driver (AGD) for Dynamic Current Balancing

4.2.1 Active Balancing Methodology

The detailed design of the proposed AGD is introduced in this section, including the balancing method, signal processing circuit, and driving circuit. Fig. 4-30 compares the turn-on switching waveforms of SiC MOSFET using conventional gate driver (CGD) and AGD.

In CGD case as shown in Fig. 4-30(a), upon receiving the turn-on signal V_{PWM} at t_0, the gate driving voltage V_g is set to a constant voltage of V_{DD}, charging the C_{GS} of all paralleled devices. The delay between t_0 and t_1 results from inherent response time of driving components. Throughout the turn-on process, including turn-on delay t_d and rising time t_r, the V_g remains at V_{DD}.

In contrast, the proposed AGD shown in Fig. 4-30(b) actively controls the V_g of each device based on unbalanced dynamic currents obtained from the *di/dt*-RC sensing. During dynamic switching transients, the SiC MOSFET can be modeled as a voltage-controlled current-source, where the channel current can be regulated by the applied V_g. To accelerate the charging of C_{GS}, the AGD initially applies a higher voltage V_{DD1} during t_d. Once the v_{GS} reaches V_{th} and starts conducing current, V_g reduces to a lower V_{DD2} during t_r to control the slew rate *di/dt* of the current, thereby achieving balanced current sharing.

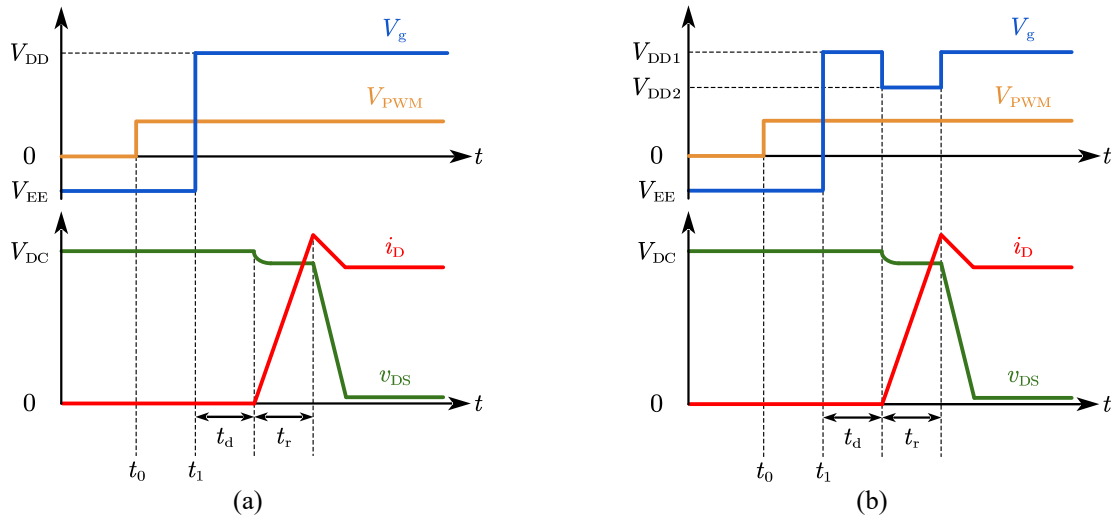


Fig. 4-30 Comparison of switching waveforms using (a) CGD and (b) AGD.

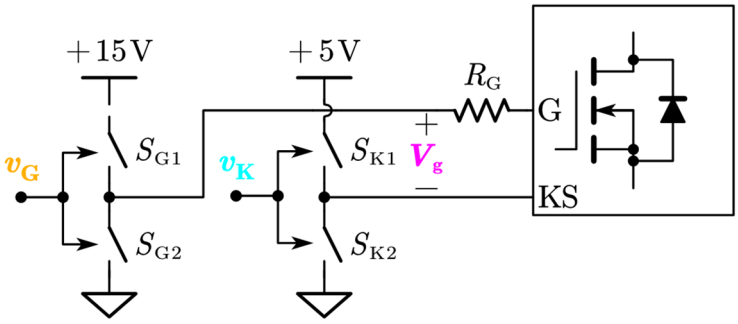


Fig. 4-31 Conceptual circuit diagram of driving circuit to achieve multi-voltage gate control.

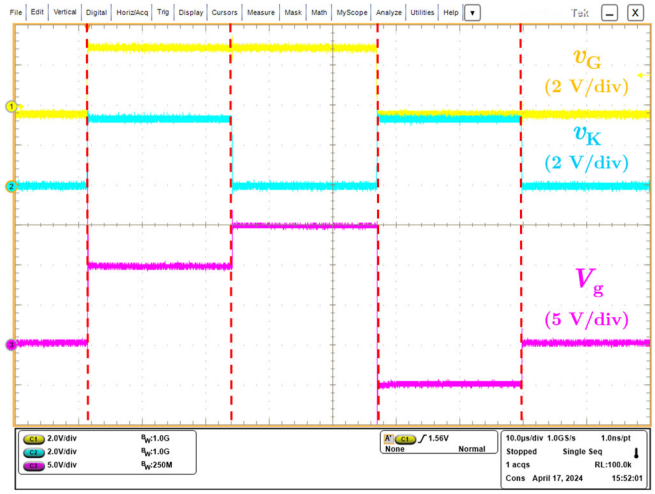


Fig. 4-32 Experimental waveform of driving circuit.

To realize the multi-voltage control of V_g illustrated in Fig. 4-30(b), Fig. 4-31 presents the conceptual diagram with designated current boosters connected to device's gate and KS pins. These current boosters are driven by driving signals v_G and v_K from the controller, producing the V_g as shown in Fig. 4-32. By applying high-low logic combinations of v_G and v_K, four voltage levels of V_g can be generated to drive the devices:

- Both v_G and v_K are logic high: S_{G1} and S_{K1} are turned on, equivalent V_g = 10 V.
- The v_G is logic high and v_K is logic low: S_{G1} and S_{K2} are turned on, equivalent V_g = 15 V.
- The v_G is logic low and v_K is logic high: S_{G2} and S_{K1} are turned on, equivalent V_g = -5 V.
- Both v_G and v_K are logic low: S_{G2} and S_{K2} are turned on, equivalent V_g = 0 V.

The +15 V and +10 V can be used for turning on the devices, while -5 V and 0 V are for turn-off.

The current-balancing methodology is depicted in Fig. 4-33 over the switching cycles. In Fig. 4-33(a), though paralleled devices received V_g simultaneously, the i_{D1} turns on earlier than i_{D2} due

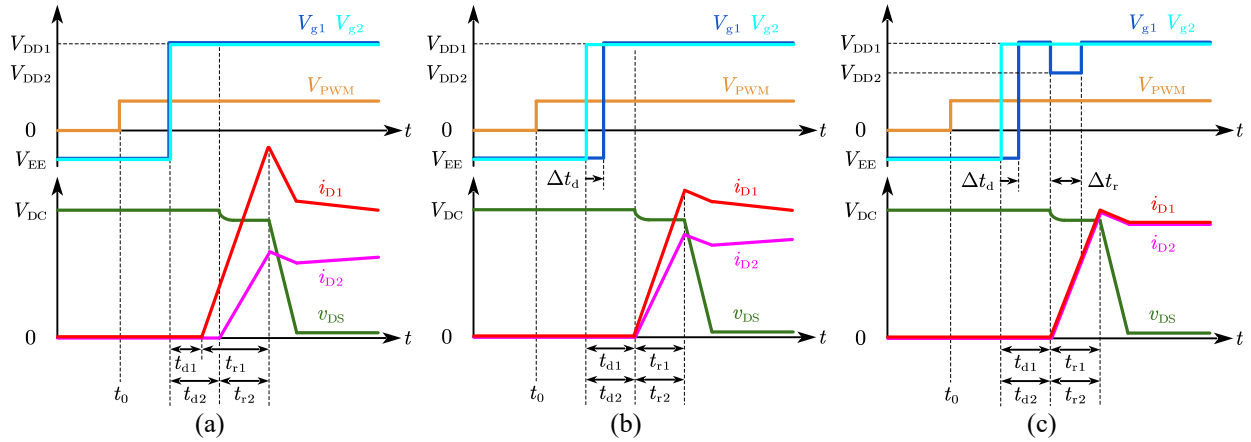


Fig. 4-33 Current-balancing methodology to gradually balance currents (a) 1st cycle, (b)2nd cycle, and (c) 3rd cycle.

to a lower V_{th}, and further exhibits a greater *di/dt* because of asymmetric layout. To compensate for the mismatched V_{th}, in the next cycle as shown in Fig. 4-33(b), the turn-on timing of V_{g1} is delayed by a short period of time Δt_d to synchronize the current turn-on edges. Next, a Δt_r is introduced, reducing V_{g1} to V_{DD2} to slow down the charging speed of i_{D1} and further align the *di/dt*. Both Δt_d and Δt_r are gradually adjusted on a cycle-by-cycle basis. The controller is programmed to prioritize synchronizing the current edges, followed by aligning the dynamic current *di/dt*.

4.2.2 Circuit Structure of the AGD

Fig. 4-34 shows the overall structure of the proposed AGD, consisting of three main functions:

- Current sensing: The *di/dt*-RC sensing with enhance R_K sensing structure is used to detect individual device's current i_S and generate sensed signal v_{sense}.
- Signal processing: The sensed v_{sense} is amplified by op-amp-based differential-to-single-ended circuit, and comparator circuit outputs v_{c1} and v_{c2} to indicate current's turn-on edge and slew rate.
- Driving circuit: Based on the information of currents, driving signals are sent by the controller, and designated current boosters allow multi-voltage of V_g to actively control the applied V_g of SiC MOSFET.

In Fig. 4-34, once the v_{sense} is generated based on current i_S, a differential-to-single-ended (D2SE) circuit is implemented to amplify the v_{sense} by a designed gain of 5. This circuit inverts the negative

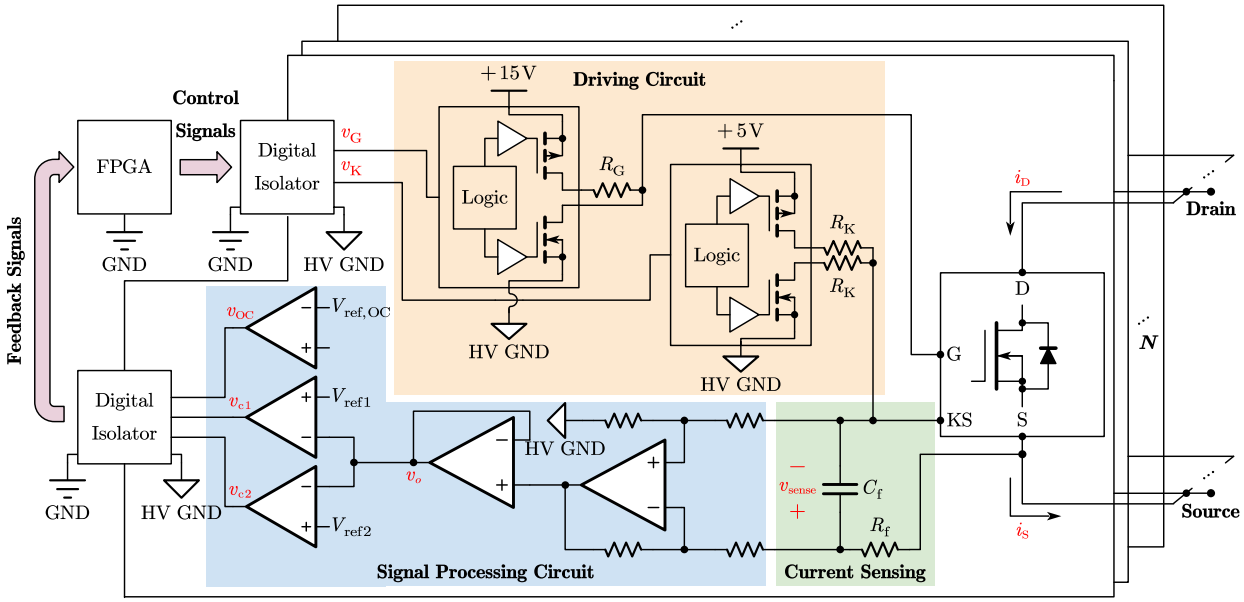


Fig. 4-34 Overall structure of the proposed AGD.

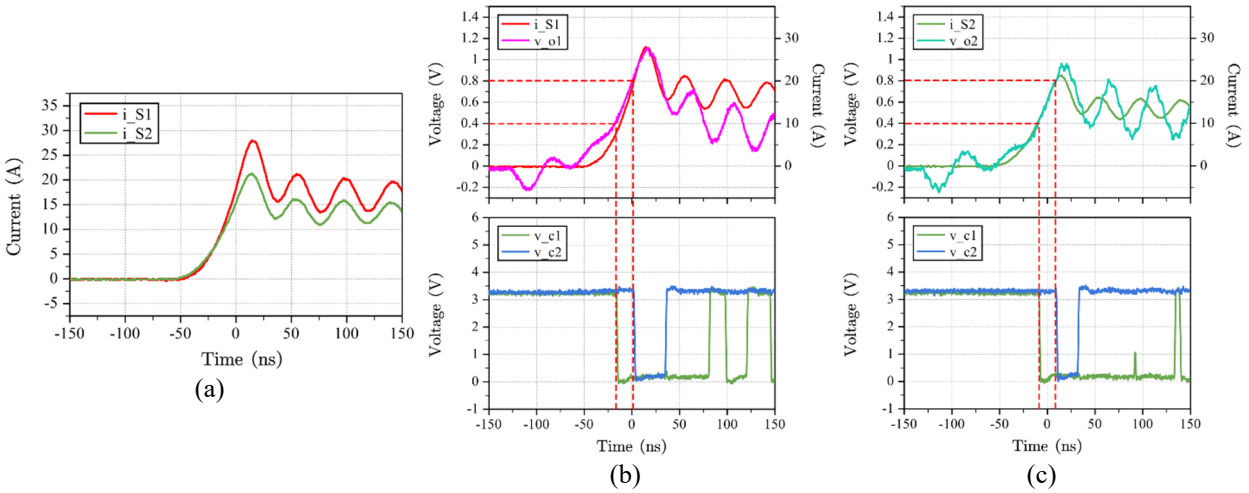


Fig. 4-35 Experiment waveforms of (a) real current, (b) feedback signals of MOSFET 1, and (c) feedback signals of MOSFET 2.

v_{sense} to a positive output voltage v_o for reference comparison, and a voltage follower is connected to provide infinite input impedance. Depending on the noise sensitivity, the single-op-amp D2SE can also be replaced by the three-op-amp amplifier configuration to improve common-mode noise rejection.

The amplified signal v_o is then processed by two comparators to detect both turn-on edge and slew rate of current i_S. Fig. 4-35 shows the experimental waveforms of key signals. During the turn-on transient, the v_o directly reflect the dynamic currents i_S. Once v_o surpasses the first reference

voltage V_{ref1}, which is set as 0.4 V, comparator 1 generates a falling-edge signal v_{c1}. As the v_o continuously rises beyond the second reference voltage V_{ref2}, which is 0.8 V, comparator 2 generates another falling-edge signal v_{c2}. Both v_{c1} and v_{c2} are transmitted through digital isolator to the FPGA controller for subsequent logic control.

An XOR logic gate is programmed in the FPGA to extract current information. As shown in Fig. 4-36 together with Fig. 4-35, during t_d, both v_{c1} and v_{c2} are logic high, keeping the v_{XOR} remains as logic low. Once the falling edge of v_{c1} is detected, the v_{XOR} switches to logic high. And when the falling edge of v_{c2} is also detected, the v_{XOR} returns to logic low. In this way, both the turn-on edge and slew rate can be identified from v_{XOR}. A clock frequency of 84 MHz is selected to ensure precise timing resolution. By comparing v_{XOR} from paralleled SiC MOSFETs, the relative current imbalance can be determined, enabling the FPGA to generate appropriate driving signals v_G and v_K for actively control of individual SiC MOSFET.

Each SiC MOSFET is equipped with its own set of current sensing, signal processing, and driving circuits. The gate resistance R_G is connected to the source of the gate current booster, while the R_K sensing structure is adopted to improve sensing accuracy. Two R_K are placed at both source and sink of KS current booster, allowing accurate measurement when turning on at either +15 V or +10 V. For active Miller clamp (AMC) protection, the device can be clamped at 0 V and a diode D_{AMC} is introduced to bypass R_K, creating a small-impedance current path for Miller current. In addition, a third comparator with a higher reference threshold $V_{ref,OC}$ is used for overcurrent detection of each individual device. Most importantly, only a single FPGA is required in the proposed AGD structure, which makes it well-suited for industry applications. For instance, in a 3-phase traction inverter, the proposed single-controller AGD significantly reduces system cost when compared to multi-controller approaches in the literature.

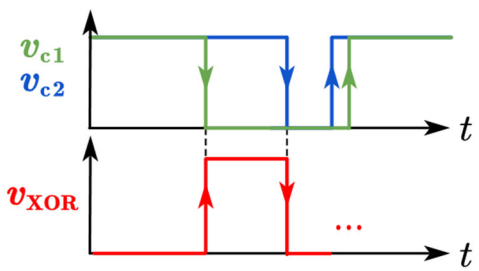


Fig. 4-36 The XOR function in FPGA.

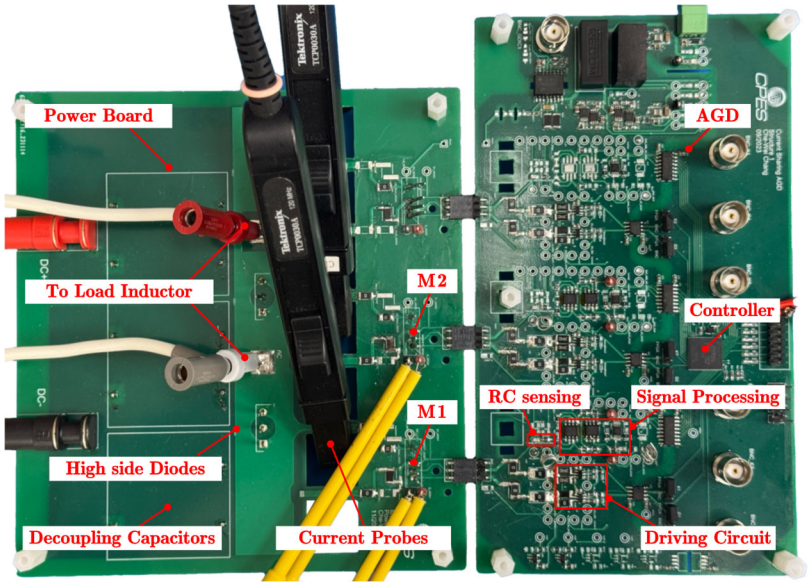


Fig. 4-37 Top view of designed AGD.

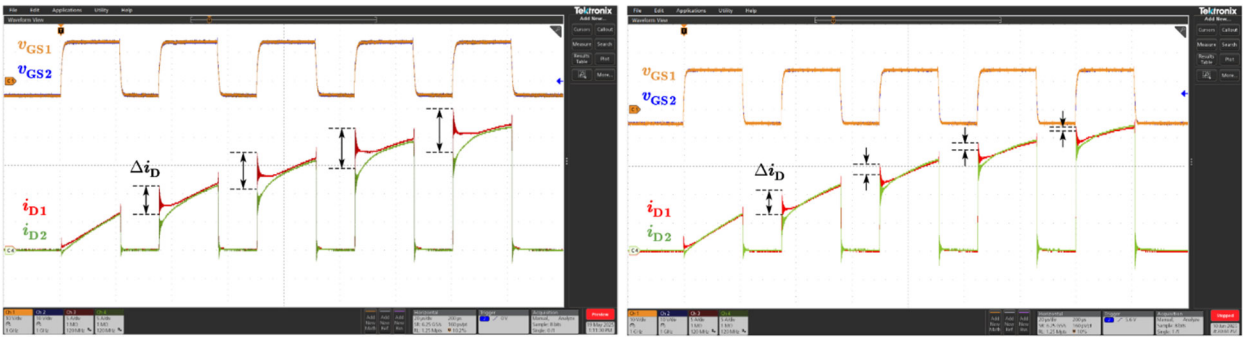
4.2.3 Experimental Verification

The DPT environment in Fig. 2-17(b) is used to verify the proposed AGD which is shown in Fig. 4-37. This setup has been explicitly detailed in Chapter 2. In total 5 pulses of driving signals are generated to drive both M1 and M2, and the experimental waveforms are shown in Fig. 4-38.

In Fig. 4-38(a), by using CGD, both M1 and M2 are driven by the same signal and driving voltage. Consequently, the current difference Δi_D is determined by the degree of asymmetric layout and mismatched devices, leading to unbalanced currents. As the total load current increases, the Δi_D further increases across switching cycles.

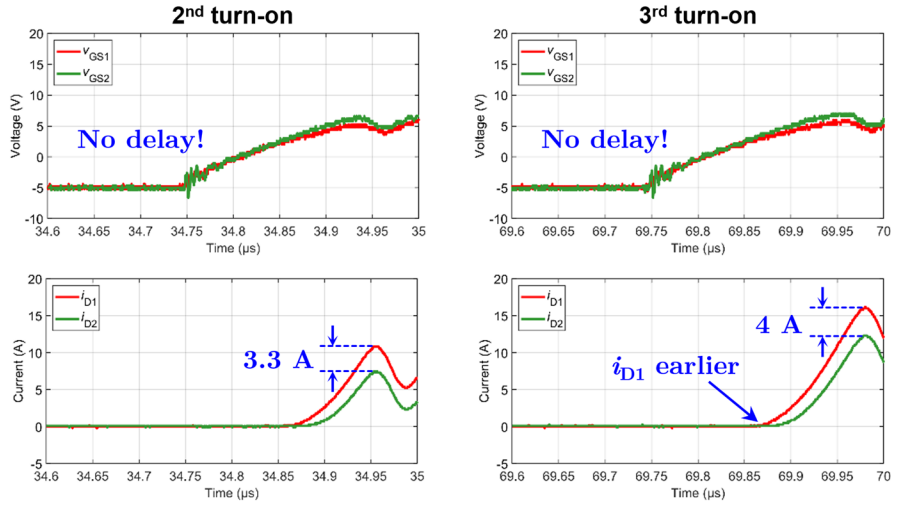
In contrast, the performance of the proposed AGD is demonstrated by open-loop tests in Fig. 4-38(b). By enabling flexible adjustment of both turn-on timing and driving voltage, the AGD actively suppresses current divergence. As a result, the dynamic currents are significantly more balanced compared to Fig. 4-38(a). The experimental results validate the effectiveness of the proposed AGD.

Fig. 4-39 shows the zoom-in waveforms of dynamic transients in Fig. 4-38, focusing on the 2nd and 3rd turn-on events. In Fig. 4-39(a), the CGD charges both v_{GS1} and v_{GS2} at the same time with the same V_g. Because of the mismatched V_{th}, M1 turns on earlier than M2, resulting in a higher i_{D1}

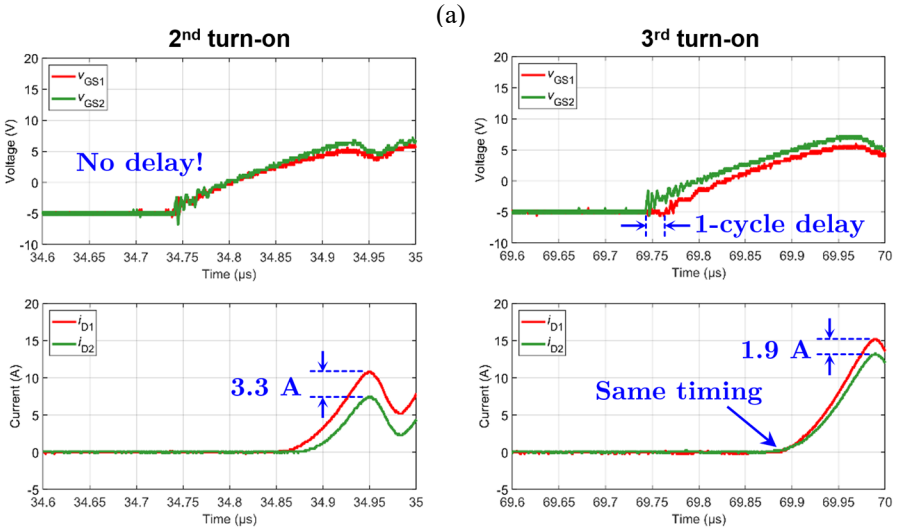


(a) (b)

Fig. 4-38 Experimental cycle-by-cycle waveforms by using (a) CGD and (b) proposed AGD.



(a)



(b)

Fig. 4-39 Based on Fig. 5-37, the zoom-in transients of 2nd and 3rd turn-on events by using (a) CGD without adjusting delay and (b) proposed AGD with adjusting delay.

at the beginning. Additionally, during the current rising period, i_{D1} has a greater *di/dt* caused by smaller L_{S1}, leading to a $\Delta i_{D,peak}$ around 3.3 A and 4 A at the 2nd and 3rd turn on events, respectively. The waveforms of AGD is shown in Fig. 4-39(b), and both M1 and M2 in the 2nd turn-on event are driven by the same $V_g = V_{g1} = V_{g2}$ without adjusting delay. Once the *di/dt*-RC sensing senses the unbalanced currents and feedback to FPGA, started from the 3rd turn-on event, the V_{g1} is delayed by one clock cycle. Consequently, the turn-on timing of M1 is adjusted, and both i_{D1} and i_{D2} conduct currents at the same timings. However, the asymmetric layout still exists which leads to a greater *di/dt* of i_{D1} than i_{D2}, thereby resulting in a $\Delta i_{D,peak}$ around 1.9 A.

The effect of varying V_g is presented in Fig. 4-40, showing the 3rd, 4th, and 5th turn-on events. As described in Fig. 4-32, when v_G remains high all the time, the equivalent driving voltage V_g is 15 V when v_K is low, and becomes 10 V when v_K is high. For the CGD case in Fig. 4-40(a), the v_{K1} =

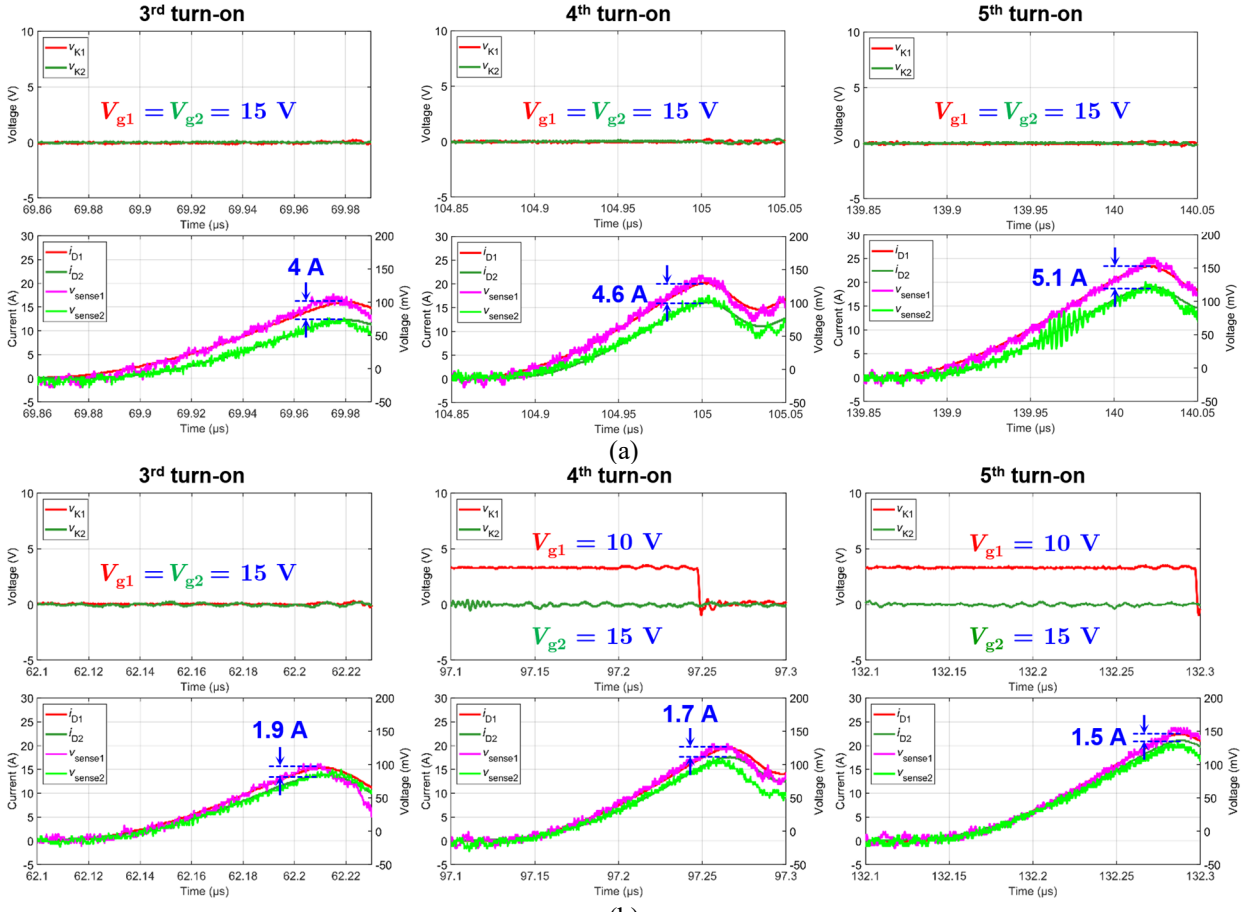


Fig. 4-40 Based on Fig. 5-37, the zoom-in transients of 3rd, 4th, and 5th turn-on events by using (a) CGD without adjusting delay and applied V_g and (b) proposed AGD with adjusting delay and applied V_g.

v_{K2} = 0 V are always low across the cycles, and M1 and M2 are being driving by $V_{g1} = V_{g2}$ = 15 V. The corresponding $\Delta i_{D,peak}$ in 3rd, 4th, and 5th events are 4 A, 4.6 A, and 5.1 A, respectively.

In contrast, Fig. 4-40(b) shows that the proposed AGD begins adjusting V_{g1} in the 4th turn-on event to match *di/dt* of paralleled devices. As a result, the $\Delta i_{D,peak}$ is significantly reduced compared to Fig. 4-40(a). Moreover, in all cases, the sensed signal v_{sense} closely follows the actual current i_D, verifying the sensing accuracy of the proposed sensing structure in Section 4.1. These experimental results validate the effectiveness of the proposed AGD.

4.3. Conclusion

For current imbalance among paralleled devices, it is crucial to note that there is a behavioral difference between asymmetric layout case and mismatched devices case. The experimental results in Fig. 4-4 show that while the actual current i_{D1} is larger than i_{D2} in both cases, the difference between the source voltage potentials Δv_S (voltage across source inductance) in two cases are in entirely opposite direction. This behavioral difference creates an opposite direction of i_{cir} which affects the accuracy of conventional *di/dt*-RC sensing structure, potentially leading to erroneous trigger or information received by the employed processing circuit. To address this issue, the proposed R_K sensing structure should be adopted. Furthermore, the effectiveness of the proposed AGD is verified by the experimental results, balancing the currents regardless of original cause of current imbalance. With only one controller needed, the proposed AGD presents an attractive option, making it a strong candidate for high-power applications where precise current balancing is required.

Chapter 5
Systematic Integration Strategy for High-Density Inverter

5.1. Introduction

The challenges related to device-level current sharing have been thoroughly analyzed and addressed in the previous chapters, with proposed current-balancing solutions verified. At the system level, however, achieving power density targets remains a significant challenge. As discussed in Chapter 1, there is still a gap between most current inverter designs and DOE's 2025 power density target of 100 kW/L. Commercial EV inverters typically achieve no more than 30 kW/L, while the highest density reported in academia to date is approximately 71 kW/L [64]. To move beyond this bottleneck, it is essential to first examine the component-level breakdown of a traction inverter, identifying the major components and reviewing their state-of-the-art technologies, before exploring strategies for system-level improvement.

As indicated in the inverter structure diagram in Fig. 1-1, research efforts for improving power density have targeted in five major areas, including:

- Topology developments and control schemes
- Power device materials, packaging, and drivers
- Capacitor technologies
- Cooling techniques
- Advanced current sensors

Among topology candidates shown in Fig. 5-1, the three-phase 2L VSI is the most adopted in commercial EVs, favored for its simplicity and cost-effective. As a tradeoff, it introduces greater harmonics and steeper *dv/dt* at output nodes, leading to insulation challenge of motor winding. Multilevel topology like three-level (3L) TNPC alleviates these challenges by introducing

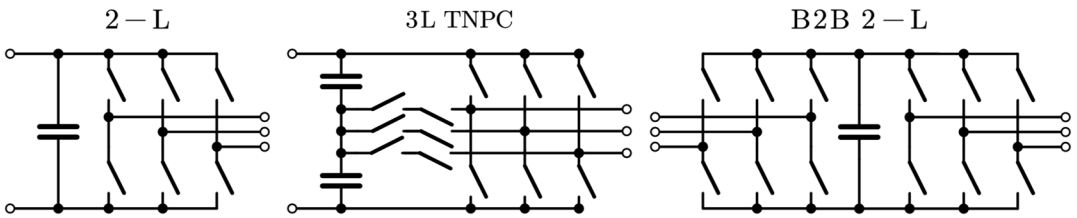


Fig. 5-1 Popular inverter topologies in commercial EVs and academia.

additional voltage level with sacrifices of control complexity. Studies have shown benefit of 3L TNPC for propulsion system due to weight reduction of EMI filters [27, 138-140]. Recently, the B2B 2L has been implemented in some EVs. Although the switching positions are doubled, the current rating of each switching position is cut by half for the same output power, thereby reducing the volume for cables and busbars. Furthermore, the volume of dc-link capacitors can be minimized by implementing phase-shifting pulse width modulation (PWM) carriers [141-143].

For power devices and packaging, as shown in Fig. 5-2, SiC power devices in various package options are widely available on the market. For example, Tesla Model 3 and Cybertruck inverters employs paralleled discrete SiC devices in TO-247-like packages [17, 18]. In Rivian R1T or Ford Mach-E, customized and compact SiC modules are used [19, 20]. Recent research has explored embedded die PCB technology which has demonstrated remarkable power density improvements [38, 39]. Some advanced inverters have employed high-density GaN devices which promise high-density and high-efficiency [64-67]. Typically, the gate driver design is closely tied to the employed power devices, requiring appropriate power supplies, driving components, and protection functions such as overcurrent and crosstalk protection. To minimize the driving loop parasitic, the gate driver board is placed near the power devices. Since most driving components have smaller size than power devices, the board dimensions are usually designed to be smaller or to match the footprint area of power devices.

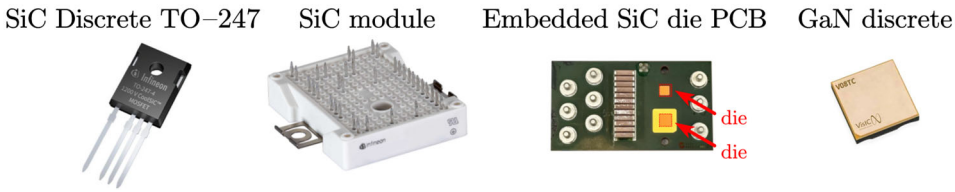


Fig. 5-2 Power device options with various package options that are available on the market.

Fig. 5-3 Capacitor candidate types for high-power traction inverters.

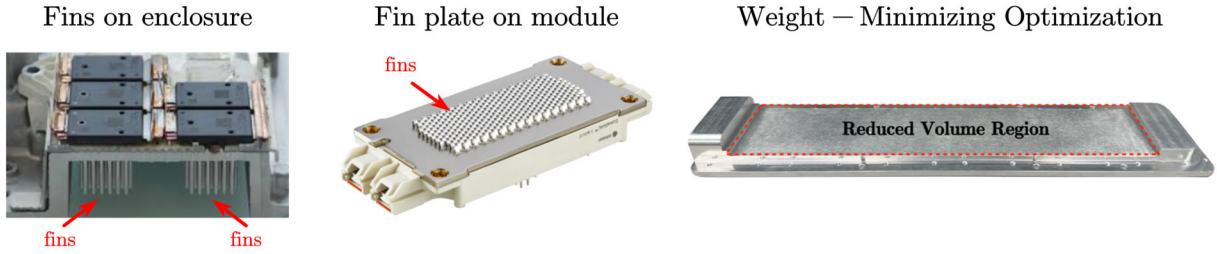


Fig. 5-4 The MLC cold plates or cooling fins are often integrated with the inverter enclosure or device backplate.

For the dc-link capacitor, as presented in Fig. 5-3, several candidates in different package options are available for high-power inverters. The film capacitors remain the most common choice in commercial EVs due to cost and safety considerations [144]. Package options include standard cubic and low-profile types. Advanced alternatives, such as lead lanthanum zirconium titanate (PLZT) CeraLink [145] or high-temperature ThermoLink capacitors [146], offer high energy density and current carrying capacity, suitable for high-temperature applications despite higher cost.

To fulfill the cooling needs of SiC/GaN devices, the MLC is a mature, efficient, and low-cost solution, capable of handling heat flux from 100 to 1000 W/cm^2 [1, 147-151]. By fabricating micro-level cooling fins, the heat transfer area and cooling efficiency are significantly increased. Furthermore, a weight-minimizing optimization for MLC proposed in [152] help reduce the weight and volume of the MLC. In commercial EVs, as illustrated in Fig. 5-4, the MLC cold plates or cooling fins are often integrated into the inverter enclosure or the power module back plates. In this cross-functional integration, the enclosure serves not only housing for inverter but also a cooling device for power devices, realizing high density integration.

Lastly, the current sensors that measure the currents for feedback and protection occupy certain spaces within traction inverters. Advanced sensing technologies aim to improve performance while minimizing size, including PCB-embedded Rogowski coils for protection and ac current reconstructions [43, 153, 154], anisotropic magnetoresistance (AMR) sensor for surge current

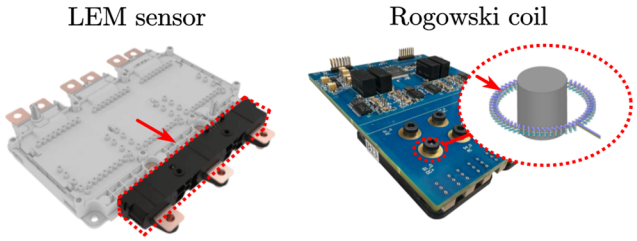


Fig. 5-5 Current sensor technologies that are being used in high-power inverters.

detection [155], parasitic-based sensors with adaptive compensation [95], and low-cost *di/dt*-RC sensing method for paralleled SiC devices [156, 157]. These innovative sensing methods help reduce inverter weight, volume, and cost.

Across these five component areas, extensive research has been conducted to improve efficiency and compactness. Moreover, systematic trade-off analyses and component-level optimizations have also been performed in[27, 64] to identify optimal design points. However, achieving DOE's target of 100 kW/L remains an unsolved challenge. This chapter builds upon the reviewed advancements and proposes a systematic integration strategy, aiming to provide design guidelines toward high-density inverter design.

5.2. Proposed Systematic Integration Strategy

Reviewing the inverter designs of commercial EVs in Table 1-1 and those in literature in Fig. 1-5, they share a common architecture: a "sandwich" multi-board structure, where PCBs and components are vertically stacked. From the power density perspective, this "sandwich" design approach presents several drawbacks described as follows:

- Numerous mechanical parts: Connectors, busbars, and mechanical parts are needed to bridge multiple PCBs, busbars, and components. And enclosures with internal metal plates are needed for mechanical support, increasing complexity.
- Thermal limitations: Multi-boards structure inevitably creates stagnating air space, resulting in localized hot spots and deteriorating thermal performance. Mitigating this issue requires additional cooling devices or layers of thermal interface material (TIM) on internal plates for heat dissipation.
- Insulation challenges: The insulation design can be challenging and complicated due to

multiple interfaces and close spacing of boards.

- EMI susceptibility: The cables, jumping wires, and connectors between controller and driving stages are prone to picking up noise, resulting in EMI issues.
- Module dependency: Reliance on customized power modules not only raises supply chain risk, but also forces the dimensions of the remaining PCBs to follow the module footprint.
- Manufacturing difficulties: The sandwich structure complicates the assembling process, impedes robotic manufacturing, hinders maintenance, and requires more time and effort to build each unit.

Given these drawbacks, it is obvious that the conventional sandwich structure presents inherent barriers to achieving higher power density. Therefore, alternative integration strategies must be explored for the next generation of high-density traction inverters.

To overcome these drawbacks, this dissertation proposes a "single-board" systematic integration strategy, which fundamentally restructure the inverter layout and packaging. The proposed strategy can be described as follows:

- Single-board structure: Eliminating multiple stacked PCBs reduces connectors, busbars, and internal plates, thereby simplifying assembly for robotic manufacturing and removing potential hot spots.
- Low-profile components: It help minimize the heigh difference between different components and maximize the horizontal utilization, improving thermal heat spreading
- Discrete devices in universal packages: Using paralleled discrete devices in standardized packages avoids reliance on customized modules, reducing supply chain risk while maintaining flexibility in scaling power ratings.
- Modular circuit design: Partitioning the board into functional sub-modules helps simplify the process when scaling power ratings, especially when using paralleled discrete devices.
- Cross-functional integrations: Embedding busbars, power devices, gate drivers, sensors, control stage into a single PCB unit, and integrating cold plates into enclosure which enable double-side cooling for PCB.

To demonstrate the proposed "single-board" integration strategy, an all-in-one HB PCB is designed, using discrete devices in TO-247 package for demonstration.

5.3. Demonstrated All-in-One Half-Bridge (HB)

Fig. 5-6 shows the designed all-in-one HB PCB with its circuit diagram and internal board structure. The specifications of this design are summarized in Table 5-1. By following the proposed "single-board" integration strategy, the designed all-in-one HB PCB achieves a power density of 101.7 kW/L which incorporates the following components:

- dc and ac busbars (integrated within PCB)
- power devices at both HS and LS switching positions
- dc-link capacitors C_{DC}
- all gate driving components and power supplies
- ac current sensor
- MLC cold plate (integrated within enclosure body which is not shown in Fig. 5-6)
- space for controller stage

The calculated power density becomes 123 kW/L if the areas for mounting holes on both sides are removed from the calculation since those areas are only for alignment purposes without internal layout structure in the PCB.

In this single-board structure, all busbars are integrated into the PCB, eliminating the need of additional interconnectors, cables, and stagnating air space typically found between boards. The all-in-one HB PCB can be directly connected to external voltage source V_{DC} or load inductor L_{load} through exposed copper terminals (DC+, DC-, and AC). Assembling process is further simplified since only a few screws are required to mount the board onto the enclosure, making it suitable for robotic manufacturing. By employing low-profile components, the design maximizes horizontal utilization, allowing more uniform heat spreading and more efficient thermal transfer, as thermal resistances are inversely proportional to footprint area. Also, this structure minimizes the unused air space which is typically generated by vertical height difference between standard package components. Both high-power and low-power stages in Fig. 5-6(a) are integrated into a single PCB. The internal PCB structure uses 1 oz copper for the outer layers (top and bottom) and 16 oz for the four inner high-current layers. Isolation barriers between high and low power stages are created by the PCB dielectric, isolated gate driver ICs, and isolated power supplies.

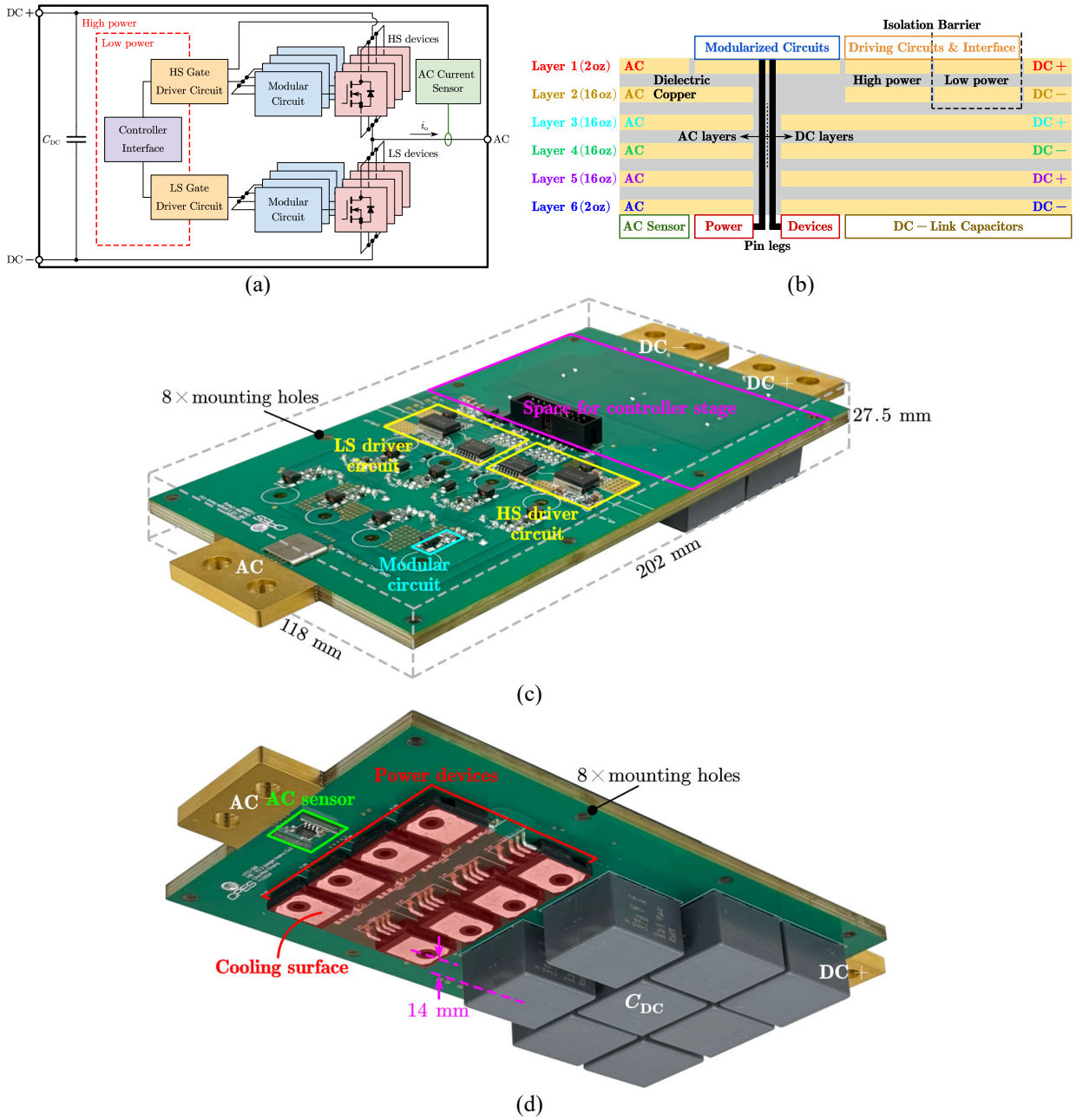


Fig. 5-6 Designed all-in-one HB PCB, achieving a power density of 101.7 kW/L by following the proposed single-board integration strategy (a) PCB circuit diagram, (b) internal layer structure, (c) top view of the HB PCB, and (d) bottom view of the HB PCB.

TABLE 5-1 SPECIFICATIONS OF THE ALL-IN-ONE HB PCB

Parameters	Values
Power rating (P_o)	67 kW
dc-link voltage (V_{DC})	800 V
dc-link capacitance (C_{DC})	48 μF
rated ac output current (i_o)	250 Arms
ac peak line frequency (f_{line})	1 kHz
Switching frequency (f_{sw})	20 kHz
Efficiency (η)	> 98.5 %

The discrete SiC MOSFETs in universal TO-247 packages adopted adopted due to their low unit cost and high design flexibility. More importantly, they significantly reduce the supply chain risk, as devices in the same package can be easily substituted with different candidates from different manufacturers. On contrary, customized power modules require redesign and new manufacturing processes which are time- and cost-consuming. By incorporating modular circuit design, the power rating can also be easily scaled to meet higher power requirements, reducing redesign time and effort. Considering the device characterization results in Fig. 2-5 and Fig. 2-6, four SiC MOSFET IMZA120R007M1H are paralleled in both HS and LS positions. The devices in the same switching position are driven by a single gate driver IC which is powered by low-profile dual-voltage power supply. The power devices are soldered on the bottom side of the PCB and the pin legs are bent 90 degrees, making cooling surface of the devices facing downward for MLC cold plate mounting. To ensure balanced current sharing among paralleled discrete devices, the proposed DB layout and DMC gate driver are implemented in the all-in-one HB PCB.

From the cross-functional integration perspective, the MLC cold plate is integrated into the enclosure body, using the space created by height difference between power devices and C_{DC} (around 14 mm) to maximize volume utilization. Moreover, the flat PCB structure enables it to be be double-side cooled by bottom cold plate and top enclosure, alleviating thermal challenges yielded by high power density. Thin layers of gap-filler TIM can be used to provide conductive heat transfer paths. For ac current measurement, a Hall-effect sensor is used to measure the output current i_o with line frequency f_{line}, and its auxiliary and isolation circuits are integrated into the HS gate driver IC. A U-shield is adopted to enhance sensing performance. The detailed circuit design will be presented in later Section 5.3.2.

The prototype of a 200 kW three-phase 2L inverter is shown in Fig. 5-7, consisting of three all-in-one HB PCBs, the enclosure, and a control board for demonstration. The detailed assembling process is illustrated in Fig. 5-8. The all-in-one HB PCBs are arranged side by side in horizontal direction, forming a flat, compact, and high-density inverter unit. Three MLC cold plates are integrated into the enclosure body to cool power devices, and their cooling path is arranged in a series configuration. The dimensions of the enclosure are slightly larger than PCB themselves to accommodate the MLC cold plates. By applying gap-filler TIM on both top and bottom surfaces of the PCB, the heat can be removed efficiently through the MLC cold plates and the enclosure

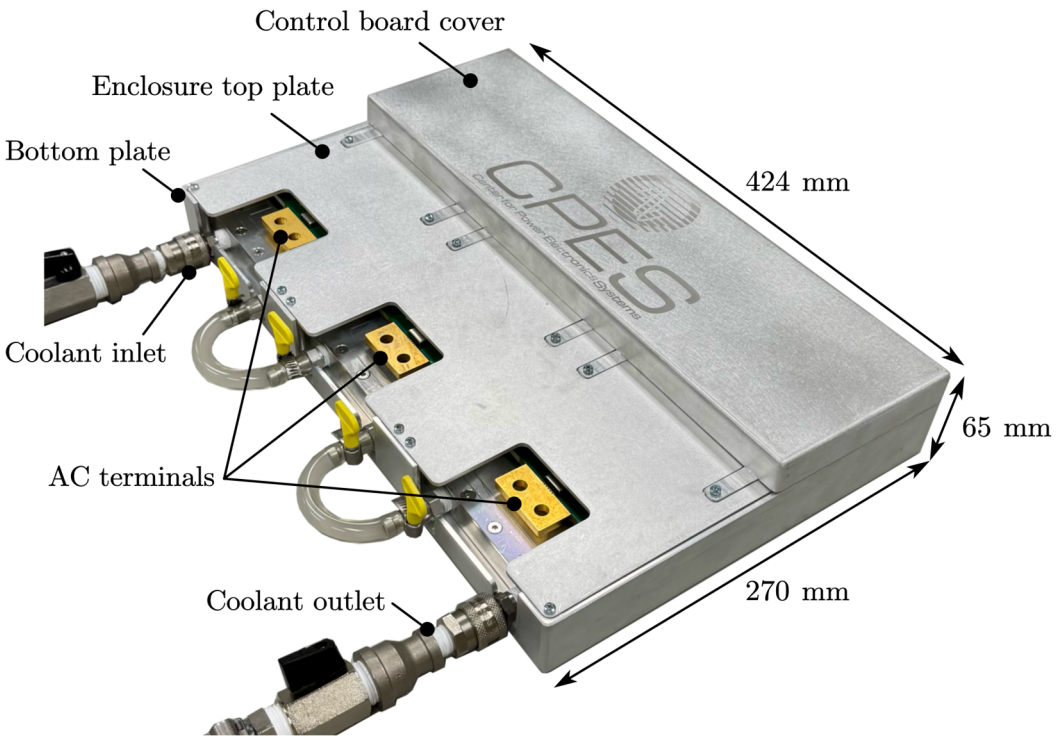


Fig. 5-7 Demonstration of a high-density 200 kW 3-phase inverter assembly consists of three all-in-one HB PCBs in a partial-opened enclosure.

top plate. The thickness of the gap-filler TIM is around 5.5 mm which is 10 % thicker than the actual gap, and its thermal resistance is minimized by applying pressure using screws.

A three-phase control board is mounted on top of the HB PCBs, specifically in the area without any components. While designed separately for testing purposes, the control board can be later integrated into the HB-PCBs by placing components at the empty top surface area above dc-link capacitors. Additionally, its placement on quiet DC potentials helps minimize the influence of EMI. Apparently, the demonstrated single-board all-in-one HB PCB discards the needs of additional busbars and connectors, thereby reducing weight, improving power density, simplifying assembling process, and facilitating robotic manufacturing. Only a few screws are required to mount the PCBs onto the enclosure which substantially saves assembly time and effort. The designed all-in-one HB PCB validates the proposed single-board integration strategy, highlighting a promising direction toward next-generation inverter design. The following sections present the detailed optimization and circuit design of the all-in-one HB PCB.

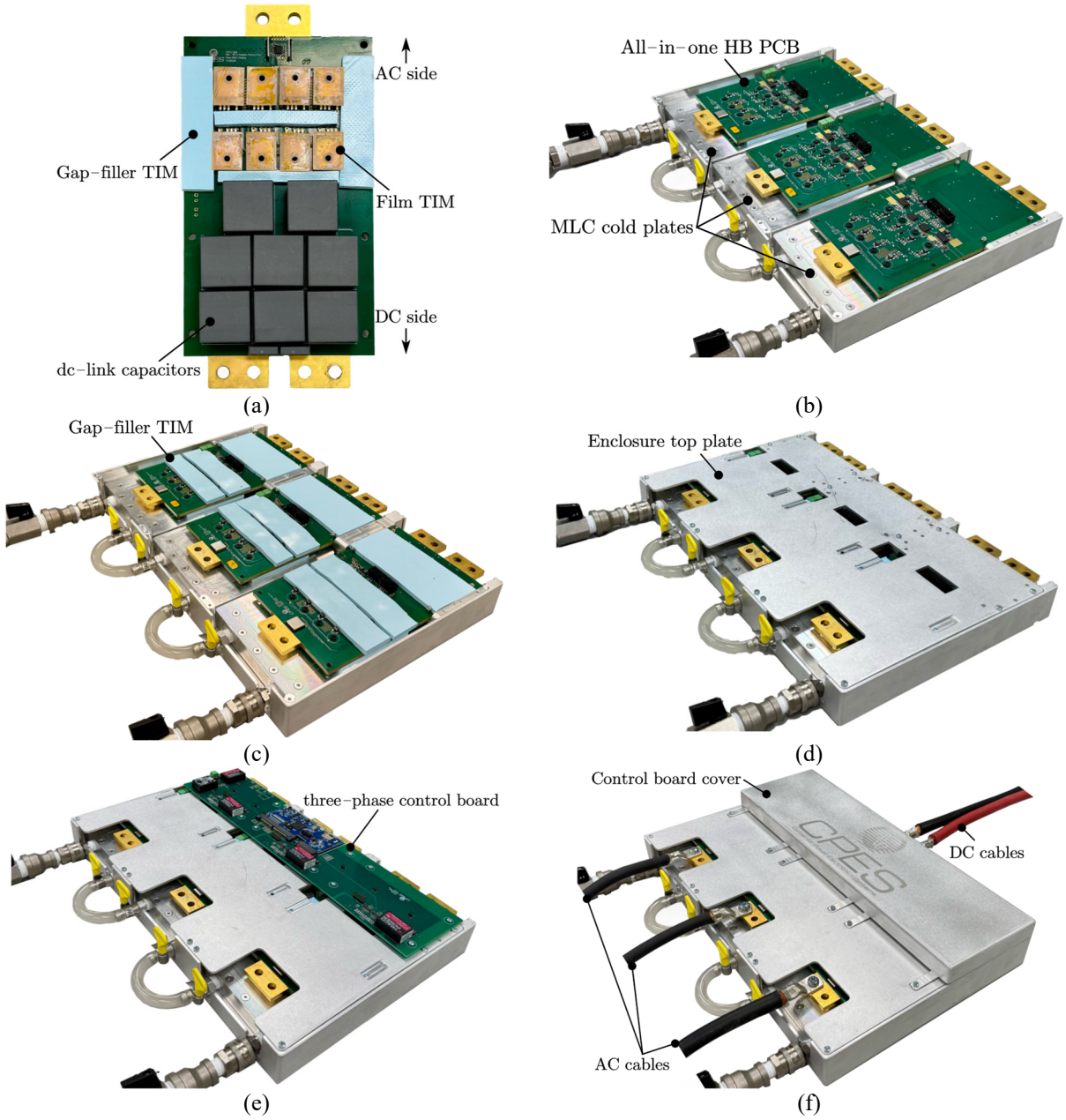
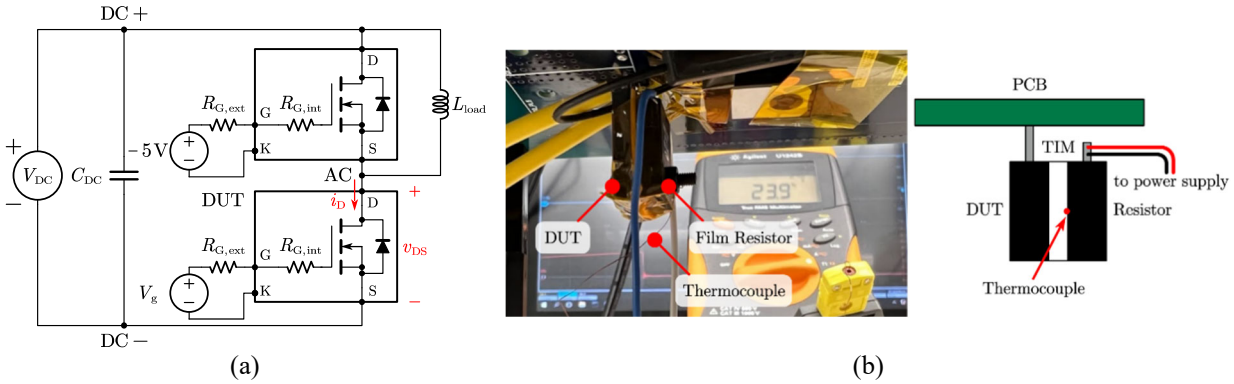


Fig. 5-8 Detailed assembly process of the demonstrated 200 kW three-phase inverter (a) all-in-one HB PCB with gap-filler TIM for PCB and film TIM for power devices, (b) mount PCBs onto MLC cold plates, (c) apply gap-filler TIM on top surface of PCB, (d) close and apply pressure from enclosure top plate, (e) connect 3-phase control board, and (f) install cables and cover.

5.3.1 Power Stage Optimizations: System Efficiency and Capacitor Volume

To optimize the system efficiency η and select appropriate number of paralleled devices N_{device}, the device candidates in Fig. 2-3 are characterized by a DPT setup shown in Fig. 5-9. The switching



(a) (b)

Fig. 5-9 The DPT test for switching energy characterization at different T_c (a) circuit diagram and (b) test setup.

energies of the DUT is measured under different V_{DC}, i_D, $R_{G,ext}$, and case temperatures T_c, and a same device is soldered at HS position acting as freewheeling diode. As presented in Fig. 5-9(b), a film resistor is attached to DUT's back plate to control T_c of the DUT. Fig. 5-10 depicts the total switching energy E_{total} (sum of turn-on energy E_{on} and turn-off energy E_{off}) under different conditions, where equivalent $R_{G,eq}$ is the sum of $R_{G,ext}$ and $R_{G,int}$ of DUT. Among candidates, the Infineon and Onsemi devices exhibit the largest and smallest E_{total}, respectively.

The results of E_{total} in Fig. 5-10 and characterized $R_{DS,on}$ in Fig. 2-6 are later imported into circuit-level simulations in Simulink to calculate system η by sweeping switching frequency f_{sw} and N_{device}. By incorporating the results of estimated η and device consistency in Fig. 2-5, the Infineon SiC MOSFET IMZA120R007M1H is selected as power devices, reaching a peak η = 99.55 % when operating at N_{device} = 4 at f_{sw} = 20 kHz. To ensure balanced current sharing, the DB layout passive solution is implemented in all-in-one HB PCB. Since the power layout has been presented in Fig. 3-15, it is not shown again in this section.

A volume optimization for dc-link capacitor is conducted and presented in this section. The design for dc-link capacitor is mainly driven by two parameters, peak-to-peak voltage ripple $\Delta V_{r,pk\text{-}pk}$ and capacitor current stress $I_{C,rms}$. The $\Delta V_{r,pk\text{-}pk}$ is caused by the discontinuous current from V_{DC}. For a 3-phase 2L inverter, the relationship between $\Delta V_{r,pk\text{-}pk}$ and required capacitance C_{DC} can be found in [158, 159], and the $I_{C,rms}$ induced by switching of power devices can be derived from [160], thus, the related equations are not shown to obscure the main focus. In conclusion, the capacitance C_{DC} should be large enough to suppress $\Delta V_{r,pk\text{-}pk}$, and number of capacitors N_{cap} should be sufficient to carry $I_{C,rms}$. Fig. 5-11 depicts the minimum required number of capacitors $N_{cap,min}$ over f_{sw} according to $\Delta V_{r,pk\text{-}pk}$ and $I_{C,rms}$ requirements using different capacitor candidates.

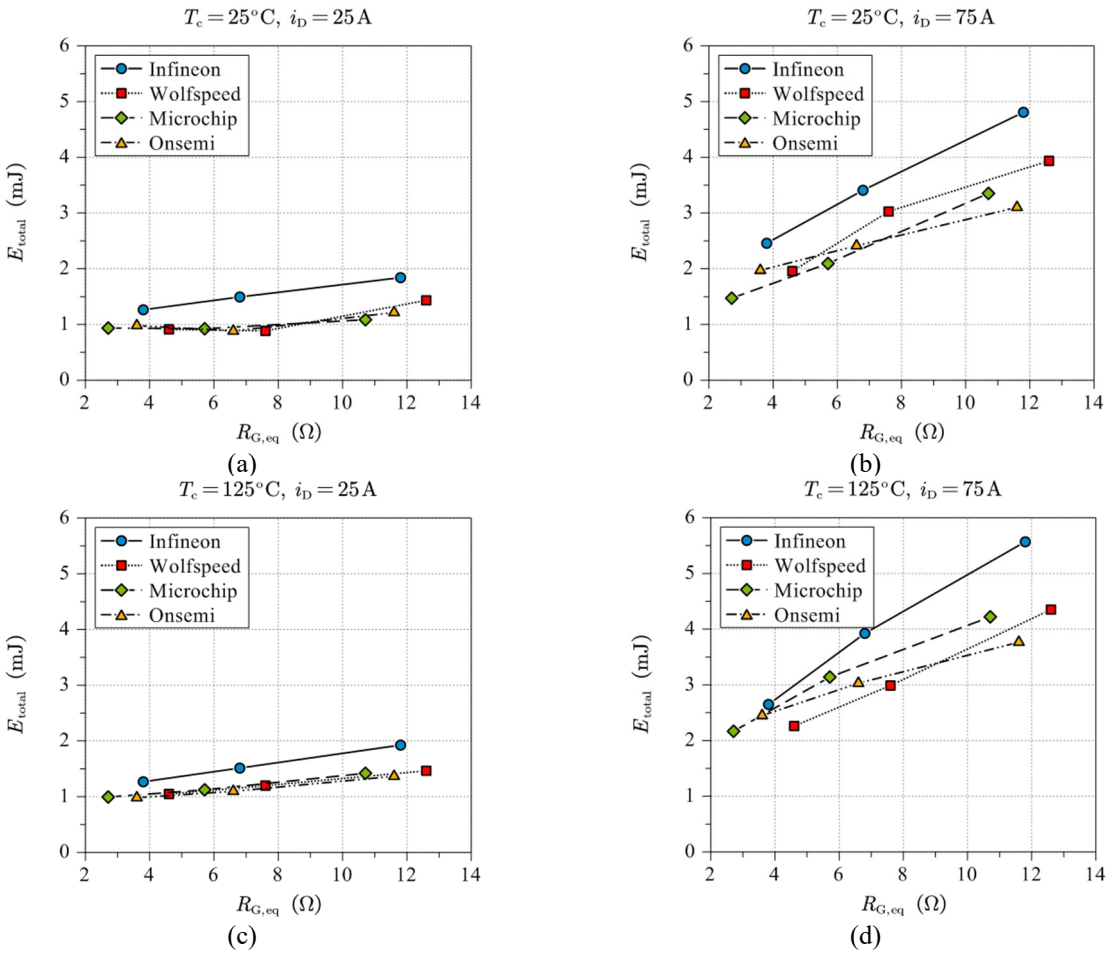


Fig. 5-10 The E_{total} comparison of (a) Infineon IMZA120R007M1H, (b) Wolfspeed C3M0016120K, (c) Microchip MSC017SMA120B4, and (d) Onsemi NTH4L020N120SC1.

In Fig. 5-11(a), for the film capacitors which generally have higher capacitance but lower rated current of each capacitor unit, while N_{cap} for $\Delta V_{r,pk\text{-}pk}$ decreases due to reduced required C_{DC} at higher f_{sw}, the $N_{cap,min}$ is mainly driven by $I_{C,rms}$ requirement. On the other hand, for the CeraLink in Fig. 5-11(b), the $N_{cap,min}$ is constrained by $\Delta V_{r,pk\text{-}pk}$ requirement, as ceramic capacitors have higher rated current but lower capacitance per unit. To optimize the volume of capacitors and increase power density, a volume optimization flow chart for capacitor selection is proposed.

Fig. 5-12 presents the proposed flow chart with considerations of thermal and derating factors of voltage δ_V and current δ_I. The required C_{DC} for $\Delta V_{r,pk\text{-}pk}$ and $I_{C,rms}$ requirements are first calculated according to [158-160], and the ambient temperature T_{amb} is also identified. When a capacitor candidate is selected, both δ_V and δ_I can be acquired from its datasheet. The capacitor's actual

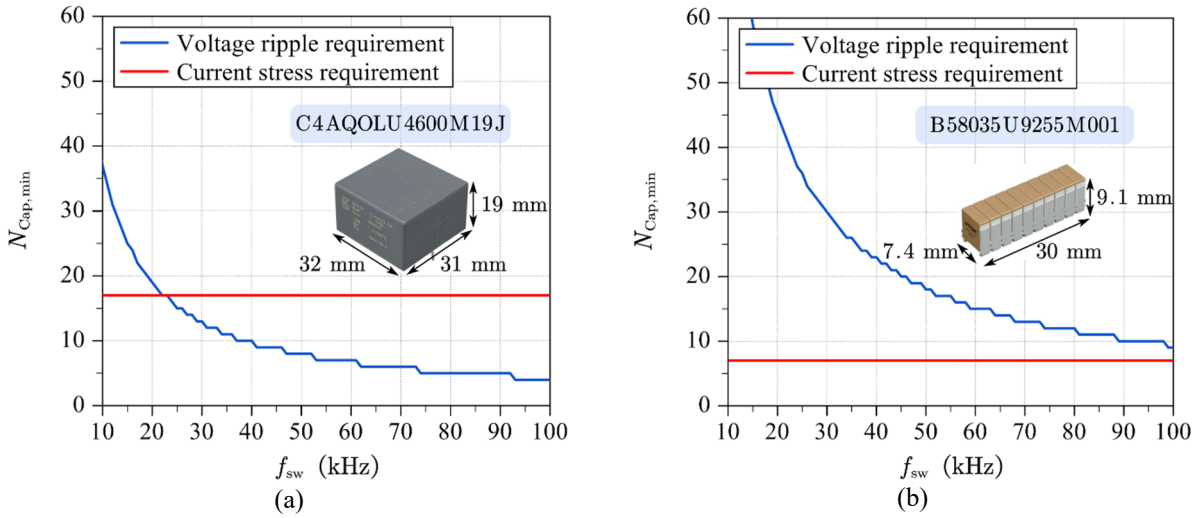


Fig. 5-11 The required $N_{Cap,min}$ for achieving both voltage ripple and current stress requirements by using (a) film capacitor and (b) ceramic capacitor.

rated current $I_{rated,real}$ is determined as rated current at 70 ºC I_{rated} times δ_I:

$$I_{rated,real} = I_{rated} \cdot \delta_I \tag{5.1}$$

Once the $N_{cap,min}$ is derived by considering both $\Delta V_{r,pk\text{-}pk}$ and $I_{C,rms}$ requirements (based on $I_{rated,real}$), the temperature of capacitor T_{cap} can be calculated by using parasitic resistance ESR and thermal resistance $R_{th,cap}$ values in the datasheet. As the capacitor's rated voltage V_{rated} decreases as T_{cap} increases, the actual $V_{rated,real}$ in (5.2) is checked whether it is greater than operating voltage, which is 800 V in this case.

$$V_{rated,real} = V_{rated} \cdot \delta_V \tag{5.2}$$

For most capacitors, both δ_V and δ_I are smaller than 1 as T_{cap} elevated. To reduce T_{cap}, the $N_{cap,min}$ can be increased to reduce $I_{C,rms}$ in each capacitor. Finally, the volume of a specific capacitor candidate can be calculated and compared with that of other candidates. Fig. 5-13 shows the volume comparison by evaluated capacitor candidates from TDK, Vishay, Panasonic, and KEMET, selecting candidates with V_{rated} from 800 V to 1200 V. Only the candidates with $V_{rated,real}$ higher than 800 V are shown. For designed three-phase 2L inverter in Fig. 5-7, in total of 24 KEMET 800 V C4AQOLU4600M19J film capacitors are used for traction inverter (8 capacitors for each all-in-one HB PCB) due to its lowest total volume of 452.3 cm^3 in Fig. 5-13 among different candidates.

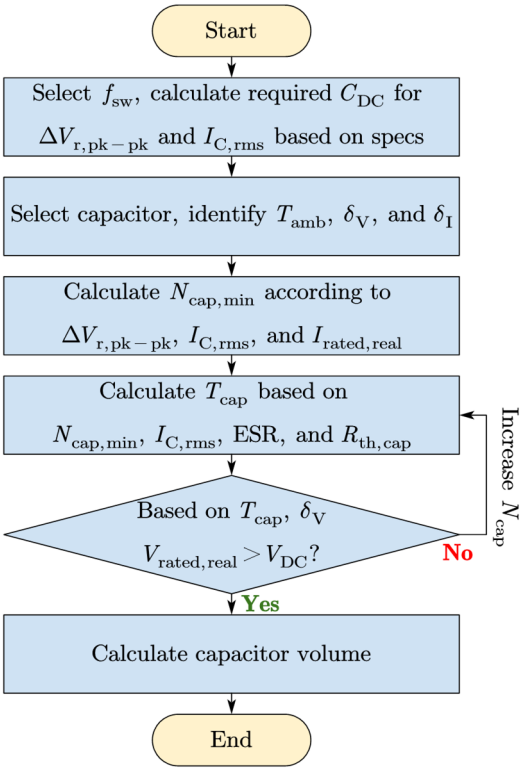


Fig. 5-12 Proposed volume optimization flow chart for C_{DC} selection.

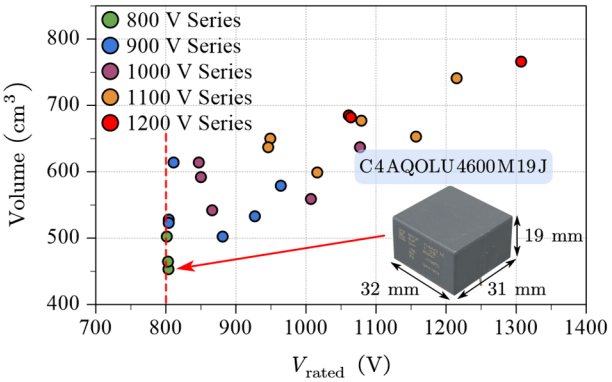


Fig. 5-13 Comparison of capacitor candidates from different capacitor series. Selected capacitor is KEMET C4AQOLU4600M19J in low-profile package.

5.3.2 Design of Gate Driving Stage

The power loop design adopts the proposed DB layout concept to improve both static and dynamic current sharing. To further improve dynamic current sharing, the DMC gate driver is integrated into the all-in-one HB PCB. Fig. 5-14 depicts the circuit design of gate driving stage, including modular circuit and protection functions. Four DMCs are connected to four paralleled devices for dynamic current balancing. Following the structure in Fig. 3-35, one side of the primary winding connects to the gate of each device, another side connects to the output of the gate driver IC, and the secondary windings of each DMC are connected in series.

The DMC is integrated into the modular circuit for each device. Fig. 5-15 shows the modular circuit of a specific device on top surface of the PCB, consisting of localized turn-on gate resistor $R_{G,on}$, turn-off gate resistor $R_{G,off}$, turn-off diode D_{off}, DMC, and AMC diode D_{AMC} for crosstalk protection. The modular design can be easily scaled for higher power applications when more devices are paralleled.

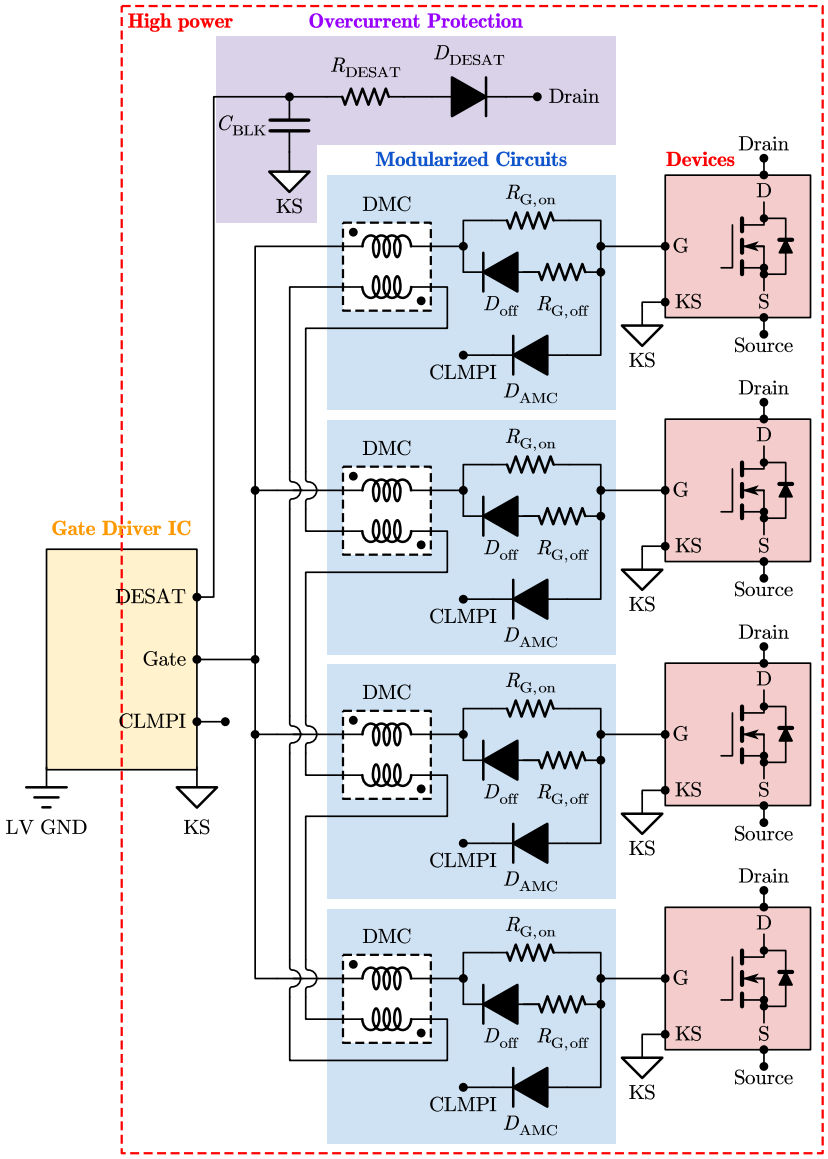


Fig. 5-14 Implemented DMC gate driver structure in all-in-one HB PCB.

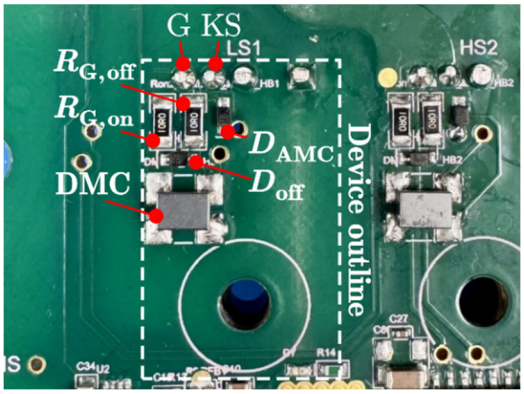


Fig. 5-15 Modular circuit for each individual device on all-in-one HB PCB.

As shown in Fig. 5-14, the overcurrent protection is achieved by DESAT function provided by gate driver integrated circuit (IC). The blanking time is determined by external blanking capacitor C_{BLK}, and the threshold of overcurrent protection is determined by R_{DESAT} and D_{DESAT} together [161]. In all-in-one HB PCB, the threshold is set as total current of 640 A, which is 160 A peak of each device.

On the other hand, the AMC diode D_{AMC} in Fig. 5-14, provides protection from crosstalk issue. During the turn-on or turn-off events of specific switching position, the high-*dv/dt* jumping node voltage generates a Miller current from drain to gate via C_{GD} of complementary position. This Miller current flows through the gate driving components and creates voltage offset on v_{GS} of complementary position, potentially leading to false turn-on and shoot through event [128]. In all-in-one HB PCB, the anode and cathode of D_{AMC} are connected to the gate of the device and the clamping CLMPI pin of gate driver IC, respectively. As shown in Fig. 5-15, the D_{AMC} is placed close to the gate of power devices, creating a low-impedance path for the crosstalk Miller current. Only one diode is needed for each device, featuring low-cost and easy to implement.

A Hall-effect low-profile current sensor MLX91216 is placed above the AC traces to sense the output current i_o, and its sensing and insulated circuit are integrated into the HS gate driver IC. The sensor converts i_o of (-600 A ~ 600 A) to an output signal v_{Hall} (0.5 V ~ 4.5 V). Traditionally, the v_{Hall} is directly connected to the controller circuit for signal processing. However, the output jumping node with high *dv/dt* can induce noise issue which may lead to fault triggering of the controller [155]. Therefore, as shown in the structure diagram in Fig. 5-16, the ac current sensor is tied to the output jumping node (AC which is also KS ground reference of HS), and the HS gate driver IC is used as isolation barrier for the current sensor. The AIN pin of gate driver IC converts the analog signal v_{Hall} to a 400 kHz APWM signal v_{APWM} with duty (88 % ~ 10 %) corresponding to the input v_{Hall} values. The v_{APWM} can be directly sent to controller for duty cycle calculation. By implemented the proposed sensing structure, the noise issue caused by high-*dv/dt* jumping node can be eliminated without the need of additional digital isolator and signal processing components.

The bandwidth of the sensing is determined by AIN-APWM pins of gate driver IC, which is 10 kHz, rather than 250 kHz of current sensor IC itself. Fig. 5-17 presents the open loop testing of the ac current sensing structure, injecting sinusoidal signal v_{Hall} with different f_{line}. In Fig. 5-17(a), by

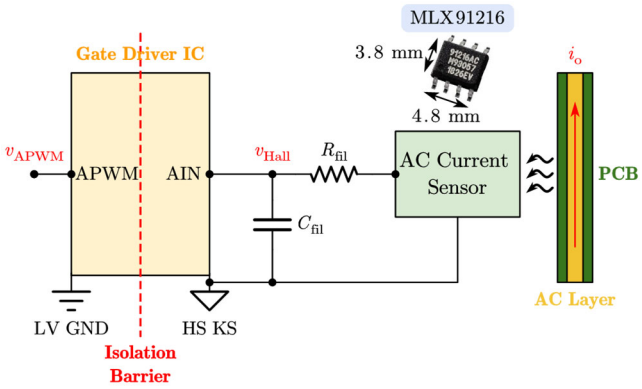


Fig. 5-16 Integration of ac current sensor and HS gate driver IC.

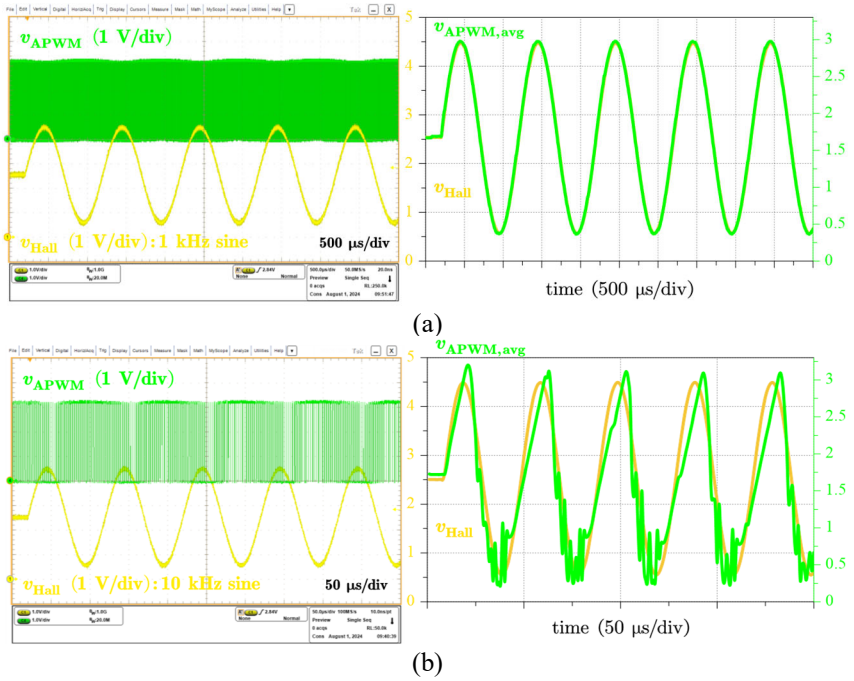


Fig. 5-17 Open loop testing when v_{Hall} has (a) f_{line} = 1 kHz (b) f_{line} = 10 kHz.

calculating the average values of v_{APWM} in every 400 kHz period, the $v_{APWM,avg}$ follows the v_{Hall} with f_{line} = 1 kHz perfectly. In contrast, when the f_{line} is increased to 10 kHz as seen in Fig. 5-17(b), distortion appears in $v_{APWM,avg}$ and affect sensing accuracy. Though current sensor is unable to measure high frequency current, it is sufficient to measure the i_o with f_{line} = 1 kHz in this application.

Lastly, the detailed layout design for the gate driving stage is presented Fig. 5-18, removing the power stage layout which have been previously shown in Fig. 3-15. All components in modular circuits, gate driving circuits, and low-voltage (LV) low power stage are soldered on the 1st layer. The low power stage only uses the 1st and 2nd layers for LV components their ground reference

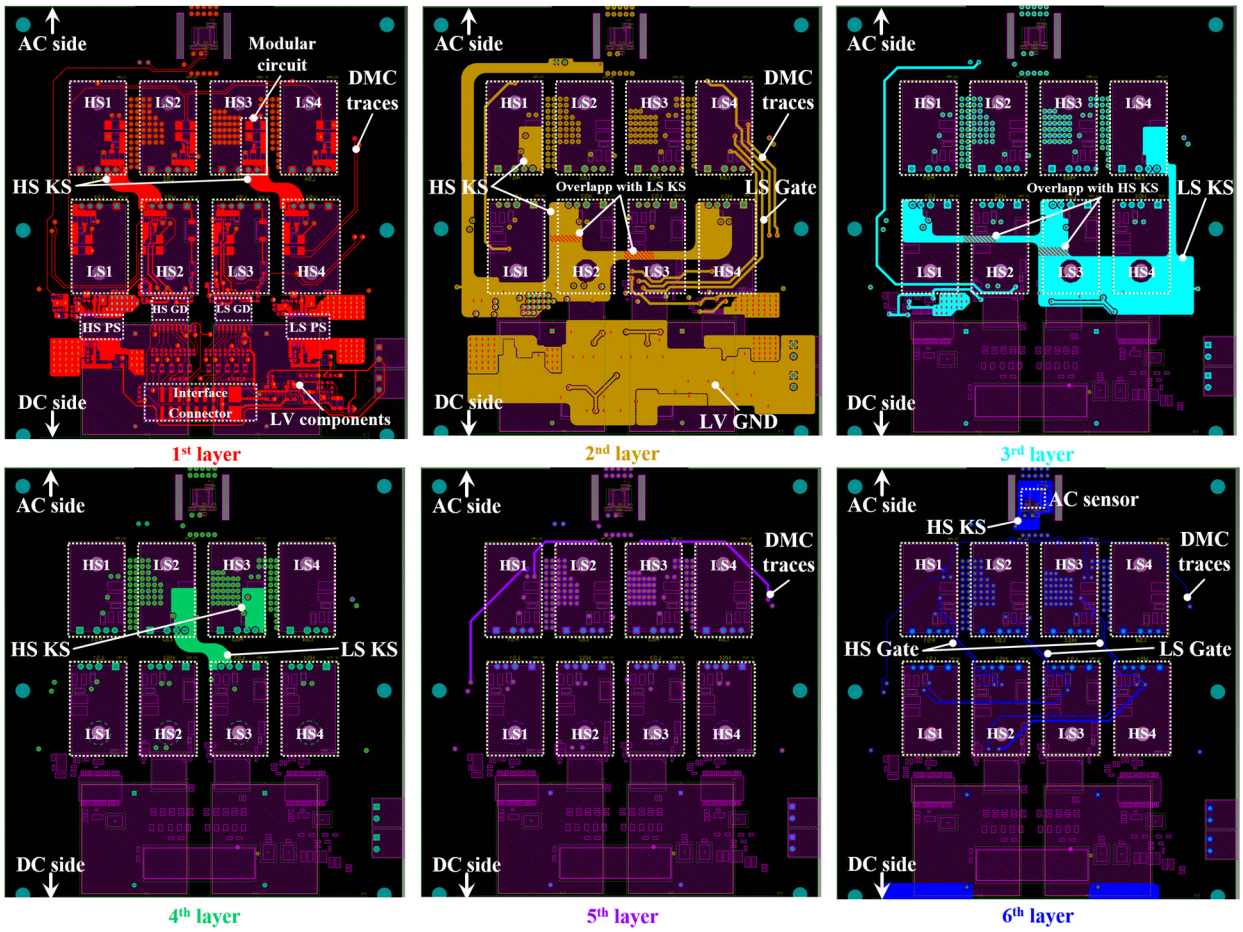


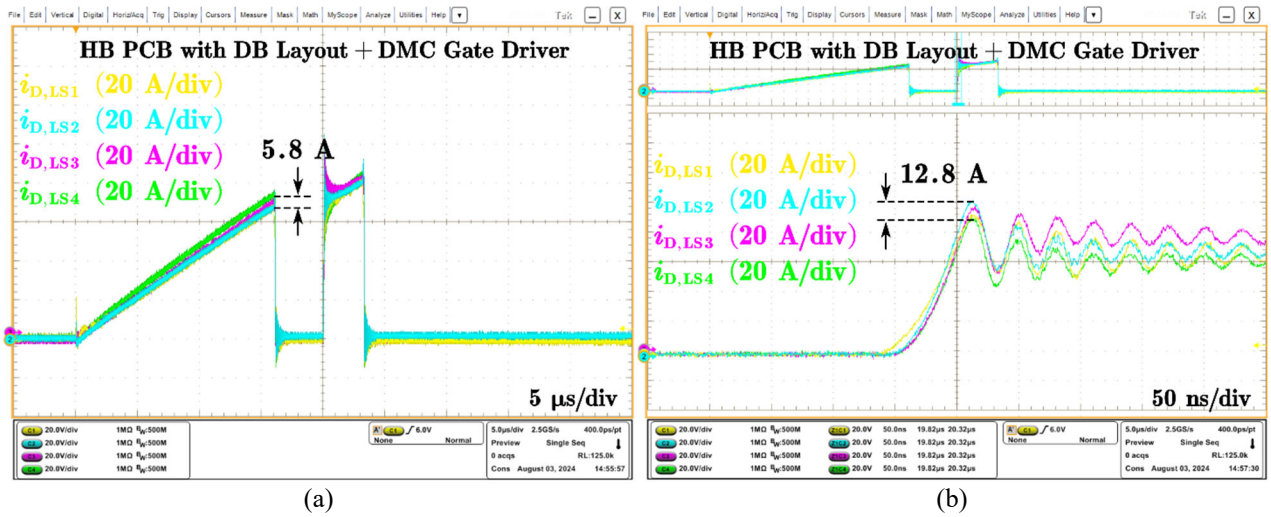
Fig. 5-18 Detailed layouts of high power gate driving stage and low power stage. The power loop layouts in Fig. 3-15 are removed in this figure.

(LV GND), corresponding to the layer structure in Fig. 5-6 (b). The isolation barrier between high power and low power stages is created by isolated gate drivers (GD), isolated power supplies (PS), and dielectric between the 2nd and 3rd layers. On the high power side, the KS of HS mainly uses the 2nd layer, while that of LS is in the 3rd layer. The shaded areas indicate the overlapping area between the HS KS and LS KS, and these areas are minimized to avoid noise issues since HS KS is tied to the high-*dv/dt* AC jumping node. The gate signal traces from gate driver IC (HS GD and LS GD) to paralleled devices are not necessary to made symmetric due to the negligible impact of mismatched gate impedances on dynamic current sharing of paralleled devices. These signal traces are covered by corresponding KS polygons, providing low impedance return paths. While the middle area of the PCB has been used for power layout (see Fig. 4-15), the DMCs of DMC gate driver are routed using periphery area surrounding power devices. The overlapping areas between DMC traces and AC jumping node are also minimized.

5.4. Experimental Verification of All-in-One HB PCB

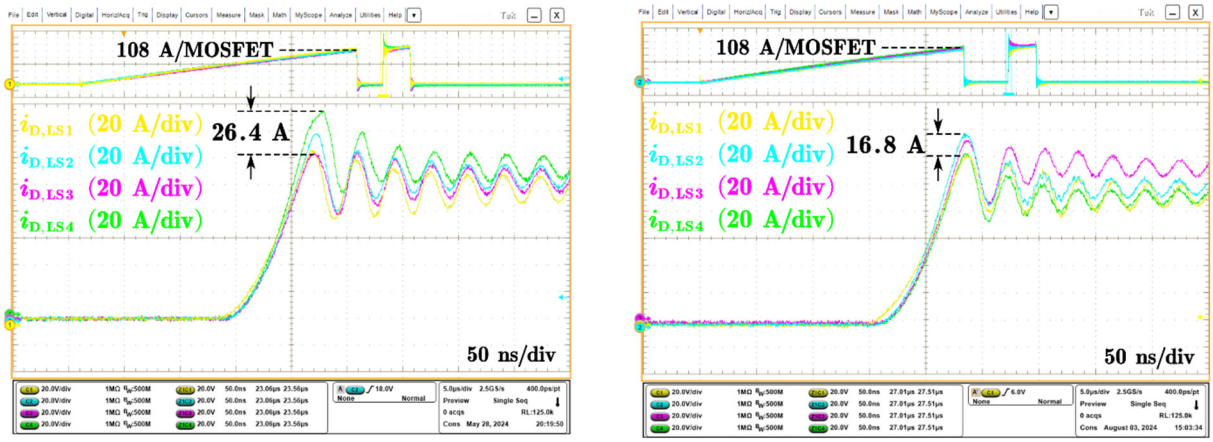
While the effectiveness of the DB layout have been previously validated in Fig. 3-18, Fig. 3-19, and Fig. 3-20, this section verify the effectiveness of DMC gate driver in all-in-one HB PCB. The DMCs are added to the all-in-one HB PCB to verify the dynamic current sharing. Fig. 5-19 shows the current sharing performances of all-in-one HB PCB after implementing DMC gate driver under testing conditions in Fig. 3-17. Comparing Fig. 5-19(a) to Fig. 3-18(b), since the DMC gate driver has no impact on static current sharing, the static $\Delta i_{D,pk}$ = 5.8 A remains almost the same with that $\Delta i_{D,pk}$ = 6 A using DB layout only. Fig. 5-19(b) further presents the zoom-in turn-on transient. Since the operating conditions and R_G are the same for all cases, the switching speeds in Fig. 5-19(b) are identical with those in Fig. 3-19. Comparing Fig. 5-19(b) to Fig. 3-19(b), the dynamic current sharing is further enhanced by DMC gate driver which reduces dynamic $\Delta i_{D,pk}$ from original 18.4 A to 12.8 A. When compared to the baseline design in Fig. 3-19(a), an 83 % reduction in dynamic $\Delta i_{D,pk}$ is achieved.

The experimental waveforms of overpower condition, which is total current of 430 A under V_{DC} = 800 V, are shown in Fig. 5-20, comparing $\Delta i_{D,pk}$ when using DB layout only or both DB layout and DMC gate driver. Apparently, the combining of both DB layout and DMC gate driver significantly improves dynamic current sharing. Fig. 5-21 summarizes the tested dynamic $\Delta i_{D,pk}$ across tests in Chapter 3 and this chapter under different total current conditions but the same



(a) (b)

Fig. 5-19 All-in-one HB PCB when implementing both DB layout and DMC gate driver (a) static current sharing (b) dynamic current sharing.



(a) (b)

Fig. 5-20 When operating at overpower condition, comparison of dynamic current sharing using HB PCB with (a) DB layout only and (b) both DB layout and DMC gate driver.

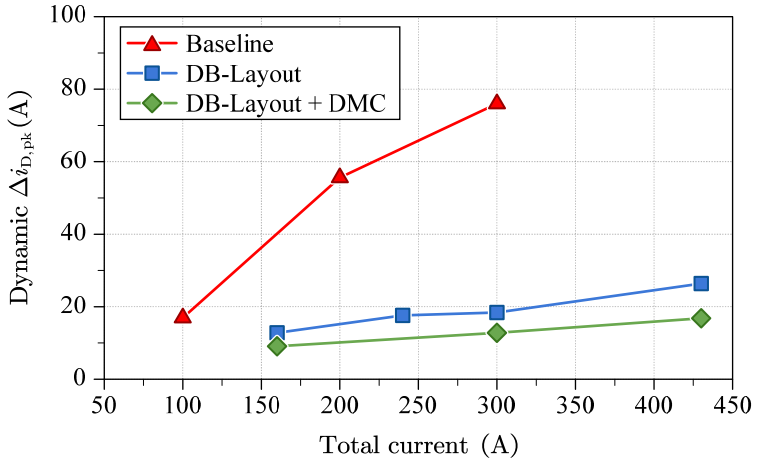
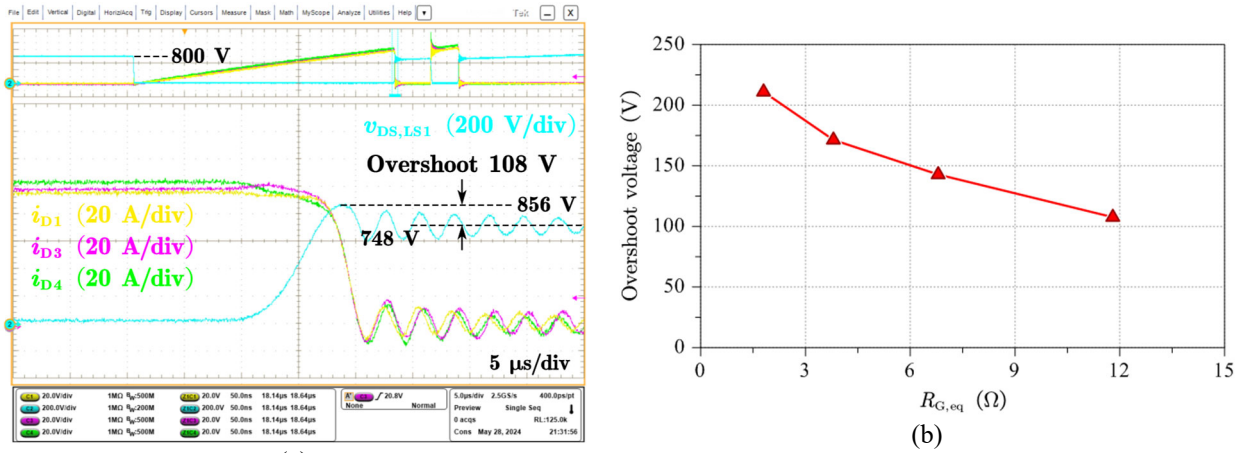


Fig. 5-21 Peak dynamic $\Delta i_{D,pk}$ under different total current conditions.

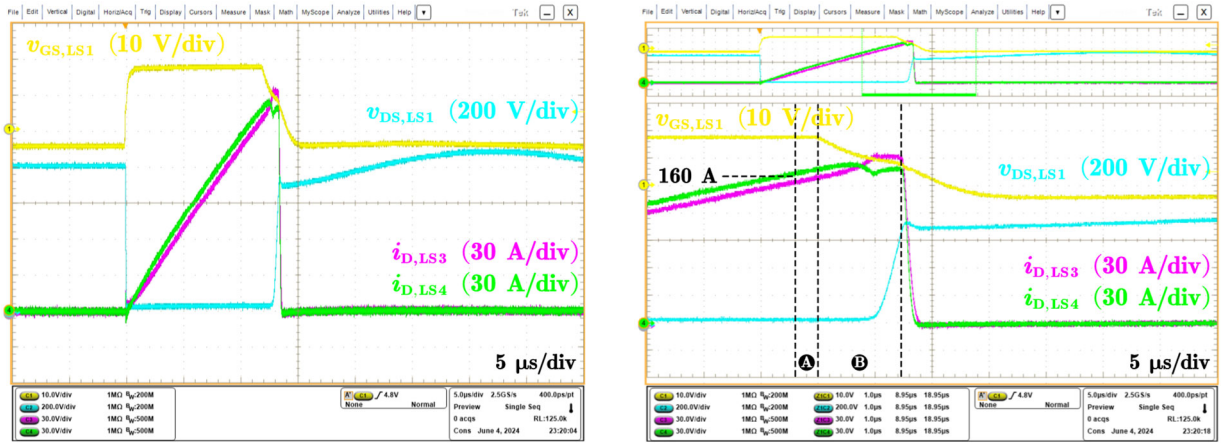
switching speed and power devices. The baseline layout design in Fig. 3-14 is tested to total current of only 300 A due to safety consideration, while the all-in-one HB PCB is tested up to overpower condition of 430 A without current sharing issue. The experimental results verify the effectiveness of proposed current-balancing solutions.

Fig. 5-22(a) shows the switching turn-off transient under the same conditions with Fig. 5-21, measuring an overshoot voltage of 108 V when peak *dv/dt* = 16 V/ns. The *dv/dt* is measured by the steepest slope of v_{DS}. Fig. 5-22(b) presents the overshoot voltage over $R_{G,eq}$ ($R_{G,ext} + R_{G,int}$). The peak overshoot voltage is around 209 V when $R_{G,ext}$ is close to 0 Ω with the peak *dv/dt* slightly above 51 V/ns.



(a) (b)

Fig. 5-22 The (a) turn-off switching transient of LS devices and (b) overshoot voltage with different $R_{G,eq}$.



(a) (b)

Fig. 5-23 Experimental result of DESAT overcurrent protection (a) overview and (b) zoom-in transient.

The DESAT overcurrent protection is tested in Fig. 5-23. As mentioned in Section 5.3.2, the threshold is set as total current of 640 A (160 A/device). In Fig. 5-23(a), the protection is triggered when all four devices reach 160 A, while only the currents of devices LS3 and LS4 are shown. Fig. 5-23(b) enlarges the soft-turn-off process. The v_{GS} starts decreasing after a blanking time around 420 ns in region A, and takes another 1.5 µs to completely turn off the devices in region B. The DESAT function protects the devices from being damaged by shoot-through event.

On the other hand, the effectiveness of AMC protection is presented in Fig. 5-24. In Fig. 5-24(a), it shows the experimental waveforms when Miller crosstalk occurs without D_{AMC}. When HS devices start conducting current $i_{D,HS}$, the v_{GS} of LS devices are affected by crosstalk Miller current, resulting in peak voltage of 3.4 V which is very close to the rated V_{th} of 4.2 V. After the D_{AMC} is added in Fig. 5-24(b), under the same testing conditions, the peak v_{GS} is greatly reduced from

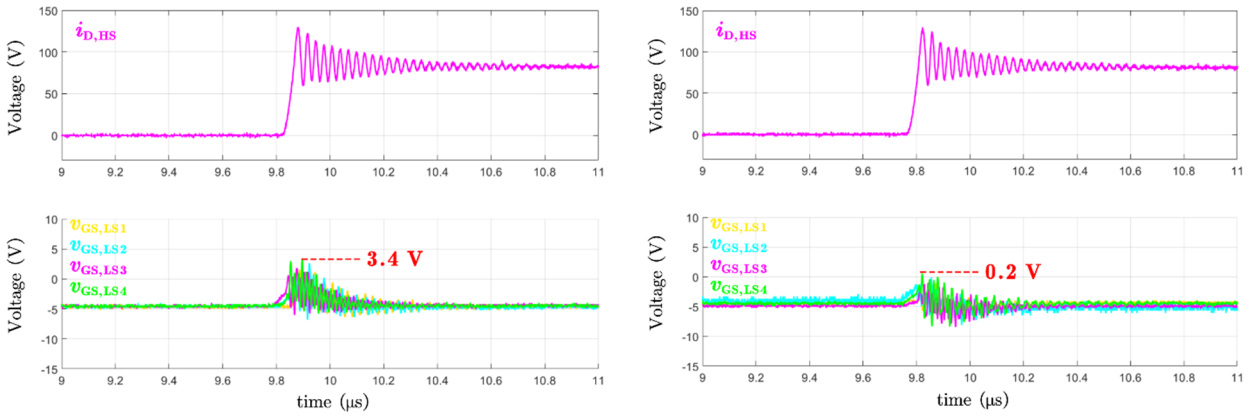
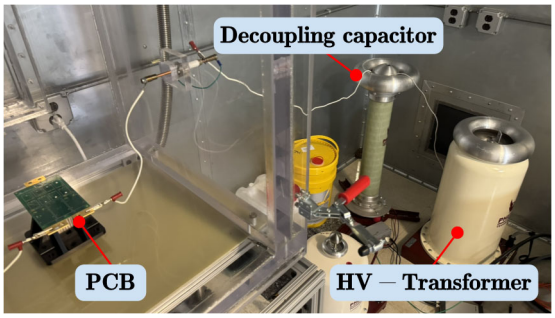


Fig. 5-24 Experimental results of crosstalk protection (a) without D_{AMC} and (b) with D_{AMC}.

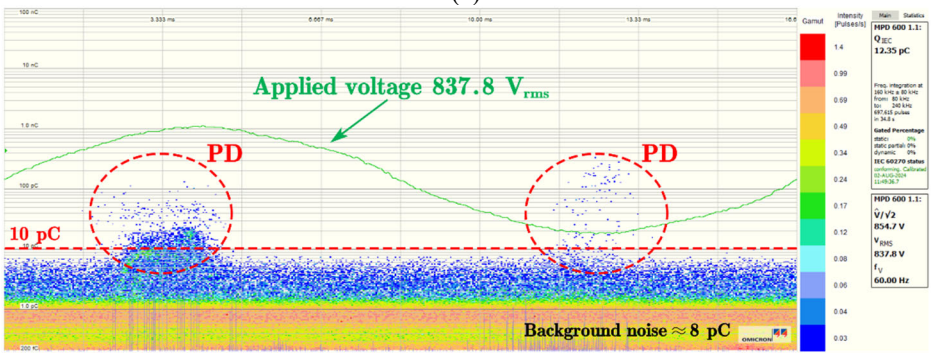
original 3.4 V to only 0.2 V, validating the AMC protection function. It should be noted that, due to the fixed current direction of D_{AMC}, it has no effect for turn-off crosstalk caused by the Miller current in opposite direction.

Because both high-power and low-power stages are integrated into all-in-one HB PCB, it is crucial to verify the insulation design. Two insulation tests, the partial discharge (PD) test and breakdown voltage high potential (Hipot) test, are performed. Fig. 5-25(a) presents the test setup for PD test where an unpopulated PCB is connected to HV-transformer and decoupling capacitor. By following standard IEC60270, the PD should be smaller than 10 pC to prevent insulation material being damaged in long-term operation. In Fig. 5-25(b), a background noise of 8 pC is observed when applied voltage = 0 Vrms. As the applied voltage increases to 837.8 Vrms (which is 1184.8 V), the PD occurs on the PCB. The PD inception voltage (PDIV) is 384.8 V higher than the nominal operating voltage of 800 V. Additionally, the breakdown voltage Hipot test is conducted as shown in Fig. 5-26. The PCB is connected to the HV output controlled by the controller. According to the standard IEC60950, the applied voltage should be two times the operating voltage plus an additional 1 kV, which is at least 2*800 V + 1 kV = 2.6 kV in this case. In Fig. 5-26, a voltage of 2.7 kV is applied to the PCB and the duration time is set to one minute. No breakdown is observed in the designed all-in-one HB PCB. Both PD and Hipot insulation tests validate the design of all-in-one HB PCB.

To verify the full-power operation of the designed 200 kW inverter, a test environment is built as shown in Fig. 5-27. The parameters of the full-power test are listed in Table 5-2. The test in

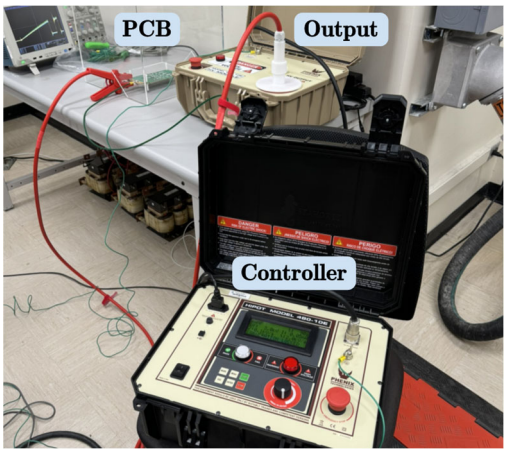


(a)



(b)

Fig. 5-25 For the partial discharge test (a) setup and (b) test result.



(a)

Fig. 5-26 The breakdown voltage Hipot test.

conducted with pure-inductive load, and an external capacitor bank is connected in between V_{DC} and PCBs' to provide neutral mid-point n. Fig. 5-27(c) shows the tested continuous full-power waveforms, operating at $V_{DC} = 800$ V, $i_o = 250$ Arms. The experimental results verify the feasibility of designed HB PCB for three-phase operation. The full-power thermal test will be presented in Chapter 6.

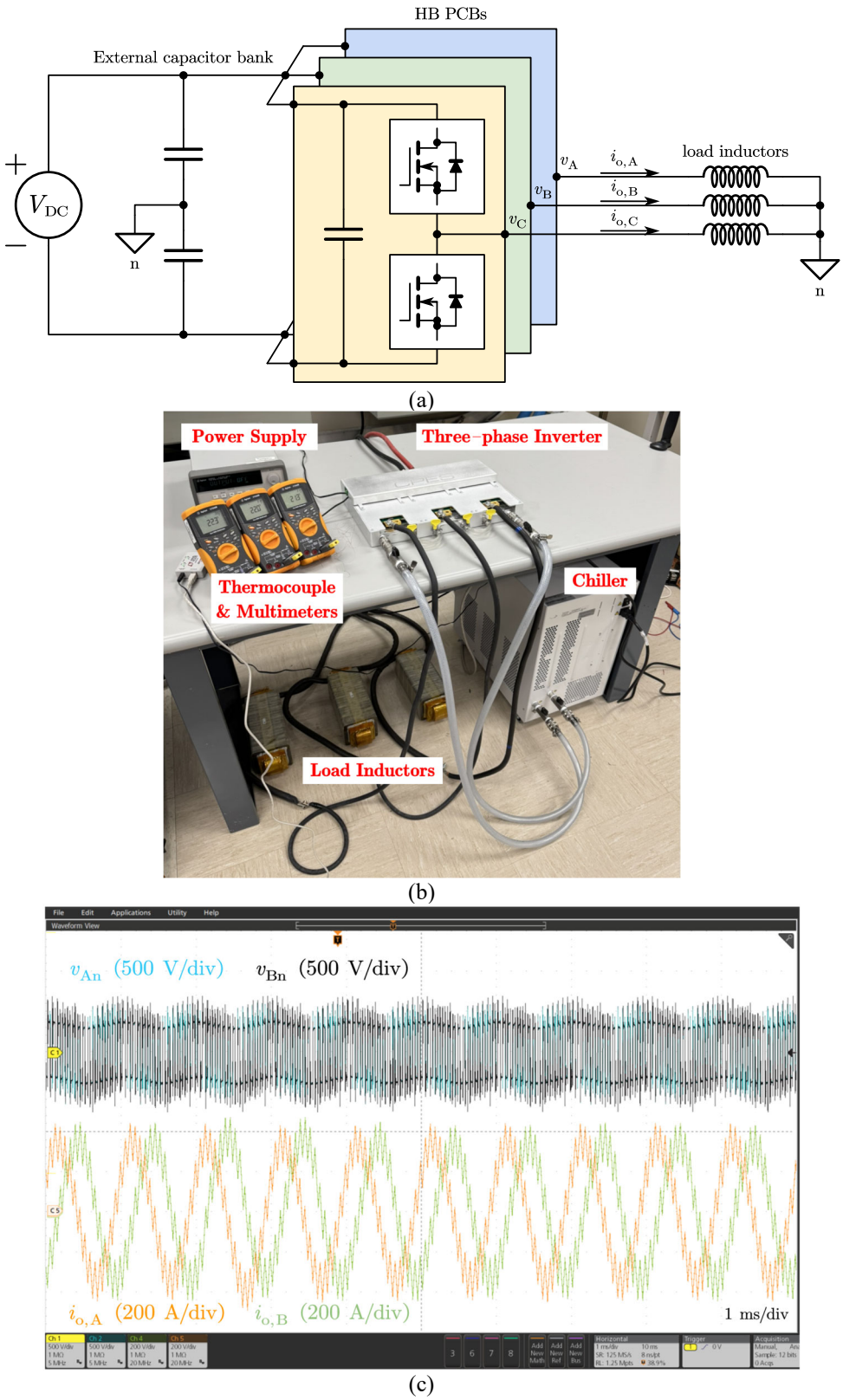


Fig. 5-27 Three-phase 800-V dc-ac continuous-power operation (a) circuit diagram, (b) test setup (c) full-power waveforms of i_o = 250 Arms.

TABLE 5-2 SPECIFICATIONS OF THE ALL-IN-ONE HB PCB

Parameters	Values
Output current (i_o)	250 Arms
dc-link voltage (V_{DC})	800 V
ac line frequency (f_{line})	1 kHz
Switching frequency (f_{sw})	20 kHz
Modulation index (M)	0.5

Lastly, the ac current measurement is validated using the setup in Fig. 5-27(a). As shown in Fig. 5-16, the gate driver IC converted the current information into a 400 kHz v_{APWM} signal for feedback control. Fig. 5-28(a) presents the experimental results when measuring the output current $i_{o,A}$ = 200 Arms with f_{line} = 1 kHz. The averaged $v_{APWM,avg}$ is illustrated in Fig. 5-28(b), overlapping with the actual current for comparison. Obviously, the $v_{APWM,avg}$ well corresponds to the actual current $i_{o,A}$, validating the concept of integrating ac current sensor with the gate driver IC.

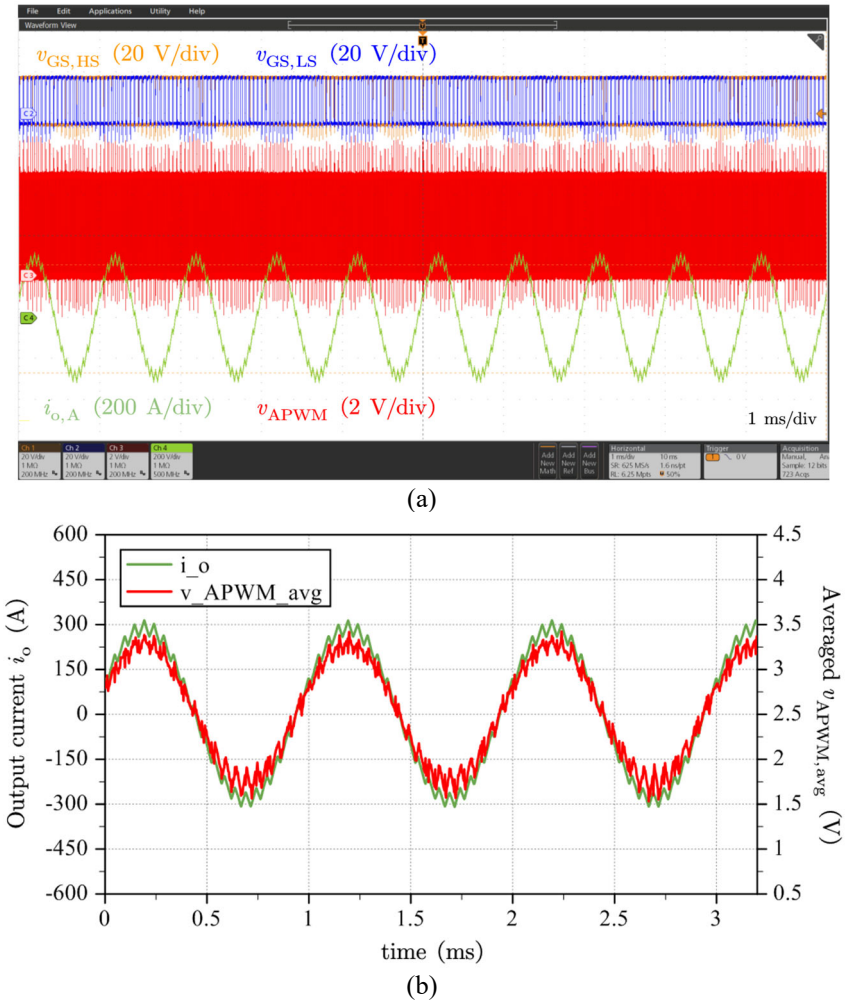


Fig. 5-28 Experimental results of ac Hall sensor (a) waveforms of 1 kHz output current i_o = 200 Arms and (b) converted $v_{PWM,avg}$.

5.5. Conclusion

The proposed “single-board” integration strategy is validated by the demonstrated all-in-one HB PCB, highlighting a promising direction toward next-generation inverter design. Moreover, by implementing the heavy copper PCB technology for single-board integration, the designed all-in-one HB PCB achieves a power density of 101.7 kW/L while ensuring balanced current sharing among paralleled devices and meeting insulation requirements. Furthermore, a three-phase 200 kW inverter assembly is built for full-power continuous operation, verifying the feasibility of all-in-one HB PCB for traction inverter applications.

Chapter 6
Systematic Methodology for Thermal Management

6.1. Introduction

As inverter volume shrinks to meet DOE's aggressive targets, the increasing heat flux necessitates efficient and integrated cooling solutions. Addressing thermal challenges is essential to fully realize the benefits of SiC-based traction inverters. After all, optimal electrical design can only be achieved when supported by strong thermal performance.

Cooling technologies have been developed to cool components within power inverters, especially for power devices since they typically incur high losses. Single-phase cooling using coolants of air or water mixtures are most popular methods. However, in traction or propulsion systems, the inverters are often housed in sealed enclosures for safety reasons, which makes it challenging for conventional air cooling to meet the cooling requirements [162, 163]. The cooling capability of conventional forced air cooling is usually lower than 50 W/cm^2 [164, 165], and is insufficient to meet cooling demand for high-power devices especially when the total loss exceeds 1500 W [166]. To address the cooling demand of higher power dissipation, MLC, which has a cooling capability higher than 100 W/cm^2, has become a widely adopted solution in power inverters due to its industry maturity, low weight, and low cost [1]. Researchers have conducted studies to optimize the thermal performance of MLC. [147, 150, 167-172]. The results indicate that the cooling capacity of MLC is significantly influenced by factors such as channel geometry, fluid characteristics, and coolant path configuration [152, 173-175].

The cooling capability can be further enhanced by using a coolant with higher thermal conductivity, such as a metal liquid coolant. This approach has been shown to reduce temperature-rise by 38 % [176]. Additionally, recent studies have demonstrated the benefits of reduced pump power consumption compared to water-based pump [177]. The combination of metal liquid

coolant and MLC has been demonstrated to achieve cooling capacities greater than 1000 W/cm^2 [148]. Another advanced single-phase cooling technique, jet impingement liquid cooling, can offer cooling capability ranging from 200 to 1000 W/cm^2 [178]. The cooling capacity of this method is largely impacted by nozzle design [167, 179-183]. Although jet impingement has been utilized in some applications [184-186], it is not commonly adopted in electric vehicles (EV) or high-altitude more electric aircraft (MEA) due to its higher pressure drop and complex structure [167]. The risk of coolant leakage between the device and cooling chamber also renders it unsuitable for high-altitude MEA applications.

Two-phase cooling technologies such as vapor chambers offer cooling capabilities beyond 1000 W/cm^2. The technique leverages the fluid phase change transition and exhibits higher heat transfer efficiency and excellent heat spreading performance, making it ideal for applications with limited space constraints [187-190]. The vapor chamber can also be utilized as a substitute for traditional copper baseplate of MLC to reduce thermal resistance and improve temperature distribution. A study [191] demonstrated that the maximum temperature can be reduced by 26 % and temperature distribution improved. Furthermore, an ultra-thin vapor chamber with a thickness of 0.4 mm has been found to possess thermal conductivity 30 times greater than that of a copper baseplate [192].

Recently, researchers have focused on eliminating the TIM layer by integrating the cooling device into the device package or housing [5, 193]. Studies [194, 195] have demonstrated that incorporating MLC into an AlN-layer in the direct bond copper (DBC) layer reduces thermal resistance by 80 %. This concept has also been utilized in some EVs for power devices [196]. The MLC has also been embedded in a printed circuit board (PCB) to cool chips [151]. A vapor chamber baseplate with a DBC substrate integrated into power modules was presented in [197], resulting in a 40 % improvement in total loop thermal resistance. Double-side cooling has been demonstrated for a 10 kV SiC MOSFET module [198, 199], achieving a cooling capability higher than 250 W/cm^2. A comprehensive comparison of single-side cooling for different PCB technologies for power dies embedded in a PCB was recently published in [38], and double-side cooling for embedded die PCBs was also shown to result in a 57 % reduction in junction-to-case thermal resistance compared to TO-247 devices [39].

Effective cooling of components beyond power devices is also a focus of research to mitigate

localized hotspots. A thermal model for PCB-winding based transformers is proposed and show accuracy [200]. In [47], an air cooling duct is designed to cool planar transformer windings. By optimizing the cooling airflow, the peak winding temperature is reduced by 8 % and the power consumption is four times smaller than that without airflow optimization. Similarly, [201] utilized forced-air cooling for the PCB-winding of transformers, reducing hotspot temperatures by 40 %. The combination of forced-air and phase change heat pipe has also been applied to cool transformer, as described in [202, 203]. A liquid cooling chamber was designed for 50 kW filters in high-altitude applications in [204]. This approach was also utilized to cool EMI filters, as shown in [205].

Although cooling has been done for individual components in high-density power electronics inverter, a systematic thermal design process is missing in the literature. This chapter addresses this gap by presenting a design methodology for thermal management, beginning with comprehensive thermal modeling and thermal analysis.

6.2. Thermal Modeling and Proposed Methodology

Before establishing methodology of thermal management, a proper thermal model should be built to understand heat transfer. In all cases, the heat source temperature T_{hs} in power inverters can be impacted by factors listed as follows:

- Heat source
- Heat transfer form
- Heat transfer path
- Ambient Environment or cooling condition

In a thermal system, the heat flux dissipated from a heat source will always seek a path to transfer to the lowest temperature. This temperature is usually determined by the ambient environment or cooling condition. Multiple paths may exist for heat dissipation, and each path may involve various forms of heat transfer, such as conduction between solids, convection between solid and fluid, and radiation between surfaces. The specific form and path of heat transfer vary depending on the situation. However, all cases can be described by using a thermal resistance R_{th} network.

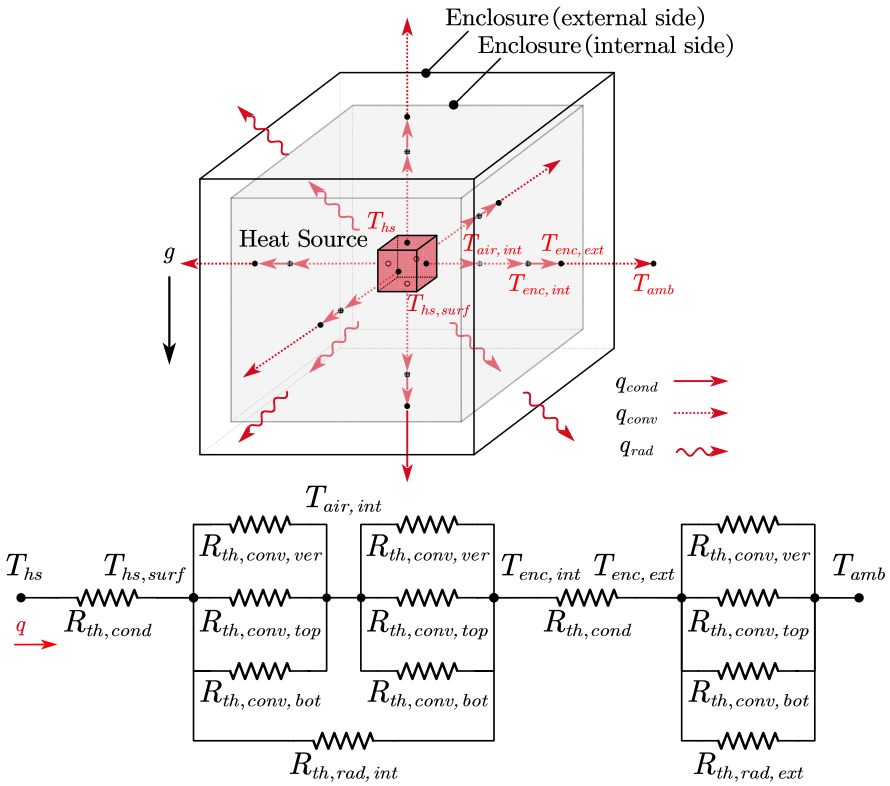


Fig. 6-1 The thermal structure and thermal resistance network when a heat source within a sealed enclosure dissipates the heat via natural convection.

Fig. 6-1 illustrates the simplest thermal structure, wherein a heat source with passive cooling is located inside a sealed enclosure. For the purpose of analysis, the heat source can be assumed to have a rectangular body. The $T_{enc,int}$ and $T_{enc,ext}$ denote the temperatures of internal and external side of enclosure, respectively. To model this structure, the generated heat q is transferred from T_{hs} to the ambient temperature T_{amb} through events in categories of:

- T_{hs} to heat source surface $T_{hs,surf}$ by conduction
- $T_{hs,surf}$ to internal air $T_{air,int}$ by convection
- $T_{air,int}$ to T_{amb} by heat exchange
- $T_{hs,surf}$ to $T_{enc,int}$ and $T_{enc,ext}$ to T_{amb} through radiation

The first event involves sole conduction through heat source body, which may consist of various conduction paths such as die bonding, lead frame, device package, PCB, and thermal via. The conduction thermal resistance $R_{th,cond}$ can be expressed as:

$$R_{th,cond} = \frac{L_{cond}}{k_{cond} \cdot A_{cond}} \tag{6.1}$$

where L_{cond}, k_{cond}, and A_{cond} is the thickness, thermal conductivity, and area of the solid, respectively. In the second event, the heat is transferred by convection as shown in dashed arrow in Fig. 6-1. By defining the $T_{air,int}$ as average bulk temperature of internal air, the convective thermal resistance $R_{th,conv}$ can be written as:

$$R_{th,conv} = \frac{1}{h_{conv} \cdot A_{conv}} \tag{6.2}$$

where h_{conv} is convective heat transfer coefficient:

$$h_{conv} = \frac{k_{air}}{L_c} \cdot Nu \tag{6.3}$$

where A_{conv} is convection area, k_{air} is the conductivity of the air, and L_c is the characteristic length which is defined as:

$$L_c = \frac{A_{conv}}{P} \tag{6.4}$$

where P is the perimeter of the object surface. The Nu in (6.3) is the Nusselt number. For the case of natural convection, the correlation of Nu is impacted by the directions of convection. By assuming that all six surfaces of the heat source are flat surfaces, the empirical Nu for top, bottom, and vertical surfaces can be derived as [206, 207]:

$$Nu_{top} = \begin{cases} 0.54\,(GrPr)^{1/4} & 10^4 < GrPr < 10^7 \\ 0.15\,(GrPr)^{1/3} & 10^7 < GrPr < 10^{11} \end{cases} \tag{6.5}$$

$$Nu_{bot} = 0.27\,(GrPr)^{1/4} \quad 10^5 < GrPr < 10^{11} \tag{6.6}$$

$$Nu_{ver} = \begin{cases} \left\{0.825 + \dfrac{0.387\,(GrPr)^{1/6}}{\left[1+(0.492/Pr)^{9/16}\right]^{8/27}}\right\}^2 \\ 0.68 + \dfrac{0.67\,(GrPr)^{1/4}}{\left[1+(0.492/Pr)^{9/16}\right]^{4/9}} \quad GrPr \le 10^9 \end{cases} \tag{6.7}$$

where Gr is the Grashof number which describes the ratio between buoyancy to viscous forces

acting on air, and *Pr* is the Prandtl number that defines the ratio of momentum diffusivity and thermal diffusivity. Clearly, the Nu_{top} is the highest due to the nature of fluid mechanics, leading to a higher h_{conv} at top surface compared to bottom and vertical surfaces. The *Gr* and *Pr* in (6.5) to (6.7) can be expressed as:

$$Gr = \frac{g \cdot \beta \cdot {L_c}^3 (T_{hs,surf} - T_{air,int})}{\nu^2} \tag{6.8}$$

$$Pr = \frac{C_\rho \cdot \mu}{k_{air}} = \frac{C_\rho \cdot \rho \cdot \nu}{k_{air}} \tag{6.9}$$

where g is gravitational acceleration, β is the thermal expansion coefficient, ν is the kinematic viscosity, C_ρ is the specific heat, μ is dynamic viscosity, and ρ is fluid density.

The mechanism of the third event can be understood through the analogy of a heat exchanger, in which two fluids are separated by a solid that facilitates heat exchange between them. The solid can be assumed to be a flat, clean, and unfinned surface composed of a single material. Therefore, the R_{th} components in the third event consist of two $R_{th,conv}$ in series with one $R_{th,cond}$ in middle of them. Additionally, the third event is in series with the first and second events.

For the final event, heat can also be transferred through radiation without any interaction with air. Unlike conduction and convection, radiation does not require a medium and is most efficient in vacuum. Radiation can also occur between two bodies separated by a medium at a temperature colder than both bodies. Therefore, an additional path for radiation appears between two surfaces and is in parallel with the previous events. Assuming that the heat source within enclosure is one enclosed system, with radiation $q_{rad,int}$, while the enclosure surrounded by external isothermal ambient is another enclosed system with $q_{rad,ext}$, the equations can be written by obeying Kirchhoff's law:

$$q_{rad,int} = \frac{\sigma \cdot ({T_{hs,surf}}^4 - {T_{enc,int}}^4)}{\frac{1-\varepsilon_{hs}}{\varepsilon_{hs} \cdot A_{hs}} + \frac{1}{A_{hs} \cdot F_{hs-enc}} + \frac{1-\varepsilon_{enc}}{\varepsilon_{enc} \cdot A_{enc,int}}} \tag{6.10}$$

$$q_{rad,ext} = \frac{\sigma \cdot ({T_{enc,ext}}^4 - {T_{amb}}^4)}{\frac{1-\varepsilon_{enc}}{\varepsilon_{enc} \cdot A_{enc,ext}} + \frac{1}{A_{enc,ext} \cdot F_{enc-air}} + \frac{1-\varepsilon_{amb}}{\varepsilon_{amb} \cdot A_{amb}}} \tag{6.11}$$

where σ is the Stefan-Boltzmann constant, ε is the emissivity of the material based on its radiative

property, and F is the view factor which depends on the geometry. For the second enclosed system, since the area of ambient air A_{amb} can be assumed to be infinite, and $F_{enc,ext\text{-}amb}$ equals 1, then (11) can be simplified as:

$$q_{rad,ext} \approx \varepsilon_{enc} \cdot A_{enc,ext} \cdot \sigma \cdot ({T_{enc,ext}}^4 - {T_{amb}}^4) \tag{6.12}$$

It is observed that the radiation transfer is positively related to temperature, while the temperature dependence of convective h_{conv} is usually weak. The radiative thermal resistance $R_{th,rad}$ is:

$$R_{th,rad} = \frac{\Delta T}{q_{rad}} \tag{6.13}$$

Finally, by combining (6.1) to (6.13), the corresponding R_{th} network for Fig. 6-1 can be depicted. The model is valid when assumptions are made as follows:

- The system reaches a steady state.
- The surfaces are isothermal.
- The surfaces are gray bodies (emissivity = absorptivity), opaque (transmissivity = 0), and diffuse.
- The radiation is uniform on each surface.

The model in Fig. 6-1 illustrates the mechanism of natural heat transfer from heat source to the ambient. The steady state T_{hs} requires iterative process for results to converge which can be easily implemented in computing software like MATLAB.

Other than passive cooling, if the cooling solutions like forced air or liquid cooling are adopted to cool components with a high heat flux, the thermal scenario is described in Fig. 6-2. The heat source inside the enclosure is attached to the cooling device such as heat sink or cold plate. The cooling path aims to bring heat to the ambient or external system. To model the structure, the mechanism is summarized as in below events:

- T_{hs} to $T_{hs,surf}$ through conduction
- $T_{hs,surf}$ to $T_{cool,surf1}$ to $T_{cool,surf2}$ through spreading and conduction
- $T_{cool,surf2}$ to $T_{cool,out}$ through convection
- Temperature-rise between inlet $T_{cool,in}$ and outlet $T_{cool,out}$

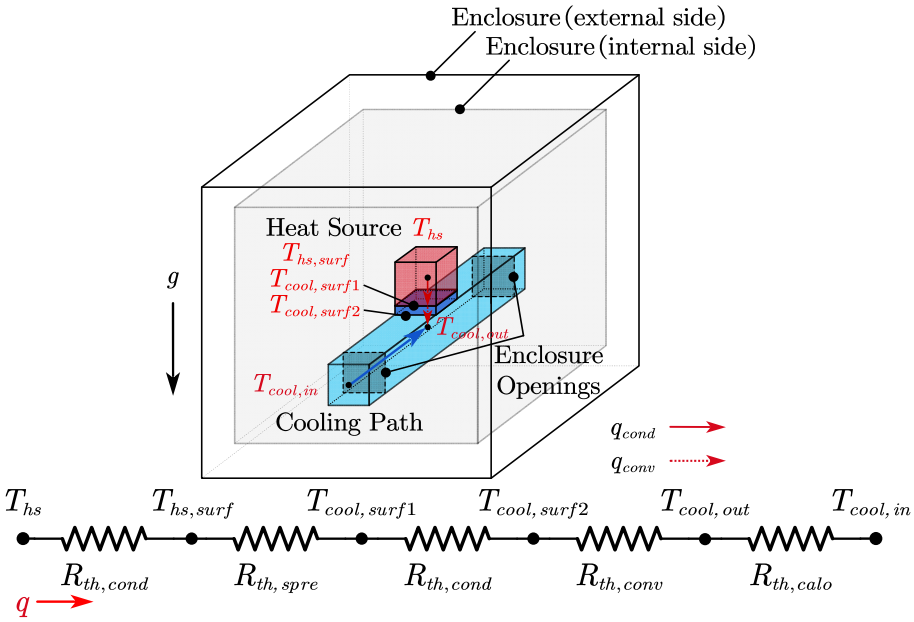


Fig. 6-2 The thermal structure and corresponding R_{th} network when forced or active cooling method is adopted for heat source.

Similarly, the first event involves conduction from T_{hs} to the $T_{hs,surf}$. In the second event, heat spreads from $T_{hs,surf}$ to $T_{cool,surf1}$ due to area mismatch, followed by conduction from $T_{cool,surf1}$ to $T_{cool,surf2}$ which contacts the cooling path. If the cooling device area is designed to be the same or similar as the heat source area, the spreading thermal resistance $R_{th,spre}$ can be negligible [208]. In the third event, the general expression is given in (6.2). The value of h_{conv} varies depending on the cooling techniques and requires empirical study. For the final event, the $R_{th,calo}$ can be expressed as [209]:

$$R_{th,calo} = \frac{1}{2 \cdot \dot{m} \cdot C_{\rho}} \tag{6.14}$$

where $\dot{m}$ is mass flow rate and $R_{th,calo}$ is usually a much smaller fraction of the total R_{th}. Based on above equations, the R_{th} network is illustrated in Fig. 6-2 with assumptions:

- The natural convection and radiation from the heat source to the ambient are neglected since they are much larger than the branch of active cooling path.
- The fluid temperature is considered as the average bulk temperature of the fluid.

Fig. 6-3 presents a design process of thermal management [210]. First, the heat sources and ambient environment of the inverter should be identified. Once the q from the heat source is

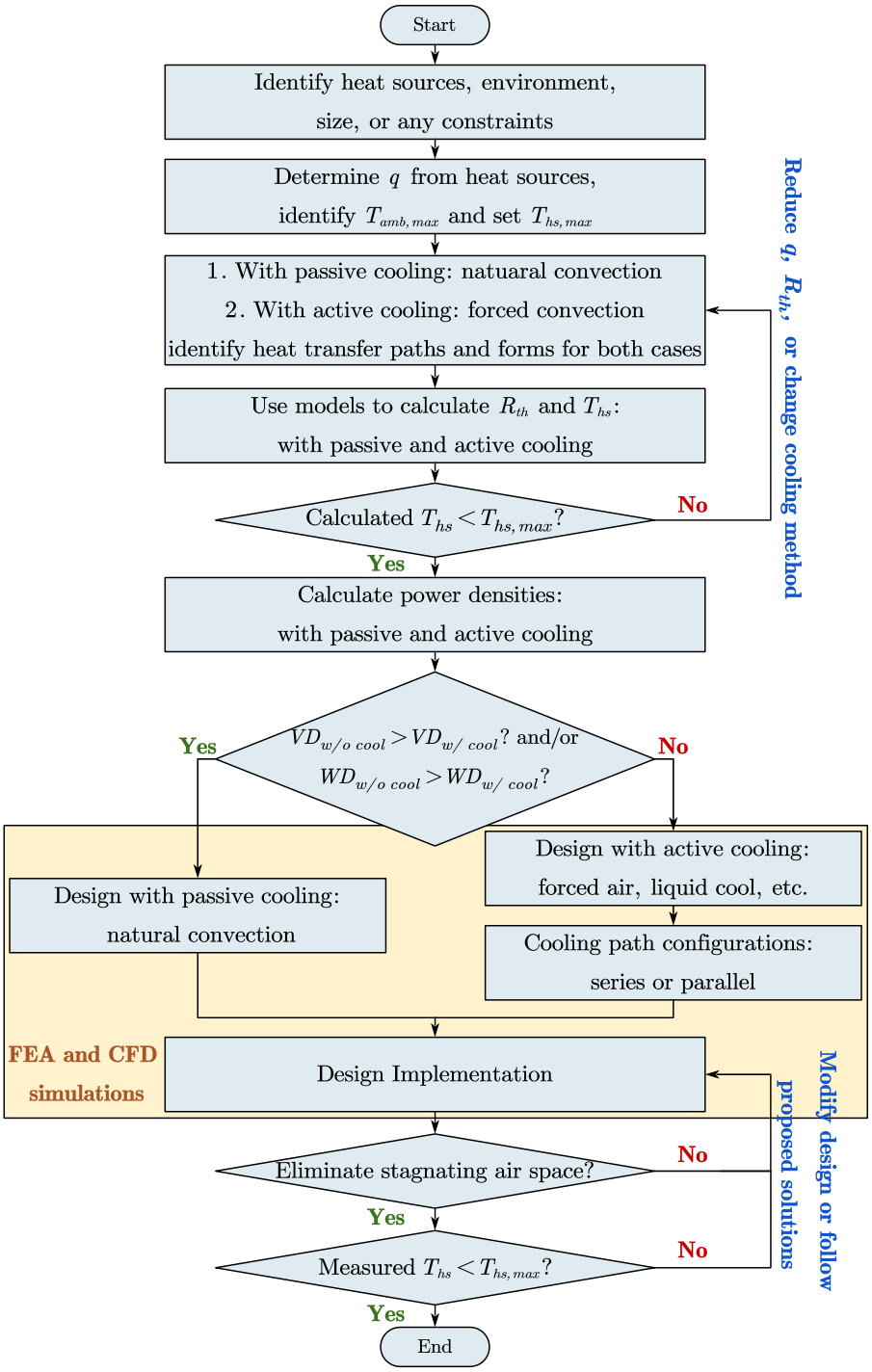


Fig. 6-3 Proposed systematic methodology for thermal management.

obtained, a decision must be made to use either natural convection (with passive cooling) or forced convection (with active cooling), based on the volume density (VD) and weight density (WD) of the two cases. Depending on the power dissipation of object, a cooling method with sufficient cooling capacity can be preliminarily selected. The T_{hs} can be estimated by using models presented

in Fig. 6-1 and Fig. 6-2. If the q cannot be further decreased, the loop R_{th} should be minimized by modifying geometry parameters or adopting more advanced cooling. Once the T_{hs} meets the targeted temperature $T_{hs,max}$, the VD and WD of both cases can be calculated and compared to make a final decision based on the application's requirement. In addition, if the cooling method is used to cool multiple heat sources, the cooling path can be arranged in either series or parallel configurations. The design stage should also consider electrical performances, and the process can be optimized utilizing finite element analysis (FEA) or computational fluid dynamics (CFD) simulations. It is crucial to identify any stagnating air space in the designed structure. As power inverters become more compact, the trapping heat in stagnating air space can cause hotspot in surrounding components. Section 6.4 presents the impact of stagnating air space and proposed solutions. To demonstrate the feasibility and thoroughness of the proposed methodology, thermal designs and mitigation strategies are presented for a 200 kW high-altitude 3L TNPC SiC inverter, which poses more challenging thermal issues than a sea-level 2L traction inverter.

6.3. Demonstrated 3L TNPC Propulsion Inverter

6.3.1 Overview of the Demonstrated 3L TNPC Inverter

Fig. 6-4 shows the single-phase circuit and overview of the demonstrated 3L TNPC inverter, and Table 6-1 summarizes the specifications of the inverter assembly [27, 211]. This prototype is a suitable candidate to demonstrate the proposed methodology due to multi-level topology, incorporation of more devices and EMI filters, and harsh environmental impact. The inverter is required to operate to thermal steady state at full load condition at high altitude, i.e., V_{DC} range of 740 V and i_o of 300 Arms at 7,620 m. In accordance with the design process illustrated in Fig. 6-3, the heat sources in the demonstrated inverter can be identified as busbars, power devices, DC-link capacitors, and DC and AC EMI filters. The inverter adopts PCB-busbar technology for laminated busbar to control e-field for insulation. The losses in the PCB-busbars are generated when conducting currents such as DC current I_{DC}, capacitor current i_C, device current i_S, and output current i_o, between nodes. For a worst-case scenario in thermal design, the maximum current values should be used in calculations. The copper trace resistance R_{PCB} can be easily calculated using available standards [212, 213]. The power devices in the inverter contribute to

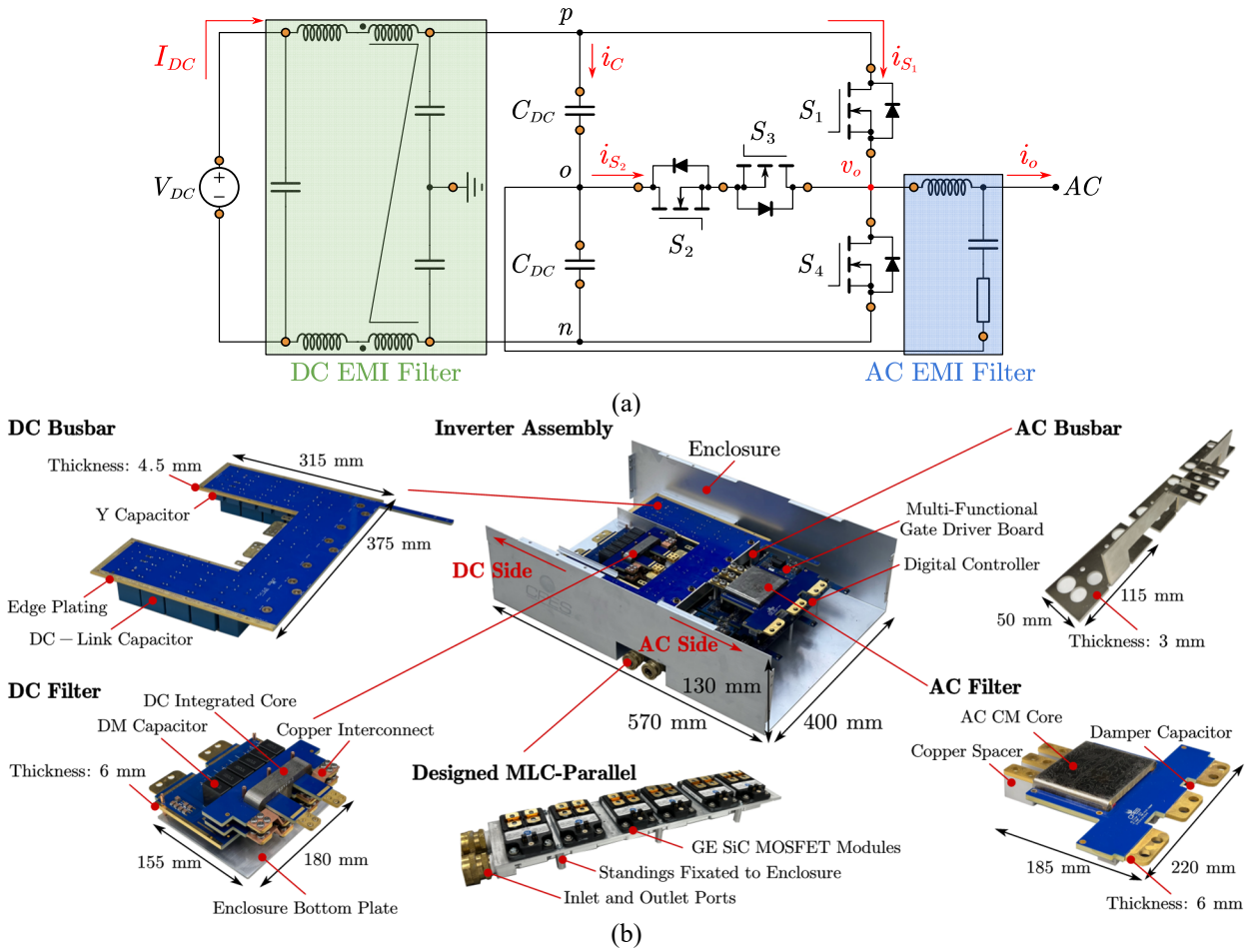


Fig. 6-4 The (a) single-phase circuit and (b) designed assembly of the demonstrated 200 kW 3L TNPC propulsion inverter with EMI filters. Critical conducting currents between connecting nodes of components are highlighted in the circuit diagram. For the convenience of displaying the inverter, power cables, some connectors, and spacers as well as top and side plates of the enclosure are removed.

dissipated loss mainly from switching and conduction losses. The losses incurred in different switching positions depend on the adopted PWM scheme, switching status, and operating conditions [25]. In this work, the inverter employs the conventional modulation of 3L Sinusoidal-PWM (SPWM). Fig. 6-5 and Fig. 6-6 illustrate the normalized switching loss and current distributions in different switching positions over one line-cycle, obtained from the circuit-level simulations. The results show that the generated losses are significantly affected by the power factor φ and modulation index (MI). In particular, switching position S_1/S_4 generates more switching loss at high φ, and conducting currents between S_1/S_4 and S_2/S_3 become more balanced at high MI.

TABLE 6-1 SPECIFICATIONS OF 3L TNPC INVERTER

Parameters	Value
Power Rating P_o	200 kW
Continuous Output Current i_o	300 Arms
DC Voltage V_{DC}	500-1000 V
Power Factor φ	0.91
Modulation Index MI	0.87
Peak Efficiency η	≥ 99 %
Ambient Temperature T_{amb}	75 °C
Operating Altitude	≤ 7,620 m (25,000 ft)
EMI Standard	DO-160

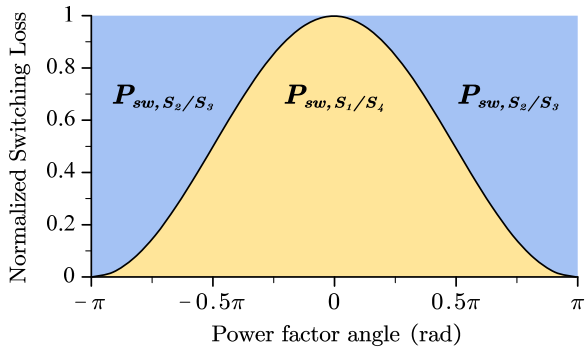


Fig. 6-5 By using 3L SPWM schemes, the switching loss distribution in S_1/S_4 and S_2/S_3.

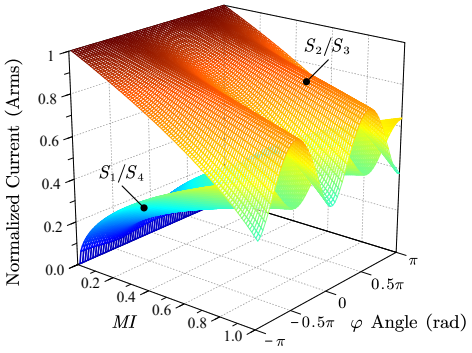


Fig. 6-6 The rms currents distribution in S_1/S_4 and S_2/S_3.

The DC-link capacitor bank is designed to handle the switching current and limit the voltage ripple across the capacitor bank under all operating conditions. The capacitor loss P_C is generated when capacitor current i_C with switching ripples flows through capacitor bank [144]. The losses of both DC and AC filters are mainly determined by conduction losses when currents conducting in the filter windings. The maximum currents in DC and AC filter windings are I_{DC} and i_o, respectively. In addition, the total core loss can be estimated by the improved Generalized Steinmetz Equation (iGSE) [214].

Table 6-2 summarizes all critical currents and dissipated losses in the inverter based on specifications in Table 6-1. By conducting systematic optimization [215], a total of six 1200-V SiC MOSFET modules from GE shown in Fig. 6-7 are selected as power devices. The values in Table 6-2 will be used for temperature estimation and thermal design.

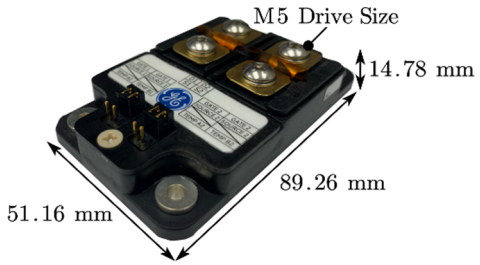


Fig. 6-7 The selected SiC MOSFET module for 3L TNPC.

TABLE 6-2 LOSS DISSIPATION IN DEMONSTRATED 3L TNPC INVERTER

Parameters	Value
DC Current I_{DC}	285 A
Capacitor Current i_C	159 Arms
Power Device Current of S_1/S_4	162 Arms
Power Device Current of S_2/S_3	193 Arms
DC-Link Capacitor Unit	TDK B3277 1200V Series
Power Devices of S_1/S_4 and S_2/S_3	GE Dual SiC MOSFET Module
Dissipated Loss of S_1 & S_4	198 W
Dissipated Loss of S_2 & S_3	98 W
DC Filters Current	Same as I_{DC} = 285 A
DC Filters Core Loss	2.4 W
AC Filters Current	Same as i_o = 300 Arms
AC Filters Core Loss	0.5 W

6.3.2 Harsh Environment Impact

As shown in Table 6-2, the harsh environment at high-altitude causes deterioration of convective $R_{th,conv}$ due to the decreased air density. Table 6-3 lists the parameters of air at both sea level and 7,620 m (25,000 ft) in 75 °C ambient. Fig. 6-8 further shows the comparisons of calculated $R_{th,conv}$ at different altitudes with different natural convective area A_{conv}. Due to air's lower ρ and higher v, the Gr and Pr are influenced and the $R_{th,conv}$ at 7,620 m becomes higher than that at sea level. Fig. 6-8 also suggests that the thermal path is mainly determined by $R_{th,conv,top}$ and $R_{th,conv,bot}$ in which $R_{th,conv,ver}$ can be neglected.

TABLE 6-3 PARAMETERS OF 75 °C AIR AT DIFFERENT ALTITUDE

Parameters	Sea Level	High-altitude of 7,620 m
Thermal Conductivity k_{air}	0.029 W/m·K	0.029 W/m·K
Gravitational Acceleration g	9.8 m/s^2	9.8 m/s^2
Thermal Expansion Coefficient β	0.0029 K^{-1}	0.0029 K^{-1}
Air Density ρ_{air}	1.02 kg/m^3	0.43 kg/m^3
Dynamic Viscosity μ_{air}	1.85e-5 Ns/m^2	1.85e-5 Ns/m^2
Kinematic Viscosity v_{air}	1.82e-5 m^2/s	4.3e-5 m^2/s
Specific Heat $C_{\rho,air}$	1009 J/kg·K	1009 J/kg·K

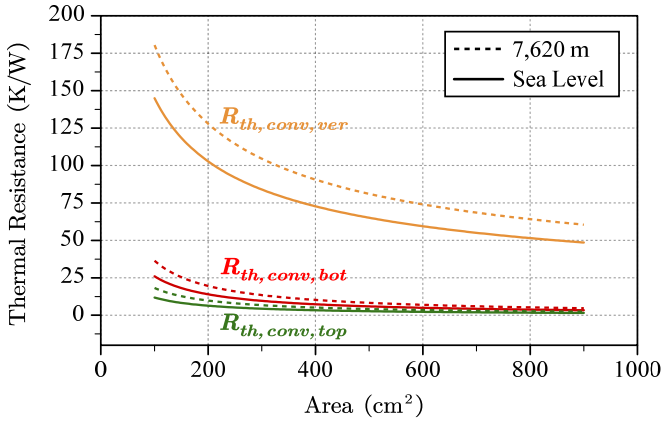


Fig. 6-8 The calculated $R_{th,conv}$ for top, bottom, and vertical surfaces at an ambient temperature of 75 °C and altitude of 7,620 m based on parameters in Table 6-1.

6.3.3 Thermal Mitigation Techniques and Design Workflow

The initial geometry for a thermal design is usually determined by the electrical components. The next step is to identify thermal paths and forms, with the aim of reducing thermal resistance R_{th} along the heat transfer path. In a system with passive cooling, such as the one shown in Fig. 6-1, heat is mainly transferred through $R_{th,cond}$ and $R_{th,conv}$, while $R_{th,rad}$ becomes more significant only in a vacuum environment. To mitigate $R_{th,cond}$ in (6.1), the thickness L_{cond} can be reduced, or k_{cond} and A_{cond} can be increased. To reduce $R_{th,conv}$ in (6.2), h_{conv} and the area A_{conv} can be increased. As presented in (6.5), natural convection is most intense at the top surface, so it is desirable to place heat sources facing upward to achieve a higher h_{conv}.

Conduction is much more effective than convection for heat transfer efficiency. If heat is difficult to dissipate by natural convection alone, an additional conduction path, such as using TIM to fill the air gap, can help reduce the total loop R_{th}. If forced cooling technique is adopted, Fig. 6-2 explains the improvements between different cooling solutions. Forced air cooling method can significantly increase h_{conv} by improving Nu in (6.3). Different approaches such as optimizing fin efficiency for MLC, jet impingement, two-phase cooling, and immersion cooling seek to improve either h_{conv} or A_{conv} to reduce $R_{th,conv}$. Using a heat spreader like a heat pipe or vapor chamber can further reduce $R_{th,cond}$, $R_{th,spre}$, and $R_{th,conv}$ due to the wick's high spreading performance and the fluid's two-phase transition nature [187]. For the double-side cooling method, the cooling area is basically doubled [38, 199].

To decide whether to adopt passive or active cooling methods for heat sources, power densities should be compared. Taking the PCB-busbars as an example, the ambient temperature is set to 75 °C. Since the footprint area of PCB-busbars is preliminarily determined by electrical components, the losses from all PCB-busbars can be easily calculated with the current values in Table 6-2. When passive cooling is adopted, the generated heat of the PCB-busbars is dissipated through natural convection, and the T_{hs} can be estimated using the model in Fig. 6-1. To keep the temperature within $T_{hs,max}$, the heavy copper PCB technology is adopted, and the copper thickness is increased to minimize the electrical resistance.

On the other hand, if active cooling is adopted to cool PCB-busbars, the T_{hs} can be calculated using the model in Fig. 6-2. Because of the low heat flux, the forced air-cooling solution is selected to compare the power densities with the case with passive cooling. If $T_{hs,max}$ is set to a lower value, the size of heat sink and required fans are increased to achieve a lower loop R_{th}. The total volume and weight can be estimated based on the documented data from off-the-shelf products.

Fig. 6-9 shows the comparisons of VD and WD between two cases. When $T_{hs,max}$ is set to a specific value, the case with passive cooling always has higher VD than the case using forced air cooling. Furthermore, when $T_{hs,max}$ is set to be higher than 87 °C, the case with passive cooling also has higher WD than the case with active cooling. By increasing the copper thickness of busbars, the T_{hs} can be kept within $T_{hs,max}$ without mounting bulky heatsink and fans. The workflow can be applied to other heat sources. For power devices with high heat flux, if passive cooling is adopted, the resulting power densities to keep T_{hs} within $T_{hs,max}$ are extremely low. Therefore, active cooling solutions should be adopted to cool power devices.

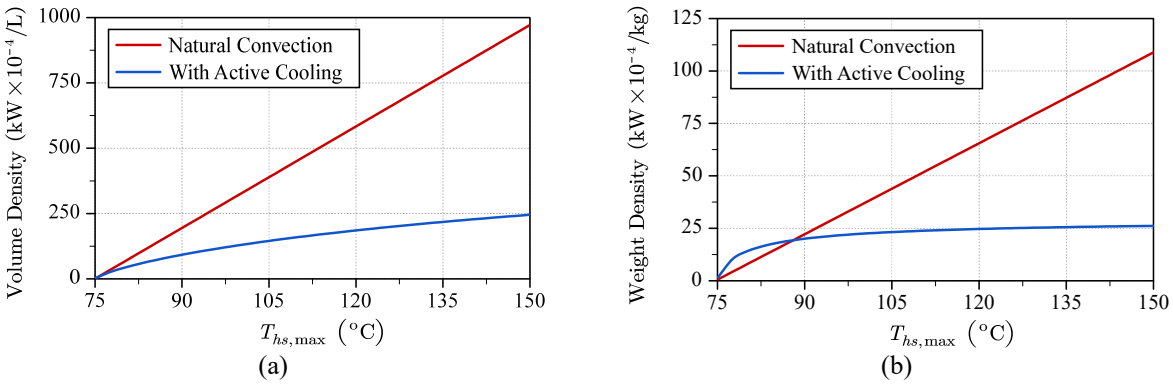


Fig. 6-9 The comparisons of (a) volume density and (b) weight density for PCB-busbar under conditions of with passive and active cooling.

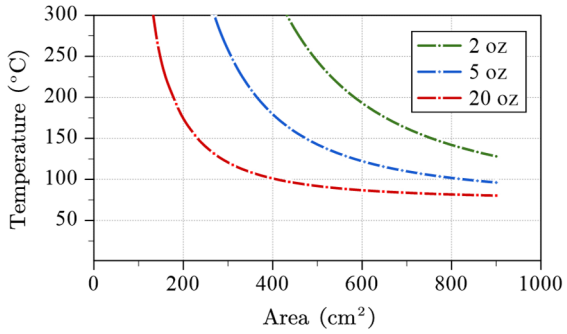


Fig. 6-10 Estimated temperatures using different copper thicknesses for PCB-busbar at an ambient of 75 °C and altitude of 7,620 m.

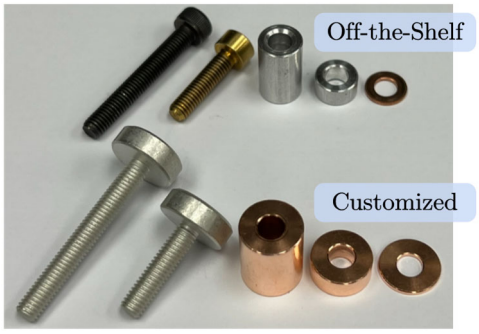


Fig. 6-11 Off-the-shelf products and customized copper parts.

As shown in Fig. 6-4(b), the inverter includes various components that are designed for DC busbar, DC filter, AC filter, and AC busbars. To address the thermal issue of localized heat sources, the $T_{hs,max}$ is set to 130 °C for all operating conditions. The designed boards utilize heavy copper PCB technology. Fig. 6-10 illustrates temperature comparisons obtained using different copper thicknesses while conducting a current of 300 A. The results indicated that the 2 oz copper is inadequate to withstand the harsh environment at high altitude. By using 20 oz copper, the temperature could be lower to below 130 °C for a footprint area approximately 275 cm^2.

The DC busbar has three main potentials layers, namely *p*, *n*, and *o* potentials that are responsible for conducting high currents. Each potential layer is manufactured with a copper thickness of 0.8 mm to ensure optimal thermal and current density performance. Additionally, the edge plating technique is utilized to ensure that the board is in direct in contact with the enclosure, providing an additional conduction path. The DC-link capacitors are positioned below the DC busbar and are also in contact with the bottom of the enclosure. As a result, the enclosure served as a large heatsink for the DC busbar and capacitors, and the surface of PCB is exposed to the top direction, thereby accelerating natural convection based on (6.5).

The DC EMI filter features a three-turn winding with an integrated DM-CM core structure, as shown in the bottom-left of Fig. 6-4(b). To handle the DC current I_{DC} of 285 A, two layers of 2 mm thick copper and current density of 3.4 A/mm^2 are selected for PCB-based windings. The winding turns are connected by copper interconnects, which are firmly fixated by four M5 screws to provide sufficient A_{cond} and reduce air gap between parts. Moreover, the DC integrated core is positioned naturally on the bottom plate of the enclosure, serving as both a grounding connection

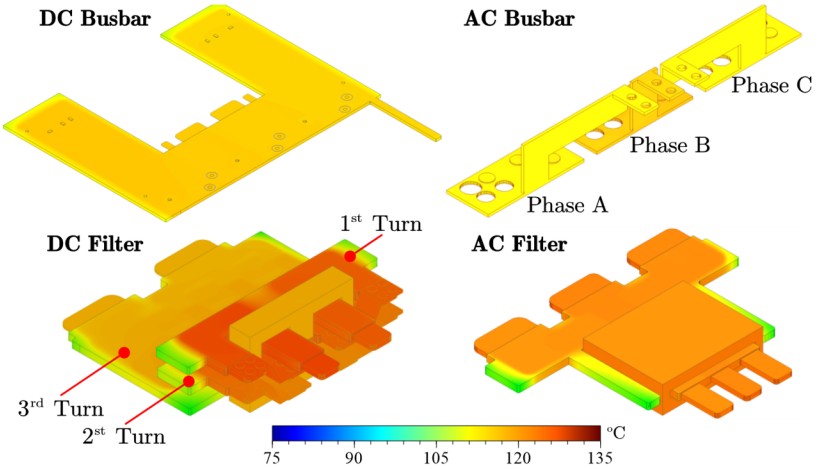


Fig. 6-12 ANSYS thermal FEA simulation results for localized heat sources.

and a conduction path for heat dissipation. The AC busbars that conduct i_o of 300 Arms have a copper thickness of 3 mm. They are separated from other PCBs to improve heat dissipation by exposing themselves to the air without FR4 material layers. The AC EMI filter shown in the bottom-right of Fig. 6-4(b) features a single-turn winding structure realized by using heavy copper PCB with two 2 mm thick copper layers. The AC CM core is designed to have a large contacting area A_{cond} with the PCB. For more detailed design optimization of the DC and AC filters, please refer to [216-219].

Fig. 6-11 depicts customized screws and spacers that are utilized to connect the boards. Copper is used as the material for these customized parts due to its higher k_{cond} as compared to the steel alloy of off-the-shelf parts. The copper parts provide lower conducting resistance and reduce $R_{th,cond}$ by improving k_{cond} and A_{cond} from wider screw head and body radius. Fig. 6-12 shows the FEA simulations that are performed to validate the thermal designs when boards are conducting currents at an ambient temperature of 75 °C and an altitude of 7,620 m. All boards are well controlled below 130 °C by following the design process.

6.3.4 Weight-Minimizing Optimization for MLC

In high altitude environments, the reduced air density makes it difficult to cool power devices with high heat flux using natural convection or conventional air-cooling methods. To maintain a safe junction temperature T_j within $T_{j,max}$, an aluminum-based liquid cooling MLC is selected due to its low weight, low cost, and high cooling capability.

TABLE 6-4 LIQUID COOLING CONDITIONS FOR POWER DEVICES

Parameters	Value
Modules Footprint Area (each) A_M	40.8 cm^2
Desired Junction Temperature $T_{j,max}$	≤ 150 ºC
Liquid Coolant	EGW 50/50
Coolant Inlet Temperature T_{inlet}	75 ºC
Flow Rate $\dot{m}$	0.05 kg/s - 0.25 kg/s
Maximum Allowable Pressure Drop ΔP_{max}	0.4 bar

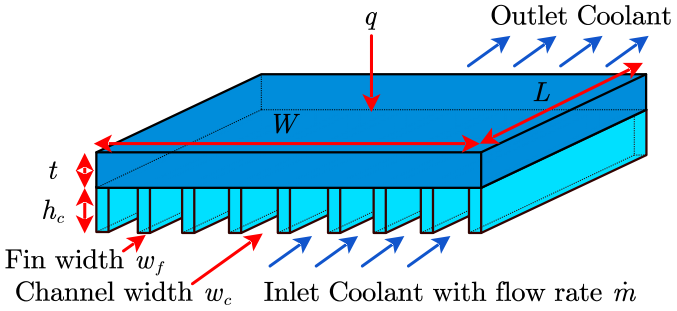


Fig. 6-13 The physical structure of MLC.

The MLC is designed based on a highest loss of 198 W from each switching position with additional thermal margin. The cooling conditions are listed in Table 6-4. By using the derived model in Fig. 6-2, the thermal requirement of the MLC can be derived. Fig. 6-13 shows the physical structure of the MLC. The concept is to increase A_{conv} by fabricating micro-level fins on the fin plate to reduce overall $R_{th,conv}$ [147]. Using MLC, the L_c and increased A_{conv} can be expressed as:

$$L_c = \frac{4 \cdot h_c \cdot w_c}{2(h_c + w_c)} \tag{6.15}$$

$$A_{conv} = N \cdot (L \cdot w_c + 2 \cdot L \cdot h_c \cdot \eta_{fin}) \tag{6.16}$$

where N is the number of fins and η_{fin} is the fin's efficiency [220]. The Nu can be written by correlation studied in [221]:

$$Nu = 0.00805 \cdot Re^{0.8} \cdot Pr^{0.33} \tag{6.17}$$

where Re is the Reynolds number that describes the fluid characteristics. In addition to the thermal performance, the pressure-drop ΔP between the inlet and outlet coolant is also important since it determines the required external pumping power P_{pump}:

$$P_{pump} = \frac{\dot{m}}{\rho} \cdot \Delta P \tag{6.18}$$

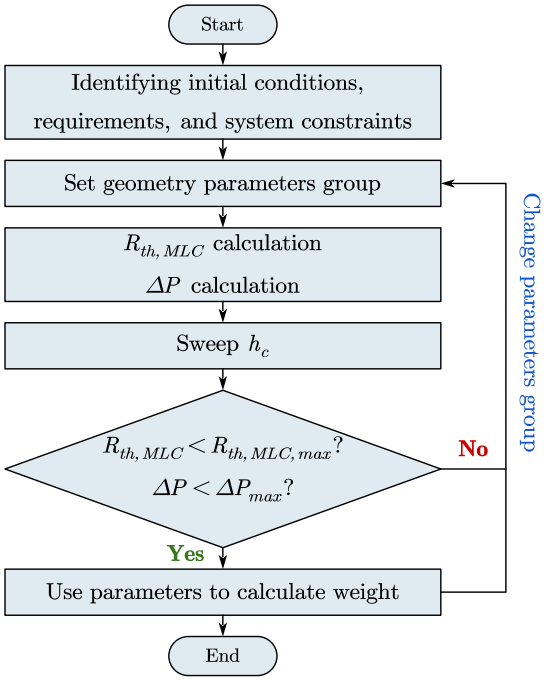


Fig. 6-14 Flow chart of MLC optimization to achieve minimum weight.

$$\Delta P = f \frac{L}{L_c} \frac{\rho \cdot {u_{cha}}^2}{2} + 1.5 \frac{\rho \cdot {u_{cha}}^2}{2} \tag{6.19}$$

$$u_{cha} = \frac{\dot{m}}{N \cdot h_c \cdot w_c \cdot \rho} \tag{6.20}$$

where f is the *Fanning* friction factor [220], and u_{cha} is the coolant velocity in single channel. The MLC with lower ΔP help reduces the weight of external pump since the size of the pump is usually positively related to its rating power. The design process of the MLC is illustrated in Fig. 6-14 [152]. The idea is to shrink the fin height h_c to reduce the weight of MLC while still meet all requirements. Once the initial conditions are identified, the performance and weight can be calculated depending on geometry parameters.

To effectively cool multiple power devices using MLC, it is necessary to compare the performance of different cooling path configurations, such as series and parallel configurations, following the design process [173]. Thus, the MLC optimization is separately conducted for both configurations, and their performances are further compared through CFD simulations. The designed MLCs for both configurations, namely, MLC-Series and MLC-Parallel, are shown in Fig. 6-15, with loose

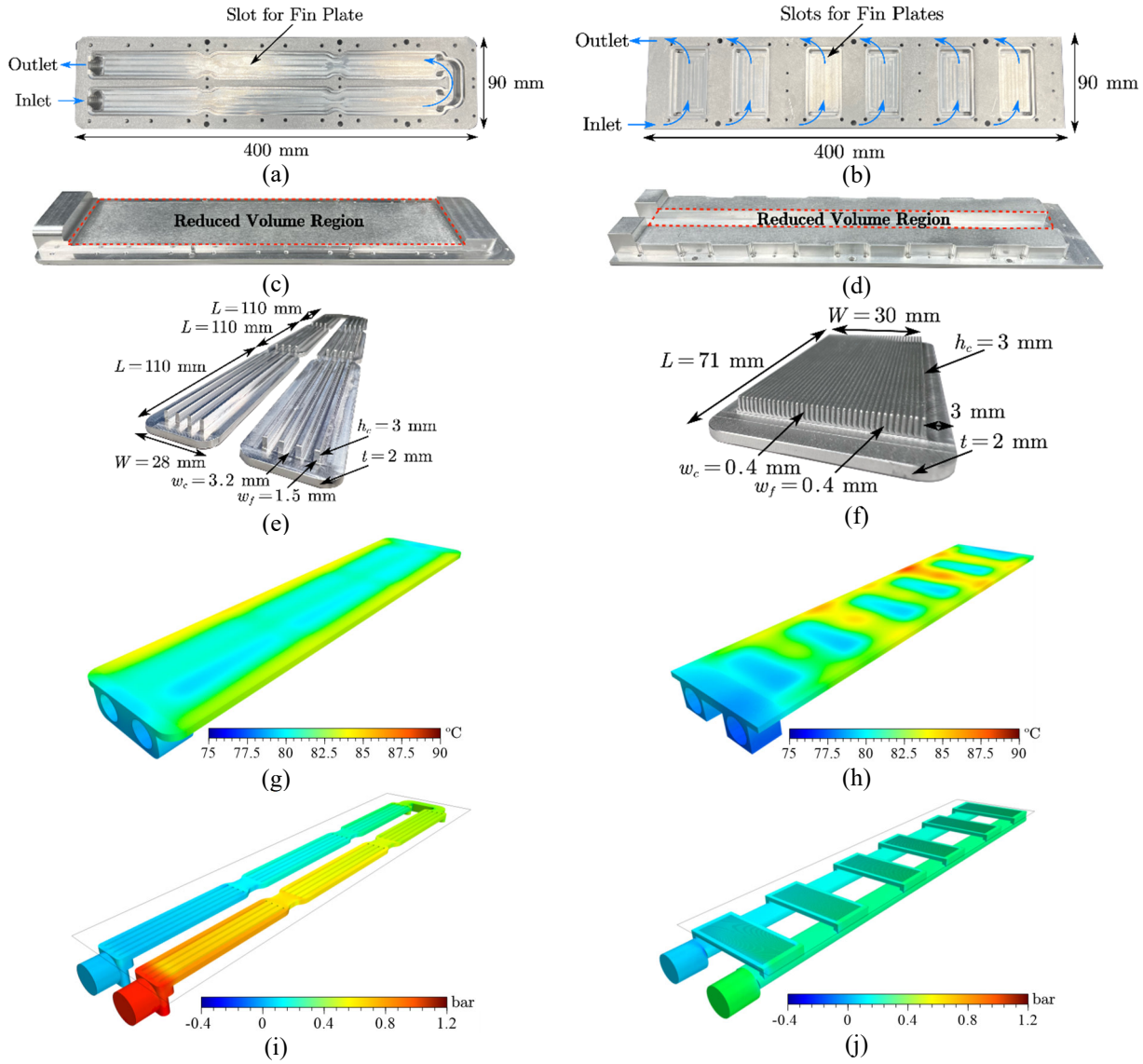


Fig. 6-15 For the MLC-Series: (a) base plate, (c) back-side, (e) fin plate, (g) thermal simulation, and (i) pressure-drop simulation. For the MLC-Parallel: (b) base plate, (d) back-side, (f) fin plate, (h) thermal simulation, and (j) pressure-drop simulation. The CFD simulation results are obtained from Star-CCM+.

part samples illustrating the internal fin structure. Fig. 6-15(a) and (b) show the base plates of both designs, with the power modules on MLC-Series cooled by the total amount of mass flow rate $\dot{m}$, while the $\dot{m}$ in MLC-Parallel is separated into 6 paralleled branches. The effect of design optimization is revealed in Fig. 6-15(c) and (d). where minimizing h_c eliminates additional volume on the back side of the MLCs. The MLC-Series and MLC-Parallel weigh 671 g and 810 g, respectively. Fig. 6-15(e) and (f) compare the corresponding fin plates of both versions, with the MLC-Series having fewer fins than MLC-Parallel, due to the characteristic of large ΔP caused by a long-distance L in (19). Installing more fins would increase u_{cha} due to a narrower channel,

eventually exceed ΔP_{max}. Conversely, the MLC-Parallel has a larger ΔP margin, allowing more fins to be manufactured.

To compare the thermal performances, the CFD simulation results using Star-CCM+ are shown in Fig. 6-15(g) and (h). Each module is assigned to dissipate 300 W (total 1800 W) while $T_{cool,in}$ and $\dot{m}$ are set to be 75 ºC and 0.25 kg/s, respectively. The modules are not included in the CFD simulations to show the surface temperature of the MLCs. The results show that the highest surface temperature of MLC-Series is 87 ℃, which is lower than 89 ℃ of MLC-Parallel, but only at the top right corner where no coolant path is present. If only focusing on the fin plate locations where the modules are mounted, the MLC-Parallel has a temperature of only 78 ºC which is 3 ºC lower than the 81 ºC of MLC-Series, indicating that the former has a better dissipation efficiency for power modules than the latter. Fig. 6-15(i) and (j) further show the ΔP of the MLC-Parallel is several times lower than that of the MLC-Series, implying that using an MLC-Parallel would result in a lighter external pump. Although MLC-Parallel is slightly heavier than MLC-Series, when considering a footprint area of 360 cm², it is at least 40 % lighter than most off-the-shelf cold plates on the market. Therefore, the MLC-Parallel is chosen as final design due to its better efficiency and ΔP performances.

6.4. Thermal Issue of Stagnating Air Space

While the individual designed parts meet the thermal requirements, the high-density inverter with multi-board structure is still prone to stagnating air spaces after assembly. As shown in the methodology in Fig. 6-3, the next step is to avoid or mitigate the impact caused by stagnating air space. It is most desirable to eliminate it at the beginning of the design stage, however, is also hard to anticipate the impact at the time.

6.4.1 Thermal Impact of Stagnating Air Space

The negative impact of stagnating air space on thermal performance is demonstrated by inverter structure in Fig. 6-4(b). The side view of the boards configuration is shown in Fig. 6-16(a). To optimize the commutation loops, the *p*, *o*, and *n* potential layers are embedded in the gate driver board. These layers, along with decoupling MLCCs, work together with the AC busbars to form

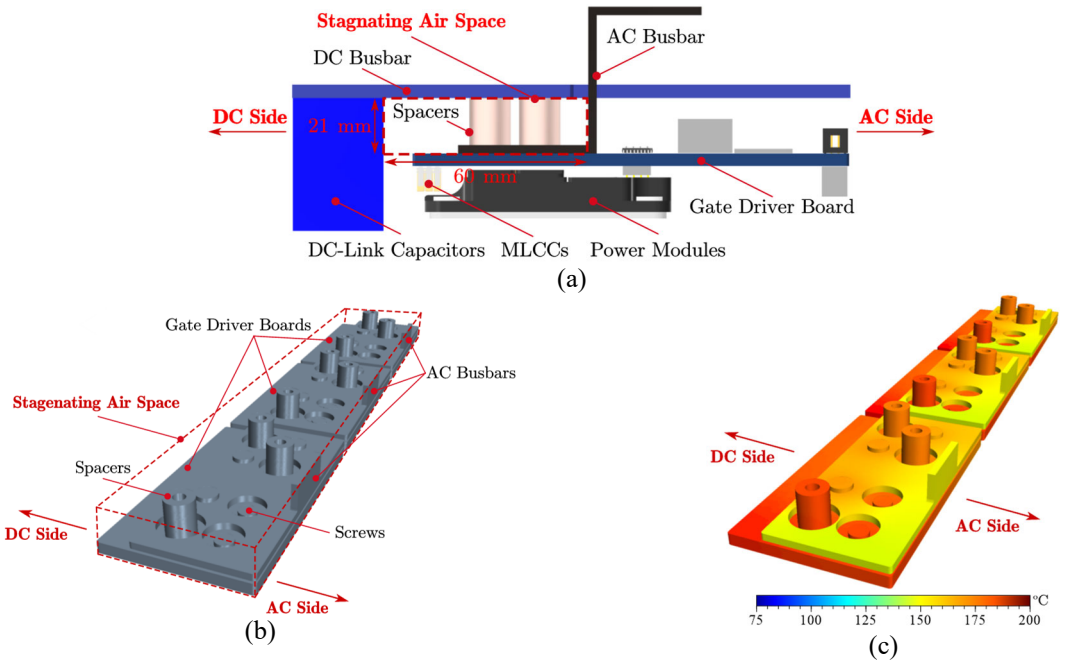


Fig. 6-16 The (a) side view of board structure, (b) highlighted stagnating air space, and the (c) thermal impact obtained from Star-CCM+ simulation.

TABLE 6-5 CONDITIONS OF STAGNATING AIR SPACE IN SIMULATION

Parameters	Value
Ambient Temperature	75 ºC
Altitude	7,620 m
Loss from MLCC Vias on each Gate Driver Board	26.5 W
Loss from each AC Busbar	2.3 W
Loss from Screws (per phase)	1.2 W
Loss from Spacers (per phase)	0.5 W

loops [222, 223]. However, as indicated by the red dashed box, a stagnating air space is formed, which is trapped by the DC busbar, DC-link capacitors, gate driver boards, and AC busbars. Furthermore, both sides of the air tunnel are blocked by the enclosure. Fig. 6-16(b) highlights the stagnating air space, and the corresponding CFD simulation result is shown in Fig. 6-16(c) with thermal conditions listed in Table 6-5. Heat is generated when currents conduct through MLCC vias on gate driver boards and AC busbars, which leads to an undesirable high temperature of around 180 ºC on the left side of the driver boards. Although the AC busbars on the right are exposed to ambient air, the temperature still reaches almost 150 ºC. Clearly, the stagnating air space has a detrimental effect on thermal performance and is created due to the combination of optimal electric performance and high-density nature.

6.4.2 Proposed Solutions for Stagnating Air Space

To mitigate the impact of stagnating air space in a sealed enclosure, several solutions are proposed as follows:

- Modify or redesign the inverter structure: This solution involves eliminating existing stagnating air space or hotspots by modifying or redesigning the inverter structure. While suitable for early-stage design processes, achieving the original optimal electrical performance may not be possible, and the redesign process can be time-consuming and costly.
- Introduce additional cooling methods: This solution involves installing additional heatsinks or cold plates to cool the high-temperature regions. It is a cost-effective and time-efficient solution that allows for maintaining the original optimal electrical performance. However, it may increase the weight of the inverter due to additional parts, and the required power of fans, external heat exchangers, or pumps may further increase external system weight.
- Introduce circulating air to harmonize the temperature distribution in sealed enclosure: This solution involves introducing circulating air to eliminate the stagnating air spaces by using an internal cooling air duct (AD). The circulating air stream can be created by using internal fan or from external air sources. It requires minimal cost and time, and original optimal electrical performance can also be maintained. Moreover, fan and AD add little weight to the inverter system. However, fan-generated acoustic noise and AD's optimal airflow requires additional design efforts.

The most appropriate solution for eliminating stagnating air space depends on the specifics of each case. In this study, the method of introducing circulating air by utilizing an internal fan and cooling AD is chosen due to its low cost, short design time, and ability to maintain optimal electrical performance with minimal drawbacks such as increased noise and weight.

Fans provide blowing air, while the AD aims to guide the cooling flow to the hotspots. When space is not a constraint, the conventional rectangular AD (AD-REC) is a good option due to its simple and design-less structure. However, in most cases, the remaining space inside the sealed enclosure is limited, and the AD-REC cannot fit. To overcome this dilemma, an alternative

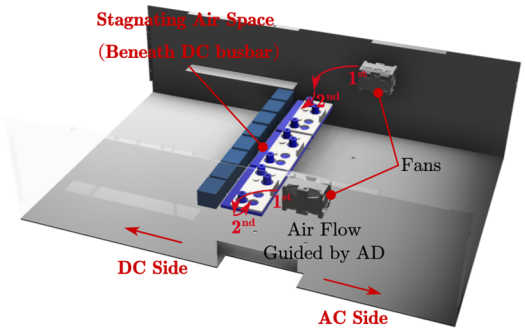


Fig. 6-17 Proposed solution for eliminating stagnating air space to prevent enlarging the enclosure.

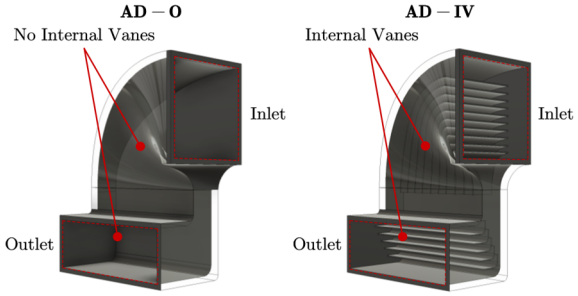


Fig. 6-18 The (a) original AD (AD-O) and (b) modified AD with internal guided vanes (AD-IV) to reduce pressure-drop caused by sharp bend turns.

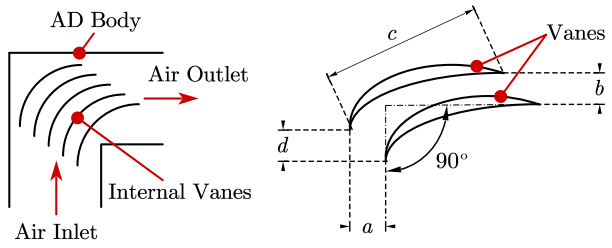


Fig. 6-19 The guided vanes structure and geometry parameters.

solution is proposed in Fig. 6-17, which highlights the stagnating air space with fans installed on both internal sides of the enclosure. This solution requires designed AD to guide the air through two 90-degree turns and provide consistent airflow to the stagnating air space. Fig. 6-18(a) shows the conceptual original AD (AD-O) without airflow optimization. The AD-O serves as a design benchmark and is optimized through the next two steps.

The purpose of the fan is to provide necessary power to overcome the head loss h_L experienced by the air as it flows through the path including AD. The relationship can be simplified from extended Bernoulli equation and expressed as:

$$h_L = \frac{p_{f,o} - p_{f,i}}{\gamma} = \frac{\Delta P}{\gamma} \tag{6.21}$$

where γ is the specific weight of the fluid, $p_{f,o}$ and $p_{f,i}$ are the pressure of the outlet and inlet of the fan, respectively. The (21) is valid by assuming the inlet and outlet ports of the fan have the same flow velocity and height level. It also suggests that the pressure-drop ΔP is positively related to h_L. The required fan power P_{fan} can be expressed as a function of AD's cross-section area $A_{AD,o}$ and velocity $V_{AD,o}$:

$$P_{fan} = A_{AD,o} \cdot V_{AD,o} \cdot \Delta P \tag{6.22}$$

From (22), if the P_{fan} and $A_{AD,o}$ is fixed, an AD with a smaller ΔP(or h_L) can result in a higher $V_{AD,o}$. Since the h_{conv} is positively related to the flow velocity, an AD with a higher $V_{AD,o}$ provides a better cooling. By using AD-O in Fig. 6-18(a), the calculated h_L is around 2.2 [220].

Fig. 6-18(b) shows the modified AD with optimized internal vanes (AD-IV) to optimize internal airflow [224]. The AD-IV is proposed to reduce the h_L for better cooling performance. Internal vanes are installed inside the AD-IV at the locations of two sharp turns. The vane structure is shown in Fig. 6-19 and the geometry parameters are defined as:

$$\alpha = \frac{b}{a} \tag{6.23}$$

$$\beta = \frac{d}{c} \tag{6.16}$$

The comprehensive analysis for vane parameters is studied in [225, 226]. In this work, the α and β are selected as 1 and 0.25, respectively. With aid of the internal guided vanes, the calculated h_L of AD-IV is around 0.4 which is 5.5 times lower than the 2.2 of AD-O.

The impact of internal airflow optimization can be observed from CFD simulations, as shown in Fig. 6-20(a) and (b) where airflow comparisons are presented at the outlet ports of AD- O and AD-IV, respectively. Line probes are placed to measure airflow velocity along horizontal distance. Using the same fan and having same outlet area $A_{AD,o}$, it is evident that the AD-IV has much more evenly distributed airflow at the outlet port than the AD-O. The outlet air velocity of AD-O is extremely uneven and accumulates at the bottom of the duct. In contrast, the airflow for the AD-IV, as shown in Fig. 6-20(b), presents much better distribution as the air velocity is evenly distributed around 12.5 m/s. The AD-IV efficiently guides the airflow from fan to hotspots even with sharp turns. Furthermore, the cooling performances of AD-O and AD-IV are compared in Fig. 6-21, using same conditions in Table 6-5. Both top and side views are shown for airflow and thermal comparisons. Comparing with the original case in Fig. 6-16(c), using AD-O improves the highest temperature from original 180 ºC to 145 ºC. However, the design is not satisfactory because the blowing air is unevenly distributed, and consequently, the airflow is unable to cover all hotspots on the gate driver boards. Moreover, the middle phase gate driver board experiences a

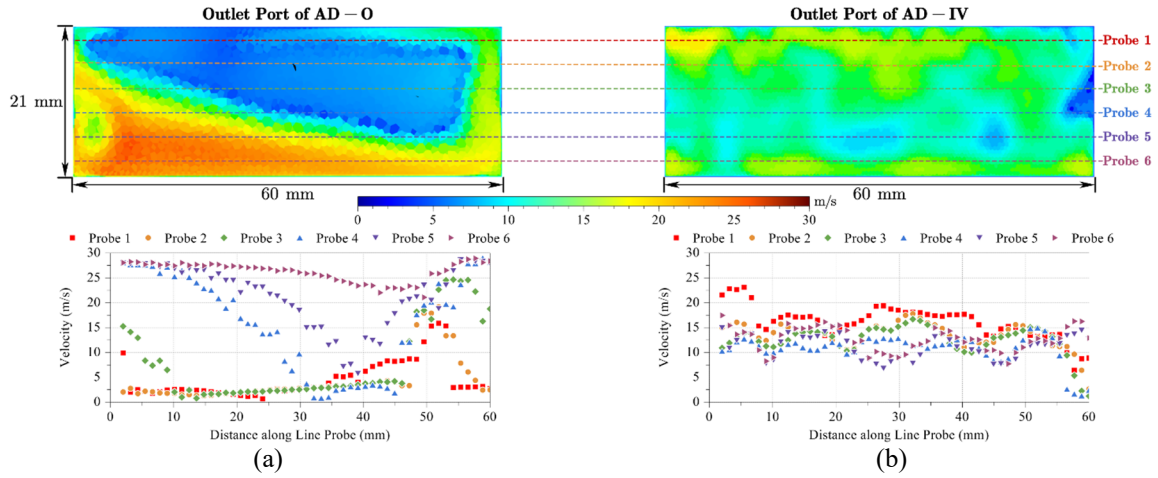


Fig. 6-20 The comparison of airflow distribution at the outlet port of (a) AD-O and (b) AD-IV.

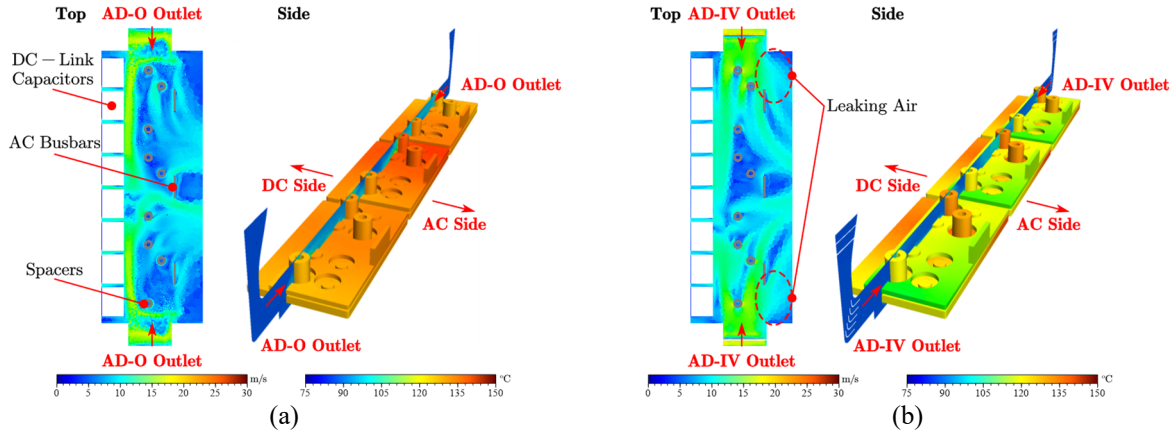


Fig. 6-21 The comparisons of airflow and cooling performance by using (a) AD-O and (b) AD-IV in CFD simulations.

10 ºC higher temperature than other two phases. On the contrary, using AD-IV not only reduces the highest temperature to 130 ºC, but also results in much better temperature distribution among three phases. Since AD-IV has a lower h_L than AD-O, a higher average V_{AD} at outlet of AD-IV can be expected, which aids the convective heat transfer efficiency.

The thermal robustness can be further enhanced by optimizing external airflow. In Fig. 6-21(b), although AD-IV successfully addresses the issue of stagnating air space, some air leaks through certain areas and goes unused. This results in reduced cooling efficiency. To mitigate this issue, an air block is added to the AD-IV, namely AD-IVB, as shown in Fig. 6-22(a).

Comparing the performance in Fig. 6-22(b) with the case using AD-IV in Fig. 6-21(b), the airflow in Fig. 6-22(b) penetrates the stagnating air space more efficiently with minimum leaking air. The highest temperature is further reduced to approximately 125 ºC. The final designed AD-IVB is 3D

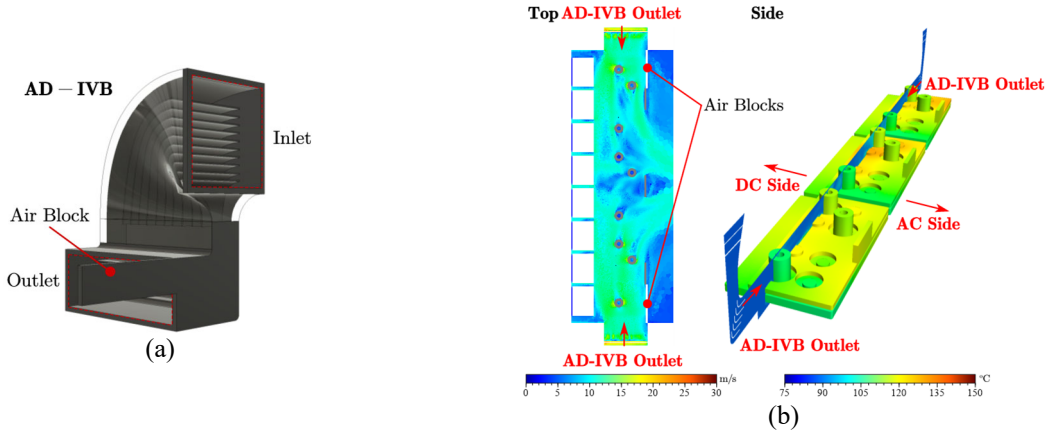


Fig. 6-22 The (a) AD-IVB with air block to improve external airflow and (b) airflow and cooling performances.

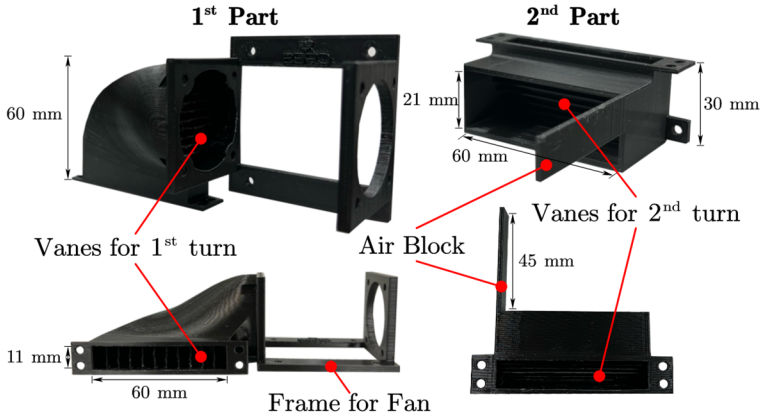


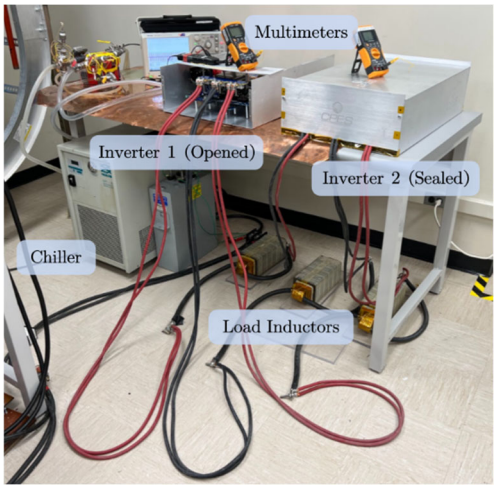
Fig. 6-23 The AD-IVB is 3D printed into two parts to show the internal vane design.

printed using resin as shown in Fig. 6-23. Each AD-IVB has a volume of 45 cm^3 and weighs 59 g. The weight is increased to 179 g if the fan and screws are included. The printed AD-IVB can be even lighter by using other materials. The designed AD-IVB proves to be a suitable solution for cases that have limited space to eliminate the stagnating air space. In this way, the optimal electrical performance and inverter structure can remain unchanged.

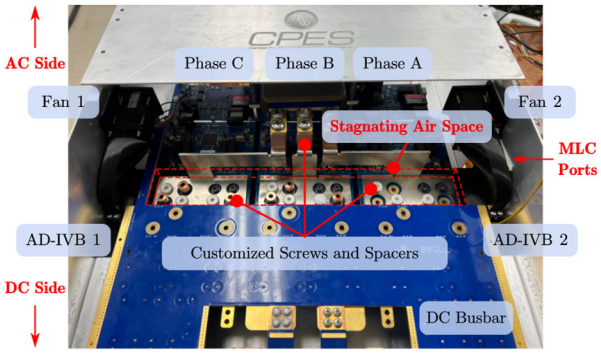
6.5. Experimental Validation

6.5.1 Verification of Demonstrated Propulsion Inverter

To conduct thermal test at full-power, two 3L TNPC inverters are assembled and arranged in pump-back configuration as shown in Fig. 6-24(a). Both inverter 1 and inverter 2 have identical designs. The enclosure for the Inverter 1 is opened to the ambient environment to allow for easy



(a)



(b)

Fig. 6-24 The (a) pump-back setup and (b) closer view of Inverter 1.

TABLE 6-6 PARAMETERS FOR FULL-POWER PUMP-BACK TEST

Parameters	Value
Peak AC Output Current $I_{o,pk}$	424 A
DC Voltage V_{DC}	≈ 700 V
DC Current I_{DC}	252 A
Power Factor φ	0.99 for Inverter 1 -0.99 for Inverter 2
Modulation Index	0.8
Dissipated Loss of S_1 & S_4 in Inverter 1	192 W
Dissipated Loss of S_2 & S_3 in Inverter 1	144 W
Room Temperature	25 °C
Coolant	EGW 50/50
Inlet Coolant Temperature $T_{cool,in}$	30 °C
Coolant Flow Rate $\dot{m}$	0.25 kg/s

monitoring of all hotspots' temperature, while the Inverter 2 is sealed to validate the final thermal design. The edges are sealed with Kapton tape, which creates a worst-case scenario due to its low thermal conductivity. Considering safety for thermal tests, all power cables, inverters, and components are arranged carefully to prevent contact with each other. Fig. 6-24(b) provides a closer view of Inverter 1. The DC busbar is disconnected to reveal the stagnating air space beneath it. Table 6-6 details the testing parameters for the full-power thermal test, while the tested full-power waveforms are presented in Fig. 6-25. All thermal tests last at least 20 minutes with V_{DC} around 700 V and i_o of 300 Arms to reach thermal steady-state.

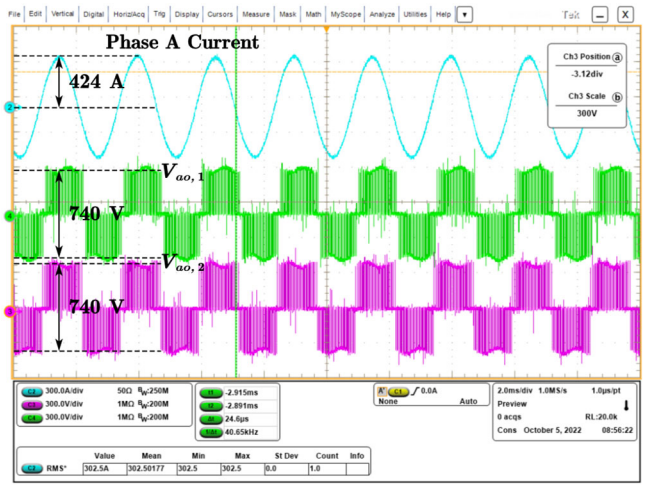


Fig. 6-25 Waveforms of continuous full-power pump-back test.

To evaluate the performance of the MLCs, power resistors with similar size to the power modules are used in preliminary tests. The fin and base plates of the tested MLCs are soldered together by the manufacturer to ensure a leakage-free system. The $\dot{m}$ is controlled by the external heat exchanger and chiller and is monitored by flowmeter. Fig. 6-26 and Fig. 6-27 show the comparisons of $R_{th,MLC}$ and ΔP performances of MLC-Series and MLC-Parallel, respectively. In both Fig. 6-26 and Fig. 6-27, the CFD simulation results well correspond to the mathematical predictions for both $R_{th,MLC}$ and ΔP. In Fig. 6-26(a), when compared to the model results, the experimental $R_{th,MLC}$ have overall error less than 30 % and are always higher than results obtained from mathematical model. The experimental ΔP in Fig. 6-26(b) is also 0.05 bar higher than results from both model and CFD simulations. This error may be caused by the reading error from measurement. On the other hand, in Fig. 6-27(a), the experimental $R_{th,MLC}$ of MLC-Parallel are always higher than mathematical results with maximum error around 28.5 %. However, as shown in Fig. 6-27(b), differences of ΔP are discovered between model and experimental results. The experimental ΔP is larger than both model and CFD simulations It is suspected that this difference is caused by the fabrication defects of the fin plate.

Fig. 6-28 shows the loose part sample of the fin plate of MLC-Parallel. The deformation of fins and small particles on the fin plate may block the channel and result in higher ΔP. It is found that the optimized performance of MLC-Parallel requires effort of fine manufacturing. Since the channels of MLC-Series are much wider than those of MLC-Parallel, no major defects are observed so the experimental results match with the model and CFD simulations with small error.

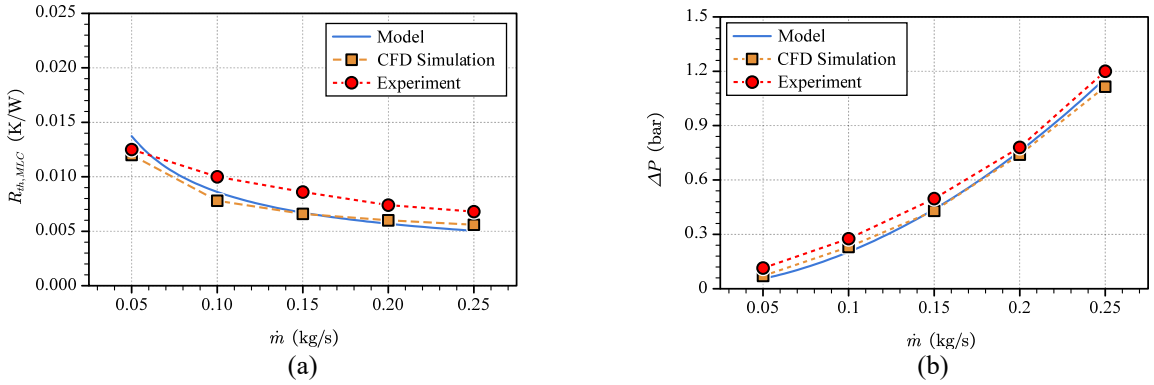


Fig. 6-26 The result comparisons of (a) $R_{th,MLC}$ and (b) ΔP of MLC-Series.

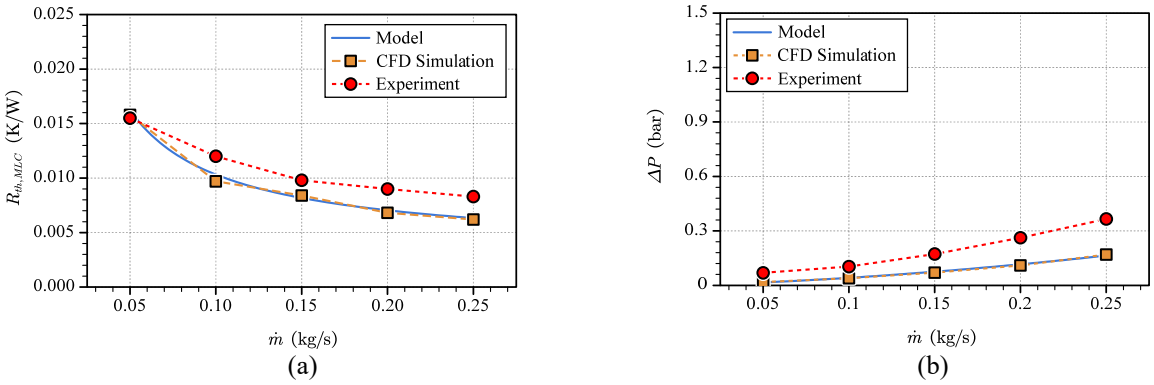


Fig. 6-27 The result comparisons of (a) $R_{th,MLC}$ and (b) ΔP of MLC-Parallel.

Despite that, the measured maximum ΔP of MLC-Parallel is always lower than 0.37 bar which is three times lower than that of the MLC-Series. As a result, the MLC-Parallel is a more attractive design. Since the 30 ºC EGW 50/50 has lower thermal conductivity and higher viscosity than the 75 ºC one [227], both $R_{th,MLC}$ and ΔP performances are expected to be better when the 75 ºC EGW 50/50 is adopted as coolant.

The junction temperature T_j is measured by the temperature detector of power module. The thermal grease TIM with thermal conductivity of 3 W/m·K is applied between modules and MLC-Parallel. All switching positions in the Inverter 1 are measured, and the results are summarized in Fig. 6-29. By using the designed MLC-Parallel, the maximum measured T_j is around 67 ºC at full power when $\dot{m}$ is at 0.25 kg/s. Fig. 6-29 also reveals that the temperature distribution is mainly determined by the loss difference among switching positions in the 3L TNPC inverter instead of the configuration of paralleling coolant paths. The small temperature difference among modules may be caused by the fin plate difference. The TIM may also have an impact on temperature distribution if the applied thickness is uneven for different modules.

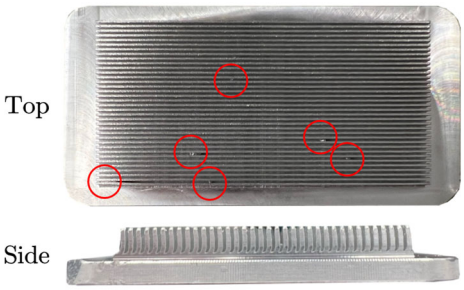


Fig. 6-28 The fabrication defects of small particles and distorted channels in the loose part sample fin plate of MLC-Parallel.

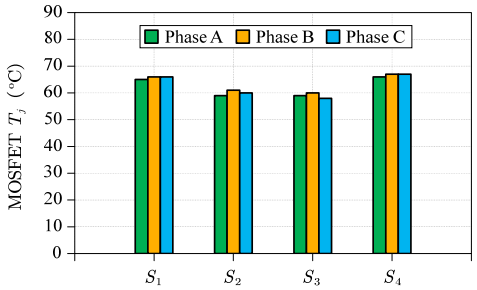


Fig. 6-29 The measured T_j of power modules in different switching positions when using 30 °C EGW 50/50 as coolant with $\dot{m}$ of 0.25 kg/s.

Two ADs in Fig. 6-24(b) are firstly removed from inverter to understand the thermal performances of localized heat sources. The temperatures of all heat sources are measured by using K-type thermocouples U1186A with multimeters. A comparison of two setups is shown in Table 6-7 by using off-the-shelf and customized parts. The measured temperatures using designed heavy copper PCBs and customized parts are much alleviated when compared to the case using off-the-shelf parts. By replacing parts, the maximum hotspot temperature-rise is improved by 34.4 %. The highest temperatures can be observed on AC busbar screws and MLCC vias on gate driver boards which are located in the stagnating air space. These locations are highlighted in Fig. 6-30. It is undesirable to have a temperature of 101 °C on the gate driver boards when tests are conducted at a room temperature of 25 °C. To verify the proposed circulating air AD solution for stagnating air space, the following tests would focus on those hotspot locations shown in Fig. 6-30.

The ADs are later installed in inverter to improve the hotspot temperatures in the stagnating air space. The fan used in this work is GFB0412ES-E from Delta Electronics. Fig. 6-31 shows the temperature improvements by using different versions of ADs. By introducing circulating air using AD-O, the temperatures of AC busbar screws and MLCC vias drop significantly from 95 °C to 74 °C and 101 °C to a decent 52 °C, respectively. The result in Fig. 6-31 also suggests the necessity of optimizing the cooling airflow. Due to a smaller h_L, the AD-IV with internal vanes helps decrease temperatures by around 10 °C compared to the case using AD-O. With optimization of both internal and external airflow using AD-IVB, another 5 °C temperature drop is achieved. Fig. 6-32 shows the phtted thermal images of the Inverter 1 using AD-IVB. The heat is observed concentrating in the location of the stagnating air space. The highest temperature of 59.8 °C is only located on the bottom of middle phase AC busbar. The measured temperature profile validates the thermal designs and proposed solution for stagnating air space.

TABLE 6-7 MEASURED STEADY STATE TEMPERATURE OF LOCALIZED HEAT SOURCES AT FULL-POWER AFTER 20 MINUTES

Measured Locations Parts	Off-the-Shelf	Customized
DC Busbar Screws (*p*, *n*)	71 ºC	61 ºC
DC Busbar Screws (*o*)	84 ºC	64 ºC
AC Busbar Screws	138 ºC	95 ºC
MLCC Vias on Gate Driver Board	141 ºC	101 ºC
DC Filter Core	29 ºC	28 ºC
DC Filter Winding PCB	54 ºC	49 ºC
AC Filter Core	45 ºC	43 ºC
AC Filter Winding PCB	78 ºC	63 ºC

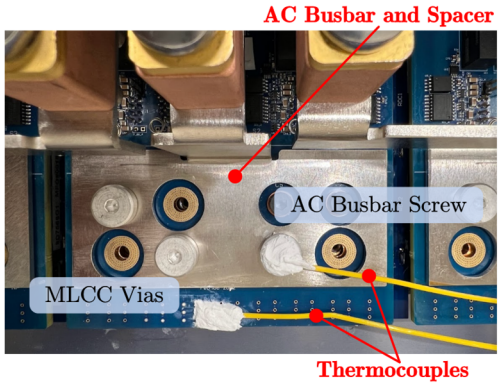


Fig. 6-30 Two locations of hotspot temperature in stagnating air space.

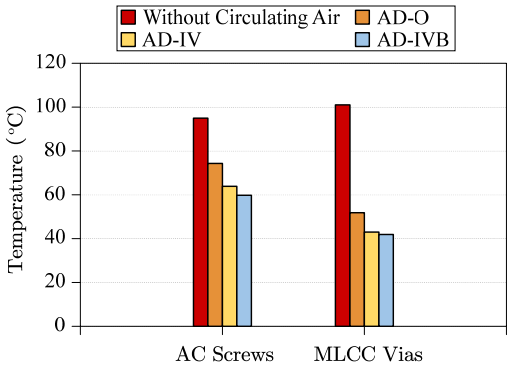


Fig. 6-31 The measured temperature of hotspots in stagnating air space by using different versions of AD.

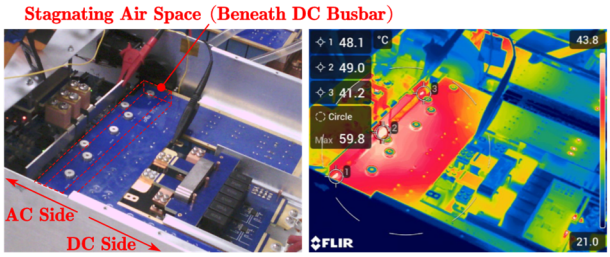


Fig. 6-32 Thermal images of full-power thermal test after 20 minutes.

The thermal design is further tested by using Inverter 2 with sealed enclosure. Only the temperatures of AC busbar screws are measured since they present highest temperature in thermal tests and images. Compared to the opened enclosure case, the measured hotspot temperature-rise increases approximately 19% in the sealed enclosure from temperature 59.8 ºC to 66.4 ºC. The enclosure temperature also rises to 31.5 ºC since the heat is dissipated to the ambient through the enclosure.

The temperature-rise at high altitude of 7,620 m is estimated based on thermal tests conducted in

the low-pressure chamber as shown in Fig. 6-33(a). The DC busbar, gate driver board, and AC busbar are placed in the low-pressure chamber with thermocouples mounted on them. A DC current of 200 A flows through the DC busbar and the measured steady temperatures are recorded in Fig. 6-33(b). When the altitude increases from sea level to 7,620 m, the temperature-rise increases around 40 %. Since the AC busbar has no current conducting, the temperature-rise is not obvious in this test. The error between theoretical and measured temperature is around 6 ºC which may cause by airflow difference between chamber and real environment [228]. The dynamic viscosity μ and air density ρ would also have impact on natural convection and generate a slightly lower thermal resistance which results in a lower measured temperature.

To summarize the testing results, the MLCs are firstly tested, and the accuracy of the mathematical model is validated by both CFD simulations and experimental results. The designed MLC-Parallel is proven to have good $R_{th,MLC}$ and superior ΔP performances when compared to MLC-Series. The ΔP of MLC-Parallel is always lower than 0.37 bar within the flow rate range from 0.05 to 0.25 kg/s. The power modules are later mounted on the MLC-Parallel and the maximum T_j is around 67 ºC at full power condition when $\dot{m}$ is at 0.25 kg/s. The temperatures of all localized heat sources are also measured by using thermocouples. By replacing the off-the-shelf mechanical parts with optimized copper parts, the hotspot temperature-rise is reduced by 34 % for AC screws. Moreover, the temperature-rise is further reduced by 54 % by introducing circulating air which is intended to harmonize the temperature distribution within the enclosure. After the enclosure is sealed, a 19 %

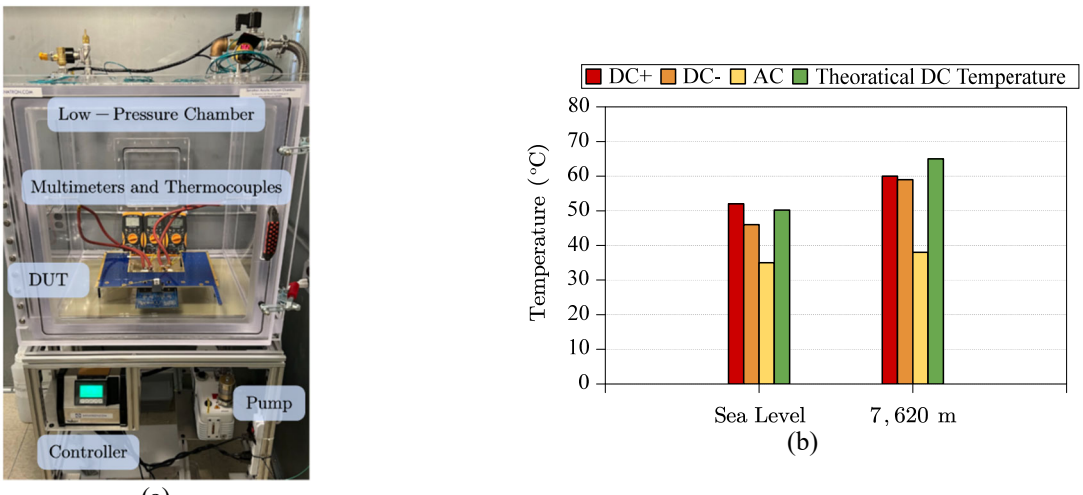


Fig. 6-33 The (a) pressure chamber test setup and (b) measured temperatures. Due to limited space, it is unable to place entire inverter into the chamber.

temperature-rise increment is observed from the hotspot temperature. By using the pressure chamber to run thermal test at the altitude of 7620 m, the temperature-rise increases around 40 % when compared to that at sea level. Combining all thermal results from the above tests, the maximum hotspot temperature within sealed enclosure can be estimated as around 130 ^{o}C at the ambient temperature of 75 ^{o}C and altitude of 7,620 m. Also, the highest temperature only occurs on part of the AC busbar without damaging other electrical components. The experimental results verified the feasibility of the proposed systematic design flow of thermal management.

6.5.2 Verification for High-Density All-in-One HB PCB

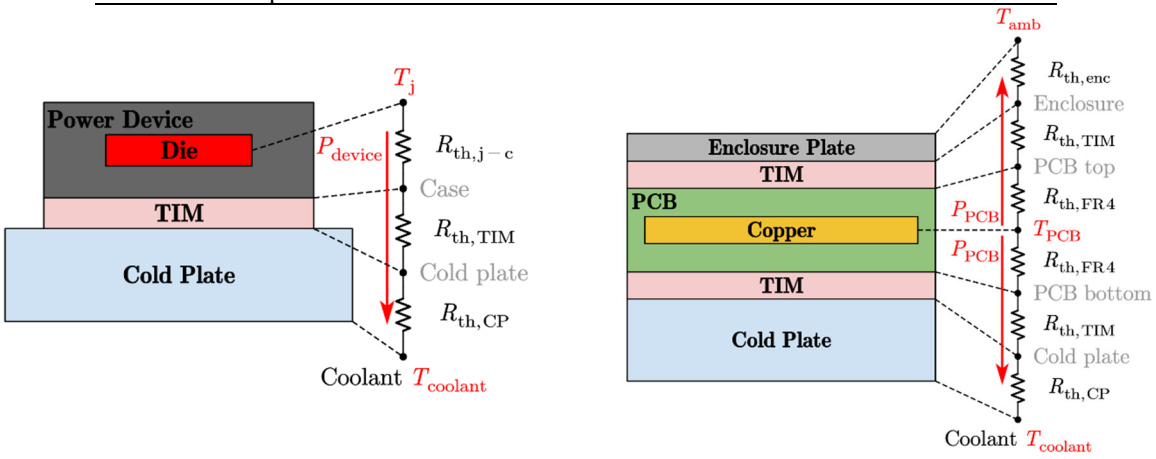
As the demonstrated multi-level inverter successfully verify the feasibility of the proposed design methodology, the same thermal design process is applied to the high-density all-in-one HB PCB. In the all-in-one HB PCB, major localized heat sources are the power devices, dc-link capacitors, and PCB itself. The loss information is summarized in Table 6-8. Losses of power devices P_{device} consists of switching and conduction losses, whereas the PCB loss P_{PCB} is mainly the conduction loss generated when conducting high-power currents. Fig. 6-34(a) depicts the steady-state thermal model of power devices, transferring P_{device} from junction temperature T_{j} to coolant temperature T_{coolant} via thermal resistances of junction-to-case $R_{\text{th,j-c}}$, TIM $R_{\text{th,TIM}}$, and MLC cold plate $R_{\text{th,CP}}$. The calculations of these resistances have been detailed in Section 6.2. Furthermore, the weight-minimizing optimization in Section 6.3.4 is applied to shrink the thickness of MLC cold plates shown in Fig. 5-8, and the cold plates are integrated into enclosure to achieve high integration.

The thermal model of the PCB is illustrated in Fig. 6-34. Owing to its single-board structure with low-profile components (Fig. 5-8), the PCB can be double-side cooled by both bottom MLC and enclosure top plate through gap-filler TIM. Similarly, the dc-link capacitors are cooled by bottom enclosure via gap-filler TIM. The footprint area of the gap-filler TIM is calculated according to the model in Section 6.2. The enclosure serves not only as mechanical housing but also as a cooling device for the all-in-one HB PCBs.

To verify the thermal designs, two thermal tests are conducted using the three-phase test setup in Fig. 5-27(b). The first thermal test investigates potential hot spots with a thermal camera, while operating the inverter at a lower current level of 120 Arms per phase to prevent overheating since

TABLE 6-8 LOSS DISSIPATION IN ALL-IN-ONE HB PCB

Parameters	Value
DC Current from V_{DC}	250 A
Capacitor Current $I_{C,rms}$	195 Arms
DC-Link Capacitor	KEMET C4AQ 800 V series
AC output current i_o	250 Arms/phase
Power Devices	Infineon IMZA120R007M1H
Loss of power devices P_{device}	55.5 W/device



(a) (b)

Fig. 6-34 Thermal models of (a) power devices to cold plate and (b) double-side cooled PCB.

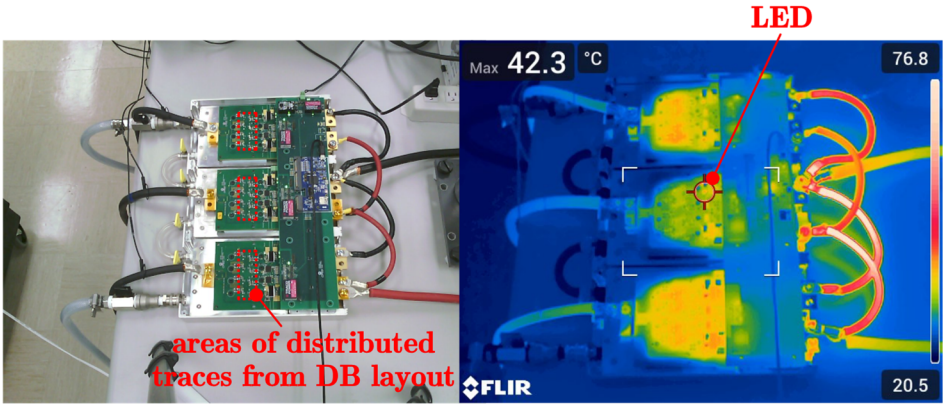


Fig. 6-35 Thermal images when enclosure top plate is removed and operating at i_o = 120 Arms/phase.

the enclosure top plate must be removed for thermal imaging. Fig. 6-35 shows the thermal images from top view of the setup after 20 minutes of operation. The PCBs stabilize at around 29 °C under a room temperature of 20 °C. In thermal images, the areas of distributed traces from proposed DB layout have slightly higher temperatures than surrounding area since all dc and ac currents concentrate in these regions. Moreover, the middle phase is slightly cooler than other two side phases, likely due to variations in either applied pressure of gap-filler TIM or MLC cold plates. Despite that, most importantly, no significant hot spots are identified in this test.

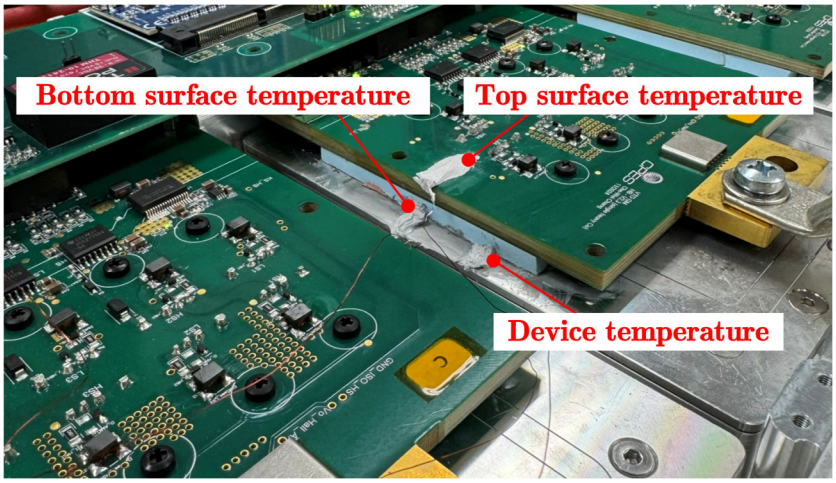


Fig. 6-36 Locations of thermocouples for full-current thermal tests.

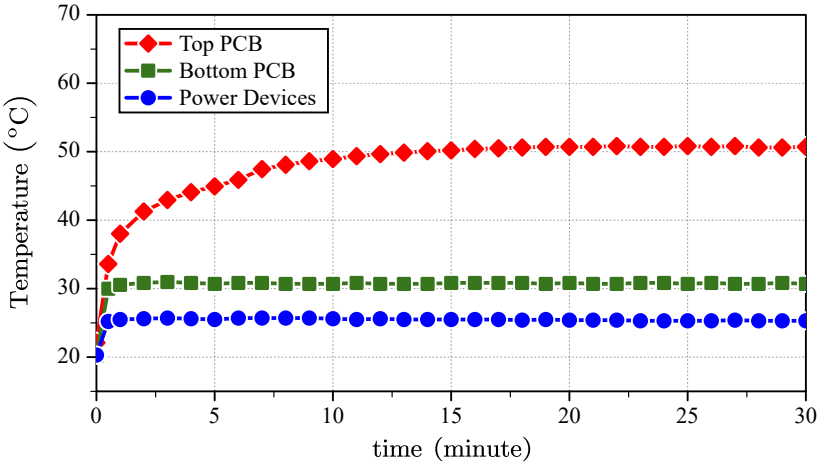


Fig. 6-37 Measured temperatures in the three-phase inverter when operating at full-current of i_o = 250 Arms.

The second thermal test evaluates the inverter under full-current operation at of i_o = 250 Arms under a room temperature of 20 ºC. In this test, the enclosure top plate is fully closed, and the key temperatures are measured by thermocouples. As shown in Fig. 6-36, three thermocouples are fixated by thermal putty, attaching to the top surface of PCB, bottom surface of PCB, and cold plate surface right behind the back plate of power devices to measure their temperatures. The measured results are summarized in Fig. 6-37 spanning 30 minutes. Since power device and the bottom surface of PCB are directly cooled by MLC cold plate, their temperatures quickly stabilize around 25.3 ºC and 30.6 ºC, respectively. The top surface PCB, which transfers heat to enclosure top plate and rely on natural convection to the plate, reaches the highest temperature of 51 ºC. Also, it takes more than 15 minutes for it to become thermal steady. Typically, the PCB is recommended to operate at temperature lower than 130 ºC. The experimental thermal results

confirm that the designed 200 kW high-density traction inverter meet not only the power density target of 100 kW/L, but also thermal requirements and is capable of reliable operation even at a higher ambient temperature in EVs.

6.6. Conclusion

In this chapter, a systematic methodology for thermal management in high-density high-power inverter is presented. The methodology is first demonstrated by a 200 kW multi-level inverter operating in a harsh environment, and later applied to the designed all-in-one HB PCB. Based on the derived thermal models, thermal mitigation techniques as well as cooling designs with high density and high efficiency are proposed. In addition, it is found that the stagnating air space created by multi-board sandwich structure of the inverter has a detrimental effect on thermal performance and can generate localized hotspots on electrical components. To address the thermal issue, several solutions are proposed, and the experimental full-power thermal tests validate the thermal design which shows a safe 130 ^{o}C at an ambient temperature of 75 ^{o}C and an altitude of 7,620 m. Furthermore, the final thermal tests are conducted to evaluate the thermal performance of designed all-in-one HB PCB. By leveraging integrated cold-plate cooling and enclosure-assisted heat dissipation, the inverter achieves safe operating temperatures under full-load conditions without any hot spots. The results not only confirm the feasibility of the proposed integration and thermal design strategies for designed 200 kW traction inverter but also highlight its robustness for future high-density power electronic systems.

Chapter 7
Conclusions and Future Work

7.1. Contributions

This dissertation focuses on optimizing high-power high-density dc/ac traction inverter with enhanced current sharing for paralleled discrete devices. The main contributions of this work are:

- Current sharing modeling and analysis: Comprehensive modeling and analysis are performed to study current sharing among paralleled devices. The derived models enable prediction of time-domain waveforms, identify key impact parameters, and provide practical layout guidelines.
- Passive current-balancing solutions: Guided by the derived models, two passive current-balancing solutions, the distributed block (DB) layout and differential-mode-choke (DMC) gate driver, are proposed and thoroughly evaluated. By implementing both techniques, when compared to the original baseline design, the static current sharing is improved by 66.7 %, and the dynamic current sharing is enhanced by 83 %.
- Active current-balancing solution: An active gate driver (AGD) is proposed to achieve near-perfect balanced currents. The *di/dt*-RC sensing method enhanced by proposed R_K sensing structure is adopted to measure device currents. Moreover, the behavioral difference between cases of asymmetric layout and mismatched devices is uncovered. The proposed AGD requires only one controller for the entire inverter system which makes it more practical for industrial applications than other AGD solutions.
- Systematic integration strategy: A “single-board” integration strategy is proposed for traction inverters to maximize high power density. While the conventional “sandwich” structure struggle to meet DOE targets, by following the proposed strategy, an all-in-one HB PCB is designed and successfully demonstrates a record power density of 101.7 kW/L.
- Methodology for thermal management: Comprehensive thermal modeling is established, and a systematic methodology for thermal management is proposed to address thermal

challenges in high-density inverters. The inverter prototypes successfully demonstrate the feasibility of the proposed methodology.

7.2. Future Work

Future work in the following areas include:

- Current sharing modeling: The time-domain model can be more completed by taking the transition region (in between dynamic and static regions) into consideration, allowing study of voltage and current oscillations and guide the circuit design.
- Passive current-balancing solutions: The proposed methods in this dissertation mainly focus on current imbalance caused by asymmetric layout, and the impact of mismatched devices is neglected. Though active solution of AGD helps balance currents regardless of causes, additional circuits and controller are required. Therefore, a passive solution that can balance the currents under all conditions will be very attractive for industrial applications.
- Active current-balancing solution: So far, the feasibility of AGD is verified via open-loop test. For practical applications, the close-loop control and continuous operation of AGD may yield challenges and should be further investigated in the future.

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