Integrated EMI/Thermal Design for Switching Power Supplies

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Thesis submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Master of Science
in
Electrical Engineering

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February 9, 1998
Blacksburg, Virginia

Keywords: EMI, Thermal, Switching power supplies

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(ABSTRACT)

This work presents the modeling and analysis of EMI and thermal performance for switch power supply by using the CAD tools. The methodology and design guidelines are developed.

By using a boost PFC circuit as an example, an equivalent circuit model is built for EMI noise prediction and analysis. The parasitic elements of circuit layout and components are extracted analytically or by using CAD tools. Based on the model, circuit layout and magnetic component design are modified to minimize circuit EMI. EMI filter can be designed at an early stage without prototype implementation.

In the second part, thermal analyses are conducted for the circuit by using the software *Flotherm,* which includes the mechanism of conduction, convection and radiation. Thermal models are built for the components. Thermal performance of the circuit and the temperature profile of components are predicted. Improved thermal management and winding arrangement are investigated to reduce temperature.

In the third part, several circuit layouts and inductor design examples are checked from both the EMI and thermal point of view. Insightful information is obtained.

Acknowledgements

I would like to express the deepest and sincere gratitude for my advisors Dr. Fred C. Lee and Dr. Dan Y. Chen, for their guidance and great support during the work. The extensive knowledge and insightful advice of Dr. Lee have guided me thorough the research. The many helpful suggestions and detail discussions with Dr. Chen enable me to finish the work. Without the help from them, it is impossible for me to start and finish the work. I must also thank my Master's committee member Dr. Dushan Borojevich, for his great support regarding the research.

I am grateful for the excellent faculty, staff and students at Virginia Power Electronics Center for their friendship and technical help. Particularly, I would like to thank Dr. Michael T. Zhang, Dr. Glenn R. Skutt for their initiative guidance and help in the study. I would like to express my appreciation to Mr. Liming Ye, Mr. Wei Chen, etc., for their friendship and sharing the knowledge with me.

Finally I would like to dedicate the thesis to my dear parents, Guowei Zhang and Sufang Ren, for their love and support in these years. The great thank goes to my mother for her accompanying me and sacrifice during the time for preparing the thesis.

This work was supported under Philip's Fellowship, provided by Philip's Laboratory, U.S.A.

Table of Contents

Chapter 1 1

Introduction 1

1.1. Background and Motivation 1

1.2. Approach 2

1.3. Thesis Outline 3

Chapter Two 5

EMI Prediction and Minimization 5

2.1. Parasitic Parameter Extraction and Modeling 8

2.1.1. Layout Inductance Extraction 9

2.1.2. Parasitic Capacitance Calculation 13

2.1.3. Power Device Models 13

2.1.4 . Passive Components Model 15

2.1.5 . Magnetic Components Model 19

2.1.5.1. Analytical Estimation of Winding Capacitance 19

2.1.5.2. Lab Measurement of Parasitic C 24

2.2. Conducted EMI Prediction and Verification 25

2.2.1. LISN Model 25

2.2.2. Noise Spectrum Calculation 25

2.2.3. Experimental Verification 27

2.3. Conducted Noise Analysis 29

2.3.1. Differential-mode Noise 29

2.3.2. Common-mode Noise 30

2.4. Noise Minimization 37

2.4.1. Sensitive Traces of Layout 37

2.4.2. Effect of ground plane spacing 42

2.4.3. Parasitic of The Magnetic Component 45

2.5. . EMI Filter Design ... 48

Chapter 3 ... 55

Thermal Analysis by Simulation ... 55

3.1. Component Power Loss Estimation ... 56

3.1.1. MOSFET Loss Calculation ... 56

3.1.2. Diode Loss ... 58

3.1.3. Rectifier Loss ... 58

3.1.4. Output Capacitor Loss Calculation ... 60

3.1.5. Inductor Loss Estimation ... 63

3.1.6. Summary of component losses for *60 w 250 kHz* PFC circuit ... 64

3.2. Thermal Modeling and Analysis ... 68

3.2.1. Model of Copper Traces ... 69

3.2.2. Device Thermal Model ... 73

3.2.2.1. Diode Model ... 74

3.2.2.2. Mosfet Model ... 77

3.2.2.3. Rectifier Model ... 77

3.2.2.4. Capacitor Model ... 77

3.2.2.5. Planar Inductor Model ... 79

3.3. Thermal Simulation Results ... 85

3.3.1. Temperature Prediction ... 85

3.3.1.1. Temperature Profile of The Board ... 85

3.3.1.2. Inductor Temperature Profile ... 88

3.3.2. Minimize Inductor Temperature Rise ... 90

3.3.2.1. Effect of Thermal Spreader ... 90

3.3.2.2. Effect of Winding Arrangement ... 93

Chapter 4 ... 98

EMI and Thermal Interaction ... 98

4.1. Layout Effect ... 98

4.1.1. The Trade offs of Component Position ... 99

4.1.2. Influence of The PAD Size ... 105

4.2. Magnetic component design 108

Chapter 5 114

Conclusions and Future Work 114

Table of Figures

Fig. 1.1. Flow chart of the integrated power supply design.. 4
Fig. 2.1. (a) Circuit diagram (b) Inductor current wave-form 7
Fig. 2.2. Hybrid circuit structure.. 8
Fig. 2.3. Rectangular shaped loop.. 9
Fig. 2.4. The interconnection traces of circuit 11
Fig. 2.5. Calculated results from *InCa*………………………………………………….. 12
Fig. 2.6 Equivalent circuit with layout inductance 12
Fig. 2.7. Equivalent circuit with layout inductance/capacitance 14
Fig. 2.8. Parasitic capacitance of trace………………………………………………….. 14
Fig. 2.9. MOSFET circuit diagram 16
Fig. 2.10 Diode circuit diagram 17
Fig. 2.11 (a) Input capacitor characteristics measurement (b) equivalent circuit for input capacitor.. 18
Fig. 2.12 Equivalent circuit for output capacitor 18
Fig. 2.13 Inductor model for EMI simulation... 19
Fig . 2.14. Planar inductor structure.. 21
Fig. 2.15. Parasitic capacitance between the conductors 22
Fig. 2.16. Voltage potential between the conductors... 22
Fig. 2.17 Impedance measurement for the planar inductor 24
Fig. 2.18. (a) Circuit model of LISN (b). EMI simulation circuit 26
Fig. 2.19 Comparison of predicted and measured EMI spectrum 28
Fig. 2.20. Input current spectrum... 31
Fig. 2.21. Differential-mode current coupled by winding capacitor............................... 31
Fig. 2. 22. Comparison of MOSFET current LISN 50-Ω voltage 32
Fig. 2. 23. Comparison of EMI noise envelope 36
Fig. 2. 24. Sensitive traces of layout.. 39
Fig. 2.25. (a) Original design (b) Modified layout design 40
Fig. 2.26. Comparison of EMI noise envelopes of the two layout designs: (a) total; (b)CM; (c) DM.. 41
Fig. 2.27 Influence of ground plane distance *d*.. 43
Fig. 2.28. EMI noises as functions of ground plane distance (a) total (b) CM (c) DM... 44
Fig. 2.29 (a) Proposed winding arrangement (b) voltage potential between the conductors of adjacent layers 46
Fig. 2.30. DM noise comparison.. 47
Fig.2.31. EMI filter structure 48
Fig. 2.32. Noise spectrum for original design... 51
Fig.2.33. Noise filter attenuation 52
Fig.2.34. Noise spectrum with the filter 54
Fig.3.1. Integration of Mosfet v(t)·i(t) in PFC circuit... 57
Fig.3.2. Integration of diode v(t)·i(t) in PFC circuit 57
Fig.3.3. Rectifier model for loss calculation.. 58

Fig.3.4. (a)Input current and rectifier bridge current (b) $\int i_{in} dt$ (c) $\int i_{in}^2 dt$ 59
Fig.3.5.Output capacitor loss 62
Fig.3.6. Conductor loss versus position (from reference 17)... 66
Fig.3.7 Component power loss of the boost PFC circuit. 67
Fig.3.8. Heat source on the copper trace... 70
Fig.3.9. Model for case I 71
Fig. 3.10. Heat source temperature versus PADs area for case I.................................... 71
Fig.3.11. Model for case II.. 72
Fig.3.12. Heat source temperature versus PADs length in case II.................................. 72
Fig. 3.13. Equivalent device model 74
Fig.3.14. (a) Diode structure (b) thermal conduction path 74
Fig.3.15. Temperature contour of diode (a) device model (b) equivalent device model.. 76
Fig. 3.16. MOSFET IRF740 with D2 packaging.. 78
Fig. 3.17. DF06 rectifier structure 78
Fig.3.18. Thermal model for ceramic cap... 78
Fig.3.19. Inductor structure... 80
Fig.3.20. Inductor model... 80
Fig.3.21. Equivalent conductivity calculation 81
Fig. 3.22. (a) Detail model (b) simplified model 83
Fig. 3.23. Inductor model for board simulation.. 84
Fig.3.24.(a) Flotherm thermal model (b) predicted temperature 86
Fig.3.25. (a) Temperature contour of substrate (b) side view... 87
Fig.3.26.(a) Inductor temperature contour (b)conductor temperature versus position..... 89
Fig.3.27. (a) Insert a thermal spreader between inductor and top enclosure (b) components temperature comparison 91
Fig.3.28. (a) case I (b) case II (c) component temperature using PCB inductor original–w/o thermal conductor; case I–with thermal conductor; case II–increase the size of thermal conductor 92
Fig.3.29. (a) winding arrangement with keep away region (b)conductor loss versus position (from reference 17) 95
Fig.3.30. (a) device temperature compared with the original design (b)inductor temperature profile (c)conductors temperature... 97
Fig.4.1. Circuit diagram... 99
Fig.4.2. Case A.. 101
Fig.4.3. Case B.. 102
Fig.4.4. Case C.. 103
Fig.4.5. (a) EMI noise comparison of the three cases (b) Component temperature comparison... 105
Fig. 4.6. Increased pads size (a) case C (b) case D... 106
Fig. 4.7. Comparison of noise envelope 107

Tables List

Table 2-1 Parasitic capacitance of traces ... 13
Table 2-2 Features of MOSFET model ... 16
Table 2-3 Features of diode model ... 17
Table 3-1 Equivalent resistance of conductors ... 65
Table 3-2 Temperature of case I and case II ... 83
Table 4-1 Integrated study for the planar inductor ... 109

CHAPTER 1

INTRODUCTION

1.1. Background and Motivation

In recent years, many of the design issues of a power supply have been intensively addressed. Issues such as power stage topology, control modeling, performance analysis, soft-switching topologies, and magnetic component optimization. However, two major issues, EMI control and thermal management have been far from adequately addressed. Cut and trial method is normally used to solve these problems.

Switch-mode power supplies generate high frequency noises because of their switching action. In the continuous effort to increase converter power density, switching frequency is becoming higher which, in general, makes EMI performance worse. The generated noises from the power stage may cause malfunction of control circuitry within the converter itself, as well as electromagnetic compatibility (EMC) problems to the surrounding equipment. EMI noises need to be controlled and minimized. A variety of EMC standards regulates conducted and radiated emission and have become more stringent in recent years.

The failure probability of electronic components depends primarily on the operating temperature. According to statistics of the U.S. military department, thermal overstressing is the cause for most of the failures in modern electronic systems [25]. To ensure proper operation, the maximum allowable temperature is usually determined for

the semiconductor device and magnetic components. In the continuous effort to decrease the volume of power converters, the switching frequency is becoming higher, and the power density of converters is higher. The increasing use of surface-mount technology, avoidance of fans to reduce noise and volume, and reduced package dimensions all intensify the thermal design requirement.

At the present time, the design practice in power supply industry is that both EMI and thermal requirements are tested at the final hardware implementation stage. A long redesign time is normally necessary if corrections are needed. A more efficient way to deal with these two issues is to tackle them in the design process, before the hardware implementation is done. It's the primary objective of this thesis to develop a methodology to deal with the issues and demonstrate the feasibility in a practical power circuit. With these tools, not only design time can be greatly reduced but also extrapolation of performance can be easily made for design optimization.

1.2. Approach

The approach used in this thesis is based on four existing simulation tools, the *InCa*, a parasitic parameter extracting software, the *Ansoft*, a Maxwell electromagnetic field simulation and parameter extraction tool, the *Saber*, a circuit simulation tool, and the *Flotherm*, a thermal analysis tool. These will be discussed in the following.

Conducted EMI simulation

Parasitic elements play major roles in the EMI performance of a power supply. Therefore, all the essential parasitic elements of the power circuit and the printed circuit board must be included to perform EMI simulation. For the discrete components such as MOSFETs and diodes, the parasitic elements can be found from the product manual. For the input and output capacitors, the parasitic elements can be measured by an Impedance Analyzer. The parasitic elements of magnetic component can be analytically calculated or practically measured. And the software *InCa* is used to extract the layout parasitic elements and generate an equivalent circuit. Both the power circuit and the layout equivalent circuit are then connected for EMI performance simulation. Software *Saber* is then used to simulate the circuit.

Thermal simulation

The first step to perform thermal simulation is to predict power losses of the various electrical components such as MOSFET, diode, inductor, and capacitors. *Saber* can be used to predict the loss of each component, and the *Maxwell Field Solver* of *Ansoft* is used to predict the loss distribution of the inductor winding. All the above information is then used by thermal performance simulation tool *Flotherm.* Thermal models are built for the circuit components. Both the system level simulation and the component level simulation can be performed.

Fig.1.1. shows the flow chats of both the conventional approach and the EMI/thermal integrated design approach. In the integrated approach, both the EMI and the thermal performance are checked early in the design process.

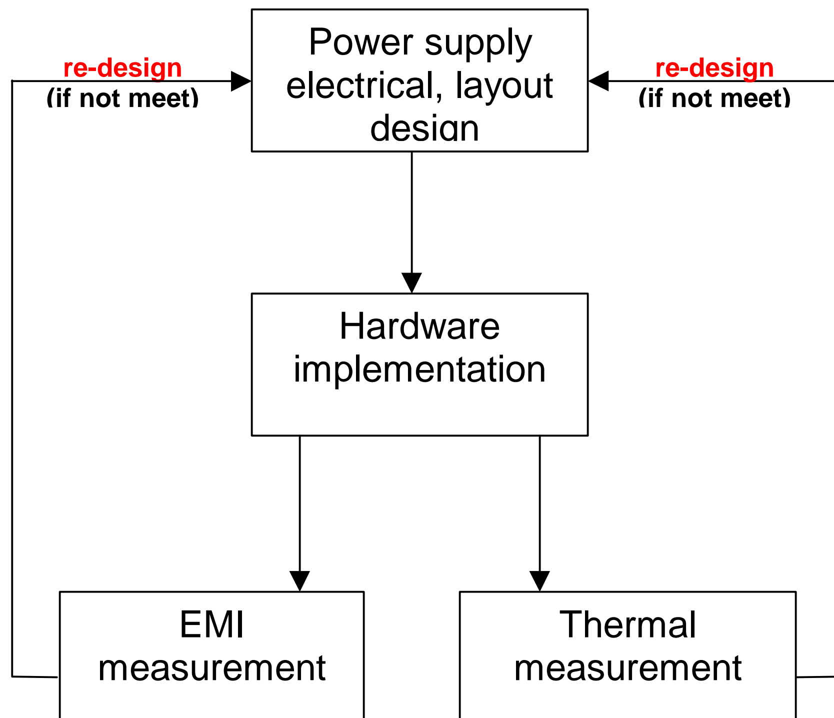
1.3. Thesis Outline

In Chapter 2, the EMI noise of a boost PFC circuit is investigated by using the above tools. The circuit EMI emissions are predicted by simulation with the equivalent circuit. Noise sources are analyzed and the circuit EMI performance is improved by suppressing the noise sources.

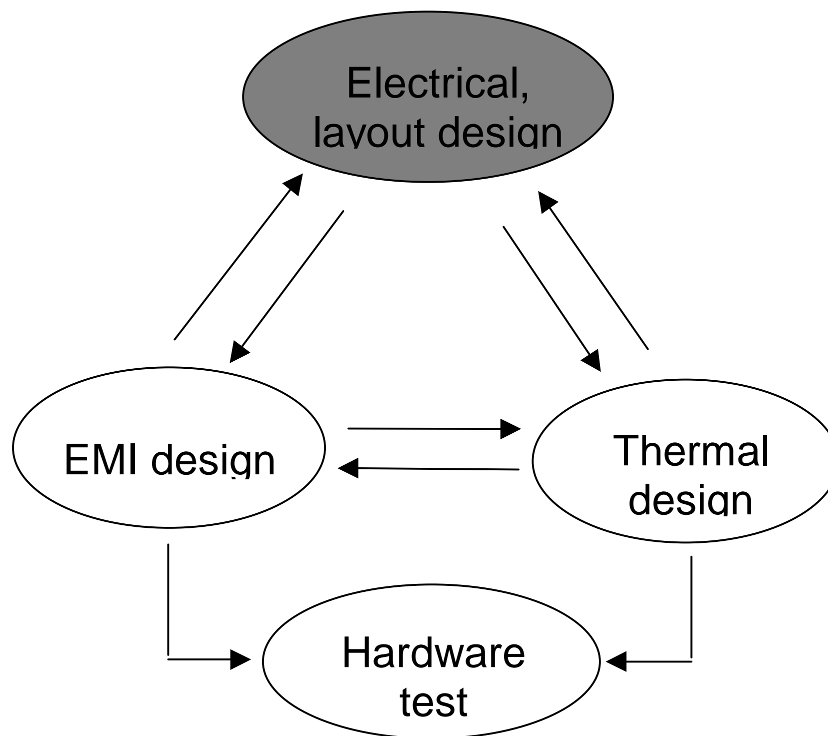
Chapter 3, the thermal performance of the circuit is simulated by using the *Flotherm.* Component losses are calculated and the thermal models are described. The thermal performance of the circuit and the internal temperature profile of a planar inductor in the circuit are predicted. Improved thermal designs are investigated.

Chpater 4, the EMI and thermal interactions are studied. Most of the time, EMI design and thermal design are trade-off. Both are difficult to quantify. By using the tools and the model developed, the tradeoffs between EMI and thermal performance can be quantitatively checked. A compromised design can be proposed based on the analysis. In this chapter, a circuit layout example and a planar inductor design example are studied from both the EMI, thermal and electrical point of views.

The conclusions in Chapter 5 with suggestions for future research.



(a) Conventional power converter design



(b) Integrated power supply design

Fig. 1.1. Flow chart of the integrated power supply design

CHAPTER TWO

EMI PREDICTION AND MINIMIZATION

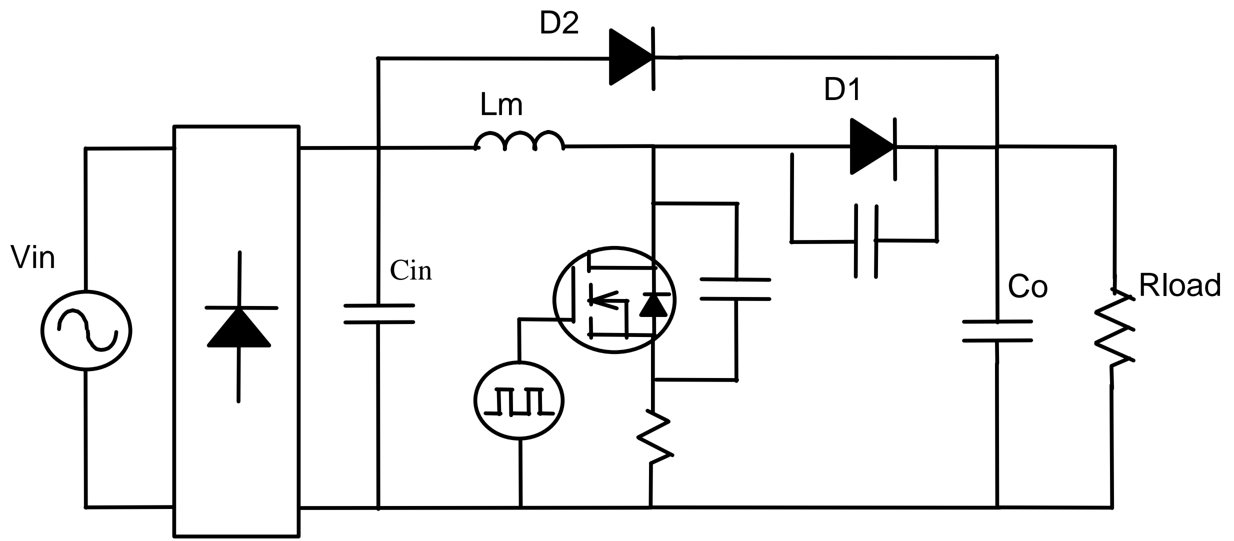
Most of the current EMI designs use experimental trial-and-error methods, which are time consuming and difficult for performance optimization. In order to optimize EMC performance, the EMI characteristics of power supplies need to be analyzed at an early design stage for a cost-effective and time-efficient design approach. Common-mode and differential-mode conducted EMI noises are related to the circuit, device packaging, circuit layout, the high *dv/dt* and *di/dt* slew rates in the power supplies. Therefore, for accurate EMI predictions and optimizations, the extraction of circuit parasitic elements is necessary.

Finite Element Analysis (FEA) has been widely used for parasitic parameter extraction. However, it is computation-extensive for complex structures and requires identification of excitation sources, which are not available without an analysis of switch-mode power supply circuit. All these obstacles contribute to the difficulty of applying FEA directly to EMI analysis for power supplies. In contrast to the FEA approach, the partial element equivalent circuit (PEEC) method determines parasitic elements by the geometrical structure of the circuit layout and packaging using simplified integral Maxwell equations [6], [7]. This not only alleviates the computation demand, but also eliminates the requirement of predetermination of EMI excitation sources.

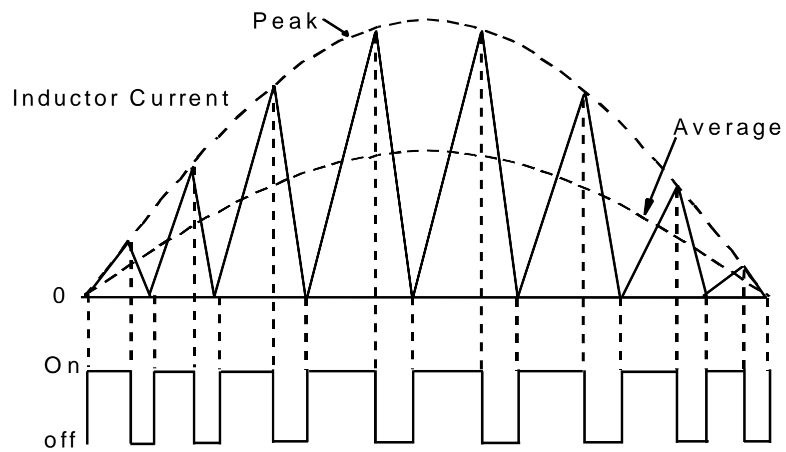
In this chapter, the conducted EMI noises of a boost PFC ballast circuit are investigated. In Section 2.1., the circuit layout modeling and device models are described. Power device models including parasitics are obtained from the *Saber* component library. Modeling of circuit layout and magnetic components are highlighted in this part. Circuit layout parasitics are obtained by using software *InCa* (*Inductance Calculation*) based on

PEEC method. In Section 2.2, the combined equivalent circuit models including power circuit and parasitics are used for EMI predictions. Common-mode, differential-mode, and total noises are analyzed. Experimental verifications are compared with the theoretical predictions. In Section 2.3, the noise sources and coupling paths are analyzed. EMI noises can be minimized by suppressing the noise sources, which is discussed in section 2.4. Design guidelines on proper PCB layout, circuit packaging and magnetic component design are given to improve EMI performance. In section 2.5, the EMI filter can be designed based on the predicted noise spectrum.

The methodology described above is used to predict a 60-W ac/dc boost rectifier Fig. 2.1(a) shows the circuit diagram. This circuit works in the discontinuous conduction mode with variable frequency control (constant on-time) to achieve power factor correction, as shown in Fig. 2.1(b). As can be seen from the key waveforms in Fig. 2.1(b), the active switch turns off at the peak of the inductor current and causes a high *di/dt* slew rate, while the rectifier turns off at zero current without diode reverse recovery problem. Also due to the switching action, the drain of the MOSFET presents a high *dv/dt* slew rate every time the switch turns on or off. All these actions contribute to EMI noise.



(a)



(b)

Fig. 2.1. .(a) Circuit diagram (b) Inductor current wave-form

2.1. Parasitic Parameter Extraction and Modeling

EMI noise is closely related to parasitic elements. To quantitatively analyze and predict the EMI noise, circuit parasitics need to be extracted. The parasitics for semiconductor devices such as Mosfet and diodes, usually can be found from the application manual. Most of the difficulties come from the parasitic of layout and the magnetic component. They are design related and have important effects on the circuit EMI.

The layout of this PFC circuit is shown as Fig. 2.2, it is a two-layer SMT structure. The top copper layer is the interconnection traces, the bottom layer is the thermal conductor, which is also electrically conductive, and between them is the dielectric layer alumina.

In this section the extraction and modeling of the layout parasitics and magnetic parasitics are discribed. Based on the information of geometry structure, the software *InCa* and *Maxwell 3D Parameter Extractor* are used to calculate these parasitic elements. The models of Mosfet and diodes come from the component library of the circuit simulation software *Saber*. Modeling of the capacitor parasitics is briefly summarized.

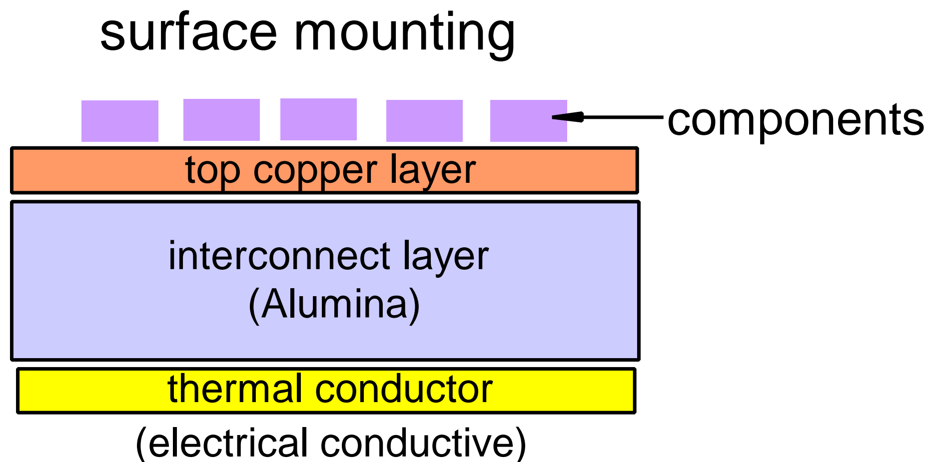


Fig. 2.2. Hybrid circuit structure

2.1.1. Layout Inductance Extraction

For a power supply circuit, during switch-on and -off the circuit topology is different, which means that the current path will change periodically during the operation of the circuit. As a result, the circuit loop inductance will change, as will the mutual inductance between the loops. Thus the partial element equivalent method should be applied to calculate the trace inductance of the layout, which ascribes a portion of global inductance to each part of the loop. The software *Inductance Calculation (InCa)* is developed based on this concept. Using the partial inductance notion, use of *InCa* will lead to an equivalent circuit model composed of localized resistors, inductance and mutual coefficients for electrical connections.

Theory of *InCa* calculation

A brief description of *InCa* parasitic extract theory is given below [6].

Considering a rectangular shaped loop carrying current I, loop inductance is defined as:

$$L_{\text{loop}} = \frac{1}{I} \oiint_{p} \vec{B} \bullet d\vec{S} \qquad (2.1)$$

where $\vec{B}$ represents magnetic induction and $d\vec{S}$ is the normal vector (normal to surface *p*).

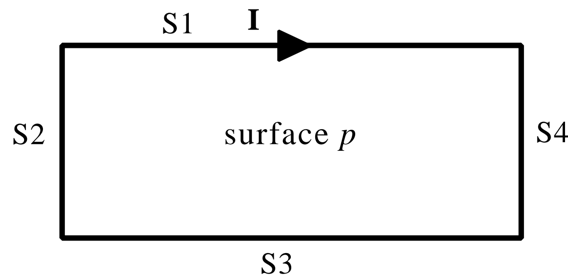


Fig. 2.3. Rectangular shaped loop

This formula can be rewritten using magnetic vector potential $\vec{A}(\vec{B} = curl\vec{A})$ and Stokes theorem as:

$$L_{\text{loop}} = \frac{1}{I}\oint_{c} \vec{A} \bullet d\vec{l} \tag{2.2}$$

Thus integration along the closed path C can be separated on the four segments forming the loop:

$$L_{\text{loop}} = \frac{1}{I}\left[\int_{S1} \vec{A} \bullet d\vec{l} + \int_{S2} \vec{A} \bullet d\vec{l} + \int_{S3} \vec{A} \bullet d\vec{l} + \int_{S4} \vec{A} \bullet d\vec{l}\right] \tag{2.3}$$

Furthermore, vector potential $\vec{A}$ can be considered the sum of each segment's contribution:

$$\vec{A} = \vec{A}_{S1} + \vec{A}_{S2} + \vec{A}_{S3} + \vec{A}_{S4} \tag{2.4}$$

Then we have,

$$L_{loop} = \frac{1}{I}\sum_{n=1}^{4}\sum_{m=1}^{4}\int_{Sn} \vec{A}_{Sm} \bullet d\vec{l} \tag{2.5}$$

Thus the partial self-inductance and mutual inductance are defined by:

$$M_{pmn} = \frac{1}{I}\int_{Sn} \vec{A}_{Sm} \bullet d\vec{l} \tag{2.6}$$

When m=n, M_{pmn} is a partial inductance. If $m \neq n$, M_{pmn} is the mutual partial inductance. And loop inductance is finally:

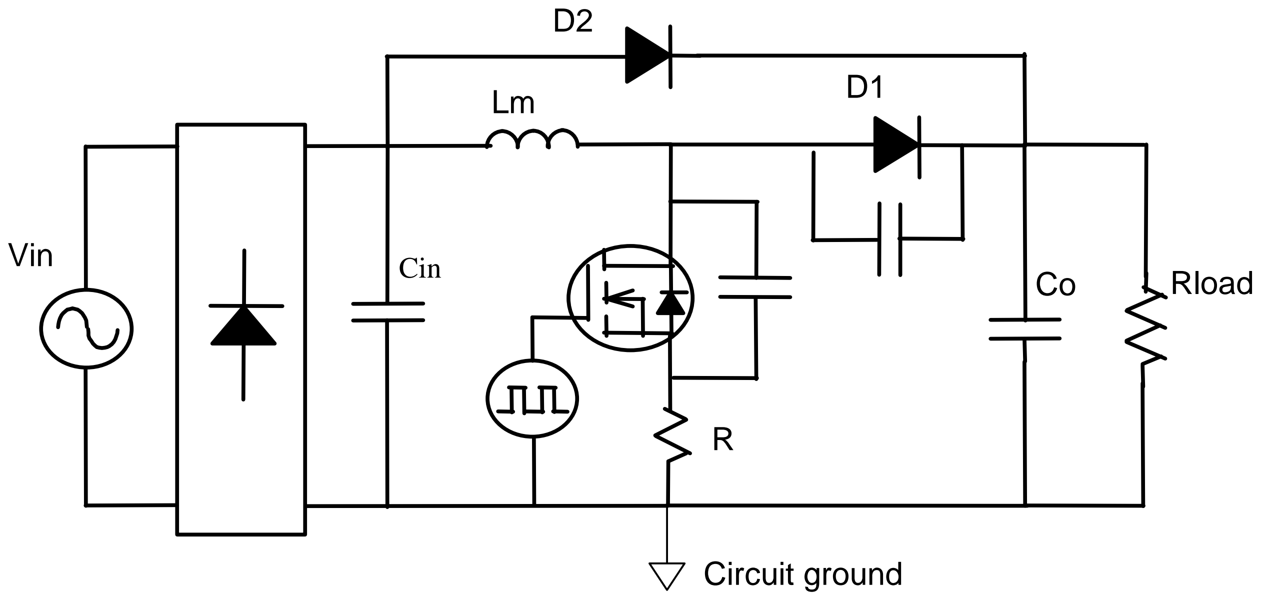
$$L_{loop} = \sum_{m=1}^{4}\sum_{n=1}^{4} M_{pmn} \tag{2.7}$$

When the switch turns on and off, the current path is changed. However, the partial inductance will not change. Based on this method, the parasitic inductance of PCB layout can be modeled. For the boost PFC circuit, the interconnection traces of the circuit and the components position is shown as Fig. 2.4.

The copper traces that have the same current are considered as one partial inductance. The influence of the used ground plane (bottom layer conductor) is taken into consideration using the image method. At high frequency, eddy current causes uneven current distribution in each trace and it is also accounted for during parasitic extraction. We get the following partial inductance matrix from *InCa*, where the diagonal elements are the self-inductance, and the off-diagonal elements are the mutual inductance.

With layout inductance included, the equivalent circuit is shown as Fig. 2.5. The equivalent layout inductance is shown with the lighter color in the diagram. There exist

mutual couplings between the inductance, the dots show the polarity of the inductance.



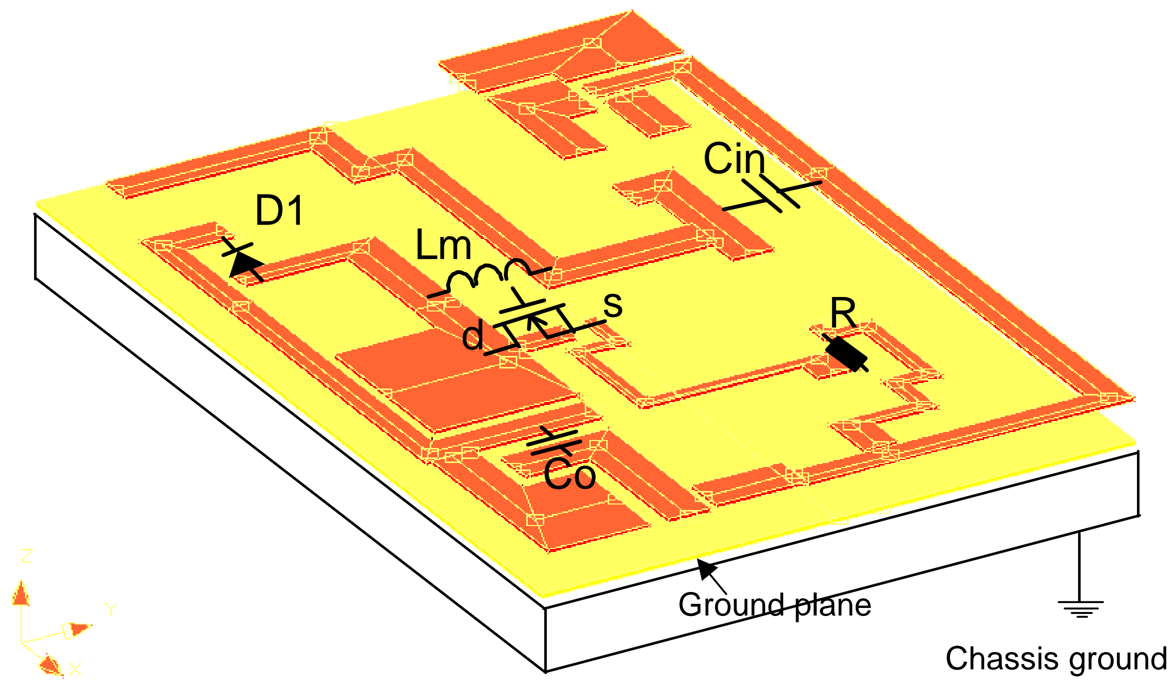


Fig.2.4 The interconnection traces of circuit

$$
L=\begin{bmatrix}
1.74e3 & -4.59 & -7.62 & -1.24 & 0.58 & 0.09 & 0.26 & 0.73 & 0.18 & 0.29 & 2 & 1.78 & 15.2 & -0.05 & 0.07 \\
 & 1.47e3 & 1.12 & 1.28 & 1.28 & -2.39 & 0.24 & 0 & -0.14 & -0.29 & 0 & 0 & 0 & 0 & 0 \\
 & & 6.53e3 & 22.5 & -4.34 & -0.26 & 4.01 & -3.75 & -0.47 & -0.59 & -4.37 & -1 & -2.77 & 0.13 & -0.31 \\
 & & & 2.85e3 & -58.9 & -0.51 & 4.27 & -8.7 & -0.45 & -0.52 & -2.59 & -0.38 & -0.65 & 0.14 & -0.59 \\
 & & & & 1.15e3 & -8.19 & 1.51 & 8.77 & -0.16 & -3.13 & 15.3 & 0.73 & 1.01 & 0.76 & -41.4 \\
 & & & & & 0.616e3 & -0.09 & 0 & 0.17 & 0.53 & -24.9 & -0.06 & -0.2 & -0.31 & 2.44 \\
 & & & & & & 2.41e3 & 80.9 & 0.21 & 0.13 & 0.51 & 0.19 & 0.36 & 0.05 & -0.14 \\
 & & & & & & & 4.62e3 & 24.2 & 3.1 & 4.87 & 0.92 & 1.07 & 0 & 0 \\
 & & & & & & & & 1.5e3 & 34 & 2.94 & 0.39 & 0.03 & -3.74 & 5.61 \\
 & & & & & & & & & 2.26e3 & 8.7 & 1.92 & 0.49 & -2.8 & 54.6 \\
 & & & & & & & & & & 6.9e3 & 26.1 & 0.95 & -5.05 & 7.56 \\
 & & & & & & & & & & & 5.48e3 & 64 & 11.6 & -0.44 \\
 & & & & & & & & & & & & 9.08e3 & 81.4 & -0.72 \\
 & & & & & & & & & & & & & 2.12 & -2.48 \\
 & & & & & & & & & & & & & & 1.84
\end{bmatrix} pH
$$

(Columns, left to right: L3 L4 L5 L6 L7 L8 L9 L10 L11 L12 L13 L14 L16 L17 L18)

Fig.2.5 Calculated results from *InCa*

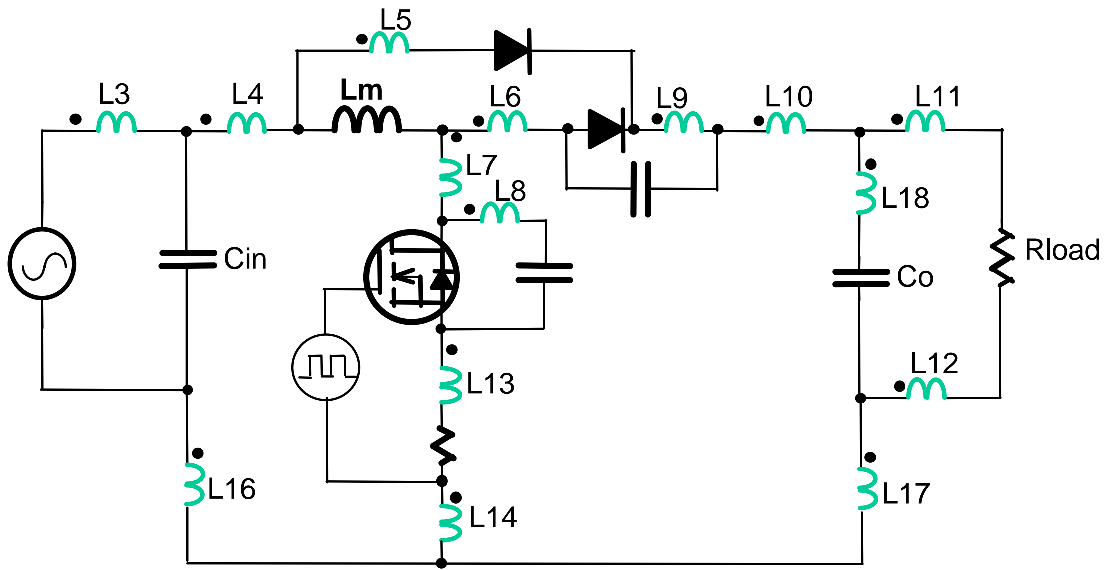


Fig.2.6 Equivalent circuit with layout inductance

2.1.2. Parasitic Capacitance Calculation

Common-mode noise is directly related to stray capacitance. In this circuit when Mosfet turns on and off, the drain of Mosfet and the Anode of diode will see a large *dv/dt*. Since the Mosfet is mounted flat on the board, the major common-mode capacitance comes from the capacitance between the Mosfet drain and ground plane, and that between the ground plane and the traces connected with Mosfet drain. To predict the conducted emission levels, we need to find the values of these parasitic elements. The software based on FEA methods – *Maxwell 3D Parameter Extractor* from *Ansoft*, provides the tools for parasitic capacitance calculation.

After defining the geometric model, materials, and the electromagnetic sources, all the parasitic capacitance between the traces and the ground plane can be calculated. Only the value for the traces connected with Mosfet drain are important for the common-mode noise. The data in table 2-1 is obtained with *Maxwell 3D parameter extractor*, in which heat-sink refers to the bottom layer of circuit.

Table 2-1

	MOS	drain2	drain3	drain4
heat-sink	8.6pF	2.7pF	4.7pF	1.8pF

The lumped model in Fig. 2.7 is obtained by combining the calculated partial capacitance and inductance elements.

Where, $Cp = \mathrm{C}drain2 + \mathrm{C}drain3 + \mathrm{C}drain4 + \mathrm{C}mos = 17.8(pF)$

2.1.3. Power Device Models

The switching characteristics of a power device such as Mosfet or diode is critical for determining the circuit *di/dt* and *dv/dt* slew rate when Mosfet turns on or off. Therefore power device models are important for EMI noise prediction. The device models from the *Saber* component library are used for Mosfet and diode.

The assessment of a power MOSFET model is based on its ability to accurately reproduce the switching of the device. The critical factors determining the switching

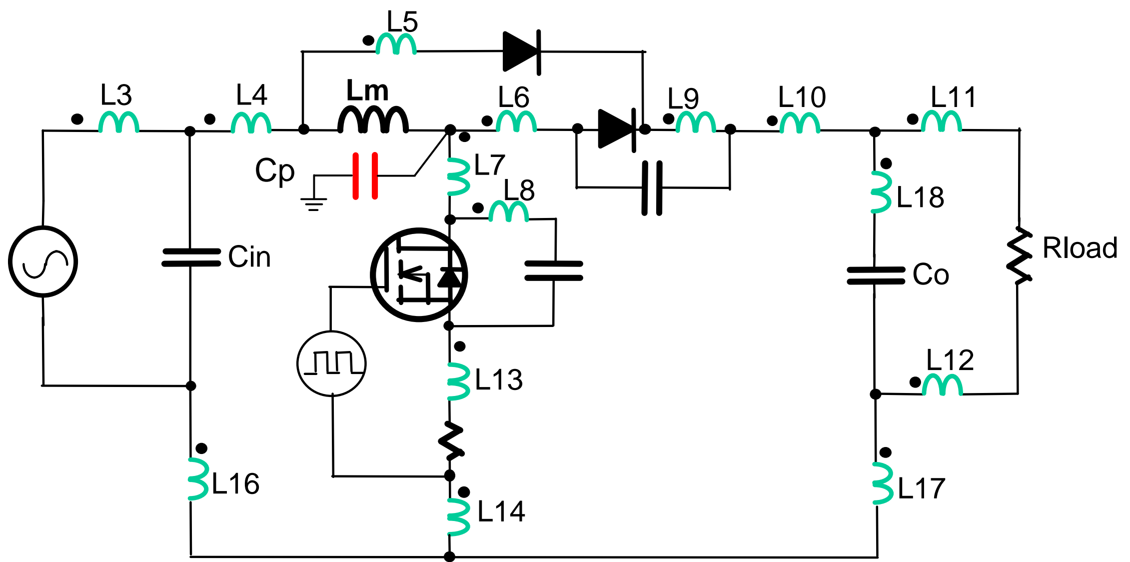


Fig. 2.7. Equivalent circuit with layout inductance/capacitance

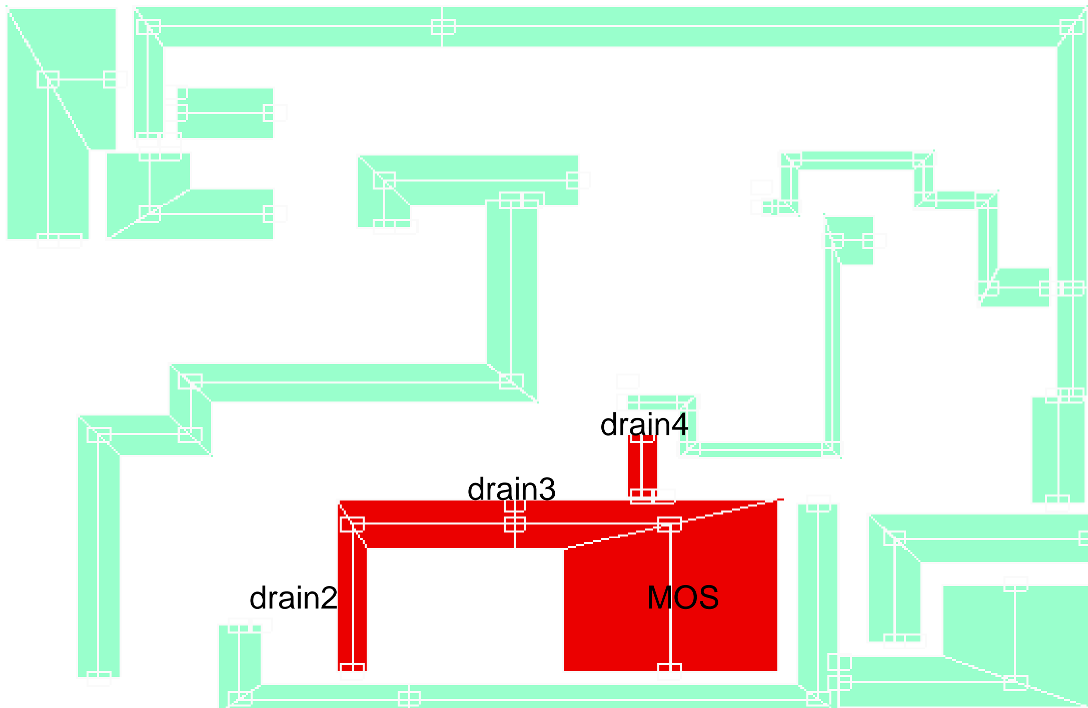


Fig. 2.8 Parasitic capacitance of trace

behavior of a power MOSFET include the drain-gate (Miller) capacitor which varies with the drain-gate voltage, the body-drain diode, and package inductance, which are important elements for power MOSFET switching due to the high di/dt values involved.

The power MOSFET model in the *Saber* component library incorporates variable parasitics from gate-to-drain, normal MOSFET parameters, along with external parasitics unique to power devices. Parameters are grouped into four structures: mmodel (the MOSFET), dmodel (the body diode), cmodel (the nonlinear capacitors) and cktmodel (the parasitic components in the netlist, including: cgs, cgd, rg, ld, ls, rd, rs, etc.). The limitation and features of the *Saber* MOSFET model are summarized Table 2.1 [13]. The model is shown in Fig. 2.9.

Diode switching performance, reverse recovery characteristics and other features are important to EMI behavior. The circuit models for diode is summarized in Fig. 2.10. The features and limitations of the *Saber* model are summarized in Table 2.2. [13].

2.1.4 . Passive Components Model

The passive components as input and output capacitors are used to shunt high frequency ripple at input current and absorb the voltage ripple at output. At a high frequency, due to its ESR and ESL, the effectiveness of the capacitor will be attenuated.

To quantify the circuit EMI, the parasitics of input and output capacitors need to be extracted. The *Hp4195A Impedance Analyzer* can be used for this purpose. Fig. 2.11(a) shows the measured magnitude and phase of input capacitor versus frequency. *Cin* is a Multi-layer ceramic capacitor. We see that the resonant frequency for this capacitor is about 3 MHz. Beyond this frequency the impedance of the capacitor will increase with frequency, exhibiting the effect of the ESL. By choosing the circuit model in Fig. 2.11(b), ESR and ESL can be found by the equipment. We see that the characteristics of an equivalent model, which is shown with the dotted line, match very well with the measurement.

In the same way, the equivalent circuit for the output capacitor can be found. The diagram and the value of an output capacitor model is shown in Fig. 2.12.

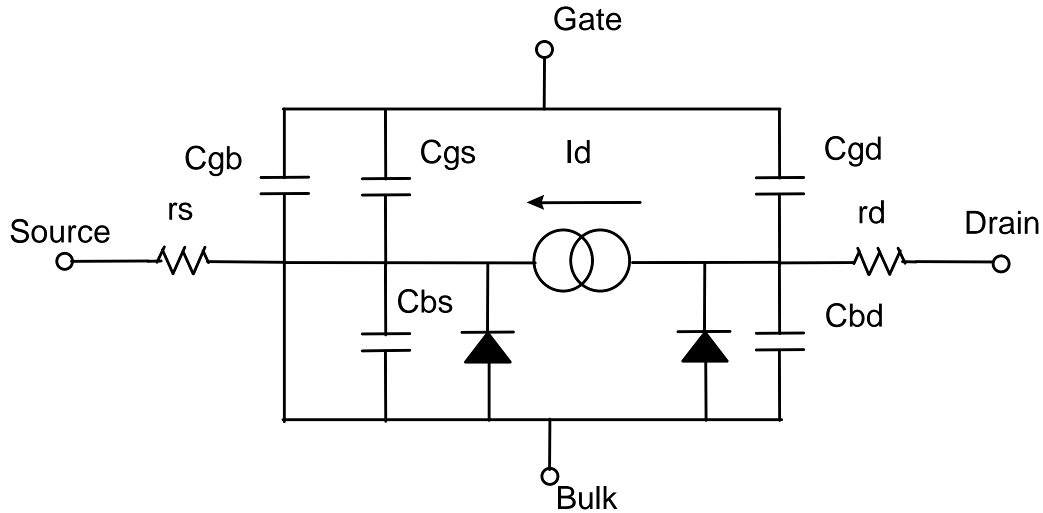


Fig. 2.9. MOSFET circuit diagram

Table-2.2 Features of the Mosfet model

Power MOSFET features included	*Features that are not included*
transconductance as a function of gate voltage	conductivity modulated drain resistance
sub_threshhold region	self-heating effect
linear region of operation	failure effects
saturation region of operation	noise
body diode DC characteristics	
body diode reverse recovery time	
Cds, Cgs, Cgd as a function of bias voltage	
lead inductance on drain, source, gate	
low, typical, high parameters values	
temperature effects	
drain source breakdown	
absolute limits	

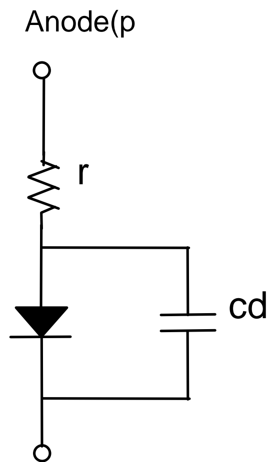
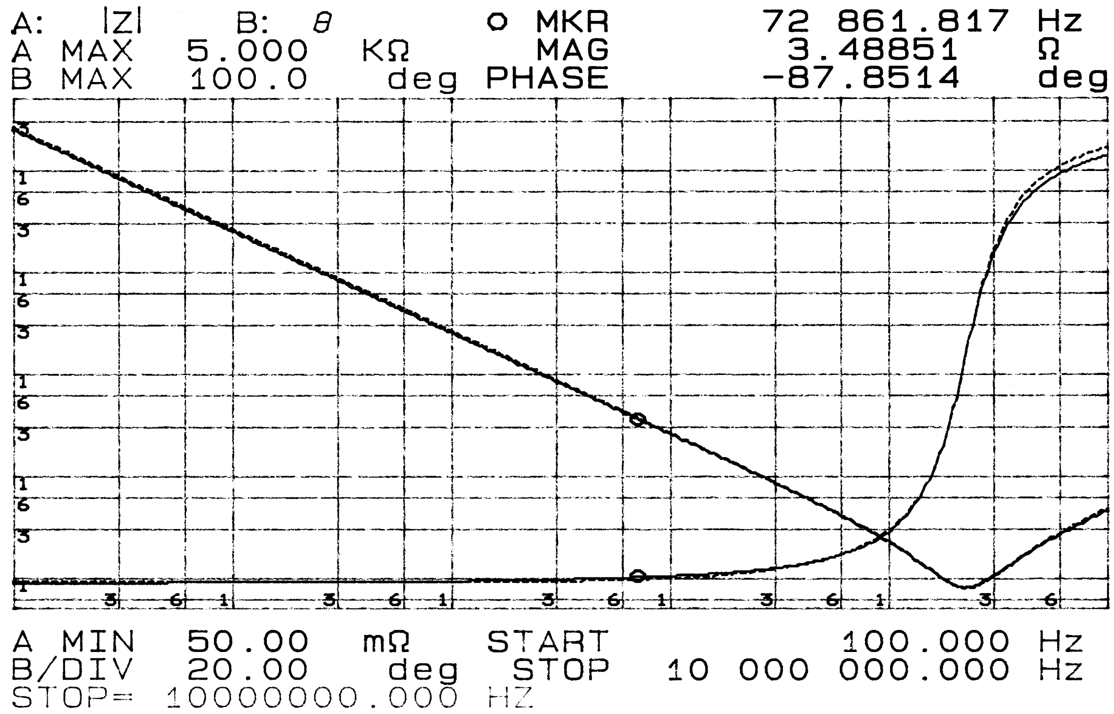


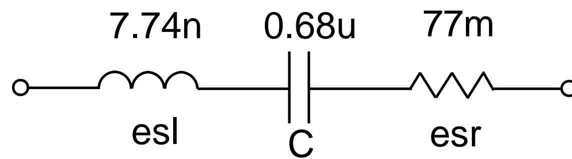
Fig. 2.10 Diode circuit diagram

Table-2.3 Features of the diode model

Diode features included	*Features that are not included*
foward diode voltage as a function of current	self_heating effects
reverse diode voltage as a function of current	absolute limits (SOA)
junction capacitance as function of bias voltage	failure effects
low, typical, high parameter values	noise
temperature effects	
reverse breakdown	



(a)



(b)

Fig.2.11 (a) Input capacitor characteristics measurement (b) equivalent circuit for input capacitor

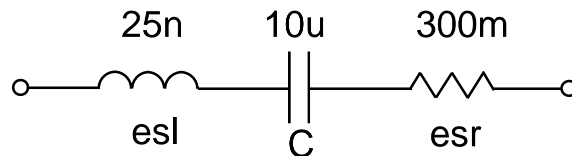


Fig.2.12 Equivalent circuit for output capacitor

2.1.5 . Magnetic Components Model

The winding capacitance of the inductor plays an important role for circuit EMI performance. As the switching frequency becomes higher, the effect of winding capacitance becomes more important. In this section, an analytical method of estimating the capacitance is given. And the analytical result is verified with a real measurement.

2.1.5.1. Analytical Estimation of Winding Capacitance

To improve circuit EMC performance, the magnetic design needs to be optimized to reduce parasitic effect. The one cell model shown in Fig. 2.13 is used for EMI simulation, in which the inductor is in parallel with a capacitor. In this section we expect to find a closed-form solution for the winding capacitance *Cp*. Then the EMI prediction and minimization can be implemented at the design stage without hardware implementation. Design guidelines of better EMC performance for the planar inductor will be determined.

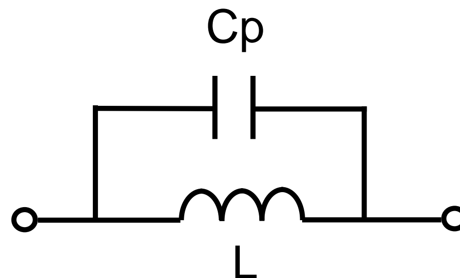


Fig.2.13. Inductor model for EMI simulation

The structure of the planar inductor is shown in Fig. 2.14. It is a nine-layer structure, and there are 27 turns in total. Each layer has 3 turns. The arrangement of winding is shown in Fig. 2.14(a). Fig. 2.14(b) is the top view.The equivalent winding capacitance is found by calculating the capacitive energy stored within the inductor. Two steps are needed to find the capacitive energy of the planar inductor. First, the parasitic

capacitance between the conducts is calculated. Second, the voltage potential between the conductors needs to be determined.

The dimension of inductor winding layers is shown in Fig. 2.15. Two kinds of parasitic capacitance are shown in Fig. 2.15, one is the *Y* direction capacitance *C1*, and the other is the *X* direction capacitance *C2*. We can see that *C2<<C1,* therefore it is assumed that omitting the capacitance in the *X* direction will not make big difference for energy calculation.

The parasitic capacitance *C1* is estimated by Eq. (2.9).

$$C1 = \frac{\varepsilon_r \varepsilon_0 \cdot A}{d} = \frac{\varepsilon_r \varepsilon_0 \cdot w \cdot l}{d} \qquad (2.\ 9)$$

where ,

ε_o : permitivity of free air *8.854e-12 F/m*

ε_r: relative permitivity of polyamide, which is *4.9*

w: width of the conductor, *1.0 mm*

l: the length of the conductor per turn, which is *7.0 cm*

d: thickness of the dielectric, *0.0762mm*

A: average surface area per turn

We have *C1=41.7(pF).*

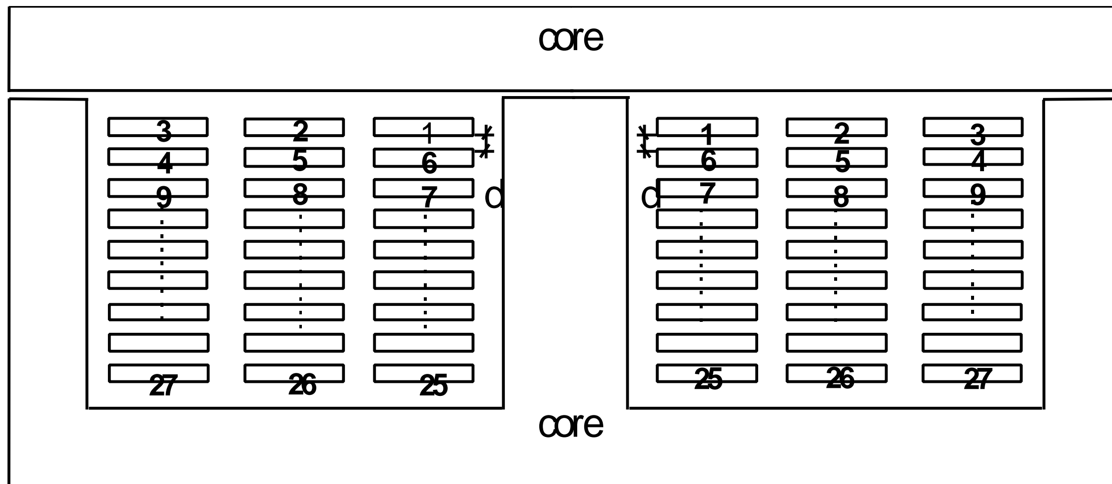
The next step is to calculate the voltage potential between the conductors at *Y* direction. The voltage on each turn is first calculated, then the voltage difference between the conductors can be computed.

To illustrate the process, the voltage potential between the conductors is shown in Fig. 2.16 for turns 1~9. *Vt* is the voltage drop on each turn. It is seen that the voltage difference between the conductors at the adjacent layers remains the same (e.g. 1 & 6, 2 & 5, 3 & 4, …). However, the value is different for the conductor pairs at different positions, which is also shown in Fig. 2.16.

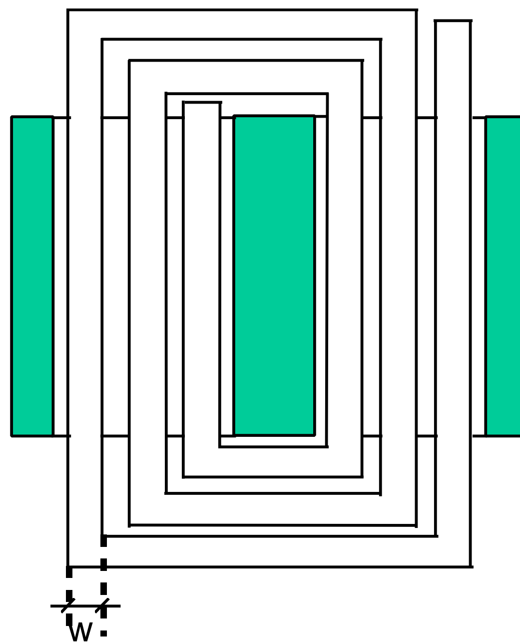
The total capacitive energy stored within the inductor is calculated by summarizing all the energy stored in *C1* capacitance, which is calculated as Eq.(2.10):

$$P_C = \frac{(m-1)}{2} \cdot (C_1 V_1^2 + C_1 V_2^2 + C_1 V_3^2) \qquad (2.10)$$

We have:



(a) Front view



(b) Top view

Fig.2.14. Planar inductor structure

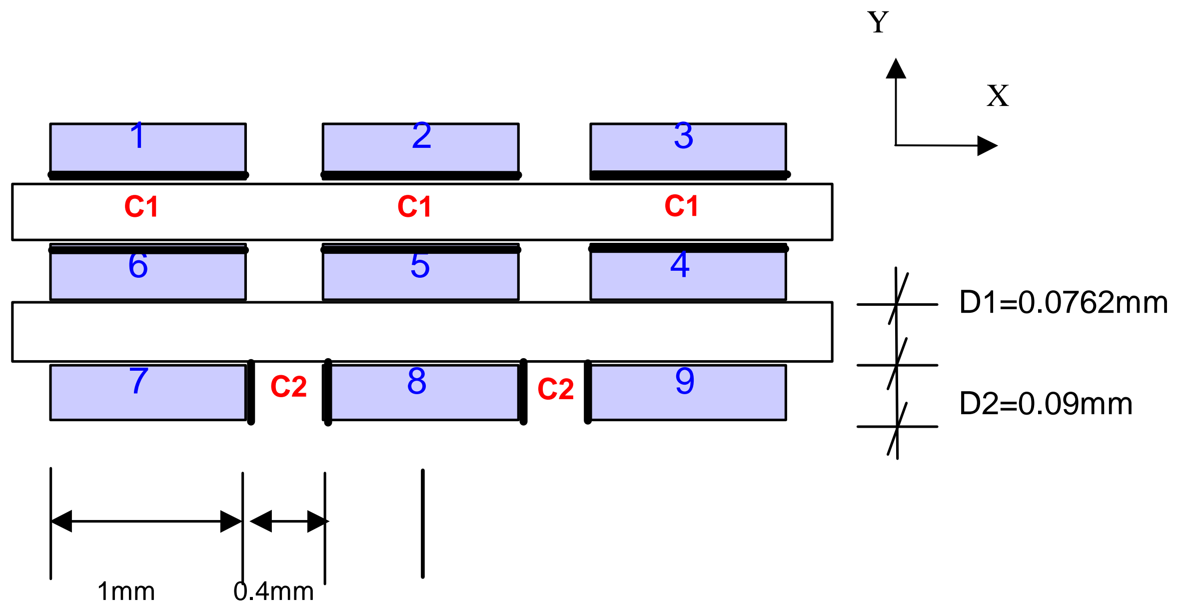


Fig. 2.15. Parasitic capacitance between the conductors

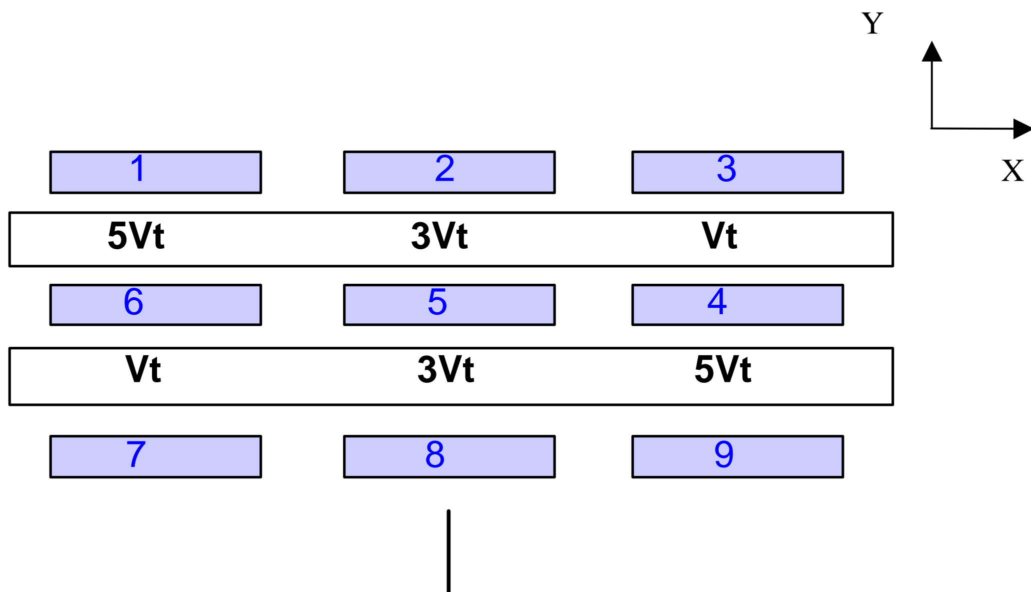


Fig. 2.16. Voltage potential between the conductors

$$V_1 = Vt \tag{2.11}$$

$$V_2 = 3Vt \tag{2.12}$$

$$V_3 = 5Vt \tag{2.13}$$

$$Vt = \frac{V}{n} \tag{2.14}$$

where,

C1:	parasitic capacitance between two turns of adjacent layers
V:	inductor voltage
Vt:	voltage drop per turn
n:	number of turns
m:	number of layers
V1, V2, V3:	voltage difference between the conductor pairs

Substitute (2.11)~(2.14) into (2.10), we have the total energy as Eq. (2.15). This value should be equal to the energy stored in the equivalent capacitor *Cp* in Fig. 2.13. Thus we have Eq. (2.16), and the equivalent capacitor *Cp* is calculated as Eq.(2.17).

$$P_C = \frac{(m-1)}{2n^2} \cdot (1^2 + 3^2 + 5^2) \cdot C_1 V^2 \tag{2.15}$$

$$\frac{1}{2} Cp \cdot V^2 = \frac{(m-1)}{2n^2} \cdot (1^2 + 3^2 + 5^2) \quad C_1 V^2 \tag{2.16}$$

$$Cp = \frac{(m-1)}{n^2} \cdot (1^2 + 3^2 + 5^2) \cdot C_1 \tag{2.17}$$

We have

$$Cp = \frac{8}{27^2} \cdot (1^2 + 3^2 + 5^2) \cdot C_1$$

Thus,

$$Cp = 16 \ (pF)$$

The resonant frequency of inductor can be calculated as Eq. (2.18).

$$f_o = \frac{1}{2\text{p}\sqrt{LC_{eq}}} = \frac{1}{2\text{p}\sqrt{170 \times 16 \times 10^{-18}}} = 3.05 MHz \tag{2.18}$$

2.1.5.2. Lab Measurement of Parasitic C

The impedance characteristics of the planar inductor can be measured by *Hp4195A Impedance Analyzer*. Measurement results for the boost inductor is shown in Fig. 2.17. Within the conductive frequency range *100k~30MHz*, only one resonant frequency is noticed at *2.94MHz*. Therefore the one cell model shown in Fig. 2.13 is reasonable. The resonant frequency is as Eq. (2.8). The measured value for the winding capacitance is *Cp=18.6 pF,* and the resonant frequency is *2.94 MHz.* We can see that the analytical predictions match very well with the lab measurement.

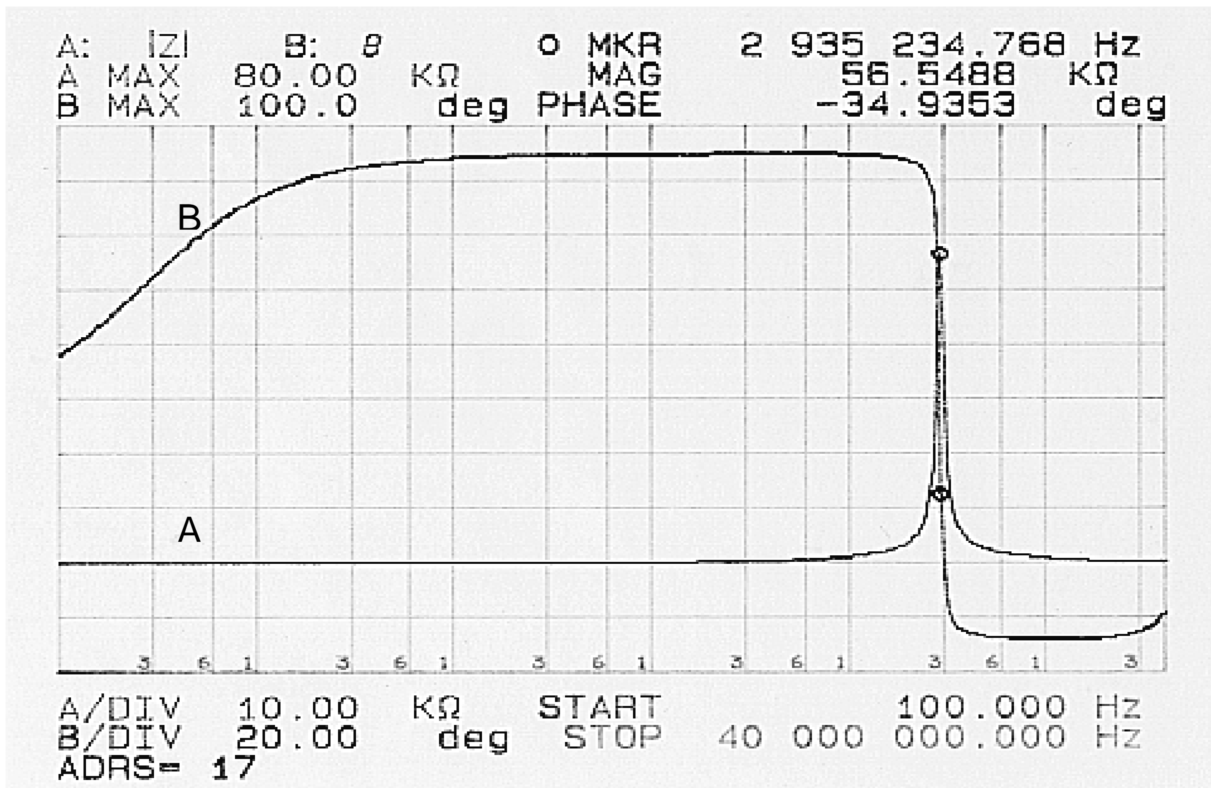


Fig.2.17 Impedance measurement for the planar inductor

2.2. Conducted EMI Prediction and Verification

With all the components and layout parasitics extracted, the equivalent circuit model can be built for EMI simulation. In this section the effort on noise extraction and separation, and noise spectrum calculation is presented. The predicted noise is compared with measurement results.

2.2.1. LISN Model

To comply with EMI test regulations, a Line Impedance Stabilization Network (LISN) is inserted between the input source and the power converter. LISN represents a standard power line impedance to the Equipment Under Test (EUT), and isolates the supply generated noise form the EUT at the same time. The LISN model is shown in Fig. 2.18.

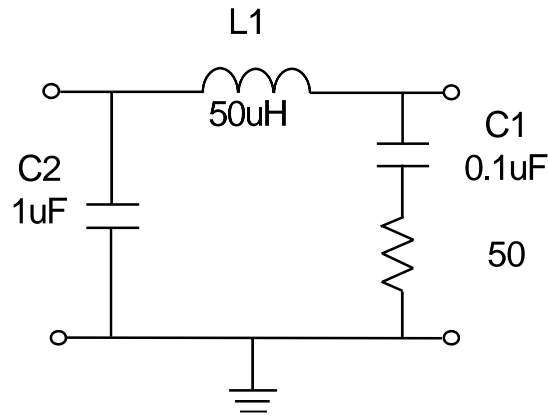
By applying the circuit simulation tool *Saber*, EMI noise can be examined on the 50Ω resistor. Differential-mode and common-mode noises are calculated according to Eq. (2.19) and (2.20). *Vn1* and *Vn2* are as shown in Fig. 2.9.

$$V_{CM} = \frac{V_{n1} + V_{n2}}{2} \tag{2.19}$$

$$V_{DM} = \frac{V_{n1} - V_{n2}}{2} \tag{2.20}$$

2.2.2. Noise Spectrum Calculation

Using the FFT (Fast Fourie Transform) function in *Saber*, the noise spectrum can be found from the time domain signal. To comply with EMI regulations, the Resolution Bandwidth (RBW) needs to be specified. According to the FCC, the RBW of spectrum analyzer is set at *200 Hz* for noise frequency less than *150 kHz*. If the noise frequency is between *150 kHz* and *30 MHz*, the RBW should be set at *9 kHz*. RBW will make a difference for measurements of narrow-band and broadband noise signals. For a broadband signal, as RBW is widened, more of the spectral lines which are close together in frequency will be included in the RBW envelope. Thus, the displayed signal level will increase. For single frequency narrow-band source, because only one frequency is measured in the envelope, the signal level will not change much with respect to different RBWs.



(a)

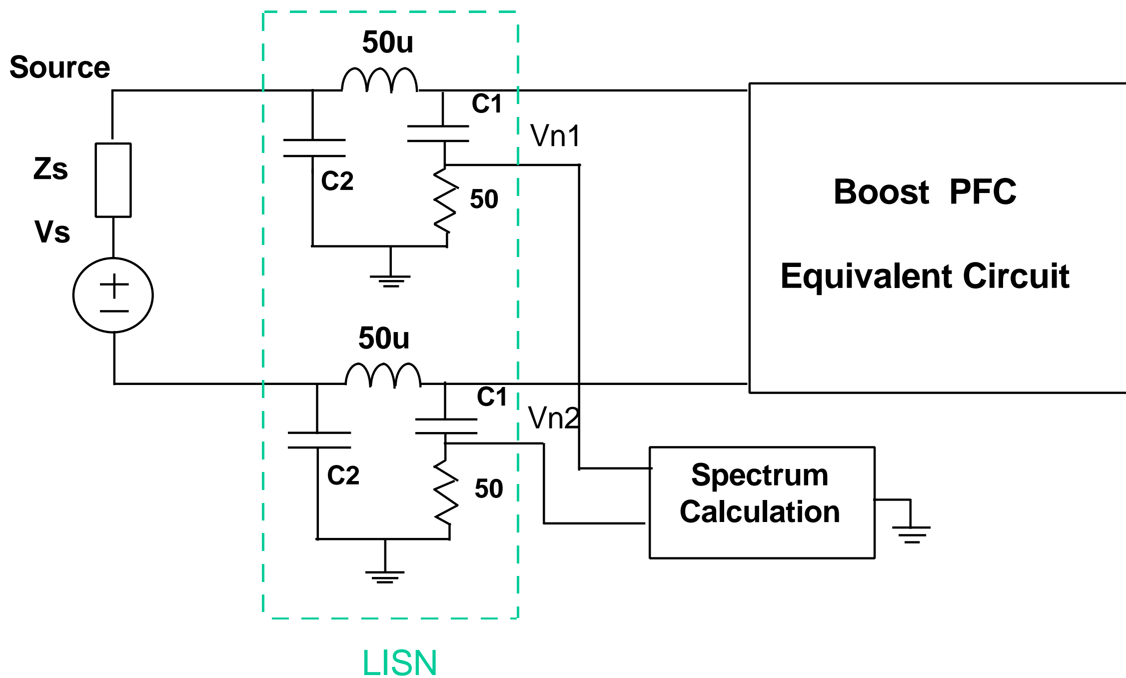


Fig.2.18. (a) Circuit model of LISN (b). EMI simulation circuit

The following steps should by followed when performing FFT analysis. For the background knowledge please refer to the theory of Discrete Fourie Transform.

Step 1: Determine the required length of time domain signal T, which is given by RBW and the windowing function used.

$$T = \frac{k}{f_{RBW}} \tag{2.21}$$

where, f_{RBW} - Resolution Bandwidth of FFT

k - constant corresponding to windowing function, which determines the *3dB* bandwidth of main band.

($k=0.89$ for Rectangular window, $k=1.3$ for Hamming window)

Step 2: Calculate the number of sampling points N.

$$N = 2^r \geq f_s \cdot T \tag{2.22}$$

$$f_s \geq 2 f_{max} \tag{2.23}$$

Where, r – integer 0,1,2, …

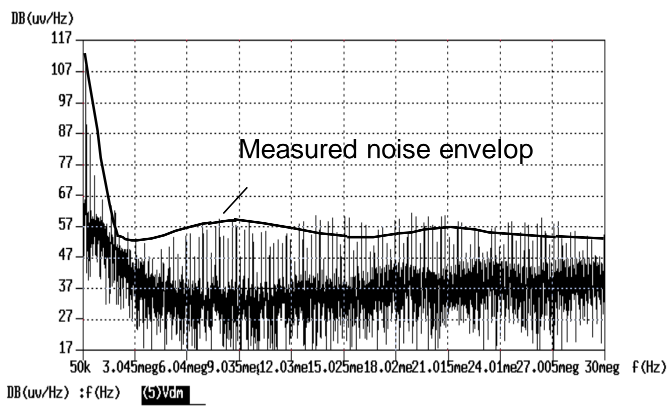
f_s – sampling frequency

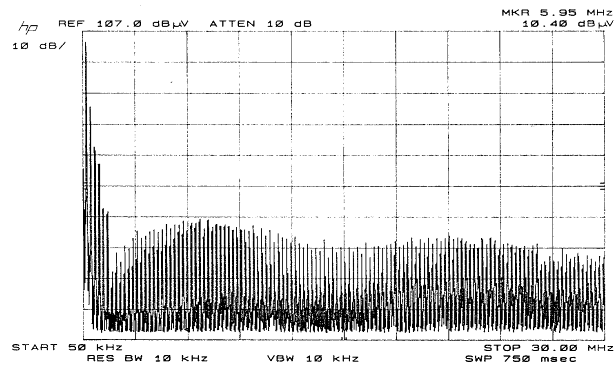
f_{max} – maximum frequency of FFT, which is *30MHz*

Equation (2.23) is based on the sampling theory that, to avoid distortion of the frequency spectrum, the sampling frequency should be two times greater than the highest frequency in the original signal.

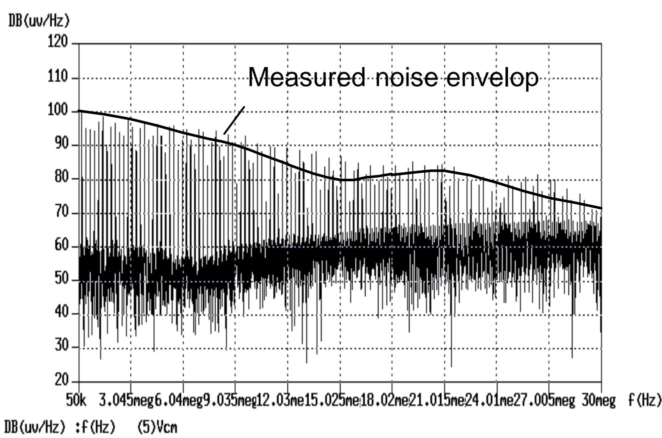
2.2.3. Experimental Verification

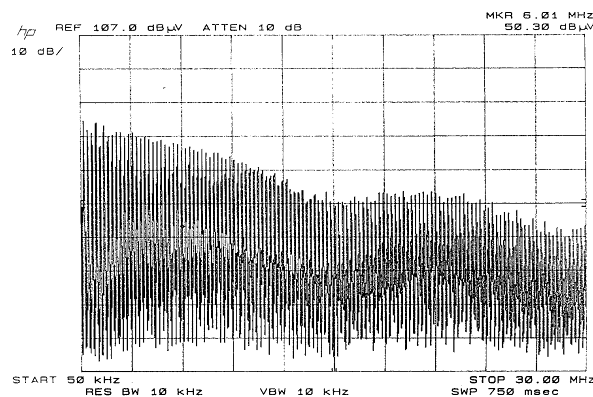
The EMI prediction model was simulated by using the circuit simulator *Saber*. The conducted EMI measurement was taken in compliance with EMI regulations, using a noise separator to distinguish the differential-mode (DM) and common-mode (CM) noises. The comparisons of the predicted and experimental EMI noises are shown in Fig. 2.19, for DM, CM, and total noises. Due to the attenuation of DM and CM noise separators, the measured DM values in Fig. 2.19(a) are 10 dB below the actual values, while the measured CM values are 13 dB attenuated from the actual values. It can be seen that simulation and measurement agree very well both in dB values and the envelope shapes.



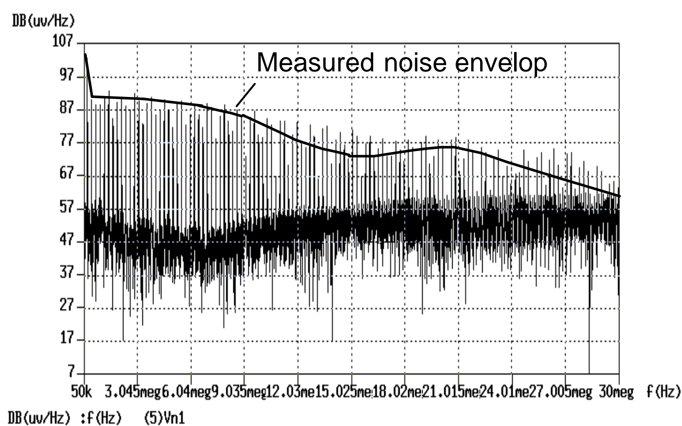


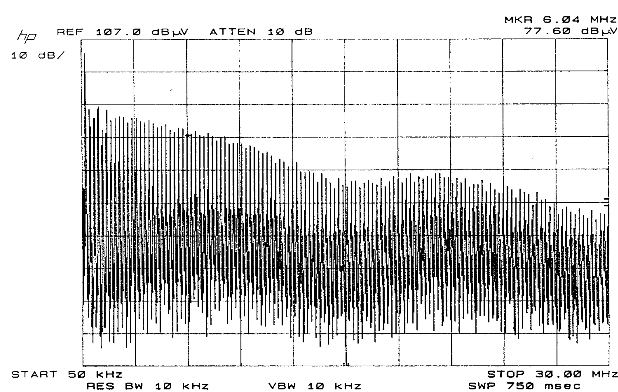
(a) DM noise spectrum





(b) CM noise spectrum





(c) total noise spectrum

Fig. 2.19. Comparison of predicted and measured noise spectrum: (a) DM; (b) CM; (c) total. The predictions are on the left with the measurements on the right

2.3. Conducted Noise Analysis

Conventional efforts on EMI reduction focus on the EMI filter design to meet the EMI regulation requirement. However, a more thorough solution to minimize EMI noise is to suppress the noise sources thorough proper circuit layout and packaging. This not only minimizes the generated noises from the power supply, but also alleviates the attenuation requirement on the EMI filter, and thus can potentially meet the EMI regulation with a smaller EMI filter. Therefore knowledge of the noise source and coupling paths are necessary. Fig. 2.20 shows the circuit diagram for the power factor correction (PFC) circuit under investigation.

EMI noise source of the boost circuit is analyzed in this section. Then in Section 2.4., the circuit layout and component design are modified to reduce the EMI emission. Thus the circuit's EMC performance can be improved.

2.3.1. Differential-mode Noise

The input ripple current generates DM noises. The large ripple current due to DCM operation is shown in Fig. 2.20, together with its frequency spectrum. Ideally, the input capacitor *Cin* shunts most of the high frequency components of the input current to ground. However, due to its ESR and ESL, the effectiveness of absorbing the ripple current is reduced at high frequency. Thus, it is desirable to have a high-performance (low ESL and low ESR) input capacitor.

Due to the winding capacitance of the boost inductor, and the large *dv/dt* at MOSFET turn-on and -off transient, the charge and discharge current will be coupled into the input as a differential mode current, where $i = C_w \frac{dv}{dt}$. The equivalent circuit is shown as Fig. 2.21. The input voltage is a low frequency signal, and during MOSFET on and off, it can be regarded as a constant voltage. Vd is the MOSFET drain voltage, and Vo is the output voltage.

Large *di/dt* will appear in the circuit during MOSFET turn-on and -off. By means of the layout inductance, the large *di/dt* will introduce further differential-mode noise. For

IRF740, the current rise and fall time is about *25n*s, peak current is about *2A*, and the current slew rate is about *8 ´*10^{6} *A/s.*

Fig. 2.22. shows the simulated time domain waveforms of the MOSFET current *i(t)* and the voltage across the 50Ω resistor of LISN *v(t)* for two different equivalent circuit models: (a) without parasitic elements of boost inductor and layout; (b) parasitic elements of the boost inductor and circuit layout is included with *(a).* The initial current peaking is caused by discharge of the MOSFET output capacitor at the switch turn-on moment. In Fig. 2.22(a), it is seen that the noise voltage across the 50Ω resistor is very clear although there is spike and ringing on the MOFET current during switch turn-on and -off. However, after the parasitic elements are included, the high frequency glitches are seen on the 50Ω resistor, as shown in Fig. 2.22(b).

To illustrate the individual contributions of all these parasitic elements on differential mode noises, the DM noise spectrum are compared in Fig. 2.23 for the followed four cases. (a) without parasitic elements of boost inductor and layout; (b) layout parasitic inductance are included, (c) winding capacitance of the boost inductor is included, (d) common-mode capacitance is included.

As can be seen form the comparison, the switched ripple current is responsible for the low frequency components in the DM noise signal. And the high frequency DM noises are coupled by means of the layout inductance and inductor winding capacitance. The DM noise is further increased when the common-mode capacitance is included, which is due to the unbalance of common-mode current.

2.3.2. Common-mode Noise

Common-mode noise is determined by the voltage slew rate *dv/dt* and the amount of common-mode parasitic capacitance. The high spikes in the *v(t)* waveform at the switch turn-on and off moments are caused by the large *dv/dt* slew rates. The boost converter under study is common-mode dominant. Therefore, in order to suppress the total EMI noise to meet EMI regulations, design optimization should focus on the common-mode noise, which will be illustrated in the next section.

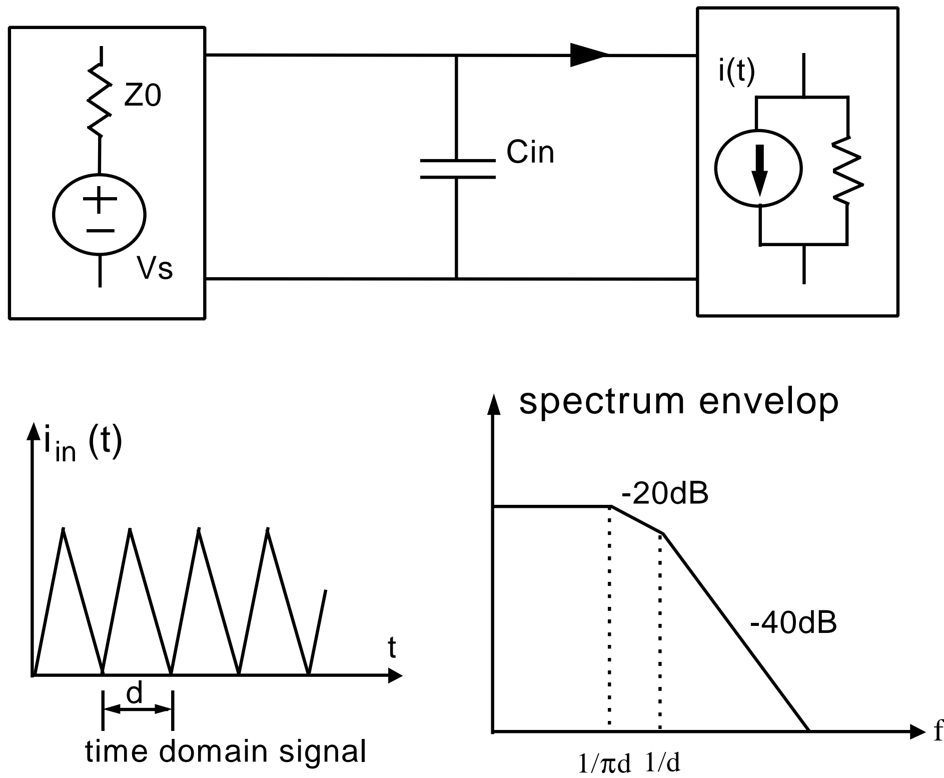


Fig. 2.20. Input current spectrum.

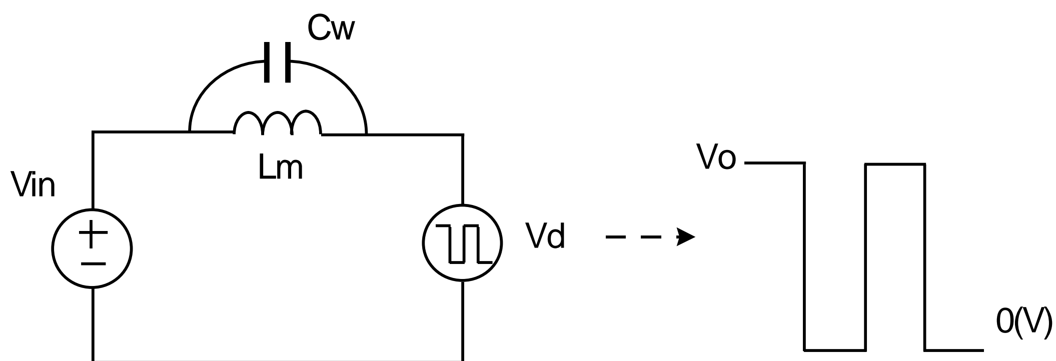
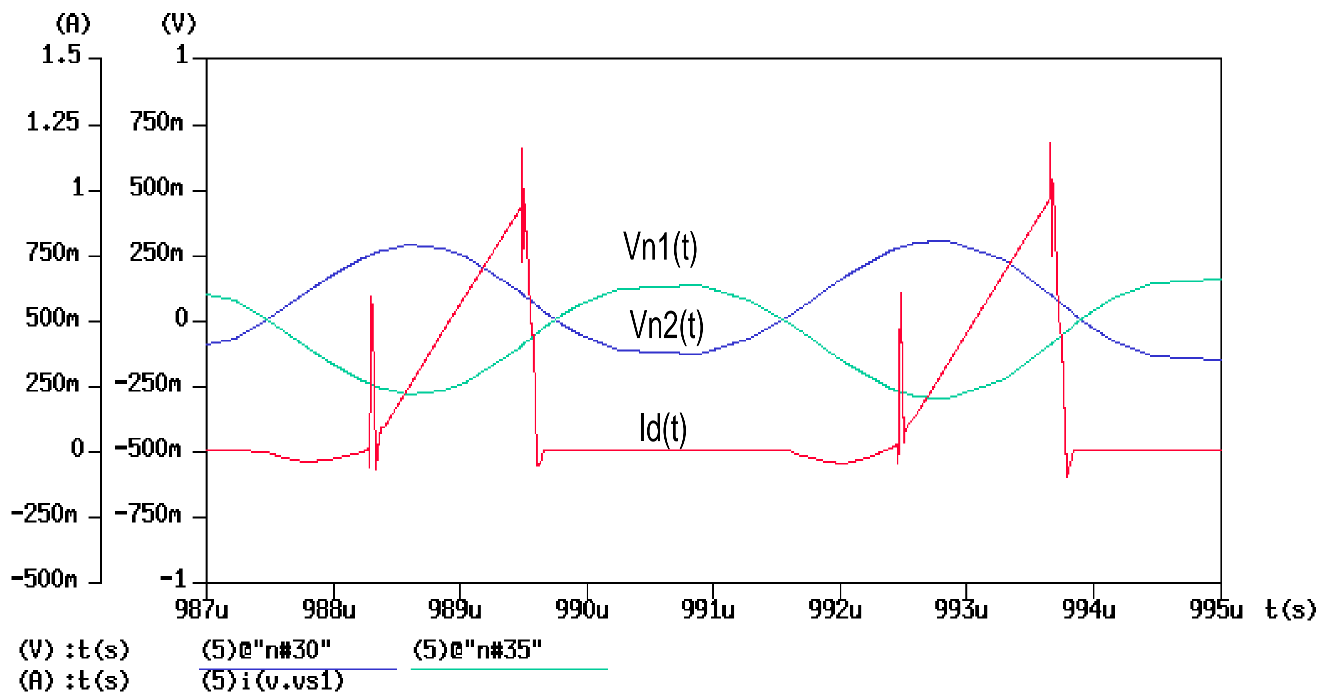
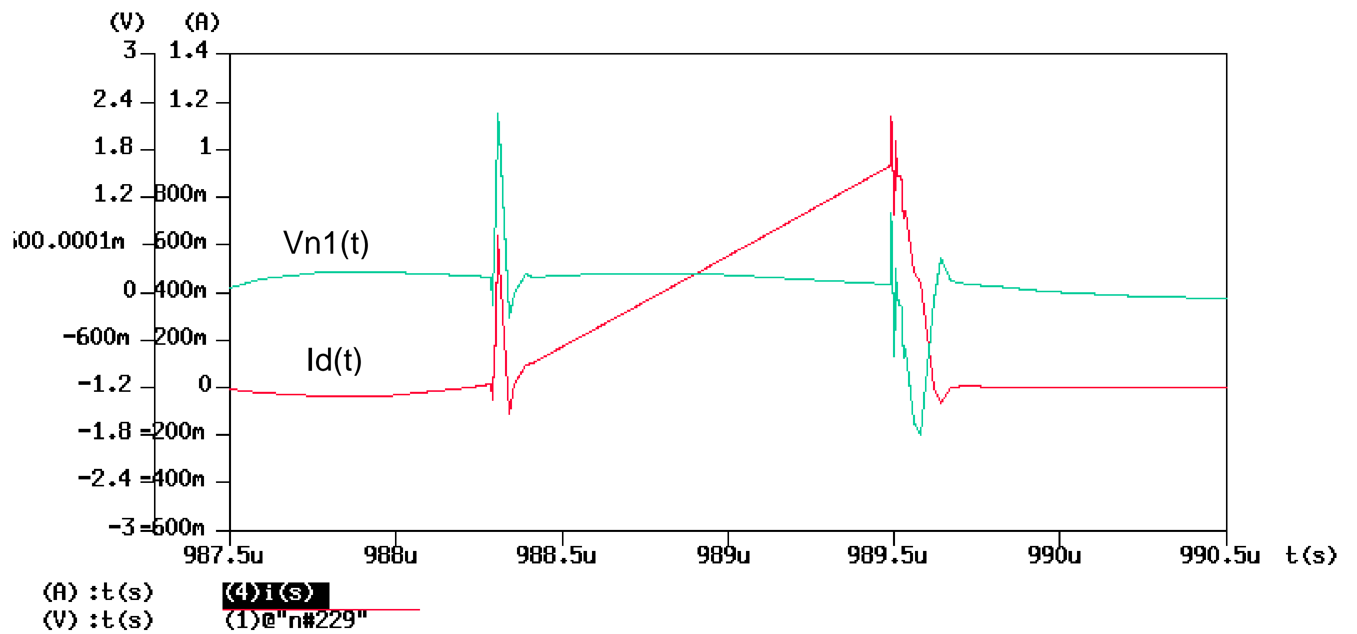


Fig.2.21. Differential-mode current coupled by winding capacitor

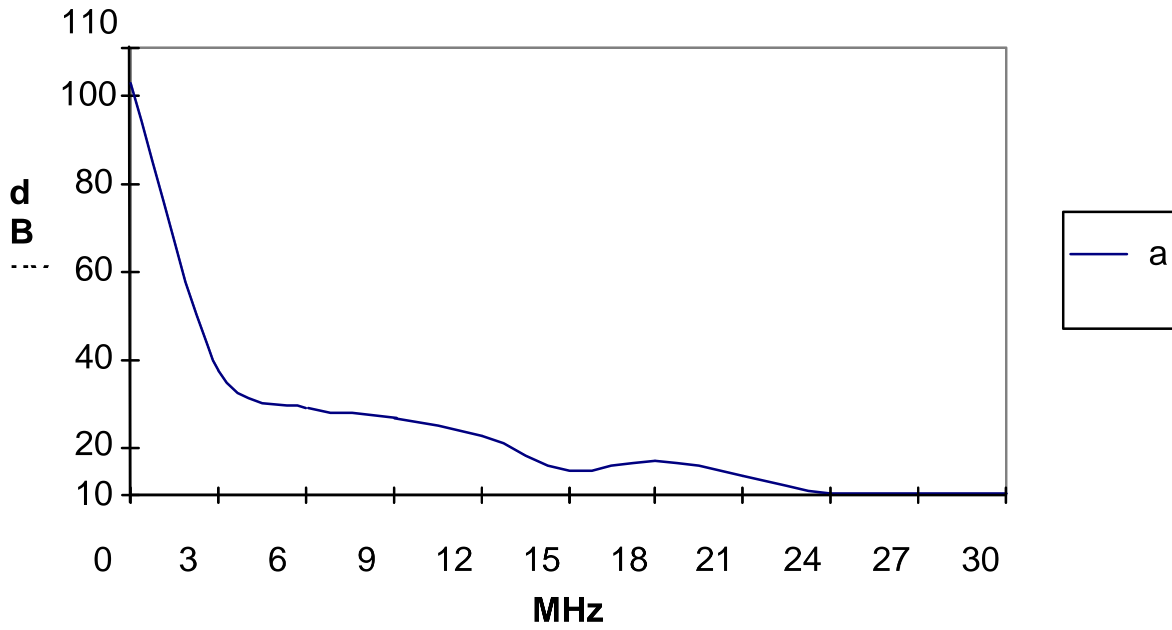


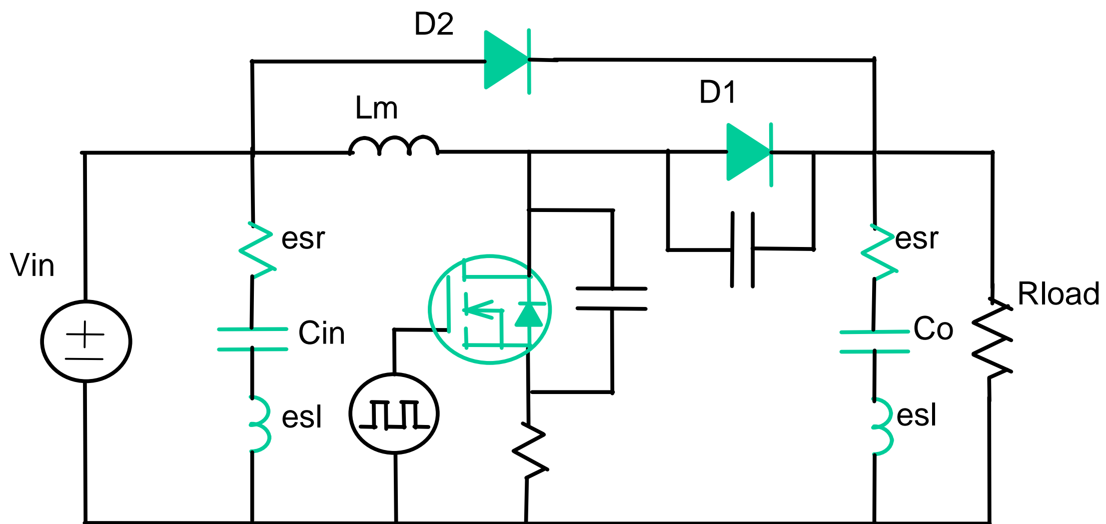
(a)



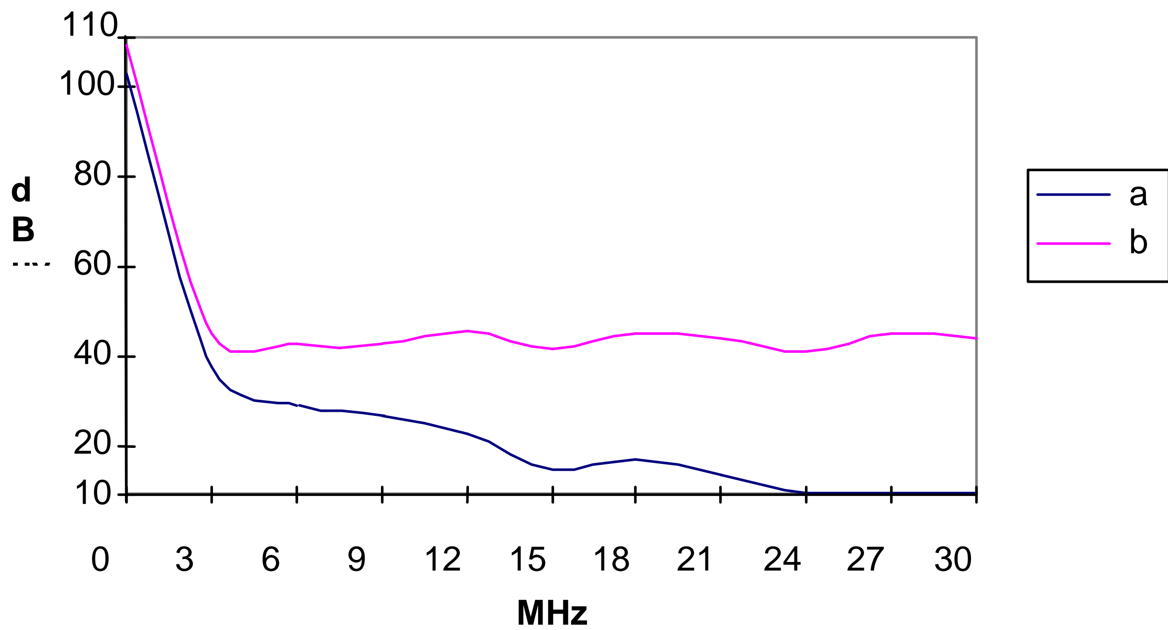
(b)

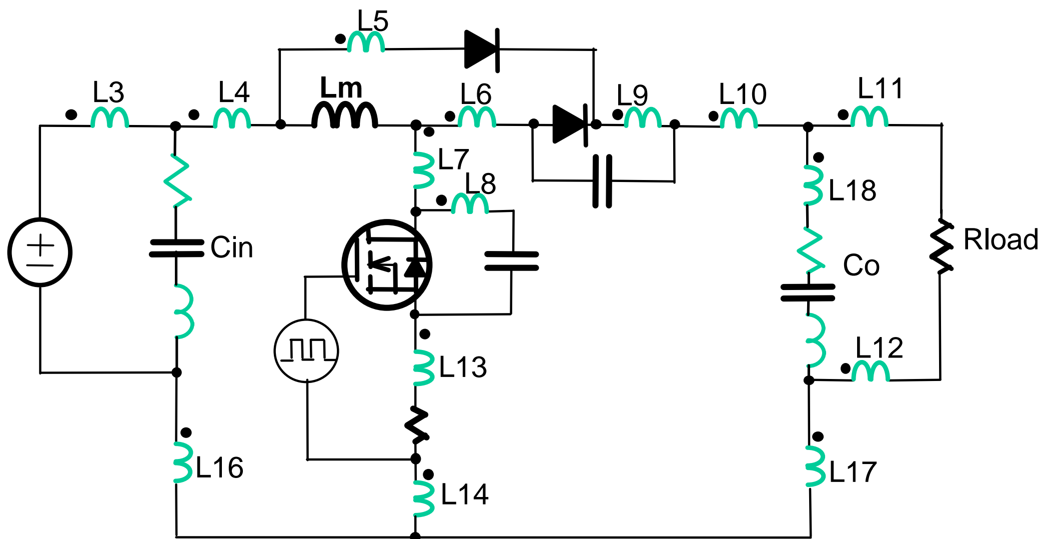
Fig.2.22. Comparison of MOSFET current and LISN 50-Ω voltage (*refer to Fig. 2 18*) (a) without parasitic elements of boost inductor and layout; (b) parasitic element of boost inductor and circuit layout is included to (a).



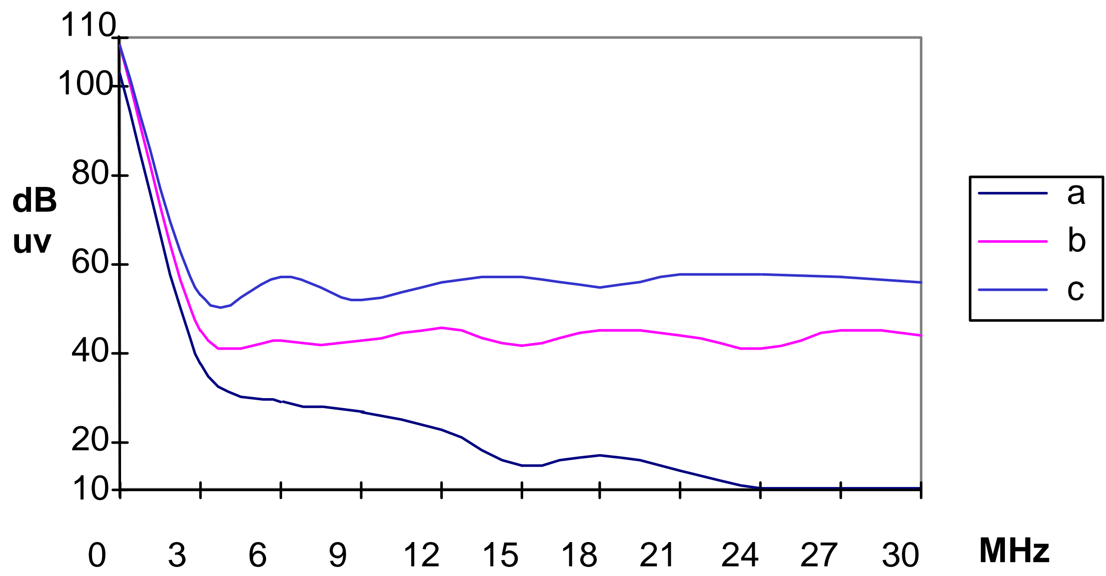


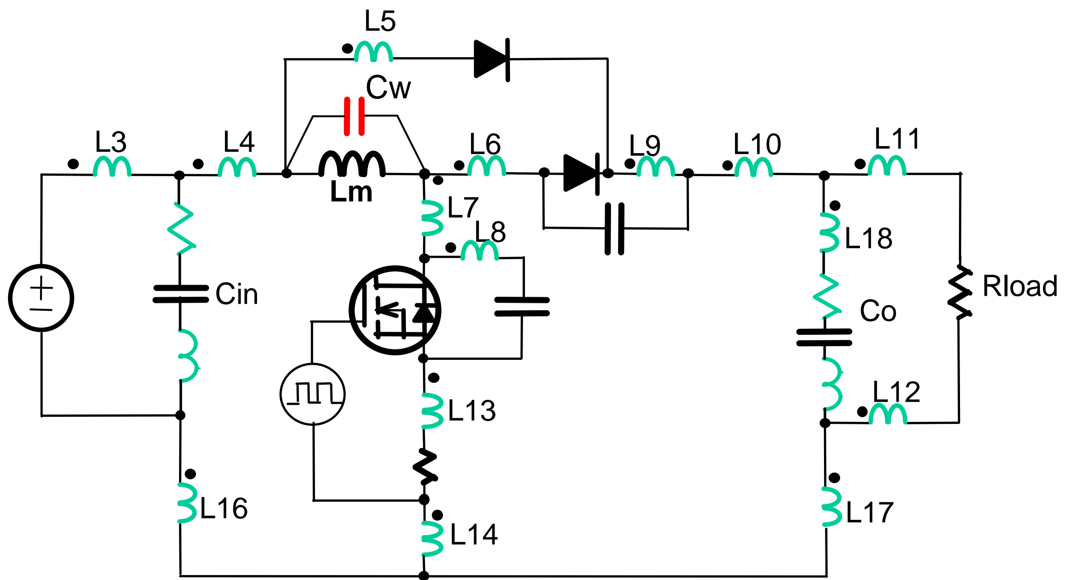
(a) without parasitic elements of boost inductor and layout



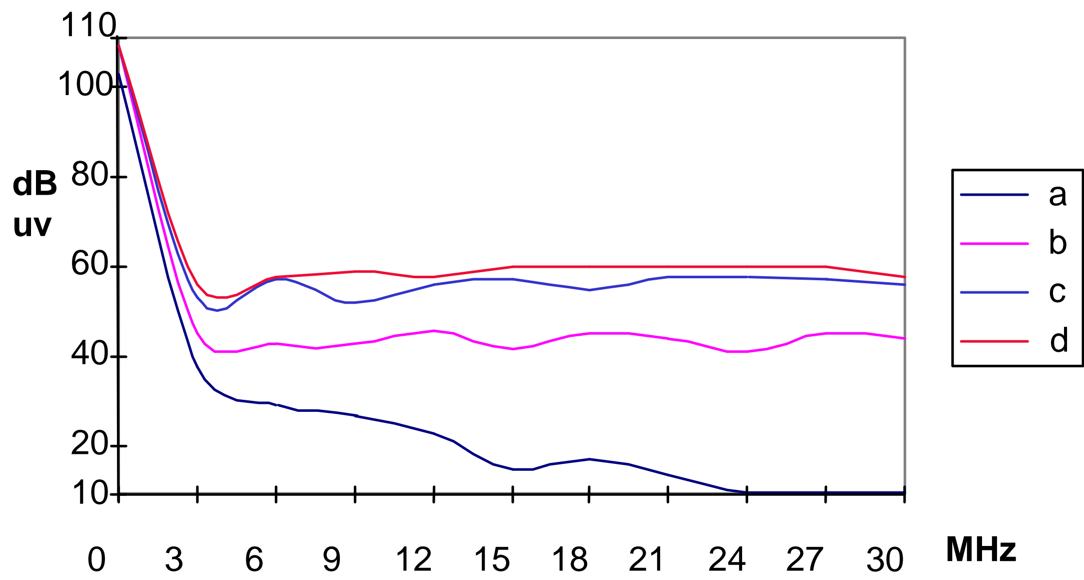


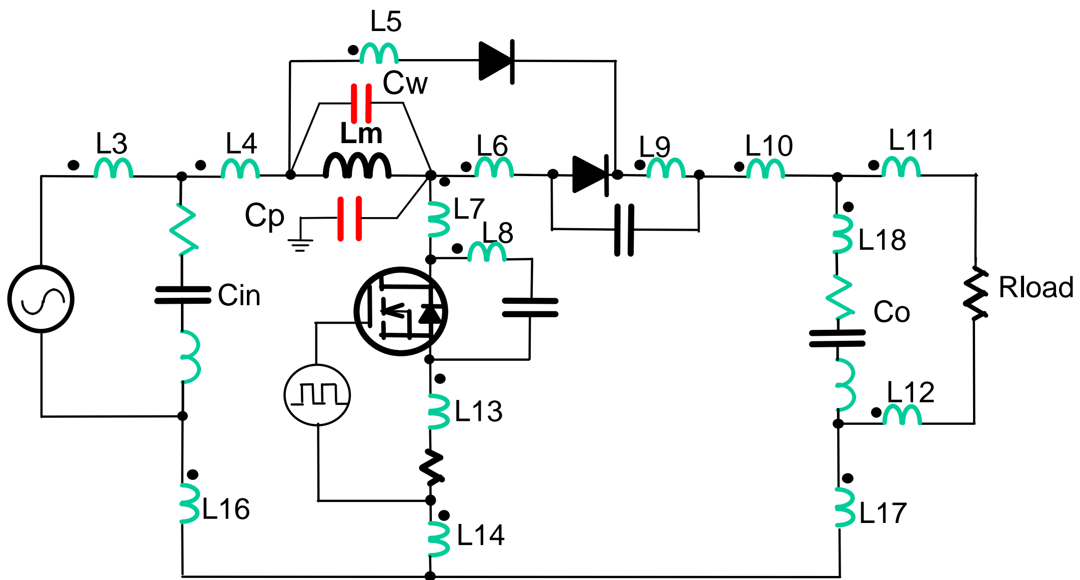
(b) parasitic inductance of layout is included





(c) winding capacitance of boost inductor is included





(d) common-mode capacitance is included.

Fig.2.23. Comparison of DM noise envelope

.

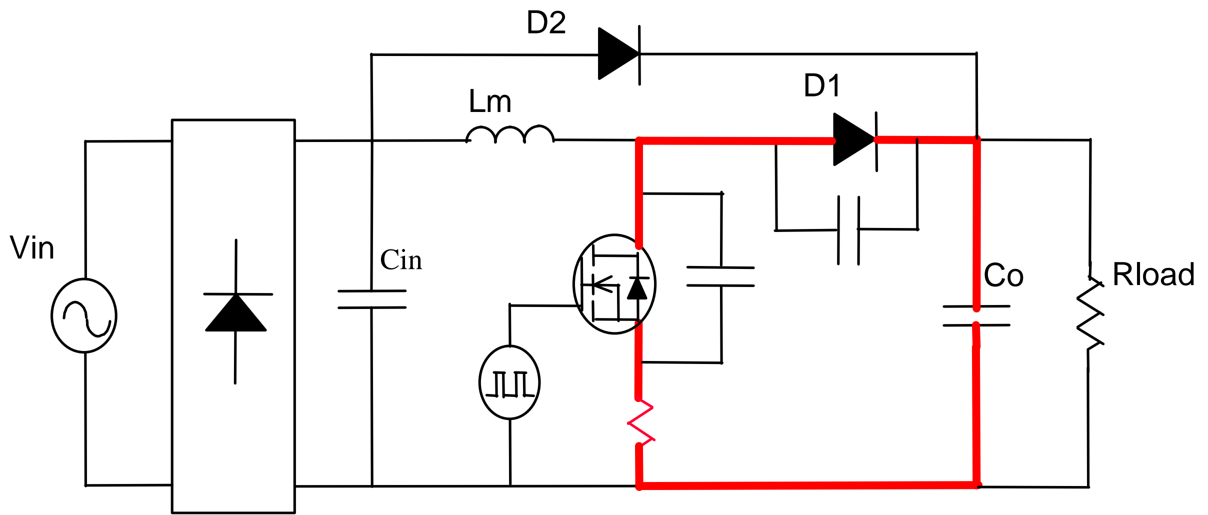
2.4. Noise Minimization

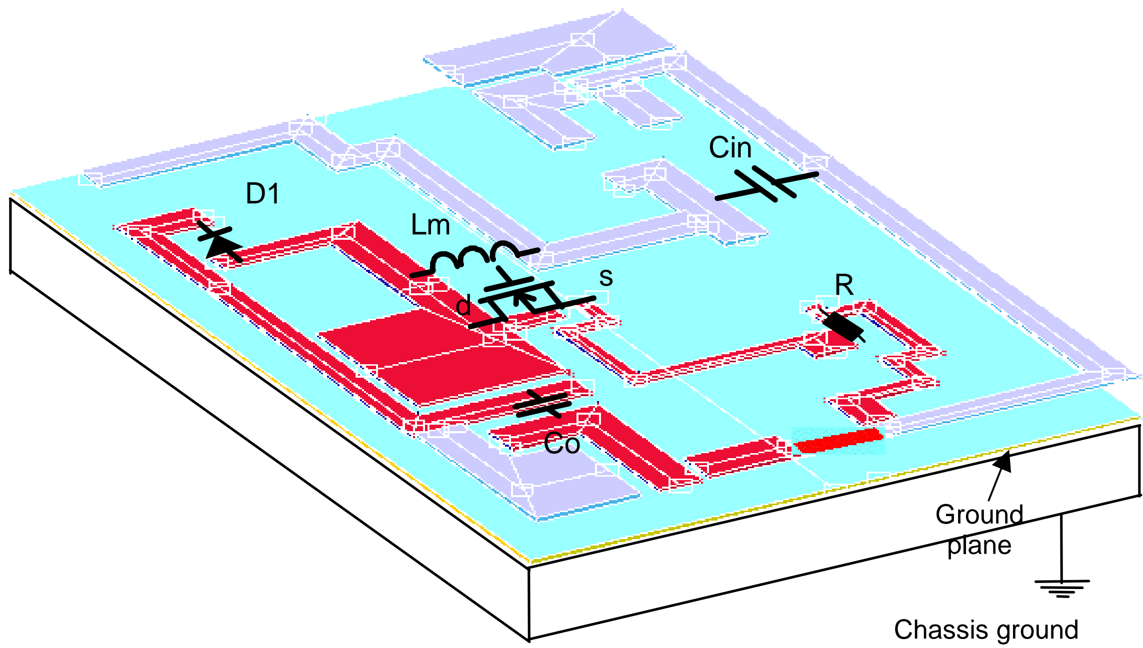
2.4.1. Sensitive Traces of Layout

As seen in the previous section, the layout parasitics have a decisive effect on the DM noise, especially those in the loops that carry high-frequency switched currents. In switch-mode power supplies, these loops usually involve semiconductor devices. For the boost circuit, the critical loop is identified and shown in Fig. 2.24(a) (the thick lines that consist of Mosfet, D1 and Co). To reduce the effect of the parasitic loop inductance, this loop area needs to be minimized. An improved design that reduced the loop area is shown in Fig. 2.25(b).

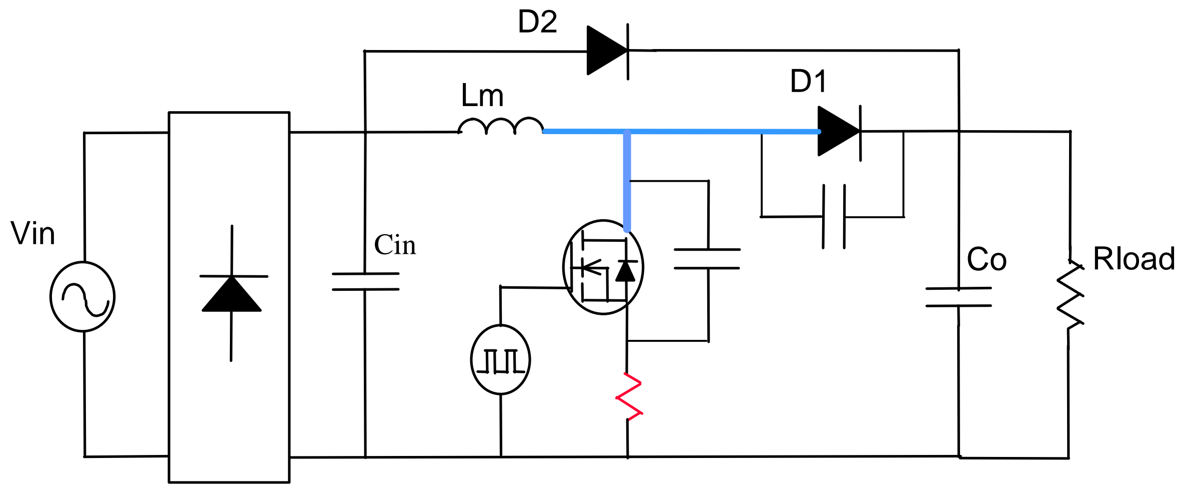
For a hard-switched circuit, the *dv/dt* slew rate is mainly determined by the device characteristics. To suppress the common-mode noise, which is related to *C·dv/dt*, a viable solution is to reduce the common-mode capacitance. In the boost converter, this CM capacitance is contributed mainly from the capacitance between the Mosfet drain trace and the chaise ground. The critical *dv/dt* traces are shown in Fig. 2.24(b).

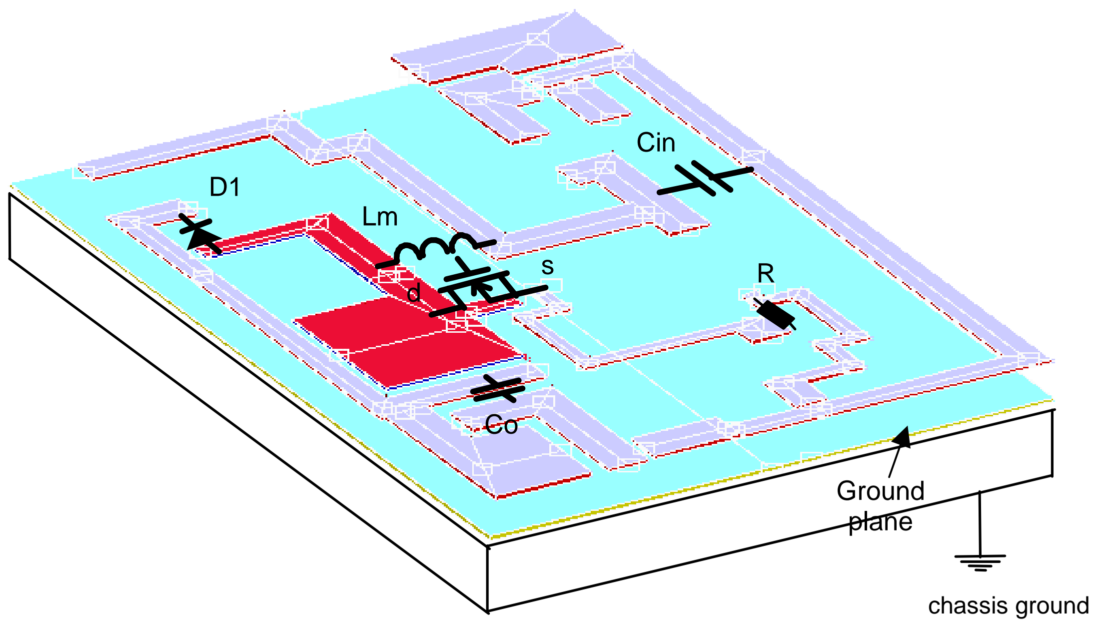
In the new layout design of Fig. 2.25 the drain traces are also minimized to decrease the total area. The performance of the improved layout design was simulated and shown in Fig. 2.26 in comparison with the results of the original design, in which the envelopes of the noise voltage are shown. We see that noise reduction in a wide frequency range is obtained in total, common-mode and differential-mode noise. It can be clearly seen from Fig. 2.10 that the new design not only reduces DM noise due to a smaller loop area, but also lowers CM noise because of the minimized area of drain traces. As a result, the total noise is reduced with the new layout design.





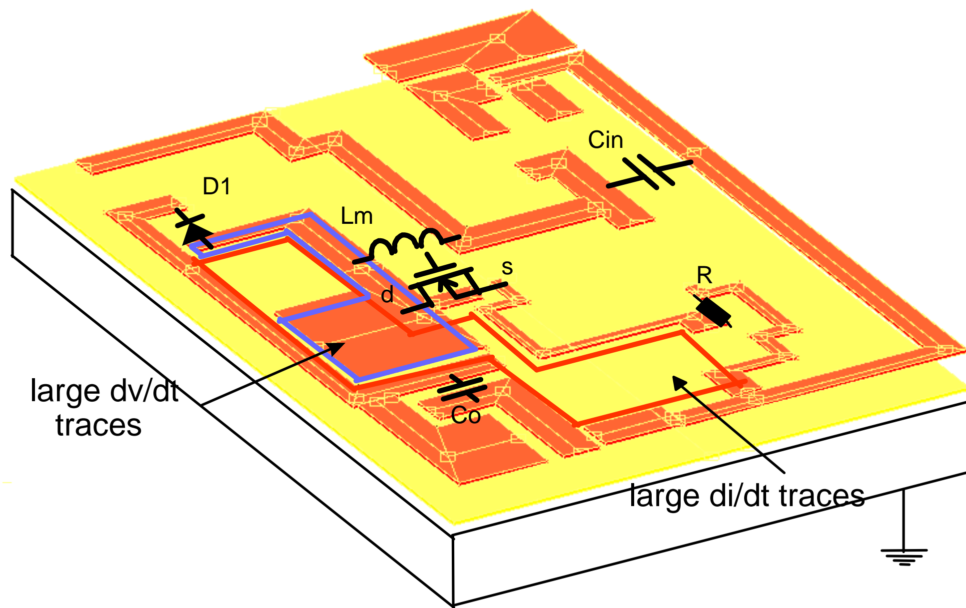
(a) Large *di/dt* traces



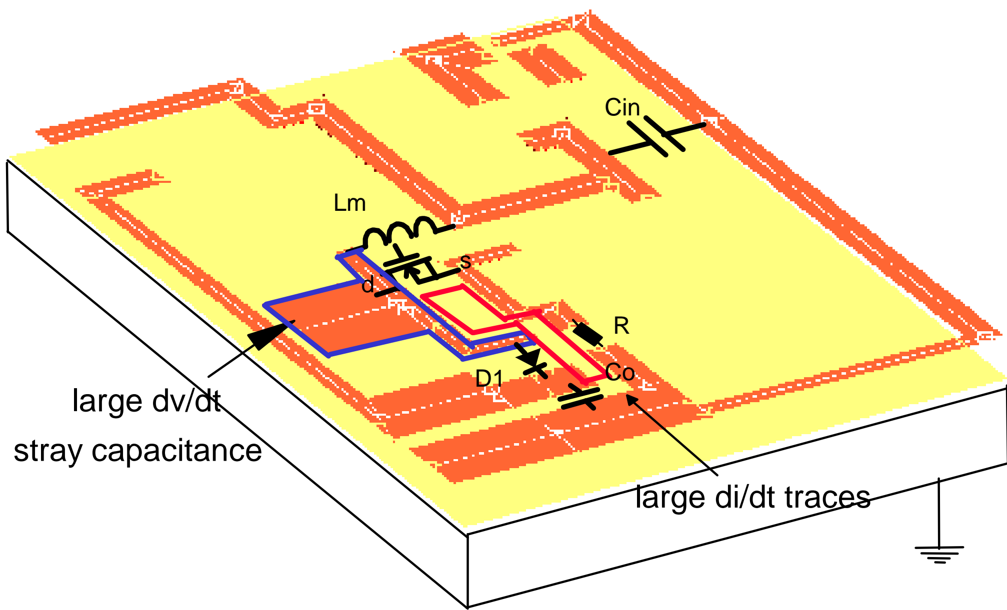


(b) large *dv/dt* traces

Fig. 2.24. Sensitive traces of layout

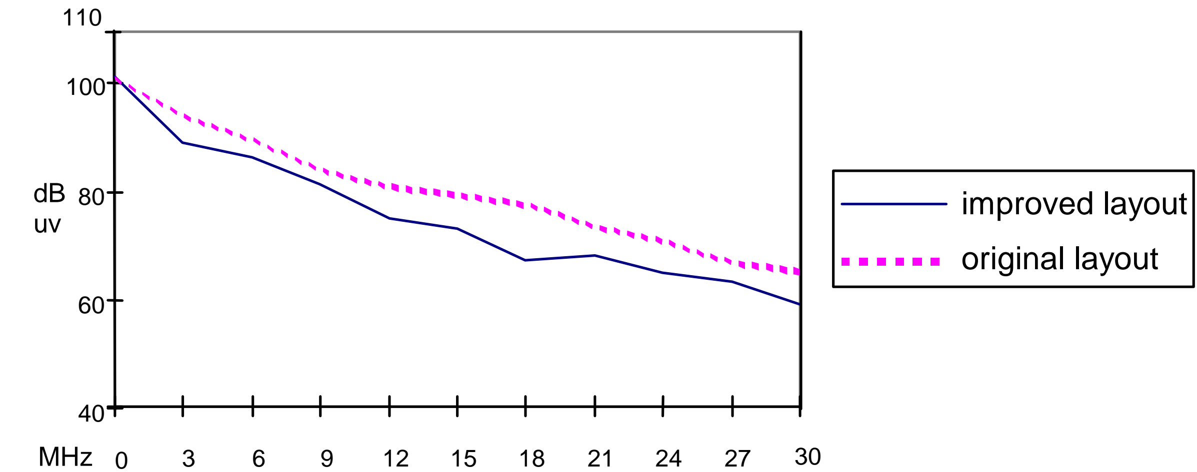


(a)

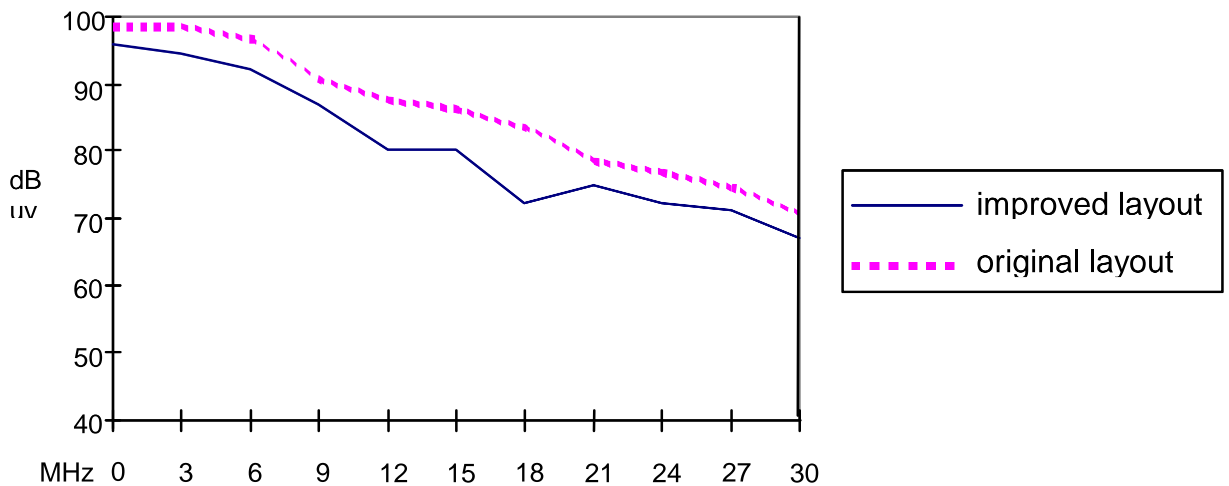


(b)

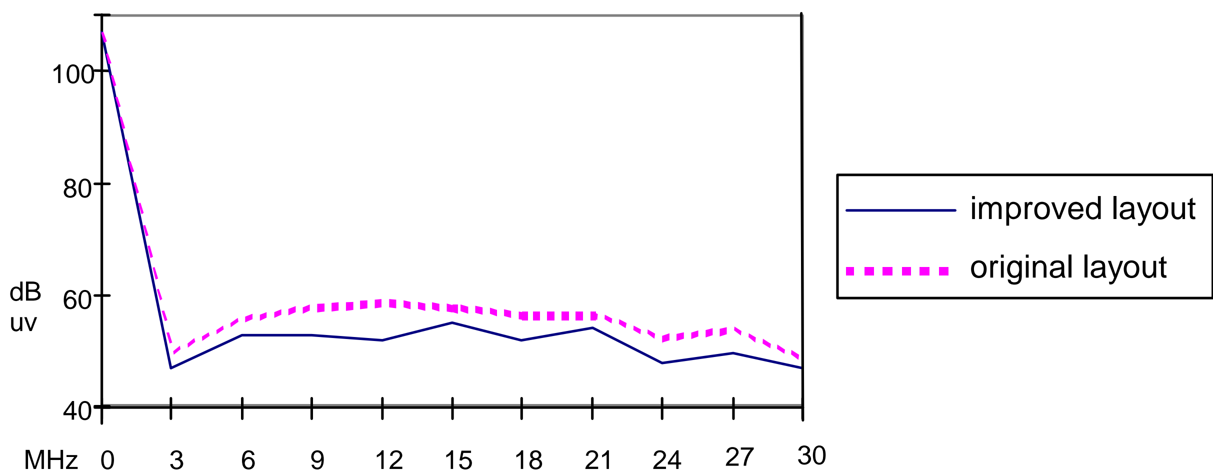
Fig.2.25. (a) Original design (b) Modified layout desig



(a)



(b)



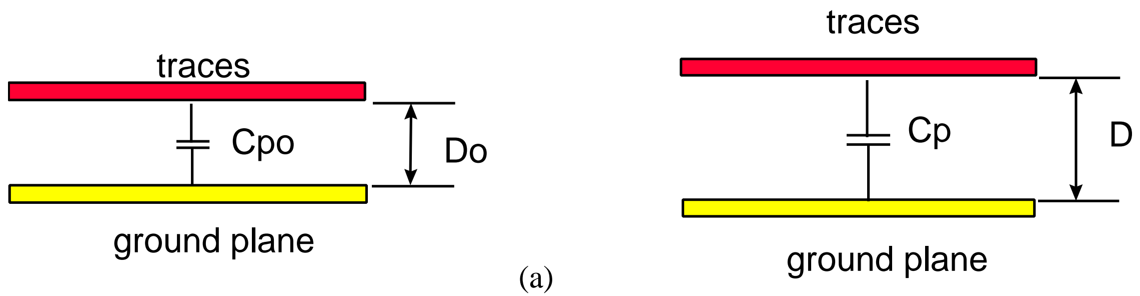
(c)

Fig.2.26. Comparison of EMI noise envelopes of the two layout designs:
(a) total; (b) CM; (c) DM.

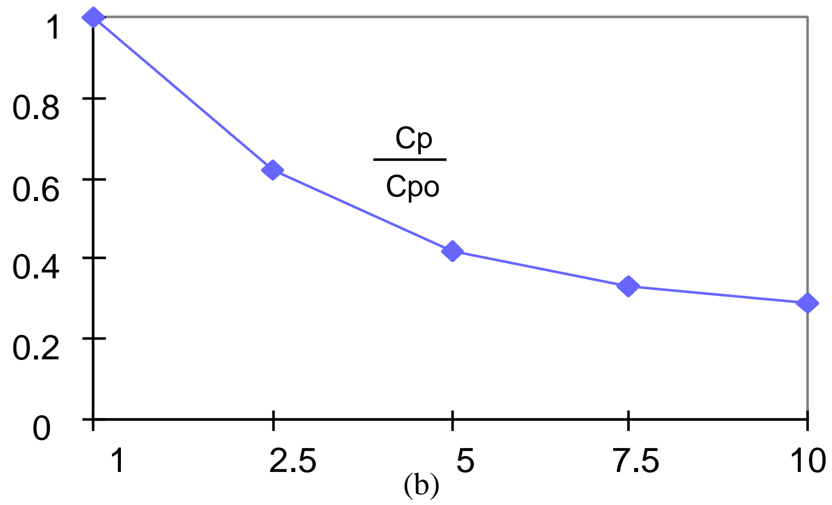
2.4.2. Effect of ground plane spacing

The spacing *d* between the copper trace and the ground plane has a decisive effect on the CM capacitance, and consequently, the CM noise. However, changing the spacing *d* also affects the layout parasitic inductance values because the coupling between the parasitic inductance and its image inductance depends on the spacing. As a result, differential-mode noise of the circuit is affected. Fig. 2.27 shows the common-mode capacitance values versus the distance *d*, as well as the layout parasitic inductance versus *d*.

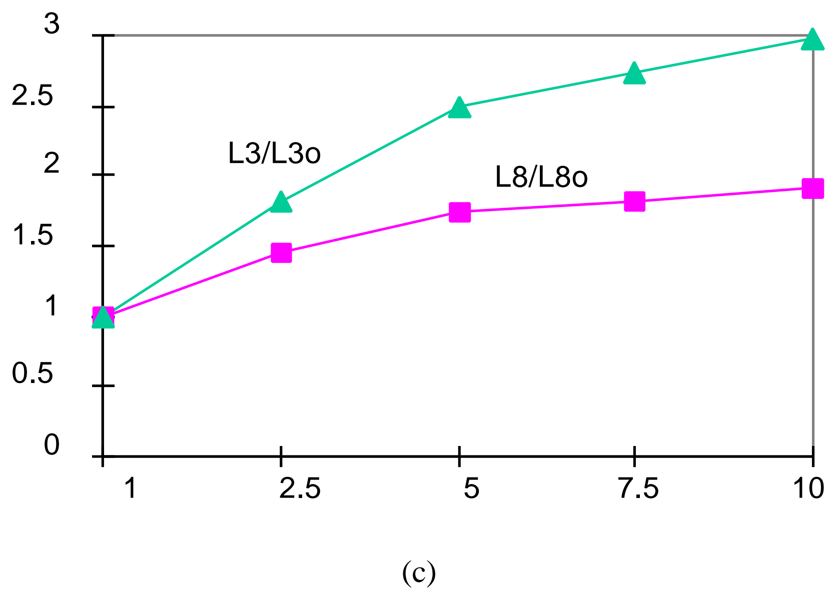
Fig. 2.28. shows the simulation results for different *d* values in order to investigate effects of the ground-plane spacing on the EMI performance. It can be observed that the total noise and CM noise decrease as the spacing of *d* increases. However, DM noise is essentially not affected. The reason is that in the modified layout design, the critical loop inductance is greatly reduced. The parasitic capacitance between PCB traces and ground plane is decreased as *d* increases, and consequently reduces the CM emission which is closely related to $C\cdot\frac{dv}{dt}$. Therefore, overall, it is desirable to have large spacing between the ground plane and the PCB layer for the EMI consideration, as long as the critical loop inductance is minimized. On the other hand, because the ground plane also acts as a heat-spreader and an interface with the heat-sink, an increased *d* value increases the thermal resistance from the PCB layer to the ground plane and reduces the effectiveness of heat removal. Therefore, the optimization of the *d* value should be determined by the trade-off study of the EMI performance and thermal requirement.



(a)

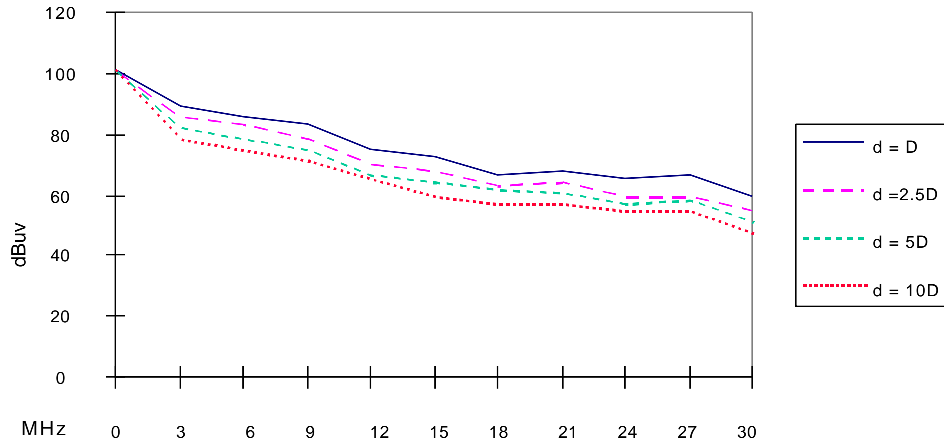


(b)

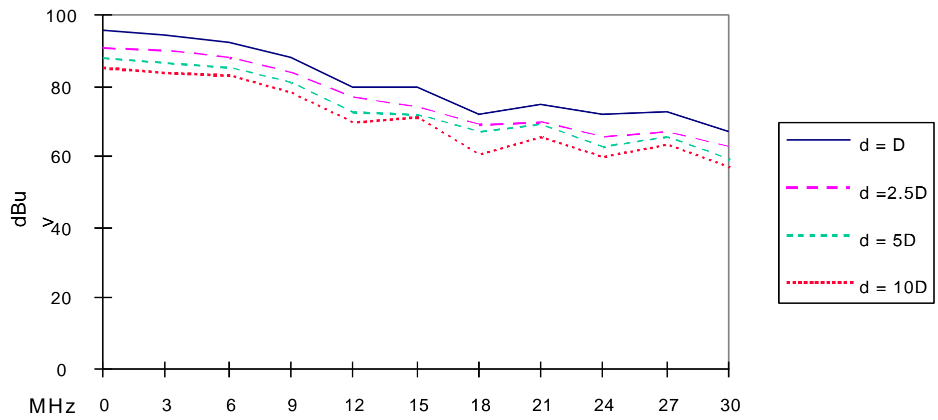


(c)

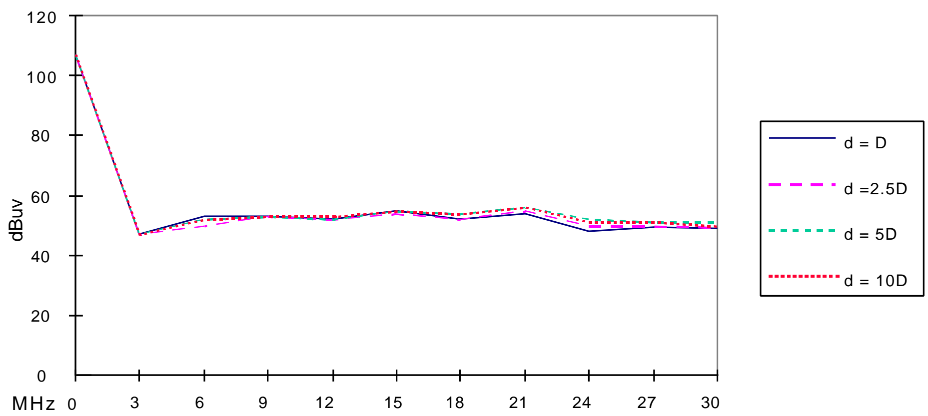
Fig.2.27 Influence of ground plane distance *d*



(a) total noise



(b) CM noise



(d) DM nois

Fig.2.28. EMI noises as functions of ground plane distance (a) total (b) CM (c) DM

2.4.3. Parasitic of The Magnetic Component

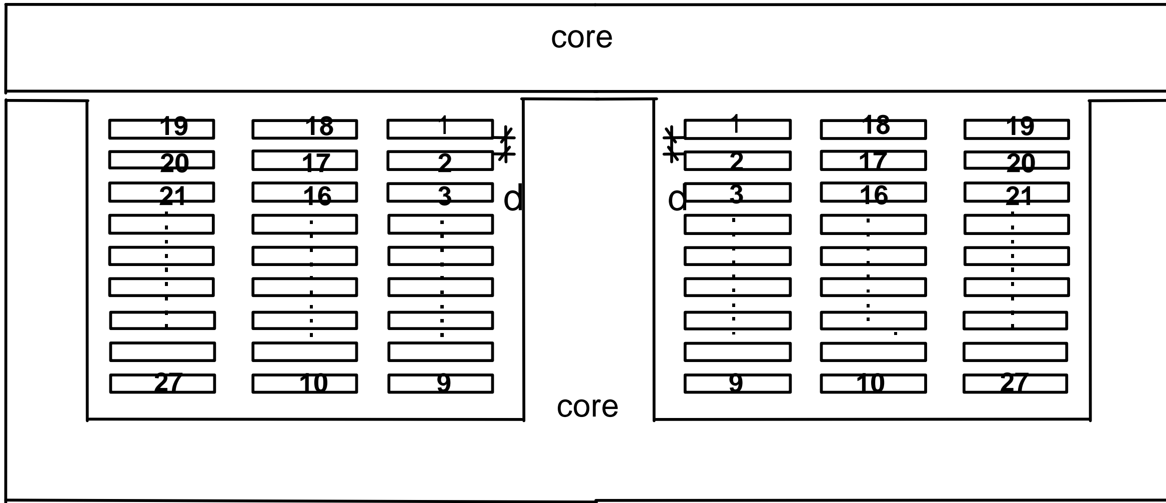
As can be seen in Section 2.3.1, the winding capacitance of the boost inductor has an important effect on differential-mode noise. To reduce the conductive EMI, this parasitic element should be minimized. From Eq. (2.17) we see that several parameters can be modified to change this element. For example, increasing the insulator thickness will reduce parasitic capacitance between the winding layers. By modifying the number of turns and the winding arrangement, *Ceq* can also be modified.

Here the technique of winding arrangement is studied. Basically the structure and the size of inductor remain the same, while the capacitive energy stored in the inductor will change when the winding sequence is modified. The parasitic element of the planar inductor is dominated by the parasitic capacitance between adjacent layers. By reducing the voltage potential between the conductors at adjacent layers, which means that *n1, n2* and *n3* are reduced, the capacitive energy stored in the planar inductor is expected to decrease.

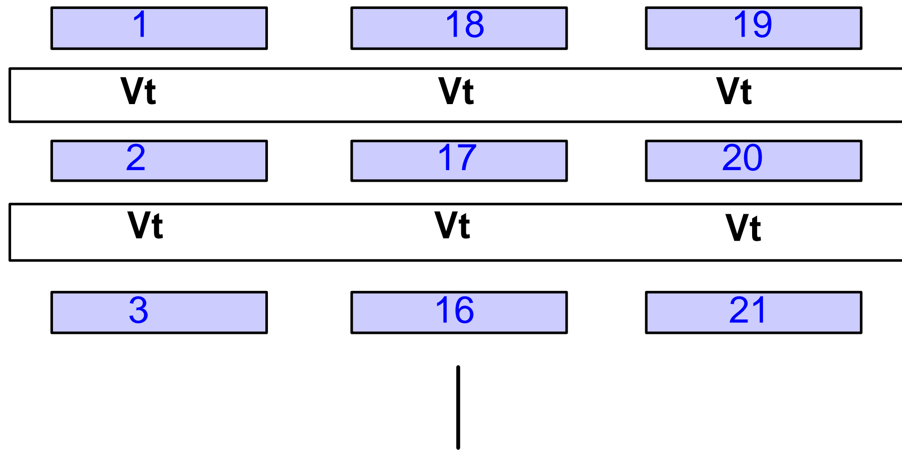
The proposed winding arrangement is shown in Fig. 2.29(a). The voltage potential between the conductors at adjacent layers is shown in Fig. 2.29(b). We have *n1*=*n2*=*n3*=1. According to Eq. (2.17), the equivalent winding capacitance can be calculated as

$$C_{eq} = \frac{(m-1)}{n^2} \cdot (1^2 + 1^2 + 1^2) \cdot C_t = \frac{8}{27^2} \cdot (1^2 + 1^2 + 1^2) \cdot Ct = 1.4\,(pF)$$

Simulated EMI noise spectrum is compared with that of the original design in Fig. 2.30. We see that differential-mode noise is reduced by about 10dB. However, this may not be a practical design at present due to manufacture problem.

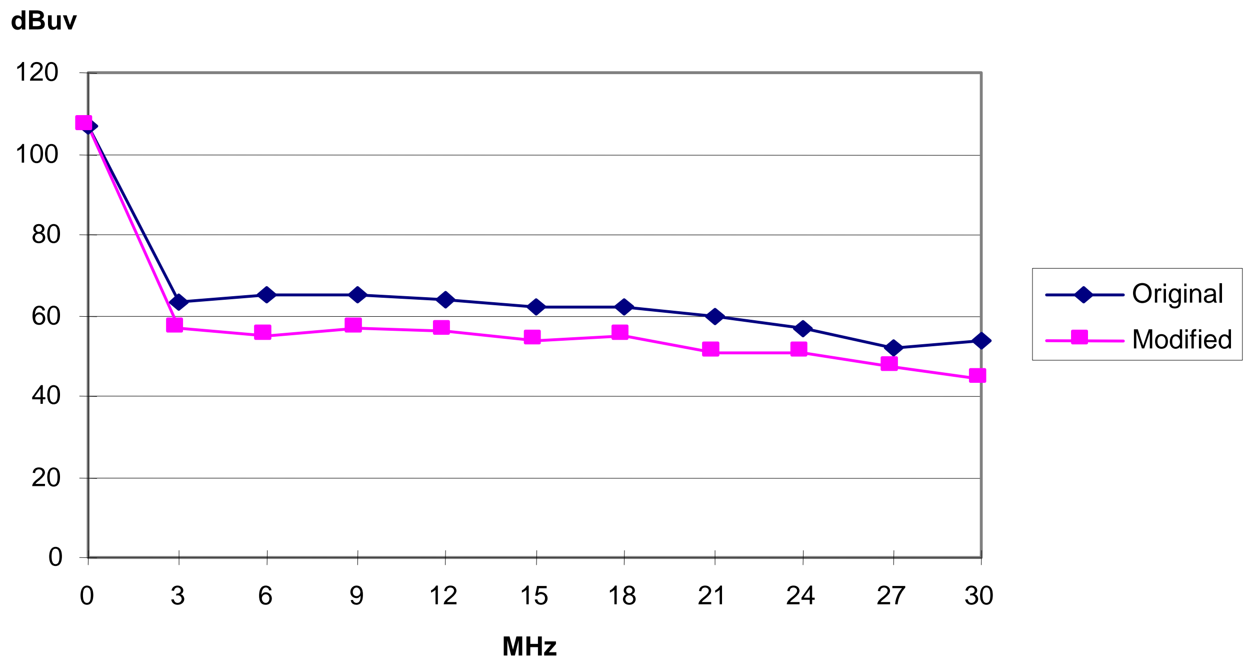


(a)



(b)

Fig. 2.29 (a) Proposed winding arrangement (b) voltage potential between the conductors of adjacent layers



2.30. DM noise comparison

2.5. . EMI Filter Design

The EMI filter is used to attenuate the conducted noise and meet the EMI regulations, which is usually designed and checked at the hardware implementation stage. With the simulation tools, the conducted noise can be predicted at an early design stage, and thus the EMI filter can be designed at the design stage. Furthermore, with the improved layout design, the conducted noise can be reduced, and thus it is possible to decrease the size of the EMI filter.

As an example, the EMI filter is designed for the boost PFC circuit based on the predicted noise level. VDE 0871A is used as the EMI standards, and the structure of the EMI filter is shown as Fig. 2.31. The EMI design procedure is referred to in[8].

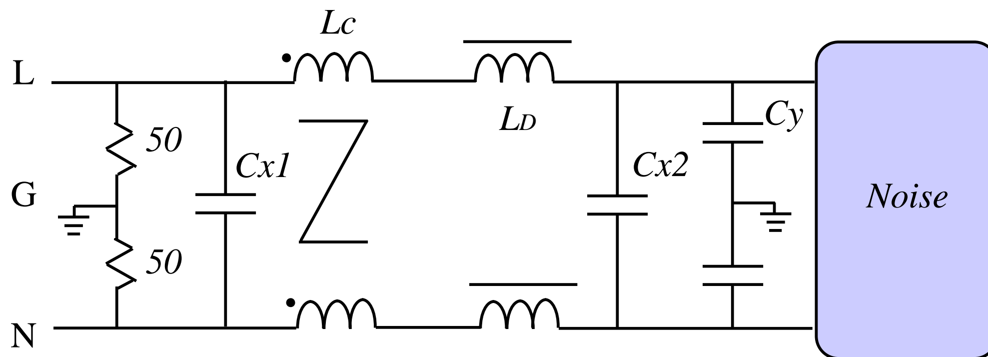


Fig.2.31. EMI filter structure

According to the predicted noise level and EMI requirement shown as Fig. 2.32, the attenuation requirement for the total, common-mode and differential-mode noise can be calculated. The corner frequency of EMI filter is found as Fig. 2.33, which is *28 KHz* for CM noise, and *20.5 kHz* for DM noise. Then the parameters for the EMI filter can be calculated as the following:

For CM part, use $C_y=3300pF$, and calculate *Lc* according to Eq. (2.21):

$$Lc=\left(\frac{1}{2\mathbf{p}\cdot f_{R,CM}}\right)^2\cdot\frac{1}{2C_Y} \qquad (2.21)$$

where $f_{R,CM}=28KHz$, thus

$$Lc=4.9mH$$

(a) Generally the leakage inductance is in the range of 0.5%-2% of the Lc value, assume

$$L_{leakage}=1\%*Lc=49uH$$

Then, decide the L_{DM} and C_{DM} according to Eq.(2), where $f_{R,DM}=20.5\ KHz$, then

$$C_{X1}=C_{X2}=C_{DM}=\left(\frac{1}{2\pi\cdot f_{R,DM}}\right)^2\cdot\frac{1}{L_{DM}} \tag{2.22}$$

Use the leakage inductance as the DM choke $L_{DM}=L_{leakage}$, then $C_{DM}(=C_{X1}=C_{X2})=1.23uF$.

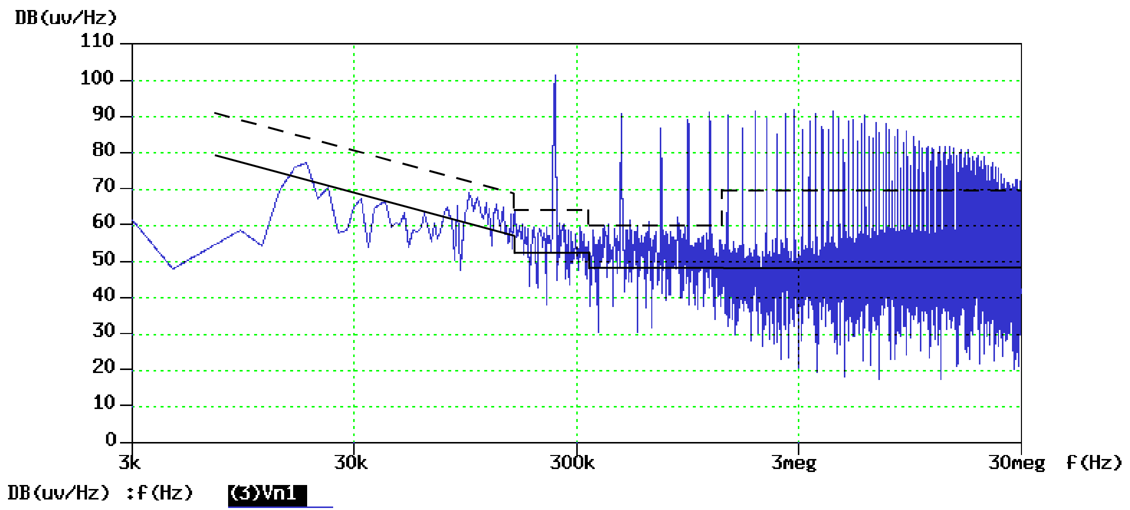
b) Choose C_{DM} as $0.47uF$, which is commonly available, then $L_{DM}=128uH$ and

$L_D=\dfrac{L_{DM}-L_{leakage}}{2}=40uH$.

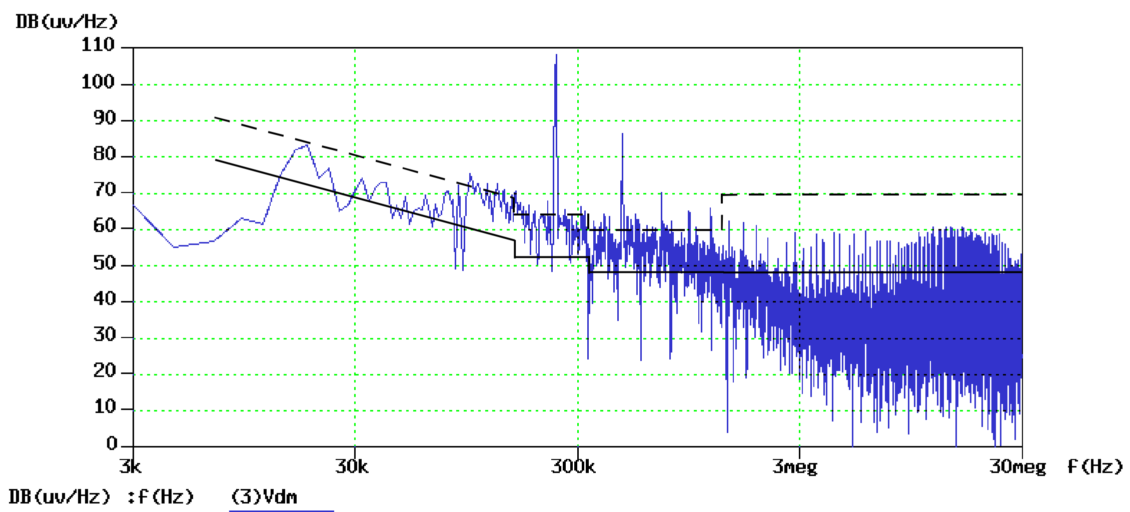
c) If choosing $C_{DM}=0.22uF$, then $L_{DM}=274uH$, and $L_D=112uH$.

The circuit noise spectrum with the EMI filter inserted is shown as Fig. 2.34.

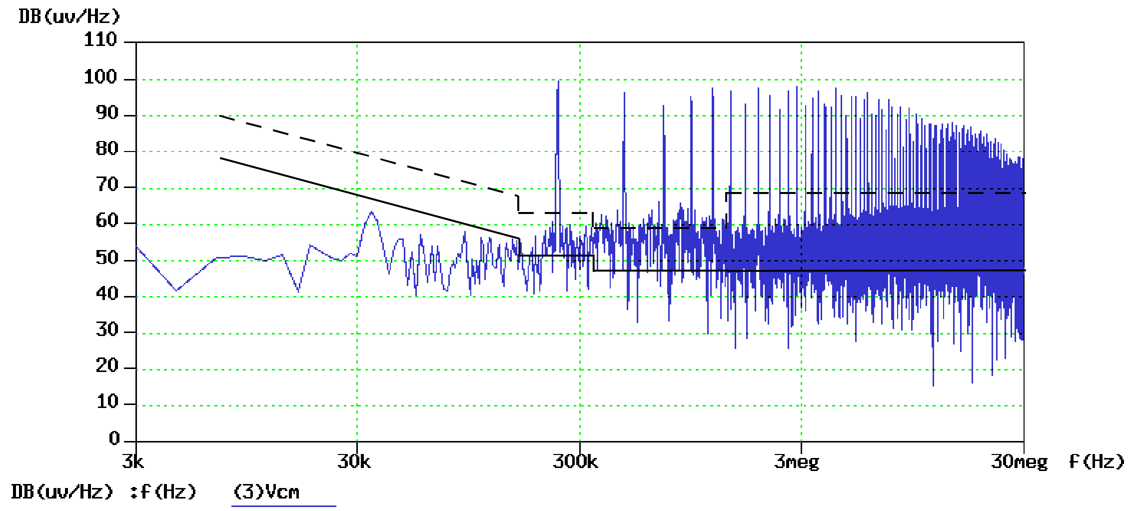
It is seen that the component values for DM noise filtering are practical, while the size of the common-mode choke may be undesirable. Hence, we can reduce the filter size by suppressing the common-mode noises in the circuit. To minimize the common-mode noise by changing the circuit layout is one way to remedy the problem.



(a) Total noise spectrum

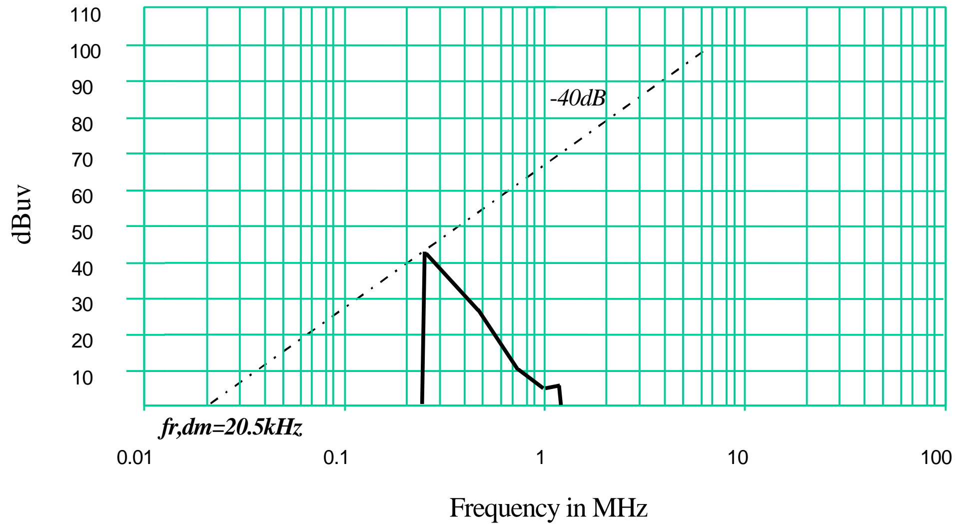


(b) DM noise spectrum

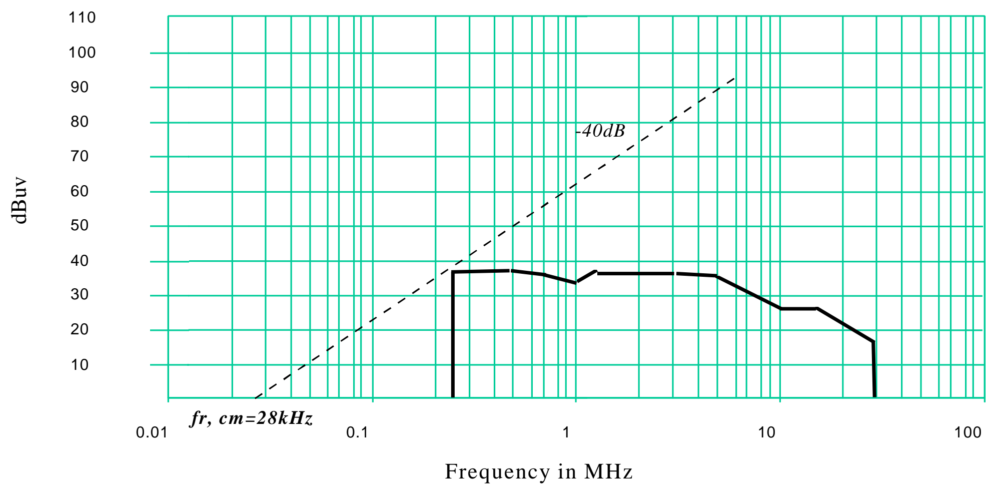


(c) CM noise spectrum

Fig. 2.32. Noise spectrum for original design

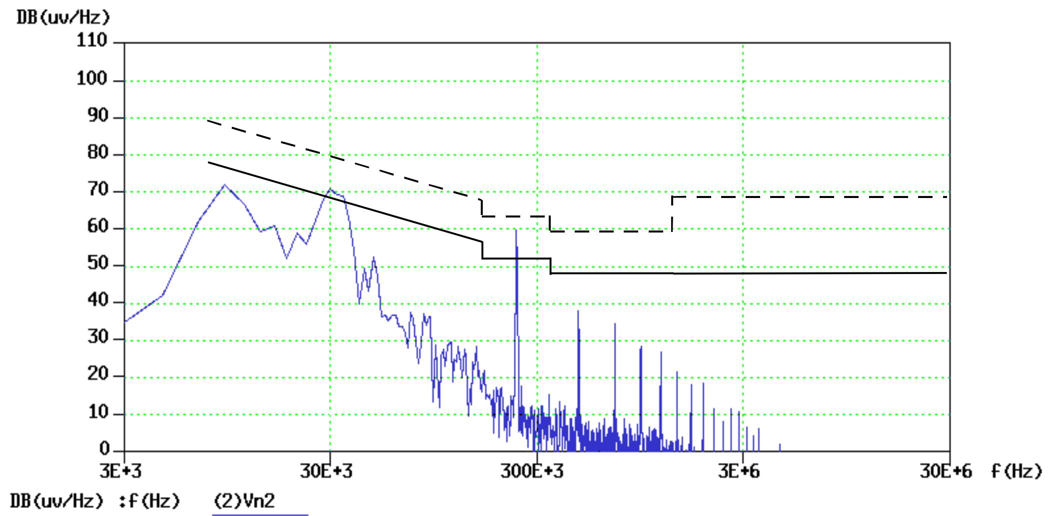


(a) DM noise attenuation

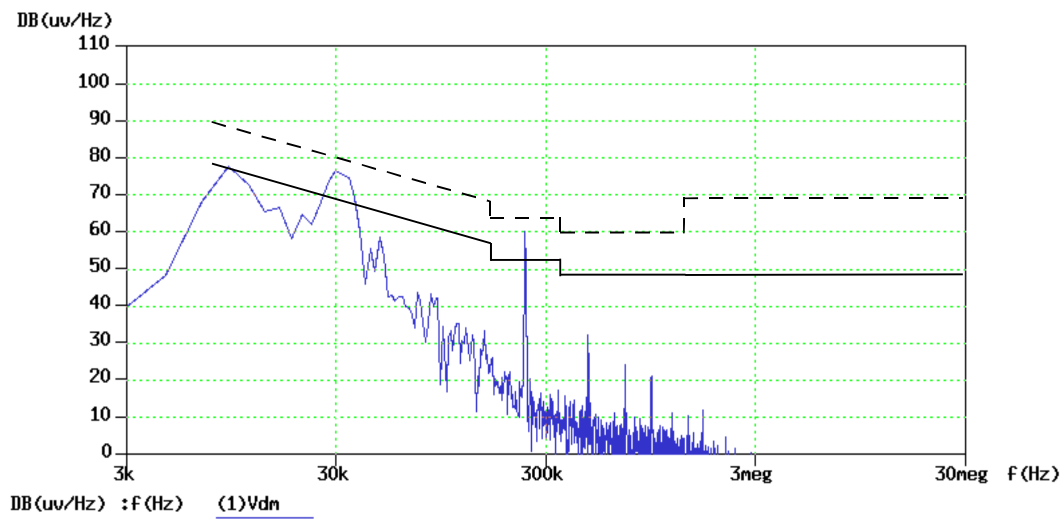


(b) CM noise attenuation

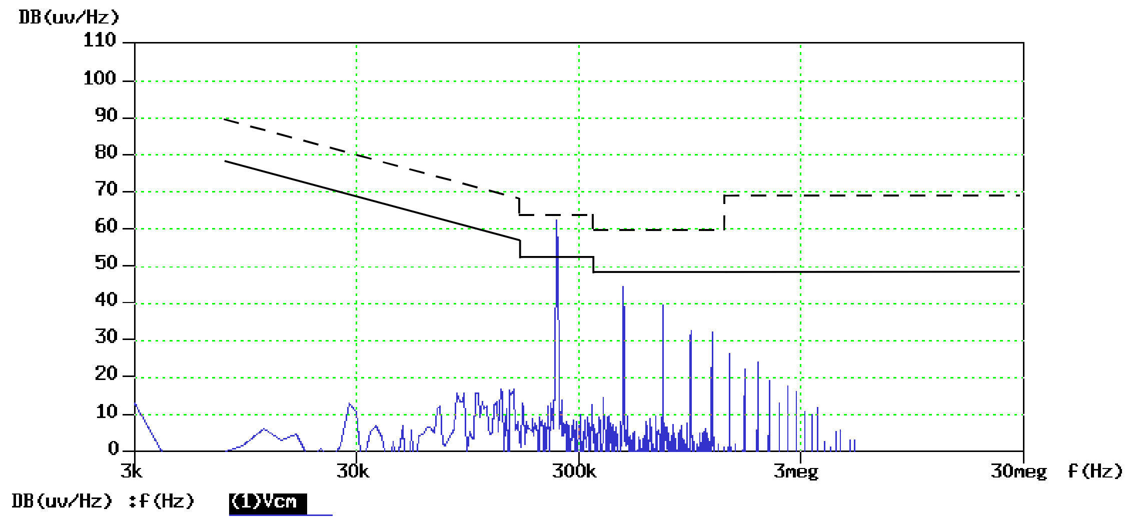
Fig.2.33. Noise filter attenuation



(a) Total Noise



(b) DM noise



(C). CM noise

Fig.2.34. Noise spectrum with the filter

CHAPTER 3

THERMAL ANALYSIS BY SIMULATION

In this chapter, thermal analysis is conducted for the PFC converter by using *Flotherm.* Applying *Computational Fluid Dynamics (CFD)* techniques, the software *Flotherm* provides a tool to implement thermal analysis at the early design stage. The CFD program takes into account the thermal transfer mechanisms of forced, mixed and natural convection, conduction over a wide range of conductivities, radiation, laminar and turbulent flows simultaneously. The above mechanisms are taken into account by *Flotherm* without the need to assume heat transfer coefficients, and thus provides an efficient tool to deal with the thermal design problem at an early stage.

To use *Flotherm,* component power loss must be calculated first. Section 3.1. describes the procedure to obtain the power losses for various components. The losses of Mosfet, diode, input rectifier and output capacitor for the boost PFC circuit are estimated by circuit simulation with *Saber.* Inductor winding loss is estimated by FEA methods using *Maxwell Field Simulator* of *Ansoft,* in which the high frequency skin effect, proximity effect and fringing effect are included. In Section 3.2, thermal models are proposed for the boost converter. Component models for thermal simulation are introduced. The modeling and thermal spreading effect of PADs is analyzed. Based on the models developed, the thermal performance of boost PFC circuit can be predicted. The hot spot temperature of semiconductor devices and magnetic component is important for the reliability of the converter circuit. Usually the hot spot temperature of a magnetic component is unknown. However, by using the models developed in Section 3.2 and the loss information from FEA analysis, the internal temperature profile of planar inductor can be found by using *Flotherm* simulation. To improve thermal management, several examples are studied to reduce inductor temperature, which is implemented by optimizing the heat transfer path for the inductor and reducing its power loss. The analysis results are summarized in Section 3.3.

3.1. Component Power Loss Estimation

Considerable effort has been directed toward power loss estimation in the PFC circuit. Power loss information is absolutely essential in determining thermal behavior of the circuit. As in the first part, a description of component loss estimation technique is given. The results of the estimation are given for a *60 w, 250 KHz* PFC circuit.

Basically, the circuit simulation package *Saber* is used for the estimation of power losses. By using *Saber*, both *i(t)* and *v(t)* waveforms can be obtained and Eq.(3.1) is used for estimating the loss of each component. The models of each component will be

$$P_{LOSS} = \frac{1}{T}\int_0^T i(t)\cdot v(t)\cdot dt \qquad (3.1)$$

described in detail. However, there are two issues that need to be pointed out. One is the issue of the effect of layout parasitic on component power losses, and the other issue is the fact that the circuit under consideration is a PFC circuit which is periodic with respect to *120 Hz* frequency but not PWM frequency.

The simulation results show that the component losses are nearly the same with and without layout parasitic included. Thus the loss calculation can be conducted with the circuit that has no layout parasitics included.

The power integration of Eq. (3.1) should be done over a *60 Hz* cycle to find out the average power loss in a particular component, since the waveforms of a PFC circuit is periodic with respect to *60 Hz* (period of *16.67 ms*). However, because of waveform symmetry, the minimum integration period for power loss calculation is a half cycle, which is *8.33 ms*. The loss for the component as power Mosfet, diode, rectifier and capacitor ESR is calculated as follows.

3.1.1. MOSFET Loss Calculation

As in Chapter 1, the semiconductor device model from the *Saber* component library is used for electrical simulation. By running the simulation for the circuit, the integration of the Mosfet $id(t)\times Vds(t)$ is found within half a line cycle as shown in Fig. 3.1, and the Mosfet loss can be estimated as:

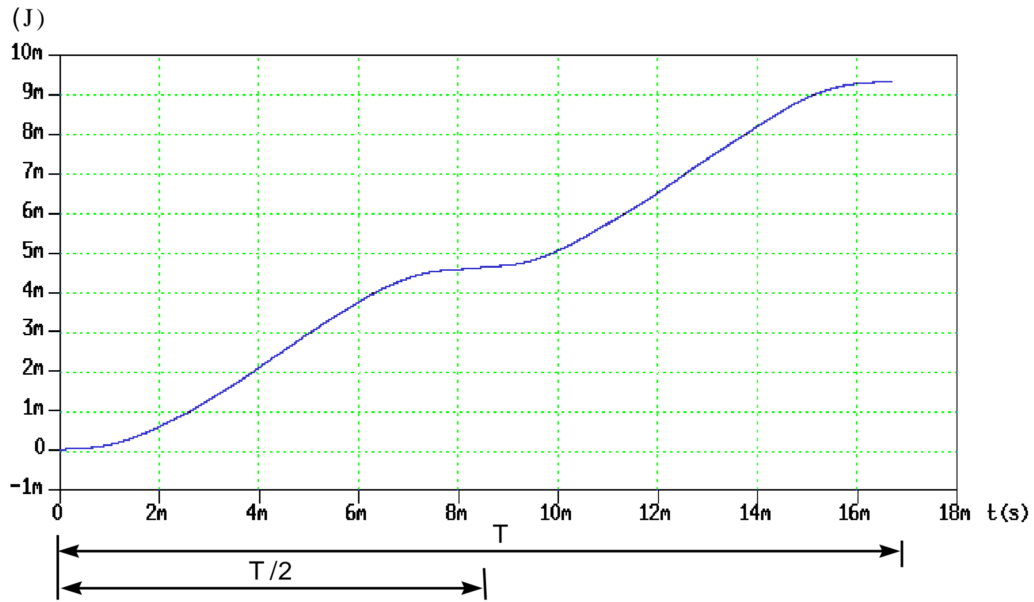


Fig.3.1. Integration of Mosfet v(t)·i(t) in PFC circuit

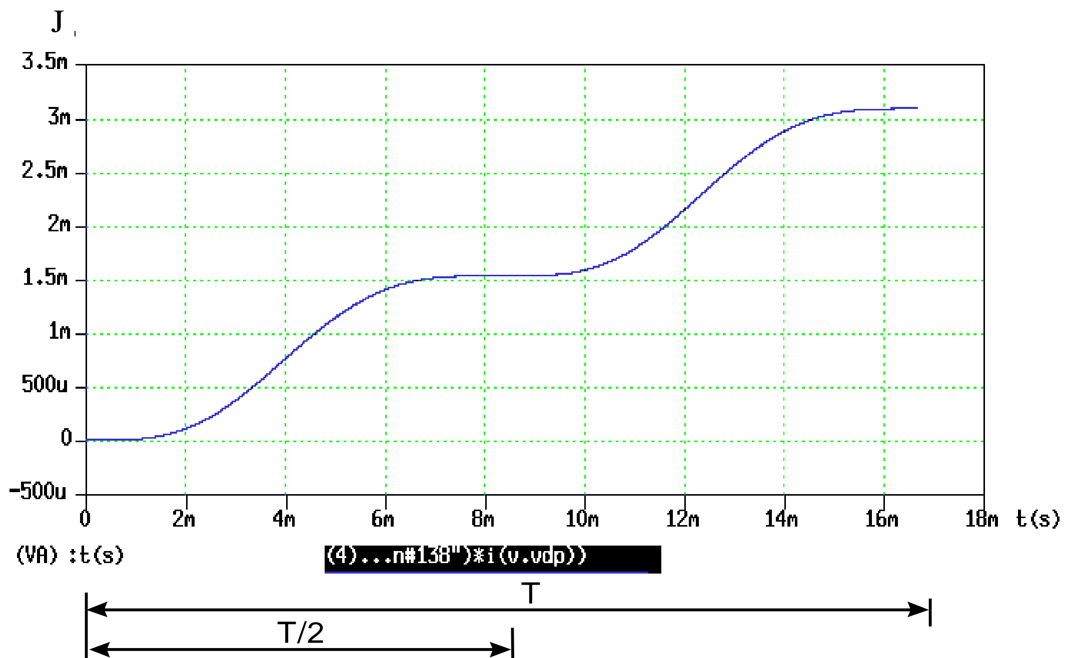


Fig.3.2. Integration of diode v(t)·i(t) in PFC circuit

$$Pmos = \frac{1}{T}\int (id \cdot Vds) \cdot dt \quad (3.2)$$

$$= \frac{Energy(at \cdot t = T) - Energy(at \cdot t = T/2)}{T/2}$$

$$= \frac{9.4 - 4.6}{8.33} = 0.58w$$

3.1.2. Diode Loss

The diode model from the *Saber* library is used for circuit simulation. The integration of the diode *i(t)×Vdp(t)* is found within half a line cycle as shown in Fig. 3.2, and the diode loss can be estimated as Eq. (3.3).

$$Pdiode = \frac{1}{T}\int (i \cdot Vdp)dt \quad (3.3)$$

$$= \frac{Energy(at \cdot t = T) - Energy(at \cdot t = T/2)}{T/2} = 0.19w$$

3.1.3. Rectifier Loss

The bridge rectifier DF-06 cannot be found in the *Saber* component library. Thus the equivalent circuit shown in Fig. 3.11 is used to estimate the rectifier loss. The bridge current of PFC circuit can be found by simulation as shown in Fig. 3.4. And rectifier loss is calculated according to Eq. (3.4).

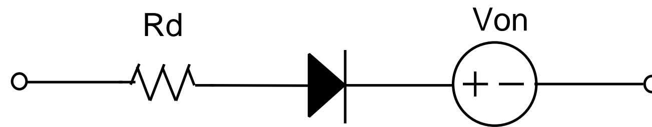
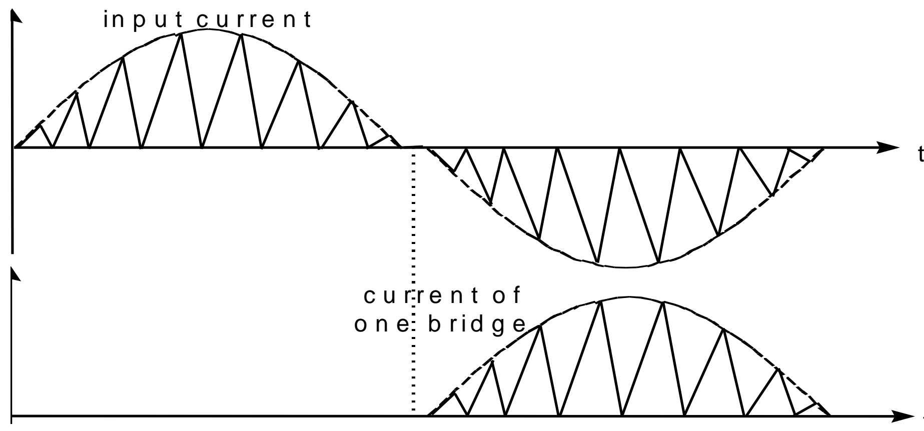


Fig.3.3. Rectifier model for loss calculation

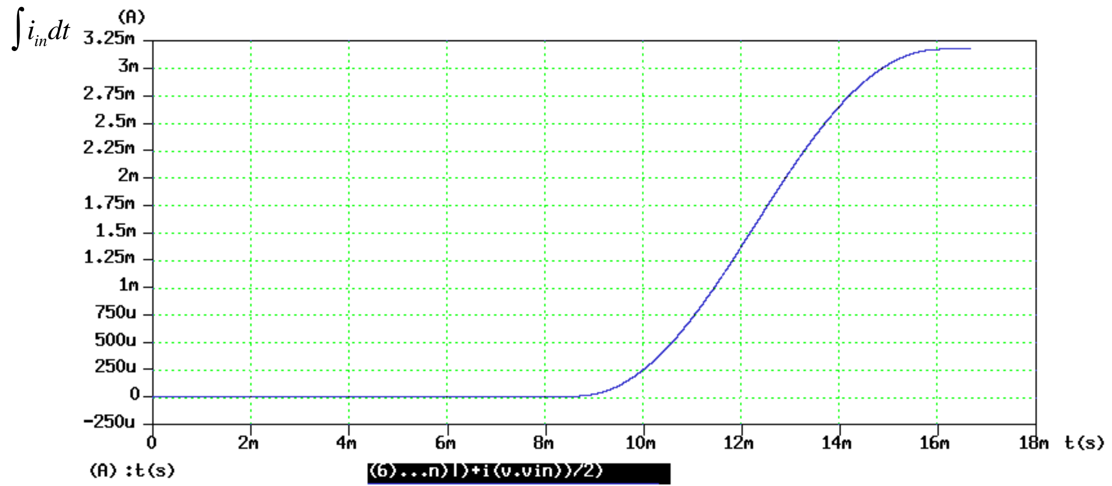
$$\Pr ect = \frac{4}{T}\int (i_{in} \cdot v)dt = \frac{4}{T}\int i_{in} \cdot (i_{in} \cdot Rd + Von)dt \quad (3.4)$$

$$= 4(\frac{Von}{T}\int i_{in}dt + \frac{Rd}{T}\int i_{in}^2 dt) = 0.86w$$

where, Von=0.7(V) & Rd=0.15Ω.



(a)



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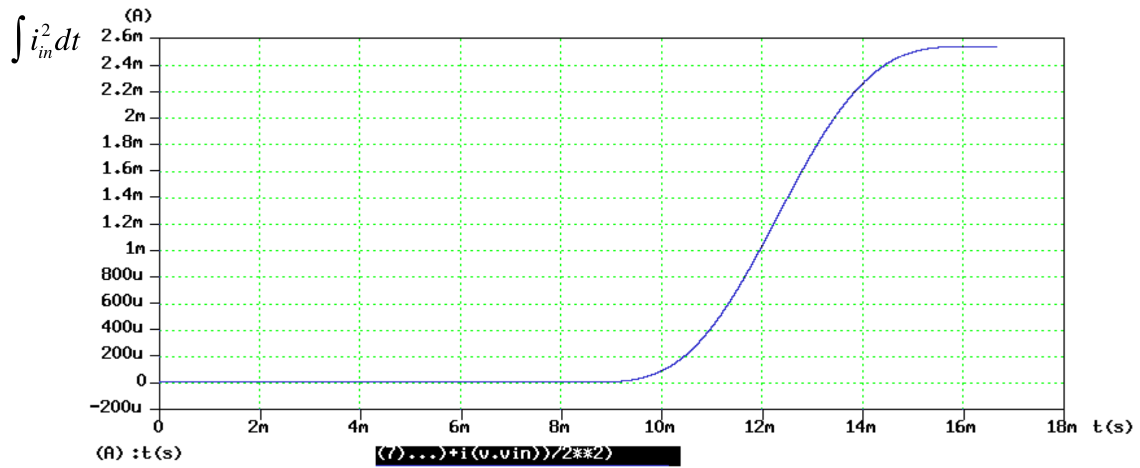


(c)

Fig.3.4 (a) Input current and rectifier bridge current (b) $\int i_{in} dt$ (c) $\int i_{in}^2 dt$

3.1.4. Output Capacitor Loss Calculation

Capacitor loss is due to its ESR. The current waveform of the output capacitor is shown in Fig. 3.6(b). It contains both the low frequency and high frequency components. Because the capacitor ESR value changes greatly from low frequency to high frequency, the low frequency and high frequency part of the capacitor current needs to be calculated. The capacitor loss is calculated by summarizing its low frequency loss and high frequency loss. As the first step, the low frequency elements and high frequency elements for output capacitor is estimated as follows.

For the PFC circuit, The frequency spectrum of capacitor current can be found by FFT function in *Saber*. The spectrum of capacitor current is in the multiplier of the half line frequency *120 Hz,* and the magnitude is also modulated by the switching frequency *250 kHz*. Because the capacitor ESR value decreases above *100 kHz*, the current harmonics below *100 kHz* is defined as low frequency components, for which a large ESR value should be used. The low frequency components (between *120 Hz and 200 kHz* can be read from the spectrum, which are listed as the following:

Harmonic number *k:*	*0*	*1*	*2*	*3*	*4*	*5*	...
Amplitude of harmonic *i(k):*	*0m*	*110m*	*60m*	*3m*	*1m*	*0 ...*	...

Thus the rms current for low frequency components is calculated by:

$$I_{rmsl} = \sqrt{I_o^2 + \frac{1}{2}\sum_{k=1}^{10} I_k^2} = \sqrt{\frac{1}{2}[(110m)^2 + (60m)^2 + ... + (1m)^2]} = 99mA \tag{3.5}$$

The high frequency components are found by subtracting the low frequency components from the total current. The total capacitor rms current of the PFC circuit is calculated by integration in Fig. 3.5(c):

$$i^2_{crms} = \frac{1}{T}\int \quad i_c^2 \, . \, dt \tag{3.6}$$

We have $i^2_{crms}=0.135$. Thus the high frequency rms current is:

$$I_{rmsl} = \sqrt{(total.rms)^2 - (lowfreq.rms)^2} \tag{3.7}$$

$$= \sqrt{I_{crms}^2 - I_{rmsl}^2} = 0.35 \text{ A} \qquad \text{using Eq.(3.5) and (3.6)}$$

Total loss of the capacitor is the summation of low frequency loss and high frequency loss. Thus,

$$Pesr = (lowfreq\ I_{rms})^2.R_{lowf} + (highfreq\ I_{rms})^2\ R_{highf}$$

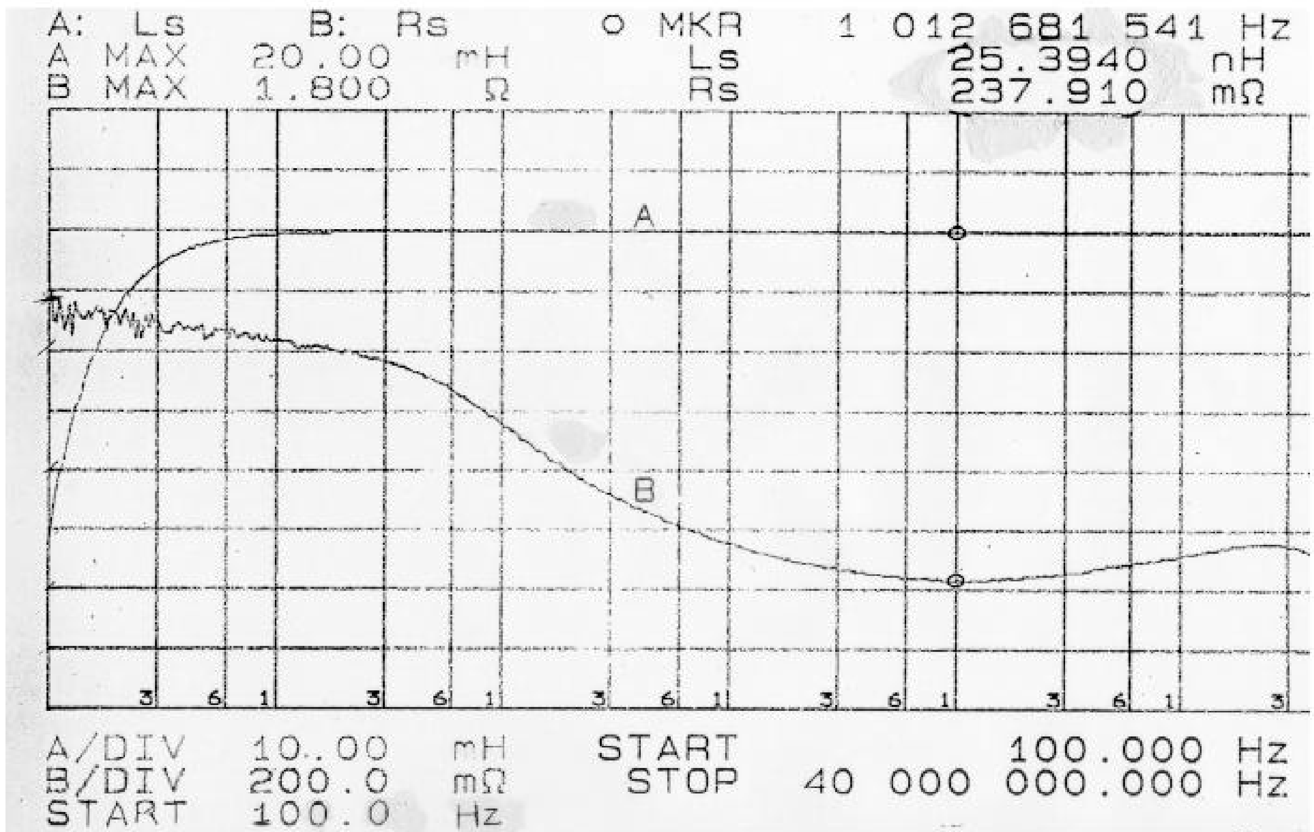
$$= I_{rmsl}^2 \cdot R_{lowf} + I_{rmsh}^2 \cdot R_{highf} \qquad (3.8)$$

From Eq.(3.6), have low frequency rms current $I_{rmsl} = 99\ mA$

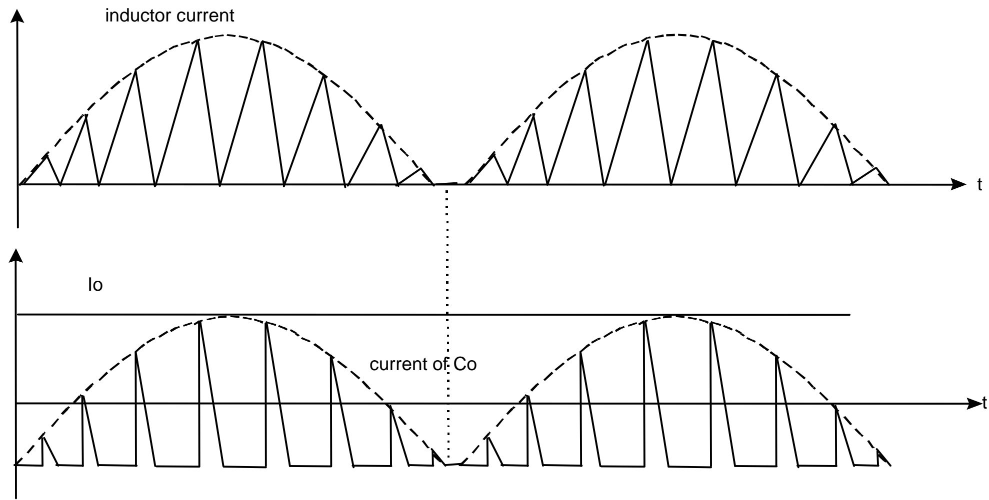
From Eq.(3.7), have high frequency rms current $I_{rmsh} = 0.35\ A$

While from the measured data shown in Fig. 3.5(a), we have $R_{lowf} = 1.8\mathbf{W}$, $R_{highf} = 0.3\mathbf{W}$, for capacitor. Thus

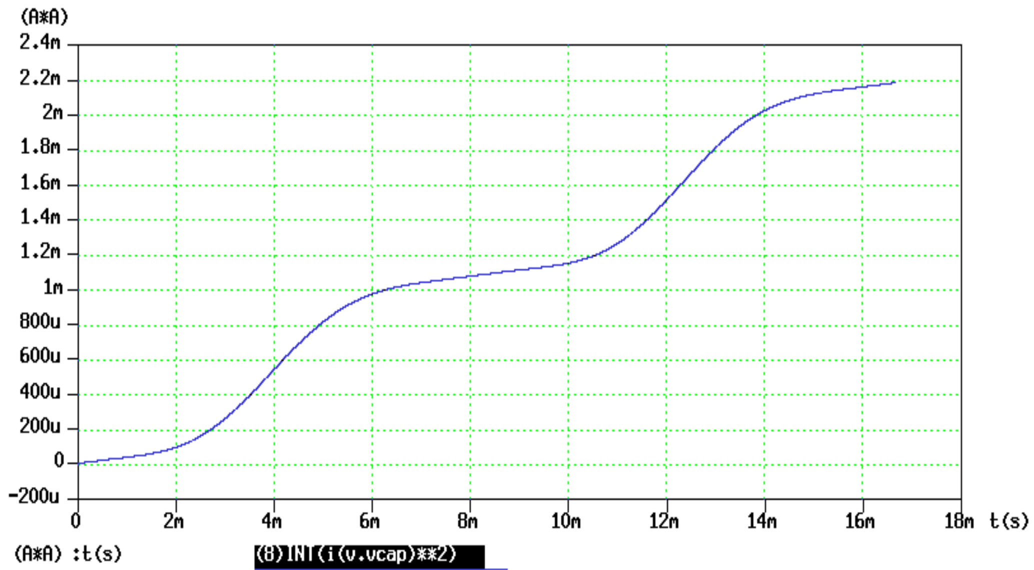
$$Pesr = (99)^2.\ R_{lowf} + (0.35)^2.\ R_{highf} = 0.1w$$



(a) Measured impedance characteristics of Co



(b) Current of Co



(c) Integration of i^2(co)

Fig. 3.5 Output capacitor loss

3.1.5. Inductor Loss Estimation

An air-gaped EI core is used for the planar inductor, and a multi-layer flex circuit (MFC) structure is used to fabricate the planar windings. Inductor core loss is estimated by an empirical equation, while the winding loss is calculated by FEA methods. Two issues are related to winding loss estimation: one is the fringing effect of air-gap, and the other is multi-excitation frequency of the PFC circuit. The following equations and results are extracted from reference [17].

Due to the fringing effect of the air-gap, conductor eddy current loss is greatly increased, which constitutes an important part of winding loss. Due to this effect, the 1D analytically approximated solutions are not available for winding loss estimation. However, by using the FEA simulation tool of *Maxwell Field Simulator*, inductor winding loss can be estimated. The high frequency skin effect, proximity effect and fringing effect that contribute to the winding loss are included in this estimation. Equivalent resistance is found for the conductors by using FEA, and then the copper loss can be calculated.

Due to the effect of the air-gap, eddy current loss is high when a conductor is close to the core air-gap and the excitation frequency is high. Thus the conductor loss is different for different positions. In the 2D field simulator, the inductor is modeled as a structure of infinite length in the *z*-direction, which means that the 2D solver treats the entire winding structure as if it exists within the core window. The equivalent winding resistance (Ω/m) for low frequency excitation is approximated by the value at *120 Hz,* while the high frequency resistance is approximated by the value at *200 kHz.* The calculated winding resistance by FEA methods is summarized in Table 4-2. It is seen that at high excitation frequency, the conductor loss is a function of its position due to eddy current effect.

For a PFC circuit, there are both high frequency and low frequency components in magnetic field excitation. The *rms* values for the high frequency and low frequency components are calculated as following according to [17].

$$I_{rms.low\text{-}freq}=0.8132(A)$$

$$I_{rms.high\text{-}freq}=0.4695(A)$$

Winding loss at *60 w* output is calculated as Eq. (3.9),

$$P_{conductor} \approx I^2_{rms,low-freq} \cdot R_{dc} + I^2_{rms,high-frq} \cdot R_{ac(200kHz)} \tag{3.9}$$

At high frequency, the conductor close to the air-gap has a larger resistance, and thus copper loss is higher. Calculated loss for each conductor is shown in Fig. 3.6 versus the conductor position. For the planar inductor there are 27 turns in total, which are divided into 3 blocks (w1~w3) in Fig. 3.6. Each block has 9 turns, which are layers 1~9 from bottom to top.

Therefore, the copper loss within the window area is calculated to be *0.462(w)*. For the winding sections that wrap around the outer section of the core, the fringing effect is significantly smaller than that within the window area. The copper loss is estimated to be 30% of that within the window area. By empirical equation, we have

$$Pcore=0.14(w)$$

The total loss is

$$Pinductor=Pwinding+Pcore=0.74(w)$$

3.1.6. Summary of component losses for *60 w 250 kHz* PFC circuit

$P_{MOSFET} = 0.58w$

$P_{diode} = 0.19w$

$P_{rectifier} = 0.86w$

$P_{inductor} = 0.74w$

$P_{outputcap} = 0.1w$

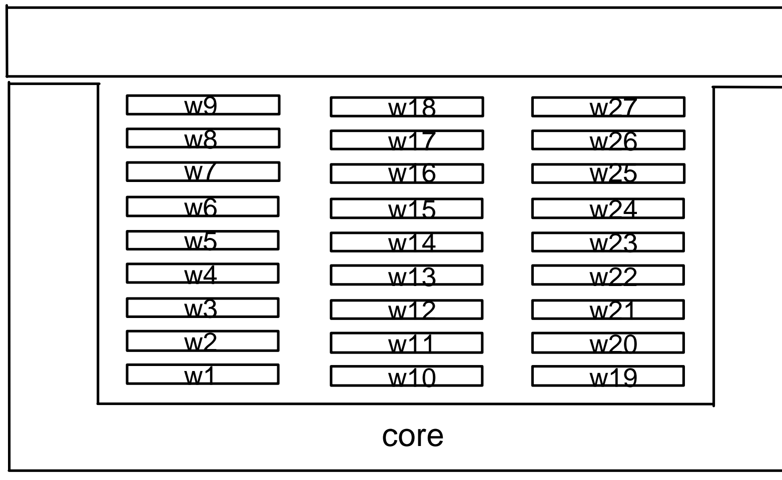
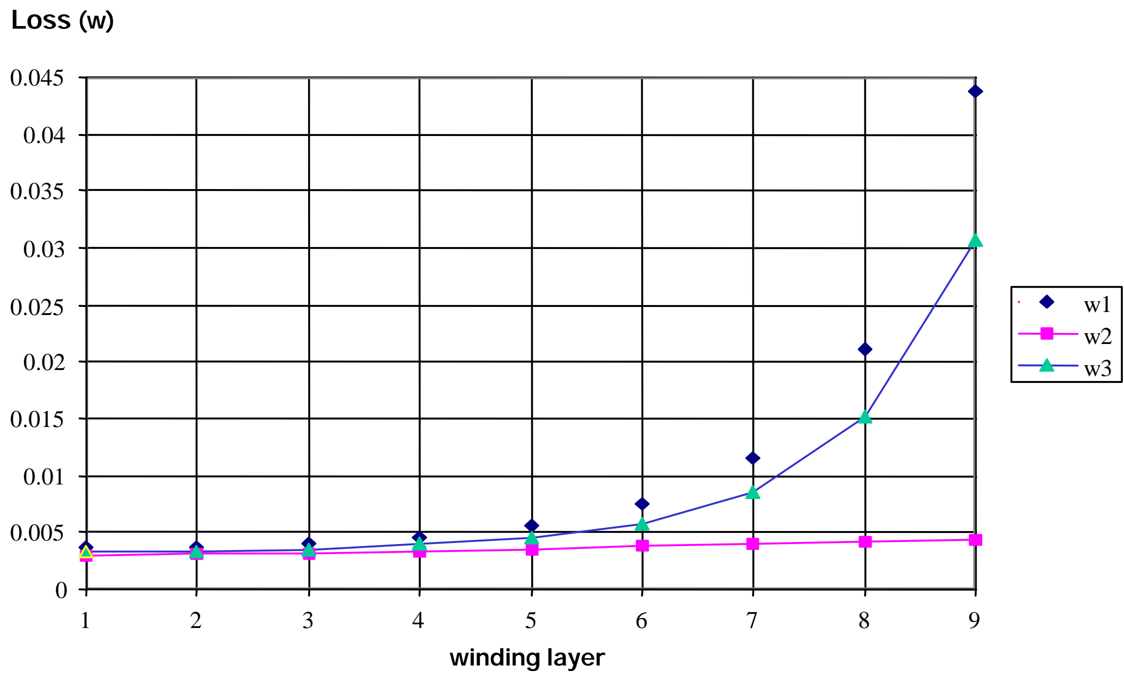


Table 3-1. Equivalent resistance of conductors (from reference 17)

conductor	resistance @120Hz	resistance @200Hz
w1	0.1916	0.3616
w2	0.1916	0.3811
w3	0.1916	0.4484
w4	0.1916	0.478
w5	0.1916	0.805
w6	0.1916	1.2326
w7	0.1916	2.1546
w8	0.1916	4.344
w9	0.1916	9.466
w10	0.1916	0.2345
w11	0.1916	0.247
w12	0.1916	0.2716
w13	0.1916	0.3075
w14	0.1916	0.3533
w15	0.1916	0.4055
w16	0.1916	0.4576
w17	0.1916	0.5024
w18	0.1916	0.5262
w19	0.1916	0.2828
w20	0.1916	0.299
w21	0.1916	0.3463
w22	0.1916	0.4344
w23	0.1916	0.5877
w24	0.1916	0.8752
w25	0.1916	1.4993
w26	0.1916	2.9908
w27	0.1916	6.5325



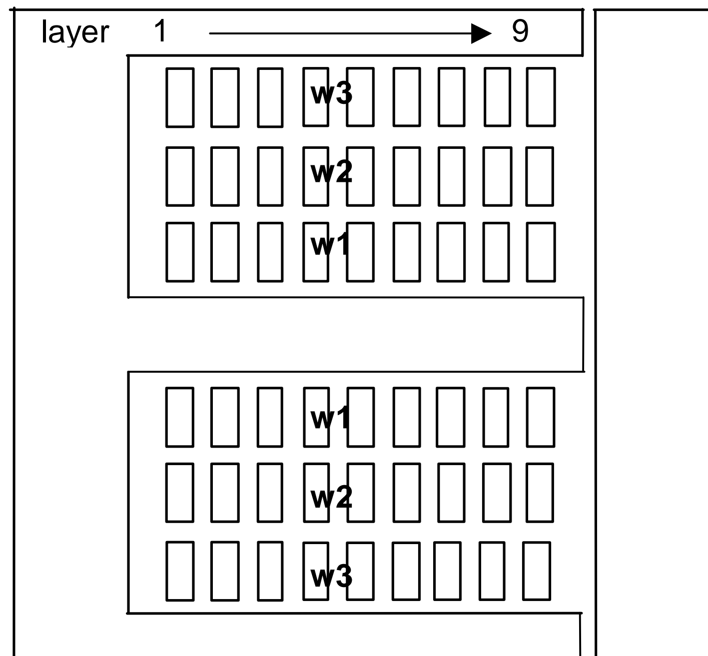


Fig.3.6. Conductor loss versus position (from reference 17)

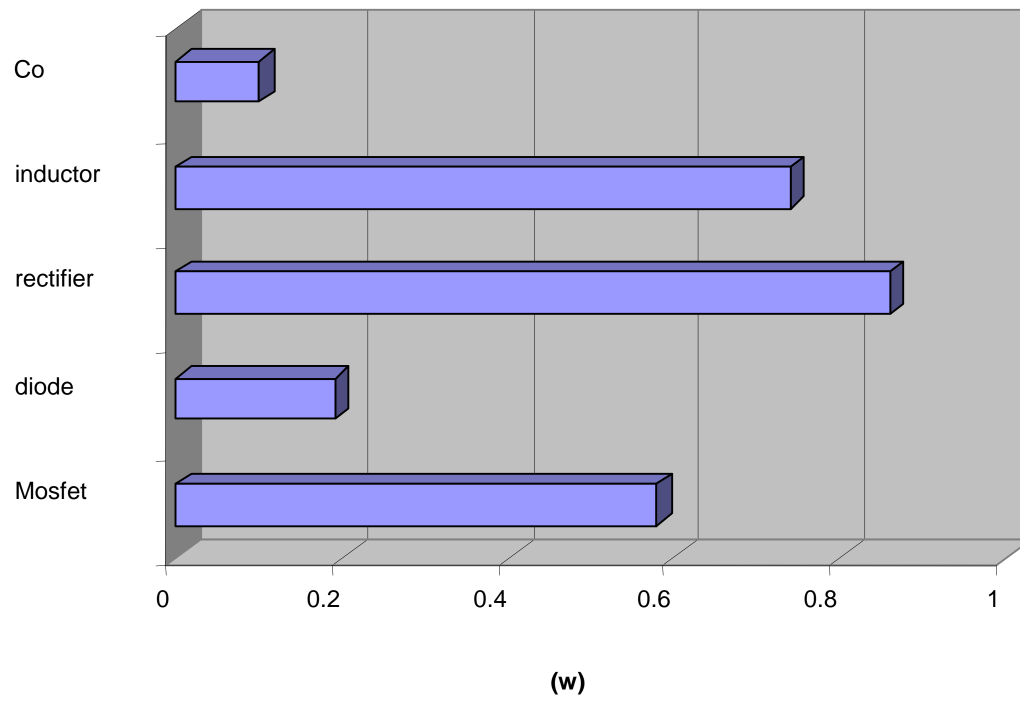


Fig.3.7. Component power loss of the boost PFC circuit

3.2. Thermal Modeling and Analysis

In this section the effort toward thermal modeling and thermal design improvement is introduced**.** Using the boost PFC circuit as an example, Multi-level thermal models are built for the boost circuit. The objective of board level simulation is to study the thermal interactions between the components and the cooling characteristics of the circuit. Therefore, a simplified uniform heat body is used as the thermal model for the components. The component surface temperature can be predicted by board level simulation. While by component level simulation, the thermal behavior and hot spots temperature within a component can be found.

For a hybrid circuit, the device's thermal energy is first conducted to the substrate and then dissipated to the ambient. Therefore the thermal characteristics between the device and substrate need to be properly defined. The interconnection traces and PADs on substrate work as heat spreaders for the components. Their effects are analyzed and modeled in Section 3.2.1. From the thermal point of view, a wide trace provides good thermal spreading. However, from the EMI point of view, it is not good for the traces to have a very large area, as shown in Section 2.3. Both EMI and thermal behavior must be taken into consideration.

In Section 3.2.2, the thermal models for Mosfet, diode, rectifier, capacitors and the planar inductor are described. Both the detail component models and the simplified models are introduced. The simplified model is deduced from the detail component model. The procedure is described. In Section 3.2.3, thermal performance of the circuit is studied by simulation with *Flotherm*. Improved thermal management for better performance is investigated. The hot spot temperature within the MOSFET, diode and other components can be predicted by performing thermal simulation using the detail component models. Usually the temperature profile and hot spots temperatures within the magnetic components are unknown. As an example here, by using the loss information from the FEA analysis, and the thermal models built for the planar inductor, the temperature profile within the planar inductor is predicted by *Flotherm* simulation.

3.2.1. Model of Copper Traces

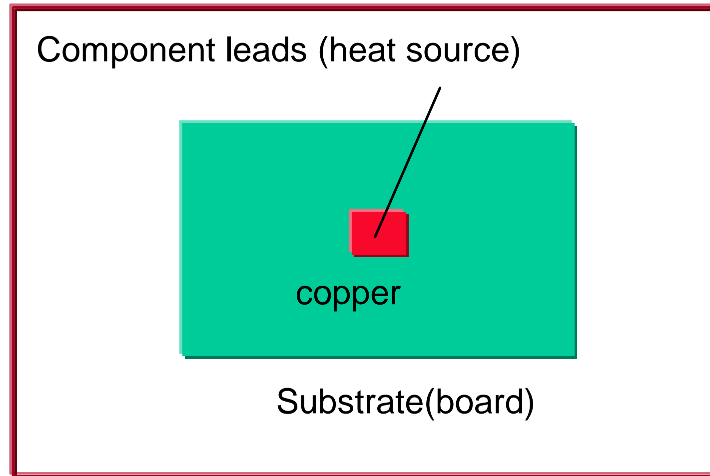
Because of its high thermal conductivity, copper traces on the substrate improve heat spreading and dissipate thermal energy. The copper traces can be modeled in two ways. One is the average model, in which the substrate thermal conductivity is increased to take into account the effect of copper trace [23]. For the other method used here, the thermal characteristics between the component and substrate is modified to take into account this effect, which can be defined as a local model. The choice of the average model or the local model depends on the geometry and thermal properties of the board s.o. traces, which will be discussed below.

As the first step, the spreading effect of copper traces is analyzed. The problem can be analyzed by the model shown in Fig. 3.8. It is obvious that the copper heat spreading effect dominates, when thermal resistance of the copper traces is much less than the resistance when heat is transferred by the substrate. However, as the copper trace geometry exceeds certain limit, the spreading effect is diminishing small.

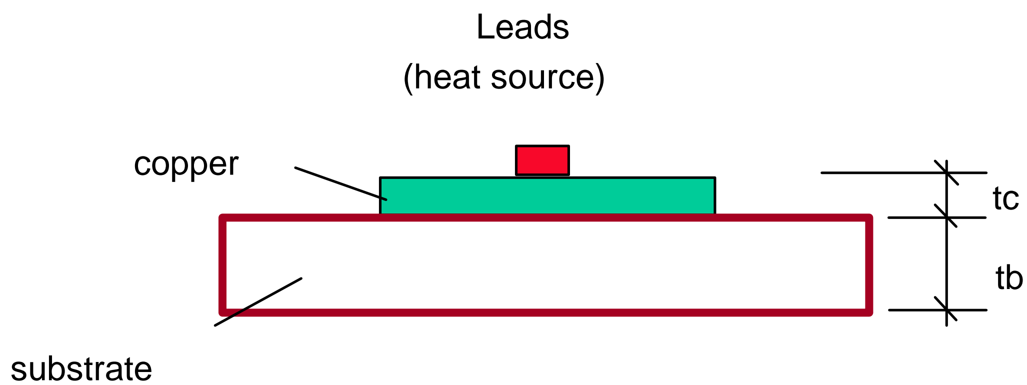
Two cases are simulated. In the first case, the length and the width of the heat source are about the same. Heat is spread evenly in all direction. By simulation, the heat source temperature versus copper area is predicted as Fig. 3.10. Three kinds of substrate material are applied. It is seen that the effectiveness of copper trace is minimized beyond some value. With the further increase of copper area, the heat source temperature reduction is minimal.

Also, for different substrate material the effective copper area is different. For the substrate with higher thermal conductivity this value is minimized, which means that the required copper area is reduced for the substrate with higher *K*.

The second case is shown in Fig. 3.11, in which the length (y) of leads is much greater than the width (x). The simulation result for alumina substrate is shown in Fig. 3.12.



(a) Top view



(b) side view

Fig.3.8. Heat source on the copper trace

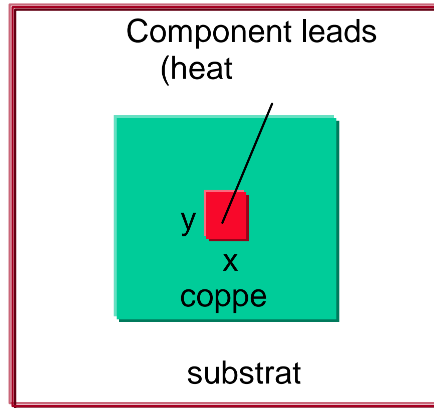


Fig.3.9 Model for case I

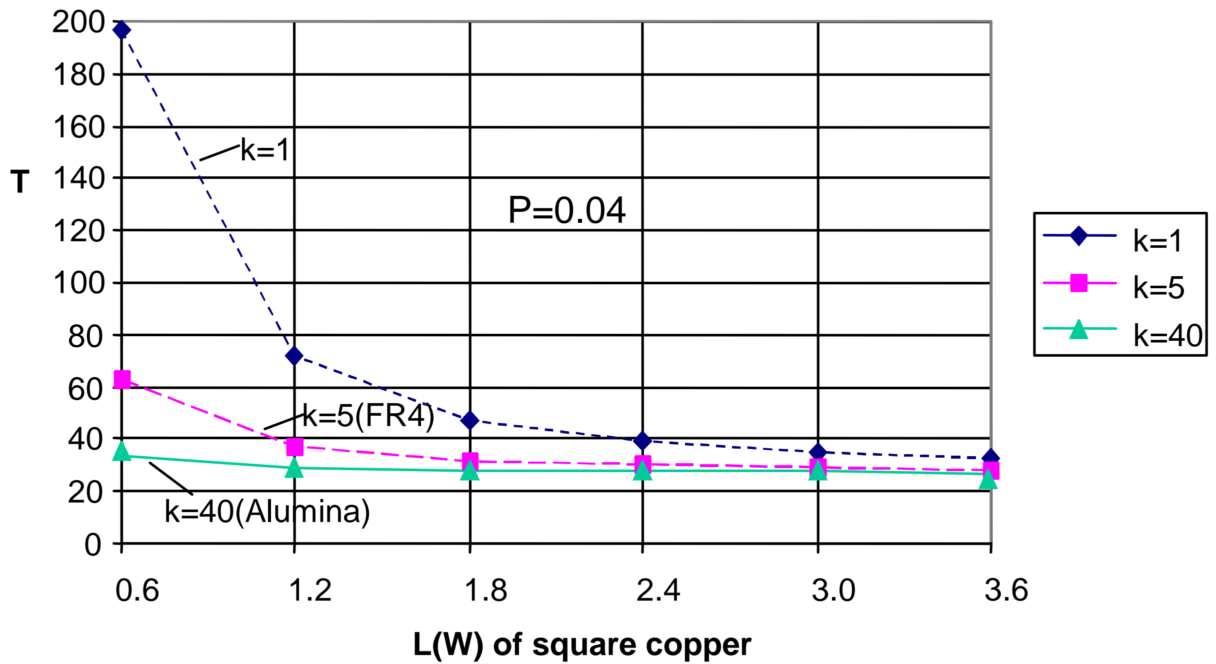


Fig. 3.10 Heat source temperature versus PADs area for case I

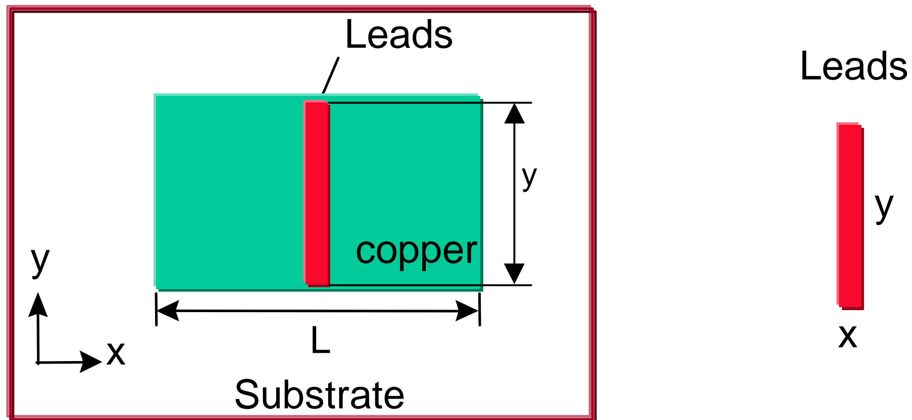


Fig.3.11. Model for case II

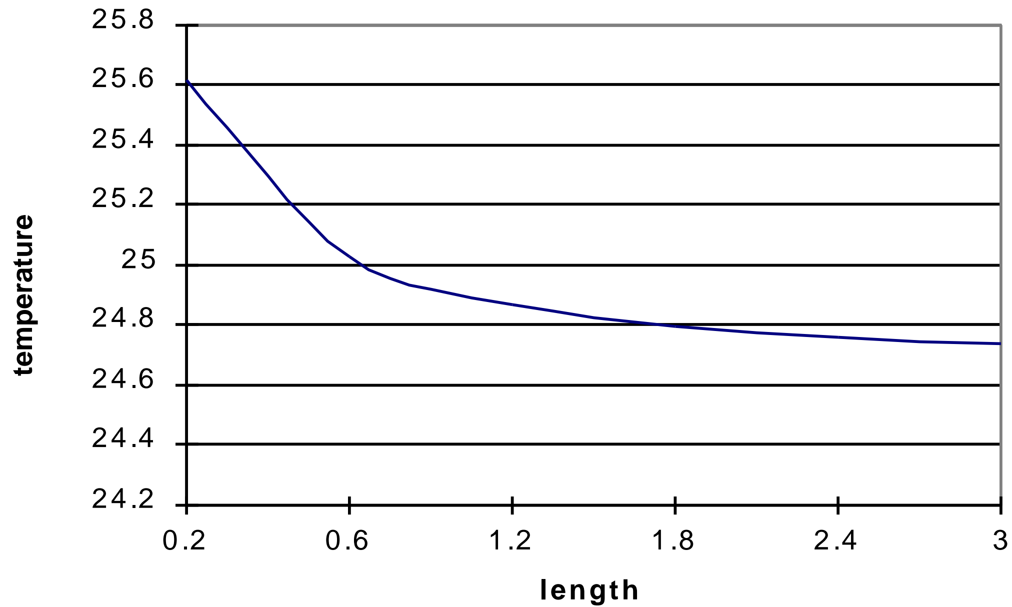


Fig.3.12. Heat source temperature versus PADs length in case II

Significance of maximum radium:

In general, the larger the area of the interconnection trace the better the heat spreading effect, but the worse the common-mode EMI. However, as the trace geometry exceeds certain limits, the heat spreading capability is diminishingly small. Therefore, this limit should serve as the guidance for layout, because any increase in the copper trace only hurts EMI performance and occupies board area, while contributing little to the heat spreading capability. In summary, for the board under study the most effective copper area is r£ $0.5r_{max}=1mm$ for case A, and l£ $0.5l_{max}=0.75mm$ for case B. In the layout design the above conditions should be met. As noted above, as the number K_c/K_b increase, for example, using a board with lower thermal conductivity, the required copper area should be increased to spread the heat effectively. As a result, the EMI performance may be aggravated due to this modification.

Model the copper effect:

Based on the previous calculation, we see that due to the high thermal conductivity of alumina substrate, the spreading effect of the copper trace is very limited for this hybrid board. The required PADs area for effective heat spreading is small. Thus a local model can be used to calculate the effect of copper trace, in which the thermal resistance between the device and substrate is modified. By simulation-comparison iteration between the device model and simplified model introduced in the following sections, the equivalent thermal resistance can be found.

3.2.2. Device Thermal Model

For a hybrid board, the thermal energy of the device is conducted to alumina substrate via the leads or heat-sink, and then dissipated to the ambient. Thus the thermal characteristics between the component and substrate need to be properly modeled. For board level simulation a simplified uniform heat body is used to model the components. And the thermal characteristic between the component and substrate is defined by a equivalent thermal resistance between the heat body and substrate, which is shown in Fig. 3.13. All the power loss information is obtained from section 3.1.6 for a *250 kHz, 60 w* PFC circuit.

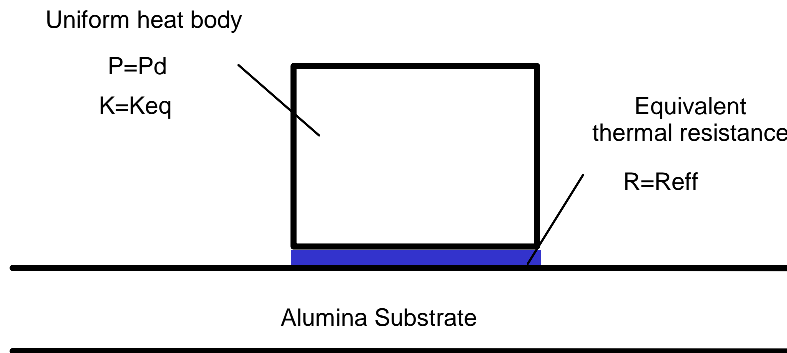


Fig. 3.13. Equivalent device model

3.2.2.1. *Diode Model*

The structure of the diode is shown in Fig. 3.14. Practically, the thermal energy of the silicon chip is conducted to the substrate via the leads, encapsulation material and air-gap, and is then dissipated to the enclosure and ambient. The thermal conduction path is shown in Fig. 3.8, in which *R1* represents the thermal resistance of leads, and *R2* represents the thermal resistance of the air-gap and encapsulation material. A detailed thermal model can be built for the diode

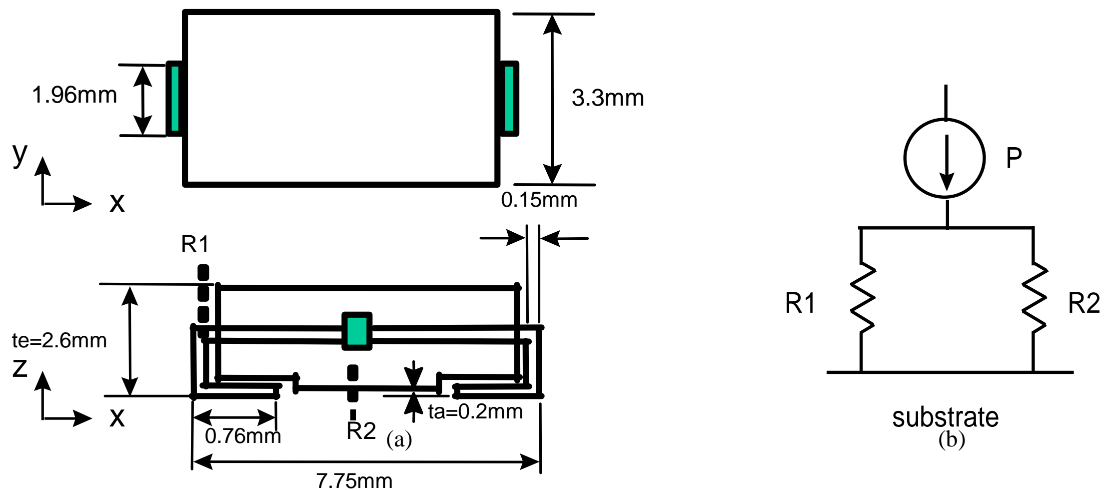


Fig.3.14. (a) Diode structure (b) thermal conduction path

based on its structure, and material property. However, using the detailed model, it takes a long time and excessive memory to simulate. For board simulation, an equivalent simplified model is proposed as shown in Fig. 3.7. The effective thermal resistance R_{eff} can be obtained by theoretical calculation and simulation iteration as explained below.

Step 1. Estimate R_{eff} by theoretical calculation

The thermal resistance R_{th} can be approximated. *R1* and *R2* is approximated by the following equations:

$$R1 = \frac{t1}{K1 \cdot A1} \tag{3.11}$$

$$R2 = \mathrm{Re} + Ra = \frac{te}{Ke \cdot A2} + \frac{ta}{Ka \cdot A2} \tag{3.12}$$

Where,

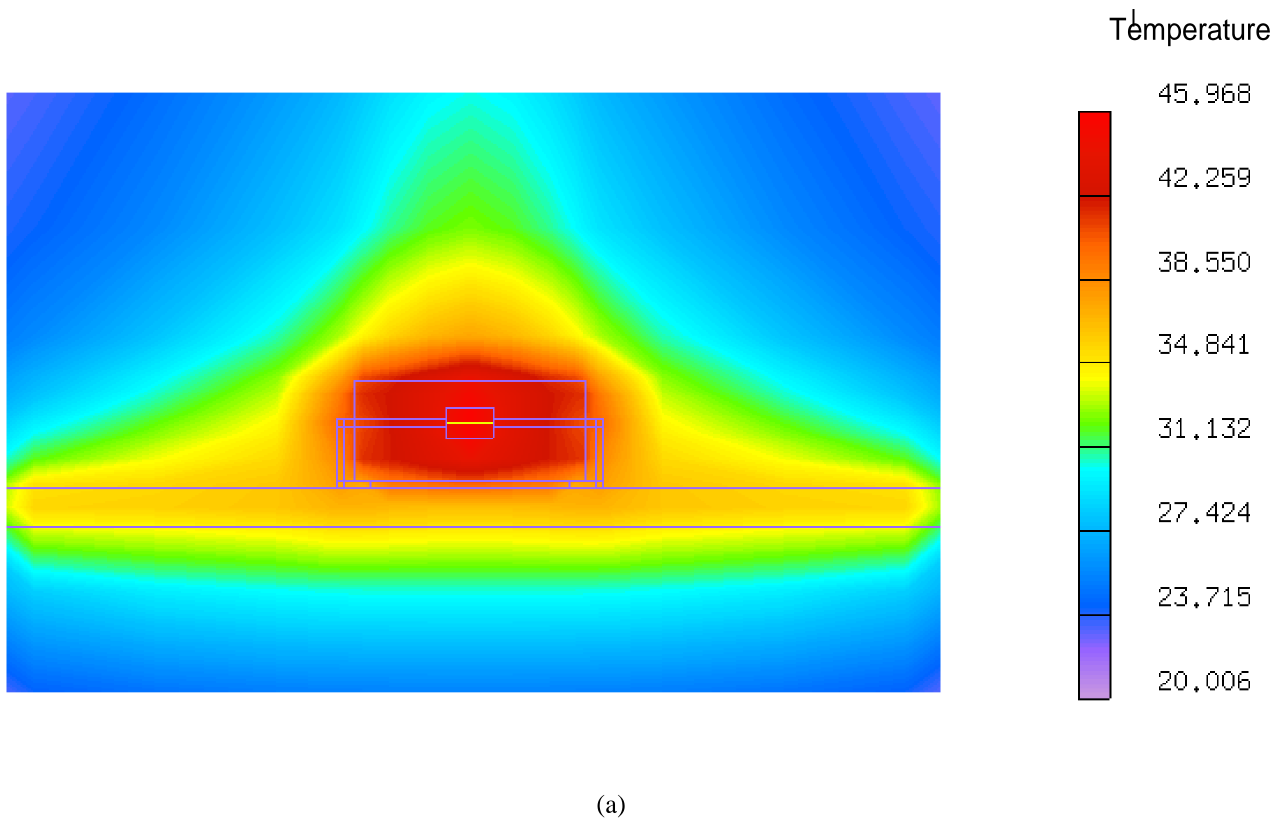
t1 :	the length of leads, *6.62 mm*
A1 :	section area of leads, $0.44\ mm^2$
K1 :	thermal conductivity of leads, *150w/mK*
te :	encapsulation thickness, *1.4mm*
Ke:	thermal conductivity of encapsulation, *1.58w/mK*
A2 :	diode foot print area, $37mm^2$
ta :	air-gap thickness, *0.2mm*
Ka :	thermal conductivity of air, *0.026w/mK*

The total resistance is *R1* in parallel with *R2*, and we have $Ra >> R$; thus:

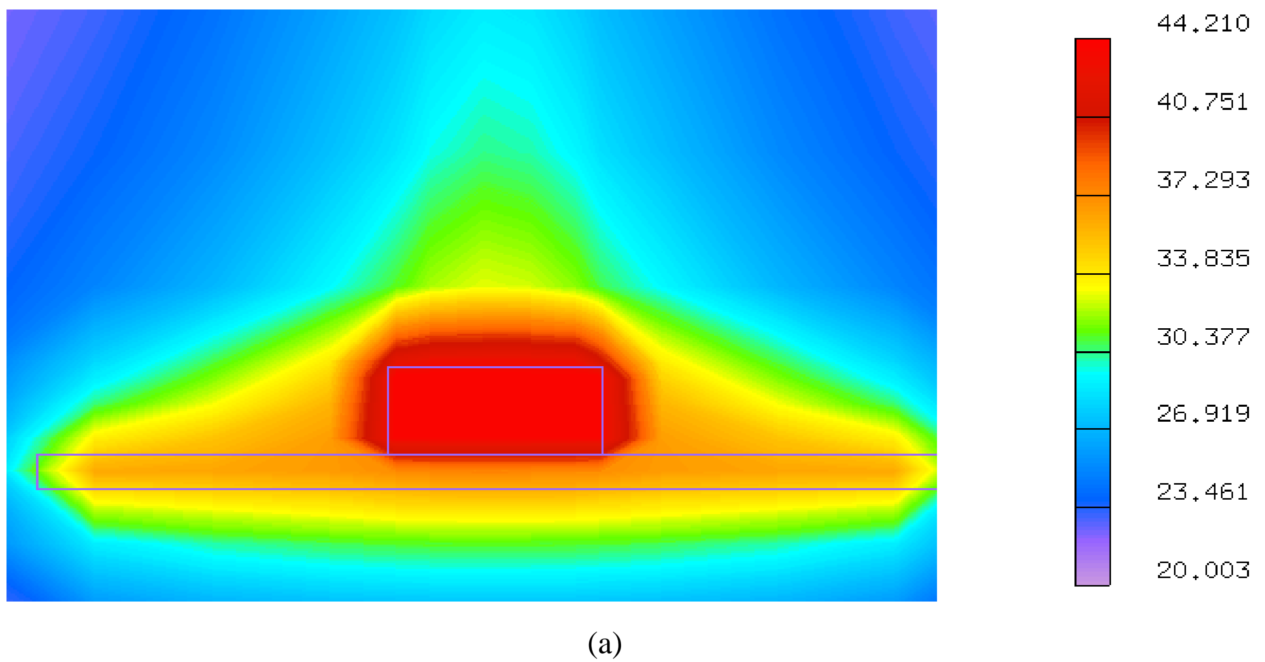
$$\frac{1}{R_{eff}} = \frac{1}{R1} + \frac{1}{R2} = \frac{K1A1}{t1} + \frac{KaA2}{ta} = \frac{K1A1}{t1}\left(1 + \frac{Ka \cdot A2 \cdot t1}{K1 \cdot A1 \cdot ta}\right) \tag{3.13}$$

Substitute the specific numbers into Eq. (3.13), and R_{eff} is found to be *67.8K/w*.

Step II. Run two separate simulations, one with simplified model, and the other with the detailed model. The PADs are also defined with the detailed model to take into consideration the thermal spreading effect. Adjust R_{eff} in the simplified model until the temperature profile on both case converges (the surface temperature of the two cases are expected to be the same). Fig. 3.15. shows the simulation results.



(a)



(a)

Fig.3.15. Temperature contour of diode (a) device model (b) equivalent device model

By simulation iteration, the effective thermal resistance is found to be *48.8 K/w* without PADs included. And the value is *43 K/w* with PADs included.

3.2.2.2. Mosfet Model

The power Mosfet is in a D2 package, which is shown in Fig. 3.17. The metal tab performs as a heat-sink for the silicon chip. Due to its large area, the PADs spreading effect is very limited for the MOSFET (refer to Section 3.1). The thermal characteristics between the component and substrate is determined by the metal tab. R_{eff} is estimated by Eq. (3.14).

$$R_{eff} = \frac{t_m}{K_m \cdot A_m} \tag{3.14}$$

Where, $t1$: the thickness of metal tab, *0.6 mm*

$A1$: area of metal tab, $34.2\ mm^2$

$K1$: thermal conductivity of metal tab, *150w/mK*

By the simulation and comparison iteration explained in Section 3.2.2.1, the equivalent thermal resistance is found to be *0.1 K/w*, which is negligible.

3.2.2.3. Rectifier Model

The structure of rectifier is shown in Fig. 3.11. Using the same concept explained in 3.2.2.1, R_{eff} *=23.2 K/w* without PADs, and R_{eff}*=20.8 K/w* with PADs.

3.2.2.4. Capacitor Model

A multi-layer ceramic capacitor (surface-mount) is used in the circuit. Because the loss of the capacitor is relatively small, the thermal model used is simplified to a capacitor block on board. The capacitor model is shown in Fig. 3.18, in which k_{eq} is an empirical number [16].

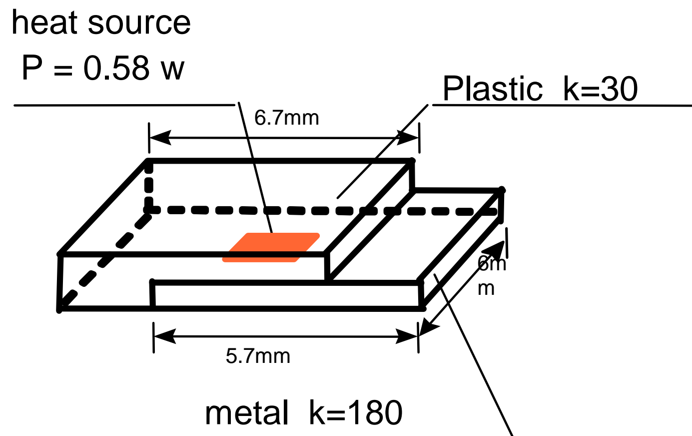


Fig. 3.16. MOSFET IRF740 with D2 packaging

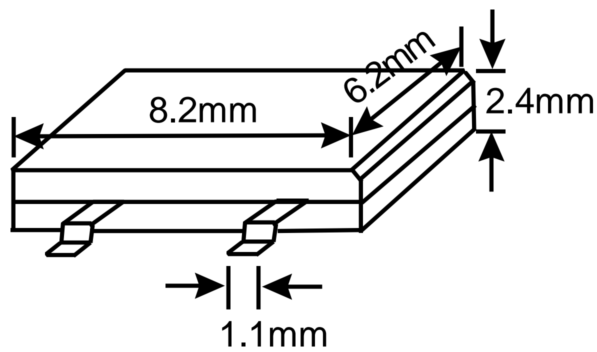


Fig. 3.17. DF06 rectifier structure

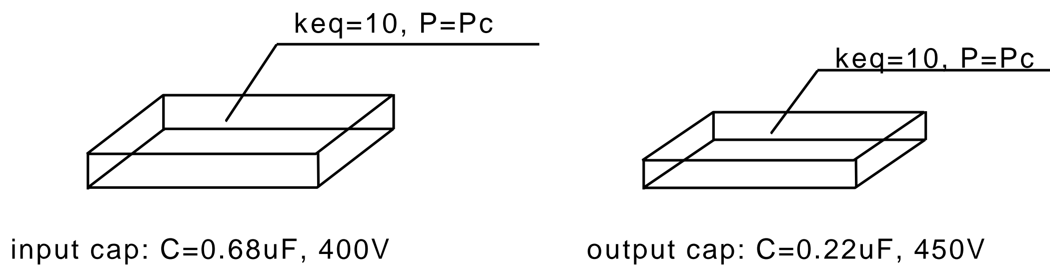


Fig.3.18. Thermal model for ceramic cap

3.2.2.5. Planar Inductor Model

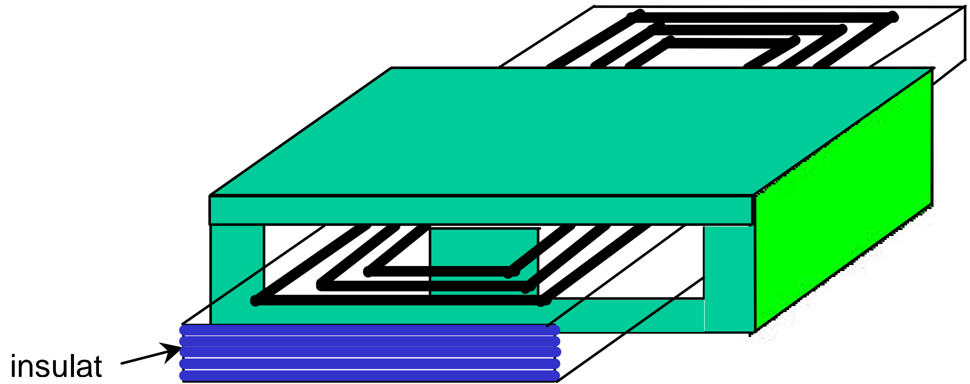
The increasing demand for power supplies with small volumes and weights results in the development of power supply circuits operating at frequencies higher than several hundred kilohertz to reduce the size of magnetic components. Due to their bulky size, the magnetic components are a crucial part of the switching power supply. There are a lot of issues related to the design of magnetic components operating at high frequencies. Due to the higher frequency, magnetic core loss, winding loss induced by fringing, proximity and skin effect increase. Higher power loss adds to the challenges of thermal design. The hot spot temperature of the inductor should be maintained below the maximum temperature to ensure proper operation.

<u>Inductor model for component simulation:</u>

As an example, component level thermal analysis is performed for the inductor to find the hot spot temperature. The inductor structure is shown in Fig. 3.19. The planar inductor is multi-layer flexible circuit (MFC) structure, and the insulator between them is polyamide. The loss of each conductor is found by the FEA method as explained in Section 3.1.5. The inductor thermal model can be built by defining its detailed structure and material property. However, it is very time consuming and may require excessive computer memory.

The inductor is simplified to the model shown in Fig. 3.20, where the multi-layer conductors and insulators are grouped into uniform bodies. Each conductor is defined as a planar source inserted within the block, because of the high thermal conductivity of copper. The internal heat transfer mechanism of the planar inductor is dominated by conduction; thus the equivalent thermal conductivity of a uniform block can be calculated by integrating the conductors and insulators.

Figure 3.21 shows the inductor winding structure and the simplified uniform blocks. Two kinds of uniform blocks are assumed; one is the equivalent block of copper and insulator (R1), and the other is the equivalent block of insulator and air. The calculation for the equivalent thermal conductivity of the blocks is shown in Fig. 3.21(b), where *Rc* is the thermal resistance of conductor, *Rd* is the thermal resistance of insulator, and *Ra* is the thermal resistance of air.



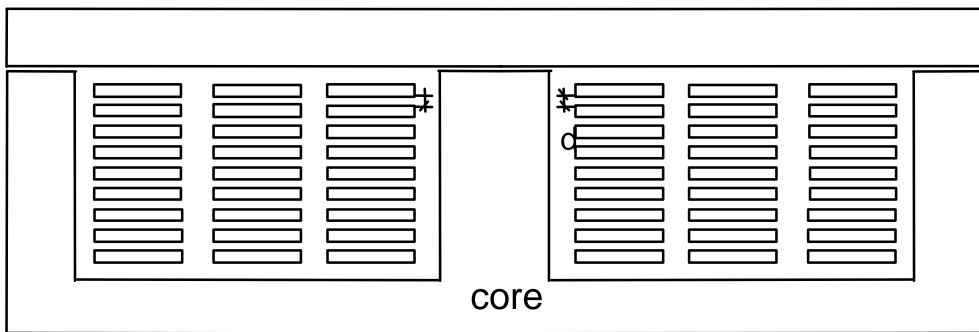


Fig.3.19. Inductor structure

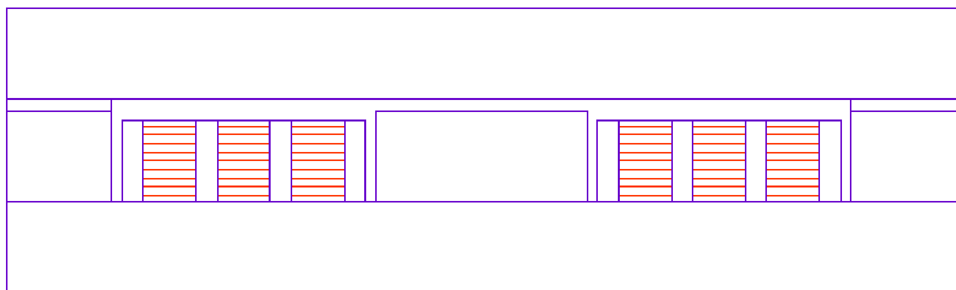
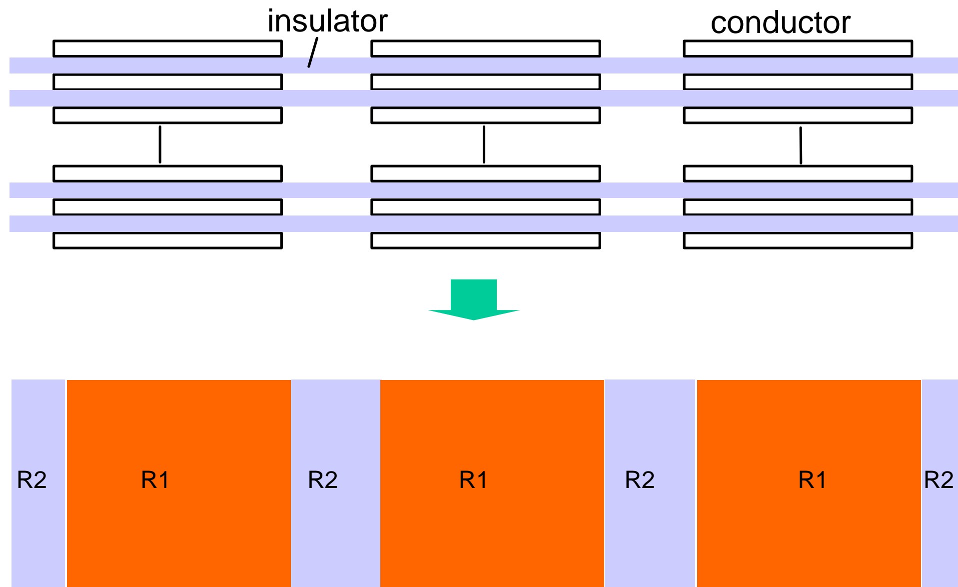
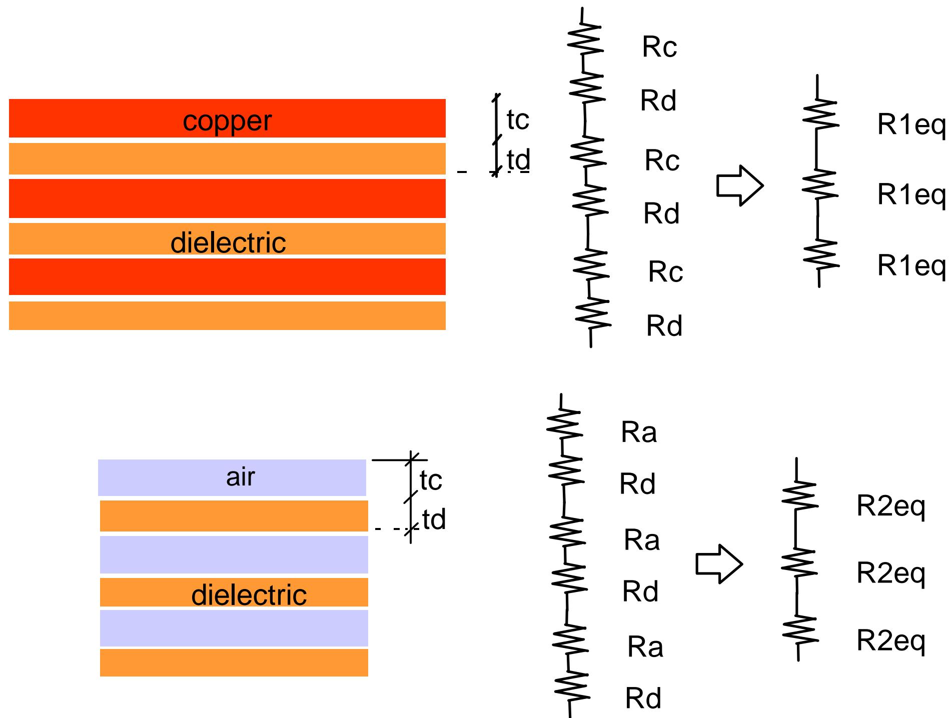


Fig.3.20. Inductor model



(a)



(b)

Fig.3.21. Equivalent conductivity calculation

We have,

$$Rc = \frac{tc}{KcA} \tag{3.15}$$

$$Rd = \frac{td}{KdA} \tag{3.16}$$

$$R1eq = \frac{tc + td}{KeqA} \tag{3.17}$$

$$R1eq = Rc + Rd. \tag{3.18}$$

Where,

tc: thickness of conductor *0.09mm*

Kc: thermal conductivity of conductor *400w/mK*

A: conductor area

td: thickness of insulator *0.0762mm*

Kd: thermal conductivity of insulator *0.2w/mK*

Keq: equivalent thermal conductivity of uniform block

Thus *Keq* for block 1 is found as:

$$\frac{tc + td}{Keq1A} = \frac{tc}{KcA} + \frac{td}{KdA} \tag{3.19}$$

$$Keq1 = \frac{tc + td}{\frac{tc}{Kc} + \frac{td}{Kd}} = \frac{1}{\frac{tc}{(tc + td)Kc} + \frac{td}{(tc + td)Kd}} \tag{3.20}$$

We have *Keq1=0.436w/mK.*

In the same way, the equivalent thermal conductivity for block 2 is found in equation (3.21).

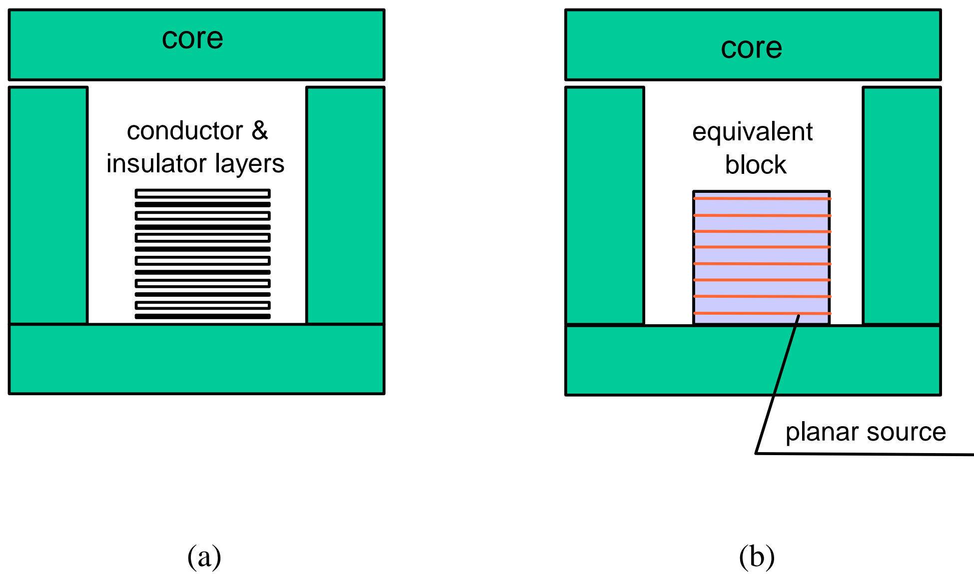
$$Keq2 = \frac{ta + td}{\frac{ta}{Ka} + \frac{td}{Kd}} = \frac{1}{\frac{ta}{(ta + td)Ka} + \frac{td}{(ta + td)Kd}} \tag{3.21}$$

We have *Ka=0.026w/mK, ta=0.09mm,* thus *Keq2=0.04w/mK.*

To investigate the accuracy of the simplified model, both a detailed model and a simplified model are defined for a six-layer winding block placed within a core, which is shown in Fig. 3.22. The detailed model gives the exact physical structure and material property, while the simplified model is built as described above. A free convection condition is assumed in the simulation. Predicted conductor temperatures for the two cases are shown in Table 3-1. It is seen that the results match very well.

Table 3-2. Temperature of case I and case II

	c1	c2	c3	c4	c5	c6
detail model	50.1	51.4	52.3	53.3	54	54.4
simplified model	50.1	51.4	52.3	53.3	54	54.4



(a) (b)

Fig. 3.22 (a) Detail model (b) simplified model

Inductor model for board simulation:

A simplified model is built for the inductor for board level simulation as shown in Fig. 3.23. A uniform winding block and a core block are defined. Loss of the winding block is the total loss of each conductors. The ferrite thermal conductivity is assigned to the core block, and *Kc=4w/mK.* The equivalent thermal conductivity of the winding block is calculated as follows. Assume *Keq=Keq1,* then run two separate simulations, one with Model I and the other with Model II. Adjust *Keq* of model II, until the temperature profile in both cases converge (the surface temperatures are expected to be the same). By simulation *Keq* is found to be *0.4 w/mK*. The model is shown in Fig. 3.22.

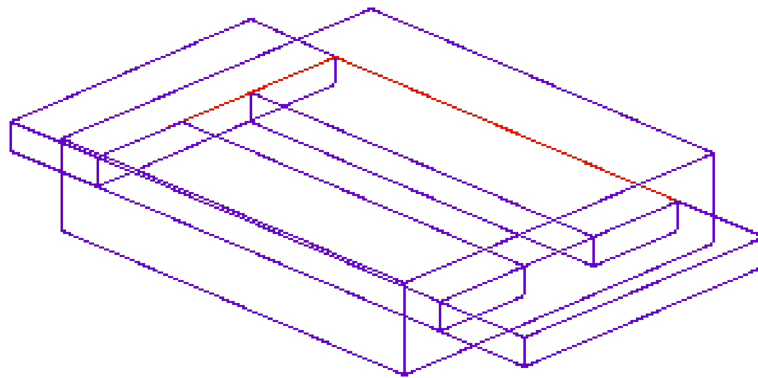


Fig. 3.23 Inductor model for board simulation

3.3. Thermal Simulation Results

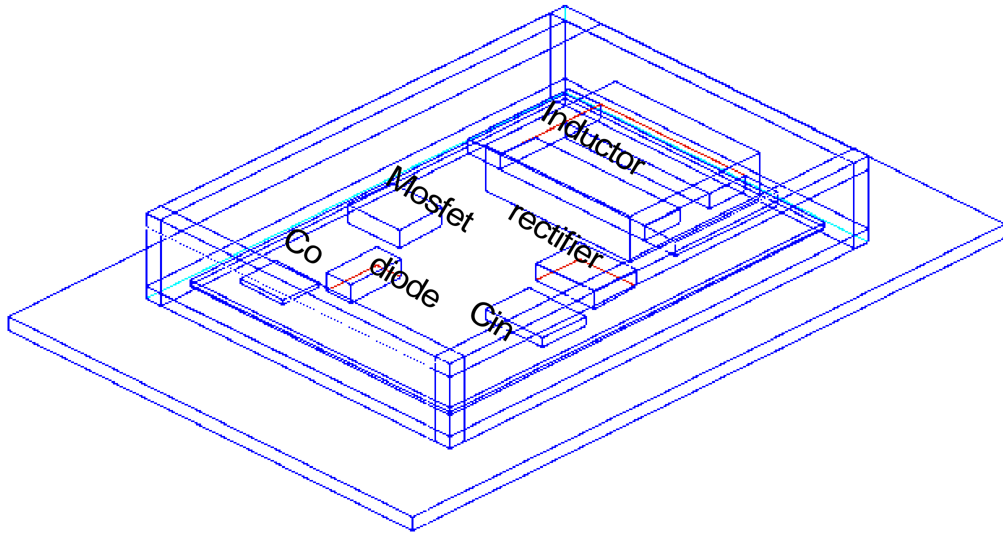
Thermal performance of the PFC circuit within a plastic enclosure is studied. The objective of the heat transfer design is to provide equipment that will transfer and dissipate thermal energy from the heat source to the energy sinks. For the case under study, heat transfer inside the enclosure is dominated by conduction, and then dissipated to the ambient by convection and radiation on the surface of enclosure. The thermal energy generated by the devices as power Mosfet, diode, rectifier, and boost inductor, is conducted to the substrate and then transferred to the enclosure. All the important components are included in the board thermal model, which either has high power loss or is temperature sensitive.

The component thermal models built in the previous section are used in the simulation. The thermal characteristics of the circuit and hot spots on the board can be studied by using this model. By using the detailed component thermal model, the temperature profile and hot spot within a component can be found. Usually the internal temperature profile of a magnetic device is unknown, which has significant influence on the converter reliability and performance. As an example here, by both the board simulation and component simulation, the hot spot temperature of the planar inductor in the boost PFC circuit can be predicted. The board thermal model and simulation results are summarized in Section 3.3.1. , while in Section 3.3.2, several examples are studied to minimize inductor temperature.

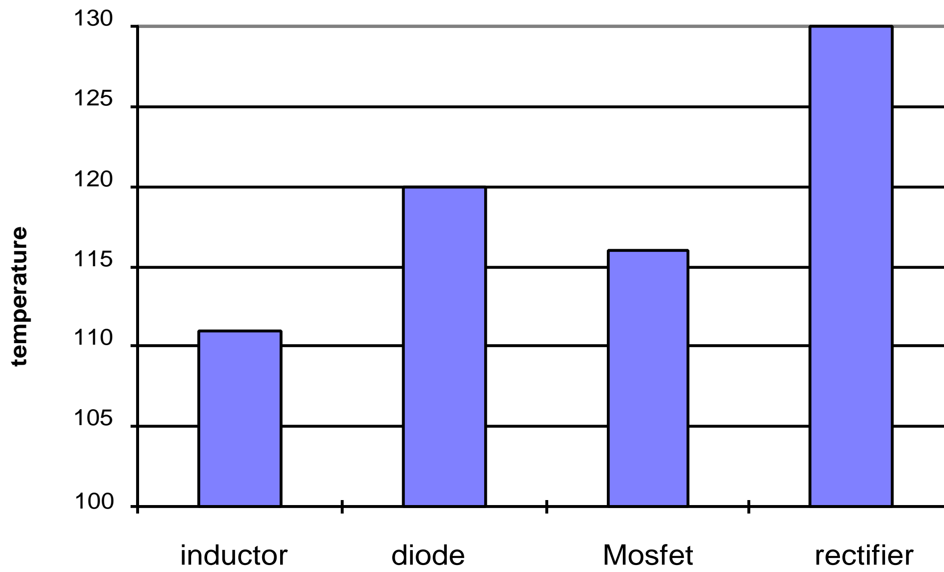
3.3.1. Temperature Prediction

3.3.1.1. Temperature Profile of The Board

The *Flotherm* thermal model for the boost PFC circuit is shown in Fig. 3.24(a). Fig. 3.24(b) shows the temperature profile of the board.

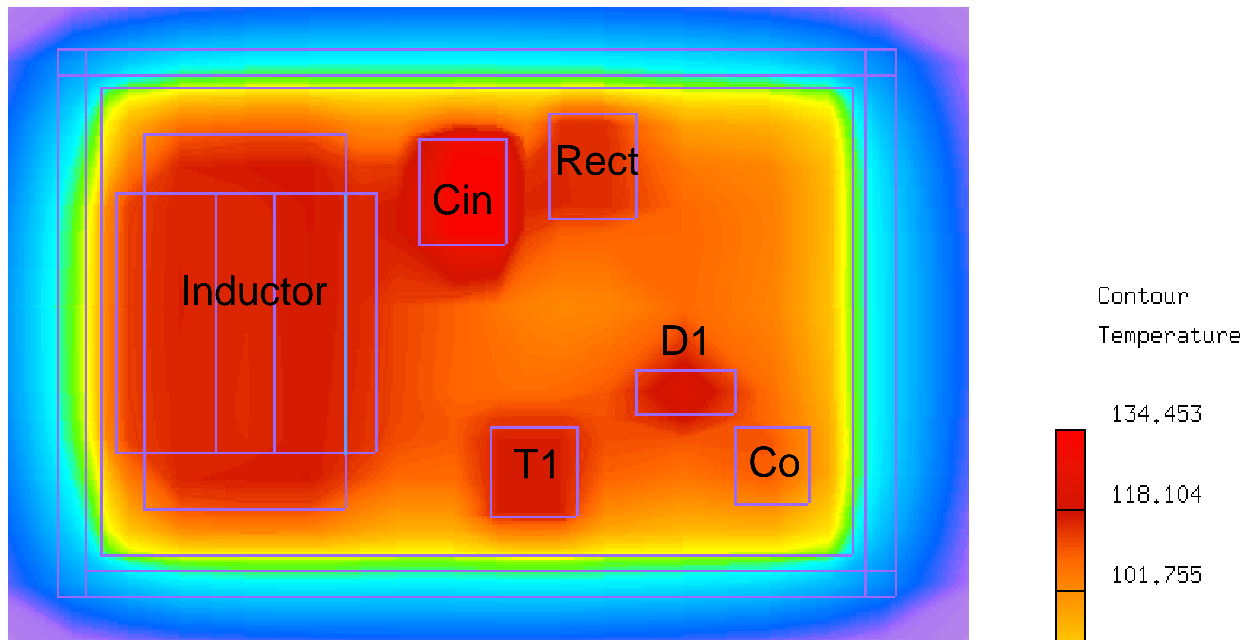


(a)

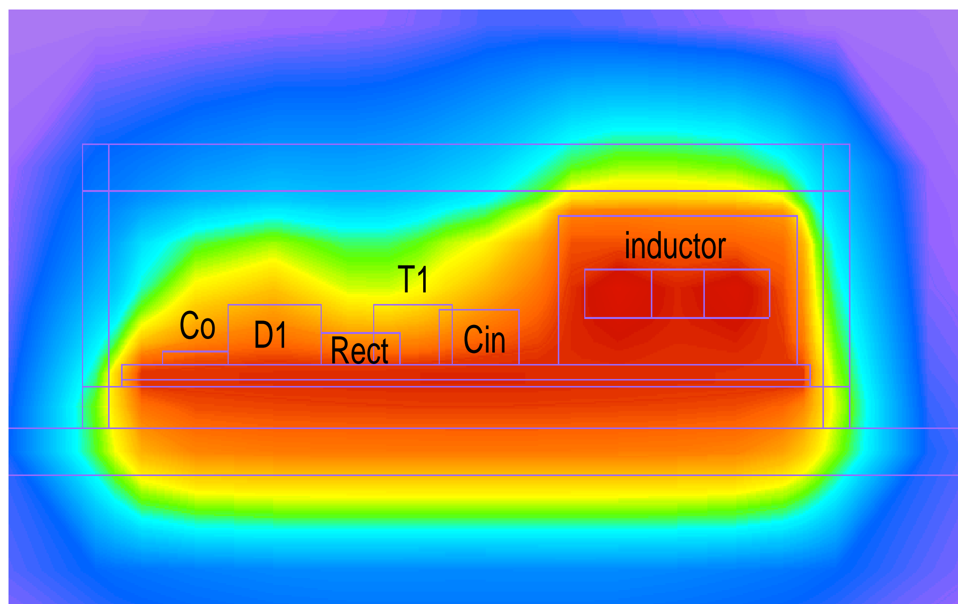


(b)

Fig.3.24.(a) *Flotherm* thermal model (b) predicted temperature



(a



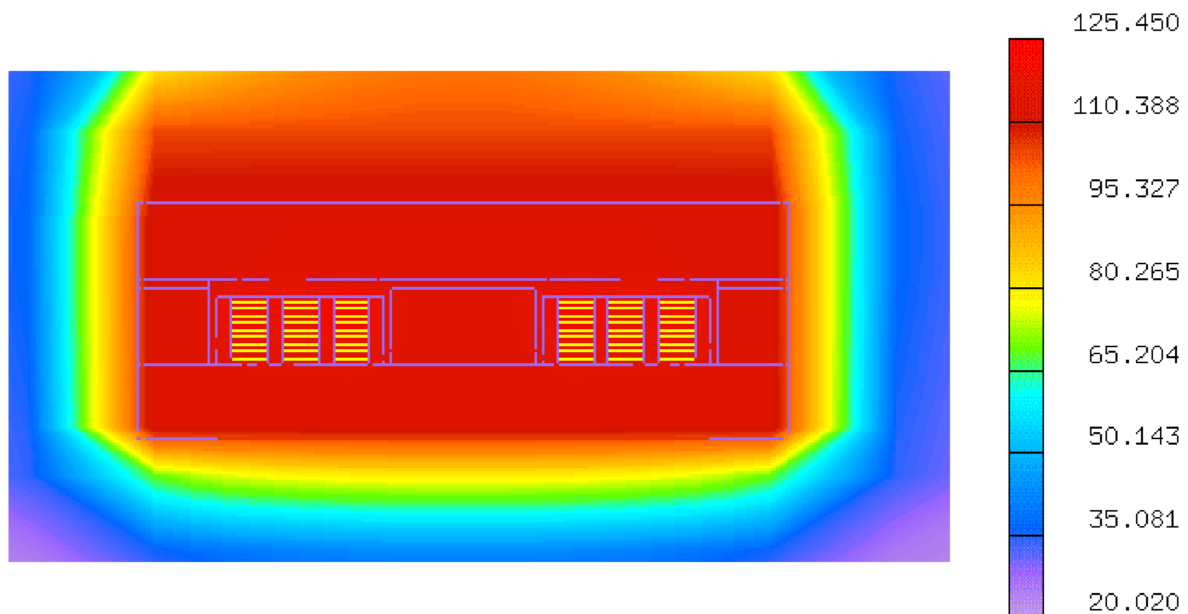
(b)

Fig.3.25. (a) temperature contour of substrate (b) side view

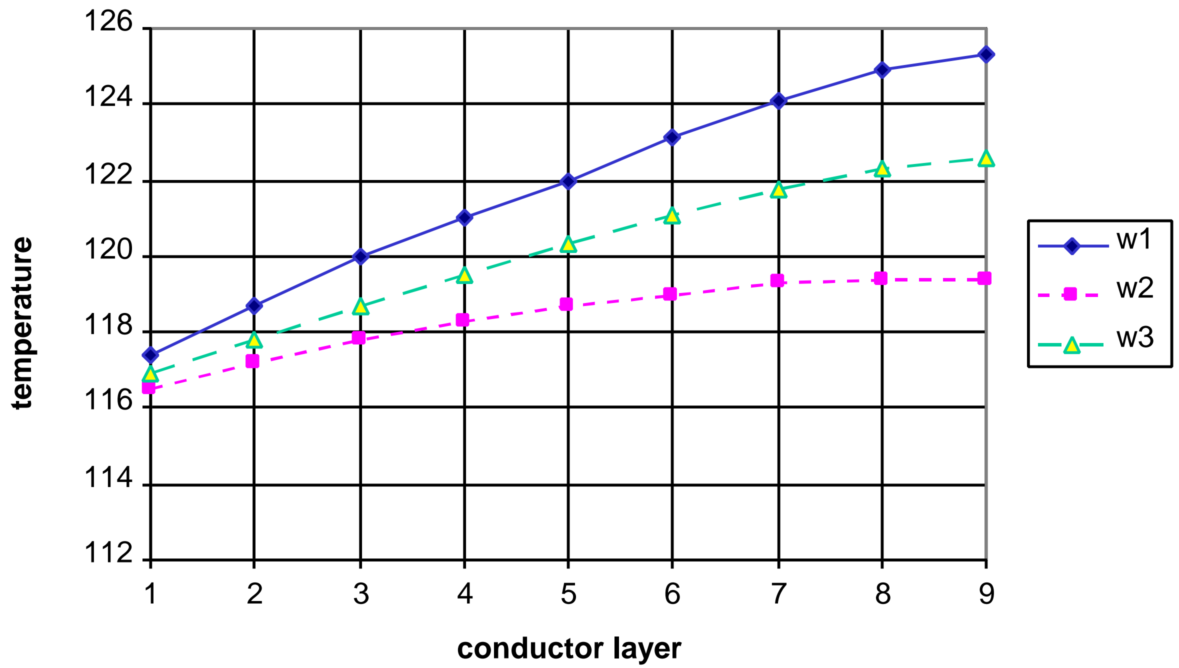
3.3.1.2. Inductor Temperature Profile

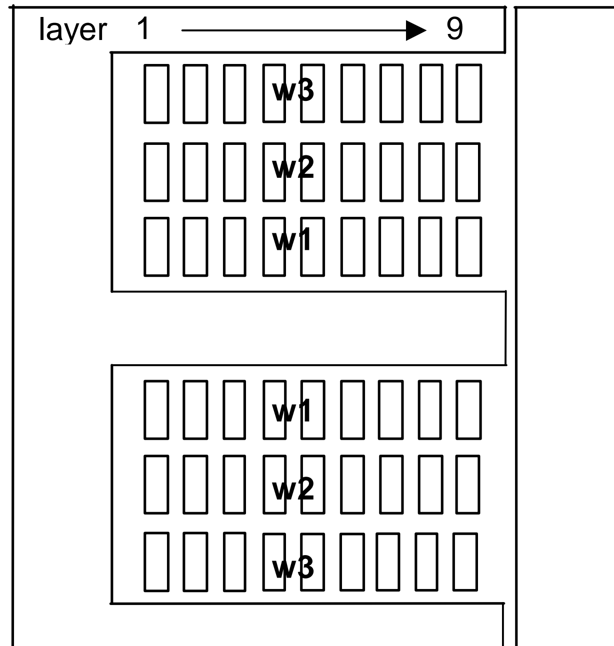
By board-level simulation the surface temperature of the planar inductor can be found. However, for effective thermal design it is important to find the hot spot temperature of the inductor, which can be achieved by component level simulation for the inductor.

As described in the previous section, by using FEA software *Maxwell Field Simulator,* the copper loss of each conductor can be found. With the predicted surface temperature from the board simulation, and the loss information from the FEA analysis, the temperature profile of the planar inductor is found by component level simulation. Temperature profile of the inductor is shown in Fig. 3.26(a), and the temperature of each conductor is indicated in Fig. 3.26(b). It can be seen that the conductors at the top layers have higher temperature. This is due to larger thermal resistance to the ambient for top layers, and higher copper loss introduced by the fringing effect of air-gap.



(a)





(b)

Fig. 3.26.(a)Inductor temperature contour (b)conductor temperature versus position

3.3.2. Minimize Inductor Temperature Rise

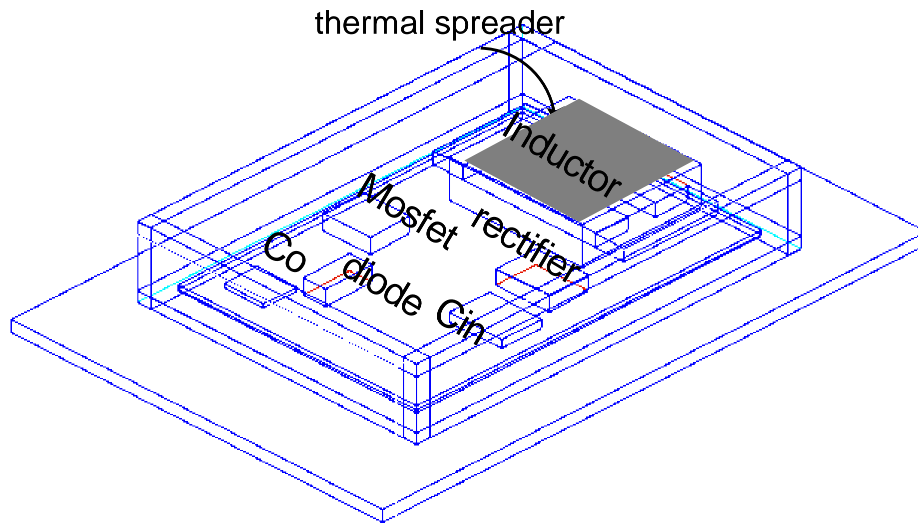
There are two ways to minimize inductor temperature. One is by improving board thermal management to minimize thermal resistance between the inductor and ambient. The other way is by improving component design, i.e. to minimize inductor loss or improve the component thermal design.

3.3.2.1. Effect of Thermal Spreader

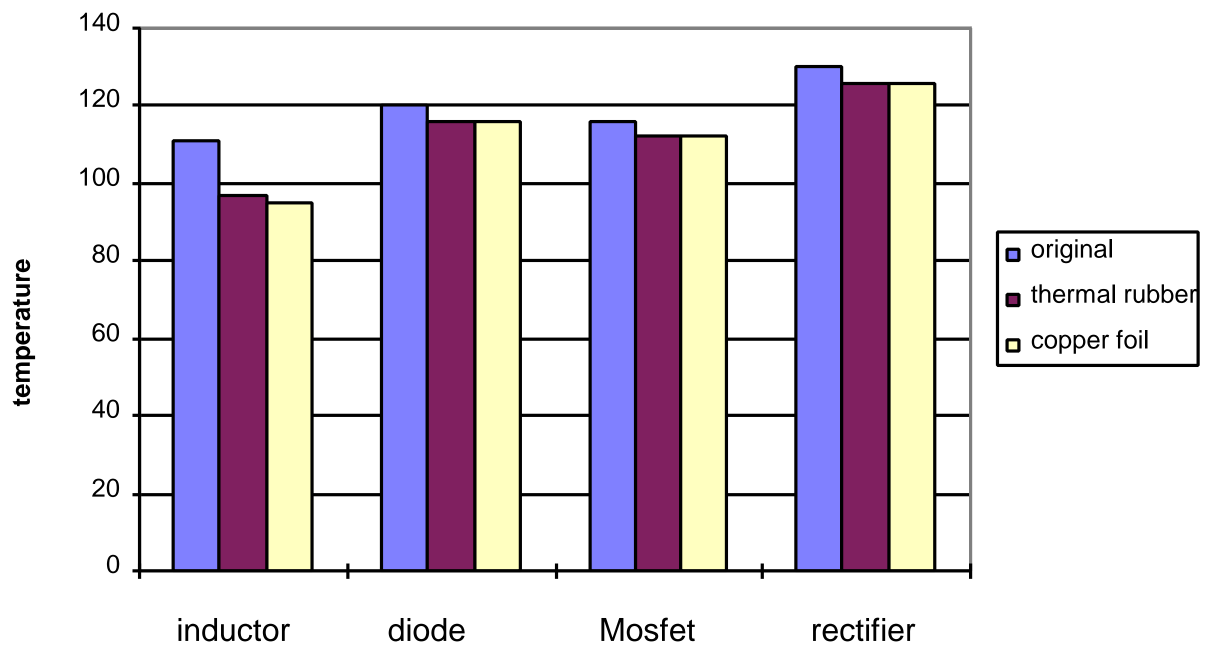
Even temperature distribution on the enclosure surface will help to dissipate heat [15]. In order to increase the power capability of the enclosure, one needs to eliminate the hot spot and achieve an even distribution of temperature. To minimize the inductor temperature rise, the thermal conduction path between the inductor and enclosure surface should be designed to have low resistance. Direct contact between the inductor and the enclosure will reduce the thermal resistance. The heat dissipation of the enclosure's top surface is more efficient than the bottom, because it is in contact with free air, and the heat can be radiated to the surroundings besides conduction and convection. Therefore the inductor is brought in contact with the top of the enclosure, and a thermal spreader is inserted between them to enable better contact between the inductor and the enclosure. The thickness of the thermal spreader is *2mm*.

Two cases are simulated to investigate the effectiveness of the thermal spreader by assigning different thermal conductivities to the material. In the first case, thermal rubber is applied and the thermal conductivity is *2w/mK*. In the second case, copper foil is applied and the thermal conductivity is *170w/mK*. Simulation results are shown in Fig. 3.27. It s seen that inductor temperature is reduced by approximately 15°C in both cases. Due to the interactions between the components, Mosfet and the diode temperature are reduced by approximately 6°C. The temperature variation between the two cases is less than *1°C*. Therefore the effectiveness of the thermal spreader dose not depend on the material applied.

In the previous case, the footprint of thermal spreader is the same as that of the inductor core. By increasing the area of the thermal rubber, the thermal energy of the inductor can be further spread, thus further minimizing inductor temperature. Fig. 3.28(a)

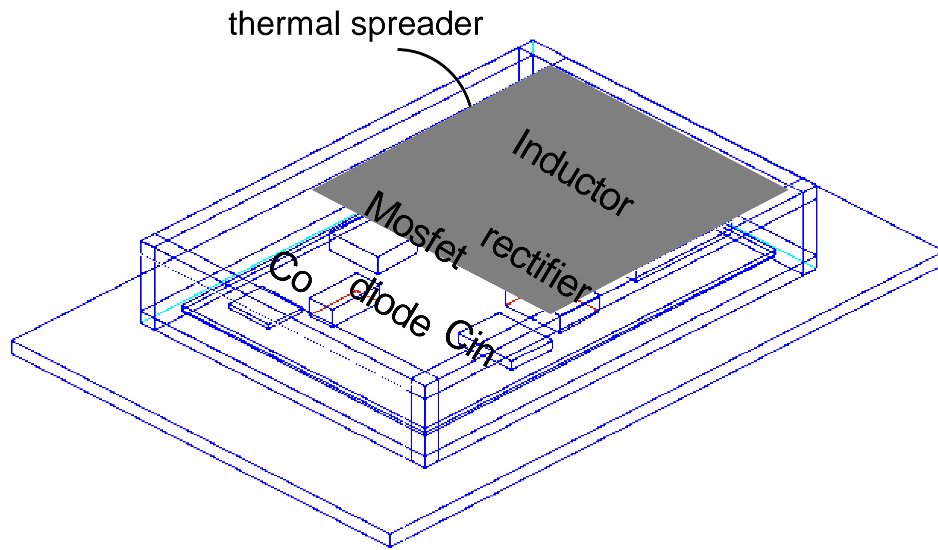


(a)



(b)

Fig.3.27. (a) Insert a thermal spreader between inductor and top enclosure (b) components temperature comparison



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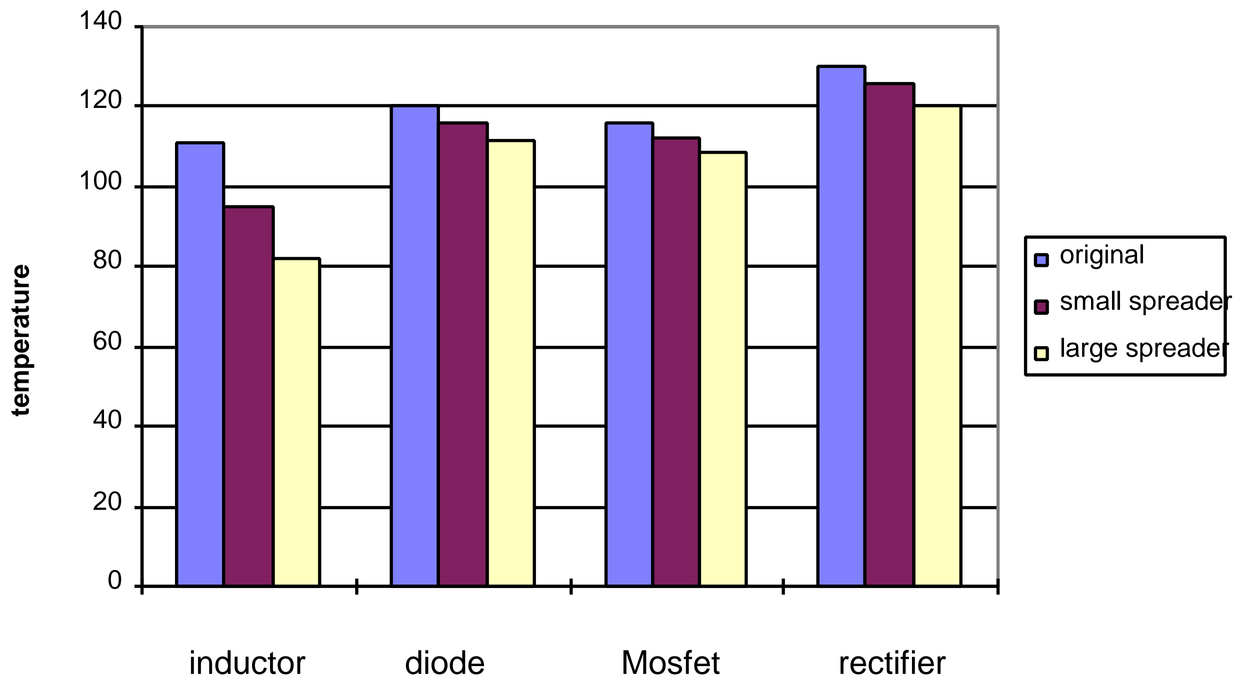


(c)

Fig.3.28. (a) case I (b) case II (c) component temperature using PCB inductor original–w/o thermal conductor; case I–with thermal conductor; case II–increase the size of thermal conductor

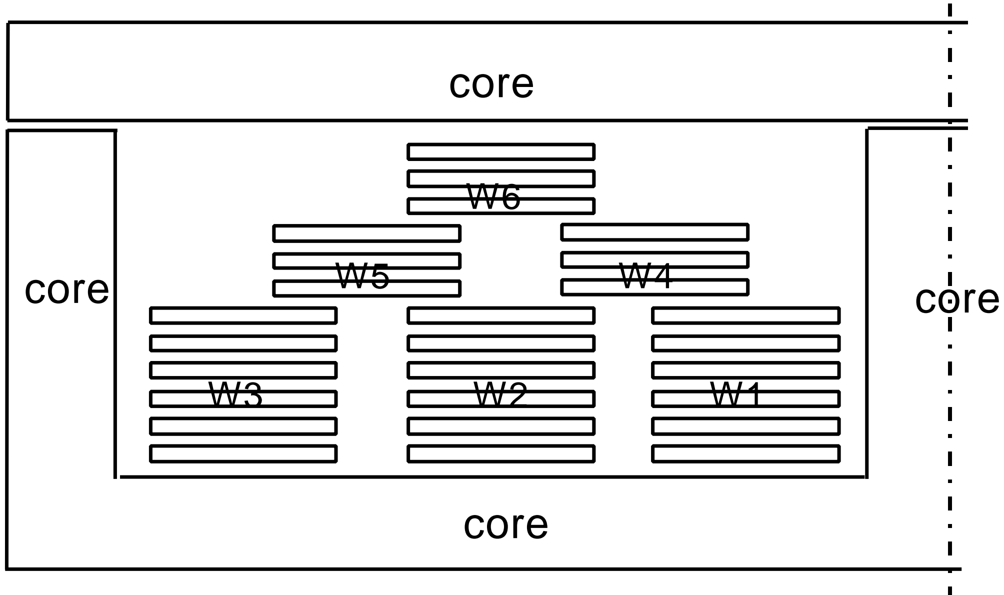
shows the relative area of the thermal spreader and the component arrangement. Fig. 3.28(b) shows the component temperature of the original design in comparison with the case with the small thermal spreader, and the case with the large thermal spreader. It is seen that the inductor temperature is further reduced by about 12°C by increasing the area of the thermal spreader. Therefore, it is meaningful to increase the thermal spreader size, while increasing the thermal conductivity of the spreader adds little improvement in reducing inductor temperature.

3.3.2.2. Effect of Winding Arrangement

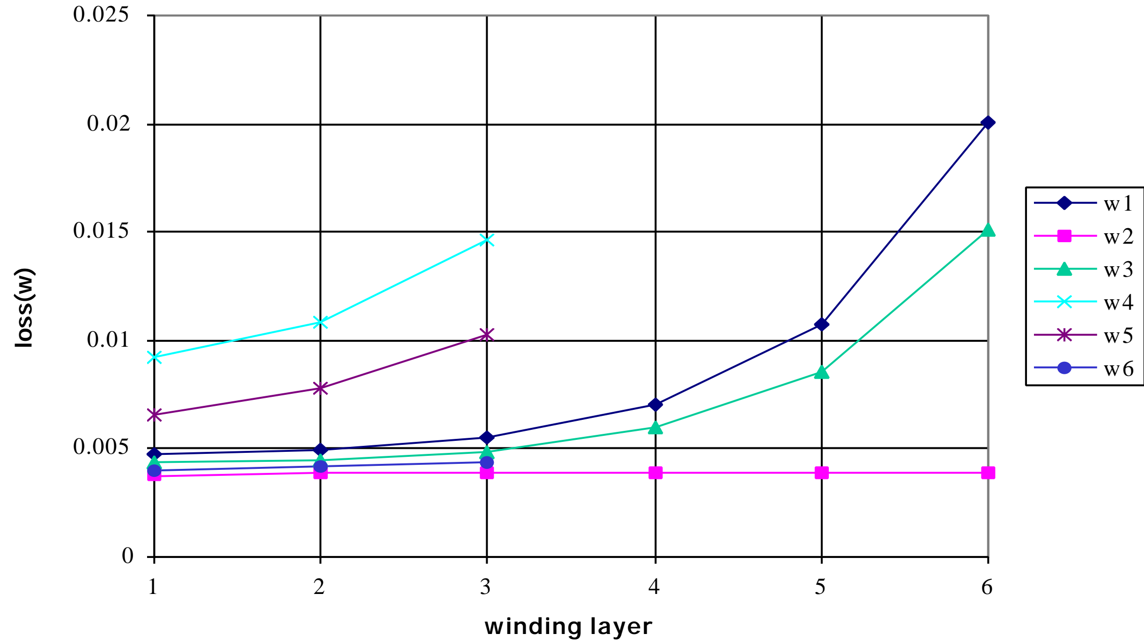
From a component point of view, inductor thermal performance can be improved by minimizing inductor loss, reducing thermal resistance of the internal heat transfer, or suppressing the hot spot within the inductor. Therefore, proper core and winding design is required to minimize inductor temperature.

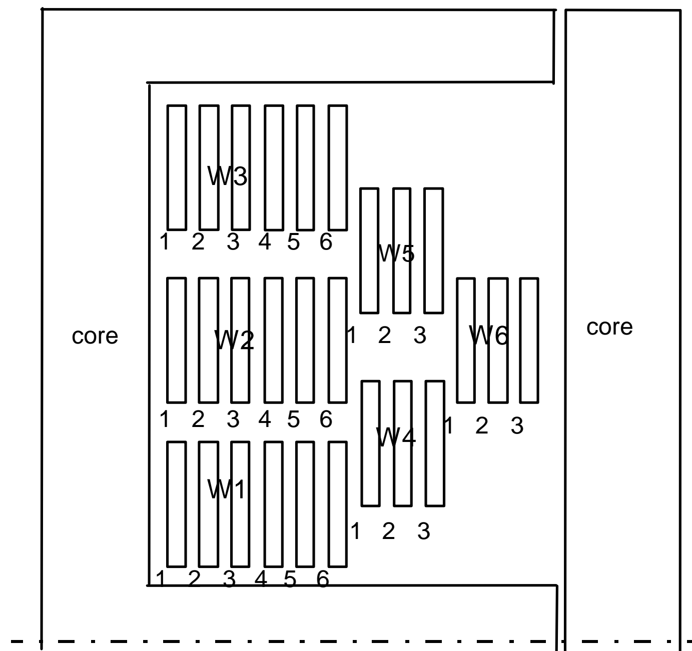
Since core loss is related to the core material, core loss reduction is limited because of the availability of the materials. On the other hand, winding loss is largely due to the high frequency skin effect, the proximity effect and the fringing effect. Because a lumped air-gap is seen within the inductor, the eddy current loss introduced by the fringing effect of the air-gap constitutes a significant part of the winding loss. By minimizing this fringing effect the inductor winding loss can be reduced. An improved winding arrangement by defining the keep-away region is proposed by [18]. It is found that when the distance between a conductor and an air gap is greater than approximately three times the gap length, the loss becomes less than 10% of the loss for the same conductor at a position right beside the gap [18].

The proposed winding arrangement is shown in Fig. 3.29(a). The predicted winding loss by the FEA method is shown in Fig. 3.29(b). It is seen that total winding loss and the uneven conductor loss caused by the air-gap effect is minimized. By thermal simulation, the component temperature of the circuit is predicted as shown in Fig. 2.30(a) in comparison with that of the original design. The temperature profile within the inductor is found in Fig. 3.30(b), and the conductors' temperatures are shown in Fig. 3.30(c). The hot spot temperature of the new winding arrangement is reduced by about 11°C.



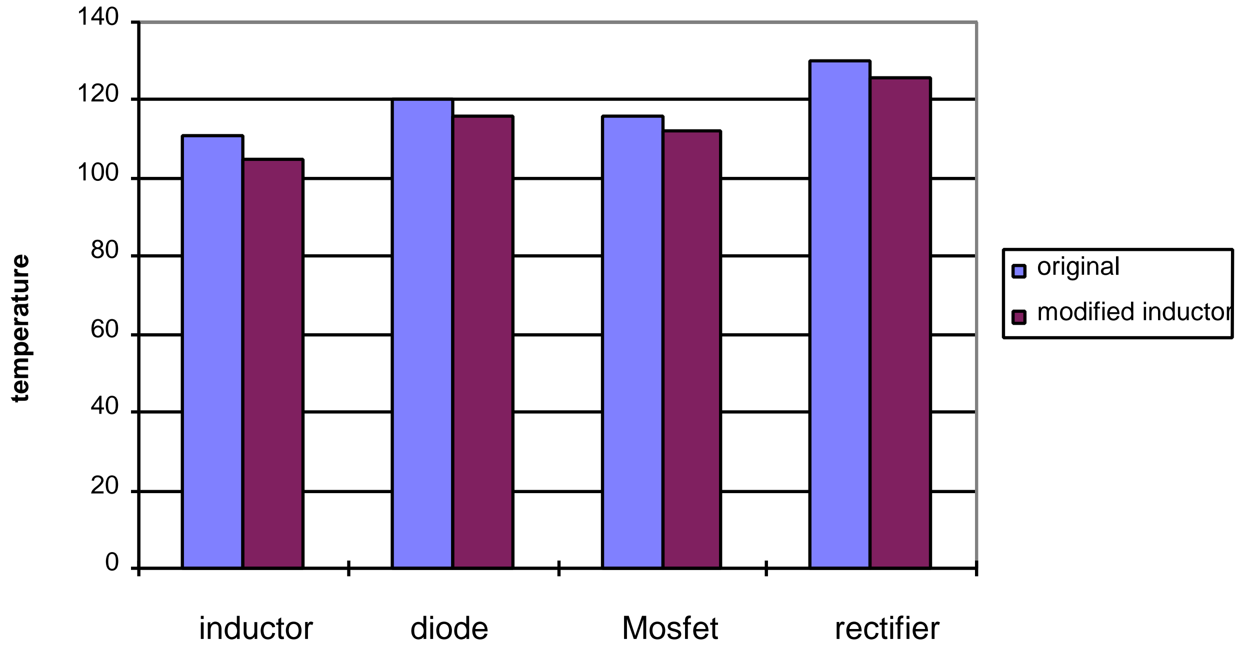
(a)



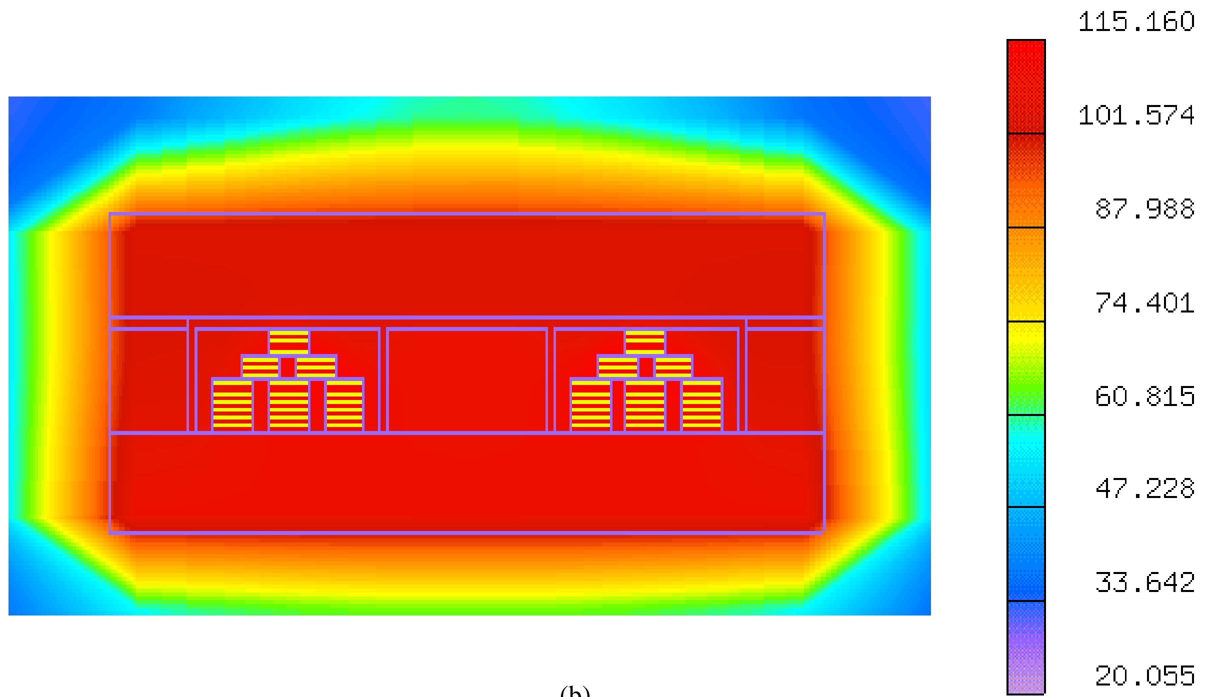


(b)

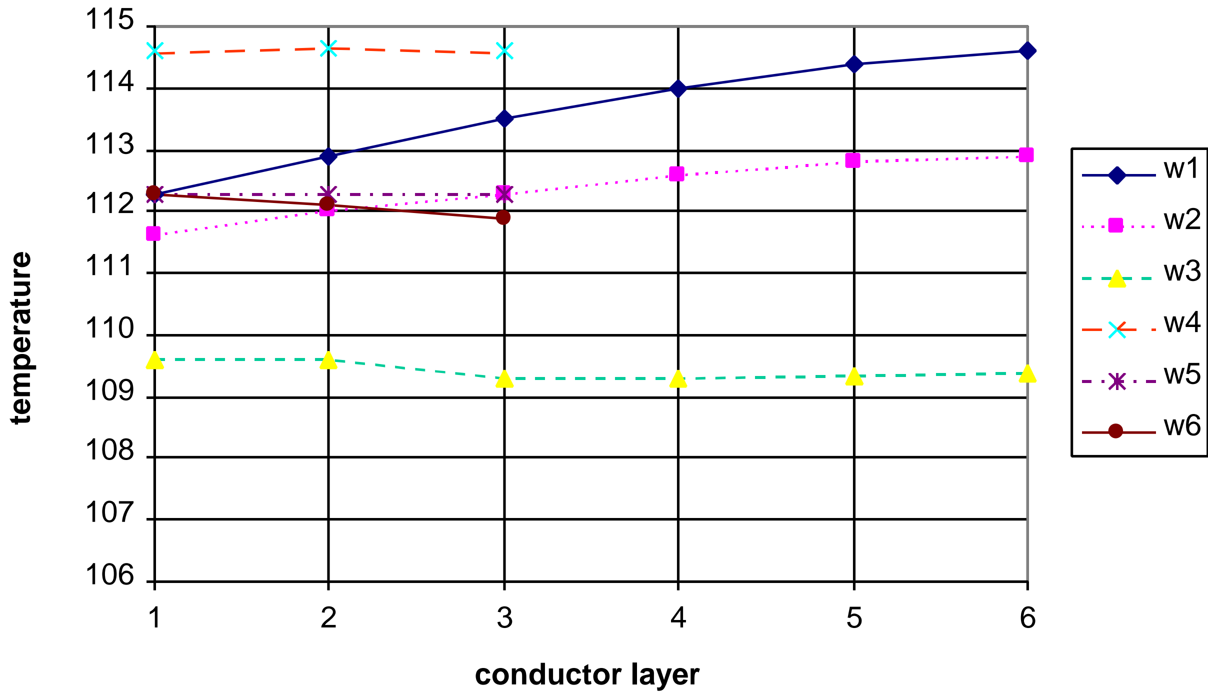
Fig.3.29. (a) winding arrangement with keep away region (b)conductor loss versus position (from reference 17)

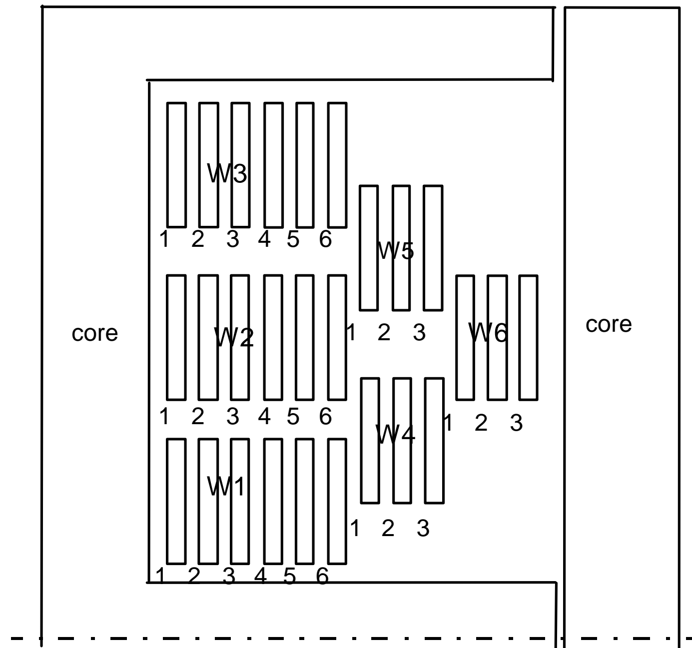


(a)



(b)





(c)

Fig.3.30. (a) device temperature compared with the original design (b)inductor temperature profile (c)conductors temperature

CHAPTER 4

EMI AND THERMAL INTERACTION

In Chapter 2 and Chapter 3 respectively, the model and tools for EMI and thermal analysis are developed. By using the guidelines developed in these two chapters, it is possible to improve the circuit EMI or thermal performance. However, in most cases EMI and thermal design improvement have conflicting requirements. With the tools developed in the previous two chapters, it is possible to quantitatively analyze interactions between EMI and thermal performance.

In this chapter, several examples are investigated to study EMI and thermal design tradeoffs. The design guidelines of the previous chapters are applied to deal with the conflicting requirements of EMI and thermal design. In Section 4.1., the influence of circuit layout is investigated to study the effect of the component position, copper trace, etc. Circuit EMI and thermal performances are given respectively. In Section 4.3., as an example of component analysis, the electrical loss, EMI characteristic and thermal performance of boost inductor are examined. Several examples are investigated.

4.1. Layout Effect

In general, when a circuit layout is designed, from an EMI point of view it is beneficial to minimize the board size and put the components as close together as possible. However, from a thermal point of view, to separate the components will be favorable to reducing their temperature.

4.1.1. The Trade offs of Component Position

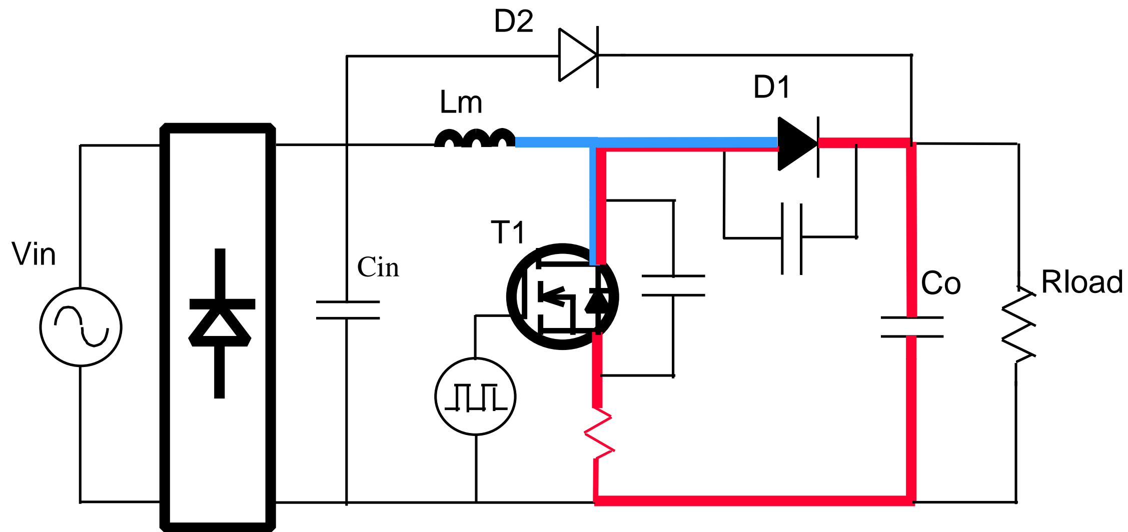


Fig.4.1. Circuit diagram

Fig. 4.1 shows the diagram of this boost PFC circuit. The critical components for thermal performance are shown with thick lines in the diagram, these are the boost inductor (Lm), Mosfet (T1), diode (D1) and the rectifier bridge. They have the highest power losses in the circuit, and are potentially the hottest components. Also, the critical loops and traces for EMI noise reduction are identified with thick lines.

A. Minimize board size

In this case, to minimize the power stage size the components are put very close together. Because the power stage is minimized, the circuit EMI noise is expected to decrease. The circuit layout is shown in Fig. 4.2(b). By *Flotherm* simulation and EMI simulation, the component temperature and circuit EMI noises are predicted. The temperature profile for the circuit is shown in Fig. 4.2(a). It is seen that the high temperature components are put very close together, thus forming a hot spot on the board. EMI simulation results are shown in Fig. 4.5(a). It is seen that the EMI spectrum is not minimized. This is because, although board size is minimized, the sensitive traces and loops are not minimized in the layout. Therefore, this is not an optimal design from either a thermal or an EMI point of view.

B. Improved thermal design

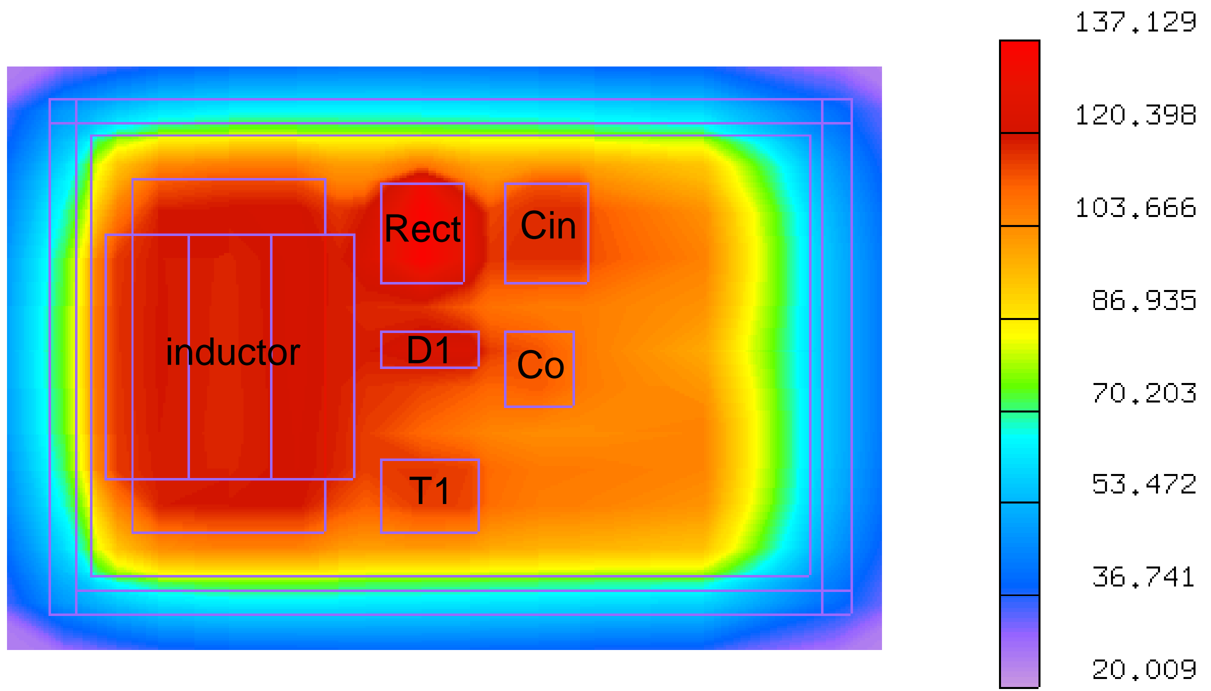
In order to reduce the temperature, in the second case the components are seperated. The rectifier is moved away from the inductor, and the diode is moved away from the hot components. Also, a heat spreader is inserted between the inductor and the enclosure, to dissipate thermal energy. The board temperature contour is shown in Fig. 4.3(a). It is seen that the high temperature components are far away from each other. And the hot spot on the board, the inductor temperature, is greatly reduced. The thermal simulation result is shown in Fig. 4.5(b). It is seen that inductor temperature is reduced by approximately 20°C. And the temperature for other components is reduced by about 10°C.

On the other hand, because the objective here is to improve thermal performance, the criteria for EMI improvement is not met. Fig. 4.3(b) shows the interconnection traces of the circuit. It is seen that the critical loop area is large and the critical trace area is not minimized. The EMI noise spectrum for the circuit is shown in Fig. 4.5(b).

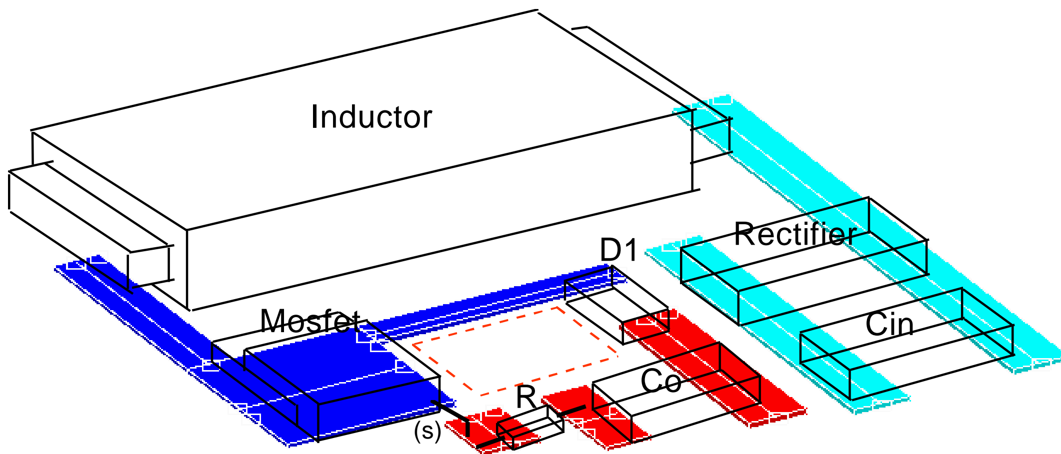
C. Compromised design

By using the guidelines in the previous chapters, an improved layout design is proposed in Fig. 4.4. From an EMI point of view, the critical loop and the critical trace size should be kept as small as possible. Thus, Mosfet T1, diode D1 and the output capacitor Co are put closer together to form a small loop. From a thermal point of view, the rectifier and the inductor are the circuit hot spots. They should be moved apart from each other, and kept away from the other components as far as possible. Also, the heat spreaders are inserted between the hot spots and the enclosure. In this case, the EMI and thermal requirements are compromised.

Fig. 4.4(a) shows the temperature contour of the circuit, and Fig. 4.4.(b) shows the interconnection traces of the circuit. The simulated EMI performance and device temperature of the three cases are compared in Fig.4.5.

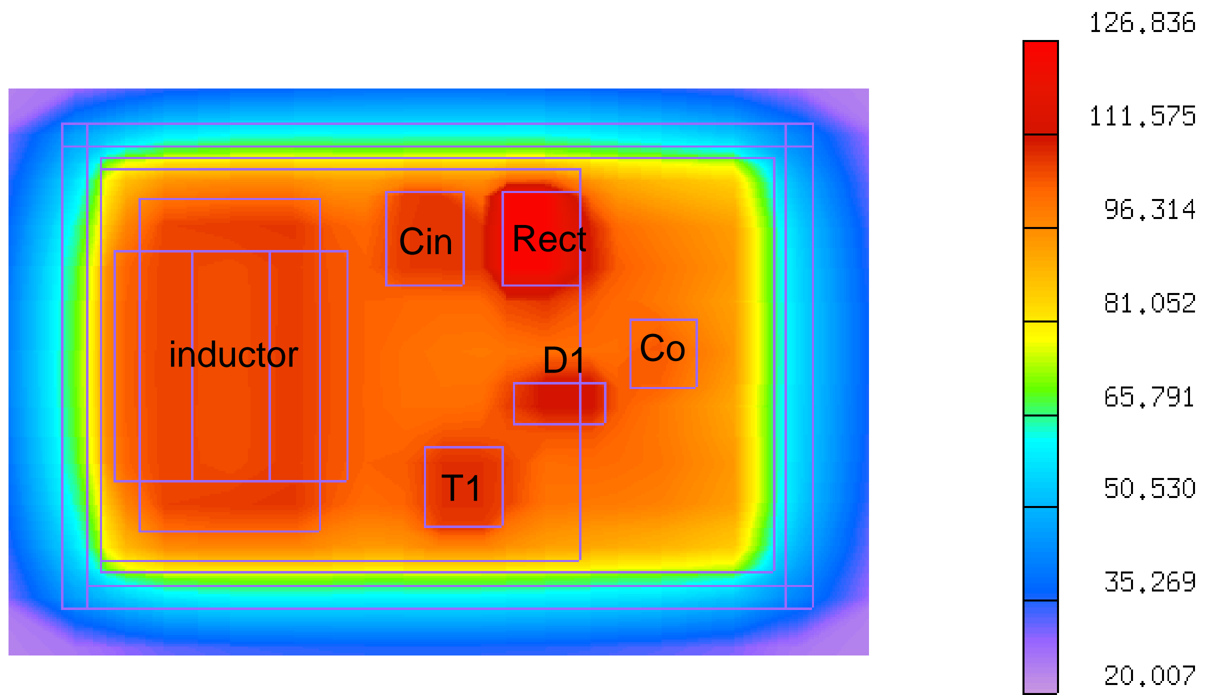


(a)

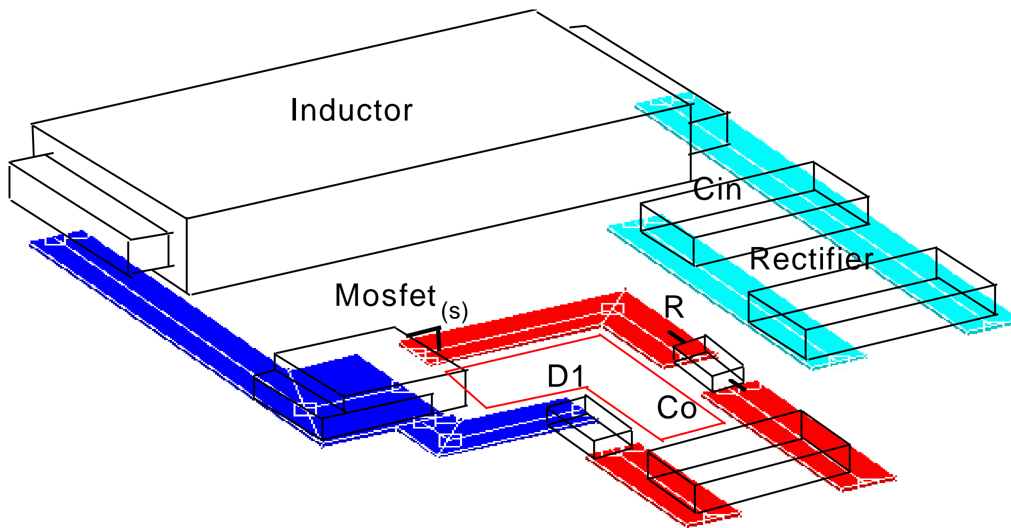


(b)

Fig.4.2. Case A
(a)temperature contour (b) interconnection traces

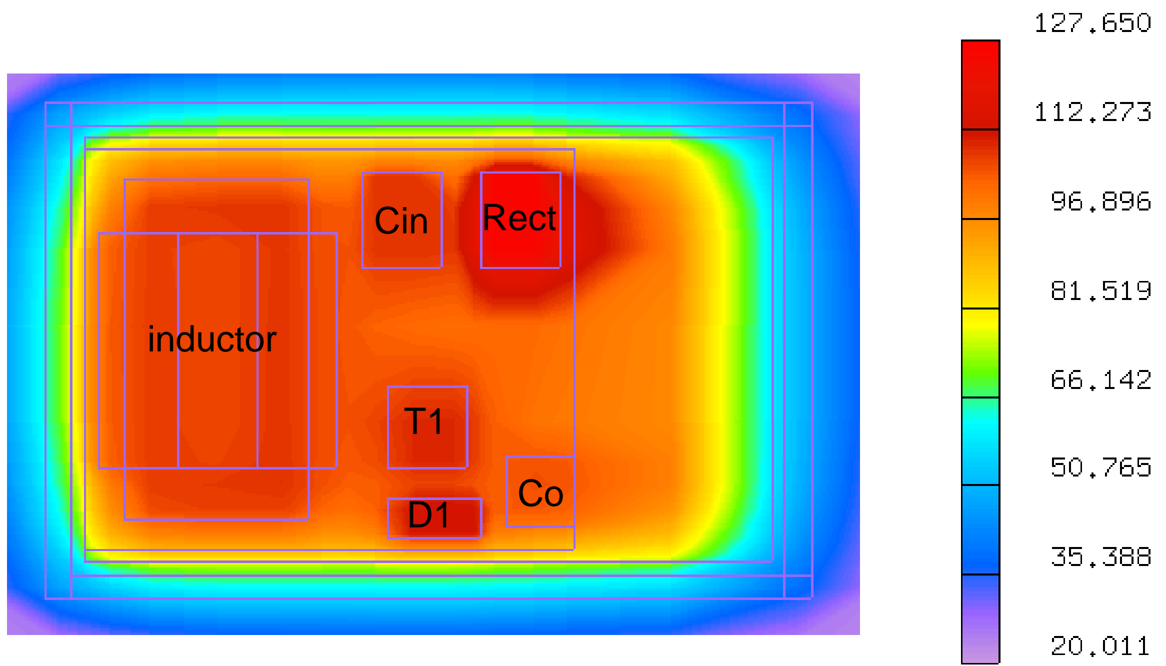


(a)

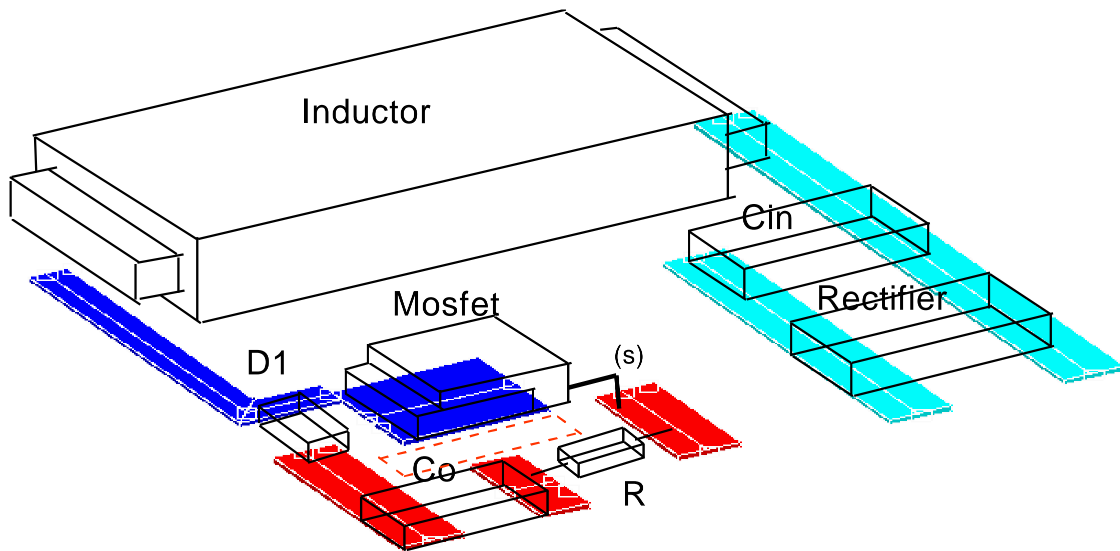


(b)

Fig.4.3. Case B
(a)temperature contour (b) interconnection traces



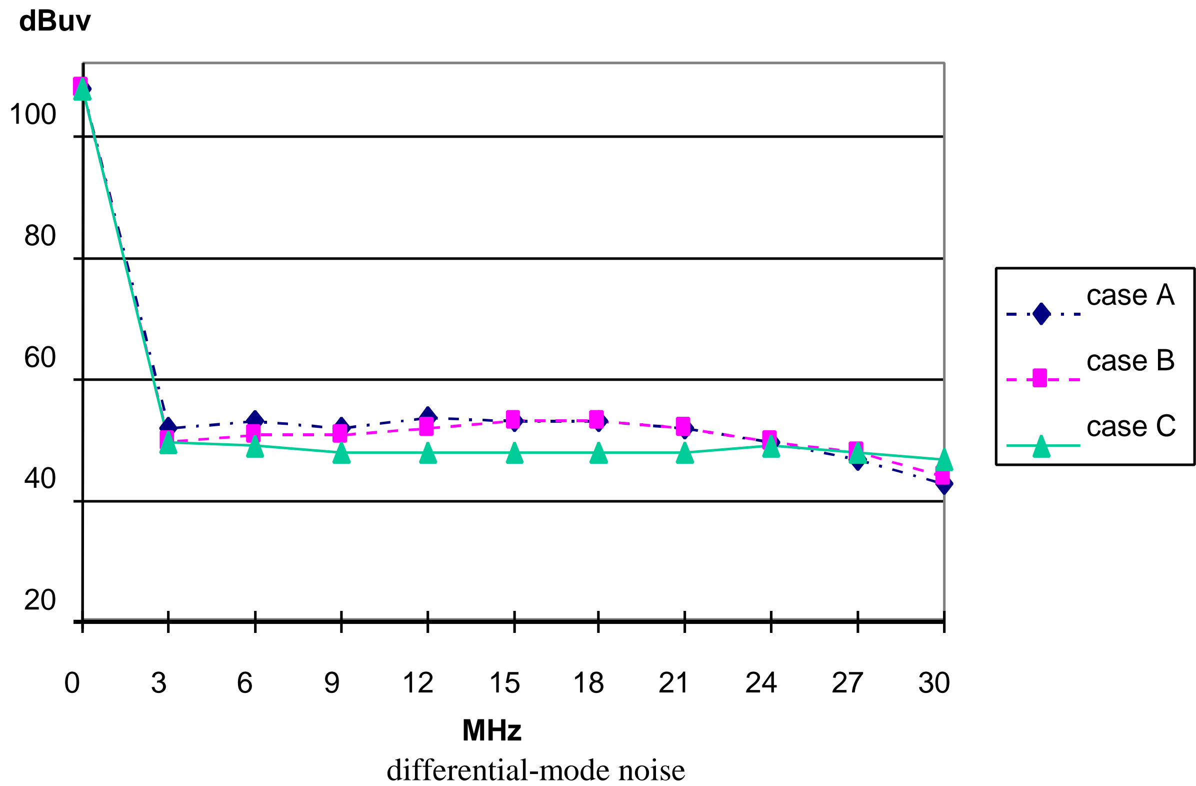
(a)



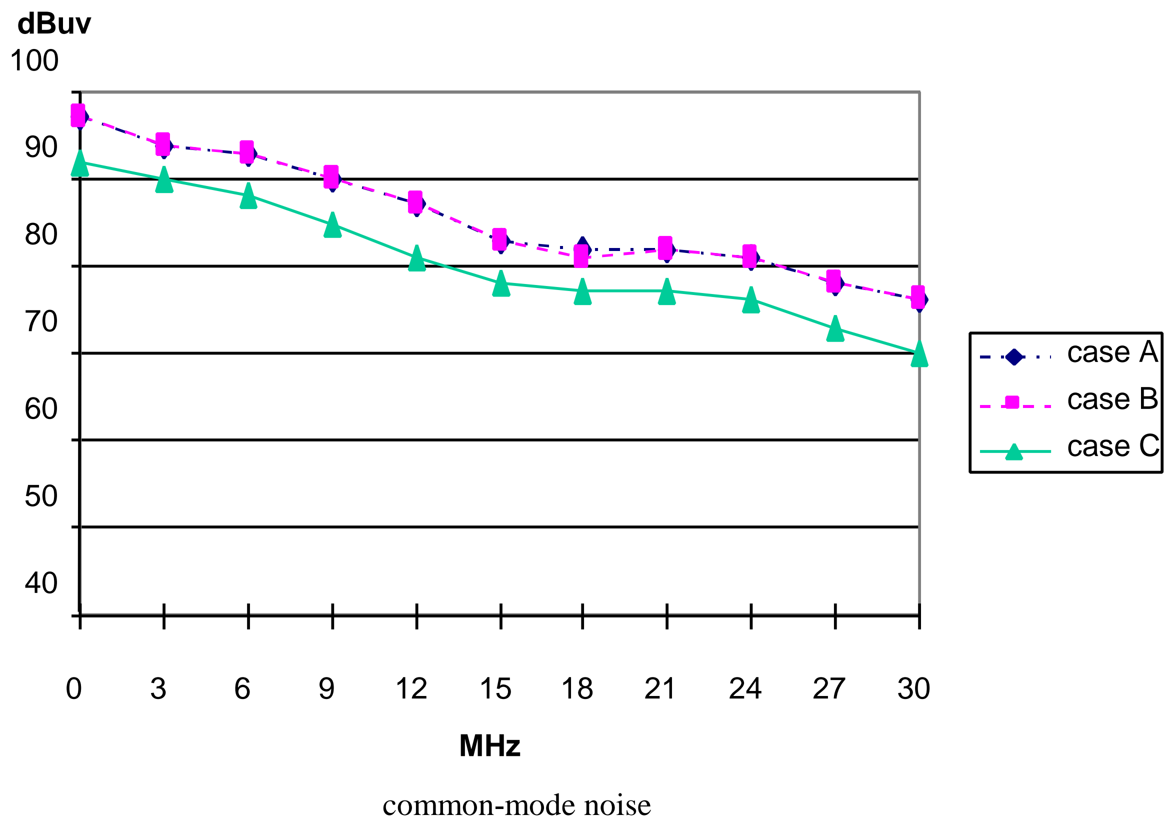
(b)

Fig.4.4. Case C

(a)temperature conour (b) interconnection traces

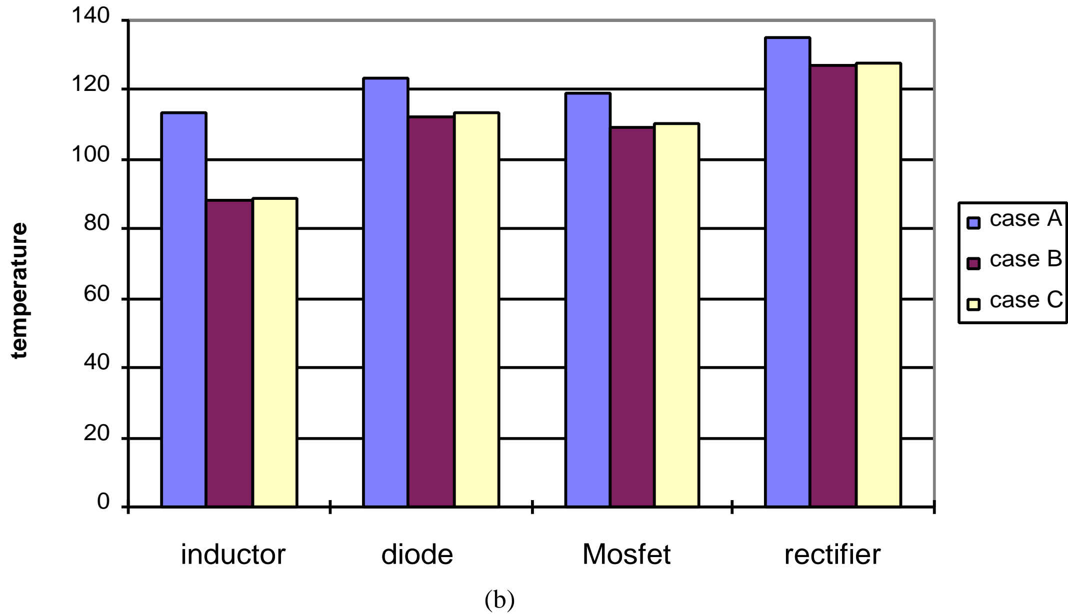


differential-mode noise



common-mode noise

(a)



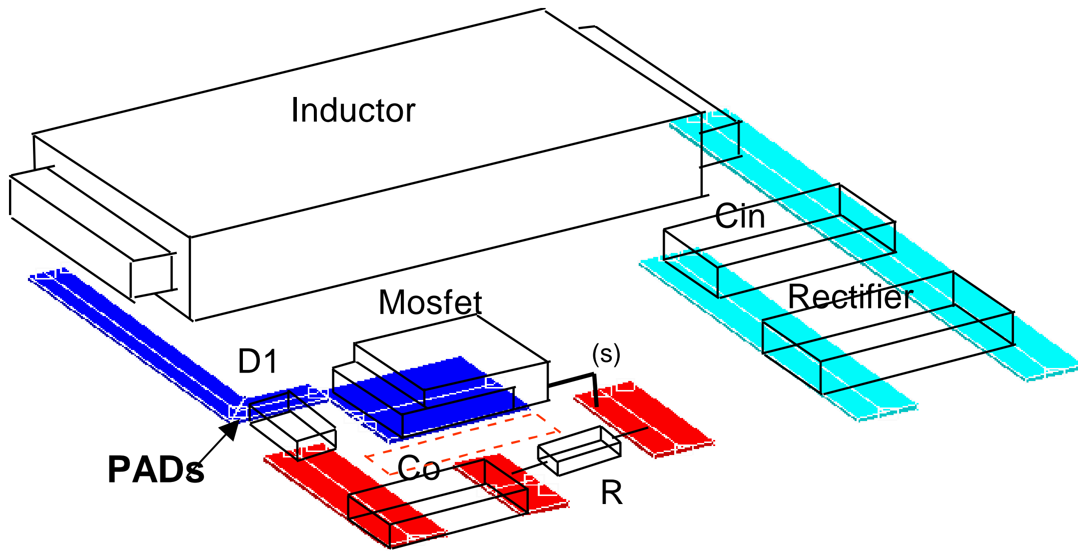
(b)

Fig.4.5. (a) EMI noise comparison of the three cases (b) Component temperature comparison

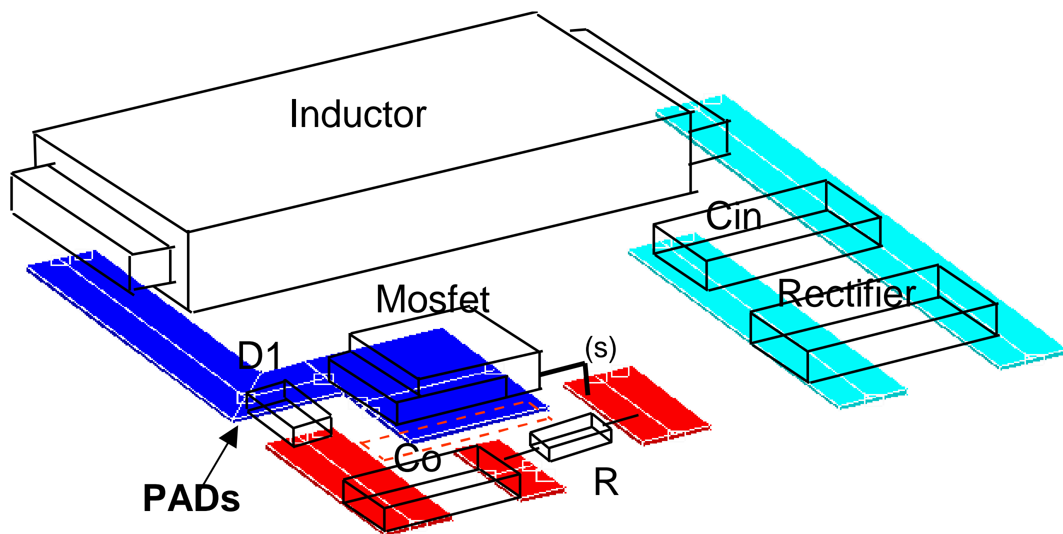
4.1.2. Influence of The PAD Size

Increasing the PAD size will help to spread heat and reduce the component temperature. However, in some circumstances the enlarged PAD may magnify the EMI noises due to the increase of common-mode capacitance. For this boost PFC circuit, Mosfet drain and the diode Anode are included in the critical traces. Excessive PAD size for the two nodes will increase common-mode capacitance. According to the simulation result in Chapter 3, the most appropriate PAD size can be found for effective thermal spreading. A further increase of the PAD area will only hurt the EMI performance, while giving little help to thermal performance.

As an example, for the board under study, the diminishing small point for the PAD is approximately *1 mm* (Fig. 3.10). If we increase its size as shown in Fig. 4.6, the circuit EMI noise will increase, while the component temperature remains approximately the same. The circuit noise spectrum and components temperatures are in Fig. 4.7.

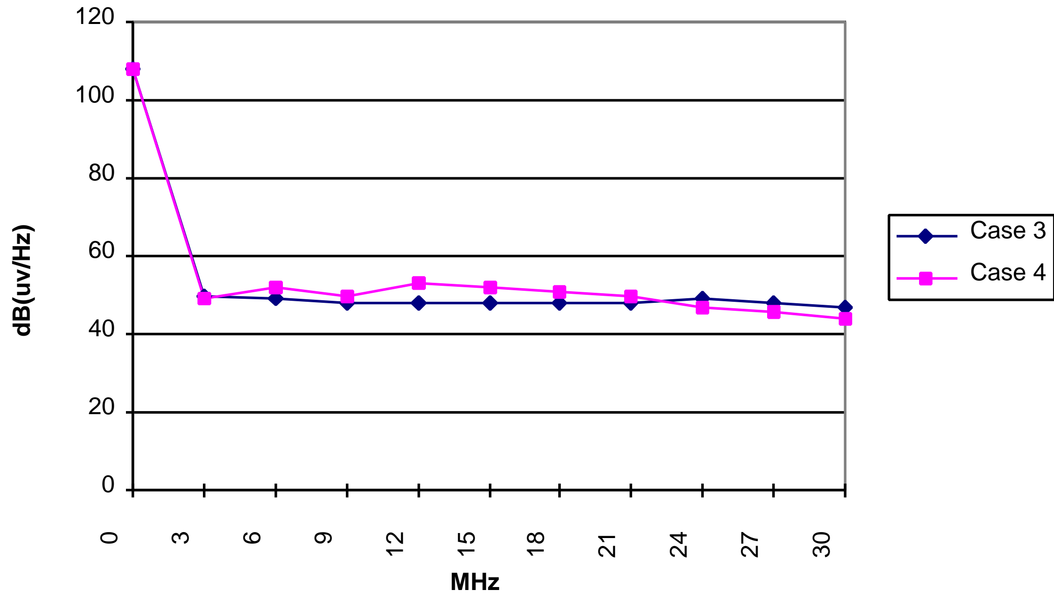


(a) case C

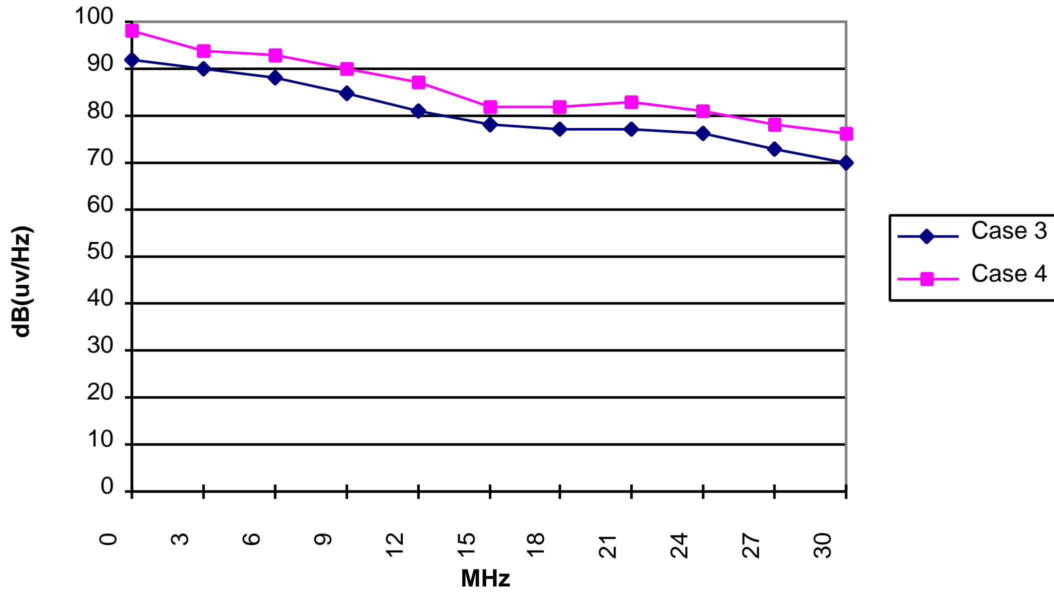


(b) Case D

Fig. 4.6. Increased pads size (a) case C (b) case D



(a) differential-mode noise



(b) Common-mode noise

Fig.4.7. Comparison of noise envelope

4.2. Magnetic component design

Due to their bulky size, the magnetic components are a crucial part of a switching power supply. There are many issues related to the design of magnetic components operating at high frequencies. The magnetic core loss, winding loss introduced by fringing, proximity and skin effect will increase due to the higher frequency. Higher power loss adds to the challenges of thermal design. The hot spot temperature of the inductor should be maintained below the maximum temperature to ensure proper operation. In additions, due to the effect of winding capacitance, the inductor behaves like a capacitor above its first self-resonant frequency. As the switching frequency becomes higher, the effect of parasitic capacitance is more important. This winding capacitance plays an important role for circuit EMI performance. In summary, the design optimization of the magnetic components is an integrated study of electrical, EMI and thermal performance.

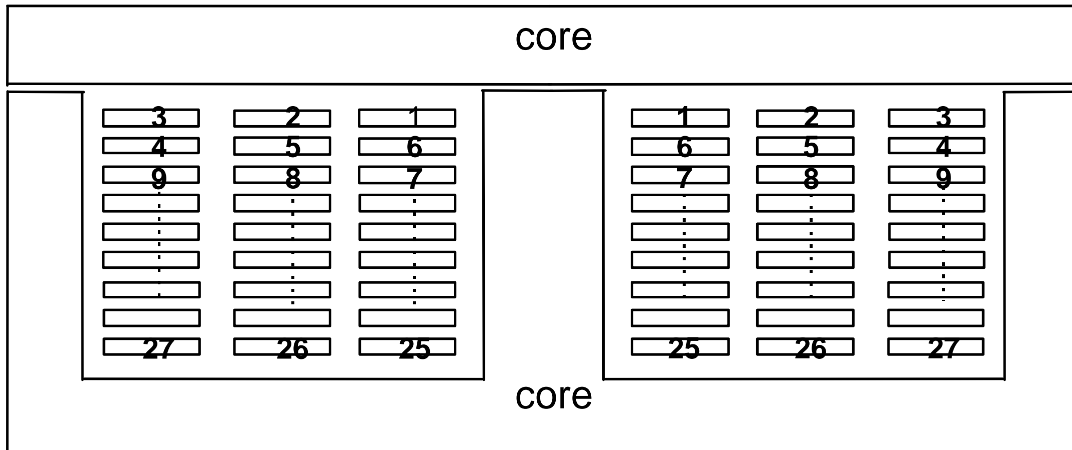
In Chapter 2, the design of planar inductor is improved from an EMI point of view. A new winding arrangement is proposed to reduce the parasitic capacitance. In Chapter 3, by defining the keep away region, the inductor copper loss is reduced. Inductor thermal performance is improved. In this section, several inductor designs are checked from electrical, EMI and thermal points of view. Two additional examples are investigated. By using the tools and design guidelines in the previous two chapters, the tradeoffs between EMI and thermal performance can be quantitatively compared. The simulation and analysis results for the several examples are summarized in Table 4-1.

Case 1 is the original design. In case 2, the winding arrangement is modified to reduce the parasitic winding capacitance. Due to this modification, the circuit EMI performance will be improved. In this case, the inductor loss and thermal performance remain the same as the original design. However, this design may have problem on the winding termination. Design 3 is another method to reduce winding capacitance.

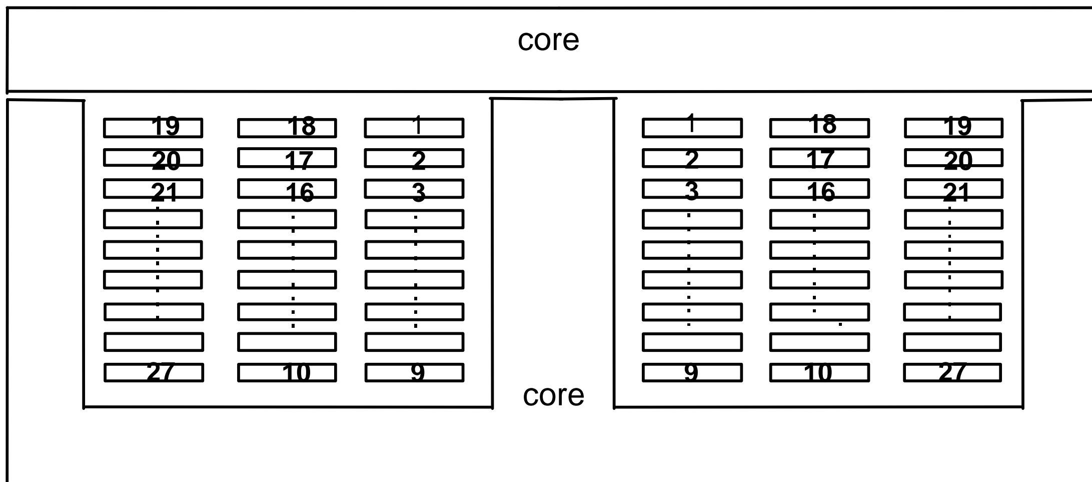
In case 4, the winding design with keep away region defined is applied to reduce inductor loss and minimize temperature rise. It is seen that the hot spot temperature of the inductor is reduced by 10°C or so, and the winding capacitance is slightly reduced due to the modified winding arrangement. However, the inductor window height is increased as

Table 4-1 Integrated study for the planar inductor

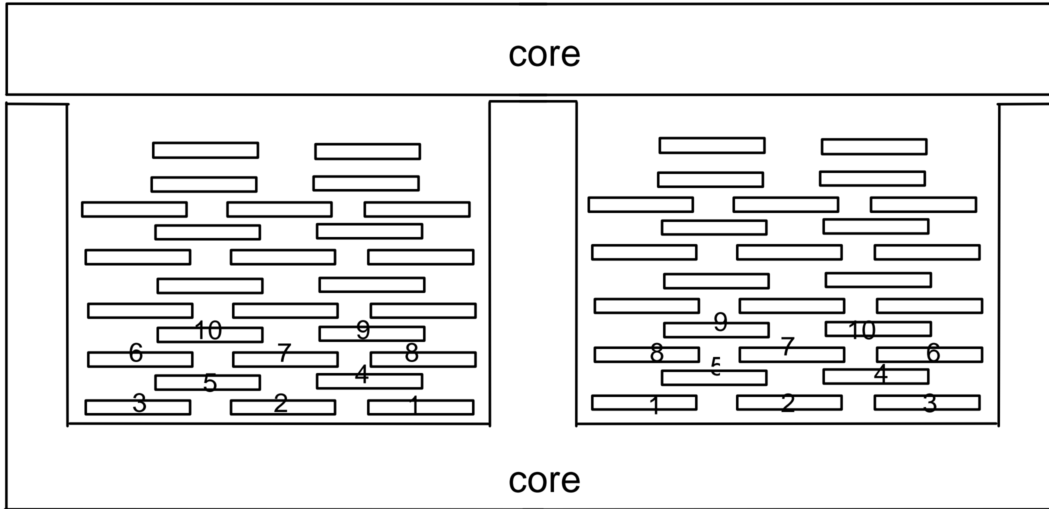
	window height	winding loss	max. temperature	calculated winding Cp	Measured winding Cp
Original	1.572 (mm)	0.462 (w)	124 C	16 (pF)	18.66 (pF)
Design 2	1.572 (mm)	"	"	1.4(pF)	/
Design 3	1.9(mm)	to be calculated	to be simulated	6(pF)	/
Design 4	2.09 (mm)	0.374 (w)	116 C	12 (pF)	15.8 (pF)
Design 5	1.572 (mm)	to be calculated	to be simulated	12 (pF)	/
Design 6	1.572 (mm)	0.374 (w)	"	26.4 (pF)	/



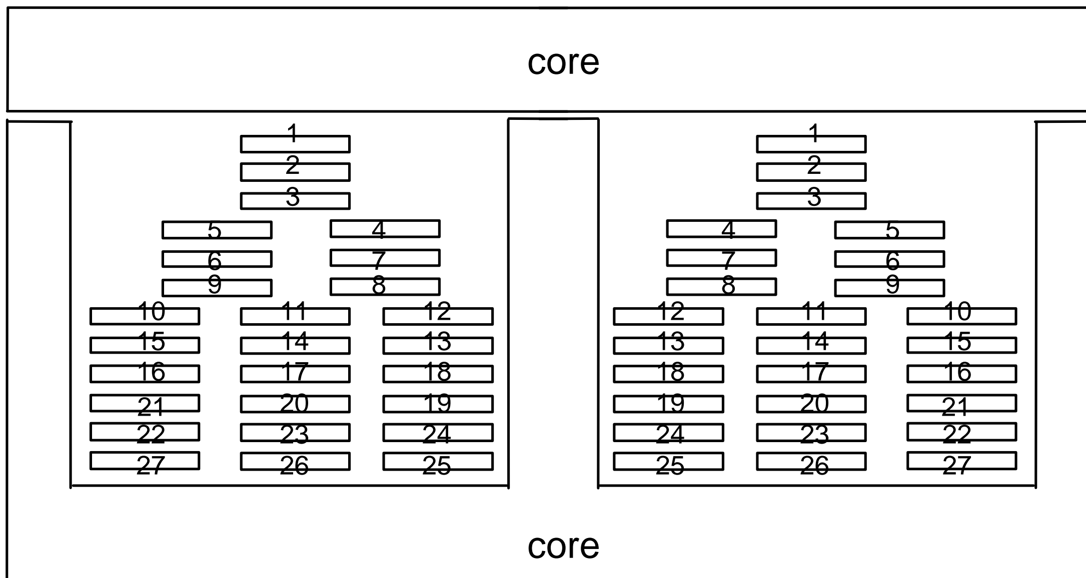
(a) original



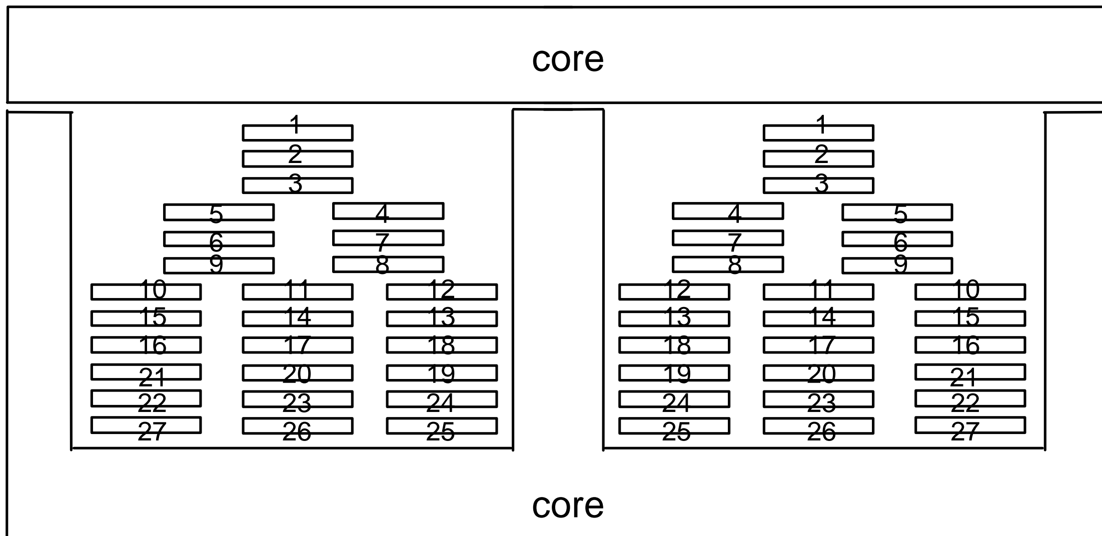
(b) design 2



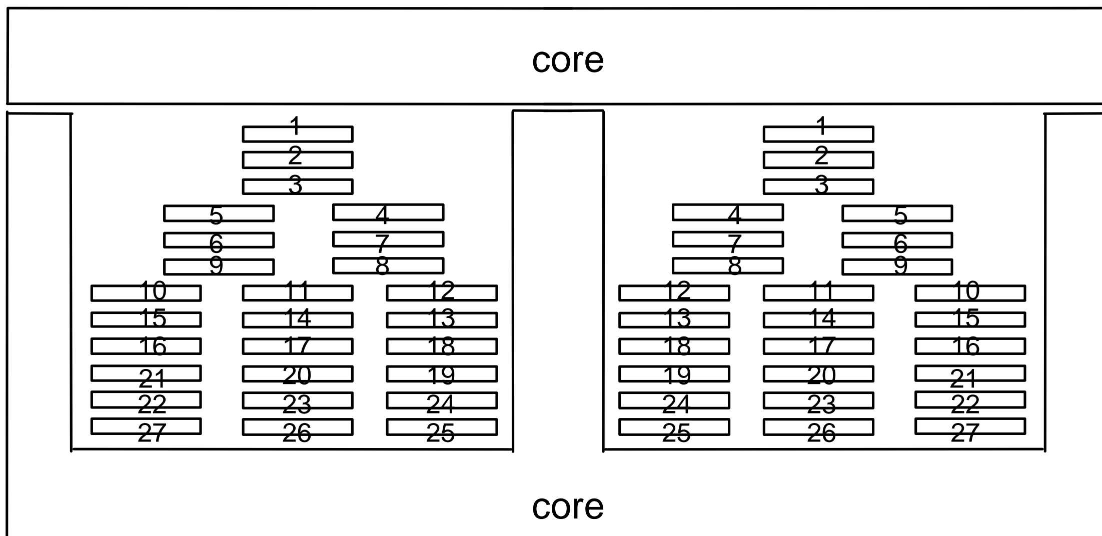
(c) design 3



(d)design 4



(e) design 5



(f) design 6

Fig. 4.8 Planar inductors

(a)original design (b) reduce winding capacitance I (c)reduce winding capacitance II (d)minimize loss & temperature (e) reduce conductor thickness (f) reudce insulator thickness

A tradeoff:

To keep the inductor window height the same, two more cases are studied. In case 5, the conductor thickness is reduced. As a result, the inductor copper loss increases, and thus the inductor temperature rise will be increased. Since the insulator thickness remains the same, the inductor winding capacitance remains the same.

In case 6, the insulator thickness is reduced. As a result, the inductor winding capacitance is increased. Because the conductors are farther from the keep away region compared with case 3, the inductor winding loss and temperature may be slightly reduced. Due to the reduced insulator thickness, the winding capacitance is increased as shown in table-4.1.

Therefore, we can see that different winding arrangement can be selected according to the design issues. For example, for a circuit in which the EMI emission is an issue, design 2 may be selected. While, for a circuit in which thermal requirement is an issue, design 4 may be selected.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

To deal with the issues regarding EMI and thermal requirement and improve circuit reliability, a methodology is developed that integrate EMI and thermal analysis into power converter design by using CAD tools.

To predict converter noise emission, an equivalent circuit is built for EMI simulation by using the PEEC method. The software *InCa* and *Maxwell 3D Parameter Extractor* are used to extract layout parasitic elements, which have an important effect on circuit noises. The parasitic element of magnetic component is calculated analytically. By measurement verification it is seen that this methods presents a good estimation for converter EMI noise. Based on the model, noise sources are analyzed. Improved EMI design is achieved by suppressing the noise sources in circuit, which is implemented by improving circuit layout and magnetic component design. EMI design tradeoffs can be quantitatively compared.

Circuit thermal analysis is conducted by using *Flotherm.* The cooling characteristics of power converter circuit and the interactions between components can be studied by using the 3D model , which considering the mechanism of conduction , convection and radiation. The thermal spreading effect of PADs is studied by simulation. Thermal models for power devices, magnetic component, and passive components are built for temperature prediction and thermal analysis. The temperature profile within the component can be studied by multi-level modeling. As an example, inductor thermal performance in the PFC circuit is examined, and the hot spot temperature is predicted.

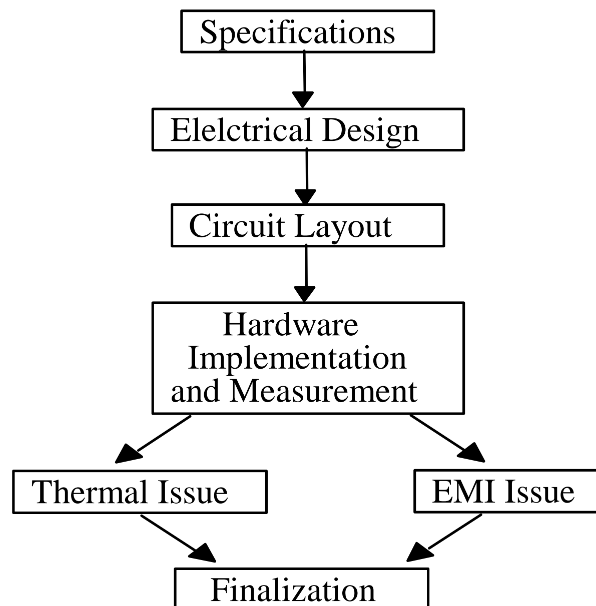
Using the tools, the interactions between the EMI and thermal requirement can be investigated. Several versions of circuit layout are evaluated from both the EMI and thermal point of view by using the tools developed. Several planar inductor designs are evaluated from the electrical, thermal and EMI point of view. Insightful information is obtained through these evaluations.

The comparison of the conventional power supply design and the integrated EMI/thermal switching power supply design is summarized in the flow chart followed.

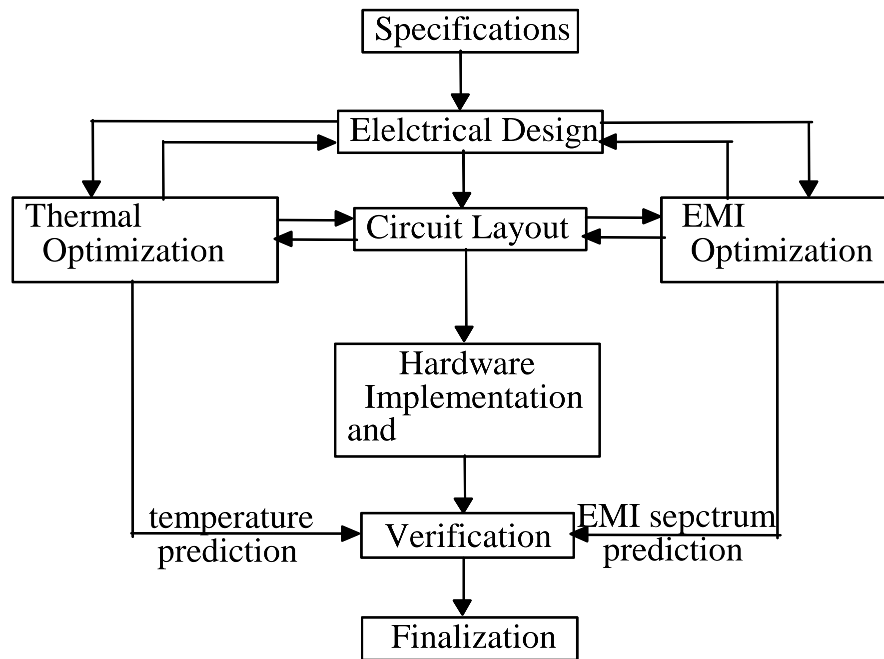
In the future, research should be further conducted in the following directions.

For EMI simulation and prediction, The PEEC method is only valid for conducted noise simulation and analysis. In the future, research should be conducted in the area of radiated noise prediction and optimization, which will involve electromagnetic field theory.

Further EMI/thermal designs should be conducted to study the influence of power stage topology, soft-switching techniques, and the control issues, etc. At present, the data interchange between the tools is manually implemented. The tools will be more effective, if an automatic design loop can be implemented.



(a) conventional power supply design



(b) integrated EMI/thermal design for switching power supplies

References

EMI prediction and minimization

[1] W. Zhang, M.Zhang and F. Lee, "Conducted EMI analysis of a boost PFC converter", *IEEE APEC. Proc.*, 1997, pp.223-229

[2] R. Redl, "Power electronics and electromagnetic compatibility," *IEEE PESC Rec.*, 1996, pp. 15-21.

[3] M.K.W. Wu, C.K. Tse and P. Chan, "An intergrated CAD tool for switching power supply design with elelctromagnetic interference prediction", *IEEE Appl. Power Electroni. Conf. Proc.*, 1996, pp.340-346.

[4] F. Klotz, J. Petzoldt, and H. Volker, "Experimental and simulative investigations of conducted EMI performance of IGBTs for 5-10kVA converters," *IEEE PESC*, *Rec.*, 1996, pp. 1986-1991.

[5] E.Laboure, F.Costa, C.Gautier, W.Melhem, "Accurate simulation of conducted interference in isolated DC to DC converters regarding to EMI standards," *IEEE PESC Rec.*, 1996, pp.1973-1978.

[6] A. E. Ruehli, "Equivalent circuit models for three-dimensional multiconductor systems," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-22, no. 3, pp. 216-221, Mar. 1974.

[7] A. E. Ruehli, "Inductance calculations in a complex integrated circuit environment," *IBM J. Res. Develop.*, vol. 16, pp. 470-481, Sept. 1972.

[8] E. Clavel, "InCa, Prédétermination des inductance de câlage par la méthod PEEC," LEG/ENSIEG (CNRS URA 355), Mar. 1995.

[9] D.A.Weston, *Electromagnetic compatibility principles and applications*. New York: Marcel Dekker, 1991.

[10] H. W. Ott, *Noise reduction techniques in electronics systems*. New York: John Wiley & Sons. 1988.

[11] A. Massarini, M.K. Kazimierczuk, and G. Grandi, "Lumped parameter models for single- and multiple- layer inductors," *Proc. Industry Applications Conf.,* vol. 3, pp.295-301, 1995.

[12] Fu-Yuan Shih, Dan Y. Chen, Yan-Pei Wu, and Yie-Tone Chen, "A procedure for Designing EMI Filters For AC Line Applications", *PELS Transactions.*

[13] Analogy, *"Component Library", "Fundamental of template"*

Thermal analysis by simulation

[14] D.J.Dean, *Thermal Design of Electronic Circuit Boards and Packages,* Electrochemical Publications Limited 1985.

[15] M.Zhang, F.Lee, "Design and Analysis of Thermal Management for High-Power-Density Converters in Sealed Enclosures", *IEEE APEC. Proc*., 1997, pp.405-412

[16] M. Zhang, " Integrated power supply design," for Delta fellowship annual report.

[17] L.Ye, G.Skutt, R.Wolf & F.C.Lee, *Winding Design For Planar Inductors,* report for Philips Laboratories, August 15, 1996

[18] *FLOTHERM Reference Manual,* 1994 Flomerics Limited

[19] *FLOTHERM Instruction Manual,* 1994 Flometrics Limited

[20] R. Blattner, W, Mcdaniel, "Thermal management in on-board dc-to dc power conversion," *High Freq. Power Conversion Conf., Proc.,* 1995, pp.73-85.

[21] B.A. Smetana, G. Venkataramana, "Advanced thermal management for high density distributed power systems," *High Freq. Power Conversion Conf., Proc.,* 1995, pp.27-32.

[22] R. Ridley, M. Reynell, and S. Kern, "Thermal design considerations for distributed Power converter systems," *Proc. IEEE Appl. Power Electron. Conf.,* 1993, pp.866-872.

[23] Tony Kordyban, "Estimating the influence of PCB and Component Thermal Conductivity on Component temperatures in Natural Convection", *Flotherm* reference

[24] J.H.Seely and R.C.Chu, *Heat transfer in microelectronic equipment,* Marcel Dekker Inc., New York, 1972

[25] "About *Flotherm*," *http//www.flomerics.com.*

Vita

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