Performance Improvements of Multi-Channel Interleaving Voltage Regulator Modules with Integrated Coupling Inductors

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Dissertation submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
in
Electrical Engineering

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March 28, 2001
Blacksburg, Virginia

Keywords: voltage regulator module, critical inductance, channel coupling, flux source reluctance model

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(ABSTRACT)

The emergence of the Intel Pentium ™ processor necessitates that a dedicated converter, the voltage regulator module (VRM), be physically located very close to the processor in computer power systems. The efficiency and transient response specifications of the VRM place contradictory requirements on the inductance. This dissertation discusses possible VRM inductor designs to improve efficiency without compromising transient responses.

The multi-channel interleaving buck converter is the most popular topology for present VRMs. Analysis in this work shows that the small-signal model of an n-channel interleaving buck can be simplified as a single buck converter. The equivalent inductance is 1/n of the inductance in the interleaving channel. The equivalent switching frequency is n times the switching frequency in each channel.

Through the transient response analysis, the critical inductance of the VRM is identified. The critical inductance is a tradeoff point between transient response and efficiency. The inductances smaller than the critical inductance have equal transient responses. For the inductances larger than the critical inductance, the VRM transient voltage spikes increase with the inductance. The critical inductance is the largest inductance that gives the fastest transient responses. The critical inductance is a function of the control bandwidth and the load transient steps.

Although multi-channel interleaving reduces the current ripple stress on the output capacitors, it cannot reduce the current ripples in each channel. The large current ripples reduce the efficiency of the VRM. With the proposed concept of integrated coupling inductors between channels, the converters have larger equivalent inductances in steady-state operation and smaller equivalent inductances in transient response. The steady-state current ripples can be reduced without compromising the transient response. The overall efficiency of the converter is improved.

In order to evaluate the application of the coupling inductor concept in multi-channels, an appropriate magnetic model is required. This dissertation proposes a flux reluctance model for the core and winding structures. With this reluctance model and mathematical transformations, the coupled inductors can be decoupled in the electric circuit simulation model. This reduces the complexity of the model when a large number of inductors are coupled. The model can be easily scaled to model the structures that involve more inductors. Examples are presented to show the application of this proposed model.

TO MY PARENTS

HENG WONG
LEI-LEI IAO

ACKNOWLEDGMENTS

Pursuing this degree has been a very lengthy journey for me. When I first came to a different country to study in the area of power electronics, which was then totally new to me, the path was full of confusion, frustration and pain. Like a dark night, I could never have gone through it alone. So many of you are the stars that have helped me through this journey. Now, I come to the final stage and look back. I feel so lucky to have had all of you to help me reach my goal. Some of you may never know you were so helpful to me.

I would first like to thank my advisor, Dr. Fred C. Lee. Maybe the research attitude I learned from him is much more important than the knowledge of power electronics. His continuous challenge of my research quite often made me feel frustrated. As I look back now, I realize that if it wasn't for his challenges, I would never be able to work to this potential.

I am grateful to my committee: Dr. Dushan Boroyevich, Dr. Dan Y. Chen, Dr. Alex Q. Huang and Dr. Douglas Nelson. I appreciate Dr. Daan van Wyk for his valuable suggestions and comments on magnetics.

It has been a great pleasure to work in the Center for Power Electronics Systems (CPES), not only because of the talented colleagues but also the friendships. In particular, I would like to thank Dr. Chih-Yi Lin, Dr. Jinrong Qian, Dr. Qiong Li, Dr. Michael Zhang, Dr. Glenn Skutt, Dr. Kun Xing, Mr. Qun Zhao, Mr. Fengfeng Tao, Mr. Deng-Ming Peng, Mr. Wei Dong, Mr. Jae-Young Choi, Mr. Ray-Lee Lin, Mr. Zhou Chen, Mr. Francisco Canales and Mr. Peter Barbosa for the delightful discussions, both related and non-related to power electronics.

The basketball, volleyball and ping-pong games have made my stay in Blacksburg more pleasant. Thanks to my playmates Mr. Qun Zhao, Mr. Yuibin Zhu, Mr. Yuanxuan Hu, Mr. Yong Li, Mr. Sihua Wen, Mr. Rengang Chen, Mr.

Yin Liu, Mr. Wei Xu, Mr. Kaiwei Yao, Miss Jinghong Guo, Mr. Zhenxue Xu, Mr. Lingying Zhao, Mr. Yuming Bai and Mr. Jinghai Zhou. I personally think that those Friday evenings in the War Memorial Gym were more fun than those weekly meetings in the lab.

I would also like to acknowledge the CPES administrative and lab management staff, Ms. Teresa Shaw, Mr. Jeffery Baston, Ms. Lida Fitzgerald, Ms. Trish Rose, Ms. Ann Craig and Ms. Linda Gallagher for their countless help in my CPES work. Thanks to Mr. Steve Chen, Mr. Jiyuan Luan and Mr. Changrong Liu for their help with computers.

I am especially indebted to my colleagues in the VRM group, which was the most hard-working group in CPES (we know VRM also means “very robust man”). Thanks to Dr. Xunwei Zhou, Mr. Peng Xu, Mr. Bo Yang, Mr. Ho-Pu Wu, Mr. Jiabin Chen, Mr. Xiaowu Sun, Mr. Luca Amoroso, Mr. Kaiwei Yao, Mr. Yuhui Chen, Ms. QiaoqiaoWu, Mr. Faruk Nome, Mr. Jia Wei, Mr. Mao Ye, Mr. Yang Qiu, Mr. Yuancheng Ren, Prof. Wei Chen and Prof. Xiaochuan Jia. It was a pleasure to work with such a talented and creative group.

Thanks to Dr. Robert Watson for his words “hang in there guys, it will happen,” which helped me through those dark days.

With much love, I would like to thank my parents. I know you pray for your son every day. Although it was only through the phone line and letters, you gave me the most valuable strength and courage to go through this journey.

There are some friends outside CPES who made my life in Blacksburg enjoyable. You may never realize the value of your help to me. I will not list the names here; you already know who you are.

This work was supported by the VRM consortium (Intel, Texas Instruments, ST Microelectronics, National Semiconductor, Delta Electronics, International Rectifier, IBM, Intersil, TDK, Hitachi, Hipro, Power-One) and the ERC program of the National Science Foundation under award number EEC-9731677.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

Chapter 1

Introduction

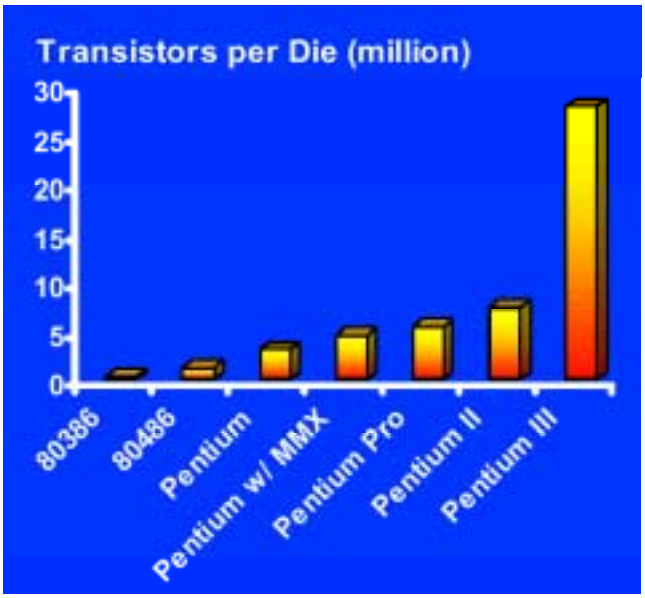
1.1 Background and Objectives

Advances in microprocessor technology challenge the power supplies of these devices. Complying with Moore's Law, which states that "transistor density … doubles every eighteen months," the transistors per die in the microprocessors have been increasing steadily in the past decade, as shown Fig. 1.1 [A2].

The increasing number of transistors in the microprocessors results in continuous increase of the microprocessor current demands. In order to reduce the power consumption of the microprocessors, the supply voltages have been decreased, as shown in Fig. 1.2 [A2]. Moreover, due to the high frequencies, the microprocessors' load transition speeds also increase. The trends for microprocessor current demands and load current slew rates are shown in Fig. 1.3 [A2]. The low voltage, high current and fast load transition speeds are the challenges imposed on microprocessors' power supplies.

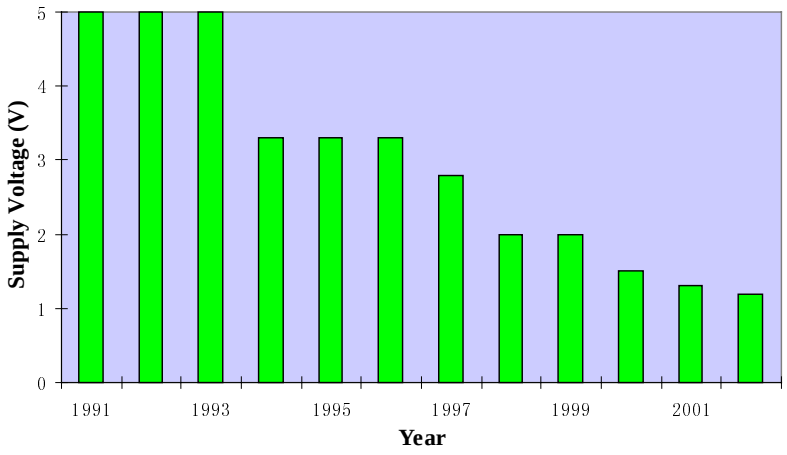
Starting from the Intel Pentium ^{TM} microprocessor, microprocessors began to use a non-standard power supply of less than 5V. Opposite to the voltage decrease, the current requirements of the microprocessors greatly increased. Because of the microprocessors' low voltage and high current demands, the parasitic resistors and inductors of the connections between the centralized silver boxes and the microprocessors have a severe, negative impact on power quality. It is no longer practical for the bulky silver box to provide energy directly to the

microprocessor. It is now necessary to power the microprocessors of computer systems with dedicated converters, voltage regulator modules (VRMs).



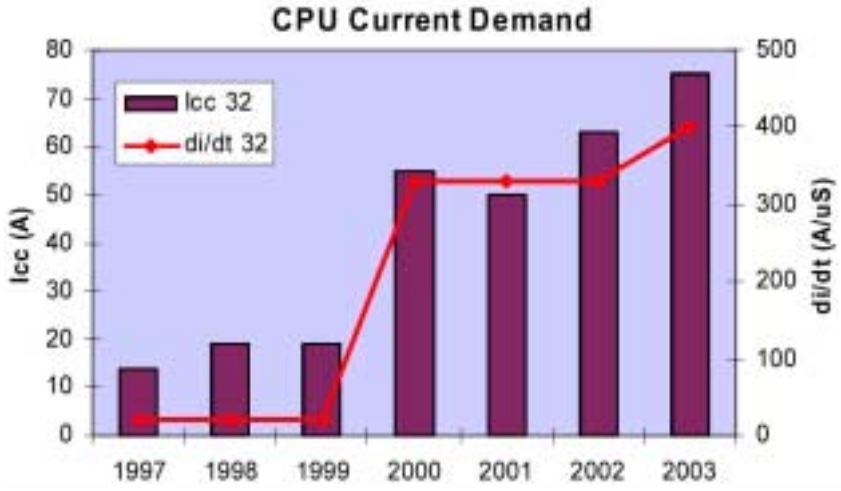
(From *Intel Technology Symposium 2000*, by Jerry Budelman, Intel)

Fig. 1.1. Number of transistors in the microprocessors increases exponentially.



(Based on data from *Intel Technology Symposium 2000*, by Dr. Anthony J. Stratakos, Volterra)

Fig. 1.2. Microprocessors' supply voltages decrease in order to reduce power consumption.



(From *Intel Technology Symposium 2000*, by Mike Walters, Intersil)

Fig. 1.3. Current demands and load transition slew rates of the microprocessors continuously increase.

In order to minimize the impact of the parasitic impedance on the VRM transient response, VRMs need to be located very close to the microprocessors. There are basically two types of VRMs: modular VRM, which is a power module that can be plugged into a standard socket on the motherboard, and the on-board VRM, which is built directly onto the motherboard, as shown in Fig. 1.4 and 1.5, respectively.

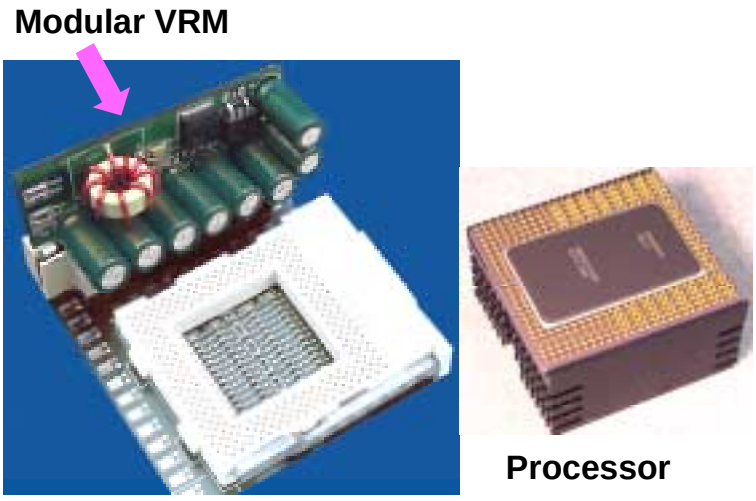


Fig. 1.4. Modular VRM.

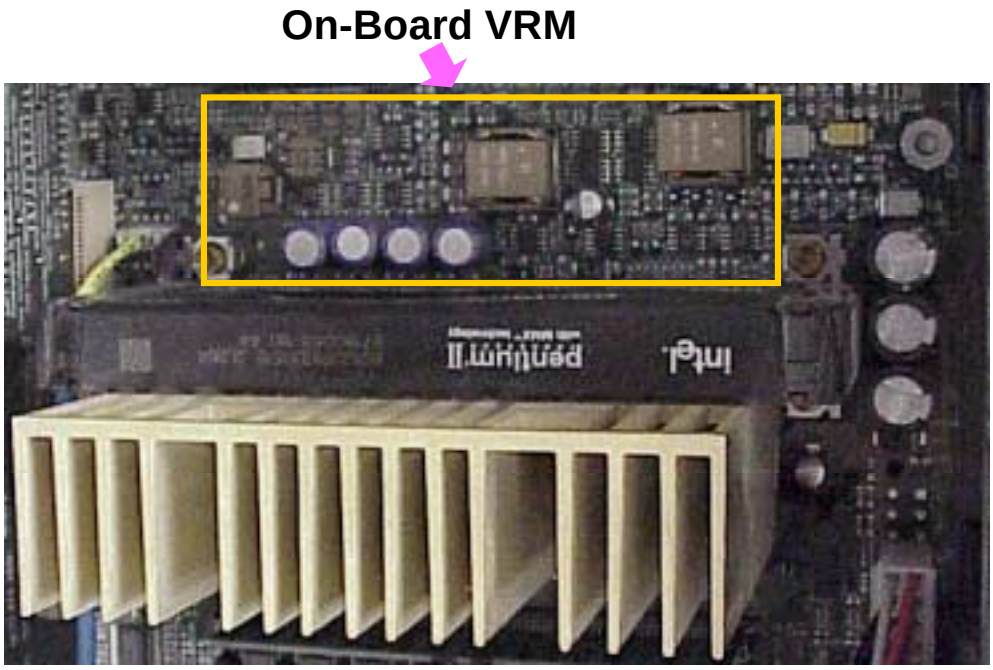


Fig. 1.5. On-board VRM.

The major benefit of the modular VRM is that the VRM is changeable. The purpose of the on-board VRM is to reduce the connection parasitic impedance of the connection socket between the VRM and the motherboard. Because of the stringent requirements of the VRM transient responses, the parasitic impedances between the VRMs and the microprocessors have to be minimized. The on-board VRMs are more common in recent years' desktop PC systems.

The purpose of the VRM is to maintain the voltage to the microprocessor during its transient response periods. When the microprocessor switches between "sleep mode" and "active mode," and vice versa, the current demand of the microprocessor transits between no load and full load with very high current slew rates. During operation, the microprocessors also have fast transitions between different load levels due to the number of transistors involved in the computations. Because of the tremendous clock speed of the microprocessor, the transitions need to be completed quickly, which imposes very high current slew rates on the VRMs. The transition corresponding to microprocessor load current

increase is called the step-up transient. The load current decrease transition is called the step-down transient.

For the next generation of microprocessors, the supply voltage is expected to decrease to about 1V in order to reduce power consumption. The transient voltage tolerance is also expected to decrease to 2%. For a 1.2V VRM output, the voltage deviation is only ±36mV. High load currents, high current slew rates and low voltage variances are the most stringent requirements of the VRMs.

Moreover, because of the high cost of the board area in computers, power density and efficiency are also very important. The synchronous rectifier buck is the most common circuit topology of conventional VRMs. The synchronous buck is efficient in low-voltage applications. High power density means that the output capacitors of the VRMs are limited. The VRMs should be able to quickly transfer energy from the input to the output during the transient response periods. Small inductances enable this action. However, small inductances also result in large current ripples in the converter, which increase the steady-state voltage ripples at the output capacitors. In order to improve the transient responses, the inductances need to be so small that the steady-state voltage ripples could be comparable to transient voltage spikes. It is impractical for the converter to work this way.

Multi-channel interleaving greatly reduces the total current ripples flowing into the output capacitors, making practical those VRMs with very small inductances. With the current ripple reduction, the steady-state voltage ripples at the output capacitors are greatly reduced. The transient voltage spikes can also be reduced due to the smaller output inductances. A much smaller output capacitance can meet the requirements of both the transient voltage spikes and the steady-state output voltage ripples.

Another serious disadvantage of the large current ripple is the losses that occur in MOSFETs. Large current ripples not only increase the conduction losses

but also increase the turn-off losses of the top MOSFETs. The large current ripples in the inductors also increase the losses in the inductors. The current ripples in the MOSFETs and the inductors are the same as those in the converters with the same number of channel in parallel. Although channel interleaving reduces the current ripple flowing into the output capacitors, it cannot reduce the current ripples in either the MOSFETs or the inductors. These ripples reduce steady-state efficiency.

To achieve fast transient responses, a small inductance is preferred. However, from the standpoint of efficiency, a large output inductance is required. Although these requirements are contradictory, they are both very important for the VRM.

Finding a way to improve transient responses of VRMs without compromising their efficiency is the main purpose of this dissertation.

1.2 Resonant Loops in Conventional VRM Transient Responses

The most common circuit topology of conventional VRMs is the synchronous rectifier buck, as shown in Fig. 1.6. The parameters of interconnection in the circuit are typical for a desktop PC system with Pentium Pro microprocessor.

In order to limit the output ripples at steady state, large output filter inductors are used. The typical values are 2~4μH. The parasitic parameters play very important roles in VRMs. The physical capacitors can no longer be simplified as ideal capacitors. The capacitor should be considered as an ideal capacitor in series with an equivalent serial resistor (ESR) and an equivalent serial inductor (ESL). The parasitic inductors and resistors of the interconnections cannot be neglected either.

There are four different capacitors in the topology shown in Fig. 1.6. The capacitor inside the block marked as "synchronous rectifier buck VRM" is the bulk output capacitor of the VRM. It consists of the physical capacitors (usually electrolytic capacitors) with large capacitances and high power densities. The "decoupling capacitors" are usually small ceramic capacitors with low ESR. There are also microprocessor packaging and die parasitic capacitors, as shown in Fig. 1.6.

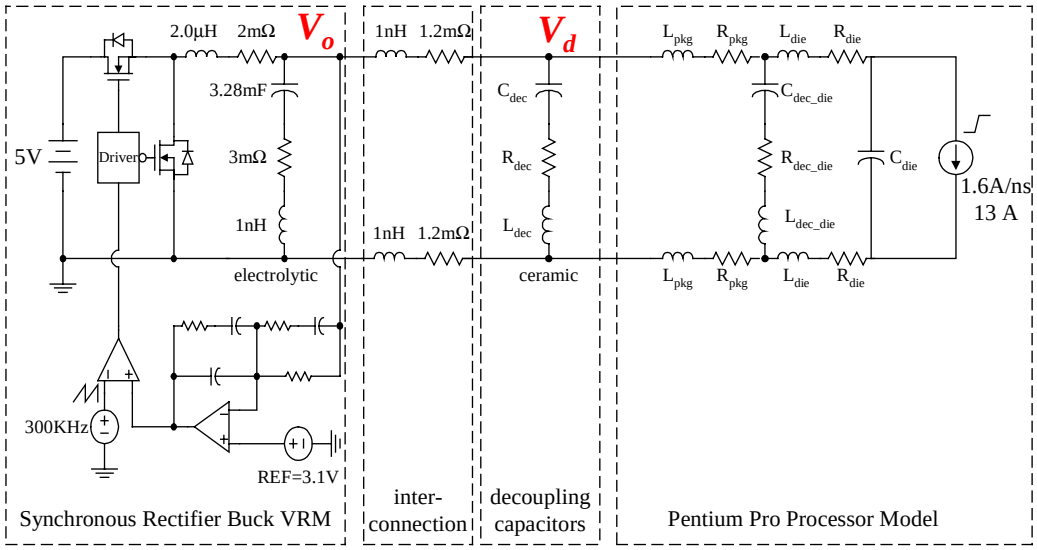


Fig. 1.6. Pentium Pro microprocessor simulation model.

The parasitic parameters of the connections are represented as the resistors and inductors in the figure. The connections include the parasitic parameters between the VRM and the decoupling capacitors, the decoupling capacitors and the microprocessor chip. Even inside the chip, there are parasitic parameters associated with the packaging.

The typical step-up transient voltage waveforms at the VRM output V_o and the decoupling capacitors V_d are shown in Fig. 1.7. The VRM output voltage has three spikes marked as "1st spike," "2nd spike" and "3rd spike." For the Pentium Pro, the transient voltage deviation limit at the VRM output is 5%, and is 7% at

the decoupling capacitors. The waveforms show that they both meet their requirements.

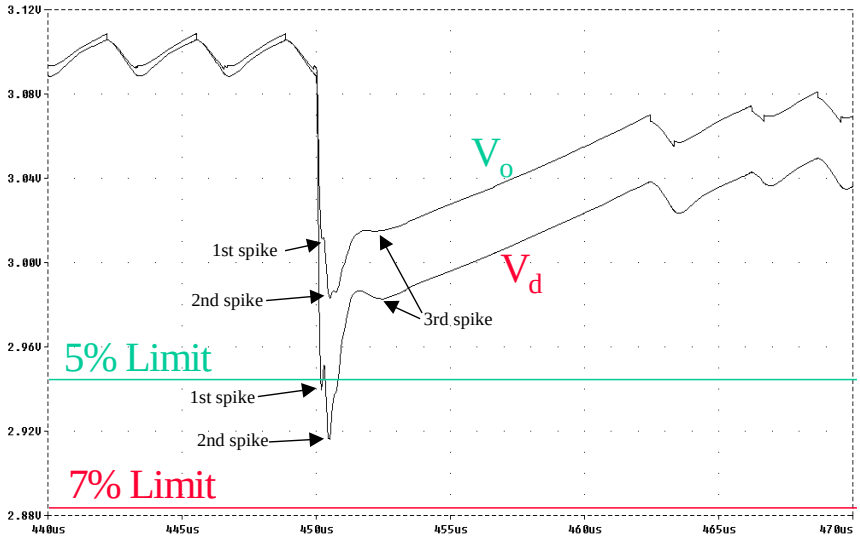


Fig. 1.7. Transient voltage waveforms at the VRM output and the decoupling capacitor in the Pentium Pro model.

The three spikes have different time constants. Analysis shows that the different spikes are due to the different resonant loops in the VRM and microprocessor system. The different resonant loops are marked in Fig. 1.8.

The first spike is due to the resonant loop formed by the ceramic capacitors, the packaging capacitors, and the interconnection parasitic parameters between them. The parameters in the loop are capacitors, inductors and resistors. This is basically a second-order system. The resonant frequency of the loop can be easily calculated. The second spike is due to the resonant loop formed between the VRM output capacitors and the decoupling capacitors. This is still a second-order system. The elements in these two resonant loops are all passive components. The only way to reduce the first two voltage spikes is the parameters of the capacitors and the connections. The third spike is due to the feedback control of the VRM. As it is shown in Chapter 3, the loop can also be approximated as a second-order system.

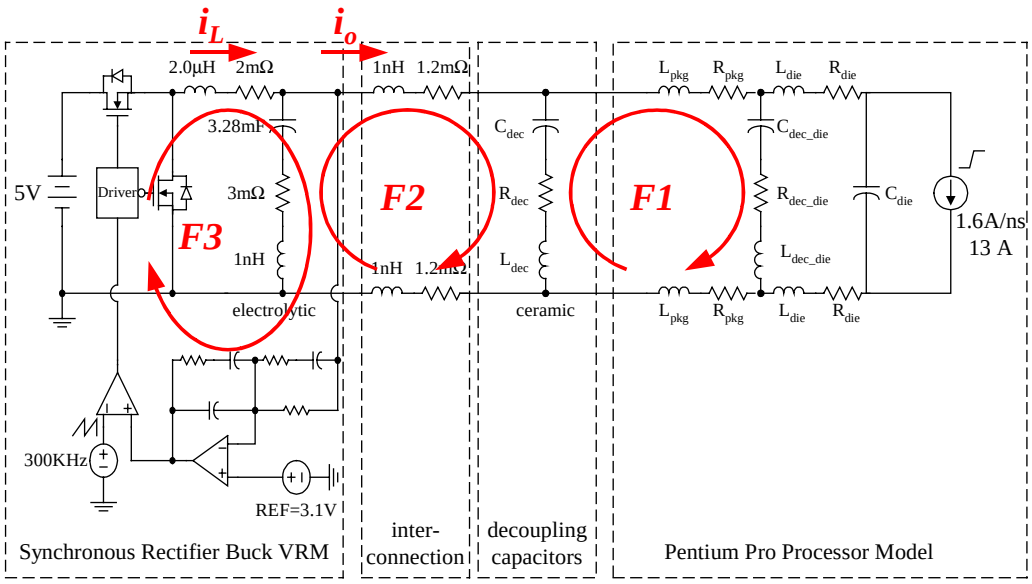


Fig. 1.8. The three resonant loops in the system determine the three transient voltage spikes.

The characteristic frequencies of the three loops are marked as *F1*, *F2* and *F3*, respectively, in Fig. 1.8. Because of the different parameters in the different loops, the three frequencies are well separated, i.e. *F1>>F2>>F3*. Because of the separation of the frequencies, the loops can be decoupled. A typical resonant loop is shown in Fig. 1.9. The corresponding current waveforms are shown in Fig. 1.10.

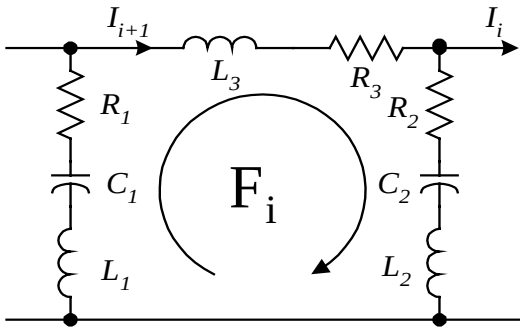


Fig. 1.9. The resonant loops in the VRM-microprocessor system can be decoupled.

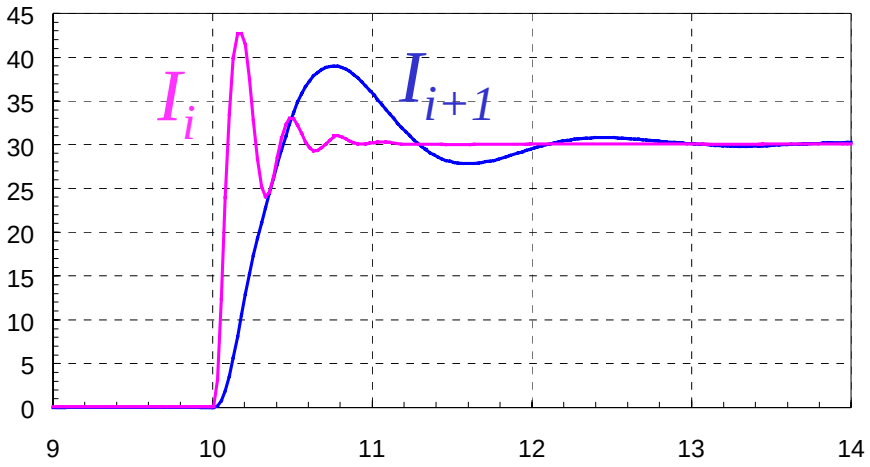


Fig. 1.10. Typical current waveforms of a resonant loop: I_i and I_{i+1} can be approximated as a step input and a step response of a seconde-order system, respectively.

The current I_i can be approximated as the step input to the resonant loop. The current in the loop, I_{i+1}, can be approximated as the step response of the resonant loop. The step response of a second-order system is determined only by the characteristics of the system. The current I_i would not affect the shape of I_{i+1}, because the change of the current I_i is too fast for the loop to have a response. The frequency shown in the current I_{i+1} is just the resonant frequency of the loop. In this sense, the different resonant loops in the system can be decoupled. Decoupling the resonant loops eases the design of the different loops.

1.3 VRM Output Capacitor Estimation

As shown in Fig. 1.10, the difference between the two current waveforms causes the unbalanced charges that need to be provided by the corresponding capacitors. The VRM output capacitors must hold the voltage during the transient response to provide the unbalanced charges. Based on unbalanced charges, the

output capacitance can be estimated. The unbalanced charges are due to the different slew rates between the current flowing into and out of the VRM output capacitors. The unbalanced charges can be approximated as the shaded areas shown in Fig. 1.11. The definitions of the two currents are in given in Fig. 1.8.

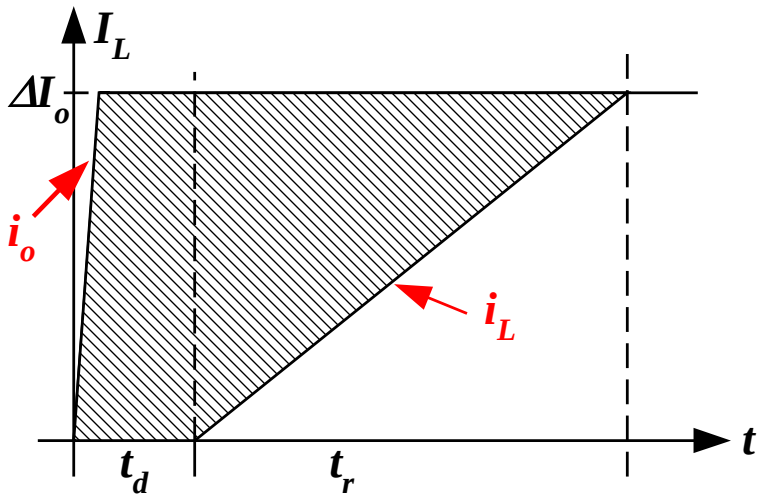


Fig. 1.11. Unbalanced charges of VRM output capacitors.

The unbalanced charges can be divided into two parts: the delay time t_d and inductor current rise time t_r.

The delays in the real circuit include the MOSFET gate driver delay, the MOSFET turn-on and turn-off delays, etc., but the majority is the switching action delay, which is discussed in detail in the Appendix. In trailing-edge modulation, the switching action causes delays in step-up transients. The worst case scenario relates to the load transient occurring at the turn-off edge of the top switch. The delays in step-down transients are insignificant in trailing-edge modulation. However, in leading-edge modulation, the situation is the opposite. The step-up transients do not have much delay. The switching action delays mainly occur in the step-down transients. The worst case scenario relates to the load transient occurring at the turn-on edge of the top switch. For output

capacitance estimation, the delay in the worst case should be used. The delay is basically determined by the circuit operation and will not be discussed further.

The rise time t_r depends on the inductor current slew rate, and can be calculated as follows:

$$t_r = \frac{\Delta I_o}{SR(I_L)}, \tag{1.1}$$

where $SR(I_L)$ is the inductor current slew rate.

In the cases in which the duty cycle is not saturated during transient responses, $SR(I_L)$ represents the average inductor current slew rate, which is discussed further in Chapter 3. For the cases in which the duty cycle is saturated during transient responses, the inductor current slew rates for the step-up and step-down transients can be easily found, as follow:

$$SR(I_L)_{up} = \frac{V_{in} - V_o}{L}, \text{ and} \tag{1.2}$$

$$SR(I_L)_{down} = \frac{-V_o}{L}. \tag{1.3}$$

Because of the separation of the different loops' frequencies, the transient load current slew rate is much higher than the VRM inductor current slew rate. The rise time of the load current can be ignored. The unbalanced charges in the shaded area can be described as follows:

$$Q = \Delta I_o \cdot t_d + \frac{1}{2} \cdot \Delta I_o \cdot t_r. \tag{1.4}$$

While providing the unbalanced charges, the VRM output capacitors have a voltage drop of ΔV_o. The required capacitance is as follows:

$$C_{out} = \frac{Q}{\Delta V_o} = \frac{\Delta I_o}{\Delta V_o} \cdot (t_d + \frac{t_r}{2}). \tag{1.5}$$

The preceding formula gives the minimum requirement of the VRM output capacitance. Of course, the ESR and ESL of the capacitors also cause voltage drops during transient responses. These will not be discussed further.

1.4 Multi-Channel Interleaving VRMs

In order to reduce the VRM output capacitance, a large inductor current slew rate is preferred. Smaller inductances give larger inductor current slew rates, so that a smaller VRM output capacitance can be used to meet the transient requirements. In order to greatly increase the transient inductor current slew rate, the inductances need to be reduced significantly, as compared with those in conventional designs.

However, small inductances result in large current ripples in the circuit steady-state operation. The large current ripples generate large steady-state voltage ripples at the VRM output capacitors. The steady-state output voltage ripples can be so large that they are comparable to transient voltage spikes. It is impractical for the converter to work this way. Moreover, the large current ripples also worsen the electromagnetic interference (EMI) problems and increase the losses in the output capacitors, the conduction and switching losses in the MOSFET and the copper losses in the inductors.

In 1997, VPEC (CPES) proposed using interleaving technology to solve the large current ripples in quasi-square-wave (QSW) VRMs. Interleaving greatly reduces the current ripples to the output capacitors, which in turn greatly reduces the steady-state output voltage ripples, making it possible to use very small

inductances in VRMs to improve transient responses. Interleaving VRMs with small inductances reduce both the steady-state voltage ripples and the transient voltage spikes, so that a much smaller output capacitance can be used to meet the steady-state and transient voltage requirements. The power density can be significantly improved. Moreover, interleaving makes the thermal dissipation more evenly distributed. Studies show that in high-current applications, the overall cost of the converter can be reduced using interleaving. The concept of applying interleaving to VRMs is so successful that it has become standard practice in VRM industry.

The topology of an n-channel interleaving buck converter is shown in Fig. 1.12. It consists of n identical converters with interconnected input and output. The duty cycles of adjacent channels have a phase shift of $\varphi = \frac{360^o}{n}$, where *n* is the total channel number.

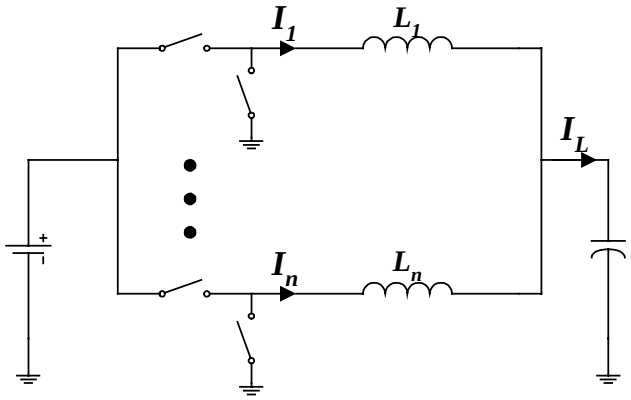


Fig. 1.12. Topology of n-channel interleaving buck converter.

The current ripple cancellation effect in interleaving topology is defined as follows:

$$k = \frac{\Delta I_L}{\Delta I_i}, \quad (i=1, 2, \ldots, n), \tag{1.6}$$

where ΔI_L is the peak-to-peak value of the total output current, and ΔI_i is the peak-to-peak value of the individual inductor currents. The ripple cancellation effect is a function of the channel number and steady-state duty cycle. For a multi-channel interleaving buck converter, the steady-state current ripple reduction effects are shown in Fig. 1.13.

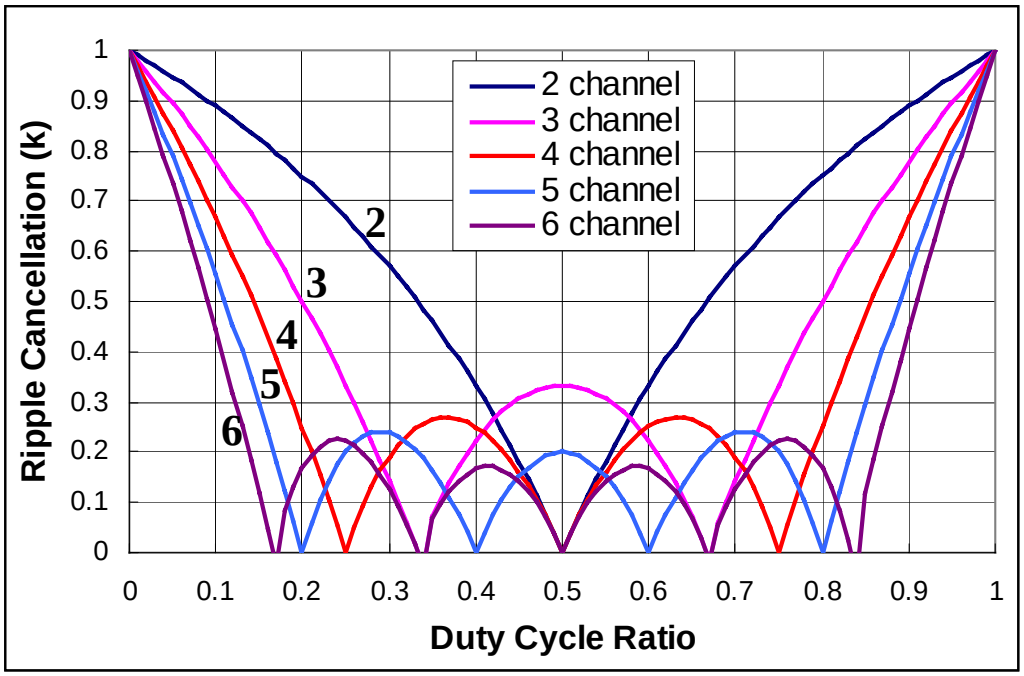


Fig. 1.13. Current ripple reduction in interleaving buck converter.

For every steady-state cycle, there is a corresponding channel number that gives ripple-free total output current. The n-channel interleaving structure gives (n-1) ripple-free points at:

$$D = \frac{m}{n} \qquad (m = 1,2,\cdots,n-1)\,. \tag{1.7}$$

Interleaving technology not only reduces the current ripple in the total output currents, but also increases the total output current frequency. The ripple frequency of the total inductor currents is n times the frequency of each channel.

The high current ripple frequency has two main benefits in transient responses. The switching action delay in the worst cases can be reduced, which is discussed in the Appendix. The high current ripple frequency also affects the small-signal model of the converter, which will be discussed in Chapter 2.

The preceding discussions have detailed the advantages of interleaving topology. However, it is important to note that channel interleaving only reduces the total output current; the inductor current in each channel still has large ripples if small inductances are used. The large conduction and switching losses in the MOSFET and the copper losses in the inductors that occur due to the large current ripples are problems that cannot be solved in channel interleaving. These losses comprise the majority of total losses in VRMs. Basically, interleaving cannot improve the efficiency. The conflicting requirements of inductance in transient response and steady-state efficiency are not solved in channel interleaving. Utilization of small inductances in interleaving VRMs improves the transient responses, but at the expense of steady-state efficiency. Finding a way to improve the transient responses without compromising the efficiency is the objective of this dissertation, and will be discussed in the following chapters.

Another drawback of applying interleaving is the increased complexity of the circuit. Compared to single buck converters, the multi-channel interleaving structure has more components. The number of MOSFETs is determined by the power level, losses, cost, etc. Interleaving VRMs require more complicated controllers not only because they have more control signals but also because of the timing and matching of control signals in different channels. In interleaving VRMs, current sharing control among channels is usually a necessity in order to balance the load among the channels. This is another factor that makes the interleaving controller more complicated. Fortunately, with the varieties of commercial control integrated circuits (ICs), the cost of the controller is acceptable. Interleaving VRMs also involve more inductors than are required by a

single-channel VRM. This dissertation also discusses utilization of integrated magnetic components to simplify the topology and improve its performances.

In summary, multi-channel interleaving reduces the steady-state current ripples to the output capacitors, which enables the use of small inductances in VRMs in order to improve transient responses. Because of these improvements, a much smaller output capacitance can be used, thus improving the power density. However, interleaving cannot improve efficiency. The transient response improvements in interleaving VRMs compromise steady-state efficiency.

1.5 Literature Review and Dissertation Outline

This dissertation is composed of six chapters and appendices.

Chapter 1 is the background review of existing VRM technologies related to the topic of this dissertation. The challenges of the VRM are the low voltage, high current, fast transient responses and high efficiency [A1-7]. Although the topology of the conventional VRM is very simple, which is just a single buck, lots of work has been done to optimize the design of the converter [A8-14]. The resonant loops formed by the parasitic parameter in the VRM-microprocessor system have different resonant frequencies, which cause the three spikes in the VRM transient responses [A15-16]. The VRM transient voltage drops can be estimated from the unbalanced charges. In order to reduce the unbalanced charges, small inductances have to be used, which generate large current ripples. The ripple cancellation in multi-channel interleaving converter makes it possible to use very small inductances in VRM to improve the transient responses [A17-23]. However, each channel still has large current ripple, which reduces the converter efficiency. Although the light load efficiency can be improved by turning off the synchronous rectifiers to reduce the current ripples [A24], the efficiency at heavy

load still suffers. The main objective of this dissertation is to discuss the design of inductors to improve the converter efficiency while maintaining the fast transient responses of interleaving QSW VRM. The high frequency [A26-29] and high input voltage (both non-isolated [A30-33] and isolated [A34-38]) are the hot research areas of VRM. The results of this dissertation can also be applied to high frequency and high input VRMs.

Chapter 2 discusses the small-signal equivalent model of the multi-channel interleaving buck VRM. The average models (both state average model [B1-3] and PWM switch cell model [B4-6]) give accurate small-signal model for PWM converters. Based on the average model, the equivalent inductance of the parallel buck converter (interleaving converter can be considered as a special case of parallel converters) can be found as 1/n of the inductance in a channel [B7]. However, the average models do not have switching frequency information, which is important when the converter is designed to very high bandwidth. Although it is taken for granted in some circumstances that interleaving improves the bandwidth limit, it is not strictly proven. The sampled-data model [B8-11] and the describing function method [B13-16] have the switching frequency information in the small-signal model. The bandwidth limitation of interleaving converters could be found with these methods. However, the models involve difficult mathematic derivation. Thanks to the great improvements of computer technology and circuit simulation software, the small-signal model of a PWM converter can be found through switching circuit simulation with SIMPLIS [B17]. This chapter utilizes the advanced simulation software to verify the equivalent switching frequency of the interleaving buck converters. The effects of the large current ripples in each channel on the small-signal transfer functions can be ignored [B19-21].

Chapter 3 analyzes the inductance and control bandwidth effects on VRM transient responses. The concept of critical inductance is presented. The critical

inductance is the largest inductance that gives the fastest transient responses. The basic theory behind the concept of critical inductance is the optimal control of systems with limited input, which can be found in many control textbooks [E3-4]. In control systems, the purpose is to design the optimal control strategy for a fixed object. However, in critical inductance discussion, the purpose is to design the object to fully utilize the limited control input so that the optimal control target can be achieved.

Chapter 4 proposes the concept of applying coupling inductors between the interleaving channels with 180^{o} to reduce the steady-state current ripples and improve transient responses. The converter efficiency can be increased without compromising the transient responses. The concept of coupling inductors begins with the objective to improve the non-coupled integrated inductors in interleaving VRMs proposed by Dr. Wei Chen [C3-4]. Many integrated magnetic concepts have been proposed to improve the performances of power converters [C5-13]. In order to improve the power density of VRMs, low profile planar cores are used. The high switching frequencies of VRMs generate special design issues for the planar cores [C14-21]. The winding and air gap design has important effects to the losses in the high frequency planar magnetic components [C22-28]. However, the core and winding structure of the non-coupled integrated inductors [C3-4] not only is mechanically unstable but also has large winding losses due to the large air gap in the outer legs. In order to solve the problem, coupling effects are introduced in the integrated inductors. Further analysis shows that the coupling integrated inductors reduce the steady-state current ripples and improve transient responses, which turn out to be the major benefits of the coupling inductors. Finite element analysis (FEA) results show that the proposed integrated coupling inductors reduce both the core and winding losses.

In order to extend the coupling inductor concept to more channels, Chapter 5 proposes a novel magnetic modeling concept based on the flux source reluctance

model. Examples used in this chapter show both how to apply the model to different magnetic structures and the benefits of this magnetic model. For two-channel coupling inductors, the π-model is the simplest model. However, the π-model extended to three coupling inductors is very difficult to use, and it is impractical to be extended to more than three coupling inductors [D2]. The Δ-model, which is directly derived from the coupling inductor equations (5.2), can be extended to more coupling inductors [D3]. However, the parameters in the model are difficult to derive either from the core structure or the measurement results.

Using duality between the electric circuit and reluctance circuit, the parameters in the magnetic model can be easily derived from the reluctance circuit [D4-5]. However, for some structures, the inductors required in the model can be much more than the physical inductors. Moreover, ideal transformers are required in the models for inductors with different turns, which usually cause converging problems in simulation [D6]. The model proposed by Dr. Qing Chen is a modification of π-model [D5]. The parameters in the model can be derived from FEA of the structure geometry or the measurement results. However, the model is very complicated with large number of inductors.

Based on the analogy between the electric and magnetic circuits, the reluctance model can be directly included in the electric simulation circuit with an interface [D6-7]. Although, the concept is straightforward, the interface is complicated and time-consuming in computer simulation.

The objective of the magnetic model proposed in Chapter 5 is to evaluate the different coupling core structures. The model is based on the magnetic reluctance circuit, which is assumed can be derived from the core and winding structures as in [D3-6]. In multi-winding transformers with complicated winding structures, derivation of the parameters in the reluctance model can also be very difficult

[D8-10]. In the coupling inductors, the winding structures are usually simpler. The reluctance model should be easier to derive. The derivation of the reluctance model is not discussed in this dissertation.

Complete models of magnetic components in power electronic circuits are very complicated including the parasitic parameters [D11-12], such as capacitive effects [D13] and losses [D14-15]. The parameters of the core materials are usually functions of temperature and frequency, which also affect the reluctance model [D16-17]. The magnetic model proposed in Chapter 5 does not deal with the capacitive effects, losses or the temperature and frequency effects to the material parameters.

As long as the reluctance model of a core and winding structure is given, the corresponding accurate electric simulation circuit can be derived based on the proposed modeling concept. Examples are provided to show how to apply the model to different magnetic structures.

Chapter 6 summarizes the conclusions and proposes ideas for future work.

Appendices include some in-depth analyses, which are related to the dissertation but are too detailed to be included in the chapters. The appendices include analysis of the switching action delays, phase margin's effect to inductor current rise time, transient analysis of coupling inductors in different duty cycle ranges, coupling effects on inductor current ripples, and some formula derivations.

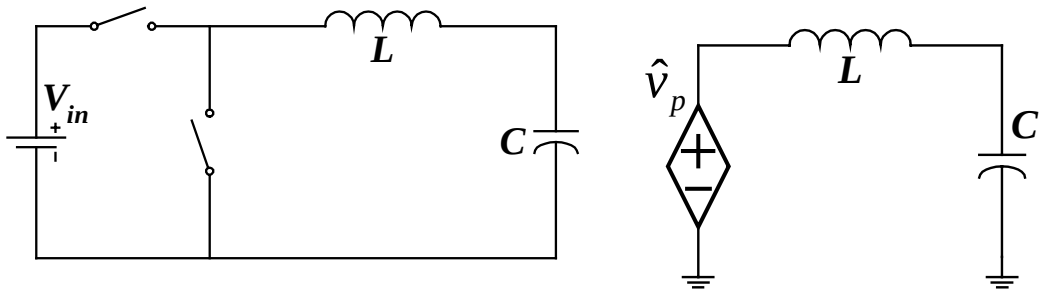
Chapter 2

Small-Signal Model of Interleaving Buck Converters

The multi-channel interleaving synchronous buck is the most common of today's VRM topologies. This chapter uses simulation software to verify its small-signal model, for which the interleaving buck can be simplified as an equivalent single buck. The equivalent inductance is 1/n of the channel inductance, and the equivalent switching frequency is n times the channel switching frequency for an n-channel interleaving buck.

2.1 Average Model of the Interleaving Buck

The average model is the most commonly used method for deriving the small-signal model of a converter. For the single buck converter shown in Fig. 2.1(a), the average model is shown in Fig. 2.1(b).



(a) (b)

Fig. 2.1. A single buck converter (a) and its average model (b).

The controlled voltage sources $\hat{v}_p$ in the figure represent the small signal perturbations, as follows:

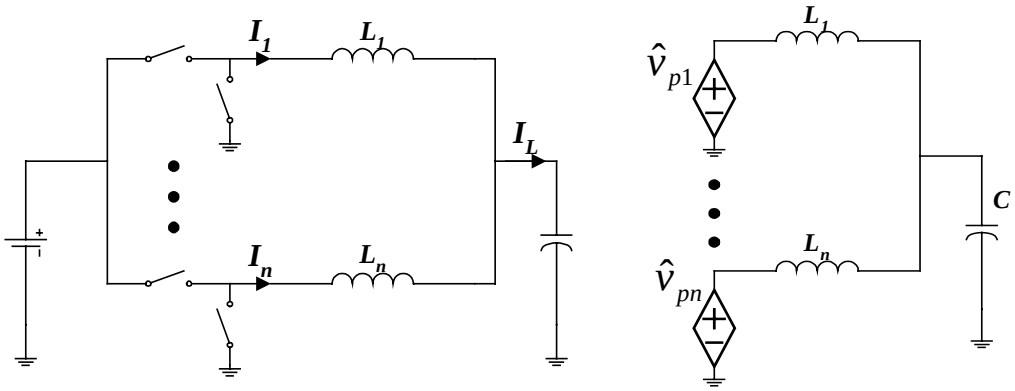
$$\hat{v}_p = (V_{in} + \hat{v}_{in}) \cdot (D + \hat{d}) - V_{in} \cdot D \,, \tag{2.1}$$

where V_{in} and D are the steady-state input voltage and duty cycle, respectively, and $\hat{v}_{in}$ and $\hat{d}$ are the small-signal perturbations of the steady-state input voltage and duty cycle, respectively. In this dissertation, constant input voltage ($\hat{v}_{in}$ =0) is assumed. In these cases, $\hat{v}_p$ can be simplified as follows:

$$\hat{v}_p = V_{in} \cdot \hat{d} \,. \tag{2.2}$$

The small-signal model can be easily derived from the average model shown in Fig. 2.1(b).

Based on the same method, the average model of a multi-channel interleaving buck can be derived. An n-channel interleaving buck and its average model are shown in Fig. 2.2.



(a) (b)

Fig. 2.2. An n-channel interleaving buck (a) and its average model (b).

For interleaving converters, the input voltages for each channel are the same. In voltage feedback control, the interleaving channels share the same compensator. There is only one error signal from the compensator. The duty cycle perturbation can be considered the same for different channels. Thus, the small perturbation signals $\hat{v}_p$ are the same in different channels. These perturbations can be connected together, which makes the inductors for different channels in parallel. The inductors can be replaced by a single equivalent inductance L_{eq}, as shown in Fig. 2.3.

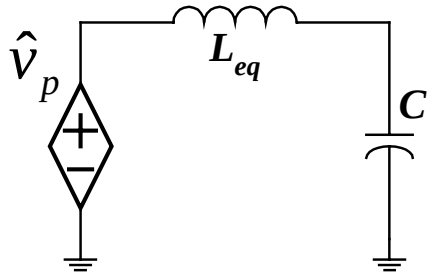


Fig. 2.3. Simplified small-signal model of an n-channel interleaving buck.

The equivalent inductance is simply the parallel of the inductors in different channels. For symmetric channels ($L_1=L_2=\ldots=L_n=L$), there exists

$$L_{eq} = \frac{L}{n}. \tag{2.3}$$

From Fig. 2.3, the small-signal model of the interleaving buck can be simplified as a single buck with the inductance equal to 1/n of the inductance in each channel.

In order to verify the validity of the simplified small-signal model of the interleaving buck, the control-to-output-voltage transfer function $G_{dv}'(s)$ of a four-channel interleaving QSW buck is measured for comparison from the hardware, the setup for which is shown in Fig. 2.4.

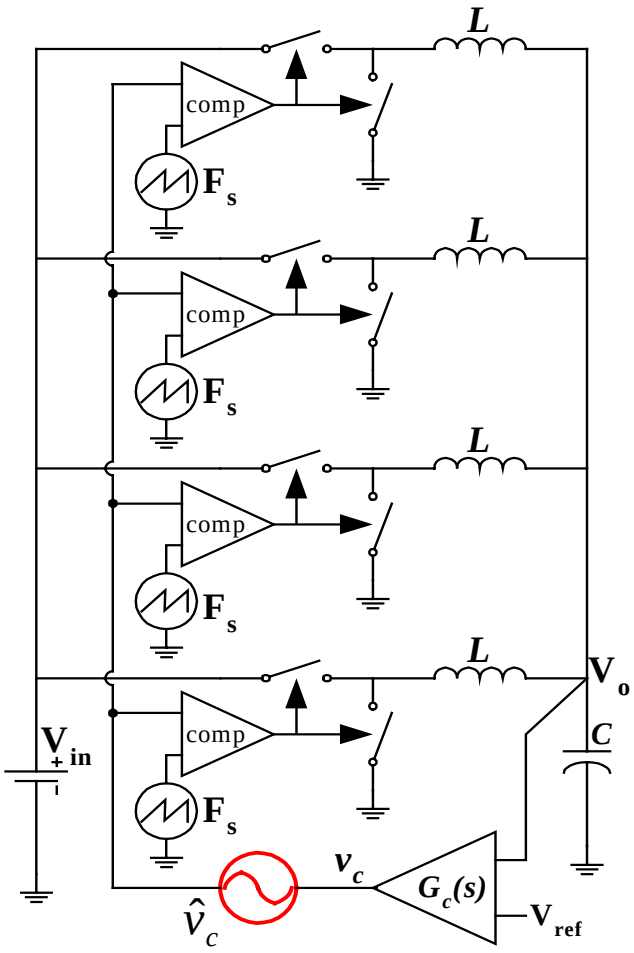


Fig. 2.4. Hardware setup of control-to-output-voltage transfer function measurement of a four-channel interleaving buck.

In the hardware measurements, a Hewlett-Packard 4194A impedance/gain-phase analyzer is used. The sinusoidal stimulus source from the analyzer, which is marked as $\hat{v}_c$ in the figure, is injected into the error signal from the compensator. This stimulus generates a perturbation at the VRM output voltage added upon its average DC value V_o. The reference channel of the analyzer is connected to $\hat{v}_c$, and the test channel of the analyzer is connected to the converter output. The tracking band-pass filter in the test channel of the analyzer allows only the VRM output voltage perturbation at the stimulus frequency (marked $\hat{v}_o$) to follow

through. The ratios between $\hat{v}_o$ and $\hat{v}_c$ at different frequencies determine the control-to-output-voltage transfer function $G_{dv}'(s)$, as follows:

$$G_{dv}'(s) = \frac{\hat{v}_o(s)}{\hat{v}_c(s)}. \tag{2.4}$$

It should be noted that the measured curve is different from the duty-cycle-to-output-voltage transfer function $G_{dv}(s)$. The relationship between $G_{dv}'(s)$ and $G_{dv}(s)$ is as follows:

$$G_{dv}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = V_{tr} \cdot \frac{\hat{v}_o(s)}{\hat{v}_c(s)} = V_{tr} \cdot G_{dv}'(s), \tag{2.5}$$

where V_{tr} is the magnitude of the sawtooth signal used for the comparator. The two transfer functions have the same shape and a constant coefficient.

The hardware measurement of the transfer function $G_{dv}'(s)$ is shown in Fig. 2.5.

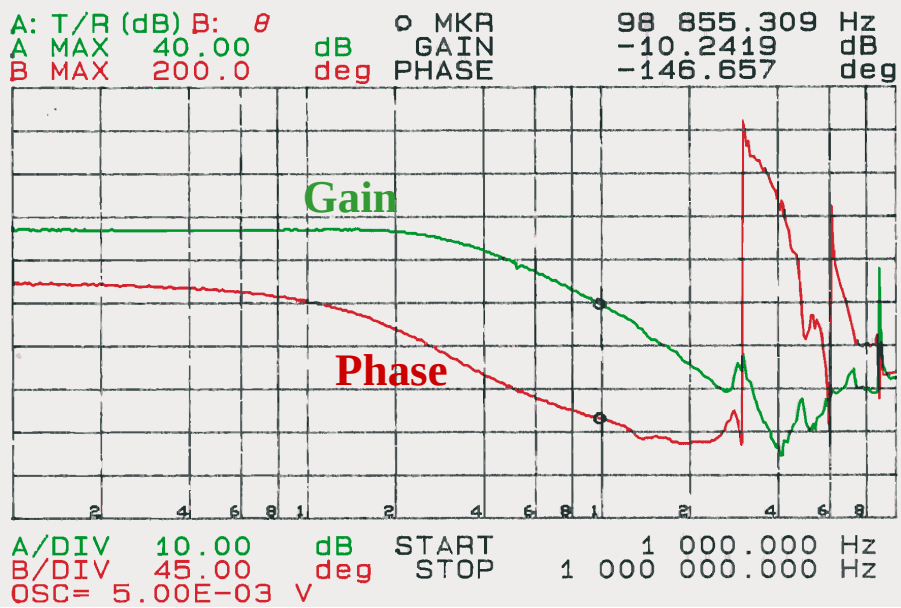


Fig. 2.5. Measurement of $G_{dv}'(s)$ from a four-channel interleaving QSW VRM.

The control-to-output-voltage transfer functions derived from the average model are shown in Fig. 2.6 for comparison. The dashed curve is the transfer function for one channel in the interleaving converter. The solid curve is the transfer function of the four-channel interleaving QSW buck VRM, based on the simplified average model shown in Fig. 2.3.

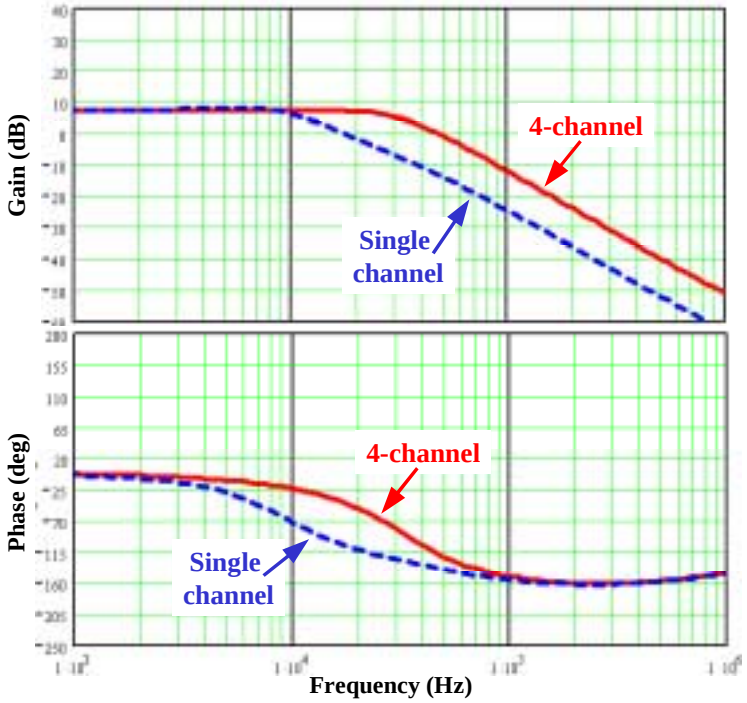


Fig. 2.6. $G_{dv}'(s)$ of interleaving buck based on the simplified average model.

The resonant frequency of the four-channel interleaving converter is higher than that of the single channel. This is because the equivalent inductance in the simplified model is smaller than the inductance in each channel.

The transfer function derived from the simplified average model closely matches the measurement results. This verifies the validity of the simplified small-signal model of the multi-channel interleaving buck. Another important quality shown in the comparison is that the large inductor current ripples in each channel do not affect the small-signal model of the interleaving buck. In

summary, the small-signal model of an n-channel interleaving buck can be simplified as a single buck converter with the equivalent inductance equal to 1/n of the channel inductance.

However, the average model is only an approximation of the switching circuit, and only describes the double poles of the converter. The average model does not contain information on switching frequencies. The switching frequency is important to the converter because it tells the limitation of the control bandwidth. For a single converter, it is conventionally granted that the average small-signal model is valid up to half of the switching frequency. What is the frequency to which the average small-signal model for the interleaving converters is accurate?

The simplified small-signal model in Fig. 2.3 cannot answer this question. In order to analyze the equivalent switching frequency of the interleaving buck, a different modeling method should be used.

2.2 Switching Small-Signal Model of the Interleaving Buck

There are quite a few models that address switching frequency issues; these include the sampled-data model, the discrete-average model, the discrete model, the harmonic balance method, etc. Jim Groves and Dr. Richard Tymerski published papers about these different models, which are accurate beyond the half switching frequency. The switching frequency can be seen in the model.

However, the problem common to these models is their complexity: All involve lengthy and difficult mathematic derivations, which prevents them from wide acceptance. This chapter uses a computer simulation tool to identify the switching frequencies in the small-signal models, thus avoiding the abstruse mathematics.

Start from the basic operation of a switching power converter. As shown in Fig. 2.4, the duty cycle is generated when the error signal v_c intersects the sawtooth signal. In steady-state operations, the error signal can be approximated as a constant voltage, which intersects the sawtooth signal in a different cycle at the same point, so that the constant duty cycle is generated, as shown in Fig. 2.7.

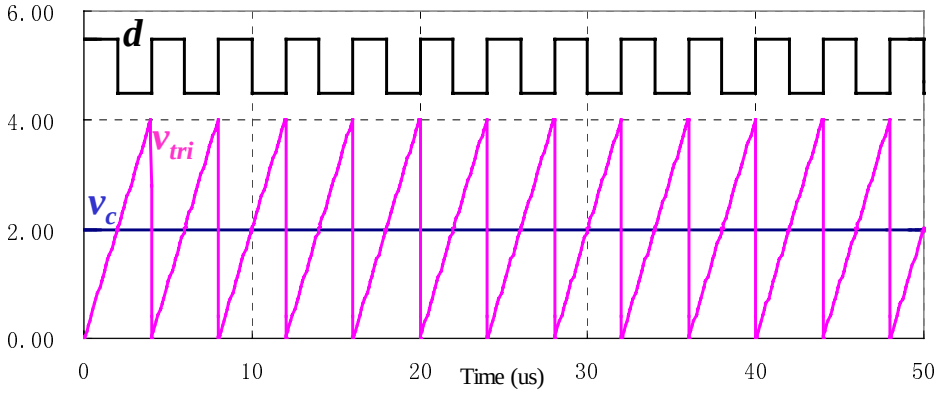


Fig. 2.7. Constant error signal generates constant duty cycle in steady state.

When a low-frequency sinusoidal perturbation signal $\hat{v}_c$ is added to the error signal, the error signal intersects the sawtooth at different points in different cycles. The duty cycle varies at the frequency of the perturbation signal, as shown in Fig. 2.8.

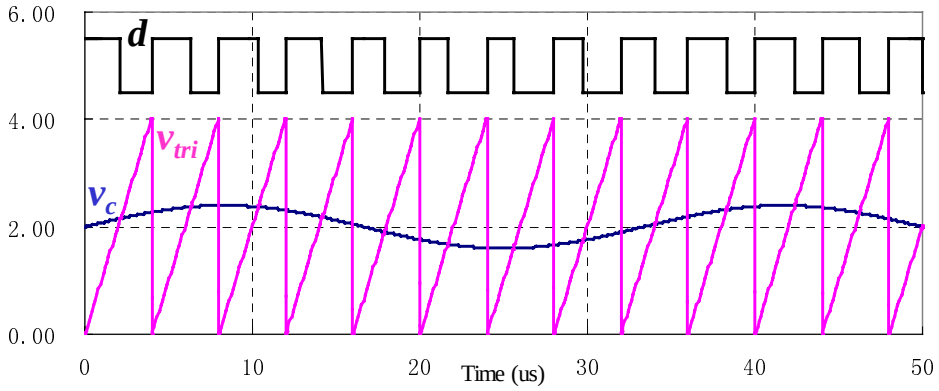


Fig. 2.8. Low-frequency perturbation in error signal generates perturbations in duty cycle.

The perturbation of the duty cycle results in the same frequency perturbation at the converter output voltage $\hat{v}_o$. The ratio between $\hat{v}_o$ and $\hat{v}_c$ at different frequencies determines the control-to-output-voltage transfer function $G_{dv}'(s)$.

The switching action can be considered as a sampling effect. The sampling frequency is the switching frequency. The sampling object is the error signal. The sampling point is the point at which the error signal intersects the sawtooth signal. A signal at the same frequency as the sampling frequency cannot be detected.

When the perturbation frequency of the error signal is the same as the sawtooth signal frequency, the error signal always intersects the sawtooth at the same point. This results in the constant duty cycle, as shown in Fig. 2.9. This is the same as it is in steady-state operation: A constant duty cycle results in constant output voltage, i.e. $\hat{v}_o$=0. A minimum point is expected on the transfer function $G_{dv}'(s)$ at the switching frequency.

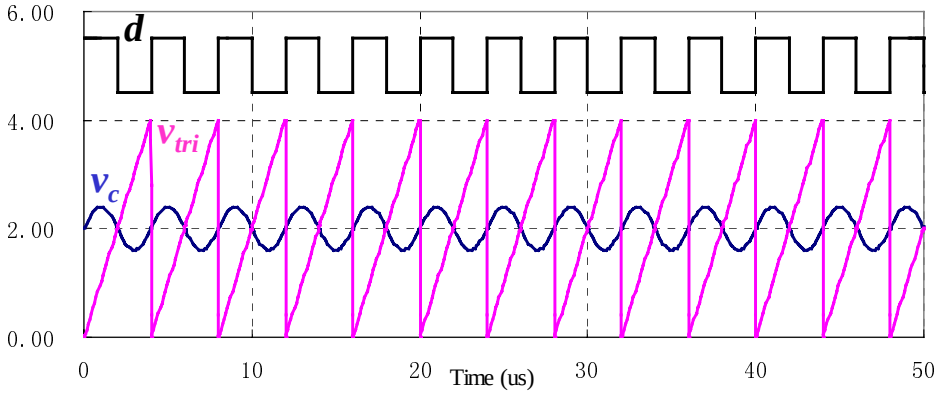


Fig. 2.9. Switching frequency perturbation in error signal results in constant duty cycle.

It is easy to imagine that if the perturbation frequencies of the error signal are integral multiples of the switching frequency, the error signal will always intersect with the sawtooth signal at the same point and give a constant duty cycle. Similar

to the previous discussion, minimum points are expected on the transfer function $G_{dv}'(s)$ at the integral multiple switching frequencies. The case of error-signal perturbation at three times the switching frequency is shown in Fig. 2.10; this simulation also results in a constant duty cycle.

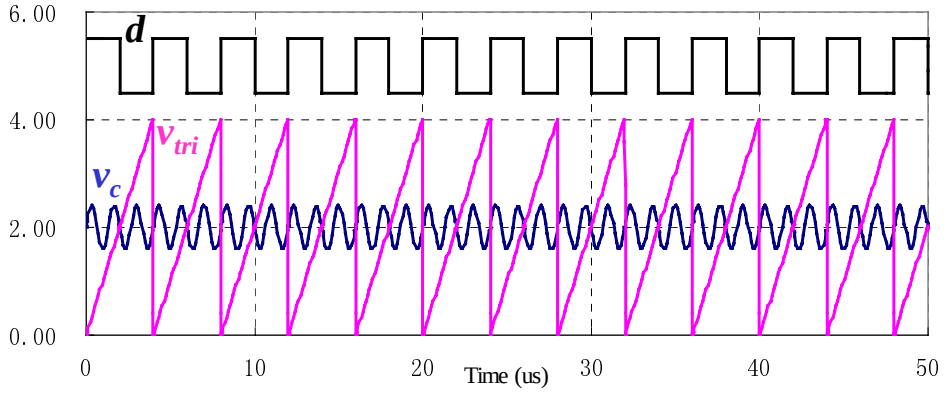


Fig. 2.10. Integral multiple switching frequency perturbation in the error signal results in a constant duty cycle.

The preceding discussion shows that switching frequency information can be present in the control-to-output-voltage transfer function $G_{dv}'(s)$. When the perturbation frequency of the error signal sweeps from low to high frequencies, the transfer function $G_{dv}'(s)$ should have minimum points at the integral multiples of the switching frequency.

This can be verified using circuit simulation. The switching model of the single buck converter shown in Fig. 2.11 is used for simulation. For simplicity, the parasitic parameters in the inductor and capacitor are not shown in the figure. The switching frequency is 300kHz.

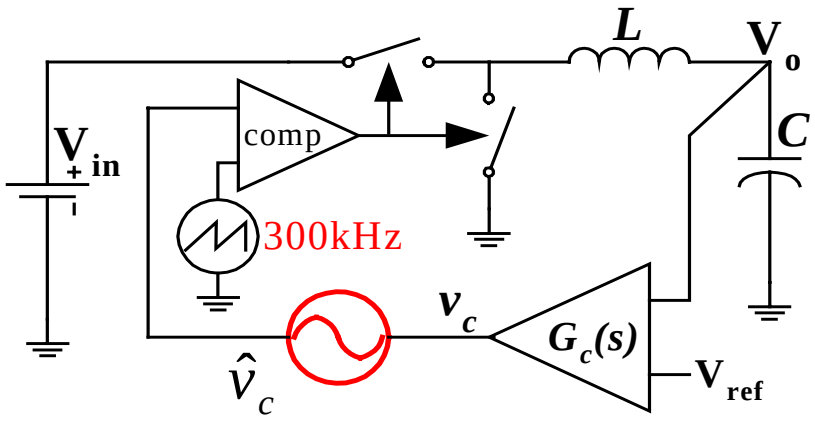


Fig. 2.11. Switching model of a single buck converter under simulation.

A perturbation signal $\hat{v}_c$ is added to the steady-state operation point. The ratios between the output voltage perturbations $\hat{v}_o$ and $\hat{v}_c$ at different frequencies are plotted in Fig. 2.12. This is the control-to-output-voltage transfer function.

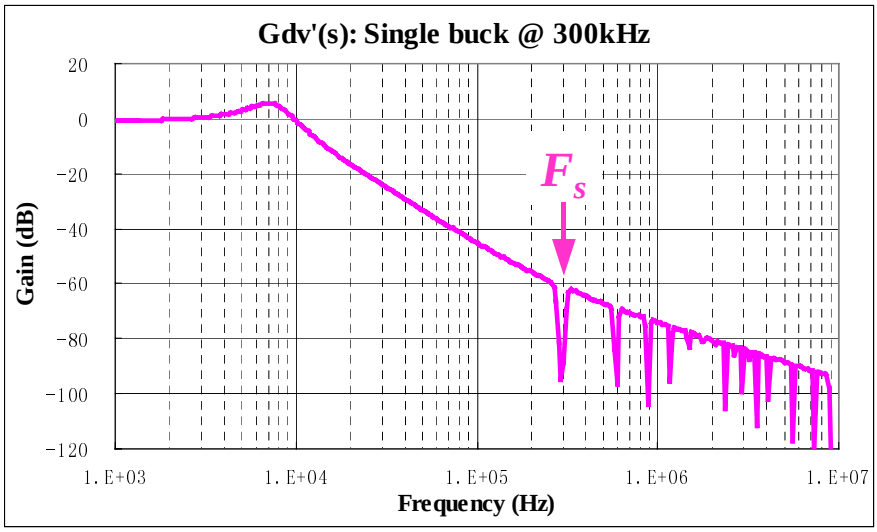


Fig. 2.12. $G_{dv}'(s)$ of a single buck based on circuit simulation.

The simulation software used is SIMPLIS. The results at different frequencies are based on the switching model simulation. The transfer function curve has

minimum points at the integral multiples of the switching frequency. The first minimum point occurs at the switching frequency, which is what was expected.

The purpose of this research is to determine the frequency limitation of the control bandwidth. In order to do so, the preceding simulation of a single buck is expanded to a four-channel interleaving buck, as shown in Fig. 2.4. The inductance in each channel is the same as that in the single buck. The output capacitances are the same in both cases. The switching frequency of each channel is 300kHz. The transfer function from the switching circuit simulation is shown in Fig. 2.13.

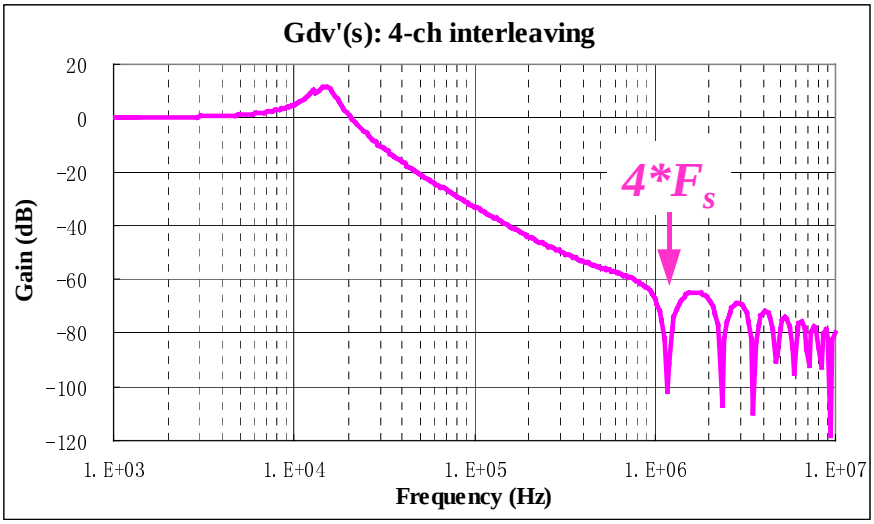


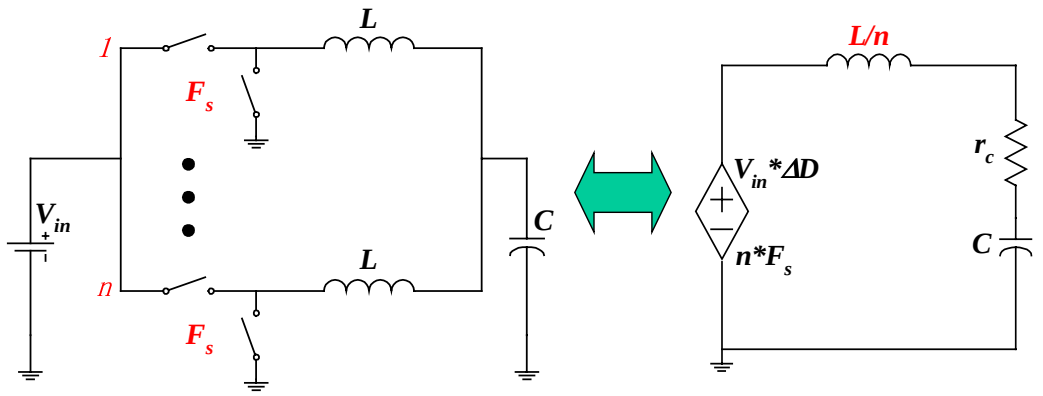
Fig. 2.13. $G_{dv}'(s)$ of four-channel interleaving buck based on circuit simulation.

It is clear that the first spike in the transfer function occurs at four times the switching frequency in each channel. This is similar to a single buck operating at four times the switching frequency. As discussed previously, the switching action is similar to a sampling effect. There are n switching actions in a switching cycle for an n-channel interleaving converter. This is similar to a single converter sampling at n times higher frequency. Thus, the equivalent switching frequency of an n-channel interleaving converter is n times the switching frequency in each

channel. Similar to the conventional average small-signal model, the simplified average small-signal model of n-channel interleaving converters shown in Fig. 2.3 is accurate up to n/2 of the switching frequency in each channel.

The double pole frequency in the transfer function of the interleaving buck converter is also higher than that in the single buck converter. This is consistent with the equivalent inductances discussion regarding the average small-signal model.

Based on the results of this simulation, the small-signal model of an interleaving buck can be simplified as a single buck converter, as shown in Fig. 2.14. The equivalent inductance in the simplified model is 1/n of the inductance in each channel. The equivalent switching frequency of the simplified model is n times the switching frequency in each channel.



(a) (b)

Fig. 2.14. An n-channel interleaving buck converter can be simplified as a single buck converter (*L/n, n*Fs*) for small-signal analysis: (a) n-channel interleaving buck; and (b) equivalent single buck converter.

The equivalent small-signal model of a four-channel interleaving buck is simulated to verify its validity. The small-signal transfer function is shown in Fig. 2.15.

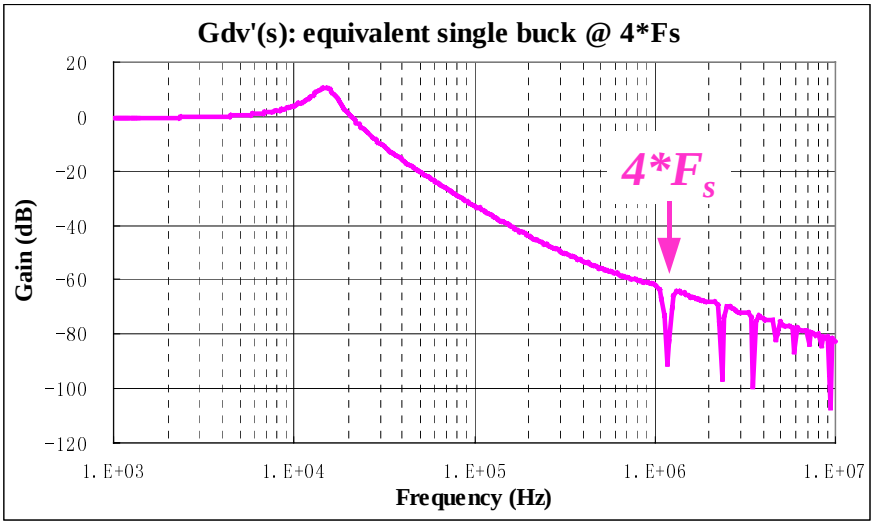


Fig. 2.15. The equivalent model gives the same small-signal transfer function as the four-channel interleaving buck.

The transfer function has the same double pole frequency and the same spikes as the four-channel interleaving buck transfer function shown in Fig. 2.13. This verifies the validity of the equivalent model of the interleaving buck converter shown in Fig. 2.14.

2.3 Summary

This chapter uses SIMPLIS to verify the small-signal model of the multi-channel interleaving buck based on switching model simulation. The small-signal model of an n-channel interleaving buck can be simplified as a single buck converter. The equivalent inductance in the simplified model is 1/n of the inductance in each channel. The equivalent switching frequency of the simplified model is n times the switching frequency in each channel. Using this analogy, the small-signal analysis of the interleaving buck is no different from a single buck.

Chapter 3

VRM Critical Inductance

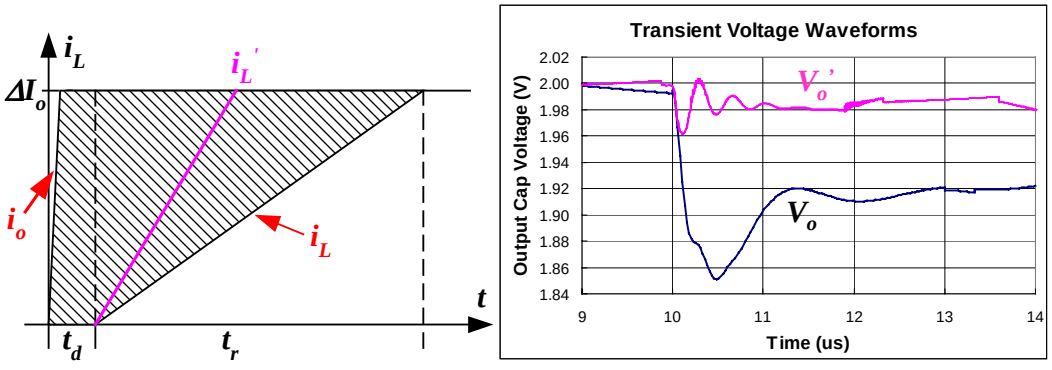
The voltage drops in the VRM output capacitor occur due to the unbalanced charges between the current flowing into the capacitor and that flowing out. Increasing the VRM output inductor current slew rate reduces the unbalanced charges so that the VRM transient response can be improved. The VRM output inductor current slew rate can be improved by reducing output inductance. However, small output inductance generates large current ripple, which results in inferior efficiency. In this chapter, the effects of the feedback control and output inductance on the VRM inductor current slew rate are analyzed. The critical inductance is defined, which gives the largest VRM output inductance value without compromising the inductor current slew rate. The critical inductance is a function of the feedback control bandwidth, the transient current magnitude and the VRM steady-state operating point. For optimal design of the VRM, the output inductance should be close to this critical inductance.

3.1 Introduction

As shown by the analysis in the previous chapter, the transient voltage drops on the VRM output occur because the VRM output capacitors need to provide current during the transient responses. Because of the different time constants in the different resonant loops, the current demand of the VRM has a much higher slew rate than that of the VRM inductor current. The difference between the two

currents determines the charges that need to be provided by the VRM output capacitors. If the unbalanced charges can be reduced, the VRM transient voltage spikes can also be reduced for the same VRM output capacitors. The unbalanced charges can be divided into two parts: those related to the delay time t_d, and those related to the rise time t_r. The switching action delay is determined by the circuit operation and will not be discussed here. In this chapter, the discussions focus on the charges corresponding to the rise time, which appear as the triangle part in Fig. 3.1(a) of the unbalanced charges. This part is affected by the output inductance design.

The triangle part in Fig. 3.1(a) of the unbalanced charges is determined by the inductor current slew rate and the magnitude of the current step. The current step magnitude is determined by the applications, which cannot be changed. The only way to reduce the unbalanced charges is to increase the current slew rate flowing into the VRM output capacitors so that the transient voltage spike on the capacitors can be reduced. This can be verified by simulation. As shown in Fig. 3.1, when the VRM inductor current slew rate increases from I_L to I_L', the VRM transient output voltage spikes can be much reduced from V_o to V_o'.



(a) (b)

Fig. 3.1. Effect of inductor current slew rate on VRM output transient voltages: (a) two different inductor current slew rates; and (b) different corresponding transient voltage waveforms.

In conventional VRMs, a single synchronous buck is used. Due to the steady-state ripple requirements, large inductances must be used. The duty cycle becomes saturated during transient responses. The inductor current slew rate is limited by the large output inductance.

The output current ripple reduction effects in the multi-channel interleaving buck VRMs allow the use of very small inductances in the VRM to improve transient responses. This advantage of the multi-channel interleaving VRM makes it the common practice in VRM industry. However, interleaving cannot reduce the current ripples in the channels. Because of the small inductance, each channel has large current ripples, which cause extra conduction and switching losses and reduce the converter efficiency. The small inductances in multi-channel interleaving VRMs improve the transient responses, but at the expense of efficiency.

In summary, from the efficiency standpoint, large inductances are preferred because larger inductances give smaller current ripples. From the standpoint of transient response, however, small inductance is required. The steady-state and dynamic performances of VRMs have contradictory requirements for inductance. How to select an appropriate inductance for VRMs has been an unanswered question for a long time.

This chapter tries to answer this question based on the analysis of the relationship between the inductance and the VRM transient responses. The discussions begin with the small-signal model analysis.

3.2 Average Current Transfer Function

As discussed in Chapter 2, for small signal analysis, the multi-channel interleaving buck converter can be simplified as a single buck converter. For the

small-signal analysis in this chapter, only a single buck converter is discussed. It is important to note that all the discussions are also valid for the corresponding multi-channel interleaving buck converters.

From the viewpoint of control system, the transient unbalanced charges shown in Fig. 3.1(a) are actually a function of how well the inductor current i_L can follow the changes of load current i_o, as shown in Fig. 3.2.

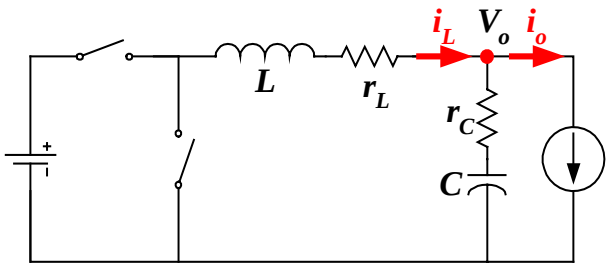


Fig. 3.2. How well the inductor current can follow the load current determines the transient unbalanced charges.

To describe the ability of the inductor current to follow the load current, the average current transfer function is defined as follows:

$$G_{ii}(s) = \frac{\tilde{i}_L(s)}{\tilde{i}_o(s)}, \tag{3.1}$$

where $\tilde{i}_L(s)$ and $\tilde{i}_o(s)$ are the perturbations added to the inductor current i_L and load current i_o, respectively. The transfer function can be easily derived from the circuit shown in Fig. 3.2, as follows:

$$G_{ii}(s) = \frac{\tilde{i}_L(s)}{\tilde{i}_o(s)} = \frac{s \cdot r_C \cdot C + 1}{s^2 \cdot L \cdot C + s \cdot (r_C + r_L) \cdot C + 1}. \tag{3.2}$$

This transfer function is determined only by the passive component parameters; the duty cycle, load current and input voltage do not affect it. If linear

parameters are assumed, (3.2) is also valid for the large-signal perturbations as long as the duty cycle is not saturated. This linearity is valid for the buck converter, but may not be true for other topologies.

The bode plot of the current transfer function $G_{ii}(s)$ is shown in Fig. 3.3.

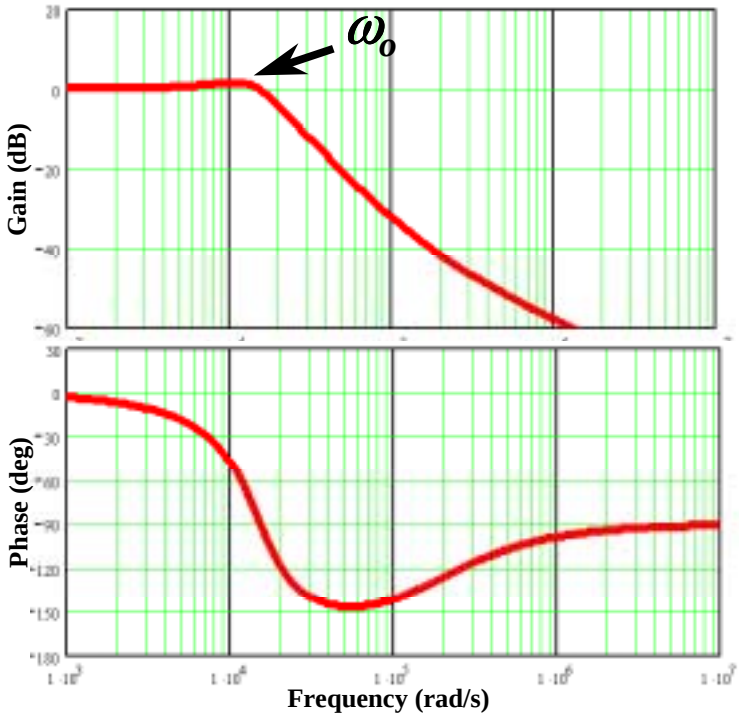


Fig. 3.3. Open-loop current transfer function $G_{ii}(s)$.

The corner frequency in the plot, ω_o, represents the double poles of the power stage. For the frequencies below the corner frequency, the transfer function is close to one. This means that if there is a low-frequency perturbation of the load current, the inductor average current can follow it closely. The mismatch between the load current and the inductor current would be very small, as would be the unbalanced charges. Very small voltage spikes are expected at the VRM output capacitors.

However, as discussed previously, the load current slew rate is much faster than that of the VRM inductor. From this point, the load current transition can be approximated as a step change to the system. The transient response of the inductor current can be considered as the step response of the current transfer function $G_{ii}(s)$. The normalized step response waveform of the open-loop current transfer function in time domain is shown in Fig. 3.4.

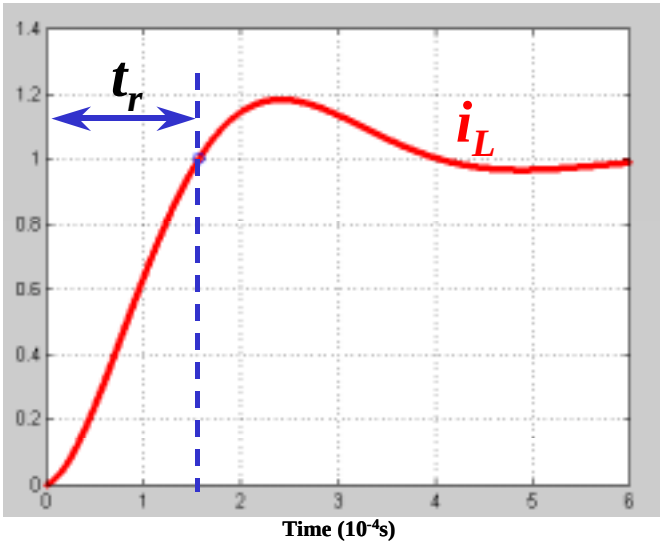


Fig. 3.4. Step response of open-loop current transfer function.

As shown in (3.2), the current transfer function has a pair of power stage double poles and an output capacitor ESR zero. The VRM output capacitors require very low ESR in order to minimize the transient voltage spikes. The ESR zero is usually at much higher frequencies than the power stage double poles. The dynamic performances of the current transfer function are basically determined by the power stage double poles. The simulation waveform in Fig. 3.4 verifies this characteristic.

The waveform, which represents the average inductor current, is close to the step response of a typical under-damping second-order system. The rise time t_r (defined in Fig. 3.4) describes the mismatch between the inductor current and the

load current. The definition of the rise time t_r is consistent with the definition given in Fig. 3.1(a). Of course, the current slew rate is not constant within the rise time. For simplicity, the average inductor current slew rate during the transient response can be approximated as follows:

$$\left.\frac{di}{dt}\right|_{avg} = \frac{\Delta I_o}{t_r}, \tag{3.3}$$

where ΔI_o is the load step current magnitude. The rise time t_r also describes the average inductor current slew rate. Therefore, increasing the inductor current slew rate, which has been our target, accomplishes the dual purpose of reducing the rise time t_r as well.

Feedback control is used in VRMs to regulate output voltages. The following discussion attempts to identify how the feedback control affects both the rise time and the transient response of the VRM. In order to do so, the closed-loop current transfer function must be derived. For a buck converter with feedback control, the small-signal model transfer function block diagram is shown in Fig. 3.5.

The closed-loop current transfer function can be derived from the block diagram. This dissertation considers only the cases in which voltage loop feedback controls are used. With voltage feedback control, the closed-loop current transfer function is as follows:

$$G_{iic}(s) = G_{ii}(s) - G_{di}(s) \cdot G_c(s) \cdot \frac{Z_O(s)}{1+T(s)}, \tag{3.4}$$

where $G_{di}(s)$ is the duty-cycle-to-inductor-current transfer function, $G_c(s)$ is the transfer function of the compensator, $Z_o(s)$ is the converter output impedance, and $T(s)$ is the loop gain. The loop gain is described as follows:

$$T(s) = K \cdot G_{dv}(s) \cdot G_c(s), \tag{3.5}$$

where $G_{dv}(s)$ is the duty-cycle-to-output-voltage transfer function, and K is the gain of the compensator, as shown in Fig. 3.5.

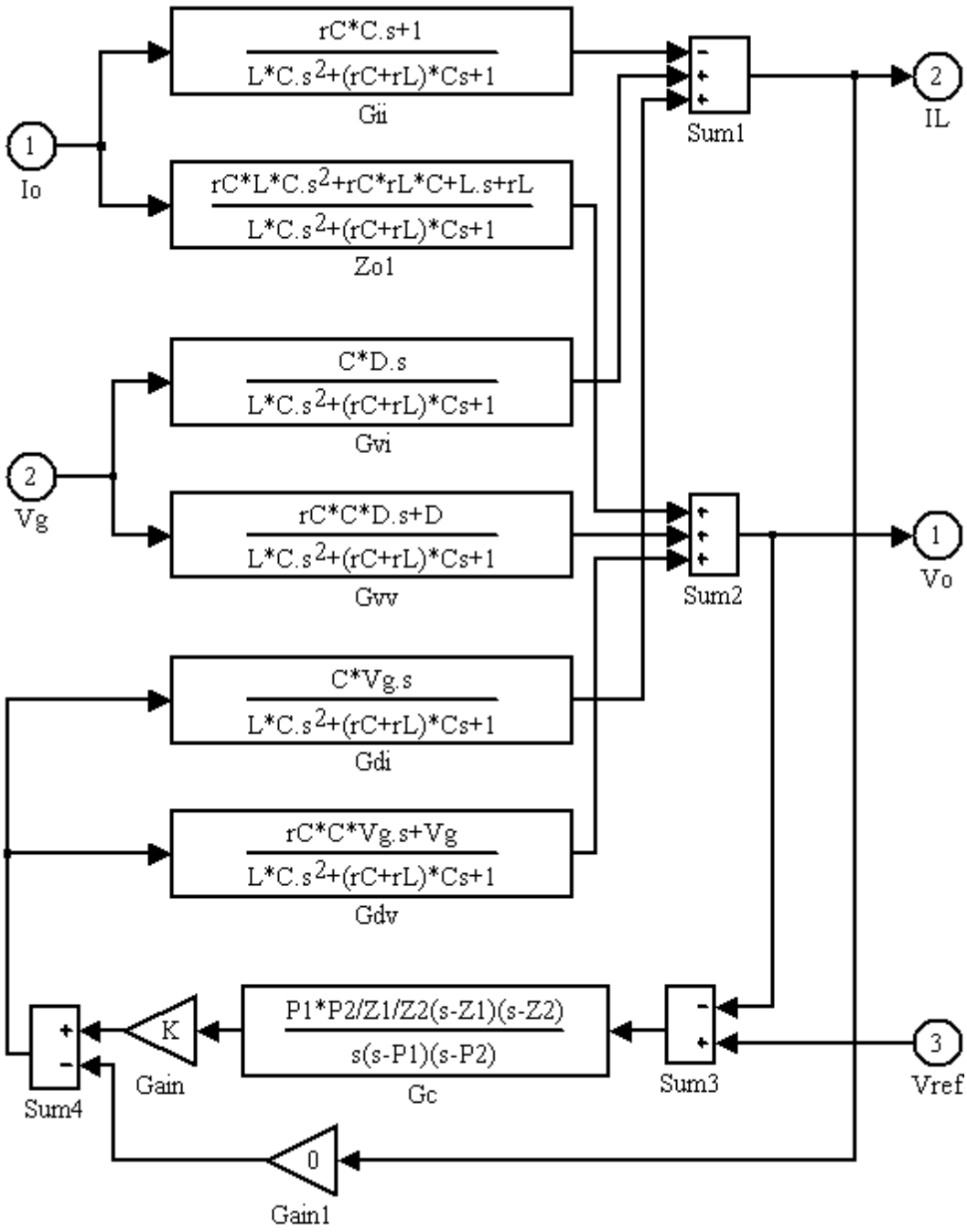


Fig. 3.5. Block diagram of buck converter.

The transfer functions involved in the closed-loop current transfer function $G_{iic}(s)$ are K, $G_c(s)$, $Z_o(s)$, $G_{ii}(s)$, $G_{di}(s)$ and $G_{dv}(s)$. K and $G_c(s)$ represent the compensator, which is linear. As illustrated in Fig. 3.5, $Z_o(s)$ and $G_{ii}(s)$ are determined only by the passive component parameters. $G_{di}(s)$ and $G_{dv}(s)$ include only the input voltage and the passive parameters. In the cases in which input voltages are fixed, the cases on which this work focuses, $G_{di}(s)$ and $G_{dv}(s)$ are also linear. During load transient responses, the duty cycle changes. Fortunately, the duty cycle change does not affect the closed-loop current transfer function $G_{iic}(s)$. In load transient responses, as long as the duty cycle is not saturated, the small-signal model transfer function is also valid for large signal analysis. Thus, $G_{iic}(s)$ can be used to accurately analyze the large-signal load transient responses. This conclusion is valid for buck converters, and may not apply to other topologies.

For a certain feedback control loop design, the open-loop and closed-loop current transfer functions, $G_{ii}(s)$ and $G_{iic}(s)$, and the loop gain $T(s)$ are shown in Fig. 3.6.

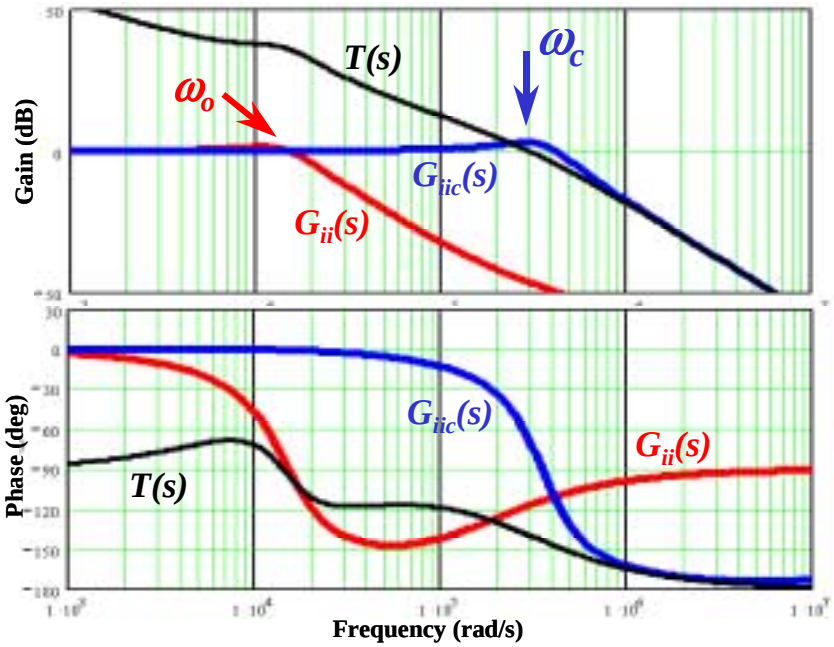


Fig. 3.6. Transfer functions: $G_{ii}(s)$, $G_{iic}(s)$ and $T(s)$.

As shown in Fig. 3.6, the closed-loop current transfer function has the same shape as its open-loop counterpart unless the corner frequency moves to ω_c, which is the feedback control bandwidth. The control bandwidth ω_c is much higher than the power stage double poles' frequency ω_o.

In order to show the effects of the feedback control on the closed-loop current transfer function, the second term in (3.4) is defined as $G_{it}(s)$, as shown in (3.6). The closed-loop current transfer function is the sum of the open-loop current transfer function and $G_{it}(s)$. The bode plots of $G_{ii}(s)$ and $G_{it}(s)$ are shown in Fig. 3.7. The feedback control effect $G_{it}(s)$ looks similar to a band-pass filter. It provides a unit transfer function between the power stage double poles' frequency and the control bandwidth, which expands the corner frequency of the current transfer function from ω_o to ω_c.

$$G_{it}(s) = -G_{di}(s) \cdot G_c(s) \cdot \frac{Z_O(s)}{1+T(s)}. \tag{3.6}$$

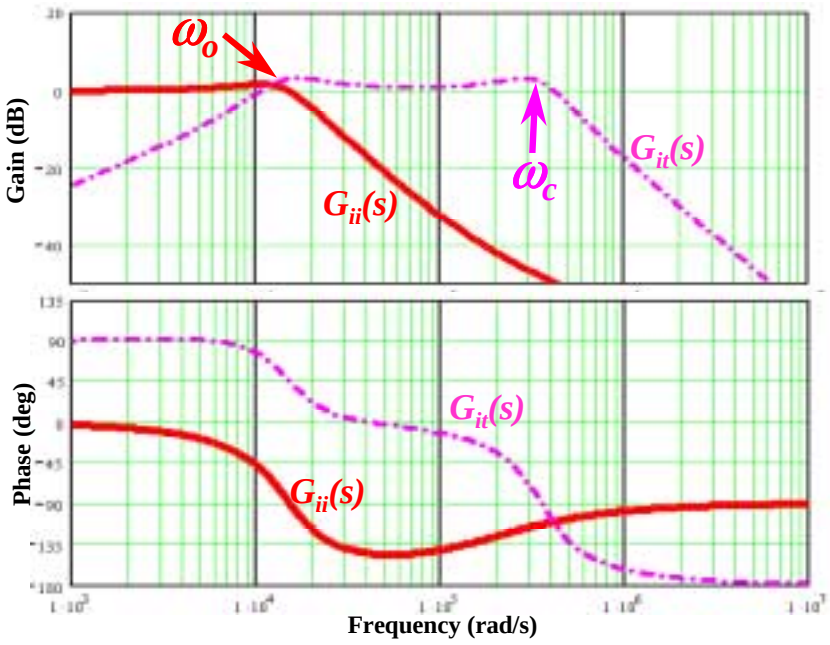


Fig. 3.7 Transfer functions: $G_{ii}(s)$ and $G_{it}(s)$.

The bode plots shown in Fig. 3.6 also show that the power stage double poles do not appear in the closed-loop current transfer function. Despite the complexity of (3.4), the closed-loop current transfer function $G_{iic}(s)$ is still very close to a second-order system as illustrated by its bode plot shown in Fig. 3.6. It seems that the corner frequency is the only difference between the open-loop and closed-loop current transfer functions.

The zeros and poles of the closed-loop current transfer function are shown in Fig. 3.8.

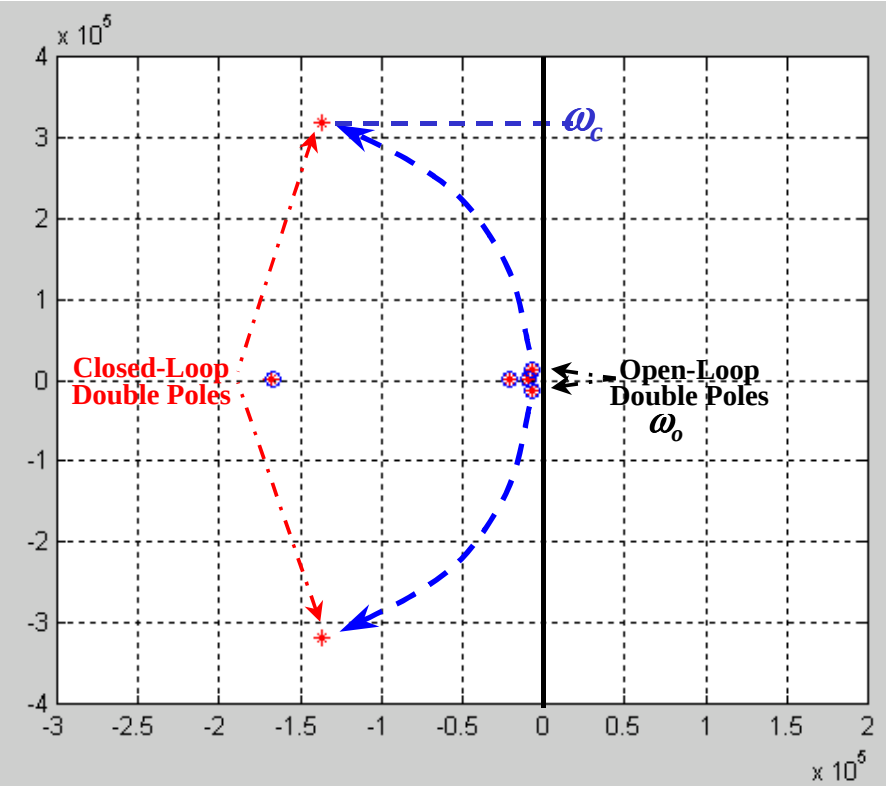


Fig. 3.8. Poles and zeros of closed-loop current transfer function.

The poles are represented as '*' in the figure. The zeros are represented as 'o'. The feedback control generates both a pair of double zeros to cancel the power stage double poles and a pair of double poles at the control bandwidth. In other words, the feedback control moves the open-loop double poles from the power

stage corner frequency to the control bandwidth. The power stage double poles do not have much effect on the closed-loop current transfer function. Within the switching frequency range, the closed-loop current transfer function only has a pair of double poles at the control bandwidth. The closed-loop current transfer function is a second-order system. The double poles determine the time domain performances of the transfer function.

The open-loop and closed-loop current transfer functions are both second-order systems. The difference lies is the frequencies of their double poles, which results in different time domain performances of the two transfer functions. The time domain step responses of the two transfer functions are compared in Fig. 3.9.

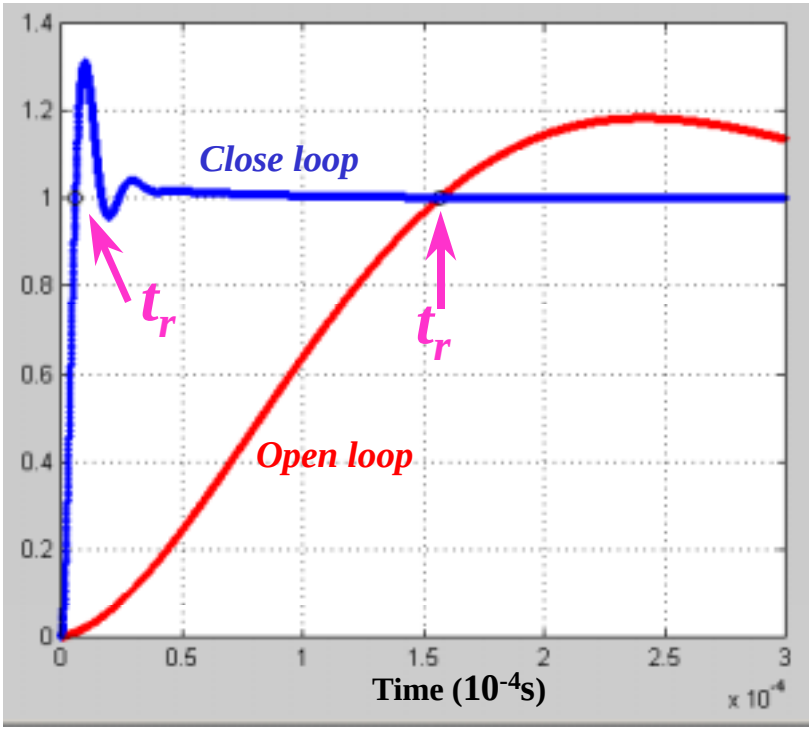


Fig. 3.9. Step responses of open- and closed-loop current transfer functions.

The rise time of the closed-loop step response is much smaller than that of the open-loop step response. The unbalanced charge area is greatly reduced. Much faster transient response can be expected with feedback control. Our interest is to

quantify this improvement. What is the inductor current slew rate? Or, what is the inductor current rise time?

The double pole frequency is the resonant frequency of the second order system. For a non-damped second-order system, the rise time is one-fourth of its resonant cycle. The relationship between rise time and control bandwidth can be approximated as follows:

$$t_r = \frac{T_c}{4} = \frac{\pi/2}{\omega_c}. \tag{3.7}$$

For systems with light damping, the rise time is close to that given in (3.7). But how close is the approximation given by this formula? To answer this question, three buck converters with different output filters are designed with different control bandwidths. Their rise time are compared in Fig. 3.10.

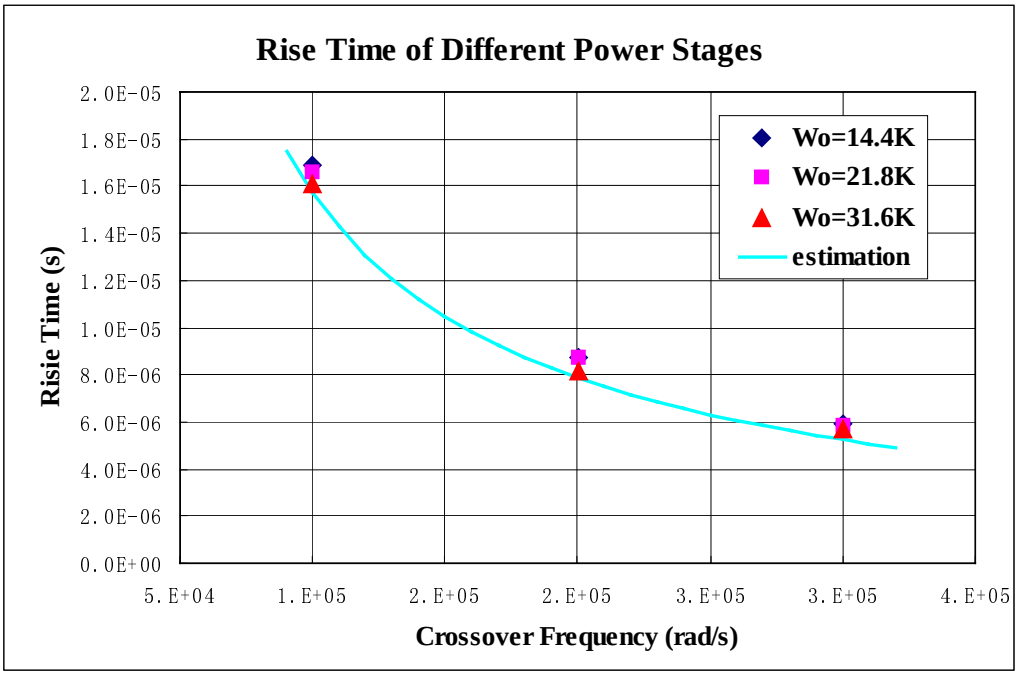


Fig. 3.10. Closed-loop inductor current rise time for different power stages.

The power stage double poles' frequencies of the three buck converters are 14.4K(rad/s), 21.8K(rad/s) and 31.6K(rad/s). For each power stage, the control bandwidths are designed to be 1000K(rad/s), 2000K(rad/s) and 3000K(rad/s). There are nine cases. The measurement results of the rise time from simulation of these nine cases are the data points in Fig. 3.10. The curve in Fig. 3.10 is drawn based on (3.7). All the measured rise times of the different power stages at different feedback bandwidths follow the estimation curve very closely.

The discussions in the Appendix also show that within certain reasonable ranges of control phase margin, the control phase margin does not affect the rise time. The only factor that determines the inductor current rise time during transient responses is the feedback control bandwidth, as shown in (3.7). Formula (3.7) is true for different power stages. Substituting (3.7) into (3.3), the inductor current slew rate can be easily derived, as follows:

$$\left.\frac{di}{dt}\right|_{avg} = \frac{\Delta I_o \cdot \omega_c}{\pi / 2}. \tag{3.8}$$

3.3 Concept of Critical Inductance

The preceding discussions of the inductor current slew rate are based on the average model. The average model gives accurate description of a physical buck converter as long as the duty cycle is not saturated.

The inductor current slew rate can also be derived from the circuit operation. For the buck converter shown in Fig. 3.11, the steady-state duty cycle is *D*. The voltages of the both terminals of the inductor are V_{in}*D. No net average voltage is applied to the inductor. The inductor current is constant in the average sense. During transient responses, the feedback control generates duty cycle increase

ΔD. The duty cycle increase generates net voltage $V_{in}*\Delta D$ on the inductor, which causes the inductor current to increase. The average inductor current slew rate can be easily derived as follows:

$$\left.\frac{di}{dt}\right|_{avg} = \frac{V_{in} \cdot \Delta D}{L}. \tag{3.9}$$

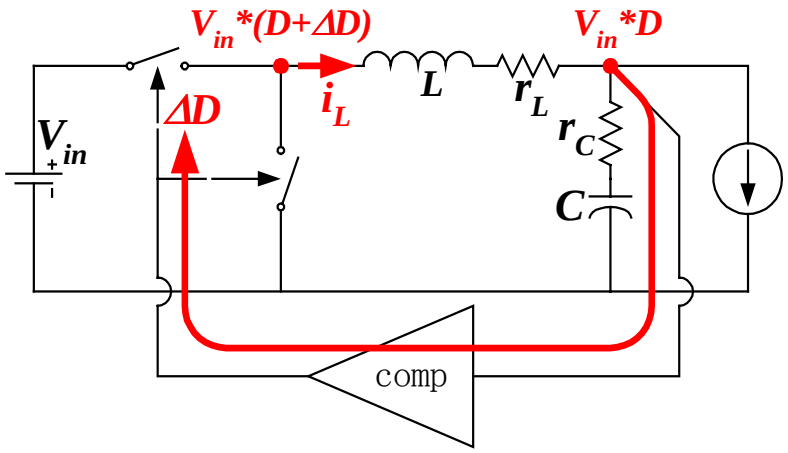


Fig. 3.11. Volt-seconds on inductor during a transient response.

Formulas (3.8) and (3.9) derive the inductor current slew rate from two different viewpoints: the former is valid as long as the duty cycle is not saturated, while the latter is always true. In the ranges for which the duty cycle is not saturated, the two formulas should be equal.

By equalizing (3.8) and (3.9), the transient duty cycle increase can be described as follows:

$$\Delta D = \frac{\Delta I_o \cdot \omega_c}{(\pi/2) \cdot V_{in}} \cdot L. \tag{3.10}$$

In order to increase the VRM response speed, the control loop bandwidth ω_c should be designed to be as high as possible. The bandwidth is limited by the

switching frequency of the converter. For different power stages operating at the same switching frequency, we can assume that the control bandwidths are the same. For those with the same input voltage and load current step, (3.10) tells that the transient duty cycle increase is proportional to the inductance. This is not an obvious concept; the following paragraph uses diagrams to explain.

As shown in Fig 2.11, the transient duty cycle increase ΔD is determined by the voltage variation at the VRM output capacitors and the feedback compensator. Two power stages with the same output capacitors and different inductances are considered. The two power stages are designed to have the same control bandwidth ω_c. Assume that the duty cycle is not saturated during the transient response. The inductor average current slew rates, which are determined by the control bandwidth, are the same in both power stages. Because the output capacitors of the two power stages are the same, the transient voltage variations at output capacitors should also be the same.

The open-loop transfer functions of the two power stages are shown in Fig. 3.12. The power stage with a larger inductance has a low corner frequency. Beyond the corner frequency, the gain is lower than it is in the stage with the smaller inductance. However, the two power stages are designed to have the same control bandwidth ω_c. At frequency ω_c, the power stage with the larger inductance requires a larger gain from the compensator to achieve the same loop gain $T(s)$, as shown in Fig. 3.12. Because the transient voltage variations at the output capacitors are the same for both power stages, the one with the larger compensator gain results in a larger transient duty cycle increase ΔD. This example intuitively explains (3.10).

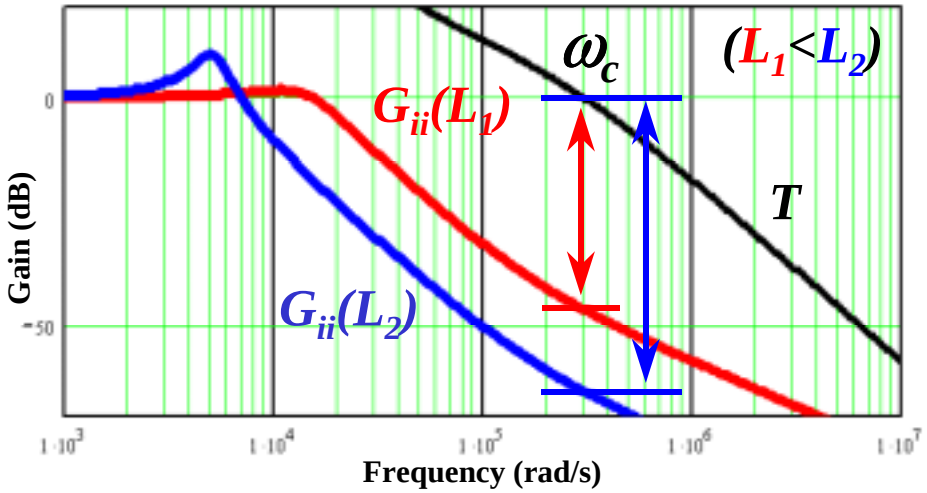


Fig. 3.12. Larger inductance requires higher compensator gain to achieve the same control bandwidth.

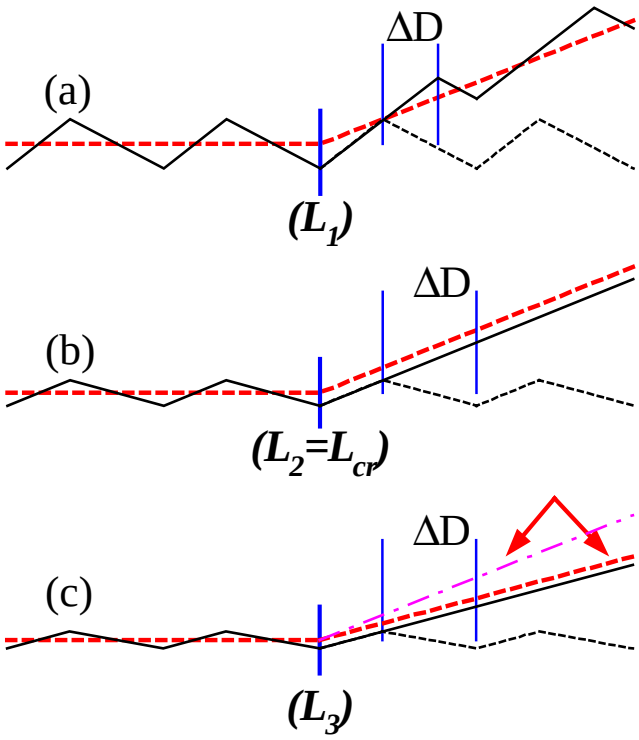
Based on the previous analysis, a discussion of the effects of inductance on transient responses now begins. The concept is explained using the three cases shown in Fig. 3.13. For the three cases, the control bandwidths ω_c are the same, while the inductances are different. There exists $L_1<L_2<L_3$.

The solid lines are the inductor current waveforms. The dashed lines are the average inductor current waveforms. The smaller inductance corresponds to the smaller steady-state current ripples. According to (3.10), the small inductance in case (a) corresponds to a small duty cycle increase ΔD during the transient response. The duty cycle is not saturated in this case. The average current slew rate is determined by the control bandwidth (3.8).

In case (b), the larger inductance results in larger ΔD. In this case, the duty cycle is at the boundary of saturation. The average current slew rate is also determined by the control bandwidth (3.8). Because the control bandwidths are the same for all the three cases, the average current slew rates in cases (a) and (b) are the same. Although the switching inductor current waveforms are different in these two cases, the average inductor current waveforms (the dashed lines) are the

same. Same transient voltage spikes are expected at the VRM output if the same output capacitors are used.

For case (c), the inductance is even larger. The compensator gives a larger error signal than in case (b). However, the duty cycle applied to the power stage is the same as that in case (b). In both cases, the duty cycle is saturated during the transient responses. When the duty cycle becomes saturated, (3.8) is no longer valid. According to (3.9), case (c) has a lower current slew rate than that of case (b). The dot-dashed line in case (c) is the average current of cases (a) and (b). It has higher slew rate than that of the dashed line, which is the average inductor current in case (c).



(Constant ω_c, $L_1<L_2<L_3$)

Fig. 3.13. Effects of inductance on inductor current slew rate: (a) & (b), same current slew rate, determined by ω_c; (c) lower current slew rate, determined by (V_{in}*$\Delta D/L$)

The important concept presented in Fig. 3.13 is that from case (a) to (b), although the inductance increases, the average current slew rates are the same. The transient voltage spikes are expected to be the same. The specific inductance in case (b) is the largest inductance that gives the same fast transient responses; this specific inductance is defined as the critical inductance. For a converter designed at the critical inductance, the duty cycle would barely become saturated during the transient responses.

The critical inductance can be calculated by letting ΔD in (3.10) equal ΔD_{max}, as follows:

$$L_{ct} = \frac{(\pi/2)\cdot V_{in}}{\Delta I_o \cdot \omega_c} \cdot \Delta D_{\max}, \tag{3.11}$$

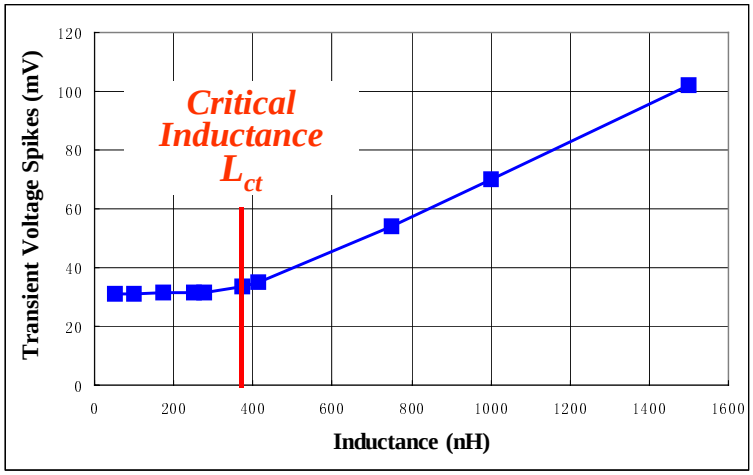
where ΔD_{max} is the maximum duty cycle increase during the transient response. For step-up transient responses, there exists

$$\Delta D_{\max} = D_{\max} - D, \tag{3.12}$$

where D_{max} is the maximum duty cycle. When the duty cycle reaches D_{max}, the circuit is considered saturated.

The critical inductance concept is also explained in Fig. 3.14. The curve in the figure is based on the average model simulation of step-up transient responses for a 5V-input, 2V-output buck VRM. D_{max}=1 is assumed. For all the data points in the figure, the control bandwidths and the converter output capacitors are kept the same. The compensators for the different inductances are different in order to keep the same bandwidth. When the inductance is smaller than the critical inductance, the duty cycle does not become saturated during transient responses. The transient responses are the same, and are determined by the control bandwidth. In this range, the inductance does not affect the transient response.

When the inductance is larger than the critical inductance, the duty cycle becomes saturated during transient responses. The inductor current slew rate decreases as the inductance increases. In this range, the transient voltage spikes increase linearly as the inductances increase.



(Constant ω_c)

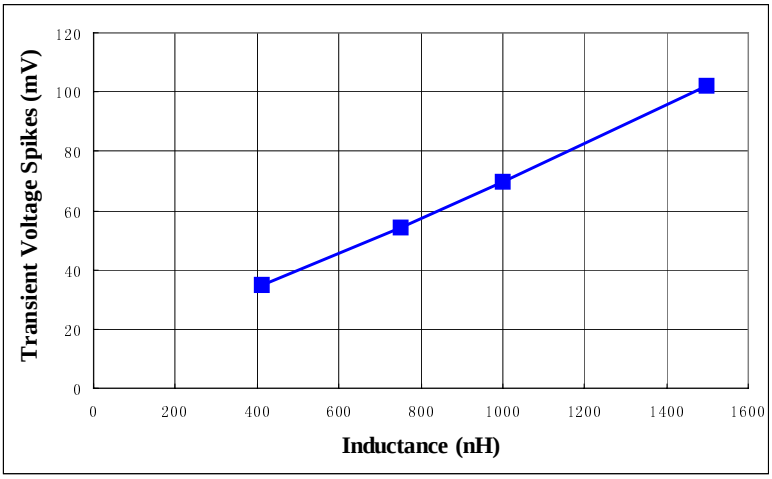
Fig. 3.14. Inductances smaller than L_{ct} give the same transient responses; transient voltage spikes increase linearly for inductances larger than L_{ct}.

The curve shown in Fig. 3.14 is different from the conventional understanding. Large inductances are used in conventional designs. The duty cycle always becomes saturated during the transient responses. The inductor current slew rates during transient responses are determined as follows:

$$\frac{di}{dt} = \frac{V_{in} \cdot \Delta D_{\max}}{L}. \tag{3.13}$$

The inductor current slew rates increase as the inductances decrease. Reducing the inductance always improves the transient responses, as shown in Fig. 3.15. However, this is not always the case. As discussed previously, when small inductances are used, the duty cycle is not saturated during transient responses. In these cases, (3.13) is no longer valid. In fact, the curve in Fig. 3.15

is only part of the curve in Fig. 3.14. Fig. 3.15 corresponds to the cases in which the inductances are larger than the critical inductance.



(Constant ΔD)

Fig. 3.15. Conventional understanding: transient voltage spikes decrease as the inductances decrease.

3.4 Discussions of Critical Inductance

The transient voltage spikes shown in Fig. 3.14 are related only to the unbalanced charges in the triangle area shown in Fig. 3.1(a). Voltage variations related to the delays and the ESR voltage drops are close to constant for different inductances. They add a constant offset in the total transient voltage spikes. If these effects are taken into account, the curve in Fig. 3.14 will be higher in the graph. But its shape and the critical inductance will remain the same. Different output capacitors have similar effects on the curve, moving it higher or lower in the graph but not changing either the shape of the curve or the critical inductance. This independence of the critical inductance greatly facilitates the power stage output filter design.

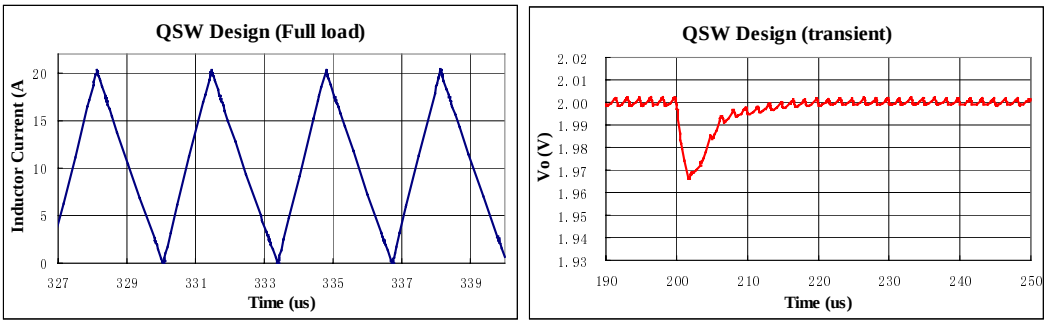
Conventional VRMs are designed in continuous current mode (CCM), in which large inductances are used. The duty cycle becomes saturated during transient responses. The inductor current slew rate is limited by the inductance. Large output capacitance must be used to reduce transient voltage spikes. For the QSW design proposed by VPEC/CPES in 1997, very small inductances are used. The duty cycle is not saturated during transient responses. A much smaller output capacitance is required because of the fast inductor current slew rate. However, small inductances result in large current ripples in the MOSFET, which cause large conduction losses and turn-off losses in the MOSFET.

The critical inductance is between the inductances based on QSW and CCM designs. Critical inductance design gives the same transient response as QSW design, but the current ripples of the former can be much reduced.

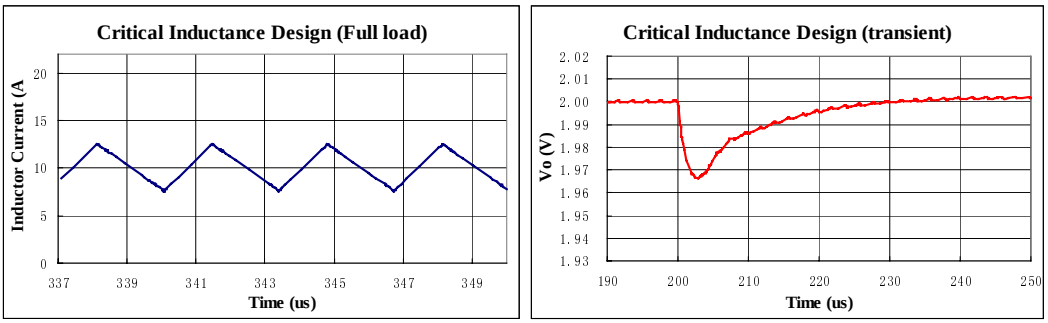
To illustrate the differences among the three designs, the simulation results of the CCM, QSW and critical inductance designs are compared in Fig. 3.16. Two-channel interleaving is used for all three designs. The input and output voltages are 5V and 2V, respectively. The switching frequency and control bandwidth are 300kHz and 100kHz, respectively. The total step-up load transient is 20A.

For n-channel interleaving buck VRMs, L_{ct} and ΔI_o in (3.11) are the critical inductance and load step current magnitude in each channel. ΔI_o is 1/n of the total load step current magnitude.

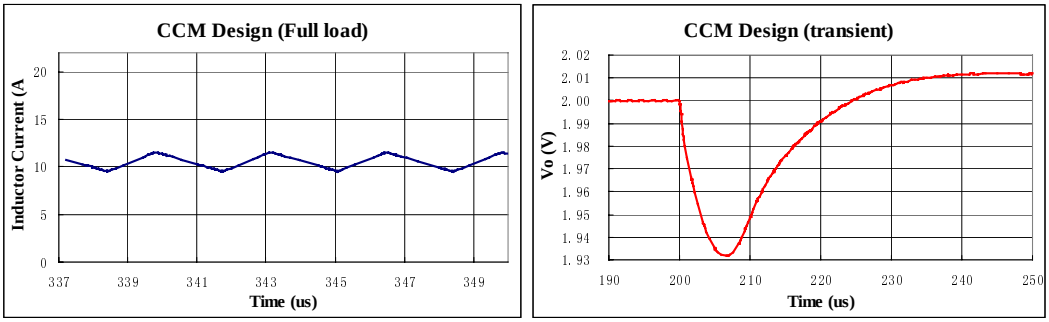
The inductances for the three designs are $L_{QSW}=200nH$, $L_{ct}=827nH$ and $L_{CCM}=2000nH$. From the steady-state inductor current waveforms, the peak-to-peak currents in each channel are 20A for QSW design, 4.8A for critical inductance design and 2A for CCM design. The QSW design has much larger root-mean-square (RMS) current than the other two. The lowest efficiency is expected for the QSW design if the other components in the circuits are kept the same.



(a)



(b)



(c)

Fig. 3.16. Steady-state inductor current and transient output voltage waveforms of different inductance designs:

(a) QSW design, L=200nH, ΔVo=33mV; (b) critical inductance design, L=827nH, ΔVo=33mV; and (c) CCM design, L=2000nH, ΔVo=68mV.

The transient voltage spikes at the output capacitors are 33mV for both the QSW and critical inductance designs, and 68mV for the CCM design. Compared to the QSW design, the critical inductance design is expected to have a higher efficiency but the same transient responses. Compared to the CCM design, the

critical inductance design gives a much faster transient response. The critical inductance design offers a reasonable tradeoff between the steady-state efficiency and transient responses.

The preceding discussions of critical inductance are based only on the load step-up transient responses. The load step-down transient response also needs to be considered; the average model discussions are valid for these as well. Formulas (3.7) and (3.8) are still valid for step-down transients. The feedback control bandwidths ω_c for step-down transients are the same as those for step-up transients. During step-down transients, the duty cycle decreases. The critical inductance for a step-down transient response is defined for the case in which the duty cycle is close to the minimum duty cycle D_{min}. The step-down critical inductance can still be obtained from (3.11). However, ΔD_{max} in (3.12) needs to be rewritten as follows:

$$\Delta D_{\max} = D - D_{\min} . \tag{3.14}$$

For the step-down transients, a curve similar to that shown in Fig. 3.14 can be obtained, as shown in Fig. 3.17.

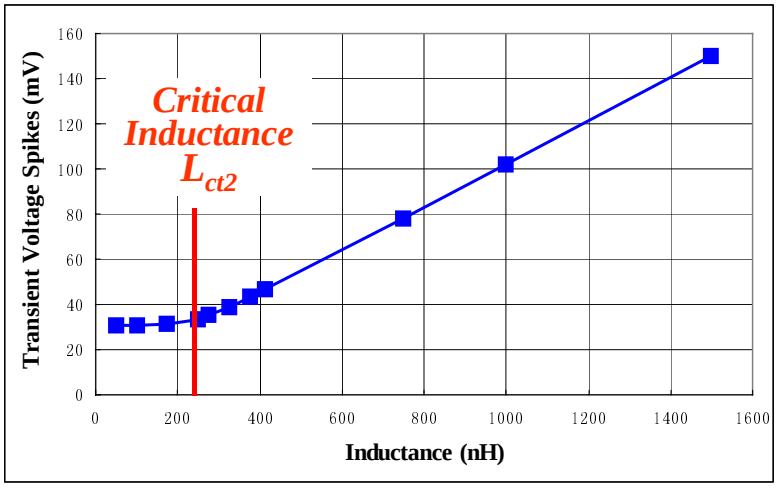


Fig. 3.17. Inductance effects on step-down transient voltage spikes.

Because ΔD_{max} may not be the same for step-up and step-down transient responses, the critical inductance for the two transient responses can be different. The step-up and step-down critical inductances are defined as L_{ct1} and L_{ct2}, respectively.

Considering the curves in Fig. 3.14 and 3.17, the level of the horizontal lines in the two figures should be the same for the same converter, because in these ranges, the transient voltage spikes are determined by the control bandwidth ω_c, which is the same for both the step-up and step-down transient responses.

The step-up and step-down transient voltage curves are shown for comparison in Fig. 3.18.

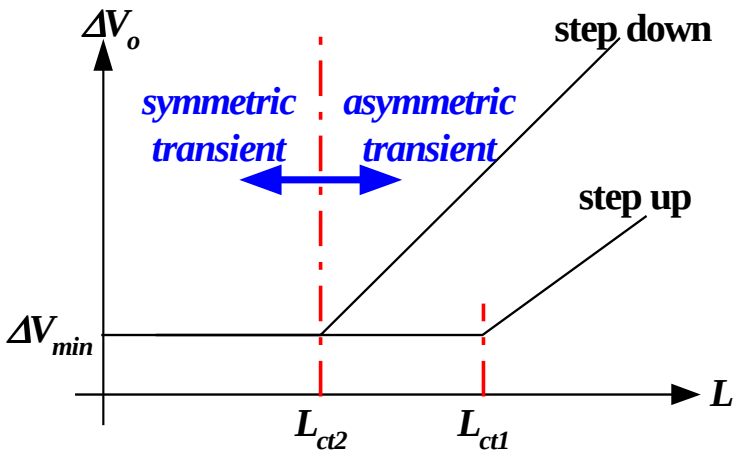


Fig. 3.18. Inductances smaller than L_{ctm} give symmetric step-up and step-down transient responses.

When the inductance is smaller than L_{ctm}, as defined in (3.15), the duty cycle is not saturated in either the step-up or step-down transient response. The transient response is determined by the control bandwidth. The converter has symmetric transient voltage spikes for both step-up and step-down transient responses.

$$L_{ctm} = \min(L_{ct1}, L_{ct2}). \tag{3.15}$$

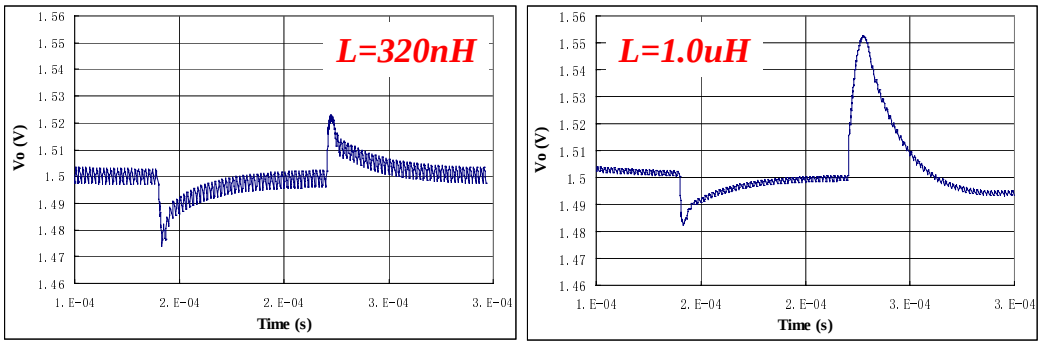
When the inductance is larger than L_{ctm}, the step-up and step-down transient responses are no longer symmetric. Both the symmetric and the asymmetric transient responses can happen in different VRMs; the occurrence depends on the inductance design.

This, again, is different from conventional understanding. In conventional VRM designs, the duty cycle becomes saturated during transient responses. For the cases in which the steady-state duty cycle is not 0.5, the average voltages applied to the inductor are different for step-up and step-down transient responses, which results in different inductor current slew rates, and thus asymmetric step-up and step-down transient responses. However, this scenario is not true when the duty cycle is not saturated during transient responses. The scenario corresponding to the range in which the inductances are large than L_{ct1} is shown in Fig. 3.18.

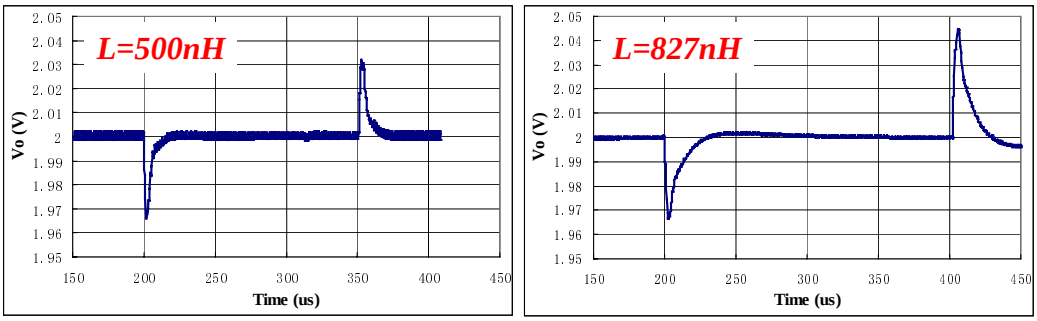
To verify the curves shown in Fig. 3.18, four different simulation results are shown in Fig. 3.19.

For the two VRM transient voltage waveforms in Fig. 3.19(a), the input and output voltages are 12V and 1.5V, respectively. When a small inductance ($L=320nH$) is used, the step-up and step-down transient voltage spikes are the same. However, when a large inductance ($L=1.0\mu H$) is used, the voltage spike in the step-down transient response is much larger than that in the step-up response.

For the two waveforms in Fig. 3.19(b), the input and output voltages are 5V and 2V, respectively. Similar to the cases in Fig. 12.19(a), a small inductance ($L=500nH$) results in symmetric step-up and step-down transient responses, while a large inductance ($L=827nH$) results in asymmetric transient responses. The symmetric or asymmetric step-up and step-down transient responses can occur in VRMs with different input voltages. This occurrence is only a matter of the inductance design position on the curves shown in Fig. 3.18.



(a)



(b)

Fig. 3.19. Symmetric and asymmetric transient responses exist in different input voltages: (a) Vin=12V, Vo=1.5V; and (b) Vin=5V, Vo=2V.

Another observation from the simulation waveforms shown in Fig. 3.19 is that when asymmetric transient responses occur, at least one of the transient voltage spikes is larger than the voltage spikes with symmetric transient responses. This is clear from Fig. 3.18.

Symmetric transient responses are desirable. When the adaptive reference voltage is used, the total output voltage variance is the larger of the step-up and step-down transient voltage spikes. Symmetric transient responses give smaller total output voltage variance. For asymmetric transient responses, the output capacitors are over-designed for one transient response. The output capacitors designed for symmetric transient responses are smaller than those for the asymmetric cases. The critical inductance L_{ctm} is the largest inductance that gives symmetric and fastest transient responses.

Of course, the step-up and step-down critical inductances (L_{ct1} and L_{ct2}) in 5V VRMs are much closer than those in 12V VRMs. Although asymmetric transient responses exist in 5V VRMs, they are less severe than the asymmetry in 12V VRMs.

In order the show the benefit of critical inductance design, the ratio between L_{ctm} and L_{QSW} is compared in Fig. 3.20. L_{QSW} is the inductance based on the QSW buck design, which is determined as follows:

$$L_{QSW} = \frac{V_{in} \cdot D \cdot (1-D)}{2 \cdot I_o \cdot F_s}, \tag{3.16}$$

where F_s and I_o are the switching frequency and full load current, respectively. For n-channel interleaving VRMs, F_s and I_o are the switching frequency and full load current in each channel. I_o is 1/n of the total load current. Formula (3.16) gives the QSW inductance in each channel.

Assuming D_{max}=1 and D_{min}=0, L_{ctm} can be simplified as follows:

$$L_{ctm} = \frac{(\pi/2) \cdot V_{in}}{\Delta I_o \cdot \omega_c} \cdot \min((1-D), D). \tag{3.17}$$

Similar to (3.16), for n-channel interleaving buck VRMs, ΔI_o is 1/n of the total load step current magnitude. Formula (3.17) gives the critical inductance in each channel.

Assuming $\Delta I_o = I_o$, the ratio between L_{ctm} and L_{QSW} can be described as follows:

$$\frac{L_{ctm}}{L_{QSW}} = \frac{\min(D, (1-D))}{2 \cdot D \cdot (1-D)} \cdot \frac{F_s}{F_c}. \tag{3.18}$$

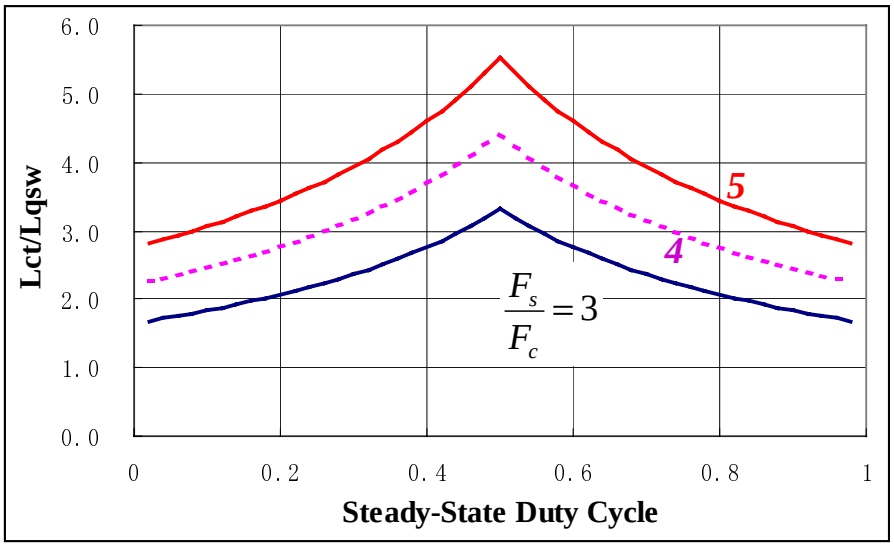


Fig. 3.20. Comparison of critical inductance and QSW inductance.

The critical inductance design has larger inductance than the QSW design. The current ripples can be reduced, and the circuit efficiency can be improved. The transient responses are the same. In this sense, there is no point to design a VRM based on QSW operation.

The following section discusses the factors that impact the transient voltage spike curve. As shown in (3.11), the critical inductance is inversely proportional to the control bandwidth. The effects of the control bandwidth on the transient voltage spike curve are shown in Fig. 3.21. Each curve in the figure corresponds to a constant control bandwidth. As the control bandwidth increases, the critical inductance decreases. The minimum voltage spikes decrease, too. The oblique line stays the same.

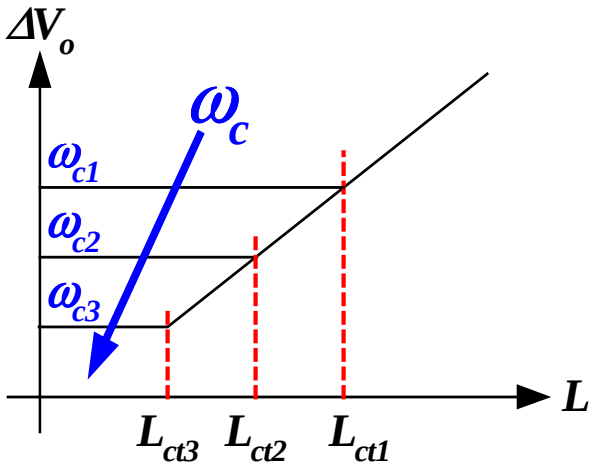


Fig. 3.21. Increasing control bandwidth reduces the critical inductance and improves transient responses.

From Fig. 3.21, in the range in which the inductances are larger than the critical inductance, increasing the control bandwidth cannot improve the transient responses. In conventional VRM designs, the control bandwidth is pushed as high as possible, but the inductance is not decreased. The transient response cannot be improved. However, the combination of increased control bandwidth and decreased inductance can improve the transient responses.

For the inductances smaller than the critical inductance, the unbalanced charges in the triangle area shown in Fig. 3.1(a) can be described as follows:

$$\Delta Q_{tri} = \frac{\Delta I_o \cdot t_r}{2} = \frac{\Delta I_o \cdot \pi}{4 \cdot \omega_c}. \tag{3.19}$$

If only the unbalanced charges in the triangle area are considered, the relationship between the transient voltage drops and the control bandwidth can be described as follows:

$$\Delta v_o = \frac{\Delta Q_{tri}}{C_o} = \frac{\Delta I_o \cdot \pi}{4 \cdot \omega_c \cdot C_o}. \tag{3.20}$$

For the inductances larger than the critical inductance, the current slew rate is shown in (3.13). The unbalanced charges in the triangle area shown in Fig. 3.1(a) can be described as follows:

$$\Delta Q_{tri} = \frac{\Delta I_o \cdot t_r}{2} = \frac{(\Delta I_o)^2 \cdot L}{2 \cdot V_{in} \cdot \Delta D_{\max}}. \tag{3.21}$$

The relationship between the transient voltage drops and the inductance can be described as follows:

$$\Delta v_o = \frac{\Delta Q_{tri}}{C_o} = \frac{(\Delta I_o)^2 \cdot L}{2 \cdot V_{in} \cdot \Delta D_{\max} \cdot C_o}. \tag{3.22}$$

Formulas (3.20) and (3.22) give a quick estimation of the VRM output voltage spikes during transient responses. The curves in Fig. 3.21 can be easily drawn using these two formulas.

The family of curves in Fig. 3.21 can be drawn in another format, as shown in Fig. 3.22.

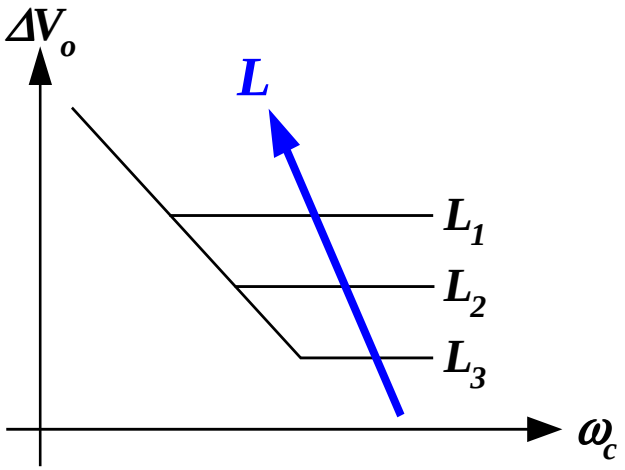


Fig. 3.22. Increasing control bandwidth and reducing inductance improves transient responses.

Each curve in the figure corresponds to a constant inductance. In the oblique line region, the duty cycle is not saturated during transient responses. In this region, higher control bandwidths result in higher inductor current slew rates and smaller transient voltage spikes. In the horizontal line region, the duty cycle saturates during transient responses. The control bandwidth increase cannot improve the transient responses. The transient voltage spikes are determined by the inductances. For smaller inductances, the duty cycle begins to become saturated at a higher bandwidth.

The effects of the load step current magnitude, ΔI_o, on the transient voltage spike are shown in Fig. 3.23. Each curve in the figure corresponds to the same load transition. According to (3.11), the critical inductance decreases as ΔI_o increases. However, the minimum voltage spike increases as ΔI_o increases, because of the increase of the unbalanced charges during transient responses. It is important to note that the slopes of the oblique lines in Fig. 3.23 become steeper as ΔI_o Increases. This can be easily derived and will not be discussed further.

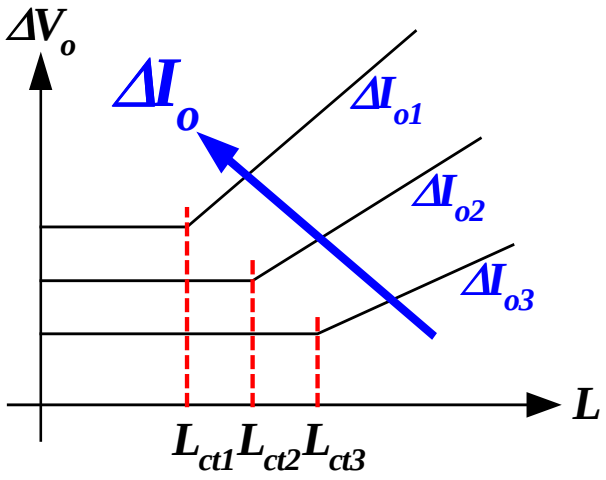


Fig. 3.23. Larger load step current results in smaller critical inductance and larger transient voltage spikes.

3.5 Utilization of Critical Inductance Concept in VRM Design

The preceding sections present the concept of critical inductance and discuss its effects on VRM transient responses. In this section, experimental data are presented to show the extent to which the critical inductance can potentially improve real converters. The critical inductance concept has not yet been adopted in industry designs. This section also compares the critical inductance design with some industry design practices.

As discussed previously, inductance affects converter efficiency. The question is the importance of this effect. In order to make this determination, a synchronous buck converter is built for the efficiency comparison of different inductances. The input and output voltages of the circuit are 5V and 2V, respectively. The switching frequency is 500kHz. Full-load output current is 11A. The switches used are HAT2064Rs from Hitachi. For the QSW design, the inductance is 110nH. For the critical inductance design, the inductance depends on the control bandwidth. The critical inductance is 270nH for F_s/F_c = 3, and 460nH for F_s/F_c = 5. Packed inductors from Vishay are used in the circuit. The inductance value is not continuous. The inductances of 100nH, 240nH, 470nH and 1000nH are selected in the experiments: The first represents the QSW design; the second and third represent the critical inductance designs; and the purpose of the fourth inductance is to show the extent to which increasing inductance can make even greater improvements in efficiencies. The experimental results are shown in Fig. 3.24.

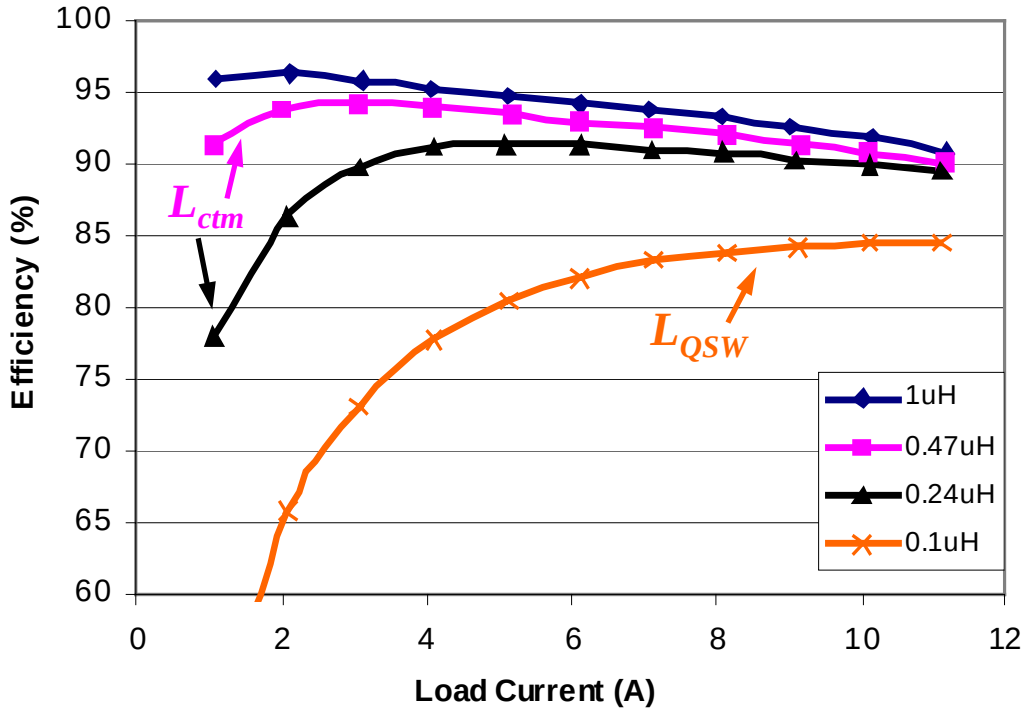


Fig. 3.24. Efficiency comparison of different inductance designs.

The critical inductance designs have much higher efficiency compared to that of the QSW design. Further increase of the inductance does not significantly improve efficiency, but it slows down the transient responses. In this sense, the critical inductance design is a good tradeoff between the steady-state and transient performances of the VRM.

The latest VRM specifications are the VRM 9.0 from Intel: Its output voltage is about 1.6V, and the maximum load step current is about 50A. Because of the low output voltage, there exists $L_{ctm}=L_{ct2}$. The minimum duty cycle is usually zero ($D_{min}=0$). The critical inductance is a function of the channel number and control bandwidth. Based on these data, the critical inductance can be calculated, as shown in the following table.

Table 3.1. Critical inductance designs based on VRM 9.0.

bandwidth \ channel number	2	3	4
20 kHz	800 nH	1.20 μH	1.60 μH
50 kHz	**320 nH**	**480 nH**	**640 nH**
80 kHz	200 nH	300 nH	400 nH
100 kHz	160 nH	240 nH	320 nH

For a given control bandwidth and channel number, Table 3.1 gives the critical inductance design based on VRM 9.0 specifications. In today's industrial VRM designs, the selection of inductance usually does not take into consideration the control bandwidth and channel numbers. In order to compare the industrial designs in terms of critical inductance, the control bandwidth is assumed to be 50kHz (as highlighted in Table 3.1), which is normal in today's VRM products.

The following lists some VRM design examples from industry. In Intersil's HIP6301 design, the inductance for the three-channel interleaving buck is 850nH, which is about 75% larger than the critical inductance. In Analog Devices' ADP3160 and On Semiconductor's CS5332 designs, the inductance for the two-channel interleaving buck is 600nH, which is about twice the critical inductance. In Linear Technology's LTC1629 design, the inductance for the two-channel interleaving buck is 1000nH, which is about three times the critical inductance. For these designs, the inductance can be reduced to improve the transient responses.

In National Semiconductor's LM2639 and Semtech's SC1144 designs, the inductance for the four-channel interleaving buck is 300nH, which is less than half of the critical inductance. In these designs, the inductances can be increased to improve efficiency without compromising transient responses.

Similar to the small-signal analysis discussion in Chapter 2, the multi-channel interleaving buck can be normalized to an equivalent single buck converter. After normalization, the inductance designs of different channel numbers can be compared on the same curve as shown in Fig. 3.25. The curve can be easily drawn based on (3.20) and (3.21); the control bandwidth is assumed to be 50kHz.

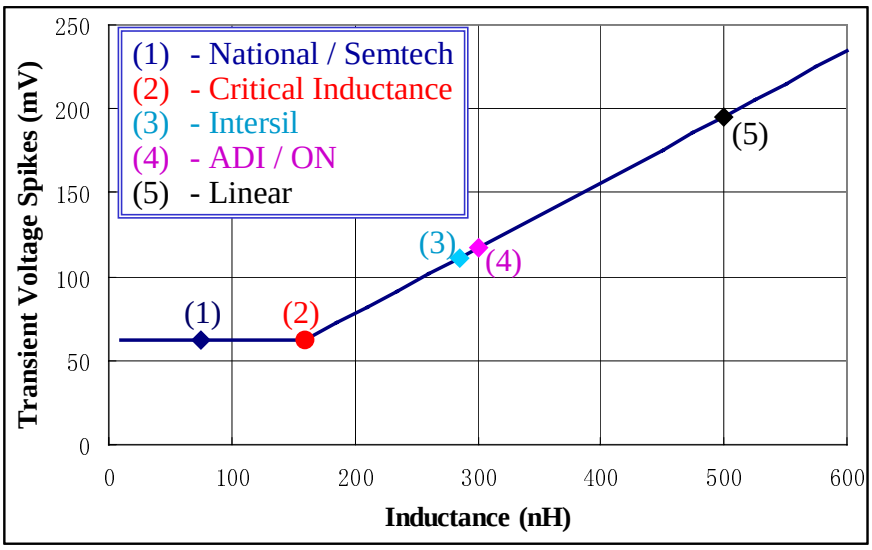


Fig. 3.25. Comparison of industrial designs with critical inductance.

The selection of control bandwidth to be 50kHz is based on one-sixth of 300kHz, which is the common switching frequency in today's industrial practice. As discussed in Chapter 2, the equivalent switching frequency of an n-channel interleaving converter is n times the switching frequency in each channel. Assuming four-channel interleaving topology is used, the equivalent switching frequency can be increased to four times, so can the control bandwidth, which is 200kHz. The transient responses can be greatly improved because of this control bandwidth increase. The transient response curves of control bandwidth equal to 50kHz and 200kHz are compared in Fig. 3.26. Today's industrial design can be greatly improved.

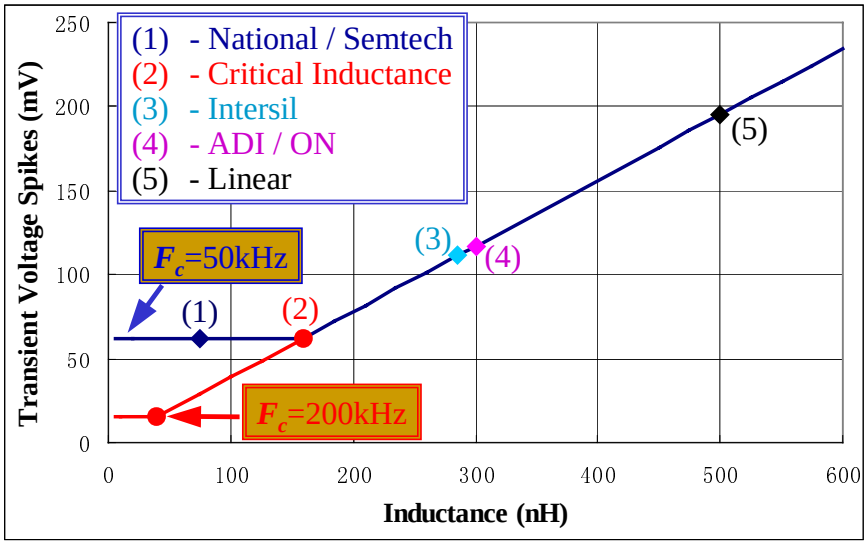


Fig. 3.26. High equivalent switching frequency in interleaving converters improves transient responses.

In critical inductance design, transient response is determined by control bandwidth. To improve the transient response, the control bandwidth must be increased, which requires higher equivalent switching frequency, which can be achieved either by increasing the switching frequency in each channel or by increasing the interleaving channel number. Although the latter increases the complexity of the converter, the efficiency can be greatly improved because of the low switching frequencies. The design processor is shown in Fig. 3.27.

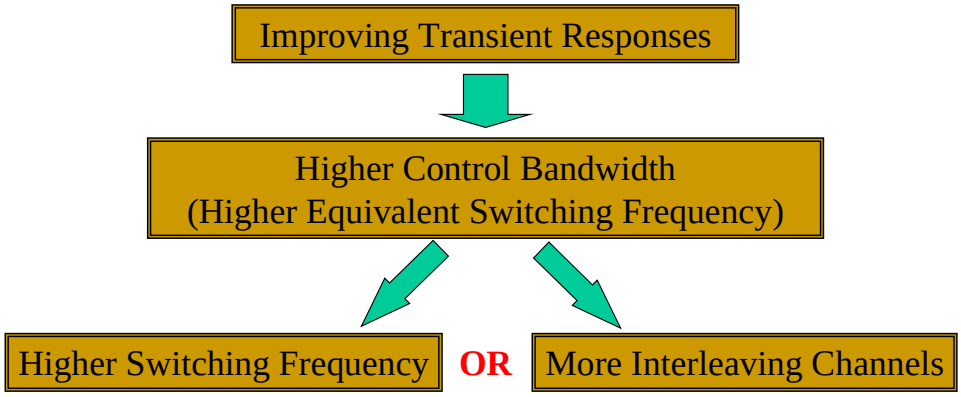


Fig. 3.27. More interleaving channels can improve transient response without increasing switching frequency.

Research of the today's industry VRM design practices shows that the concept of critical inductance has not yet been adopted. The inductance designs are either much larger or smaller than the critical inductances. There is room to improve today's VRM designs.

3.6 Summary

In this chapter, the concept of critical inductance is presented: The critical inductance is defined as the point at which the duty cycle is close to saturation during transient responses; it is the largest inductance that gives the fastest transient responses; and it is a function of the control bandwidth and load current step. Critical inductance is a good tradeoff between the steady-state and transient performances of the VRM.

Both the step-up and step-down transient responses have corresponding critical inductances. The inductances smaller than the lesser of the two critical inductances give symmetric step-up and step-down transient responses. The transient voltage spikes in symmetric transient responses are smaller than those in asymmetric transient responses.

The concept of critical inductance has not yet been adopted in industry. There is room for improvement of today's VRM designs.

Chapter 4

Performance Improvements of Interleaving VRMs with Coupling Inductors

Integrated magnetic components are used in the multi-channel interleaving buck VRM in order to reduce circuit complexity, to reduce the size of the converter and to improve efficiency. However, the structure of the integrated magnetics requires precise adjustment and is not mechanically stable. Moreover, the conflicting inductance requirements for fast transient responses and smaller steady-state current ripples cannot be solved by channel interleaving or integrated magnetic technology.

This chapter proposes the use of integrated coupling inductors between the interleaving channels to solve these problems. The coupling inductors between the channels give different equivalent inductances for transient response and steady-state operation. With the proper design, coupling inductors can improve both the steady-state and dynamic performances. Moreover, the core structure of the integrated coupling inductors is easier to manufacture.

4.1 Integrated Inductors for Interleaving VRMs

Although multi-channel interleaving VRMs have lots of benefits, the major drawback is the complexity of the circuit. As discussed in Chapter 1, the number of MOSFETs used in a single buck and an interleaving buck should be the same for fair comparison. With the variety of commercial control ICs, the cost of the

more complicated controllers required by interleaving VRMs is acceptable. The complexity of the interleaving VRMs is mainly due to the higher number of inductors involved in the converter.

In order to simplify the magnetic components used in interleaving VRMs, Professor Wei Chen proposed the use of integrated inductors in interleaving buck VRMs to reduce the core number. The concept is to integrate the two individual inductors of the two interleaving channels with a 180^o phase shift into a single pair of E-E or E-I cores. The circuit is shown in Fig. 4.1.

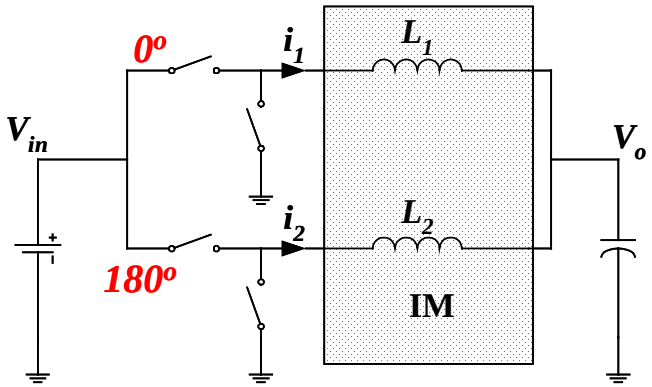


Fig. 4.1. Integrated inductors in a two-channel interleaving buck VRM.

The concept of the integrated inductors is explained in Fig. 4.2. Conventionally, the two inductors L_1 and L_2 can be built on two pairs of separate U-I cores, as shown in Fig. 4.2(a). The directions of the winding currents are marked in the figure. The air gaps are evenly distributed in the two legs. Of course, the air gaps can also be moved into one leg, as shown in Fig. 4.2(b), without changing the inductances. The two pairs of U-I cores can then be moved together and combined into a pair of E-I cores, as shown in Fig. 4.2(c). There is no air gap in the center leg of the E-I cores. The center leg is a low-reluctance path. The fluxes generated by the two windings in the two outer legs all flow through the center leg. As shown in Fig. 4.2(c), there is no interaction between the two flux loops. Although the two inductors are built on the same pair of E-I cores,

there is no coupling effect between them. The circuit operation of the two-channel interleaving buck circuit shown in Fig. 4.1 is not affected by this magnetic structure change. The core structure is simplified.

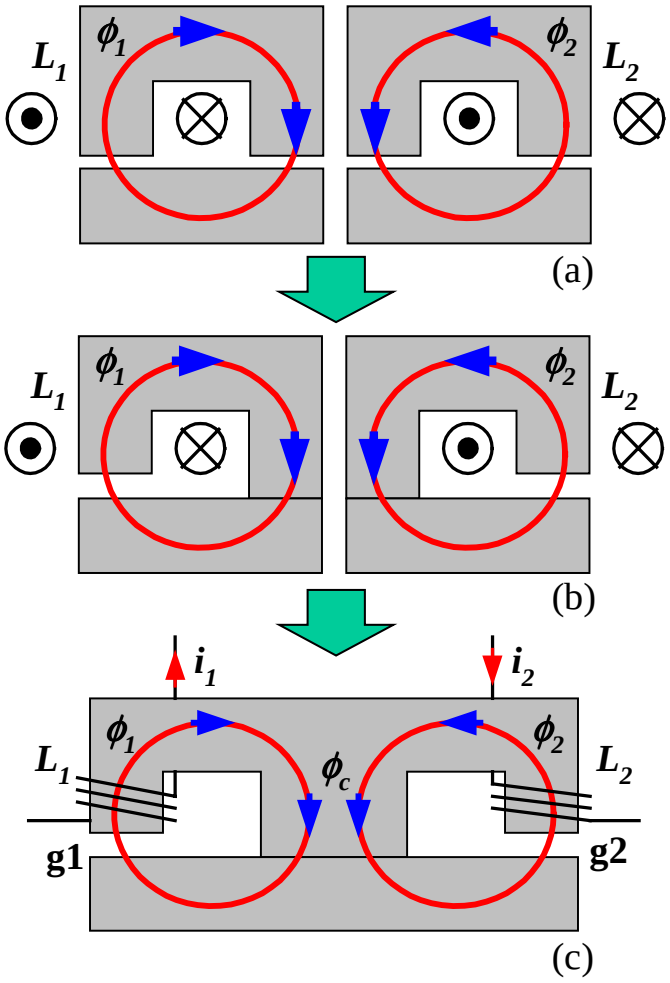


Fig. 4.2. Integrated inductor structure proposed by Prof. W. Chen.

Another benefit of this integrated inductor structure is that the flux in the center leg has smaller ripples. As discussed in Chapter 1, the purpose of the interleaving VRM is to use small inductance to improve the transient responses. Small inductances result in large current ripples in each channel. The fluxes in the core, which have waveforms similar to those of the winding currents, also have

large ripples. The large flux ripples cause extra core losses. In the integrated inductor core structure, with the winding currents flowing in the directions defined in Fig. 4.2, the flux in the center leg is the sum of those in the two outer legs. The phase shift between the two outer leg fluxes is 180^{o}, the same as that between the two winding currents. Due to the ripple cancellation effects, the sum of the two fluxes has much smaller ripples, as shown in Fig. 4.3. Because of the small flux ripples in the center leg, the core losses in the center leg can be reduced.

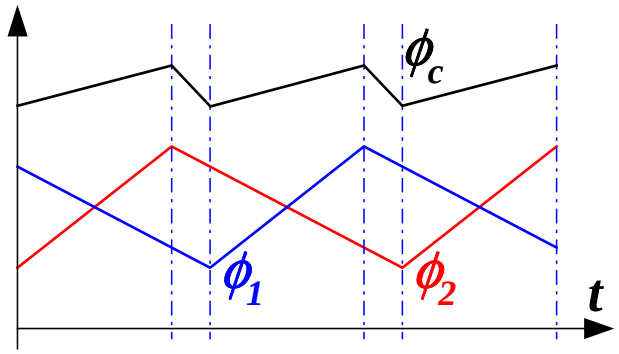


Fig. 4.3. The integrated inductor structure has a flux ripple cancellation effect in the center leg.

Because of the small inductance requirements in the VRM, few turns are required for the windings. PCB winding and the planar cores can be used to reduce the profile of the power stage. The core and PCB winding structures are shown in Fig. 4.4.

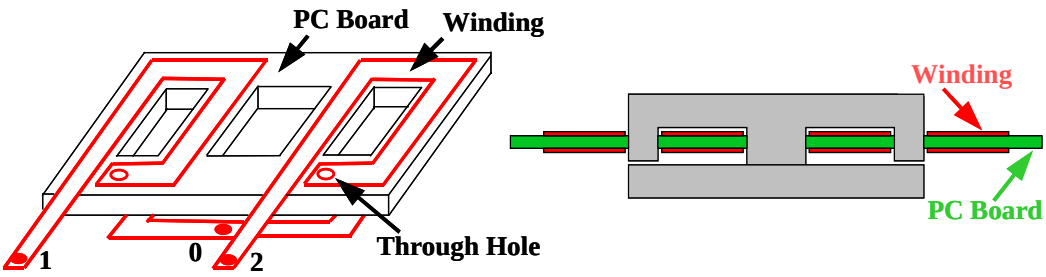


Fig. 4.4. Use PCB winding in the integrated inductors.

With the PCB winding, the parasitic resistances of the inductors in different channels can be easily controlled, which enables the current-sharing methods that rely on the inductor DC resistance.

Despite all these advantages, this integrated inductor structure also has some drawbacks. This kind of magnetic core is not a standard industry practice. The cores need to be precisely adjusted. The two pieces of the core connect together only at the center leg. To ensure mechanical stability, gap filling must be used in the air gap of the two outer legs. Because no air gap is allowed in the center leg, the thicknesses of the gap fillings in the two outer legs must be precisely equal to the thicknesses of the air gaps. This makes mass production difficult and costly. Besides the cost, the single connection in the center leg makes the structure mechanically unstable. Audio noises might be detected in relation to large load transient responses. Moreover, contrary to conventional inductor designs in which the air gap can be adjusted to achieve different inductances, once the integrated inductor core is cut only one inductance value can be obtained. This also reduces the flexibility of the core.

This chapter proposes to use the coupling inductors between channels in order to solve the mechanical instability of the integrated inductor core structure. It turns out that the coupling inductors not only improve the core structures but also improve both the steady-state and dynamic performances of the VRMs.

4.2 Equivalent Inductances in Coupling Inductors

In order to improve the mechanical stability of the core structure, an air gap is introduced into the center leg of the E-I core, as shown in Fig. 4.5.

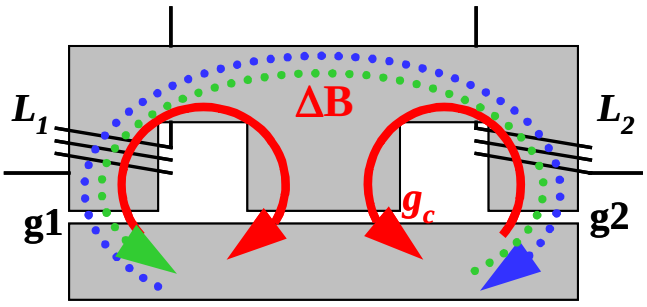


Fig. 4.5. Core structure of the proposed integrated coupling inductors.

The only difference between the core structures shown in Fig. 4.5 and 4.2(c) is the air gap in the center leg. With the air gap in the center leg, the thicknesses of the gap fillings of the two outer legs do not need to be very precise. This structure ensures mechanic stability. Because of the air gap, the center leg is no longer a low magnetic reluctance path for flux. The flux generated by the winding of L_1 can go through all three legs if the winding of L_2 is an open circuit. The flux generated by the winding of L_2 has a similar path. The flux interaction between the windings, the dotted line in Fig. 4.5, indicates the coupling effect between these two inductors. The following analyzes how the coupling effect affects the steady-state and dynamic performances of the converter.

Because of the coupling effect, the two inductors can no longer be considered as two individual inductors. A coupling inductance M between the two inductors can represent the coupling effect, as shown in Fig. 4.6.

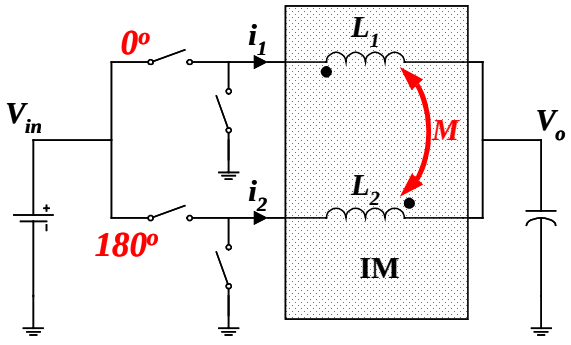
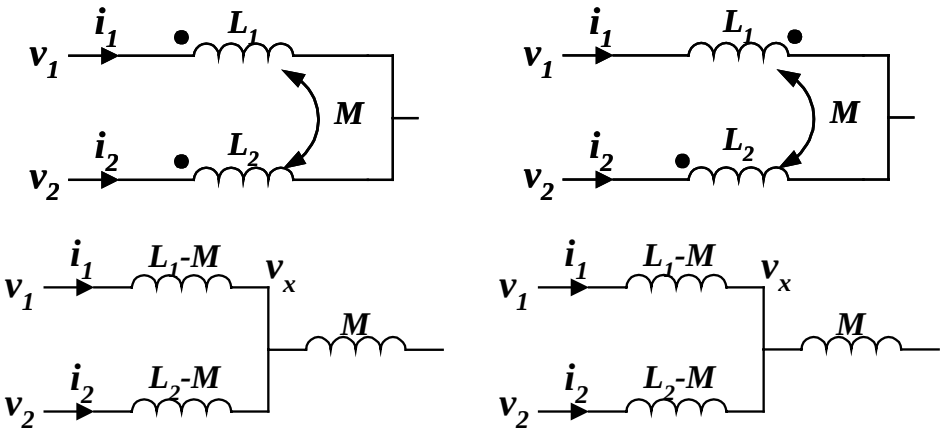


Fig. 4.6. Interleaving bucks with coupling output inductors.

For simplicity, the two inductances built on the same core are considered to be the same (L_1=L_2=L). The two inductors can be directly coupled or inversely coupled, due to the different direction selections between the two windings. There are two similar equivalent circuits for each coupling format, as shown in Fig. 4.7. If coupling inductance M in the direct coupling case is defined to be positive, and the coupling inductance in the inverse coupling case is defined to be negative, the two equivalent circuits are identical. There exists

$$M = \alpha \cdot L, \quad (-1 < \alpha < 1). \tag{4.1}$$



(a) (b)

Fig. 4.7. Two different coupling formats: (a) direct coupling (M>0); and (b) inverse coupling (M<0).

With this definition of the coupling inductance M, both the two coupling formats can be described as follows:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} L & M \\ M & L \end{bmatrix} \cdot \begin{bmatrix} di_1/dt \\ di_2/dt \end{bmatrix}, \tag{4.2}$$

where v_1 and v_2 are the voltages applied to the two corresponding inductors. There are two possible voltage values for v_1 and v_2: V_a, corresponding to the turn-on of the top switches; and V_b, corresponding to the turn-on of the bottom switches:

$$\begin{cases} V_a = V_{in} - V_O \\ V_b = -V_O \end{cases}, \tag{4.3}$$

where V_{in} and V_o are the input and output voltages of the converter, as defined in Fig. 4.6. For the buck converter, there exists $V_{in} = D*V_o$. The relationship between V_a and V_b can be found as follows:

$$D \cdot V_a = -(1-D) \cdot V_b = -D' \cdot V_b . \tag{4.4}$$

For the non-coupling inductor case ($M=0$), the corresponding equations are as follows:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} L & 0 \\ 0 & L \end{bmatrix} \cdot \begin{bmatrix} di_1/dt \\ di_2/dt \end{bmatrix}. \tag{4.5}$$

In order to compare the equivalent inductances of the coupling and non-coupling inductors, (4.2) is rewritten in a format similar to that of (4.5), as follows:

$$\begin{bmatrix} v_1 - \frac{M}{L} \cdot v_2 \\ v_2 - \frac{M}{L} \cdot v_1 \end{bmatrix} = \begin{bmatrix} L - \frac{M^2}{L} & 0 \\ 0 & L - \frac{M^2}{L} \end{bmatrix} \cdot \begin{bmatrix} di_1/dt \\ di_2/dt \end{bmatrix}. \tag{4.6}$$

For (4.6), if the relationship between v_1 and v_2 can be found, the two inductors can be decoupled, so that they can be compared with the non-coupling inductors. For the circuit with coupling inductors, the switch operation is exactly the same as

that of the circuit with non-coupling inductors. The waveforms of v_1 and v_2 for duty cycle D<0.5 are shown in Fig. 4.8.

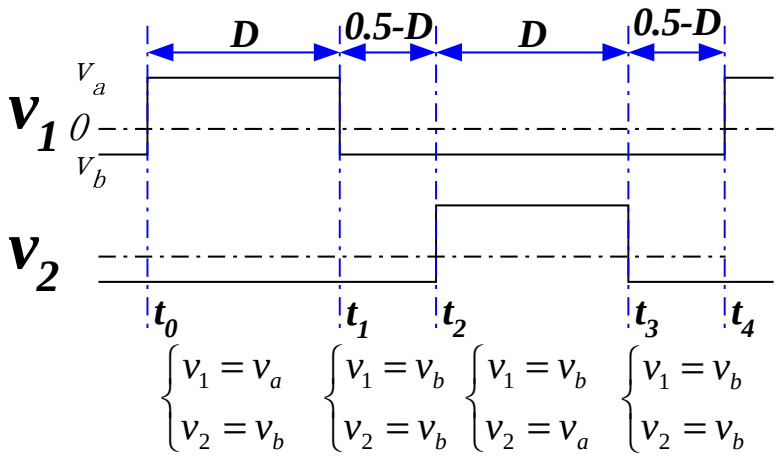


Fig. 4.8. Inductor voltage waveforms.

A switching cycle can be divided into four time intervals. The relationships between v_1 and v_2 are different in each time interval. During (t_0-t_1), the top switch of the first channel is on (v_1=V_a), and the bottom switch of the second channel is on (v_2=V_b). The relationship between the two inductor voltages can be determined from (4.4) as follows:

$$v_1 = -\frac{D'}{D} v_2 . \tag{4.7}$$

With (4.7), (4.6) can be rewritten as follows:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} \dfrac{L - \dfrac{M^2}{L}}{1 + \dfrac{M}{L} \cdot \dfrac{D}{D'}} & 0 \\ 0 & \dfrac{L - \dfrac{M^2}{L}}{1 + \dfrac{M}{L} \cdot \dfrac{D'}{D}} \end{bmatrix} \cdot \begin{bmatrix} di_1/dt \\ di_2/dt \end{bmatrix}. \tag{4.8}$$

Using the preceding mathematical operations, the equations for the two-channel interleaving buck with coupled inductors can be decoupled. Formula (4.8) has the same format as (4.5). An equivalent inductance can be defined by comparing (4.8) with (4.5). For simplification, only the equivalent inductance in the first channel is discussed. The equivalent inductance in the second channel is similar expect for a phase shift. For the first channel, the equivalent inductance in the time interval of (t_0-t_1) is as follows:

$$L_{eq1} = \frac{L^2 - M^2}{L + \frac{D}{D'} \cdot M}. \tag{4.9}$$

For the different time intervals, (4.6) is always true. However, (4.7) will change according to the relationship between the two inductor voltages in the time intervals. Thus, different equivalent inductances can be derived for each time interval in a switching cycle.

For time interval (t_1-t_2), the bottom switches of both channels are turned on. The voltages applied to the two channels are the same. In this time interval, (4.7) needs to be changed to (4.10):

$$v_1 = v_2 = v_b. \tag{4.10}$$

With (4.10), (4.6) can be simplified as follows:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} L+M & 0 \\ 0 & L+M \end{bmatrix} \cdot \begin{bmatrix} di_1/dt \\ di_2/dt \end{bmatrix}. \tag{4.11}$$

Based on (4.11), the equivalent inductance for the first channel during time interval (t_1-t_2) can be defined as follows:

$$L_{eq2} = L + M \ . \tag{4.12}$$

Similarly, for time interval (t_2-t_3), the relationship between the two inductor voltages are as follows:

$$v_1 = -\frac{D}{D'} v_2 \, . \tag{4.13}$$

The equivalent inductance in this time interval can be derived as follows:

$$L_{eq3} = \frac{L^2 - M^2}{L + \frac{D'}{D} \cdot M} \, . \tag{4.14}$$

During time interval (t_3-t_4), the voltages applied to the two inductors are exactly the same as during time interval (t_2-t_3). Thus, the equivalent inductance in this time interval should equal L_{eq2}. There are three different equivalent inductances in a switching cycle.

The voltage waveforms for the case of steady-state duty cycle D>0.5 are shown in Fig. 4.9. Following the same process as for the case in which D<0.5, it can be found that the equivalent inductances for all the four time intervals in the case of D>0.5 are exactly the same as those in the case of D<0.5.

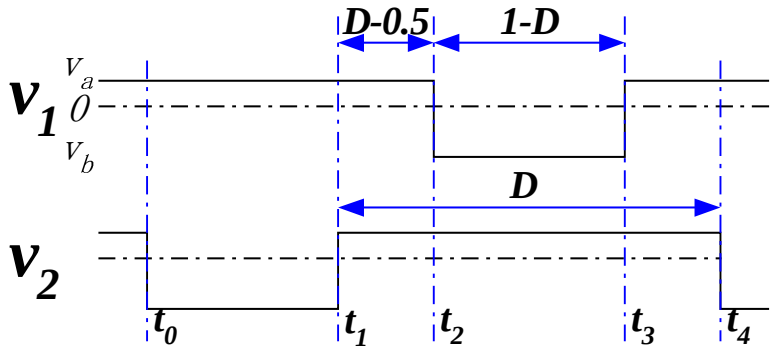


Fig. 4.9. Inductor voltage waveforms (D>0.5).

The purpose of the equivalent inductances is to mathematically decouple the two coupled inductors, so that they are comparable to the non-coupling inductors. The coupling inductor case has different equivalent inductances during each time interval in a switching cycle, while the inductances in the non-coupling case are always the same for the whole switching cycle.

The equivalent inductances are functions of the self-inductance L, the coupling inductance M, and the relationship between the two inductor voltages. In this work, the relationship between the two inductor voltages is represented by the steady-state duty cycle D. It is important to note that the duty cycle changes during transient responses. However, the two possible voltages applied to the windings are still the same (V_{in}-V_o or -V_o) if the small transient voltage variances are ignored. Thus, the equivalent inductances are still valid during transient responses. The parameter D in the equivalent inductance formula should always use the steady-state duty cycle rather than the transient duty cycles.

4.3 Inductor Coupling Effects on Converter Performances

Based on the preceding equivalent inductance discussion, this section analyzes the effects of the coupling inductors on converter performance both in steady-state operations and during transient responses. The steady-state criterion is the current ripple because it has a direct impact on converter efficiency. The transient criterion is the current slew rate during transient responses.

The voltage and current waveforms of non-coupling inductors are shown in Fig. 4.10. Because the channels work independently, only one channel is shown. The steady-state waveforms are the solid lines.

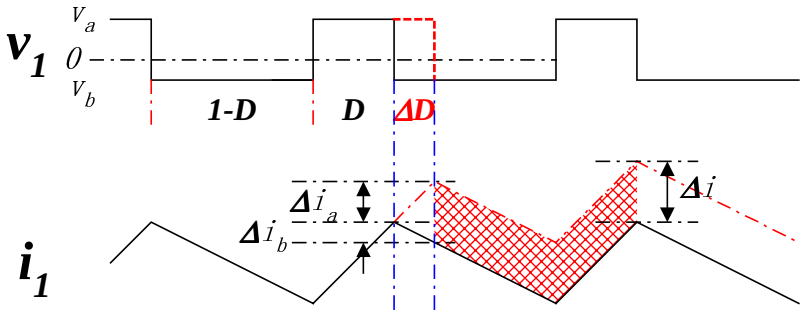


Fig. 4.10. Inductor voltage and current waveforms for non-coupling inductor.

The steady-state peak-to-peak current is as follows:

$$I_{pp\_nc} = \frac{v_a \cdot D}{L \cdot F_s}. \tag{4.15}$$

During transient responses, assume the duty cycle has an increase of ΔD, as discussed in the preceding chapter. The transient inductor current waveform is the dotted line in Fig. 4.10. After a switching cycle, the inductor current has an increase of Δi. From the waveform, Δi can be derived as follows:

$$\Delta i = \frac{V_{in} \cdot \Delta D}{L \cdot F_s}. \tag{4.16}$$

Formula (4.16) is consistent with (3.9), the equation for the average current slew rate given in the preceding chapter.

$$\left.\frac{di}{dt}\right|_{avg} = \frac{\Delta i}{T_s} = \frac{V_{in} \cdot \Delta D}{L}. \tag{4.17}$$

For steady-state operation, a large inductance is preferred so that the current ripples can be reduced. However, for the transient response, a small inductance is preferred so that a high transient inductor current slew rate can be achieved. As discussed before, the steady-state and dynamic performances have contradictory

requirements of the inductance. For non-coupling inductors, there is only one inductance in the two formulas. The steady-state performance must be sacrificed to achieve fast transient responses.

For the coupling inductors between the interleaving channels, the inductor current waveforms in steady state and transient response are more complicated, and need to be divided into different categories. The case in which the steady-state duty cycle D<0.5 is analyzed first.

Fig. 4.11(a) compares the steady-state inductor voltage and current waveforms of the non-coupling and direct coupling cases (M>0) for the steady-state duty cycle D<0.5. The inductor voltage waveforms are exactly the same for the two cases. The solid lines are the inductor current waveforms for direct coupling inductors, while the dotted-dashed lines are the inductor current waveforms for non-coupling inductors. Fig. 4.11(b) compares the non-coupling and inverse coupling (M<0) inductors' waveforms.

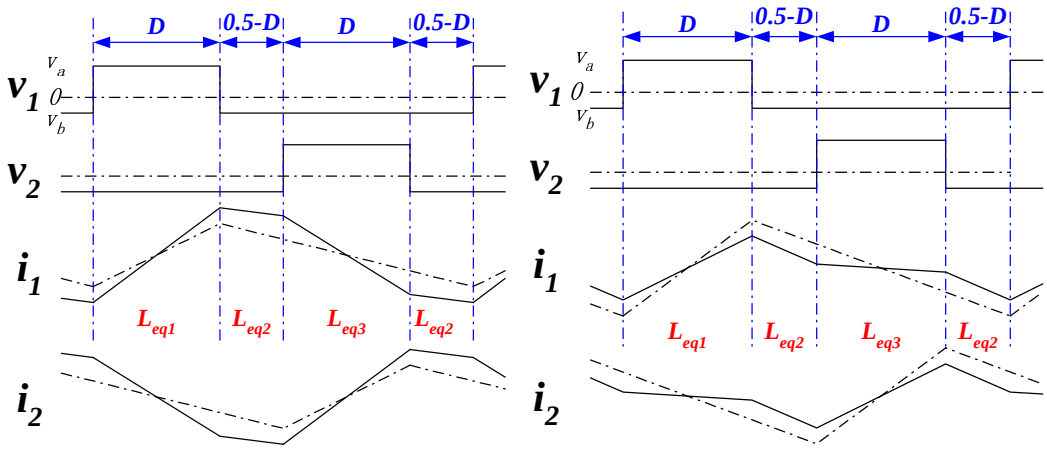


Fig. 4.11. Steady-state voltage and current waveforms for coupling inductors (D<0.5): (a) direct coupling (M>0); and (b) inverse coupling (M<0).

For both coupling cases (M>0 or M<0) in Fig. 4.11, the inductor current ripples are determined only by L_{eq1}. The inductor peak-to-peak current is described in (4.18). Comparing (4.18) with (4.15), the only difference is the inductances. Thus, L_{eq1} is defined as the steady-state equivalent inductance.

$$I_{pp\_cp(D<0.5)} = \frac{v_a \cdot D}{L_{eq1} \cdot F_s}. \tag{4.18}$$

From the definition of L_{eq1} in (4.9), it can be found that for M>0, there always exists $L_{eq1}<L$, which results in larger current ripples than those that occur in the non-coupling inductors. A comparison of the steady-state inductor current ripples is also shown in Fig. 4.11(a). However, for M<0, under the condition of (4.19), there exists $L_{eq1}>L$. In this case, the steady-state current ripple can be reduced below that of the non-coupling case, as shown in Fig. 4.11(b).

$$-\frac{M}{L} < \frac{D}{D'}. \tag{4.19}$$

In summary, direct coupling inductors have larger steady-state current ripples than the non-coupling inductors. Through proper design, inverse coupling inductors can reduce steady-state current ripples. Smaller current ripples are preferable.

Similar to the transient analysis of the non-coupling case, a duty cycle increase of ΔD is assumed during the transient response. As discussed in Chapter 2, the ΔD values in the two interleaving channels are the same. The inductor voltage and current waveforms (both M>0 and M<0) during transient responses are shown in Fig. 4.12.

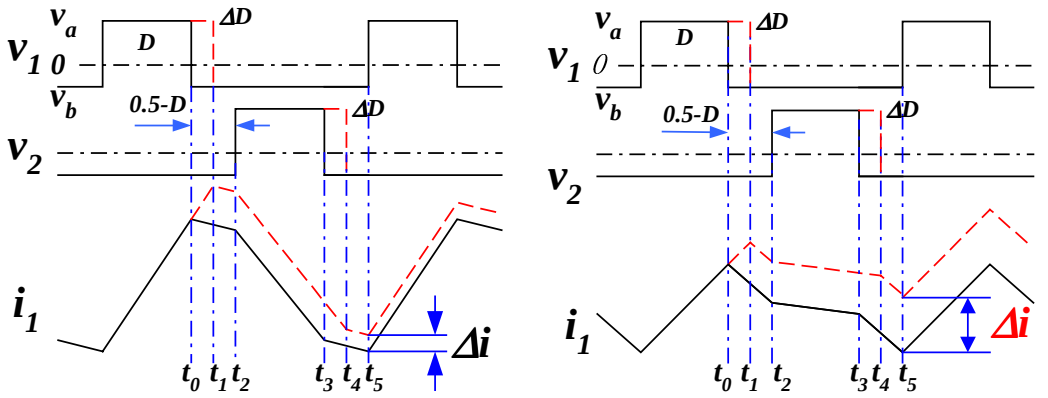


Fig. 4.12. Transient voltage and current waveforms for coupling inductors (D<0.5 and 0<ΔD<(0.5-D)): (a) direct coupling (M>0); and (b) inverse coupling (M<0).

From the waveforms, the inductor current increase after a switching cycle can be derived as shown in (4.20). The formula is valid for both M>0 and M<0. For the waveforms in Fig. 4.12, the steady-state duty cycle D<0.5 and transient duty cycle increase 0<ΔD<(0.5-D) are assumed. It can be proved that (4.20) is valid for cases in which D<0.5 and D>0.5 for the whole transient duty cycle increase range of (-D)<ΔD<(1-D). For detailed derivations, refer to the Appendix.

$$\Delta i = \frac{V_{in} \cdot \Delta D}{L_{eq2} \cdot F_s} \cdot \tag{4.20}$$

Comparing (4.20) and (4.16), the only difference is the inductance. L_{eq2} is the only inductance that determines the inductor current slew rate. The equivalent inductance L_{eq2} is defined as the transient equivalent inductance.

The transient inductor current slew rate can also be explained using the average model, as discussed in Chapter 2. Similar to Fig. 2.2, the average model of the two-channel interleaving buck converter with coupling inductors shown in Fig. 4.6 is shown in Fig. 4.13.

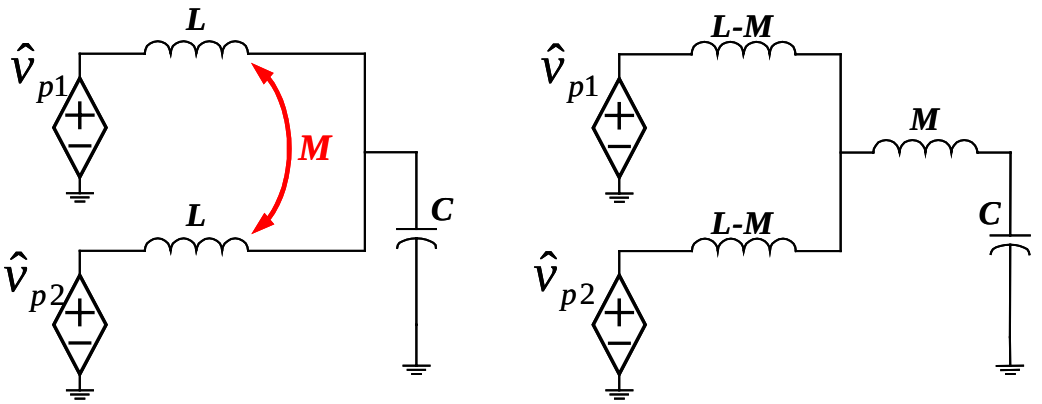


Fig. 4.13. Average model for the two-channel interleaving buck with coupling inductors.

Similar to the discussion in Chapter 2, the average voltages applied to the two inductors during transient responses are the same, as shown in the following:

$$\hat{v}_{p1} = \hat{v}_{p2} = \hat{v}_p = V_{in} \cdot \Delta D \,. \tag{4.21}$$

Fig. 4.13 can be simplified, as shown in Fig. 4.14.

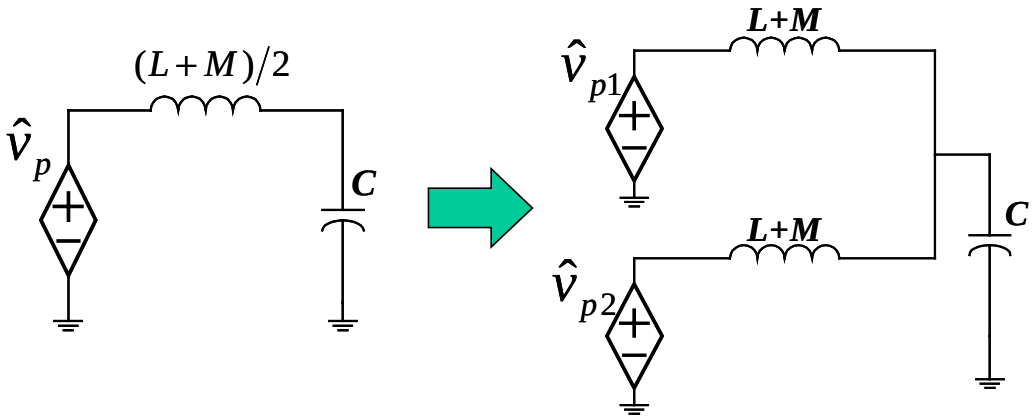


Fig. 4.14. Using the average model, the coupling inductors in the interleaving buck converter can be decoupled during transient responses.

With the circuit transformation, the coupling inductors in the two-channel interleaving buck converter can be decoupled during transient responses. The

average inductor current slew rate in each channel can be easily derived as follows:

$$\left.\frac{di}{dt}\right|_{avg} = \frac{V_{in}\cdot\Delta D}{L+M} = \frac{V_{in}\cdot\Delta D}{L_{eq2}}. \tag{4.22}$$

Formula (4.22) is equivalent to (4.20). The preceding discussions based on the average model do not assume the steady-state duty cycle or transient duty cycle increase ranges. Thus, (4.22) is valid for all duty cycle ranges in each case.

The transient equivalent inductance $L_{eq2}=L+M$ is the only inductance that determines the transient inductor current slew rate. To improve the transient responses, a small inductance is preferred. From the definition of L_{eq2} in (4.12), the inverse coupling inductor ($M<0$) gives a smaller transient equivalent inductance.

As discussed in Chapter 2, the inductance in the average model can be observed in small-signal transfer functions. Similar to the small signal transfer function simulation based on the switching model used in Chapter 2, a two-channel interleaving buck converter with different coupling inductors is simulated. The control-to-output-voltage transfer functions $G_{dv}'(s)$ are shown in Fig. 4.15.

For the three curves in Fig. 4.15, the self-inductances are the same, while the mutual inductances are different. The corner frequencies of the curves are determined by the transient equivalent inductance $L_{eq2}=L+M$ and the output capacitance. In all cases, same output capacitances are used. The smaller L_{eq2} corresponds to higher corner frequencies.

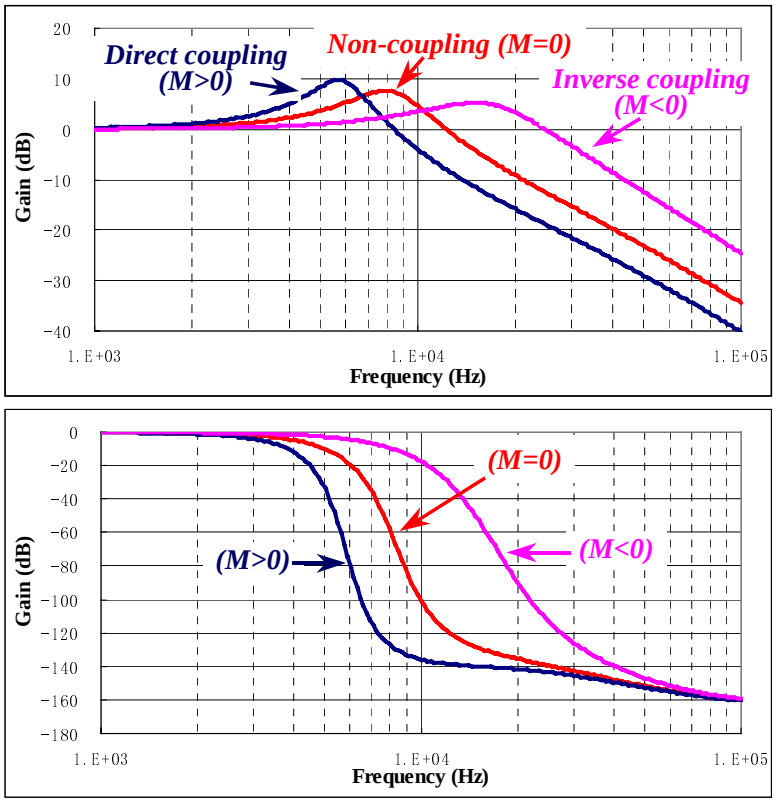
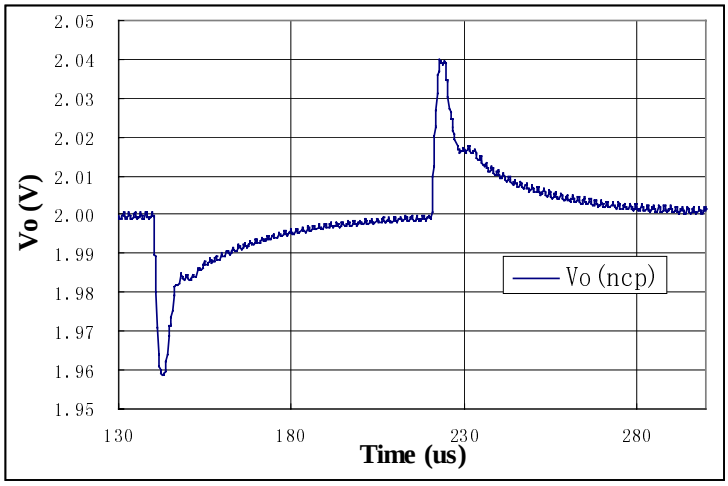
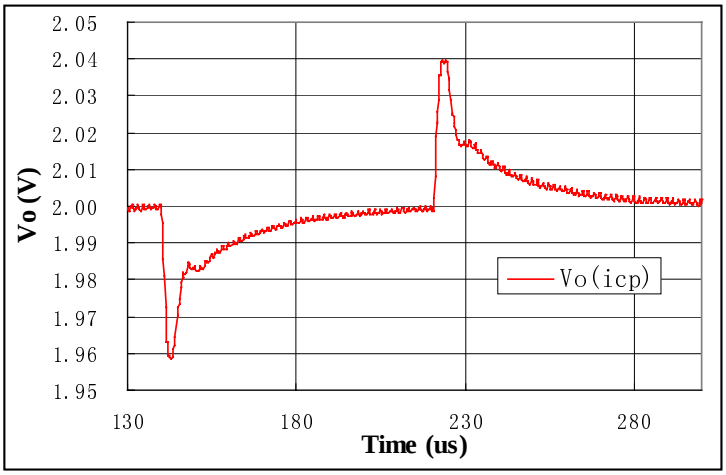


Fig. 4.15. Switching model simulation results of small signal transfer functions of different coupling inductors.

As discussed in Chapter 3, the transient response is determined by the inductance and the control bandwidth. If the transient equivalent inductances L_{eq2} are designed to be the same for both the non-coupling and coupling inductors, the small-signal models of these two cases are the same. The same feedback controller can be used in both cases. The transient responses of these two cases should also be the same. The time domain simulation waveforms of a two-channel interleaving VRM transient responses with non-coupling and inverse coupling inductors are shown in Fig. 4.16(a) and (b), respectively. The two simulation circuits have the same transient equivalent inductances L_{eq2}, but different self-inductances. Both the step-up and step-down transient voltage spikes for the two cases are the same. This also verifies that it is the transient equivalent inductance L_{eq2} that determines the transient responses.



(a)



(b)

Fig. 4.16. Transient voltage waveforms of different coupling inductors: (a) non-coupling and (b) inverse coupling.

Another important objective in using interleaving is to reduce the overall output current ripples. How would the coupling inductors affect the overall output current waveforms $i_o=i_1+i_2$? The inductor current waveform in each channel of the non-coupling core structure is determined in (4.2). The output current waveform, which is the sum of the inductor current waveforms, can be found by adding the two equations in (4.2) as follows:

$$v_1 + v_2 = (L + M) \cdot \frac{d(i_1 + i_2)}{dt} = L_{eq2} \cdot \frac{di_o}{dt}. \tag{4.23}$$

Formula (4.23) shows that if the transient equivalent inductances of the converters are the same, the output current waveforms are the same for different inductor structure designs.

All the preceding simulation results and discussions show that the transient equivalent inductance is not a parameter defined only for mathematical analysis; it is a parameter with physical meanings, and it plays important roles in VRM performance.

In summary, if properly designed, inverse coupling between the two inductors gives smaller transient equivalent inductance L_{eq2} and larger steady-state equivalent inductance L_{eq1}. The inverse coupling inductors are able to improve both the transient and steady-state performances over those of non-coupling inductors. Direct coupling inductors are not desirable because not only do they increase the steady-state current ripples, but they also slow down the transient current slew rate.

The major benefit of the coupling inductors is the different equivalent inductances for steady-state and transient performances. The inductance requirements for steady state operations and transient responses are contradictory. For the non-coupling case, there is only one inductance, which makes it impossible to improve the steady-state and dynamic performances simultaneously. For coupling inductors, the steady-state and dynamic performances are determined by different equivalent inductances. Under certain conditions, both the steady-state and dynamic performances can be improved by adjusting the corresponding equivalent inductances. The possibility of improving both the steady-state and transient performances is the main benefit of using coupling inductors in interleaving VRMs.

4.4 Design and Simulation Results

Analysis in the previous section shows that inverse coupling between the inductors in the two channels with a 180^o phase shift can improve both the transient and steady-state performances of the VRM. This section discusses the optimal design of the inductances and the magnetic cores to achieve the maximum possible benefits from the coupling inductor concept. The discussions include the inductance values, AC and DC flux distribution in the core, and winding losses.

The non-coupling interleaving VRM is used as the benchmark for comparison to show the improvements offered by coupling inductors. In order to have fair comparison between the non-coupling and coupling inductors, the circuit designs of the two cases should be as similar as possible, except for the inductors. As discussed previously, if the converters are designed to have the same transient equivalent inductance, the small-signal transfer functions would be the same, and the same feedback controller can be used. The only difference between the converters is the inductors, an approach which offers the least difference between the converters under comparison. With the same transient equivalent inductance, the transient responses are expected to be same. The coupling inductors can improve the steady-state efficiency. The following comparisons of the converters are based on the assumption that the transient equivalent inductances will be the same.

To have the same transient equivalent inductance, the self-inductance in the non-coupling and coupling structures should follow the following formula:

$$L_{nc} = L_{eq2} = L_{cp} + M = (1+\alpha)\cdot L_{cp}, \tag{4.24}$$

where L_{nc} is the inductance of the non-coupling case, while L_{cp} is the self-inductance of the coupling inductors.

Based on (4.24), the relationship between the steady-state inductor peak-to-peak currents of non-coupling and coupling inductors can be found and compared as follows:

$$\frac{I_{pp\_cp(D<0.5)}}{I_{pp\_nc}} = \frac{L_{nc}}{L_{eq1}} = \frac{1+\frac{D}{D'}\cdot\alpha}{1-\alpha}. \tag{4.25}$$

As indicated in the formula, (4.25) is valid for the cases of steady-state duty cycle D<0.5. For the cases of D>0.5, the results are similar. Detailed discussions can be found in the Appendix.

The current ripple reductions by the coupling inductors are functions of steady-state duty cycle D and coupling effects α. The relationship shown in (4.25) is plotted in Fig. 4.17. The steady-state duty cycle closer to 0.5 results in more effective current ripple reduction. Stronger coupling effects give smaller current ripples.

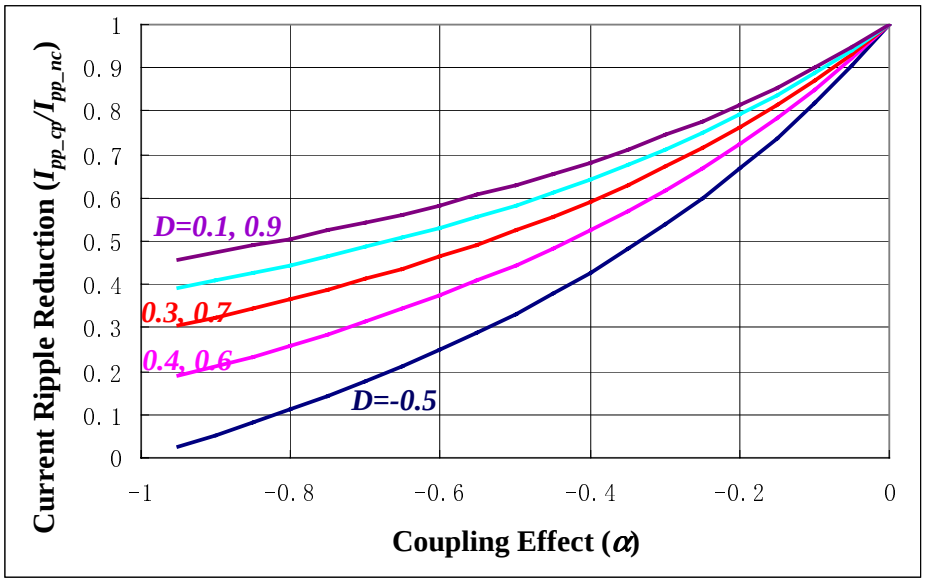


Fig. 4.17. Steady-state current ripple reduction in coupling inductors.

In order to have the same transient responses and achieve smaller steady-state current ripples, the coupling inductors should be designed to have L_{cp} and α as large as possible while maintaining the same L_{eq2}.

Simulation waveforms of non-coupling and coupling inductors are shown in Fig. 4.18 to illustrate the inductor current ripple reduction in coupling inductors. In the two cases in the figure, the transient equivalent inductances are kept to 500nH. The coupling effect of the inverse coupling inductors is –0.5. The individual inductor current ripples are greatly reduced in the coupling inductors. The total output current ripples are the same in the two cases, as explained in (4.23).

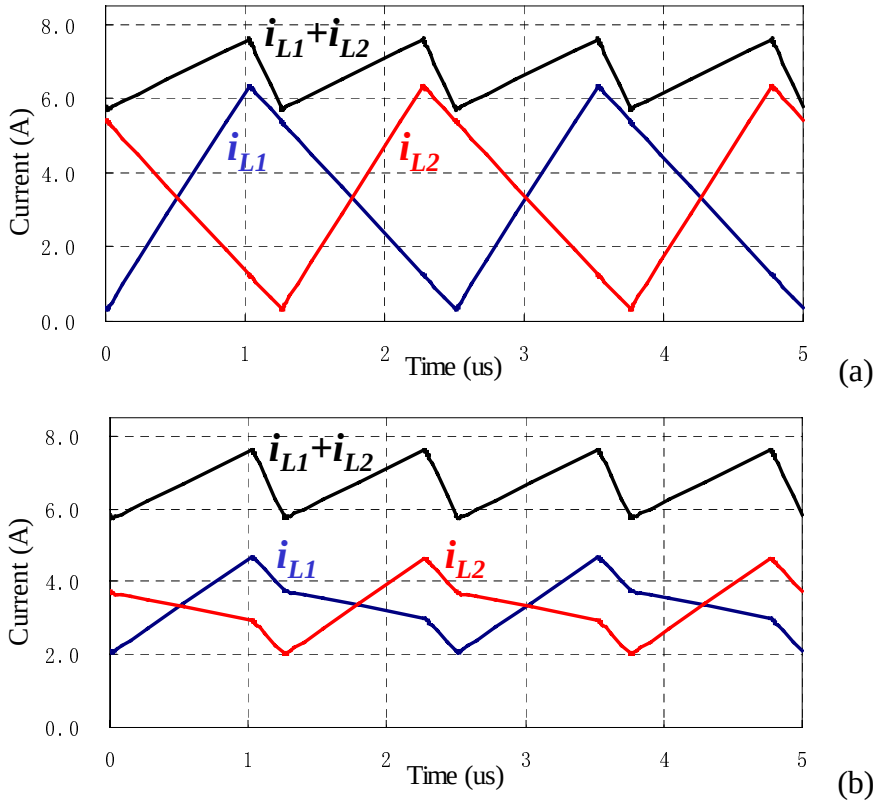


Fig. 4.18. Inverse coupling reduces individual inductor current ripples while maintaining same total current ripples (same L_{eq2}=500nH): (a) non-coupling (M=0); and (b) inverse coupling (M=-0.5).

The following section discusses the design of the magnetic cores. For the core structure shown in Fig. 4.5, the magnetic analog circuit can be easily derived, as shown in Fig. 4.19.

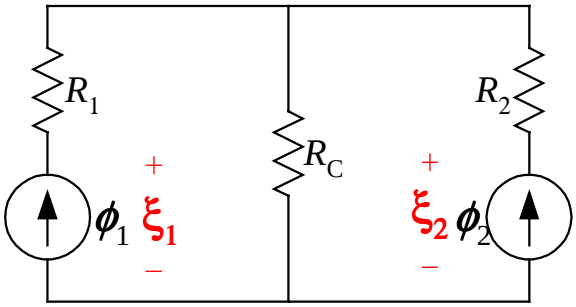


Fig. 4.19. Flux source reluctance circuit for coupling core structure.

R_1, R_2 and R_c in the figure represent the magnetic reluctances of the three legs. The AC fluxes in the two outer legs, ϕ_1 and ϕ_2, are determined only by the time integral of the voltage (which is more simply stated as volt-seconds) across the corresponding winding. For different inductor structures, the inductor voltage waveforms are always the same, so that ϕ_1 and ϕ_2 are the same. This is the reason the two windings in the magnetic analog circuit can be represented by flux sources. The AC flux in the center leg is the sum of the AC fluxes in the two outer legs. Because ϕ_1 and ϕ_2 are the same for different coupling inductors, the AC flux in the center leg should also be the same for different coupling inductors.

The simulation results of the AC fluxes in the three legs for the inverse coupling case are shown in Fig. 4.20.

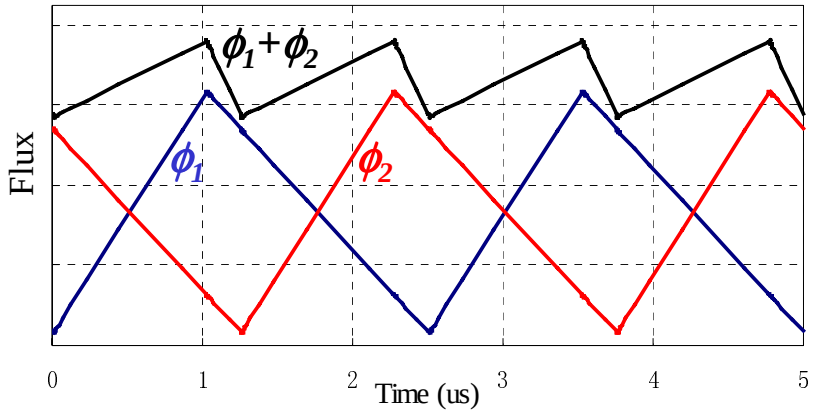


Fig. 4.20. AC flux waveforms are not affected by coupling effects.

Although the coupling effect changes the current waveforms in the inductors, it does not change the AC fluxes in the three legs of the core. The AC fluxes in the non-coupling and coupling core structures are the same as long as the same voltage waveforms are applied to the inductor windings.

The magnetic analog circuit consists of two parts: the reluctance of the magnetic path and the representation of the windings. In Fig. 4.19, the windings are represented as the flux sources, which is different from the conventional reluctance model. The flux sources' characteristics are similar to those of the current sources in electric circuits. In conventional magnetic analog circuits, the windings are represented as the magnetomotive force (MMF) sources. The characteristics of MMF sources are similar to those of the voltage sources in electric circuits. The magnetic circuit, with MMF sources representing of the windings, is shown in Fig. 4.21. The two magnetic circuits shown in Fig. 4.19 and 4.21 are identical. The fluxes through the MMF sources in Fig. 4.21 should be the same values as those shown in Fig. 4.19, while the MMF of the flux sources in Fig. 4.19 should be the same values as those of the MMF sources shown in Fig. 4.21. These two reluctance models will be discussed further in Chapter 5.

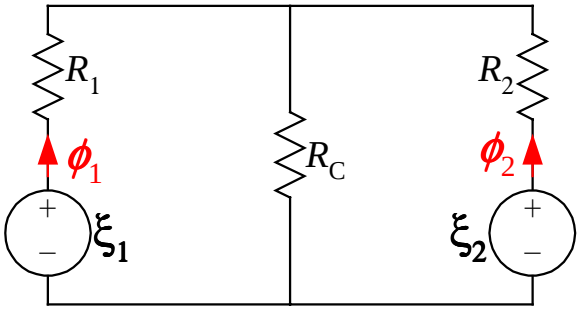


Fig. 4.21. MMF source reluctance circuit for coupling core structure.

From the magnetic reluctance circuits shown in Fig. 4.19 and 4.21, the inductances can be derived as follows (assuming $L_1=L_2=L$ and $R_1=R_2=R$):

$$\begin{cases} L = \dfrac{N^2 \cdot (R + R_c)}{R \cdot (R + 2 \cdot R_c)} \\ M = -\dfrac{N^2 \cdot R_c}{R \cdot (R + 2 \cdot R_c)} \\ \alpha = \dfrac{M}{L} = -\dfrac{R_c}{R + R_c} \end{cases}. \tag{4.26}$$

Another important factor in inductor design is the DC flux bias in the cores. In order to achieve small steady-state current ripples, the coupling inductor structures have larger self-inductances than do the non-coupling structures. In conventional inductor design, larger inductances usually result in high DC flux bias. The DC flux bias in the cores can be rewritten in the format of inductances and inductor currents, as follows:

$$\begin{cases} \Phi_1 = \dfrac{L}{N} \cdot I_1 + \dfrac{M}{N} \cdot I_2 \\ \Phi_2 = \dfrac{M}{N} \cdot I_1 + \dfrac{L}{N} \cdot I_2 \end{cases}, \tag{4.27}$$

where Φ_1 and Φ_2 are the DC fluxes in the two outer legs, I_1 and I_2 are the DC currents in the two inductors, and N is the turn number of the inductors (assuming the two inductors have the same number of turns).

For the symmetric DC currents in the two channels ($I_1=I_2=I$), the DC fluxes in the outer legs can be simplified as follows:

$$\Phi_1 = \frac{L \cdot I}{N} + \frac{M \cdot I}{N} = \frac{L_{eq2} \cdot I}{N}. \tag{4.28}$$

Because the transient equivalent inductance L_{eq2} is the same for both the non-coupling and coupling inductors, the DC flux biases in the two outer legs are exactly the same for the two cases.

The flux in the center leg is always the sum of the fluxes in the two outer legs. Because the two outer legs have the same DC fluxes, the center leg of the non-coupling and coupling core structures has the same DC fluxes. Thus, the DC flux bias in all the three legs in the two core structures are exactly the same as long as the two structures are designed to have the same L_{eq2}.

For inverse coupling core structures, the self-inductance is larger than the non-coupling inductance. Larger inductances usually result in larger DC fluxes if the same cores and windings are used. The same DC fluxes in the non-coupling and coupling inductors are different from conventional ideas. This can be explained briefly in Fig. 4.22. In the non-coupling core structure, the DC fluxes generated by the two windings do not affect each other, as shown in Fig. 4.22(a). For the inverse coupling core structure, part of the DC flux generated by one winding goes through the other winding. Because of the inverse direction, the DC fluxes in the two outer legs are partially cancelled. The percentage of the DC flux that is cancelled is proportional to the mutual inductance. Although larger self-inductance in the coupling core structure generates larger DC flux, the percentage

of the cancelled DC flux is also larger. The overall effect is that the net DC fluxes in the outer legs are the same as those in non-coupling inductors.

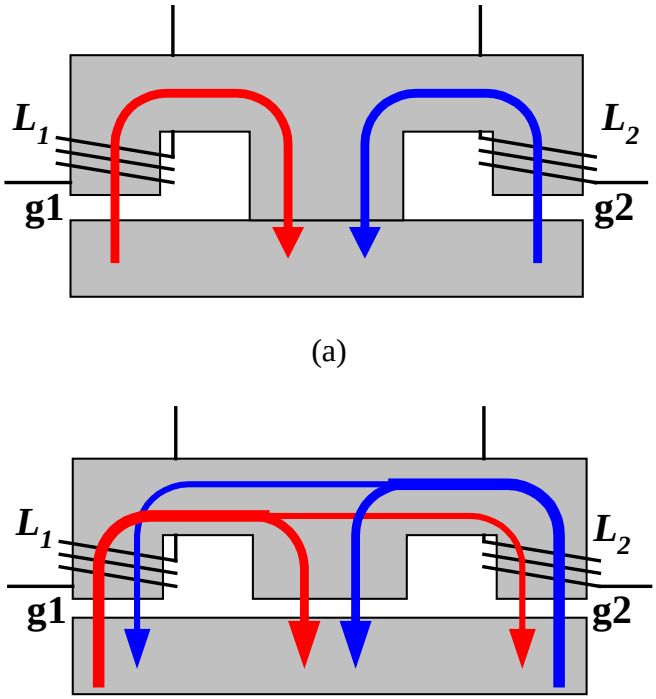


Fig. 4.22. Coupling and non-coupling inductors have same DC fluxes in the three legs (same L_{eq2}): (a) non-coupling; (b) inverse coupling.

The explanation of the DC flux in the center leg is similar. For the non-coupling core structure, the flux in the center leg is the sum of the fluxes generated by the two windings. For the coupling core structure, because part of the flux goes through the other outer leg, the flux in the center leg is only the sum of part of the flux generated by the two windings. Although the windings in the coupling core structure generate larger DC fluxes, the DC flux in the center leg is kept the same for both the non-coupling and coupling core structures.

In summary, if the same cores and windings are used, non-coupling and coupling core structures have the same AC fluxes in all the legs. If the two core

structures are designed to have the same transient equivalent inductances, the DC fluxes in all the legs are the same, too.

The previous identity results of the DC fluxes in the non-coupling and coupling core structures are based on the assumption that the average currents in the two interleaving channels are the same ($I_1=I_2=I$). This assumption might not be true in real converters without active current-sharing control. The unequal DC currents in the two channels affect the DC fluxes in the cores.

Assume the DC currents in the two channels have a difference of ΔI ($I_1=I_2+\Delta I$ and $\Delta I>0$). For the non-coupling core structure, the DC flux difference in the two outer legs is as follows:

$$\Delta\Phi_{nc} = \Phi_1 - \Phi_2 = \frac{L_{eq2} \cdot \Delta I}{N}. \tag{4.29}$$

For the coupling core structure, the DC flux difference in the two outer legs is as follows:

$$\Delta\Phi_{cp} = \frac{(L_{cp} - M) \cdot \Delta I}{N} = \frac{L_{eq2} \cdot \Delta I}{N} \cdot \frac{1-\alpha}{1+\alpha}. \tag{4.30}$$

For inverse coupling inductors, because $\alpha<0$, there exists $\Delta\Phi_{cp}>\Delta\Phi_{nc}$. For stronger coupling effects, the DC flux differences in the two outer legs are larger. This is the disadvantage of the inverse coupling core structure. This problem can be avoided by using current-sharing control between the two channels. It should be noted that the unequal DC current in the two windings does not affect the DC flux bias in the center leg in either the coupling or the non-coupling core structures.

The preceding analysis compares the AC and DC fluxes in the three legs of the coupling and non-coupling core structures, based on the magnetic reluctance

circuit model. It provides general guidance for the design of magnetic components. However, the losses in the magnetic materials are more directly related to the flux density. A section of core can have the same flux but different flux distribution, which can result in different core losses. The magnetic reluctance circuit model only gives the total fluxes; it cannot give the flux distribution in the core. In different core structures, the flux distribution can be very different even though the total fluxes are the same. The following discussion uses finite element analysis (FEA) simulation tools (Maxwell 2D field simulator from Ansoft Inc.) to analyze the flux distribution in the coupling and non-coupling core structures.

In order to make the FEA results meaningful, the simulation models need to be defined carefully. PCB windings are assumed in the simulations. The core and winding arrangements are shown in Fig. 4.4. The dimensions of the E-I cores are based on the E18/4/10 and the PLT 18/10/2 from Philips. The thicknesses of the windings are four-ounce PCB. The thicknesses of the isolations between the two layers are 1.0mm. In the different coupling structures under simulation, the total profiles of the inductors are kept the same, 6.0mm. Due to a limitation of the software, the winding currents can only be sinusoidal waves, while in real circuits the winding currents are triangle waves. The frequency of the sinusoidal waves in the simulation is 300kHz.

The design of the core structures under simulation are based on the same transient equivalent inductance (about 315nH in each channel). The reluctances of the cores are ignored. For the non-coupling core structure, the air gap in the outer leg can be easily derived, as follows:

$$l_{nc\_1} = \mu_0 \cdot A_1 \cdot \frac{N^2}{L_{nc}}, \tag{4.31}$$

where A_1 is the cross-section area of the outer leg, and l_{nc_1} is the air gap in the outer leg. Based on the inductance, the air gaps in the outer legs can be calculated (l_{nc_1}=0.32mm).

For the specific core used in the simulations, the cross-section area of the center leg is twice that of the outer legs. In the cases for which the transient equivalent inductances are the same, the relationship between the air gaps in the non-coupling and coupling structures can be found, as follows:

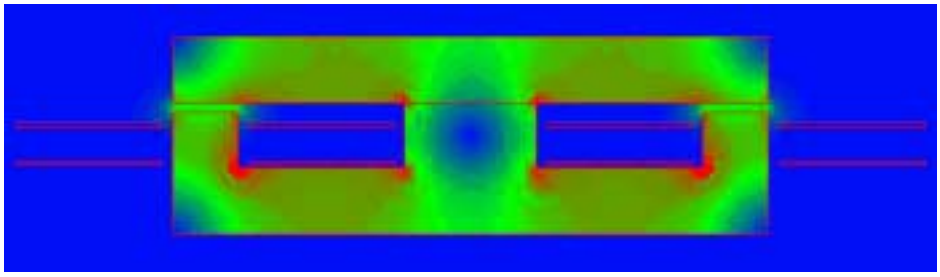
$$l_{cp\_1} + l_{cp\_c} = l_{nc\_1}, \tag{4.32}$$

where l_{cp_1} and l_{cp_c} are the air gaps in the outer and center legs of the coupling core structure, respectively. The coupling effect α can also be rewritten in the format of the air gaps, as follows:

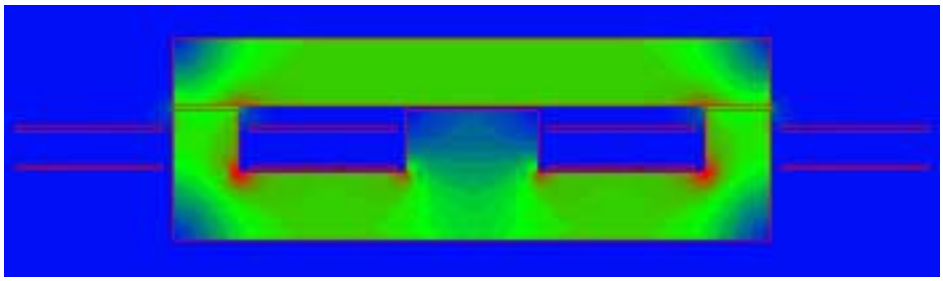
$$\alpha = \frac{l_{cp\_c}}{2 \cdot l_{cp\_1} + l_{cp\_c}}. \tag{4.33}$$

Based on the preceding discussions, the simulation model can be determined. Because the software is a two-dimensional field simulator, the dimension perpendicular to the paper is assumed to be infinite.

The FEA results of the AC flux distribution in the non-coupling and coupling core structures are shown in Fig. 4.23(a) and (b), respectively. In the two simulation cases, the air gaps follow $l_{cp_1}+l_{cp_c}=l_{nc_1}\equiv$0.32mm. As discussed previously, the AC fluxes in all three legs in the non-coupling and coupling core structures are the same. The AC flux in the center leg is the sum of the AC fluxes in the two outer legs. Due to the phase shift between the two channels, the total AC fluxes in the center legs are zero for both non-coupling and coupling core structures. However, zero total AC flux does not mean zero AC flux density throughout the whole center leg.



(a)



(b)

Fig. 4.23. Different AC flux distributions in the cores: (a) non-coupling; and (b) inverse coupling

The center leg in the non-coupling core structure is a low-reluctance path. The AC fluxes generated by the two outer legs are unwilling to disperse through the cross section of the center leg. Thus, the AC flux cancellation is not very effective in non-coupling core structures. Although the average AC flux is zero in the center leg, there are still flux-crowded areas, as shown in Fig. 4.23(a), which cause core losses. For the coupling core structure, the center leg is a high-reluctance path, which forces the AC flux to distribute more evenly through the cross section of the center leg. Thus, the AC flux cancellation is more effective in the coupling core structure, which further reduces the core losses in the center leg.

In real circuits, the winding currents are triangle waves. The AC flux in the center leg is triangle wave at the double switching frequency, as shown in Fig. 4.3. The center leg core losses in the inverse coupling core structure are still smaller than those in the non-coupling cores, because the reluctance in the center leg makes the flux ripple cancellation more effective.

From (4.32), in the cases in which the transient equivalent inductances are kept the same, the coupling core structure moves part of the air gap from the outer leg to the center leg, while keeping the total air gap constant. The greater the percentage of air gap that is moved to the center leg, the stronger are the corresponding coupling effects. Large air gaps usually associated with fringing effects and EMI problems. In conventional inductor designs, smaller evenly distributed air gaps can reduce the fringe effects and improve inductor performance. In this sense, the coupling core structure would have smaller fringing effects and fewer EMI problems.

Moreover, the flux ripples in the outer leg are much larger than those in the center leg. The AC flux through the air gap in the center leg is much smaller. The fringing effects associated with the center leg air gap are much smaller, as shown in Fig. 4.23. Stronger coupling effects result in smaller air gaps in the outer legs and smaller fringing effects. The fringing effects generate eddy currents in the windings, which cause extra conduction losses.

The Maxwell 2D field simulator also provides the current distribution in the windings. The winding current distribution from FEA is shown in Fig. 4.24.

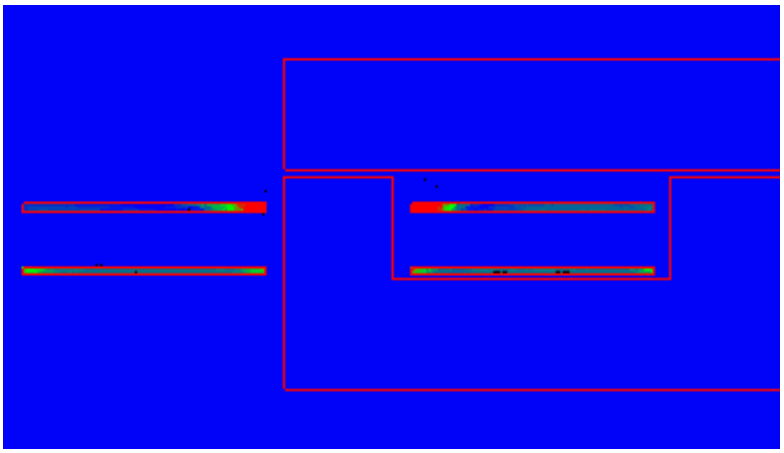


Fig. 4.24. Winding current distribution of inverse coupling structure.

Because the left and right halves of the core and winding structures are symmetric, only the left half is shown in the figure. The air gap in the outer leg generates eddy currents in the top-layer PCB windings. Because of the small amount of AC flux in the center leg, the air gap in the center leg does not cause much eddy current.

The eddy currents in the windings cause additional winding conduction losses, which are indicative of the fringing effects of the cores. The winding conduction losses of different coupling effects are shown in Fig. 4.25.

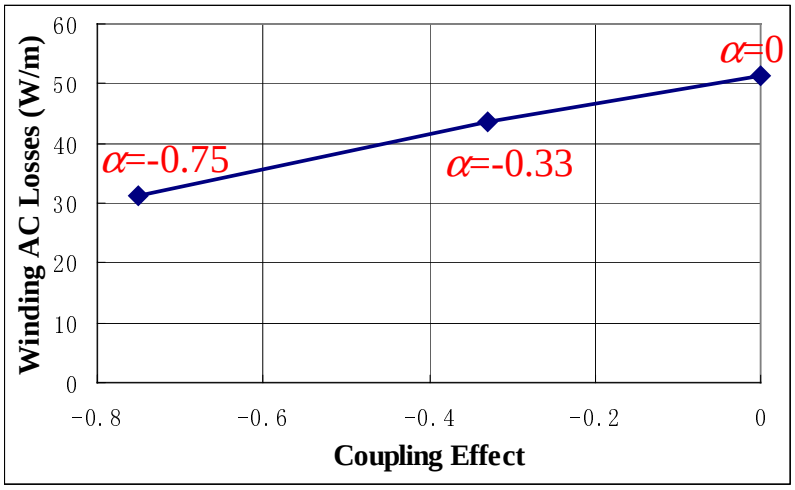


Fig. 4.25. Inverse coupling reduces winding conduction losses (same AC current).

For the three cases in Fig. 4.26, the equivalent inductances are kept the same. The overall profiles of the cores are the same (6.0mm). The coupling effect $\alpha=0$ represents the non-coupling core structure. The point of $\alpha=0.33$ corresponds to the case in which the air gaps in the three legs are the same. For each case in the figure, the same 7A, 300kHz sinusoidal winding current waveform is used. The winding AC conduction losses decrease as the coupling effects increase. The conduction losses are reduced because of the smaller outer leg air gaps in coupling core structures. The fringing effects in coupling core structures are less severe.

Of course, it is not reasonable to use the same AC current waveforms because the main purpose of the coupling inductor is to reduce the current ripples in the windings. If the winding current ripple reduction effects shown in Fig. 4.17 are considered, the AC conduction losses in the windings can be further reduced in coupling core structures, as shown in Fig. 4.26. The different conduction losses occur mainly in the top-layer windings. The current distributions in the bottom-layer windings are almost the same for different core structures.

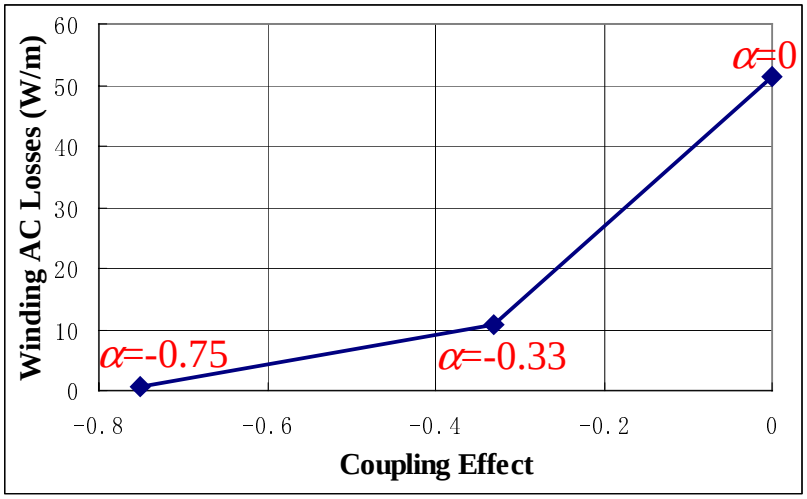


Fig. 4.26. Inverse coupling reduces winding conduction losses (AC current magnitude based on Fig. 4.18).

Of course, the placements of the windings have important effects on the winding AC conduction losses. In the preceding comparisons, the same winding structures are used in the non-coupling and coupling core structures. If different winding structures are considered, the result could be different.

In this section, the designs of the coupling and non-coupling core structures are compared. If the two structures are designed to have the same transient equivalent inductance, the total AC and DC fluxes in the three legs will be the same. Stronger inverse coupling effects between the two channels result in smaller steady-state current ripples. Due to the high reluctance in the center leg of

the coupling core structure, the AC flux in the center leg is more effectively cancelled, which reduces the core losses. The coupling core structure has smaller air gaps in the outer legs. The fringing effects in the coupling core structures are much smaller, which result in smaller current conduction losses in the windings. The disadvantage of the inverse coupling core structure is that unbalanced DC currents in the two channels result in more severe DC flux imbalance in the cores.

4.5 Hardware Setup and Experimental Results

The preceding analysis and simulation results show that inverse coupling inductors can improve the performances of VRMs. Hardware is built in order to verify the benefits of the coupling inductor concept. The two converters under comparison are a four-channel interleaving buck VRM with non-coupling integrated inductors and a four-channel interleaving buck VRM with inverse coupling inductors.

As discussed previously, the designs with the same transient equivalent inductance have the most similar circuits for the two cases. The only difference between the two cases under comparison is the air gap in the center leg. Actually, there is only one set of circuit board and controller. The cores in the converter are changeable. For the comparison experiments, only the cores in the circuit are changed. The circuit layout is shown in Fig. 4.27.

Two pairs of E-I cores are used in the four-channel interleaving synchronous buck VRM. The two channels with phase shifts of 0^o and 180^o share a pair of cores, while the other two channels with phase shifts of 90^o and 270^o share another pair of cores. The cores used are E18/4/10 and PLT 18/10/2 cores from Philips. The materials for all the cores are 3F3. Each inductor has two turns of

winding. The windings are built on the two sides of the PCB, as shown in Fig. 4.4 and 4.23.

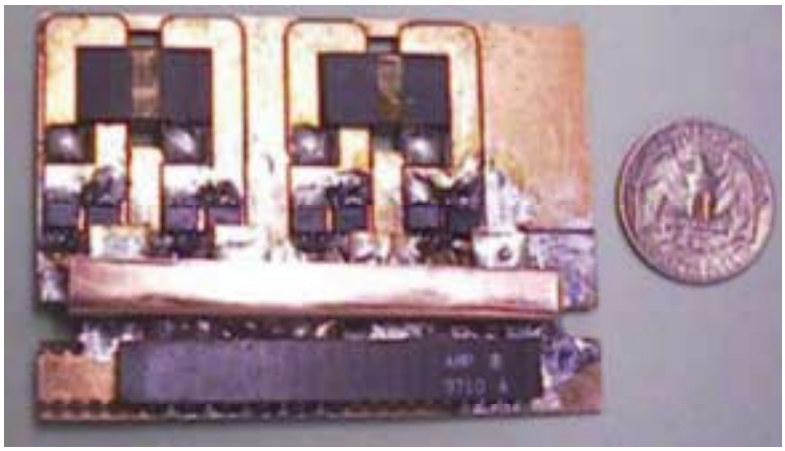


Fig. 4.27. Hardware under comparison is a four-channel interleaving buck VRM.

The circuit operation condition is Fs=300kHz, Vin=5V, Vo=2V and Io=30A. The switches used in the circuit are Si4410 MOSFETs from Siliconix Inc. Each top and bottom switch in each of the four interleaving channels uses one MOSFET, so there are eight MOSFETs in all. The output capacitors consist of two 470μF Tantalum capacitors and twenty-six 10μF ceramic capacitors.

For the non-coupling case, the inductance in each channel is about 320nH. The two outer legs of the E core need to be milled to generate the air gaps. For the coupling case, the air gaps in the three legs are the same because this is the simplest implementation. The coupling effect is α=-1/3. The self-inductance in the inverse coupling core structure is 480nH.

As shown in Fig. 4.17, the steady-state peak-to-peak current can be reduced to below 60%. The RMS currents in the inverse coupling inductors are about 82% of those in the non-coupling inductors. At full load, the conduction losses in the MOSFETs can be reduced by about 1.1W, which corresponds to about 1.4% improvement in efficiency. Moreover, due to the reduction of the peak currents,

the turn-off losses of the top MOSFETs can also be greatly reduced. The reduction in core and winding losses would also improve overall efficiency. The overall efficiency improvement is expected to be about 2% at full load.

The transient waveforms are shown in Fig. 4.28. Because of the same transient equivalent inductances and the same controller, the non-coupling and inverse coupling inductors have the same transient voltage spikes.

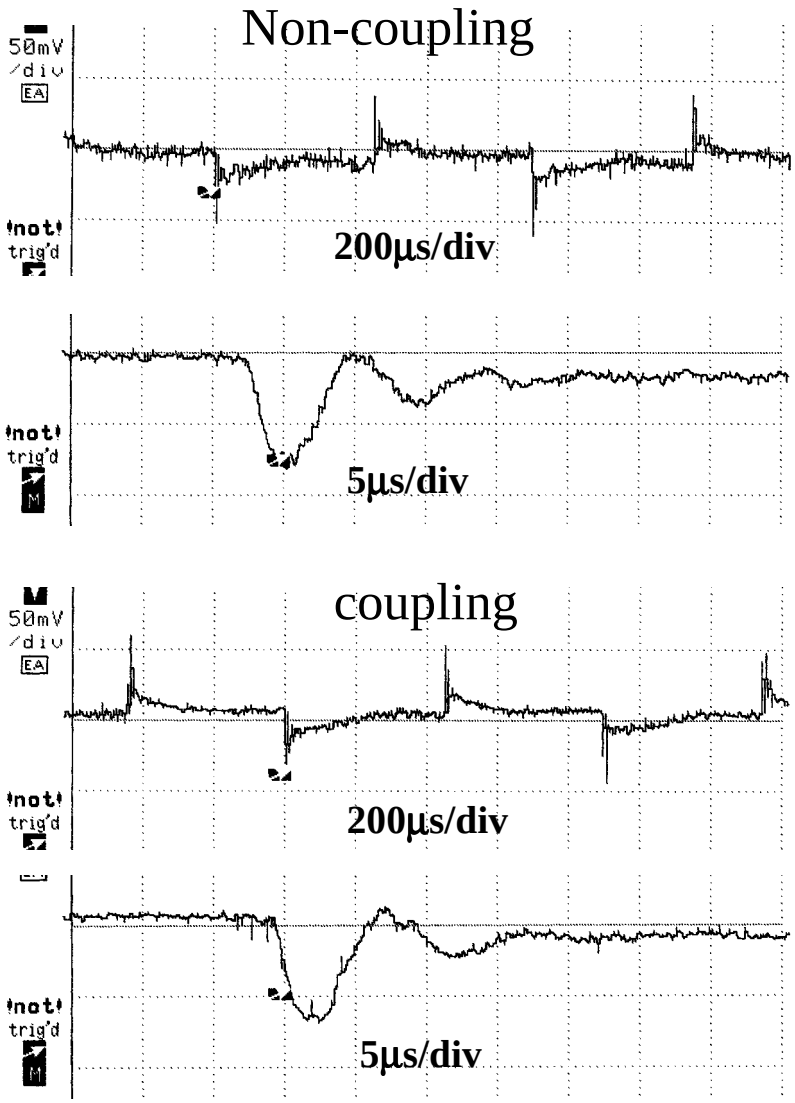


Fig. 4.28. Non-coupling and coupling inductors have same transient responses.

The efficiency comparison is shown in Fig. 4.29. Compared with the non-coupling inductors, the inverse coupling inductors improve the efficiency by about 2% at full load and about 10% at light load.

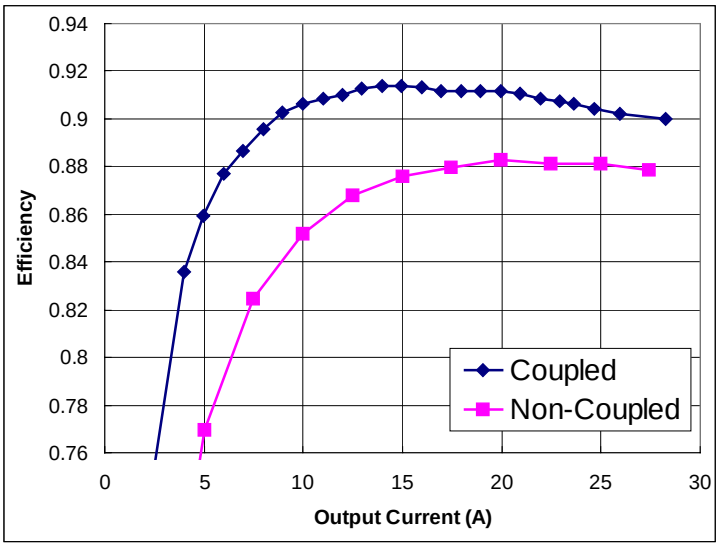


Fig. 4.29. Inverse coupling inductors improve efficiency.

The winding and core temperature comparisons are shown in Fig. 4.30. Due to the lower losses in the coupling inductors, both the core and winding temperatures are reduced by about 5^{o}C. All the experimental data are obtained under the same conditions, i.e., room temperature without fan cooling. The on-resistances of the MOSFETs increase with the junction temperatures. Lower temperature increases are also a factor in the efficiency improvements.

The experimental results show that the inverse coupling inductors greatly improve the efficiency without compromising the transient responses. The core structure is even easier to manufacture in the inverse coupling inductors.

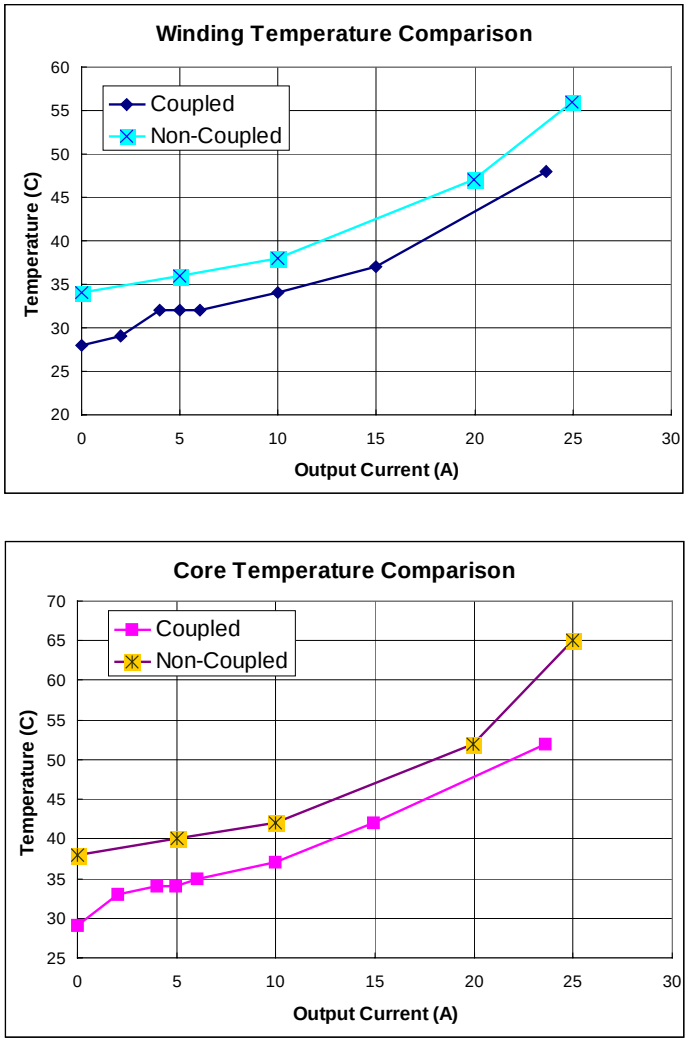


Fig. 4.30. Inverse coupling inductors reduce the winding and core temperature increases because of efficiency improvements.

4.6 Summary

This chapter presents and analyzes the concept of applying coupling inductors between the interleaving channels with 180^{o} phase shift. Coupling inductors have different equivalent inductances for steady-state and transient responses. Inverse coupling inductors between the interleaving channels reduce the steady-state

current ripples while maintaining the same transient responses. Both the conduction and switching losses of the MOSFETs can be reduced because of small current ripples in inverse coupling inductors. The air gap in the center leg of coupling cores more evenly distributes the flux, which reduces the core loss in the center leg. The smaller air gaps in the outer legs of the coupling core structure also alleviate the EMI and fringing effects of the inductor structures, which reduces the conduction losses in the windings. Experimental results show that the efficiency improvement due to inverse coupling inductors is about 2% at full loads and 10% at light loads. Moreover, the coupling inductor core structures make the manufacture of the cores easier and improve the mechanical stability of the cores.

Chapter 5

Flux Source Reluctance Model for Multi-Coupling Inductors

The previous chapter shows that inverse coupling inductors between the two channels with a 180^o phase shift improves both the steady-state and dynamic performances of the interleaving VRMs. However, the complicated electric circuit model for the multi-coupling core structures prevents the coupling concept from being extended to integrated multi-channel core structures. This chapter presents a circuit model that can be easily applied to different complicated multi-coupling core structures. The model is based on the flux source magnetic reluctance model. Compared to conventional modeling methods, the proposed method involves fewer inductors, and is more directly related to the physical core structures. The parameters involved in the model have clear physical meanings. Simpler computation is required for the model simulation.

5.1 Motivation

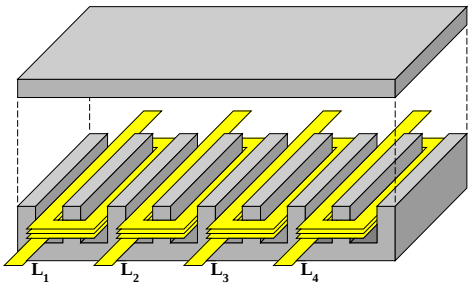
In Chapter 4, the inverse coupling inductors applied to the two channels with a 180^o phase shift reduce the steady-state current ripples while maintaining dynamic performance. The core losses and winding losses can also be reduced in coupling inductors. The core structure of the coupling inductors is even more stable and is easier to manufacture. The benefits of the coupling inductors are attractive.

In VRM design, the channel number depends on the optimization tradeoffs of efficiency, cost, etc. For increasing current ratings, more interleaving channels become preferable in VRMs. The channel number does not necessarily have to be an even number; there are commercially available control chips for three-channel interleaving VRMs. When the interleaving channels are odd numbers, there are no two channels with the 180^o phase shift in the circuit. The preceding analysis of the coupling inductors is no longer valid.

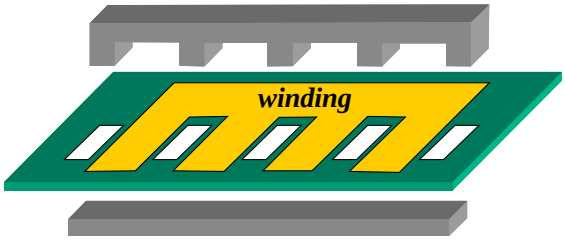
Moreover, in order to simplify the implementation and increase the power density of multi-channel interleaving VRMs, integration of more inductors in a single magnetic component is preferred. Because of the high frequencies of VRMs, the inductances required are very small. Integration of inductors is attractive and practical. Quite a few ideas have been proposed for integrating all the inductors in a VRM into a single pair of cores or a single magnetic layer. Some of these concepts are shown in Fig. 5.1.

In these methods, the implementation of the inductors is simplified. The parameters of the inductors can be easily controlled to be symmetric. The inductor size can also be reduced to achieve high power density.

Despite these attractions, a common issue in the proposed structures involves the coupling effects among the inductors. Because all the inductors share the same magnetic core or layer, the fluxes generated by the wires would have interactions, which result in the coupling effects. As shown in Chapter 4, the coupling effects are not necessarily a drawback. Proper design of the coupling effects could improve both the steady-state and transient responses of VRMs. The problem is that the coupling effects among multiple inductors are much more complicated than those between two inductors. It is unlikely that analytical formulas can be derived for the multi-coupling inductors to predict the steady-state and transient performances of the converter, as is done for the two channel coupling inductors.



(a)



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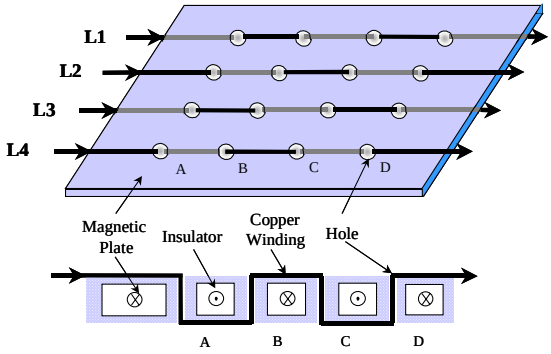
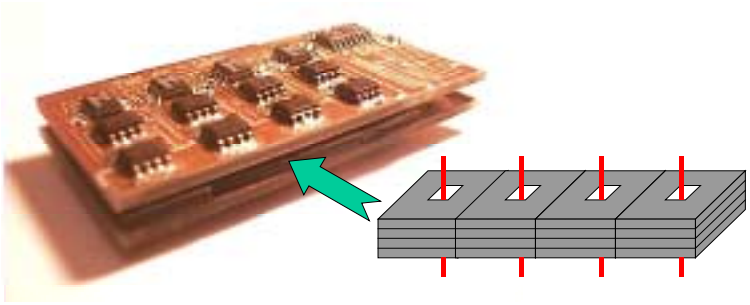


(c)



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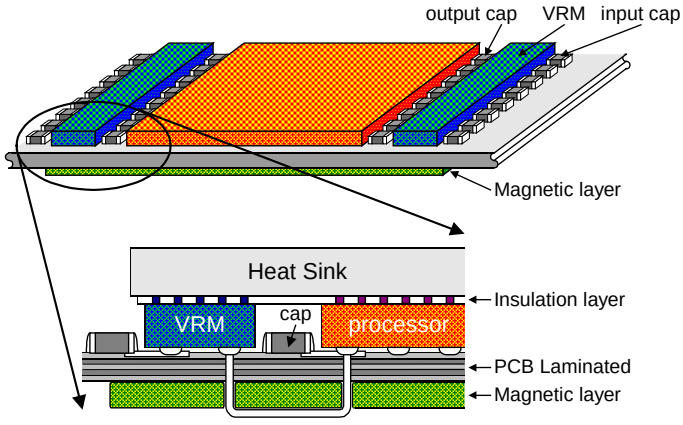


(e)

Fig. 5.1. Some integrated inductor ideas for multi-channel interleaving VRMs.

It is more reasonable to derive a general circuit model for the multi-coupling core structures that can be used in circuit simulation software. The steady-state and transient performances of the converter can be predicted from simulation results.

The review of existing magnetic models shows that the complexity of the existing models increases dramatically as the coupling inductor number increases. This complexity usually results in converging problems in circuit simulations. Moreover, the parameters in the existing models are usually difficult to derive and lack clear physical meanings. It is time-consuming to build a circuit simulation model for different coupling core structures. Because of the difficulties of the existing magnetic models, the operation of different multi-coupling core structures cannot be comprehensively studied or evaluated. This prevents the concept of coupling inductors from extending to multi-channel coupling inductor structures.

This chapter presents a new concept for magnetic simulation circuit modeling in order to solve the associated problems. The proposed model is based on magnetic reluctance models. Compared to existing models, the proposed model involves simpler computation in simulations, so converging problems are unlikely. The parameters in the model have clear physical meanings. Additionally, the circuit simulation model can be easily derived from the magnetic reluctance circuit.

5.2 Review of Existing Methods

The circuit model of the integrated multi-channel coupling core structures is similar to that of the multi-winding transformers, unless the leakage inductance in the transformers is much smaller than the magnetizing inductance. The

magnetizing inductance in transformers is the coupling inductance in coupling inductor structures. Modeling the multi-winding transformer is an extensively researched area. This section reviews the existing methods.

For two-winding transformers, the π-model is the most commonly used. For two-channel coupling inductors, the π-model can be easily applied, as shown in Fig. 4.7. The corresponding differential equation matrix of (4.2) can be rewritten as follows:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix}. \tag{5.1}$$

The π-model is perfect for the two coupling inductors. In order to extend it for general cases, (5.1) needs to be expanded to an n-by-n inductance matrix for n coupling inductors, as follows:

$$\begin{bmatrix} v_1 \\ v_2 \\ \vdots \\ v_n \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} & \cdots & L_{1n} \\ L_{21} & L_{22} & \cdots & L_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ L_{n1} & L_{n2} & \cdots & L_{nn} \end{bmatrix} \cdot \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \end{bmatrix}. \tag{5.2}$$

The inductance L_{ii} represents the self-inductance, while L_{ij} represents the coupling inductance between the *i*-th and *j*-th inductors. There exists $L_{ij}=L_{ji}$. In the inductance matrix, there are $\frac{n\cdot(n+1)}{2}$ independent variables. The π-model requires $\frac{n\cdot(n+1)}{2}$ inductors to describe *n* inter-coupled inductors.

In circuit simulations, the inductors' voltage waveforms, v_i, are usually known due to the switching actions and the inductor current waveforms, i_i, need to be solved. In order to determine the current waveforms, the inverse transformation of the inductance matrix needs to be solved. With the increase of *n*, the complexity

of the inverse transformation of the inductance matrix increases greatly. This is the main reason for the complexity in this model.

Usually, the reluctance model of the core structure can be easily derived from the geometry of the cores. The magnetic reluctance model of the core and winding structure in Fig. 5.1(b) is shown in Fig. 5.2.

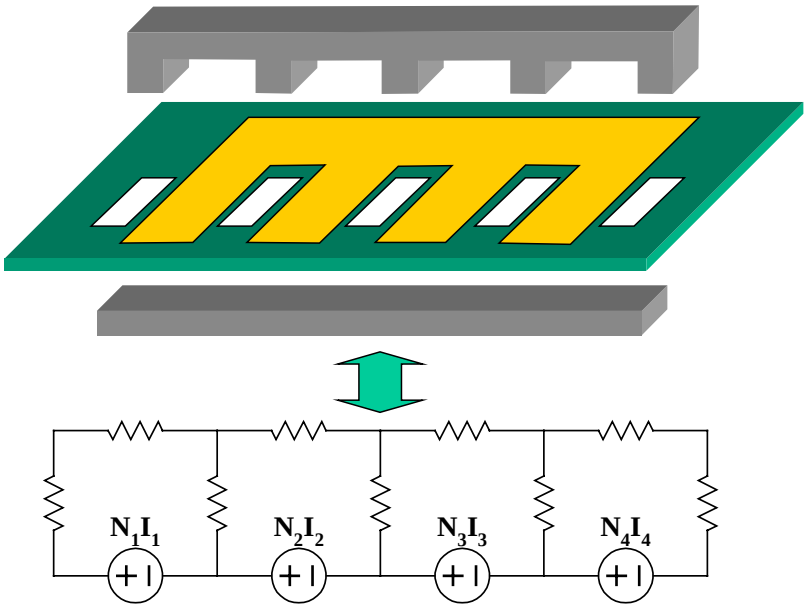


Fig. 5.2. Magnetic reluctance model can be easily derived from core structure.

The reluctance model consists of two parts: the reluctances in the flux paths, and the representation of the windings. Conventionally, the windings are represented as MMF sources, which are the products of the currents and turns of the windings. The characteristics of the MMF sources in magnetic reluctance circuits are similar to those of the voltage sources in electric circuits. The fluxes in magnetic circuits are similar to the currents in electric circuits.

The magnetic reluctances are similar to the resistors in electric circuits. The reluctances are determined by the core geometry and the permeability of the materials. The magnetic reluctance circuit can be easily derived. However, the inductances in (5.2) are not directly related to the reluctance model, so the

parameters are usually difficult to derive. This is another disadvantage of the extended π-model.

There are some models that derive the electric simulation circuits from the magnetic reluctance circuit. These methods involve the use of controlled current sources and duality transformations between the magnetic and electric circuits. However, for complex core structures, these models are usually labor-intensive and have a high probability for errors. The controlled sources or the ideal transformers in the model are likely to cause converging problems in circuit simulation.

Another method directly includes the magnetic reluctance model in the electric circuit simulations. An interface between the magnetic and electric circuits is required to transfer the parameters between the two, as shown in Fig. 5.3.

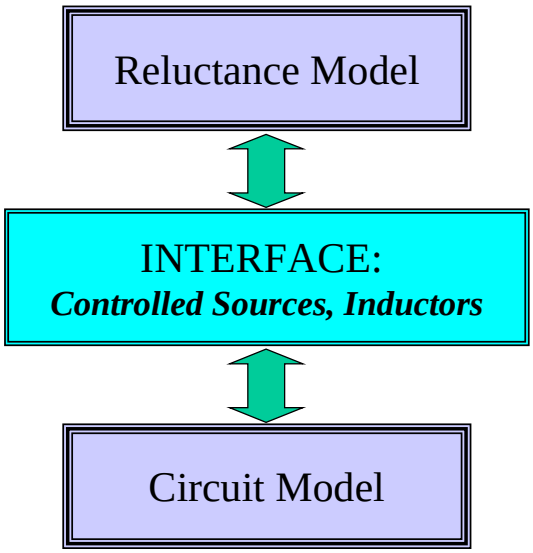


Fig. 5.3. Including the reluctance model in circuit simulation.

The interface relates the currents and voltages in the electric circuit with the fluxes and MMFs in the magnetic reluctance model. Although the concept of the interface is simple, its implementation involves current-controlled current sources,

current-controlled voltage sources, and inductors. The complexity of the interface results in time-consuming simulations as well as converging problems.

The review of the existing modeling methods shows that they all have defects, such as complexity, converging problems in simulation, or difficulties in model derivation and explanation. In order to find a proper modeling method for multi-channel coupling inductor structures, this chapter starts with a different magnetic reluctance model and proposes a novel simulation circuit model for multi-coupling inductors.

5.3 Concept of the Proposed Method

In the conventional magnetic reluctance model, the windings are represented as the MMF sources, as shown in Fig. 5.2. From another point of view, the voltages applied to the windings are also the parameters that can represent the windings. According to Faraday's Law, the winding volt-seconds determine the flux in the corresponding core leg, as shown in (5.3) and (5.4):

$$N \cdot \phi = \int v \cdot dt \quad \text{and} \tag{5.3}$$

$$v = N \cdot \frac{d\phi}{dt}. \tag{5.4}$$

If the volt-seconds of the windings are known, the flux in the corresponding core is determined. The windings can also be represented as the flux sources in the magnetic reluctance model. The values of the flux sources are the volt-seconds of the windings. To distinguish this reluctance model from the conventional magnetic reluctance model, this one is named the flux source reluctance model while the conventional model is the MMF source reluctance model.

The two reluctance models are equivalent. For the MMF source model, the MMFs are the known parameters, and the fluxes in the branches need to be obtained. For the flux source model, the fluxes in the branches are the known parameters, and the MMFs of the loops need to be determined. The reluctance model of the core structure shown in Fig. 5.2 is redrawn in Fig. 5.4.

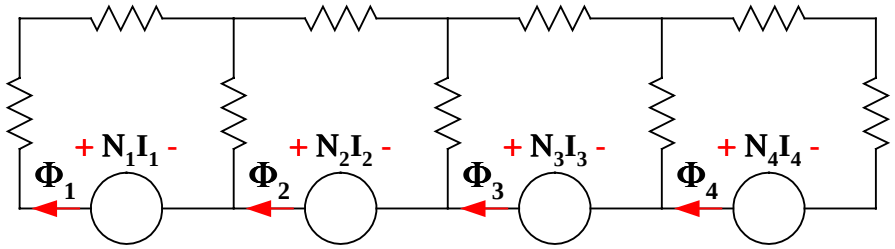


Fig. 5.4. Windings represented as unknown components in the reluctance model.

In Fig. 5.4, the windings are represented as circles with unknown parameters. If the MMFs of the windings are known, the windings can be represented as MMF sources. By solving the network of the model, the fluxes in the windings can be found. If the fluxes of the windings are known, the windings can be represented as flux sources. The MMF of the winding can be found by solving the network. The relationship between the MMFs and fluxes in the windings can be generally described as follows:

$$\begin{bmatrix} N_1 \cdot I_1 \\ N_2 \cdot I_2 \\ \vdots \\ N_2 \cdot I_n \end{bmatrix} = [R] \cdot \begin{bmatrix} \phi_1 \\ \phi_2 \\ \vdots \\ \phi_n \end{bmatrix}, \tag{5.5}$$

where the reluctance matrix **[*R*]** represents the network of the reluctance model.

From (5.5), only one set of sources (either MMF sources or flux sources) is required for the reluctance model to determine the MMF and flux in every winding. The two sets of sources are interchangeable. In this sense, the windings can be represented either as MMF sources or as flux sources. The transformation

does not result in any difference in the network. Fig. 5.5 is the flux source reluctance model for the core structure shown in Fig. 5.2.

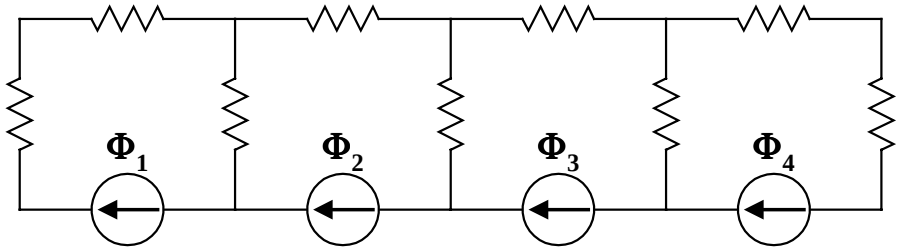


Fig. 5.5. Flux source reluctance model of core structure in Fig. 5.2.

In the electric circuit, the difference between the voltage sources and the current sources is that the voltage sources are short circuits while the current sources are open circuits. Because of the analogy between the electric and magnetic circuits, the flux sources can be considered open circuits, while the MMF sources need to be considered short circuits.

For the MMF source model, in order to see the effect of one winding on the rest of the circuit, the other windings must be short-circuited as shown in Fig. 5.6. If the windings are represented as MMF sources, all the windings are coupled together.

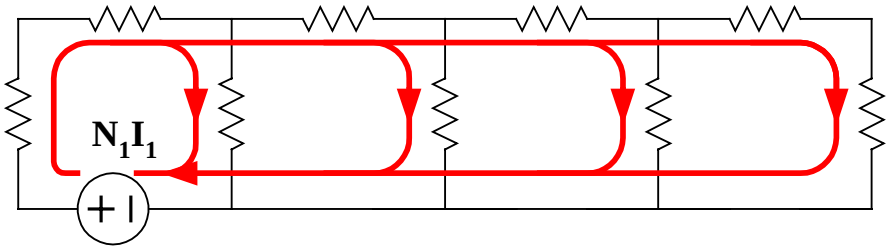


Fig. 5.6. All the windings are coupled in MMF source reluctance model.

In the flux source reluctance model, the open circuits of the flux sources basically break up the loops in the circuit. The flux in the loop is only determined by the flux source in the loop. For the branches that are involved in two loops, the

branch flux is simply the sum of the two loop fluxes. Accordingly, the MMF of the reluctance can also be determined easily. The MMF source reluctance circuit can be divided into cells, as shown in Fig. 5.7.

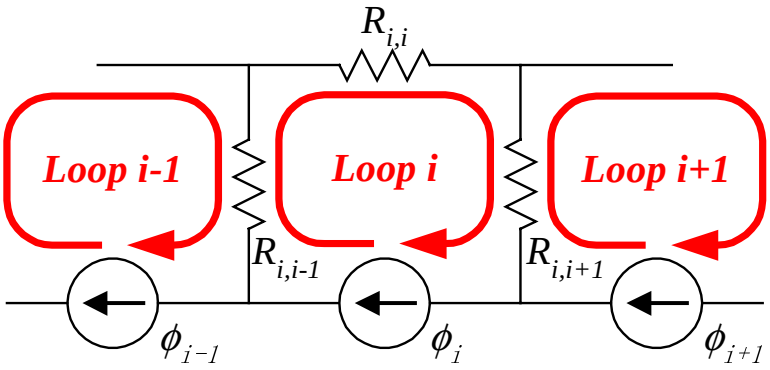


Fig. 5.7. A general cell in the flux source reluctance model.

Because of the open circuits of the flux sources, the different loops in the magnetic reluctance model can be decoupled. This makes the flux source reluctance model much simpler than the MMF source reluctance models when a large number of windings are considered.

From Fig. 5.7, the MMF of the winding (represented as flux source ϕ_i in the figure) can be described as follows:

$$N_i \cdot i_i = (R_{i,i-1} + R_{i,i} + R_{i,i+1}) \cdot \phi_i - R_{i,i-1} \cdot \phi_{i-1} - R_{i,i+1} \cdot \phi_{i+1}. \tag{5.6}$$

The sum of the reluctances in *Loop i*, $R_i = \sum_j R_{i,j} = (R_{i,i-1} + R_{i,i} + R_{i,i+1})$, is defined the self-reluctance of the loop. The reluctance involved in both *Loop i* and *j*, R_{ij}, is defined as the mutual reluctance between these two loops.

As shown in (5.6), the MMF can be divided into two parts: the self-MMF, which is generated by flux ϕ_i through the self-reluctance of the loop, and the mutual MMF, which is generated by fluxes other than ϕ_i, through the corresponding mutual-reluctances.

The differentiation of (5.6) is (5.7):

$$N_i \cdot \frac{d}{dt} i_i = R_i \cdot \frac{d}{dt} \phi_i - R_{i,i-1} \cdot \frac{d}{dt} \phi_{i-1} - R_{i,i+1} \cdot \frac{d}{dt} \phi_{i+1} . \tag{5.7}$$

Substituting (5.4) into (5.7) results in (5.8):

$$\frac{di_i}{dt} = \frac{R_i}{N_i^{\,2}} \cdot v_i - \frac{R_{i,i-1}}{N_i \cdot N_{i-1}} \cdot v_{i-1} - \frac{R_{i,i+1}}{N_i \cdot N_{i+1}} \cdot v_{i+1} , \tag{5.8}$$

where current i_i represents the current going through winding i.

In order to simplify (5.8) and derive the simulation circuit model, different inductances are defined as follows:

$$\begin{cases} L_{i,i} = \dfrac{N_i^2}{R_i} = \dfrac{N_i^2}{\sum_j R_{i,j}} & self-inductance \\ L_{i,j} = \dfrac{N_i \cdot N_j}{R_{i,j}} & mutual-inductance \end{cases} \tag{5.9}$$

The inductance $L_{i,i}$ is defined as the self-inductance of *Loop i*, which corresponds to the self-reluctance R_i of *Loop i*. The inductance $L_{i,j}$ is defined as the mutual inductance between *Loop i* and *j*, which corresponds to the mutual reluctance $R_{i,j}$ between the two loops. The polarity of the mutual inductance is determined by the relative flux directions between the two loops. For the loop flux direction defined in Fig. 5.7, the mutual inductance $L_{i,j}$ is negative. All these inductances can be directly derived from the magnetic reluctances shown in the figure.

With the definitions in (5.9), (5.8) can be simplified as follows:

$$\frac{di_i}{dt} = \frac{1}{L_{i,i}} \cdot v_i + \frac{1}{L_{i,i-1}} \cdot v_{i-1} + \frac{1}{L_{i,i+1}} \cdot v_{i+1} . \tag{5.10}$$

The current through a winding can be divided into two parts: the self-current, which is the first term in (5.10), and the mutual (or coupling) currents, which is the rest of the terms in (5.10). The definitions of self-current and mutual current are as follows:

$$\begin{cases} i_{i,i} = \dfrac{\int v_i \cdot dt}{L_{i,i}} & self-current \\ i_{i,j} = \dfrac{\int v_j \cdot dt}{L_{i,j}} & mutual-current \end{cases} . \tag{5.11}$$

Using these definitions, (5.10) can be rewritten as follows:

$$\frac{di_i}{dt} = \frac{d}{dt} i_{i,i} + \sum_j \frac{d}{dt} i_{i,j} . \tag{5.12}$$

The integral format of (5.12) gives the currents in each winding, as follows:

$$i_i = i_{i,i} + \sum_j i_{i,j} . \tag{5.13}$$

From (5.11), the winding volt-seconds (or the flux source in the loop) and the self-inductance of the corresponding loop determine the self-current in the winding. The self-current is the decoupled part of the winding current; tt has nothing to do with the volt-seconds applied to the other windings. The mutual currents are determined by the volt-seconds on the other windings and the corresponding mutual inductances. The mutual currents are the coupling effects among different windings. In the specific core and winding structure shown in Fig. 5.2, the mutual currents have only two parts that correspond to the two adjacent windings.

From another viewpoint, the volt-seconds applied to a certain winding not only generate the self-current in this winding, but also generate the mutual

currents in the other windings. The mutual- and self-currents generated by the same volt-seconds have waveforms proportional to each other. This waveform is also the flux source waveform in the loop. The mutual-current waveforms can be described as the self-current waveform generated by the same voltage with a proportional coefficient.

Formula (5.11) can be rewritten in another format, as shown in (5.14):

$$\begin{cases} i_{j,j} = \dfrac{\int v_j \cdot dt}{L_{j,j}} \\ i_{i,j} = \dfrac{\int v_j \cdot dt}{L_{i,j}} \end{cases}. \tag{5.14}$$

The difference between (5.11) and (5.14) is that the self-current and mutual current defined in (5.11) are the currents in the same winding, but are generated by different volt-seconds, while the self-current and mutual current in (5.14) are the currents generated by the same winding voltage. The currents in (5.14) have similar waveforms because they are all determined by $\int v_j \cdot dt$. The coefficients among the current waveforms can be represented as the ratios among corresponding inductances, as follows:

$$\alpha_{i,j} = \frac{i_{i,j}}{i_{j,j}} = \frac{L_{j,j}}{L_{i,j}} = \frac{R_{i,j}}{R_j} \cdot \frac{N_j}{N_i}. \tag{5.15}$$

The coefficients $\alpha_{i,j}$ represent the coupling effects, which have a meaning similar to the definition given in Chapter 4. If the inductors have same turn number, there exists ($-1 \le \alpha_{i,j} \le 1$), because ($R_{i,j}<R_j$), which is the case discussed in Chapter 4. It should be noted that if different turn numbers are considered, the coupling coefficients $\alpha_{i,j}$ can be larger than 1.

The coefficients $\alpha_{i,j}$ can be easily derived from the reluctance circuit and the turn numbers.

Given the definition of the coefficients $\alpha_{i,j}$, the winding current in (5.13) can be rewritten as follows:

$$i_i = i_{i,i} + \sum_j (\alpha_{i,j} \cdot i_{j,j}) . \tag{5.16}$$

The matrix format of (5.16) follows:

$$\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \end{bmatrix} = \begin{bmatrix} 1 & \alpha_{1,2} & \cdots & \alpha_{1,n} \\ \alpha_{2,1} & 1 & \cdots & \alpha_{2,n} \\ \vdots & \vdots & \ddots & \vdots \\ \alpha_{n,1} & \alpha_{2,n} & \cdots & 1 \end{bmatrix} \cdot \begin{bmatrix} i_{1,1} \\ i_{2,2} \\ \vdots \\ i_{n,n} \end{bmatrix} = A \cdot \begin{bmatrix} i_{1,1} \\ i_{2,2} \\ \vdots \\ i_{n,n} \end{bmatrix} . \tag{5.17}$$

The winding currents can be represented as a linear transformation of the self-currents in the windings. Matrix A in (5.17) represents the linear transformation. As discussed previously, the self-current in a winding is the decoupled part of the winding current. It is determined only by the volt-seconds applied to the individual winding or the flux source in the loop. With the transformations, the multi-coupling inductors are now decoupled!

As in Fig. 5.7, the loop in the flux source reluctance model shown usually has coupling effects only with its adjacent loops. Matrix A in (5.17) is most often a loose matrix that contains zeros. The non-zero elements are generally around the diagonal. The number of the non-zero elements in Matrix A is usually proportional to *n*, while in conventional models the number of the non-zero elements in the inductance matrix shown in (5.2) is usually proportional to n^2.

With the definition of the self-current in (5.11) or (5.14), (5.17) can be written as follows:

$$\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_n \end{bmatrix} = A \cdot \begin{bmatrix} i_{1,1} \\ i_{2,2} \\ \vdots \\ i_{n,n} \end{bmatrix} = A \cdot \begin{bmatrix} \dfrac{\int v_1 \cdot dt}{L_{1,1}} \\ \dfrac{\int v_2 \cdot dt}{L_{2,2}} \\ \vdots \\ \dfrac{\int v_n \cdot dt}{L_{n,n}} \end{bmatrix}. \tag{5.18}$$

Equation (5.18) is a general expression of the electric circuit model for n-channel coupling magnetic structures. For known winding voltage waveforms, (5.18) gives the winding current waveforms. The required parameters in (5.18) are the coefficients $\alpha_{i,j}$ and the self-inductances $L_{i,i}$. All these parameters can be derived directly from the reluctance model and the winding turn numbers, solely by observation.

Comparing (5.18) and (5.2), Matrix A in (5.20) is the inverse matrix of the inductance matrix in (5.2). The elements in (5.18) are directly related to the reluctance model, while the elements of the inductance matrix in (5.2) cannot be easily related to the reluctance model.

The next step is to implement the model in circuit simulation. From (5.18), the model requires n independent inductors for n-channel coupled core structures. The elements in Matrix A, $\alpha_{i,j}$, can be represented by the controlled current sources. The simulation model for the general cell shown in Fig. 5.7 and (5.8) is shown in Fig. 5.8.

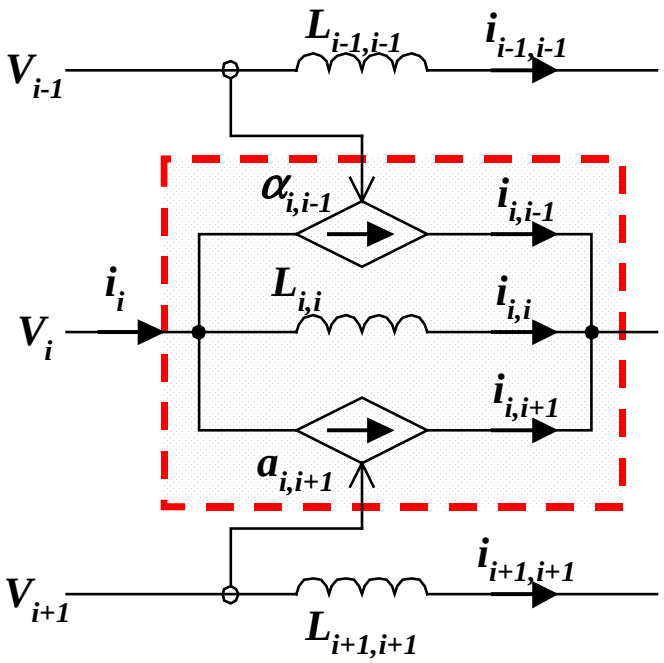


Fig. 5.8. Electric simulation circuit of the general cell.

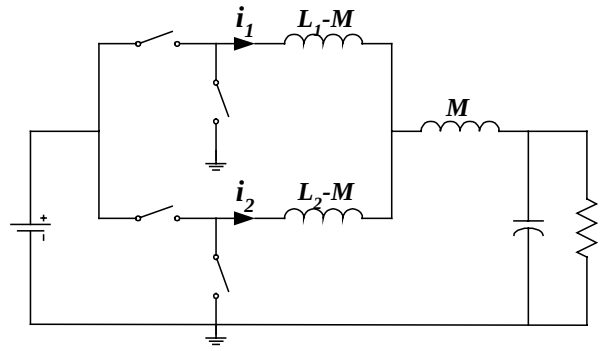
The function of the controlled current sources in Fig. 5.8 is to add up the currents in the different inductors. As will be shown in the next section, these controlled sources are not involved in circuit simulation as the controlled sources are in the conventional circuit models that are based on the MMF source reluctance model.

In physical reality, there are coupling effects among all the windings. This model has simpler expression, but the coupling effects remain. As shown in the next section, this model does result in coupling of all the windings, same as other models.

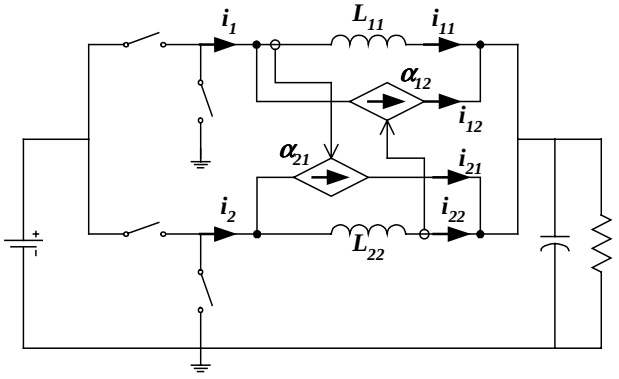
5.4 Model Verification and Simulation Results

In order to verify the validity of the proposed modeling method, simulation circuits with coupling core structures are built, based on both the proposed model

and the conventional models. The circuit is a two-channel interleaving synchronous buck converter with coupling core structures, as shown in Fig. 4.6. The flux source reluctance model is shown in Fig. 4.19. The proposed magnetic model can be derived from this reluctance model. As mentioned previously, for two-channel coupling core structures, the π-model is the simplest. The simulation circuits of the π-model and the proposed magnetic model are shown in Fig. 5.9(a) and (b), respectively.



(a)



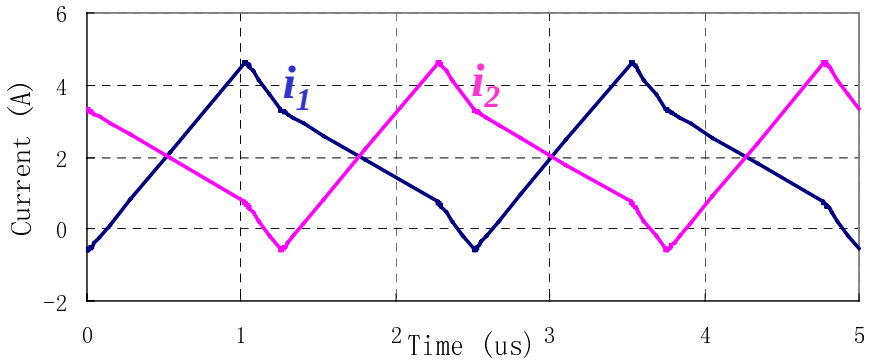
(b)

Fig. 5.9. Electric simulation models of two-channel interleaving buck with coupling inductors: (a) π-model; and (b) proposed model.

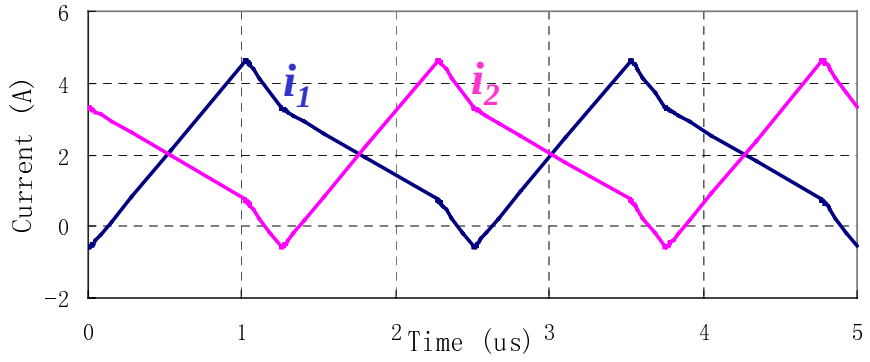
The inductances L_1 and L_2 in Fig. 5.9(a) are different from the self-inductances L_{11} and L_{22} in Fig. 5.9(b). According to the definitions of the

inductances, L_1 is the measured inductance of a winding when the other windings are open circuits, while L_{11} is the measured inductance of a winding when the other windings are short circuits.

The winding currents are i_1 and i_2 in Fig. 5.9(a) and (b). The currents i_{11} and i_{22} in Fig. 5.9(b) are the self-currents in the two windings, while i_{12} and i_{21} are the mutual currents. The simulation results of the winding currents for both models are shown in Fig. 5. 10. The two modeling methods give exactly the same results.



(a)



(b)

Fig. 5.10. Winding currents of two-channel interleaving synchronous buck with coupling core structures: (a) π-model; and (b) proposed model.

The simulation waveforms of the self-currents i_{11} and i_{22} in the proposed model are shown in Fig. 5.11. As shown by the waveforms, each self-current is

determined only by its corresponding winding voltage. The self-current is the decoupled part of the total winding current.

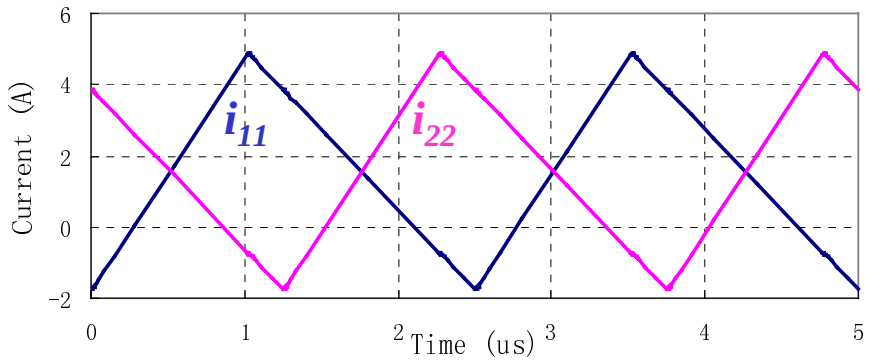


Fig. 5.11. Self-currents in the proposed model.

As illustrated in (5.8), the winding current is actually a weighted sum of the different volt-seconds applied to all the windings in the magnetic structure. To explain the concept more clearly, the process is illustrated in Fig. 5.12.

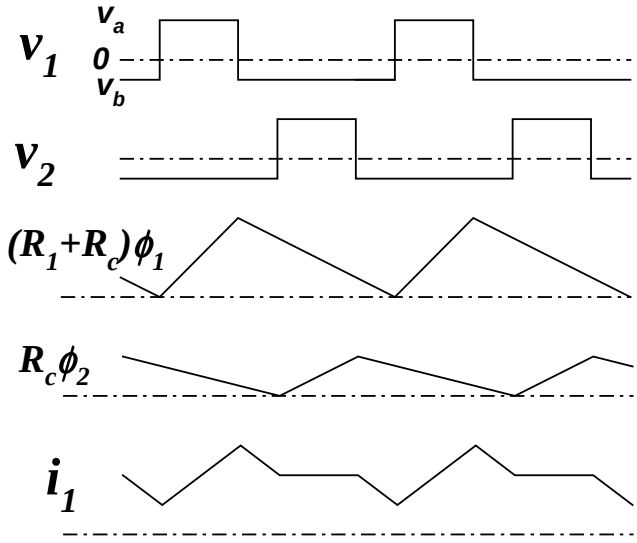


Fig. 5.12. Explanation of the concept behind the proposed method.

For the two-channel interleaving buck converters shown in Fig. 5.9, the two winding voltage waveforms v_1 and v_2 are shown in Fig. 5.12. The integration of

the voltage waveforms gives the flux waveforms in the corresponding core legs. The flux waveforms with the weighted coefficients are the waveforms of $(R_1+R_c)*\phi_1$ and $R_c*\phi_2$ in Fig. 5.12. The winding current waveform i_1 is just the weighted sum of the flux waveforms ϕ_1 and ϕ_2; the corresponding weighted factors are (R_1+R_c) and R_c, respectively. The flux waveforms are proportional to the self-current waveforms, which are the currents i_{11} and i_{22} in Fig. 5.9(b).

Of course, for two-channel coupling inductors, the proposed model is more complicated than the π-model. There is no point in using the proposed model if the coupling is only between two inductors. The proposed model is for more complicated core and winding structures for which the π-model can no longer be used.

The four-channel coupling core and winding structure shown in Fig. 5.2 could be used as the coupling inductors in a four-channel interleaving buck VRM. The corresponding electric simulation circuit of the interleaving buck VRM is shown in Fig. 5.13.

For the specific core structure shown in Fig. 5.2, Matrix A in (5.17) has the following format:

$$A=\begin{bmatrix} L_{11}^{-1} & L_{12}^{-1} & 0 & 0 \\ L_{21}^{-1} & L_{22}^{-1} & L_{23}^{-1} & 0 \\ 0 & L_{32}^{-1} & L_{33}^{-1} & L_{34}^{-1} \\ 0 & 0 & L_{43}^{-1} & L_{44}^{-1} \end{bmatrix}. \tag{5.19}$$

Because of the zeros in the matrix, the current-control current sources are only needed between the adjacent channels in the circuit model shown in Fig. 5.13.

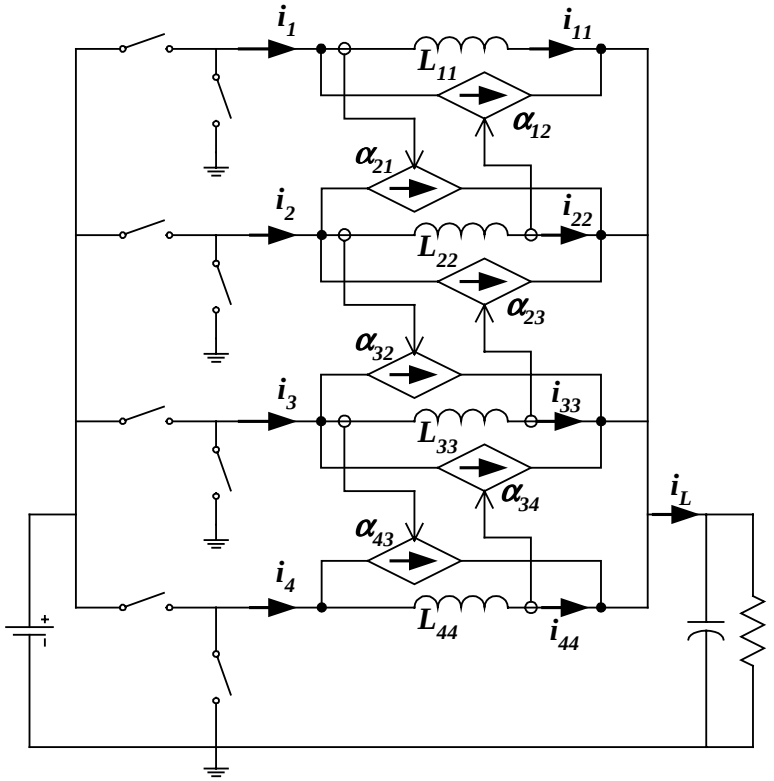
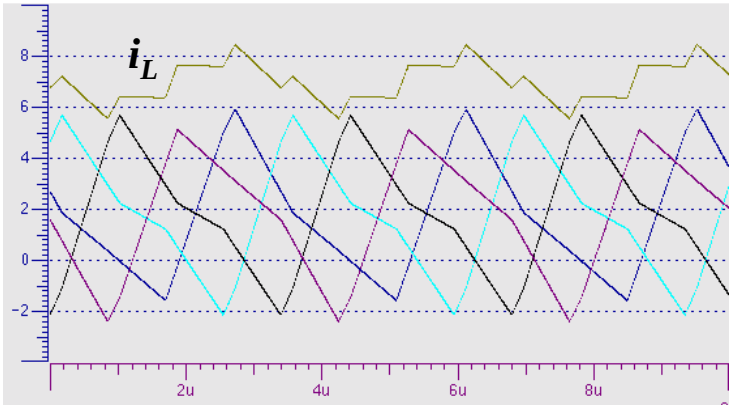


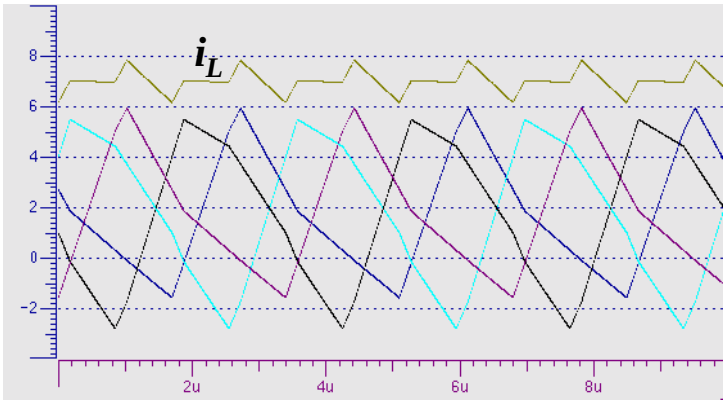
Fig. 5.13. Simulation circuit of four-channel interleaving VRM with the coupling inductor structure shown in Fig. 5.2.

As can be seen, the four-channel coupling inductor model utilizes the two-channel coupling inductor model shown in Fig. 5.9(b) as building blocks. This shows that the proposed model can be easily scaled to large number of coupling inductors, which is the major benefit of the proposed model.

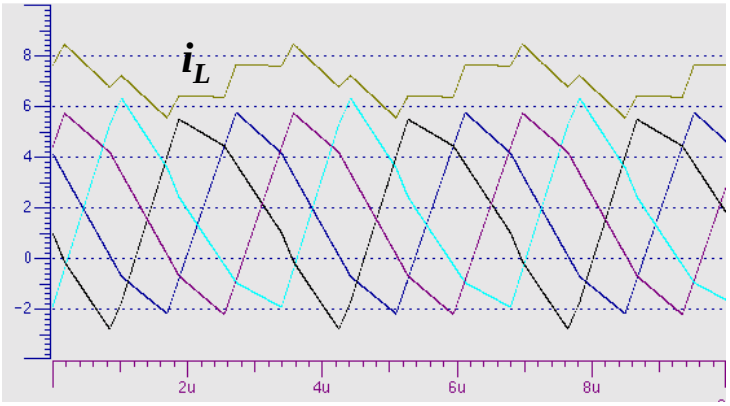
The simulation inductor winding currents and the total inductor currents are shown in Fig. 5.14.



(a)



(b)



(c)

Fig. 5.14. Four-channel VRM inductor currents with the coupling core structure shown in Fig. 5.2. Three different phase shift arrangements: (a) [0^o, 90^o, 180^o, 270^o]; (b) [0^o, 90^o, 270^o, 180^o]; and (c) [0^o, 180^o, 270^o, 90^o].

The different phase shift arrangements of the four channels in the core have different effects on the individual winding currents and the total inductor currents. The detailed performance evaluations, such as the coupling factor's effects on the waveforms, are not discussed here. (Some discussions and simulation results of the coupling core structure for multi-channel interleaving VRMs are presented in the Appendix.) The purpose is to show that small changes in the core and winding structure and arrangements might result in very different performances of the circuit. A proper magnetic model is required to evaluate the different coupling structures. The proposed model is a good tool for evaluating different coupling core structures.

If the conventional model is applied to the core structure shown in Fig. 5.2, the inductance matrix in (5.2) needs to be derived. As discussed previously, the inductance matrix is the inversion of Matrix A. Although Matrix A is simple, as shown in (5.19), its inverse matrix can be overwhelmingly complicated. For simplification, assume that all the self-inductances in (5.19) are L, and mutual inductances are M. The inversion of Matrix A is as follows:

$$A^{-1}=\frac{1}{\left(M^4-3\cdot L^2\cdot M^2+L^4\right)}\cdot L^4\cdot M^4\cdot\begin{bmatrix} \frac{\left(M^2-2\cdot L^2\right)}{\left(L^3\cdot M^2\right)} & \frac{-1}{M^3}\cdot\frac{\left(M^2-L^2\right)}{L^2} & \frac{1}{\left(M^2\cdot L\right)} & \frac{-1}{M^3} \\ \frac{-1}{M^3}\cdot\frac{\left(M^2-L^2\right)}{L^2} & \frac{1}{L^3}\cdot\frac{\left(M^2-L^2\right)}{M^2} & \frac{-1}{\left(L^2\cdot M\right)} & \frac{1}{\left(M^2\cdot L\right)} \\ \frac{1}{\left(M^2\cdot L\right)} & \frac{-1}{\left(L^2\cdot M\right)} & \frac{1}{L^3}\cdot\frac{\left(M^2-L^2\right)}{M^2} & \frac{-1}{M^3}\cdot\frac{\left(M^2-L^2\right)}{L^2} \\ \frac{-1}{M^3} & \frac{1}{\left(M^2\cdot L\right)} & \frac{-1}{M^3}\cdot\frac{\left(M^2-L^2\right)}{L^2} & \frac{\left(M^2-2\cdot L^2\right)}{\left(L^3\cdot M^2\right)} \end{bmatrix} \tag{5.20}$$

This matrix is much more complicated than (5.19). More non-zero and different inductances are involved in the matrix. The corresponding conventional model should be much more complicated than the proposed model.

The matrix in (5.20) also shows that all four inductors are coupled. Although the windings are not explicitly coupled in the proposed model, they are coupled in reality.

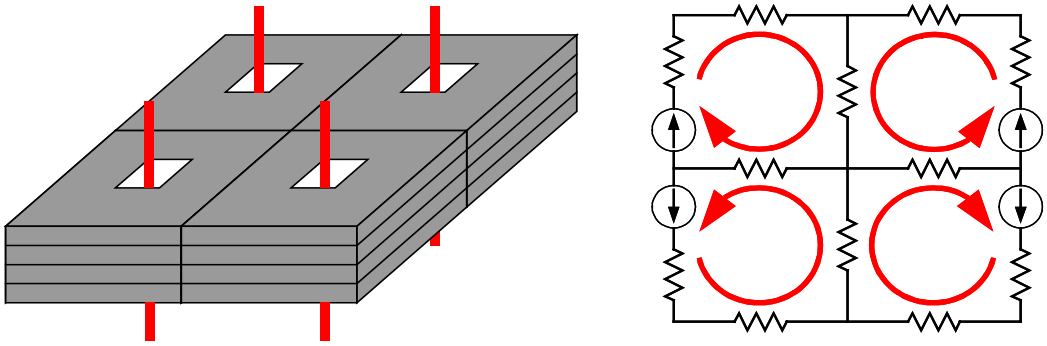
The simulation waveforms and the formulas also show that the seemingly symmetric core structure might give an asymmetric coupling pattern. Only with the accuracy and simplicity of the proposed model can the analysis of these subtle performance differences become possible.

5.5 Evaluation of Multi-Channel Coupling Inductor Structures for Interleaving Buck VRMs

As the simulation results show in Fig. 5.14, the core structure shown in Fig. 5.1(b) is not a very attractive coupling structure for multi-channel interleaving buck VRMs. No matter how the phases are arranged, the current in each channel is not symmetric, because of the asymmetric coupling patterns between channels. The coupling patterns in the first and last channels are different from those in the channels between them. To solve this problem, coupling should be introduced between the first and last channels to facilitate symmetric pattern coupling in very channel.

The core and winding structures shown in Fig. 5.15 provides symmetric coupling patterns among all channels. Symmetric current waveforms in each channel are expected.

The simulation circuit model can be easily derived from the flux source reluctance model, as shown in Fig. 5.16.



(a) (b)

Fig. 5.15. Coupling core structure for four-channel interleaving buck VRM: (a) core and winding structure; and (b) flux source reluctance model.

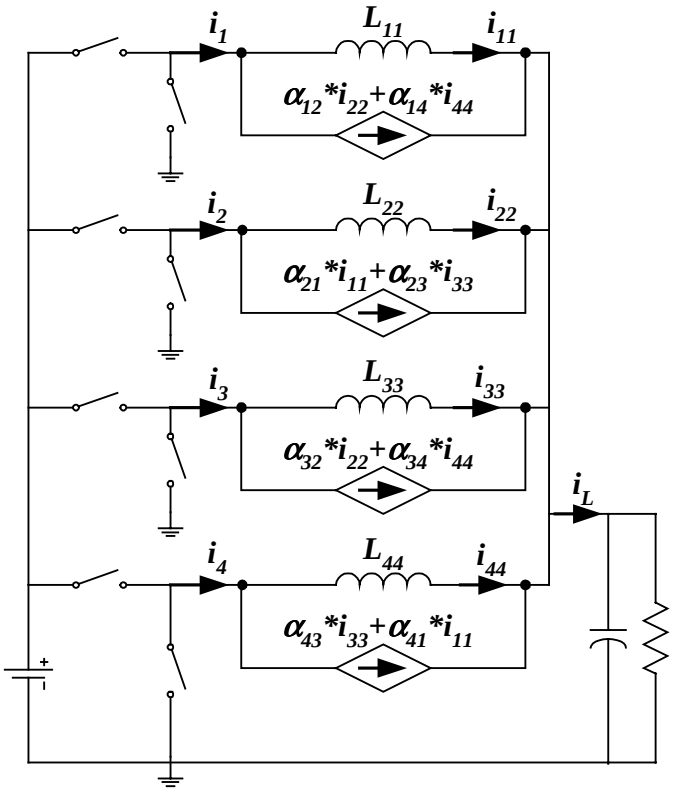


Fig. 5.16. Simulation circuit model for four-channel interleaving buck VRM with the core and winding structure shown in Fig. 5.15(a).

The four-channel interleaving buck VRM with non-coupling inductors is used as a benchmark in the comparison. Similar to the comparisons in Chapter 4, for different cases, the transient responses should be kept the same while comparing the steady-state current ripples in each channel. The transient equivalent inductance can be illustrated in the small-signal transfer functions. As shown in Chapter 2, the software of SIMPLIS can provide the small-signal transfer functions from the switching circuit simulation. In this way, the same simulation circuit model shown in Fig. 5.16 can be used to evaluate both the transient and steady-state performances of the converter.

Three cases are compared, as follows: (a) no coupling among inductors (NC); (b) inductors in each two channels with a 180^{o} phase shift are coupled (as in the case discussed in Chapter 4) (NIC); and (c) all four inductors are coupled (IC). The small-signal current transfer functions are shown in Fig. 5.17.

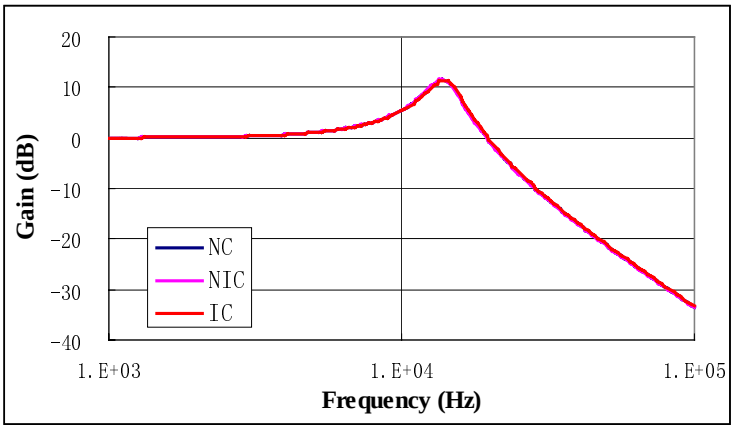
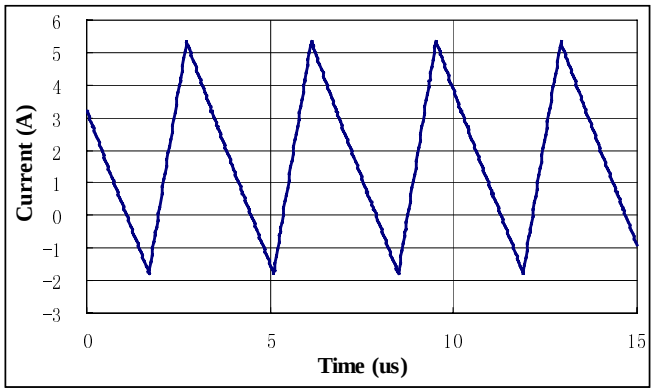


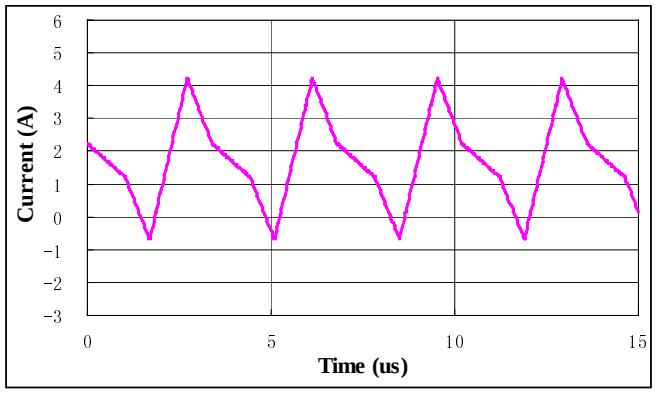
Fig. 5.17. The three cases under comparison have the same small-signal transfer functions.

All three cases under comparison have the same small-signal control-to-output-voltage transfer functions. The transient responses of these three cases should be the same if the same controller is used.

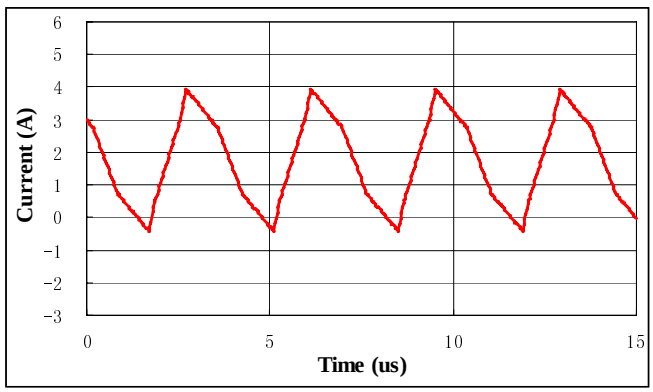
The steady-state inductor current waveforms for the three cases are compared in Fig. 5.18.



(a)



(b)

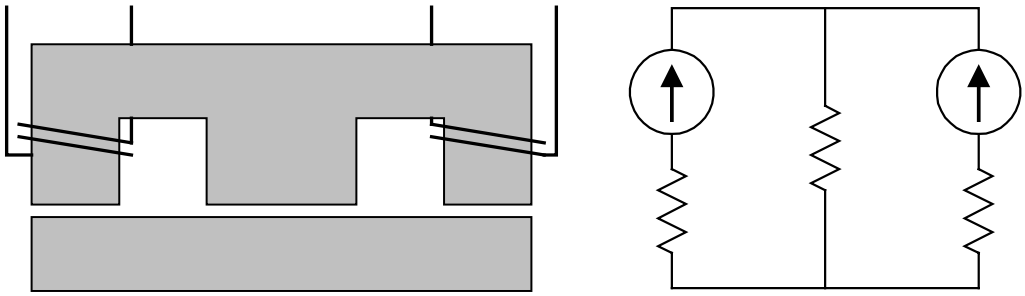


(c)

Fig. 5.18. Inductor current waveforms in a channel: (a) no coupling among inductors; (b) coupling between two channels with a 180^{o} phase shift; and (c) coupling among all four inductors.

For each case, only the inductor current in one channel is shown. The inductor currents in the other channels are the same with phase shifts. The coupling inductors reduce the inductor current ripples in each channel. Although the inductor current waveforms of case (b) and (c) are different, their peak-to-peak currents are almost the same. Similar conduction and switching losses are expected. The circuit performances of case (b) and (c) are similar. Both of them would have better efficiency than case (a).

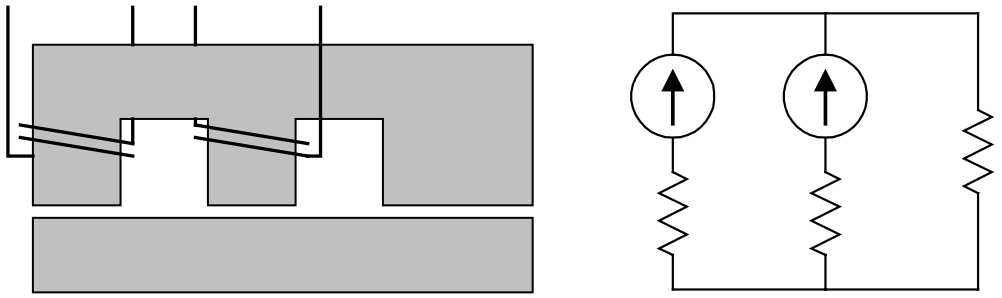
This core and winding structure is only for high switching frequency applications in which very small inductances are required. For today's switching frequencies, ferrite cores should be considered. The coupling core and winding structure shown in Fig. 4.5 can be redrawn, as shown in Fig. 5.19.



(a) (b)

Fig. 5.19. The core and winding structures redrawn from Fig. 4.5: (a) core and winding structure; and (b) flux source reluctance model.

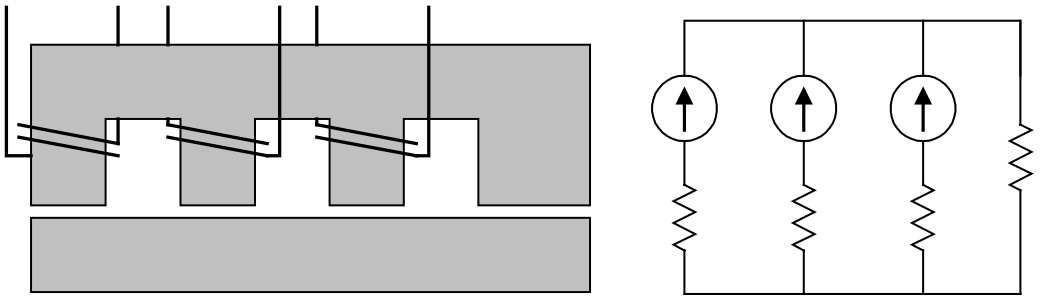
The reluctance (or air gap) in the center leg represents the coupling effects. Actually, the center leg just provides a path with magnetic reluctance. It does not have to be in the center. The center leg can be moved to the outside, as shown in Fig. 5.20.



(a) (b)

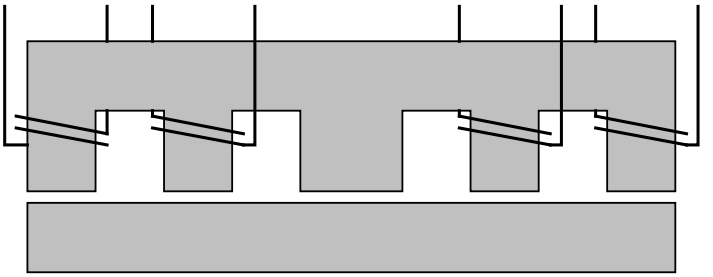
Fig. 5.20. The reluctance path does not have to be in the center: (a) core and winding structure; and (b) flux source reluctance model.

The flux source reluctance model in Figs. 5.20(b) and 5.19(b) are exactly the same. The coupling between the two inductors should also be the same, which results in similar circuit performances. Based on this structure, the coupling inductor structure for multi-channel interleaving buck VRMs can be easily derived. The coupling inductor structures for three- and four- channel interleaving buck VRMs are shown in Figs. 5.21 and 5.22, respectively.

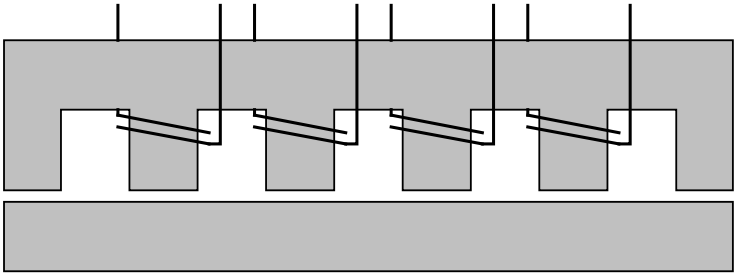


(a) (b)

Fig. 5.21. Coupling inductor structure for three-channel interleaving buck VRMs: (a) core and winding structure; and (b) flux source reluctance model.



(a)



(b)

Fig. 5.22. Coupling inductor structures for four-channel interleaving buck VRMs: (a) structure I; (b) structure II.

The core structure in Fig. 5.22(b) has one leg more than that in Fig. 5.22(a). The fluxes generated by different windings all flow through the legs without windings. As discussed in Chapter 4, the legs without windings (center leg for the structure in Fig. 4.5) have small flux ripples. The two outer legs in the structure in Fig. 5.22(b) have small flux ripples. EMI problem can be reduced in this structure. Of course, this concept of putting legs with small flux ripples outside can also be used in the other structures. The penalty is that one more leg is required in the core.

The concept of using PCB windings (shown in Fig. 4.4) can also be applied in the preceding proposed structures. For the three-channel coupling core structures shown in Fig. 5.21, PCB windings can be implemented, as shown in Fig. 5.23.

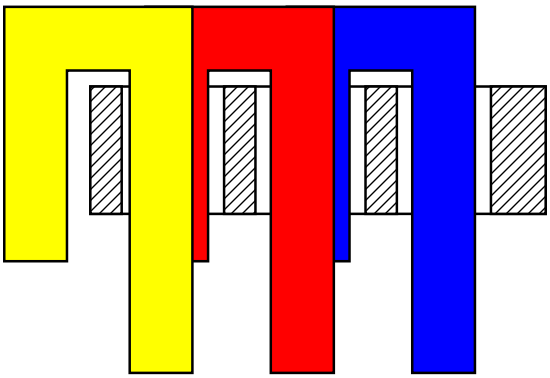


Fig. 5.23. PCB winding implementation for the three-channel coupling inductor structure.

For the three-channel interleaving buck VRM with coupling inductor structures shown in Fig. 5.21, the flux loops are defined, as shown in Fig. 5.24.

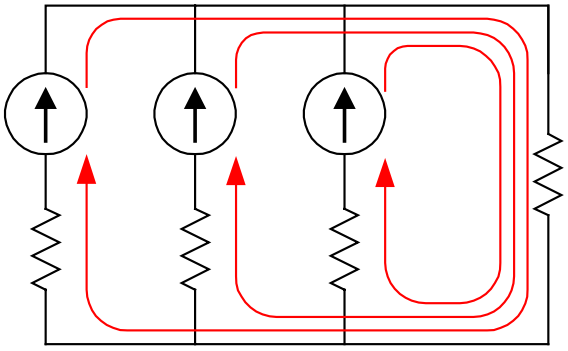


Fig. 5.24. Flux loop definition of three-channel coupling core structure.

The simulation circuit can be easily derived from the reluctance model, as shown in Fig. 5.25.

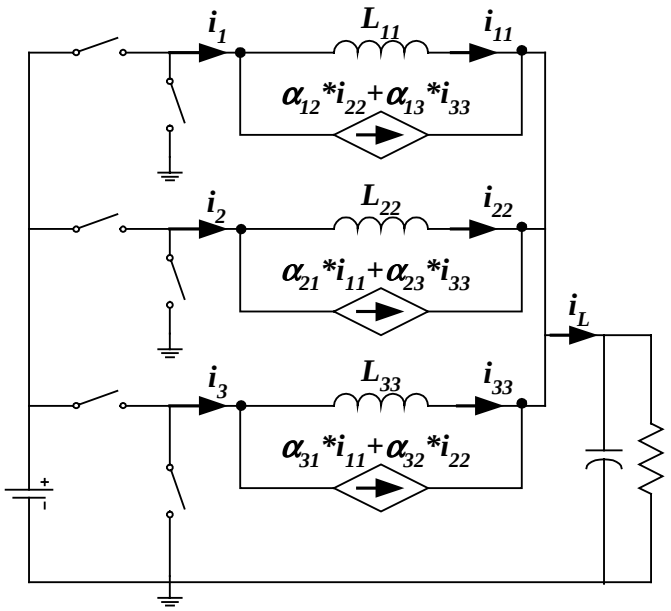
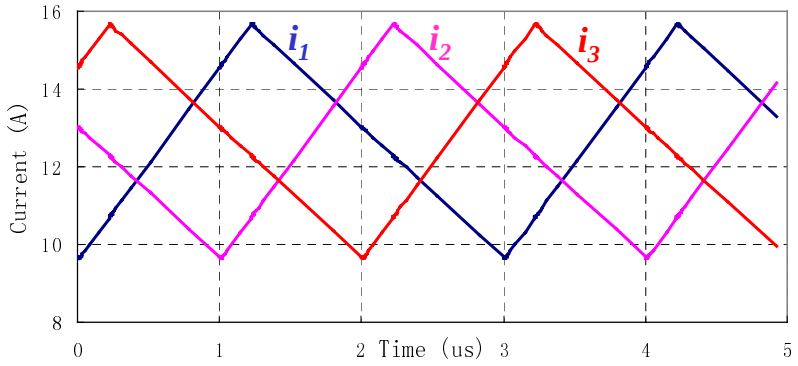
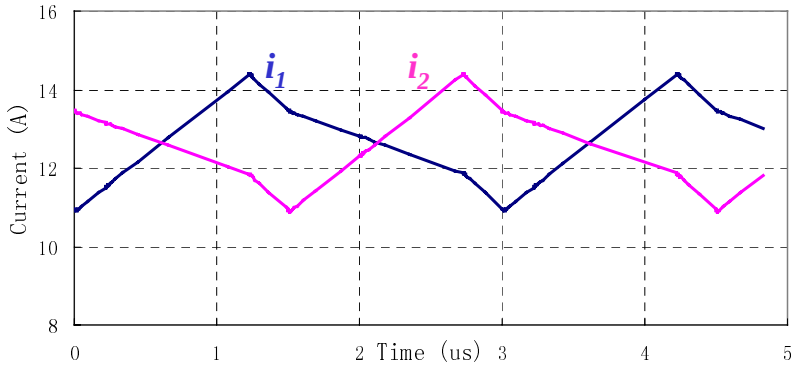


Fig. 5.25. Simulation circuit for the three-channel interleaving VRM with coupling inductors shown in Fig. 5.23.

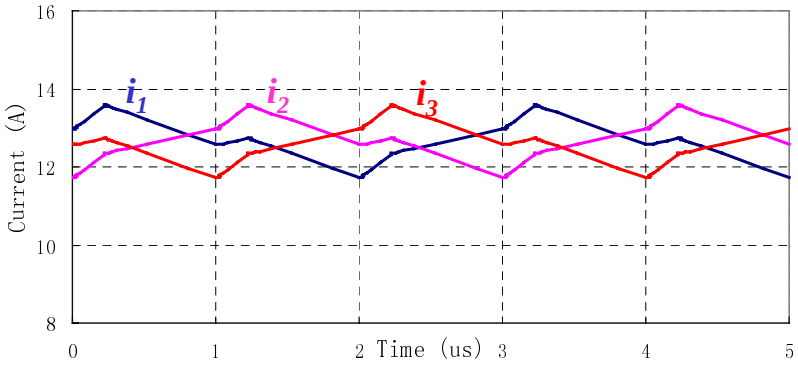
The steady-state inductor current waveforms in each channel for different coupling inductors are compared in Fig. 5.26. Fig. 5.26(a) corresponds to the three-channel interleaving buck VRM without coupling among channels. Fig. 5.26(b) corresponds to the two-channel interleaving buck VRM with inverse coupling inductors, which is the case discussed in Chapter 4. Fig. 5.26(c) corresponds to the three-channel interleaving buck VRM using the coupling inductor structure, shown in Fig. 5.21 or 5.23. For both the coupling inductor structures used in Figs. 5.26(b) and (c), assume that the same air gaps are used in all legs, and that the cross-section area of the leg without winding is twice those of the legs with windings. For the three cases compared in Fig. 5.26, the transient equivalent inductance in each channel is kept the same, 600nH. The average current in each channel is also the same.



(a)



(b)

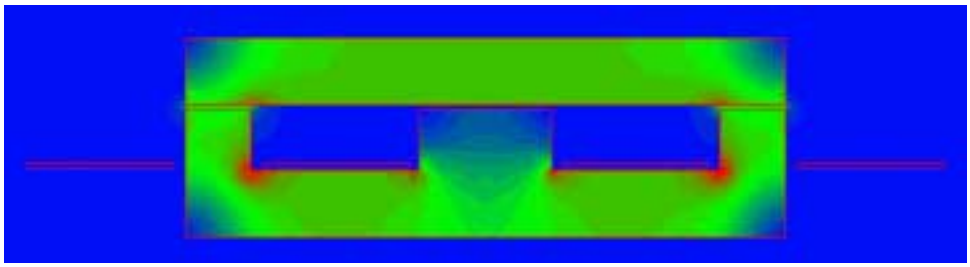


(c)

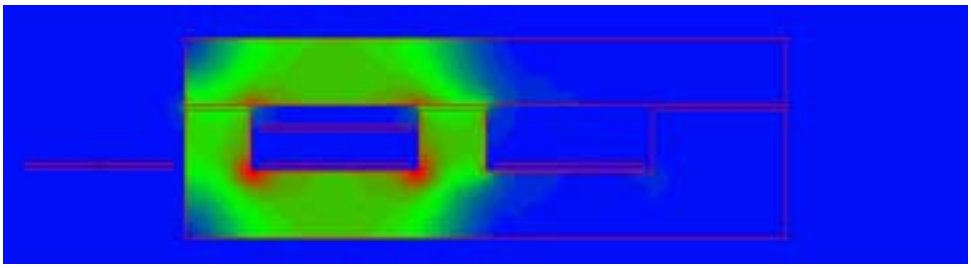
Fig. 5.26. Steady-state inductor current comparison: (a) non-coupling; (b) two-channel coupling; and (c) three-channel coupling.

The three cases compared in Fig. 5.26 should have the same transient responses, but different current ripples. From the waveforms, the peak-to-peak currents for the three cases are 6.0A, 3.5A and 1.9A, respectively. As discussed previously, smaller current ripples result in higher efficiencies. The comparison in Fig. 5.26 indicates that coupling more channels results in higher efficiencies.

Moreover, less core losses are expected in the structure shown in Fig. 5.20 than in the structure shown in Fig. 5.19. The AC flux distributions of the two cases are compared in Fig. 5.27.



(a)



(b)

Fig. 5.27. AC flux distribution comparison: (a) structure in Fig. 5.19; and (b) structure in Fig. 5.20.

Because of the AC flux ripple cancellation effects, the core structure shown in Fig. 5.27(b) has a larger area with small AC flux ripples. Thus, core losses of the structure shown in Fig. 5.27(b) should be smaller than those of the structure shown in Fig. 5.27(a).

In summary, in order to achieve symmetric current waveforms in different channels, the coupling between the inductors in different channels should be symmetric. The proposed core and winding structure for the coupling inductors in three-channel interleaving buck VRMs can reduce the current ripples in each channel and reduce the core losses. The proposed structure can be easily extended to the coupling inductors in multi-channel interleaving buck VRMs. Coupling more channels in interleaving VRMs results in further reduction of the current ripples in each channel.

5.6 Modeling of Coupling Inductors in Interleaving Tapped Buck VRMs

For high input voltage VRMs, the interleaving tapped buck topology shown in Fig. 5.28 is used in order to extend the duty cycle.

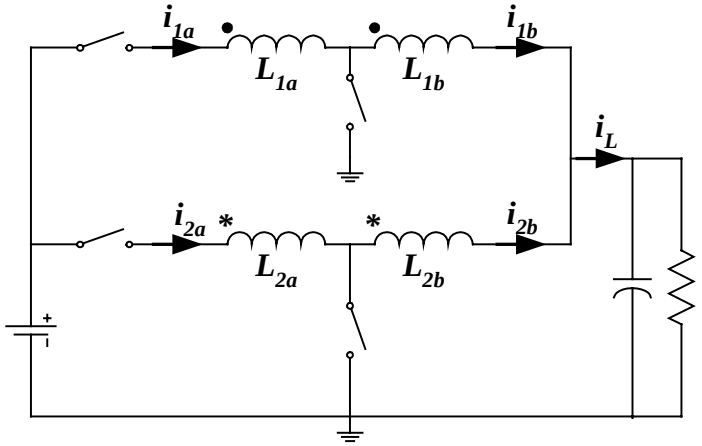


Fig. 5.28. Two-channel interleaving tapped buck VRM.

The leakage inductance between L_{1a} and L_{1b} generates large voltage spikes on the MOSFETs, which makes the circuit impractical. In order to solve this problem, a simple active clamp circuit is proposed by Mr. Kaiwei Yao, as shown in Fig. 5.29.

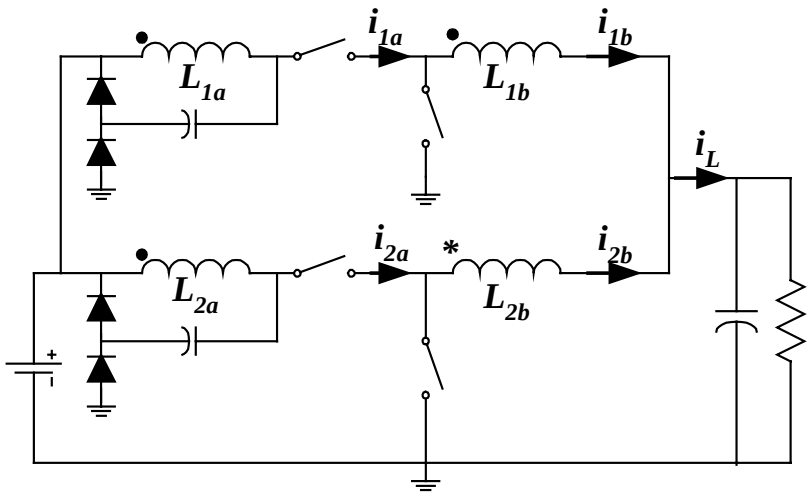


Fig. 5.29. Two-channel interleaving tapped buck VRM with clamp circuit.

The four windings in the two channels are integrated in a pair of E-I cores, as shown in Fig. 5.30.

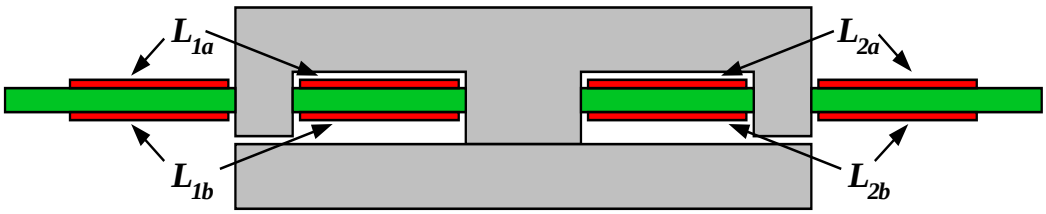


Fig. 5.30. Inductor structure of two-channel interleaving tapped buck VRM.

Single-turn PCB windings are used for the inductors. Windings L_{1a} and L_{1b} are strongly coupled with certain unavoidable leakage inductances. Because there is no air gap in the center leg, the two channels are decoupled.

Coupling effects can be introduced between the two channels by adding an air gap in the center leg, as was done in the interleaving buck VRMs discussed in Chapter 4. The core and winding structure with coupling between the two channels is shown in Fig. 5.31. The cores in use are the E18/4/10 and the PLT 18/10/2. The same air gaps are assumed in all three legs.

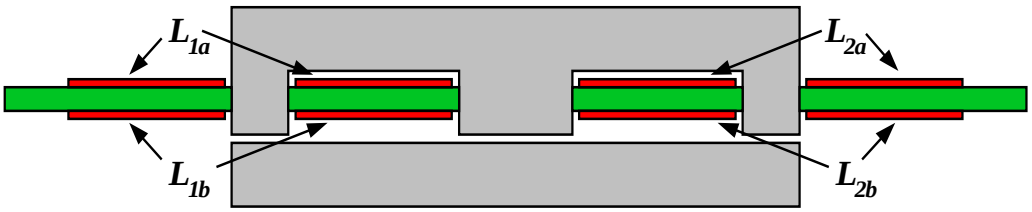


Fig. 5.31. Inductor structure for the two-channel interleaving tapped buck VRM.

There are four windings in total. Windings L_{1a} and L_{1b} are strongly coupled, as are windings L_{2a} and L_{2b}. Loose coupling effects are introduced between the two sets of windings. The simulation circuit for this coupling structure is difficult to derive using conventional magnetic models. Moreover, the turn numbers of L_{1a} and L_{1b} could be different in some designs, which is another complicating factor for the conventional magnetic models. The rest of this section uses the magnetic model proposed in this chapter to model this structure.

The reluctance model of the inductor structure shown in Fig. 5.31 can be easily derived, as shown Fig. 5.32.

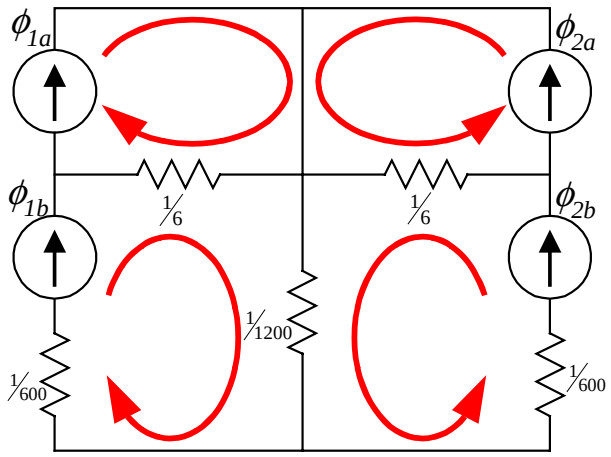


Fig. 5.32. Reluctance model for the inductor structure shown in Fig. 5.31.

The values of the reluctance can be derived from the measurement data of the inductances. The units for the reluctances shown in the Fig. 5.32 are (nH^{-1}). The

four reluctance loops are defined. Based on this reluctance model, the corresponding simulation circuit can be derived, as shown in Fig. 5.33.

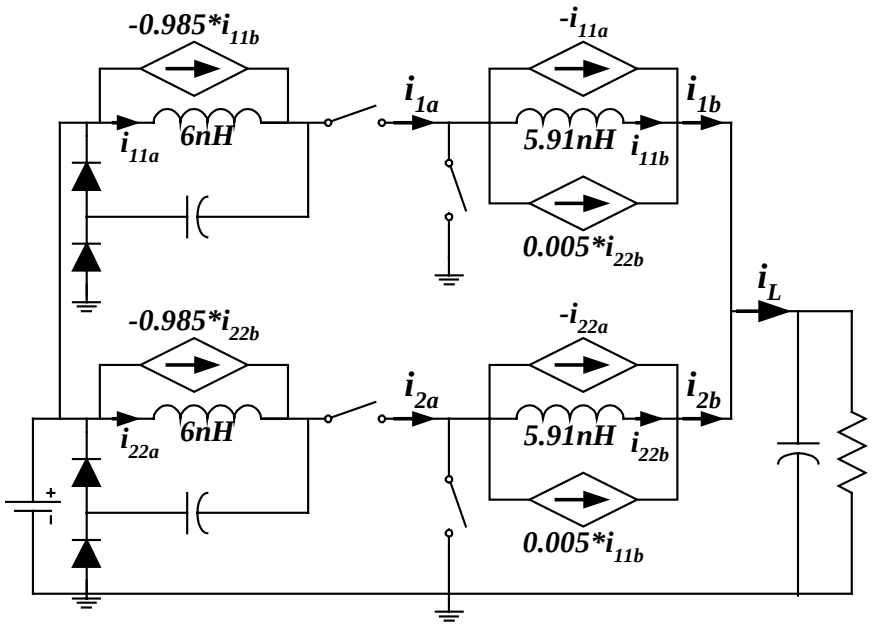
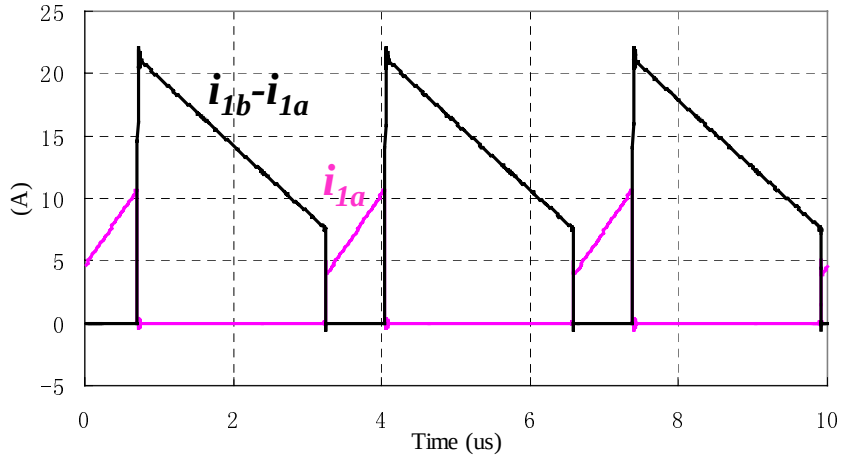


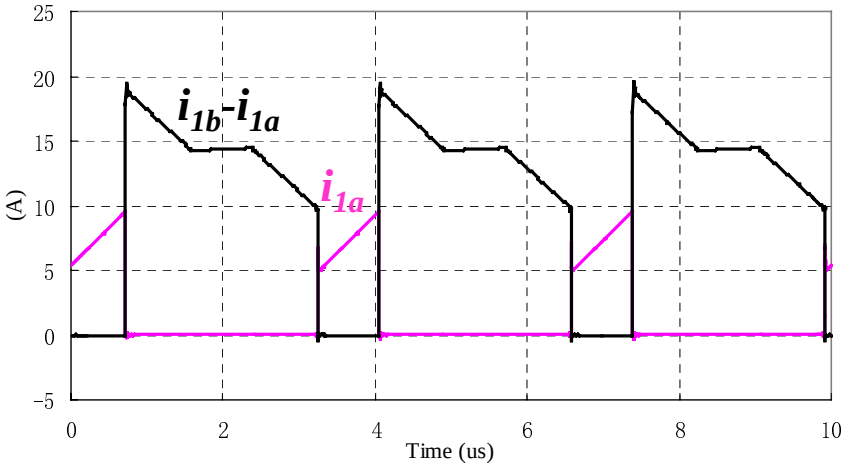
Fig. 5.33. Simulation circuit model for the two-channel interleaving tapped buck VRM with loose coupling between channels.

The simulation results with and without coupling effects between the two channels are compared in Fig. 5.34. The input and output voltage of the VRMs under simulation are 12V and 1.5V, respectively. The switching frequency is each channel is 300kHz.

As shown in the waveforms, the coupling effects between the two channels reduce the current ripples in each channel. The results are similar to the channel coupling in two-channel interleaving buck VRMs.



(a)



(b)

Fig. 5.34. Simulation current waveforms for the interleaving tapped buck VRM: (a) no coupling between channels; and (b) coupling between channels.

5.7 Summary

The conventional magnetic models are too complicated to be used for multi-channel coupling inductor core structures. This chapter shows that the windings in the coupling inductor structures can also be represented as flux sources. With this flux source reluctance model and some mathematical transformations, the coupled

inductors in a core can be decoupled mathematically. This makes the proposed model much simpler than the conventional models for cases in which more inductors are coupled. Moreover, the proposed method is directly related to the magnetic reluctance model. The parameters in the model can be easily derived from the magnetic reluctance model. Circuit simulation results for both methods are compared in order to verify the validity of the proposed method. Examples of some core and winding structures are modeled to show how to utilize the model.

The proposed model is based on the magnetic reluctance circuit, which is the prerequisite of the model. In the coupling inductors with simple windings, the reluctance model usually can be easily derived from the core and winding structure. The availability of the reluctance model is assumed, and is not discussed in this chapter. As long as the reluctance model is available, the proposed model can be derived for any coupling magnetic components.

The proposed model does not deal with the capacitance between the windings, losses or the temperature and frequency effects to the material parameters.

Simulation results based on the proposed magnetic model show that coupling of more interleaving channels can further reduce the current ripples, thus improve the converter efficiency. The concept of coupling inductor can also be applied in the center-tapped buck converters to improve efficiency.

Chapter 6

Conclusions and Future Work

With the emergence of the Intel Pentium ™ processor, the research of VRMs has become a hot area. This dissertation addresses the following issues in VRMs: verification of the small-signal modeling of multi-channel interleaving buck converters, critical inductance in transient responses, application of coupling inductors in interleaving buck VRMs, and the magnetic modeling of multi-coupling core structures.

6.1 Summary

With the advanced simulation software, the small-signal transfer functions can be obtained using the switching circuit simulations. The simulation results shows that the small-signal model of a multi-channel interleaving buck converter can be simplified to a single buck converter. The equivalent inductance of an n-channel interleaving buck converter is 1/n of the inductance in each channel. The equivalent switching frequency is n times the switching frequency in each channel.

The feedback control bandwidth determines the average inductor current slew rate. For the same control bandwidth, the duty cycle increase during transient responses is proportional to the inductance. The critical inductance is defined as the point at which the duty cycle is close to saturation during transient responses. For inductances smaller than the critical inductance, the duty cycle is not

saturated during transient responses, and the average current slew rates are determined by the feedback control bandwidths. For inductances larger than the critical inductance, the duty cycle becomes saturated during transient responses. The inductance limits the average current slew rates. The critical inductance is the largest inductance that gives the fastest transient responses. Larger inductances usually give higher efficiency. The critical inductance gives the highest efficiency without slowing down the transient responses, therefore, it could be a good design tradeoff.

Both the step-up and step-down load transient responses have corresponding critical inductances. Inductances smaller than the smaller of the two critical inductances give the symmetric step-up and step-down transient responses. The transient voltage spikes in symmetric transient responses are smaller than those in asymmetric transient responses. The symmetric transient responses have the advantage of smaller output capacitor design.

Faster transient responses require smaller inductances, which result in larger inductor ripples. Although interleaving reduces the total output current ripples, it cannot reduce the current ripples in each channel. Larger ripples result in larger conduction losses and turn-off losses in the MOSFETs, which results in lower efficiency. Applying coupling between the inductors in different channels changes the inductor current waveforms. Different equivalent inductances are defined in the different time intervals in a switching cycle. The equivalent inductance that determines the inductor current ripple is defined as the steady-state equivalent inductance, while the one that determines the transient responses is defined as the transient equivalent inductance.

Applying inverse coupling to the two inductors in the two interleaving channels with a 180^{o} phase shift increases the steady-state equivalent inductance while reducing the transient equivalent inductance. If the transient responses are designed to be the same, the coupling inductors reduce the current ripples in each

channel. The efficiency can be improved without compromising the transient responses. Stronger coupling effects give smaller current ripples. However, it makes the flux imbalance in the core more severe if the currents in the channels are not balanced.

The coupled inductor can be easily built on a pair of commercial E-I cores. Compared to the non-coupling integrated inductor structure, the coupling core structure is easier to manufacture and is mechanically more stable. Moreover, the coupling core structure reduces the core losses, because the air gap in the center leg makes the flux more evenly distributed. The fringing effects and winding losses in coupling core structures can also be reduced because of the smaller air gaps in the outer legs.

In order to evaluate the application of the coupling concept to the inductors in multi-channel interleaving structures, an appropriate magnetic model is proposed. The magnetic models are based on the magnetic reluctance model of the core and winding structure. The windings are represented as flux sources in the proposed model. With the flux source reluctance model and mathematical transformations, the coupled inductors can be decoupled in the electric circuit simulation model. This greatly reduces the complexity of the model when a large number of coupled inductors are considered. Examples show that the proposed model can be applied to a variety of different core and winding structures. The model can be easily scaled to model complicated structures.

The proposed model is based on the magnetic reluctance circuit, which is the prerequisite of the model. The availability of the reluctance model is assumed, and is not discussed in this chapter. As long as the reluctance model is available, the proposed model can be derived for any coupling magnetic components.

6.2 Future Work

In order to improve the power density of VRMs, as many as possible of the magnetic components should be integrated. The coupling inductors between two channels not only make the magnetic structure easier to manufacture and more stable, but also improve the efficiency. This concept is attractive to be applied to multi-channel inductors. With the proposed magnetic model, the circuit simulation of different core and winding structures becomes possible. Applying the proposed magnetic model to evaluate the different coupling core and winding structures could be an interesting research area.

Appendix A

Switching Action Delays in VRMs

A.1 Switching Action Delay in Single-Buck VRMs

Because of the switching action in VRMs, there are some delays between the load current transition and the response of the inductor current. The delays in the real circuit include the MOSFET gate driver delay, the MOSFET turn-on and turn-off delay, etc. Among them, the switching action delay, which is comparable to the switching cycle, is the most significant part and will be discussed in the following sections.

A single-buck VRM with typical voltage feedback control is shown in Fig. A.1. The corresponding simulation waveforms, illustrating the switching action delays during load step-up transient responses, are shown in Fig. A.2.

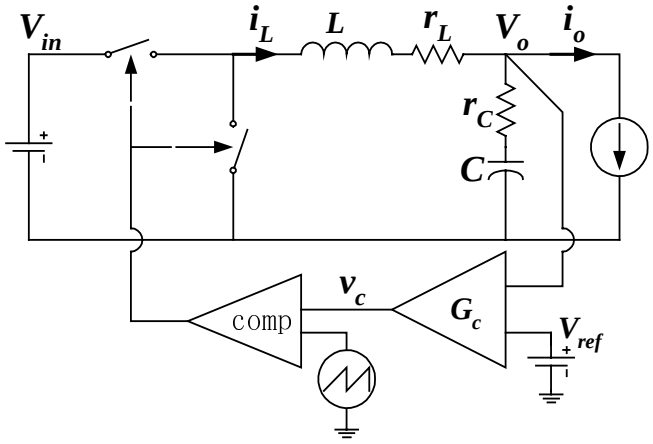


Fig. A.1. Buck VRM with typical voltage feedback control.

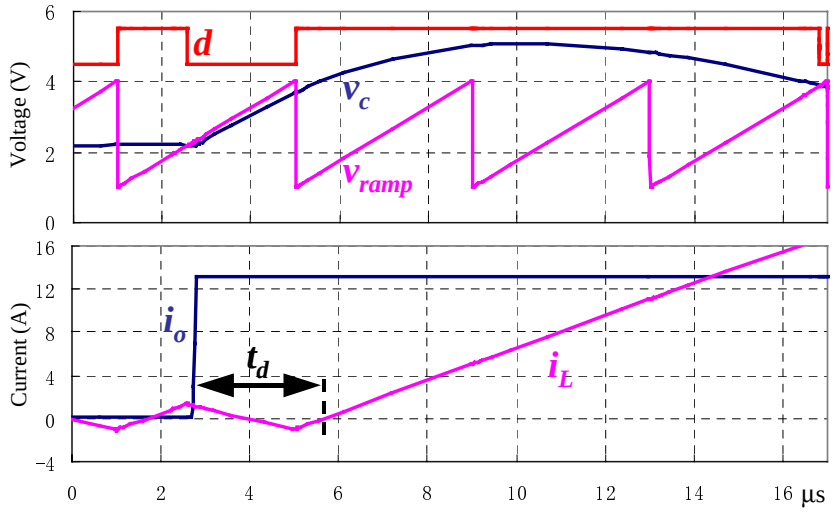


Fig. A.2. Inductor current delay due to switching actions.

The waveforms marked as i_o and i_L are the load and inductor currents, respectively, while v_c and v_{ramp} are the error signals from the compensator and the sawtooth signal, as defined in Fig. A.1. Trailing-edge modulation is assumed. As shown in Fig. A.2, the load transient occurs after the top MOSFET turns off. The error signal v_c does not intersect with the sawtooth signal v_{ramp} until the next switching cycle. The inductor current cannot increase until the next switching cycle. The period between the load transition instant and the point at which the inductor current reaches the load current before transition and starts to increase is the switching action delay, marked t_d in the figure.

In real circuits, in order to prevent false switching actions, latches are used to ensure that the switches have only one switching action in each switching cycle. For trailing-edge modulation, the top switch can only be turned on once, at the beginning of a switching cycle. After the turn-off edge, the switch cannot be turned on until the next switching cycle, even if the error signal does intersect with the sawtooth signal.

As can be imagined, if the load current transition occurs at a time instant closer to the turn-on edge of the top switch, the switching action delay t_d can be reduced, as shown in Fig. A.3.

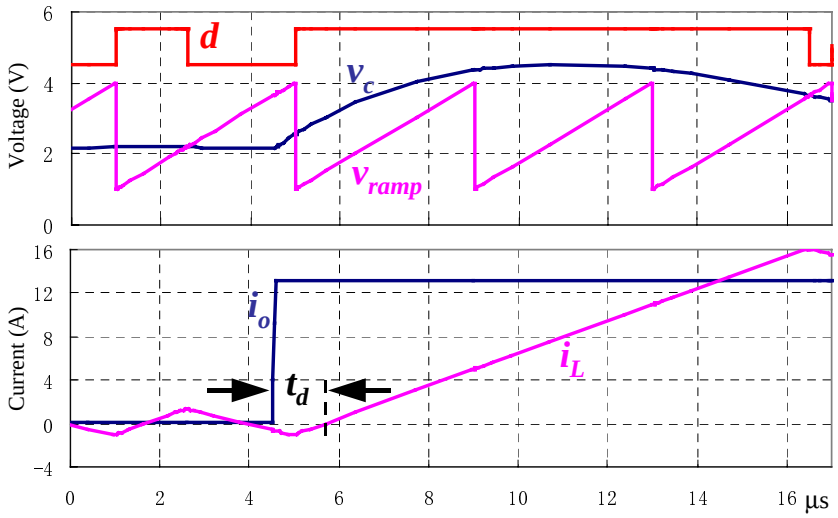


Fig. A.3. Inductor current delay is smaller when the load transient occurs closer to the beginning of a switching cycle.

When the load transient occurs during the turn-on period of the top switch, the duty cycle increases right away in this cycle. There is no switching action delay because the inductor current is at the rising period, as shown in Fig. A.4.

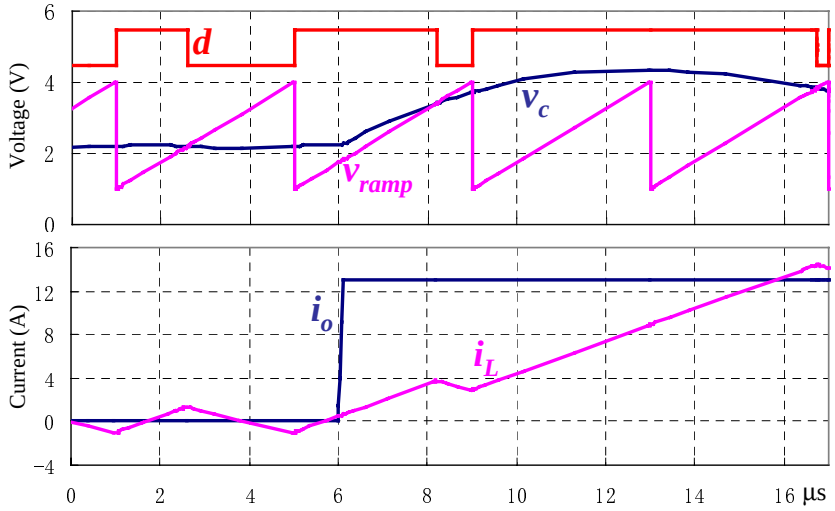


Fig. A.4. There is no delay if the load transient occurs during the turn-on period.

The purpose of the delay analysis is to facilitate the capacitor design. Because the time instant at which the load transition happens cannot be controlled, the capacitor design needs to be based on the worst case, which corresponds to the longest delay. In order to identify the worst case, a series of cases with moving load transition instants in the switching cycle are simulated. The results are shown in Fig. A.5.

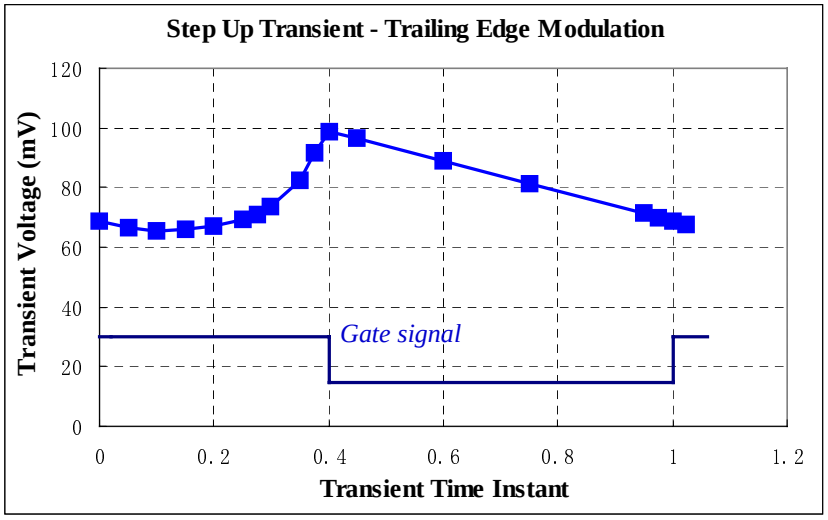


Fig. A.5. Transient time instant effects on transient voltage spikes.

The horizontal axis is the normalized time instant at which the load transients occur. The vertical axis is the voltage spike during transient responses. Larger delays correspond to larger unbalanced charges and larger voltage spikes during transient responses. As can be seen in Fig. A.5, the worst case is when the load transient happens right at the turn-off edge of the top switch.

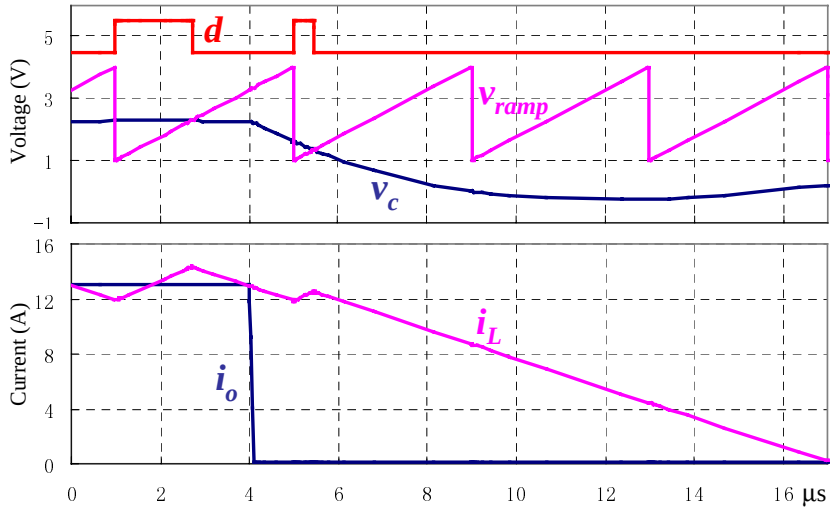
The maximum delay can be easily derived from the waveforms shown in Fig. A.2, as follows:

$$t_d = T_s \cdot (1 - D + \frac{D}{2}) = T_s \cdot (1 - \frac{D}{2}), \tag{A.1}$$

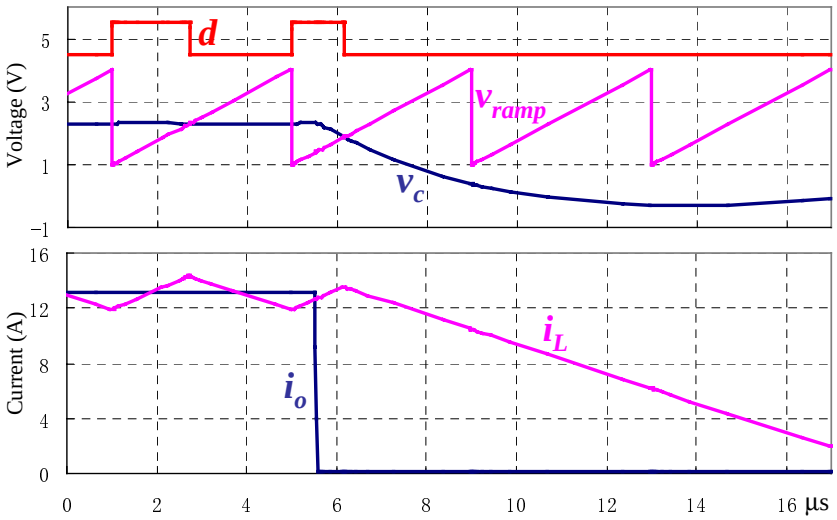
where D is the steady-state duty cycle, and T_s is the switching period. The switching delay is comparable to the switching period.

From (A.1), the smaller steady-state duty cycles corresponds to larger switching action delays. For VRMs with the same output voltages, the higher input voltages result in longer switching action delays in the worst case.

The preceding analysis is based on the load step-up transitions. For the load step-down transitions, the story is different. The simulation waveforms of the load step-down transitions are shown in Fig. A.6.



(a)



(b)

Fig. A.6. Switching action delay in load step-down transitions are not significant (trailing-edge modulation): (a) load transition during off time; and (b) load transition during on time.

In trailing-edge modulation, the top switch can be turned off at any time instant in a switching cycle, as long as the error signal intersect with the sawtooth signal. As can be seen in the simulation waveforms, the duty cycle has an

immediate change when there is a load step-down transition, whether the load transition happens during the on time or off time of the top switch. There is no delay as there is in the load step-up transient responses.

The time instant at which the load step-down transient occurs should not have much effect on the transient voltage spikes. To verify this, a series of cases similar to those shown for the load step-up transient responses are simulated for the load step-down transitions. The results are shown in Fig. A.7. Since the time instant of the load transient does not have much effect on the voltage spikes, the switching action delay in step-down transient responses can be ignored.

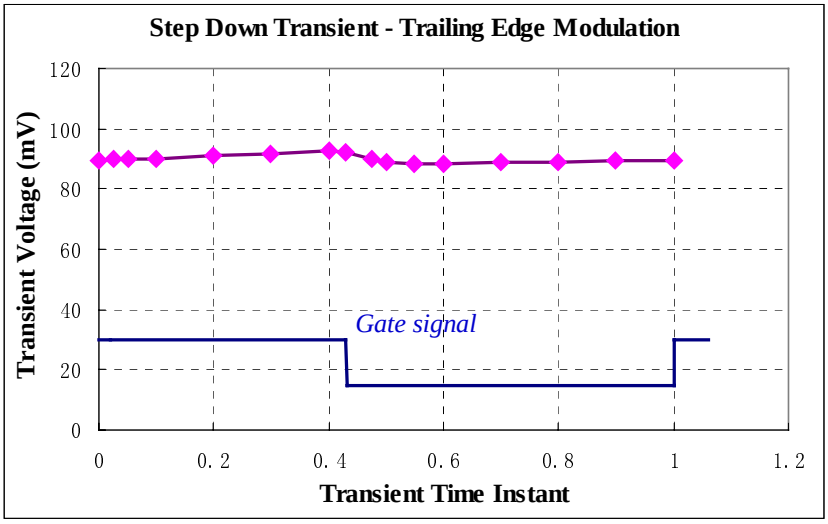


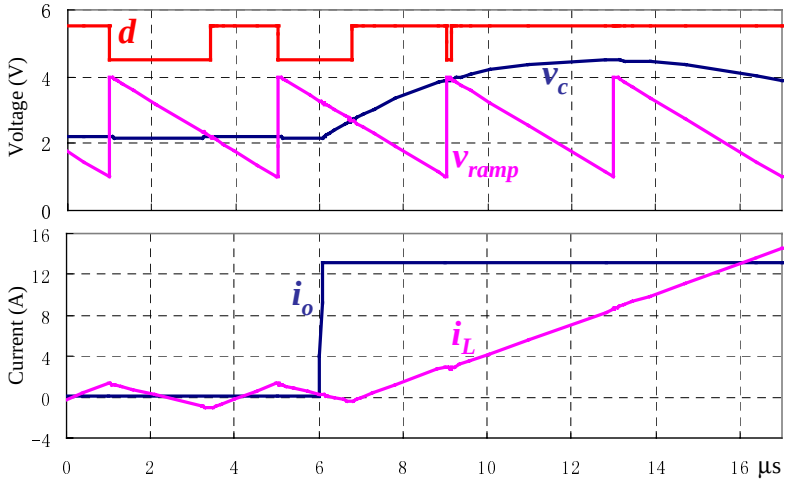
Fig. A.7. Load step-down transition time instant effects on transient voltage spikes.

The preceding discussions of the switching action delay in transient responses are based on trailing-edge modulation. The trailing-edge modulation is the most common operation of the PWM controller. In some applications, such as Rdson current sensing of the bottom switches, the fixed trailing edge is preferred. In these cases, leading-edge modulation may be used.

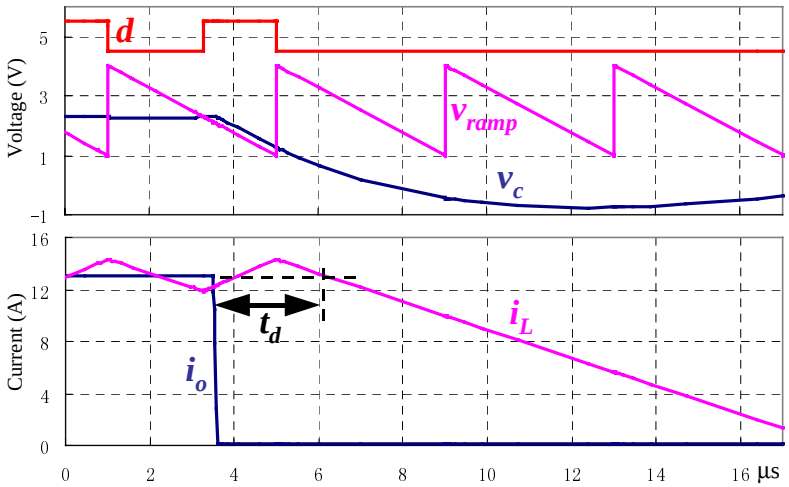
In leading-edge modulations, a different sawtooth signal is used. The top switch can be turned on at any time instant in a switching cycle, as long as the error signal intersects with the sawtooth signal. However, the top switch can be turned off only once, at the end of the switching cycle. The switch operation in leading-edge modulation is opposite to that in trailing-edge modulation. It is expected that the switching action delay in transient responses should also have different results for the two modulation methods.

In leading-edge modulation, no significant switching action delay exists in the load step-up transient responses. However, the load step-down transient voltage spikes are affected by the time instant at which the load transition occurs. The simulation waveforms for the load step-up and step-down cases are shown in Fig. A.8.

As shown in Fig. A.8, the switching action delay for the load step-down transitions can be defined as the period between the load transition time instant and the point at which the inductor current reaches the load current before load transition and starts to decrease.



(a)



(b)

Fig. A.8. Switching action delay in leading-edge modulation: (a) load step-up transition; and (b) load step-down transition.

Curves similar to those shown in Figs. A.5 and A.7 can be plotted for the leading-edge modulation, as shown in Fig. A.9.

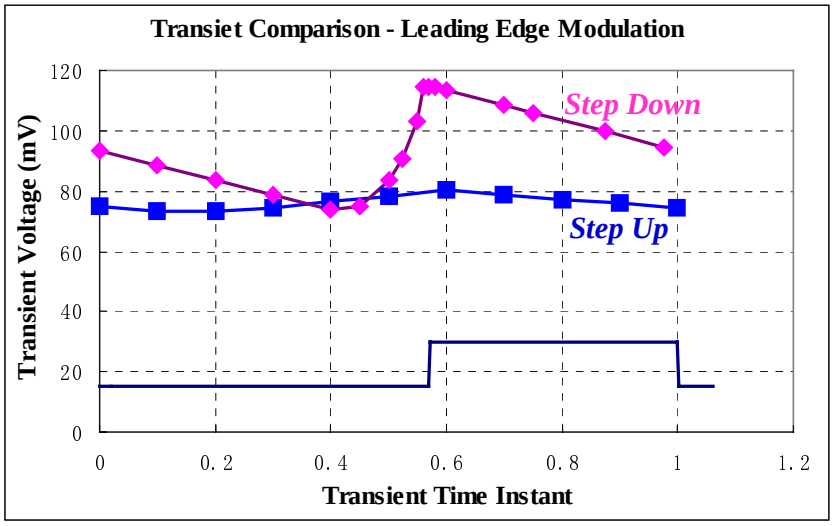


Fig. A.9. Load transition time instant effects on transient voltage spikes.

For the leading-edge modulation, the worst case of the step-down transient responses corresponds to the case in which the load transition happens at the turn-on edge of the top switch. Similarly, the maximum switching action delay time can be derived from the waveforms shown in Fig. A.8(b), as follows:

$$t_d = T_s \cdot (D + \frac{1-D}{2}) = T_s \cdot (\frac{1+D}{2}). \tag{A.2}$$

It is important to point out that the steady-state duty cycle D in (A.2), which corresponds to the full-load operation, is a little bit larger than that in (A.1), which corresponds to the no-load operation, because of the voltage drops on the parasitic resistances in the circuit.

As can be determined from (A.2), smaller steady-state duty cycles give a smaller switching action delay in step-down transient responses in the worst case.

Usually, due to the low output voltages, the VRM capacitor design is limited by the step-down transient responses. In these cases, trailing-edge modulation gives better balance between the step-up and step-down transient responses than does leading-edge modulation.

In summary, for trailing-edge modulations, the worst case of the switching action delay corresponds to the case in which the load step-up transition happens at the turn-off edge of the top switch. There is no significant switching action delay in load step-down transitions. For leading-edge modulations, the worst case of the switching action delay corresponds to the case in which the load step-down transition happens at the turn-on edge of the top switch. There is no significant switching action delay in load step-up transitions.

A.2 Switching Action Delay in Multi-Channel Interleaving Buck VRMs

For n-channel interleaving buck VRMs, the total inductor current frequency is n times the switching frequency of each channel. For a single buck, the length of the worst case switching action delay is less than a switching cycle. It is expected that for an n-channel interleaving buck VRMs, the length of the worst case switching action delay should not be larger than 1/n of the switching cycle in each channel.

The steady-state inductor current waveforms of a four-channel interleaving buck VRM are shown in Fig. A.10.

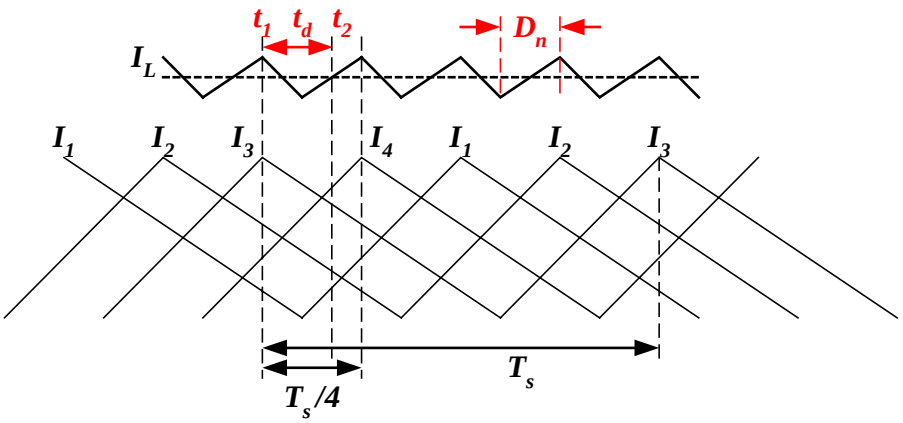


Fig. A.10. Steady-state current waveforms of a four-channel interleaving buck.

As defined in Fig. A.10, D_n is the effective steady-state duty cycle of the total inductor current in an n-channel interleaving buck VRM. D_n is a function of the steady-state duty cycle in each channel and the channel number, as follows:

$$D_n = n \cdot D - \text{int}(n \cdot D), \tag{A.3}$$

where n is the channel number. The function int(x) obtains the integral part of x.

Similar to a single-channel buck, the delay time can be derived from the steady-state current waveforms. For the waveforms shown in Fig. A.10, if trailing edge modulation is assumed, the maximum switching action delay in load step-up transient responses is marked as t_d in the figure, and is determined as follows.

$$t_d = \frac{T_s}{n} \cdot (1 - \frac{D_n}{2}). \tag{A.4}$$

Because of the reduction of the maximum switching action delay, the transient voltage spikes in the worst case should be reduced for multi-channel interleaving VRMs. The comparison of transient voltage spikes of a two-channel interleaving buck VRM and a single-buck VRM are shown in Fig. A.11.

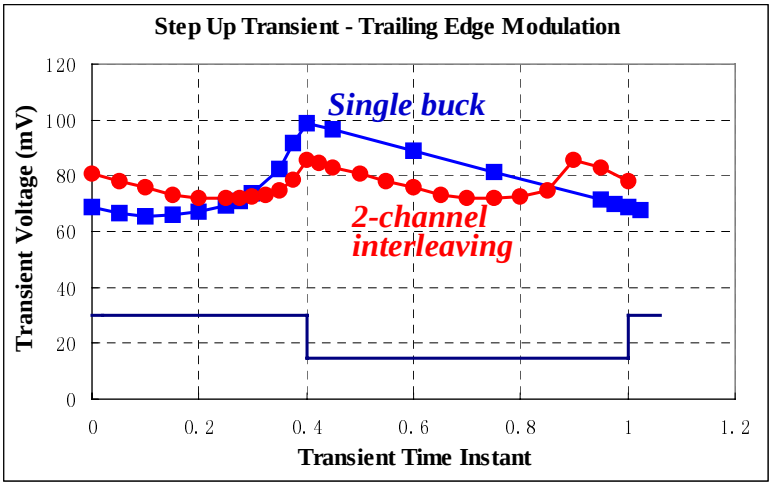


Fig. A.11. Transient voltage spike comparison between a two-channel interleaving buck VRM and a single-buck VRM.

The curves in Fig. A.11 represent the step-up transient voltage spikes that occur when trailing-edge modulation is assumed. The equivalent inductance of the two-channel interleaving buck is the same as the inductance in the single buck. The two converters use same output capacitors. Thus, the small-signal models of the two cases are the same. The same feedback controllers are used in the simulations for the two cases. As shown by the curves, the voltage spike in the worst case is reduced in the two-channel interleaving buck. For step-up transient responses in trailing-edge modulation, the worst case still occurs at the turn-off of the top switches. For the two-channel interleaving topology, there are two worst cases in a switching cycle, which correspond to the two turn-off actions of the top switches in the circuit.

For trailing-edge modulations, the switching action delay is insignificant in the step-down transient responses. The voltage spike curve for the step-down transient responses of a two-channel interleaving buck is exactly the same as that of its corresponding single buck, as shown in Fig. A.7.

A.3 Switching Action Delay's Effect on Critical Inductance

The preceding discussion shows that the factors that affect the switching action delay are the switching frequency, steady-state duty cycle and interleaving channel number. Different inductance values would not affect the switching action delay. As discussed in Section 3.24, the critical inductance will not be affected if the switching action delay is taken into consideration.

However, because the switching action delay is different in step-up and step-down transient responses, it would affect the result of the symmetric transient response. If different step-up and step-down switching action delays are considered, the curves in Fig. 3.18 need to be redrawn, as shown in Fig. A.12.

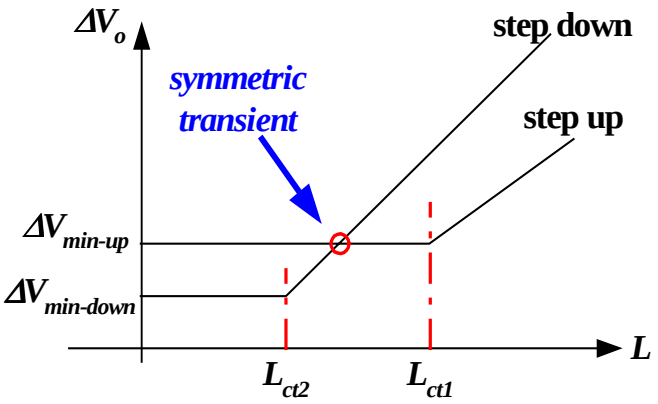


Fig. A.12. Different switching action delays in step-up and step-down transient responses affect the symmetric transient responses.

For the curves shown in Fig. A.12, assume the step-down delay is smaller than the step-up delay time. Thus, the minimum step-down transient voltage spike is smaller than the minimum step-up transient voltage spike, $\Delta V_{min\text{-}down} < \Delta V_{min\text{-}up}$. There is only one inductance value that gives symmetric step-up and step-down transient responses.

For multi-channel interleaving buck VRMs, the switching action delay is greatly reduced. The difference between $\Delta V_{min\text{-}down}$ and $V_{min\text{-}up}$ would be small.

Appendix B

Phase Margin's Effect on Current Rise Time

For power converter feedback control design, there are two important criteria: the bandwidth and the phase margin. Chapter 3 shows that the control bandwidth determines the inductor current rise time. The effect of the phase margin to the rise time is discussed in this section.

Chapter 3 states that the imaginary part of the double poles in the closed-loop current transfer function $G_{iic}(s)$ is the control bandwidth ω_c. The conclusion is based on observation. The phase margin's effect on ω_c is not mentioned. In order to verify this, a power stage is designed with different control bandwidths and phase margins. The imaginary parts of the double poles of $G_{iic}(s)$ under different control loop designs are shown in Fig. B.1.

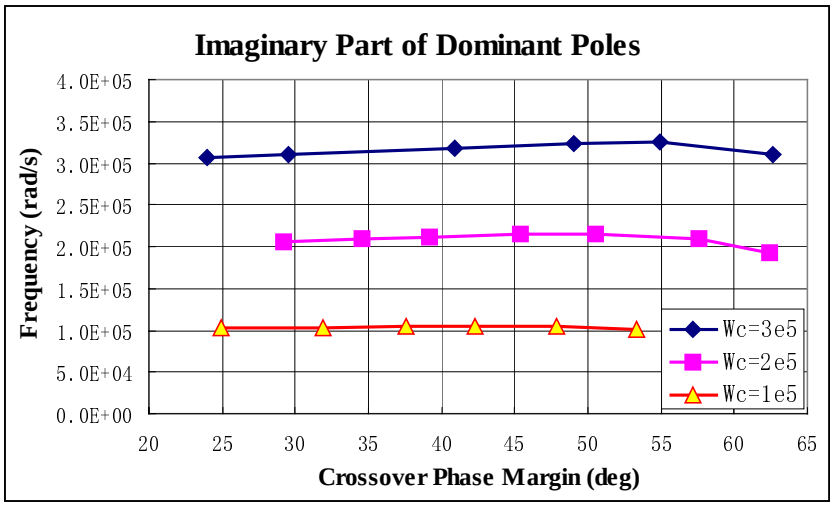


Fig. B.1. Imaginary parts of the poles of $G_{iic}(s)$ are determined by control bandwidth.

From the Fig. B.1, with the control loop phase margin within the range of 20^o - 60^o, the phase margin does not have much impact on the imaginary parts of the dominant double poles of $G_{iic}(s)$. Within this phase margin range, the imaginary part of the dominant double poles of $G_{iic}(s)$ can be approximated as the control bandwidth ω_c.

In Chapter 3, the inductor current rise time is approximated as (B.1) (also (3.7)).

$$t_r = \frac{T_c}{4} = \frac{\pi/2}{\omega_c}. \tag{B.1}$$

How close an approximation can the formula give for different feedback control bandwidths and phase margins? In order to answer this question, a power stage designed with different feedback crossover frequencies and different phase margins is simulated. The inductor current rise time measured from the simulation results are shown in Fig. B.2.

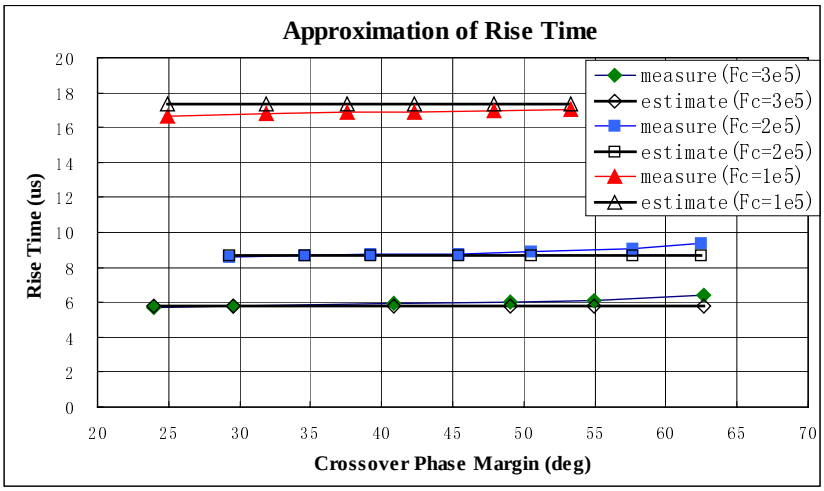


Fig. B.2. Closed-loop current rise time is determined only by control bandwidth.

For comparison, the rise times estimated from (B.1) are also shown in Fig. B.2. For phase margins in the range of 20^o - 60^o, the errors between the two sets

of results are below 5%, which is considered to be a very accurate approximation. This verifies the validity of (B.1) or (3.7).

Another fact shown by the curves in Fig. B.2 is that the rise time begins to increase when the phase margin is too large. From the transient response viewpoint, a small rise time is preferred. A phase margin that is too large slows down the transient responses, which is not desirable for VRMs.

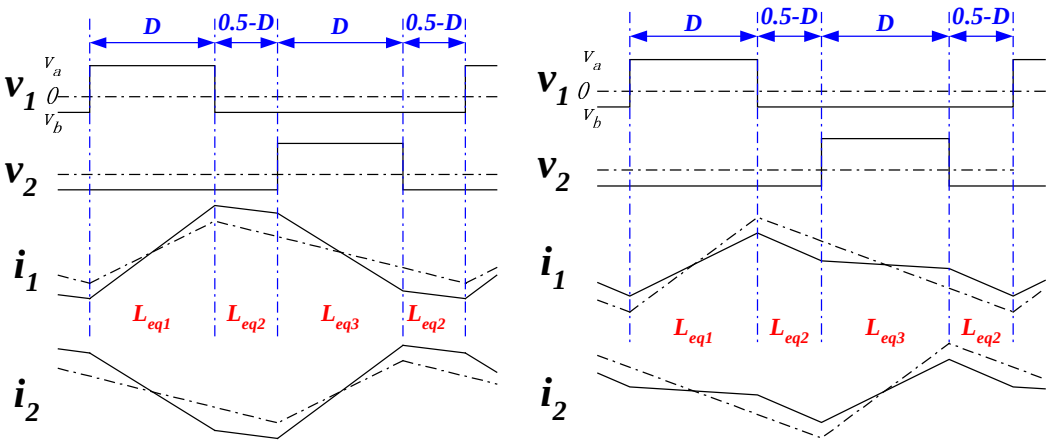
Appendix C

Transient Waveform Analysis of Two-Channel Interleaving VRMs with Coupling Inductors

The inductor current waveforms of the two-channel interleaving buck VRM with coupling inductors during transient responses are more complicated. In this Appendix, the discussions are divided into different cases, based on the range of the steady-state duty cycle D and the range of the transient duty cycle increase.

C.1 Steady-State Duty Cycle D<0.5

For the steady-state duty cycle D<0.5, the steady-state inductor voltage and current waveforms are shown in Fig. C.1 (same as Fig. 4.11).



(a) (b)

Fig. C.1. Steady-state voltage and current waveforms for coupling inductors (D<0.5): (a) direct coupling (M>0); and (b) inverse coupling (M<0).

Because the inductor currents balance in each switching cycle, for both cases of M>0 and M<0, there exists (C.1):

$$\frac{v_a}{L_{eq1}} \cdot D + \frac{v_b}{L_{eq2}} \cdot (1-2 \cdot D) + \frac{v_b}{L_{eq3}} \cdot D = 0 \,. \tag{C.1}$$

The inductor voltage and current waveforms during transient responses for (*0<ΔD<(0.5-D)*) are shown in Fig. C.2 (same as Fig. 4.12).

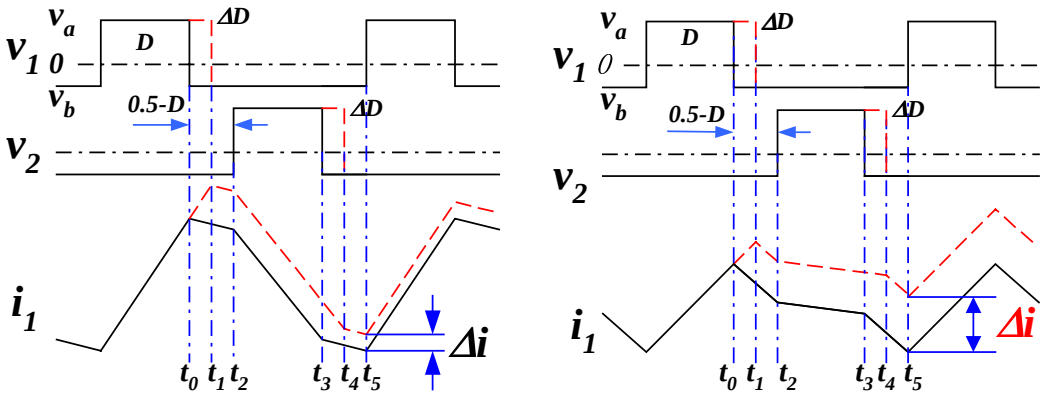


Fig. C.2. Transient voltage and current waveforms for coupling inductors (D<0.5 and 0<ΔD<(0.5-D)): (a) M>0; and (b) M<0.

The current increase can be divided into different time intervals, as follows:

$$\begin{cases} (t_0 - t_1) \mapsto \Delta i_1 = (\dfrac{v_a}{L_{eq1}} - \dfrac{v_b}{L_{eq2}}) \cdot \dfrac{\Delta D}{F_s} \\ (t_1 - t_2) \mapsto \Delta i_2 = (\dfrac{v_b}{L_{eq2}} - \dfrac{v_b}{L_{eq2}}) \cdot \dfrac{(0.5 - D - \Delta D)}{F_s} = 0 \\ (t_2 - t_3) \mapsto \Delta i_3 = (\dfrac{v_b}{L_{eq3}} - \dfrac{v_b}{L_{eq3}}) \cdot \dfrac{D}{F_s} = 0 \\ (t_3 - t_4) \mapsto \Delta i_4 = (\dfrac{v_b}{L_{eq3}} - \dfrac{v_b}{L_{eq2}}) \cdot \dfrac{\Delta D}{F_s} \\ (t_4 - t_5) \mapsto \Delta i_5 = (\dfrac{v_b}{L_{eq2}} - \dfrac{v_b}{L_{eq2}}) \cdot \dfrac{(0.5 - D - \Delta D)}{F_s} = 0 \end{cases} . \tag{C.2}$$

Formula (C.2) is valid for both cases of M>0 and M<0. The total current increase after one switching cycle is

$$\Delta i = \sum_{k=1}^{5} \Delta i_k = \left(\frac{v_a}{L_{eq1}} - \frac{2 \cdot v_b}{L_{eq2}} + \frac{v_b}{L_{eq3}}\right) \cdot \frac{\Delta D}{F_s} . \tag{C.3}$$

Replacing $\frac{v_b}{L_{eq3}}$ with (C.1), (C.3) can be simplified as (C.4):

$$\Delta i = -\frac{1}{D} \cdot \frac{v_b \cdot \Delta D}{L_{eq2} \cdot F_s} = \frac{V_{in} \cdot \Delta D}{L_{eq2} \cdot F_s} . \tag{C.4}$$

The transient inductor voltage and current waveforms for $(0.5 - D) < \Delta D < 0.5$ are shown in Fig. C.3.

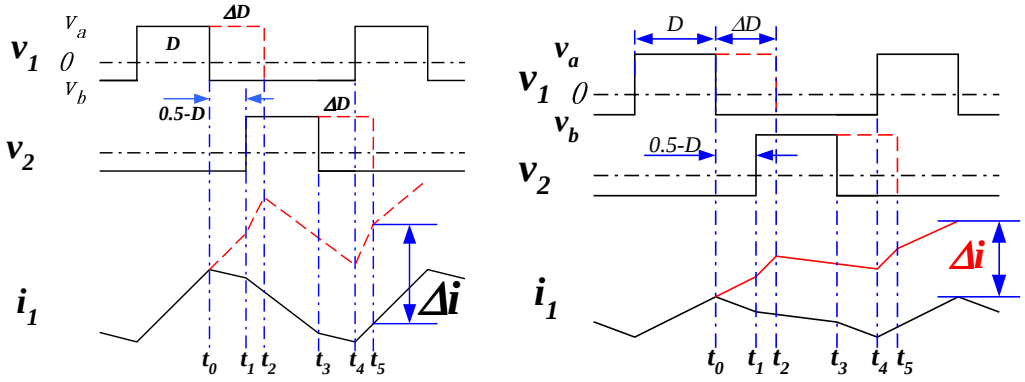


Fig. C.3. Transient voltage and current waveforms for coupling inductors (D<0.5 and (0.5-D)<ΔD<0.5): (a) M>0; and (b) M<0.

A similar equation set of the current increases in different time intervals is shown in (C.5):

$$\begin{cases} (t_0 - t_1) \mapsto \Delta i_1 = (\dfrac{v_a}{L_{eq1}} - \dfrac{v_b}{L_{eq2}}) \cdot \dfrac{(0.5 - D)}{F_s} \\ (t_1 - t_2) \mapsto \Delta i_2 = (\dfrac{v_a}{L_{eq2}} - \dfrac{v_b}{L_{eq3}}) \cdot \dfrac{(\Delta D - (0.5 - D))}{F_s} \\ (t_2 - t_3) \mapsto \Delta i_3 = (\dfrac{v_b}{L_{eq3}} - \dfrac{v_b}{L_{eq3}}) \cdot \dfrac{(0.5 - \Delta D)}{F_s} = 0 \\ (t_3 - t_4) \mapsto \Delta i_4 = (\dfrac{v_b}{L_{eq3}} - \dfrac{v_b}{L_{eq2}}) \cdot \dfrac{(0.5 - D)}{F_s} \\ (t_4 - t_5) \mapsto \Delta i_5 = (\dfrac{v_a}{L_{eq2}} - \dfrac{v_a}{L_{eq1}}) \cdot \dfrac{(\Delta D - (0.5 - D))}{F_s} \end{cases} . \quad \text{(C.5)}$$

Formula (C.5) is valid for both cases of M>0 and M<0. The total current increase after one switching cycle can be expressed as follows:

$$\Delta i = \sum_{k=1}^{5} \Delta i_k = \cdots = (\frac{2 \cdot v_a}{L_{eq2}} - \frac{v_a}{L_{eq1}} - \frac{v_b}{L_{eq3}}) \cdot \frac{\Delta D}{F_s} = \frac{v_{in}}{L_{eq2}} \cdot \frac{\Delta D}{F_s} . \quad \text{(C.6)}$$

The transient inductor voltage and current waveforms for $0.5 < \Delta D < (1 - D)$ are shown in Fig. C.4.

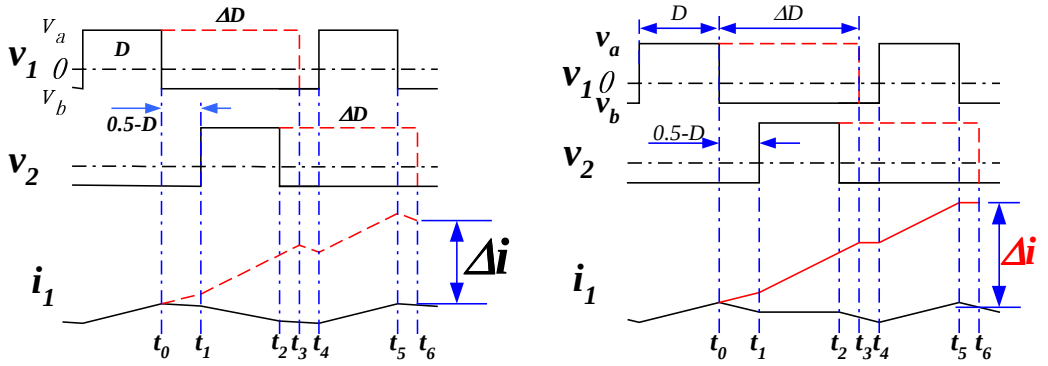


Fig. C.4. Transient voltage and current waveforms for coupling inductors (D<0.5 and 0.5<ΔD<(1-D)): (a) M>0; and (b) M<0.

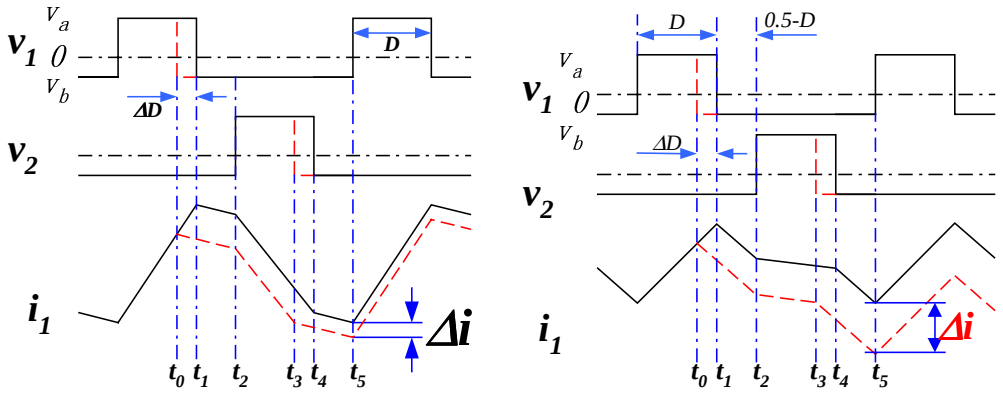
The current increases in different time intervals are described as follows:

$$\begin{cases} (t_0 - t_1) \mapsto \Delta i_1 = (\dfrac{v_a}{L_{eq1}} - \dfrac{v_b}{L_{eq2}}) \cdot \dfrac{(0.5 - D)}{F_s} \\ (t_1 - t_2) \mapsto \Delta i_2 = (\dfrac{v_a}{L_{eq2}} - \dfrac{v_b}{L_{eq3}}) \cdot \dfrac{D}{F_s} \\ (t_2 - t_3) \mapsto \Delta i_3 = (\dfrac{v_a}{L_{eq2}} - \dfrac{v_b}{L_{eq2}}) \cdot \dfrac{(\Delta D - 0.5)}{F_s} \\ (t_3 - t_4) \mapsto \Delta i_4 = (\dfrac{v_b}{L_{eq3}} - \dfrac{v_b}{L_{eq2}}) \cdot \dfrac{(1 - D - \Delta D)}{F_s} \\ (t_4 - t_5) \mapsto \Delta i_5 = (\dfrac{v_a}{L_{eq2}} - \dfrac{v_a}{L_{eq1}}) \cdot \dfrac{D}{F_s} \\ (t_5 - t_6) \mapsto \Delta i_6 = (\dfrac{v_b}{L_{eq3}} - \dfrac{v_b}{L_{eq2}}) \cdot \dfrac{(\Delta D - 0.5)}{F_s} \end{cases} . \tag{C.7}$$

Formula (C.7) is valid for both cases of M>0 and M<0. The total current increase after one switching cycle can be expressed as follows:

$$\Delta i = \sum_{k=1}^{6} \Delta i_k = \cdots = (\frac{v_a}{L_{eq2}} - \frac{v_b}{L_{eq2}}) \cdot \frac{\Delta D}{F_s} = \frac{v_{in}}{L_{eq2}} \cdot \frac{\Delta D}{F_s} . \tag{C.8}$$

For the load step-down transient responses, there exists $\Delta D < 0$. The transient waveforms for $(-D) < \Delta D < 0$ are shown in Fig. C.5.



(a) (b)

Fig. C.5. Transient voltage and current waveforms for coupling inductors (D<0.5 and -D<ΔD<0): (a) M>0; and (b) M<0.

The current increases in different time intervals are described as follows:

$$\begin{cases} (t_0 - t_1) \mapsto \Delta i_1 = (\dfrac{v_b}{L_{eq2}} - \dfrac{v_a}{L_{eq1}}) \cdot \dfrac{-\Delta D}{F_s} \\ (t_1 - t_2) \mapsto \Delta i_2 = (\dfrac{v_b}{L_{eq2}} - \dfrac{v_b}{L_{eq2}}) \cdot \dfrac{(0.5 - D)}{F_s} = 0 \\ (t_2 - t_3) \mapsto \Delta i_3 = (\dfrac{v_b}{L_{eq3}} - \dfrac{v_b}{L_{eq3}}) \cdot \dfrac{(D + \Delta D)}{F_s} = 0 \cdot \\ (t_3 - t_4) \mapsto \Delta i_4 = (\dfrac{v_b}{L_{eq2}} - \dfrac{v_b}{L_{eq3}}) \cdot \dfrac{-\Delta D}{F_s} \\ (t_4 - t_5) \mapsto \Delta i_5 = (\dfrac{v_b}{L_{eq2}} - \dfrac{v_b}{L_{eq2}}) \cdot \dfrac{(0.5 - D)}{F_s} = 0 \end{cases} \tag{C.9}$$

Formula (C.9) is valid for both cases of M>0 and M<0. The total current increase after one switching cycle can be expressed as follows:

$$\Delta i = \sum_{k=1}^{5} \Delta i_k = (-\frac{v_a}{L_{eq1}} + \frac{2 \cdot v_b}{L_{eq2}} - \frac{v_b}{L_{eq3}}) \cdot \frac{-\Delta D}{F_s} = \frac{v_{in} \cdot \Delta D}{L_{eq2} \cdot F_s} . \tag{C.10}$$

Considering (C.4), (C.6), (C.8) and (C.10), for steady-state duty cycle D<0.5, and for the whole possible transient duty cycle range (*-D<ΔD<(1-D)*), although the inductor current waveforms are different, they can be described in exactly the same formula:

$$\Delta i = \frac{v_{in} \cdot \Delta D}{L_{eq2} \cdot F_s} . \tag{C.11}$$

C.2 Steady-State Duty Cycle D>0.5

Although the case of steady-state duty cycle D>0.5 is not practical for VRM applications, it is also analyzed briefly as follows to give a complete picture. The steady-state current and voltage waveforms (both M>0 and M<0) for D>0.5 are compared with the non-coupling case, in Fig. C.6.

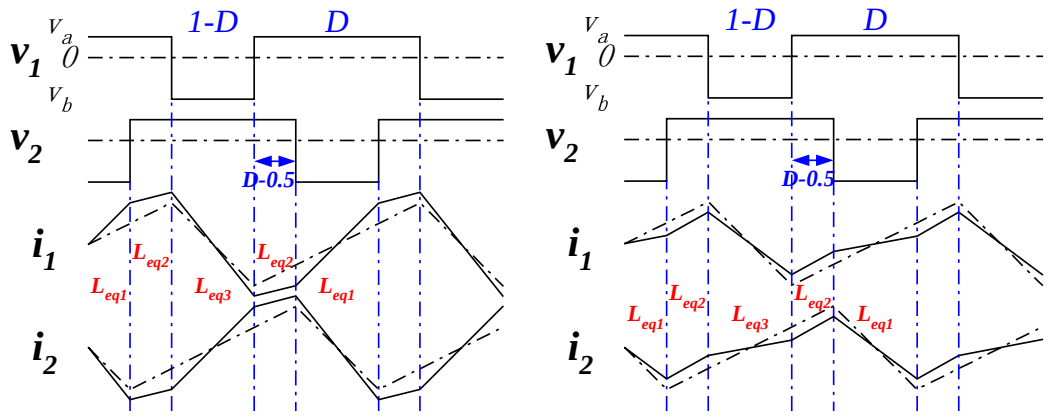


Fig. C.6. Steady-state voltage and current waveforms for coupling inductors (D>0.5): (a) (M>0); and (b) (M<0).

The steady-state peak-to-peak current ripples can be determined as follows:

$$I_{pp\_cp(D>0.5)} = \frac{-v_b \cdot D'}{L_{eq3} \cdot F_s} = \frac{v_a \cdot D}{L_{eq3} \cdot F_s} . \tag{C.12}$$

Compared with the steady-state current ripple formula for D<0.5 in (4.18), L_{eq3} can be defined as the steady-state equivalent inductance for the case in which D>0.5.

Similarly, the relationship between the different equivalent inductances and the steady-state duty cycle can be found as follows:

$$\frac{v_a}{L_{eq1}} \cdot D' + \frac{v_a}{L_{eq2}} \cdot (1 - 2 \cdot D') + \frac{v_b}{L_{eq3}} \cdot D' = 0 . \tag{C.13}$$

The transient inductor voltage and current waveforms for $0 < \Delta D < (1 - D)$ are shown in Fig. C.7.

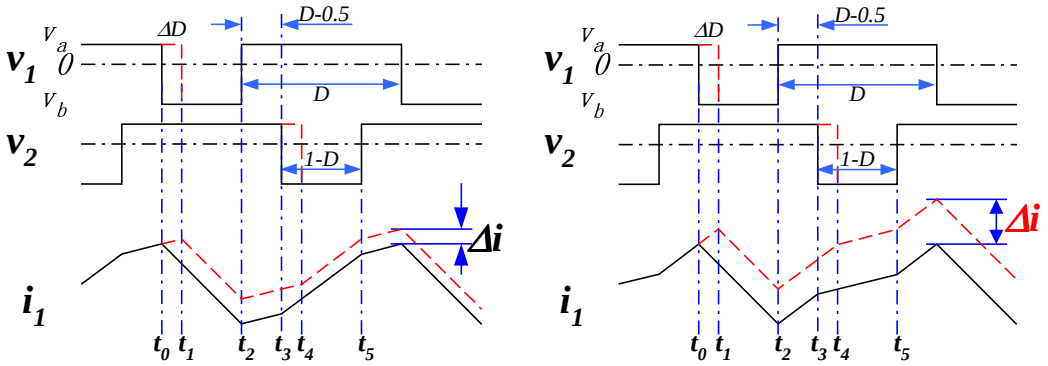


Fig. C.7. Transient voltage and current waveforms for coupling inductors (D>0.5 and 0<ΔD<(1-D)): (a) M>0; and (b) M<0.

The current increases in different time intervals are described as follows:

$$\begin{cases} (t_0 - t_1) \mapsto \Delta i_1 = (\dfrac{v_a}{L_{eq2}} - \dfrac{v_b}{L_{eq3}}) \cdot \dfrac{\Delta D}{F_s} \\ (t_1 - t_2) \mapsto \Delta i_2 = (\dfrac{v_b}{L_{eq3}} - \dfrac{v_b}{L_{eq3}}) \cdot \dfrac{(D' - \Delta D)}{F_s} = 0 \\ (t_2 - t_3) \mapsto \Delta i_3 = (\dfrac{v_a}{L_{eq2}} - \dfrac{v_a}{L_{eq2}}) \cdot \dfrac{(D - 0.5)}{F_s} = 0 \\ (t_3 - t_4) \mapsto \Delta i_4 = (\dfrac{v_a}{L_{eq2}} - \dfrac{v_a}{L_{eq1}}) \cdot \dfrac{\Delta D}{F_s} \\ (t_4 - t_5) \mapsto \Delta i_5 = (\dfrac{v_a}{L_{eq1}} - \dfrac{v_a}{L_{eq1}}) \cdot \dfrac{(D' - \Delta D)}{F_s} = 0 \end{cases} . \quad \text{(C.14)}$$

The total current increase after one switching cycle is

$$\Delta i = \sum_{k=1}^{5} \Delta i_k = (-\frac{v_a}{L_{eq1}} + \frac{2 \cdot v_a}{L_{eq2}} - \frac{v_b}{L_{eq3}}) \cdot \frac{\Delta D}{F_s} . \quad \text{(C.15)}$$

Replacing $\dfrac{v_b}{L_{eq3}}$ with (C.13), (C.15) can be simplified as follows:

$$\Delta i = -\frac{1}{D'} \cdot \frac{v_a \cdot \Delta D}{L_{eq2} \cdot F_s} = \frac{v_{in} \cdot \Delta D}{L_{eq2} \cdot F_s} \cdot . \tag{C.16}$$

The transient voltage and current waveforms for the cases in which $\Delta D<0$ are not shown here. The analysis shows that for the cases of $D>0.5$ and $\Delta D<0$, (C.16) is also valid.

In summary, for all the cases of $D>0.5$ or $D<0.5$ and $(-D)<\Delta D<(1-D)$, the transient inductor current increase during transient responses can all be described as (D.11). This is consistent with the conclusion drawn in Chapter 4. The transient responses are determined only by L_{eq2}, which is defined as the transient equivalent inductance.

Appendix D

Coupling Effect on Inductor Current Ripples

For coupling inductors in the two interleaving channel with 180^{o} phase shift, the relationship between the coupling effects and the steady-state inductor peak-to-peak current ripples is shown in (4.25) and Fig. 4.17. This Appendix explains and illustrates this relationship.

The different coupling inductor designs keep the same transient equivalent inductance L_{eq2}. For the steady-state duty cycle range D<0.5, the steady-state inductor current waveforms of different coupling effects are shown in Fig. D.1.

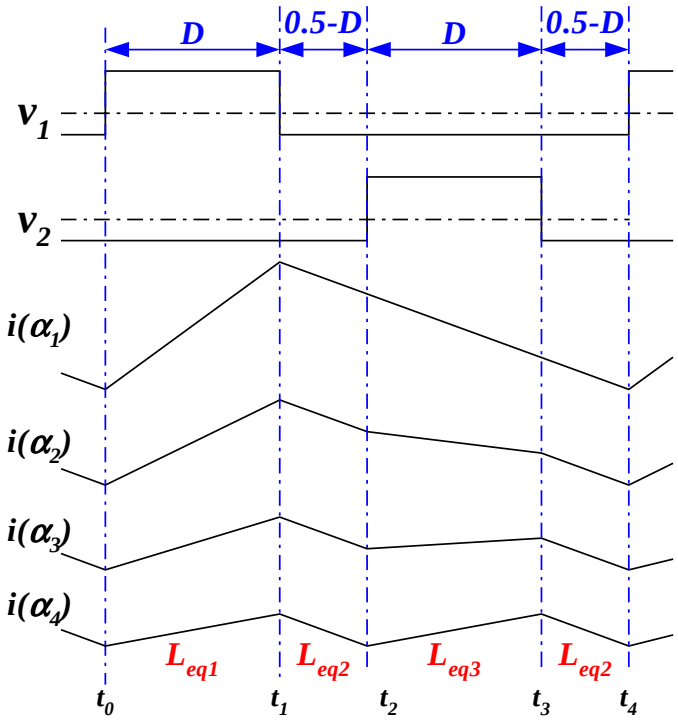


Fig. D.1. Steady-state inductor current waveforms of different coupling effects.

The inductor current waveforms shown in Fig. D.1 correspond to different coupling effects ($0=\alpha_1>\alpha_2>\alpha_3>\alpha_4\rightarrow -1$). Because of the same transient equivalent inductance L_{eq2}, the current slopes in the time intervals of (t_1-t_2) and (t_3-t_4) are the same for the different coupling effects. As shown in Fig. D.1, the current slope during the time intervals of (t_2-t_3) can be either positive or negative. This can also be derived from the equation of the equivalent inductance L_{eq3}. For D<0.5, the equivalent inductance during (t_2-t_3) is as follows (same as (4.14)):

$$L_{eq3}=\frac{1-\alpha^2}{1+\frac{D'}{D}\cdot\alpha}\cdot L=\frac{1-\alpha}{1+\frac{D'}{D}\cdot\alpha}\cdot L_{eq2}\,. \tag{D.1}$$

For

$$0>\alpha>-\frac{D}{D'}, \tag{D.2}$$

there exists

$$L_{eq3}>0, \tag{D.3}$$

while for

$$\alpha<-\frac{D}{D'}, \tag{D.4}$$

there exists

$$L_{eq3}<0\,. \tag{D.5}$$

For the four cases shown in Fig. D.1, there exists

$$0=\alpha_1>\alpha_2>-\frac{D}{D'}>\alpha_3>\alpha_4\rightarrow -1\,. \tag{D.6}$$

For the cases of L_{eq3}>0, it is clear that the peak-to-peak current in a switch cycle can be easily written in the format of L_{eq1} as follows (same as (4.18)):

$$I_{pp\_cp(D<0.5)} = \frac{V_{in} \cdot D \cdot (1-D)}{F_s \cdot L_{eq1}}. \tag{D.7}$$

For the cases of L_{eq3}<0, if it can be proved that the current increase during the time interval of (t_1-t_2) is larger than the current decrease during the time interval of (t_2-t_3), the peak-to-peak current in a switch cycle can also be described in (D.7). The current increase during (t_1-t_2) has the same expression as (D.7) as follows:

$$\Delta I_{12} = \frac{v_a \cdot D}{F_s \cdot L_{eq1}} = \frac{V_{in} \cdot D' \cdot D}{F_s \cdot L_{eq1}}. \tag{D.8}$$

The current change during (t_2-t_3) can be expressed in (D.9).

$$\Delta I_{23} = \frac{v_b \cdot (0.5-D)}{F_s \cdot L_{eq2}} = \frac{V_{in} \cdot D \cdot (0.5-D)}{F_s \cdot L_{eq2}}. \tag{D.9}$$

Similar to (D.1), L_{eq1} can also be written in the format of L_{eq2} as follows:

$$L_{eq1} = \frac{1-\alpha^2}{1+\frac{D}{D'}\cdot\alpha} \cdot L = \frac{1-\alpha}{1+\frac{D}{D'}\cdot\alpha} \cdot L_{eq2}. \tag{D.10}$$

Substituting (D.10) into (D.8), ΔI_{12} can be rewritten as follows:

$$\Delta I_{12} = \frac{V_{in} \cdot D}{F_s \cdot L_{eq2}} \cdot \frac{D' + D \cdot \alpha}{1-\alpha}. \tag{D.11}$$

Because 0>α>-1, (D.11) satisfies formula (D.12)

$$\Delta I_{12} = \frac{V_{in} \cdot D}{F_s \cdot L_{eq2}} \cdot \frac{D' + D \cdot \alpha}{1-\alpha} > \frac{V_{in} \cdot D}{F_s \cdot L_{eq2}} \cdot \frac{1-2 \cdot D}{1-(-1)} = \Delta I_{23}. \tag{D.12}$$

Formula (D.12) proves that for the cases of D<0.5, the peak-to-peak inductor current in a switch cycle can be simply expressed as (D.7). This is the reason L_{eq1} is the steady-state equivalent inductance. Formula (D.12) shows that for a certain transient equivalent inductance, the inductor current ripple is a function of duty cycle and the coupling effect as follows:

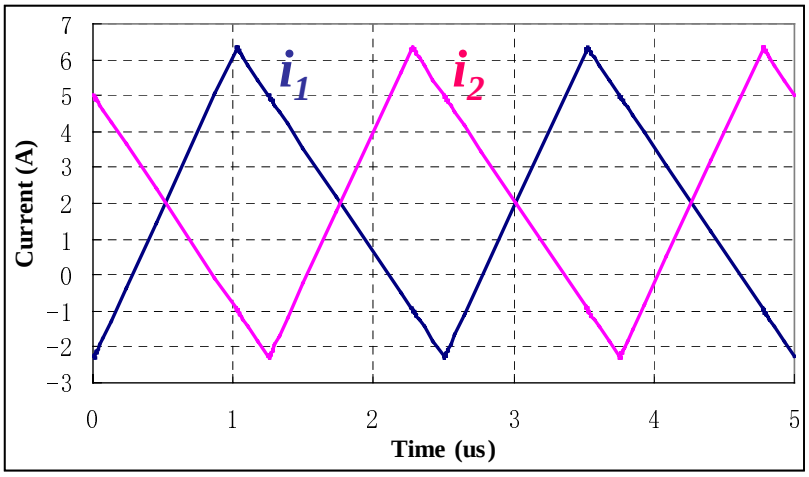
$$I_{pp(D<0.5)} = \frac{V_{in} \cdot D}{F_s \cdot L_{eq2}} \cdot \frac{D' + D \cdot \alpha}{1-\alpha}. \tag{D.13}$$

Comparing to the non-coupling inductors, the peak-to-peak current ratio due to the coupling effects can be derived as follows (same as (4.25)):

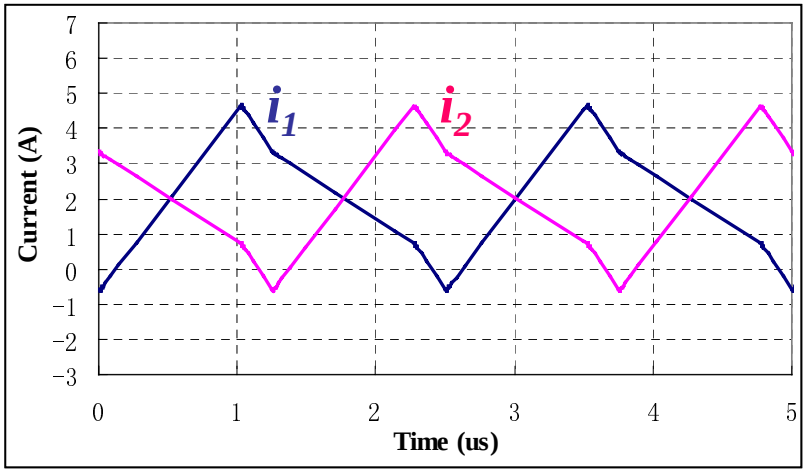
$$\frac{I_{pp\_cp(D<0.5)}}{I_{pp\_nc}} = \frac{L_{nc}}{L_{eq1}} = \frac{1+\frac{D}{D'} \cdot \alpha}{1-\alpha}. \tag{D.14}$$

It is can also clear from (D.12) that when $\alpha \to -1$, $\Delta I_{12} \to \Delta I_{23}$, which corresponds to the current waveform $i(\alpha_4)$ shown in Fig. D.1. In this case, the frequency of the inductor current in each channel is twice the switching frequency. However, this is only an unreal case. Because $L_{eq2}=L+M$ requires to be a finite value, there always exists $M<L$. The case of $\alpha \to -1$ happens only when $L \to \infty$, which is impossible. Moreover, as shown in (4.30), when strong coupling effect is used ($\alpha \to -1$), a tiny unbalance between the channel currents results in huge flux unbalance in the legs. This makes the strong coupling between channels impractical.

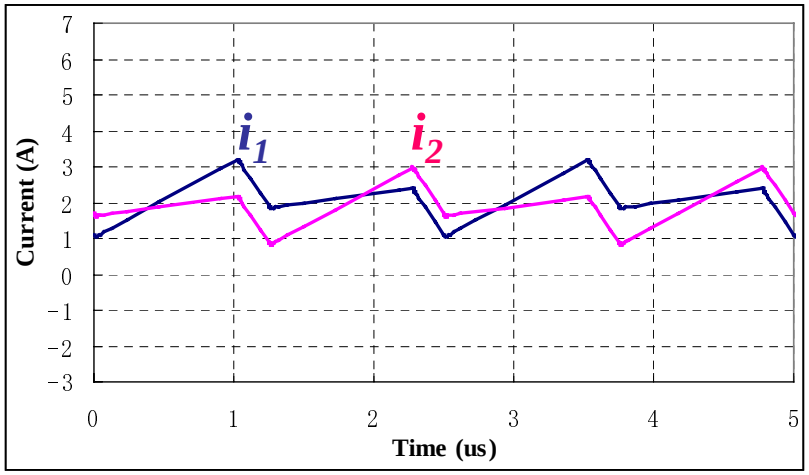
The simulation inductor current waveforms of different coupling effects are shown in Fig. D.2.



(a)



(b)



(c)

Fig. D.2. Simulation inductor current waveforms of same L_{eq2} and different α: (a) α=0; (b) α=0.3; (c) α=0.8.

For the three cases shown in Fig. D.2, the transient equivalent inductance are the same: L_{eq2}=350nH. The steady-state duty cycle is 0.4. As discussed in (D.2-5), the boundary of the negative L_{eq3} is α=2/3. Thus, case (c) has negative L_{eq3}. The curves in the figure show that stronger coupling effects result in smaller inductor current ripples. The simulation results verify the discussion shown in Fig. D.1.

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