Characterization and Modeling of High-Switching-Speed Behavior of SiC Active Devices

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Abstract

To support the study of potential utilization of the emerging silicon carbide (SiC) devices, two SiC active switches, namely 1.2 kV, 5 A SiC JFET manufactured by SiCED, and 1.2 kV, 20 A SiC MOSFET by CREE, have been investigated systematically in this thesis. The static and switching characteristics of the two switches have firstly been characterized to get the basic device information. Specific issues in the respective characterization process have been explored and discussed. Many of the characterization procedures presented are generic, so that they can be applied to the study of any future SiC unipolar active switches.

Based on the characterization data, different modeling procedures have also been introduced for the two SiC devices. Considerations and measures about model improvement have been investigated and discussed, such as predicting the MOSFET transfer characteristics under high drain-source bias from switching waveforms. Both models have been verified by comparing simulation waveforms with the experimental results. Limitations of each model have been explained as well.

In order to capture the parasitic ringing in the very fast switching transients, a modeling methodology has also been proposed considering the circuit parasitics, with which a device-package combined simulation can be conducted to reproduce the detailed switching waveforms during the commutation process. This simulation, however, is

inadequate to provide deep insights into the physics behind the ringing. Therefore a parametric study has also been conducted about the influence of parasitic impedances on the device's high-speed switching behavior. The main contributors to the parasitic oscillations have been identified to be the switching loop inductance and the device output junction capacitances. The effects of different parasitic components on the device stresses, switching energies, as well as electromagnetic interference (EMI) have all been thoroughly analyzed, whose results exhibit that the parasitic ringing fundamentally does not increase the switching loss but worsens the device stresses and EMI radiation.

Based on the parametric study results, this thesis finally compares the difference of SiC JFET and MOSFET in their respective switching behavior, comes up with the concept of device switching speed limit under circuit parasitics, and establishes a general design guideline for high-speed switching circuits on device selection and layout optimization.

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Chapter 1 Introduction

1.1 Silicon Carbide Power Devices

The development of power semiconductor devices has always been a driving force for power electronics systems. For a long time silicon-based power devices have dominated the power electronics and power system applications. As the needs and requirements for electric energy continuously grow nowadays, silicon (Si) devices are coming to face some fundamental limits in performance due to the inherent limitations of Si material properties, which make them incompetent for future demands, especially in high-voltage, high-efficiency, and high-power-density applications. For example, presently Si insulated-gate bipolar transistors (IGBTs) are able to handle high voltage over 5 kV and high current over 1000 A, whereas the bipolar nature of the device limits the switching frequency of converter systems below 100 kHz and thus the efficiency and integration of the system [1]. On the other hand, Si metal-oxide-semiconductor field effect transistors (MOSFETs), although ideal for high-switching-frequency applications up to MHz, suffer from relatively high on-state resistance and hence high conduction loss as the blocking voltage increases, which virtually constrains the use of the device in medium and low voltage applications less than 600 V. What is more, the general 150 °C limit of maximum

junction temperature further hinders the use of Si devices in high-power-density and high-temperature situations.

The emerging silicon carbide (SiC) technology is bringing solutions to all the above problems, thanks to its superior material properties compared to Si. Being a wide bandgap material, SiC offers a critical electric field of 2.0×10^6 V/cm – an order of magnitude higher than Si. This increases the blocking capability of SiC power devices and also allows them to be fabricated with much thinner and higher doped drift layers, significantly reducing the on-state resistance. The high thermal conductivity of SiC (4.9 W/cm·K) enhances heat dissipation and, coupled with the wide bandgap energy (3.3 eV), allows high-temperature operation above 300 °C. All of the above advantages make the SiC power devices an ideal substitution for Si counterparts in future high-voltage and high-power converter systems [2-5].

Table 1-1 compares some of the properties of Si and SiC [2].

Table 1-1. Comparison of Si and SiC material properties

Parameter	Si	4H-SiC	Unit
Bandgap energy	1.1	3.3	eV
Relative permittivity	11.8	10	-
Critical electric field	0.3	2.0	MV/cm
Electron saturated drift velocity	1.0	2.0	$\times 10^7$ cm/s
Thermal conductivity	1.5	4.9	W/cm·K

The great advantages of SiC have urged the commercialization of SiC Schottky barrier diode by Infineon and CREE since 2001, which features ultra-fast turn-on speed and almost zero reverse recovery effect [4, 6, 7]. Regarding the SiC active switches in development, the main research focus now is directed at the unipolar devices of JFET and

MOSFET for voltages starting from 600 V up to approximately 2 kV, with a clear target of 1.2 kV blocking voltage, although higher voltage level devices are also under study and development [5, 12-13]. So far, SiCED has developed their 1.2 kV, normally-on SiC JFET with an on-state resistance as low as 100 mΩ, while CREE claims their 1.2 kV, 20 A normally-off SiC MOSFETs are already nearing commercial viability [8-11]. Compared to conventional devices with the same voltage rating, these SiC active switches provide much lower on-state resistance than Si MOSFET and much higher switching speed than Si IGBT, which is promising to resolve the trade-off between high frequency and high efficiency for 600-800 V energy conversion systems.

1.2 Research Motivations and Objectives

With great progress in the improvement of SiC active switches, much effort has been invested in studying the SiC JFET and MOSFET characteristics and their potential utilization in power converter systems. Temperature-dependent characteristics of the two devices have been extensively studied [14-18]. Different physics-based and behavioral device models have also been developed for SiC JFET and MOSFET [18-23]. The potential utilization of the devices has been widely explored as well by many researchers [24-30].

This thesis, from another angle, studies the high-switching-speed behavior of SiC JFET and MOSFET which did not receive much attention previously. The background of this work is to support the development of a high-frequency isolated DC-AC-DC converter aiming at reducing the passive component sizes and boosting system power density. To achieve this goal, SiC JFETs from SiCED and SiC MOSFETs from CREE,

both with 1.2 kV voltage rating, will be fully characterized in this thesis. Important issues which are previously overlooked during the characterization processes will be explained and discussed in detail. To favor the analyses of device switching behavior, SiC JFET and MOSFET models will also be built based on the characterization results. Different from some preceding work, the modeling procedures presented in this thesis will provide full inclusion of device electrical characteristics and easy extraction process of model parameters. Issues regarding the model accuracy will be discussed and solutions will be provided as well.

The parasitic impedances of the switching circuit are another focus of this work besides the devices. The influence of the parasitics becomes more and more remarkable in form of parasitic ringing when the device switching speed is approaching the limit. This thesis will, for the first time, systematically study the individual effects of the parasitic inductances and capacitances on the device's switching characteristics, and try to analyze the ringing mechanism from the interactions between them. Extensive simulations with the use of device models will also be conducted accompanying the experiments to help better understand the high-switching-speed behavior of these SiC switches.

Finally, based on the study results of the devices and parasitics, this thesis will be able to explain and compare the differences of SiC JFET and MOSFET in their respective switching characteristics, and come up with a new concept of switching speed limit for a power device. A design guideline will also be established regarding the device selection and circuit layout optimization for high-speed switching circuits.

1.3 Thesis Organization

Based on the above objectives, the thesis is thus organized as follows.

Chapter 2 introduces the general study approaches used in the thesis that are common for both SiC JFET and SiC MOSFET. Chapter 3 and 4 conduct the extensive static and switching characterizations on the two devices. Based on the characterization data different device modeling procedures are presented and relative modeling issues are discussed for improving accuracy. The device models, however, are not able to predict the high-frequency ringing during switching transients because the circuit parasitics are not considered in the simulation. To resolve this, in Chapter 5 a complete modeling process is presented to model the entire switching circuit including the interconnect parasitics. Though with all the models a device-package combined simulation can be run to accurately reproduce the detailed ringing waveforms, the simulation results still do not provide too much insight into the high-speed-switching behavior of the devices. Therefore, in Chapter 6 the ringing mechanism is analyzed thoroughly through the parametric study on the parasitic impedances. From the experimental and simulation results, the effect of each parasitic parameter is identified and qualitatively explained. According to the study, Chapter 7 compares the differences between SiC JFET and MOSFET in their respective switching behavior, and proposes a design guideline for high-speed switching circuits. Some future work is also suggested in Chapter 7.

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Chapter 2 General Approaches of Study

2.1 Introduction

Although certain characterization issues and modeling procedures are specific to SiC JFET or SiC MOSFET, there are still many study approaches similar or common for both devices. This chapter introduces the general static and switching characterization processes, terminologies, device switching behavior, etc, which are applicable to both SiC JFET and SiC MOSFET, so that these contents will not have to be repeated in their own chapters. However, particular characteristics and issues of each device will still be discussed in Chapter 3 and Chapter 4 respectively.

2.2 Static Characterization Approaches and Terminology

Static characteristics are the most basic evaluations of the performance of a power semiconductor device (For generality, called device under test, or DUT, hereafter), which include the DC characteristics (current-voltage relationship, I-V) and AC characteristics (impedances). For SiC JFET and SiC MOSFET, DC characteristics are mainly represented by the blocking capability, output and transfer characteristics, on-state resistance, and body diode I-V curves, which are measured with a Tektronix 371B curve

tracer in this work. The AC characteristics include the internal gate resistance, nonlinear junction capacitances, as well as package parasitic inductances, which can be measured using an Agilent 4294A impedance analyzer. All these parameters are directly related to the performance evaluation and modeling of the device.

Characteristics of semiconductor devices are also sensitive to the operating temperature. For the temperature-dependent characterizations, an additional heating device can be used to heat the DUT, since neither of the above mentioned instruments can handle elevated temperatures. An example of the measurement setup with the use of the curve tracer is shown in Figure 2-1. As seen, a hotplate is used to control the DUT junction temperature, which is measured by a thermometer with a T-type thermocouple attached to the device case. The GPIB (General Purpose Interface Bus) controller is used to send commands to the curve tracer and collect the measurement data.

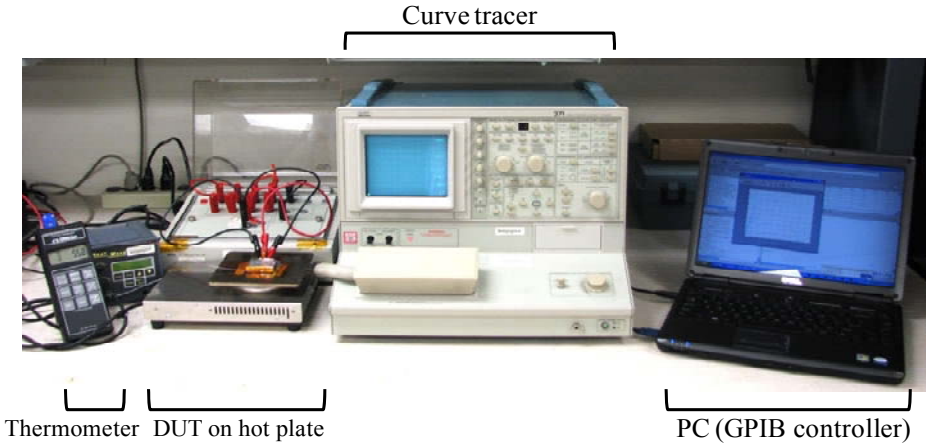

Figure 2-1. Static characterization setup with curve tracer

2.2.1 Pre-Characterization Precautions

There are several issues that need to be aware of before characterizations in order to achieve accurate and meaningful measurements.

(1) Kelvin sensing

Contact and wire resistances may cause measurement error under High Current Mode of the curve tracer. Kelvin sensing (or four-terminal sensing) thus should be used to eliminate this error. Conventional device packages (e.g. TO-220 or TO-247) can usually fit into the curve tracer adapter panel with the use of a test adapter such as Tektronix A1002, and in this condition Kelvin sensing is ensured [1]. However, if the device package cannot fit into any test adapter, like the SiC MOSFET to be presented in Chapter 5, wires have to be used for interconnection. In this condition the wire and contact resistances should also be measured and subtracted off the final results. It is important to do so because the on-state resistance of SiC devices can easily reach as small as 100 mΩ, and the wire resistance can be 30 % to 40 % of that value, causing great relative error.

(2) Temperature control

To ensure that the characterization is conducted under a fixed temperature, it is necessary to pay attention to the junction temperature change of the DUT during the measurement. The curve tracer measures the static I-V curves by switching the DUT with a duty cycle smaller than 0.5 %. However even with this duty cycle, long-time measurement will still cause junction temperature rise. So the measurement data should be collected as quickly as possible to avoid junction temperature change.

(3) Preventing electrostatic discharge (ESD)

ESD can sometimes destroy the MOSFET gate-source oxide layer permanently when the DUT is not properly handled [2]. To protect from ESD, some measures need to be taken when storing or transporting the DUT:

(i) Shorting the gate-source terminals;

(ii) Keeping the DUT in anti-ESD boxes;

(iii) Handling the DUT by the plastic case, not the metal leads;

(iv) Using anti-ESD wrist strap and grounding mat if possible.

2.2.2 Blocking Capability

The device blocking capability can usually be evaluated by two parameters: BV_{DSS} – the drain-source breakdown voltage, and I_{DSS} – the drain leakage current at the rated voltage. Take MOSFET for example. BV_{DSS} of MOSFET is usually defined as the voltage which produces 250 μA drain leakage current with the gate-source terminals shorted. Under this criterion, BV_{DSS} is usually measured to be higher than the rated voltage. However, under elevated temperatures, SiC prototype devices may break down even before the leakage current reaches 250 μA. For mature and rugged devices, all the single cells within the device are uniform in their blocking capability. These devices also have built-in avalanche capability that helps them survive from short-time unexpected over-voltage stress. However, for certain prototype DUTs, some single cells are weaker than the others, which will break down first under high voltage stress, and the resultant damage is usually not recoverable [3-4]. In this case, the DUT is destroyed (i.e. can no longer block voltage) even if the output characteristics still look fine.

To avoid possible damages to the SiC DUTs, I_{DSS} is adopted in this work to evaluate the device blocking capability instead of BV_{DSS}, and is measured under the High Voltage Mode of the curve tracer. Measuring I_{DSS} is relatively safer because the leakage current is obtained under rated V_{DS} voltage with the channel pinched-off.

2.2.3 Output and Transfer Characteristics

The output characteristics are drain current I_D versus drain-source voltage V_{DS} relationships under different gate-source voltages V_{GS}. The transfer characteristic, on the other hand, is I_D vs. V_{GS} for a given V_{DS} bias. These are basic device characteristics and fundamental measurement functions of the curve tracer [1]. The only difference between SiC JFET and SiC MOSFET is the applied gate voltage. For SiC JFET, a negative V_{GS} is required because it is a normally-on device, while for SiC MOSFET the applied V_{GS} is positive.

2.2.4 On-State Resistance $R_{DS(ON)}$

The on-state resistance can be read directly from the output characteristic curves. However there is some ambiguity in the definition of $R_{DS(ON)}$. Some papers define this parameter to be the maximum slope of the output I-V curve for a given turn-on voltage [5-6], but in most datasheets it is defined at a specific drain current, as seen in Figure 2-2. The former definition gives the minimum possible $R_{DS(ON)}$ for a given V_{GS}, however it does not reflect the real device resistance when the drain current is non-zero. Therefore, the latter definition is adopted in this work. Namely, $R_{DS(ON)}$ is taken at a given V_{GS} and I_D.

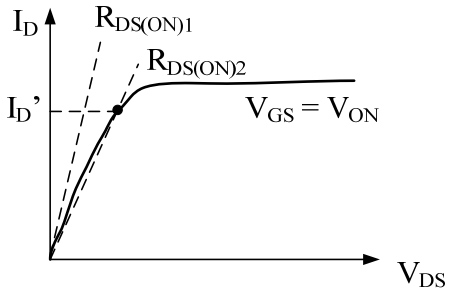

Figure 2-2. Different definitions of $R_{DS(ON)}$

2.2.5 Body Diode I-V Characteristics

Due to the device structure, both SiC JFET and SiC MOSFET have intrinsic body diodes. The measurement of body diode I-V curves is the same process as measuring an ordinary diode using the curve tracer, except that the device channel needs to be pinched off during the measurement. This means applying a negative pinch-off voltage on the gate-source of the SiC JFET, and shorting the gate-source terminals of the SiC MOSFET, when characterizing the body diode. However, neither body diode behaves like a pure PiN or Schottky diode, which will be discussed in Chapter 4 and Chapter 5 respectively.

Other static characteristics are different at least in some way for SiC JFET and SiC MOSFET, and will be discussed in detail in the respective chapters.

2.3 Switching Characterization Approaches and Terminology

2.3.1 Double-Pulse Tester

Two inductive-load double-pulse testers (DPT) have been built to test the switching characteristics of SiC JFET and SiC MOSFET. The testers are essentially step-down converters whose schematics are shown in Figure 2-3 (a) and (b). The only difference between the two testers is the gate drive circuit. In Figure 2-3 (a) a zero-to-negative gate voltage is used to switch the SiC JFET, while in Figure 2-3 (b) a zero-to-positive gate voltage is used for SiC MOSFET. The DUTs are driven by a high-speed, high-current gate driver integrated circuit (IC) IXDD414 from IXYS, with gate bias voltage from -30 V to 0 V for JFET, and 0 V to 15 V for MOSFET. Also seen in Figure 2-3 (a) is an R-C-D network used between the gate driver and the JFET to adapt to the different gate characteristics in case of multi-JFET paralleling [7]. In this configuration the SiC JFET is

working in the gate breakdown mode, and the capacitor in the R-C-D network takes the voltage difference between the JFET gate breakdown voltage and the gate drive turn-off voltage. The configuration, however, is not necessary for SiC MOSFET.

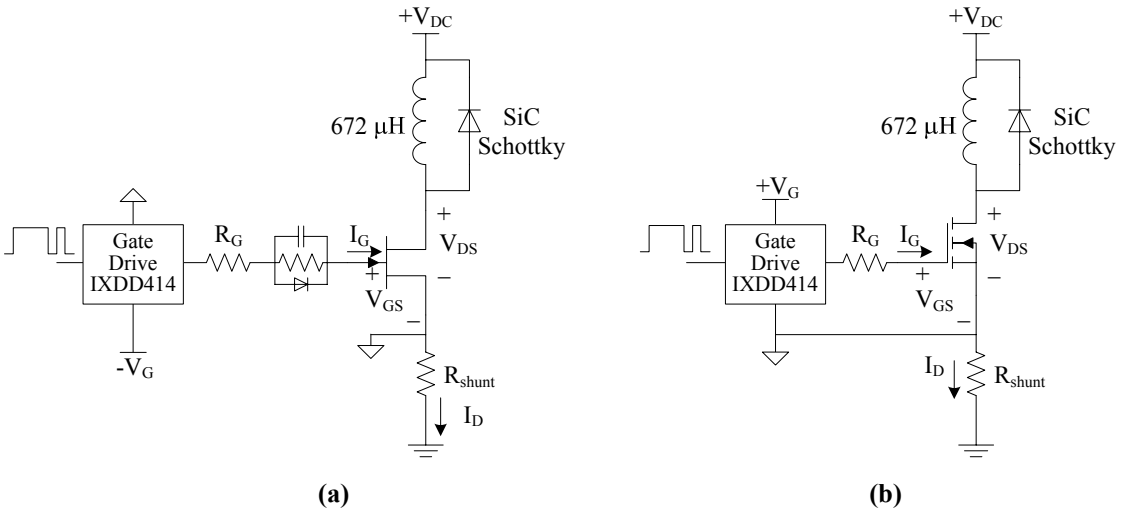

Figure 2-3. Double-pulse tester schematics for SiC JFET (a) and SiC MOSFET (b)

Figure 2-4 displays the typical test waveforms. As seen from the figure, at the end of the first pulse and beginning of the second pulse the device's switching transients can be captured under the pre-set drain-source voltage and drain current conditions. In this sense the devices can be switched under any desired voltage and current stresses. Besides, because each time only two pulses are launched and the DUT is switched only twice, the device junction temperature rise due to the switching loss is reduced to minimum, and the junction temperature can then be controlled externally by a heating device to study the temperature-dependent switching characteristics.

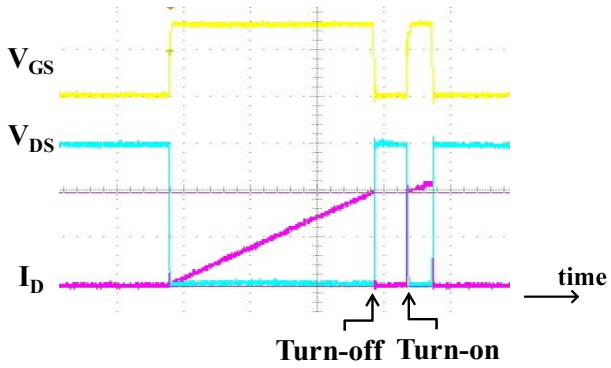

Figure 2-4. Double-pulse test typical switching waveforms

The high-side freewheeling diodes used in both testers are the same 1.2 kV, 20 A prototype SiC Schottky barrier diode (SBD) from Infineon. The use of the SBD can eliminate the reverse recovery effect, and thus limit the current spike of the DUT during turn-on process.

The load inductor is constructed by connecting four equivalent small inductors in series. Each inductor has only one layer of windings so that its equivalent parallel capacitance (EPC) is minimized [8]. Putting four such inductors in series further reduces the total EPC, which results in only 1 pF for the total load inductor.

The drain current of the DUT is also measured through a 0.1 Ω shunt resistance from T&M Research connected in series with the device source terminal. The printed circuit board (PCB) of the tester is designed to achieve minimized parasitic impedances so that the DUT can be switched to its very speed limit without suffering a lot from the parasitic ringing. Detailed design considerations of such a high-speed DPT can be found in [9].

2.3.2 High-Speed Measurement Considerations

The switching characterization of the device basically includes three waveforms, namely gate-source voltage V_{GS}, drain-source voltage V_{DS} and drain current I_D. A coaxial

shunt resistor is chosen for the drain current measurement instead of other measures (e.g. Rogowski coil, current transformer, etc) because of its high bandwidth which does not cause unacceptable aberrations in measuring the fast-changing waveform [10]. In this configuration, all three voltage measurements share the common point of the DUT source terminal, which is then used as the grounding point for the voltage probes. However, the drain current needs to be flipped in the scope to get the correct waveform. Also due to the fact that the DUTs are on the low side, all three probes can be single-ended passive probes.

The high-speed switching transients of the SiC device requires that the probes should have enough bandwidth in order to capture the fast rise and fall edges of the switching waveforms in fidelity [11]. As it will be shown in Chapter 3, the rise / fall time of the SiC JFET V_{DS} can reach as short as 20 ns. I_D can be even faster, with a minimum rise time of only 5 ns. According to the signal theory, the effective bandwidth of a slope signal with a rise time t_r can be expressed as [12]

$$f_{BW} = \frac{0.35}{t_r} \tag{2-1}$$

Based on (2-1), a 20 ns rise time should be corresponding to 17.5 MHz bandwidth, while 5 ns corresponding to 70 MHz. If leaving five times margin, the bandwidths of probes should not be less than 90 MHz and 350 MHz respectively.

In this work, a Tektronix P6139 300 V, 500 MHz, 10x passive probe is used to measure V_{GS}, while a high-voltage P5100 2500 V, 250 MHz, 100x passive probe is used to measure V_{DS}. The shunt resistor claims a corner frequency of 2 GHz and can be connected to the scope directly through a coaxial cable. All these measurements meet the bandwidth requirement in our case.

Different types of probes, however, possess different propagation delays. Although these delays are usually only several nanoseconds, if not compensated properly, they will still cause serious timing misalignment for high-speed transients, eventually leading to wrong conclusions such as too big or too small switching loss. In this work, the coaxial cable usually possesses the minimum propagation delay, while the high-voltage probe has the longest. The delays, however, can be compensated in the following way.

(1) Choose one probe as the baseline. No delay compensation for this probe.

(2) Connect the baseline probe and a second probe to the Probe Compensation output of the scope (Tektronix TDS7054 in this work) to measure the same square waveform.

(3) Zoom in the square wave to observe its rising edge or falling edge.

(4) Adjust the "Deskew" option of the second probe in the scope to align its rising or falling edge with that of the baseline probe.

(5) Repeat (1) to (4) for the third probe.

In this work, P6139 is used as the baseline, compared to which the coaxial cable has minus 2.5 ns delay and P5100 has 7.3 ns delay.

2.3.3 Characterization Setup

The switching characterization setup is illustrated in Figure 2-5. As seen, the double-pulse signals with adjustable pulse widths are sent from an Agilent 33220A arbitrary waveform generator, which is controlled by a PC through a USB or RS-232 cable. The switching waveforms are then measured by a Tektronix TDS7054 digital oscilloscope, and the data are transferred back to the controller through a GPIB or LAN cable. The PC controller is responsible for editing the double-pulse signals, collecting switching waveforms, and post-processing the raw data, such as calculating the switching times and

energies. With this configuration, the switching characteristics can be obtained as soon as the waveforms are collected.

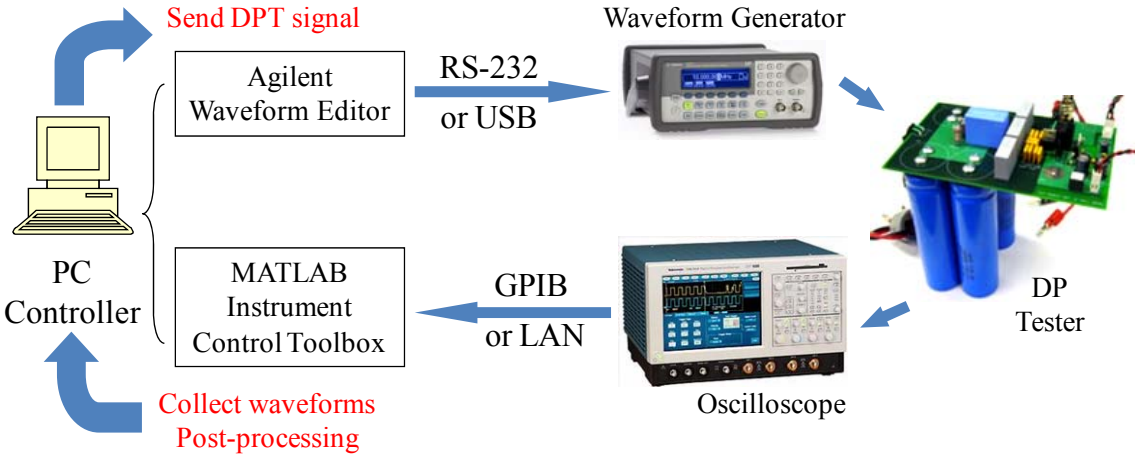

Figure 2-5. Switching characterization setup

2.3.4 Definitions of Switching Characteristics

The following terms are used in this thesis to evaluate the SiC device's switching characteristics. These terms are also illustrated in Figure 2-6.

The turn-on time t_{on} is defined as the time from I_D reaching 10% of the steady-state current to V_{DS} falling to 10% of the DC bus voltage.

The turn-off time t_{off} is defined as from V_{DS} rising to 10% of the bus voltage to I_D falling to 10% of the load current.

The turn-on switching energy E_{on} and turn-off energy E_{off} are integrals of the product of V_{DS} and I_D over t_{on} and t_{off} respectively.

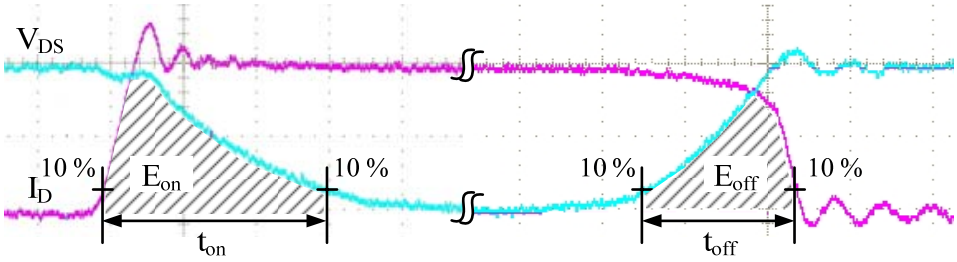

Figure 2-6. Definitions of switching times and energies

2.4 MOSFET Switching Behavior under Clamped Inductive Load

Under the condition of clamped inductive load, the load inductance is usually sufficient enough to maintain a nearly constant load current throughout the switching cycle. This means, during the MOSFET switching transients, the load inductor current keeps unchanged, while the switching current commutates from MOSFET to the freewheeling diode during MOSFET turn-off, or the opposite during MOSFET turn-on. The double-pulse tester is just a good example of such a load condition. Switching under this load is also the most common commutation mode for the power devices in a pulse-width modulation (PWM), hard-switching type converter. For this reason, there have been a lot of publications explaining the general operation of MOSFET and IGBT under the clamped inductive load [13-18]. This section will first briefly summarize from these works the ideal MOSFET switching behavior, and then discuss some non-idealities and their effects on the MOSFET switching waveforms.

2.4.1 Ideal MOSFET Switching Behavior

The simple circuit of the double-pulse tester is used again in this section to explain the MOSFET switching behavior. For easier understanding, the circuit schematic is redrawn in Figure 2-7.

The following assumptions need to be introduced to simply the analysis:

(1) The load inductor current does not change during the switching process;

(2) The freewheeling diode is ideal, without junction capacitance and forward voltage drop;

(3) The gate driver is an ideal step voltage source. The on-state level is V_{GS_ON} and the off-state level is zero;

(4) There is no parasitic inductance from either device packages or the circuit.

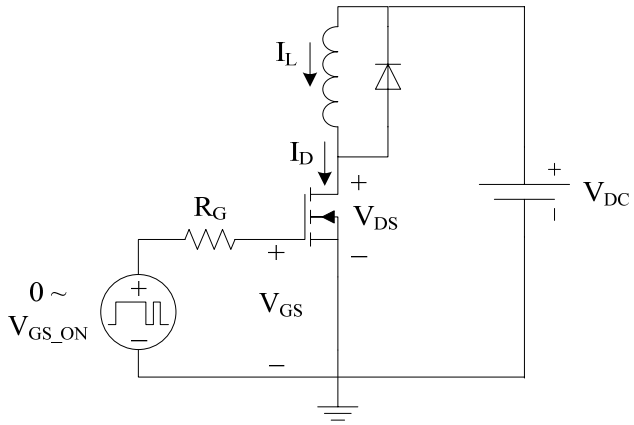

Figure 2-7. Clamped inductive load switching circuit

Turn-on process

The switching waveforms of the MOSFET turn-on process can be divided into four phases, as sketched in Figure 2-8:

Phase 1 – Turn-on delay ($t_{d,on}$)

Right after the gate drive voltage steps from zero to V_{GS_ON}, the input capacitance of the MOSFET starts to be charged and the gate-source voltage V_{GS} starts to rise. However, the MOSFET won't switch current until V_{GS} hits the gate threshold voltage V_{TH}. This period thus represents the turn-on delay. During this phase:

$$V_{DS} = V_{DC}$$

$$I_D = 0$$

$$V_{GS} = V_{GS\_ON}\left[1 - \exp\left(-\frac{t}{R_G C_{ISS}}\right)\right] \tag{2-2}$$

$$t_{d,on} = R_G C_{ISS} \ln\left(\frac{V_{GS\_ON}}{V_{GS\_ON} - V_{TH}}\right) \tag{2-3}$$

From (2-2) it can be inferred that the time constant in this gate charging circuit is determined by the gate resistance R_G and the MOSFET input capacitance C_{ISS}.

Phase 2 – Current rise period (t_{ir})

At the end of Phase 1, V_{GS} has reached the threshold voltage, and the MOSFET can start to conduct current. Therefore in Phase 2 part of the load current is transferred from the freewheeling diode to the MOSFET channel. As V_{GS} increases, the channel resistance reduces and more current flows through the MOSFET. During this period, however, the drain-source terminals keep blocking V_{DC} as long as the diode is still conducting. This phase ends when the load current is completely transferred from the diode to the MOSFET.

During this period:

$$V_{DS} = V_{DC}$$

$$I_D = g_{fs}(V_{GS}, V_{DS})V_{GS} \tag{2-4}$$

$$V_{GS} = V_{GS\_ON}\left[1 - \exp\left(-\frac{t}{R_G C_{ISS}}\right)\right] \tag{2-5}$$

$$t_{ir} = R_G C_{ISS} \ln\left(\frac{V_{GS\_ON} - V_{TH}}{V_{GS\_ON} - V_{plateau}}\right) \tag{2-6}$$

In (2-4) g_{fs} is the transconductance of the MOSFET which is a function of both V_{GS} and V_{DS}. Since in this phase V_{DS} is still high, the MOSFET is effectively in the saturation region and the channel current is simply determined by the applied V_{GS}. Also notice that in this phase the time constant for the gate circuit is still $R_G C_{ISS}$.

Phase 3 – Voltage fall period (t_{vf})

After the entire load current is transferred to the MOSFET, the freewheeling diode stops conducting and starts to block voltage. The drain-source voltage of MOSFET hence starts decreasing. However, in this period V_{GS} keeps almost unchanged (= $V_{plateau}$) because the MOSFET is still operating in the saturation region and I_D keeps equal to I_L. Consequently the gate current deviates from C_{GS} to mainly discharge the Miller capacitance C_{GD}. This phase ends when V_{DS} drops to the on-state voltage, which is equal to the product of the load current and the on-state resistance.

During this period:

$$\frac{dV_{DS}}{dt} = -\frac{V_{GS\_ON} - V_{plateau}}{R_G C_{GD}} \tag{2-7}$$

$$I_D = I_L$$

$$V_{GS} = V_{plateau} = g_{fs}^{-1} I_L \tag{2-8}$$

$$t_{vf} = \frac{Q_{GD} R_G}{V_{GS\_ON} - V_{plateau}} \tag{2-9}$$

Here V_{DS} is hard to be expressed explicitly because C_{GD} is a strongly nonlinear function of V_{DS}. In (2-9) Q_{GD} is the charge in the Miller capacitor provided by the gate current within this period, which can be obtained from the gate charge characteristic of the MOSFET.

Also note that C_{DS} is not considered here in the equations for simplicity. However the stored charge in this capacitor will be discharged as V_{DS} drops. This current will flow into the MOSFET channel in addition to the load current and Miller capacitance current.

Phase 4 – V_{GS} rise period

The MOSFET turn-on process has effectively finished at the end of Phase 3. However to provide low enough channel resistance V_{GS_ON} is usually higher than $V_{plateau}$, and Phase 4 is the period when V_{GS} is continuously charged to V_{GS_ON}. During this period:

$$V_{DS} = R_{DS(ON)} I_L$$

$$I_D = I_L$$

The gate circuit time constant for this phase is still given by $R_G C_{ISS}$. However the capacitance of C_{ISS} has increased since V_{DS} is now almost zero.

Turn-off process

Similar to turn-on, the turn-off process can still be divided into four phases, as sketched in Figure 2-9.

Phase 1 – Turn-off delay ($t_{d,off}$)

V_{GS} starts to decrease right after the gate drive voltage steps to zero. V_{DS} will increase a little bit due to the increasing channel resistance. This phase ends when V_{GS} drops to the Miller plateau voltage. The expressions of the waveforms are given by

$$V_{DS} = R_{DS(ON)} I_L$$

$$I_D = I_L$$

$$V_{GS} = V_{GS\_ON} \exp\left(-\frac{t}{R_G C_{ISS}}\right) \tag{2-10}$$

$$t_{d,off} = R_G C_{ISS} \ln\left(\frac{V_{GS\_ON}}{V_{plateau}}\right) \tag{2-11}$$

Phase 2 – Voltage rise period (t_{vr})

The MOSFET enters the saturation region from linear region when V_{GS} reduces to $V_{plateau}$. During the build-up phase of V_{DS}, V_{GS} must remain at $V_{plateau}$ for the MOSFET to afford the load current I_L. The waveform expressions are:

$$\frac{dV_{DS}}{dt} = \frac{V_{plateau}}{R_G C_{GD}} \tag{2-12}$$

$$I_D = I_L$$

$$V_{GS} = V_{plateau} = g_{fs}^{-1} I_L \tag{2-13}$$

$$t_{vr} = \frac{Q_{GD} R_G}{V_{plateau}} \tag{2-14}$$

This phase ends when V_{DS} reaches the DC bus voltage and the freewheeling diode starts to distract the load current.

Phase 3 – Current fall period (t_{if})

During this period the load current is transferred from the MOSFET channel to the freewheeling diode. Since the diode is conducting, the MOSFET V_{DS} is clamped to be the bus voltage V_{DC}. The input capacitance of MOSFET continues to be discharged until V_{GS} hits the threshold again. During this period:

$$V_{DS} = V_{DC}$$

$$I_D = g_{fs}(V_{GS}, V_{DS}) V_{GS} \tag{2-15}$$

$$V_{GS} = V_{plateau} \exp\left(-\frac{t}{R_G C_{ISS}}\right) \tag{2-16}$$

$$t_{if} = R_G C_{ISS} \ln\left(\frac{V_{plateau}}{V_{TH}}\right) \tag{2-17}$$

Phase 4 – V_{GS} fall period

The turn-off process of the MOSFET finishes at the end of Phase 3, but the rest of the charge stored in the MOSFET input capacitance will keep discharging until V_{GS} reaches zero. For this phase:

$$V_{DS} = V_{DC}$$

$$I_D = 0$$

To summarize the above expressions, Table 2-1 exhibits how the length of each phase is positively related to what device parameters and operating conditions.

Table 2-1. Influences of device parameters and operating conditions on MOSFET switching behavior

Turn-on / Turn-off	Influence factors	Phase 1	Phase 2	Phase 3	Phase 4
Turn-on	Device parameters	$R_G C_{ISS}$	$R_G C_{ISS}$	$R_G Q_{GD}$	$R_G C_{ISS}$
	Operating conditions	$\frac{1}{1 - I_L/(g_{fs} V_{GS\_ON})}$		$\frac{1}{V_{GS\_ON} - I_L/g_{fs}}$	-
Turn-off	Device parameters	$R_G C_{ISS}$	$R_G Q_{GD}$	$R_G C_{ISS}$	$R_G C_{ISS}$
	Operating conditions	$\frac{V_{GS\_ON}}{I_L/g_{fs}}$	$\frac{1}{I_L/g_{fs}}$	$\frac{I_L/g_{fs}}{V_{TH}}$	-

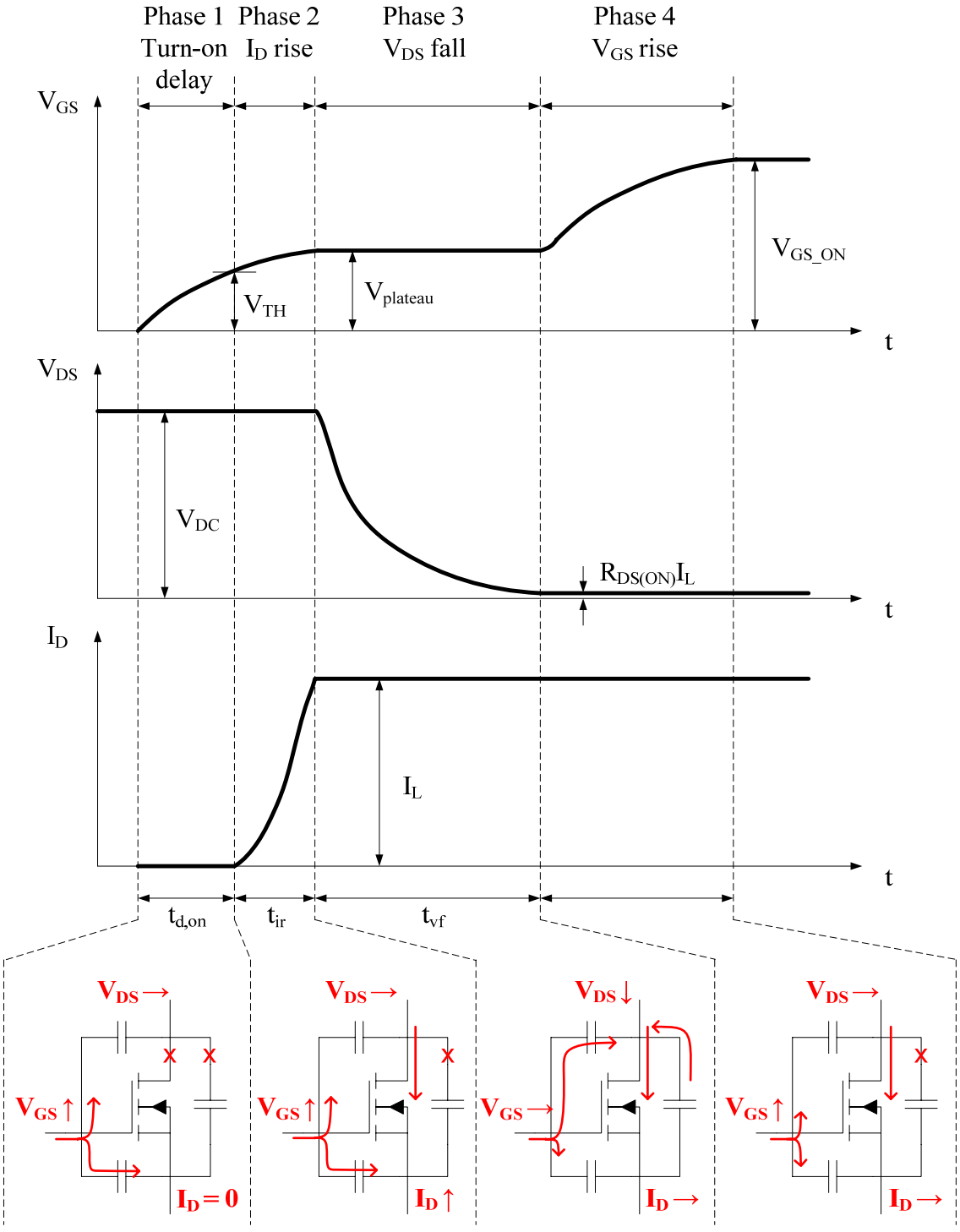

Figure 2-8. MOSFET turn-on process

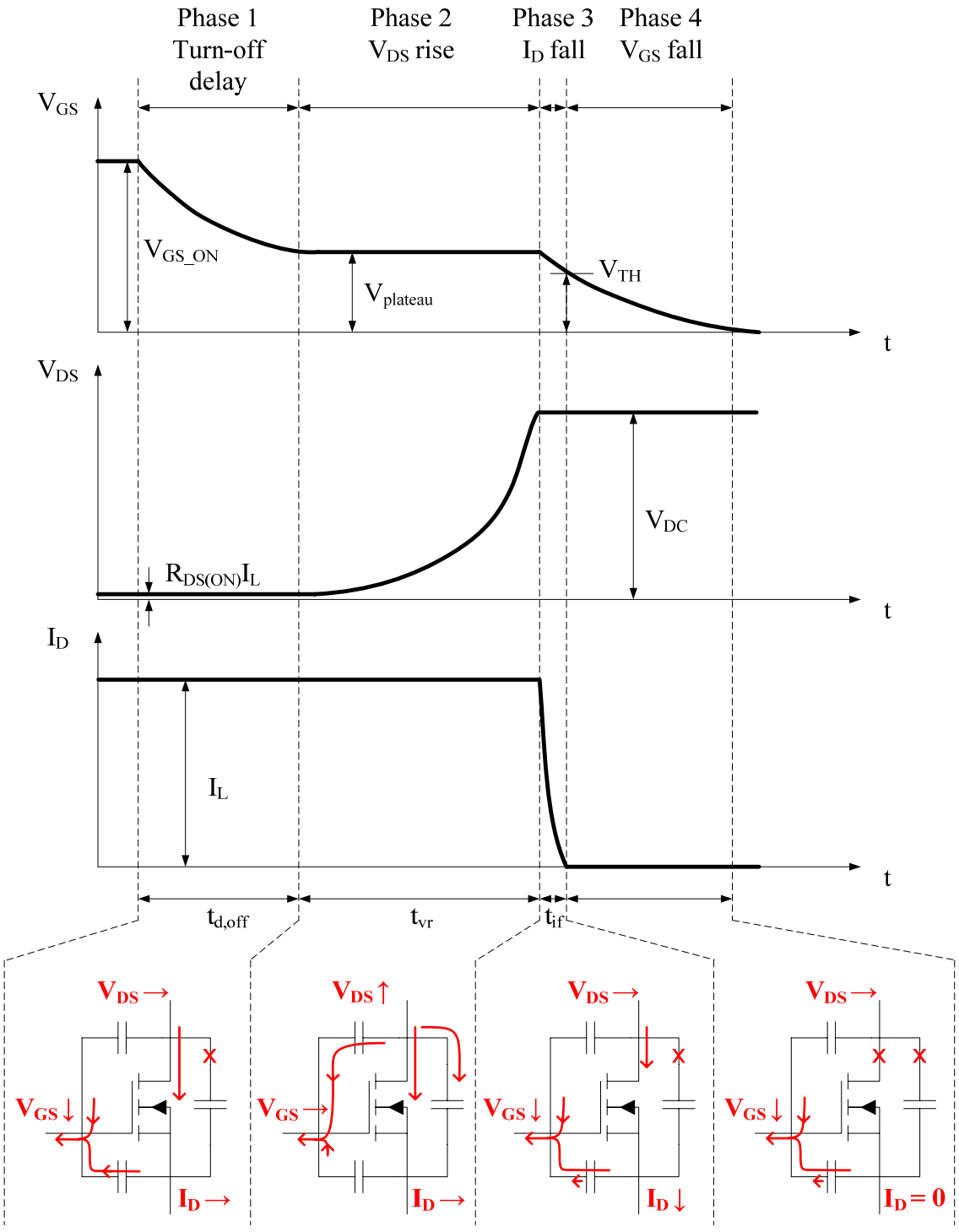

Figure 2-9. MOSFET turn-off process

The above table can lead to the following conclusions:

(1) From the device point of view, it is always good to have smaller junction capacitances to reduce the switching time;

(2) From the gate driver side, higher turn-on voltage and lower gate resistance can help speed up the switching transients;

(3) Under higher load current, all phases lengthen during the turn-on process, while during turn-off Phase 1 and Phase 2 shrink and Phase 3 expands. Consequently, the turn-on time of the MOSFET always increases with the load current, but the turn-off time may decrease when the load current becomes bigger. An experimental example of this can be found in Chapter 4.

2.4.2 Non-Idealities and Their Effects

The MOSFET switching waveforms appear somewhat different when including the non-idealities of the devices and the circuit. In this section the following non-idealities are considered: freewheeling diode junction capacitance C_J, switching loop inductance L_{DS}, and MOSFET drain-source capacitance C_{DS}. The double-pulse tester is then redrawn in Figure 2-10 illustrating the positions of these non-ideal components.

The existence of the diode junction capacitance basically reshapes the drain current measured outside the MOSFET. Because during the MOSFET turn-on process the freewheeling diode is blocking voltage, C_J is charged and the charging current will add to I_D together with the load current. This is why in the experiment the drain current spike is still observed even with the SBD which does not have reverse recovery effect. On the other hand, during turn-off C_J is discharged by drawing part of the load current, causing I_D to drop even before the diode starts forward conducting.

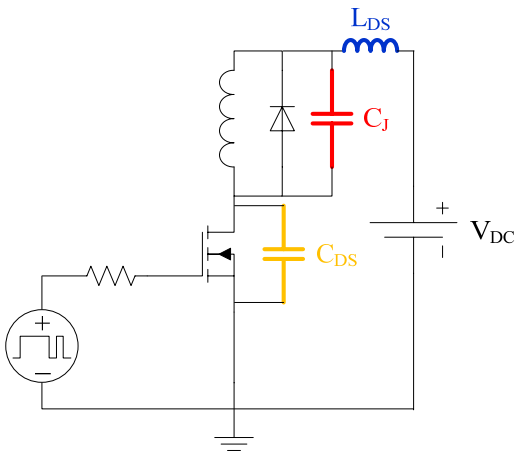

Figure 2-10. Schematic of double-pulse tester considering the non-idealities

The load inductor EPC is effectively in parallel with C_J, and thus has the same effect. For this reason, the load inductor should be designed to have a minimal EPC to reduce the MOSFET current spike.

The switching loop inductance L_{DS} mainly comes from the parasitic inductance along the drain current paths, namely from the DC source, through the freewheeling diode and the MOSFET, then back to the source. As the drain current swings between I_L and zero, the voltage drop across this inductance reshapes V_{DS}, forming a notch during turn-on and a peak during turn-off. Also, L_{DS} tends to resonate with the device junction capacitances during the switching transients, resulting in high-frequency ringing in the waveforms.

The effect of the drain-source capacitance C_{DS}, though cannot be observed outside the MOSFET, does change the current distribution within the device. During MOSFET turn-on, the energy stored in this capacitance discharges through the MOSFET channel, causing the channel current to be bigger than what is measured outside. During turn-off, this capacitance is charged as V_{DS} rises, drawing some current from the load, which makes the channel current smaller than the measured I_D. This explains why the turn-on V_{GS} has a higher plateau voltage level than turn-off. The direct consequence of C_{DS} is that

the calculated energy from $\int I_D V_{DS} dt$ does not represent the real switching loss. In fact this expression underestimates the turn-on loss and overestimates the turn-off loss. However, as it will be shown later in Chapter 6, the sum of these two energies will still represent the real switching loss of one switching cycle.

The corresponding MOSFET switching waveforms are sketched in Figure 2-11, which are more close to the experimental results.

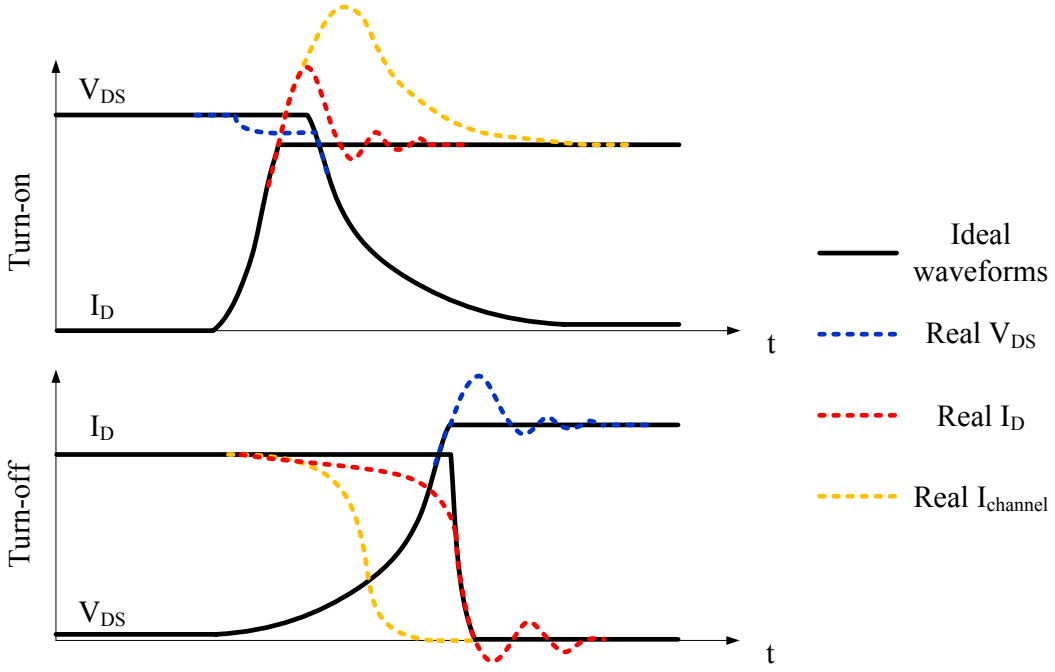

Figure 2-11. Effects of non-idealities on the MOSFET switching waveforms

2.4.3 Switching Trajectory

The switching trajectory is another way of studying the MOSFET switching behavior by superimposing the I_D vs. V_{DS} relationships during the switching transients upon the device's output characteristics. The switching trajectory is sometimes more direct in explaining the MOSFET switching behavior. For instance, from the ideal switching trajectories plotted in Figure 2-12, it is very easy to distinguish the four phases during the

switching transients, and it can be intuitively seen as well that V_{GS} keeps constant in Phase 3 during turn-on and in Phase 2 during turn-off. Figure 2-13 sketches the switching trajectories considering the non-idealities.

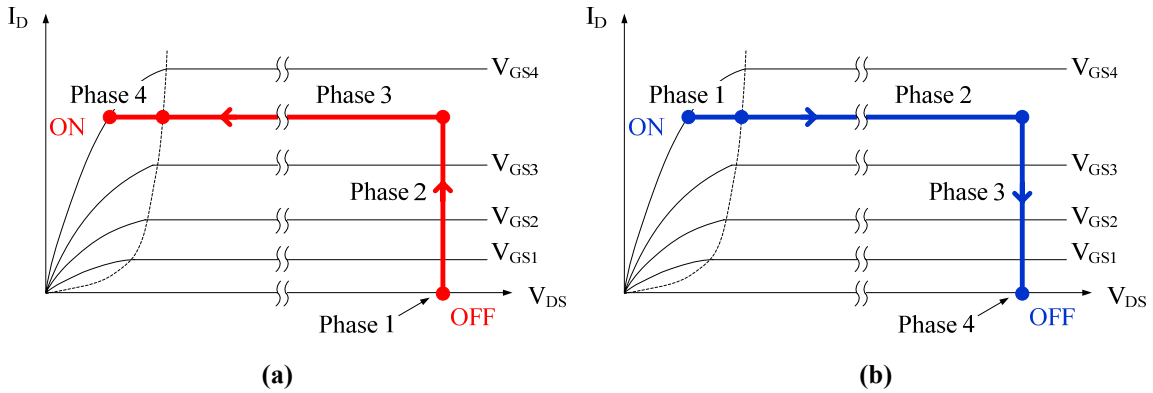

Figure 2-12. Ideal switching trajectories. (a) Turn-on, (b) turn-off

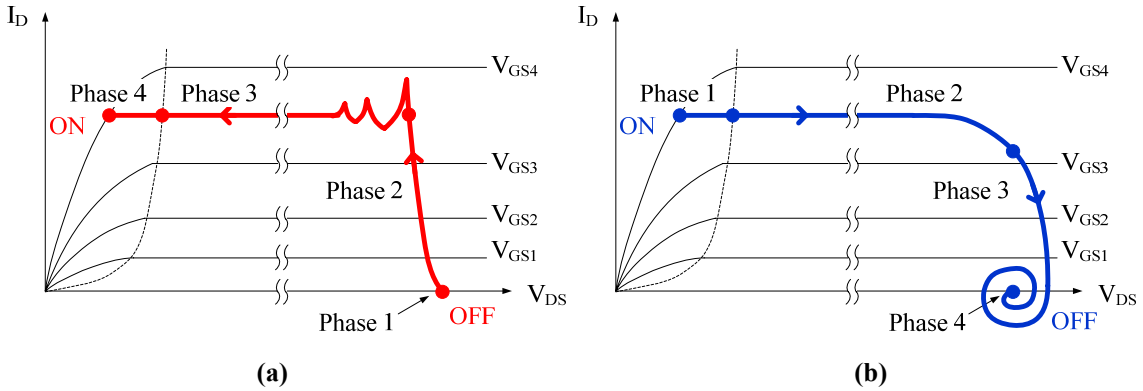

Figure 2-13. Non-ideal switching trajectories. (a) Turn-on, (b) turn-off

2.5 References

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Chapter 3 Characterization and Modeling of 1.2 kV, 5 A SiC JFETs

3.1 Introduction

Although being normally-on is generally not a desirable feature for a power switch, the development and application of silicon carbide (SiC) JFETs are still very hot topics today due to its reliability and more mature manufacturing techniques compared to other categories of SiC devices (e.g. SiC MOSFET). At the time of this work, the only available 1.2 kV level SiC active switches that have been demonstrated to operate reliably at temperatures beyond 150 °C are SiC JFETs, which are also expected to be the first commercialized SiC active switches, following the SiC Schottky diodes [1-5].

So far there have been many efforts on the characterization and modeling of SiC JFETs. To name a few, [1] and [6] measured the SiC JFET static and capacitance characteristics under different temperatures, and tried to fit the characterization data to a subcircuit model based on the SPICE Version 2 (SPICE 2) JFET model. [2] and [7], on the other hand, established more physics-based equations to describe the static and dynamic behaviors of the device. The characterization and modeling work in our case, however, requires the easy availability of device characteristics, fast and convenient

extraction process of model parameters, as well as the full inclusion of all the electrical characteristics particular to the SiC JFETs, so that the developed device model can be incorporated in system-level simulation for the future converter design. The first and second conditions require that the characterization can be achieved with the use of basic instruments such as the curve tracer and the impedance analyzer, and the model parameters can be extracted directly based on the characterization results. This usually eliminates the use of the physics-based device models because many parameters in such models are not accessible to device users, such as the doping density, electron mobility, etc. Plus, the development of a physics-based model requires professional knowledge in solid-state physics and semiconductor devices, and the model itself is generally too complicated to be suitable for system-level simulation. In this sense, a subcircuit model is more preferable in our case. The mostly used subcircuit model in the papers, however, is generally based on the SPICE 2 JFET model which is originally developed for a lateral structure JFET. Therefore, certain features are not included in this model for high-voltage, vertical structure SiC JFETs. This makes the direct use of the SPICE 2 model inadequate for SiC JFETs, and the model needs to be modified accordingly to include the particular features of vertical JFET, such as the body diode. Unfortunately none of the previous work fulfilled all these requirements, and thus a characterization and modeling procedure becomes necessary in this work.

This chapter will present the development of a SPICE 2-based SiC JFET model and its corresponding characterization process. The device under study is a 1.2 kV, 5 A SiC JFET prototype manufactured by SiCED [8], with a 2.4 mm × 2.4 mm die packaged in a TO-220 case. The adaption of the SPICE 2 model to fit the SiC JFET, issues in the device

characterizations, as well as the limitations of the model will all be discussed in this chapter.

3.2 SPICE 2-Based SiC JFET Model

The proposed SiC JFET model is illustrated in Figure 3-1 (a). The core of this model is a SPICE-2 JFET model which describes the basic JFET static (current-voltage, I-V) and dynamic (capacitance-voltage, C-V) characteristics, as seen in Figure 3-1 (b).This level-1 SPICE-2 model contains less than 20 parameters, which can be easily extracted from conventional characterization data, such as the output and transfer characteristics. The detailed descriptions of the SPICE 2 JFET model can be found in [9].

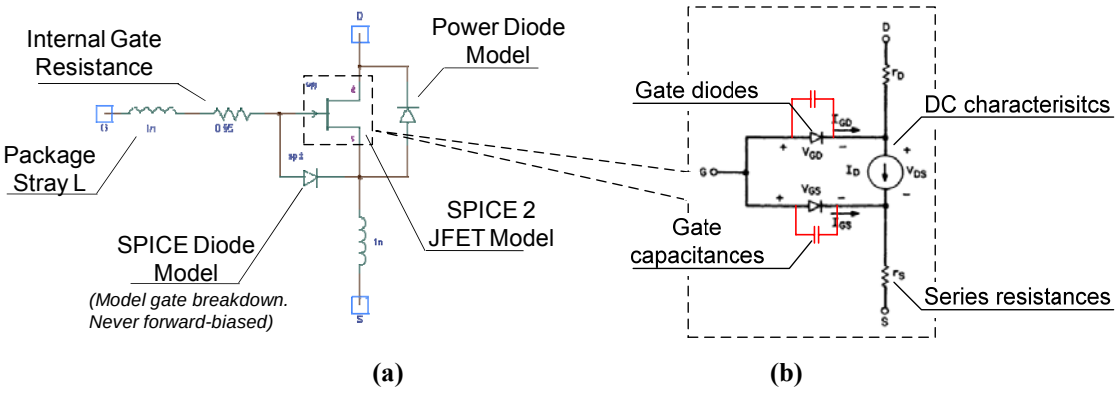

Figure 3-1. Model structures for SiC JFET. (a) Proposed model, (b) SPICE 2 JFET model

As previously said, the SPICE 2 JFET model is originally developed for lateral structure device, therefore it is inadequate to model the vertical structure SiC JFET. Figure 3-2 exhibits a typical cross-sectional structure of SiC JFET. As seen, instead of all three terminals being on the same side, the drain terminal of the device is on the bottom in vertical structure while the source and gate sit on the top. The P^+ layer buried under the source terminal and the N layers under that constitute a PN junction between the drain

and source terminals. This equivalently forms a body diode as well as a drain-source junction capacitance C_{DS} to the JFET, which is not modeled for lateral structure in the SPICE 2 model. This body diode is included in the proposed model by adding an anti-paralleled power diode model to the SPICE 2 model, and the drain-source capacitance is then interpreted as the diode junction capacitance, as seen in Figure 3-1 (a).

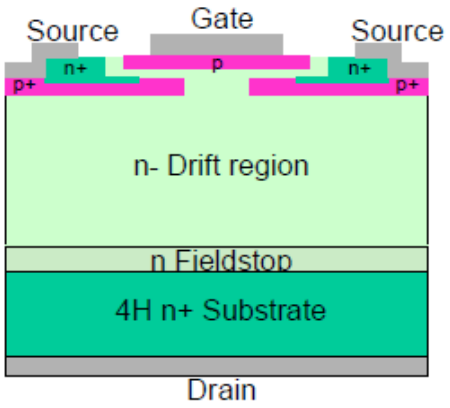

Figure 3-2. Typical cross-sectional structure of SiC JFET [1]

Besides the body diode, an extra SPICE diode model is also added across the gate-source terminals in order to model the gate breakdown characteristics of the device. This is necessary for the case when the gate of the SiC JFET is intentionally driven in breakdown mode [10]. Also seen in Figure 3-1 (a) is a resistor connected in series with the gate terminal representing the internal gate resistance of the device, while the package stray inductances are lumped into two series inductances. All these components together describe the SiC JFET static and switching behavior under normal operating conditions.

3.3 Characterizations of SiC JFET and Model Parameter Extractions

3.3.1 Static I-V Characteristics

Figure 3-3 shows the output and transfer characteristics of the SiC JFET, from which it can be told that device under test (DUT) has an on-state resistance $R_{DS(ON)}$ of around 0.3 Ω at V_{GS} = 0 V and I_{DS} = 5 A, and the device is pinched off at $V_{GS} \approx$ -22 V.

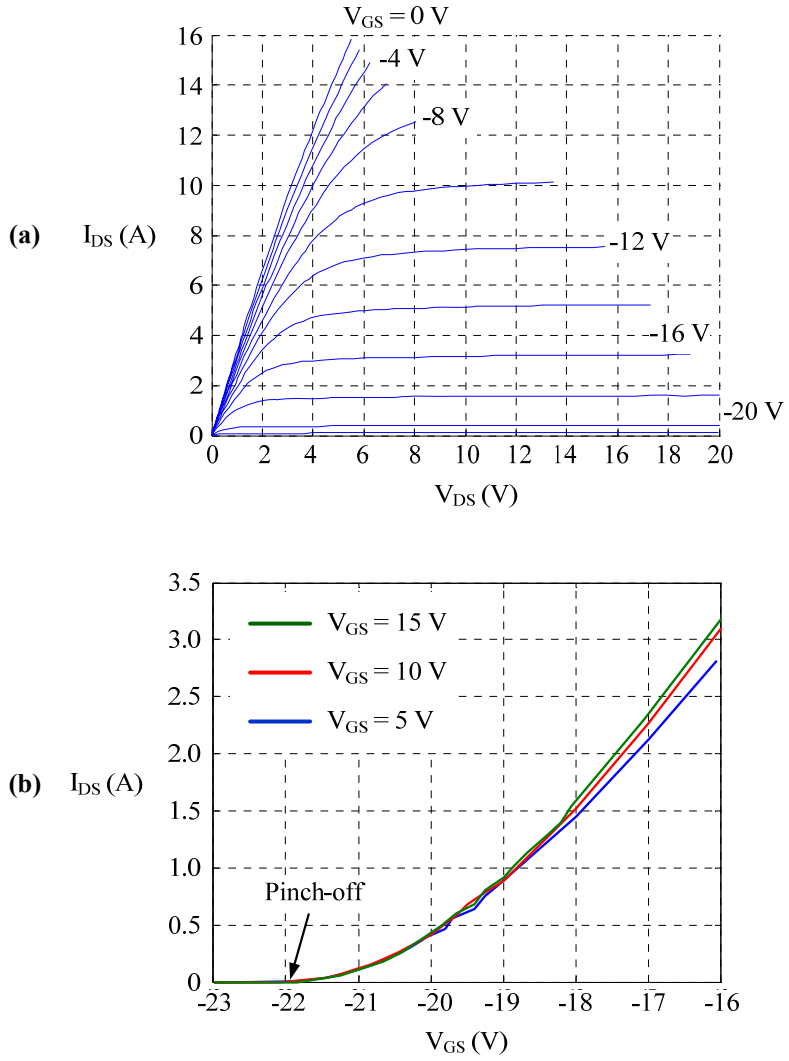

Figure 3-3. SiC JFET output (a) and transfer (b) characteristics

In SPICE 2, the JFET model uses the following piecewise equations to describe the output characteristics:

$$I_D = \begin{cases} 0, & V_{GS} - V_{T0} \le 0 \quad \text{(Pinch-off)} \\ \beta(V_{GS} - V_{T0})^2(1 + \lambda V_{DS}), & 0 < V_{GS} - V_{T0} \le V_{DS} \quad \text{(Saturation)} \\ \beta V_{DS}[2(V_{GS} - V_{T0}) - V_{DS}](1 + \lambda V_{DS}), & 0 < V_{DS} < V_{GS} - V_{T0} \quad \text{(Linear)} \end{cases} \tag{3-1}$$

where model parameter β is the transconductance, λ is the channel-length modulation parameter, and V_{T0} is the threshold voltage.

A curve-fitting method is carried out in Matlab to extract these parameters. Basically V_{T0} can be extracted from the interception point of V_{GS} for the square root value of I_{DS}-V_{GS} graph. The square root of β can be approximated by the slope of the square root value of the same graph [1][6][11]. The optimized V_{T0}, β and λ can be determined by running a least-mean-square (LMS) Matlab program to curve fit the measurement data.

Considering the nominal current rating of the DUT, the curve fitting is done within a current range of 0 to 3 A. The result is shown in Figure 3-4 as the set of red dashed curves, where as seen a good agreement is achieved between the measured and simulated curves.

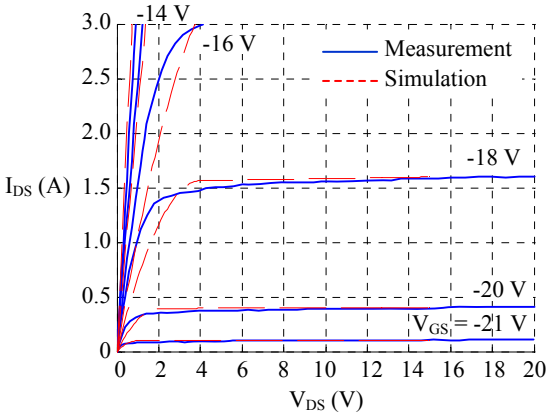

Figure 3-4. Curve-fitting results of SiC JFET output characteristics.

3.3.2 Gate Junction Diode Characteristics

The JFET gate-drain and gate-source junctions behave like two diodes when forward-biased, due to the PN junctions formed between the terminals as seen in Figure 3-2. The static characteristics of the two gate diodes are displayed in Figure 3-5.

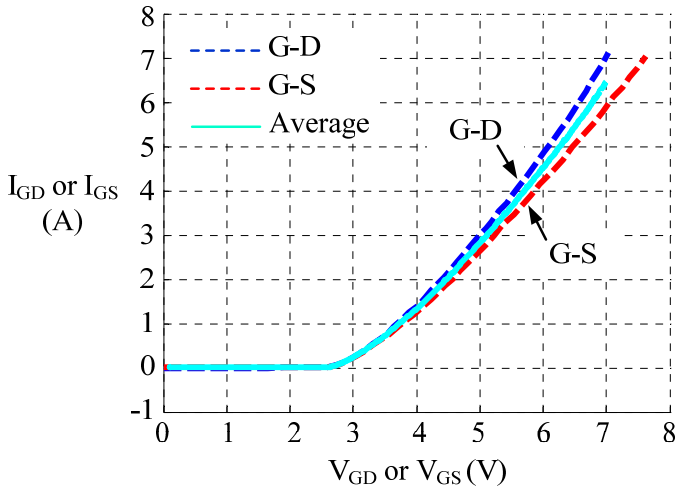

Figure 3-5. Gate junction diodes forward static characteristics

Note in the figure that due to the asymmetrical structure of the G-D junction and G-S junction, the static characteristics of the two diodes are slightly different. However, the SPICE 2 model uses exactly the same equations to describe these two diodes because in lateral structure JFET the positions of the drain and source terminals are basically symmetrical. In SPICE the equation for G-D junction is given as follows:

$$I_{GD} = \begin{cases} -I_S + V_{GD} GMIN, & V_{GD} \le -5\dfrac{kT}{q} \\ I_S\left(e^{qV_{GD}/kT} - 1\right) + V_{GD} GMIN, & V_{GD} > -5\dfrac{kT}{q} \end{cases} \tag{3-2}$$

where I_S is the saturation current, q is the electron charge, T is the temperature in Kelvin and k is the Boltzmann constant. *GMIN* is a parameter for simulation convergence. Replacing I_{GD}, V_{GD} with I_{GS} and V_{GS} in (3-2) gives the equation for G-S junction.

In order to extract the model parameters the G-D and G-S diode characteristics are averaged to get one curve for the curve-fitting, which is shown as the cyan curve in Figure 3-5. This is based on the facts that (1) the two characteristics are only slightly different, and (2) the two gate diodes are never forward biased in normal JFET operation, and the forward characteristics of these diodes will not affect the model behavior a lot in our case. The LMS curve fitting is still carried out in Matlab and the result is shown in Figure 3-6.

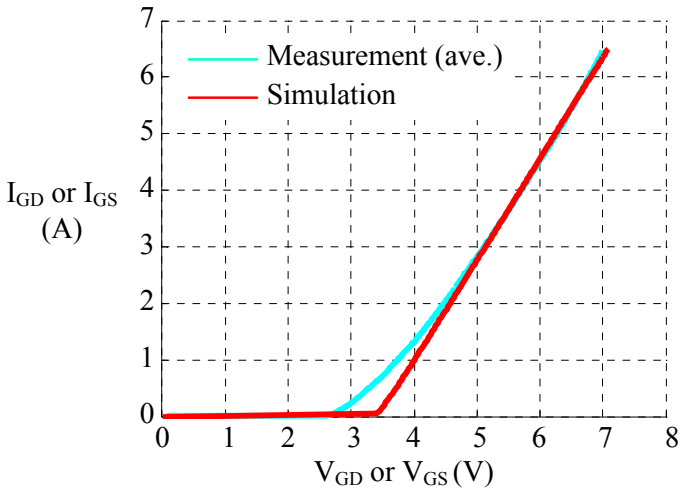

Figure 3-6. Curve-fitting result of gate diode forward characteristics

3.3.3 Junction Capacitance Characteristics

Two gate junction capacitances, namely gate-source capacitance C_{GS} and gate-drain capacitance C_{GD} are included in the SPICE 2 model. The C_{GS} capacitance is described by

$$C_{GS} = \frac{C_{GS}(0)}{\sqrt{1 - V_{GS} / \phi_0}} \tag{3-3}$$

where the model parameter $C_{GS}(0)$ is the G-S capacitance at zero bias voltage, and ϕ_0 is the gate junction potential parameter. Substituting C_{GS}, V_{GS} with C_{GD} and V_{GD} in (3-3) gives the equation for the C_{GD} capacitance.

The capacitance-voltage curves can be measured with an Agilent 4294A impedance analyzer [1-2][12]. From the parameter extraction point of view, it is necessary to obtain the C-V characteristics of these two capacitances from zero bias voltage. However, being a normally-on device, the SiC JFET has a shorted channel when it is not pinched off, which means C_{GS} and C_{GD} are effectively paralleled without pinching off the channel. Consequently, the only measurable capacitance from device terminals is the input capacitance C_{ISS} (= C_{GS} + C_{GD}). Figure 3-7 shows three configurations trying to measure C_{GS} and C_{GD} directly, where Hp, Hc and Lp, Lc represent the High Potential / High Current and Low Potential / Low Current terminals of the impedance analyzer. The measurement results shown in Figure 3-8, however, indicate clearly that the C-V curves measured from the first two setups in Figure 3-7 overlap from zero bias to around -22 V, the pinch-off voltage. And the measurement in Figure 3-7 (c) proves that this overlap range is the input capacitance C_{ISS}.

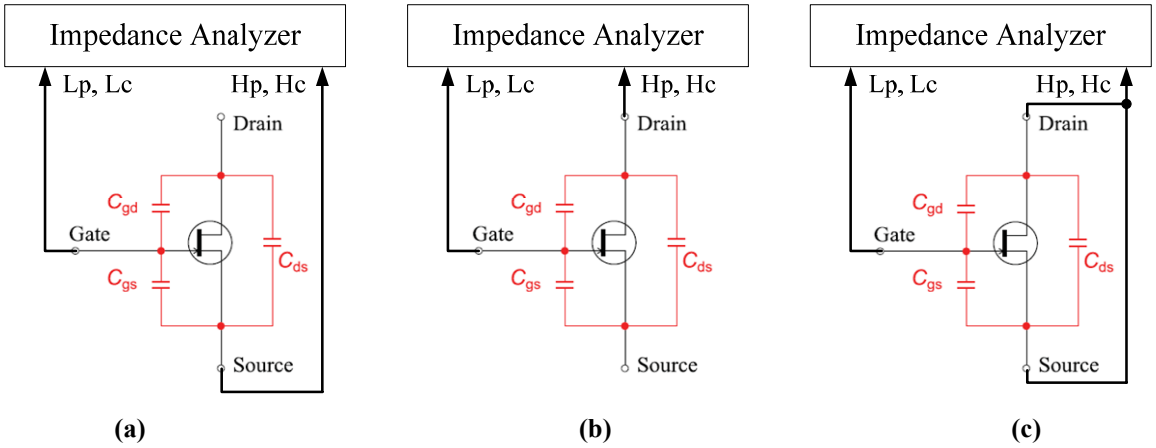

Figure 3-7. Direct measurement configurations of junction capacitances.
(a) Measuring G-S terminals, (b) measuring G-D terminals, (c) measuring G-D with D-S shorted

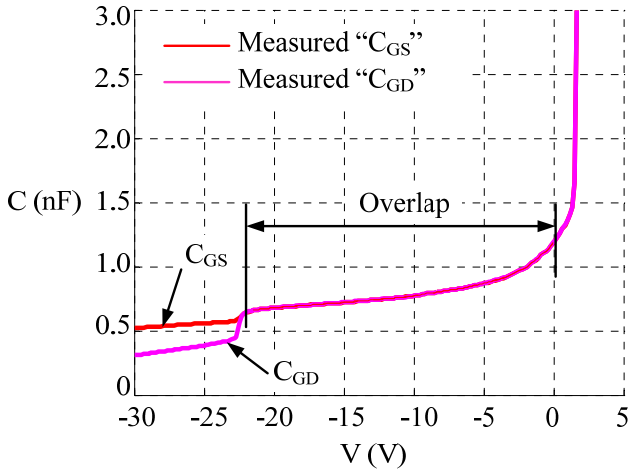

Figure 3-8. C-V characteristics measured from configurations in Figure 3-7.
Red: Figure 3-7 (a); magenta: Figure 3-7 (b)

In order to measure C_{GS} and C_{GD} separately, it is first necessary to pinch off the JFET channel, and a three-terminal measurement should be implemented with the Agilent 16047E test fixture [13]. Figure 3-9 shows the 4294A setup for C_{GD} measurement. The black components represent the instrument internal functions to generate the magnitude-phase vs. frequency characteristic of the impedance to be measured. The red part is the equivalent circuit of the JFET. The blue components are the auxiliary circuits: a voltage

source V_G of 25 V is connected across G-S terminals to pinch off the JFET, and C_D is an isolating capacitor to block the ampere meter within the instrument. This configuration, at first sight, seems to be able to measure the correct C_{GD}. However, the external V_G already imposes a negative bias of -25 V across the gate-drain capacitor, and this negative bias cannot be offset by using the DC bias voltage across drain-source terminals because this voltage will be clamped by the JFET body diode. As a result, the C_{GD}-V_{GD} characteristic can only be measured for voltages lower than pinch-off. C_{GS}-V_{GS} measurement has the same problem [14]. Unfortunately this fact is not discussed in [12].

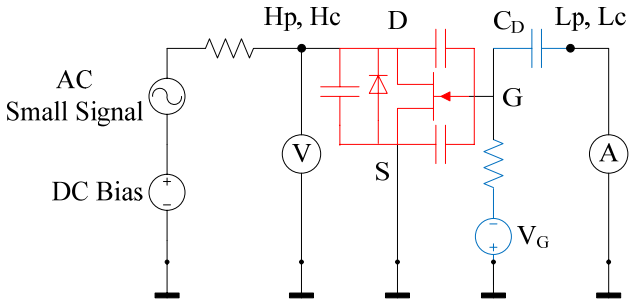

Figure 3-9. Impedance analyzer measurement of C_{GD}

Although C_{GS} and C_{GD} cannot be measured independently from zero to pinch-off voltage, the sum of these two can still be measured as shown in Figure 3-8. One way to determine $C_{GS}(0)$ and $C_{GD}(0)$ is to estimate them from $C_{ISS}(0)$ by matching the simulation waveforms with the experimental results. Another more reasonable way than "guessing" is to look at the gate charge characteristics of the DUT. However this method is more complicated and requires specially-designed test circuits, thus is not adopted in this work for simplicity.

The measurement of the drain-source capacitance C_{DS} is similar to that of C_{GS} and C_{GD}, but in this case C_{DS} does not suffer from the pinch-off problem. Figure 3-10 shows

the measurement setup, and the result is displayed in Figure 3-11. This capacitance does not exist in lateral structure JFET and it will be modeled as the junction capacitance of the body diode, which will be discussed in the next section.

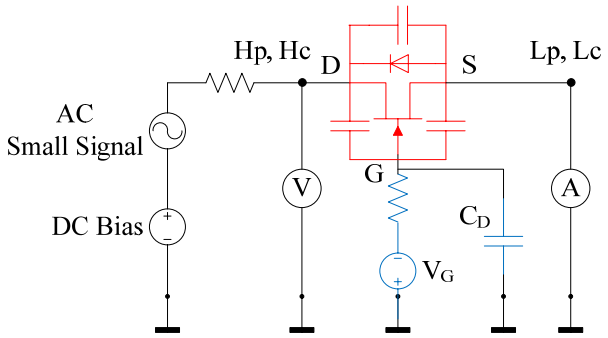

Figure 3-10. Impedance analyzer measurement of C_{DS}

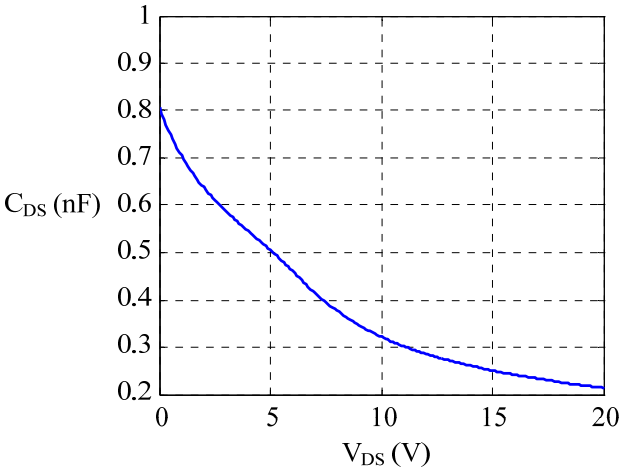

Figure 3-11. C_{DS} measurement result

3.3.4 Body Diode Characteristics

The measurement of the body diode I-V curve is described in Chapter 2. Unlike conventional PiN or Schottky diodes, the I-V characteristic of the SiC JFET body diode is gate-voltage dependent. Figure 3-12 shows an example of this characteristic. For this SiC JFET (not the same DUT as used above), the channel is completely pinched off

below -19 V, whereas the I-V curve is seen to shift to the right with decreasing gate-source voltage, i.e. the turn-on voltage becomes bigger. The slopes of these curves remain constant, which means there is no change in the diode series resistance.

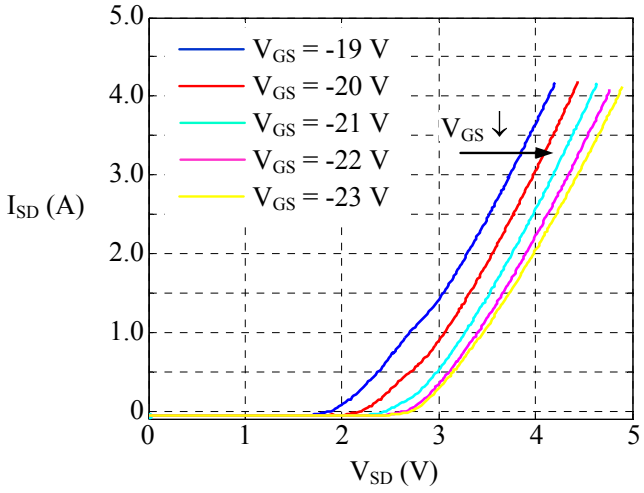

Figure 3-12. Gate-voltage-dependent body diode I-V curves

This gate-voltage dependence cannot be modeled by any existing model. In this work, the body diode is still treated as being independent of the gate voltage, and a specific I-V curve is picked for modeling according to the final gate voltage used in the circuit. The model is built with the *Power Diode Tool* in Synopsys Saber, where the device characteristics (i.e. I_{SD}-V_{SD} and C_{DS}-V_{DS} curves) are tuned visually to fit the characterization data [15]. The curve-fitting results are shown in Figure 3-13, where a good agreement can be seen between the simulation and the measurement. The resultant power diode model is then connected in anti-parallel with the SPICE 2 JFET model as shown in Figure 3-1 (a).

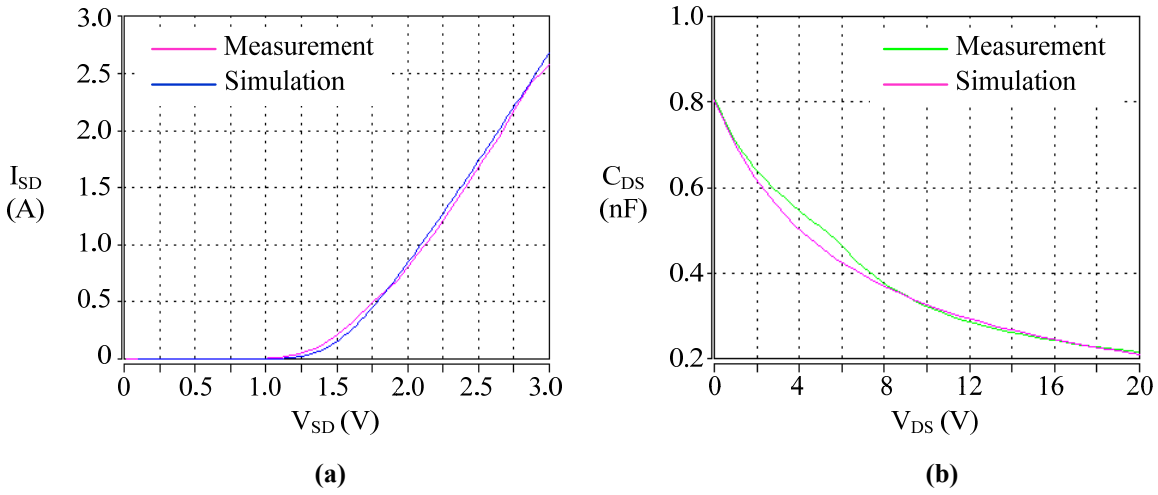

Figure 3-13. Body diode curve-fitting results. (a) Forward I-V, (b) junction capacitance

3.3.5 Other Parameters

In some applications the gate of the SiC JFET is intentionally driven in breakdown mode to adapt to the non-uniformity in the JFET gate characteristics [10]. To include that feature into the device model, an additional SPICE diode model is paralleled to the G-S of the SPICE 2 JFET model to simulate the gate breakdown effect since it is not modeled in SPICE 2. The only parameters modified in the diode model are BV and VJ. BV is the reverse breakdown voltage and is set as the actual gate breakdown voltage of the SiC JFET. VJ is the junction potential or forward turn-on voltage. This parameter should be set bigger than that of the JFET intrinsic gate-source diode such that it will never be conducting in the simulation.

The internal gate resistance R_{GI} is also important and necessary for the SiC JFET model as it determines the ultimate switching speed of the device. In this work R_{GI} is finely adjusted to match the experimental waveforms. The package parasitic inductances L_G and L_S, on the other hand, are simply taken as 1 nH each, which are typical values for the TO-220 package.

The finalized parameters for the proposed SiC JFET model are listed in Table 3-1.

Table 3-1. SiC JFET model parameters

Parameter	Value	Unit
SPICE 2 JFET model		
VT0	-22.02	V
BETA	0.096	AV^{-2}
LAMBDA	0.002	V^{-1}
RD	0	Ω
RS	0	Ω
IS	1×10^{-58}	A
CGS0	1000	pF
CGD0	190	pF
PB	7.7	V
FC	0	-
Power diode model (body diode)		
RS	0.48	Ω

Parameter	Value	Unit
ISL	17.673	nA
NL	3.037	-
ISH	97.667	nA
NH	3.887	-
CJO	806.4	pF
VJ	5.8	V
M	0.9	-
FC	0.5	-
Other Parameters		
G-S SPICE diode BV	-28	V
Internal gate RGI	5	Ω
Stray LG, LS	1	nH

3.4 Model Verifications

The SiC JFET switching waveforms are obtained using the double-pulse tester described in Chapter 2. A 0 Ω external gate resistance is used to switch the JFET as fast as possible. The same DPT circuit is simulated in Synopsys Saber [16] to verify the device model previously built. The gate drive IC is replaced by an ideal voltage source in the simulation, and the freewheeling diode is replaced by the model of a similar CREE 1.2 kV, 10 A SiC Schottky diode, because the Infineon diode model is not available at the time of the work. A comparison of experimental switching waveforms and the simulated results is displayed in Figure 3-14.

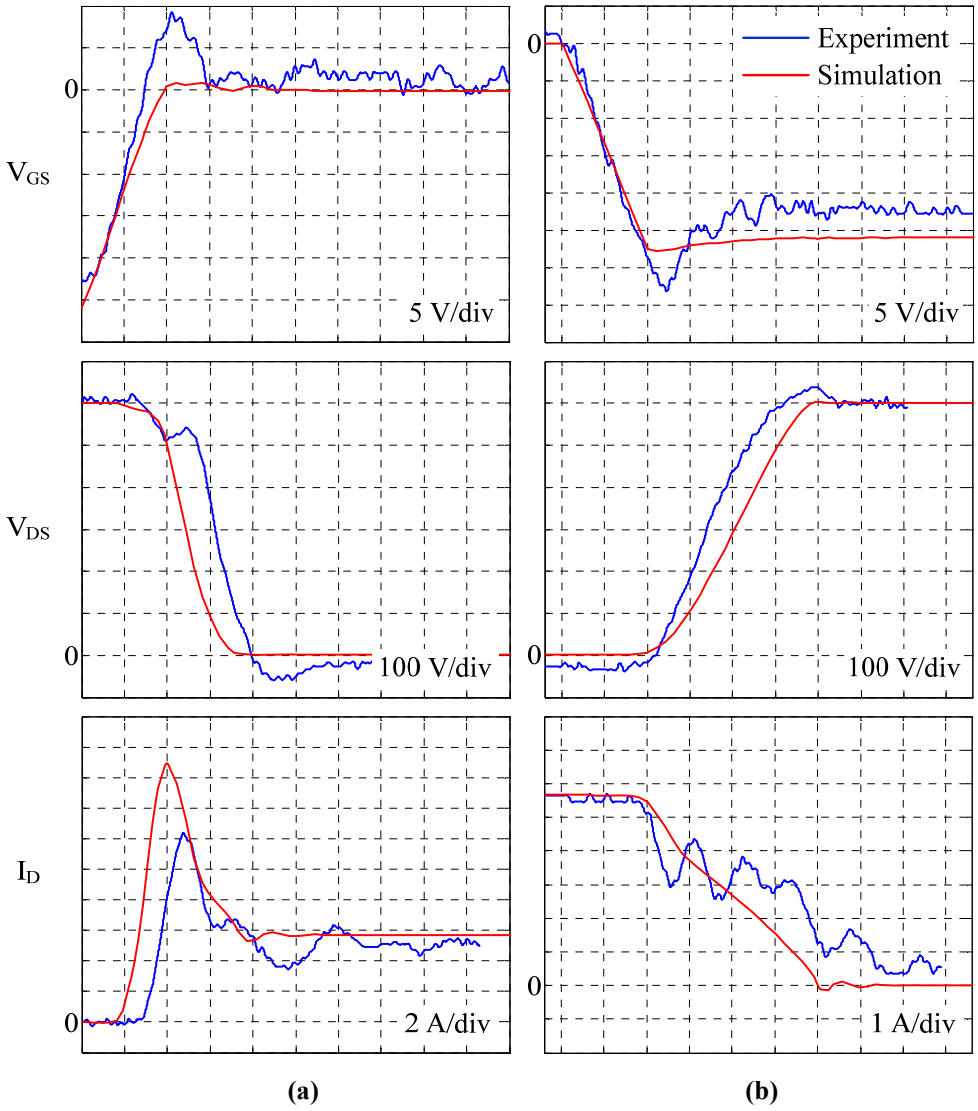

Figure 3-14. Model verification: experiment vs. simulation. Time: 5 ns/div. (a) Turn-on, (b) turn-off

The waveforms are obtained under 600 V and 5.5 A load conditions. To do the comparison the experimental and simulated V_{GS} waveforms are aligned in time. As seen, for the turn-on transients the JFET drain-source voltage V_{DS} and drain current I_D have around 4 ns advance in time compared to the experiments, which means the model predicts less turn-on delay than the real condition. Nonetheless this 4 ns is small enough and tolerable in this work. The slew rates of V_{DS} and I_D are predicted quite well by the model during both turn-on and turn-off processes, indicating that the model is good

enough overall in predicting the correct waveforms and switching loss of the SiC JFET. Also note that the additional SPICE diode model is working well because during turn-off V_{GS} ends at around -28 V, the gate breakdown voltage, instead of -30 V, the gate drive turn-off voltage. The only discrepancy is the turn-on current spike which in the simulation is about 4 A higher than the experiment. This current spike is mainly related to the characteristics of the freewheeling diode, and in this work a different diode model is used in the simulation. If the Infineon diode model is available, the simulation would match the experiment even better.

Another fact worth noting is the fast switching speed of this SiC JFET. As seen from Figure 3-14, the DUT switches 600 V and 5.5 A within 20 to 30 ns, achieving a maximum dv/dt rate of around 60 kV/μs and a maximum di/dt rate of 3 kA/μs, much faster than the conventional silicon bipolar devices (e.g. IGBT) of similar nominal voltage and current ratings. It is thus foreseeable that with the use of SiC devices, the high-frequency, high-temperature and high-power-density applications become achievable more easily.

3.5 Conclusions and Discussions

This chapter has proposed a SPICE 2-based SiC JFET model which is suitable for system-level simulation, and has presented the modeling process of a 1.2 kV, 5 A SiC JFET prototype from SiCED. Device characterizations have been conducted on this JFET to extract the model parameters. Issues during the characterization process have been explained and solutions have been provided. By comparing the simulation with the experiment, the effectiveness of the device model has also been verified.

The SPICE 2 JFET model is chosen in the first place as the base of the proposed SiC JFET model because (1) it is a compact model without too many parameters, which is preferable considering that the model will finally be used in system-level simulation. (2) The model parameters do not contain physical ones that are inaccessible to the device users, thus are easy to be extracted from conventional characterization process. Nevertheless, the use of the SPICE 2 model also poses some limitations on the final SiC JFET model.

First of all, since the SPICE 2 model is originally developed for lateral structure JFETs, Equation (3-1) is not able to describe the full-scale static I-V characteristics of the SiC JFET very well. Figure 3-15 (a) is the curve fitting result of (3-1) in a 0 to 3 A current range, which looks quite good, whereas Figure 3-15 (b) shows the same curve fitting but on a 0 to 20 A scale. It can be seen clearly that the SPICE model fails to match the measurement as the current increases, although in our case this does not bother because the SiC JFET to be modeled will never operate in that high current range.

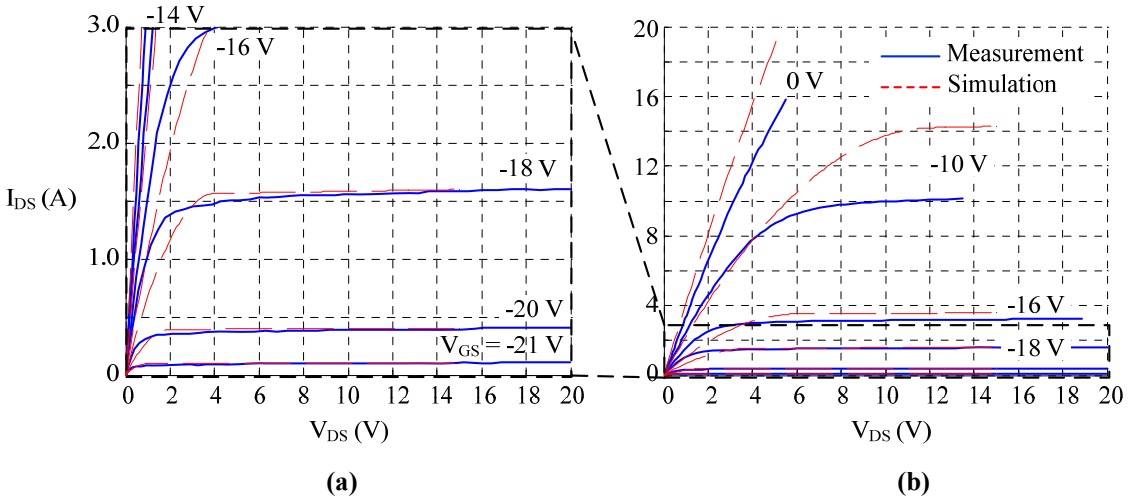

Figure 3-15. SPICE 2 model fails to predict static characteristics in large scale.
(a) 0-3 A curve fitting, (b) same curve fitting on 0-20 A scale

The second problem is with the gate diode description. Under the assumption of symmetrical lateral structure the SPICE model uses the same equation for both G-D and G-S diodes, which is not true for the vertical structure SiC JFET. Besides, there is no emission coefficient n existent in (3-2) which would usually appear in the exponential term $exp(qV/nkT)$. This leads to the unreasonable small saturation current IS (1×10^{-58} A) from curve fitting.

Thirdly, though the SPICE model requires junction capacitance parameters CGS0 and CGD0, it has been explained that it is not easy to directly measure these two capacitances from zero bias. Although this work adjusts the two parameters to match the experiments, using the gate charge characteristic is still a better way to determine their values more precisely.

As a matter of fact, SiCED has also developed device models for their newer batches of SiC JFETs available at http://siced.com/hp1016/Switches.htm (accessed on Nov. 24, 2009), which can be referred for future model development or improvement.

Some other work that has not been conducted but is worth doing includes the temperature-dependent device characterization and modeling. This is important since the SiC JFET would not be working in room temperature in the converter eventually. The same characterization process introduced in this chapter can still be applied, except that the junction temperature of the device needs to be controlled during measurement. Besides that, future efforts are also worthwhile in studying and understanding the nature of the SiC JFET body diode.

3.6 References

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Chapter 4 Characterization and Modeling of 1.2 kV, 20 A SiC MOSFETs

4.1 Introduction

Silicon carbide (SiC) MOSFET has become another competitor among new wide bandgap devices which is promising to substitute silicon (Si) devices in high-voltage, high-frequency applications, due to its higher breakdown voltage, lower on-state resistance, and better high-temperature operation capability [1-3]. Compared to SiC JFET, it also possesses the advantage of being a normally-off device, providing more benefits to the converters in terms of safe operation and failure protection. Currently, laboratory prototypes of this new device are still under improvement and have not been commercialized yet, which means manufacturer datasheets are still unavailable. Therefore, it is necessary to fully characterize these SiC MOSFETs in order to evaluate their potential performance in converter systems and to compare them with their Si counterparts. The work described in this chapter investigates a TO-247 packaged, 1.2 kV, 20 A SiC MOSFET manufactured by CREE [4] (See Figure 4-1). The most important static characteristics, namely I-V curves, body diode, junction capacitances, etc, have all been measured and their respective measurement methods have been described as well.

The static characterizations have also been carried out under different temperatures from 25 °C to 200 °C, the results of which show the superiorities of the SiC device under much higher junction temperature than Si.

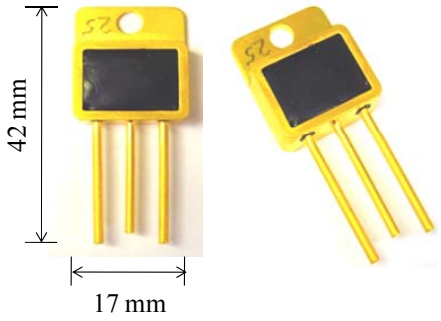


Figure 4-1. CREE 1.2 kV, 20 A prototype SiC MOSFET in TO-247 package

The switching characterization of the device has been conducted under room temperature as well. As described in Chapter 2, a carefully designed double-pulse tester (DPT) with minimized circuit parasitics is used to reveal the intrinsic switching behavior of the SiC MOSFET. Important quantities such as switching times and losses are also recorded and investigated in this chapter.

For the design and analysis of converters utilizing the new device, a compact device model is also a necessity. In this chapter, the Synopsys Saber *Power MOSFET Tool* – a mature Si MOSFET modeling tool – has been used to model the SiC MOSFET successfully. This chapter presents its use as well as some modeling issues and measures about predicting more accurate switching waveforms of the SiC MOSFET.

4.2 Static Characterizations

The static characterizations of SiC MOSFET include DC characteristics (I-V) measured with a Tektronix 371B curve tracer, and AC characteristics (impedances)

measured using an Agilent 4294A impedance analyzer. Characterizations common to both SiC MOSFET and JFET can be found in Chapter 2.

4.2.1 Drain Leakage Current I_{DSS}

Figure 4-2 shows the drain leakage current versus temperature relationship, where a positive temperature coefficient for I_{DSS} can be inferred. As seen from the figure, the leakage current for this SiC MOSFET is well below 10 μA at 1200 V for the entire temperature range, which indicates a good blocking capability of the device at the rated voltage.

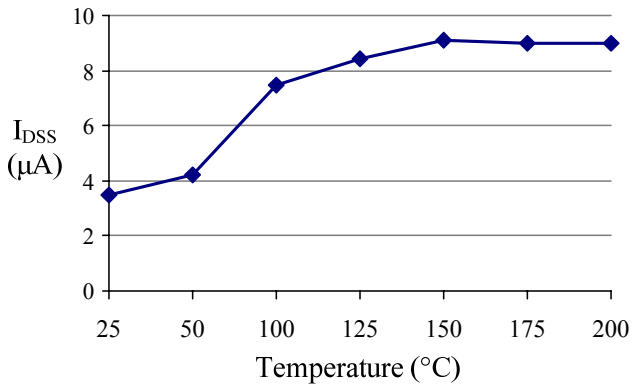


Figure 4-2. Leakage current vs. temperature

4.2.2 Output and Transfer Characteristics

The output characteristics are measured under different gate voltage V_{GS} up to 15 V, which is the suggested drive voltage by the manufacturer. The transfer characteristic, on the other hand, is obtained under 15 V V_{DS} bias while varying V_{GS}. Figure 4-3 plots these characteristics under 25, 100, 125 and 200 °C respectively. The temperature dependence of the output I-V curves of this 1.2 kV SiC MOSFET is quite different from what would be expected for Si MOSFETs, as seen from Figure 4-3 (a). For $V_{GS} < 9$ V, the channel

conductivity increases with the increasing temperature, while for V_{GS} = 15 V the slope of the I-V curve first becomes steeper but then decreases again as the temperature goes up. For the transfer characteristics shown in Figure 4-3 (b), the threshold voltage $V_{GS(TH)}$ basically decreases with increasing temperature as expected, whereas the transconductance g_{fs} increases. Again this is against the general knowledge about Si MOSFETs that g_{fs} should drop under higher temperature. These phenomena, however, can be explained from the temperature dependence of the on-state resistance which will be talked about in the next section.

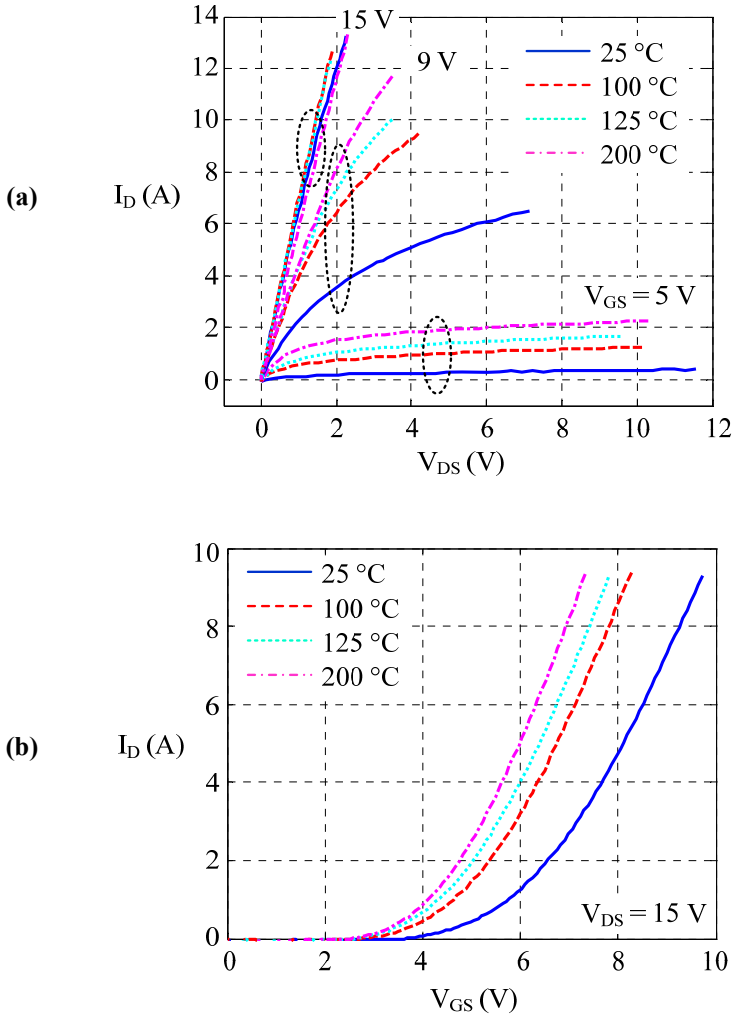


Figure 4-3. Temperature-dependent output (a) and transfer (b) characteristics

4.2.3 On-State Resistance $R_{DS(ON)}$

The on-state resistance can be read directly from the output characteristic curves. In this work $R_{DS(ON)}$ is measured under V_{GS} = 15 V and I_D = 10 A. Figure 4-4 shows the variation of $R_{DS(ON)}$ with regard to the temperature. Different from Si, the SiC MOSFET takes on an initial decrease in $R_{DS(ON)}$ with increasing temperature at low temperatures (< 100 °C), then followed by an increase at higher temperatures. This is because of the different temperature dependence of three primary resistances within the device: channel resistance R_{CH}, JFET region resistance R_{JFET}, and drift layer resistance R_{DRIFT}. These resistances originate from different parts of the MOSFET structure [5]. R_{CH} decreases with increasing temperature due to the threshold voltage reduction and simultaneous increase in the channel mobility. The latter phenomenon is just opposite to Si MOSFET whose channel mobility usually has negative temperature coefficient. R_{JFET} and R_{DRIFT}, on the other hand, increase as temperature rises due to the more active lattice vibrations. At low temperatures, R_{CH} decreases faster than the combined effect of R_{JFET} and R_{DRIFT}, causing the initial decrease in $R_{DS(ON)}$. At higher temperatures, the increasing effect of R_{JFET} and R_{DRIFT} dominates the overall resistance, resulting in the consequent increase in $R_{DS(ON)}$ [6-9]. The non-intuitive temperature dependence of the output and transfer characteristics is thus explained.

It needs to be noted that the above phenomenon is only observed for lower voltage level (e.g. 1.2 kV) SiC MOSFETs, since their channel resistance is comparable to the JFET and drift layer resistances [8-9]. For higher voltage rating SiC MOSFET (e.g. 10 kV), the much thicker drift layer makes R_{CH} negligible compared to R_{DRIFT} and thus gives a positive temperature coefficient for $R_{DS(ON)}$ at all temperatures [3].

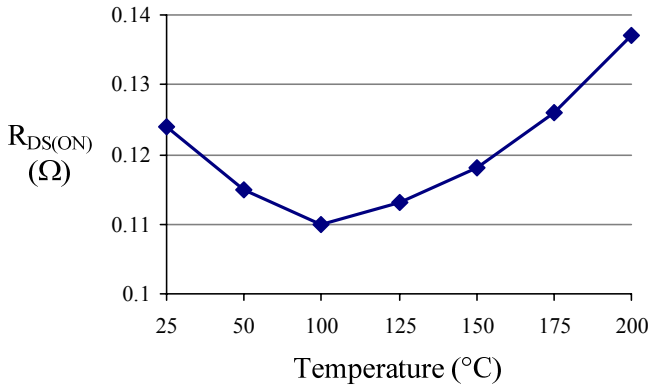


Figure 4-4. On-state resistance vs. temperature

When comparing with state-of-the-art Si technology, a 5-8 times reduction in $R_{DS(ON)}$ can be found for SiC MOSFET at this voltage level. Figure 4-5 (a) illustrates the on-state resistance comparison between the SiC MOSFET under study and a 600 V, 20 A Si CoolMOS (APT20N60BCF by MicroSemi), while Figure 4-5 (b) sketches the $R_{DS(ON)}$ breakdown for SiC and Si MOSFETs respectively. As seen from the figures, the higher breakdown field of the SiC material allows big shrink in drift layer thickness to block the same voltage, resulting in much smaller on-state resistance. Moreover, the junction temperature of SiC MOSFET can go up to as high as 200 °C, while 150 °C is almost the limit for normal Si MOSFET operation. Over the entire temperature range, the resistance of SiC MOSFET is also seen to be less sensitive to the temperature change compared to Si MOSFET.

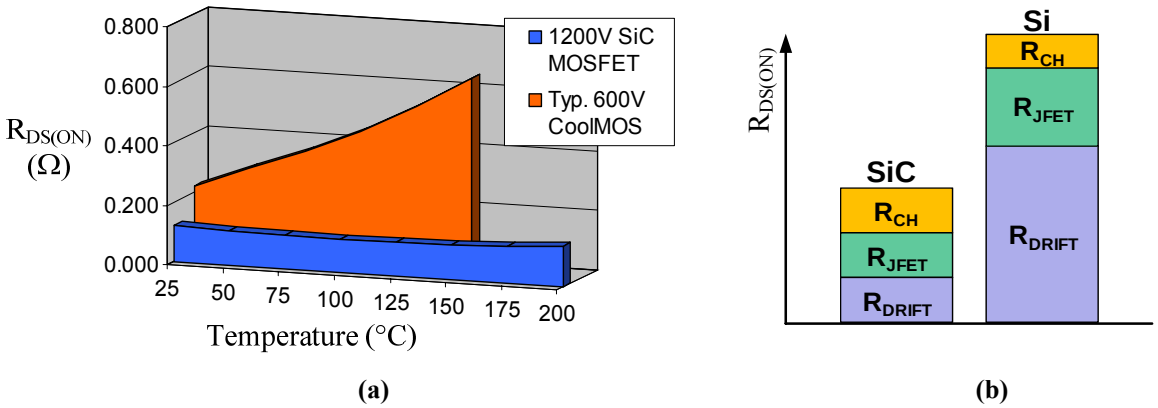


Figure 4-5. $R_{DS(ON)}$ comparison: Si vs. SiC

4.2.4 Gate Threshold Voltage $V_{GS(TH)}$

In some application notes, the gate threshold voltage $V_{GS(TH)}$ is defined as the gate-source voltage which produces 250 μA drain current when drain and gate are shorted (e.g. $V_{DS} = V_{GS}$) [10], but this criterion differs. Some datasheets use bigger drain current such as 1 mA, 2.5 mA, etc, which leads to bigger $V_{GS(TH)}$. This work follows the criterion of 250 μA.

The curve tracer is still used for this measurement because it can sense very small current (μA to mA level) in the High Voltage Mode. However, under this mode the minimum voltage resolution of the instrument is 50 V/div, too coarse for $V_{GS(TH)}$ measurement. Thus an oscilloscope is used to measure the accurate gate-source peak voltage, whose results are shown in Figure 4-6. As one can see, $V_{GS(TH)}$ basically decreases with the increasing temperature, with its lowest value found to be 1.5 V at 150 °C. Note that if a higher drain current criterion were used, the measured $V_{GS(TH)}$ would be higher. However the lower $V_{GS(TH)}$ at higher temperatures still indicates potential false trigger problem of the SiC MOSFET when operating in full power.

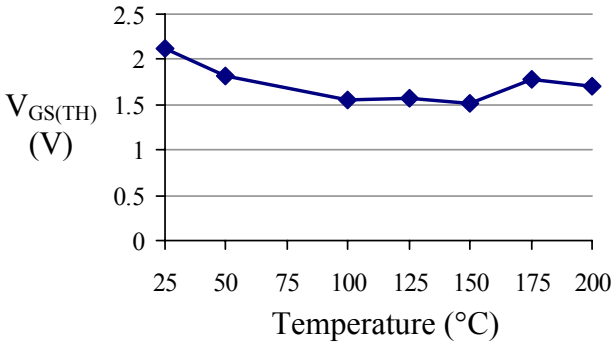


Figure 4-6. Gate threshold voltage vs. temperature

4.2.5 Body Diode I-V Characteristics

The body diode I-V curves are shown in Figure 4-7. Less steep slants are observed as expected due to the increasing series resistance of the diode as the temperature goes up. However, the forward turn-on voltage does not always decrease as expected, and an increase is observed for the 200 °C condition. This phenomenon is different from conventional Si MOSFETs. The cause, according to the manufacturer, is that the body diode conduction involves certain interaction with the MOSFET channel, thus this diode is not a pure PiN diode and its I-V curves are also affected by the channel I-V characteristics. However the essential mechanism behind this phenomenon is still under study now and publications about this issue have not been found so far.

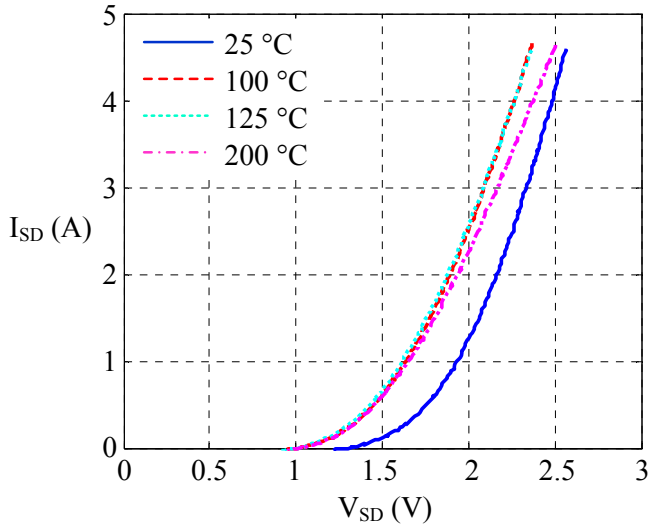


Figure 4-7. Temperature-dependent body diode I-V curves

4.2.6 Internal Gate Resistance R_{GI}

The internal gate resistance is modeled as a lumped resistance in series with the MOSFET gate terminal, representing the distributed resistor network connecting the individual cells within the device [11]. Its value is important as it affects the time constant of the gate voltage and ultimately determines the switching speed limit of the SiC MOSFET. However, this parameter is usually not provided in the datasheet. The measurement of R_{GI} is identical to the measurement of a capacitor equivalent series resistance (ESR), and is carried out with an impedance analyzer measuring the gate-source terminals with the drain and source of the device shorted, as shown in Figure 4-8 (a). This setup equivalently measures the impedance of R_{GI} in series with the input capacitance C_{ISS} (= C_{GS} + C_{GD}), seen as Figure 4-8 (b).

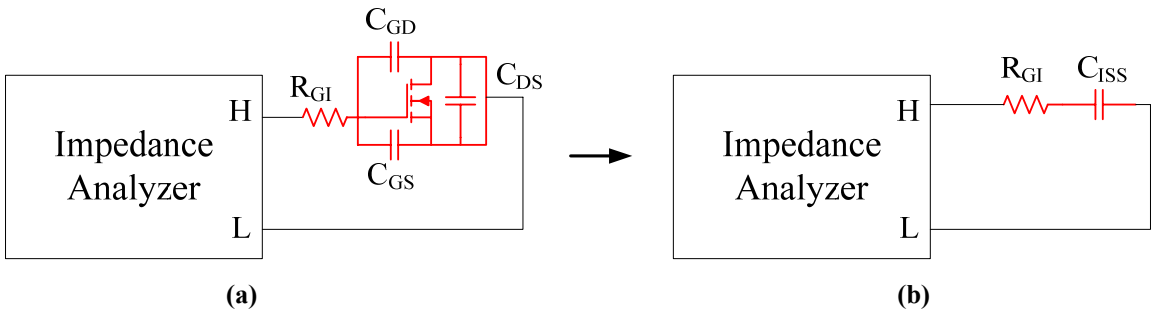
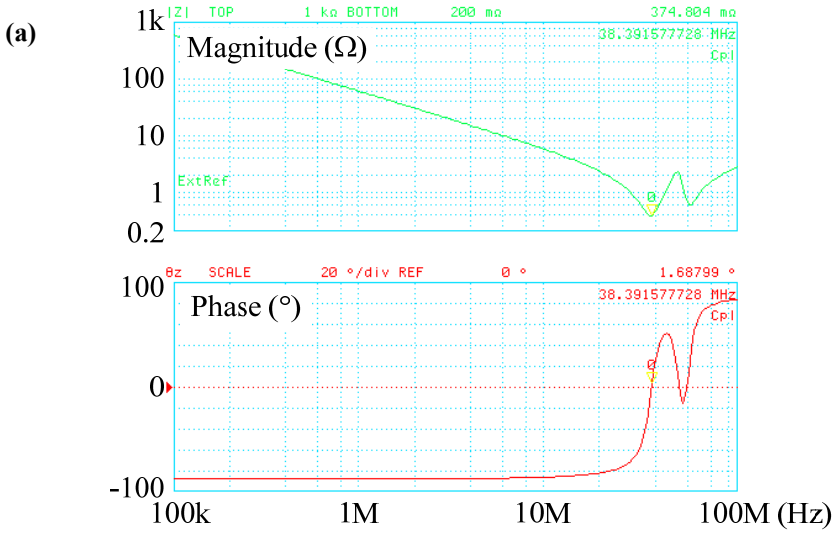


Figure 4-8. Internal gate resistance measurement setup.
(a) Measurement setup, (b) equivalent circuit

The measurement results are displayed in Figure 4-9. Figure 4-9 (a) exhibits the originally measured impedance vs. frequency curves. As one can see, the distributed parameter nature of the internal gate resistance causes several resonant peaks beyond 30 MHz, whereas only one value should be selected for the lumped R_{GI} model. If choosing the resistance at the first resonant peak (at around 38 MHz), then R_{GI} vs. temperature graph can be plotted in Figure 4-9 (b), which depicts an linearly increasing resistance of 0.4 Ω to 0.55 Ω with the increasing temperature.



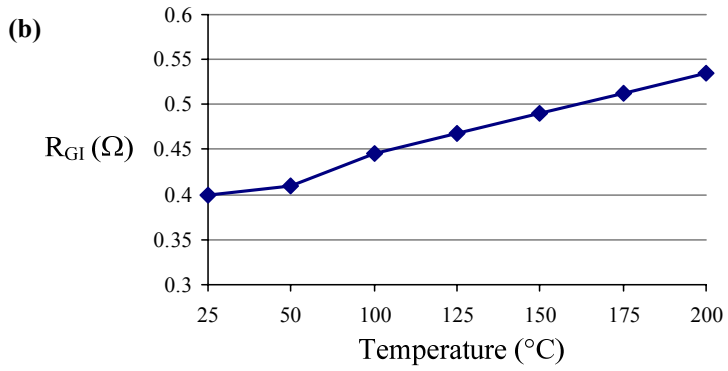


Figure 4-9. Internal gate resistance. (a) Measured impedance at 25 °C, (b) R_{GI} vs. temperature

4.2.7 Nonlinear Junction Capacitances C_{ISS}, C_{RSS} and C_{OSS}

The junction capacitances, namely input capacitance C_{ISS} (= C_{GS} + C_{GD}), reverse transfer capacitance (or Miller capacitance) C_{RSS} (= C_{GD}), and output capacitance C_{OSS} (= C_{DS} + C_{GD}), are formed by the gate oxide layer and PN junctions within the MOSFET. From the device structure, the gate oxide layer capacitance C_{GS} is essentially a linear capacitance, while the PN junction capacitances C_{GD} and C_{DS} are strongly nonlinear functions of drain-source voltage V_{DS} [12]. These parameters are of vital importance to the MOSFET as they determine the dynamic behavior of the device during switching transients. As for their measurements, the impedance analyzer alone is not sufficient as it cannot provide high enough voltage to bias the device (only 40 V maximum for Agilent 4294A). In this case, auxiliary circuits are adopted together with the impedance analyzer to extend the voltage bias to a much wider range. The circuits used in this work are modified from [10], [13], and are illustrated in Figure 4-10 through Figure 4-12.

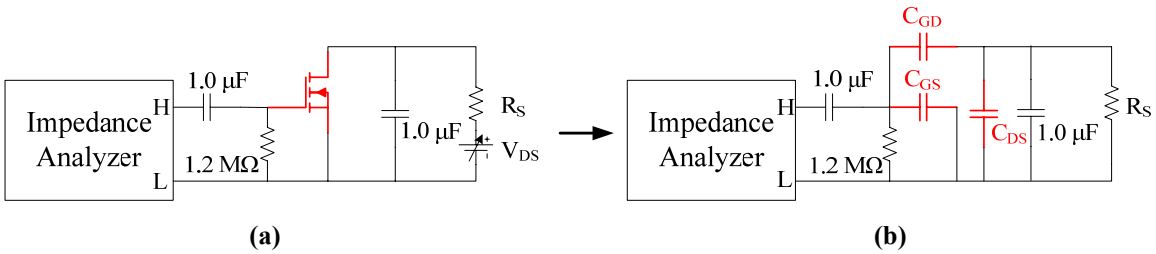


Figure 4-10. C_{ISS} measurement setups. (a) Real circuit, (b) equivalent AC circuit

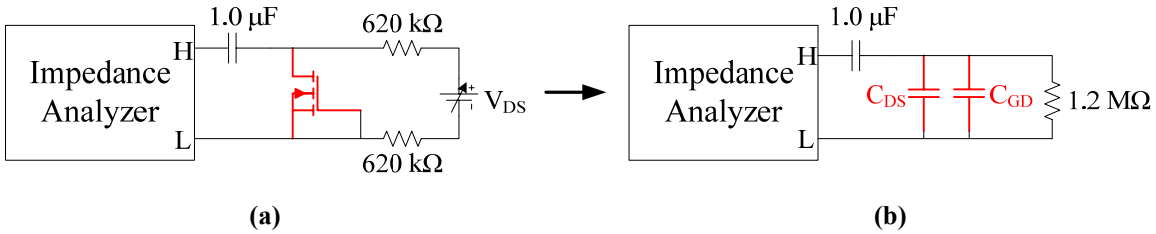


Figure 4-11. C_{OSS} measurement setups. (a) Real circuit, (b) equivalent AC circuit

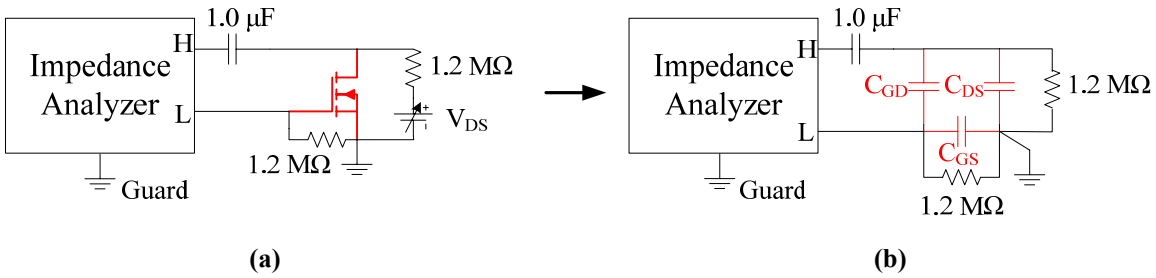


Figure 4-12. C_{RSS} measurement setups. (a) Real circuit, (b) equivalent AC circuit

In the above figures, the 1 µF capacitor directly connected to the "H" terminal is used to isolate the instrument from the high voltage DC source V_{DS}. The oscillation level of the impedance analyzer is chosen to be only 50 mV because the junction capacitances are very sensitive to the amplitude of the small signal. The capacitance values are read at 1 MHz for all measurements, which is also the frequency used in most datasheets. With the above configurations, the measured capacitance is effectively the junction capacitance in series with the isolation capacitance, and the capacitance of interest can be simply compensated by

$$C_u = \frac{C_k C_m}{C_k - C_m} \tag{4-1}$$

where C_u is the junction capacitance to be measured, C_k is the isolation capacitance, and C_m is the measured capacitance. In this case, however, considering that junction capacitances are usually in the range of tens of pF to several nF, these measurements will still produce very small error even without compensating off C_k, namely $C_u \approx C_m$.

The measurements are taken under three different temperatures 25, 125, and 200 °C respectively, and the results are shown in Figure 4-13. As seen, the junction capacitances drop drastically in the first 30 V and then decrease very slowly as the bias voltage continues increasing. The bias voltage stops at 250 V since the trend of each C-V curve can be seen clearly and extrapolation is quite easy. One can also tell from the overlapped curves that the C-V characteristics are insensitive to the change of temperature.

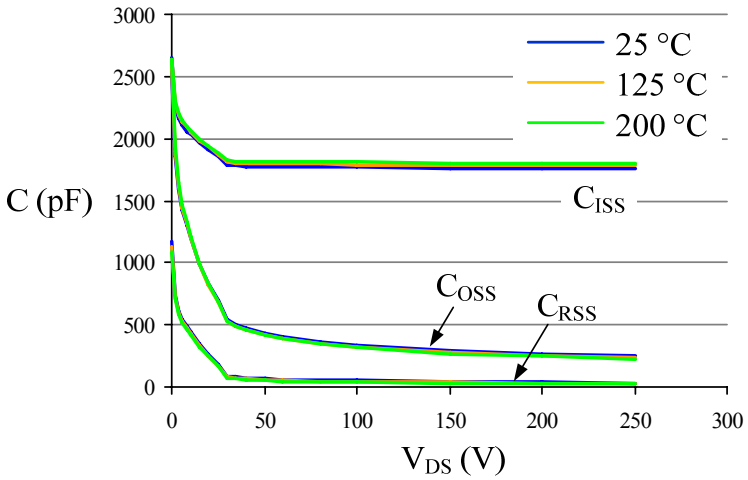


Figure 4-13. Temperature-dependent capacitance-voltage characteristics

It also needs to be noted that, although the measurement circuits look very simple, they cannot be implemented using breadboards, because the breadboards themselves

carry tens of pF intrinsic parasitic capacitance which will cause great relative error to the measurement results at high V_{DS} bias. For this reason, three small printed circuit boards (PCB) are made to provide interconnection for each measurement. Besides eliminating parasitic capacitances, these small PCBs are also suitable for temperature-dependent measurements, as seen in Figure 4-14 (a) and (b).

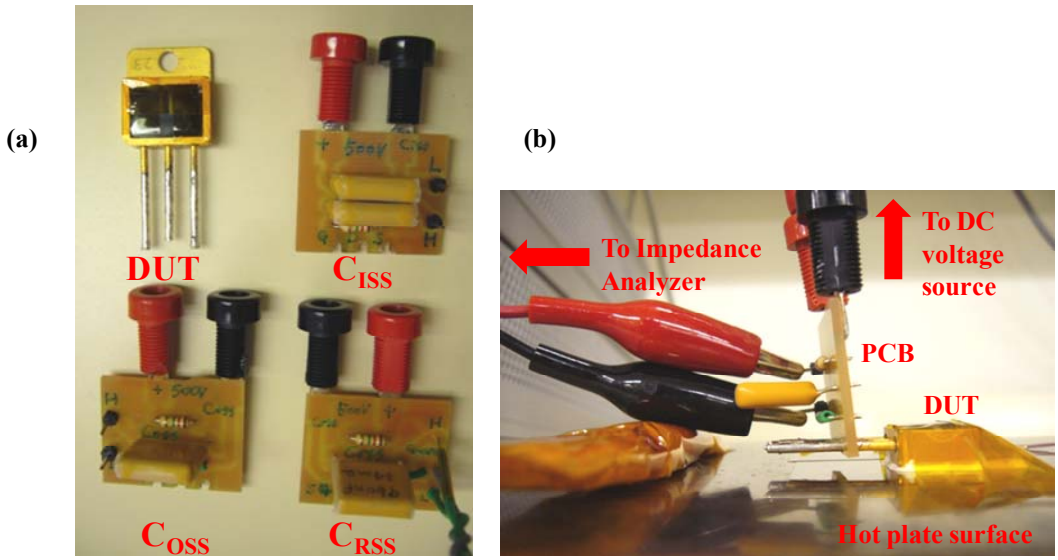


Figure 4-14. Junction capacitance measurement PCBs.
(a) DUT and PCBs, (b) setup for elevated temperature measurements

4.2.8 Package Stray Inductances L_G, L_D and L_S

The device under study is in a TO-247 package. The stray impedances of the package can be lumped by three inductances L_G, L_D and L_S, which are in series with the gate, drain, and source terminals respectively [14]. Basically three measurements are necessary to extract the stray inductances. As shown in Figure 4-15, measuring the inductance between gate and source terminals with the drain floating gives the value of $L_G + L_S$. Likewise, measuring drain and source inductance gives $L_D + L_S$, and measuring gate and drain gives $L_G + L_D$. The respective stray inductances can then be simply calculated from

these measurements. In this case, the inductances are measured to be L_G = 4.5 nH, L_D = 0.04 nH, and L_S = 3.2 nH respectively, which are typical values for the package. Note that L_D is much smaller than the other two inductances because the drain of the MOSFET is attached to the package case, forming smaller loop and thus smaller inductance.

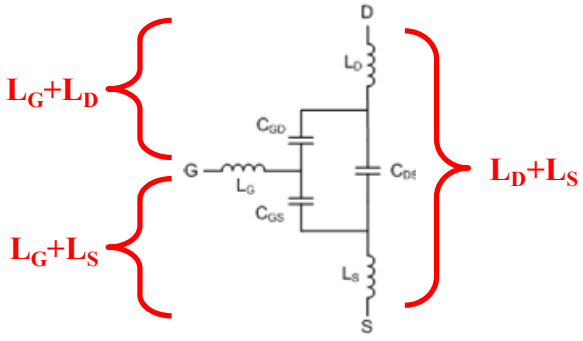


Figure 4-15. Measurements of package stray inductances

The measured stray inductances, however, are strongly affected by the lead lengths in the measurements. The above results are measured at the roots of the package leads (See Figure 4-16 (a)), but when measured at the tips of the leads, the inductances would be almost five times bigger (Figure 4-16(b)). Therefore, when including package parasitics in the MOSFET model, it is important to relate the actual stray inductances to how the device is mounted on the PCB, otherwise the stray inductance values would be meaningless.

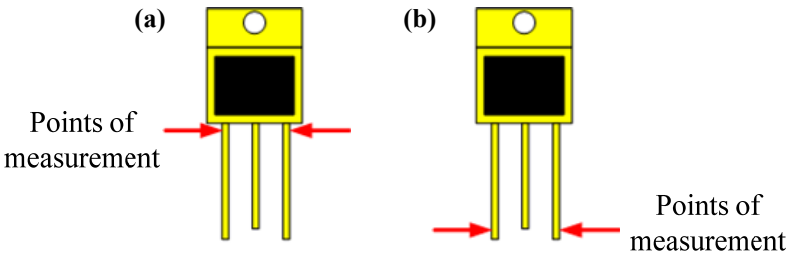


Figure 4-16. Different measurements of package stray inductances. (a) At roots, (b) at tips

4.3 Switching Characterizations

The switching characteristics of the SiC MOSFET are also measured under room temperature with the use of the double-pulse tester described in Chapter 2. In this work, the switching characterizations are done up to 600 V while varying the load current from 4 A to 10 A, leaving enough margin for the current spike. The switching speed is adjusted by using different gate resistances of 10 Ω, 5 Ω and 2 Ω respectively.

4.3.1 Typical Switching Waveforms of SiC MOSFET

Figure 4-17 shows the typical turn-on and turn-off transients of the gate voltage V_{GS} and current I_G, the drain-source voltage V_{DS}, as well as the drain current I_D, under 600 V, 8 A switching condition with a gate resistance of 10 Ω. As seen from the figure, the rise and fall slew rates of I_D are quite fast compared to V_{DS}, achieving 6.5 ns during turn-on and 24.4 ns during turn-off, while it takes 63.1 n and 41.2 ns for V_{DS} to achieve full swing during turn-on and turn-off respectively. Also, compared with typical Si MOSFET gate voltage waveform, the SiC MOSFET does not have a very obvious "plateau" region in V_{GS}. This is because the SiC MOSFET has a bigger channel-length modulation coefficient than the conventional Si device. Or, in another word, the I-V curves of the SiC MOSFET are not as flat as those of Si MOSFET in the saturation region, which can be inferred from Figure 4-3 (a).

Similar switching characteristics can also be observed in other switching conditions with reduced gate resistance. Figure 4-18 shows the typical switching waveforms under 600 V, 8 A with R_G = 5 Ω, while Figure 4-19 exhibits the 600 V, 4 A, R_G = 2 Ω case. As seen, using smaller gate resistance makes the switching speed faster. However, this also

causes more severe parasitic ringing during the switching transients, which is apparent from these figures.

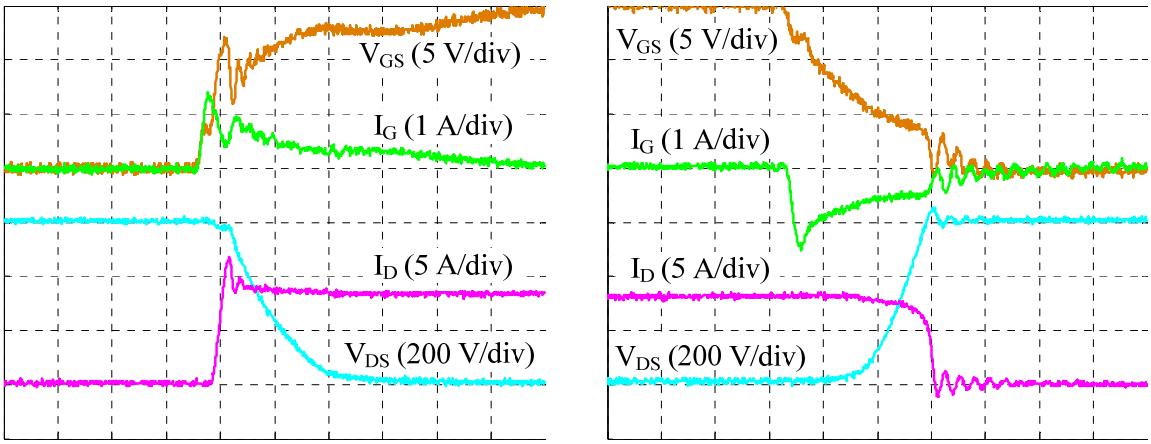


Figure 4-17. Typical turn-on (a) and turn-off (b) waveforms under 600 V, 8 A with R_G = 10 Ω. Time: 40 ns/div

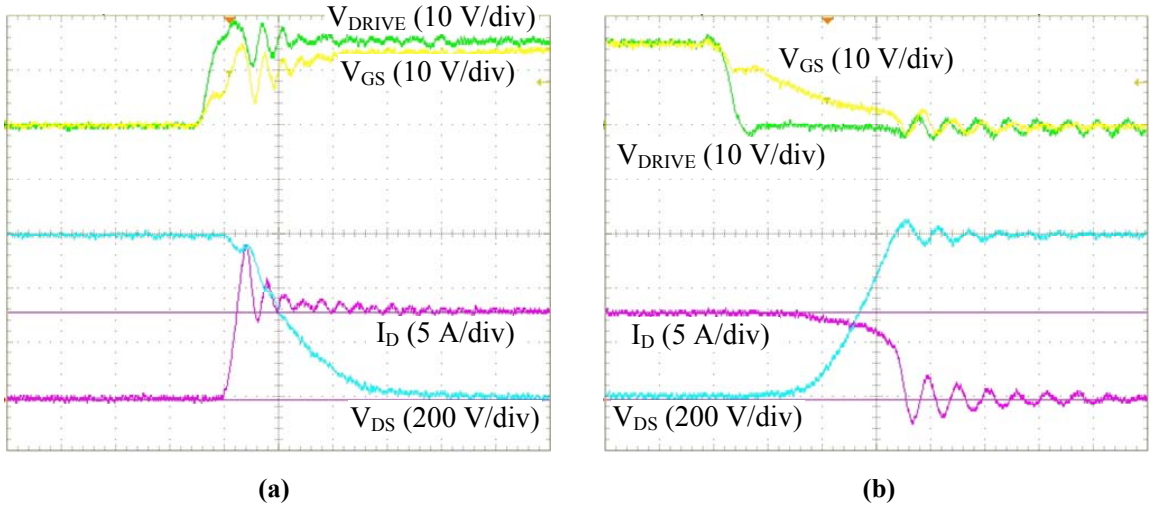


Figure 4-18. Typical turn-on (a) and turn-off (b) waveforms under 600 V, 8 A with R_G = 5 Ω. Time: 20 ns/div

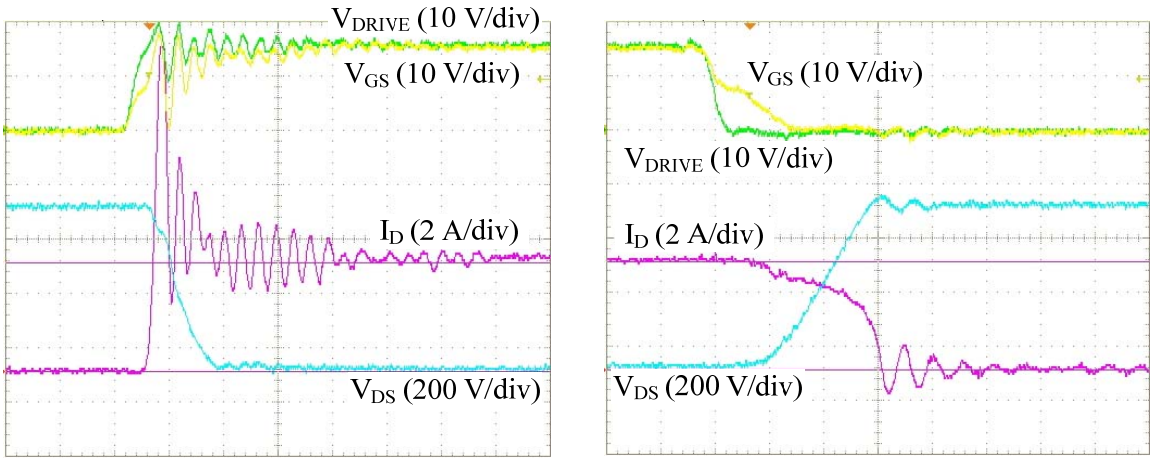


Figure 4-19. Typical turn-on (a) and turn-off (b) waveforms under 600 V, 4 A with R_G = 2 Ω. Time: 20 ns/div

4.3.2 Body Diode Reverse Recovery Characteristic

The reverse recovery characteristic of the SiC MOSFET body diode has also been tested using a similar tester except that the body diode now is working as the freewheeling diode. Figure 4-20 shows the comparison of the body diode reverse recovery characteristic between the SiC MOSFET, a 1.2 kV SiC SBD from CREE, and a 600 V Si CoolMOS from MicroSemi. At present, the inferior performance of the Si MOSFET body diode is the main bottleneck for high-frequency applications with ZVS operation. From the figure, however, it can be seen that the body diode of SiC MOSFET has a significant improvement in the reverse recovery performance, with only about 40 ns reverse recovery time (t_{rr}) at the room temperature. This performance is even comparable to that of the SiC Schottky diode. The low t_{rr} is mainly a result of the very small minority carrier lifetime as well as the thin drift layer. Moreover, unlike Si devices, t_{rr} of the SiC MOSFET is relatively insensitive to the temperature change [15].

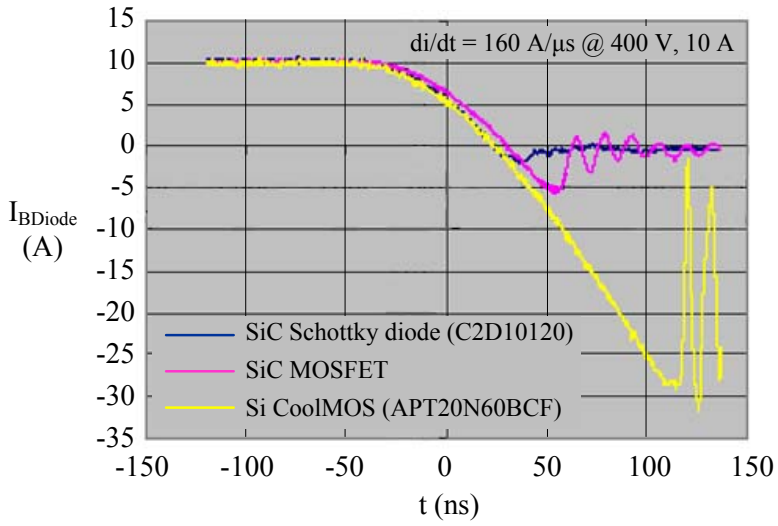


Figure 4-20. Body diode reverse recovery characteristic comparison between 1.2 kV SiC SBD, 1.2 kV SiC MOSFET, and 600 V Si CoolMOS. Measured at room temperature

4.3.3 Major Switching Characteristics

Switching times t_{on}, t_{off} and switching energies E_{on}, E_{off} are defined in Chapter 2. Figure 4-21 exhibits the device total turn-on and turn-off times at 600 V as a function of the load current for different gate resistances. As seen, both the turn-on and turn-off times are approximately in linear proportion to the load current. The turn-on time increases with the load current, which is in accord with the common intuition, whereas the turn-off time decreases with the load current. This reduction is because higher drain current leads to higher "plateau" voltage in V_{GS} during turn-off, increasing the gate discharge current and thus speeding up the turn-off process. The detailed discussion about MOSFET switching behavior can be found in Chapter 2.

Also note in the figure that only one load current (4 A) is tested for R_G = 2 Ω case. This is to leave enough margins for the very high current spike (almost three times the steady-state value as seen in Figure 4-19 (a)) during MOSFET turn-on process that would

possibly degrade the device's static characteristics. The next section will discuss more about the device degradation.

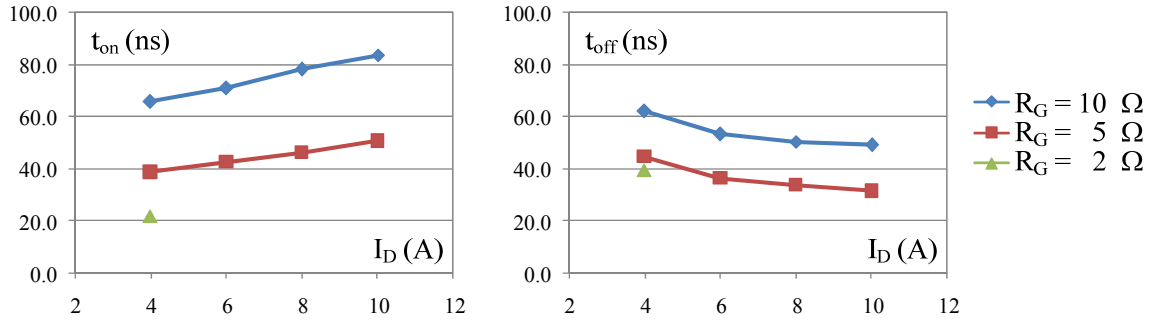


Figure 4-21. Switching times vs. load current at 600 V, for different switching speeds. (left) Turn-on times, (right) turn-off times

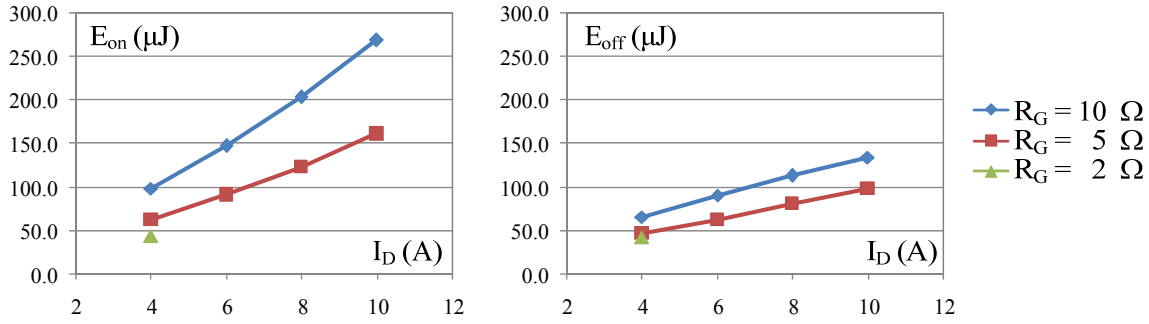


Figure 4-22. Switching energies vs. load current at 600 V, for different switching speeds. (left) Turn-on energies, (right) turn-off energies

Figure 4-22 shows the switching energies versus drain current for different switching speeds. Both the turn-on and turn-off energies increase almost linearly with the load. However, E_{off} does not increase as fast as E_{on} because of the reduction in the turn-off time. Also seen from the figure is the remarkable reduction in the switching energies as the gate resistance is cut by half from 10 Ω to 5 Ω, while only minor improvement can be observed when R_G is further reduced by half to 2 Ω. Figure 4-23, on the other hand, exhibits the device stresses under the increasing switching speed, which implies that the

benefits obtained from faster switching speed are accompanied by the penalties of worse device stresses and electromagnetic noises due to the high-frequency parasitic ringing.

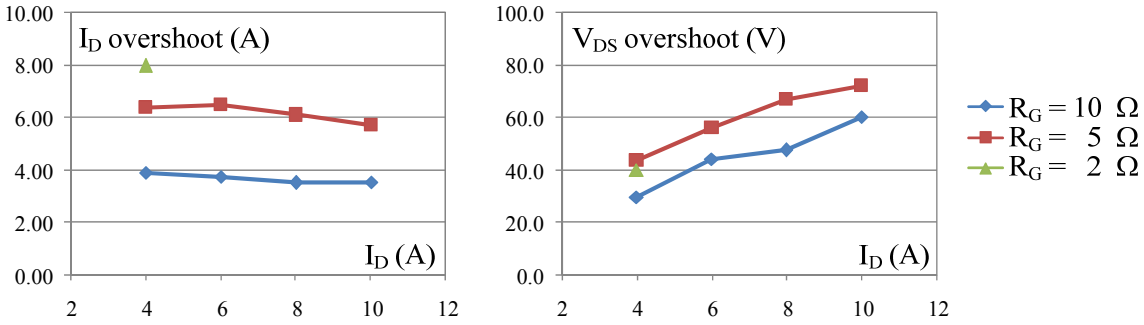


Figure 4-23. Device stresses vs. load current for different switching speeds. (left) I_D overshoot during turn-on, (right) V_{DS} overshoot during turn-off

4.3.4 Summary of Device Characterization

To summarize the SiC MOSFET static and switching characterization results, the following "datasheet" can be tabulated.

Table 4-1. CREE 1.2 kV, 20 A SiC MOSFET datasheet

Parameter	Symbol	Test Conditions	Value	Unit
Drain leakage current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 1200 V	3.5 / 9.2 (1)	µA
Gate threshold voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 µA	2.1 / 1.7 (1)	V
On-state resistance	$R_{DS(ON)}$	V_{GS} = 15 V, I_D = 10 A	0.124 / 0.137 (1)	Ω
Input capacitance	C_{ISS}	f = 1 MHz, osc. level = 50 mV	1955 / 1864 (2)	pF
Output capacitance	C_{OSS}		617 / 170 (2)	
Reverse transfer capacitance	C_{RSS}		185 / 37 (2)	
Gate stray inductance	L_G	Osc. level = 500 mV	4.5	nH
Drain stray inductance	L_D		0.04	
Source stray inductance	L_S		3.2	
Turn-on time	t_{on}	V_{DS} = 600 V, V_{GS} = 0/15 V, I_D = 10 A	83.7 / 50.5 (3)	ns
Turn-on energy	E_{on}		268.5 / 161.0 (3)	µJ
Turn-off time	t_{off}		49.1 / 31.4 (3)	ns

Turn-off energy	E_{off}		134.0 / 97.7 (3)	µJ

If not specified, all data are in room temperature (~ 25 °C)

(1) Before slash – 25 °C; after slash – 200 °C.

(2) Before slash – V_{DS} = 25 V; after slash – V_{DS} = 200 V.

(3) Before slash – R_G = 10 Ω; after slash – R_G = 5 Ω.

4.4 Device Degradation

Device degradation has also been observed after the switching characterization. Figure 4-24 exhibits the static I-V curves of one SiC MOSFET before (red curves) and after (blue curves) the double-pulse tests. This specific DUT has been switched up to 800 V and 20 A with 15 V gate voltage. As seen, the threshold voltage $V_{GS(TH)}$ increases by more than 1 V, and the on-state resistance $R_{DS(ON)}$ doubles from 124 mΩ to 249 mΩ after the switching tests. The body diode I-V characteristic has degraded as well. The same kind of degradation has also been confirmed by the manufacturer. The cause of the degradation, however, has many possible explanations.

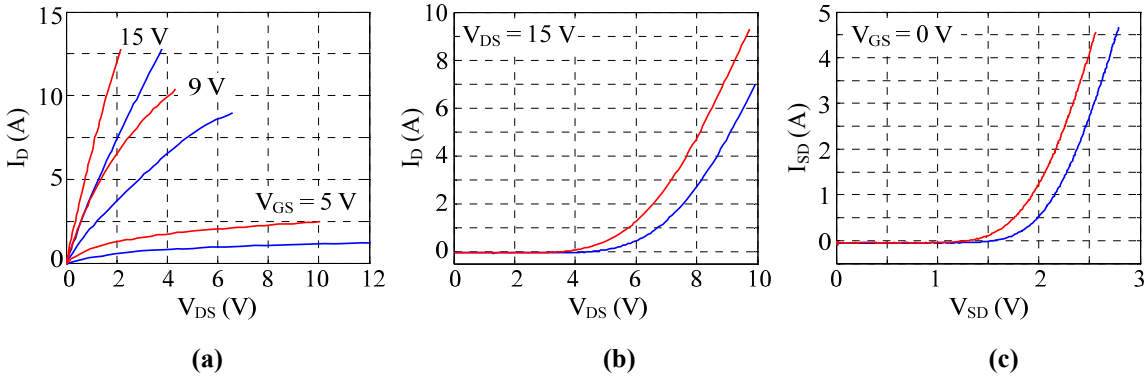


Figure 4-24. SiC MOSFET degradation after switching tests. (a) Output characteristics, (b) transfer characteristic, (c) body diode I-V characteristic. Red – before test; blue – after test

There have been several papers discussing the reliability issues of the SiC MOSFET [16-18]. According to [16], one possibility of degradation is due to the gate oxide defects

which tend to increase the threshold voltage $V_{GS(TH)}$, and resultantly increase $R_{DS(ON)}$ under the same gate voltage. The oxide defects are caused by the so-called Fowler-Nordheim tunneling current, which is higher for SiC than Si under the same oxide layer electric field due to the inherent property of the SiC-dielectric interface. Besides, to achieve a very low $R_{DS(ON)}$ a 15 V gate voltage is used to switch the SiC MOSFET, which is higher than the normal gate voltage (usually 10 V) for Si MOSFET. In this sense, SiC MOSFETs would face more serious long-term reliability issue than Si MOSFETs. According to [16-17], the gate oxide reliability issue is the most likely cause of the degradation for this 1.2 kV SiC MOSFET.

Another degradation mechanism is the stacking faults. It is reported in [18] that the phenomenon of recombination-induced stacking faults (SFs) will occur in 10 kV-level SiC MOSFETs when the body diode is conducting. The SFs are claimed to be caused by the basal plane dislocations formed in the epi-layer during the recombination process, and are positively related to the thickness of this layer. Device degradations, such as higher $R_{DS(ON)}$, larger leakage current and greater body diode on-voltage, etc, will occur due to the SFs. Therefore, it is recommended in [18] that the body diode of the 10 kV-level SiC MOSFET be bypassed by an external anti-parallel diode. However, as the epi-layer thickness reduces for lower voltage structures, such as the 1.2 kV SiC MOSFET in this work, the SFs, although still existent, are not expected to show significant impact on the device degradations.

To verify this statement, a SF test is conducted on the 1.2 kV SiC MOSFET by conducting a continuous DC current of 5 A in its body diode. The case temperature is kept at 50 °C during the test, and the conduction continues for 0.5, 1, and 1.5 hours

sequentially, adding up to a total of 3 hours, similar to the test conditions used in [18]. The MOSFET output and transfer characteristics, as well as the body diode I-V curve are measured after each period, and the results are shown in Figure 4-25. As seen, no obvious degradation can be observed after the SF test, implying that SFs are not very likely to be the cause of degradation in this work.

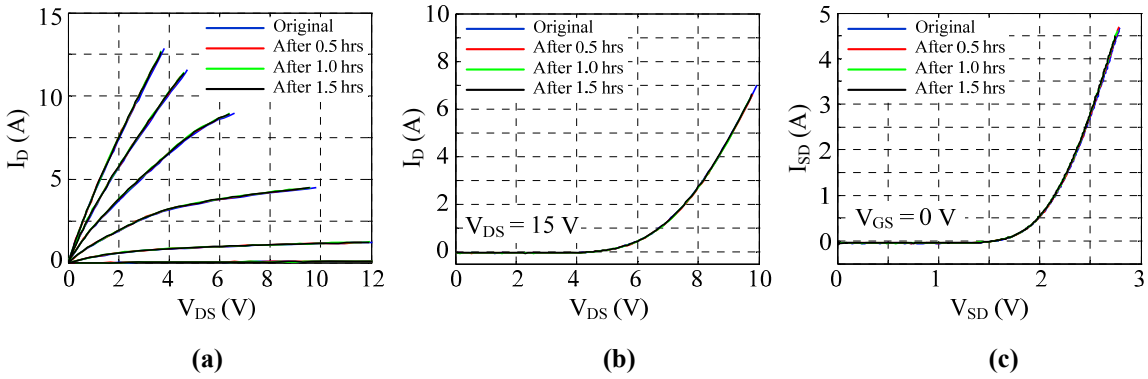


Figure 4-25. Stacking faults test results.
(a) Output characteristics, (b) transfer characteristic, (c) body diode I-V characteristic

However, the above short-term test still cannot guarantee the long-term reliability of the device. It has also been noticed that the degradation occurs only after the device switching high current. For instance, when the switching current of the MOSFET is limited within 10 A, the device is safe and its static characteristics almost do not change. Nonetheless, when the current is close to 20 A, the degradation becomes apparent right away. From this angle, the degradation may also be related to the high-current conduction in the MOSFET channel, or the combined effect of both high current and the resultant high junction temperature. Future efforts are necessary to identify the ultimate cause of the degradation.

4.5 Modeling of SiC MOSFET

4.5.1 General Structure of a Power MOSFET Subcircuit Model

There have been many preceding works on the modeling of SiC MOSFET. Some papers developed physical models for SiC MOSFET which focused more on the fundamental physical characteristics of the device, such as [19-21]. This type of MOSFET model is not suitable for circuit simulation and system analysis, so is not preferred in this work. More papers used subcircuit model instead to describe the SiC MOSFET [7][9][22]. [23-25] discussed subcircuit models of Si power MOSFET but many concepts and ideas introduced in these references are still valuable for SiC MOSFET modeling. Although the developed model differs in each work, the structures of these models, however, are more or less similar, and can be simplified as the circuit shown in Figure 4-26.

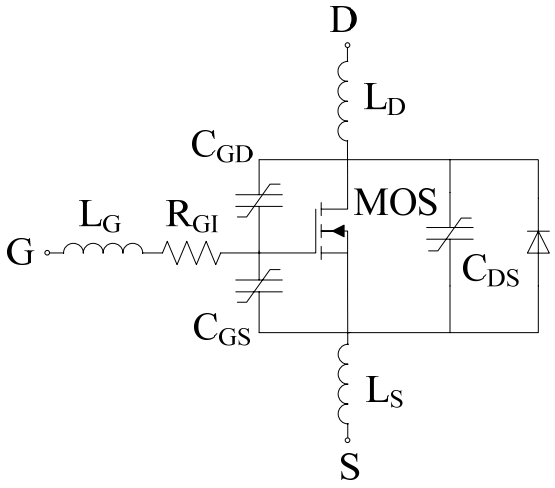


Figure 4-26. General subcircuit model structure of power MOSFETs

The major components of the MOSFET model include:

(A) MOS: Ideal MOSFET

The MOS part in the model structure looks like a MOSFET. Indeed this part represents an ideal MOSFET and describes the static I-V characteristics of the device, namely output and transfer characteristics and their temperature dependence. This is the most common subject in most MOSFET modeling papers, and different papers have different ways to describe this part. For example, [7] and [22] reuse the built-in lateral MOSFET model in SPICE to describe the characteristics of SiC MOSFET; [9], on the other hand, established its own channel current expressions that considered the different channel regions and enhanced linear region transconductance of SiC MOSFETs. No matter what method is used, the goal is always to capture the device static characteristics accurately.

(B) Body diode

The body diode is a parasitic component formed by the PN junction between the drain-source terminals of the vertical structure power MOSFET. This diode is necessary for the MOSFET if used, and can usually be modeled as a power diode connected in anti-parallel with the MOSFET. The major characteristics include the forward conduction characteristic, junction capacitance, as well as reverse recovery characteristic. The junction capacitance can usually be lumped into the MOSFET drain-source capacitance C_{DS}. [26-27] discussed general PiN diode modeling and SiC PiN diode modeling.

(C) C_{GS}, C_{GD} and C_{DS}: MOSFET parasitic capacitances

The capacitances surrounding the MOSFET in Figure 4-26 are the device parasitic capacitances, where C_{GS} is mainly the gate oxide capacitance and C_{GD}, C_{DS} represent the PN junction capacitances between gate-drain and drain-source terminals. These

parameters are significant to the MOSFET model because they determine the switching behavior of the device.

Most models treat C_{GS} as a linear capacitance due to the fact that it is mainly formed by a linear dielectric – the gate oxide layer. However, as some papers pointed out, this capacitance increases when V_{GS} becomes negative [24-25]. This nonlinearity is important for the model when a negative gate voltage is used.

C_{GD} is also called the Miller capacitance and is the most important nonlinear capacitance for the MOSFET model especially in the inductive load, hard-switching condition, due to the Miller effect [24]. The reason for this will be explained mathematically later. Different papers use different nonlinear equations to describe the voltage dependence of this capacitance, and the independent variable (i.e. the voltage) also differs. Some papers model C_{GD} to be dependent on V_{GD} [7][9][23], while some other works and most datasheets express C_{GD} as a function of V_{DS}.

C_{DS} is also a nonlinear function of V_{DS}. [24] pointed out that this capacitance is important in damping V_{DS} overshoot in unclamped inductive load and ZVS operation, but not significant in determining PWM clamped inductive load switching waveforms. Perhaps for this reason most papers do not talk about the modeling of this capacitance and its effect on the MOSFET switching waveforms. However, in Chapter 6 of this thesis, C_{DS} effects as well as those of the other two capacitances will all be studied and discussed in detail.

(D) R_{GI}: Internal gate resistance

The internal gate resistance becomes important in high-speed switching conditions. As the external gate resistance is reduced to speed up the switching transients, this resistance

will finally become the major damping factor within the gate drive loop. Considering the distributed nature of the gate contact mesh, the modeling of a lumped resistance R_{GI} is only an approximation of the overall contact resistances.

(E) L_G, L_D, L_S: Package stray inductances

These inductances are necessary only if the MOSFET is packaged. They can be removed or set to zero when the device comes in die form.

The purpose of this work is to build a SiC MOSFET model so that its switching behavior and performance can be studied through simulation. To achieve this goal all of the above components should be included to make a complete MOSFET model. This effectively eliminates the papers which only talk about part of (A) to (E), such as [20-21]. Moreover, the model should be simple in terms of parameter extraction and should not contain any inaccessible parameters to the device users. This also makes some other approaches not suitable for this work, such as [7] and [9]. Based on these reasons, this work explores the possibility of building a SiC MOSFET model based on the conventional static and switching characterization data previously obtained, by the use of a mature Si MOSFET modeling tool. To this end, the Synopsys Saber *Power MOSFET Tool* is used to build the model for this 1.2 kV SiC MOSFET [28].

4.5.2 Modeling Processes and Issues

The Saber *Power MOSFET Tool* generates the level-1 model which is well suited for examining the switching transients and losses of the power MOSFET. The graphic user interface of the program is displayed in Figure 4-27, which also shows the model structure. It can be seen that this model basically follows the general model structure shown in Figure 4-26.

This modeling tool requires the device information of output and transfer characteristics, body diode characteristic, parasitic capacitances, internal gate resistance, as well as package stray inductances, all of which can be obtained from the characterization process presented in Section 4.2 and 4.3. These characteristic curves and parameters can be imported into the program, and the model parameters can be adjusted visually to curve-fit the imported data. A built-in optimization function of the program can also be used to achieve an optimal curve-fit of the imported data. Detailed modeling procedures can be found in Chapter 4 and Chapter 8 of [29].

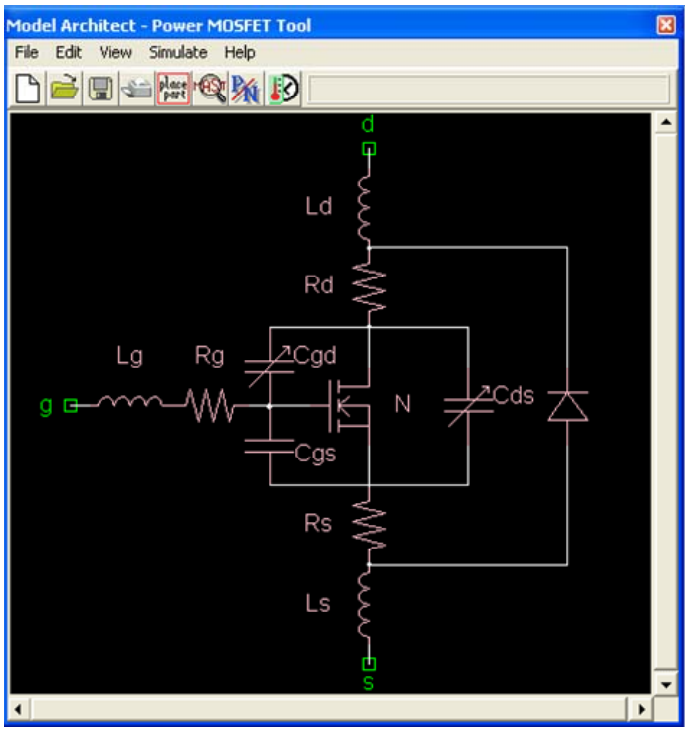


Figure 4-27. Saber *Power MOSFET Tool* graphic user interface

The temperature-dependent characteristics of the device will be modeled in this program as different sets of model parameters for several discrete temperatures, and Saber will automatically calculate the linear interpolations of these parameters to

determine the model behavior at any given temperature. In this sense, modeling at 25 °C has the same process as modeling at 200 °C. Therefore in this section the SiC MOSFET is only modeled at the room temperature.

Figure 4-28 shows the curve fitting results of the SiC MOSFET output and junction capacitance characteristics, which are apparently good predictions from the figure. However, in order to simulate the switching behavior of the device more accurately, measures should be taken beyond simply fitting the characteristic curves.

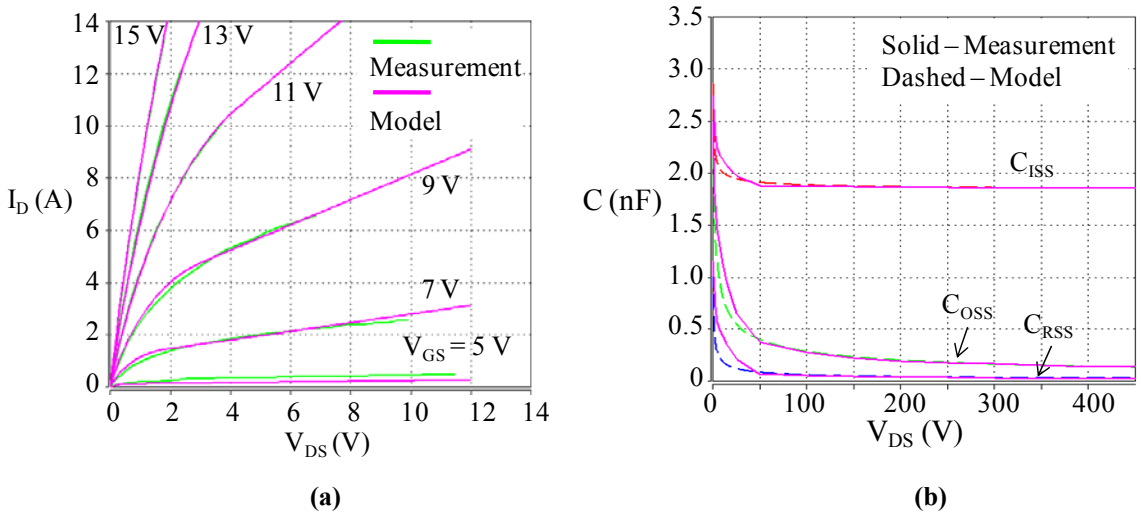


Figure 4-28. Curve fitting results of (a) output characteristics, and (b) junction capacitances

One problem lies in the curve-fitting of the output characteristics. Different from Si MOSFET, the I-V characteristics of SiC MOSFET transit gradually from the linear region to the saturation region [9]. Therefore, the device has not fully entered the saturation region even if the curve tracer has reached its maximum output voltage of 30 V, which can be inferred from Figure 4-3 (a). Conducting the curve-fitting only in the linear and transition regions may lead to erroneous saturation region characteristics for the model. In Figure 4-28 (a) the mathematically optimal curve-fitting result gives the

channel-length modulation parameter LAMBDA (i.e. the slope of the I-V curves in the saturation region) of about 0.15, which is far too big for a reasonable LAMBDA value.

The parameter of LAMBDA is critical as it determines the shape of the saturation region. Simulation shows that the model with better fitted saturation region can predict the switching waveforms more accurately (Refer to Appendix A). This result is also intuitive because, according to Chapter 2, most part of the device switching trajectory lies in the saturation region under the clamped inductive load. The major slew rates of both the voltage and current waveforms are consequently affected by the shape of this region. Therefore, it is necessary to get a picture about how the saturation region looks like, when it is not available from the curve tracer measurement.

The information needed for reconstructing the saturation region is the transfer characteristic under high V_{DS} bias, which can be extracted by plotting I_D vs. V_{GS} from the switching waveforms. This follows from the MOSFET switching theory that when I_D rises and falls in a clamped inductive load, V_{DS} keeps almost constant, and the switching trajectory is well within the saturation region where the I_D vs. V_{GS} graph represents the transfer characteristic at the corresponding V_{DS} bias [12]. To get this graph, the MOSFET should be switched very slowly at the desired V_{DS} by using a big gate resistance to minimize the circuit parasitic ringing and the currents flowing through the MOSFET junction capacitors. In this work, a 200 Ω gate resistance is used and the MOSFET is still switched using the aforementioned double-pulse tester.

The I_D-V_{GS} curves obtained in this way, however, are different for turn-on and turn-off processes, seen as the blue and yellow curves in Figure 4-29 (a). This is due to the voltage measurement aberrance in the V_{GS} waveform caused by the common source

inductance L_{SS}, as illustrated in Figure 4-29 (b). To compensate off the L_{SS} effect, the real I_D-V_{GS} relationship can be derived as follows.

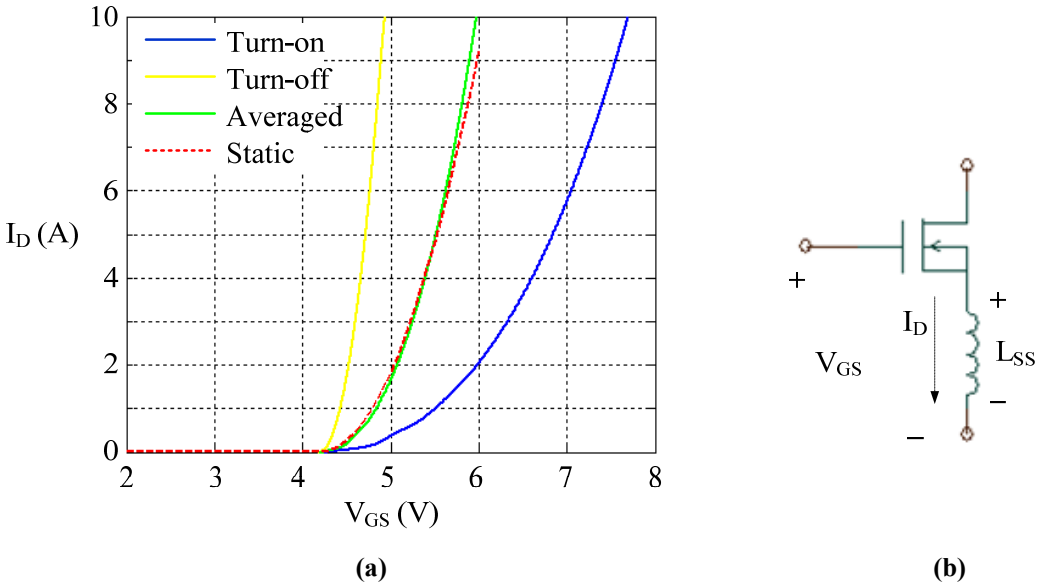


Figure 4-29. Verification of transfer characteristic prediction in simulation.
(a) I_D-V_{GS} curves, (b) V_{GS} measurement includes L_{SS} voltage drop

During turn-on:

$$v_{GS\_on} = v_{GI} + L_{SS}\frac{\Delta I_D}{\Delta t_r} \tag{4-2}$$

During turn-off:

$$v_{GS\_off} = v_{GI} - L_{SS}\frac{\Delta I_D}{\Delta t_f} \tag{4-3}$$

where v_{GS_on} and v_{GS_off} are the measured gate voltages, v_{GI} is the real MOSFET gate voltage, Δt_r and Δt_f are the drain current rise and fall times, and ΔI_D is the switching current. It is assumed here that the drain current changes linearly during the switching transients, and that the gate current slew rate is much smaller than that of the drain current, so that the voltage drop across L_{SS} is solely determined by I_D.

The real gate voltage is hence the weighted average of

$$v_{GI} = \frac{v_{GS\_on}\Delta t_r + v_{GS\_off}\Delta t_f}{\Delta t_r + \Delta t_f} \tag{4-4}$$

Plotting I_D vs. v_{GI} will then give the "real" transfer characteristic.

This method has been verified through Saber simulation. As shown in Figure 4-29 (a), the blue and yellow curves are got from the slow switching waveforms of the preliminary version of the SiC MOSFET model built in this work. The green curve is an averaged curve based on the blue and yellow curves. The red dotted curve in the figure is the "static" transfer characteristic of the MOSFET model at the same V_{DS} voltage, which is obtained from a DC sweep of the model. The close match of the green and red curves proves the effectiveness of this method.

Using the proposed method, the "predicted" transfer characteristics of the SiC MOSFET are obtained experimentally and plotted in Figure 4-30. As seen, the characteristic curves shift to the left as the V_{DS} bias increases, indicating a bigger transconductance under higher drain-source voltage, which is reasonable for power MOSFET in general. In this work, the additional transfer characteristic at 300 V is imported into the *Power MOSFET Tool* to adjust LAMBDA, which turns out to be 0.009 after adjustment (See Figure 4-31). Note that by doing this certain accuracy is sacrificed in the linear and transition region curve fittings. However, as it will be shown later, better fitting in the saturation region of the model will still produce more accurate results in matching the experimental switching waveforms.

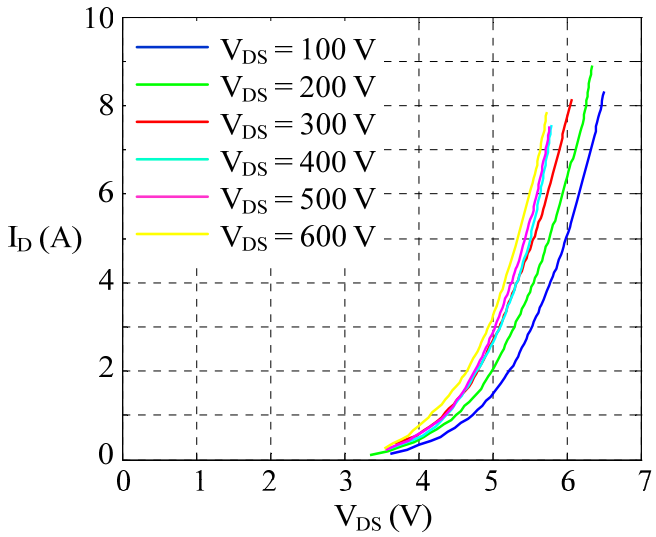


Figure 4-30. Predicted transfer characteristics from slow switching test

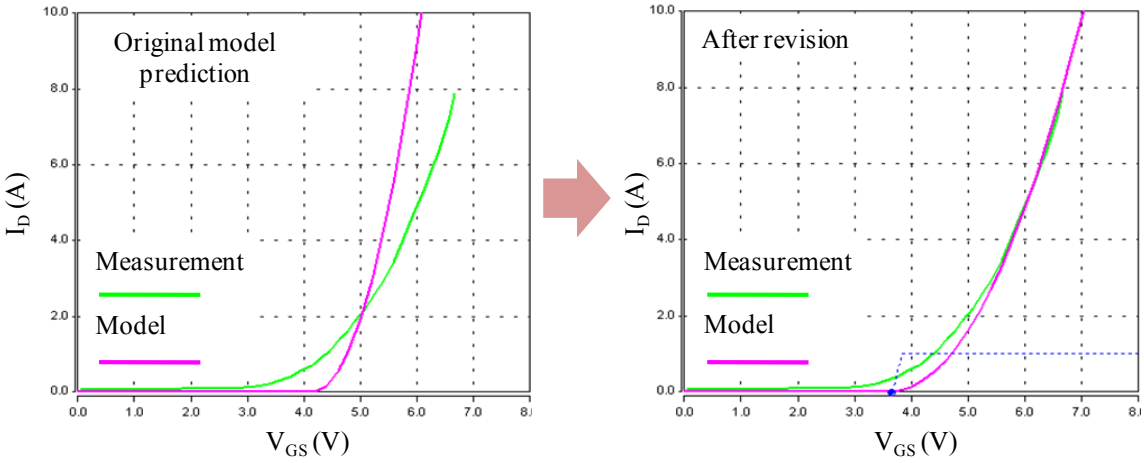


Figure 4-31. Model revision using predicted transfer characteristics. (left) Original model transfer characteristic at V_{DS} = 300 V, (right) revised transfer characteristic at V_{DS} = 300 V

Another important parameter in MOSFET modeling is the Miller capacitance C_{RSS}. It is found from simulation that the MOSFET switching waveforms are extremely sensitive to the characteristic of C_{RSS}, especially in the inductive load, hard switching condition, whereas small changes in C_{ISS} or C_{OSS} do not affect the switching behavior too much. This has also been stated elsewhere but the reason has not been explained explicitly [24]. In principle, C_{RSS} is a capacitor connecting the input (gate) and the output (drain) of the

MOSFET if one regards the device as a two-port network. According to the Miller Effect theory, this capacitor can be decoupled by putting two equivalent capacitors at the input and output ports separately, as shown in Figure 4-32. From the input side, the decoupling capacitance is given by

$$C_{GD\_input} = C_{RSS}(1 - A_v) \tag{4-5}$$

where A_v is the AC amplification coefficient, given by

$$A_v = \frac{dV_{DS}}{dV_{GS}} = \frac{dV_{DS}}{dt} \Big/ \frac{dV_{GS}}{dt} \tag{4-6}$$

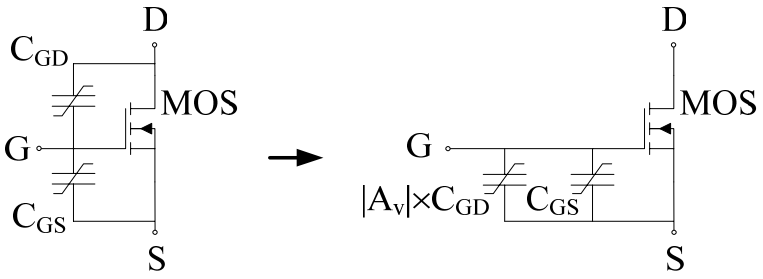


Figure 4-32. Decoupling of the Miller capacitance (Only input capacitances are displayed)

Because V_{GS} and V_{DS} always change in the opposite direction, therefore $A_v < 0$. During the switching transients, when V_{DS} does not change, $A_v = 0$ and the input capacitance is simply C_{ISS}. However, during V_{DS} rising or falling period, V_{GS} is effectively in its "plateau" stage while V_{DS} swings drastically between full bus voltage and nearly zero. This results in an extremely large A_v which significantly magnifies C_{RSS} and makes C_{GD_input} dominate the input capacitance. Any small discrepancy in C_{RSS} will then be exaggerated by A_v, leading to switching waveform mismatch, especially in V_{DS}. As a result, the seemingly perfect C_{RSS} curve fitting does not guarantee an accurate prediction of the switching waveforms, as even several pF changes in C_{RSS} can make a

big difference in C_{GD_input}. In this case, experimental waveforms must be obtained so that the C-V curve of C_{RSS} can be finely adjusted in the model to match the real switching waveforms.

4.5.3 Model Verifications

Figure 4-33 shows the comparisons of experimental and simulation waveforms under 600 V, 8 A inductive load, hard-switching condition with R_G = 10 Ω. This is also the case used to finely adjust C_{RSS}. Both simulation results with and without adopting the transfer characteristic prediction are superimposed to show the difference. As seen from the figure, the model considering the saturation region characteristics simulates the voltage and current slew rates much better than the one only fitting the linear and transition regions.

The model is then used to predict another switching condition where the gate resistance is reduced to 5 Ω, as shown in Figure 4-34. The device model simulates correctly the major characteristics of the switching waveforms, such as V_{DS} and I_D slew rates, I_D and V_{GS} spikes during turn-on, as well as V_{GS} notch during turn-off. However, the simulation is not able to capture the high-frequency ringing in the waveforms because the parasitic components in the tester circuit are not considered in the simulation. These parasitics need to be involved in order to predict more precisely the high-speed switching behavior of SiC MOSFET under the influence of these parasitics. This will be taken care of in Chapter 5.

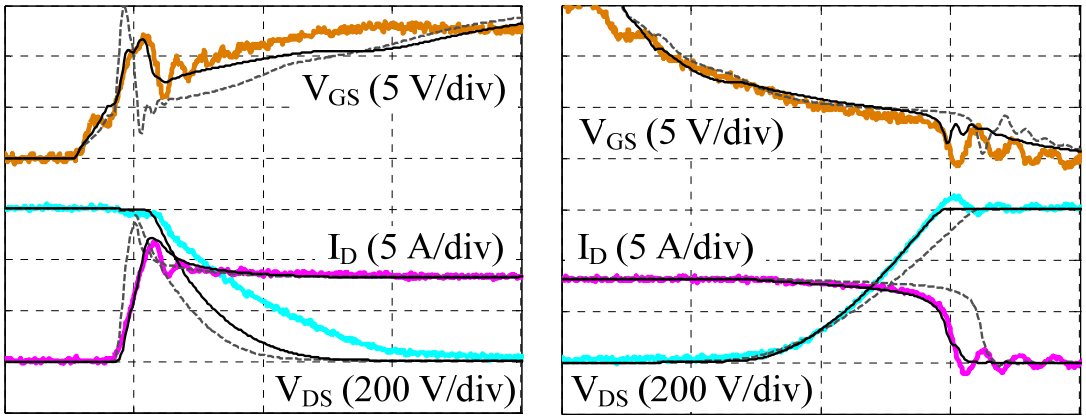


Figure 4-33. Comparisons of experimental (colored) and simulation (black and grey) waveforms under R_G = 10 Ω. (left) Turn-on, (right) turn-off. Time: 40 ns/div. Black – with transfer characteristic prediction; grey dashed – without transfer characteristic prediction

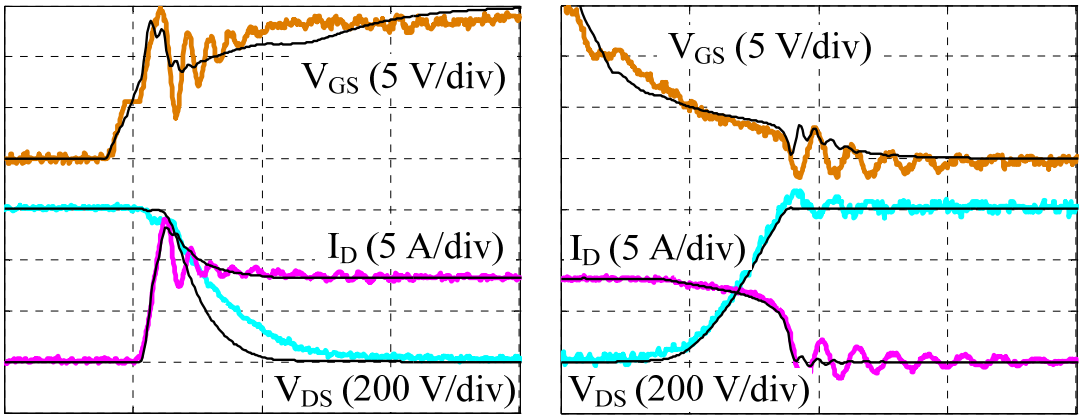


Figure 4-34. Comparisons of experimental (colored) and simulation (black) waveforms under R_G = 5 Ω. (left) Turn-on, (right) turn-off. Time: 40 ns/div

The only discrepancies observed in the above figures are the V_{GS} and V_{DS} waveform mismatches during the turn-on process. As seen, the simulated V_{GS} seems to have a shorter "plateau" period, thus leading to a faster V_{DS} falling rate. Looking back at the MOSFET modeling process, one can find that only one transfer characteristic curve is allowed to be imported and fitted in the MOSFET modeling tool, limited by the program function, which means the saturation region can only be partially fitted. Besides, the Si MOSFET model still has difficulties in fitting perfectly both the linear and saturation

regions, and both the low-current and high-current regions of the SiC MOSFET I-V characteristics at the same time.

Another possible cause for the discrepancies is that the gate structure of the MOSFET is simplified as a single internal gate resistance in the model, whereas a more accurate circuit for the fast switching condition would be an R-C ladder, as multiple resonant peaks can be observed beyond 50 MHz in Figure 4-9. This is another limitation of this SiC MOSFET model.

4.6 Conclusions

This chapter has presented the full static and switching characterizations of a 1.2 kV, 20 A prototype SiC MOSFET. The static characterization results show the SiC device's superiority in blocking higher voltage while still keeping a very low $R_{DS(ON)}$ even under much higher junction temperature compared to Si technology. The characterization process is also generic so that it can be applied to studying any new MOSFET. Several explanations have been introduced for the possible cause of the device degradation observed after the switching tests.

The characterization data are then used to build a SiC MOSFET model using the Si power MOSFET modeling tool. Discussions have been made on the most critical factors in the modeling process – the saturation region characteristics and the Miller capacitance – in order to accurately predict the MOSFET switching behavior. A technique has also been proposed to obtain saturation region characteristics from switching waveforms. The developed model successfully simulates the real switching behavior of the device, although some discrepancies are also observed and explained. The discussions presented

in this chapter are applicable to the general MOSFET modeling procedures, and are helpful for developing and building future models for SiC MOSFETs.

4.7 References

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Chapter 5 Modeling and Simulation of SiC MOSFET Fast Switching Behavior under Circuit Parasitics

5.1 Introduction

The demands of modern power electronics converters for high density and high efficiency require that the power semiconductor devices have minimized conduction loss and switching loss, which means they should have very small on-state voltage and resistance, and can be switched as fast as possible. However, the problem accompanying the faster switching speed is the more severe high-frequency ringing during the switching transients, due to the existence of the circuit parasitic impedances. The parasitic ringing deteriorates the electromagnetic interference (EMI) and device stress, which ultimately offsets the benefits of reduced switching loss from faster switching speed.

Designers usually need to be very careful in designing the layouts for these high-speed switching circuits, trying to minimize the circuit parasitics and the side effects brought by these parasitics, even though it is impossible to make them totally zero. The problem of the current practice is that the effects of the circuit parasitics can be observed only after the circuit (say a printed circuit board (PCB) or a power electronics module) is manufactured and tested, because it is very hard to estimate their values and impacts on the device switching waveforms beforehand. If the circuit performance does not meet the

requirement, the entire design process has to be repeated to get a refined circuit, which is usually quite costly and time-consuming.

For this reason, it is preferable to simulate the device switching behavior under the influence of circuit parasitics before realizing the circuit physically. This is especially helpful in the design of high-speed switching circuits, where designers can adjust their circuit layouts or compare different layout options based on the simulation results. Another advantage with the simulation method is that, as long as the simulation is accurate enough in predicting the real waveforms, measurement components and test points can be saved in the hardware to make the design more compact. Moreover, quantities that are hard to measure physically in the circuit can also be observed in simulation without any difficulty, such as the current distributions between multiple dice in a power module.

To this end, this chapter explores a modeling methodology to predict the silicon carbide (SiC) MOSFET fast switching behavior under the influence of circuit parasitics. The MOSFET double-pulse tester presented in previous chapters has been used again as the case study in this work. The major components of the tester, including the passive components (inductor and capacitors), SiC Schottky diode, gate drive integrated circuit (IC), as well as the PCB parasitics, have all been modeled. These models are then combined with the SiC MOSFET model in a circuit simulator to predict the device switching waveforms. Finally, simulation results are compared with the experiments to verify the effectiveness of this modeling methodology.

5.2 Modeling of Surrounding Circuit Components

The surrounding circuit components in the double-pulse tester include the freewheeling diode, load inductor, gate drive IC, PCB package, as well as other passive components like the DC bus capacitors and gate drive power supply capacitors. These components also play very important roles in determining the fast switching behavior of the main switch, so it is necessary to consider all of them in the simulation in order to predict the real switching waveforms with detailed spikes and ringing. The following sections discuss the modeling of these components.

5.2.1 The Load Inductor

The load inductor used in the double-pulse tester is composed of 4 small inductors connected in series, achieving a total inductance of 672 μH. The considerations of the inductor design are (1) to have a very low equivalent parallel capacitance (EPC) so that the MOSFET turn-on current spike can be minimized, and (2) to have a high enough saturation current level so that the device can be tested up to the desired current without saturating the inductor.

Figure 5-1 shows the measured impedance of the final inductor versus frequency, from which an EPC of only 1 pF can be observed.

The inductor is modeled by including an ESR, an EPC, as well as an EPR together with the main inductance, as shown in Figure 5-2. By curve fitting the measured impedance, the parameters of the inductor model are extracted to be L = 672 μH, ESR = 0.11 Ω, EPC = 1 pF, and EPR = 69 kΩ. The Bode plot of the model is also shown in Figure 5-1 as the red dashed curves, where a good agreement is achieved up to 2 MHz for

this model. Above that frequency, the parasitic components from interconnections of the inductor become effective, and modeling of that part is not necessary in this work.

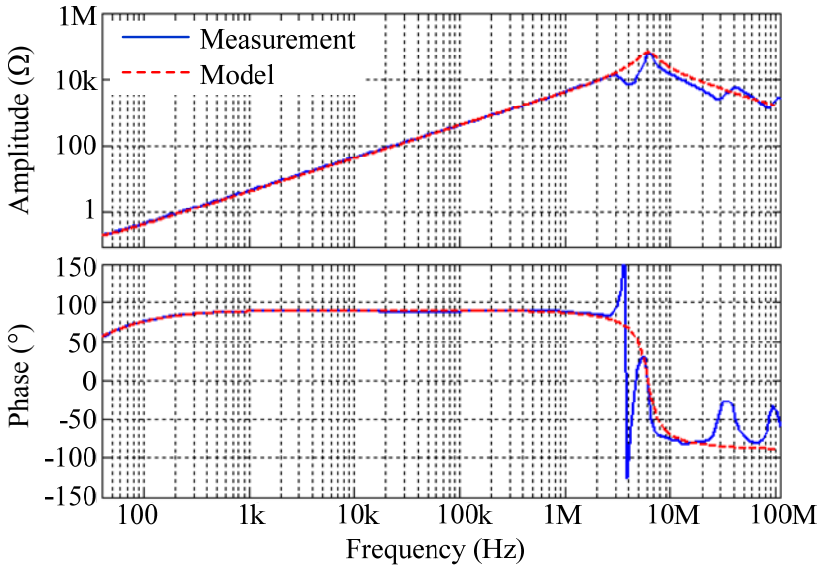


Figure 5-1. Load inductor measurement vs. model

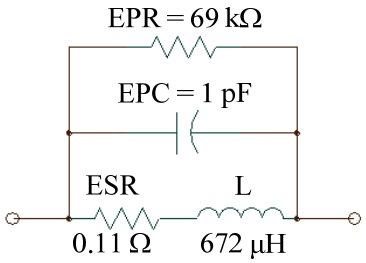


Figure 5-2. Inductor equivalent circuit

5.2.2 The Freewheeling Diode

The freewheeling diode is a 1.2 kV, 20 A SiC Schottky barrier diode (SBD) prototype from Infineon. The forward I-V curve of the diode is measured using the Tektronix 371B curve tracer, and the junction capacitance-voltage characteristic is obtained from the Agilent 4294A impedance analyzer using a similar method as introduced in Chapter 4. The diode model is then built using Saber *Power Diode Tool* [1]. Similar to Saber *Power*

MOSFET Tool, the static and capacitance characteristics of the diode model are tuned visually to match the imported measurement data [2]. Figure 5-3 shows the graphic user interface of the diode modeling tool and the model structure. The ideal diode and series resistance R_S represent the forward I-V characteristic of the device, C_J represents the junction capacitance, and Q_{rr} represents the reverse recovery characteristic. The curve fitting results are shown in Figure 5-4, from which a good agreement can be seen between the measurement and the model. It needs to be noted that the diode used is of Schottky type, whereas the program generates models for PiN diodes. Therefore to adapt the model for the SBD, the reverse recovery effect of the diode model is set to minimum, as seen in Figure 5-4 (c).

The stray inductance from the device's TO-220 package has also been measured and modeled as a 7 nH inductance in series with the diode model.

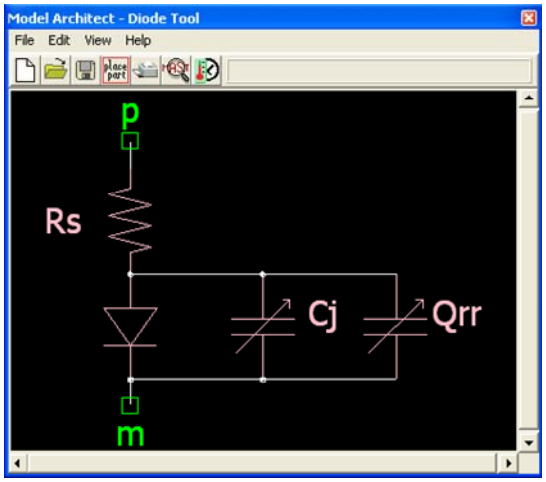


Figure 5-3. Saber *Power Diode Tool* graphic user interface

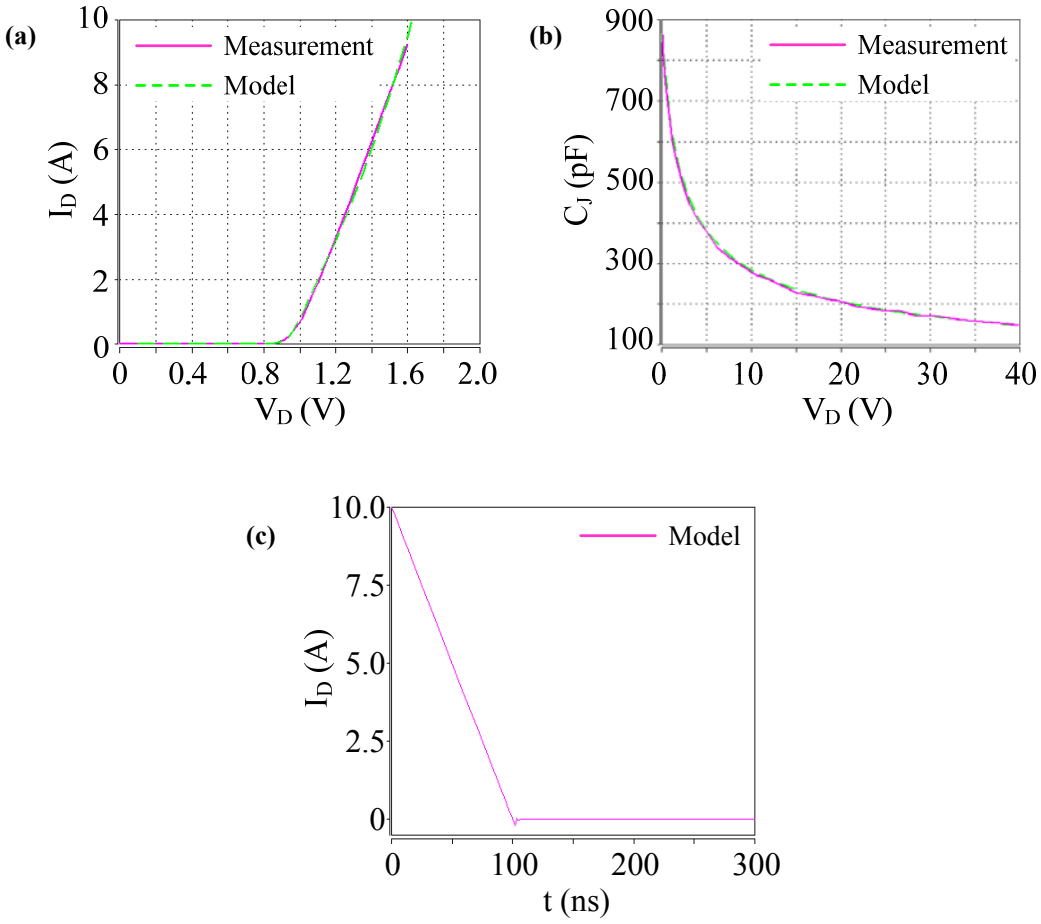


Figure 5-4. Diode model curve fitting results.
(a) Forward I-V curve, (b) junction capacitance-voltage curve, (c) reverse recovery characteristic

5.2.3 The Gate Drive IC

The gate drive IC used in the tester is IXYS IXDD414. The SPICE model of this chip can be downloaded from the manufacturer's website. Figure 5-5 shows the equivalent circuit of the SPICE model. This model, however, is quite complicated and cannot be translated into Saber template directly, so a simplified Saber model is built based on the SPICE model, as shown in Figure 5-6. Fortunately, the output totem-pole structure of the original model uses only conventional SPICE MOSFET models with all the parameters given, and therefore can be easily rebuilt in the Saber model. The digital logic portion of

the SPICE model is just simplified as a NAND gate with certain propagation delay, as seen in Figure 5-6.

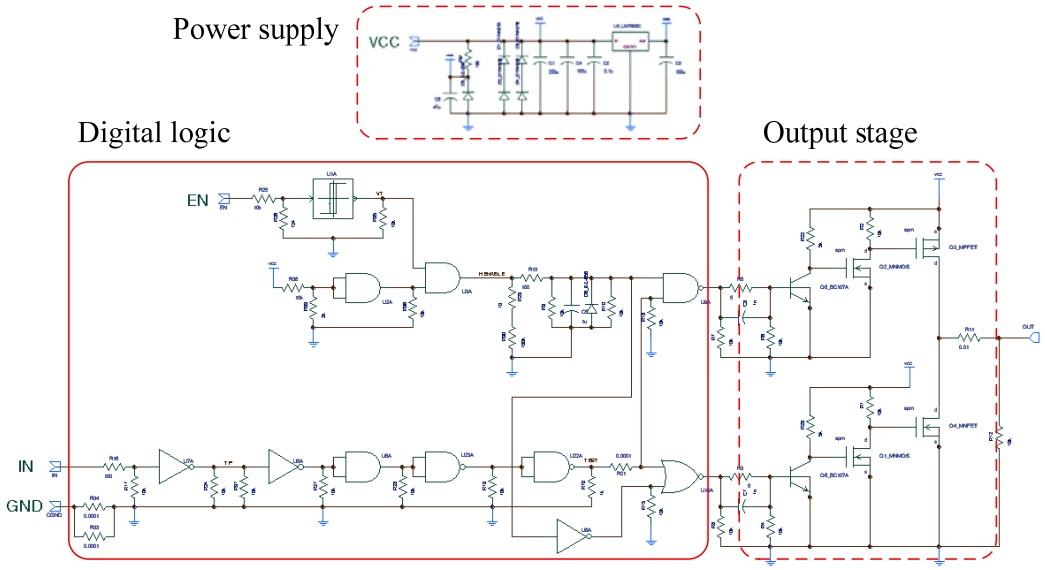


Figure 5-5. Equivalent circuit of original IXDD414 SPICE model

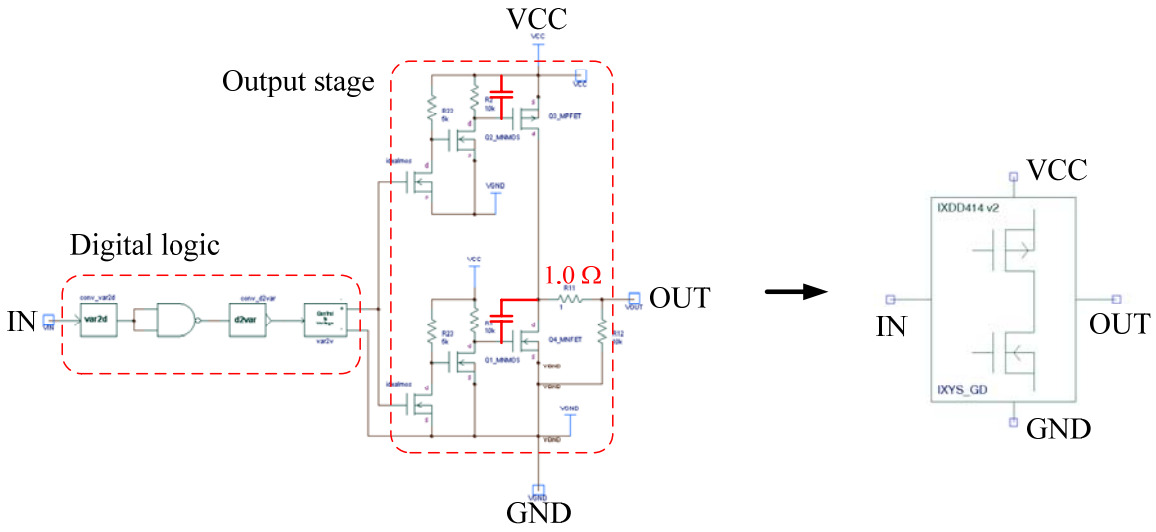


Figure 5-6. Simplified Saber model of the gate drive IC

The Saber model with the original parameters, however, does not match the IC datasheet, as this model switches 2 nF capacitive load within 1 ns, while in the datasheet

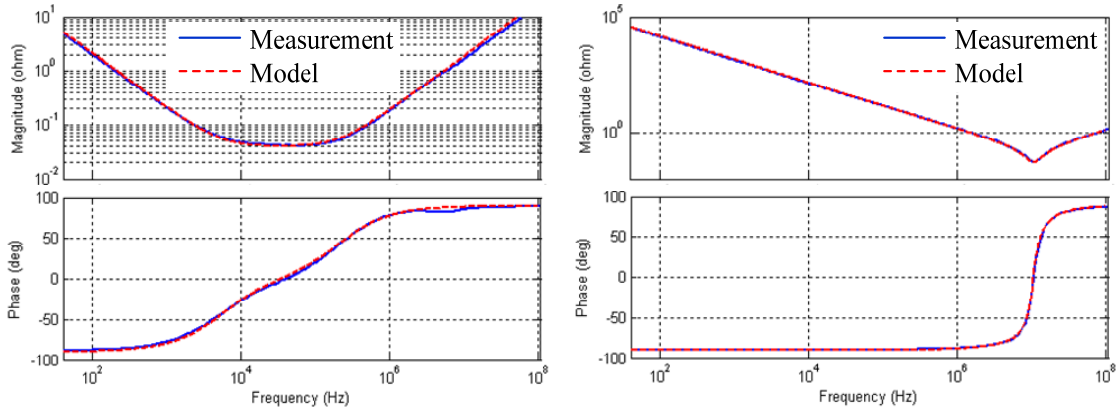
the rise time and fall time are around 10 ns. To adjust the rise and fall times of the model, two small capacitances (red in Figure 5-6) are added to the top PMOS and bottom NMOS respectively, both of which are smaller than 1 pF. The output resistance of the model is also adjusted to be 1 Ω according to the datasheet to get the correct the rise and fall times.

5.2.4 The Capacitors

The capacitors used in the double-pulse tester, namely the DC bus bulk and decoupling capacitors, as well as the gate drive power supply capacitors, are also measured and modeled. The parasitic ESRs and ESLs are taken into consideration in the capacitor modeling, as shown in Figure 5-7. These parameters are important as they, especially ESLs, affect the high-frequency ringing during the fast switching transients.

The ESRs and ESLs can be extracted using the curve fitting method, and two examples of the capacitor models are displayed in Figure 5-8. A full list of the capacitor models is also given in Table 5-1.

Figure 5-7. Capacitor model equivalent circuit



(a) **(b)**

Figure 5-8. Capacitor model examples.
(a) 820 µF DC bus bulk cap, (b) 100 nF gate drive power supply cap

Table 5-1. Capacitor model parameters

Capacitor	Capacitance (F)	ESL (nH)	ESR (Ω)
DC bus bulk and decoupling capacitances			
820 µF	750µ	30	0.04
300 nF	300n	15	0.019
120 nF	120n	9	0.027
100 nF	100n	4.5	0.08
Gate drive power supply capacitances			
470 µF	450µ	4	0.15
10 µF	10µ	4	1
100 nF	110n	2	0.05

5.2.5 The Coaxial Shunt Resistor

In the double-pulse tester the coaxial shunt resistor is selected over other current sensors to measure the MOSFET drain current because of its significantly higher bandwidth [3]. This work uses a 0.1 Ω shunt resistor (SSDN-10) manufactured by T&M Research, whose appearance and equivalent circuit are illustrated in Figure 5-9. This

shunt resistor claims an equivalent bandwidth over 1 GHz [3-5]. However, when measuring the impedance of the resistor from A port (See Figure 5-9), a 2.2 nH series inductance can be observed from the Agilent 4294A impedance analyzer. Based on the following equation

$$f = \frac{1}{2\pi}\frac{R}{L}, \tag{5-1}$$

this corresponds to a corner frequency of only 7.2 MHz, which is obviously too low for the shunt resistor. On the other hand, when measuring from B port, a 5 nH series inductance can still be observed. Including 2 nH in series with the shunt resistance would greatly increase the aberration in the measurement of fast changing current, which seems to contradict the manufacturer's specification on the bandwidth. This seeming contradiction can be explained by looking at the internal structure of the shunt resistor.

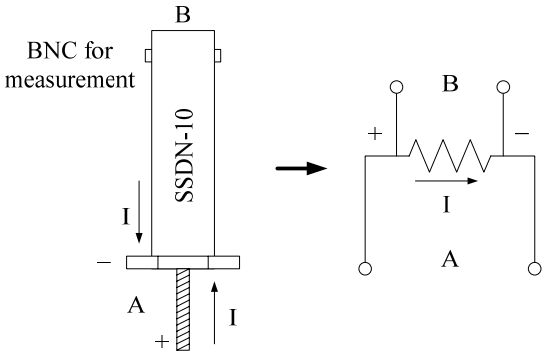


Figure 5-9. Coaxial shunt resistor (left) and equivalent circuit (right)

Shown in Figure 5-10 (left) is the internal structure of the coaxial shunt resistor. The principle of this device is that the current flowing through the inner and outer resistance tubes creates a zero magnetic field region within the shunt resistor. Therefore, wires can be extended in this region for measurement (B port) without any induced voltage due to the fast changing current, which guarantees the accuracy in the measurement [5].

However, the main current, seen as the red arrows in the figure, still forms a big loop within the resistor which causes the 2.2 nH measured from the impedance analyzer. But notice that the real resistance for measurement is made up of the inner and outer resistance tubes which are only a small part of the current loop. This part thus produces a parasitic inductance much smaller than 2.2 nH. Furthermore, although the twisted pair to B-port is not inducing any voltage from the main current loop, it still causes around 5 nH parasitic inductance itself. It is just that this inductance is in series with the measurement probe with much higher impedance, and thus will not cause big aberration in the measurement.

Based on the above analyses, the equivalent circuit of the coaxial shunt resistor is shown on the right hand side of Figure 5-10. In a word, the 2.2 nH is indeed in series with the resistance, however its voltage drop will not be included by the measurement port.

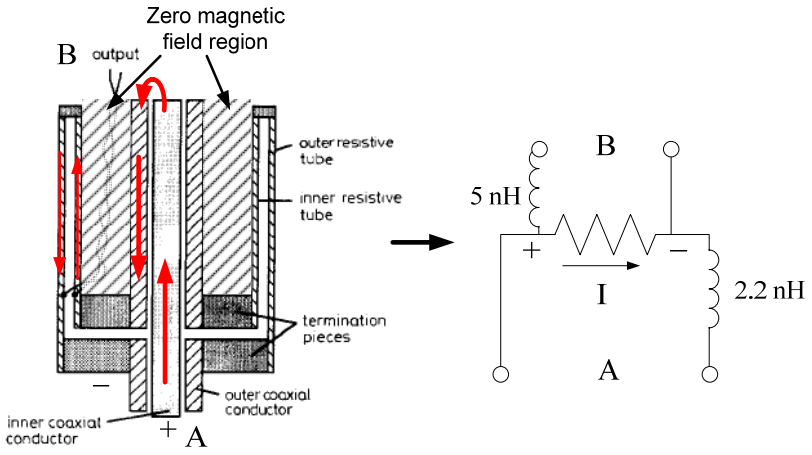


Figure 5-10. Coaxial shunt resistor internal structure (left) and model (right) [5]

5.2.6 The PCB Parasitics

Many preceding works have conducted the evaluations and analyses of circuit parasitics in converters and their impacts on the device switching characteristics.

Basically these works can be divided into two major categories in terms of study method. One is the measurement-based method, which evaluates the parasitic impedances of the existent PCB or power module through physical measurement, such as [6-8]. These works used either time domain reflectometry (TDR) method or the impedance analyzer to evaluate the circuit parasitics. This method, however, is complicated and time consuming, and only applies to some simple circuits where the parasitic inductances and capacitances can be clearly defined and identified. For more complex power modules or printed circuit boards, measuring the parasitics becomes unpractical because for so many erratically separated interconnects it is even hard to identify the parasitic impedances, not to mention measuring them and applying the measurement results in future simulation to investigate their effects. Furthermore, some quantities are very difficult to measure even in simple circuits, such as tiny small inductances and mutual inductances. All of these factors confine the use of this measurement-based method to a very narrow scope.

Another method adopted by many works is the simulation-based method, which extracts the package parasitics using finite element analysis (FEA) or partial element equivalent circuit (PEEC) methods. Electromagnetic (EM) analysis software such as INCA and Ansoft Q3D have been used in these works for the parasitics extraction [9-12]. Using the FEA method, any arbitrary interconnect geometry can be analyzed numerically as long as they can be modeled in the software. The separated interconnects without physically measurable inductance can also be evaluated based on the well-established concept of partial inductance, and the mutual terms can be taken care of automatically as well [13-15]. Furthermore, some EM analysis software also provide interfaces for

commonly-used circuit simulators such that the evaluation results can be directly used in circuit simulations to see the impacts of the parasitics.

For the reasons stated above, this work adopts the simulation-based method to evaluate the PCB parastics of the double-pulse tester. The software used in this work is Ansoft Quick 3D Extractor, which is used not only because of its availability in the lab, but also because of its modeling capability of arbitrary 3-dimentional geometries and accurate calculations of RLC parasitic parameters [16-17]. The modeling process of the PCB is illustrated in Figure 5-11. The main steps are:

(A) Designing the PCB layout

The original PCB layout is designed in Altium Designer – commonly-used PCB design software.

(B) Exporting the geometry model

Altium Designer supports exporting the PCB layout in different 3D geometry model formats, such as AutoCAD drawing format and STEP (Standard for the Exchange of Product model data) format. In this work, AutoCAD is selected just for simplicity.

(C) Building Q3D model

The geometry model obtained in (B) is then imported into Q3D. In this work four layers of copper traces are obtained after import, as seen in Figure 5-11 (C). Material properties are then assigned to different structures (copper for traces and FR4 epoxy for insulators) in Q3D because the original geometry model does not carry any material information. Also for simplicity some geometric details are removed, such as vias, through-holes and round corners. Interconnects for the digital circuits are also removed. Only the gate drive and power stage interconnects are modeled finally.

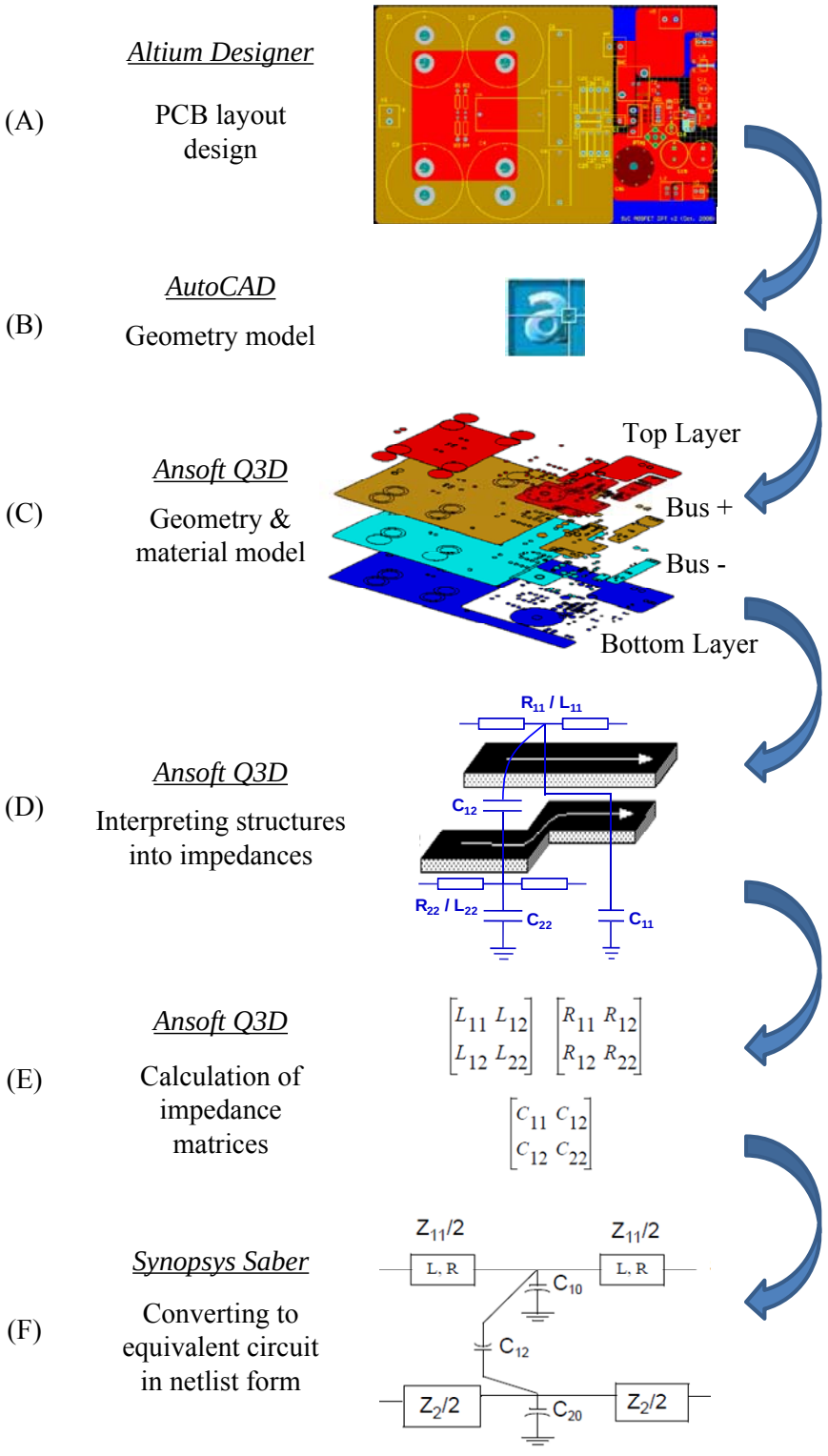


Figure 5-11. PCB modeling procedure

(D) Interpreting structures into impedances

After assigning electrical excitations to different copper traces, Q3D analyzes the structural parasitics and calculates the corresponding self and mutual impedances. The detailed calculation method and process can be found in [15].

(E) Calculation of impedance matrices

Q3D presents the results in forms of resistance, inductance, and capacitance matrices after the analysis.

(F) Converting to Saber equivalent circuit

The impedance matrices are then exported in netlist form and converted to Saber template for the subsequent circuit simulation. Details about this step can be found in Appendix B.

5.3 Device-Package Combined Simulation

5.3.1 Simulation vs. Experiment

All of the above models are then combined together in Saber to simulate the switching waveforms of the SiC MOSFET under circuit parasitics. Figure 5-12 shows the device-package combined simulation circuit in Saber. The circuit includes the SiC MOSFET and SiC Schottky diode models with their respective package parasitics, gate drive IC model, PCB model, as well as passive component models with the corresponding ESR/EPC or ESR/ESL. The operation condition of the simulation circuit, namely the DC bus voltage and the pulse widths of the double-pulse signal, are exactly the same as what are used in the experiments.

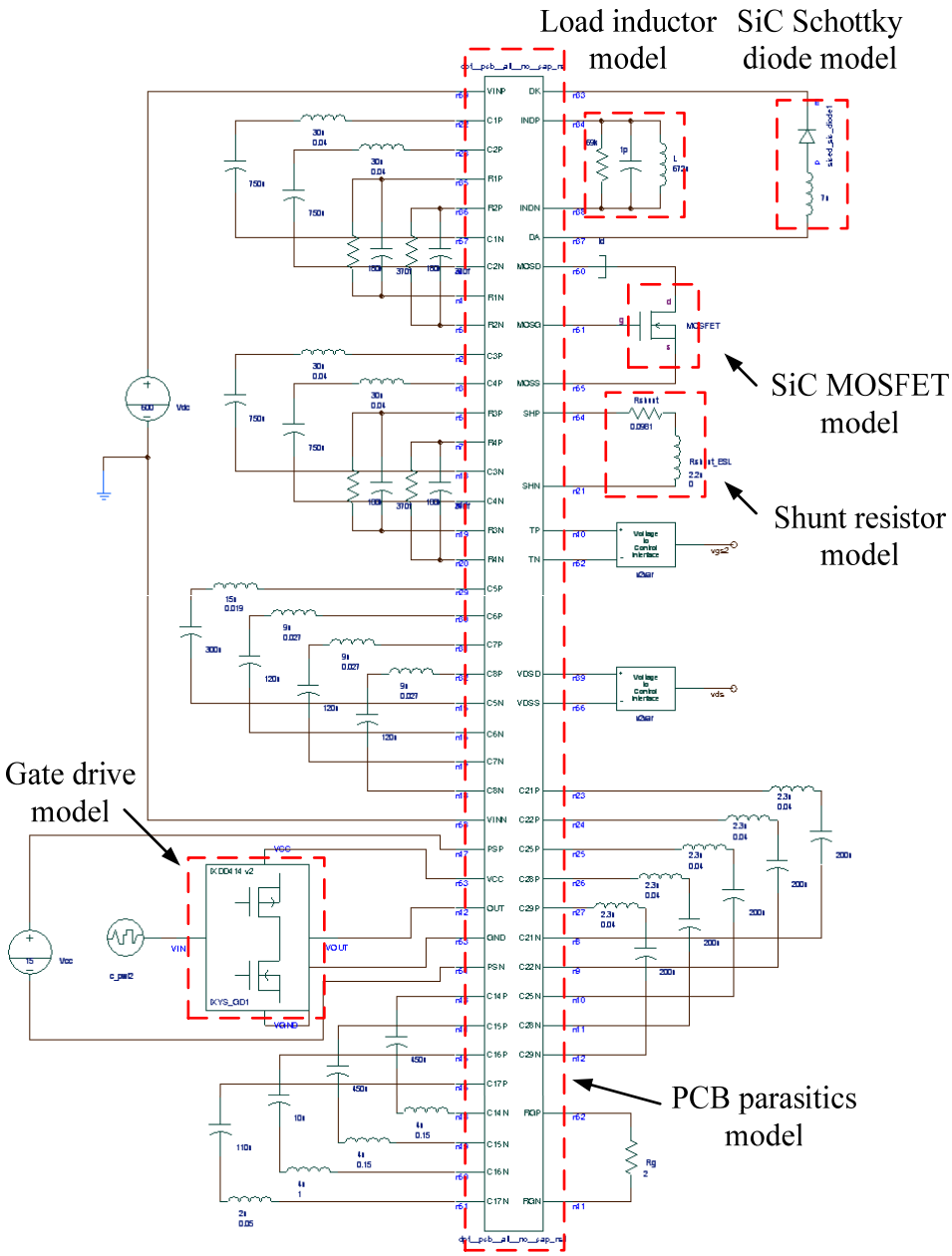


Figure 5-12. Saber circuit of device-package combined simulation

Figure 5-13 shows the waveform comparison between experiment and simulation under 600 V, 8 A switching condition with 5 Ω gate resistance. As seen from the figure, the simulation waveforms resemble the experimental ones very well, with the correct prediction of the parasitic ringing in the drain current I_D waveform, and the overshoot in

the drain-source voltage V_{DS} waveform. What does not match the experiment most is the gate drive output voltage V_{DRIVE} due to the model problem. However, the currently used gate drive model is still kept in the simulation since it is essentially manufacturer's model. On the other hand, the I_D spike in the simulation is slightly higher than the experiment and the settling time is longer, as seen in Figure 5-13 (a). This is probably due to the modeling of the parasitic resistance and the freewheeling diode, which will be discussed in detail later.

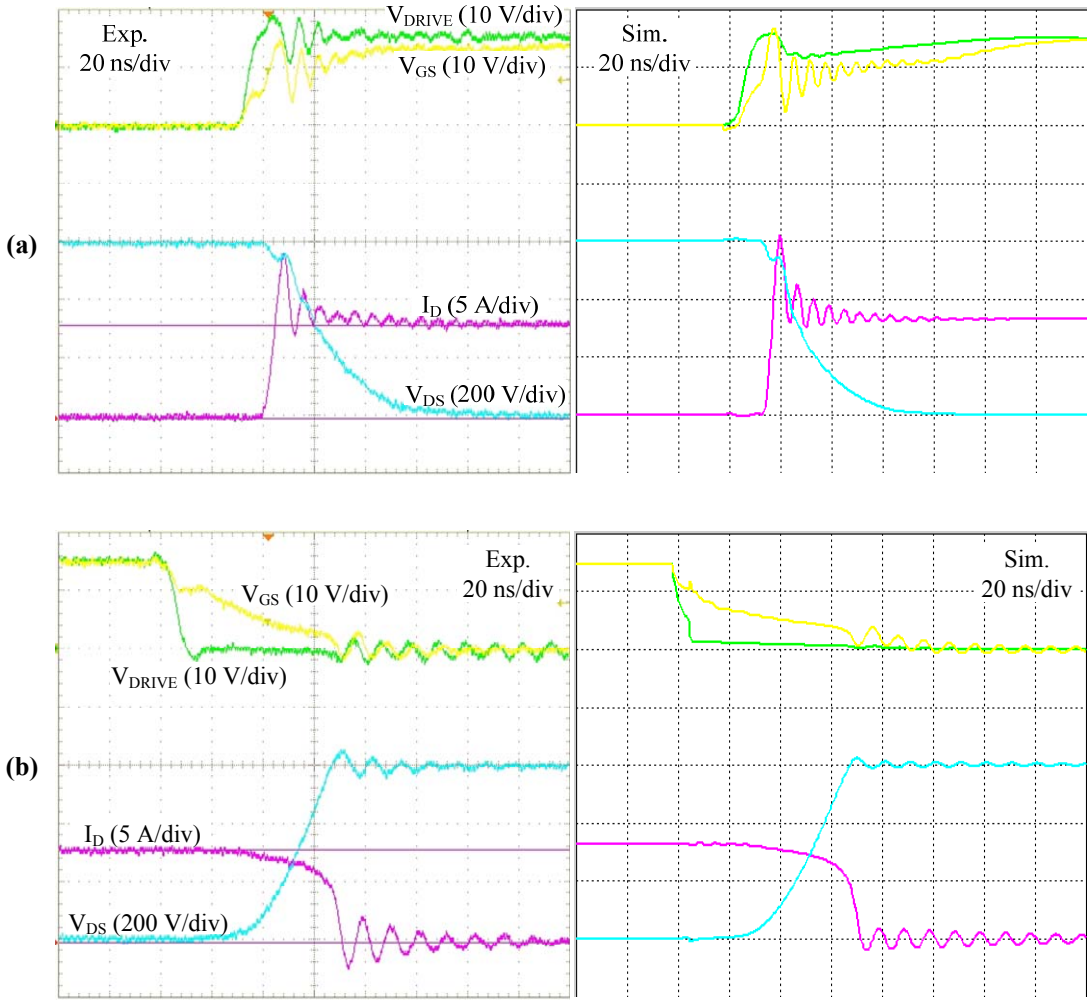


Figure 5-13. Comparison of experimental (left) and simulation (right) waveforms: 600 V, 8 A, R_G = 5 Ω. (a) Turn-on transients, (b) turn-off transients

The above analyses also apply to Figure 5-14, where the SiC MOSFET is switched under 600 V, 4 A with 2 Ω gate resistance. As one can see, in this case the simulation again captures correctly the more severe parasitic ringing with increased switching speed, especially in I_D waveform.

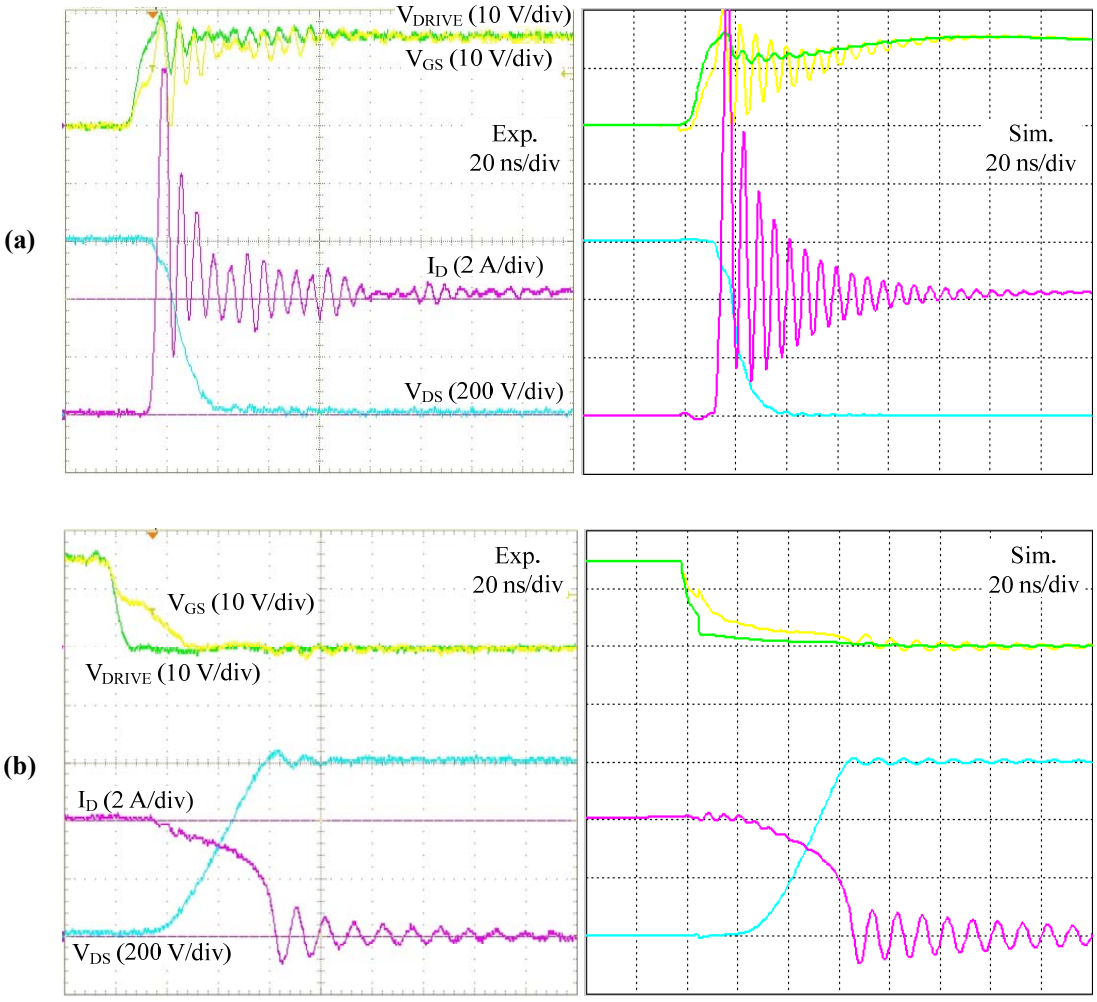


Figure 5-14. Comparison of experimental (left) and simulation (right) waveforms: 600 V, 4 A, R_G = 2 Ω. (a) Turn-on transients, (b) turn-off transients

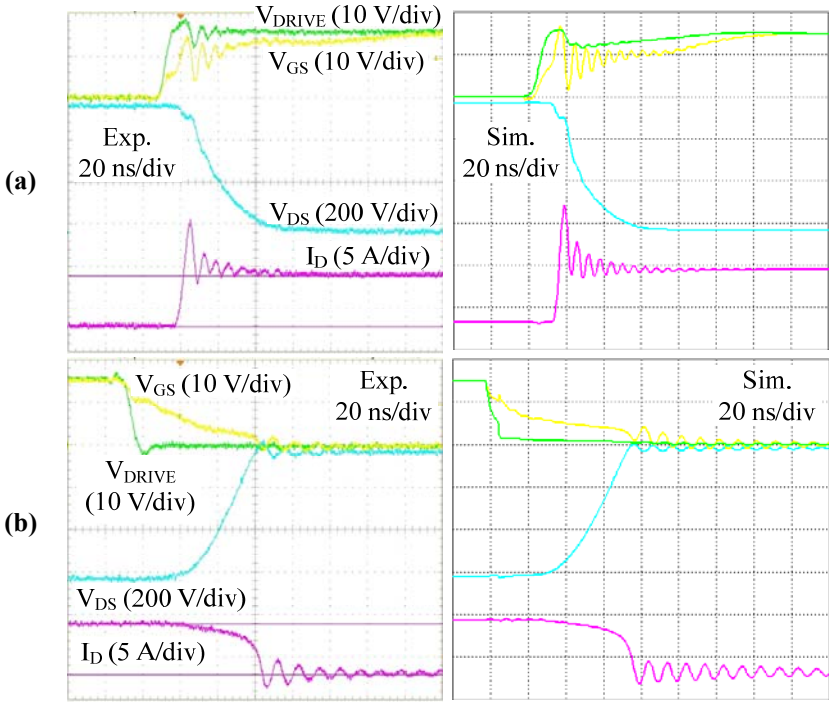


Figure 5-15. Comparison of experimental (left) and simulation (right) waveforms: 600 V, 6 A, R_G = 5 Ω. (a) Turn-on transients, (b) turn-off transients

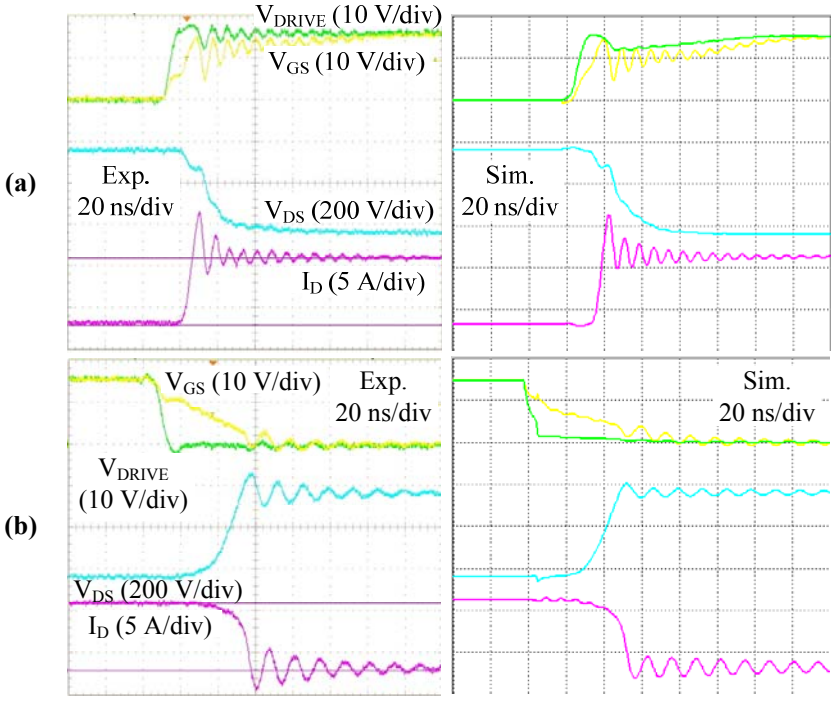


Figure 5-16. Comparison of experimental (left) and simulation (right) waveforms: 200 V, 8 A, R_G = 5 Ω. (a) Turn-on transients, (b) turn-off transients

To verify the simulation, two other conditions with different load current and bus voltage have also been simulated and compared to the experiments. Figure 5-15 shows the switching waveforms under 600 V, 6 A with R_G = 5 Ω, while Figure 5-16 displays the condition of 200 V, 8 A with R_G = 5 Ω. As seen, in both cases the simulation predicts the MOSFET switching behavior very well, validating the effectiveness of this modeling methodology.

As a comparison, now look back at Figure 4-33 and 4-34, where the simulation does not consider any parasitics coming from the circuit. It is very clear in these figures that all the details about the parasitic ringing are lost in the fast switching transients. This again emphasizes the importance of the circuit parasitics in the modeling process so as to study their impacts on the SiC MOSFET switching behavior from simulation.

5.3.2 Quantification of Simulation Results

To evaluate the accuracy of the simulation, the simulated waveforms have also been quantified and compared to the experiments in terms of the switching energy, voltage and current overshoots, as well as parasitic ringing frequency. Shown in Figure 5-17 is the switching energy comparison where the energies during turn-on and turn-off are plotted against different load current for V_{DS} = 600 V and R_G = 5 Ω condition. As seen, the simulated turn-off energy predicts the real E_{off} quite well, whereas the turn-on energy is smaller in the simulation compared to the experiment. This discrepancy is due to the faster turn-on V_{DS} slew rate in the simulation because of the MOSFET model problem, which has already been discussed in Chapter 4. In another word, the accuracy of the switching energy is to a great extent related to the accuracy of the device models instead

of the circuit parasitics. As long as a better SiC MOSFET is available, the prediction of the switching energy can be improved.

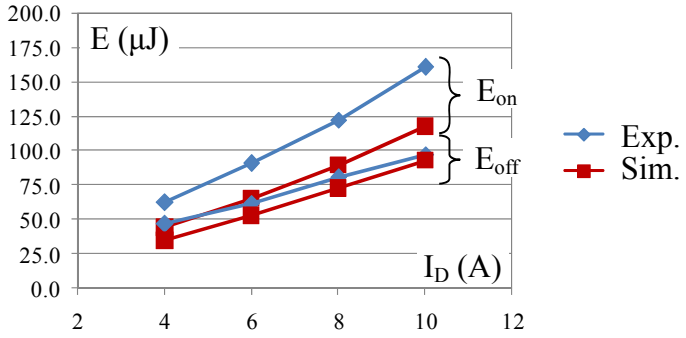


Figure 5-17. Switching energy comparison between experiment and simulation. Test condition: 600 V, R_G = 5 Ω

Figure 5-18 compares the drain current I_D and drain-source voltage V_{DS} overshoots between simulation and experiment. The current overshoot is predicted very well by the simulation, except that a positive systematic error can be inferred from the figure due to the accuracy of the freewheeling diode model. As discussed in Section 5.2.2, the SBD used in the tester is modeled by a PiN diode model, whose intrinsic reverse recovery characteristic, though has already been set to a very small value, cannot be totally set to zero. This results in a relatively higher reverse recovery current under fast switching transients (i.e. high di/dt), and accounts for the consequent systematic error observed in the figure. Moreover, the I_D overshoot, as discussed in Chapter 2, is mainly contributed by the charging current of the SBD junction capacitance, and is almost the same for different load current because V_{DS} keeps unchanged, and so does its dv/dt. The descending trend of the overshoot percentage is simply because the load current is increasing.

The prediction of V_{DS} overshoot is still good, though it is not as precise as that of I_D. The simulation predicts less V_{DS} peak voltage by 5 to 8 percent compared to the experiment. It can thus be inferred that the models previously obtained underestimate the parasitic inductance from either the device packages or the PCB within the main switching loop.

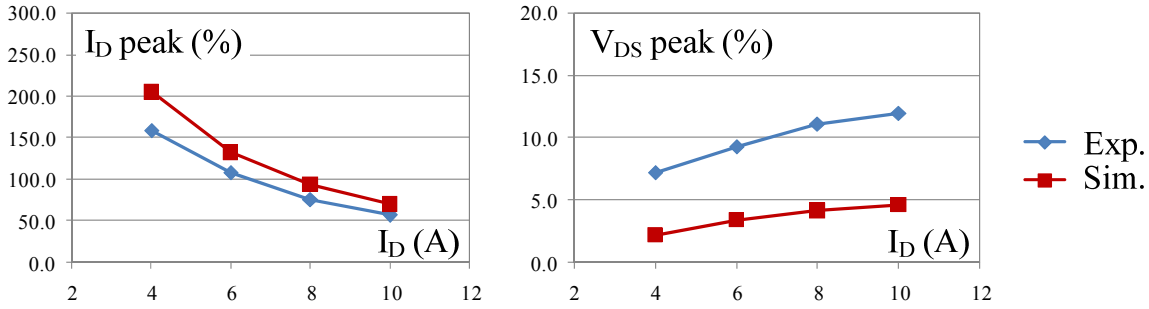


Figure 5-18. Turn-on current overshoot (left) and turn-off voltage overshoot (right) comparisons. Test condition: 600 V, R_G = 5 Ω

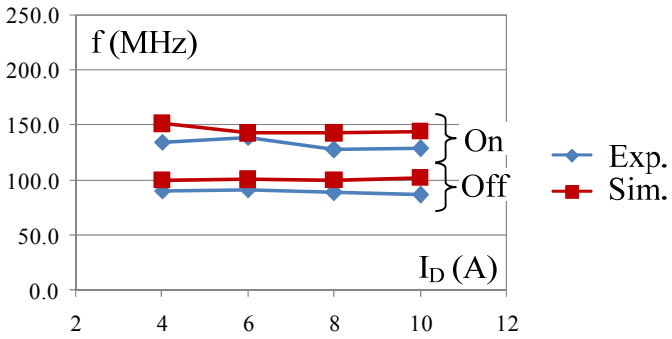


Figure 5-19. Ringing frequency comparisons between experiment and simulation. Test condition: 600 V, R_G = 5 Ω

Figure 5-19, on the other hand, compares the experimental and simulated ringing frequency of I_D during both turn-on and turn-off processes, where a good agreement can be seen between the two. Note that here the "ringing frequency" is measured from the first ringing period of I_D waveforms, since the device junction capacitances change

during the switching transients and hence the ringing frequency. Also notice that the ringing is faster during turn-on than turn-off because the switching loop parasitic inductance resonates with different capacitances during the two transients. This will be discussed in detail in Chapter 6.

5.4 Conclusions and Discussions

This chapter presents the modeling of the surrounding components in the double-pulse tester and the simulation combining both device and package models. The modeling methodology has been proven effective in predicting the fast switching behavior of the SiC MOSFET under the influence of circuit parasitics. This methodology would be a very useful tool for the engineers to design and verify high-speed switching circuit layout before manufacturing and testing the hardware, saving great amount of time and effort in the development of this kind of circuits.

Nevertheless, there are still quite a few drawbacks with this modeling and simulation method. First of all, in order to capture the high-frequency switching characteristics, the circuit needs to be modeled in as much detail as possible. The parasitic impedances coming from both the components and the PCB need to be considered during the modeling process. It can be imagined that when the circuit complexity increases, the modeling itself would be quite a burden, and so would be the subsequent simulation. This practically constrains the applicability of this modeling method to relatively simple circuits.

Secondly, some simplifications in the modeling process prevent the simulation from precisely predicting the experimental waveforms. For example, the parasitic resistances extracted from Q3D are frequency-independent, and in this case are simply modeled as

DC resistances. For the high-frequency ringing current, the effective resistances actually become bigger due to the skin effect, and thus would damp the ringing faster. Besides resistances, the parasitic inductances are also affected by the frequency. However, it is commonly known that the frequency-dependent impedance is hard to be modeled and implemented in time-domain simulation. Even if it is doable, taking this effect into account would further increase the complexity of the modeling and simulation.

Lastly, the PCB modeling treats the parasitics as a network which contains hundreds and thousands of small self and mutual impedances representing each trace on the board. Therefore, it is hard to tell from so many impedances the most important ones that would shape the switching behavior of the MOSFET. It is also difficult to conclude a rule of thumb about how to optimize the circuit layout by just looking at this huge impedance network. For this reason, it is necessary to identify several impedances to be "the most critical" ones and study their effects individually. The identification and study of these impedances will be the topic of the next chapter.

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Chapter 6 Parametric Study of the Parasitic Impedance Influence on MOSET Switching Behavior

6.1 Introduction

It has been shown in Chapter 4 and 5 that in high-speed switching circuits, the parasitic inductances become a significant factor that can cause severe ringing in the switching waveforms. Due to the existence of these parasitics, faster switching speed always comes with the penalties of worsened device stresses and electromagnetic interference (EMI), which can easily overwhelm the benefits of the lower switching loss. Therefore, great care needs to be taken when designing the layout for this kind of high-speed circuits. Chapter 5 has exhibited the detailed modeling of the double-pulse tester which successfully reproduces the real switching waveforms. However the modeling tool is still unable to provide the designers with a general guideline about what should be optimized in the circuit to reduce the parasitic ringing and maximize the benefits of higher switching speed. To achieve this goal, it is very important to understand the influence of different parasitic impedances on the MOSFET switching behavior.

There have been a lot of preceding efforts on the study of circuit parasitic inductances. Some of them have focused on the extraction and modeling of these parasitic parameters so as to capture their effect from circuit simulations [1-6]. In these, the parasitic

inductances have been directly measured on existent circuits or power modules, or calculated using theoretical or finite element analysis. However, the above pieces of work usually treated the parasitic components as an inductive network and did not study their effects individually.

Some other contributions have investigated the effects of individual stray inductances analytically, where differential equations were established to solve the switching waveforms under different parasitic inductances [7-9]. Due to the nonlinear nature of the switching device, however, the solutions were usually very complicated and thus the stray inductance effects could not be intuitively seen from the expressions. Furthermore, the analytical solutions were only approximate because of the many assumptions made to make the equations solvable. This would also limit the conclusions obtained from the analytical study in question.

This chapter, from another angle, systematically studies the effects of the two aspects of the switching ringing – the parasitic inductances coming from the device packages and circuit interconnections, and the parasitic capacitances originating from the device junctions. Instead of analytical analysis, the parametric study has been conducted mainly through experiments. Several most critical parasitic parameters have been identified and investigated on their individual effect through the MOSFET switching test. Corresponding circuit simulations have been used to verify the conclusions obtained from the experiments. The influence of the parasitics on the MOSFET switching characteristics has also been studied and summarized.

6.2 Parametric Study on the Parasitic Inductances

The MOSFET switching test is still conducted with the use of the double-pulse tester introduced in Chapter 2. To save the costly SiC MOSFET, a 600 V, 20 A Si CoolMOS (APT20N60BCF from MicroSemi) is used instead for the study, and the gate drive voltage from IXDD414 is accordingly adjusted to 0 ~ 10 V. The other circuit components remain the same.

From the derivation of Faraday's Law, it is clear that inductance is only defined for a closed contour. This means that it is the closed current loop formed by a wire that has inductance, not the wire itself [10]. Based on this concept, three primary stray inductances can be identified based on the structure of the double-pulse tester (See Figure 2-3), namely (1) the gate loop inductance L_{GS} formed by the gate current path; (2) the main switching loop inductance L_{DS} formed by the drain current path, and (3) the common source inductance L_{SS} shared by both loops. The switching loop inductance is essentially a lumped one which includes the partial inductances from the MOSFET and diode packages, and the PCB interconnections. The common source inductance can be treated as a mutual inductance between the gate loop and the switching loop.

To study the influence of these parasitic parameters, the current paths in the tester have been broken at the points shown in Figure 6-1 (a), so that small inductances can be inserted into the loop to mimic the parasitic ones coming from the structure. The small inductances are made of several air-core coils with 2 turns, 4 turns and 5 turns respectively (Figure 6-1 (b)), which produce the corresponding inductances of 22 nH, 47 nH and 65 nH. In the experiment, each type of stray inductance is controlled with the rest breakpoints simply shorted, such that its effect can be studied independently.

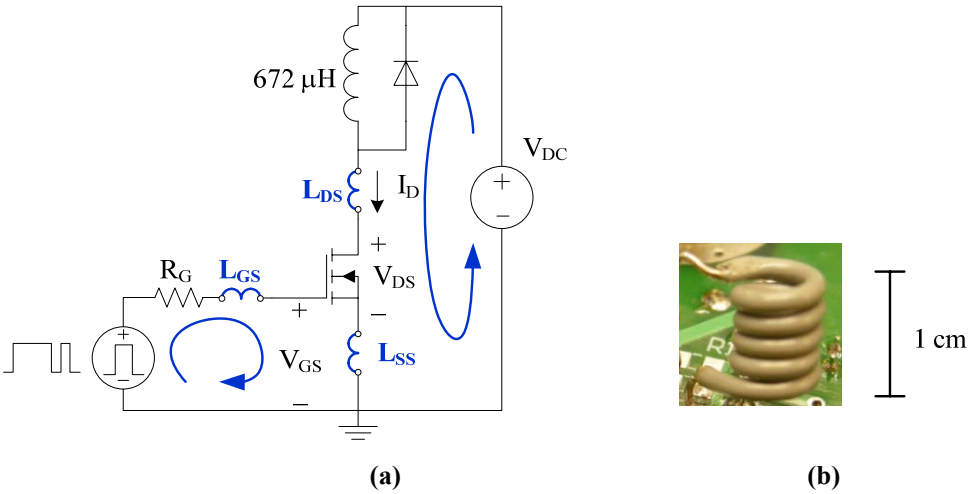

Figure 6-1. Double-pulse tester with external parasitic inductances. (a) Schematic, (b) inductor coil

In the experiment, the MOSFET is switched up to 400 V, 10 A, with different gate resistances to adjust the switching speed. A similar simulation circuit is also built in Synopsys Saber, where 5 nH gate loop inductance and 20 nH switching loop inductance are assumed for the intrinsic parasitics of the PCB. The MOSFET model is provided by the manufacturer and available on their website.

6.2.1 Gate Loop Stray Inductance L_{GS}

Figure 6-2 shows the MOSFET 400 V, 10 A switching waveforms with 5 Ω gate resistance, under the influence of the gate loop stray inductance L_{GS}. In the experiment, L_{GS} is increased gradually from 0 nH to 65 nH. This inductance, as stated in many publications, tends to resonate with the MOSFET input capacitance and thus causes oscillation in the gate-source voltage waveform, which is quite apparent in the turn-off transients. However, the oscillation in V_{GS} only leads to limited ringing in drain-source voltage and drain current waveforms. For the turn-on transients, V_{DS} and I_D almost do not change; while for turn-off the ringing starts to deteriorate in these waveforms as L_{GS} increases. For instance, the turn-off V_{DS} spike increases from about 460 V when L_{GS} = 0, to 480 V when L_{GS} = 65 nH. Even so, the influence of L_{GS} is still quite limited within the gate loop, and the MOSFET switching waveforms are only slightly affected if compared to the effect of the main switching loop inductance L_{DS}.

Accordingly, the simulation results are shown in Figure 6-3. Observed again in the figure is the limited ringing in V_{DS} and I_D caused by V_{GS}, which is consistent with the experimental results. From this it can be concluded that the gate loop oscillation can be coupled to the main switching loop, however its effect on the switching waveforms is very limited.

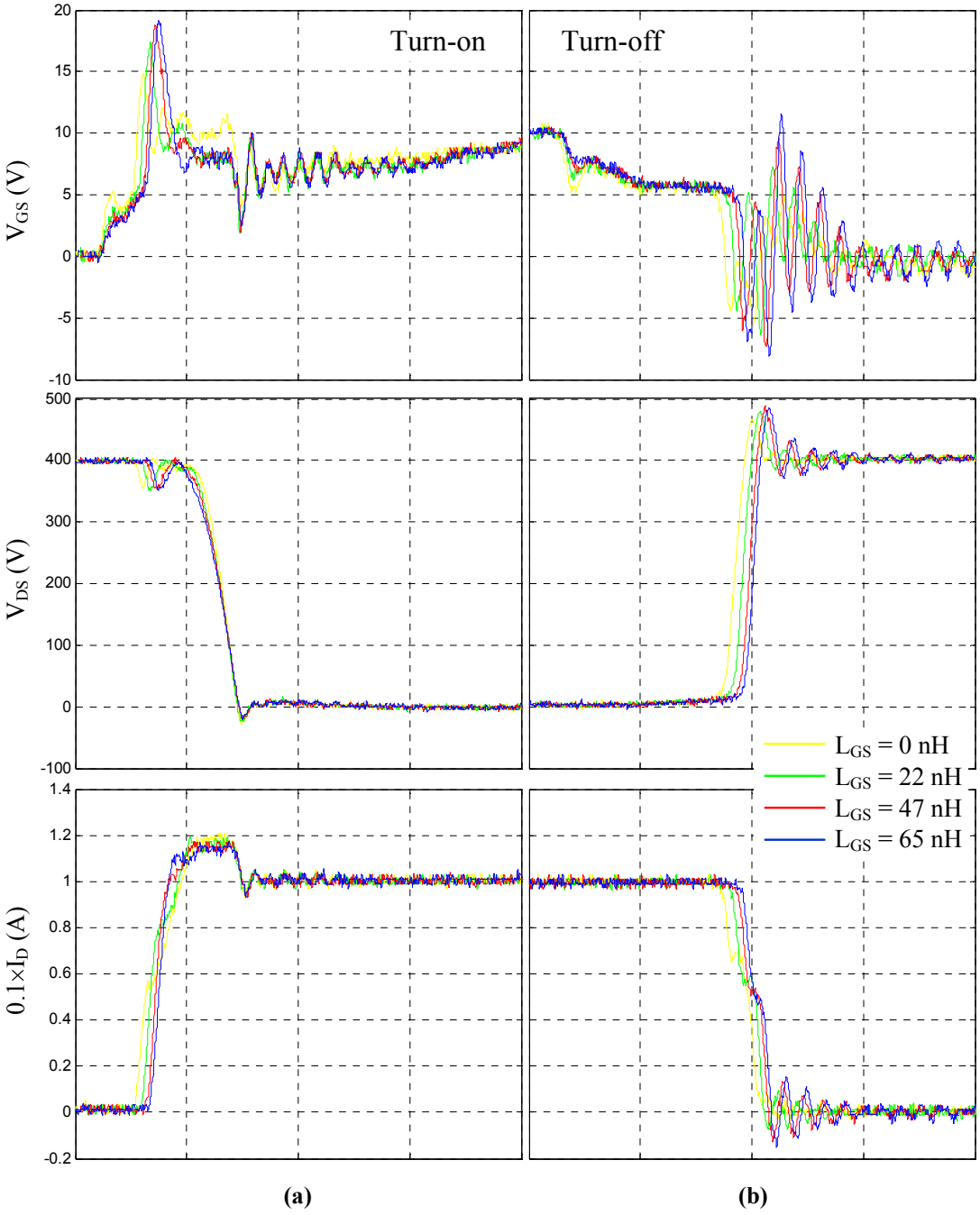

Figure 6-2. Experimental waveforms showing the influence of gate loop stray inductance L_{GS}. 400 V, 10 A, R_G = 5 Ω. (a) Turn-on, (b) turn-off. Time: 50 ns/div

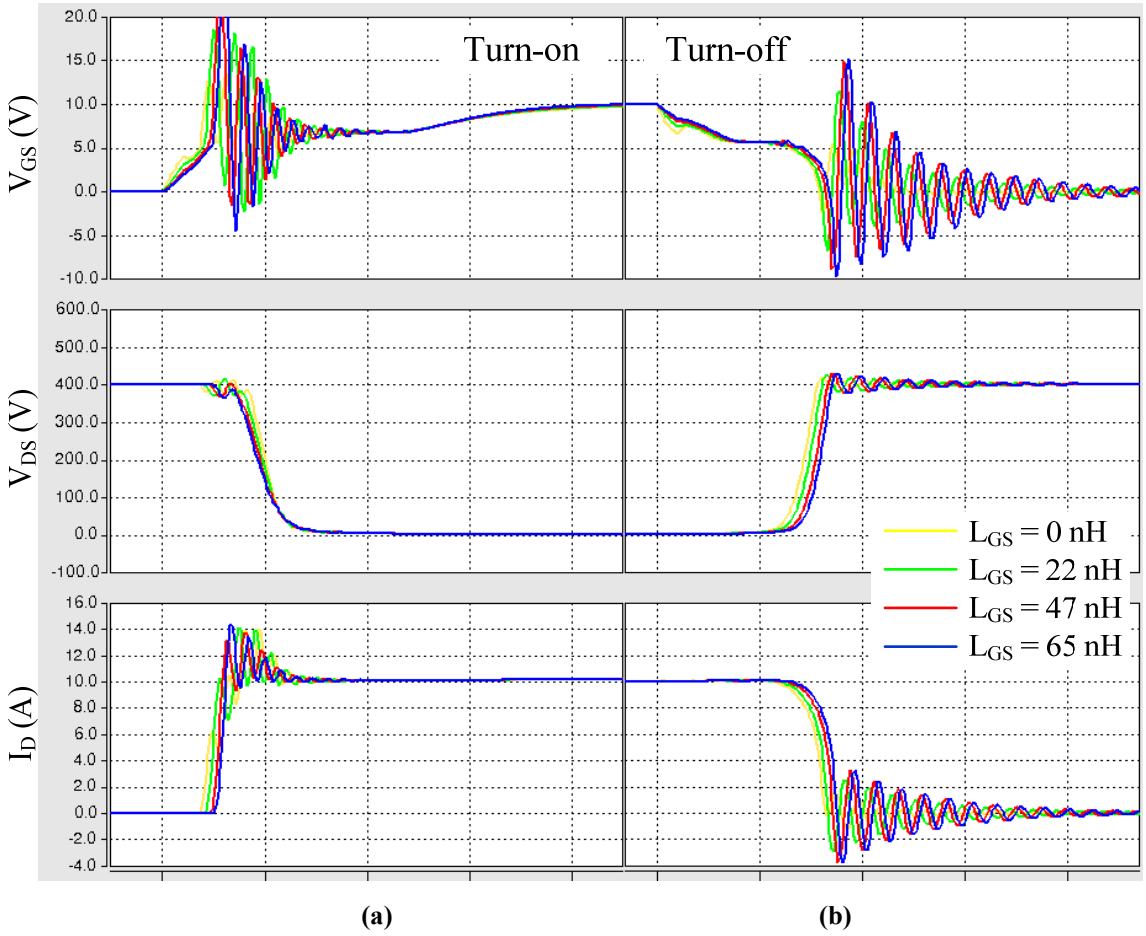

Figure 6-3. Simulation waveforms showing the influence of gate loop stray inductance L_{GS}. 400 V, 10 A, R_G = 5 Ω. (a) Turn-on, (b) turn-off. Time: 50 ns/div

6.2.2 Main Switching Loop Stray Inductance L_{DS}

Figure 6-4 shows the effect of the main switching loop stray inductance L_{DS} under the same switching condition as that of Figure 6-2. As seen from the figure, the increase in L_{DS} introduces oscillations in all V_{GS}, V_{DS} and I_D waveforms, and during both turn-on and turn-off transients. Compared with the effect of L_{GS} shown in Figure 6-2, in this case the ringing amplitude, frequency, as well as settling time all become worse with the increasing L_{DS}. Still examining the turn-off V_{DS} waveform, one may find that the voltage spike increases from about 460 V when L_{DS} = 0 nH, to almost 530 V when L_{DS} = 65 nH. By comparison, it can be clearly seen that the switching loop inductance affects the MOSFET switching characteristics much more than the gate loop inductance, causing even worse oscillation and stress on the device.

The simulated waveforms shown in Figure 6-5 again verify the results seen in the experiment. Furthermore, the simulation also shows that, as long as the parasitic inductance is serially connected within the main switching loop, it produces exactly the same waveforms no matter it is connected in direct series with the MOSFET, the diode, or the DC source. This again proves the effectiveness of lumping partial inductances along the loop to represent the total stray inductance.

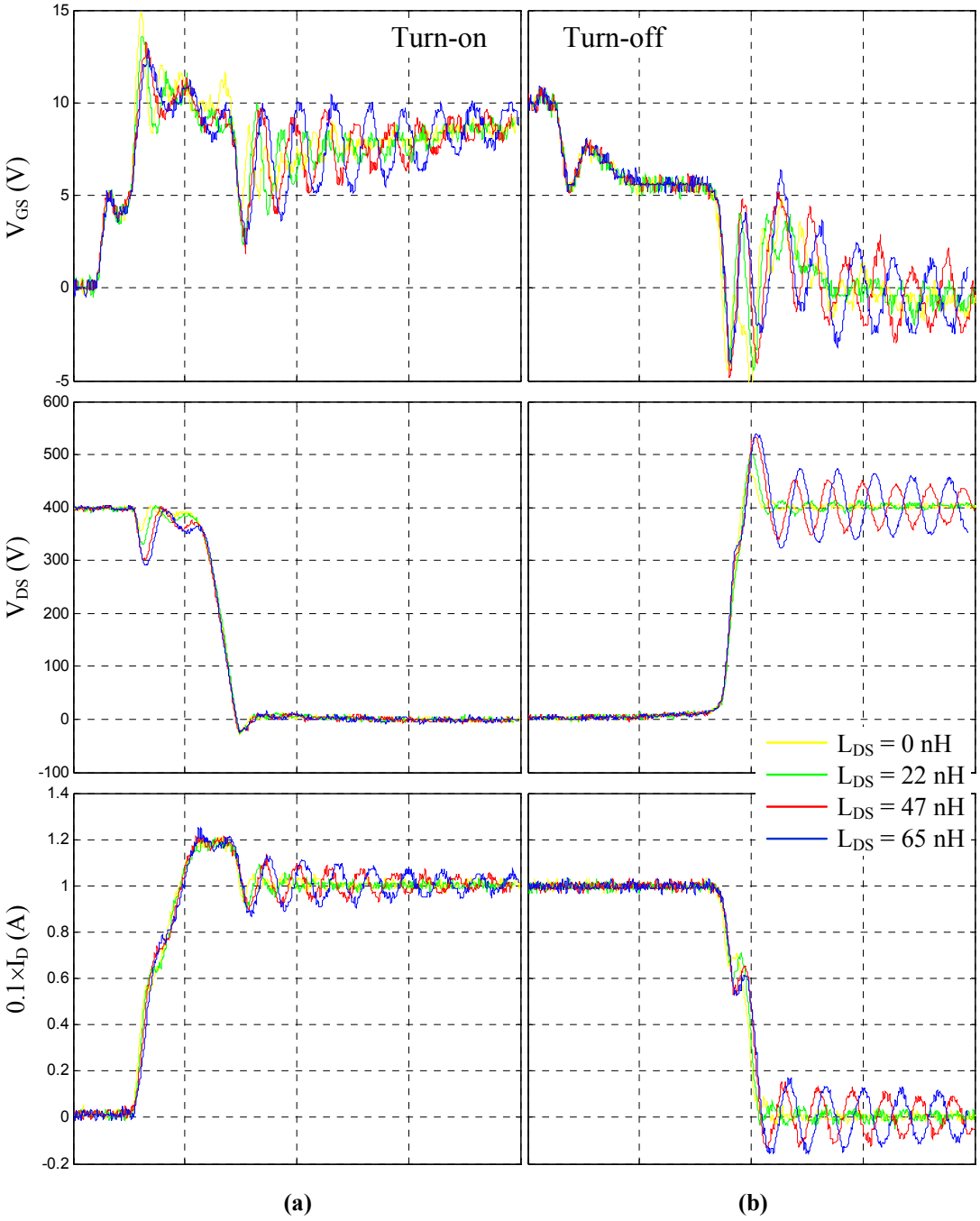

Figure 6-4. Experimental waveforms showing the influence of main switching loop inductance L_{DS}. 400 V, 10 A, R_G = 5 Ω. (a) Turn-on, (b) turn-off. Time: 50 ns/div

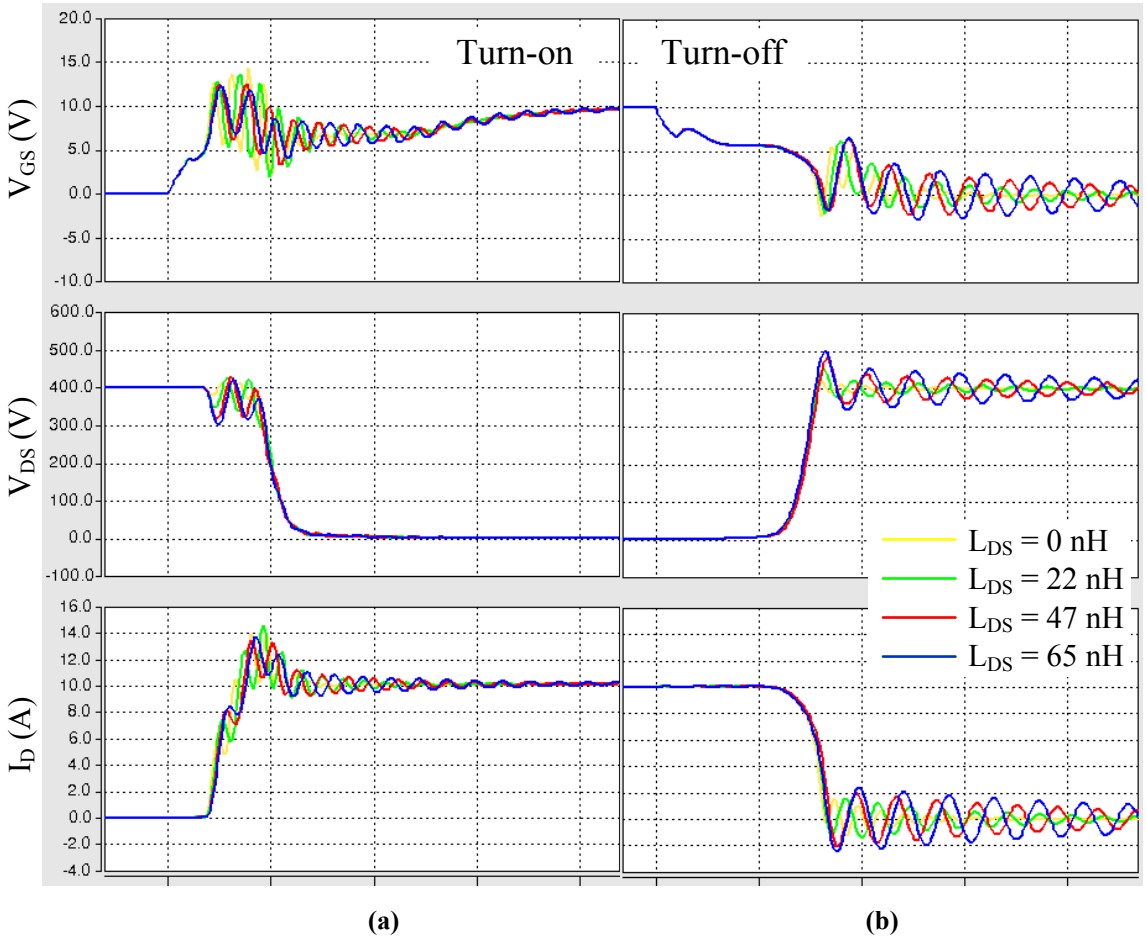

Figure 6-5. Simulation waveforms showing the influence of main switching loop inductance L_{DS}. 400 V, 10 A, R_G = 5 Ω. (a) Turn-on, (b) turn-off. Time: 50 ns/div

6.2.3 Common Source Stray Inductance L_{SS}

Figure 6-6, on the other hand, exhibits the effect of the common source inductance L_{SS} on the switching waveforms. In this case the MOSFET is tested under the same voltage and current stresses but with 15 Ω gate resistance. Basically, L_{SS} serves as a negative feedback from the main switching loop to the gate loop, as the voltage drop across L_{SS} counteracts the change of the gate voltage during I_D rise and fall periods, thus slowing down the drain current [11-12]. This can be clearly seen in Figure 6-6. The consequence of a bigger L_{SS} is not to worsen the voltage stress and current ringing of the device – due to its slowing-down effect, but to significantly increase the switching energy at turn-on and turn-off. The simulation result shown in Figure 6-7 leads to the same conclusion.

Due to the negative feedback effect of L_{SS}, when L_{DS} and L_{SS} are both in the circuit, the ringing caused by L_{DS} tends to be suppressed by L_{SS}. This can be seen from Figure 6-8, where the switching loop inductance is fixed at 65 nH, while the common source inductance varies from 0 to 47 nH. As seen, both V_{DS} and I_D spikes are reduced as L_{SS} increases, which is consistent with the analytical solutions in [8]. However the price paid is still much higher switching loss due to the slower drain current slew rate.

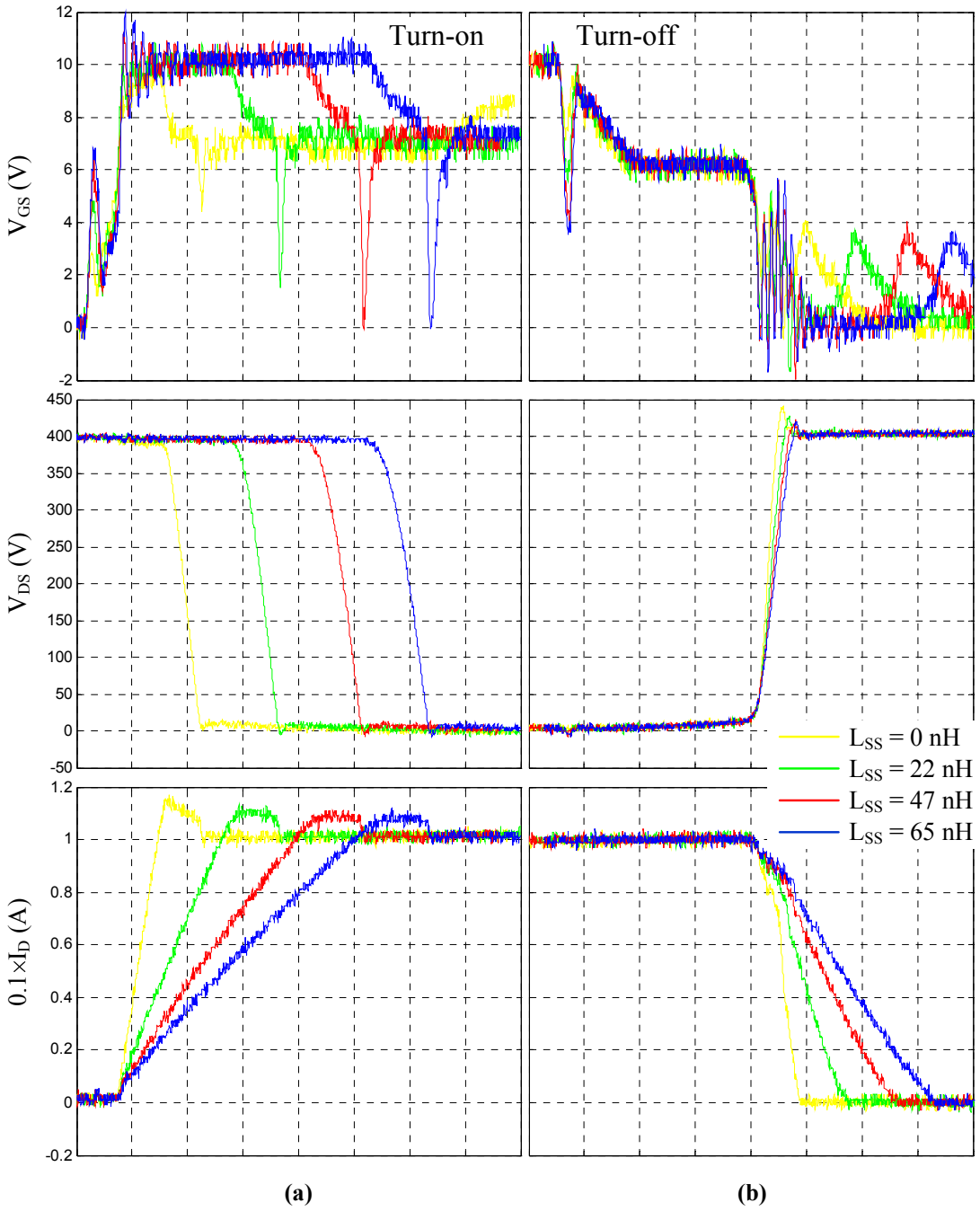

Figure 6-6. Experimental waveforms showing the influence of common source inductance L_{SS}. 400 V, 10 A, R_G = 15 Ω. (a) Turn-on, (b) turn-off. Time: 50 ns/div

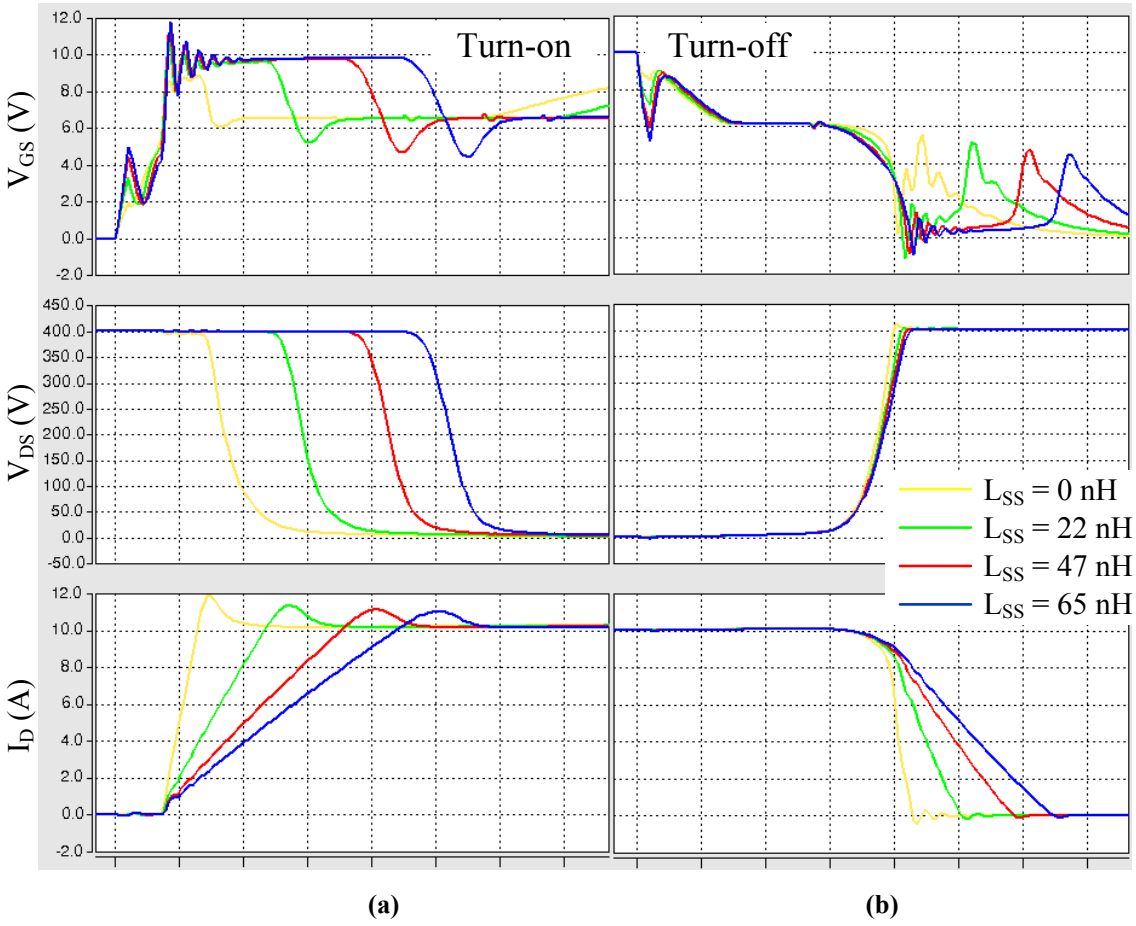

Figure 6-7. Simulation waveforms showing the influence of common source stray inductance L_{SS}. 400 V, 10 A, R_G = 15 Ω. (a) Turn-on, (b) turn-off. Time: 50 ns/div

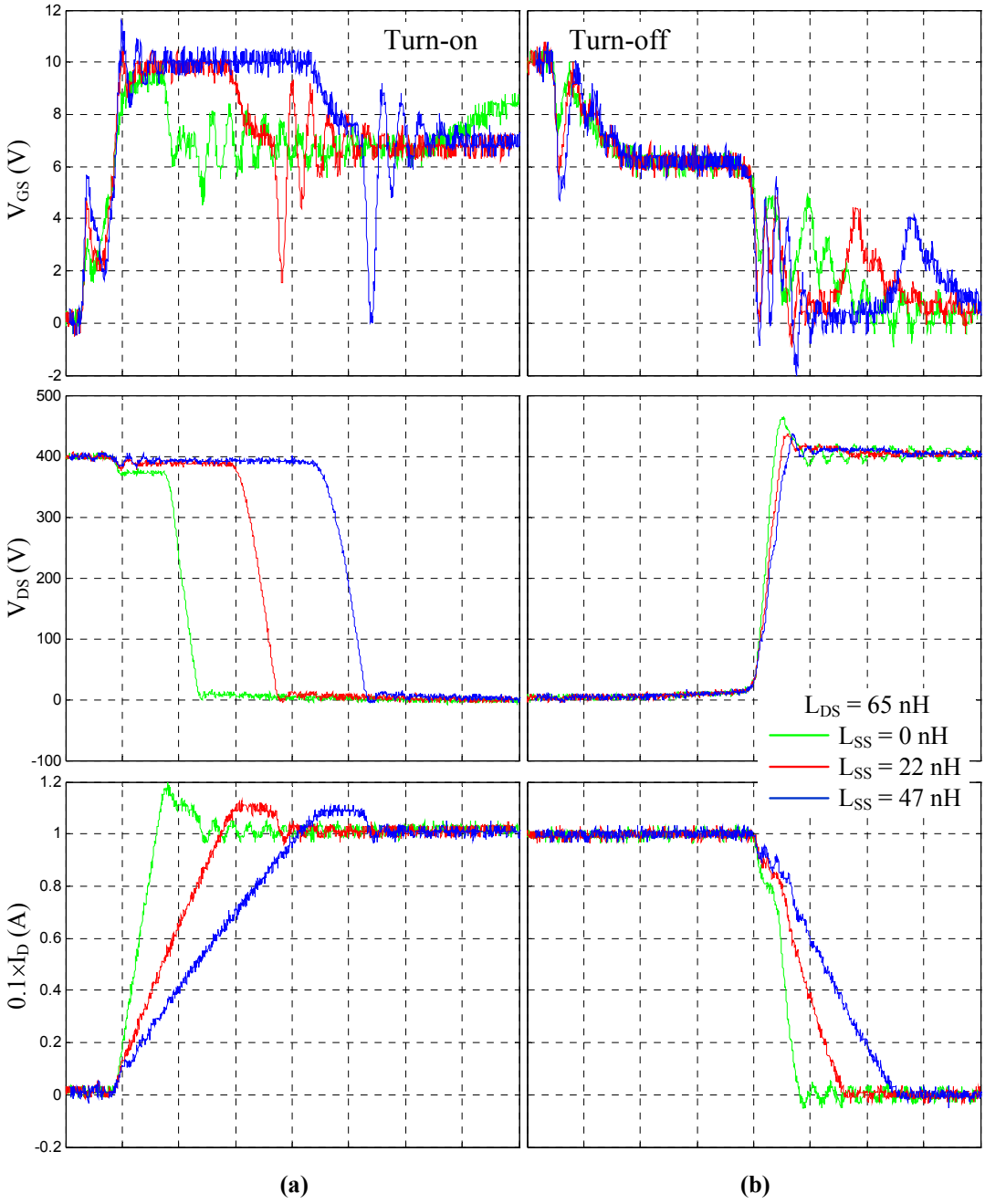

Figure 6-8. Co-effect of L_{DS} and L_{SS}.

400 V, 10 A, R_G = 15 Ω. (a) Turn-on, (b) turn-off. Time: 50 ns/div

6.2.4 Summary of Parasitic Inductance Effects

Based on the experimental and simulated results, the following conclusions can be reached from the parametric study:

(1) Generally speaking, the parasitic ringing due to fast switching speed is more sensitive to the main switching loop inductance L_{DS} than the gate loop inductance L_{GS}, although both of them increase the severity of ringing. There are three reasons for this:

First of all, the gate drive circuit layout can be localized more easily than the main power loop, which means L_{GS} is usually smaller than L_{DS};

Secondly, more damping exists in the gate loop than the switching loop, such as the gate resistance, gate driver output impedance, and MOSFET internal gate resistance, while the only damping in the switching loop comes from the interconnect resistances, which is usually too small to decay the oscillation quickly;

Thirdly, the gate current slew rate is also much smaller than that of the drain current. The peak gate current is around 1 A in this work, ten times smaller than the drain current. The corresponding di/dt in the gate loop is thus much smaller than the switching loop.

(2) The common source inductance L_{SS} works as a negative feedback from the switching loop to the gate loop, making the drain current slower, and consequently increasing the switching loss significantly. However, it hardly affects the drain-source voltage slew rate, nor does it cause any parasitic ringing in the switching waveforms.

(3) When L_{DS} and L_{SS} are both in the circuit, L_{SS} can help suppress the parasitic ringing caused by L_{DS} by slowing down the drain current. However the penalty is the increased switching loss.

6.3 *Parametric Study on the Parasitic Capacitances*

6.3.1 Understanding the Parasitic Ringing

It has been concluded from the last section that the parasitic ringing is more sensitive to the main switching loop inductance L_{DS} than the gate loop inductance L_{GS}. Then the question is: what is resonating with L_{DS} during the switching transients? This can be answered by looking at the different current paths during turn-on and turn-off respectively.

Figure 6-9 shows the current path during the turn-on process. During this period the current in the freewheeling diode is transferred to the MOSFET. After the MOSFET has taken all the load current, the drain-source voltage starts to fall and the freewheeling diode stops conducting. As V_{DS} decreases, the diode junction capacitance C_J gets charged and the MOSFET output capacitance C_{OSS} gets discharged. The ringing current then "sees" the impedance of C_J, L_{DS} and C_{OSS} in series, and the current ringing during this period should be caused by L_{DS} resonating with C_J and C_{OSS} in series.

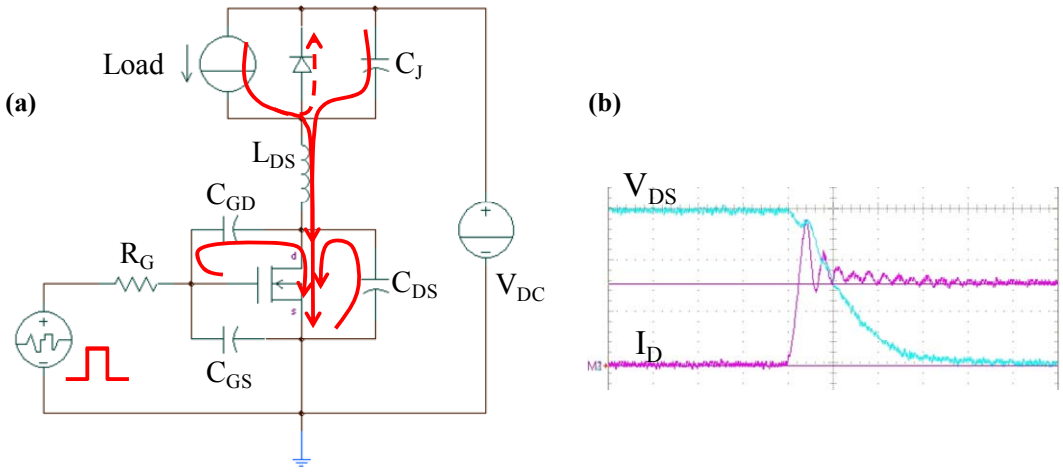

Figure 6-9. Current paths during turn-on process (a) and corresponding waveforms (b)

In this work, the junction capacitance C_J of the freewheeling Schottky barrier diode (SBD) is much smaller than the MOSFET output capacitance C_{OSS}. Therefore C_J in series with C_{OSS} results in a capacitance very close to C_J. In this sense, the turn-on ringing can be treated as solely determined by the diode junction capacitance C_J in this specific work.

On the other hand, the turn-off ringing current sees different impedance along its paths, as shown in Figure 6-10. The current in the MOSFET is transferred back to the freewheeling diode during this period. As V_{DS} rises, C_J gets discharged and C_{OSS} gets charged. Once the MOSFET blocks the full bus voltage, the freewheeling diode starts to conduct, effectively bypassing its junction capacitance. The ringing current in this case sees only L_{DS} and C_{OSS} in series. Therefore, the turn-off ringing is caused by L_{DS} resonating with C_{OSS} alone.

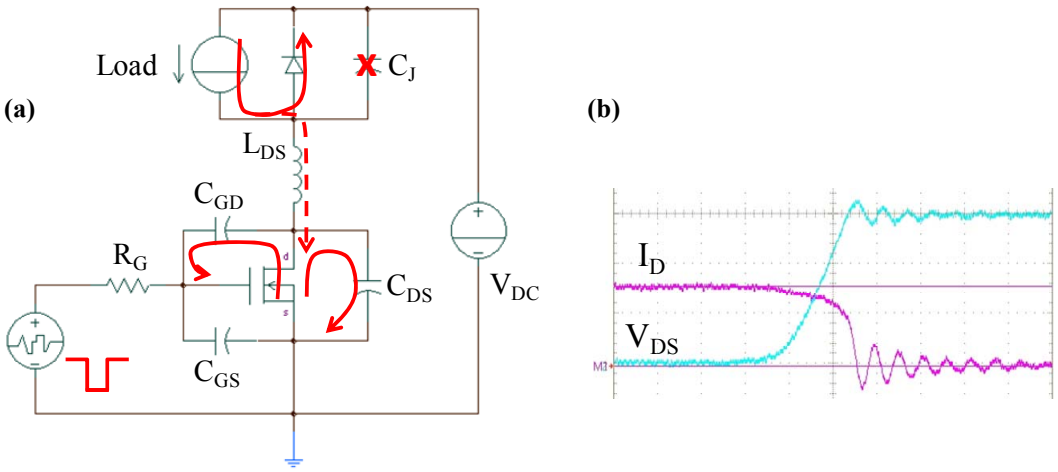

Figure 6-10. Current paths during turn-off process (a) and corresponding waveforms (b)

The different resonating capacitances during turn-on and turn-off also account for the different ringing frequencies observed for the SiC MOSFET in Chapter 4: Because C_J is smaller than C_{OSS}, the turn-on ringing always has a higher frequency than turn-off.

Based on the above analyses, it can be foreseen that devices with lower junction capacitances can be switched faster under the same condition of parasitic ringing. Actually if comparing the switching waveforms of SiC JFET in Chapter 3 and SiC MOSFET in Chapter 4, one can find that SiC JFET can be switched faster with even less parasitic ringing. The different response of the two devices to the same amount of parasitic inductance can be traced back to the difference in their junction capacitances – the SiC MOSFET has around 2.5 nF of C_{DS} at zero voltage, while the SiC JFET has only around 1.0 nF. The junction capacitances, especially the output capacitance C_{OSS}, make the difference in the switching transients.

To consolidate the above hypothesis, a parametric study has been conducted on the device parasitic capacitance as well. The same test circuit is used as in the last section. The MOSFET is switched under 400 V, 10 A with a fixed gate resistance of 15 Ω. External capacitances are added across different device terminals to mimic the bigger junction capacitances. Note that in the experiments the junction capacitances can only be made bigger by paralleling external capacitances. However, the trend is clear enough to infer what would happen in case of lower junction capacitances. For verification purposes, circuit simulation is also done under exactly the same operating condition.

6.3.2 MOSFET Drain-Source Capacitance C_{DS}

Figure 6-11 shows the effect of paralleling capacitances to the drain-source terminals of the MOSFET to mimic a bigger C_{DS}. As seen from Figure 6-11 (a), the turn-on waveforms almost do not change as the capacitance increases from 0 to 500 pF. Only V_{DS} slew rate is slowed down a little bit due to the longer charging time of C_{DS}. No excessive ringing is observed in V_{DS} or I_D waveform. This verifies the fact that during turn-on the ringing is mainly determined by the freewheeling diode junction capacitance C_J, which in this case is not changed. The simulation shown in Figure 6-12 (a) exhibits the same results.

During the turn-off transients, however, the ringing in V_{DS} and I_D waveforms increase apparently as the capacitance becomes bigger. As stated above, C_{OSS} of the MOSFET is the major contributor to the parasitic ringing during this period, and C_{DS} is just the major part of C_{OSS}. One may question the severe ringing in I_D under such moderate switching speed (R_G = 15 Ω). It is true that under normal speed the switching waveforms should not oscillate so severely, or even do not oscillate at all, but this happens for the original C_{DS} of MOSFET which is around 100 pF under V_{DS} = 400 V. In this test, however, the additional C_{DS} is over five times the original value, which causes the excessive ringing even under moderate switching speed. Or, in other word, if a device has such a big C_{DS}, even this moderate switching speed would become the speed limit for the device.

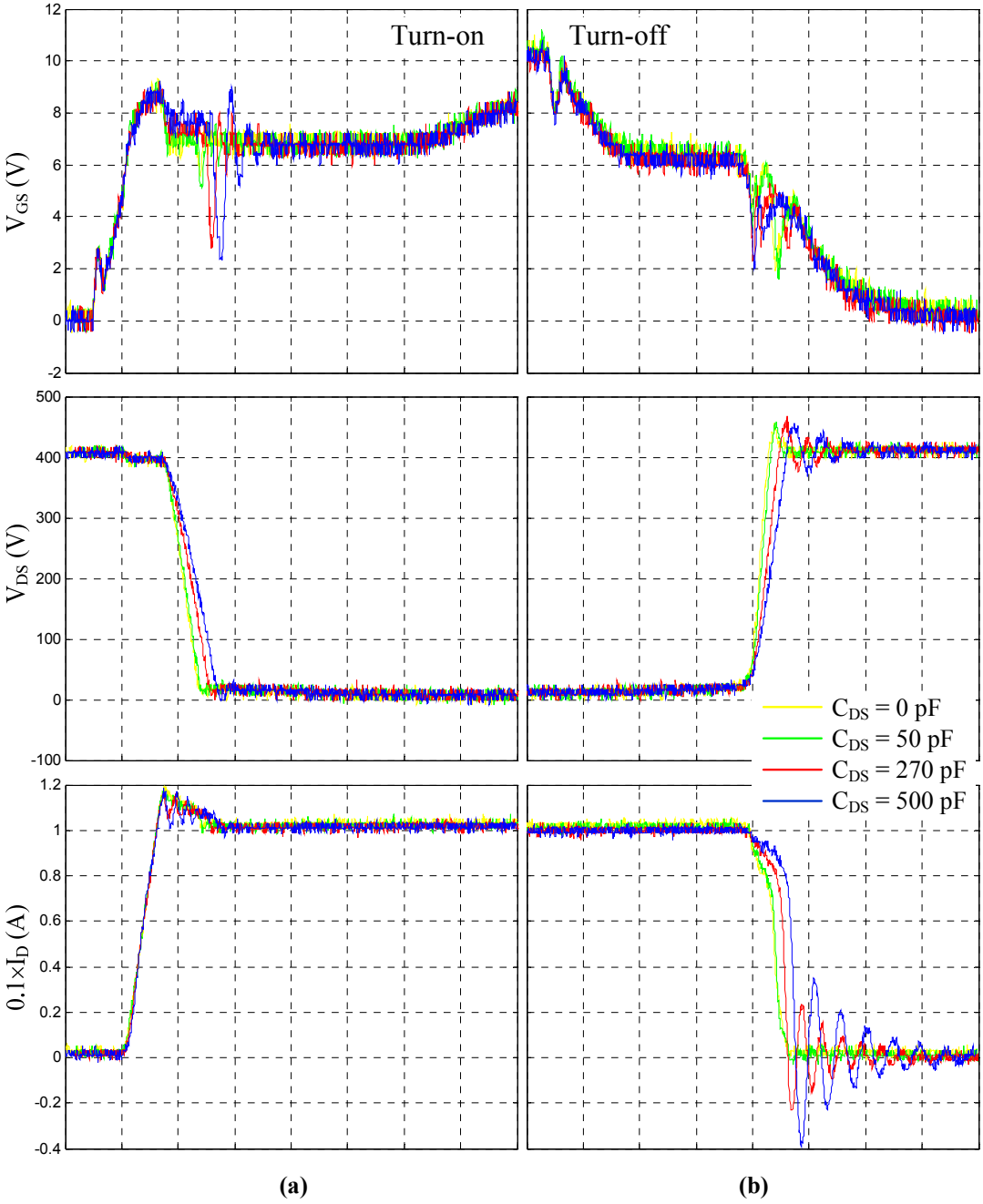

Figure 6-11. Experimental waveforms showing the influence of MOSFET C_{DS}. 400 V, 10 A, R_G = 15 Ω. (a) Turn-on, (b) turn-off. Time: 50 ns/div

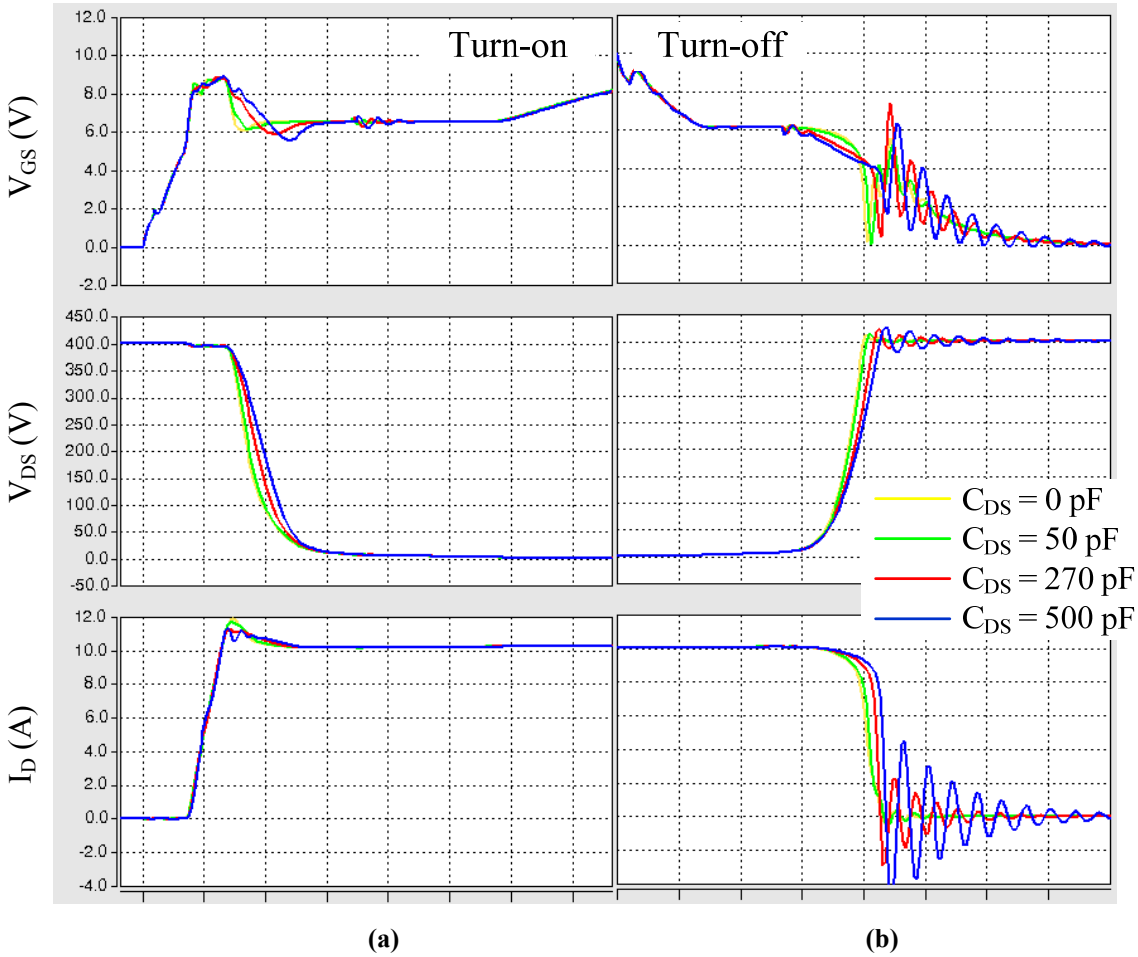

Figure 6-12. Simulation waveforms showing the influence of MOSFET C_{DS}.

400 V, 10 A, R_G = 15 Ω. (a) Turn-on, (b) turn-off. Time: 50 ns/div

6.3.3 Freewheeling Diode Junction Capacitance C_J

Figure 6-13 shows the effect of C_J, the junction capacitance of the freewheeling diode. As analyzed previously, this capacitance increases the turn-on current spike and the parasitic ringing, which is clearly seen from Figure 6-13 (a). During turn-off, C_J draws more current from the load to discharge itself, and faster I_D falling speed can be observed. However, C_J does not cause any excessive ringing during this period as seen in Figure 6-13 (b). This again proves the correctness of the previous analyses.

The simulation waveforms in Figure 6-14 do not predict the parasitic ringing. However C_J's charging and discharging effect on the drain current is still very obvious.

6.3.4 MOSFET Gate-Drain (Miller) Capacitance C_{GD}

Figure 6-15 and Figure 6-16 show the effect of the Miller capacitance C_{GD}. As explained earlier, Miller capacitance can be decoupled into an equivalent input capacitance which is greatly amplified during V_{DS} rise and fall periods. Therefore, V_{DS} slew rates are very sensitive to and essentially determined by C_{GD}. As seen from both figures, V_{DS} becomes slower (and correspondingly V_{GS} plateau region expands) as the external Miller capacitance increases from 0 to 15 pF. The I_D slew rate is not affected at all, except that during turn-off I_D is delayed a little bit due to the slower V_{DS}. However, adding extra Miller capacitance does not cause extra ringing in the switching waveforms.

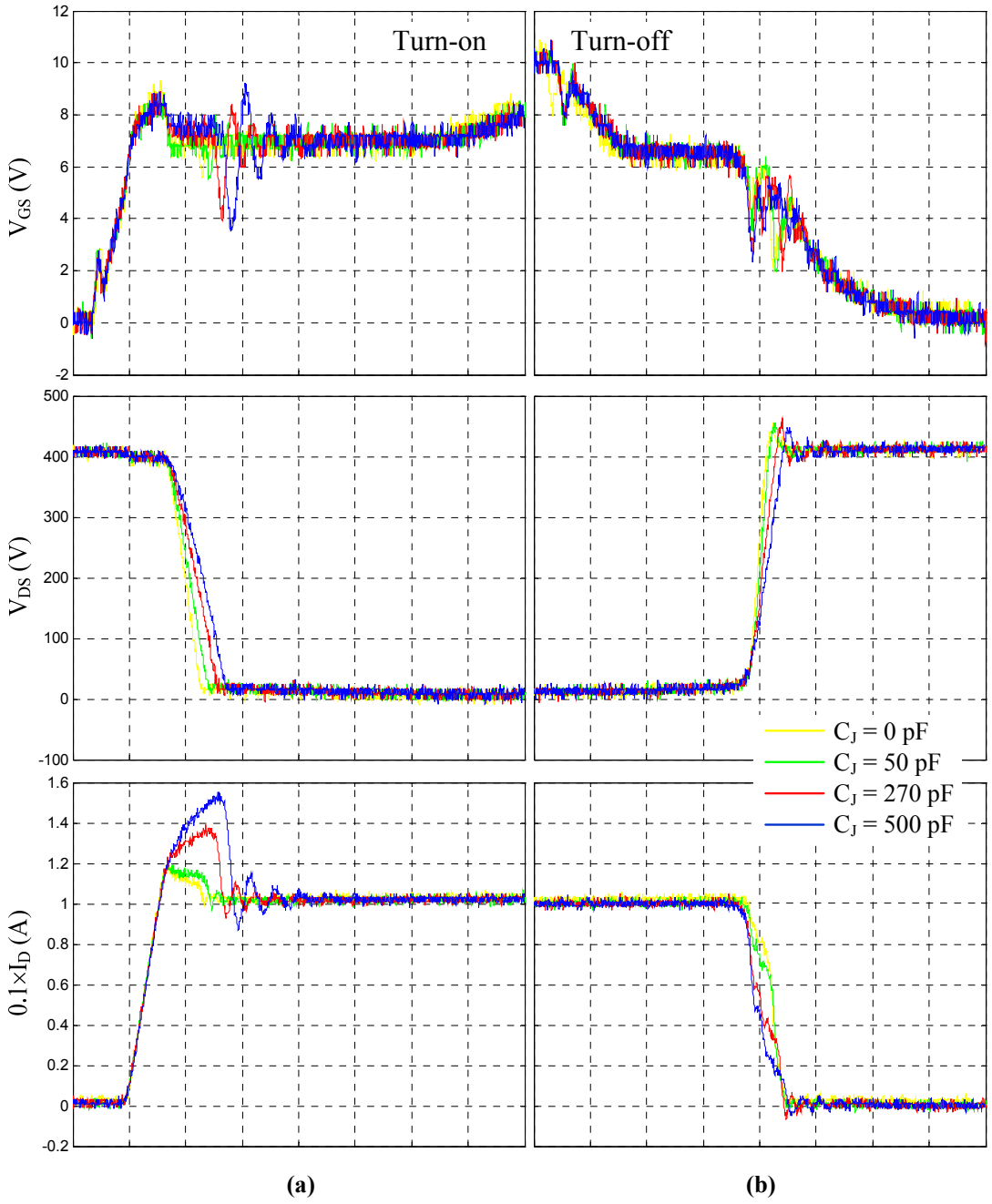

Figure 6-13. Experimental waveforms showing the influence of freewheeling diode C_J. 400 V, 10 A, R_G = 15 Ω. (a) Turn-on, (b) turn-off. Time: 50 ns/div

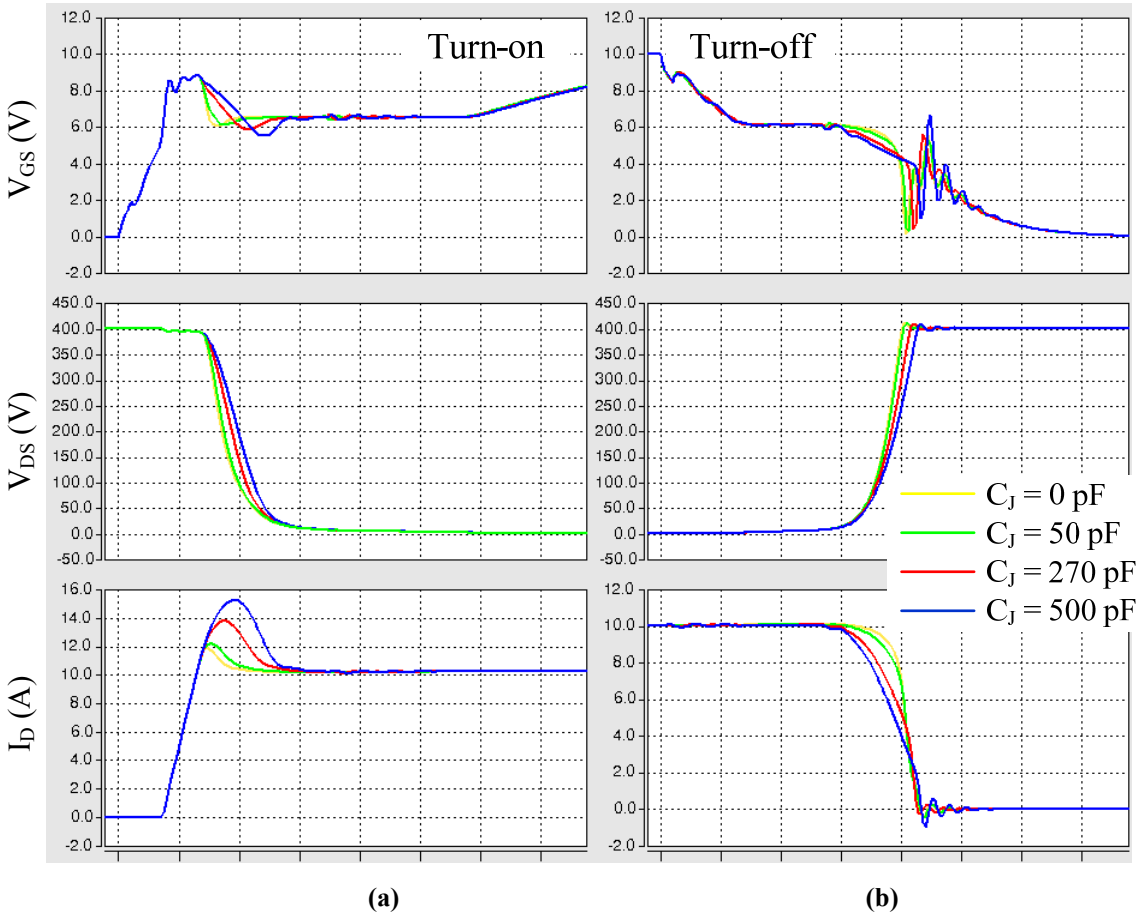

Figure 6-14. Simulation waveforms showing the influence of freewheeling diode C_J. 400 V, 10 A, R_G = 15 Ω. (a) Turn-on, (b) turn-off. Time: 50 ns/div

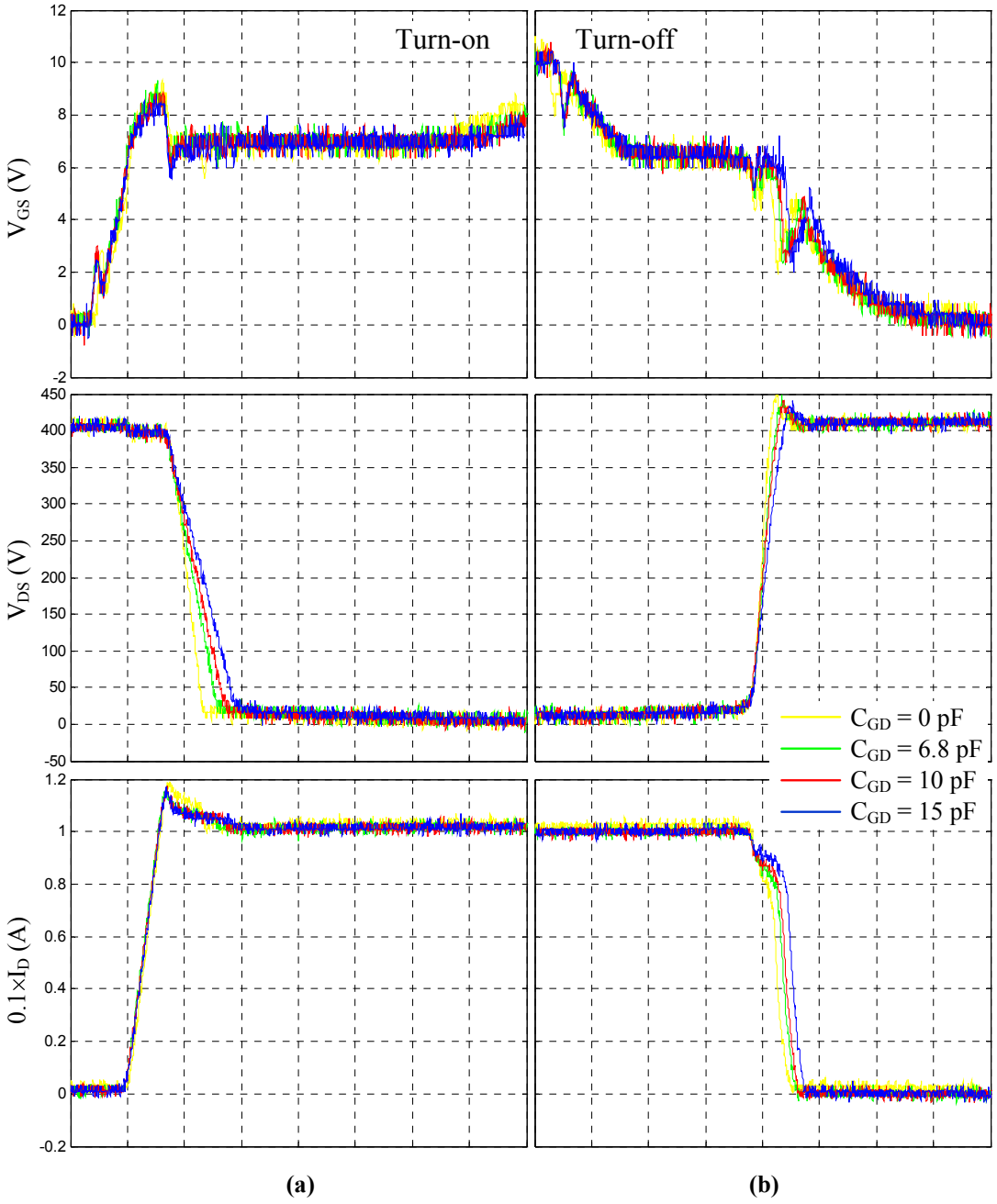

Figure 6-15. Experimental waveforms showing the influence of MOSFET C_{GD}. 400 V, 10 A, R_G = 15 Ω. (a) Turn-on, (b) turn-off. Time: 50 ns/div

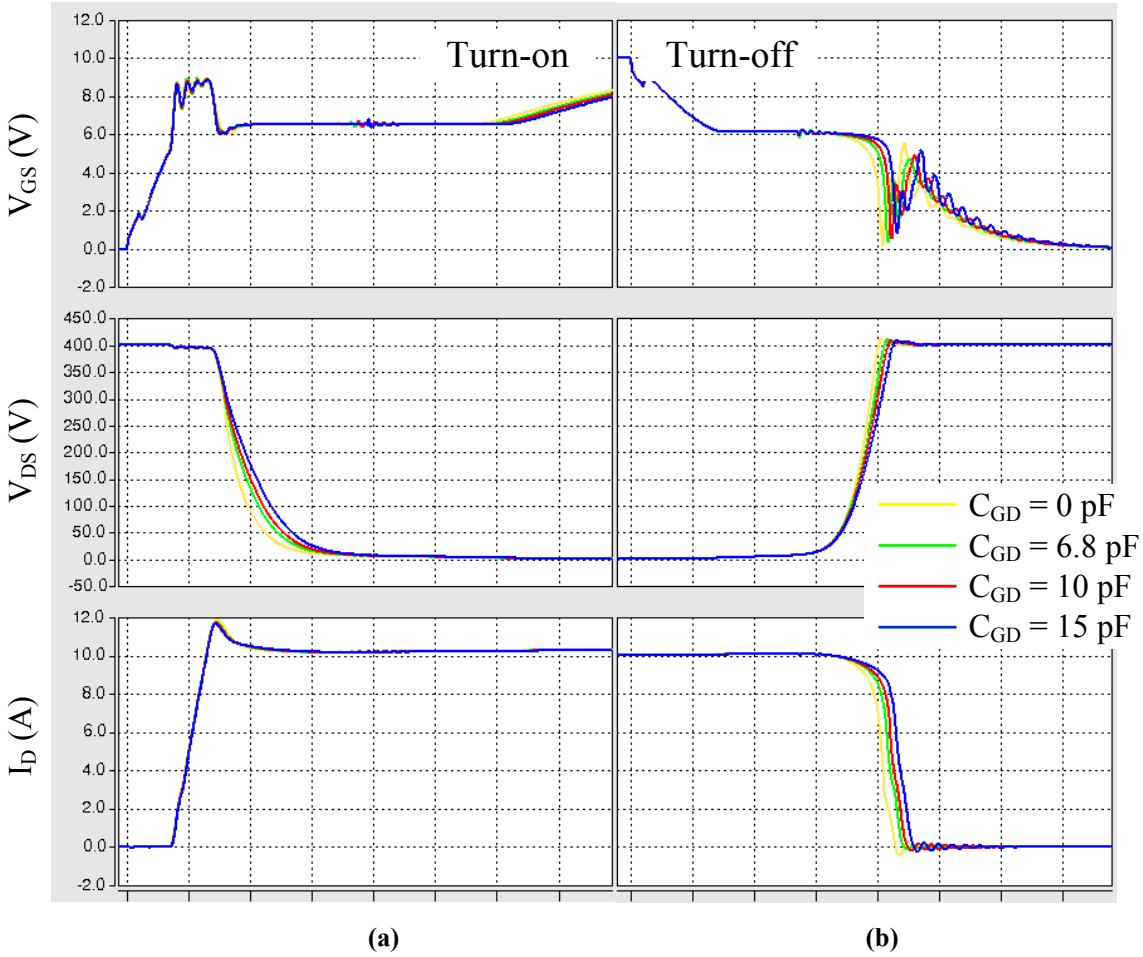

Figure 6-16. Simulation waveforms showing the influence of MOSFET C_{GD}. 400 V, 10 A, R_G = 15 Ω. (a) Turn-on, (b) turn-off. Time: 50 ns/div

6.3.5 MOSFET Gate-Source Capacitance C_{GS}

Figure 6-17 and Figure 6-18 show the effect of the gate-source capacitance C_{GS}. This capacitance mainly determines the time constant of the MOSFET gate circuit. Therefore, as the external C_{GS} increases from 0 to 1.5 nF, V_{GS} becomes slower, and accordingly the switching delay increases and I_D slew rate decreases (Refer to Table 2-1). Still, this capacitance does not have a great influence on the high-frequency parasitic ringing.

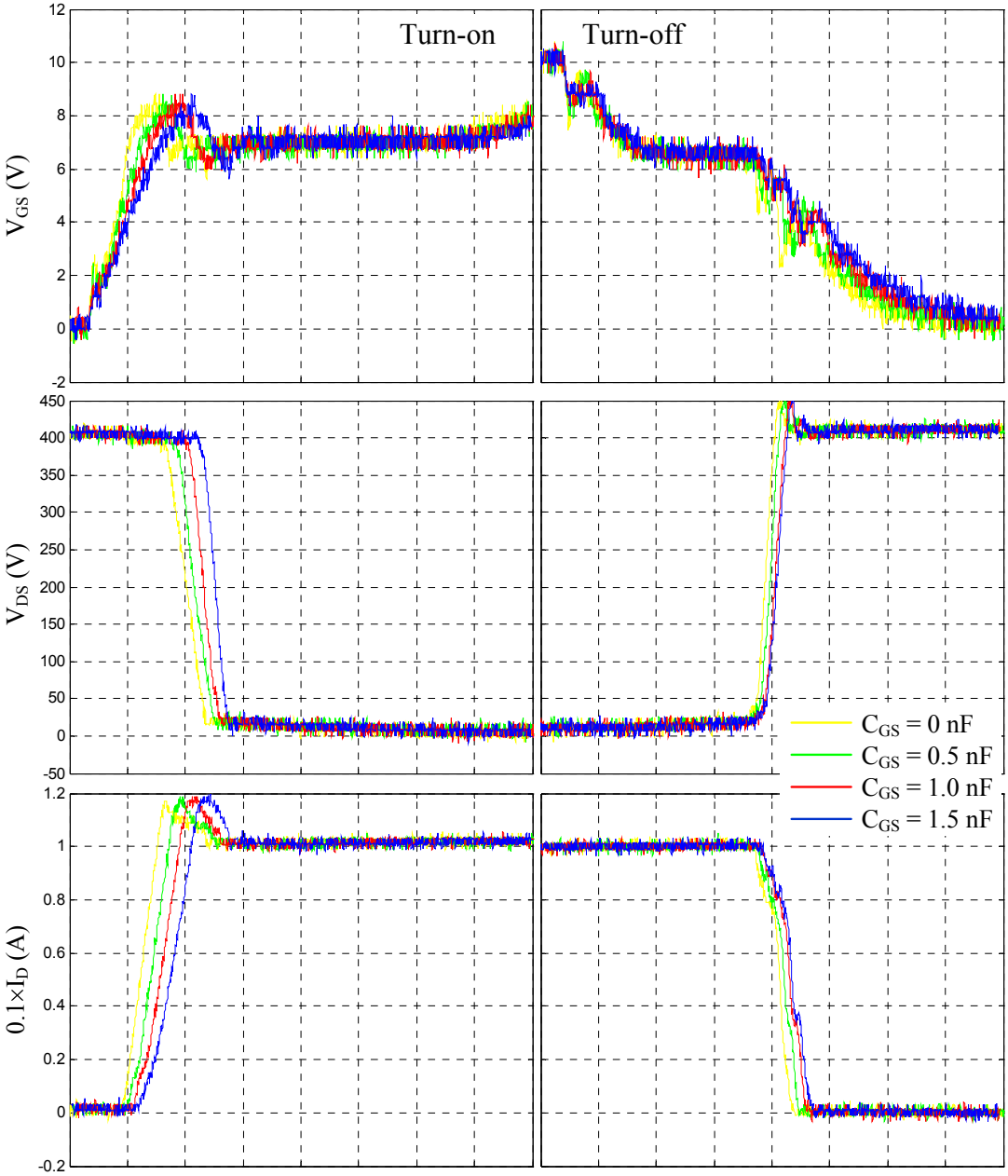

Figure 6-17. Experimental waveforms showing the influence of MOSFET C_{GS}. 400 V, 10 A, R_G = 15 Ω. (a) Turn-on, (b) turn-off. Time: 50 ns/div

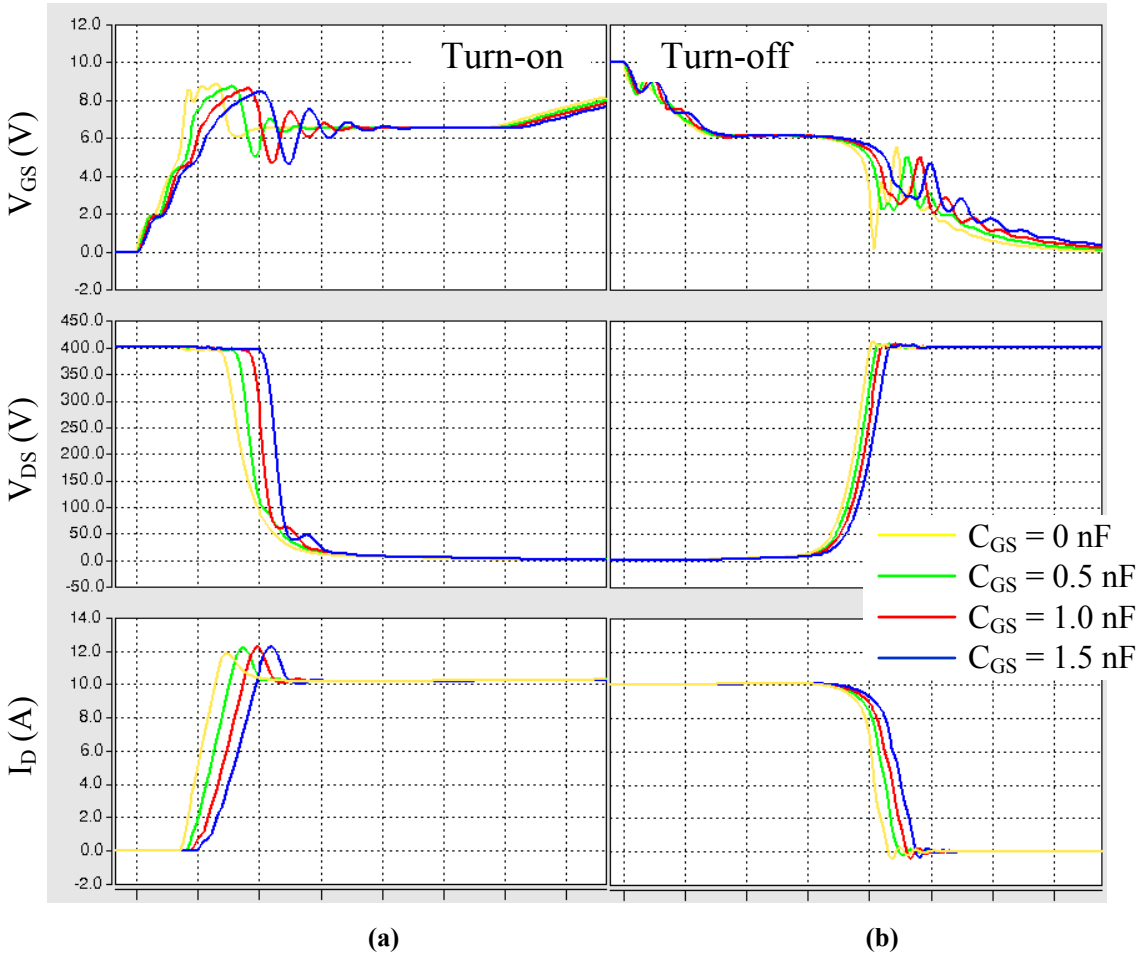

Figure 6-18. Simulation waveforms showing the influence of MOSFET C_{GS}.

400 V, 10 A, R_G = 15 Ω. (a) Turn-on, (b) turn-off. Time: 50 ns/div

6.3.6 MOSFET with Smaller Junction Capacitances

From the above parametric study it has been clearly exhibited which capacitance plays what role in the MOSFET switching characteristics. The limitation of the experiments is that the capacitances can only be made bigger. To strengthen the hypothesis, it is desirable to see how the same device behaves with less junction capacitances, and one can easily achieve this in the simulation by manipulating the MOSFET model. In the following simulation, the C_{DS}, C_{GD} and C_{GS} of the SiC MOSFET model are respectively reduced by about 50 % of their original values. The corresponding switching waveforms are then compared with the original model, which are shown from Figure 6-19 to Figure 6-21. As seen in Figure 6-19, with half C_{DS} the turn-on current ringing is reduced and turn-off ringing is almost eliminated. Whereas for the other two cases, only voltage or current slew rates and delays are changed, while the parasitic ringing still remains in the switching waveforms.

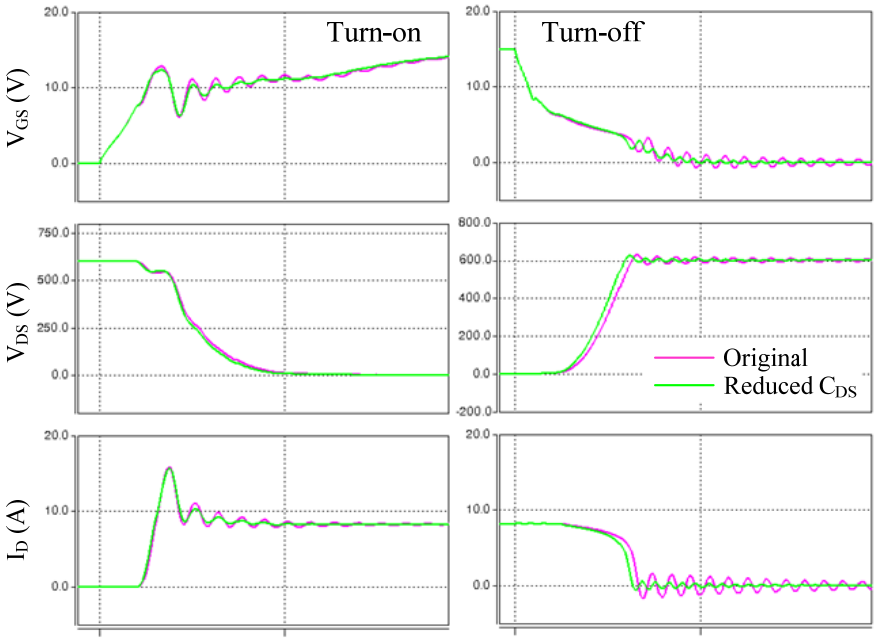

Figure 6-19. Switching waveforms of SiC MOSFET model: original vs. 50 % C_{DS}

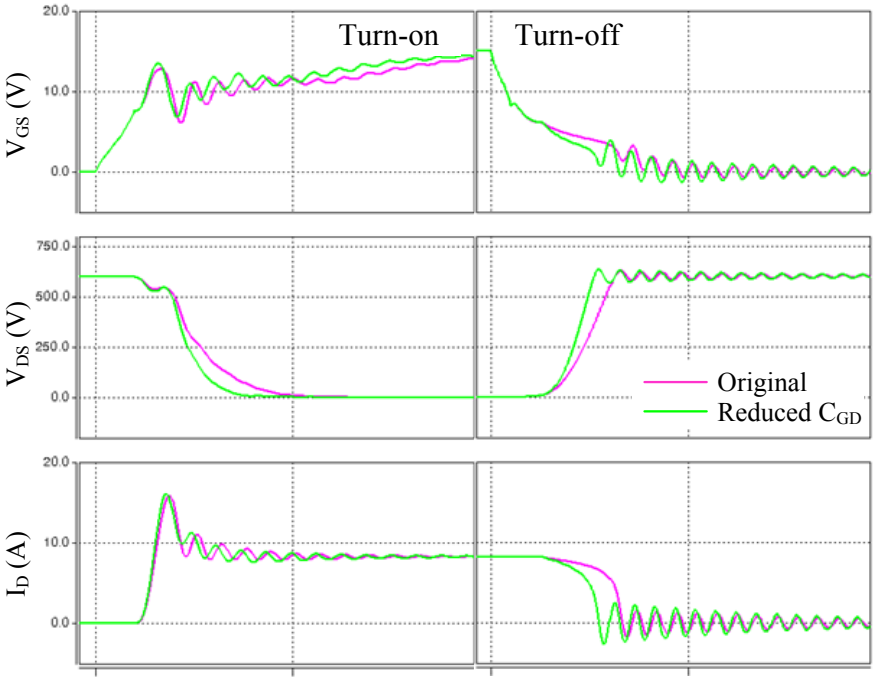

Figure 6-20. Switching waveforms of SiC MOSFET model: original vs. 50 % C_{GD}

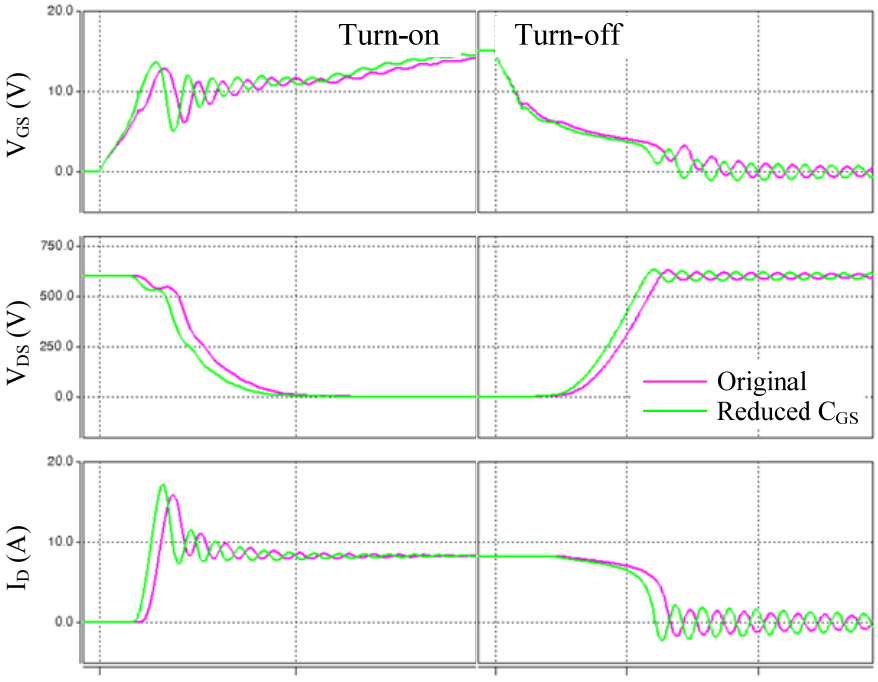

Figure 6-21. Switching waveforms of SiC MOSFET model: original vs. 50 % C_{GS}

6.3.7 Summary of Parasitic Capacitance Effects

The following can be concluded for the MOSFET parasitic capacitances:

(1) The MOSFET drain-source capacitance C_{DS} is the main contributor to the parasitic ringing. It is effective during both turn-on and turn-off transients. Smaller C_{DS} results in smaller ringing, which is most apparent in the turn-off transients.

(2) The freewheeling diode junction capacitance C_J is another major contributor to the current spike and the parasitic ringing during turn-on transients. It appears only during turn-on because during turn-off it is effectively shorted by the diode.

(3) The Miller capacitance C_{GD} mainly determines the V_{DS} slew rate. Smaller C_{GD} results in faster V_{DS} and thus lower switching loss. On the other hand, this capacitance, though part of the MOSFET output capacitance C_{OSS}, does not affect too much the parasitic ringing. Smaller C_{GD} even has a negative effect on the ringing because V_{DS} is faster.

(4) The gate-source capacitance C_{GS} mainly determines the switching delays and the drain current slew rate. It does not influence the parasitic ringing too much either.

6.4 Quantification of the Parametric Study

To evaluate the effects of the parasitics, the parametric study has also been conducted in terms of device stress, switching energy, and EMI noise.

6.4.1 Effects on Device Stresses

Figure 6-22 summarizes the V_{DS} and I_D overshoots under different parasitic impedances, in 400 V, 10 A switching condition, with 15 Ω gate resistance.

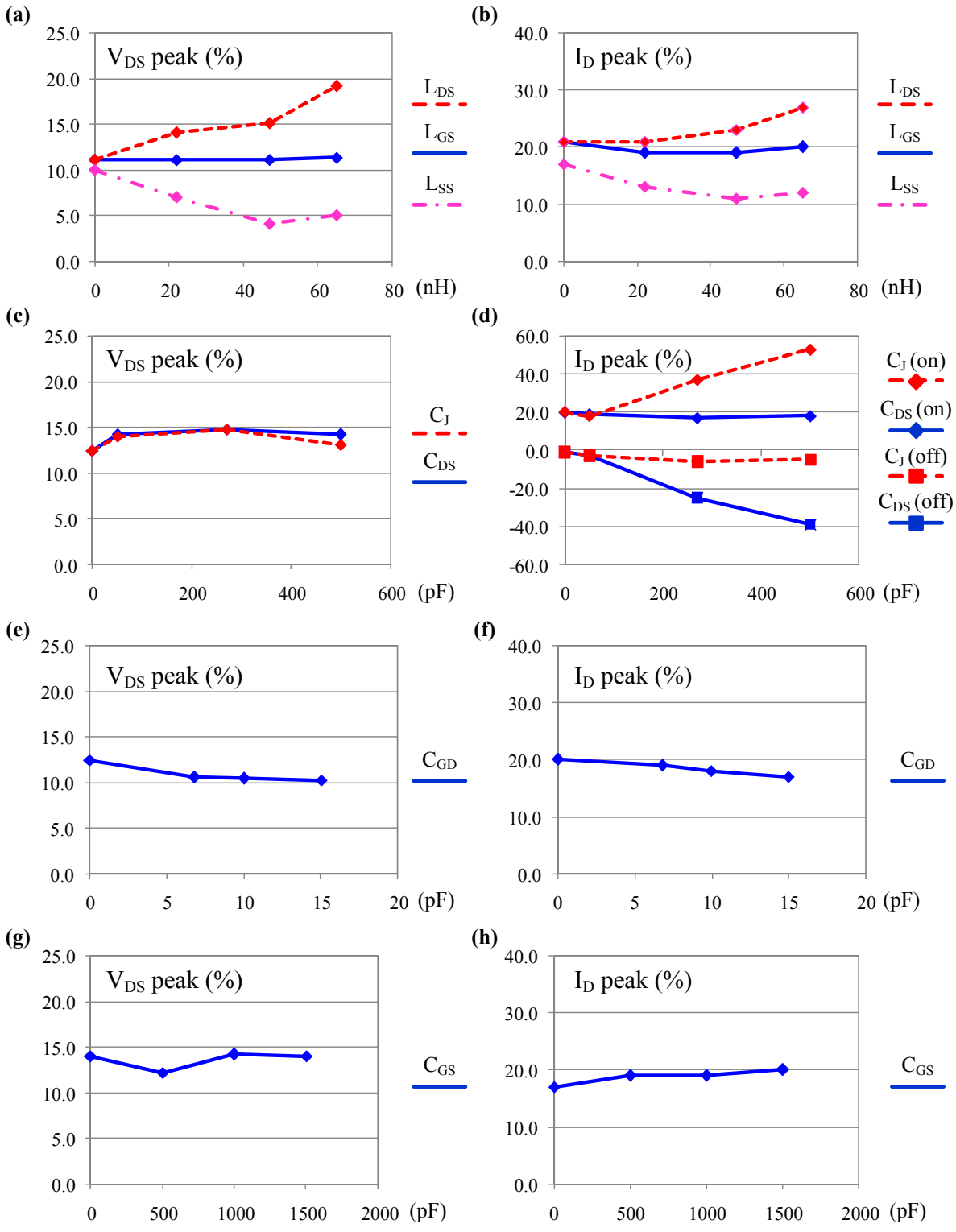

Figure 6-22. Parasitic effect on device stresses. 400 V, 10 A, R_G = 15 Ω.

(left) V_{DS} overshoot, (right) I_D overshoot

As seen from Figure 6-22 (a) and (b), the gate loop inductance has only a minor effect on the MOSFET switching waveforms. Both voltage and current overshoots basically remain unchanged in this case. The switching loop inductance on the other hand increases both overshoots. Comparing the condition where both L_{DS} and L_{GS} are 65 nH, the V_{DS} overshoot for the former case is greater by about 8 % and I_D overshoot by 7 %. Note that in this comparison R_G = 15 Ω. For even faster switching speed the difference would be further exacerbated. The common source inductance L_{SS}, as discussed, relieves the device stresses by slowing down the switching, which is also apparent from the figure.

The MOSFET C_{DS} and freewheeling diode C_J basically do not worsen the voltage stress, however they mainly cause drain current oscillations with C_{DS} being the major contributor to the turn-off ringing and C_J being the critical one to the turn-on overshoot, as seen from Figure 6-22 (c) and (d). (e) and (f) show that bigger Miller capacitance C_{GD} relieves both voltage and current stresses by slowing down the V_{DS} waveform, which is consistent with the previous analysis. The gate-source capacitance C_{GS}, however, does not have direct impact on the device stresses, as it can be seen from (g) to (h).

6.4.2 Switching Energy and Loss

Figure 6-23 shows the parasitic effect on the switching energy E_{on} and E_{off}, and the total switching loss $E_{tot} = E_{on} + E_{off}$. As seen in Figure 6-23 (a), the increase in L_{GS} and L_{DS} almost do not affect the switching energy, despite of the more severe ringing observed in the waveforms. This is verified by inspecting the instant power waveform of the MOSFET ($I_D \cdot V_{DS}$), which appears to be purely decaying reactive due to the almost 90° shifted V_{DS} and I_D ringing waveforms. A close scrutiny of (a) also tells that L_{DS} reduces the turn-on energy a little bit due to its snubber effect, and does the opposite to

E_{off} because of higher V_{DS} overshoot. The overall loss, however, is almost unchanged. Figure 6-23 (b) displays the influence of L_{SS}, which as stated above significantly increases the switching energy due to its negative feedback nature. In effect, the total switching loss when L_{SS} = 65 nH is over four times bigger than E_{tot} under the same value of L_{DS}.

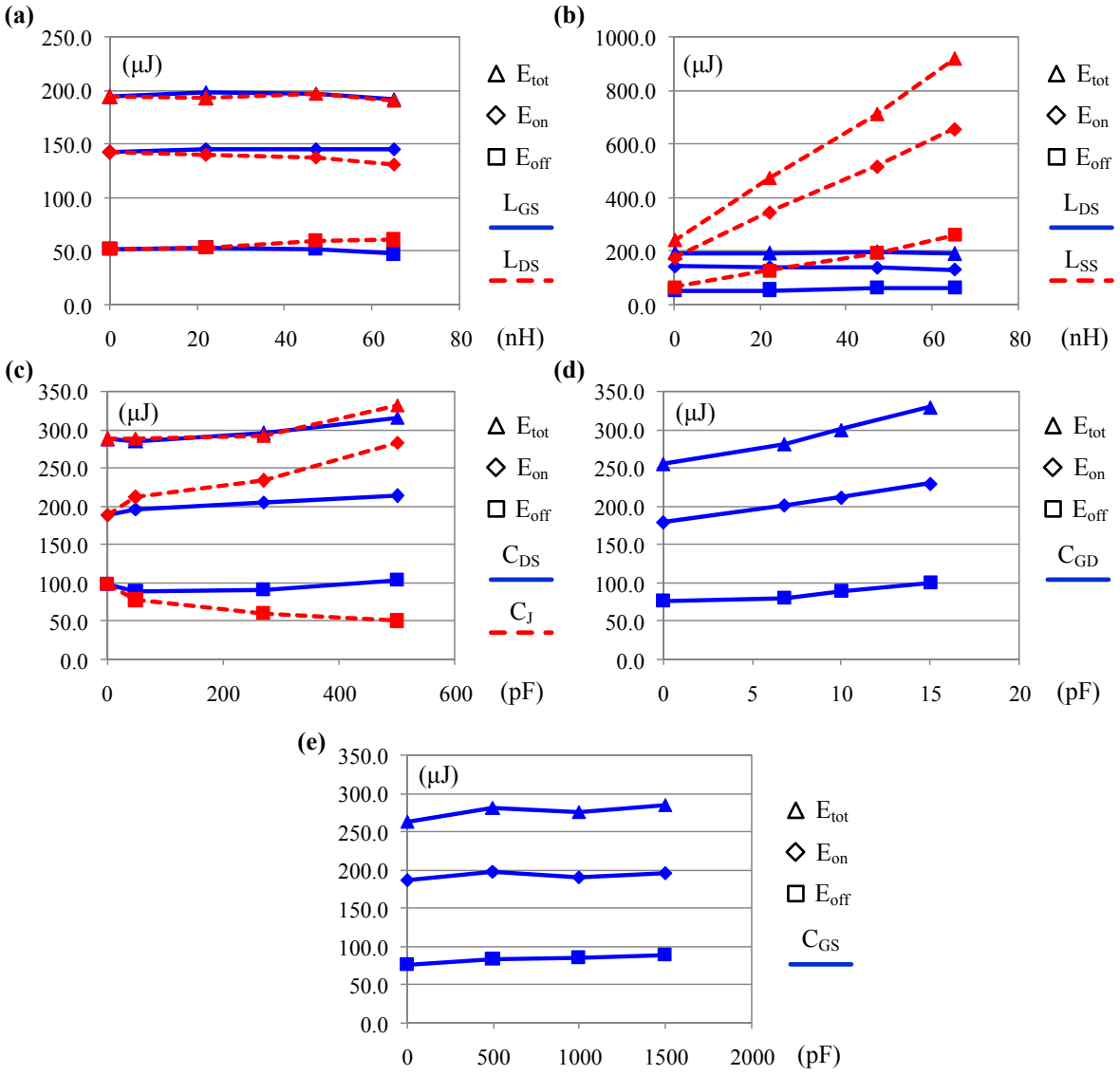

Figure 6-23. Parasitic effect on switching energy. 400 V, 10 A, R_G = 15 Ω.

In Figure 6-23 (c), it can be seen that bigger C_J increases the turn-on energy due to its discharging current that adds to the load current, and decreases the turn-off energy as it draws the load current to charge itself. The overall effect is to increase the total loss. On the other hand, adding more C_{DS} increases both switching energies and the total switching loss, which seemingly conflicts with the common knowledge that adding more drain-source capacitance can help reduce the switching loss. This will be discussed later.

Figure 6-23 (d) and (e) clearly tell that both C_{GD} and C_{GS} tend to increase the switching energy and total loss as they become bigger. It is also obvious that the switching loss is much more sensitive to C_{GD} than C_{GS}.

6.4.3 EMI Noise

Finally, to study the impact of the parasitic ringing on the EMI noise, the common-mode (CM) current on the DC bus of the double-pulse tester is also measured. Figure 6-24 displays the spectrum of this current during MOSFET turn-off transients, under L_{DS} = 0 nH and L_{DS} = 65 nH conditions respectively. As seen, the high-frequency oscillation caused by this inductance is also coupled to the DC bus CM current, whose spectrum rises by around 5 to 10 dBmA at 60 to 90 MHz – the range of the ringing frequency, indicating potentially higher EMI radiation.

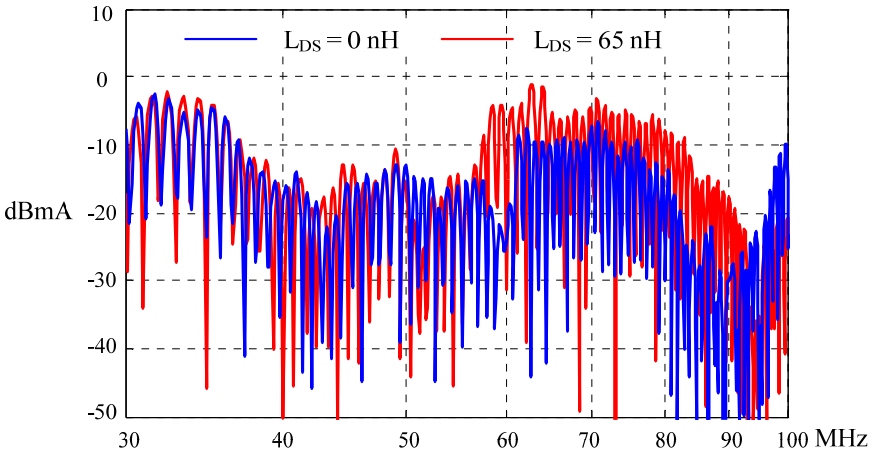

Figure 6-24. Spectrum of DC bus CM current. 400 V, 10 A, R_G = 7.5 Ω.

6.5 Effect of MOSFET Drain-Source Capacitance C_{DS}

From Figure 6-11 it can be seen that C_{DS} mainly modifies the drain-source voltage slew rate, but does not affect the di/dt of the drain current. This is intuitive because larger C_{DS} will need more time to be charged or discharged between zero and full bus voltage, thus causing both turn-on and turn-off energy to increase since they are calculated by $\int I_D V_{DS} dt$.

However, this seems to be conflicting with the common practice of paralleling external drain-source capacitances to reduce the turn-off loss. As a matter of fact, the seeming conflict originates from the way of current measurement and the definition of "switching loss". As illustrated in Figure 2-11, the existence of MOSFET C_{DS} tends to make the drain current I_D measured outside the device deviate from the real channel current $I_{channel}$. Therefore, the real switching loss should be evaluated as $\int I_{channel} V_{DS} dt$ instead of $\int I_D V_{DS} dt$. During turn-off, C_{DS} draws part of the load current to charge itself, which makes $I_{channel} < I_D$, and correspondingly $\int I_{channel} V_{DS} dt < \int I_D V_{DS} dt$. As C_{DS}

increases, more current from the load goes to charge the capacitance instead of flowing through the channel. Thus, $\int I_{channel} V_{DS} dt$ decreases although from the outside $\int I_D V_{DS} dt$ seems bigger. For the turn-on transients the process is just the opposite: the C_{DS} discharging current makes $\int I_{channel} V_{DS} dt > \int I_D V_{DS} dt$. In this sense, the expression of $\int I_D V_{DS} dt$ can only be called "switching energy" as it does not represent the real turn-on or turn-off loss.

The following simulation shown in Figure 6-25 further reveals the current distribution between the MOSFET channel and C_{DS}. In the simulation a 5 nF external linear capacitance is paralleled to the drain-source terminals of the MOSFET. It can be clearly seen from the figure how much difference C_{DS} has caused between the measured drain current and the lossy channel current.

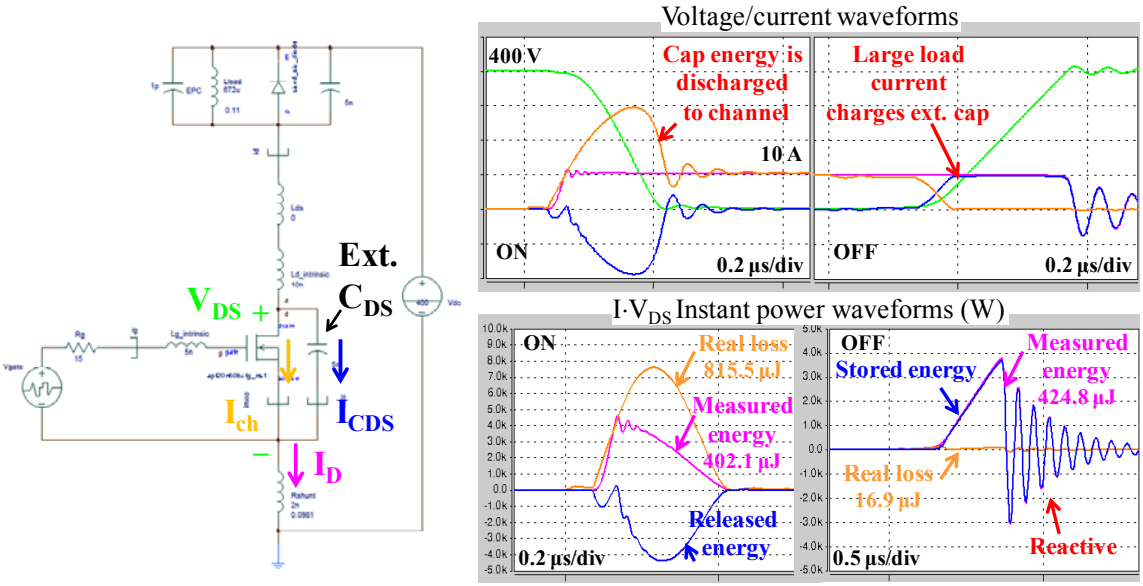

Figure 6-25. Simulation showing the effect of C_{DS}.

The following conclusions can be reached based on the above simulation:

(1) Under the clamped inductive load, increasing C_{DS} increases both turn-on and turn-off energy, although the real turn-on loss is increased and the turn-off loss is reduced.

(2) If adding the measured switching energies together (402.1 + 424.8 = 826.9 μJ) and comparing with the sum of the real loss (815.5 + 16.9 = 832.4 μJ), one can find that they are almost equal. This means although E_{on} and E_{off} do not represent the real loss, the sum of them is still the overall switching loss in one switching cycle.

(3) The I_D and V_{DS} ringing results in purely reactive power which does not cause any extra loss for the MOSFET.

The conflict is thus resolved: the external C_{DS} does reduce the turn-off loss by converting the load current to the stored energy, as long as this energy is not dissipated in the MOSFET channel during turn-on. This is true for the commonly implemented R-C-D snubber circuit where the stored energy is dissipated through the external resistor; and for the zero-voltage-switching operation where the energy is used to charge / discharge the inductor. However, if C_{DS} is internal to the MOSFET, or in another word, if the MOSFET has very big junction capacitance, the overall switching loss always increases for hard-switching operation, because the energy stored in C_{DS} can only be dissipated in the channel. The bigger C_{DS}, the bigger loss.

6.6 Conclusions

This chapter has systematically studied the impact of the parasitic impedances on the MOSFET switching behavior. From the parametric study results, the following conclusions can be reached:

(1) The parasitic ringing during the fast switching transients is mainly caused by the switching loop inductance L_{DS} resonating with the MOSFET drain-source capacitance C_{DS}.

(2) The parasitic ringing worsens the device stresses and EMI radiation, but does not significantly increase the switching loss.

(3) The common source inductance L_{SS} and the MOSFET Miller capacitance C_{GD} are the two critical factors that impact the switching speed and loss, and thus must be kept as small as possible.

(4) The measured switching energy E_{on} and E_{off} do not represent the real losses. However, the sum of E_{on} and E_{off} does represent the real switching loss in one switching cycle.

6.7 References

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Chapter 7 Conclusions and Future Work

7.1 Conclusions

This thesis systematically studies the static and switching characteristics of two SiC active unipolar devices: SiC JFET and SiC MOSFET. Characterization methods and procedures have been introduced in detail. Issues in the respective characterization process have also been explored and discussed. Many of the characterization procedures presented are generic, so that they can be applied to the study of any future SiC JFETs or MOSFETs.

Based on the characterization data, device models have also been built for the two SiC switches. Considerations and measures about model improvement have also been investigated and discussed. Both models have been verified by comparing simulation waveforms with the experimental results. Model limitations have been explained as well.

A modeling methodology has also been proposed in the thesis to predict the switching waveforms of SiC MOSFET through the device-package combined simulation, where the detailed parasitic ringing during the switching transients can be reproduced accurately. Furthermore, based on the analyses on the parasitic impedances, the origin and mechanism of the parasitic ringing has also been clearly explained.

Based on the study presented from Chapter 2 to Chapter 6, the following conclusions can be reached.

7.1.1 SiC JFET vs. SiC MOSFET

In terms of device characteristics, SiC JFET still represents the most mature technology among all SiC devices presently, and is the only device that is reported to operate reliably beyond 150 °C. SiC JFET can also be switched very fast, as the 1.2 kV, 5 A prototype studied in this work can achieve a maximum dv/dt up to 60 kV/μs and a di/dt up to 3 kA/μs, without suffering from severe parasitic ringing. The only disadvantage, however, is its normally-on feature, which is not that desirable in terms of the protection of converter failures.

The advantages of SiC JFET are also the shortcomings of SiC MOSFET. Presently the manufacturer recommended maximum junction temperature for SiC MOSFET is still constrained at 150 °C. Besides, current SiC MOSFET still faces degradation and reliability issues which is a big barrier in its way to commercialization. Bigger junction capacitances of the 1.2 kV, 20 A SiC MOSFET studied in this thesis also make it slower (with dv/dt up to 20 kV/μs and di/dt up to 2 kA/μs) compared to the SiC JFET and suffer more parasitic ringing. However, this does not necessarily say that SiC MOSFET is slower than SiC JFET in general because the two devices under study are not equally rated, and the comparison will not be fair. Even though, SiC MOSFET is still a great leap among normally-off devices, as it easily doubles the blocking capability of Si MOSFET with even reduced on-state resistance, and significantly surpasses the switching speed of Si IGBT. Thus, the future of SiC MOSFET is still quite promising.

7.1.2 Design Guidelines for High-Speed Switching Circuits

From the parametric study and analyses presented in Chapter 6, the following statement can be made:

For a certain device with certain die size (and hence certain junction capacitances), and for a particular packaging technology (such as discrete packaging, e.g. TO-2xx), there is a limit in the device switching speed defined by the parasitic ringing. Beyond this speed, any benefit obtained in the switching loss would be offset by the intolerable device stresses and EMI radiation, due to the excessive parasitic ringing.

Accordingly, the following guidelines can be established for the design of high-speed switching circuits.

As for the device selection:

(1) Always choose a MOSFET with smaller Miller capacitance C_{GD} to achieve faster V_{DS} dv/dt and minimize switching loss.

(2) Always choose a MOSFET with smaller drain-source capacitance C_{DS} to reduce the parasitic ringing, as this is the major capacitance which resonates with the switching loop inductance during the switching transients.

(3) Based on (1) and (2), select device with smaller gate-source capacitance C_{GS} to minimize the gate loop resonance and reduce switching loss.

As for the layout design:

(4) It is of first priority to minimize the switching loop inductance L_{DS} for very high-speed switching circuits. This fact is often overlooked in many publications. This loop is basically compounded by the DC bus, the top freewheeling diode and the bottom MOSFET, which means that the diode should be placed as close as physically possible to

the MOSFET to minimize the loop. This is also true for the top MOSFET and bottom diode in a phase-leg configuration. Furthermore, using DC planes in the PCB and adding necessary decoupling capacitance on the bus can also help reduce this loop and hence the loop inductance.

(5) The gate loop inductance L_{GS} should still be minimized as many have suggested by placing the gate driver as close to the power device as possible. However, its optimization could come after the minimization of L_{DS} as it only weakly affects the main switching waveforms.

(6) The common source inductance L_{SS} essentially represents the coupling effect between the gate-source and drain-source loops. It is also important and necessary to minimize this mutual inductance to reduce the switching loss.

Note that all of the above guidelines may not be applicable at the same time. Trade-off needs to be made on a case-by-case basis.

7.2 Suggestions for Future Work

7.2.1 Quantifying the Switching Speed Limit

The parametric study has explained the mechanism of the parasitic ringing and has identified its origin. Based on the study results, a switching speed limit has also been qualitatively defined for the MOSFET. It is therefore valuable to define this speed limit quantitatively. In another word, it would be very useful to determine the minimum external gate resistance from simple calculations given the device capacitance information and an approximation of the circuit parasitics. To do this it is first necessary to define the speed limit, i.e. above which level the parasitic ringing is intolerable, and

then to establish the relationship between this limit and the parasitic impedances and gate resistance, which may require the analytical solutions of the high-order, non-linear differential equations describing the switching transients.

7.2.2 Modeling the Terminal Behavior of a Phase-Leg

Although the device-package combined simulation successfully reproduces the real switching waveforms, this modeling method is still not quite suitable for high-level converter simulation due to its excessive modeling details about the device and parasitics. It is therefore preferable to develop a behavioral model for the phase-leg – the basic component of a converter, which is more suitable for system-level simulation. This model should only simulate the terminal behavior of the phase-leg, such as the mid-point voltage waveform with correct dv/dt and parasitic ringing, but should not contain any detailed information about the devices used inside. The model may use the controlled voltage / current sources to represent the device I-V characteristics, voltage-dependent nonlinear capacitances to mimic the junction capacitances, and several critical stray inductances, in order to simulate the correct waveforms. The behavioral modeling of phase-leg is especially useful for module manufacturers who want to provide module models to their customers without leaking intellectual properties.

Appendix A Extracting Transfer Characteristics from Switching Waveforms

A.1 Importance of the MOSFET Saturation Region

Two comparisons are made through simulation to shown the importance of fitting the saturation region in the MOSFET modeling. In the first case, a certain MOSFET model with the output characteristics shown as the blue curves in Figure A-1 is used, and based on which another model is built with the linear region of the output characteristics modified so that the channel conductivity is obviously lower, but the saturation region basically remains the same, seen as the magenta curves in the same figure. Other parameters such as junction capacitances remain unchanged for both models.

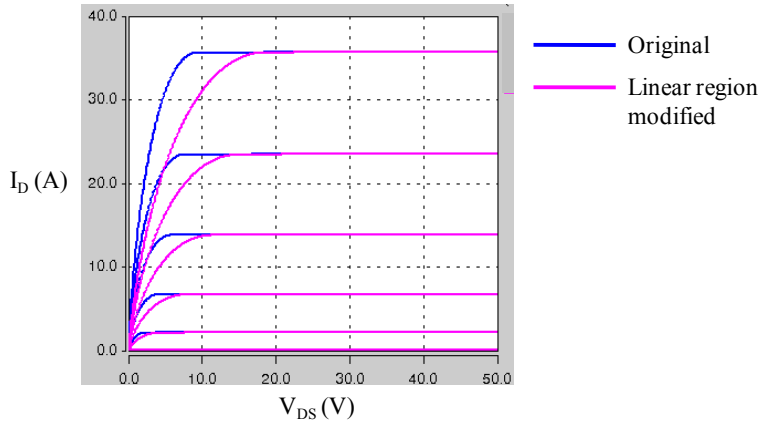

Figure A-1. Output characteristics of the MOSFET models with different linear region

The two models are then simulated in the double-pulse tester circuit in Saber to see the effect of the linear region. As shown in Figure A-2, the switching waveforms of the two models almost overlap, indicating that the linear region discrepancy does not influence the switching waveforms greatly.

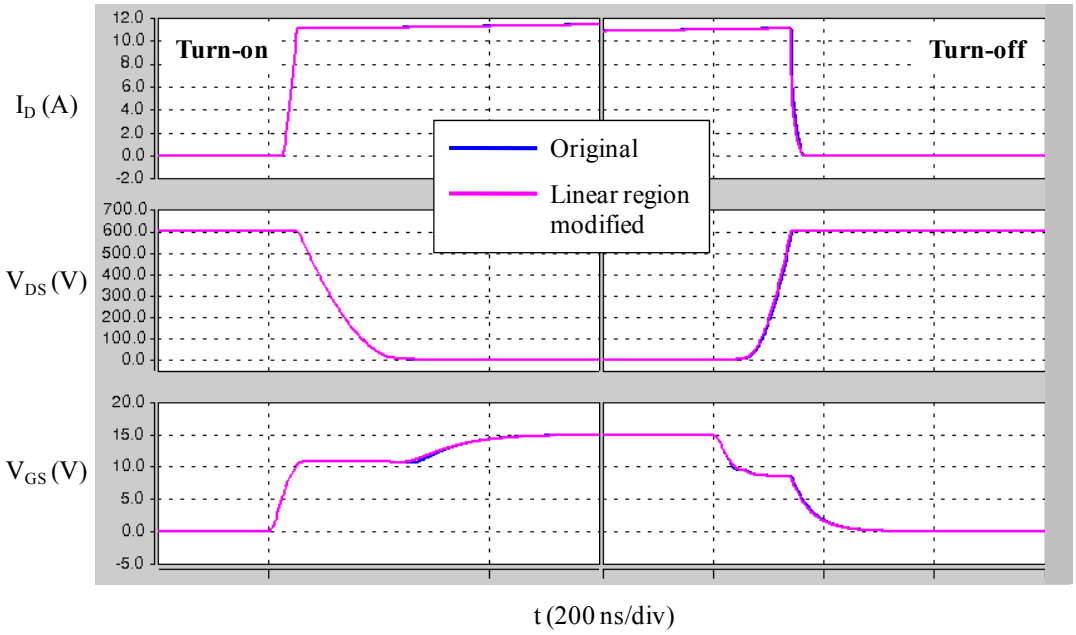

Figure A-2. Switching waveforms of the MOSFET models with different linear region

In the second case, the original MOSFET model (different from the former one) is modified in the saturation region. This time only the channel-length modulation coefficient of the model (LAMBDA) is reduced by half, so that the I-V curves in the saturation region become more flat while the linear region remains unchanged. The simulated switching waveforms are shown in Figure A-3. It is clear from the figure that this time the switching waveforms of the two models are completely different, which says that the saturation region characteristics do have a great impact on the MOSFET switching behavior. Actually this is also intuitive because, according to Chapter 2, most part of the device switching trajectory is in the saturation region during commutation

processes. As long as this region is well captured by the model, the simulated switching waveforms will be more accurate than if only fitting the linear region.

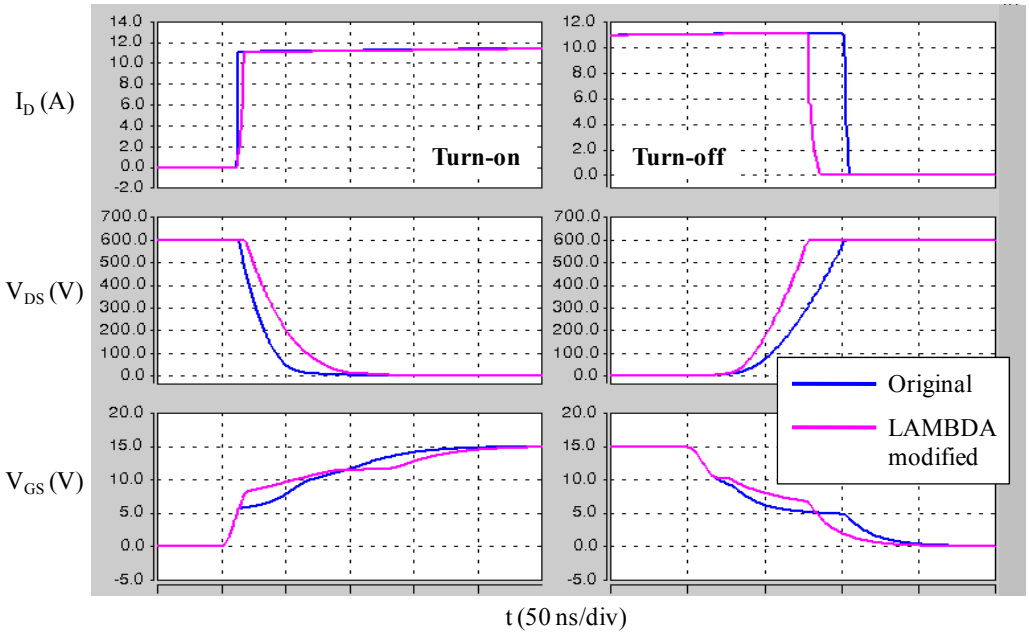

Figure A-3. Switching waveforms of the MOSFET models with different saturation region

A.2 Extracting Transfer Characteristics from Raw Data

The process of the transfer characteristic extraction basically follows Section 4.5.2. However, due to the AD conversion error of the oscilloscope, the I_D vs. V_{GS} graph directly drawn from the experimental waveforms is not smooth, but looks something like Figure A-4. The following steps are adopted in this work to produce the smooth curves as shown in Figure 4-30:

(1) The originally extracted transfer characteristics (Figure A-4, for example) are saved as an image. There are two curves, one for turn-on and one for turn-off.

(2) On this image, draw two smooth curves by hand which go through the original curves. This is an approximate averaging of the raw data which eliminates the AD conversion error.

(3) Digitize the smooth curves on the image into number arrays using image digitizing software such as *Engauge Digitizer*.

(4) Import the number arrays into Matlab and perform the weighted averaging to get the final transfer characteristic.

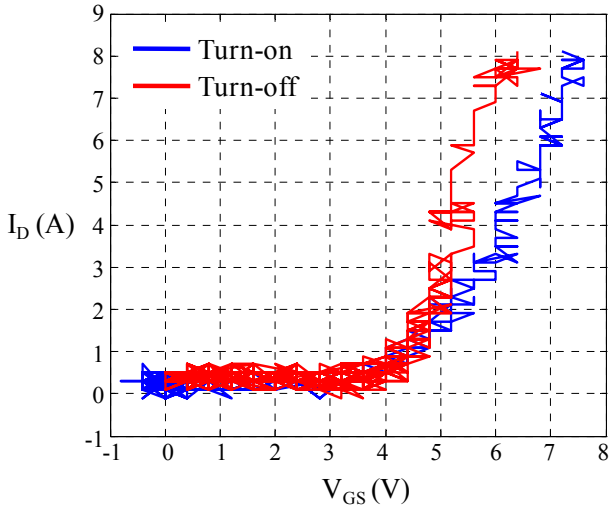

Figure A-4. Transfer characteristics directly drawn from experimental switching waveforms

Appendix B Converting Q3D Results to Saber Templates

This appendix introduces the steps of converting Ansoft Quick 3D Extractor (version 7.1.1) analysis results to Synopsys Saber (version Y2006.06) templates.

(1) Q3D operations:

(i) From the menu, select "Q3D Extractor" → "Analysis Setup" → "Export Circuit", and the "Export Circuit" dialog pops up.

(ii) In this dialog, select the export format to be ".cir" and export the analysis results to a netlist file: *filename*.cir.

(2) Saber operations:

(i) From the menu, select "Tools" → 'Model Architect", and "Model Architect" dialog pops up.

(ii) In this dialog, select from the menu "Tools" → "Nspitos".

(iii) Set the "Nspitos" dialog:

"Select a spice type" → "Pspice";

"Enter input file name" → "*filename*.cir";

"Enter catos file name" → leave blank;

"Hspice Bsim Version" and "Berkeley Bsim Version" → leave blank;

"Input File Type" → "netlist";

"Pin Name Option" → check;

"Hspice Bsim Option" → uncheck;

Finally click "Apply" to get a ".sin" template file.

(3) Modify the .sin file

(i) The .sin file generated in the last step contains three templates: *filename*_ns defines the model of the entire equivalent circuit, which recalls another two templates *filename*__half_ns and *filename*__parlel_ns. *filename*__half_ns defines the series subcircuit of the equivalent circuit, while *filename*__parlel_ns defines the parallel subcircuit (Refer to Q3D Help for equivalent circuit information).

(ii) Save the templates separately as three .sin files because in Saber each .sin file should only correspond to one template. The .sin files should have the same names as the templates, namely *filename*_ns.sin, *filename*__half_ns.sin and *filename*__parlel_ns.sin

(4) Use the .sin files in Saber

(i) Create a new symbol file in Saber Sketch.

(ii) Select from the menu: "Symbol" → "Create" → "Symbol from Model", and select *filename*_ns.sin.

(iii) Edit the symbol if necessary and save.

(iv) Put all the template files and the symbol file in the same folder for simulation.

Some issues that need to be noted:

(1) In Q3D, the default reference point for the capacitance matrix is at infinity. If the circuit has a zero potential point, such as the baseplate of a power module, this point can

be set to the ground by selecting the “Ground Net” from “Reduce Matrix” option. In this way all the calculated capacitances are referenced to this ground point.

(2) In the netlist file generated by Q3D, the ground point is automatically assigned a node reference of “0” and is not declared in the node list. From Saber point of view, this means the equivalent circuit is grounded somewhere in the block but this ground point is not accessible from the outside. If the users want to change the point of grounding, the netlist file should be modified accordingly before it is converted to Saber template.