4. CONTROL OF ZERO-SEQUENCE CURRENT IN PARALLEL THREE-PHASE CURRENT-BIDIRECTIONAL CONVERTERS

4.1 A NOVEL ZERO-SEQUENCE CURRENT CONTROL

4.1.1 Zero-Sequence Dynamics

The parallel boost rectifier model in Figure 2.14 and the parallel voltage source inverter in Figure 2.18 show that the zero-sequence dynamics are governed by their z channels. It is interesting to note that both models have the same z channel equivalent circuit except for the current direction. Since

$$\Delta d_z \cdot v_{dc} = (v_{a1} + v_{b1} + v_{c1}) - (v_{a2} + v_{b2} + v_{c2}), \tag{4.1}$$

the zero-sequence current is determined by the difference in their common-mode voltages For a single converter, the common-mode voltage does not cause any zero-sequence current because physically there is no such current path. The z channel is actually an open circuit. Besides, the common-mode voltage does not affect the converter control objectives, such as voltage regulation and current control. Therefore, the z channel is normally not considered in the control design for a single converter.

When the two converters are in parallel, the zero-sequence current path is formed. A small difference between the two common-mode voltages may cause a large zero-sequence circulating current, because the z channel is an undamped circuit with only inductors, and their ESRs in practical cases. Figure 4.1 shows the z channel model of the parallel boost rectifier system. The current direction is counter clockwise for the parallel voltage source inverter system.

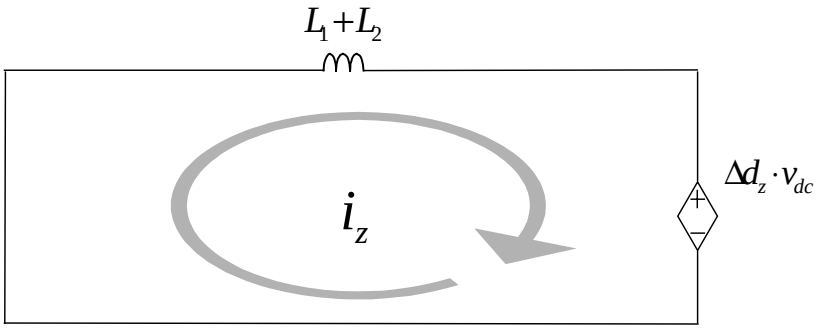


Figure 4.1 Zero-sequence dynamics model of parallel boost rectifiers.

4.1.2 A New Control Variable

In the modulation of the switching network for the three-phase converters, a space-vector modulation (SVM) technique is commonly used, for example, [11], [24], [57]. Figure 4.2 shows that the reference vector is in sector I. It can be synthesized by the vectors pnn and ppn, and their duty cycles d_1 and d_2 can be obtained by projecting the reference vector onto the two vectors, as described in Figure 4.2. The duty cycle of the zero vector is:

$$d_0 = 1 - d_1 - d_2 . \tag{4.2}$$

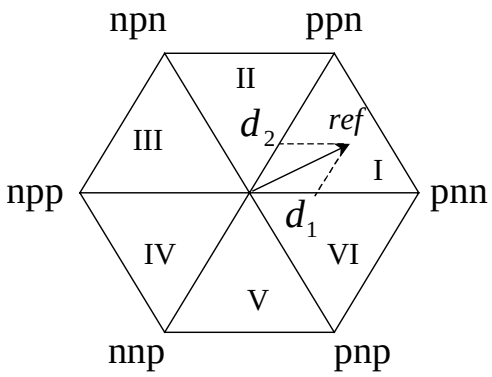


Figure 4.2 Space-vector modulation in three-phase current-bidirectional converters.

To optimize switching losses, total harmonics distortion and maximum modulation index, different SVM schemes produce different triple harmonics by distributing d_0 differently [54]-[62], thus result in different d_z. For example, Figures 4.3 shows one typical PWM pattern in one switching cycle T. The PWM pattern is so-called minimal-loss PWM, in that only two phase legs switch in one cycle. At every one-sixth AC line

cycle (1/60Hz, for example), one of the phase legs that carries the highest current does not switch.

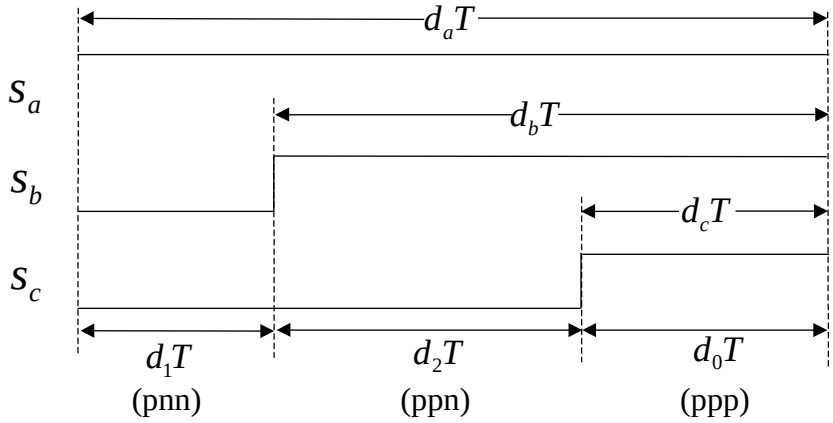


Figure 4.3 Minimal-loss SVM.

With this PWM pattern, the z-channel duty cycle can be calculated:

$$d_z = d_a + d_b + d_c = 1 + (d_2 + d_0) + d_0 = 1 + d_2 + 2d_0 . \qquad (4.3)$$

With this scheme, the phase-leg duty cycles and the duty cycle d_z are shown in Figures 4.4 and 4.5, respectively.

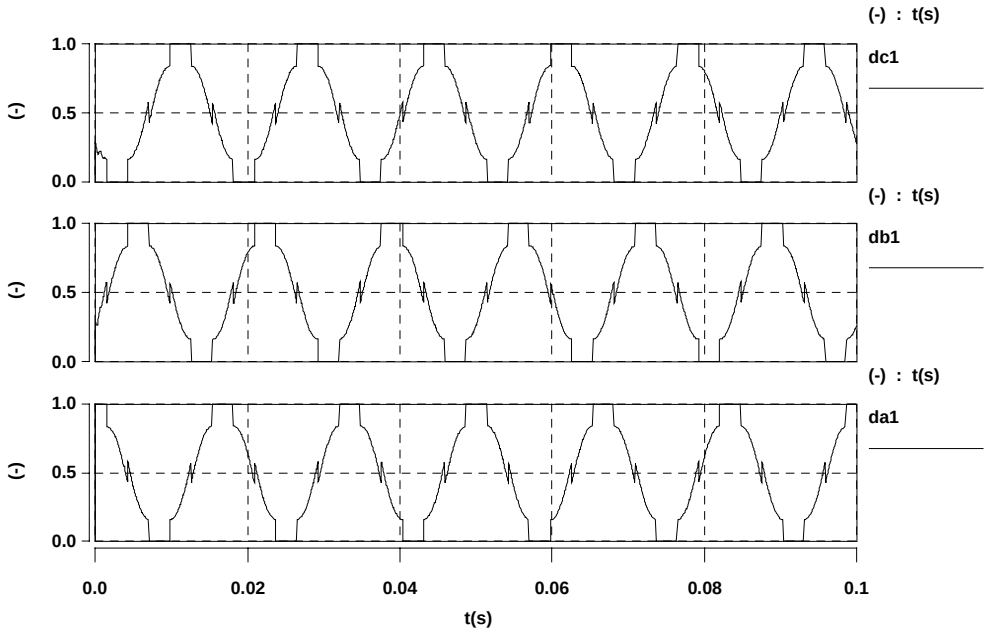


Figure 4.4 Phase-leg duty cycles d_a, d_b and d_c with minimal-loss SVM.

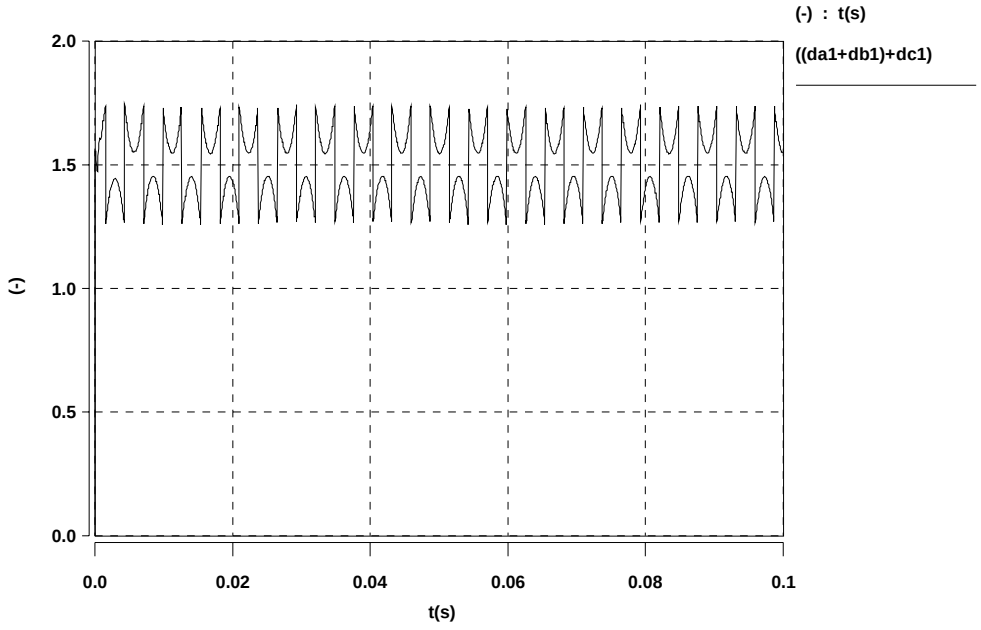


Figure 4.5 Duty cycle d_z with minimal-loss SVM.

Figure 4.6 shows another commonly used PWM pattern with alternating zero vectors.

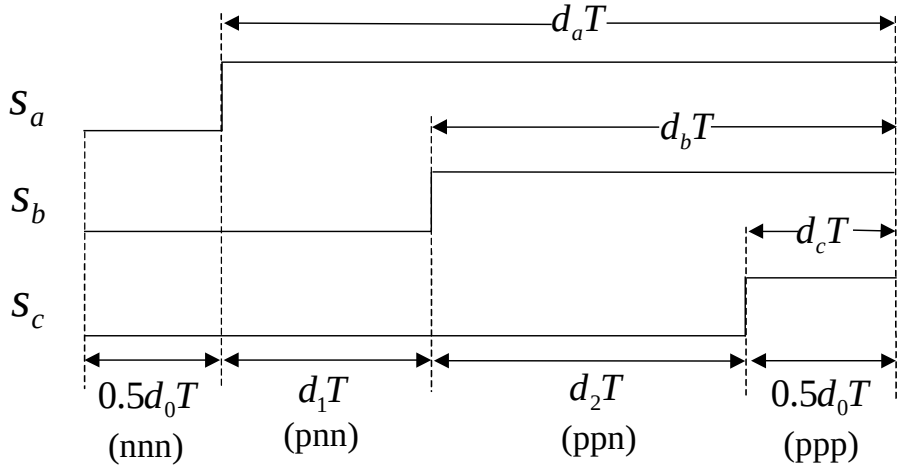


Figure 4.6 Alternating zero-vectors SVM.

With this PWM pattern, the z-channel duty cycle can be calculated:

$$d_z = d_a + d_b + d_c = (d_1 + d_2 + 0.5d_0) + (d_2 + 0.5d_0) + 0.5d_0 = d_1 + 2d_2 + 1.5d_0 \,. \quad (4.4)$$

With this scheme, the phase-leg duty cycles and the duty cycle d_z are shown in Figures 4.7 and 4.8, respectively.

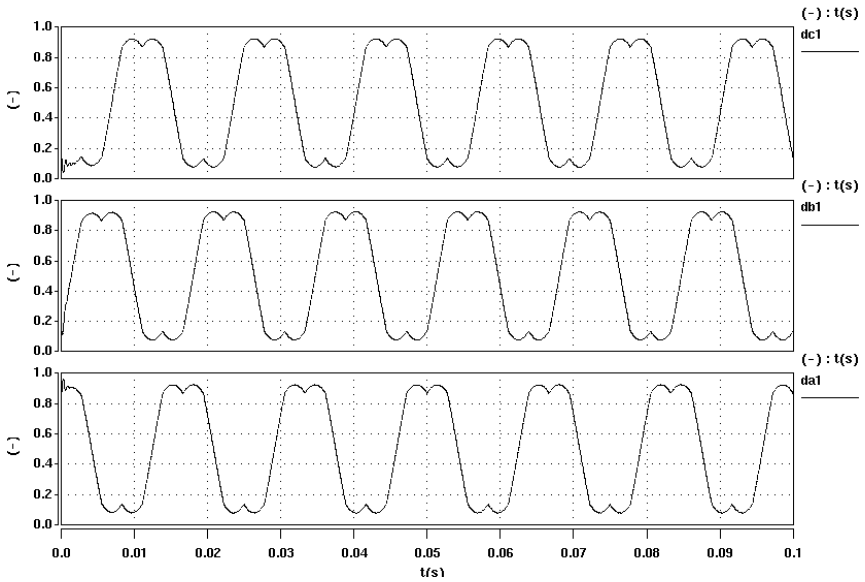


Figure 4.7 Phase-leg duty cycles d_a, d_b and d_c with alternating zero-vectors SVM.

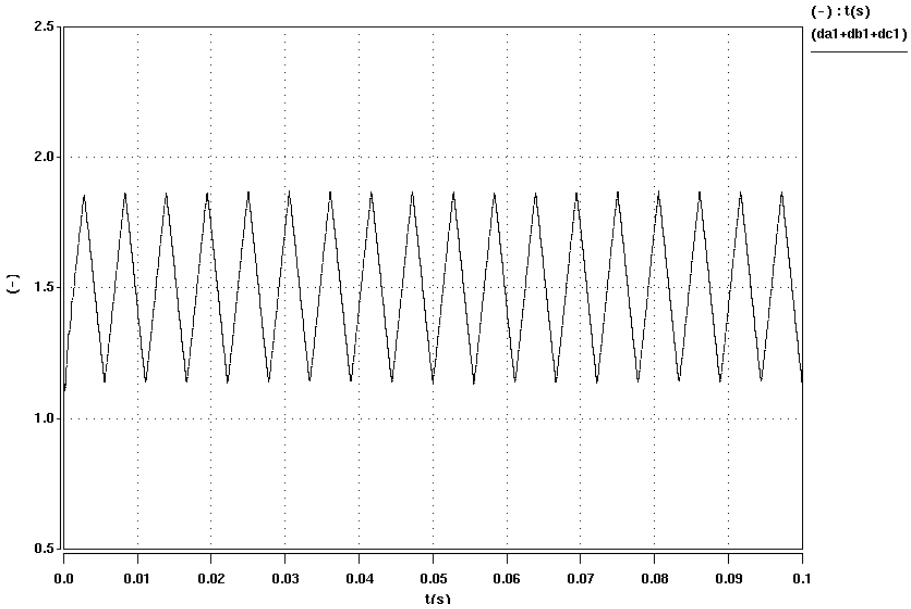


Figure 4.8 Duty cycle d_z with alternating zero-vectors SVM.

Although different schemes have different phase-leg duty cycles, they always have the same phase-to-phase duty cycles, as shown in Figure 4.9. The phase-to-phase duty cycles are used in the phase-to-phase averaging [53].

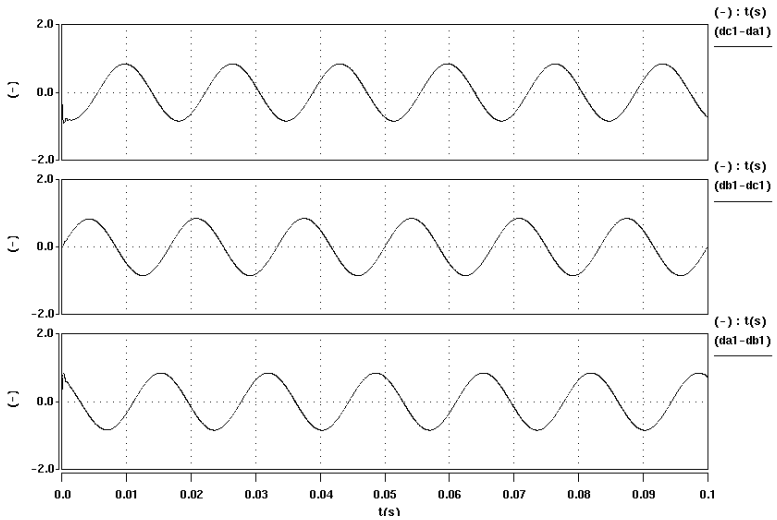


Figure 4.9 Phase-to-phase duty cycles d_{ab}, d_{bc} and d_{ca}.

The distribution of the zero vectors can vary without affecting the phase-to-phase duty cycles and the control objectives, such as the input AC currents and the output DC voltage. This indicates that d_z can be controlled by controlling the distribution of d_0. Based on this fact, a new control variable k is introduced as follows:

$$k = d_{ppp}\,, \tag{4.5}$$

where d_{ppp} is the duty cycle of the zero vector ppp, as illustrated in Figure 4.10.

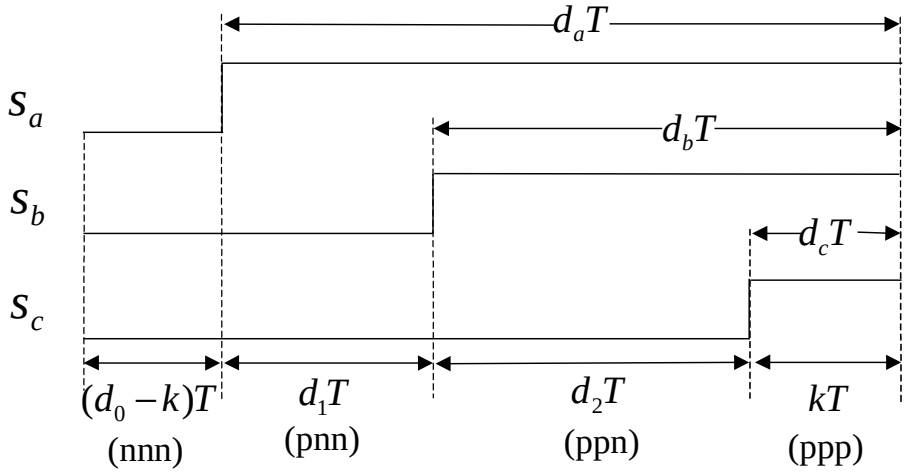


Figure 4.10 New control variable k.

Usually, for the scheme with alternating zero vectors, k=0.5d_0, as shown in Figure 4.6. With the definition in (4.5), d_z becomes

$$d_z = d_a + d_b + d_c = (d_1 + d_2 + k) + (d_2 + k) + k = d_1 + 2d_2 + 3k\,. \tag{4.6}$$

Therefore,

$$\Delta d_z \cdot v_{dc} = ((d_1 + 2d_2 + 3k_1) - (d_1 + 2d_2 + 3k_2)) \cdot v_{dc} = 3(k_1 - k_2) \cdot v_{dc}\,, \quad (4.7)$$

assuming both converters have the same reference vector, thus the same d_1 and d_2.

As a result, the new average model of the zero-sequence dynamic with the new control variable k is shown in Figure 4.11.

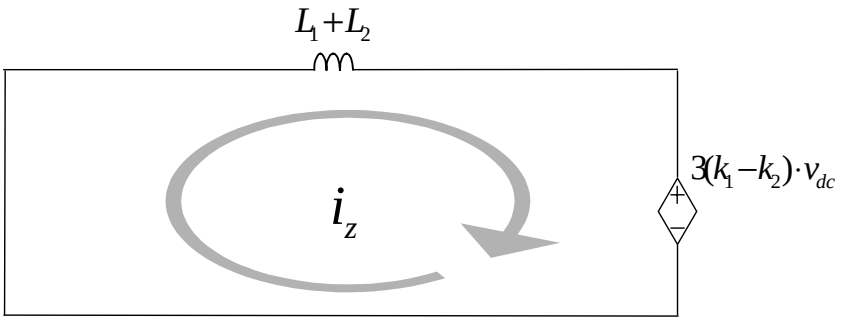


Figure 4.11 Zero-sequence dynamics model with new control variable k.

The definition of the control variable is based on the SVM scheme with alternating zero vectors. The scheme in Figure 4.3 cannot be used for the directly parallel three-phase converters. First of all, the k is always equal to d_0 and not variable. Secondly, the scheme has a discontinuous averaged z-channel duty cycle. The discontinuity causes a strong zero-sequence disturbance to the parallel system [24]. Therefore, the scheme is practically not usable for the directly parallel three-phase converters, although the scheme has less switching losses.

4.1.3 Implementation

Since the z-channel is basically a first-order system, the control bandwidth of the zero-sequence current loop can be designed to be very high, and a strong current loop that suppresses the zero-sequence current can be achieved.

In the design of the single converter with current loops, normally only two current sensors are needed, because the sum of the three phases' currents is always zero. With two converters in parallel, three current sensors are needed in order to measure the zero-sequence current. Figures 4.12 and 4.13 show the implementation of the zero-sequence current control for a two-parallel three-phase boost rectifier system and a two-parallel voltage source inverter system. In a two-parallel converter system, it is sufficient to

control the zero-sequence current in one of the two converters since there is only one zero-sequence current.

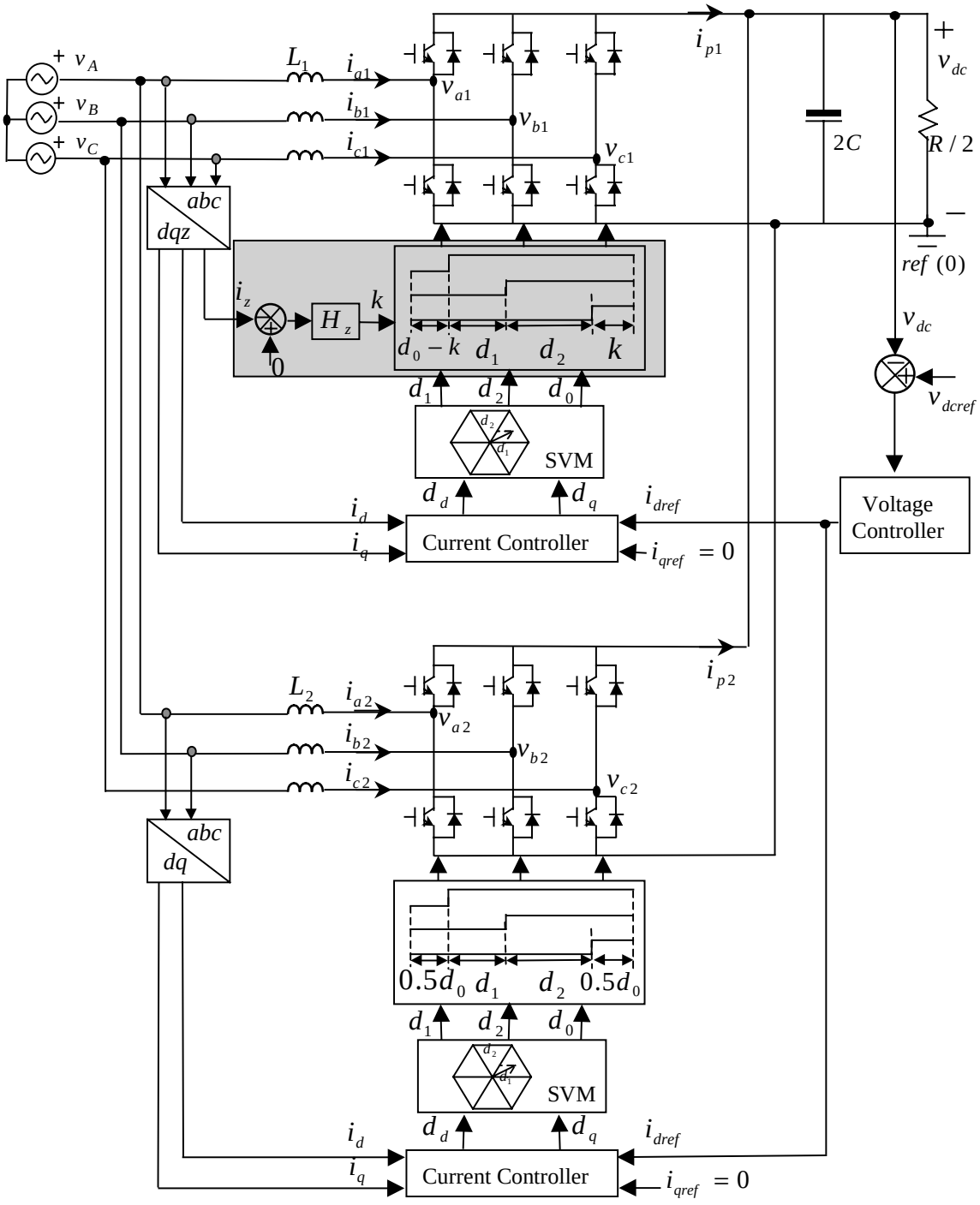


Figure 4.12 Control implementation for parallel boost rectifiers.

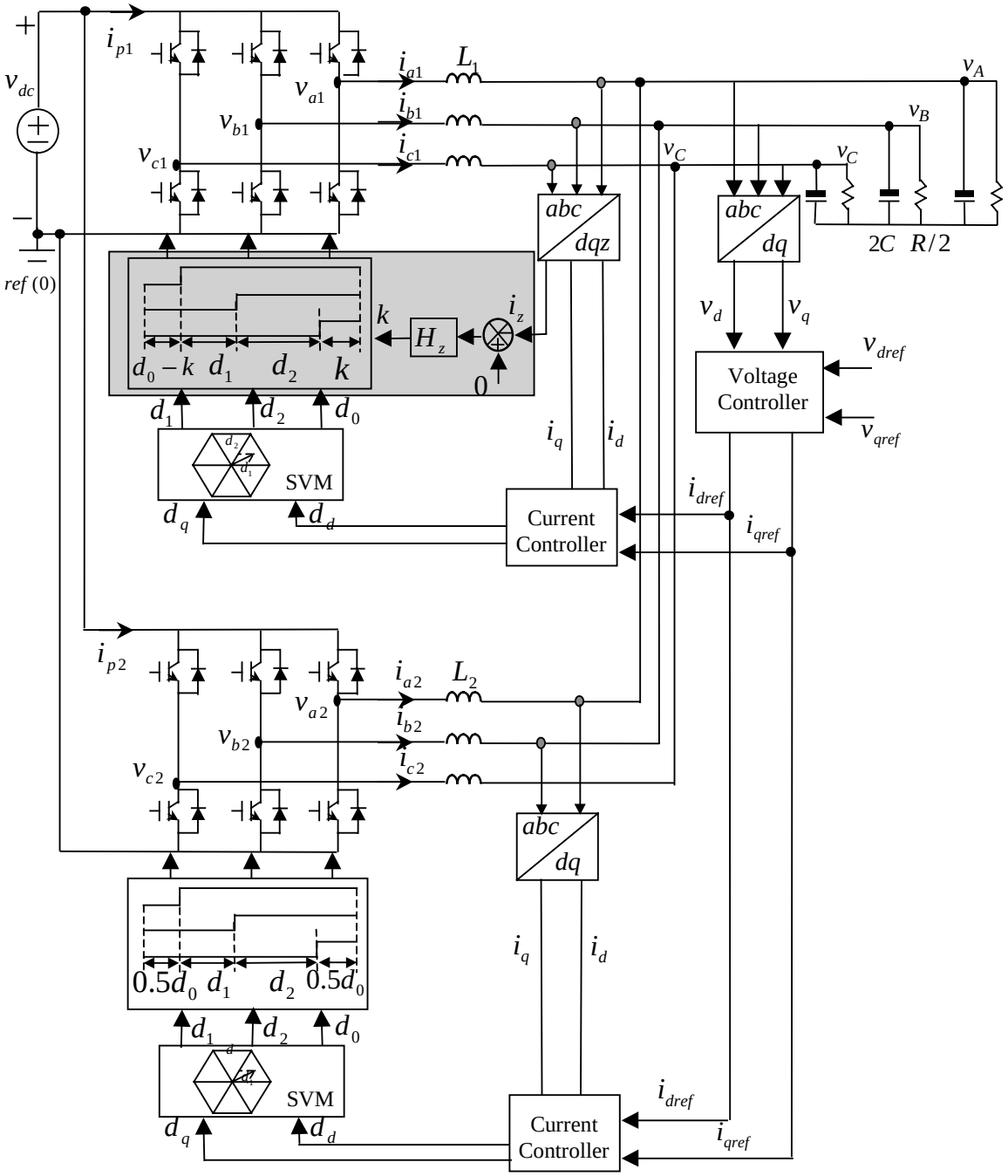


Figure 4.13 Control implementation for parallel voltage-source inverters.

The converter 2 in Figures 4.12 and 4.13 has the same control design as that used for a single converter, which normally has d and q channels current loops. Besides the regular d and q channel control, the converter 1 in Figures 4.12 and 4.13 has a zero-sequence current controller shaded with a rectangle. The zero-sequence current control part is added onto the regular control for a single converter. Since it is implemented

within the individual converter and does not need any additional interconnected circuitry, it allows modular design.

4.2 SIMULATION AND EXPERIMENTAL RESULTS

To demonstrate the concept presented in the previous sections, a parallel three-phase rectifier system is chosen as an example. Both the average and switching models were built in SABER simulator. The average model is not only used for the control design, but it is also much more efficient in simulation than the switching model, which is sometime difficult to converge for such a discrete high-order system.

A breadboard system of a two-parallel three-phase boost rectifier system was built. A preliminary experiment was conducted to validate the zero-sequence control concept.

4.2.1 Simulation Results

The parameters of the simulation model are described below:

$V_{rms(a,b,c)} = 120\,\text{V};\quad \omega = 2\pi \cdot 60\,\text{rad/s};\quad V_{dc} = 400\,\text{V};\quad P_o = 0 \sim 15\text{kW};\quad L_{1,2} = 250\mu\text{H};$

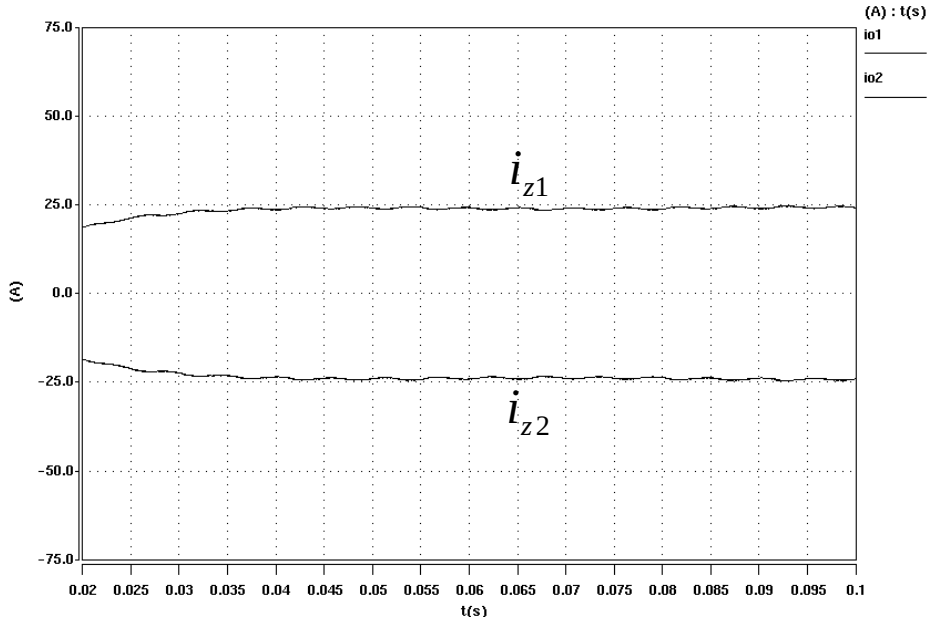
$ESR_{L_1,2} = 45m\Omega \qquad C_{1,2} = 1200\mu\text{F},\qquad ESR_{C_1,2} = 50m\Omega,\qquad f_{sw1} = 32k\text{Hz},\qquad f_{sw1} = 16k\text{Hz},$

$H_{id1,2} = \frac{-2}{2\pi \cdot 160} + \frac{-2}{s},\ H_{iq1,2} = \frac{-2}{2\pi \cdot 160} + \frac{-2}{s},\ H_v = \frac{500}{2\pi \cdot 50} + \frac{500}{s}.$

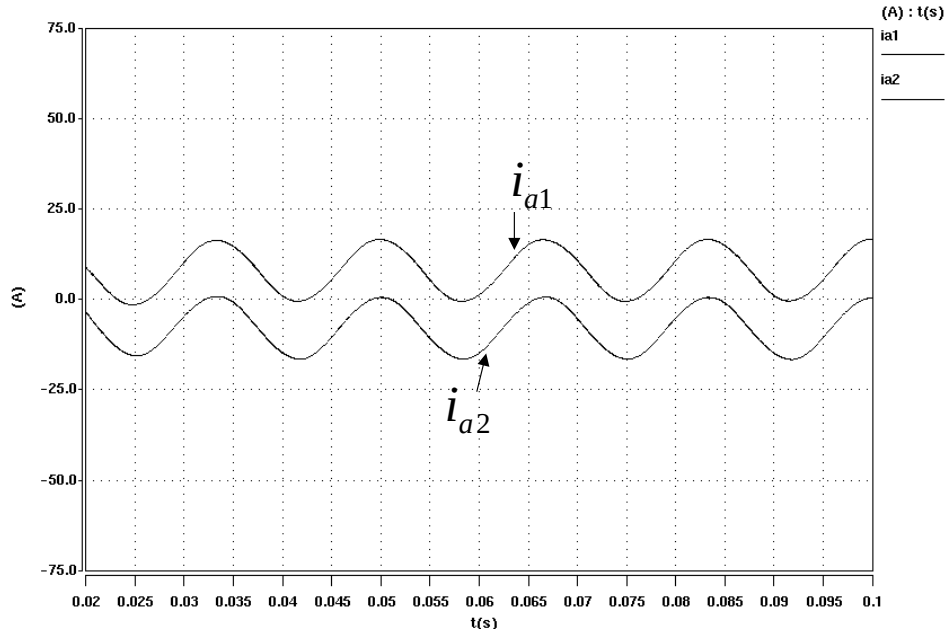
First of all, the system was simulated without the zero-sequence current control. It was demonstrated that any discrepancies between the two parallel converters (for example, different switching frequencies, different power stage parameters or different switching deadtime, all of these cases were simulated) may cause a large circulating current.

A previous research proposed to use an SVM without zero vectors to avoid the zero-sequence current [24]. However, since it is not a feedback control, the zero-sequence current can be avoided only if the two converters are identical. If there is even a small difference, a large zero-sequence current still could occur. Figure 4.14 illustrates the example that both converters use the SVM without zero vectors. The only difference between the two converters is that there is a small deadtime difference (one is 0.1μs, and

the other is 0.1μs). The deadtime difference causes a DC offset in their common-mode voltage $\Delta d_z \cdot v_{dc}$. As a result, a zero-sequence current with a DC offset exists in the parallel system. Figure 4.14(a) shows the zero-sequence current. As a consequence, Figure 4.14(b) shows that the phase currents also have a DC offset.



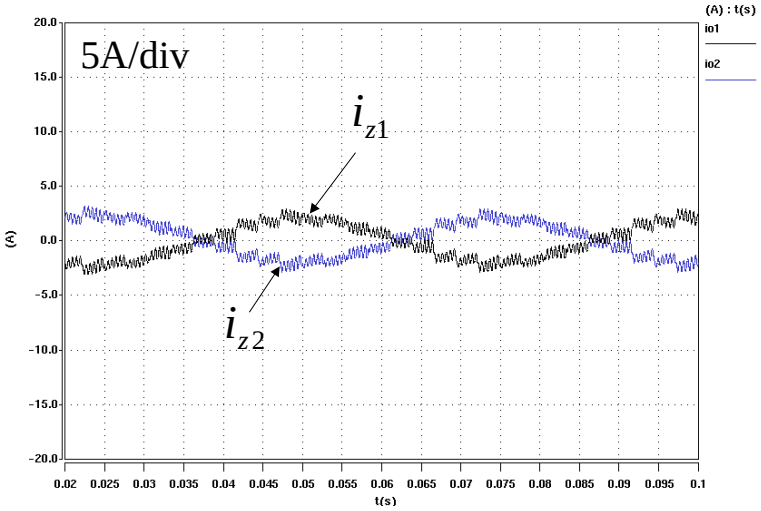
(a) Zero-sequence currents.



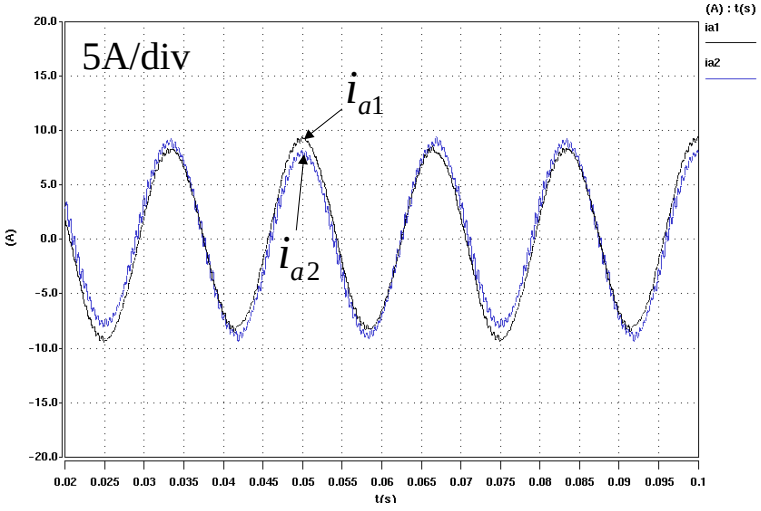
(b) Input phase currents.

Figure 4.14 Average model simulation using SVM without zero-vectors.

Figure 4.15 shows another case, in which the two rectifiers have different switching frequencies (one is 32 kHz and the other is 16 kHz). Figure 4.15(a) shows that a significant low-frequency circulating current exists in the system. The currents i_{z1} and i_{z2} are zero-sequence currents for the boost rectifiers 1 and 2, respectively. The circulating current causes distorted input line currents i_{a1} and i_{a2}, as shown in Figure 4.15(b). The circulating current has both low- and high-frequency components. The high-frequency one is basically a beat-frequency component caused by the two switching frequencies 16kHz and 32kHz.



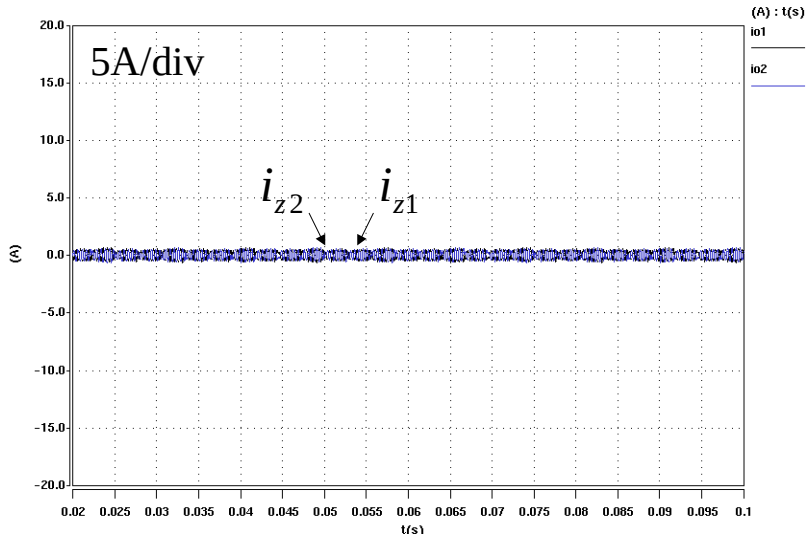
(a) Zero-sequence currents.



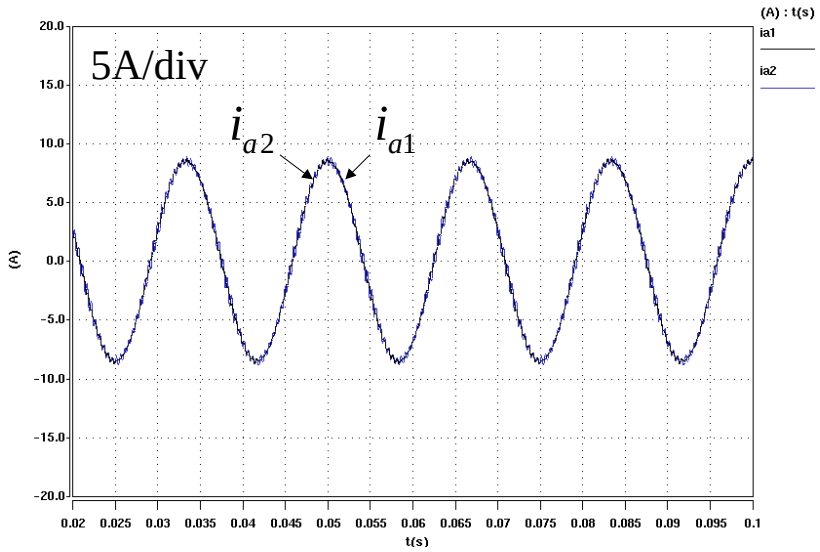
(b) Input phase currents.

Figure 4.15 Average model simulation without zero-sequence current control (fsw1=32 kHz, fsw2=16 kHz).

By applying the zero-sequence current control, the waveforms in Figure 4.16 show that the circulating current is almost gone. Only high-frequency current ripples still exist, and they can be attenuated by filters.



(a) Zero-sequence currents.



(b) Input phase currents.

Figure 4.16 Average model simulation with zero-sequence current control (fsw1=32 kHz, fsw2=16 kHz).

Figure 4.17 shows the simulation results using the switching model without the zero-sequence current control. Figure 4.18 shows the simulation results using the switching model with the zero-sequence current control.

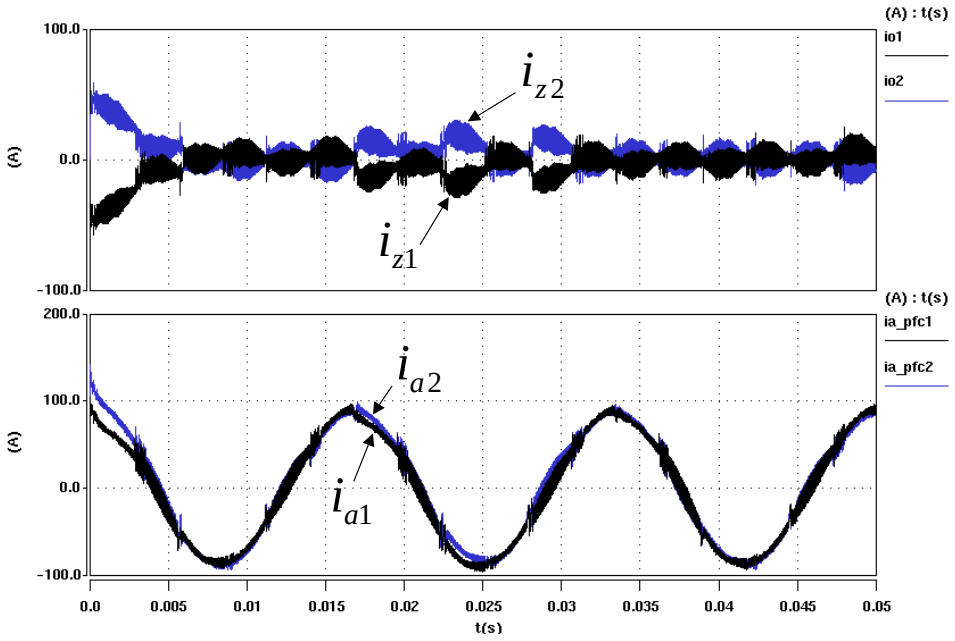


Figure 4.17 Switch model simulation without zero-sequence current control.

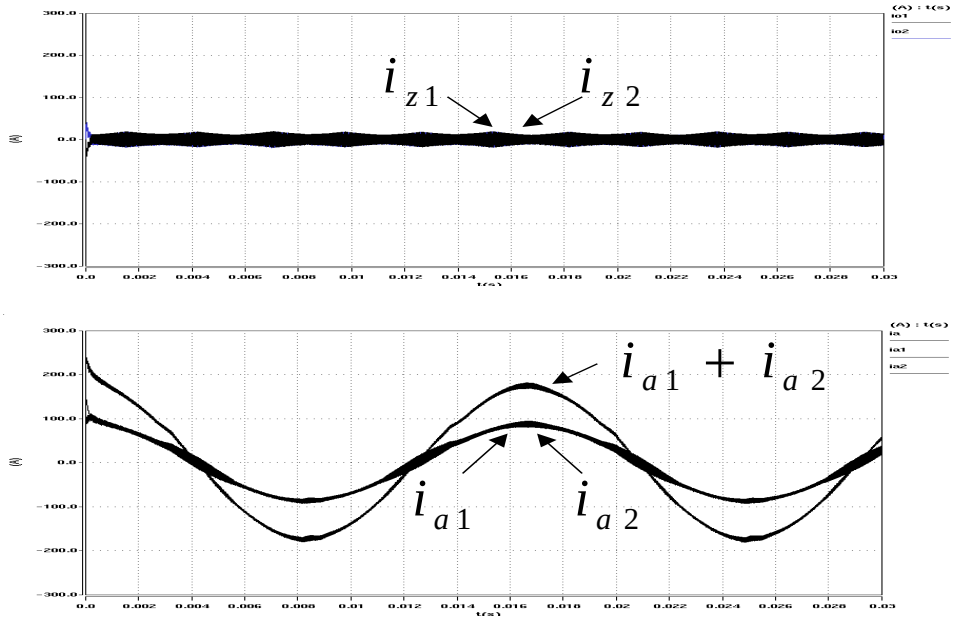


Figure 4.18 Switch model simulation with zero-sequence current control.

4.2.2 Experimental Results

A two-parallel, three-phase boost rectifier breadboard system was built and tested. The experiment setup can be referred in [24], [82]. Some parameters are shown below:

Input voltage: 3Φ, $V_{l\text{-}l}$=208V;

Output voltage: V_{dc}=400V;

Rated power: 15kW/converter;

Switching frequency: f_{sw1}=31.2kHz, f_{sw2}=15.6kHz;

Input inductor: 256μH;

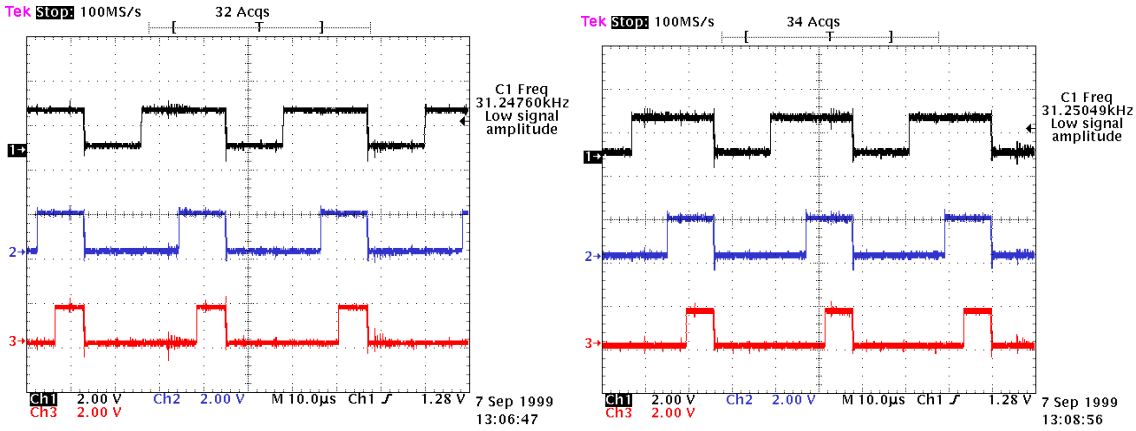
Output capacitor: 1200μF;

IGBT modules: TOSHIBA MG 150J2YS50;

DSP: ADSP2101.

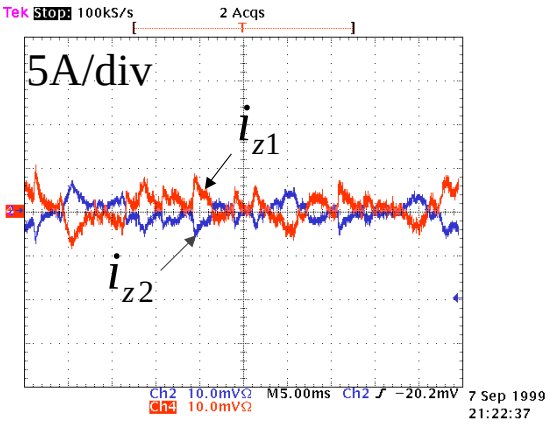
In order to implement the zero-sequence control, the PWM part of the DSP code was modified. Instead of a fixed duty cycle for zero-vector ppp, a variable duty cycle is applied based on measured zero-sequence current.

Even when the same PWM applies to the two converters shown in Figure 4.19, a strong zero-sequence interaction can still be observed, as shown in Figure 4.20, if without zero-sequence control.

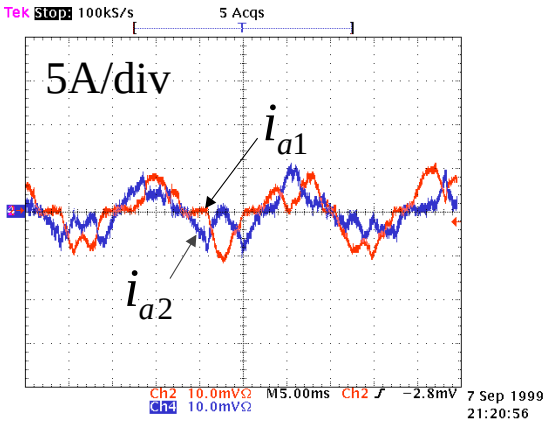


(a) PWM for the converter 1. (b) PWM for the converter 2.

Figure 4.19 Experimental waveforms – PWM applied to the parallel boost rectifiers.



(a) Zero-sequence currents.

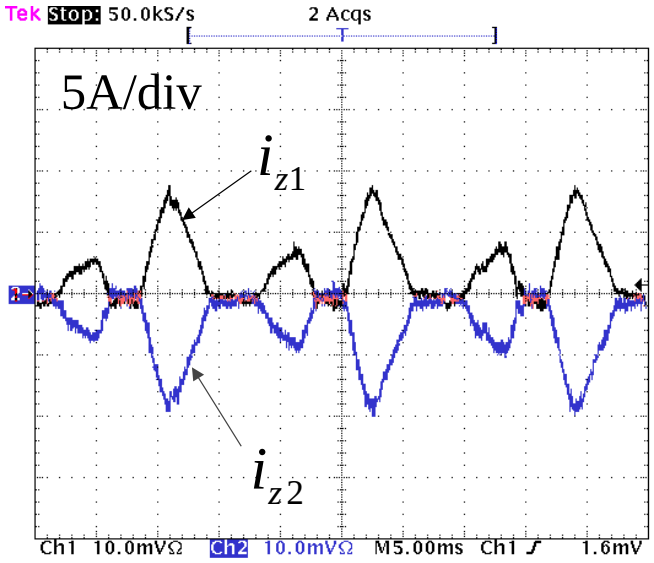


(b) Input phase currents.

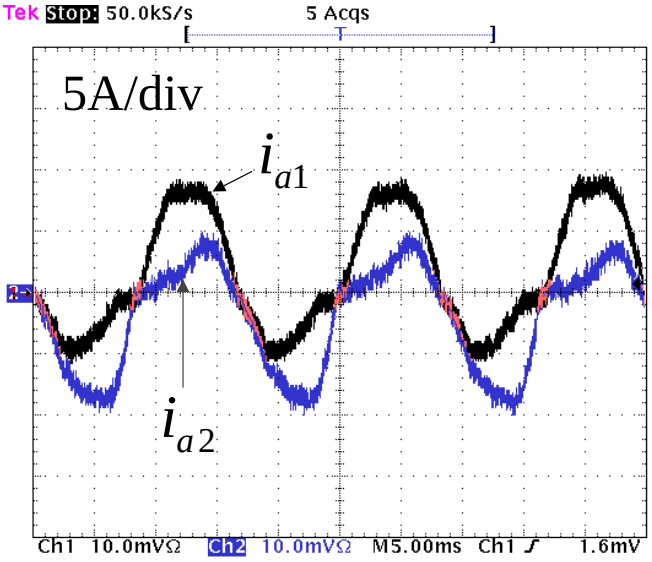
Figure 4.20 Experimental waveforms – parallel interactions with open-loop operation.

The experimental results with current-loop closed are shown in Figures 4.21 and 4.22. The output DC voltage was not regulated. Because of this, the testing power is very low in order to avoid high DC output voltage.

Figure 4.21 shows the zero-sequence currents and the line currents without zero-sequence current control, whereas Figure 4.22 shows the waveforms with control. Due to non-uniform practical conditions, such as different delays in the control circuits and sensor loops, the experimental waveforms are less uniform than simulation waveforms. Therefore, the beat-frequency component as appeared in simulation does not pronounce in the experiment. Three noticeable ripples in Figure 4.22(a) are due to distortion introduced by zero-crossing detection.

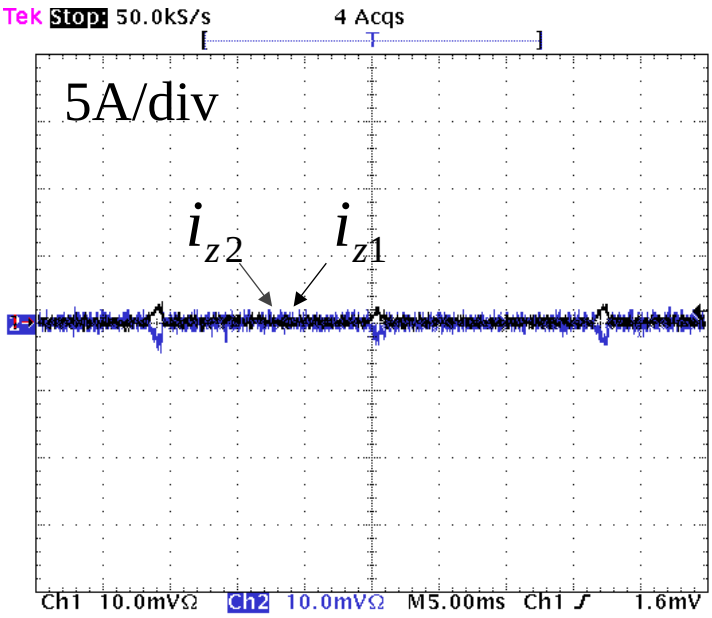


(a) Zero-sequence currents.

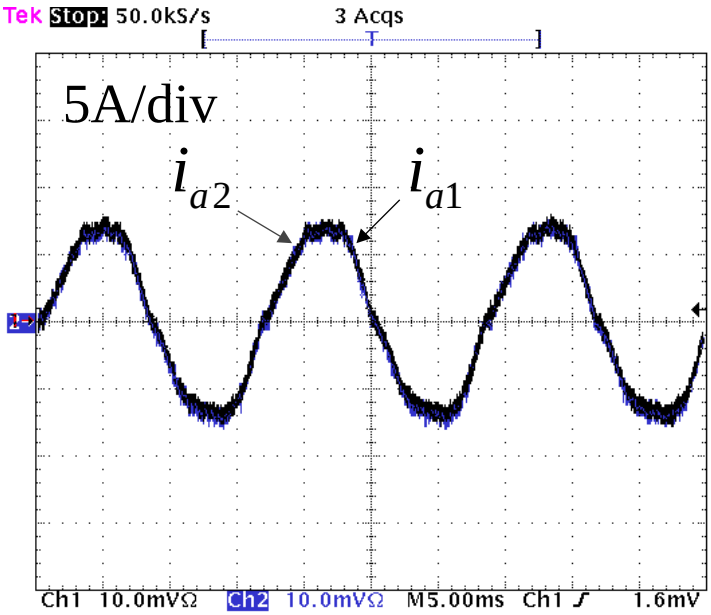


(b) Input phase currents.

Figure 4.21 Experimental waveforms – without zero-sequence current control (fsw1=31.2kHz, fsw2=15.6kHz, unsynchronized).



(a) Zero-sequence currents.

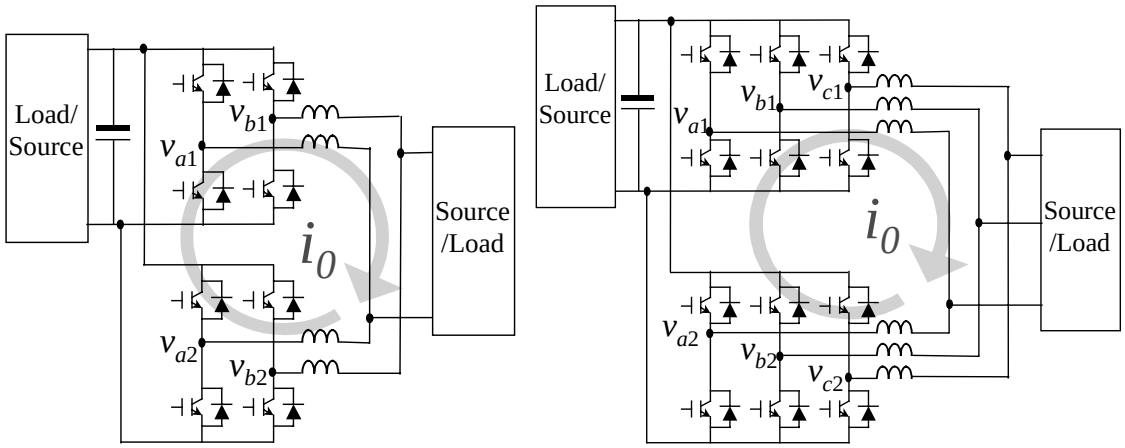


(b) Input phase currents.

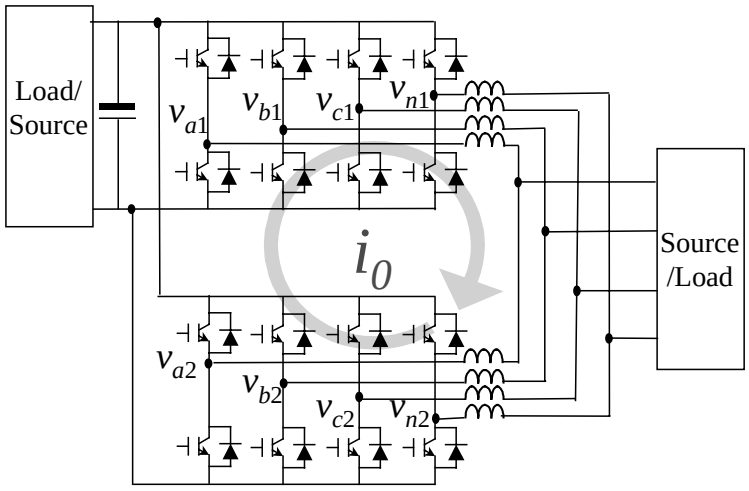
Figure 4.22 Experimental waveforms – with zero-sequence current control (fsw1=31.2kHz, fsw2=15.6kHz, unsynchronized).

4.3 GENERALIZATION TO PARALLEL N-NUMBER OF M-PHASE CURRENT-BIDIRECTIONAL CONVERTERS

This section generalizes the zero-sequence modeling and control concept to parallel N-number of M-phase current-bidirectional converters, such as full-bridge, three-phase three-leg and four-leg rectifiers and inverters, as shown in Figure 4.23 with two converters in parallel, for example.



(a) Parallel full-bridge rectifier/inverter. (b) Parallel three-phase three-leg rectifier/inverter.



(c) Parallel three-phase four-leg rectifier/inverter.

Figure 4.23 Parallel multi-phase current-bidirectional converters.

4.3.1 Zero-Sequence Current Dynamics Model

Based on the phase-leg averaging presented in Chapter 2, an average model of a multi-phase converter can be constructed by simply connecting multiple phase-leg models with the rest of the circuit. Figure 4.24 shows an average model of a generalized M-phase converter. The subscript M represents the number of phases of the converter. Referring to Figure 4.23, a full-bridge converter has M=2 and ϕ_1=a, ϕ_2=b; a three-phase, three-leg converter has M=3 and ϕ_1=a, ϕ_2=b, ϕ_3=c; and a three-phase, four-leg converter has M=4 and ϕ_1=a, ϕ_2=b, ϕ_3=c, ϕ_4=n, assuming the phase n has the same inductance as the other phases.

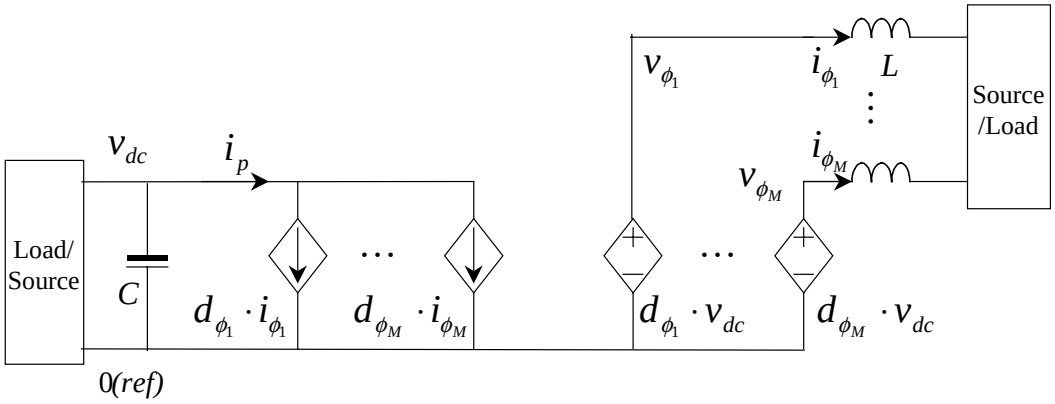


Figure 4.24 Multi-phase converter's average model.

When N-number of M-phase converters are in parallel, multiple zero-sequence current paths are formed, as shown in Figure 4.25. The zero-sequence current is defined as the sum of all phases' currents:

$$\begin{aligned} i_{z1} &= i_{\phi_1 1} + i_{\phi_2 1} + \ldots + i_{\phi_M 1} \\ &\ldots, \\ i_{zN} &= i_{\phi_1 N} + i_{\phi_2 N} + \ldots + i_{\phi_M N} \end{aligned} \quad . \tag{4.8}$$

The circuit of Figure 4.25 has equations:

$$\begin{aligned} & d_{\phi_1 1} \cdot v_{dc} - L_1 \frac{di_{\phi_1 1}}{dt} = d_{\phi_1 2} \cdot v_{dc} - L_2 \frac{di_{\phi_1 2}}{dt} = \cdots = d_{\phi_1 N} \cdot v_{dc} - L_N \frac{di_{\phi_1 N}}{dt} \\ & \ldots, \\ & d_{\phi_M 1} \cdot v_{dc} - L_1 \frac{di_{\phi_M 1}}{dt} = d_{\phi_M 2} \cdot v_{dc} - L_2 \frac{di_{\phi_M 2}}{dt} = \cdots = d_{\phi_M N} \cdot v_{dc} - L_N \frac{di_{\phi_M N}}{dt} \end{aligned} \quad . \tag{4.9}$$

In order to simplify the equations and to extract the zero-sequence components, one can obtain the following equations by summing up (4.9).

$$\begin{aligned}&(d_{\phi_1 1}+d_{\phi_2 1}+\cdots+d_{\phi_M 1})\cdot v_{dc}-L_1\frac{d(i_{\phi_1 1}+i_{\phi_2 1}+\cdots+i_{\phi_M 1})}{dt}=\\&\cdots=\\&(d_{\phi_1 N}+d_{\phi_2 N}+\cdots+d_{\phi_M N})\cdot v_{dc}-L_N\frac{d(i_{\phi_1 N}+i_{\phi_2 N}+\cdots+i_{\phi_M N})}{dt}\end{aligned}. \quad (4.10)$$

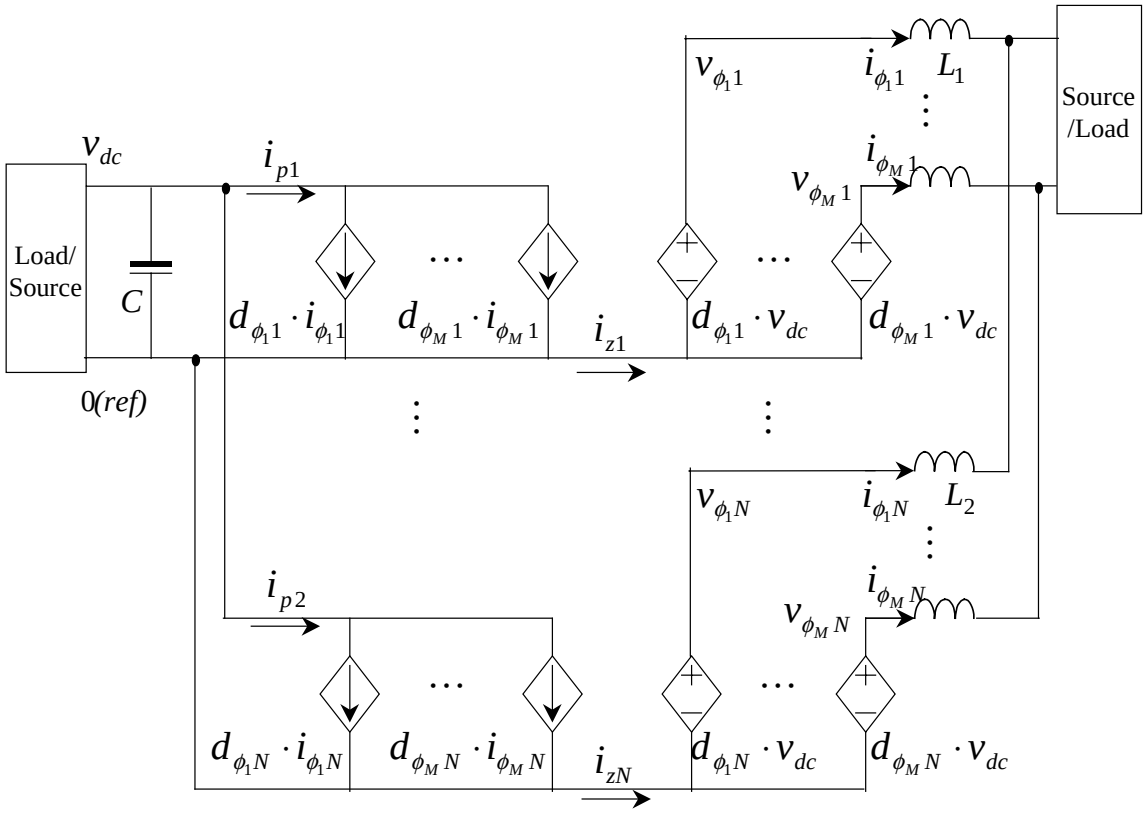


Figure 4.25 N-parallel M-phase converters' average model.

A zero-sequence duty cycle is defined as the sum of the duty cycle of all phase legs in each converter.

$$\begin{aligned}&d_{z1}=d_{\phi_1 1}+d_{\phi_2 1}+\cdots+d_{\phi_M 1}\\&\cdots,\\&d_{zN}=d_{\phi_1 N}+d_{\phi_2 N}+\cdots+d_{\phi_M N}\end{aligned}. \quad (4.11)$$

With the definition of zero-sequence currents in (4.8) and zero-sequence duty cycles in (4.11), the model of Figure 4.25 can be simplified as follows:

$$\begin{aligned} & d_{z1} \cdot v_{dc} - L_1 \frac{di_{z1}}{dt} = \\ & \cdots = \\ & d_{zN} \cdot v_{dc} - L_N \frac{di_{zN}}{dt} \end{aligned} \quad . \tag{4.12}$$

Equation (4.12) describes the dynamics of the zero-sequence currents. Figure 4.26 shows the equivalent circuit of the dynamics described in equation (4.12).

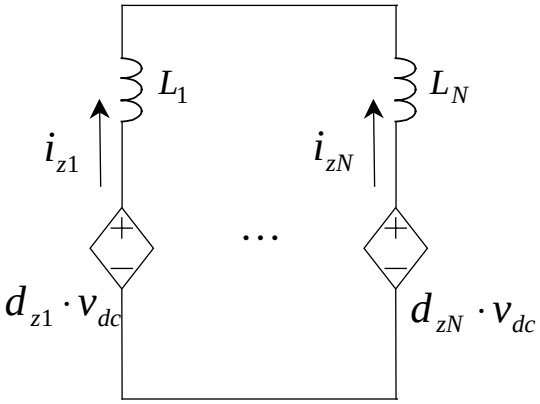


Figure 4.26 Zero-sequence dynamics model of N-parallel M-phase converters.

A control variable *k* is defined as the duration for which all top switches (usually defined as p switch, while the bottom switches are defined as n switch) are closed:

$$k = d_{p_{\phi_1} p_{\phi_2} \cdots p_{\phi_M}} \quad . \tag{4.13}$$

Figure 4.27 depicts the *k* in one switching pattern of an M-phase converter; as an example, *k* is the duration of the zero-vector *ppp* in a three-phase three-leg converter.

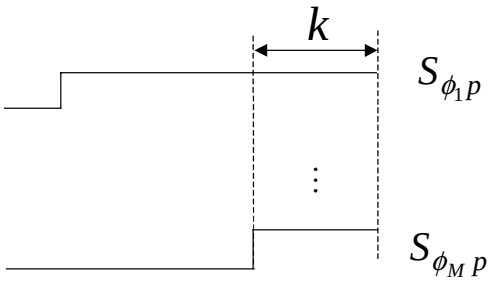


Figure 4.27 Control variable *k* in N-parallel M-phase converters.

Using the definition in (4.13), the zero-sequence duty cycles in (4.11) can be rewritten as follows:

$$\begin{aligned} d_{z1} &= d_{\phi_1 1} + d_{\phi_2 1} + \cdots + d_{\phi_M 1} = M \cdot k_1 + \sum d_{active1} \\ &\ldots, \\ d_{zN} &= d_{\phi_1 N} + d_{\phi_2 N} + \cdots + d_{\phi_M N} = M \cdot k_N + \sum d_{activeN} \end{aligned}, \qquad (4.14)$$

where $\sum d_{active}$ is the total duty cycle of the active switching vectors. For example, in a three-phase space-vector modulated converter, $\sum d_{active} = d_1 + 2d_2$.

Substituting (4.14) into (4.12), a new zero-sequence average model with the control variable *k* is obtained:

$$\begin{aligned} &(M \cdot k_1 + \sum d_{active1}) \cdot v_{dc} - L_1 \frac{di_{z1}}{dt} = \\ &\cdots = \\ &(M \cdot k_N + \sum d_{activeN}) \cdot v_{dc} - L_N \frac{di_{zN}}{dt} \end{aligned} . \qquad (4.15)$$

The equivalent circuit is shown in Figure 4.28. As a result, the zero-sequence current can be controlled by controlling k_1, k_2, …, and k_N.

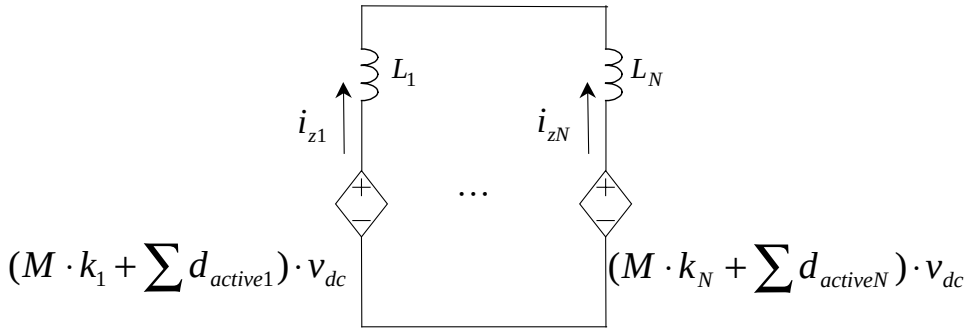


Figure 4.28 Zero-sequence dynamics model with new control variable *k* in N-parallel M-phase converters.

4.3.2 Zero-Sequence Current Control

For the N-paralleled converter system, there are N-1 independent zero sequence currents because

$$i_{z1} + i_{z2} + \ldots + i_{zN} = 0 . \qquad (4.16)$$

Therefore, only N-1 converters are needed to have a zero-sequence current control. For example, if k_N is set to a constant value K, then the steady state has a unique solution:

$$
\begin{aligned}
k_1 &= \mathrm{K} + \frac{\sum d_{activeN} - \sum d_{active1}}{M}, \\
&\cdots, \\
k_{N-1} &= \mathrm{K} + \frac{\sum d_{activeN} - \sum d_{activeN-1}}{M}, \\
k_N &= \mathrm{K}.
\end{aligned}
\tag{4.17}
$$

If all N converters are controlled, the resulting equivalent circuit is N current sources in parallel, which is not practical. First, the N current sources will have interactions because of the constraint in (4.16). Second, assuming that in steady state all currents are zero, the number of solutions is infinite because there are N-1 independent equations as in (4.18), but N unknowns (k_1, k_2, …, k_N):

$$
\begin{aligned}
M \cdot k_1 + \sum d_{active1} &= \\
M \cdot k_2 + \sum d_{active2} &= \\
\cdots &= \\
M \cdot k_N + \sum d_{activeN}
\end{aligned}
\quad . \tag{4.18}
$$

Therefore, it is necessary to have N-1 converters controlled in an N-parallel converter system. Figure 4.29 shows the zero-sequence control in an N-parallel M-phase converter system. The controllers are designed within individual converters. The converter N is not controlled and has a constant K.

The preceding analysis has been validated by simulation on a three-parallel, three-phase converter system constructed in Saber. The system is a phase-leg averaged converter model as shown in Figure 4.29.

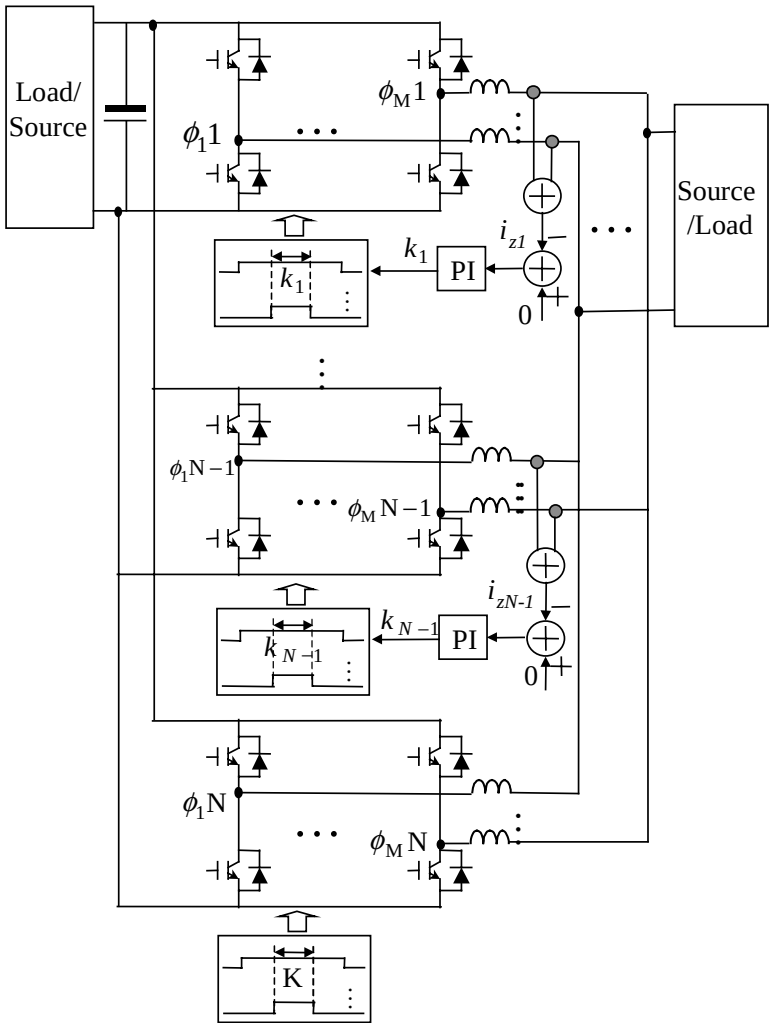


Figure 4.29 Zero-sequence current control implementation for N-parallel M-phase converters.

Figure 4.30 shows the zero-sequence current without control. The three converters have different switching frequencies (f_{sw1}=20kHz, f_{sw2}=7kHz, f_{sw3}=15kHz) and shifted switching clocks ($shift_{clock1}$=0μs, $shift_{clock2}$=10μs, $shift_{clock3}$=10μs). It can be seen that a strong zero-sequence interaction exists in the parallel system. By applying the control to two of the parallel converters, the zero-sequence currents are well controlled, as shown in Figure 4.31.

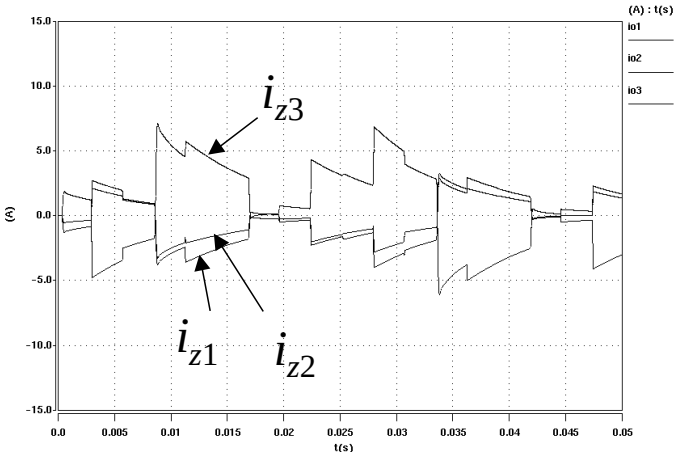


Figure 4.30 Three-parallel three-phase boost rectifiers without zero-sequence current control.

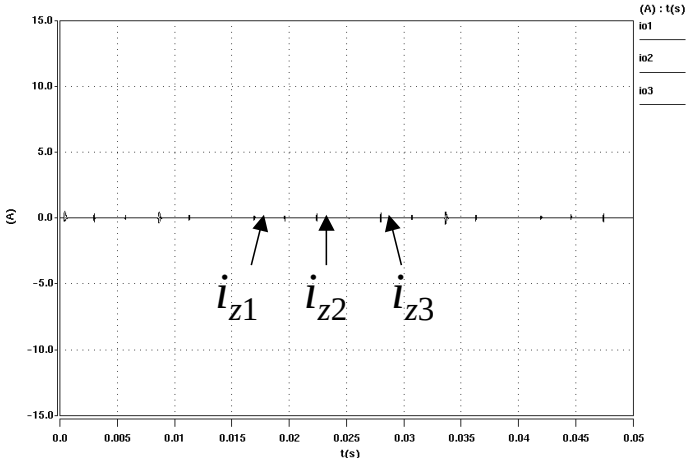


Figure 4.31 Three-parallel three-phase boost rectifiers with zero-sequence current control.