Integrated Electro-thermal Design Methodology in Distributed Power Systems (DPS)

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(ABSTRACT)

Although suitable CAD tools for thermal and electrical analyses in power electronic systems are available, traditional stand-alone simulation method seldom takes into consideration of the inter-dependency of semiconductor device power loss and junction temperature in an iterative process. However these dependencies are important, especially for applications where both cooling and power losses are driven by complex mechanisms.

For a power supply system, a dynamic design process is necessary to address both electrical and thermal issues. It is because the steady state temperatures of the system are obtained from loss-and-temperature iteration. Once a system solid body model is built, iterations between power loss and junction temperature calculations are performed to obtain the steady state temperature distribution. Since reliability and failure rate of components are directly related to temperatures, an accurate model is critical to provide proper thermal management, which achieves maximum power density. All cooling-

related data such as placement of components, airflow rate, heat sink size, and device types are subjected to design changes in order to meet ultimately the temperature requirements.

The goal of this thesis is to demonstrate the benefits of integrated analysis and design tools applied in distributed power supply systems' designs. First, it will significantly speed up the design process and eliminate the errors resulting from repeated manual data entry and information exchange. Second, the integrated electrical-thermal design tools encompass electrical, thermal, layout, and packaging design to obtain the optimal system design.

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Nomenclature

A Area, m^2

I Current, A

K Thermal conductivity, W/m-K

L Thickness, m

n Total number of critical parameters

P Power loss, W

R Thermal resistance, °C/W

t Time, s

T Temperature, °C

V Voltage, V

Acronyms

AC Alternative Current

CFD Computational Fluid Dynamics

CPES Center for Power Electronic Systems

DPS Distributed Power Supply Systems

DC Direct Current

ESC Electronic System Cooling

PFC Power Factor Correction

IPEM Integrated Power Electronic Module

MOSFET Metal Oxide Semiconductor Field Effect Transistor

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Chapter 1.

Introduction

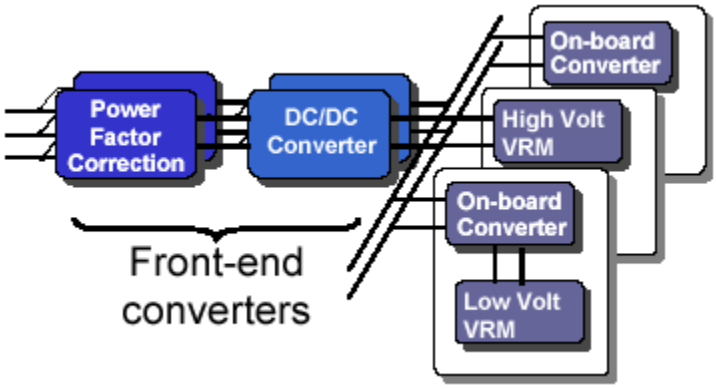
The purpose of this work is to demonstrate that integrate electrical and thermal simulation CAD tools can be used to achieve an integrated design of DPS and optimize both the electrical and thermal performance.

1.1. Background and Motivation

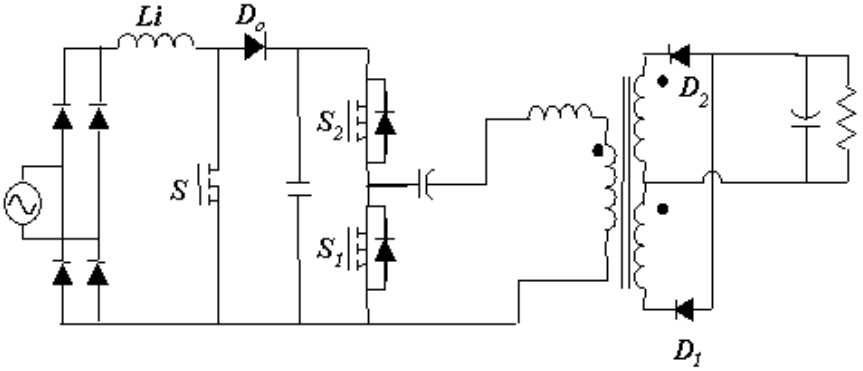
The DPS architecture has been widely adopted as an industry practice to power the next generation of information technologies. The driving force comes from several key emerging applications. The latest generation of computer and telecommunications equipment has adopted an open-architecture, modular approach to signal and data processing. Internet infrastructure requires the use of network system routers and hubs that operate naturally with modular distributed power supplies. DPSs can also better address the increasing concerns regarding fault tolerance, improved reliability, serviceability and redundancy without a significantly added cost. The widespread use of DPSs has opened up the opportunity in the power supply industry to develop a standardized modular approach to power processing. This will significantly improve

both the design and manufacturing processes, enhance the system performance and reliability, and reduce the product cycle time.

The structure of a DPS is shown in **Figure 1.1(a)**. The front-end converter features excellent utility interface such as high power factor and low harmonic distortion, and provides regulated 48V DC bus for the load converters.



(a) Distributed power systems



(b) Front-end PFC and DC/DC converters

Figure 1. 1 DPS front-end converters.

The front-end of the DPS usually adopts a two-stage approach. The first stage accomplishes the power factor correction from a universal single-phase input line voltage (90~264Vac) while the second stage provides the isolation and tightly regulated DC bus voltage as shown in **Figure 1.1 (b)**. [1] [2]

Due to the nature of electronic power processing, the design of power electronics components, converters and systems has always involved many disciplines: from circuits and solid-state physics, to electromagnetics, systems and control, thermodynamics, structural mechanics, material science and reliability like shown in **Figure 1.2**. It is practically impossible (and unnecessary anyway) to model, analyze, and design any component or system by using fundamental physical laws of energy fields and matter continuity. Therefore, the design of any specific component, converter or system would involve some disciplines to a greater extent and would need more detailed modeling and accurate analysis, while the importance of other disciplines may be only marginal. This is enabled by using different levels of abstraction, i.e., models of varying levels of fidelity, for different types of analysis that are suitable or required for different designs. [3]

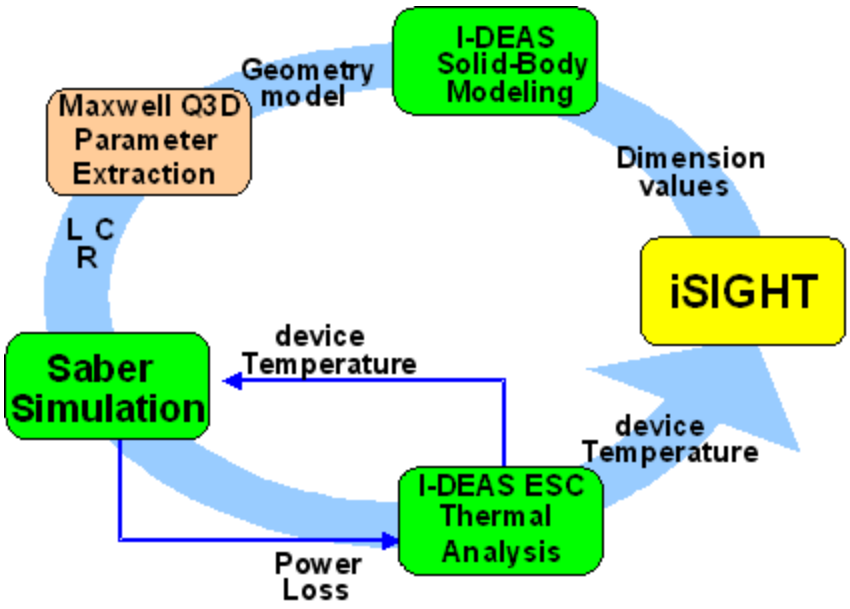


Figure 1. 2 Integrated design process in power electronics.

Traditionally, the multidisciplinary aspects in the power electronics design have involved only algebraic modeling. Although this approach may be physically justified in many instances, it often leads to significant design deficiencies. For example, the satisfactory functioning of a component or a system under nominal steady-state operation is a necessary condition, but it is not sufficient for reliable functioning during the lifetime of the product in the field. The standard ways of dealing with the problem are different forms of "worst-case" analyses, and component de-rating based on empirical experience. These analyses have been done sequentially in industry, progressing from one discipline to another and involving many prototyping iterations. Although the use of CAD tools is widespread, these tools are largely "mono-disciplinary" and, hence, require an inordinate number of labor intensive and time-consuming iterations. As a result, today's design

process in power electronics is still much less advanced than the automation levels now common in many other industries. The resulting long design cycles unduly increase the cost and turn around time, and coupled with lack of standardization, prevent levels of optimization that are now standard in most high-tech industries. The need for integrated analysis and design tools is even more pressing now, when further advancements are limited by the fundamental relationships between electrical, thermal, mechanical and material properties of the components and packaging. [4][5][6][7][8][9][10]

The goal of this thesis is to present an approach to integrate the multidisciplinary design process in power electronics through the integration of existing CAD tools, multidisciplinary modeling and demonstrate integrated electro-thermal design method with integrated CAD tools can significantly speed up the design process and eliminate the errors resulting from repeated manual data entry and information exchange design time and improve performance so as to support the market needs for the rapidly evolving computer, telecommunications and internet infrastructure industries. [11][12]

1.2. Thesis Outline

This thesis consists of five chapters including necessary background, motivation and the objectives of the research effort in Chapter 1. Chapter 1 also provides some related information and previous research done by other researchers in the same area.

Several valid and reasonable electrical and thermal modeling approaches for discrete power electronics components and integrated electro-thermal simulation environment are presented in Chapter 2.

A design example of single phase CCM PFC converter is given in Chapter 3 using integrated electro-thermal simulation developed in Chapter 2. The integrated electro-thermal design method is proposed and compared with conventional non-integrated electro-thermal design method. The demonstration for benefits of integrated electro-thermal design method is also given in Chapter 3.

The integrated electro-thermal design method is applied into integrated DPS test-bed design, which is described in Chapter 4.

Finally, Chapter 5 provides conclusions and summary of the research effort as well as the recommendations for future research interest.

Chapter 2.

Integrated Electro-thermal Modeling Approach

2.1. Introduction

Traditional design processes for power electronics circuits are usually iterative trial-and-error approaches based on hardware prototyping and testing. The design advantage of the simulation approach compared to hardware design is that it can reflect the system characteristics more accurately, for example: electric machine dynamic, parasitic parameters, MOSFET avalanche energy and switching loss. Advances software tools for thermal, electrical and mechanical analysis have enabled designers to depart from conventional methods towards more CAD-driven design processes, and are useful especially for complex designs where integration is a key aspect. That such tools are becoming more essential as integration technologies in the physical structures progress is also self-evident.

Although suitable CAD tools for thermal, electrical and mechanical analyses are widely available, stand-alone tools are incapable of taking into consideration of complete electrical versus thermal dependencies. That is, most of the device loss models are electrical behavior or physics model. And all parameters are considered thermally independent. This is not true in a real system, because several key parameters such as Rdson, Vth…would change following the temperature variation. So it would be

inappropriate to decouple the electrical and thermal design of a system. The thermal loop has to be closed in device and system level to reflect the device and system dynamics, which will improve the accuracy of the simulation and make the performance prediction reasonably close to the real system. [11][12]

2.2. Power Device Model

Accurate power semiconductor device models are needed to predict large overshoot voltages and currents, switching power losses, conducted EMI and so on in the design of high performance, reliable power converters.

A physics-based power device sub-circuit model has been developed and implemented for Saber and several SPICE platforms including PSPICE and HSPICE. The model is hierarchical in complexity and feature implementation, and includes thermal modeling of transfer function for a fixed temperature in the Level 1 model, and transient thermal behavior in the Level 2 and 3 versions. All versions include a highly efficient physics-based gate capacitance model, which is compatible with simulators having common behavioral math functions with access to the derivatives of node voltages.[15][16]

Saber by Analogy, Inc. has greatly enhanced designers' ability to model analog and mixed-mode circuits and systems by providing a flexible behavioral modeling language, MAST Hardware Description Language (HDL). With this modeling language,

a designer can behaviorally describe an analog or mixed-mode device or subsystem at whatever level of abstraction is appropriate for a given simulation accuracy-versus-speed trade-off. One can use this modeling language to write models for MOS transistors and use these models to achieve simulation results that are as accurate as those from SPICE simulations.

With Saber's MAST language, even a combination of circuit blocks with different description levels in one model description ("template") is possible. Saber provides a library with a number of predefined templates, which can be used as circuit hierarchy, and a number of predefined components. Besides, there are all kinds of PSPICE and Saber device models on manufacture's websites.[13][14][17][18][19][20] [21]

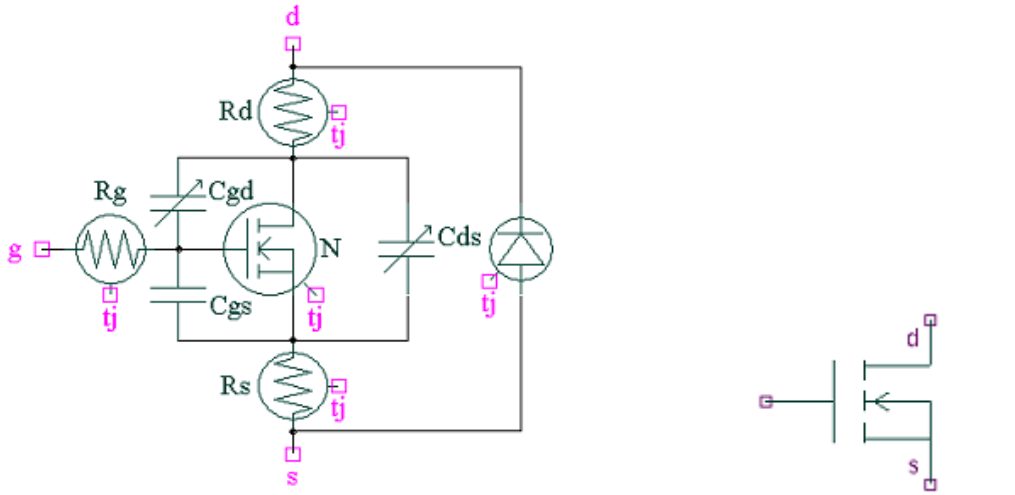
2.2.1 Power MOSFET Model

The revolutionary CoolMOS power MOSFET family enables a significant reduction of conducting and switching losses in power electronic systems like Switched Mode Power Supplies (SMPS). The inherent increase of power density stands for a superior efficiency factor of power conversion systems.

Infineon Inc. provides Saber level 3 models for CoolMOS devices [22]. They are based on a physical temperature-dependent model of the CoolMOS structure and the package.

The temperature-dependent model of the level 3 MOSFET is shown in **Figure 2.1**.

Rd, Rg and Rs are resistances, which are temperature dependent. Basic MOSFET and body diode are temperature dependent too.



(a) The level 3 model of the MOSFET in SABER **(b) The symbol of MOSFET**

Figure 2. 1 A level 3 model of the temperature-dependent MOSFET and its symbol in Saber.

Saber provides the diode models and some manufacturers provide the models for some devices. However no any manufactures guarantee the complete accuracy of their models.

Therefore efforts must be taken to verify the model accuracy for the expected operating conditions. Considering the electro-thermal design, the relationship between power loss and junction temperature of devices is needed to model accurately. Conduction loss of power devices is due to on-resistance. Besides, on-resistance is dynamically changed with junction temperature. Hence, verification for electro-thermal characteristics of power devices partly focuses on comparing the on-resistance as function of temperature between simulation results and datasheet values or experimental

data. The Rds(on)-Junction temperature curve of CoolMOS model under different junction temperatures are given in **Figure 2.2**.

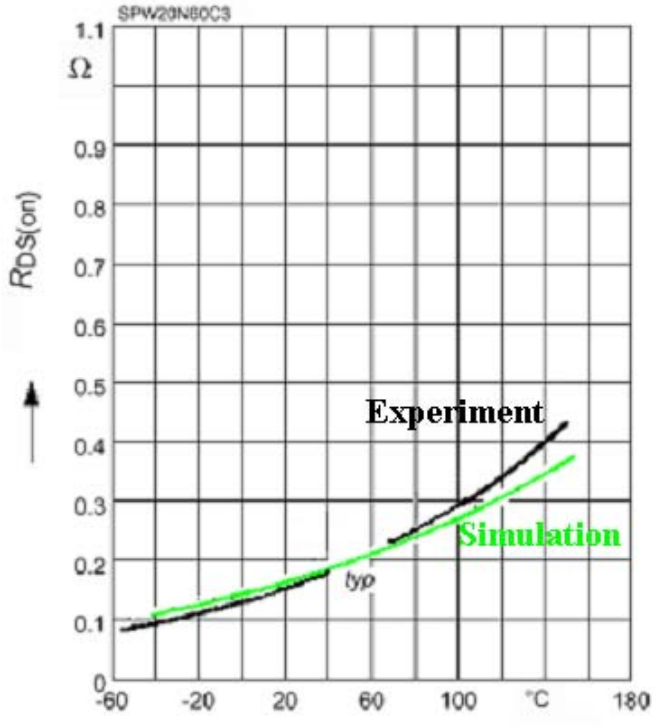


Figure 2. 2 Normalized on-resistance vs. temperature for CoolMOS (Rdson=0.19Ω @ Tj=25°C).

Parasitic inductance stores energy when current flows through it. When the device needs to be turned off, the energy is released, as a voltage spike if no external snubber exists.

Package parasitics of power devices have been shown a critical impact on the efficiency and EMI of power converters. Therefore, to design and optimize the performance and reliability of power systems, it is necessary to have accurate values of the device parasitics. [24] [26][27][28][29]

Inductance is sometimes listed on manufactures' datasheets and then usually only as an average value. Infineon Saber level 3 models for CoolMOS include the core device, junction capacitors and resistors except for parasitic inductors. A complete electrical sub-circuit of power MOSFETs with TO-247 packaging structure is proposed in **Figure 2.3**. Based on this equivalent circuit, parasitic inductors (red) can be obtained by impedance measurement. [30]

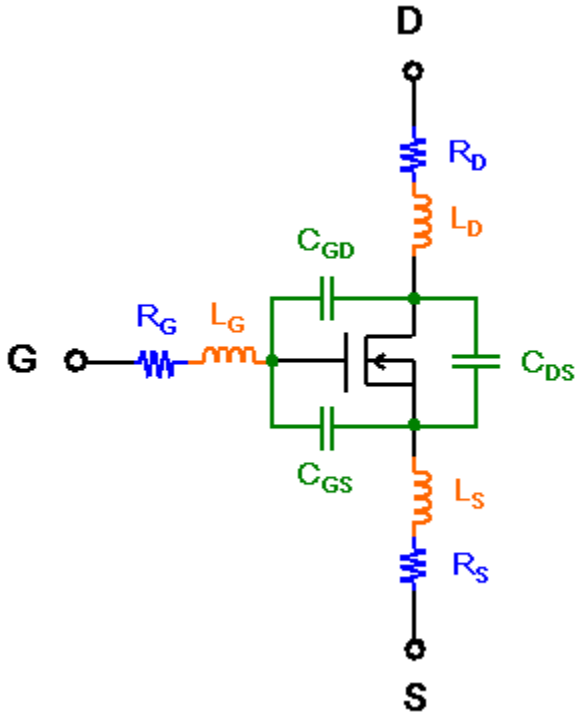


Figure 2. 3 The electrical equivalent circuit for a MOSFET with packaging parasitics.

A simple method to extract the parameters in **Figure 2.3** has been explored. First we measured the impedance across the terminals drain *(*D) and source *(*S), Z_{DS}, as shown in **Figure 2.4,** using an Agilent 4294A Impedance Analyzer. Curve- fitted values may be obtained also from the Impedance Analyzer as in equation (2.1).

$$L_D + L_S = 6.72nH \tag{2.1}$$

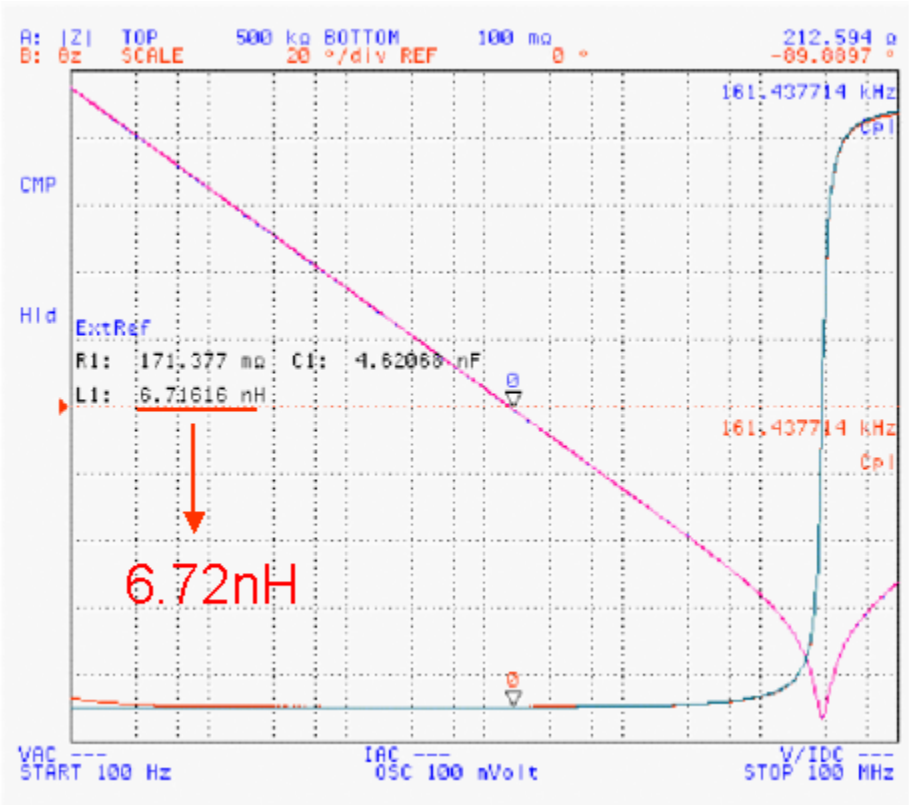


Figure 2. 4 Measured impedance of Z_{DS}.

Same measurement approach is applied to impedances of Z_{GD}, and Z_{GS}, then we have **Figure 2.5** and **Figure 2.6**, and equations (2.2)~(2.3) as follows.

$$L_G + L_D = 7.10nH \tag{2.2}$$

$$L_G + L_S = 12.48nH \tag{2.3}$$

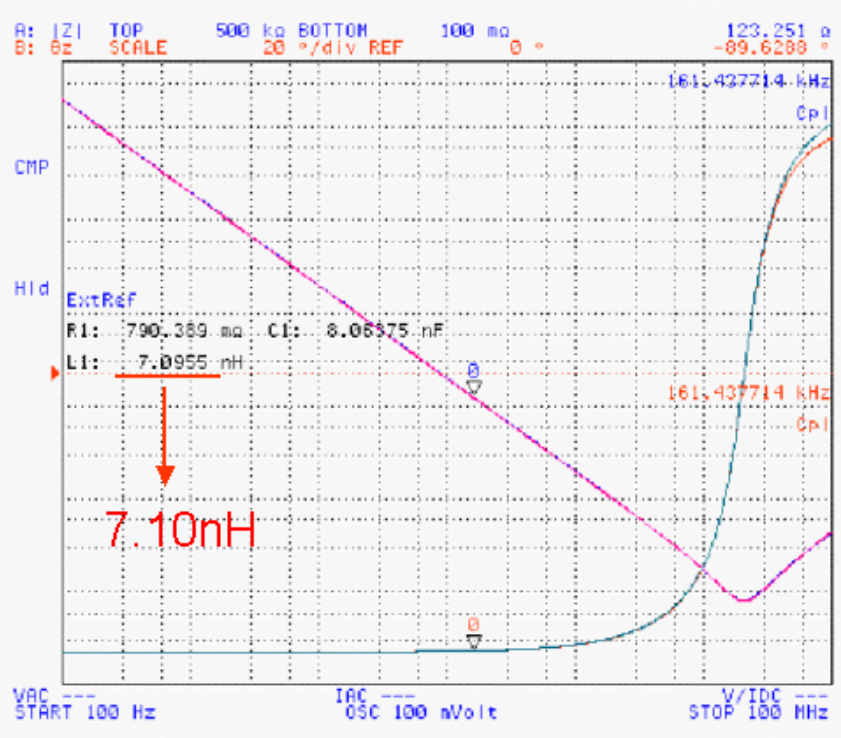


Figure 2. 5 Measured impedance of Z_{GD}.

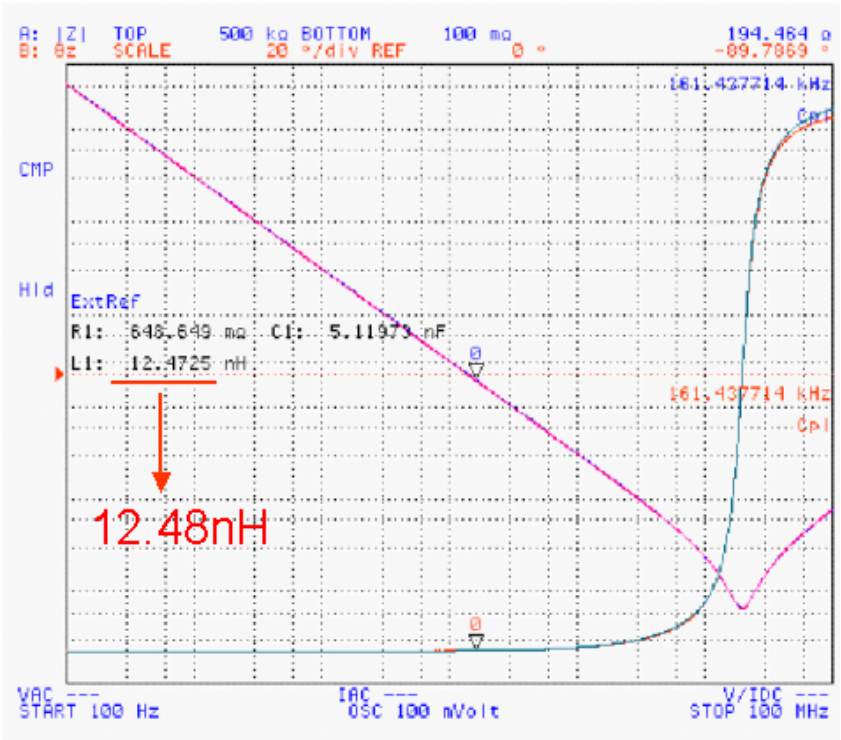


Figure 2. 6 Measured impedance of Z_{GS}.

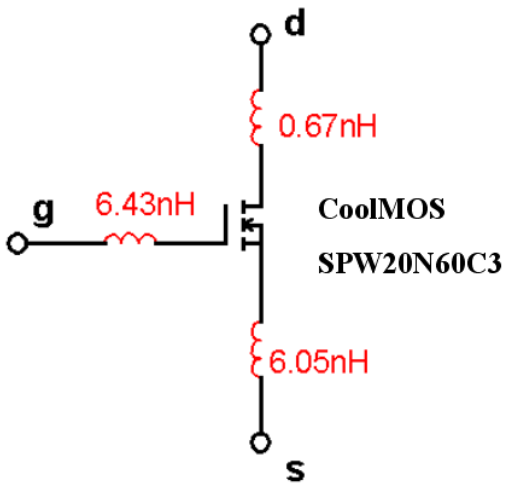


Figure 2. 7 CoolMOS model with parasitic inductors in Saber.

The leading inductances of power devices from impedance measurement can be input into schematics in Saber as shown in **Figure 2.7**, and a circuit can be built using these parasitic models and power device.

Switching characteristics of a CoolMOS model can be obtained by building a simulation circuit in Saber (**Figure 2.8**). The turn off and turn on simulation waveforms for the CoolMOS have similar switching characteristics to the measurement results respectively, as shown in **Figure 2.9**.

In order to have a quantitative comparison between the switching characteristics of the models and the actual circuit, the computed switching losses from the simulation are juxtaposed with the computed switching losses from measurement under same conditions. This is shown in **Table 2.1**, wherein the turn on and turn off switching losses are listed. We can see that the switching losses from simulation are close to measured results, which means, the models in Saber are accurate enough for predicting the losses of power devices.

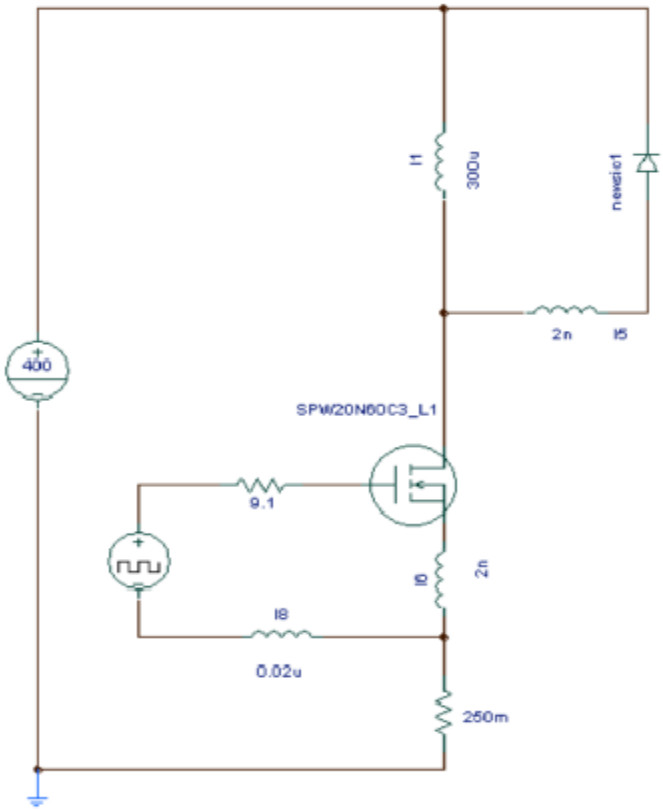
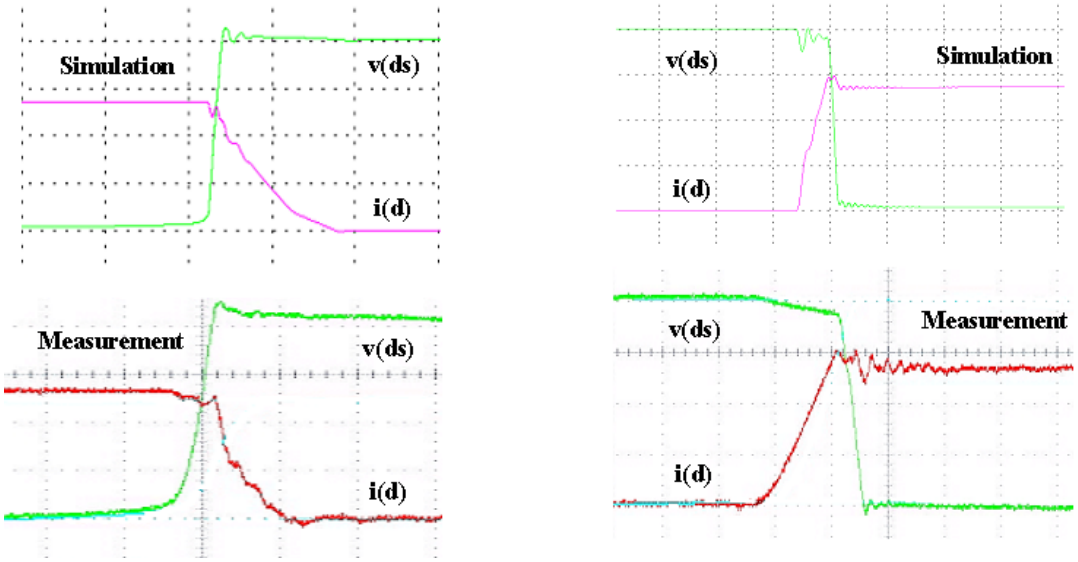


Figure 2. 8 The simulation circuit for testing switching characteristics.



(a) Turn-off waveforms **(b) Turn-on waveforms**

Figure 2. 9 Switching waveforms for CoolMOS SPW20N60C3.

Table 2. 1 Switching loss comparison between simulation and measurement

	Simulation	Measurement
Turn-off Loss	194.86uJ	200uJ
Turn-on Loss	290uJ	314uJ

2.2.2 Power Diode Model

RHRP860s are hyper-fast diodes with soft recovery characteristics (trr < 30ns). They have half the recovery time of ultra-fast diodes. Their low stored charge and hyper-fast soft recovery minimize ringing and electrical noise in power switching circuits by reducing power loss in the switching transistors.

The Diode Tool in Saber provides support to create diode models intended for use in power electronic circuits. These models are well suited for examining switching transients and losses in power supplies. The tool supports the following model features: I-V characteristics, junction capacitance, reverse recovery and dynamic thermal.

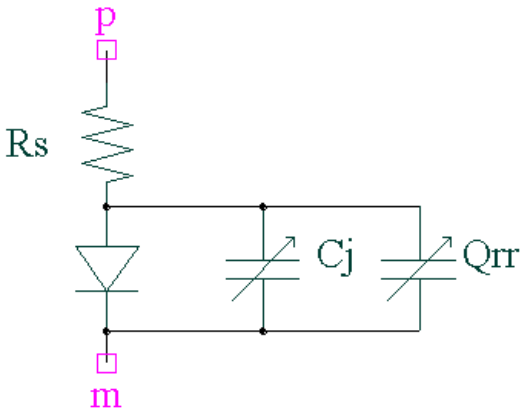


Figure 2. 10 Diode model built in Saber.

The user can select the level of model complexity that is relevant for the intended usage. Retaining the model features which are only needed helps to ensure good convergence performance as well as computation speed. A limited number of parameters make each model feature easily characterizable from datasheet information. The tool allows interactive tuning of the parameters through graphical widgets directly placed on the model characteristics (Anchor Objects). An optimizer is also provided to help match the model characteristics with experimental data.

In electro-thermal application, level 3 models are used. Such a dynamic thermal model carries a thermal connection, which across variable is the device temperature. In this model, the temperature changes with the heat flow (through variable) between the device and its thermal environment. The I-V characteristics of boost diode model under different junction temperatures are given in **Figure 2.11**.

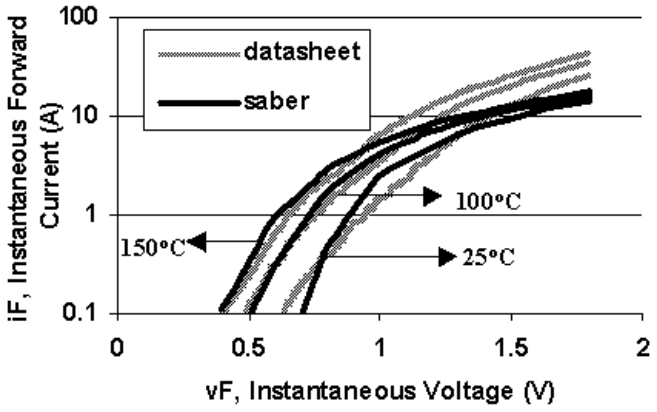


Figure 2. 11 I-V characteristics of RHRP860 under deferent temperatures.

From comparison, Saber has modeled conduction losses of devices and their dependency on temperature properly. Conduction losses of boost diode decrease as junction temperatures increase due to the negative temperature coefficients.

In CCM boost-type PFC converter, the semiconductor losses not only include conduction loss but also the reverse recovery loss from the boost diode. The current turn off waveform shape of boost diode is shown as **Figure 2.12**. The reverse recovery loss takes big part of total devices' losses. Furthermore, reverse recovery loss varies greatly with junction temperature. Therefore, the characteristics of reverse recovery loss as function of temperature cannot be neglected in electro-thermal design. **Figure 2.12** shows the complete reverse recovery processes of boost diodes under different junction temperatures.

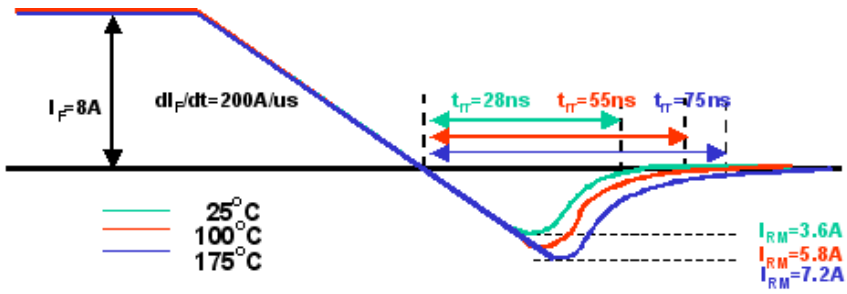


Figure 2. 12 Reverse recovery of RHRP860 under different junction temperatures.

After the diode model is modified to include temperature dependent reverse recovery loss, verification is still needed like conduction loss. In CCM PFC schematics, voltage and current waveforms under different power devices' junction temperatures can

be obtained after the simulation reaches the steady state. The temperature dependent parameters extracted from boost diode model's current waveforms are shown as **Table 2.2**.

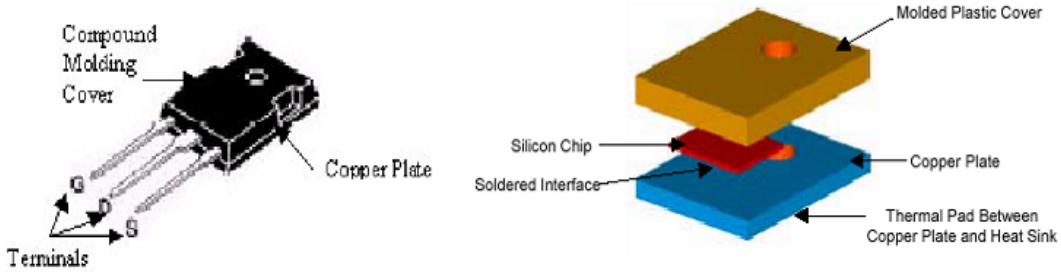
Table 2. 2 Comparison between simulation results and datasheet values.

Tj		If	dIf/dt	Irm	t_{rr}
25°C	Simulation	8A	198A/us	4.68A	29ns
	Datasheet	8A	200A/us	3.6A	28ns
100°C	Simulation	8A	199A/us	6.99A	55ns
	Datasheet	8A	200A/us	5.8A	55ns
175°C	Simulation	8A	200A/us	8.36A	75ns
	Datasheet	8A	200A/us	7.2A	75ns

2.2.3 Power Device Thermal Modeling

A discrete power electronics module such as a MOSFET consists of four elements: the gate, source, drain, and the substrate. The basic functioning principle of the MOSFET is the control of a current flowing between two semiconductor electrodes. The drain and the source are placed on the same element, with a third electrode, the gate, between the drain and the source. Both the drain and the source are n-type semiconductor, and are isolated from the p-type substrate by reversed-biased p-n diodes. The voltage applied to the gate controls the flow of electrons from the source to the drain.

A commercial package of MOSFET is an assembly of parts bonded together by solder, adhesive, molding compound, and mechanical parts such as bolts and springs. Three major physical parts of MOSFET (a copper base plate, a silicon device and a plastic injected molded cover) were modeled to form a simple computational model of TO247 package. Because the heat transfer to the three terminals extending from the package was ignored, the terminals were not modeled. **Figure 2.13** shows the thermal modeling for MOSFETs. [32] [33][34]



(a) A commercial package of MOSFET. **(b) Exploded view of MOSFET thermal model.**

Figure 2. 13 Thermal modeling for MOSFET.

Device packaging is modeled after a simple series electrical circuit.

The junction is like the battery of this circuit. It supplies the power for the thermal model's circuit. Instead of voltage this "battery" has the value of the power (in Watts) being dissipated by the device.

The case is the actual package itself. The ease with which heat transfers from one side of the case to the other depends on what material the case is made of.

This resistance to the flow of heat through the packaging material leads to the

obvious choice of modeling the package as a resistor in the thermal circuit.

Current must flow somewhere in order to complete the circuit, in most cases current flows to ground. Ground is defined as having the ability to source or absorb an infinite amount of current without generating a voltage.

The equivalent in our thermal circuit as shown in **Figure 2.14** has the ability to absorb an infinite amount of power without generating any heat. The earth's atmosphere comes close to that description so it is used as the ground in the thermal circuit. A transistor's worth of power is unlikely to change the ambient temperature of the air so the ground of the thermal circuit is known as simply ambient.

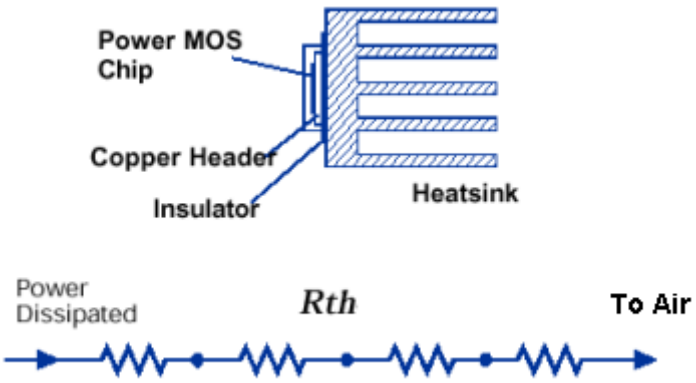


Figure 2. 14 Concept for power device construction and thermal equivalent model.

The silicon device was assumed to have a perfect contact with the compound molding cover. The soldered and thermal pad interfaces between various components were represented by equivalent thermal resistance values. These interfaces were the

interface between the copper plate and the heat sink, and the soldered interface between the silicon device and the copper plate. **Figure 2.14** illustrates the exploded view of the numerical model in I-DEAS. [31]

The power loss was assumed to be uniform across the top surface of silicon devices. In the modeling, finer grids were applied for the heat-dissipating surfaces. Within the MOSFET, there was a conduction path from the silicon device to the copper plate and the compound molding cover, from the copper plate to the heat sink, and convection from both the heat sink and the MOSFET to the ambient air.

The thermal conductivities and thermal resistance values for all of the materials used in the models are listed in **Table 2.3**. These values were used to calculate relevant thermal coupling values in the simulations.

Table 2. 3 The thermal conductivity and thermal resistance values for materials used

Meterial	Thermal Conductivity (W/mK)	Thickness (mm)
Compound Molding	1	3
Silicon	117.5	0.5
Copper	395	2
Aluminum	164	N/A
Solder	51	0.127
Thermal Interface	3.5	0.13

2.3. Integrated Electro-thermal Simulation Environment

The design of power electronics systems involves many disciplines, and several integrated multi-disciplinary approaches have been proposed to improve the design process for power electronics systems. **Figure 1.3** illustrates the process that has been adopted for the modeling, design, and analysis of integrated power electronics module (IPEM) at CPES. This process addresses three important multidisciplinary dependencies: First, it addresses the direct impact of the part geometry and material on the structural parasitic impedance, and hence the electrical performance. Second, it addresses the direct impact of the part geometry and material on the module's thermal performance. And, finally, it addresses the electrical and thermal interdependence. The electrical characteristics of the power device depend on the device temperature, and the device temperature depends on the power loss of the device. Hence, the outer loop in **Figure 1.3** shows the electrical and thermal analysis following the geometric shape definition, while the inner loop shows the electrical-thermal codependence that must be resolved iteratively before continuing along the outer loop. [5][42]

An integrated software environment is the key to implement this design process. Because most of existing CAD tools are “mono-disciplinary” and lack the ability to talk with each other directly, integration tools are necessary for interfacing with each CAD tool and allowing data sharing among them. It is until then possible to have the multidisciplinary design and analysis iterations fully automated, and hence allows for design optimization using proven optimization techniques. [42]

The integration framework is based on the commercial integration tool, iSIGHT, which manages the design variables and the analysis process. Three CAD tools are integrated through iSIGHT: I-DEAS for mechanical modeling and thermal analysis, Maxwell Q3D for the parasitic parameter extraction, and Saber for electrical circuit simulation. Each tool has inputs and outputs, both in the form of plain text files, for iSIGHT to provide parameter values to the program and monitor the analysis results. An in-house integration tool is developed to simplify the configuration by providing a generic interface to automated geometry manipulations and thermal parametric studies. The implementation detail is described as follows.

2.3.1 Process Integration in iSIGHT

The design procedure using integrated electro-thermal simulation environment involves the following steps:

1. Creating the design and simulation models. At first, a preliminary design layout is decided by rough hand calculation for power losses of power devices and for the thermal resistance of heat sink. 3D solid models are drawn into I-DEAS. Maxwell Q3D imports the elaborate layout, which is drawn by Protel. Then Maxwell Q3D performs parameter extraction and records the parasitic impedance matrix into a text file. According to such a text file, parasitic models can be combined with device loss models to build electrical models in Saber.

2. Setup the input file to the thermal simulation. This is a trivial text file which records the parameters that will be changed for the thermal simulation, e.g., the power losses for the devices. A generic thermal study tool, which is based on Open I-DEAS API, reads in this file and instructs I-DEAS through the thermal simulation.

3. Setup the input file to the electrical simulation. This is the Saber netlist file, which records the circuit schematic and simulation parameters, e.g., the temperature of the device. A Saber macro file is needed to instruct Saber through the electrical simulation.

4. Customize the electro-thermal analysis iteration in iSIGHT. This includes: initializing the design and analysis variables, instructing iSIGHT for modifying input files to and reading outputs from electrical and thermal simulations, and specifying the condition for terminating the iteration. Then the whole process is automatically executed.

5. Re-design the heat sink and repeat the loop. Based on the steady state, heat sink is reduced in order to obtain optimized design, which means higher power density and lower cost. Heat sink is changed manually in I-DEAS. Loop is automatically executed again to achieve new steady state for the changed geometry.

6. Stop the design. When it is neither over-designed nor under-designed based on design and optimization requirement, the design is the final one.

The flow chart built in iSIGHT is shown in **Figure 2.15**.

2.3.2 Interface to Saber Circuit Simulation

The interface to Saber circuit simulation is provided through Saber script files: one for Saber Sketch, and the other for Saber Scope. This is because the circuit simulation includes two steps: circuit simulation that is carried out in Sketch, and performance measurement that is carried out in Scope. These script files contain Saber commands for setting up the analysis, measuring the performance, and calculating and recoding the power dissipation into a text file. The input to the iSIGHT is a Saber netlist file in which iSIGHT modifies the circuit parameters, and the output is the text file from which iSIGHT reads out the power dissipation of the devices.

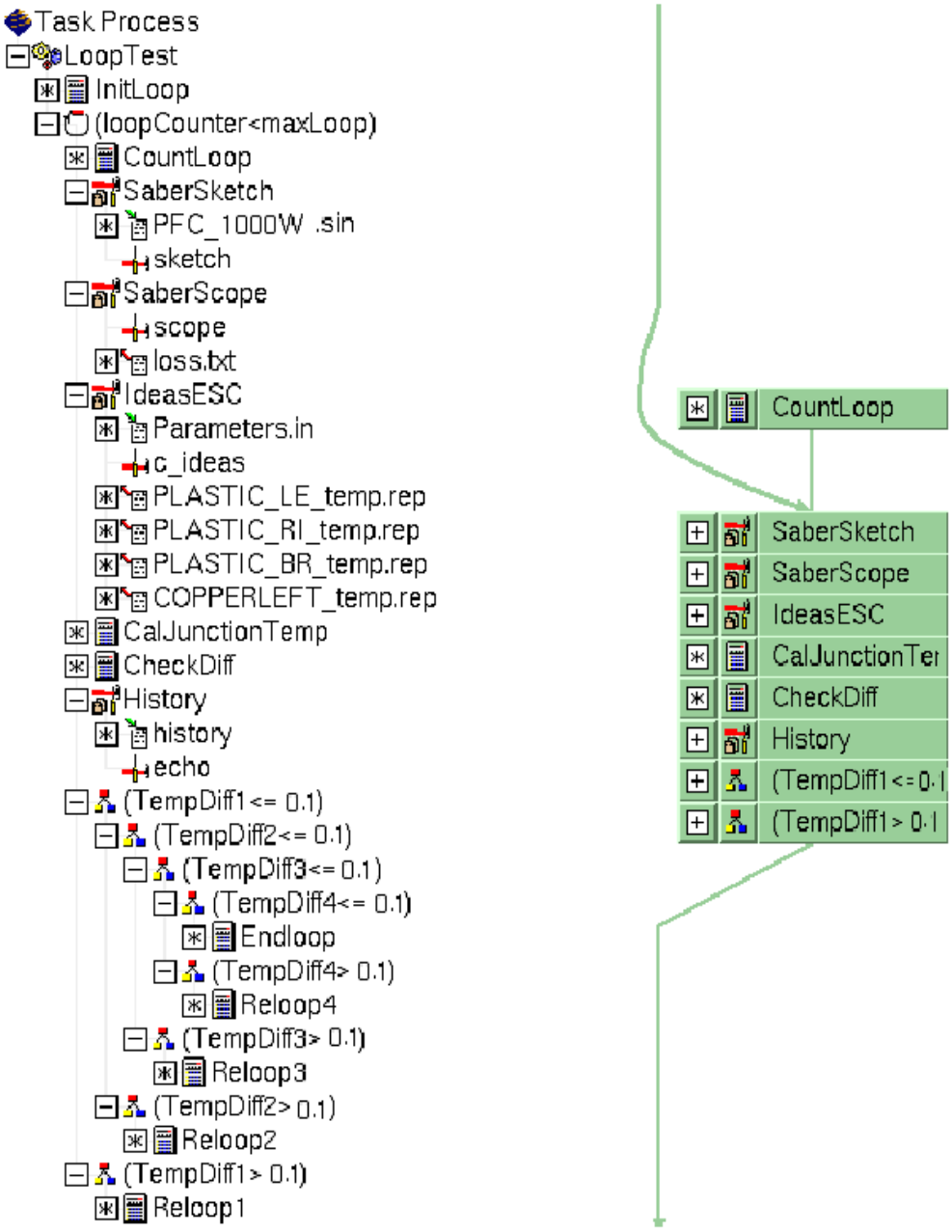


Figure 2. 15 Design process integration in iSIGHT.

2.3.3 Interface to I-DEAS Thermal Simulation

The interface to thermal simulation is provided through an in-house integration tool that is developed using Open I-DEAS API. This tool encapsulates the basic operations that are needed for parameter change and thermal simulation, and provide accesses to these operations through a simple format text file. The operations that are currently supported through this interface include: changing power dissipation parameters, modifying thermal boundary conditions, and generating temperature reports for given devices. For iSIGHT, the input file contains name-value pairs of the devices whose temperature are of interest. The outputs are text files recording device temperatures, and the values will be read into iSIGHT as shown in **Figure 2.15**.

As for now, the modeling approaches and integrated simulation environment will be used in the integrated electro-thermal design for a PFC converter and an integrated front end converter in DPS that will be discussed in Chapter 3 and 4.

Chapter 3.

Integrated Electro-thermal Design for a PFC Converter in DPS

3.1. Introduction

With the continuing industry trends towards smaller, faster, and higher power devices, thermal management is becoming increasingly important. After all, higher device performance can come at a price - higher temperatures and lower reliability - if thermal considerations aren't carefully weighed.

Not only are devices trending smaller but the system they consist of are also shrinking. Placing the units closer and closer together on smaller heat sinks and boards helps lower overall system size and cost, and improves electrical performance. As a result of improving power electronics system performance, the problem of heat dissipation from devices can no longer be ignored in the system level design for power electronics systems. That is, it has become imperative to carry out the thermal design before actual system fabrication.

For a power supply system, a dynamic design process is necessary to address both electrical and thermal issues. It is because the steady state temperatures of the system are obtained from loss-and-temperature iteration. Once a system solid body model is built, iterations between power loss and junction temperature calculations are performed to obtain the steady state temperature distribution. Since reliability and failure rate of

components are directly related to temperatures, an accurate model is critical to provide proper thermal management, which achieves maximum power density. All cooling-related data such as placement of components, airflow rate, heat sink size and device types are subjected to design changes in order to meet ultimately the temperature requirements. [35][36][37][38][39][40]

3.2. Electrical and Thermal Design Constraints

For the power factor correction stage, the most popular topology is the single switch CCM PFC, because of its simplicity and smaller EMI filter size. Due to the high conduction loss caused by the high voltage rating MOSFETs and the high switching loss caused by the severe reverse recovery problem of the boost diode, the efficiency of the converter is low. To improve the efficiency of this converter, extensive efforts for topologies have been taken and soft switching circuits have been developed. Although they can improve the converter's efficiency, because of their complexity, they are seldom adopted by the power supply industry. Therefore, low Rds(on) MOSFET and hyper-fast diode are needed to be chosen to keep circuit simple.

The cooling of electronics is often the least understood and most often ignored part of electronics design. All power electronics devices have a maximum operating junction temperature that cannot be exceeded. As for power devices, the maximum operating junction temperature is set to be 115ºC. This maximum operating junction

temperature is directly related to the maximum power dissipation. Device longevity is, in many cases, attributed to keeping its junction temperature within these limits. Therefore, thermal design optimization of power electronics systems is important in increasing the device longevity.

Understanding the thermal characteristics of power electronics systems such as a PFC converter is important for two primary reasons. The first is that maximizing the electrical performance of a PFC converter can adversely affect the thermal performance. In electrical analysis, we want to minimize the parasitic inductance in the layout. Parasitic inductance stores energy when the devices are turned on. However, this energy is released as a spike when the devices are turned off. As a function of current rate and inductance, the voltage spike increases as the current rate and parasitic inductance increase. With high parasitic inductance and high current flow rate, the high voltage spike can damage the power device easily. To improve long-term reliability, we have to reduce the parasitic inductance on the layout. One way to reduce the parasitic inductance is to reduce the etched copper area on the layout.

The second reason for understanding the thermal characteristics of a PFC converter is to predict reliability of the converter from the thermal performance. Thermal modeling is required to accurately identify hot spots and temperature distributions on the layout.

Commonly, the peak temperature at the device is referred to as the junction temperature.

For a PFC converter, the junction temperature is the peak temperature of the devices. The thermal analysis of a PFC converter is primarily a conduction problem. Radiation and convection are usually present when considering the use of a heat sink in the system. Nonetheless, the radiation effect is ignored in this optimization study. Conduction is dominant at the device level, and is the focus of this study.

In addition to the electrical constraints as discussed above, the packaging method also restricts the thermal performance of the converters. Using low thermal conductivity materials as interface materials can reduce the thermal performance of the power devices. [43][44][45]

3.3 Preliminary Design on Electrical and Thermal

The front-end of the DPS usually adopts a two-stage approach. The first stage accomplishes the power factor correction from a universal single-phase input line voltage (90~264Vac) while the second stage provides the isolation and tightly regulated DC bus voltage. Normally, a conventional single-switch CCM boost topology is used for the first stage because of simplicity as shown in **Figure 3.1**.

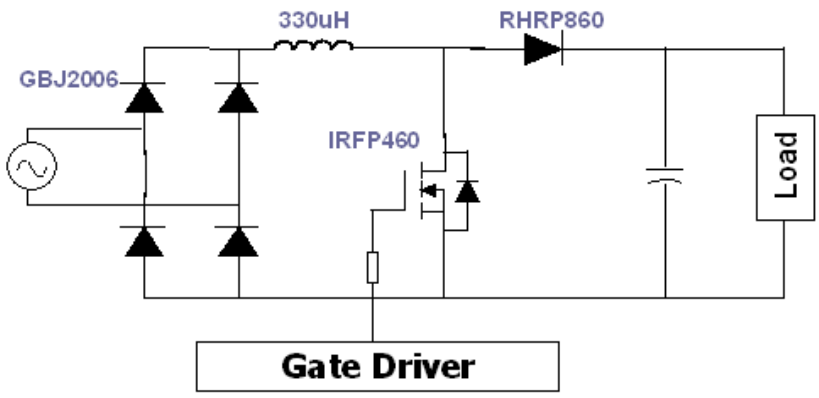


Figure 3. 1 Schematics for a single phase CCM PFC converter.

Accurate device loss models have been built in Saber and power losses under certain junction temperature are available. **Figure 3.2** and **Table 3.1** show power losses of two MOSFETs, boost diode, Diode Bridge and total device loss respectively. Power losses of MOSFETs and boost diode increase as junction temperature increases. Diode Bridge has the opposite property due to its negative temperature coefficient. Finally, the total device loss goes up greatly as junction temperature goes up.

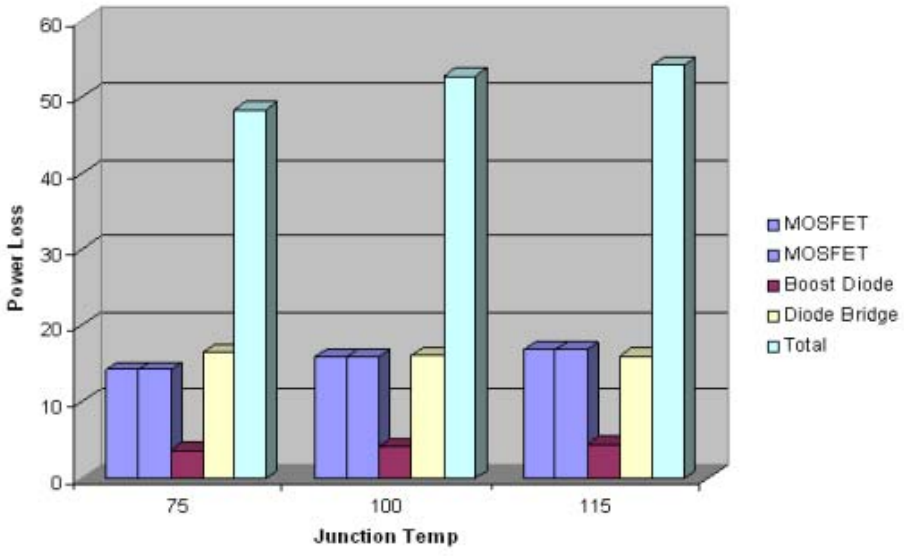


Figure 3. 2 Power loss breakdown in CCM PFC converter.

Table 3. 1 Power losses of power devices under different junction temperatures.

	Power Loss (W)				
	MOS1	MOS2	Boost Diode	Diode Bridge	Total
75°C	**14.16**	**14.16**	**3.64**	**16.42**	**48.38**
100°C	**15.85**	**15.85**	**4.09**	**16.12**	**52.72**
115°C	**16.88**	**16.88**	**4.38**	**15.98**	**54.12**

The high operating temperatures of transistors are frequent cause of failure. The high temperatures are caused by hot spotting, the tendency of current in a device to concentrate in areas around the source. Unchecked, this hot spotting results in the mechanism of thermal runaway, and eventual destruction of the device.

The on-resistance and switching loss of a power MOSFET increase with junction temperature. The power dissipated for a constant on-current increases, the junction temperature increases, the resistance and switching loss further increase until the device is in thermal equilibrium with the heat removal system. If the heat removal system is inadequate, thermal run away occurs. **Figure 3.3** shows the temperature distribution after single-step simulation and heat sink which MOSFET and boost diode are amounted on is over-designed. **Figure 3.4** comes out the "right" result after 10mm reduction of heat sink. Conventional thermal design often stops here because 116°C is within the design requirement 115°C±1°C. However, after doing mutual simulation by using integrated electro-thermal simulation tool, thermal runaway problem exists.

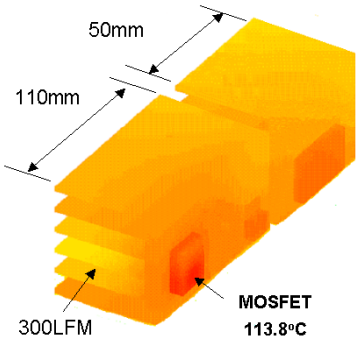


Figure 3. 3 Single step simulation results in I-DEAS with 110mm heat sink.

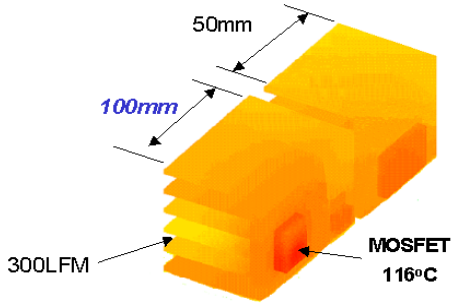


Figure 3. 4 Single step simulation results in I-DEAS with 100mm heat sink.

From **Figure 3.5** and **Figure 3.6**, junction temperature of power MOSFET goes up continually and at last thermally runs away first (150°C is the break down temperature for most power devices). Single-step simulation cannot see thermal runaway as illustrated in **Figure 3.4**. The existence of the problem can be found and effectively avoided by iterative simulation using integrated tool. After finding thermal runaway, the solution is to improve the cooling system by lowering the thermal resistance from junction to ambient.

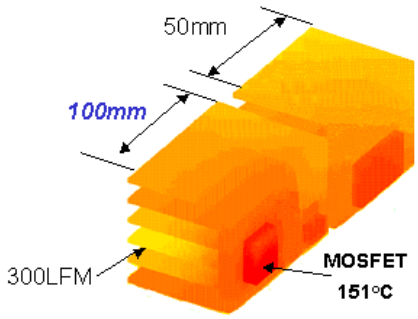


Figure 3. 5 Iterative simulation results in I-DEAS with 100mm heat sink.

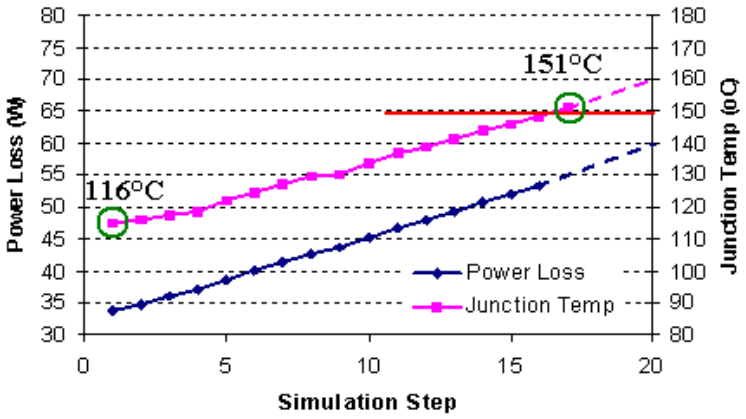


Figure 3. 6 Dynamic simulation process.

In this design, power MOSFET is the critical device because it dissipates more power loss than others and it is more sensitive to junction temperature. From **Figure 3.7,** the power losses of one single MOSFET as the main switch combine conduction loss with turn on loss due to reverse recovery loss of boost diode. Either conduction loss or turn on loss is greatly increased as junction temperature increases. Therefore, the power loss of MOSFET enhances 20% from 75^{o}C to 115 ^{o}C.

In order to reduce the hot spotting on MOSFET, MOSFETs can be operated in

parallel (shown in **Figure 3.8**) without fear that one device will rob current from the other . If any device begins to overheat, its resistance will increase, and its current will be directed away to the cooler chip.

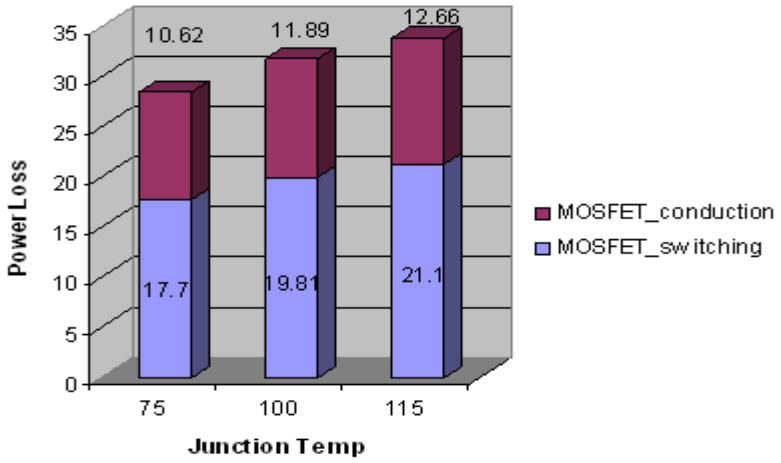


Figure 3. 7 Conduction and switching losses of two paralleling MOSFETs.

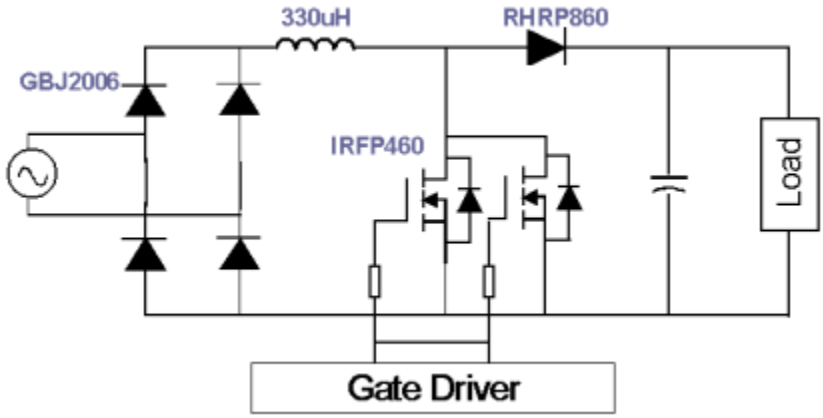
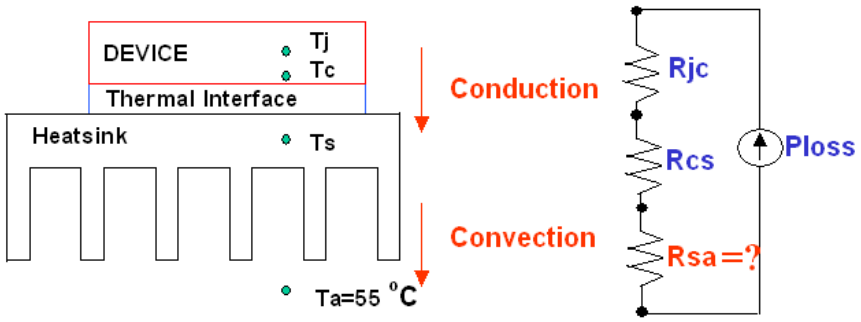


Figure 3. 8 Schematics for single-phase double-switch PFC converter.

In order to design a cooling system including heat sink and fan, calculation of thermal resistance from heat sink to ambient is needed. From thermal conductive path as shown in **Figure 3.9**, thermal resistance from junction to case of each device can be

attained in datasheets. Here Softface^{TM} is chosen as a cost-effective alternative to thermally conductive grease compounds. The thermal conductivity from datasheet is used directly to calculate the thermal impedance from case to heat sink, which depends on the area of each device as well.



(a) Partitioning of components on heat sink **(b) Thermal path**

Figure 3. 9 Models for thermal analysis.

Here Rjc is thermal resistance of device packaging from die to case, which can be got directly from datasheet; Rcs is thermal resistance from device case to base of heat sink, which is dependent on interface material and geometry; Rsa is thermal resistance from heat sink to ambient, which is determined by heat sink and heat sink-related fan's speed and position.

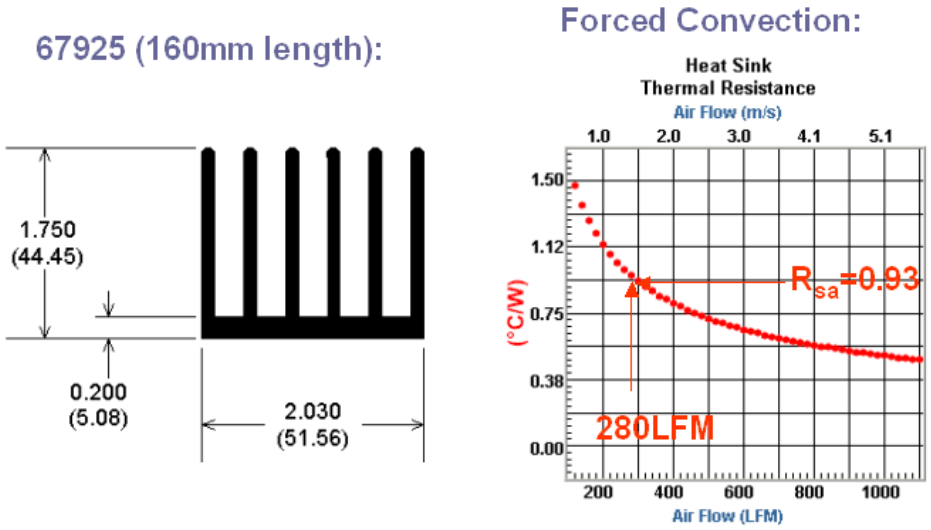
Table 3. 2 Temperature drop from junction to case for each device.

	MOSFET1	MOSFET2	Diode	DB
Ploss (W)	16.877	16.877	4.38	15.98
Rjc (°C/W)	0.4	0.4	1.2	0.4
Rcs (°C/W)	0.12	0.12	0.2	0.05
ΔTjs (°C)	8.7	8.7	6.1	7.2

The design of cooling system refers to the certain device, which has maximum temperature drop so as to guarantee all the devices have enough cooling condition to be under the maximum operating junction temperature 115^{O}C. From calculation **Table 3.2**, the critical device is MOSFET. So the maximum heat sink thermal resistance can be got as:

$$R_{sa} = \frac{T_{j(\max)} - \Delta T_{jS} - T_{A(\max)}}{Power_{Total}} = \frac{115 - 8.7 - 55}{16.877 + 16.877 + 4.38 + 15.98} = 0.93 \qquad (3.1)$$

Here, we assume the power loss distributes on heat sink uniformly and the maximum ambient temperature is 55^{O}C.



(a) Geometry of the selected heat sink **(b) Thermal resistance of heat sink vs. airflow**

Figure 3. 10 Cooling system analysis and design.

Based on design requirements, which include height and width of the heat sink, geometry of the fan and maximum airflow (usually 300LFM), a cooling system including a heat sink and a fan, as shown in **Figure 3.10**, can be selected according to thermal resistance from heat sink to ambient.

The thermal modeling techniques employed for analytical evaluations included I-DEAS Design Modeler and ESC. The Design Modeler was used to model individual parts. Three-dimensional geometric numerical models were used for all components in the physical structure. To improve the accuracy of the results, all available details were included in the model. Each model was mounted on an aluminum heat sink. To provide airflow over the model, a flow channel was included, with a constant volume flow rate of 280LFM at one end of the channel. The other end of the channel was vented to an ambient temperature of 55ºC. Diode Bridge, two MOSFETs and boost diode are arranged based on power flow direction. , A 3D solid model for CCM PFC converter is shown in **Figure 3.11.** The top of the module was assumed to be adiabatic since the actual physical module was encapsulated. After setting up the simulation conditions, I-DEAS calculated about one hour to get the result in the SUN workstation with 2GHz CPU and 1GB memory. The temperature distribution of CCM PFC converter is illustrated in **Figure 3.12**.

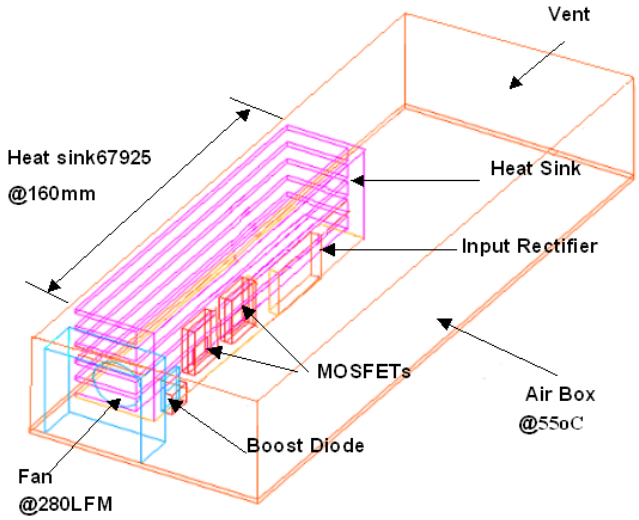


Figure 3. 11 Thermal models and boundary conditions.

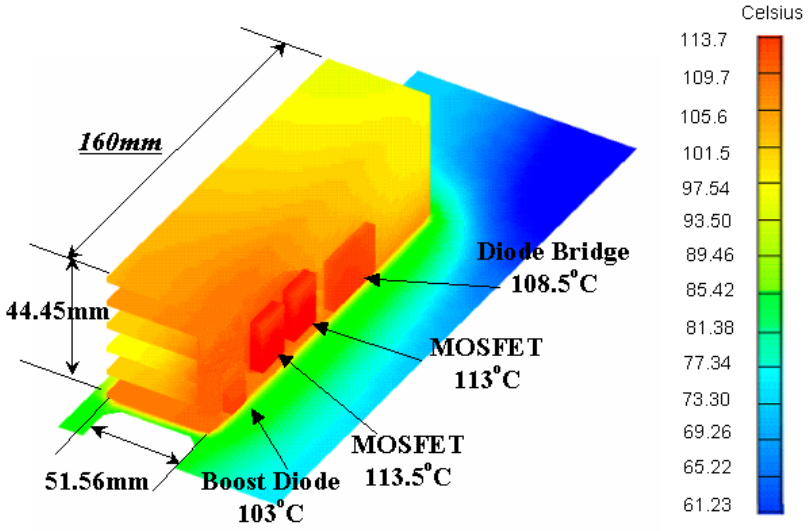


Figure 3. 12 Temperature distribution for the PFC converter.

From **Figure 3.12**, MOSFETs are much hotter than the other components of the system. From electrical point of view, it is easy to see that two MOSFETs dissipate about 17W loss respectively. And from a thermal standpoint, the MOSFETs are receiving heat

from the hot air that passes over the boost diode (which is emitting 4.38 W of heat). Furthermore, from a fluid dynamic viewpoint, the boost diode is blocking the MOSFETs from a substantial amount of airflow.

Hence, two MOSFETs should be put as close as possible to the fan so that the large amount of surface area associated with the MOSFETs close proximity to the fan. The boost diode is arranged next to the MOSFETs in order to reduce parasitic inductances. Diode Bridge is dissipating nearly 16W power, which contributes a big part of total heat. When junction temperature increases, its power loss decreases. Therefore, Diode Bridge is put further from the fan compared to other components because of its total negative temperature coefficient.

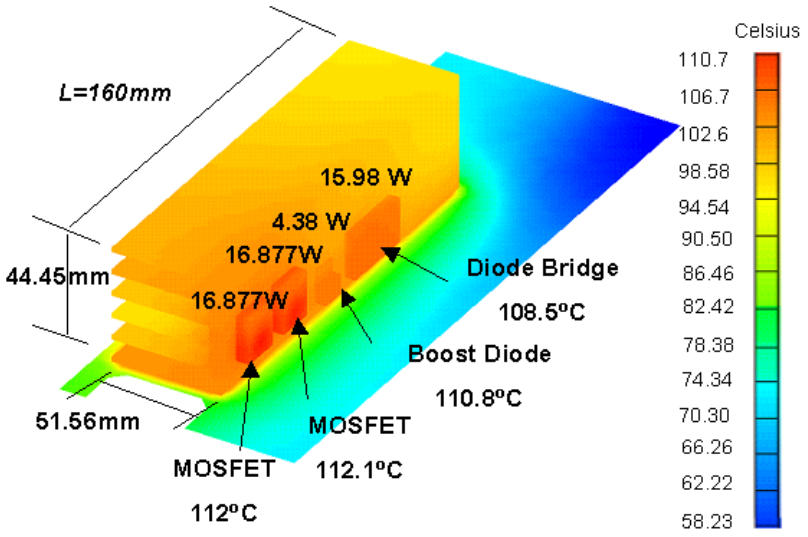


Figure 3. 13 Temperature distribution after single-step simulation.

Through re-arranging the positions of components amounted on heat sink, the layout is improved. After I-DEAS's calculating, a new temperature distribution is

illustrated in **Figure 3.13**. There is no hot spot existing any more and all temperatures of components are well under 115°C. Many electrical and thermal designers stop the design here because they assume this is the steady state temperature distribution and accept the "little" margin.

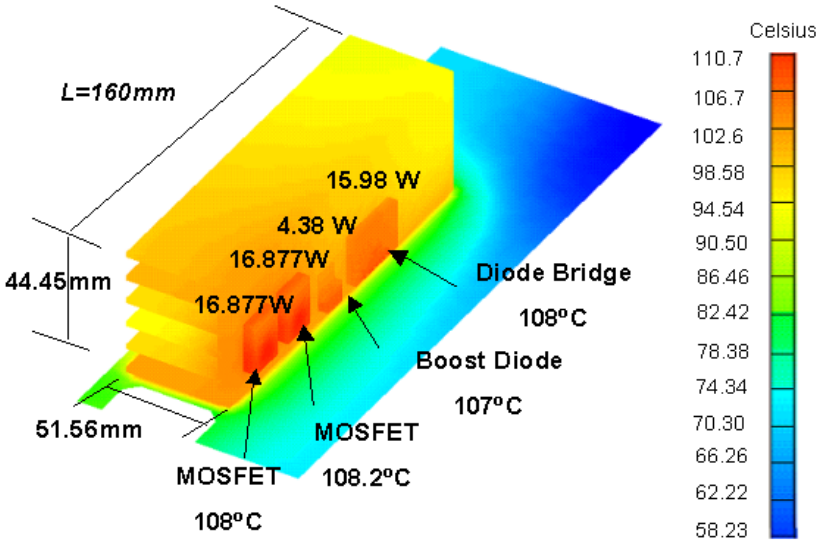


Figure 3. 14 Temperature distribution after iterative simulation.

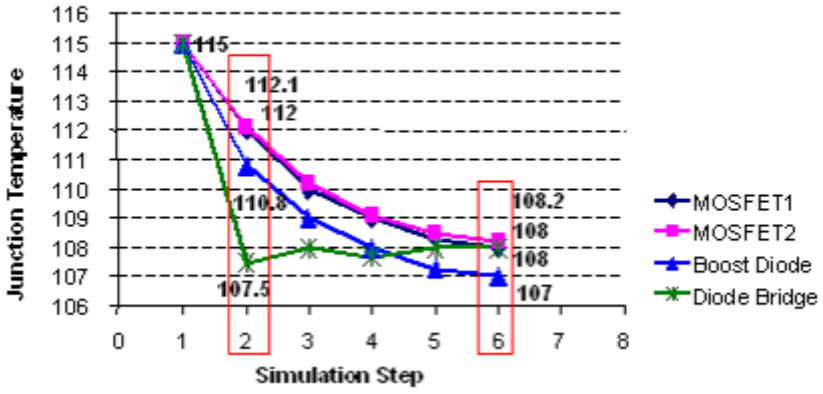


Figure 3. 15 Iterative simulation process.

However, after executing iterative jobs, which rerun the electrical and thermal simulation and validate results until get to the real steady state using integrated

simulation tool introduced in Chapter 2, from dynamic electro-thermal simulation curve (**Figure 3.15**), the following temperature points after initial 115°C are indeed the unreal "steady state" obtained from single-step electrical and thermal simulation. After four iterative simulation steps, the final steady state can be attained. And the difference between them is almost 4 degrees. From **Figure 3.16**, the critical components---two MOSFETs have the considerable change of power losses about 7.7%.

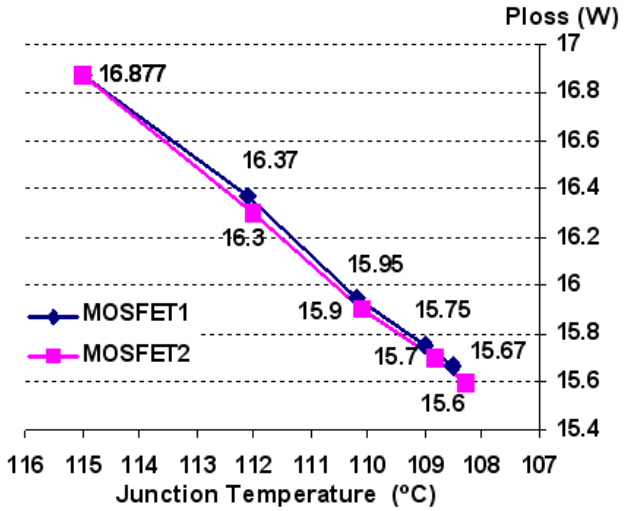


Figure 3. 16 Dynamic process of power loss and junction temperature for MOSFET.

From **Figure 3.14**, heat sink is obviously over designed because all the components are under 110°C and the margin is not "little" any more. Besides, the temperature does not distribute evenly on the heat sink. The area of the heat sink where the components focus on is much hotter than the area far from the components. Re-design procedure is needed to search for the right design of systems. Conventionally, non-integrated electro-thermal design method is used as described in Section 3.4. We propose integrated electro-thermal design method in Section 3.5.

3.4 Non-integrated Electro-thermal Design

Generally, the task of a thermal designer of power systems is to meet the thermal specifications. The objective of thermal management is to ensure that the temperatures of all components in a system are maintained within functional limits. The functional temperature limit is the range within which the electrical circuits can be expected to meet their specified performance requirements. Operation outside the functional limit can degrade system performance, cause logic errors or cause component and system damage. Temperatures exceeding the maximum operating limits may result in irreversible changes in the operating characteristics of the component. The design process can be explained in flow chart as shown in **Figure 3.17**.

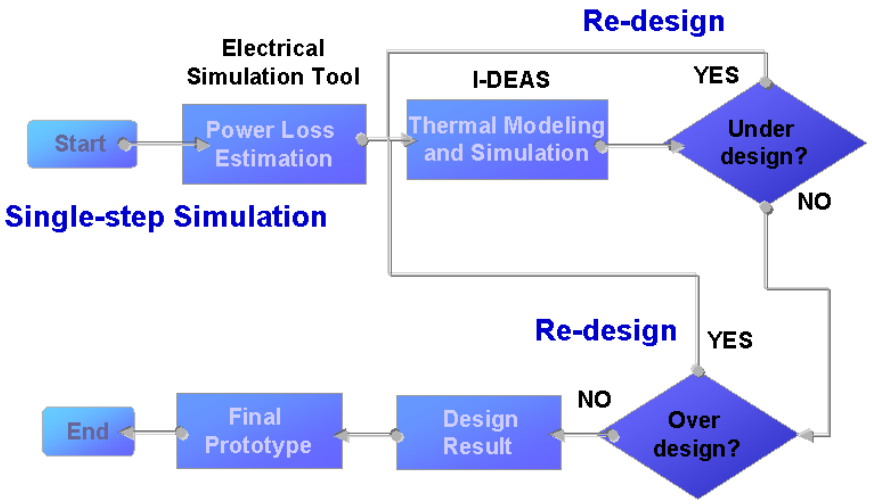


Figure 3. 17 Flow chart for non-integrated electro-thermal design.

The object of designing a CCM PFC converter is to keep devices operating within the range of maximum operating temperature 115ºC±1ºC and arrange the necessary heat transfer paths to the environment. The design begins with power loss

calculation for each device under maximum operating junction temperature 115^{o}C. Conventional method to calculate the power loss is usually spreadsheet hand calculation or PSPICE simulation. Neither spreadsheet nor Pspice is accurate to predict the power dissipation of devices due to lack of the more detailed models. Assume that advanced modeling techniques in Saber as discussed in Chapter 2 are used by non-integrated electro-thermal design method. Power losses of devices are used as heat sources to design the cooling system including heat sink and fan. Using I-DEAS, junction temperatures of devices can be attained to evaluate the cooling system. If any device temperature is out of the range 115^{O}C±1^{O}C, cooling system design is over-designed or under-designed, that is, bad design. Redesign the cooling system is needed.

While keeping the same fan and same airflow, the length of heat sink should be changed to meet design requirement. But how much heat sink should be varied? The considerations for length of heat sink are required.

The published extrusion data from thermal products (see **Table 3.3**) shows the relationship between thermal resistance and length of heat sink with fixed height and width and same airflow. Thermal resistance changes almost linearly with length as black curve shown (see **Figure 3.18**).

Table 3. 3 Heat sink thermal resistance vs. length.

Heat Sink Length	120mm	125mm	130mm	135mm	140mm	145mm
Rsa	1.068oC/W	1.046oC/W	1.026oC/W	1.007oC/W	0.989oC/W	0.971oC/W
Heat Sink Length	150mm	155mm	160mm	165mm	170mm	
Rsa	0.955oC/W	0.94oC/W	0.925oC/W	0.911oC/W	0.897oC/W	

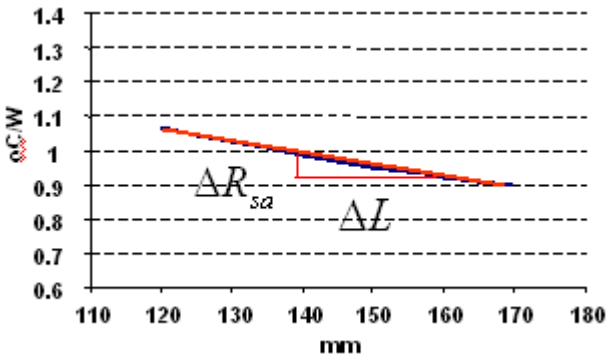


Figure 3. 18 Heat sink thermal resistance vs. length curve (Black) and fitting curve (Red).

Hence, linear curve fitting curve (red one) can be helpful to get equation (3.2).

$$\Delta R_{sa} = -0.005\Delta L \tag{3.2}$$

R_{sa} is the thermal resistance from heat sink to ambient; L is the length of heat sink.

From basic heat transfer function:

$$T_j - \Delta T_{js} - T_a = P \cdot R_{sa} \tag{3.3}$$

T_j is junction temperature of device; ΔT_{js} is temperature difference from junction to heat sink; T_a is ambient temperature; P is power loss.

The design objective is 115°C for device. So from equation (3.3), we can get the expression:

$$115 - T_j = P \cdot \Delta R_{sa} \tag{3.4}$$

ΔR_{sa} means heat sink thermal resistance difference.

Now, replacing ΔR_{sa} with ΔL using the relationship between heat sink thermal resistance and length as function (3.2) leads to

$$115 - T_j = -P \cdot 0.005 \cdot \Delta L \tag{3.5}$$

ΔL is the change of heat sink's length. Until now, expression (3.5) can be used to decide how much heat sink should be changed to reach the design objective.

From Figure 3.13, the highest junction temperature belongs to one of MOSFETs (112.1°C). So it is selected to decide how much heat sink can be lessen and under-design should be avoided at the same time.

$$115 - 112.1 = -P \cdot 0.005 \cdot \Delta L \tag{3.6}$$

The solution is:

$$\Delta L = -11mm \tag{3.7}$$

ΔL is minus, which means reduction of heat sink to rise the temperature. In non-integrated electro-thermal design method, next step is to cut 11mm, that is, heat sink becomes 149mm.

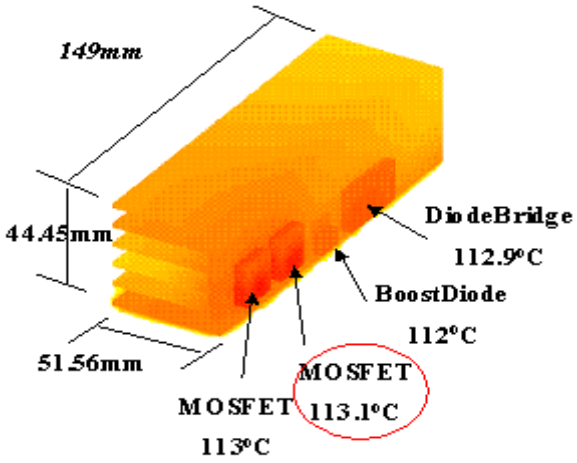


Figure 3. 19 Single-step simulation result after first heat sink's cut.

After first cutting, non-integrated electro-thermal design method got one-step simulation results as shown in **Figure 3.19** and highest temperature is 113.1°C. In order to reach the objective of 115°C, cutting based on non-steady state is continuing.

$$115 - 113.1 = -P \cdot 0.005 \cdot \Delta L \tag{3.8}$$

The solution is:

$$\Delta L = -6mm \tag{3.9}$$

Non-integrated electro-thermal design method needs heat sink's reduction of 6mm. As temperature is rising to reach the objective of 115°C, the adjustment becomes slighter and slighter. After ninth cutting, non-integrated electro-thermal design finally got its design objective. However, due to the unreal "steady state" temperatures, it cannot decrease the heat sink to the minimum and stopped at 133mm as shown in **Figure 3.20**.

For every cutting, a new 3D model for heat sink and finite element analysis are rebuilt in I-DEAS, which needs 120 minutes. Running thermal simulation for one time is about 120 minutes. However, running electrical simulation in Saber once is about 10 minutes because after getting the steady state one line cycle is enough to calculate power losses. Besides, non-integrated electro-thermal design does not use integrated simulation tool and needs 5 minutes to transfer data before every simulation. Critical junction temperature, which determines the cutting of heat sink, cutting length of heat sink and time for each design cycle are tabulated in **Table 3.4.** It also shows the final heat sink is 133mm long and total design time is 2330 minutes (green row).

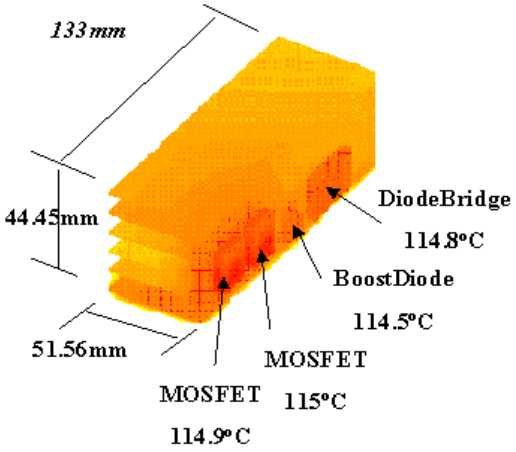


Figure 3. 20 Single-step simulation result after ninth heat sink's cut.

Table 3. 4 Critical parameters in each design cycle.

Design Cycle	Junction Temp	Length of Heat sink	Time
		160mm	125mins
1	112.1°C	-11mm	245mins
2	113.1°C	-6mm	245mins
3	114°C	-3mm	245mins
4	114.3°C	-2mm	245mins
5	114.5°C	-1mm	245mins
6	114.6°C	-1mm	245mins
7	114.7°C	-1mm	245mins
8	114.8°C	-1mm	245mins
9	114.9°C	-1mm	245mins
	115°C	133mm	2330mins

3.5 Integrated Electro-thermal Design

As shown in **Figure 3.21**, integrated electro-thermal design begins with Saber electrical simulation. Power losses of each device are obtained under maximum operating temperature 115°C using more accurate loss models and parasitic models in Saber. These power losses determine the selection of heat sink and fans and the procedure is same as non-integrated electro-thermal design. After building thermal models in I-DEAS, power losses as heat sources are input to each module in I-DEAS and junction temperatures as output are obtained after single-step simulation. Junction temperature of each device needs to go back to Saber to calculate power loss again considering the complete electrical versus thermal dependencies using automatic integrated simulation tool until the loop reaches the steady state. Similar as non-integrated, whether it is under-design or over-design is needed to judge in integrated electro-thermal design. Unlike the non-integrated design, the integrated electro-thermal design is based on real steady state after iterative simulation to decide re-design. This is a reliable, design-effective electro-thermal design solution.

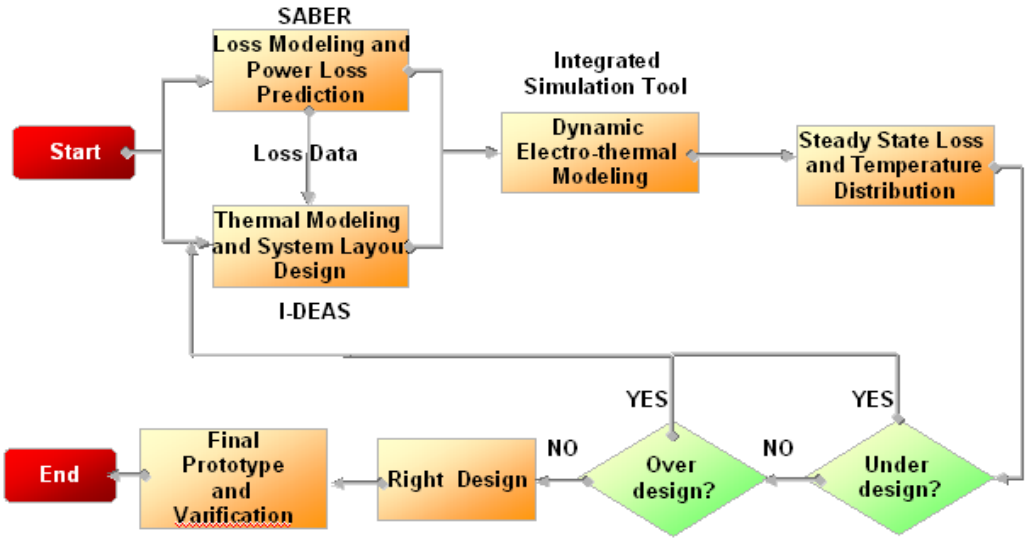


Figure 3. 21 Flow chart for proposed integrated electro-thermal design.

From **Figure 3.14**, the highest junction temperature belongs to one of MOSFETs (108.2°C).

$$115 - 108.2 - P \cdot 0.005 \cdot \Delta L \tag{3.10}$$

The solution is:

$$\Delta L = -25mm \tag{3.11}$$

In integrated electro-thermal design method, next step is to cut 25mm, that is, heat sink becomes 135mm. After iterative simulation, it reaches the steady state. **Figure 3.22** shows the steady state temperature distribution after first time cut. **Figure 3.23** illustrates the iterative simulation process for this design cycle.

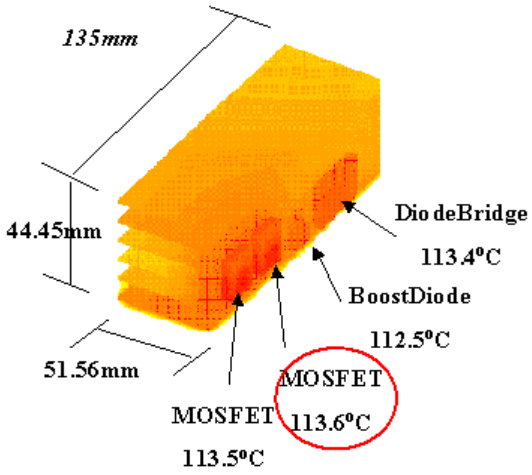


Figure 3. 22 Iterative simulation result after first heat sink's cut.

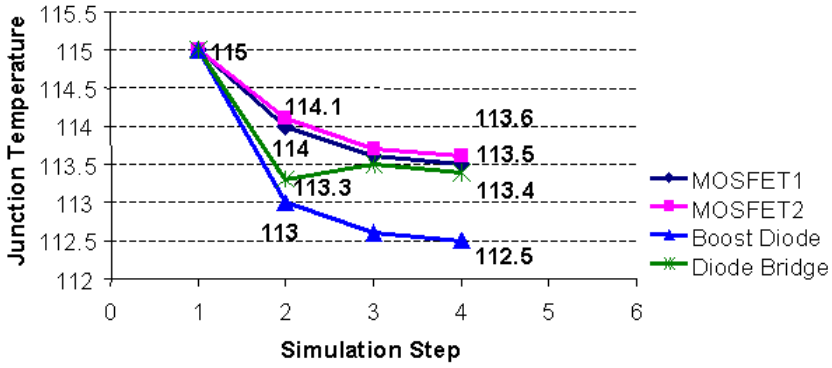


Figure 3. 23 Iterative simulation process.

After second cutting and running the iterative simulation, with integrated electro-thermal design method components get to around 115°C and temperature is uniformly distributed on the heat sink. So the objective is implemented and the design is finished. **Figure 3.24** shows the steady state temperature distribution after second time cut. **Figure 3.25** illustrates the iterative simulation process for this design cycle.

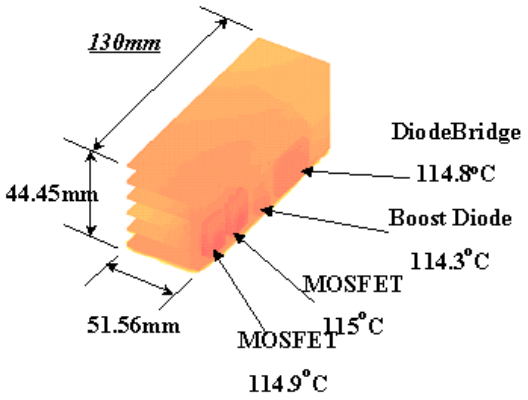


Figure 3. 24 Iterative simulation result after second heat sink's cut.

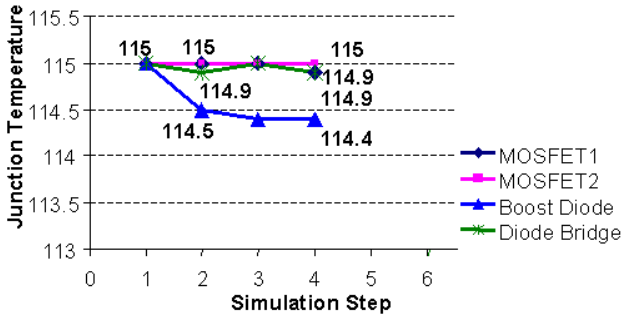


Figure 3. 25 Iterative simulation process.

Critical junction temperature, which determines the cutting of heat sink, cutting length of heat sink and time for each design cycle are tabulated in **Table 3.5.** It also shows the final heat sink is 130mm long and total design time is 1640 minutes (green row).

Table 3. 5 Critical parameters in each design cycle.

Design Cycle	Junction Temp	Length of Heat Sink	Time
		160mm	640mins
1	108.2°C	-25mm	500mins
2	113.6°C	-5mm	500mins
	115°C	130mm	1640mins

3.6 Comparison between Integrated and Non-integrated Design Methods

A. Design cycle

From **Table 3.4** and **Table 3.5**, in order to achieve the right design, non-integrated design spends nine design cycles about 2330 minutes, nevertheless, integrated design just spends two design cycles about 1640 minutes, which decreases 30%. Both of design methods use SUN workstation to do electrical and thermal simulations as previous discussion.

B. Heat sink

A conventional thermal designer usually uses spreadsheet calculate power losses of devices and design systems. The design results are always left big margin to avoid under design. For CCM PFC converter, 160mm heat sink is selected after hand calculation. Using integrated electro-thermal design method with automatic simulation tool can accurately predict the steady state power dissipation and temperature distribution. Finally, heat sink reduces 19%. Non-integrated electro-thermal design method executes the redesign with help of advanced modeling techniques. However, non-integrated design lack of electro-thermal interaction considerations and spend plenty of time to find the "right" design ---133mm heat sink. Using integrated electro-thermal design method with automatic simulation tool further reduced heat sink 2% just consuming much less time. **Figure 3.26** shows a single-phase double-switch PFC converter on the bench. This converter can work well using 130mm heat sink. The layout is a little bit different from

our electro-thermal optimal design because the thermal issue did not be considered completely.

Figure 3. 26 Hardware for single-phase CCM PFC converter.

Chapter 4.

Integrated Electro-thermal Design for an Integrated Front end Converter in DPS

4.1. Introduction

In the telecommunication and computing application, which is one of major power electronics product markets, the distributed power system (DPS) structure is widely adopted. A number of front-end converter modules are paralleled in order to obtain N+1 redundancy for the purpose of system reliability and easy power upgrade. [45]

Industry companies are under constant pressures to produce the front-end products more powerful, higher power density, and less expensive to the customers. Despite all these requirements, the front-end converter products to date are essentially custom-designed and manufactured using discrete parts, which increase labor and ultimately cost of power electronics equipment. In addition, some fundamental limits start to show up when the higher frequency operation is desired. For example, the parasitic inductance in the switch commutation loop hampers the switching speed and causes more switching losses. The parasitic capacitance between high voltage transition points to the earth ground affects the common-mode noise. Moreover, the parasitics

brought by the interconnection of the electrical layout played a negative role in the system electromagnetic interference (EMI) noise if it is not treated carefully.

To address these issues and significantly improve the performance of the power electronics product, the integrated power electronics module (IPEM) concept was proposed by the Center for Power Electronics Systems (CPES) at Virginia Tech. Following the concept, the integration efforts have been made for the front-end DPS converter. By extensive use of CAD tools, integrated electro-thermal design methodology has been applied to the integrated DPS testbed design. The computer-aided integrated DPS system design procedure is shown in **Figure 4.1**. The 3-D thermal model was employed in I-DEAS to compare different thermal management schemes. The parasitic of electrical layout was extracted via Maxwell Q3D and included into the electrical simulation in SABER to study its effect on the stress, the losses and the EMI noise. After iSIGHT's automatic loop, the optimal layout is obtained to make final prototype on bench.

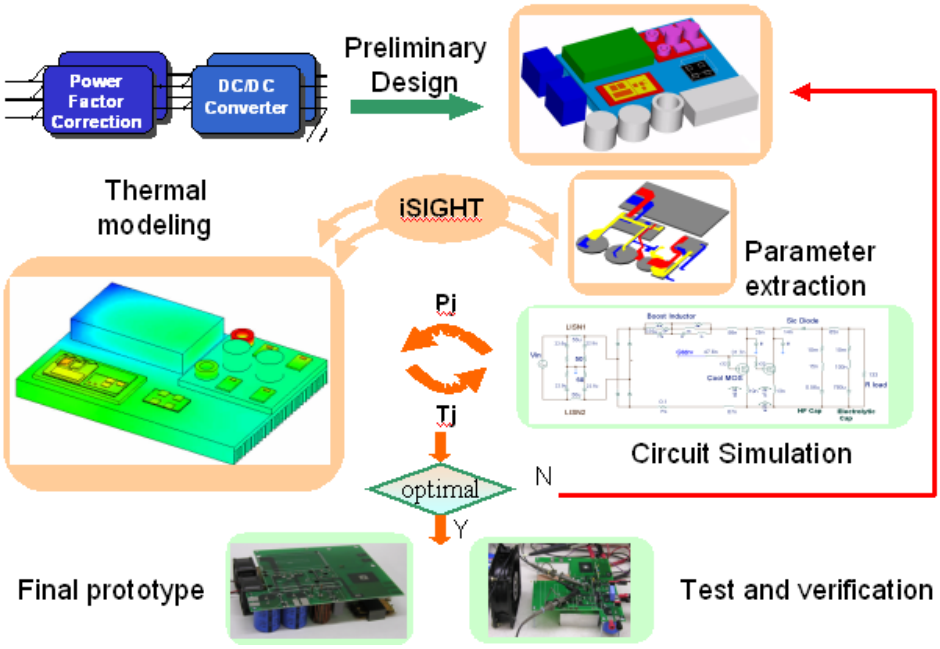


Figure 4. 1 Integrated DPS test bed design process using integrated simulation environment.

4.2. Integrated Power Electronics Modules (IPEMs)

The Generation I active integrated power electronics module (IPEM), consisting of two MOSFETs in bare die form and a hybrid gate driver, is packaged using "embedded power" technology, a hybrid MCM-based packaging technology. The two bare chips of MOSFETs are buried in a ceramic frame, and covered by a dielectric layer with etched holes over the aluminum pads of the chips. The power devices are interconnected to the rest of circuits by metal deposition. This new package method eliminates wire bonds, which could lead to potential benefits from parasitic parameters perspectives.

Meanwhile a passive IPEM, which integrates three inductors, two DC blocking capacitors, and two transformers, was designed. Both active IPEM and passive IPEM

were fabricated and demonstrated in the AHB DC/DC converter. An improved version of Generation II active IPEM was developed to include the PFC switch (CoolMOS), the boost diode (SiC diode), two DC/DC switches, their associated gate drive circuitry, and a high frequency 0.56uF bus clamping capacitor. This active IPEM greatly simplified the interconnections, thus, leading to minimal parasitic inductance of major commutation paths in the circuit. Not only did it offer smaller package size but also lowered switching losses. In addition to the improvement in the active IPEM, the integrated EMI filter similar to the integrated passive LCT (inductors, capacitors and transformers) techniques used in DC/DC converter is under development at present. In a summary, **Figure 4.2** illustrates the major IPEMs used in the integrated DPS testbed.

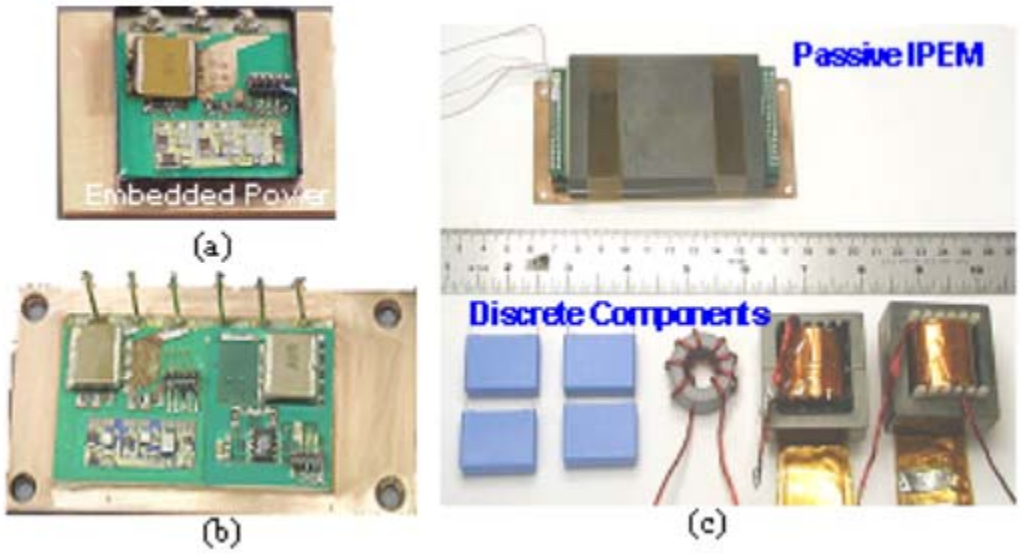


Figure 4. 2 IPEMs applied to the integrated DPS testbed.

(a). Generation I Active IPEM; (b). Generation II active IPEM; (c). Passive IPEM v.s. discrete components.

The PFC plus AHB DC/DC converter using IPEMs was developed and showed the effectiveness of the developed integration techniques. It is expected the power density can reach 11.7 W/in^3. Eventually with the IPEM approach, the integrated converter can be conceptualized in **Figure 4.3**. Except a few components like electrolytic capacitors, the major portion of the integrated DPS testbed will be composed of various IPEMs.

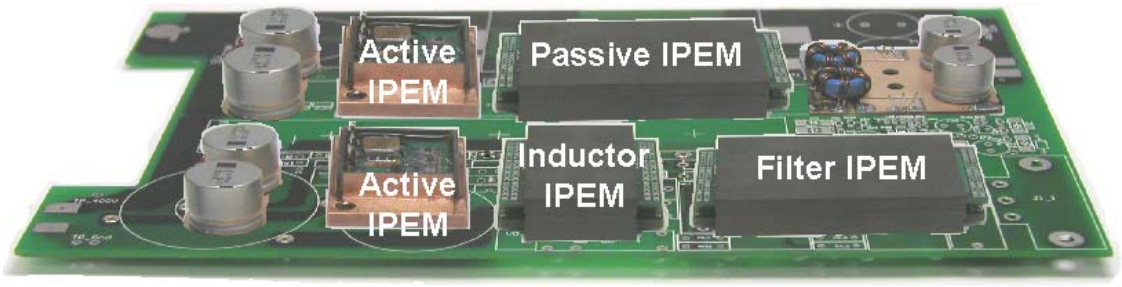


Figure 4. 3 The conceptualized integrated DPS testbed.

4.3 Dynamic Electro-thermal Modeling for an Integrated Converter

Usually a DPS front-end converter is composed of two stages, PFC (power factor correction) stage and DC/DC stage, as shown in **Figure 4.4**. The PFC stage converts the single-phase AC line voltage to about 400 Vdc and the DC/DC stage converts 400 Vdc to 48 Vdc, which can supply variety of the load converters.

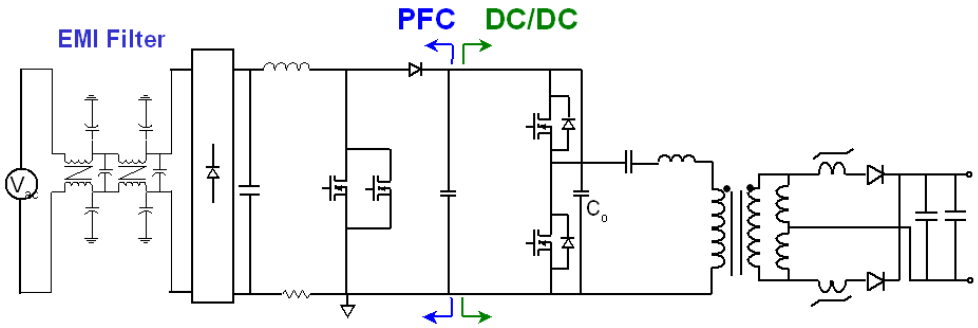


Figure 4. 4 Schematics for a front-end converter.

For the power factor correction stage, the most popular topology is the single switch CCM PFC, because of its simplicity and smaller EMI filter size. The recent study shows the good characteristics brought by CoolMOS and SiC diode could lead to superior performance in PFC converter and still keep the circuit simplicity, which gives a desirable solution for the PFC stage.

With the need of increasing the power density, the switching frequency of converter is desired to be higher. The frequency effects analysis on the EMI filter size has indicated that the EMI filter requirement does not start to reduce until the switching frequency is increased above 400 kHz. Therefore the single-switch continuous current mode (CCM) PFC converter is chosen and designed with the using of CoolMOS and SiC diode at the switching frequency of 400kHz.

Among many candidates for the DC/DC stage, the asymmetric half-bridge (AHB) PWM DC/DC converter is chosen due to simple topology and the soft-switching capability. 500V 21A MOSFET IXTH21N50 is chosen to implement the converter. Complete device models used in Saber simulation are shown in **Figure 4.5** and listed in

Table 4.1.

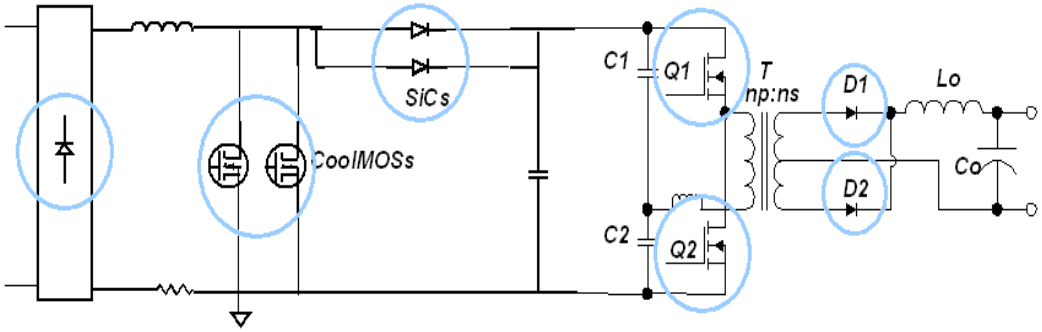


Figure 4. 5 Device models used in the simulation of a front-end converter.

Table 4. 1 Device models built in Saber.

Name	*Type*	*Model*
CoolMOS	SPW20N60C3	Infineon's SABER model
SiC	SDP06S60	Diode tool model in SABER
Output MOSFETs (Q1,Q2)	IXFH21N50	"IXFH21N50_sl" in SABER library
Output Diodes (D1,D2)	STTH3003C	"power diode" in SABER library
Input Rectifier	GBJ2006	"Gp30j_sl" in SABER library

It is known that the parasitic inductance in the switching commutation path is important to the switching losses and the ringing amplitude, especially at turn-off. By integrating bare dies of switching devices together using planar integration technology, it can be expected that the parasitic inductance due to packaging be greatly reduced. In discrete component-based design, the high frequency decoupling capacitor is paralleled with the dc link electrolytic capacitor and physically installed at the device terminals. By

integrating the capacitor into the package, the interconnection from the capacitor to PFC and DC/DC switch is simplified and the decoupling effect is improved.

Besides the concern of the parasitic inductance in the power path during switching commutation, the common source inductance between gate driver path and the main power path affects switching loss greatly too. During turn-on, the voltage drop on the common source inductance dynamically reduces the net voltage applied to the gate of MOSFET die, the switching speed is slowed down and this limits the switching loss reduction. Similarly, the common inductance impedes the turn-off process. Integrating the gate driver circuitry along with the devices further reduces the effective gate driver loop inductance. The detailed parasitic inductances in active IPEM are extracted by impedance analyzer from measurements and are completely modeled into SABER as shown in **Figure 4.6**.

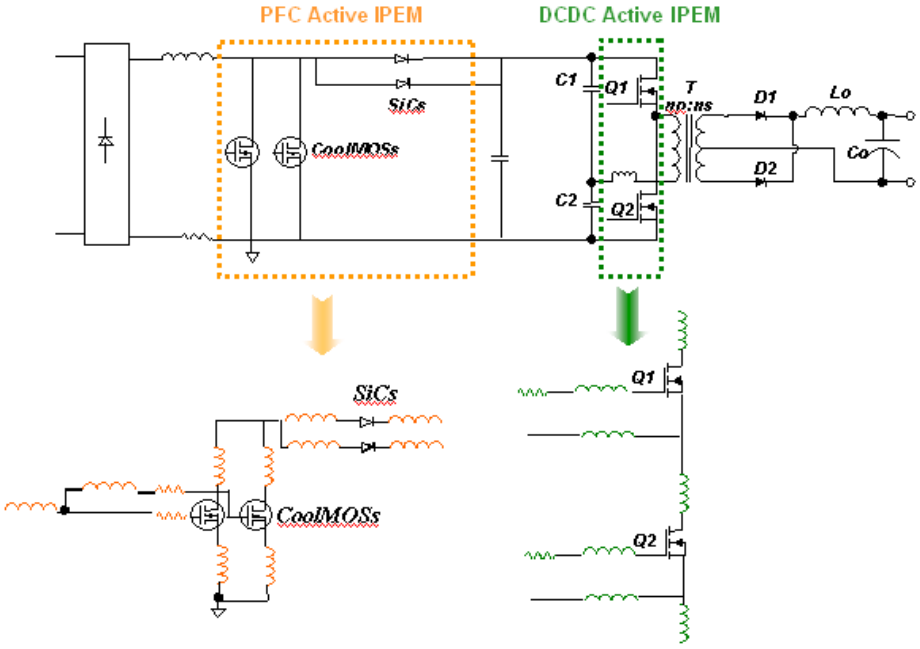
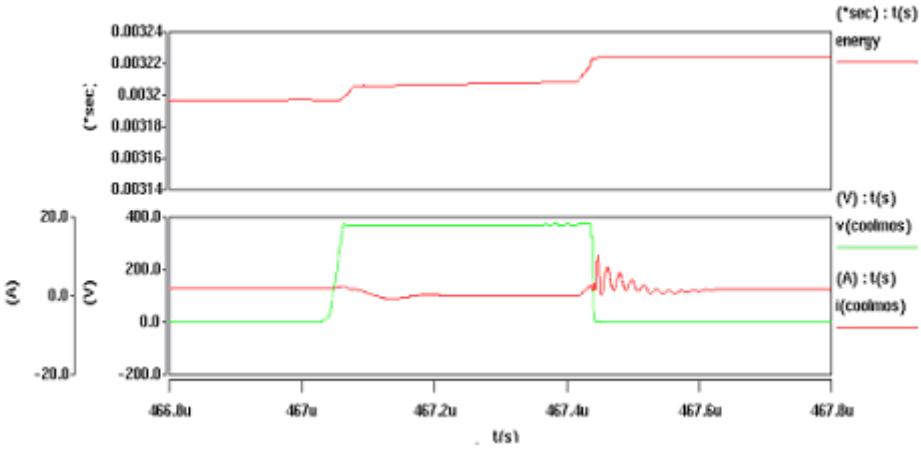
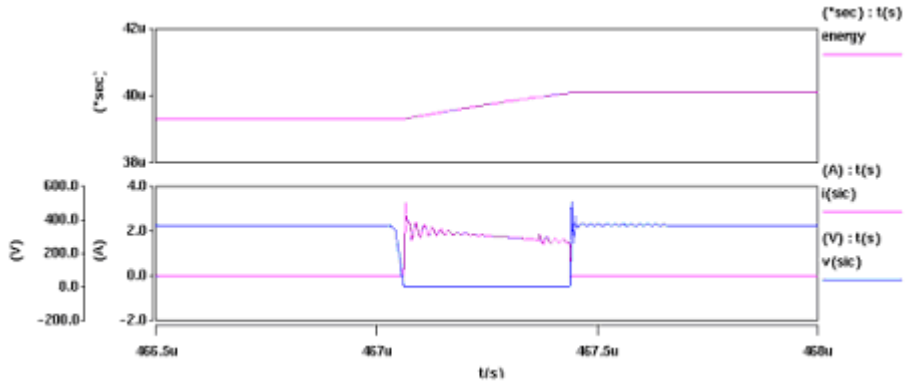


Figure 4. 6 Detailed parasitic modeling for active IPEM.

Combing the device models with parasitic models and layout models, the simulated switching waveforms of power devices are gotten in **Figure 4.7** and **Figure 4.8**.



(a)



(b)

Figure 4. 7 The switching waveforms of devices in PFC part.

(a) The turn-on, turn-off and energy waveforms of CoolMOS; (b) The turn-on, turn-off and energy waveforms of SiC.

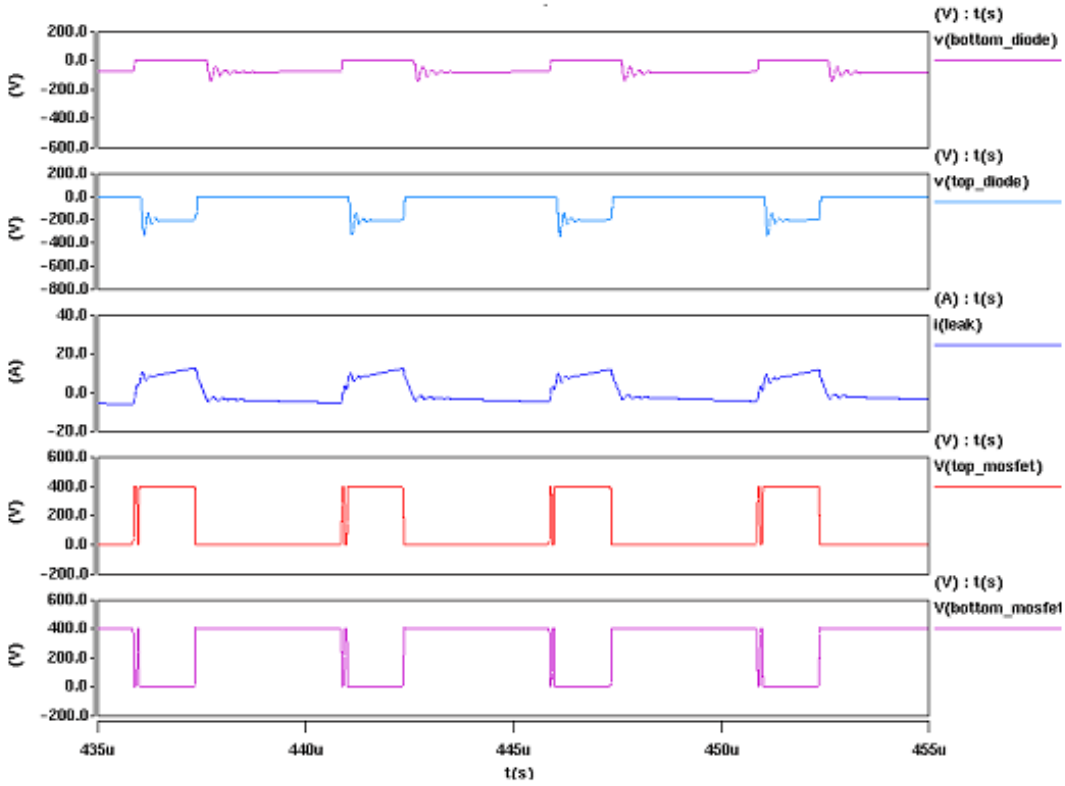


Figure 4. 8 The switching waveforms of devices in DC-DC part.

After attaining the voltage and current waveforms of power devices, the power losses can be calculated by Saber according to the expression:

$$P_{loss} = \frac{Integr(v \cdot i)}{T_{cycle}} \tag{4.1}$$

And the power losses of devices in simulation are compared with those in experiment as **Table 4.2.** They match well.

Table 4. 2 Power loss breakdown in simulation and experiment.

	Simulation	*Calculation*
PFC CoolMOSs	20W	22.8W
PFC SiCs	4W	4.7W
Input Rectifier	12W	11W
DC/DC switches	13W	14W
Output Diodes	12.1W	13W
P-IPEM	31.5W	25W

The system thermal models are needed to build in I-DEAS based on integrated electro-thermal simulation environment. The system layout that was proposed for the converter is shown in **Figure 4.9**. The components that make up the power converter are assembled into a 207.5 mm x 160 mm x 44 mm box. As shown in **Figure 4.9**, the main parts of the converter are the active IPEM (active Integrated Power Electronics Module), the passive IPEM, the output components, and the input rectifier, which all sit on top of an aluminum heat sink. The two capacitors and one inductor that sit to the side of the heat sink are part of the active IPEM. [46]

The design was generated from what was determined to be the optimal layout electrically. In the process of current going through the converter, it is doubled while the voltage is stepped down. The electrical design allows AC current at 120 V to enter from an external source into the EMI filter where it then travels to the rectifier, then to the active IPEM, then to the passive IPEM, through the output components and finally out of the converter as DC current at 48 V. To keep the system of integrated electrical

components operating below 115^{o}C, a fan and heat sink system were built into the design. Two Sanyo Denki 40 mm x 40 mm x 28 mm fans (with brushless DC motors) draw in air from the system's surroundings to provide forced convection over the components and through the heat sink.

To build what is generally considered the worst-case scenario, the air surrounding the system is assumed to be 50°C. Therefore the air drawn into the system and the air the system vents to is set at 50°C.

The aluminum parallel-plate heat sink that was chosen for the power converter's initial layout had a 116.8 mm x 164 mm x 3.7 mm base with 28 fins, each 10.8 mm in height and 164 mm x 2 mm in length and width. To increase the amount of surface area, thereby enhancing the effects of heat transfer via convection, the height of the heat sink's base was lengthened to 4 mm and the height of each fin to 14 mm. The 18mm-high heat sink is the tallest heat sink that could be used in the power converter box. After setting up the loop and convergent conditions in iSIGHT, the iterative simulation can be executed automatically. [47][48]

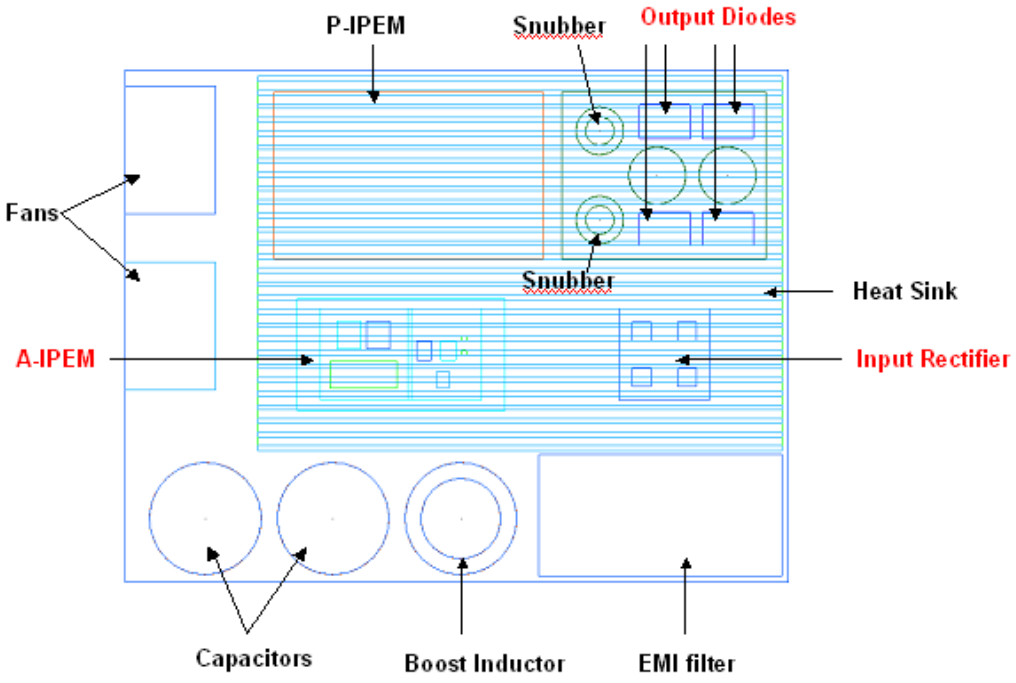


Figure 4. 9 The Top view of the system layout of the power converter.

4.4 Comparison between Iterative and Single-step Simulation Results

The iterative electro-thermal simulation process of a front-end converter is illustrated in **Figure 4.10**. It can be seen that the actual steady state temperature is found to be considerably different from the initial assumption of 115°C. Then the appropriate thermal design modification can be made to avoid the over-design in this case. The conventional thermal design approach, which executes single-step simulation (result is shown in **Figure 4.12**), usually does not incorporate the laborious nature of the manual or automatic iteration to take into account temperature dependent nature of the device losses. From **Figure 4.11**, the junction temperature points following 115°C are single-

step simulation results and the sixth junction temperature points are steady state. The maximum temperatures of various power devices are reduced by approximately 12°C from the results of iterative simulation result. Compared to conventional thermal design approach, the integrated electro-thermal design can achieve much improved thermal management improvement, and thus a higher power density based on steady state temperature distribution and power loss.

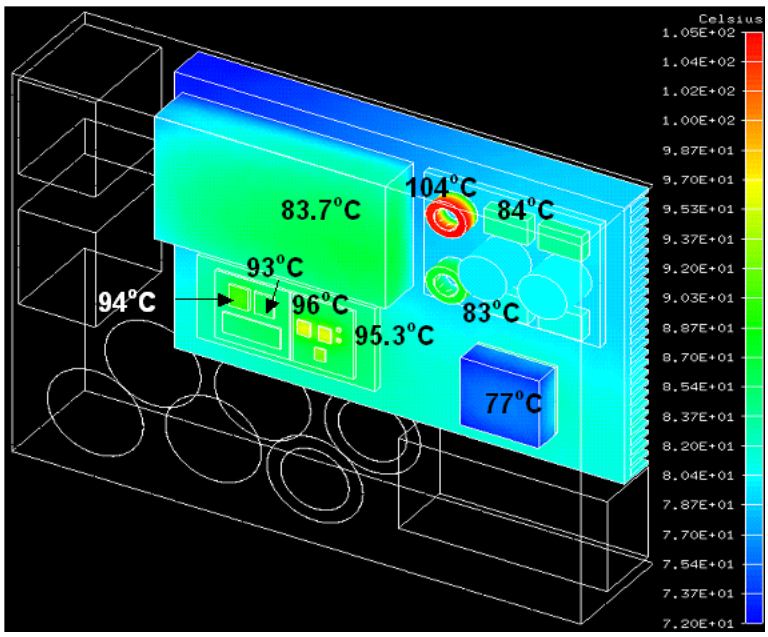


Figure 4. 10 Temperature distribution after iterative simulation using integrated electro-thermal simulation tools.

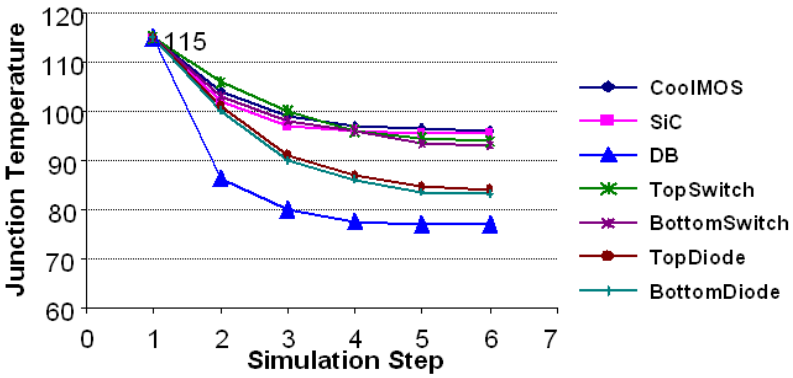


Figure 4. 11 Dynamic simulation process.

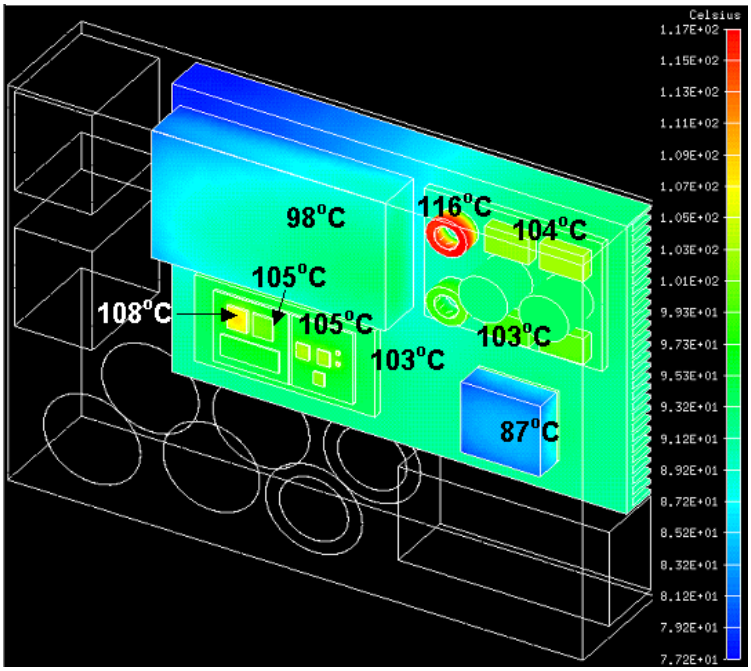


Figure 4. 12 Temperature distribution after single-step simulation using conventional thermal design method.

Note that there is one component that is much hotter than the other components of the system: snubber. From a thermal standpoint, it is easy to see that the snubber is receiving heat from the hot air that passes over the passive IPEM (which is emitting 31.5

W of heat). Furthermore, from a fluid dynamic viewpoint, the passive IPEM is blocking the snubber from a substantial amount of airflow. Despite the fact that this component only dissipates 3 W of heat volumetrically, the snubber is the hottest component of the system. Its small top surface and location relative to other components hinder heat being transferred from it. The position of the output combo is changed from horizontal to vertical in order to see if there is an opportunity to further reduce the heat sink.

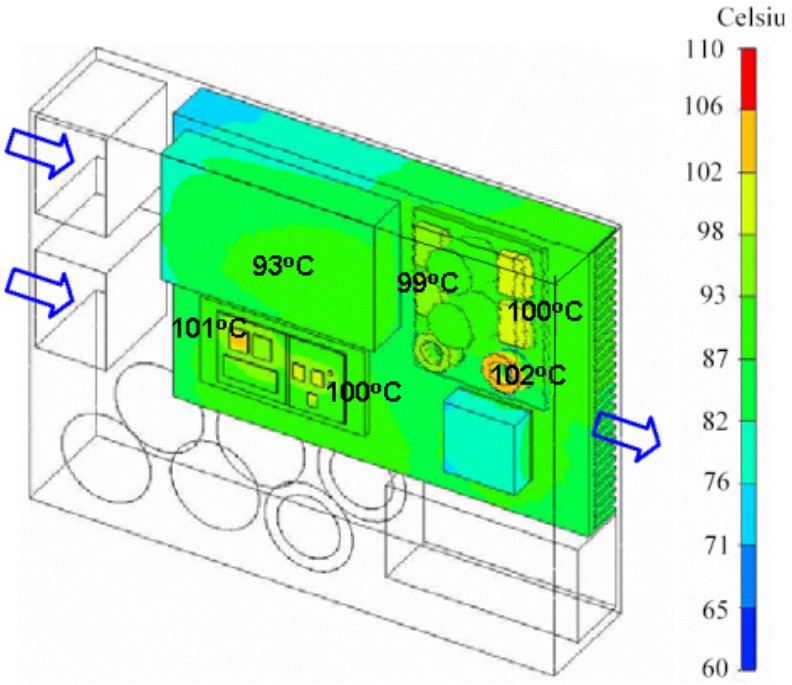


Figure 4. 13 Temperature distribution after changing the layout.

Note that, generally, there is a good distribution of heat across the components and heat sink. The passive IPEM and the MOSFETs on active IPEM, which dissipate 31.5 W and 20 W respectively, remained relatively cool. This is due to the large amount of surface area associated with the passive IPEM and the active IPEM's close proximity

to the fans. Also note that the system's component temperatures are far below the upper temperature limit of 115 ^{o}C. There is an opportunity to reduce the heat sink so as to get optimal layout.

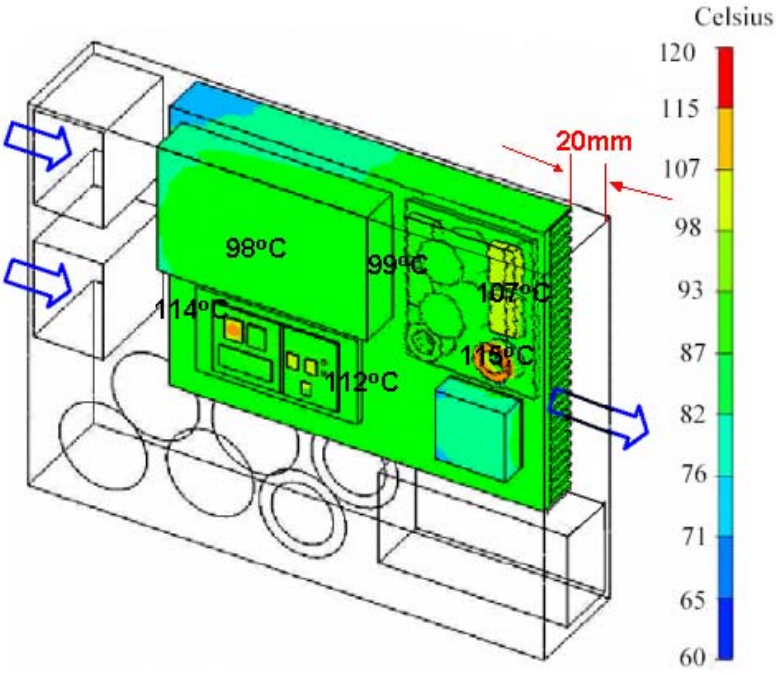


Figure 4. 14 Temperature distribution after reducing the heat sink.

Heat sink reduces 12% finally. Using integrated electro-thermal design method with automatic simulation environment can precisely predict the steady state power dissipation, temperature distribution and do optimal design for more complicated power systems like DPS front end converters. **Figure 4.15** shows the current CPES front-end converter using active and passive IPEMs, whose power density is 11.7W/in^3. The electro-thermal optimal design improves the power density 11.1% to 13 W/in^3.

Figure 4. 15 Hardware for IPEM-based front-end converter.

Chapter 5.

Conclusion and Future Works

Due to the nature of electronic power processing, the design of power electronics components, converters and systems has always involved many disciplines: from circuits and solid-state physics, to electromagnetics, systems and control, thermodynamics, structural mechanics, material science and reliability. Traditionally, these designs have been done sequentially, progressing from one discipline to another and involving many prototyping iterations. Although the use of CAD tools is widespread, these tools are largely "monodisciplinary" and, hence, require an inordinate number of labor intensive and time-consuming iterations. As a result, today's design process in power electronics is still much less advanced than the automation levels now common in many other industries. The resulting long design cycles unduly increase the cost and turn around time, and coupled with the lack of standardization, prevent levels of optimization that are now standard in most high-tech industries. The integrated analysis and design tools are proposed considering the fundamental relationships between electrical, thermal, mechanical and material properties of the components and packaging.

The goal of this thesis is to demonstrate the benefits of integrated analysis and design tools applied in distributed power supply systems' designs. First, it will significantly speed up the design process and eliminate the errors resulting from repeated

manual data entry and information exchange. Second, the integrated design optimization will result in better utilization of materials and components and will possibly allow for the discovery of new paradigms in electronic power processing.

Till now we has made efforts in establishing the accurate PFC converter model in Saber to include the temperature dependent loss effect. Meanwhile, the electrical layout and the thermal management of the converter are modeled in I-DEAS. Then I-DEAS exports the electrical interconnect geometry data to Maxwell Q3D, which can be programmed to generate the equivalent lumped circuit representing the parasitics of the system electrical layout. Then the simulation software Saber will be used to perform the electrical simulation to generate the loss data for all the components. The loss data is then transferred to I-DEAS again to update the temperature data for each component. This process is automatically executed by iSIGHT.

In addition to the attempt in the loss and thermal model, the high frequency model of active and passive IPEMs were developed. The parasitic inductance and capacitance were extracted in order to reflect the real EMI performance of IPEMs up to 30 MHz. It is our plan to develop a comprehensive electro-thermal simulation model of the whole front-end converter, which is also capable of predicting the EMI performance. With the accurate system EMI model and the loss model, we are able to use the integrated electrical-thermal design tools that encompass electrical, thermal, layout, and packaging design to obtain the optimal system design.

Appendix A

Main Power Semiconductor Models in Saber

1.IRFP460

```
template irfp460a d g s
#**********************************
#     Model Generated by MODPEX     *
#Copyright(c) Symmetry Design Systems*
#        All Rights Reserved        *
#    UNPUBLISHED LICENSED SOFTWARE   *
#   Contains Proprietary Information *
#      Which is The Property of      *
#     SYMMETRY OR ITS LICENSORS      *
#Commercial Use or Resale Restricted *
#   by Symmetry License Agreement    *
#**********************************
# Model generated on May 25, 00
# MODEL FORMAT: Saber
# Symmetry POWER MOS Model (Version 1.0)
# External Node Designations
# Node d -> Drain
```

```
# Node g -> Gate

# Node s -> Source

electrical d,g,s

{

# BODY_BEGIN

# Default values used in MM:

# The voltage-dependent capacitances are

# not included. Other default values are:

#   LD=0 CBD=0 CBS=0 CGBO=0

spm..model mm=(type=_n,

level=1,is=1e-32,rd=1e-6,

vto=4.31392,lambda=0.0114861,kp=7.87,rs=0.0001,

cgso=3.42135e-05,cgdo=1.78643e-08)

spd..model md=(is=3.31175e-09,rs=0.00898173,n=1.28697,bv=500,

ibv=2.5e-05,eg=1,xti=4,tt=0,

cjo=7.06512e-09,vj=0.908625,m=0.745936,FC=0.1)

# Default values used in MD1:

#   RS=0 EG=1.11 XTI=3.0 TT=0

#   BV=infinite IBV=1mA

spd..model md1=(is=1e-32,n=50,
```

```
cjo=2.41171e-09,vj=0.5,m=0.9,fc=1e-08)

# Default values used in MD2:

#   EG=1.11 XTI=3.0 TT=0 CJO=0

#   BV=infinite IBV=1mA

spd..model md2=(is=1e-10,n=0.976025,rs=3e-06)

# Default values used in MD3:

#   EG=1.11 XTI=3.0 TT=0 CJO=0

#   RS=0 BV=infinite IBV=1mA

spd..model md3=(is=1e-10,n=0.976025)

spm.M1 n9 n7 s s =model=mm,l=100u,w=100u

spd.d1 s d =model=md

spr.rds s d =1e+06

spr.rd n9 d =0.17183

spr.rg g n7 =6.305

spd.d2 n4 n5 =model=md1

spd.d3 0 n5 =model=md2

spr.rl n5 n10 =1

spf.fi2 n7 n9 i(spv.vfi2) =-1

spv.vfi2 n4 0 =0

spe.ev16 n10 0 n9 n7 =1

spc.cap n11 n10 =2.41171e-09
```

```
spf.fi1 n7 n9 i(spv.vfi1) =-1

spv.vfi1 n11 n6 =0

spr.rcap n6 n10 =1

spd.d4 0 n6 =model=md3

}
```

2.RHRP860

```
# Level 3 diode model produced by the Model Architect
# Diode Tool version 1.0.


element template rhrp860 p m = tempj
electrical p,m
number tempj   #=25
export val i i
export val p pwrd
{
   diode0..dc dc=[(25,0.0258084,0.000131001,0.173582,0.000832256,0.152891),
      (100,0.0289,0.000248652,0.131269,0.000741415,0.120692),
      (175,0.030497,0.00028701,0.0976857,0.000454687,0.0886716)]
   diode1..cj                              cj=(1.3677111n,666.4141p,2.71801e-011,-
1.73245,8.31095,0.27576)
```

```
        #25    diode2..recovery recovery=(8,200e6,3.6,28n)
        #100    diode2..recovery recovery=(8,200e6,5.8,55n)
        #175    diode2..recovery recovery=(8,200e6,7.2,75n)

        #115   diode2..recovery recovery=(8,200e6,6.1,59n)

           values {
              i=i(diode3.d)
              pwrd=pwrd(diode3.d)
           }
           diode3.d p m =dc=dc,cj=cj,recovery=recovery,tempj=tempj
}
```

3.CoolMOS (SPW20N60C3)

```
        * INFINEON Power Transistors
        * LEVEL 1 and LEVEL 3 SABER Library for CoolMOS Transistors
        * Version 110202
        *
        ****************************************************************
        * Simulation support: simulate@infineon.com                    *
        ****************************************************************
        *                                                              *
        * Models provided by INFINEON are not warranted by INFINEON as  *
        * fully representing all the specifications and operating      *
        * characteristics of the semiconductor product to which the    *
        #* model relates. The model describe the characteristics of a   *
        #* typical device.                                             *
        #* In all cases, the current data sheet information for a given  *
```

```
* device is the final design guideline and the only actual      *
* performance specification.                                    *
* Although models can be a useful tool in evaluating device     *
* performance, they cannot model exact device performance under *
* all conditions, nor are they intended to replace bread-       *
* boarding for final verification. INFINEON therefore does not  *
* assume any liability arising from their use.                  *
* INFINEON reserves the right to change models without prior    *
* notice.                                                       *
#*****
template SPW20N60C3_L1 drain gate source =te,dVth,dR
electrical drain,gate,source
number te=undef,dVth=0,dR=0
{
CoolMOS_L1.x1drain gate
source=model_data=(typ=600,typ2=2,Rs=1m,Rg=0.54,\
Ls=9n,Ld=5n,Lg=9n,Inn=20.7,Unn=10,Rmax=190m,act=21.05),dev_data=(te=te,
dVth=dVth,dR=dR)
}
#*****
```

4.<u>SiC</u>

```
##########################################################################
# SABER version 1.0   23.1.2002                                          #
```

```
# model based on publications:                                  #
# S.M. SZE      Physics of Semiconductors (Wiley)               #
# Kneifel et al Predictive modeling of SiC diodes .....         #
# Ruff et al    SiC devices: physics and modelling              #
#                                                               #
#################################################################
# files included:                                               #
# INFINEON_SiC_diodes.sin: model file comprising the required   #
# templates                                                     #
#                                                               #
# content:                                                      #
# SDP02S60                                                      #
# SDP06S60                                                      #
# SDP04S60                                                      #
# SDB10S30                                                      #
#                                                               #
# usage:                                                        #
#---------------------------------------------------------------#
# include model file into your template by:                     #
# <INFINEON_SiC_diodes.sin                                      #
#---------------------------------------------------------------#
# example model call:                                           #
# SDP04S60.1  plus minus tcase tref = selfh = 0, self_dc = 0    #
# plus: positiv node                                            #
# minus:        negativ node                                    #
# tcase:        thermal_c case node                             #
# tref:         thermal_c low node                              #
```

```
        # selfh:transient selfheating on= 1,off= 0, default: 0 #
        # selfh_dc:      dc selfheating  on= 1,off= 0, default: 0        #
        #                                                                 #
        # tcase and tref need to be shorted if no heat sink model       #
        # is attached                                                     #
        # data sheet thermal junction ambient model is already included #
        #                                                                 #
        # support: simulate@infineon.com                                  #
        #                                                                 #
#####################################################################
        # Level 1 diode model produced by the Model Architect
        # Diode Tool version 1.0.

        element template newsic1 p m = tempj
        electrical p,m
        number tempj=25
        export val i i
        export val p pwrd
        {
          diode0..dc                dc=[(-40,0.0527757,2.91503e-007,0.0725511,1.73054e-
006,0.632489),
              (25,0.0646574,3.75996e-010,0.0487693,2.24233e-011,0.45454),
              (100,0.0943151,4.71684e-010,0.967575,3.49869e-009,0.049797),
              (125,0.109206,2.60859e-010,0.363415,2.62462e-008,0.0547117),
              (150,0.118056,1.98493e-009,0.396215,3.1704e-007,0.062311)]
          diode1..cj cj=(834.5339p,254.6069p,5.35509e-011,0.590584,34.500884,0.48)
```

```
        values {
            i=i(diode1.d)
            pwrd=pwrd(diode1.d)
        }
        diode1.d p m =dc=dc,cj=cj,tempj=tempj
}
```

Appendix B

Software Interface Programs

1. Running Sketch in SABER

```
 #sketch.aim
# run as: /usr/local/saber20014/bin/sketch -script
/home/tsang/PFC/macro/sketch.aim test
# load schematic file
SchMgr:SchDesign  PFC_1000W.ai_sch /home/tsang/PFC

# load .sin file
Guide:LoadDesign -design /home/tsang/PFC/PFC_1000W.sin

# dc analysis
Saber:Send {dc}

# tr analysis
Saber:Send {tr (monitor 300,tbegin 0m,tend 5m,trep dc,tripeqtrep
yes,tsmax 100n,tstep 5n}
Saber:Send {tr (monitor 300,tbegin 5m,tend 10m,trep dc,tripeqtrep
yes,tsmax 100n,tstep 5n}
Saber:Send {tr (monitor 300,tbegin 10m,tend 15m,trep dc,tripeqtrep
yes,tsmax 100n,tstep 5n}
Saber:Send {tr (monitor 300,tbegin 15m,tend 20m,trep dc,tripeqtrep
yes,tsmax 100n,tstep 5n}
Saber:Send {tr (monitor 300,tbegin 20m,tend 30m,trep dc,tripeqtrep
yes,tsmax 100n,tstep 5n}
Saber:Send {tr (monitor 300,tbegin 30m,tend 40m,trep dc,tripeqtrep
yes,tsmax 100n,tstep 5n}
Saber:Send {tr (monitor 300,tbegin 40m,tend 50m,trep dc,tripeqtrep
yes,tsmax 100n,tstep 5n}
Saber:Send {tr (monitor 300,tbegin 50m,tend 60m,trep dc,tripeqtrep
yes,tsmax 100n,tstep 5n}
Saber:Send {tr (monitor 300,tbegin 60m,tend 68m,trep dc,tripeqtrep
yes,tsmax 100n,tstep 5n}
Saber:Send {tr (monitor 300,tbegin 68m,tend 92m,trep dc,tripeqtrep
yes,tsmax 100n,tstep 5n}

exit
```

2. Calculating the power losses

```
# scope.aim
# run as: /usr/local/saber20014/bin/scope -script
/home/tsang/PFC/macro/scope.aim
# define variable
set t1 70m
set t2 80m
set t3 70m
set t4 80m
set t5 70m
set t6 80m
set t7 70m
set t8 80m

# draw waveform
set pf [ScopeSigMgr:loadpffile /home/tsang/PFC/PFC_1000W.tr.ai_pl]
set wf_v_mos1 [pf:read $pf v_mos1]
set wf_v_mos2 [pf:read $pf v_mos2]
set wf_v_di [pf:read $pf v_di]
set wf_v_brdi [pf:read $pf v_brdi]
set wf_i_mos1 [pf:read $pf i_mos1]
set wf_i_mos2 [pf:read $pf i_mos2]
set wf_i_di [pf:read $pf i_di]
set wf_i_brdi [pf:read $pf i_brdi]
GrXY:NewGraph
Graph addsignal $wf_v_mos1
Graph addsignal $wf_v_mos2
Graph addsignal $wf_v_di
Graph addsignal $wf_v_brdi
Graph sigconfig Signal1 -region 0
Graph sigconfig Signal2 -region 0
#set overshoot [Measure:Overshoot $wf_v_out6]

# calculate energy
AimCalc
AimCalc:Enter $wf_v_mos1
AimCalc:Enter $wf_i_mos1
AimCalc:DoFunc multiply
```

```
AimCalc:DoFunc integ
AimCalc:GraphWaveform
AimCalc:Enter $wf_v_mos2
AimCalc:Enter $wf_i_mos2
AimCalc:DoFunc multiply
AimCalc:DoFunc integ
AimCalc:GraphWaveform
AimCalc:Enter $wf_v_di
AimCalc:Enter $wf_i_di
AimCalc:DoFunc multiply
AimCalc:DoFunc integ
AimCalc:GraphWaveform
AimCalc:Enter $wf_v_brdi
AimCalc:Enter $wf_i_brdi
AimCalc:DoFunc multiply
AimCalc:DoFunc integ
AimCalc:GraphWaveform
Graph sigconfig Signal4 -region 1
set wflist [Graph itemselect all add]
set wf_loss [lindex $wflist 0]
set wf_loss [Graph itemquery Signal3 -waveform]
set e1 [Measure:At $wf_loss $t1]
set e2 [Measure:At $wf_loss $t2]
set loss_mos1 [expr ($e2-$e1)/10m]
set wf_loss [lindex $wflist 1]
set wf_loss [Graph itemquery Signal3 -waveform]
set e3 [Measure:At $wf_loss $t3]
set e4 [Measure:At $wf_loss $t4]
set loss_mos2 [expr ($e4-$e3)/10m]
set wf_loss [lindex $wflist 2]
set wf_loss [Graph itemquery Signal3 -waveform]
set e5 [Measure:At $wf_loss $t5]
set e6 [Measure:At $wf_loss $t6]
set loss_di [expr 0.5*($e6-$e5)/10m]
set wf_loss [lindex $wflist 3]
set wf_loss [Graph itemquery Signal3 -waveform]
set e7 [Measure:At $wf_loss $t7]
set e8 [Measure:At $wf_loss $t8]
set loss_brdi [expr 2*($e8-$e7)/10m]
```

```
# write file
set ofile [open /home/tsang/PFC_weidong/macro/loss.txt w]
puts $ofile "begin"
puts $ofile "loss of mosfet1: $loss_mos1"
puts $ofile "loss of mosfet2: $loss_mos2"
puts $ofile "loss of boost diode: $loss_di"
puts $ofile "loss of bridge diodes: $loss_brdi"
#puts $ofile "peak of output: 1.3"
puts $ofile "end"
close $ofile

# fft
#set pf [ScopeSigMgr:loadpffile
/home/tsang/PEC_weidong/PFC_1200W_7_12_2001.fft]
#set sp_vr1 [pf:read $pf vr1]
#set sp_vr2 [pf:read $pf vr2]
#GrXY:NewGraph
#Graph sigconfig Signal1  -axis cphasedeg(y)
#Graph sigconfig Signal2 -axis db(y)

#AimCalc
#AimCalc:Enter  $sp_vr1
#AimCalc:Enter  $sp_vr2
#AimCalc:DoFunc add
#AimCalc:Enter 2
#AimCalc:DoFunc divide
#AimCalc:GraphWaveform
#set sp_vcmc [Graph itemquery Signal1 -waveform]
#Graph sigconfig Signal3 -region 1

exit
```

3. Outputting the power losses

```
begin
loss of mosfet1: 16.882632163859
loss of mosfet2: 16.882632163859
loss of boost diode: 4.3813160819295
loss of bridge diodes: 15.98445264327718
end
```

4. Inputting parameters to I-DEAS

```
#     Parameter Input File Template
# actions   part name   parameter   value             flag
#  to take  /directory  /flag       /material
#-------------------------------------------------------------------
#     1     Box         Depth                0.002            0
      3     Test_Box    MOSFET1          16.882632163859
      3     Test_Box    MOSFET2          16.882632163859
      3     Test_Box    BOOSTDIODE       4.3813160819295
      3     Test_Box    DIODEBRIDGE      15.98445264327718
      4     FE_Study_1  4 PLASTIC_LE PLASTIC_RI COPPERLEFT PLASTIC_BR
      0
```

5. Outputting temperatures

1) MOSFET_left

```
I-DEAS 8 :    Simulation                                    02-Aug-02
06:40:56
 SOLID-TEMP / ON NODES

 Group ID          : None
 Result Set        : 4 - SOLID-TEMP ON NODES
 Report Type       : Contour                    Units         : SI
 Result Type       : TEMPERATURE
```

```
Node  temper

   211734  1.117E+02
   211738  1.111E+02

……
 Node  temper

   217408  1.115E+02
   217410  1.114E+02



             212643
 Maximum   1.120E+02
```

2) MOSFET_right

```
I-DEAS 8 :    Simulation                                    02-Aug-02
06:41:03
 SOLID-TEMP / ON NODES

 Group ID          : None
 Result Set        : 4 - SOLID-TEMP ON NODES
 Report Type       : Contour                      Units         : SI
 Result Type       : TEMPERATURE




     Node  temper

   211718  1.117E+02
   211722  1.118E+02

……
```

```
     Node  temper

   217284  1.119E+02
   217286  1.120E+02

             212562
 Maximum   1.121E+02
```

3) Boost Diode

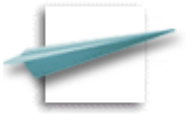
```
I-DEAS 8 :    Simulation                                    02-Aug-02
06:41:09
 SOLID-TEMP / ON NODES

 Group ID          : None
 Result Set        : 4 - SOLID-TEMP ON NODES
 Report Type       : Contour                    Units         : SI
 Result Type       : TEMPERATURE



     Node  temper

   154139  1.104E+02
   154140  1.105E+02

......
Node  temper

   158424  1.091E+02
   158426  1.090E+02


             154458
 Maximum   1.108E+02
```

4) Diode Bridge

```
I-DEAS 8 :    Simulation                                    02-Aug-02
06:41:16
 SOLID-TEMP / ON NODES

 Group ID          : None
 Result Set        : 4 - SOLID-TEMP ON NODES
 Report Type       : Contour                      Units         : SI
 Result Type       : TEMPERATURE




     Node  temper

   154143  1.081E+02
   154144  1.082E+02

……

Node  temper


   158802  1.075E+02
   158804  1.076E+02

             158618
 Maximum   1.085E+02
```

Appendix C

Polynomial Regression Curve Fitting in MathCAD



DATA ANALYSIS

Polynomial Regression

This QuickSheet demonstrates Mathcad statistical functions for polynomial regression of X-Y data.

Enter a matrix of X-Y data to be analyzed (x-coordinate in first column, y-coordinate in second):

data :=

0	9.1
1	7.3
2	3.2
3	4.6

Click on the **Input Table** above until you see the handles, and enlarge it to see the matrix data used in this example.

$X := data^{\langle 0 \rangle}$ $Y := data^{\langle 1 \rangle}$ $n := rows(data)$

Enter degree of polynomial to fit:

$k := 2$

Number of data points:

$n = 10$

$z := regress(X, Y, k)$

Polynomial fitting function:

$fit(x) := interp(z, X, Y, x)$

$coeffs := submatrix(z, 3, length(z) - 1, 0, 0)$

Coefficients:

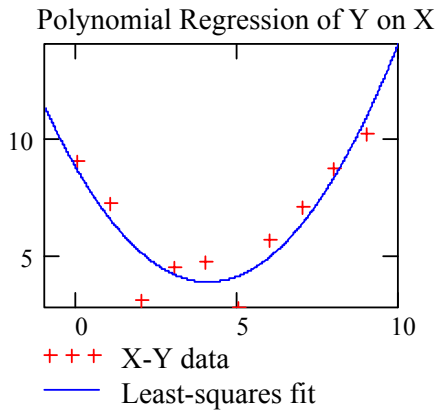
$$coeffs^{T} = (8.698 \quad -2.341 \quad 0.288)$$

R^2:

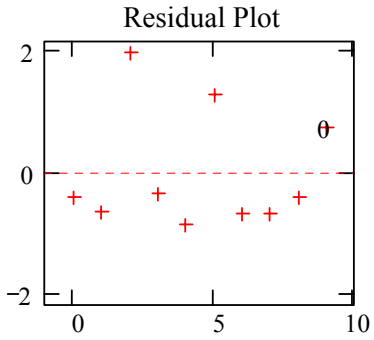
$$\frac{\sum \overrightarrow{(fit(X) - mean(Y))^2}}{\sum \overrightarrow{(Y - mean(Y))^2}} = 0.85$$

Degrees of freedom: $n - k - 1 = 7$

Plots



$$scale := \max\left(\overrightarrow{|fit(X) - Y|}\right) \cdot 1.1$$



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