STABILITY OF DISTRIBUTED POWER SUPPLY SYSTEMS

by

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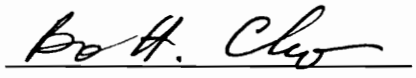

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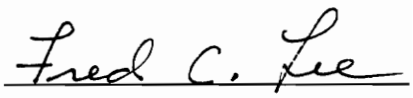

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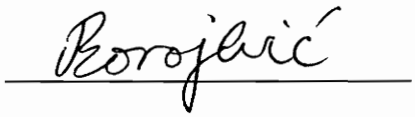

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(ABSTRACT)

A comprehensive stability analysis of a distributed power system (DPS) is performed. The possible performance degradation and stability problems caused by the loading effect of cascaded converters are analyzed. The effect of impedance overlap on the system and individual subsystems is examined.

By applying the loop gain analysis technique, a forbidden region for the polar plot of the ratio of impedances at the interface between cascaded subsystems is determined. A method of transforming the forbidden region into a load impedance specification for a given source impedance is developed. The method guarantees system stability and minimal performance degradation of the DPS, while allowing impedance overlap at the interface.

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CHAPTER 1

INTRODUCTION

With the rapid advances being made in electronic technology, there has been increasing demand placed upon power supply systems. Stringent requirements are placed upon system power density, transient response, efficiency, and speed.

The centralized power supply which uses a single regulator is often not sufficient to meet these specifications. In a power system with a single centralized power supply, the power must be distributed to the load at a low-voltage level, which leads to high conduction losses; in addition, it is difficult to tightly regulate the load voltage level, which is necessary for today's sensitive logic circuits.

To meet the demanding requirements of today's power supply systems, the distributed power system (DPS) is becoming the power system of choice. A DPS consists of multiple cascaded power supplies; the regulators of an example two-stage DPS are shown in Figure 1.1. The line conditioner(s) take the unregulated dc input voltage and regulate it to an intermediate voltage bus. This bus voltage is then distributed through the system to load converters, which convert the bus voltage to the tightly regulated low voltage level needed by the load. With the distributed power system, high power density and efficiency can be achieved, conduction losses can be decreased, and load converters can be directly mounted on the logic cards to provide tight voltage regulation [1].

The multi-stage distributed architecture offers many advantages over the single-stage centralized system, but the price paid for using a DPS is an increase in system complexity. Due to the size and complexity of a complete DPS, it is not feasible to design such a power system as a whole. The system is typically defined in terms of several

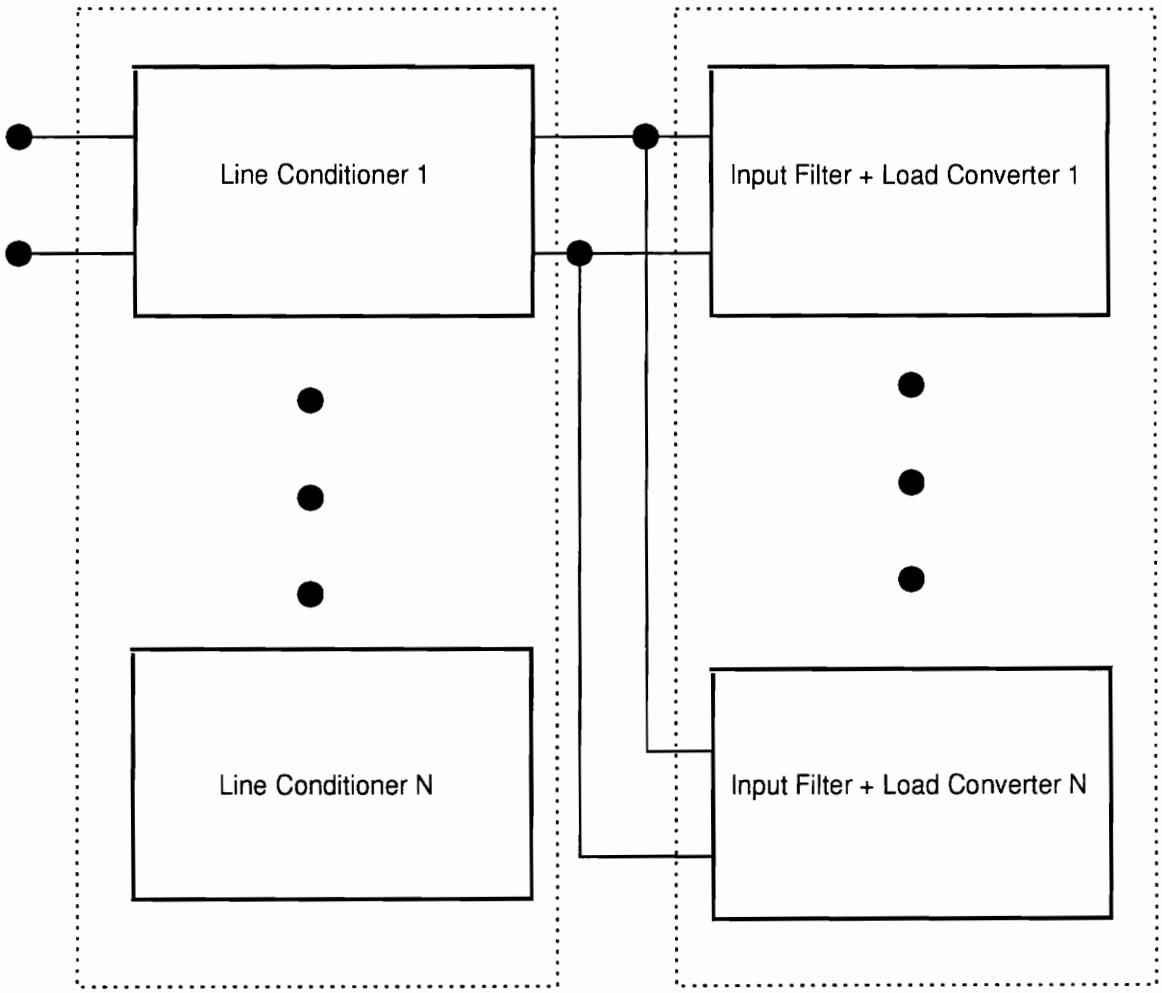


Figure 1.1 Regulators of a typical two-stage distributed power system

smaller subsystems, and each subsystem is designed individually. The subsystems are then integrated to form a complete DPS.

One of the most important issues when integrating subsystems is the possible stability problem and performance degradation resulting from interaction between the subsystems. Even though the subsystems may be well-designed for stand-alone operation, this interaction can lead to stability and performance problems after system integration [2].

This thesis introduces a design procedure which can be used to avoid undesirable interaction between subsystems and to form a stable DPS with minimal performance degradation. The design procedure guarantees the stability and performance of the integrated system by means of an input impedance specification for the load subsystem. It has been shown [1,2,6] that if no interaction between subsystems is present, then the performance and stability of the integrated system depends upon the stability and performance of the decoupled subsystems. However, in certain systems it may not be possible to have the DPS so that there is no interaction between subsystems. The design procedure developed in this thesis is needed to ensure stability and proper system performance when non-minimal interactions are present between subsystems.

Throughout this thesis a specific DPS will be used as an example to demonstrate the ideas presented. The example, unless otherwise noted, is the Space Station Freedom Power System; a block diagram of this system is shown in Figure 1.2. It can be seen that the system is very complex and contains many subsystems, including a solar array, a shunt switching unit (SSU), battery charger/discharger units (BCDUs), a direct current switching unit (DCSU), a main bus switching unit (MBSU), a dc-dc converter unit (DDCU), load converters, as well as cable impedances and input filters for the various modules.

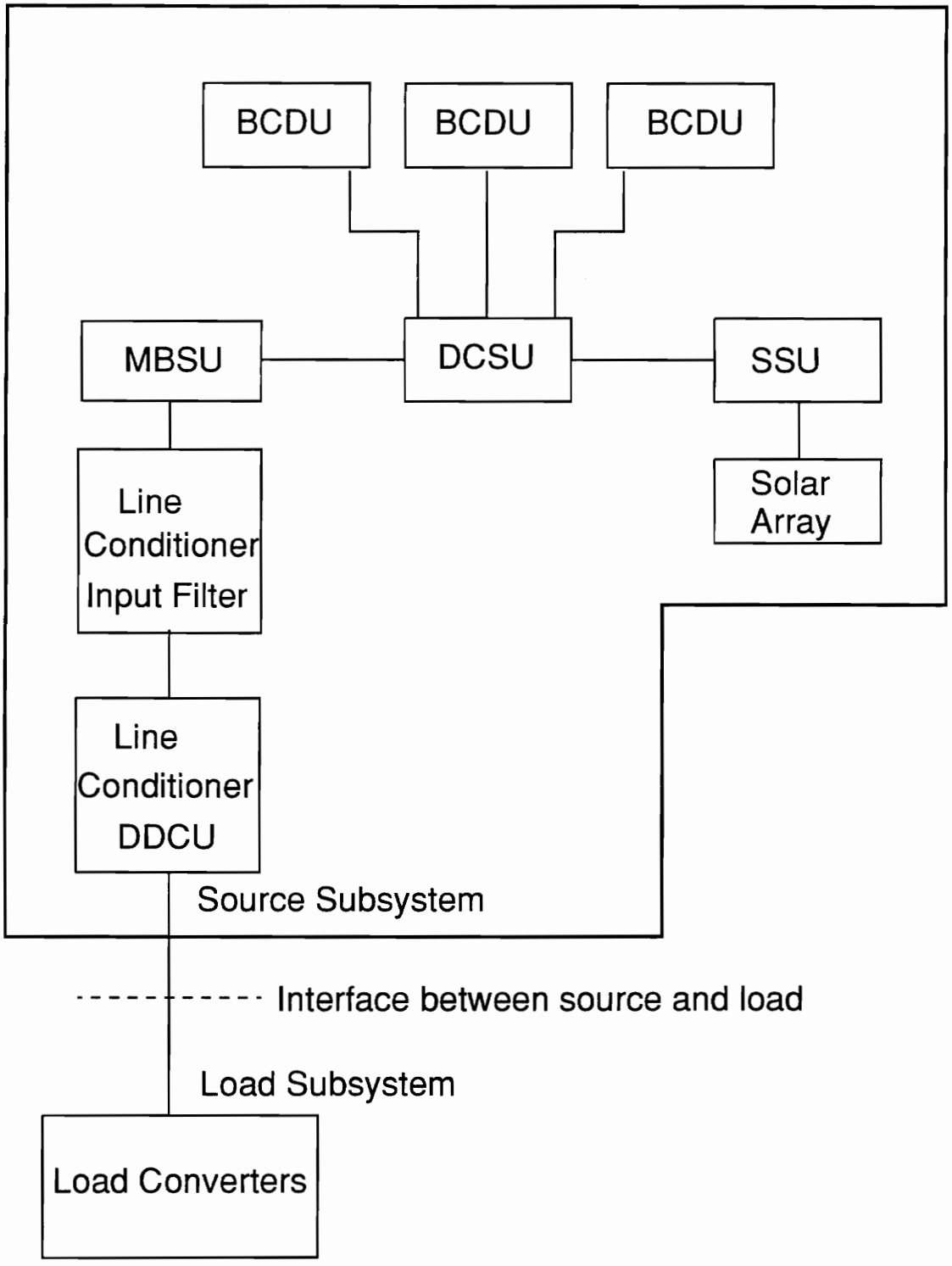


Figure 1.2 Space Station distributed power system

General interaction between two subsystems is reviewed in Chapter 2 of this thesis. The use of the impedance ratio Z_o/Z_{in}, (where Z_o is the output impedance of the source subsystem and Z_{in} is the input impedance of the load subsystem), as a loop gain which can be used to check integrated system stability is defined. The utilization of impedance overlap as a measure of system performance and its effects on subsystems are discussed. The meaning of the phase margin, in the presence of impedance overlap, is presented. A two-stage DPS is used to demonstrate the effect that impedance overlap between the line conditioner and the load subsystem has on system and subsystem performance and stability. The two stage DPS used for example purposes contains the DDCU line conditioner with input filter and an ideal source as the source subsystem, and load converters with input filters as the load subsystem.

Chapter 3 introduces a method to define a load impedance phase specification for a given source subsystem. The specification formed by this method guarantees stability and minimal performance degradation in the integrated system. The concept of a forbidden region for the loop gain defined in Chapter 2 is introduced. The entire Space Power System, including all subsystems, is used as an example. The DDCU and everything connected to its input filter side is used as the source subsystem. Methods of generating the impedance specification for the Space Station load subsystem are presented. Example load subsystems are examined to determine the feasibility of such a phase specification. The possibility of checking individual converters, which are part of the load subsystem, against the specification separately is examined.

Chapter 4 presents the conclusions of the thesis.

CHAPTER 2

SUBSYSTEM INTERACTION ANALYSIS

2.1 Introduction

Due to the impracticality of designing and analyzing a DPS all at one time, the system is usually broken down into smaller subsystems to make the design process more feasible. After designing the subsystems, they are integrated to form the DPS. Even for well designed subsystems, potential interaction problems are present when integrating the system.

This chapter will discuss the interaction between subsystems, and its effect on the subsystem and system performance and stability.

2.2 Impedance Ratio as a Loop Gain

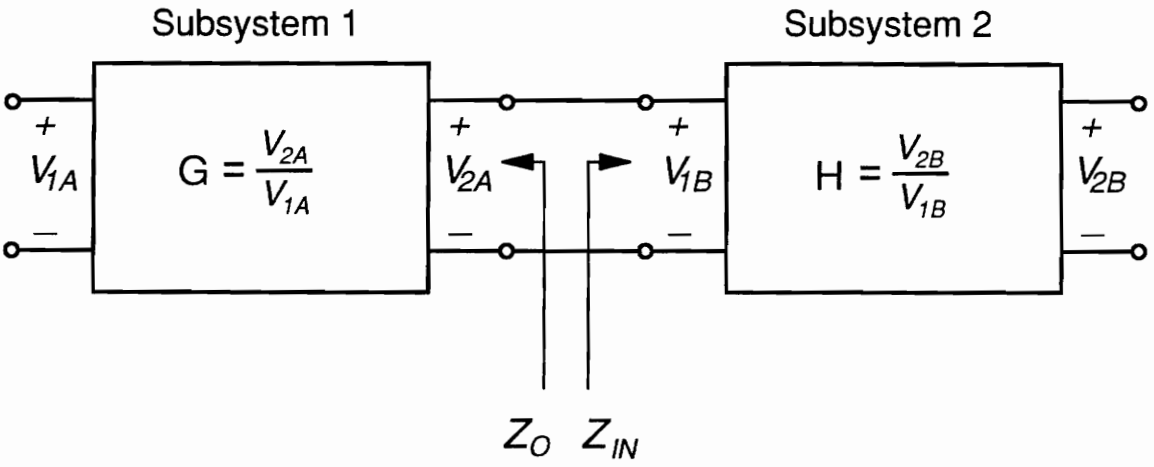
Consider the integration of the two subsystems shown in Figure 2.1. It is assumed that each subsystem is stable and well-designed for stand-alone operation. It can be found that the integrated system transfer function is [2]:

$$F = \frac{V_2}{V_1} = \frac{GH}{1 + T_m} \quad , \tag{2.1}$$

where:

$$T_m = Z_o / Z_{in} \quad , \tag{2.2}$$

G = forward voltage gain of subsystem 1 without load,



$$F = \frac{V_{2B}}{V_{1A}} = \frac{GH}{1 + \frac{Z_O}{Z_{IN}}}$$

Figure 2.1 Two cascaded subsystems

H = forward voltage gain of subsystem 2 without source,

Z_o = output impedance of subsystem 1, and

Z_{in} = input impedance of subsystem 2.

It can be seen that the term $1+T_m$ represents the loading effect caused by integrating the subsystems. Both G and Z_o have common denominators, as do H and $1/Z_{in}$; this is because both of these pairs are input-to-output transfer functions which have the same characteristic equation. Using this, and assuming all eigenvalues of each subsystem are observable at the output port, the characteristic equation for the overall system can be derived as [2]:

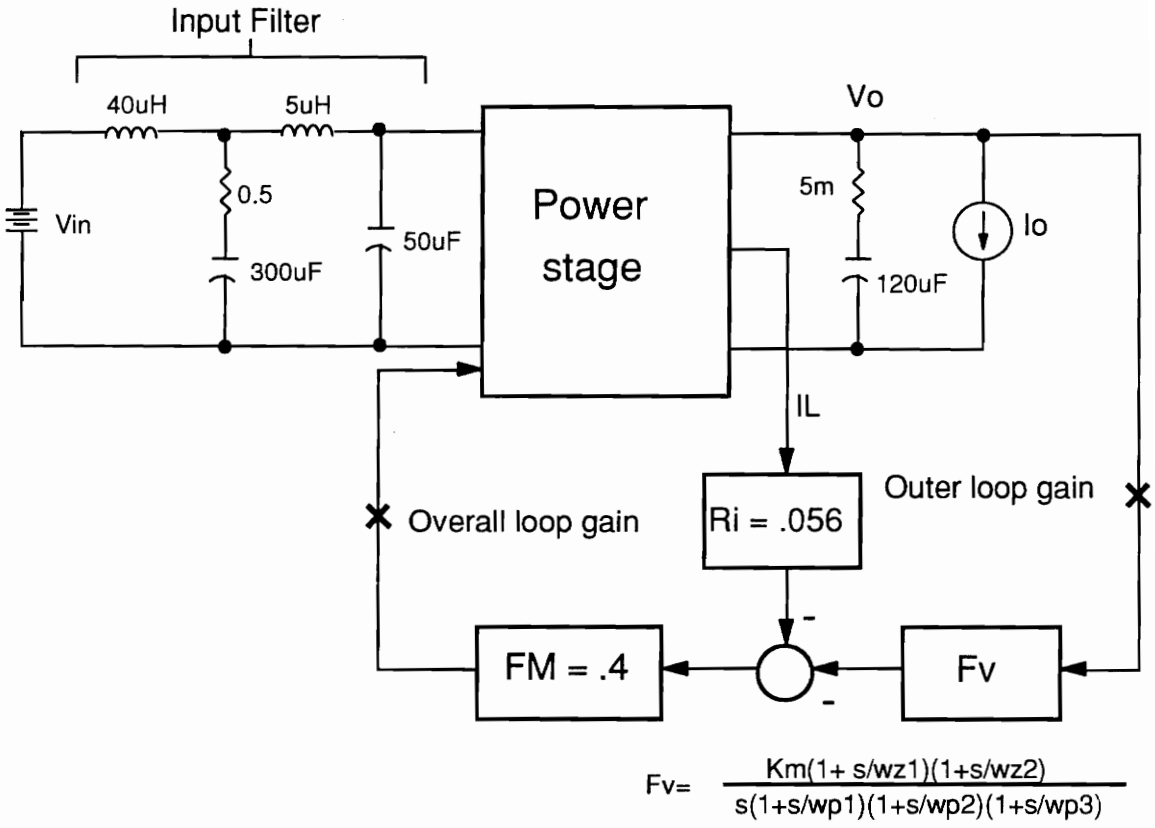
$$1+T_m=0 \quad . \tag{2.3}$$

Based upon this derivation of the characteristic equation, the term T_m, due to the loading effect, can be viewed as a system equivalent loop gain. This system loop gain can be used to determine the integrated system performance. The integrated system stability can be determined by applying the Nyquist criteria to this loop gain.

2.3 Definition of Example System

Throughout the remainder of this chapter, a two-stage DPS is used as an example. The system used consists of the DDCU line conditioner of the Space Power System with its input filter as a source subsystem and load converters with their input filters as a load subsystem.

A circuit diagram of the line conditioner is shown in Figure 2.2. The DDCU is a pulse-width-modulated (PWM) current-fed buck-derived converter which regulates an



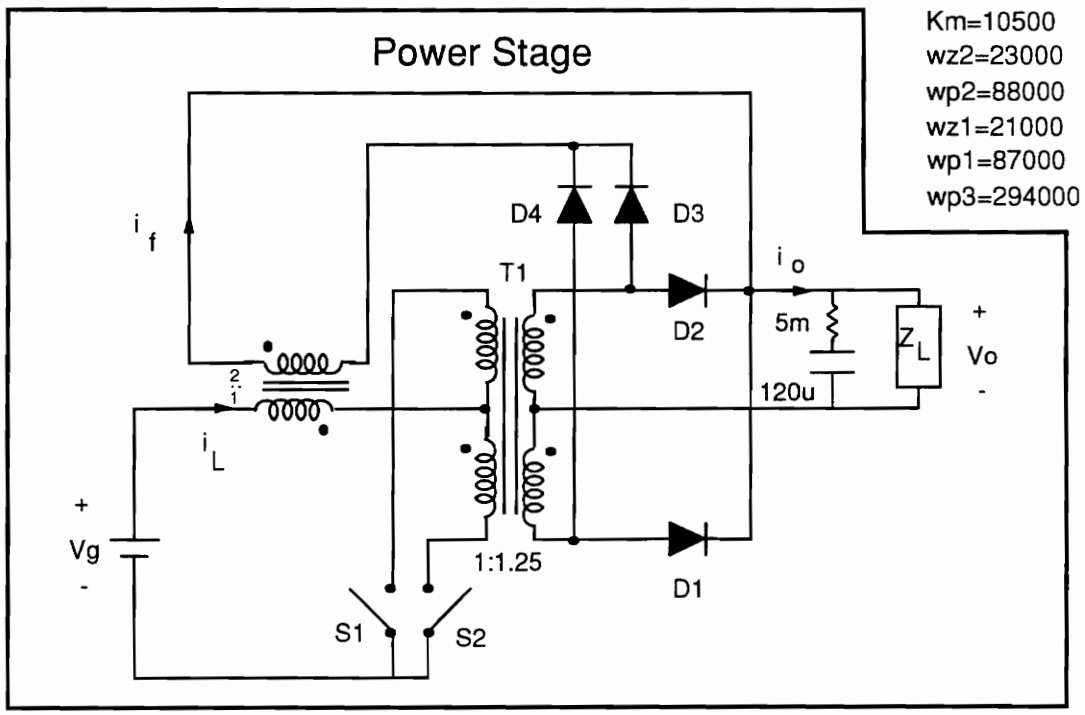


Figure 2.2 Circuit diagram of line conditioner (DDCU)

input voltage range of 115 V - 173 V to a 123 V bus. The circuit operates in the discontinuous conduction mode when output power is in the range of 0 W - 450 W and in the continuous conduction mode when output power is in the range of 450 W - 9.4 KW.

Except where otherwise noted, a filter with -R load is used to simulate load converters. This approximation is valid to simulate load converter input impedance below the loop gain crossover frequency of the line conditioner [9]. The use of this approximation can be justified by comparing the -R impedance to the input impedance of an actual converter as is done in [9]; by making this comparison, it is found that the -R load can be considered a worst-case when performing interaction analysis. In general, for a properly designed load converter, the -R load has a magnitude characteristic which is as bad or worse than that of the load converter. Also, the phase characteristic of a -R load is always $-180°$, which is the worst possible case for interaction.

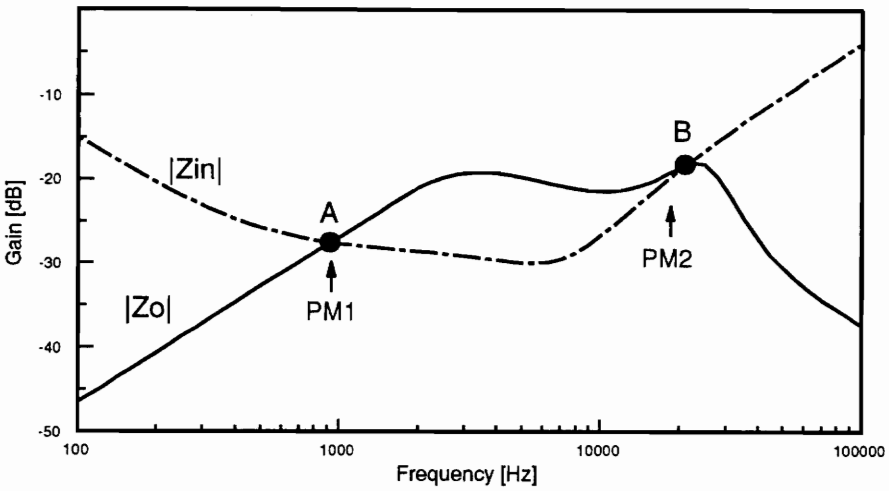
The phase characteristic of the active load is what allows the interaction between the source and load subsystems to cause potential stability problems in the system. If the load were passive instead of active, then the phase of the load subsystem would always be between $-90°$ and $90°$ which is generally the same range of phase that the output impedance of the source subsystem has. In the case of a passive load the phase of T_m generally can not be worse than $\pm 180°$ so the polar plot of the loop gain, T_m, can not encircle the (-1,0) point, and the worst possible case is a marginally stable system. However due the active nature of the load, the phase of T_m can have magnitude greater than 180 which presents the opportunity for the polar plot of the loop gain to encircle the (-1,0) point and for stability problems to result.

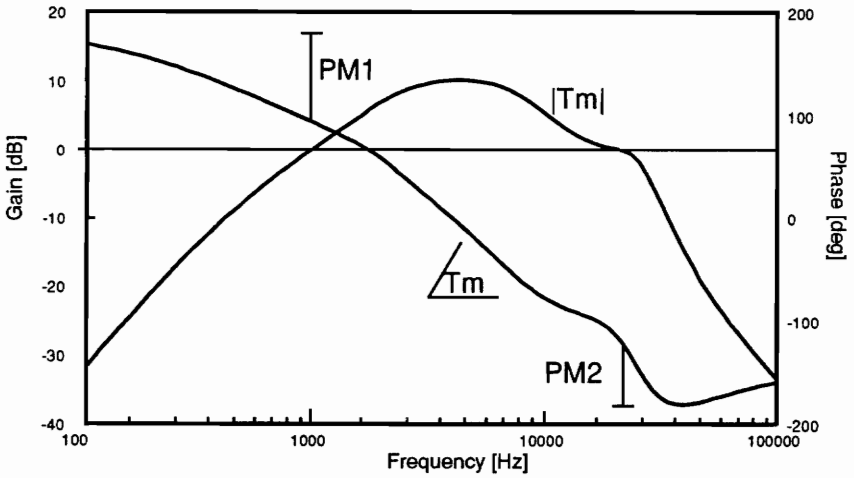
2.4 Effect of Overlap on System Stability and Performance

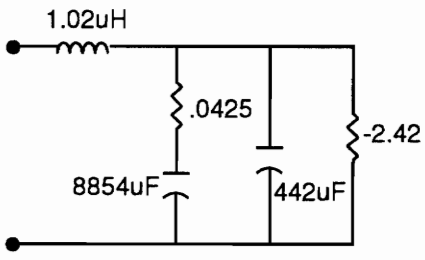
It has been shown in Section 2.2 that Z_o/Z_{in} is a loop gain and therefore can be used to analyze the integrated system stability and performance. From this loop gain and Equation 2.1, the following can be observed: if $|Z_{in}| \gg |Z_o|$ at all frequencies, then the loading effect is approximately unity, and the system has minimal interactions at the interface between the two subsystems. In such a case, the integrated system performance will depend upon the performance of the two decoupled subsystems. The system stability will depend only upon the stability of the individual subsystems. The bus impedance, Z_{bus}, which determines the quality of the bus, will be virtually identical to Z_o. System dynamics will be determined by the characteristics of the individual subsystems.

This describes the simplified case where there is no impedance overlap and no interaction between subsystems. Unfortunately, in a DPS it is often impossible for the system to have $|Z_{in}| \gg |Z_o|$ at all interfaces, while still meeting all other system specifications.

When $|Z_{in}|$ is not always much larger than $|Z_o|$, further analysis is needed to determine the system stability and to see if performance degradation is present. An example where the input impedance of the load subsystem interacts with the output impedance of the DDCU line conditioner is shown in Figure 2.3. It can be seen that $|Z_{in}| < |Z_o|$ at some frequencies, which means that interaction between these two subsystems is present. In the frequency range where $|Z_{in}| < |Z_o|$, the magnitude of loop gain T_m is greater than 0 dB, as shown in the figure. Since the loop gain, T_m, has a magnitude greater than 0 dB, this means that the loading effect is a significant factor in this system and must be taken into consideration when determining system stability and performance. The loop gain, T_m, can be used to check the stability by examining the







Circuit used to simulate Zin

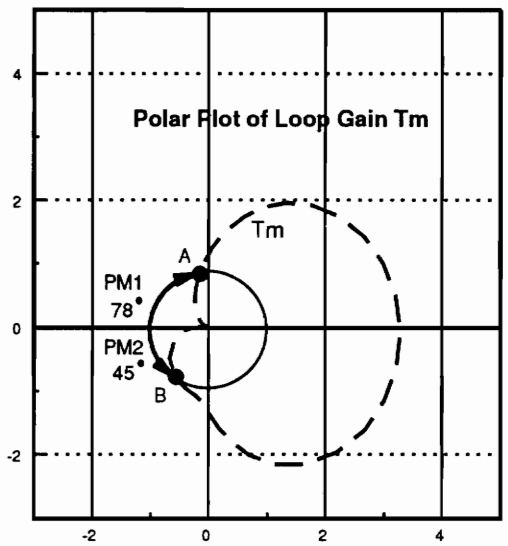


Figure 2.3 System with impedance overlap between two subsystems
Zo : Output impedance of DDCU, Vin = 115 V, Po = 6.25 KW

polar plot of the loop gain (Figure 2.3). By applying the Nyquist criteria to the polar plot, assuming that both the source and load subsystems are stable and have no RHP poles, it can be seen that this system is stable since the (-1,0) point is not encircled. Additionally, the system relative stability can be examined by looking at this polar plot. On the figure, because the magnitude of T_m is 0 dB at two frequencies, two phase margins can be defined and used to check relative stability. These two phase margins are defined at the low-frequency and high-frequency crossovers of impedance overlap, where loop gain T_m has a magnitude of 0 dB. For this example case, phase margin 1, which is defined at the low-frequency crossover of impedance overlap, is 78 degrees, and phase margin 2, which is defined at the high-frequency crossover of impedance overlap, is 45 degrees.

In addition to stability, a major concern when determining the quality of a bus is the transient response, which can be expressed in terms of the amount of voltage overshoot on the bus and the settling time needed to recover from a change in operating conditions. The amount of performance degradation of these quantities caused by the loading effect can also be predicted by examination of loop gain T_m.

To examine the transient response a two-stage DPS used for military VHSIC applications is considered as an example instead of the Space Power System. The DPS to be used is shown in Figure 2.4. The source subsystem consists of two series parallel resonant converters (SPRCs) in parallel and their input filter. The load subsystem can contain up to twenty parallel PWM and resonant load converters with input filters. The SPRCs have an input voltage range of 250 V - 450 V, which is regulated to a 50 V bus. The SPRCs are capable of providing up to 1000 W of power to the load subsystem. The SPRCs normally control the output voltage by using a variable frequency control, but in order to improve their efficiency, they utilize a duty-cycle control under high-line, light-load operating conditions.

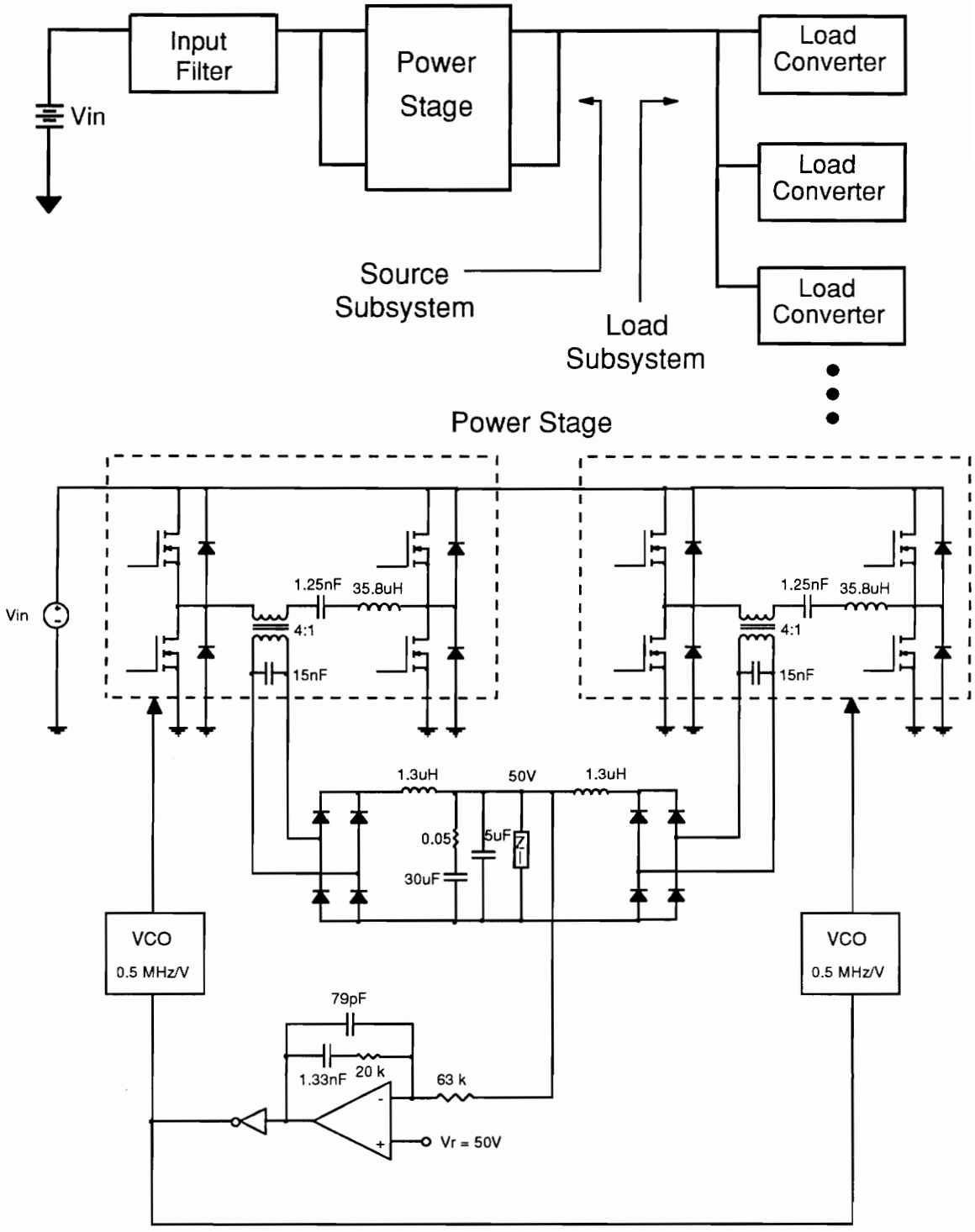


Figure 2.4 Example distributed power system used to examine transient response

The output impedance of the source subsystem is shown in Figure 2.5 in relation to the input impedance of three example load subsystems. These example loads are used to demonstrate the effect loading has on the transient response. The loop gain Tm for each of the three load cases is shown in Figure 2.6. It can be seen that for load A which does not interact, the loop gain, T_m, is always much less than 0 dB, so in this case the loading effect is negligible. However, for loads B and C, the loading effect is not negligible, and loop gain T_m has a magnitude greater than 0 dB in the frequency range where the impedances of Figure 2.5 overlap. For loads B and C, where the loop gain, T_m, has magnitude larger than 0 dB and the loading effect is not negligible, the effect of loading on the stability of the system needs to be examined. By examining the loop gain T_m of the system with load B, it is seen that the system is stable and has phase margins of 96° and 64° at the low-frequency and high-frequency crossovers of impedance overlap respectively. Likewise, by examining the loop gain T_m of the system with load C, it is seen that the system is stable and has phase margins of 24° and 78° at the low-frequency and high-frequency crossovers of impedance overlap respectively.

The worst-case voltage overshoot due to a change in current at the bus can be estimated by the peak bus impedance according to the equation:

$$\Delta V_{bus} \equiv |Z_{bus}|_{peak} \Delta I_{bus} \quad . \tag{2.4}$$

The bus impedance is equal to the parallel combination of Z_{in} and Z_o. Based upon this it can be determined that, as mentioned previously, the bus impedance is approximately equal to Z_o in the case of no overlap, because the magnitude of Z_{in} is large compared to the magnitude of Z_o. However, when impedance overlap is present, the bus impedance will be different from Z_o.

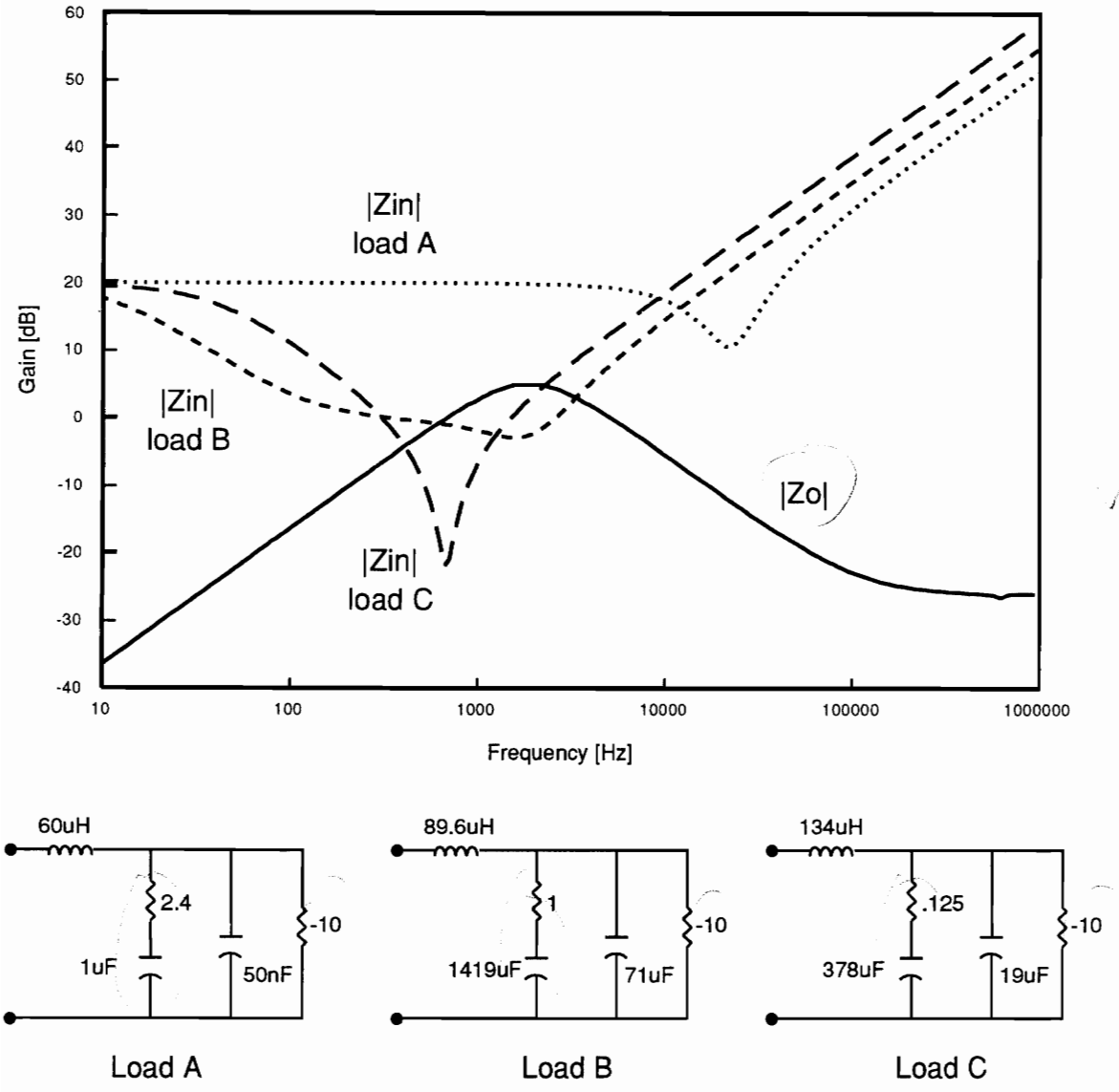


Figure 2.5 Impedance compatibility between output impedance of source subsystem and three different load subsystems

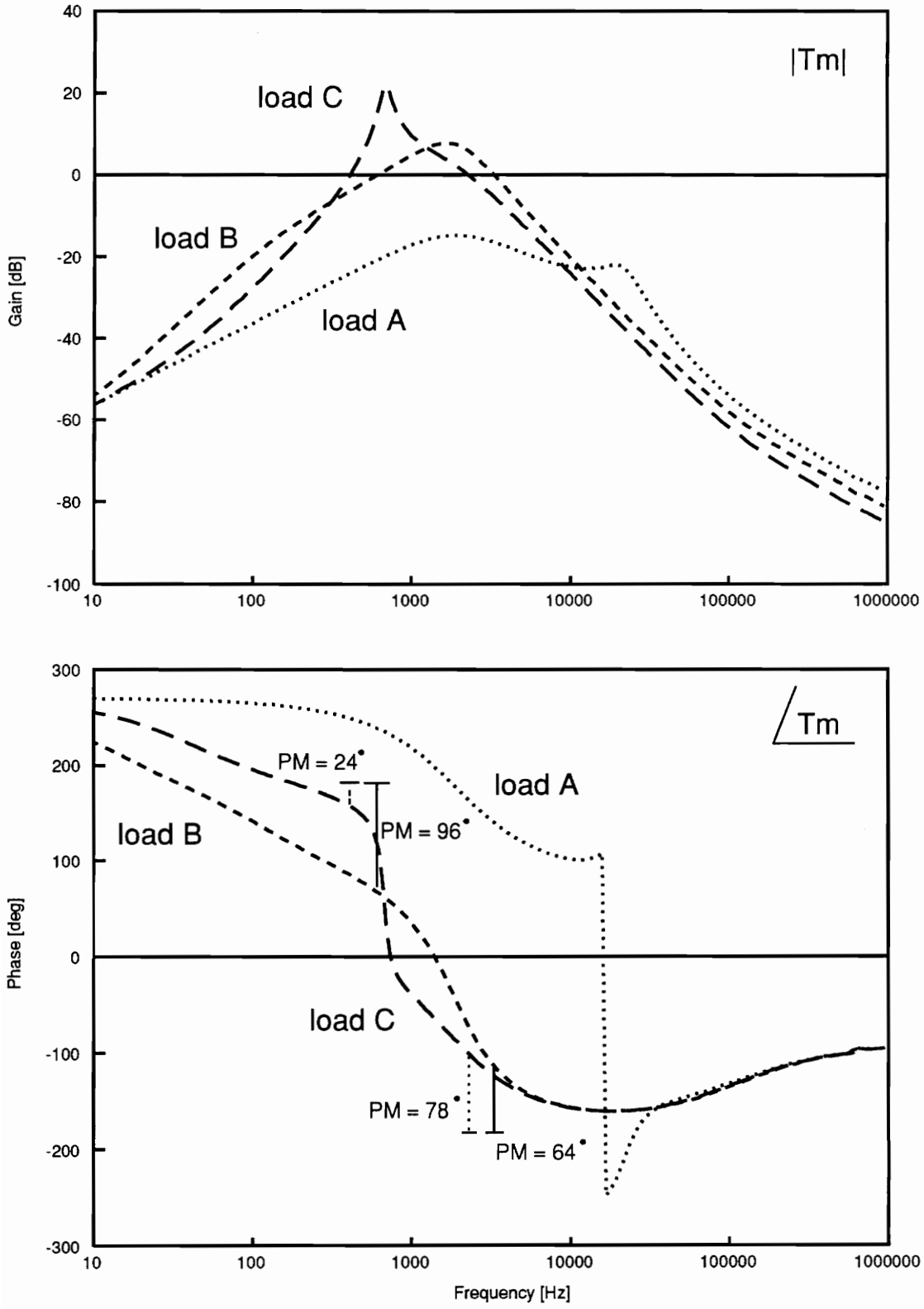


Figure 2.6 Loop gain Tm for three example load subsystems

If the phase margin of T_m is less than 60° at any point where $|Z_{in}| = |Z_o|$, there will be upward peaking of the bus impedance with respect to Z_o according to the equation:

$$|Z_{bus}| = \frac{|Z_o|}{\sqrt{2-2\cos(\phi_m)}} , \tag{2.5}$$

where ϕ_m is the phase margin at the point of overlap.

If the gain margin of T_m is defined at any frequency, there will be upward peaking of the bus impedance with respect to Z_o according to the equation:

$$|Z_{bus}| = \frac{|Z_o|}{(1-10^{-G_m/20})} , \tag{2.6}$$

where G_m is the gain margin of T_m in dB.

From these equations it can be seen that if the loop gain, T_m, has a small relative stability margin, there will be significant upward peaking of the bus impedance. By examining the peaking of the bus impedance the relative stability of the system can be predicted. The peaking of the bus impedance could cause the peak magnitude of the bus impedance to increase. This is important because the overshoot is directly proportional to the peak value of the bus impedance.

When $|Z_{in}| \gg |Z_o|$, there is no change in the bus impedance due to loading, so overshoot will remain the same as in the unloaded case. Any time the magnitude of Z_{in} is not much greater than the magnitude of Z_o, the bus impedance will be different from Z_o, and the possibility of degradation of the bus impedance and higher overshoot exists.

However, if the loop gain, T_m, has large relative stability margins and no upward peaking occurs, the bus impedance will be less than Z_o in the case of impedance overlap. This implies that impedance overlap will serve to decrease the voltage overshoot on the bus as long as the phase margin is sufficient to prevent excessive peaking of the bus impedance.

Figure 2.7a shows the bus impedance of the DPS for each of the three example loads. It is seen that both loads B and C, which have impedance overlap as shown in Figure 2.5, have a lower peak bus impedance than load A which has no impedance overlap with the source subsystem. The system with load B has lower peak bus impedance because, although impedance overlap is present, there is no significant upward peaking of the bus impedance since the phase margin is greater than 60° at both crossovers of impedance overlap. For the case of the system with load C for which T_m has a phase margin of only 24°, there is peaking of the bus impedance. This peaking causes the system with load C to have peak bus impedance higher than the system with load B, but it does not cause the peak bus impedance to be higher than that of the system with load A. Based upon the peak bus impedance values, it is expected that for a fixed change in bus current, the system with load A would have the most voltage overshoot, and the system with load B would have the least voltage overshoot. Figure 2.8 shows the transient response of the system to a step load from 350 W to 250 W for each of the example load subsystems. It is seen that as expected, the system with load C has overshoot of the bus voltage, .6 V, between that of the system with load B, .5 V, and the system with load A, .75 V.

The difference between the loaded case and the unloaded case in the settling time due to a change in operating conditions at the bus depends on the low-frequency crossover of impedance overlap. If the low-frequency crossover is as low as, or lower than, the location of the dominant poles of the stand-alone subsystems, it will have a

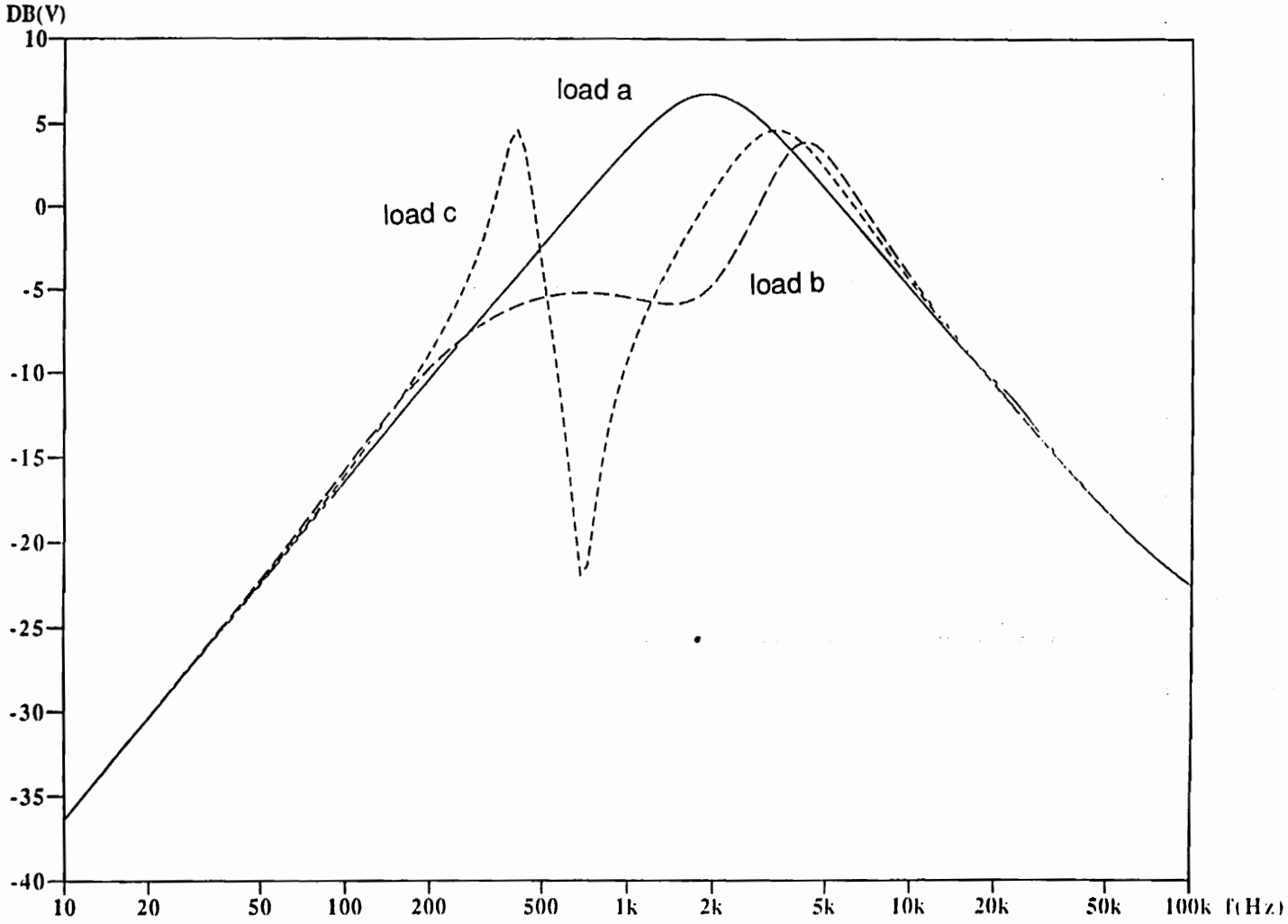


Figure 2.7a Bus impedance for three example load subsystems

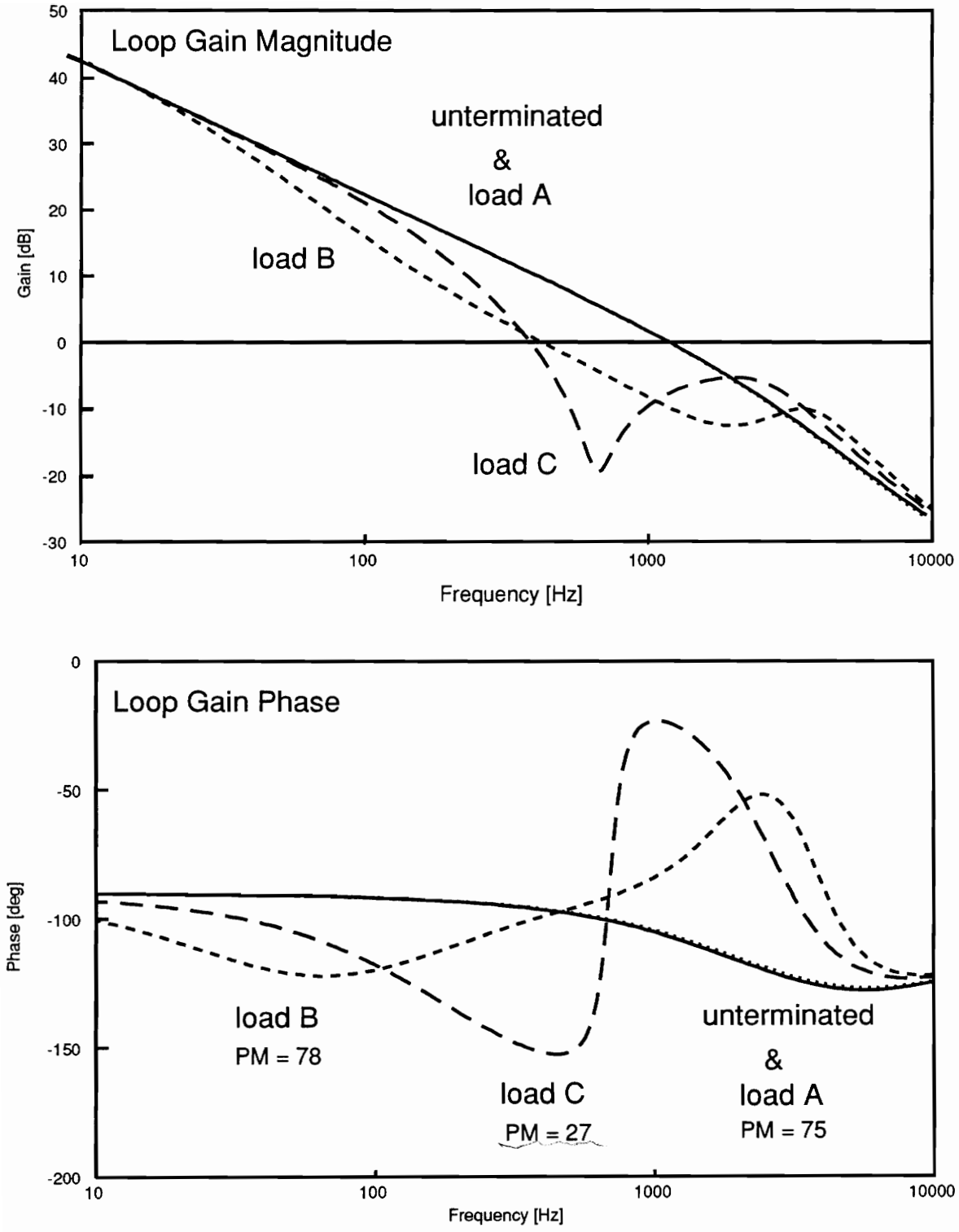


Figure 2.7b Line conditioner loop gain for three example load subsystems

significant effect on the system speed. On the other hand, if the low-frequency crossover of overlap is located at a high frequency compared to the dominant poles of the stand-alone system, then there will be no significant change in the system speed caused by the loading effect. This change in system dynamics can be predicted by examining the loop gain of the line conditioner or the bus impedance.

In Figure 2.7b, the unterminated loop gain of the SPRCs is compared to the loop gain with each of the three example loads. For load A which has no impedance overlap with the source subsystem, there is no significant change in the loop gain from the unterminated case. However, in the case of load B, the loading effect causes the loop gain to crossover at a lower frequency than in the unterminated case. The loss of loop gain bandwidth indicates that the system dynamics will respond more slowly in the case of load B than in the case of load A. In the case of load C, the loading effect causes the loop gain to crossover at a frequency slightly lower than in the case of load B. Additionally, the loaded loop gain has a much lower phase margin at the crossover frequency, 27°, then in the case of load A or B. Therefore it is expected that the system with load C will have slower more oscillatory dynamics than either the case of load A or B. When the transient response of Figure 2.8 is examined, it is seen that, as expected, the settling time of the bus voltage with load C is the longest, and that of load A is the shortest.

This change in system dynamics can also be predicted by examining the bus impedance of Figure 2.7a. The frequency at which the bus impedance begins to vary from the output impedance of the unloaded source subsystem is proportional to the change in system dynamics. It has been shown that the change in settling time between the loaded and unloaded cases depends on the low frequency crossover of impedance overlap because the dominant pole of $1+T_m$ occurs at that frequency. Due to system poles being added, it is expected that in this frequency range the bus impedance will

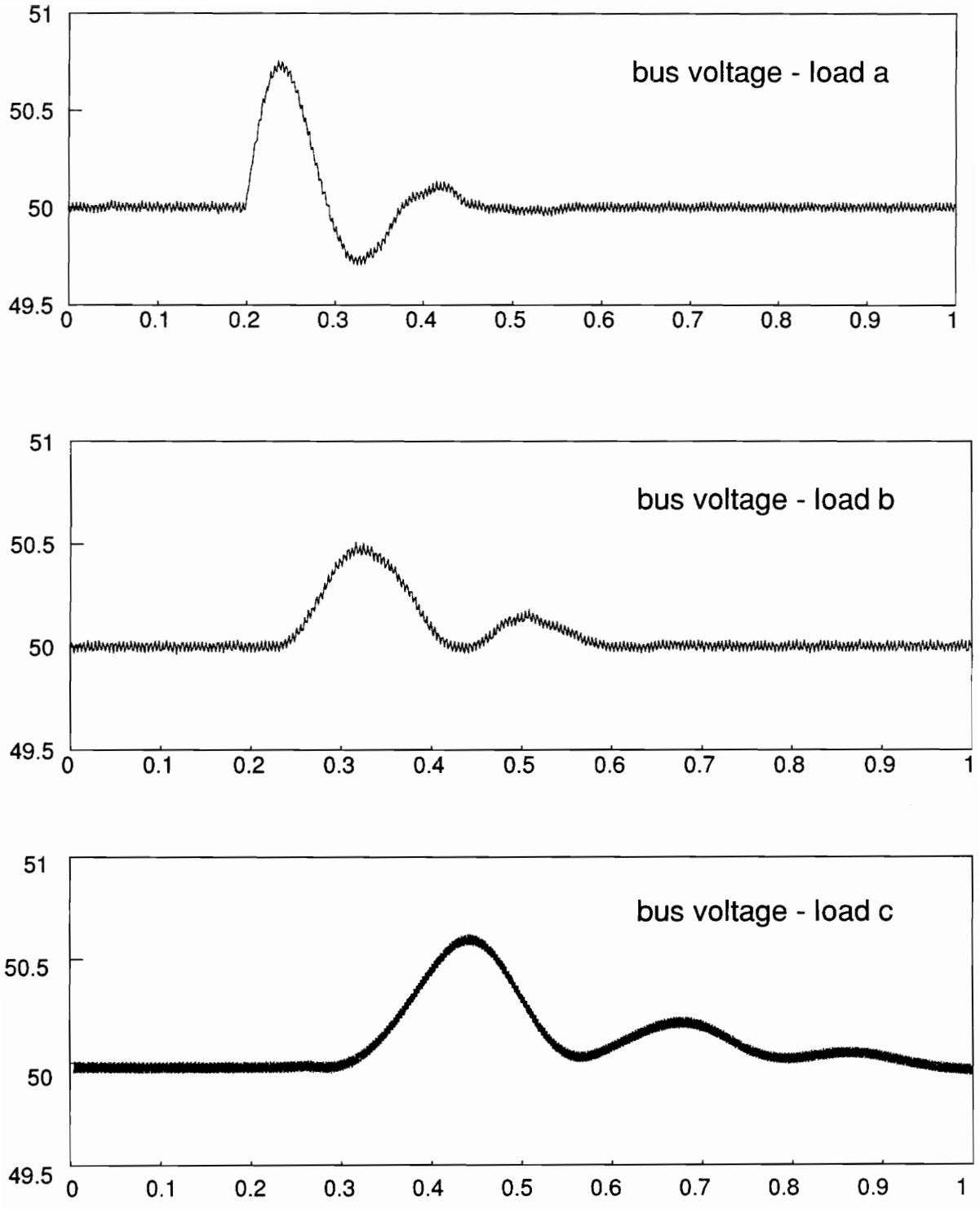


Figure 2.8 Step load response of three different load subsystems
load change from 350 W to 250 W

begin to differ from the unloaded output impedance of the source. In Figure 2.7a it can be seen that load C begins to vary from the output impedance of the source at the lowest frequency, so it is expected that the system with load C will have the slowest response of the three example load subsystems. For the case of load A which does not interact, the bus impedance is approximately equal to the output impedance of the unloaded system, so it is expected that for this load the system dynamics will not be significantly affected.

2.5 Effect of Overlap on Subsystem Performance

An examination of the effect interaction between the line conditioner and load subsystem has on the system stability and performance has been presented in the preceding sections. In this section, the effect interaction has on the individual subsystems will be investigated.

2.5.1 Effect on Source Subsystem

The effect that loading has on the source subsystem stability and performance will now be examined; this can be determined by inspecting the source subsystem loop gain, audiosusceptibility, and input impedance. A derivation of the effect loading has on the loop gain of the line conditioner is now presented [11]; Figure 2.9 shows the system to be considered.

First define:

$T_o = G_o H_o =$ unloaded source system loop gain,

G_o = unloaded control-to-output transfer function,

H_o = feedback transfer function,

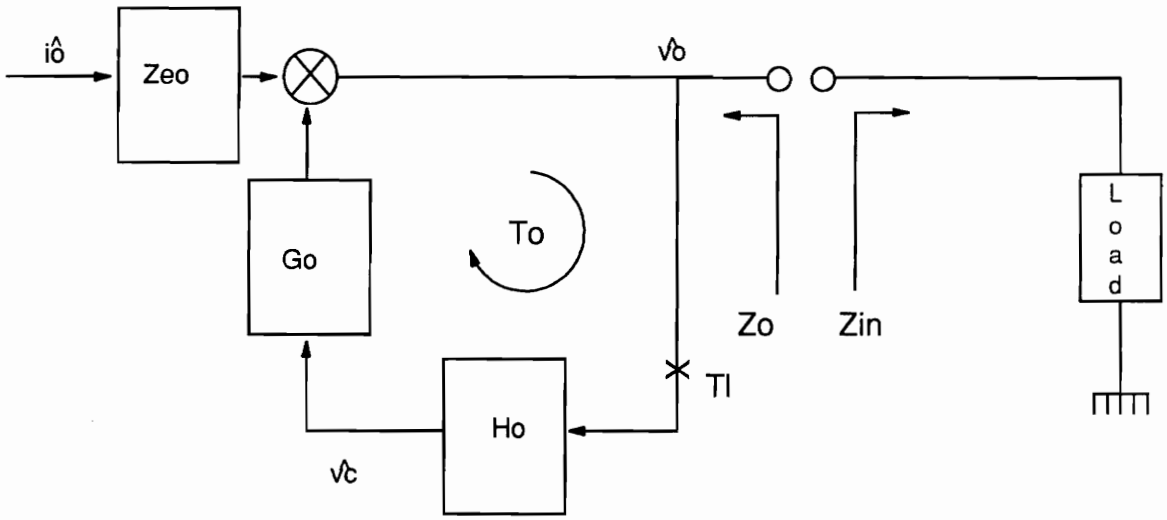


Figure 2.9 Block diagram of source subsystem

Z_{eo} = open loop output impedance of the source,

Z_o = closed loop output impedance of the source,

$$= \frac{Z_{eo}}{1+T_o} \quad ,$$

$T_m = Z_o/Z_{in}$ = loop gain due to the loading effect,

G_L = the loaded control-to-output transfer function,

$$= \frac{G_o}{1+\frac{Z_{eo}}{Z_{in}}} \quad ,$$

$T_L = G_L H_o$ = loaded source subsystem loop gain,

$$= \frac{G_o H_o}{1+\frac{Z_{eo}}{Z_{in}}}$$

$$= \frac{T_o}{1+T_m(1+T_o)} \tag{2.7}$$

By examining the loaded system loop gain, T_L, it can be seen that if the loading effect is negligible, which means $|T_m| \ll 1$ at all frequencies, then T_L is approximately equal to T_o. However, if the loading effect is not negligible, then in general there are three possible cases that exist. These three cases are interaction above, below, and near the crossover frequency of the unloaded source subsystem. All cases of interaction in an

actual system will be one of or a combination of these three cases. In this section, a qualitative sketch of each of the three cases is presented to show the general shape of T_L, T_m, and T_o for impedance overlap in each of the three frequency ranges. Then for each of the three possible cases, the effect impedance overlap between the line conditioner and load subsystem has on the loop gain of the DDCU line conditioner is investigated.

The first case to be analyzed is impedance overlap occurring above the loop gain crossover frequency of the line conditioner; this is illustrated in Figures 2.10a and 2.11. In this case, it can be seen that the loading effect on the subsystem loop gain occurs after the unloaded loop gain magnitude, T_o, is less than 0 dB. The loop gain, T_L, differs from T_o only at high frequencies when the magnitude is small, and therefore subsystem performance will be unaffected. The loop gain, T_L, has the same phase margin as T_o at the crossover frequency. This is because T_m is small, so T_L is approximately equal to T_o in this range. The only noticeable difference between T_L and T_o in this case is that the dc phase is shifted by 180°. This change in dc phase is caused by the use of a -R load in the loaded case instead of the constant current sink used in the unterminated case. The use of a -R load causes one open-loop pole of the unterminated constant current sink case to shift to the RHP [8]. This pole is responsible for the phase shift at low frequency; it will not affect the loop gain stability under steady-state conditions, provided the integrator gain is sufficient [8]. It can be determined that the relative stability margins of T_m are important to the system because if either the gain margin or phase margin are small, they will lead to peaking of the loop gain T_L with respect to T_o according to the equations:

$$|T_L| = \frac{|T_o|}{\sqrt{2-2\cos\phi_m}} , \tag{2.8}$$

where ϕ_m is the phase margin of T_m, and

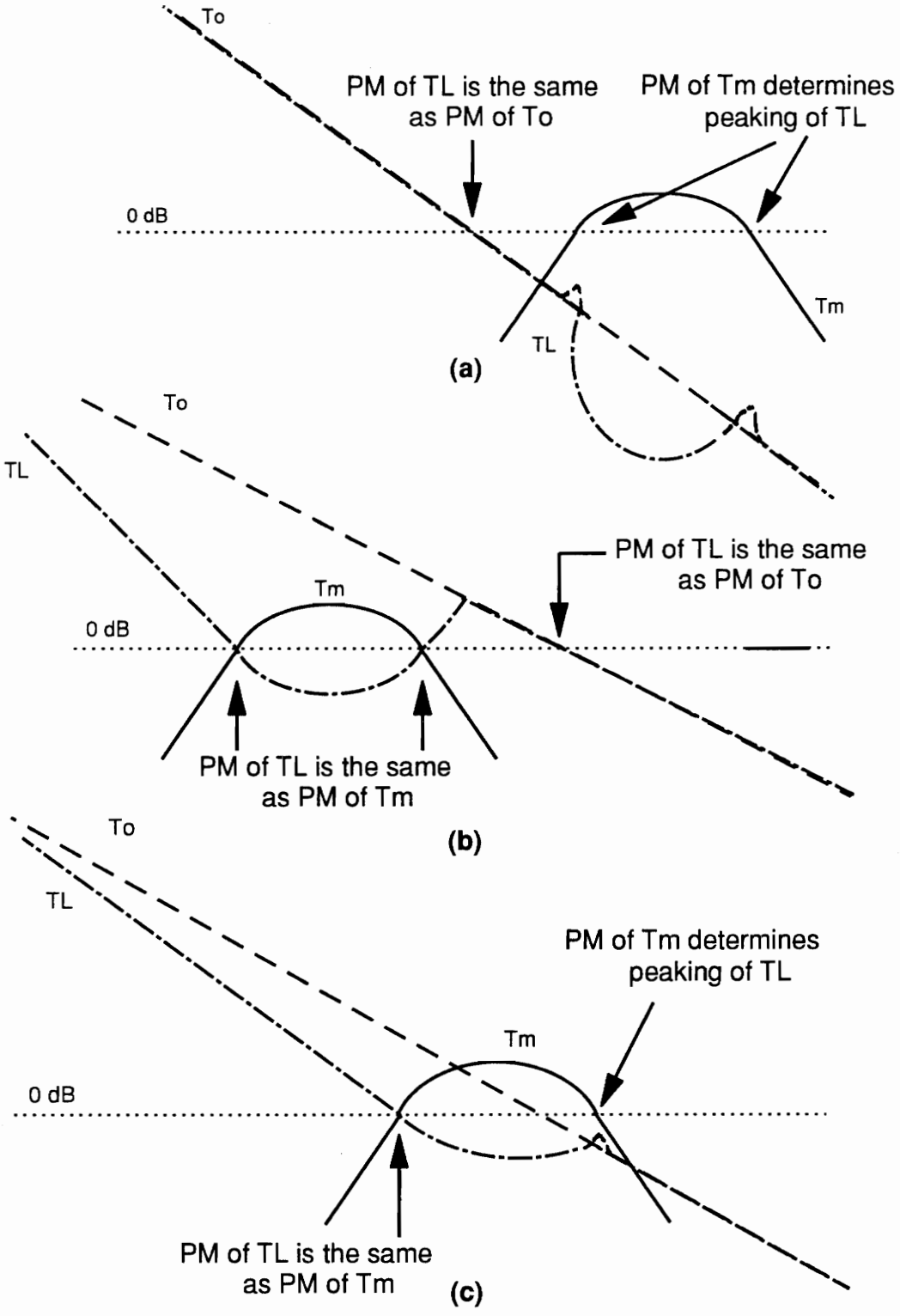


Figure 2.10 Three possible cases of interaction with respect to loop gain crossover fc: (a) above fc (b) below fc (c) around fc

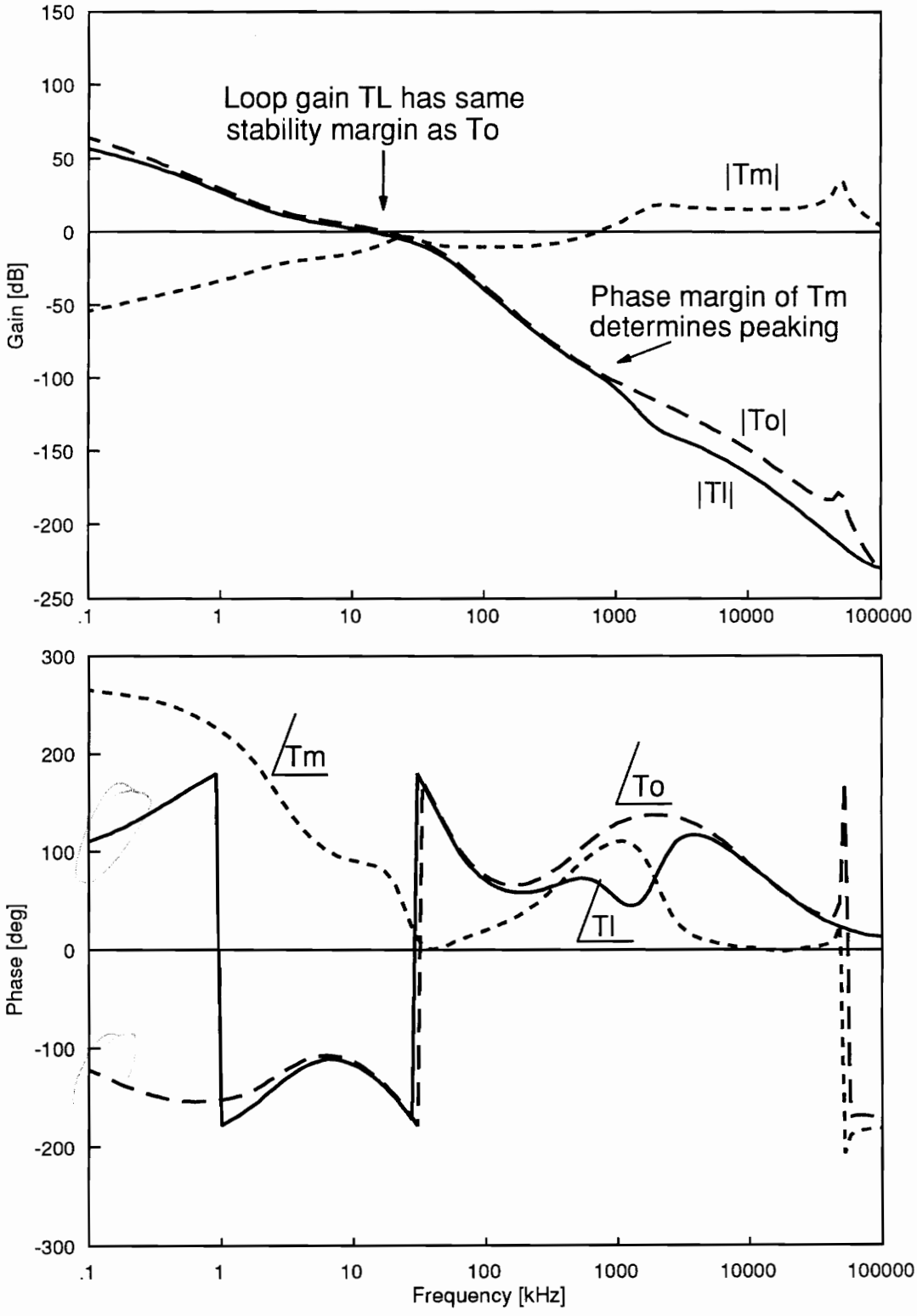


Figure 2.11 Interaction above loop gain crossover frequency of source subsystem

$$|T_L| = \frac{|T_o|}{(1-10^{-G_m/20})} \quad , \tag{2.9}$$

where G_m is the gain margin of T_m.

The second case to be analyzed is interaction well below the crossover frequency of the line conditioner; this case is illustrated in Figures 2.10b and 2.12. In this case, the loop gain T_L has three points at which it crosses over the 0 dB line. It can be seen from Equation 2.7 that at the initial and second crossover points, T_L is approximately equal to $1/T_m$, so the phase margin of T_m is the same as the phase margin of T_L. In Figure 2.12 it can clearly be seen that at the first two crossover frequencies the loaded line conditioner loop gain has approximately the same phase margin as the loop gain T_L. This means that if the loop gain T_m has a high stability margin at these crossover frequencies, then T_L does also. At the final crossover point, T_m is small, so T_L is approximately equal to T_o, and they have the same stability margin. So for this case, if both T_m and T_o have high stability margins, so does T_L. However, it can also be seen that the bandwidth of T_L is greatly reduced, which will effect the transient response. This case corresponds to the undesirable case of low-frequency interaction, which has already been shown to degrade the transient response of the system significantly.

The third case to be analyzed is interaction in the frequency range around the crossover frequency of the line conditioner; this case is illustrated in Figures 2.10c and 2.13. This case is the most common, as it is around the crossover frequency that the output impedance will have its peak value, thus making overlap most likely to occur in this frequency range. For the example cases shown, the low-frequency crossover of impedance overlap is before the loop gain crossover of the line conditioner, and the high-frequency crossover of impedance overlap is after. In this case the loop gain T_L has one point at

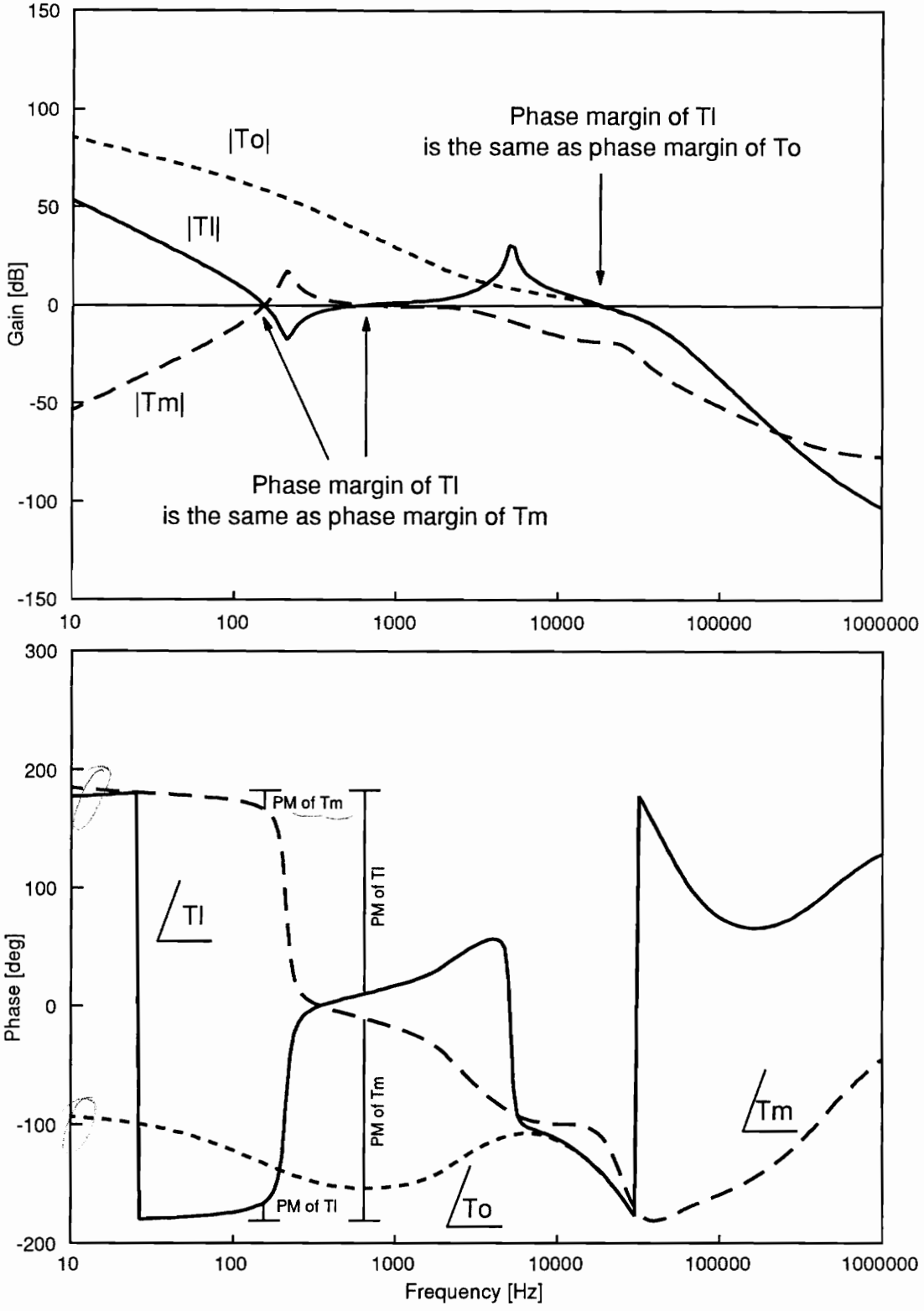


Figure 2.12 Interaction below loop gain crossover frequency of source subsystem

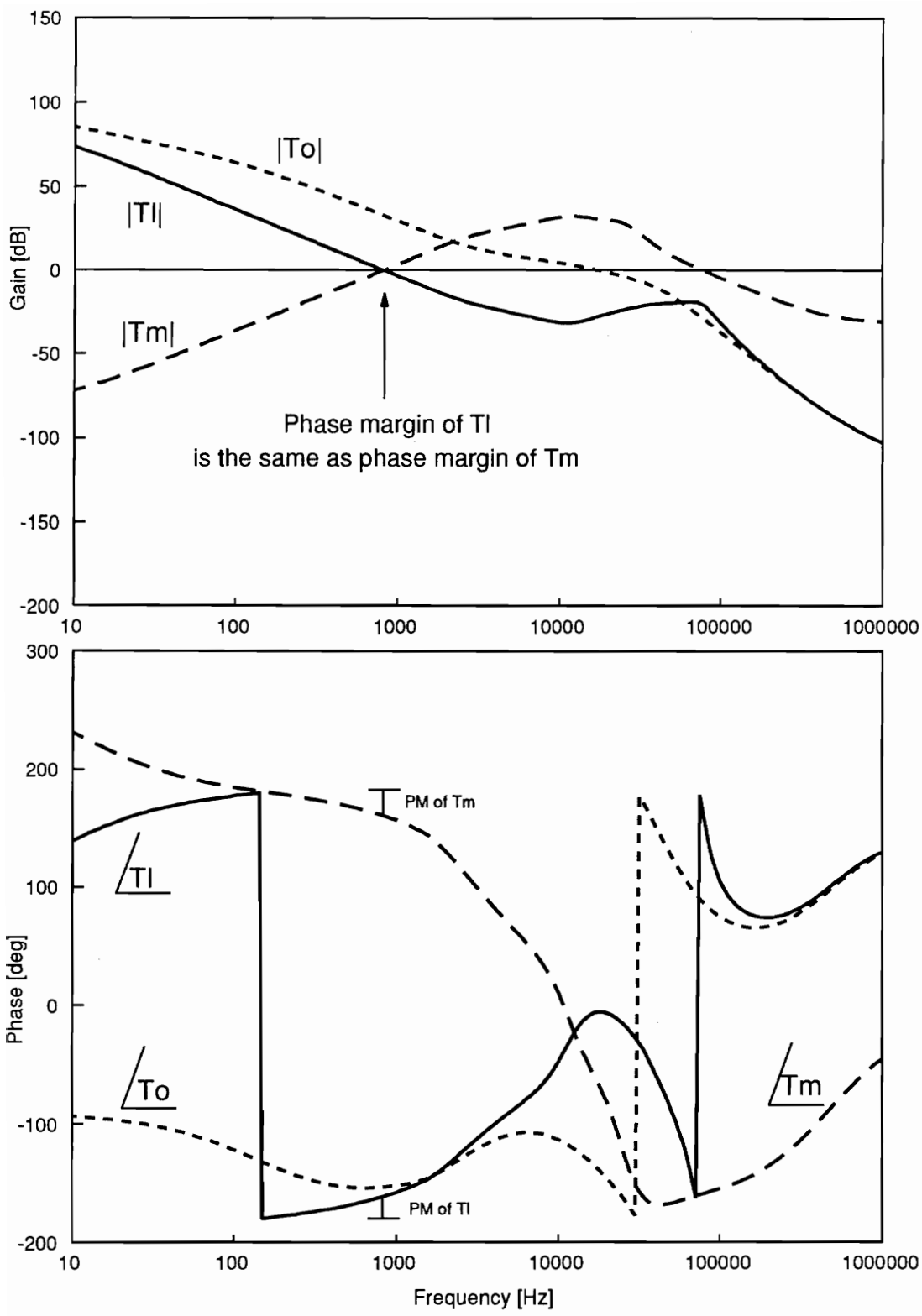
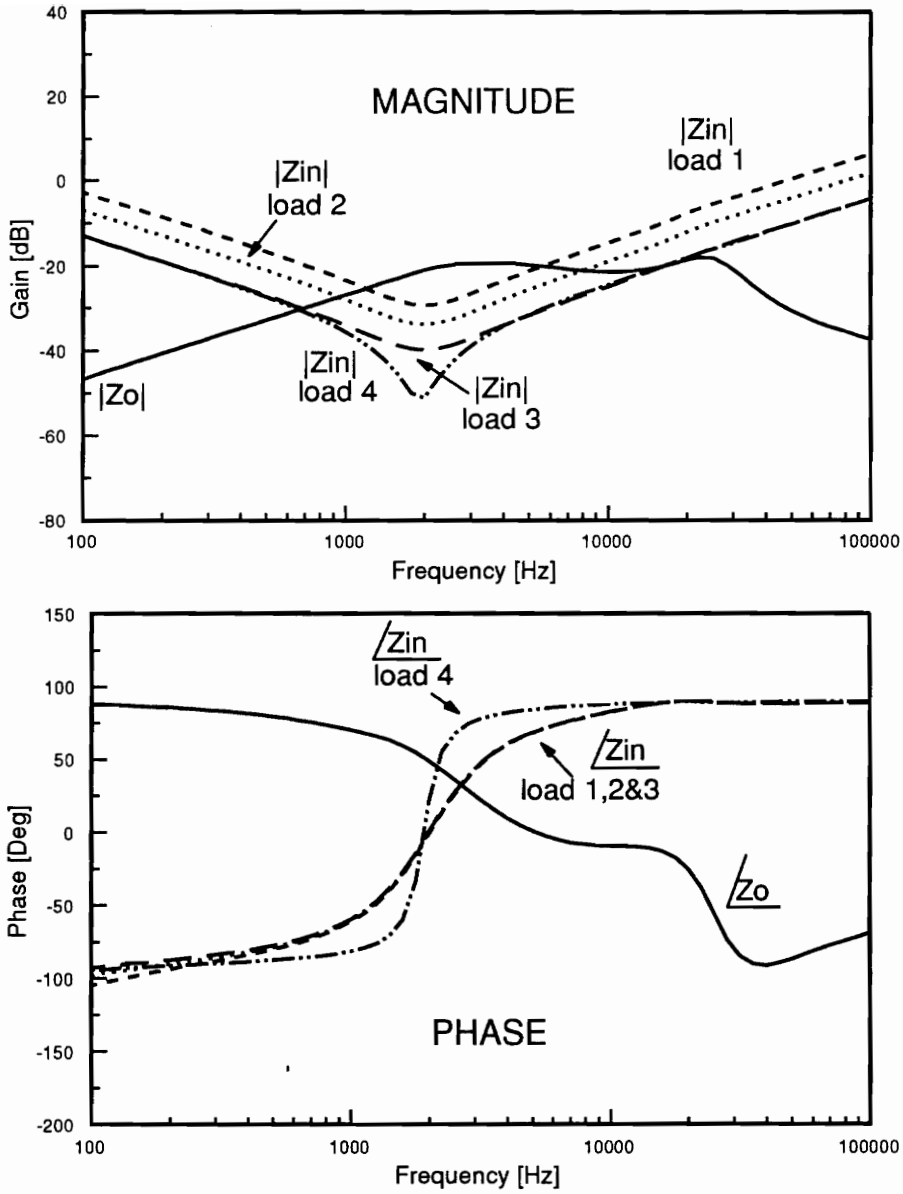


Figure 2.13 Interaction near loop gain crossover frequency of source subsystem

which it crosses over the 0 dB line. It can be seen that at the low frequency crossover of impedance overlap, the phase margin of T_m is approximately the phase margin of T_L, as in the case shown in Figure 2.12, interaction below the unloaded loop gain crossover frequency. Similarly to Figure 2.12, the bandwidth of T_L is reduced, which will negatively effect the transient response of the system. It can be seen that the high-frequency crossover of impedance overlap occurs after the unloaded loop gain crossover frequency. The phase margin of T_m at the high-frequency crossover of impedance overlap is important to T_L, because if it is small, there will be peaking of the loop gain T_L according to Equation 2.8 which could cause it to have small gain margin or magnitude larger than 0 dB. In Figure 2.13, there is some peaking of T_L at the final point of overlap, but by examining the loop gain, it can be seen there is no stability or relative stability problem because the magnitude of T_L remains well below 0 dB.

The effect varying the degree of impedance overlap has on the bus impedance, audiosusceptibility, and input impedance of the DDCU line conditioner is now examined. Figure 2.14 shows the output impedance of the line conditioner interacting with four different load subsystems. Figure 2.15 shows the circuit parameters used to generate the four load subsystems; these four loads will be used as examples throughout the remainder of this chapter.

With each successive filter, the degree of overlap increases and the phase margin decreases, as seen in the phase margin chart at the bottom of the figure. The reason that the phase margin decreases as the degree of impedance overlap increases can be observed by looking at the phase characteristics of the input and output impedances shown in the figure.



LOAD	Phase Margin at Initial Crossover	Phase Margin at Final Crossover
1	64	105
2	48	93
3	33	79
4	20	80

Figure 2.14 Impedance compatibility between output impedance of line conditioner and four load subsystems

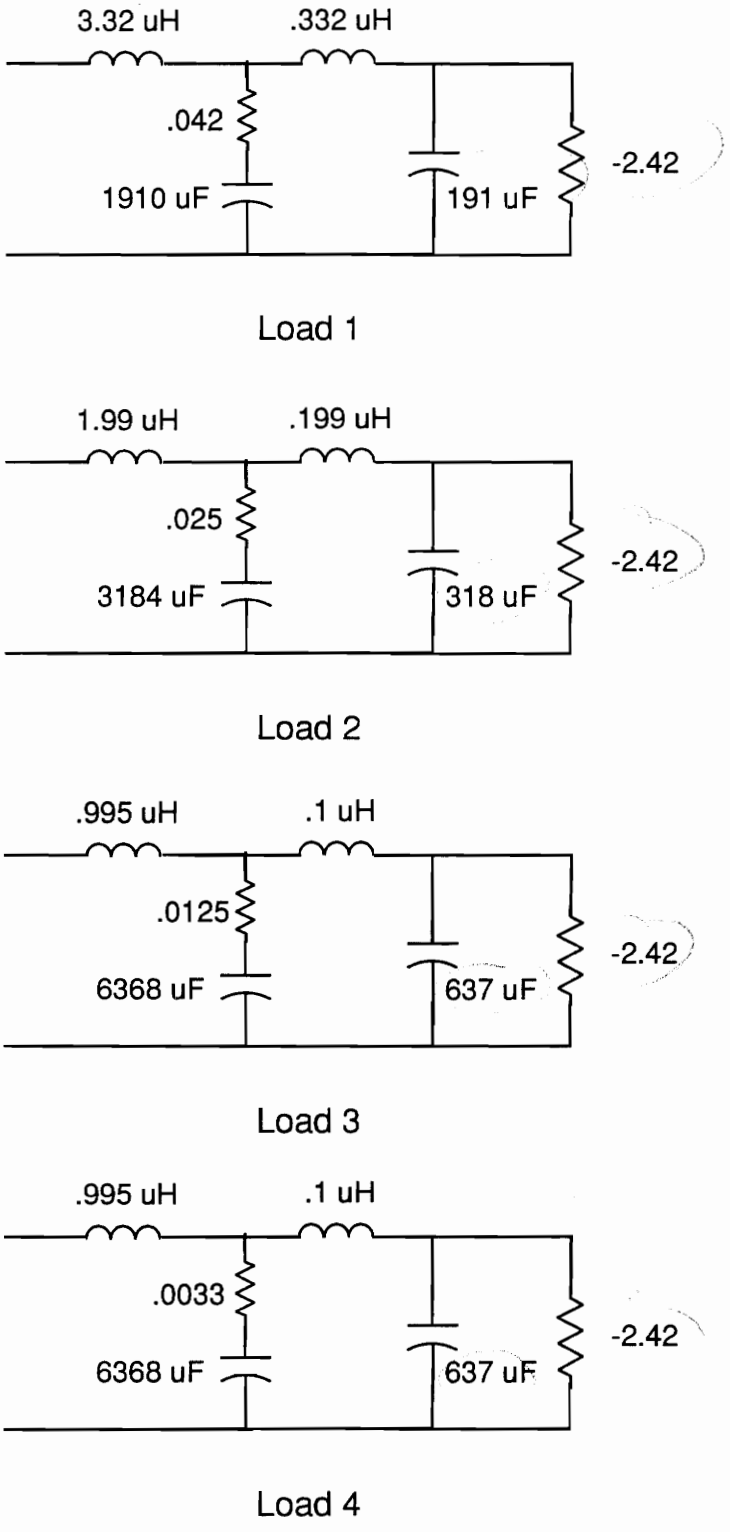


Figure 2.15 Circuit parameters of example load systems

The phase margin of T_m is defined by the equations:

$$PM1 = 180° - \angle T_m \quad = 180° - (\angle Z_o - \angle Z_{in}) \tag{2.10}$$

at the low-frequency crossover of impedance overlap, and

$$PM2 = -180° - \angle T_m \quad = -180° - (\angle Z_o - \angle Z_{in}) \tag{2.11}$$

at the high-frequency crossover of impedance overlap

By examining the phase of Z_o and Z_{in} in Figure 14, it can be seen that at low frequencies the phase of T_m approaches 180°, and at high frequencies, the phase of T_m approaches −180°. Therefore, interaction at high or low frequencies will cause loop gain, T_m, to have a small phase margin. As the degree of impedance overlap increases, the interaction moves to the low and high frequency ranges, thus causing the phase margin of T_m to decrease.

The bus impedance is shown in Figure 2.16; compared to the nominal unterminated case, the largest amount of upward deviation of the bus impedance occurs due to peaking at the point where T_m has the smallest relative stability margin. In this case the most peaking occurs at the low-frequency crossover of impedance overlap of load 4, where T_m has 20° phase margin. Less upward peaking occurs for each successive curve as the phase margin becomes larger.

The audiosusceptibility is also shown in Figure 2.16, it can be seen that the shape is similar to that of the bus impedance: there is peaking which is proportional to the relative stability margin of T_m. However, unlike the case of the bus impedance, the impedance overlap does not cause the peak audiosusceptibility to increase. For load 1, where T_m has large phase margin, there is no significant degradation, and the audiosusceptibility is improved in some frequency ranges.

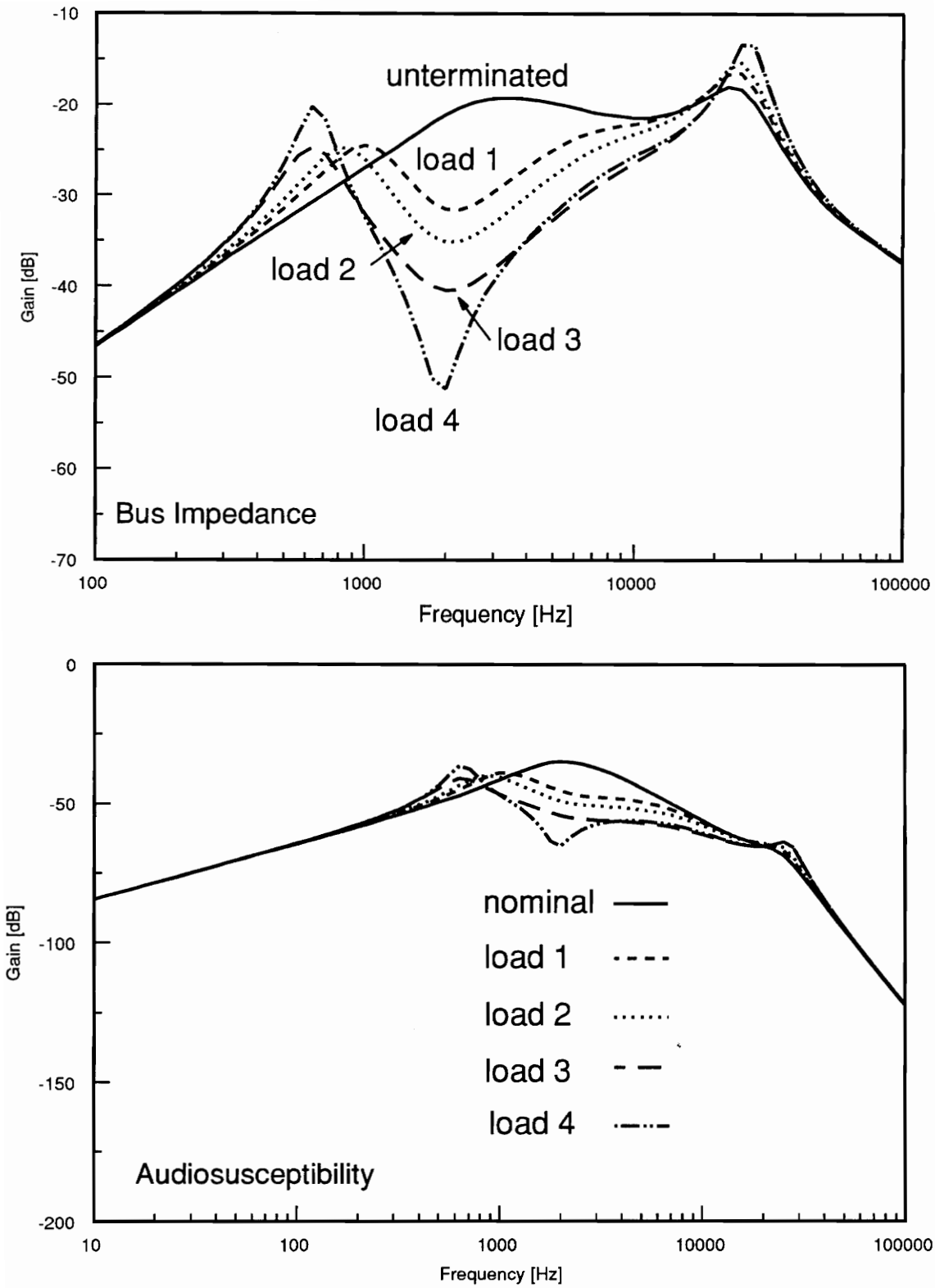


Figure 2.16 Bus impedance and audiosusceptibility for different loads

The input impedance of the DDCU line conditioner, without an input filter, is shown in Figure 2.17. Again, similar to the bus impedance and audiosusceptibility, there is peaking which is proportional to the relative stability margin, although for the input impedance it is downward peaking. For the case of load 1, which has a large phase margin, this peaking is minimal, and the input impedance does not suffer any significant degradation. If the input filter of the line conditioner is well-designed, there should be a sufficient gap between the output impedance of the filter and the input impedance of the line conditioner so that this peaking will not cause any interaction at the interface between the filter and line conditioner. However, if T_m had a very small phase margin which led to severe peaking, then such peaking could lead to undesirable interaction between the line conditioner and its input filter. Based upon the input impedance phase characteristic shown in Figure 2.17, it can be observed that such interaction could lead to a stability problem or small phase margin at the interface between the line conditioner and its input filter.

2.5.2 Effect on Load Subsystem

The effect that loading has on the load converter stability and performance will now be examined. Figure 2.18 shows a block diagram of the system to be considered; for this discussion the following parameters are defined:

Y_i = closed loop input admittance of the load converter,

Z_o = output impedance of unloaded source subsystem, and

$T_{m2} = Z_o Y_i$ = loop gain due to the loading effect.

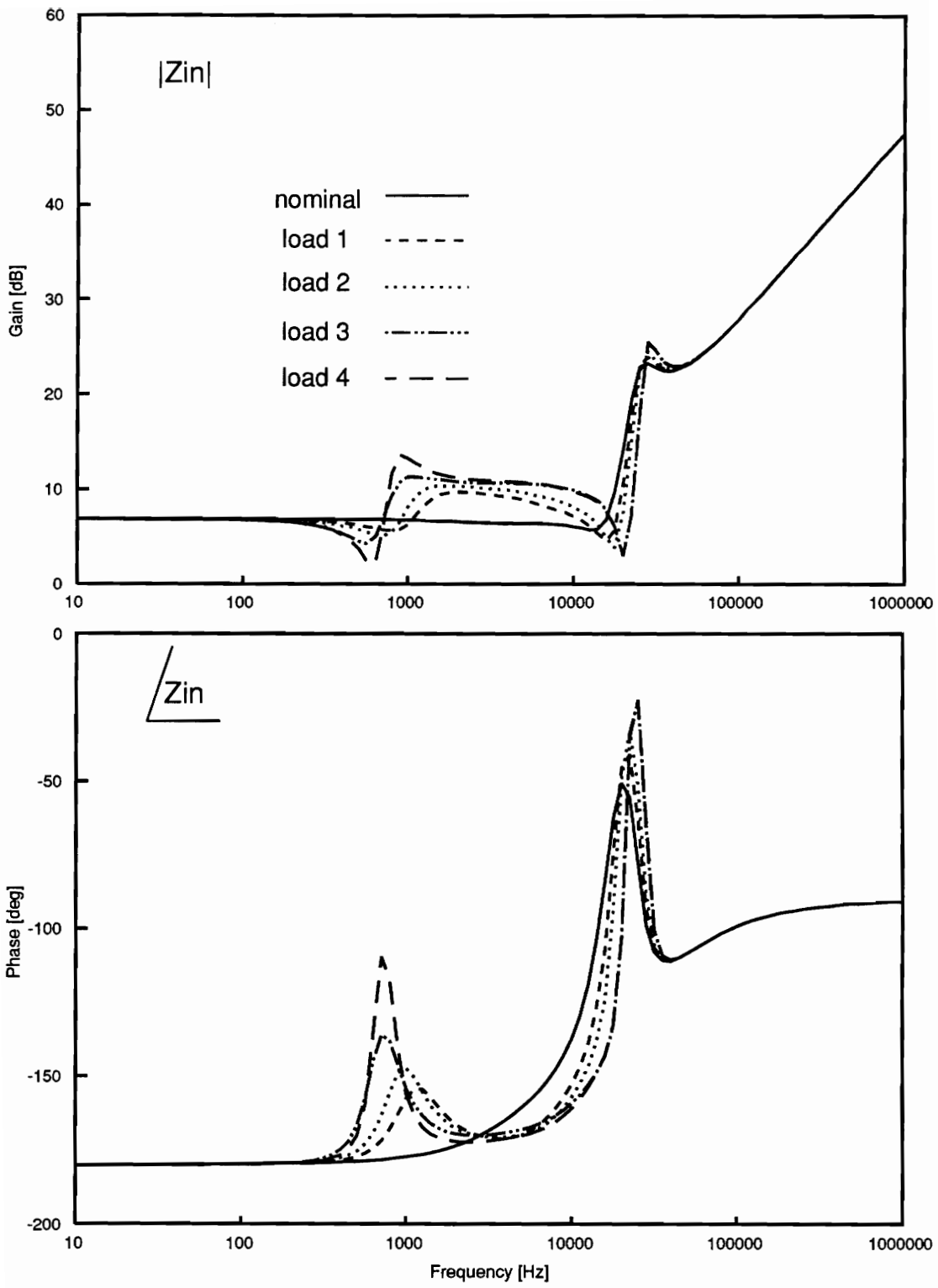


Figure 2.17 Input impedance of line conditioner without input filter for different loads

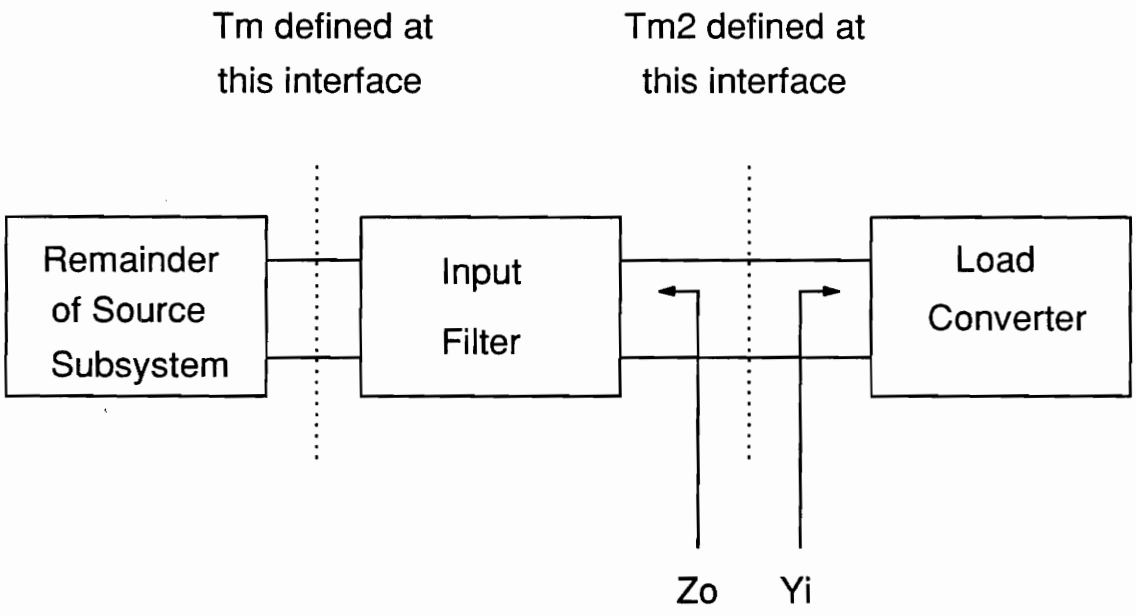


Figure 2.18 Block diagram of system

It is assumed that the load subsystem has one or more well-designed input filters between the load converters and the voltage bus. For a well-designed input filter, the input impedance of the load converter is well-separated from the output impedance of the filter, which means $|T_{m2}| \ll 1$. $|T_{m2}| \ll 1$ prevents a stability problem and performance degradation. A stability problem will occur if $|T_{m2}| > 1$ because the phase of the input impedance of a properly-designed load converter is -180 degrees at low frequency, so any interaction will lead to encirclement of the (-1,0) point and a stability problem.

Due to the wide separation of impedances at the interface between the load converter and its filter, the input filter serves as a buffer between the load converters and the bus. Therefore interaction at the bus will not affect the individual load converters, as long as loop gain T_m has relative stability margins large enough to prevent excessive peaking. An example showing this using the Space Power System is now presented using a PWM buck load converter and the four input filters from Figure 2.15. Figure 2.19 shows the input impedance of the load converter in relation to the output impedance of the series combination of its four input filter designs and the DDCU line conditioner. It can be seen that in each case there is wide separation between these impedances. This wide separation implies that loop gain T_{m2} has a magnitude much less than one and the input filter is serving as a buffer between the bus and the load converter. Since the input filter is serving as a buffer between the bus and the load converter for these cases, the interaction at the bus will have a negligible effect upon the load converter. In this example the filter serves as a good buffer, even in the case of load 4 where phase margin is only 20°.

An example where the interaction at the bus does not have a negligible effect upon the load converter is now presented using the system shown in Figure 2.20. In this example system, the filter of load one from Figure 2.15 is used with a PWM buck converter as

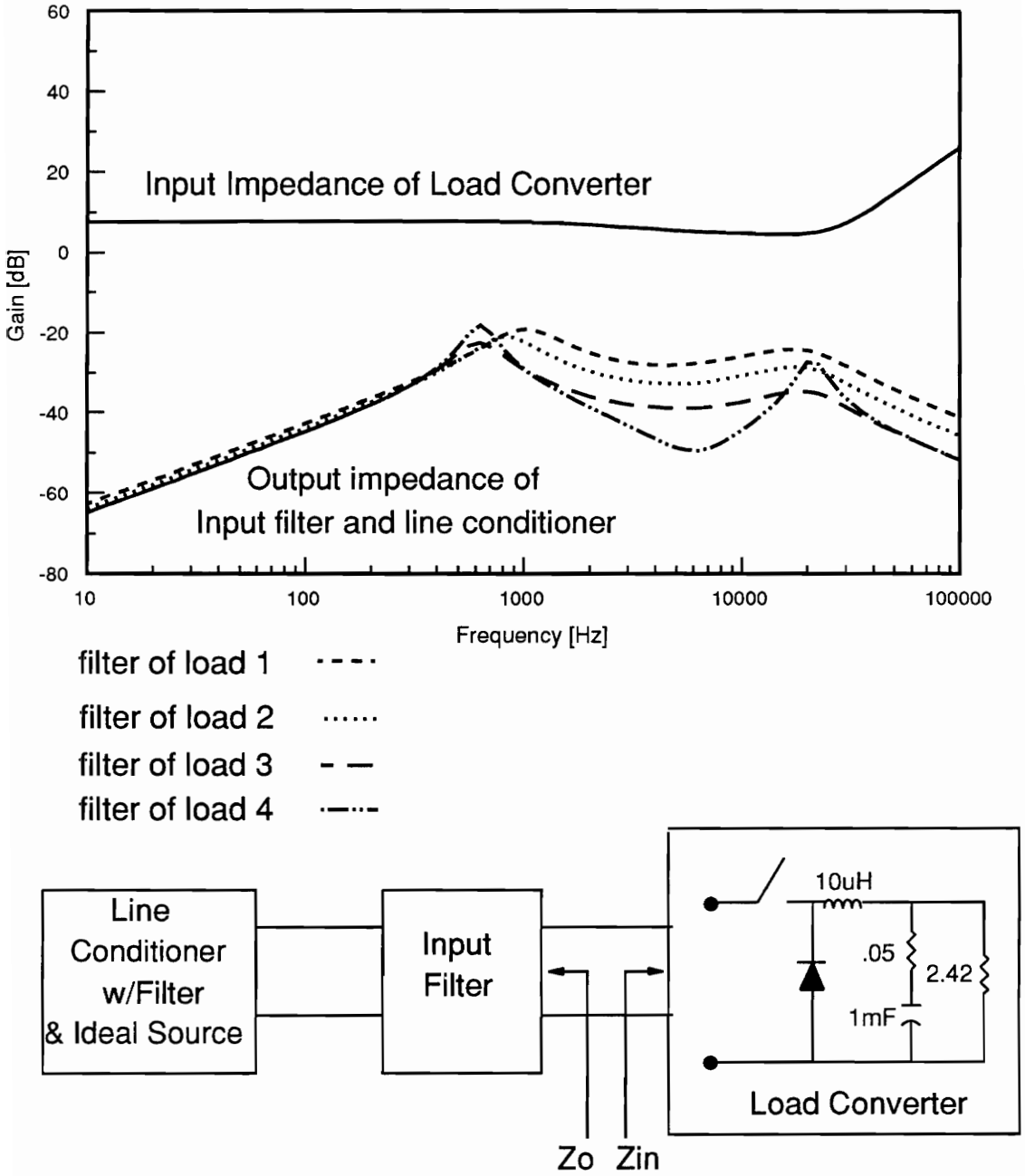


Figure 2.19 Impedance compatibility between load converter and input filter for different filters

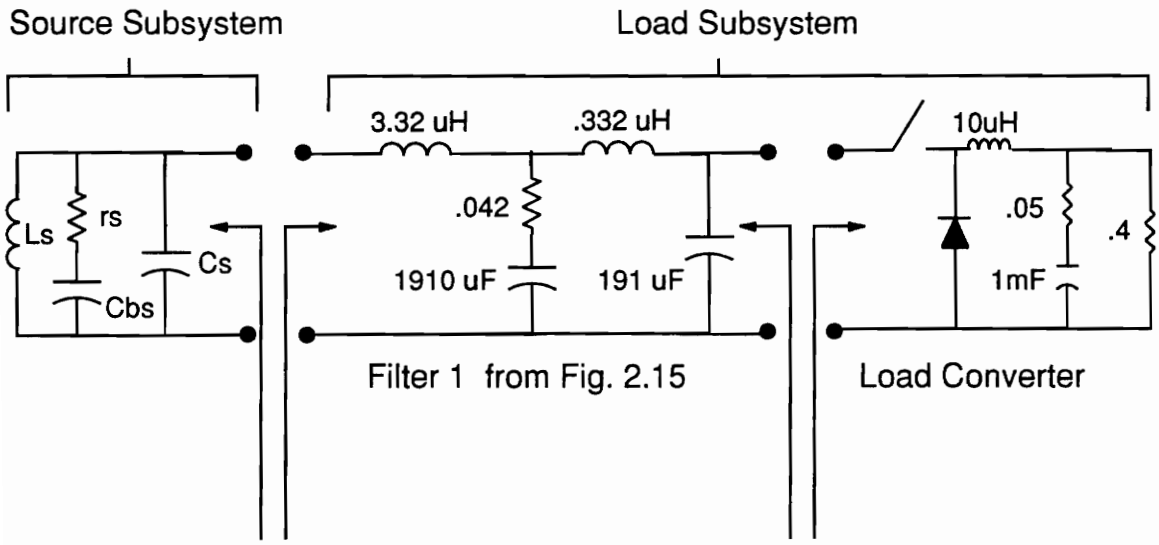


Figure 2.21
examines compatibility
at this interface

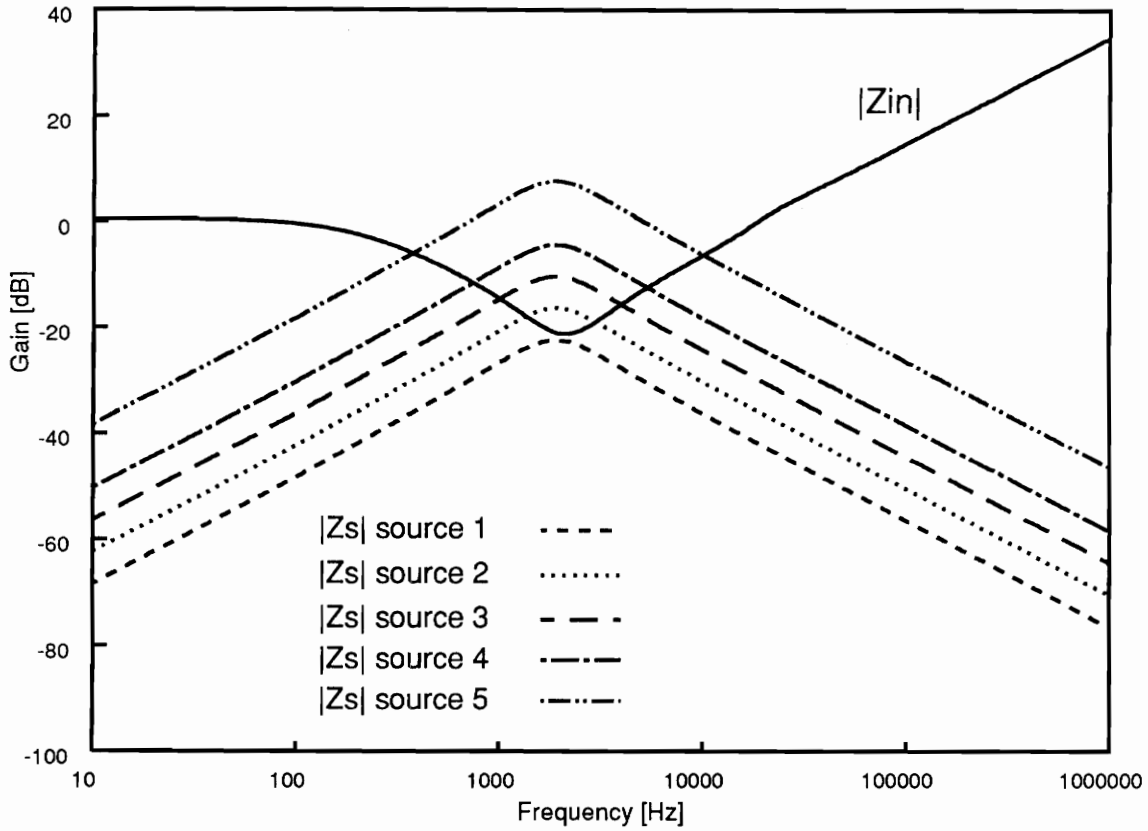
Figure 2.22
examines compatibility
at this interface

	Ls	rs	Cbs	Cs
Source 1	6uH	.075	10.6mF	1.06mF
Source 2	12uH	.15	5.3mF	530uF
Source 3	24uH	.3	2.65mF	265uF
Source 4	48uH	.6	1.33mF	133uF
Source 5	192uH	2.4	332uF	33uF

Figure 2.20 Circuit parameters and case setup for Figures 2.21 and 2.22

a load subsystem. The source subsystem is no longer the DDCU line conditioner; instead, the five source subsystems shown in Figure 2.20 are used. Figure 2.21 shows the impedance compatibility between the source subsystem and load subsystem for each of the five source impedances. For each successive source, the amount of impedance overlap with the load increases. A polar plot of the loop gain, T_m, is shown at the bottom of the figure; it can be seen that for each of the first four sources, the phase margin decreases, and finally for source five, the (-1,0) point is encircled, and the system is unstable. As explained in Section 2.3, it is the active nature of the load subsystem which causes the system to become unstable. Since the low frequency input impedance phase is $-180°$, interaction between the source and load subsystems in this frequency range causes the magnitude of the phase of loop gain T_m to become larger than 180; this causes the polar plot to encircle the (-1,0) point.

Figure 2.22 shows the impedance compatibility and a polar plot of loop gain T_{m2} at the interface between the load converter and its input filter. It can be seen that the non-ideal sources which cause the interactions of Figure 2.21 also cause the output impedance of the filter to peak, when compared to the case of the ideal source. For the first four sources, there is still a sufficient impedance gap between the output impedance of the filter and the input impedance of the load converter, so there is no significant effect on the load converter. However, for source five, which was shown in Figure 2.21 to cause an unstable system, there is impedance overlap at the interface between the load converter and its filter which leads to instability; the instability can be observed by the encirclement of the (-1,0) point on the polar plot of T_{m2}, which is also shown in Figure 2.22.



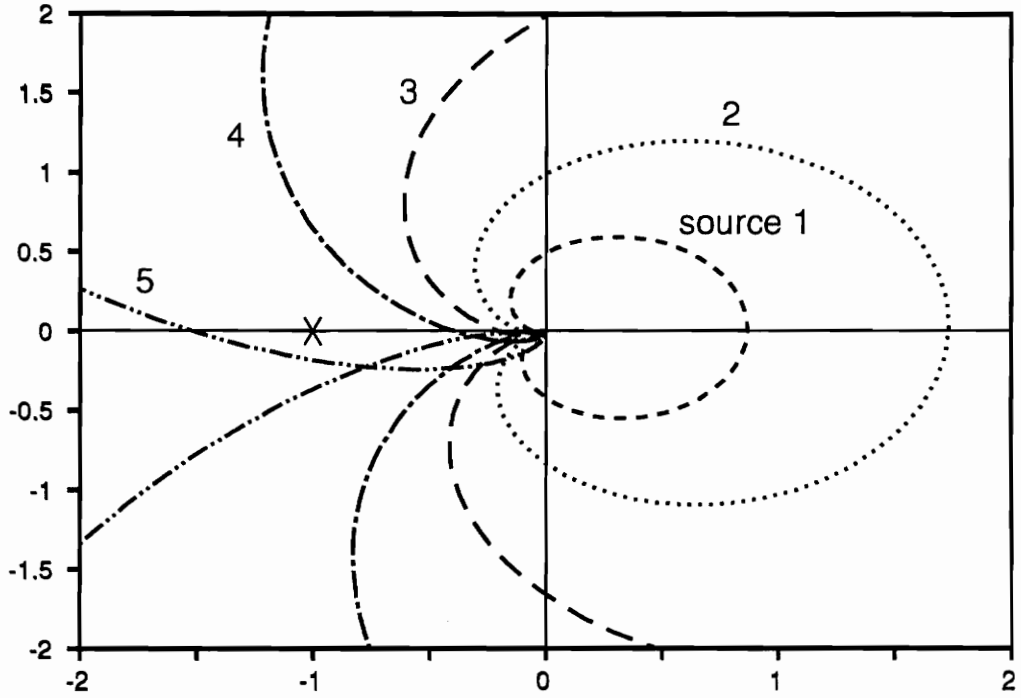


Figure 2.21 Impedance compatibility and polar plot for interaction between five source subsystems and load converter with filter of load 1

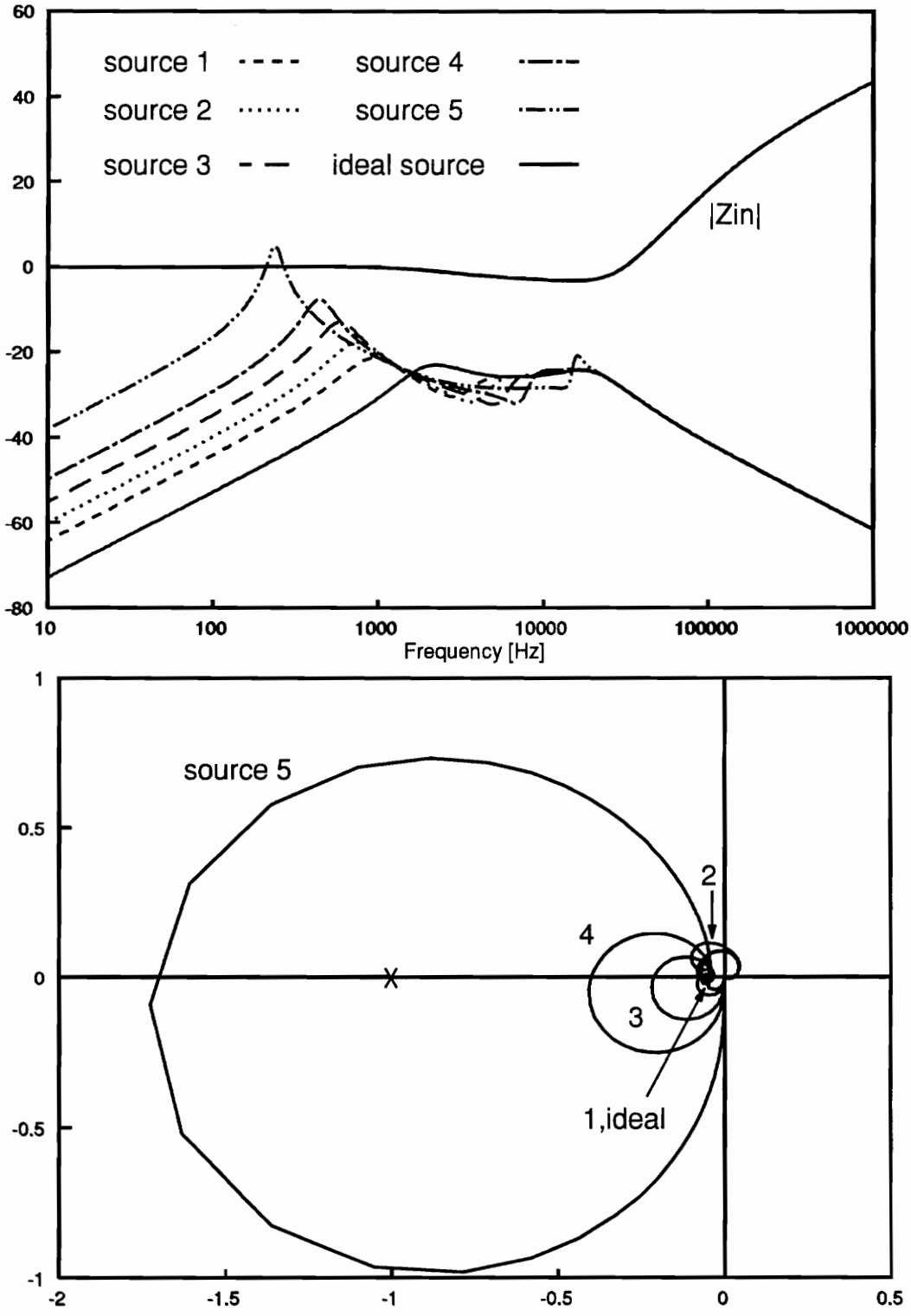


Figure 2.22 Impedance compatibility between load converter and input filter of load 1 with five source subsystems

2.6 Summary

This chapter presented an analysis of the effects of impedance overlap. It was shown that the ratio of impedances at the interface between subsystems can be viewed as a system loop gain and can be used to determine system stability and relative stability. It also was shown that if no impedance overlap between subsystems is present, then the integrated system has minimal interactions, and the integrated system performance depends upon that of the individual subsystems. If impedance overlap is present, then interaction between the subsystems is present. However, the presence of impedance overlap does not necessarily mean that the system performance will be severely degraded; it was seen that for the case where impedance overlap was present but loop gain T_m had a large phase margin, the system bus impedance, input impedance, and audiosusceptibility suffered no significant degradation. If performance degradation is present, it can cause the transient response to slow and suffer more overshoot. The amount of degradation depends on the relative stability margin of T_m and the low-frequency crossover of impedance overlap. Performance degradation can be predicted by examining peaking of the bus impedance, as well as by examining the input impedance, audiosusceptibility, and loop gain of the line conditioner.

CHAPTER 3

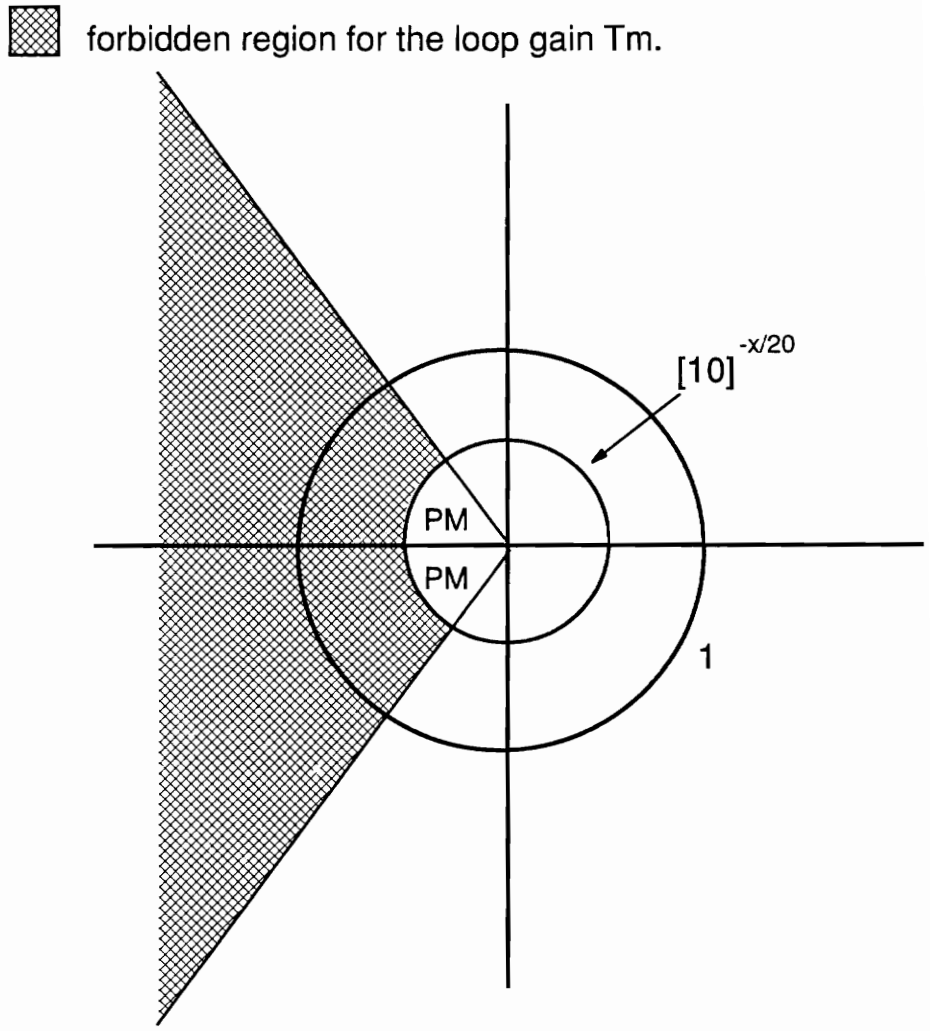
DESIGN OF DISTRIBUTED POWER SYSTEMS WITH UNSPECIFIED LOADS

3.1 Introduction

One possible design method for a DPS is to design the source subsystem using an ac unterminated modelling approach [8]. Then, based upon the worst-case output impedance of the source, an input impedance specification can be set for the load subsystem to avoid interaction which has an adverse effect on the system. In this chapter, a methodology for developing the load impedance specification for an unknown load subsystem is introduced. The method assumes that the output impedance of the source subsystem is known. It ensures stability and minimal performance degradation of the integrated system, despite allowing impedance overlap at the interface between subsystems. The Space Power System is used to demonstrate various methods of generating the load impedance specification. The various methods are compared, all of which guarantee system stability and minimal performance degradation. The possibility of checking individual components of the load subsystem against the specification, opposed to the load subsystem as a whole, is discussed.

3.2 Forbidden Region Concept

It has been seen in Chapter 2 that the stability and relative stability of loop gain T_m can be used to determine integrated system stability and performance. As shown in Figure 2.3, by applying the Nyquist criteria to a polar plot of the loop gain, T_m, both the stability and relative stability of T_m can be examined. Consider Figure 3.1; suppose that the



AVOIDING FORBIDDEN REGION ASSURES:

$180 - PM \text{ degrees} < \angle Tm < 180 + PM \text{ degrees}$

if magnitude of loop gain is 1
=> stability and desired phase margin

AND

$|Tm| < [10]^{-x/20}$

if phase of loop gain is 180 degrees
=> stability and x dB of gain margin

Figure 3.1 Forbidden region of loop gain Tm

loop gain, T_m, never enters the shaded portion of the polar plot. In such a case, assuming that the individual subsystems are stable and all eigenvalues are observable, it is not possible for the polar plot of T_m to encircle the (-1,0) point, so integrated system stability is guaranteed. Also, any time the magnitude of T_m touches the unit circle, the phase of T_m will always be such that there is at least PM degrees of phase margin. Furthermore, any time the phase of T_m is -180, the magnitude of T_m will be less than $10^{-x/20}$, so there will always be at least x dB of gain margin. If the polar plot of T_m avoids this forbidden region, then this guarantees that the integrated system will be stable, will not be conditionally stable, will have a desired stability margin, and will have minimal performance degradation.

3.3 Definition of Example System

In this chapter the Space Station Power System of Figure 1.2 will be used as an example. The system has a complex source subsystem which contains many elements and has been designed using an ac unterminated modelling approach. In Section 3.2, it was shown that it is desirable that the loop gain T_m avoid the forbidden region. In Section 2.2, it was shown that T_m depends only upon the output impedance of the source subsystem and the input impedance of the load subsystem. Therefore, it is possible to make T_m avoid the forbidden region by means of an input impedance specification for the load subsystem, since the output impedance of the source subsystem is known. The output impedance of the source subsystem is used to generate a load input impedance specification.

The source subsystem consists of the DDCU line conditioner, but it also contains several other subsystems including a solar array, DCSU, SSU, MBSU, BCDUs, as well as filters and cable impedances. It is necessary to analyze the output impedance of the

entire source subsystem in order to properly develop a load specification which will cause loop gain T_m to avoid the forbidden region of Figure 3.1 for all possible modes of operation. Analysis of the source subsystem output impedance can be greatly simplified if the input filter of the line conditioner serves as a buffer and isolates the DDCU line conditioner and its loads from the rest of the system. In such a case, the line conditioner alone can be viewed as the source subsystem. In other words, if there is wide impedance separation under all operating conditions at the interface between the DDCU line conditioner and its input filter, then the rest of the source system has a negligible effect on the output impedance of the DDCU line conditioner. If there is not wide impedance separation at this interface under all operating conditions, then the analysis of the source output impedance must consider all components of the source subsystems at all possible operating conditions: a very tedious task.

Figure 3.2 shows the worst-case impedance compatibility between the line conditioner and its input filter. It can be seen that under this worst-case condition, there is still a large impedance gap at this interface. Therefore, as explained above, it is expected that the output impedance of the line conditioner will be affected minimally by the rest of the source subsystem. Figure 3.3 shows a comparison between the output impedance of the line conditioner using an ideal source and the worst-case actual source. It can be seen that as expected, the rest of the source subsystem has a negligible effect on the output impedance of the line conditioner. This greatly simplifies the analysis of the output impedance of the source subsystem. To analyze this impedance, which is necessary to form the load input impedance specification, the rest of the source subsystem can be regarded as negligible, and the source of the line conditioner can be considered ideal.

An example where the input filter does not serve as a buffer between the converter and the rest of the source subsystem, and the source can not be considered ideal, was

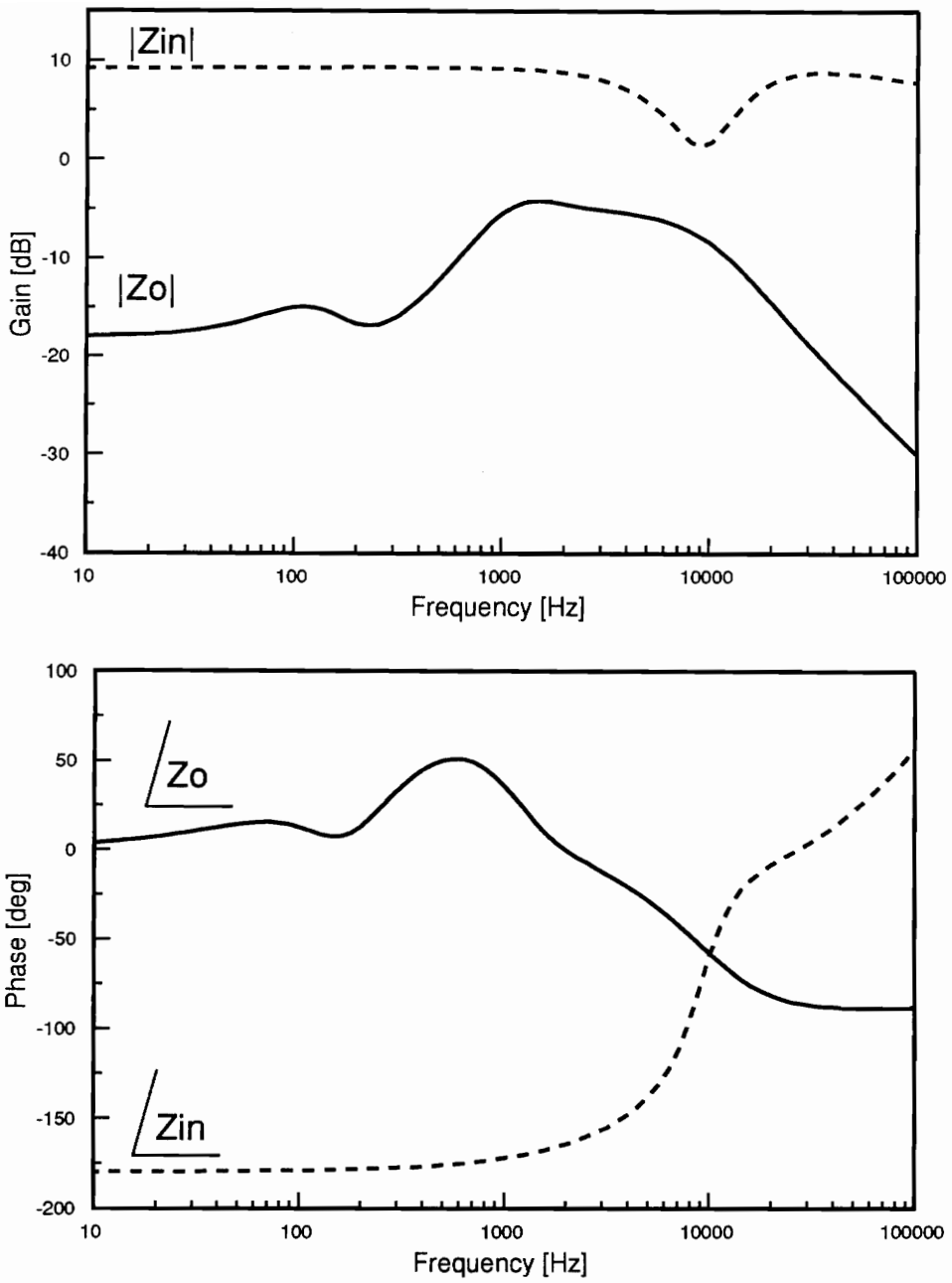


Figure 3.2 Worst case impedance compatibility between the line conditioner and its input filter

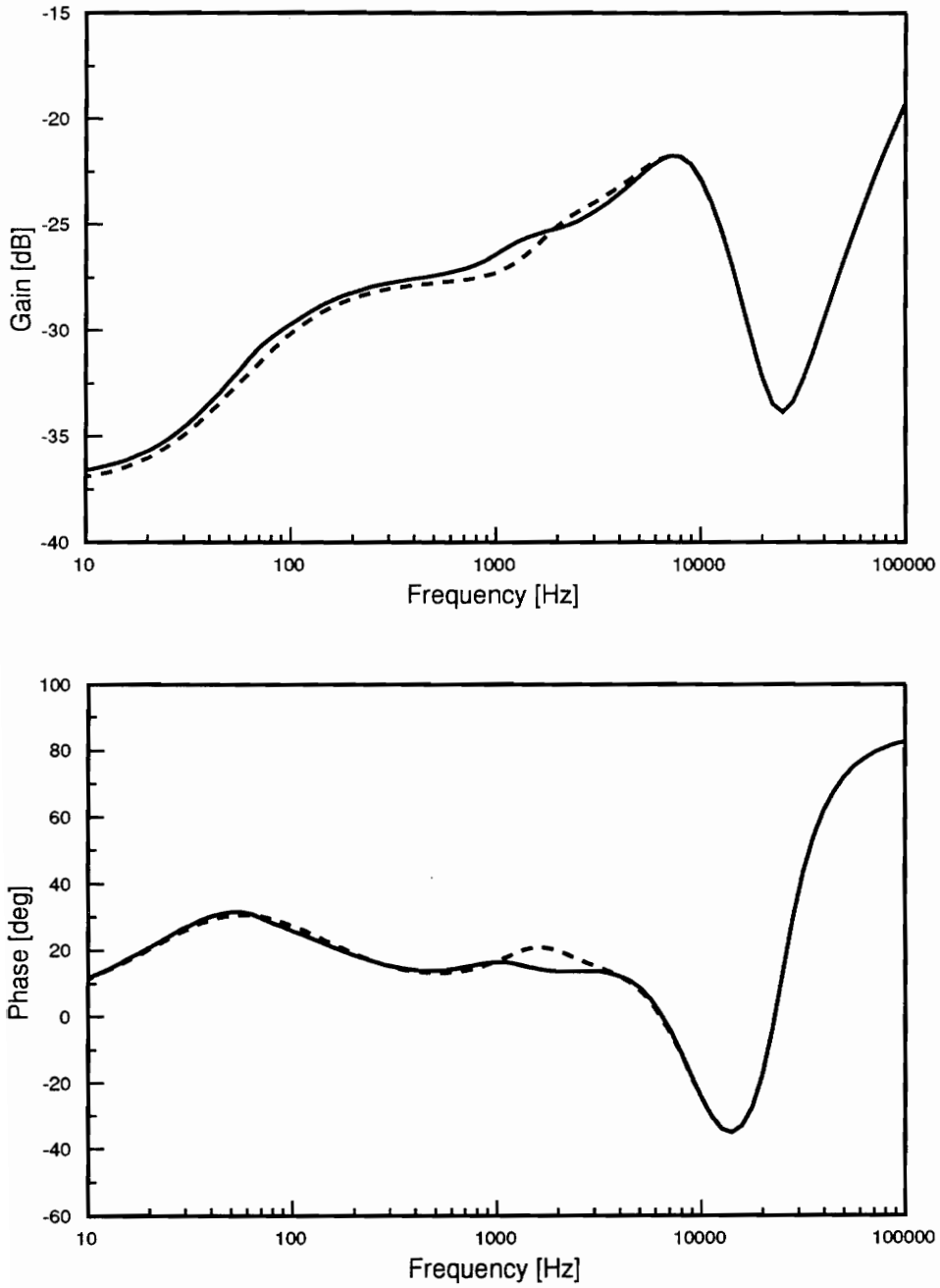


Figure 3.3 Comparison of output impedance using ideal source and actual system source

presented in Section 2.5.2. In Figure 2.22 the output impedance of the source subsystem with an ideal source is significantly different from the output impedance with each of the actual system sources. In such a case the actual system source must be used when analyzing the source subsystem output impedance.

3.4 Formation of Input Impedance Specification for Example Zo curve

The output impedance of the Space Power System line conditioner at a given operating condition is shown in Figure 3.4. Using this output impedance curve of the source subsystem, it can be shown how to generate a phase specification for the input impedance of the load subsystem which causes T_m to avoid the forbidden region of Figure 3.1.

At each frequency the phase of the output impedance is known. Based upon this, the range of input impedance phase which would cause loop gain T_m to violate the forbidden region, if interaction were to occur at a given frequency, can be determined according to the equations:

$$180° - PM < \angle Z_o - \angle Z_{in} < 180° + PM \quad , \tag{3.1}$$

and

$$-180° - PM < \angle Z_o - \angle Z_{in} < -180° + PM \quad . \tag{3.2}$$

These calculations can be made by plugging in a desired phase margin and the known output impedance phase of the source subsystem at each frequency. When these calculations are made, a phase band is generated which serves as a specification for the input impedance phase. For the example curve in Figure 3.4, and a phase margin of 60°, the phase band was calculated; it is the shaded region in Figure 3.4. Such a specification guarantees the phase margin will always be at least a specified value, in this case 60°. The next step of forming the input impedance specification is to add x dB to the

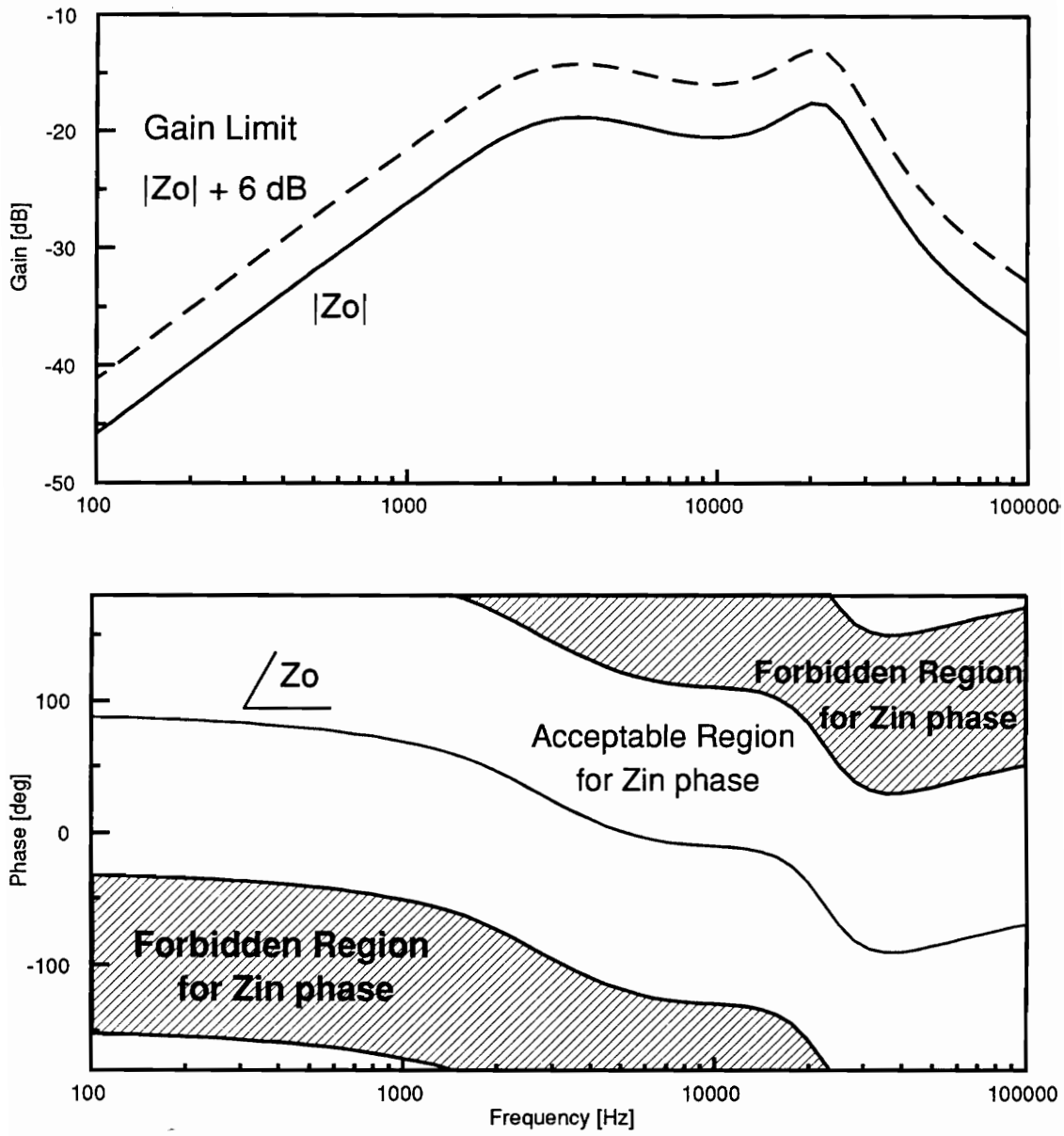


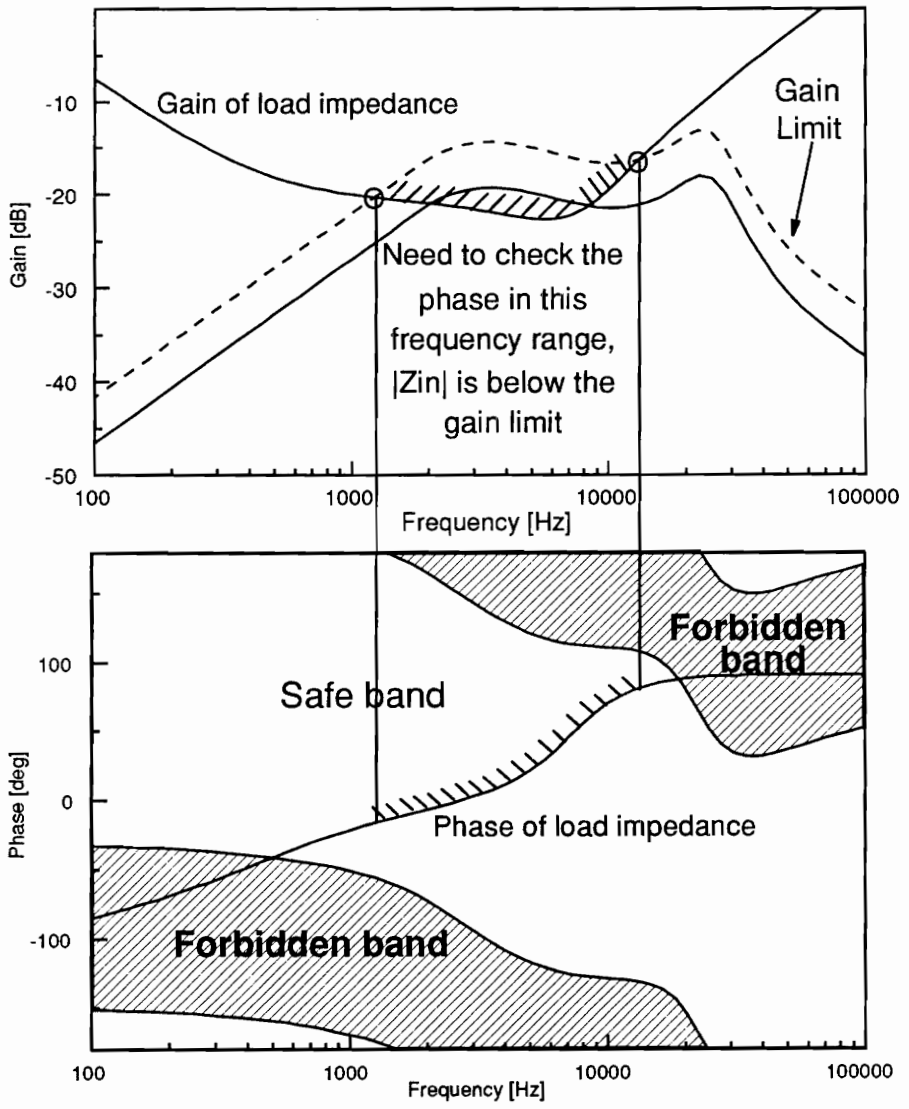
Figure 3.4 Generation of phase specification for single output impedance curve Specification ensures 60 degrees of phase margin and 6 dB of gain margin

magnitude of the output impedance curve to form a gain limit which will be used to guarantee the system has a specified gain margin. Any time that the input impedance magnitude falls below this gain limit, its phase must be checked against the phase specification, because the magnitude of T_m is greater than $10^{-\frac{x}{20}}$. The dashed line in Figure 3.4 is the gain limit; a gain margin of 6 dB was used, which means that the phase must be checked at any frequency that the magnitude of T_m is greater than .5. If the phase of the input impedance falls in the acceptable region, at all frequencies where the magnitude of Z_{in} is below the gain limit, then the loop gain T_m will avoid the forbidden region.

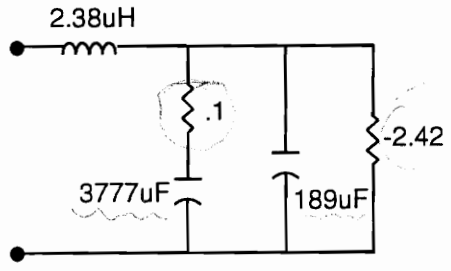
An example of the use of this specification is shown in Figure 3.5. An example load input impedance curve is shown interacting with the output impedance. Since the magnitude of the input impedance of this load falls below the gain limit, there is the possibility that the loop gain, T_m, will violate the forbidden region. In order to check if this load causes T_m to violate the forbidden region, the phase of the input impedance must be compared with the input impedance phase specification during the entire frequency range that the magnitude of the input impedance falls below the gain limit. It can be seen that the example load shown meets the specification, and therefore the polar plot of T_m avoids the forbidden region, as shown at the bottom of the figure. Since this load meets the specification, it is guaranteed that the loop gain, T_m, always has at least 6 dB of gain margin and 60° of phase margin.

3.5 Worst-Case Output Impedance

In the previous section, it was demonstrated that once the worst-case output impedance is identified, it is simply a matter of algebra to generate a phase specification which causes the loop gain, T_m, to avoid the forbidden region. However, many times in a DPS it is not possible to identify the output impedance at a single operating condition as



Load meets specification, so polar plot will avoid the forbidden region



Circuit used to simulate Zin

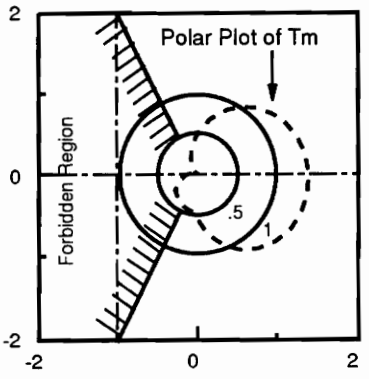


Figure 3.5 Example load interacting with line conditioner

the worst-case output impedance. Figure 3.6 demonstrates the need to consider both magnitude and phase when determining the worst case output impedance to be used to generate an input impedance specification.

The figure shows two output impedance curves which represent the output impedance of a typical source at two different operating conditions (A and B). Typically operating condition A would be considered the worst-case output impedance and be used to analyze system stability because it has larger magnitude and therefore a larger degree of impedance overlap with the load subsystem. However, for the given load impedance, the interaction with output impedance A shows stability and a 55° phase margin. On the other hand, the interaction of the load with the output impedance at operating condition B has a much lower relative stability margin; the phase margin is less than 10°.

This analysis shows that different operating conditions other than the worst-case magnitude can be the worst-case for stability. Therefore, when determining a specification for load impedance, the output impedance at operating conditions other than the worst case magnitude must be considered. It can be seen that the example phase specification for a single curve, in Section 3.4, is not sufficient to guarantee adequate phase or gain margin once the operating condition and output impedance change. The technique used to form the specification is valid, but the phase of all output impedance operating conditions for which impedance overlap is possible must be taken into consideration.

3.6 Monte Carlo Analysis

The output impedance of the DDCU line conditioner at various operating conditions is shown in Figure 3.7. It can be seen that the output impedance is not well-behaved: different operating conditions have worst-case magnitude and/or phase at different

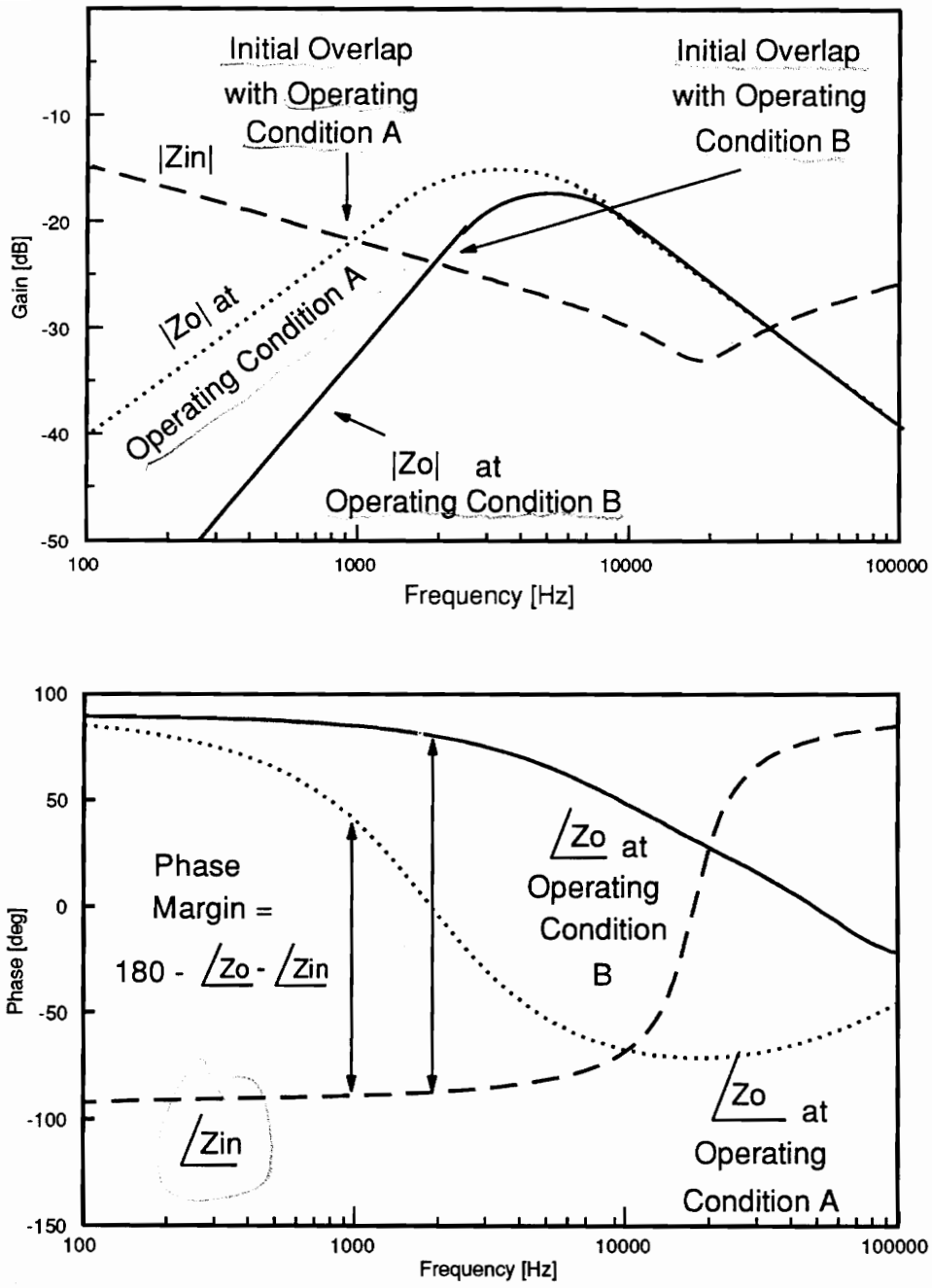
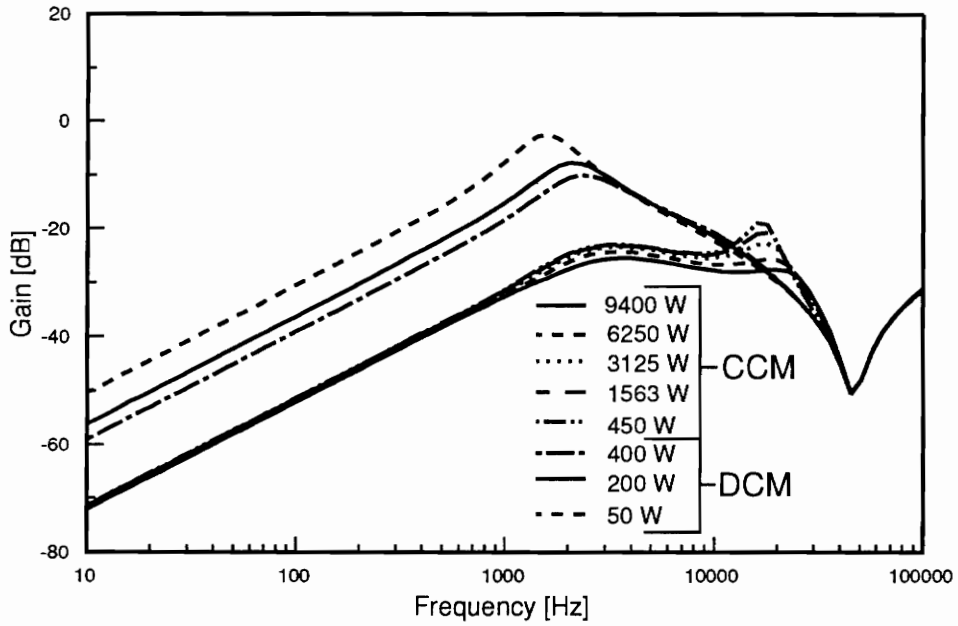


Figure 3.6 Identification of worst case output impedance:
At the initial frequency of overlap with operating condition A there is 55 degrees of phase margin
At the initial frequency of overlap with operating condition B there is less than 10 degrees of phase margin



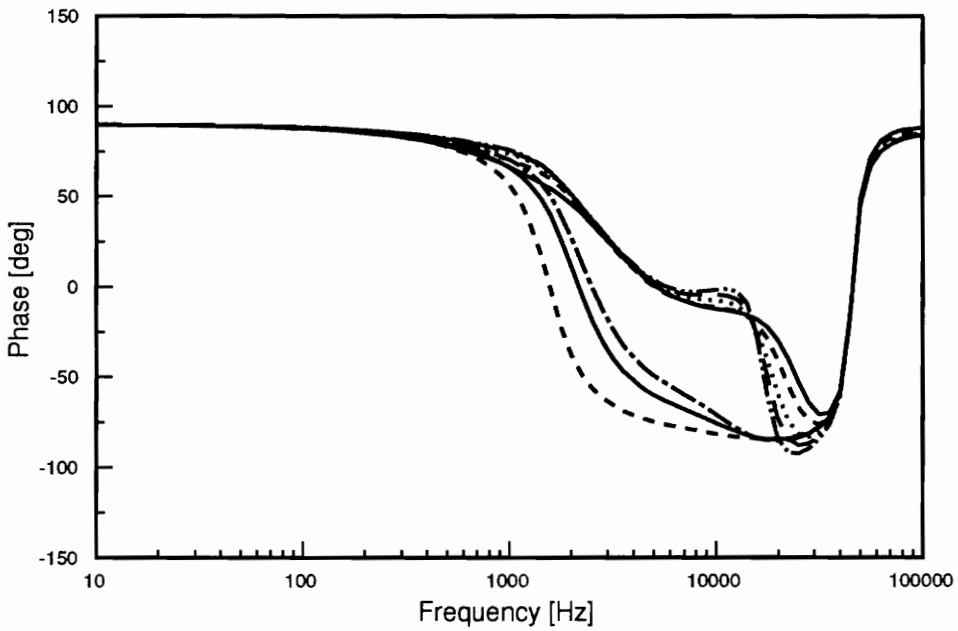


Figure 3.7 Output impedance of DDCU line conditioner for various operating conditions

frequencies. Also there is a significant jump in the output impedance magnitude as the line conditioner changes from the continuous conduction mode (CCM) to the discontinuous conduction mode (DCM) of operation. In this case, it is not possible to identify any one operating condition as the worst-case output impedance. As explained in Section 3.5, a band of possible values of output impedance phase at each frequency must be found in order to properly form a phase specification that causes loop gain T_m to avoid the forbidden region under all operating conditions.

One practical technique to find the range of possible values of output impedance phase at each frequency is to perform Monte Carlo analysis on the output impedance for a wide range of operating conditions. Monte Carlo analysis is easily performed through computer simulation, using a software package such as SABER or SPICE. With Monte Carlo analysis, circuit parameters are given a tolerance; then the computer performs multiple runs of the desired analysis, randomly choosing component values within the given tolerance range of each component. If enough runs through the circuit are performed, it can be assumed with a high level of confidence that the entire range of possible values is covered. A discussion of Monte Carlo analysis and confidence intervals is presented in [4 & 5].

Monte Carlo analysis was performed on the output impedance of the DDCU line conditioner; 2000 runs were done at each operating condition. The result of the Monte Carlo analysis for all DCM operating conditions is shown in Figure 3.8, the result for all CCM operating conditions is shown in Figure 3.9, and the result for all operating conditions, including both CCM and DCM, is shown in Figure 3.10. This Monte Carlo analysis gives a band of possible values of output impedance magnitude and phase at each frequency; it includes all operating conditions and also accounts for variations in the output impedance due to factors such as the assumption that the source is ideal,

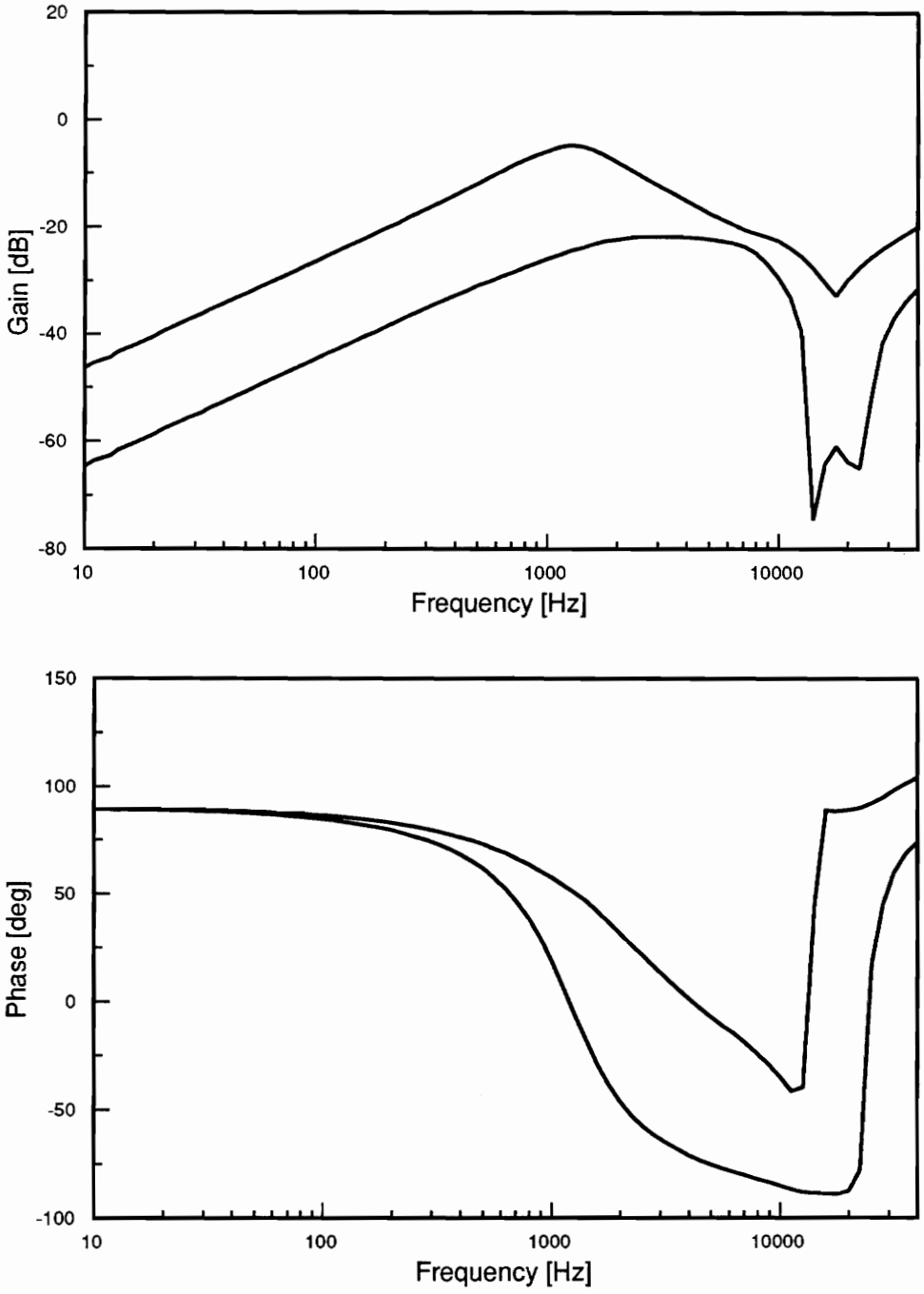


Figure 3.8 Monte Carlo analysis of line conditioner output impedance all DCM operating conditions

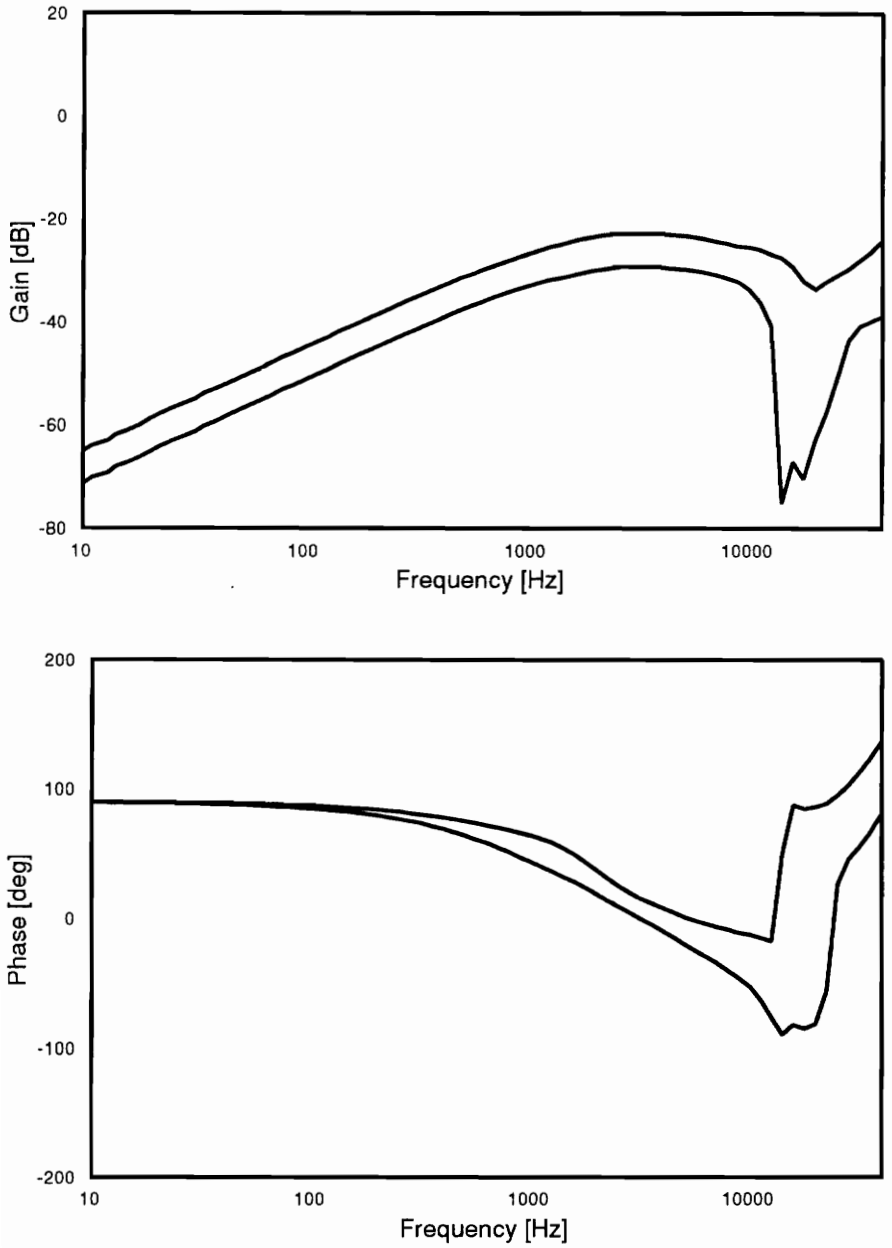
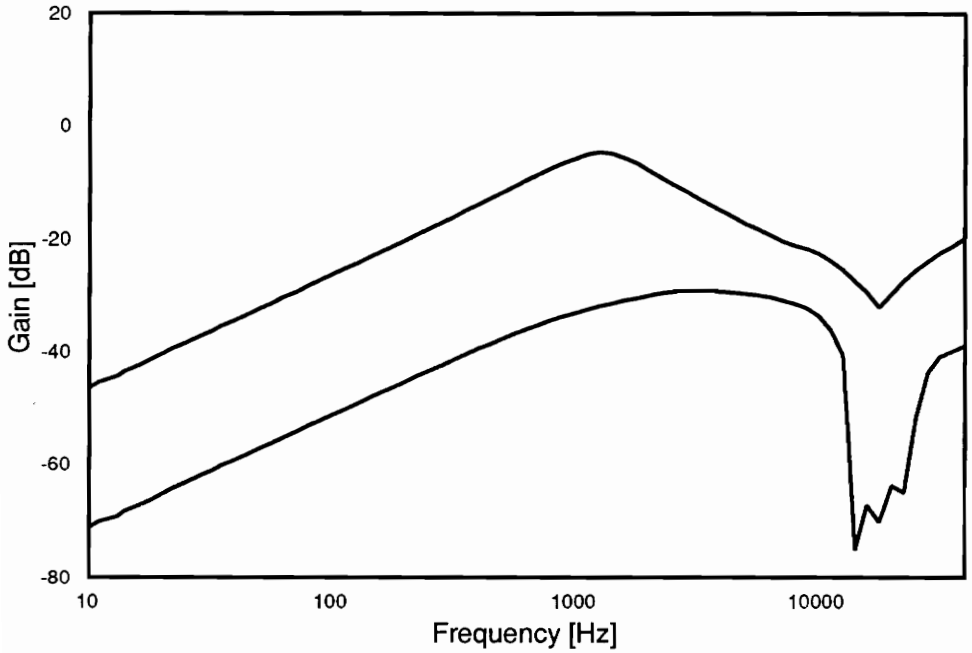


Figure 3.9 Monte Carlo analysis of line conditoner output impedance all CCM operating conditions



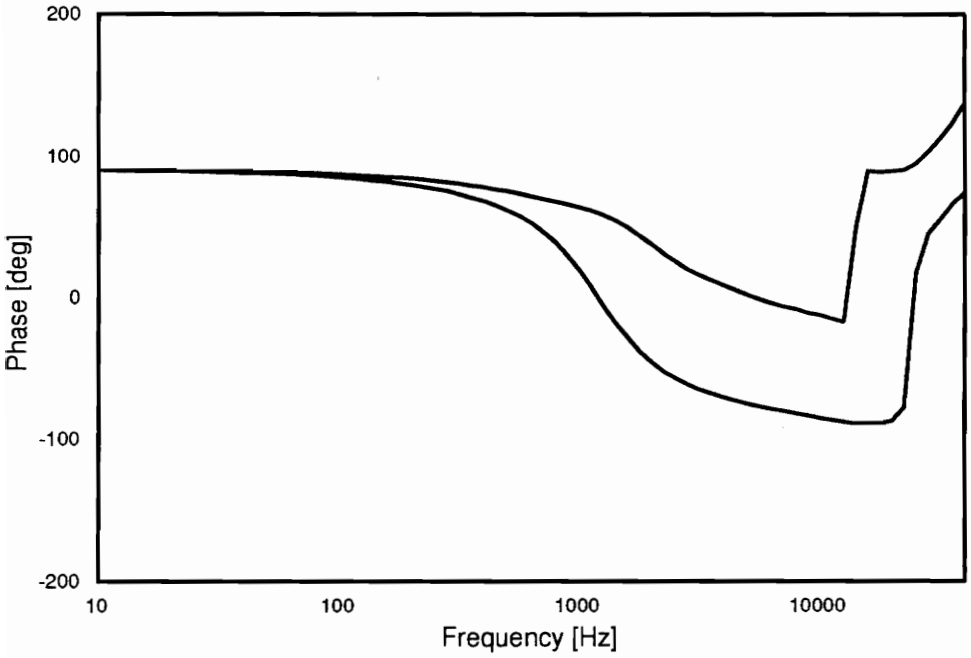


Figure 3.10 Monte Carlo analysis of line conditioner output impedance all operating conditions - DCM and CCM

temperature variation, component tolerance, and aging. Using the Monte Carlo analysis, it is now possible to derive a load impedance specification which ensures the stability and performance of the integrated system, regardless of operating condition, while not being too difficult for the load subsystem to meet.

3.7 Possible Methods of Forming the Load Input Impedance Specification

Previously it has been shown that the worst-case magnitude of the output impedance of the source subsystem should be used to form a gain limit, and all possible values of output impedance phase should be used, at each frequency, to form a forbidden phase band. However, there are several possible methods of forming a load input impedance specification while still meeting these two criteria. In this section three methods of properly forming the load impedance specification for the Space Station Power System will be introduced. The three methods all guarantee sufficient gain margin and phase margin for loop gain, T_m, in the presence of impedance overlap. A comparison of the three methods and the advantages and drawbacks of each will be discussed in Section 3.8.

The first possibility for the formation of the load impedance specification is to use the combined DCM and CCM Monte Carlo analysis and apply the technique developed in Section 3.4 to generate a phase specification for the load impedance which is valid for all operating conditions. This composite specification is shown in Figure 3.11; it guarantees that if the magnitude of the input impedance of the load falls below the gain limit, T_m will have 60° of phase margin and 6 dB of gain margin, as long as the phase of input impedance is checked at all frequencies that its magnitude is below the gain limit.

A second possible method of forming the specification is to add the magnitude specification shown in Figure 3.12. The magnitude specification means that the input

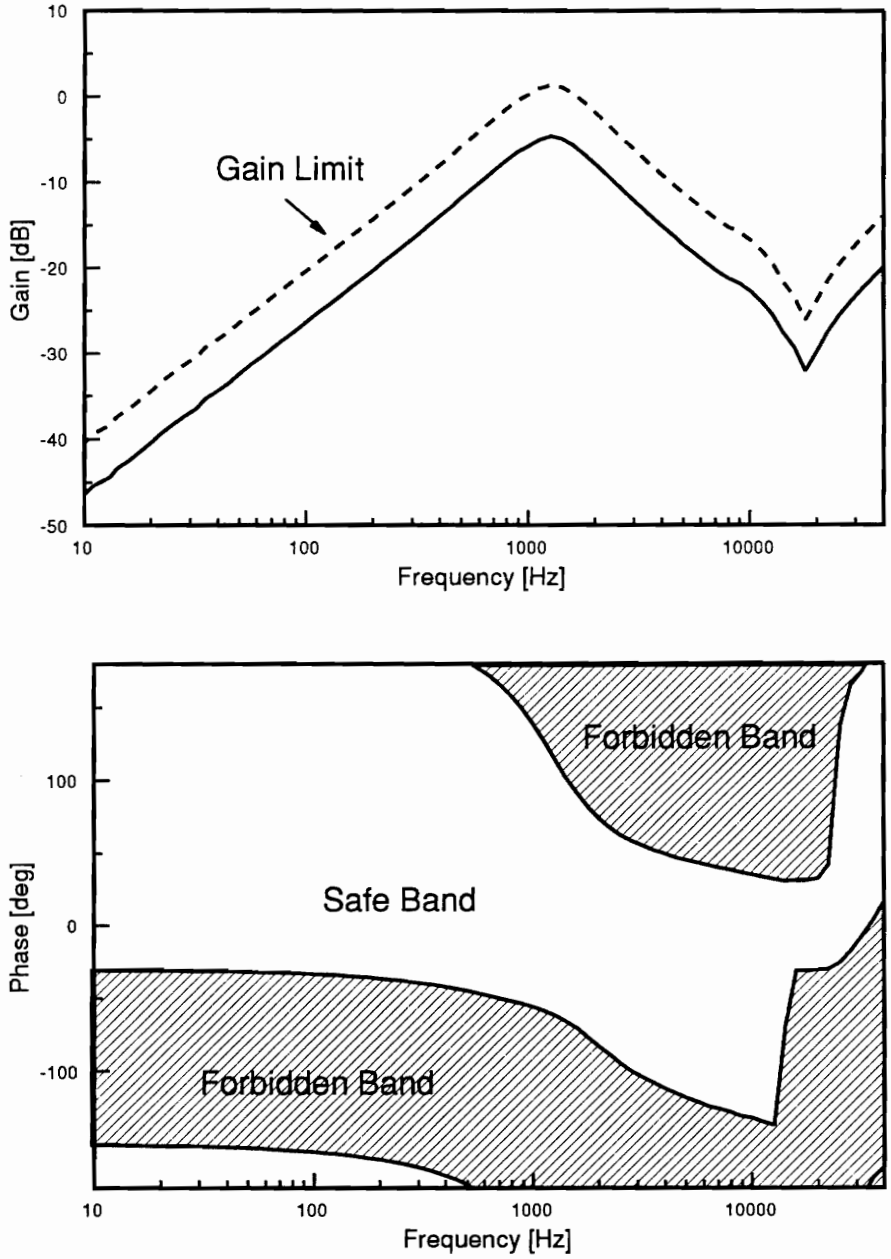


Figure 3.11 Composite specification for load input impedance valid for all operating conditions of line conditioner - CCM and DCM. Meeting the specification ensures 6 dB gain margin and 60 degree phase margin

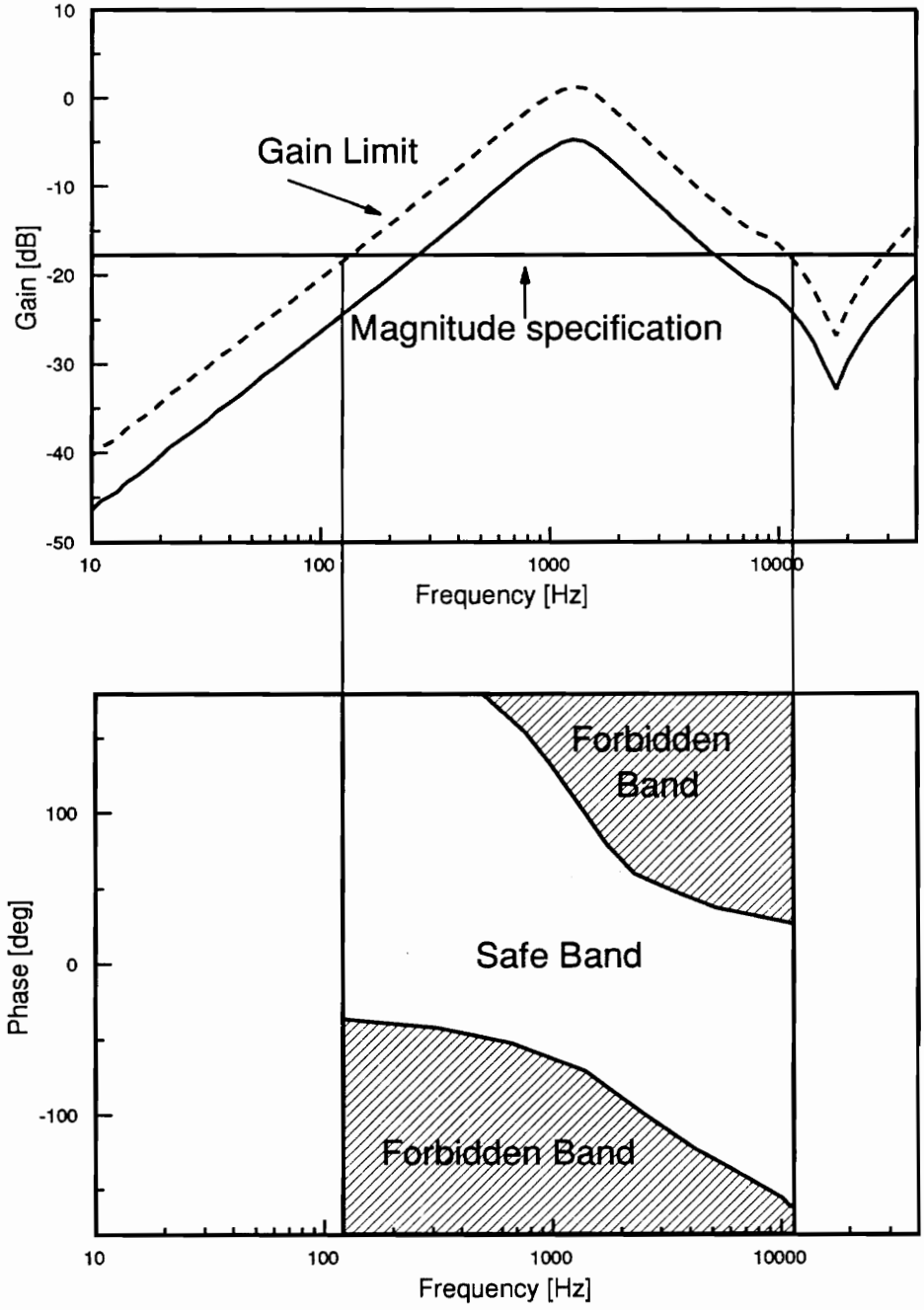


Figure 3.12 Specification for load impedance valid for all operating conditions of line conditioner, includes magnitude specification. Meeting the specification ensures 6 dB gain margin and 60 degree phase margin

impedance magnitude must remain above the specified level; if it falls below the magnitude specification at any frequency, then the load does not meet the input impedance specification. Such a specification limits the degree of overlap allowed and limits the frequency range of possible interaction. Further discussion about the addition of a magnitude specification will be presented in Section 3.9. For this case, the magnitude specification does not allow any overlap in the CCM mode of operation, so only the DCM Monte Carlo analysis needs to be considered when forming the phase specification. This level was chosen for the magnitude specification based upon the line conditioner output impedance characteristics of Figure 3.7. Since at each frequency, the entire band of possible values of output impedance phase must be considered, Figure 3.7 was used to determine which operating conditions had output impedance phases similar to one another and which operating conditions had phases different from one another. It can be seen that the DCM operating conditions have very different phase and magnitude characteristics than the CCM operating conditions at each frequency. Therefore, the most logical location for the magnitude specification is between the CCM and DCM operating conditions as shown in Figure 3.12. As in the case of the first method presented, this specification guarantees 6 dB of gain margin and 60° of phase margin for any load, provided that whenever the input impedance magnitude falls below the gain limit, it meets the phase specification.

A third possible method of forming the load impedance specification is to form separate specifications for the DCM and CCM modes of operation. The CCM specification is shown in Figure 3.13, and the DCM specification is shown in Figure 3.14. Any time the line conditioner is operating in CCM, the load subsystem needs to be checked against Figure 3.13; if the magnitude of the input impedance of the load subsystem falls below the CCM gain limit, its phase must be checked against the phase specification of Figure

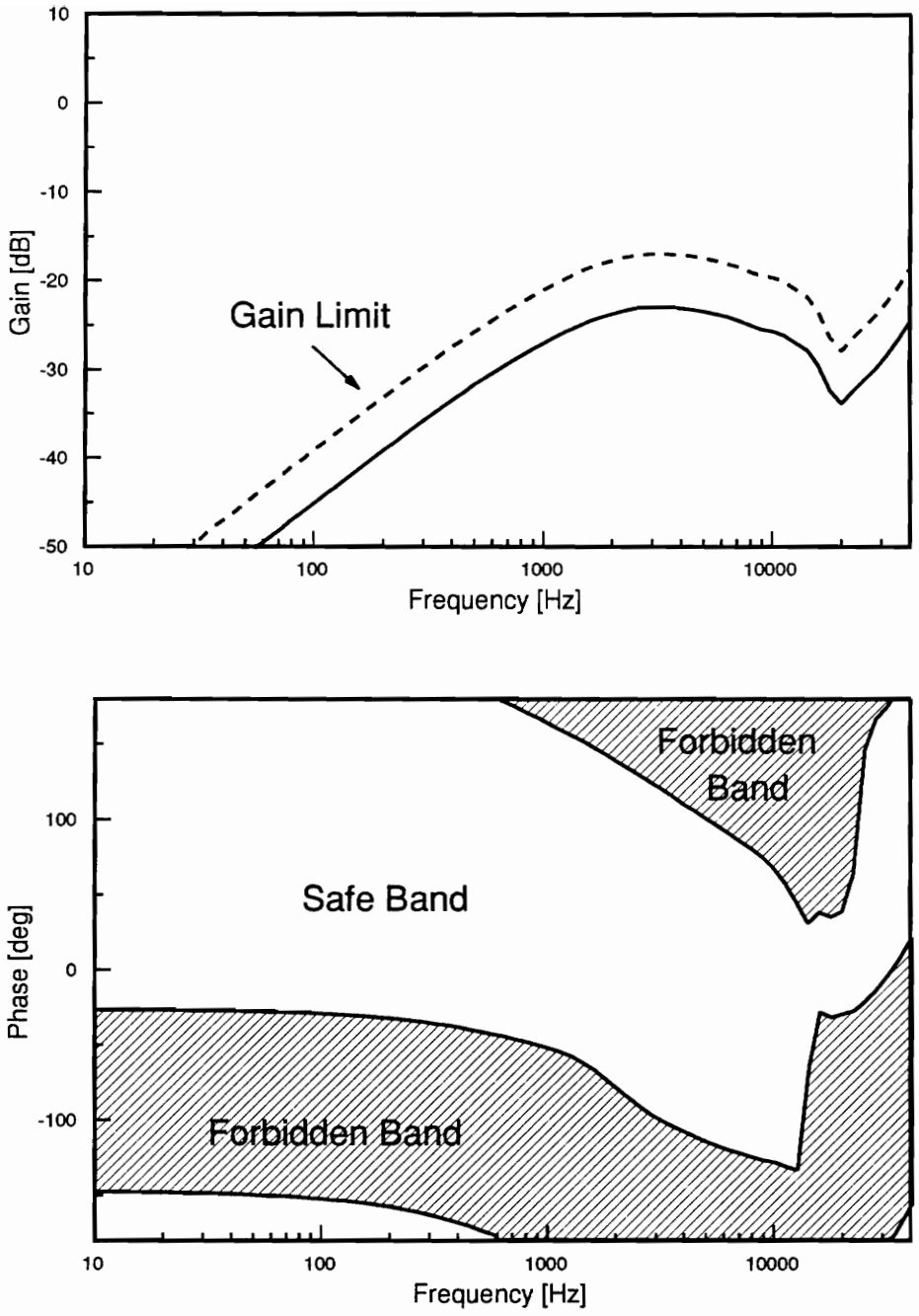


Figure 3.13 Specification for load input impedance valid when line conditioner operates in CCM mode of operation. Meeting the specification ensures 6 dB gain margin and 60 degree phase margin

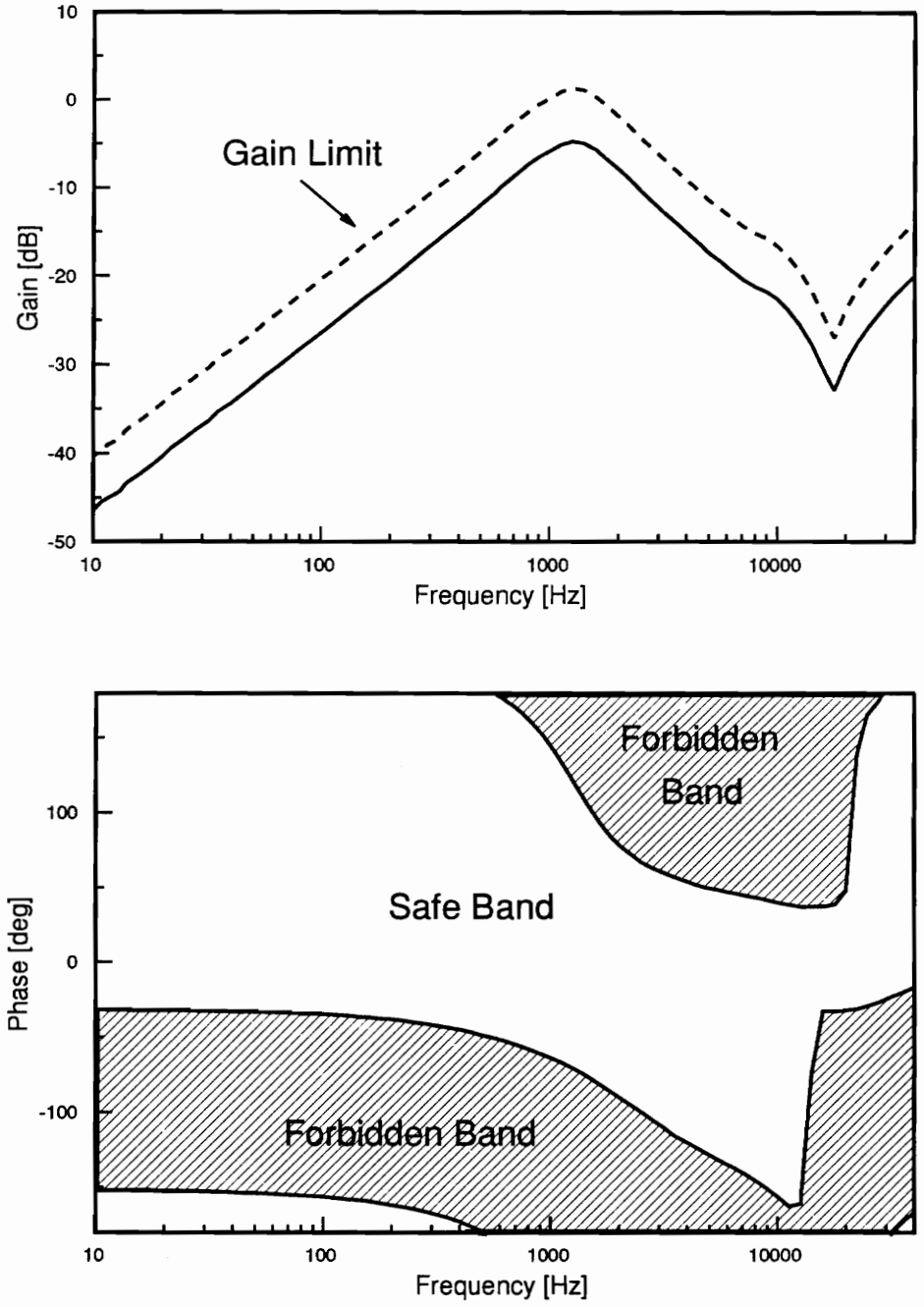


Figure 3.14 Specification for load input impedance valid when line conditioner operates in DCM mode of operation. Meeting the specification ensures 6 dB gain margin and 60 degree phase margin

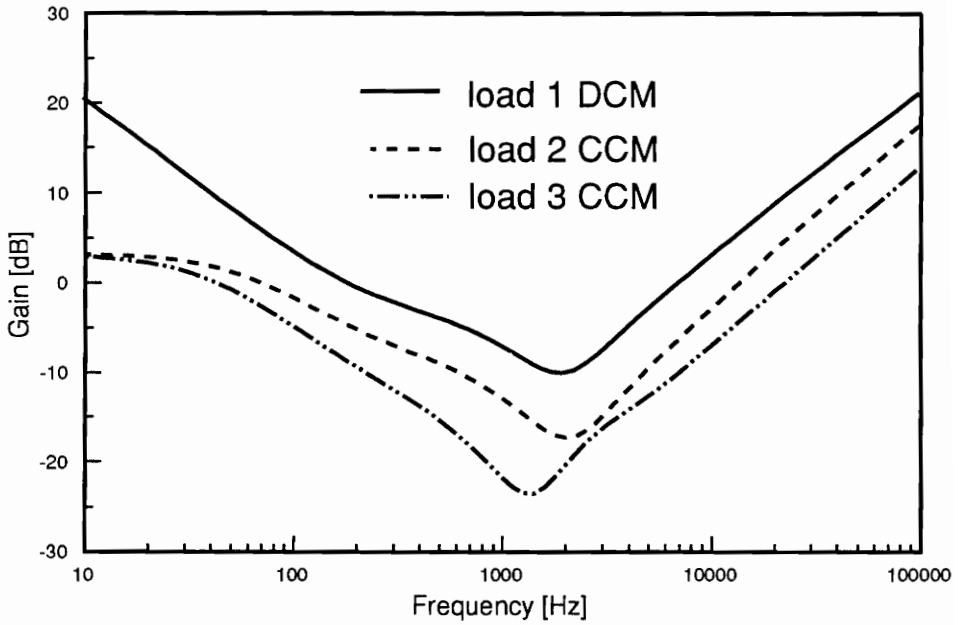
3.13. On the other hand, if the line conditioner is operating in DCM, then the load subsystem needs to have its input impedance checked against the gain limit and phase specification of Figure 3.14. If these specifications are always met, then loop gain, T_m, always has 6 dB of gain margin and 60° of phase margin.

3.8 Comparison Between Possible Methods of Specification Formation

A comparison between the three possible methods to form the load impedance specification is now presented. It is easiest to depict the differences between these specifications through the use of example load subsystems. The input impedance of the example load subsystems to be used to demonstrate the difference between the three possible methods for forming the load impedance specification are shown in Figure 3.15. Load 1 has a low power level for which the DDCU line conditioner is operating in DCM. Loads 2 and 3 have higher output power levels, which cause the DDCU line conditioner to operate in CCM.

The first specification to be considered is method two, which utilizes both a magnitude and phase specification. For this system, this method is the most restrictive of the three. As shown in Figure 3.16, loads 2 and 3 have input impedances which do not meet the magnitude specification and are not allowable. Also, for this system, the use of a magnitude specification does not make the phase specification significantly easier to meet than either of the other two methods presented. The advantages of this specification are that the frequency range over which phase must be checked is decreased, and low-frequency impedance overlap is not allowed.

Now methods one and three which do not utilize a magnitude specification are compared. Figure 3.17 shows the input impedance of the three example loads compared to the single composite input impedance specification which considers the output



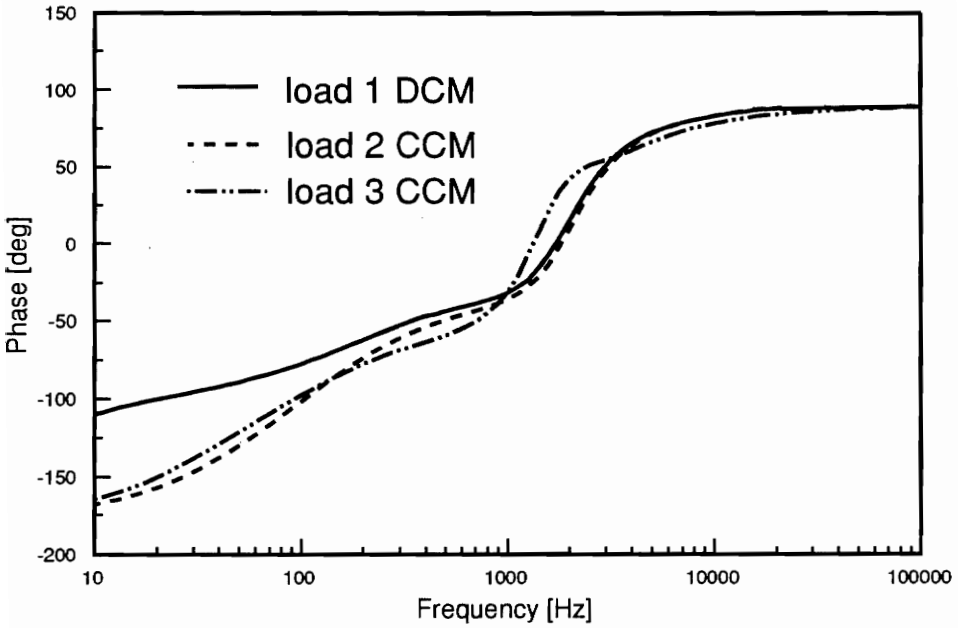


Figure 3.15 Three example load input impedances

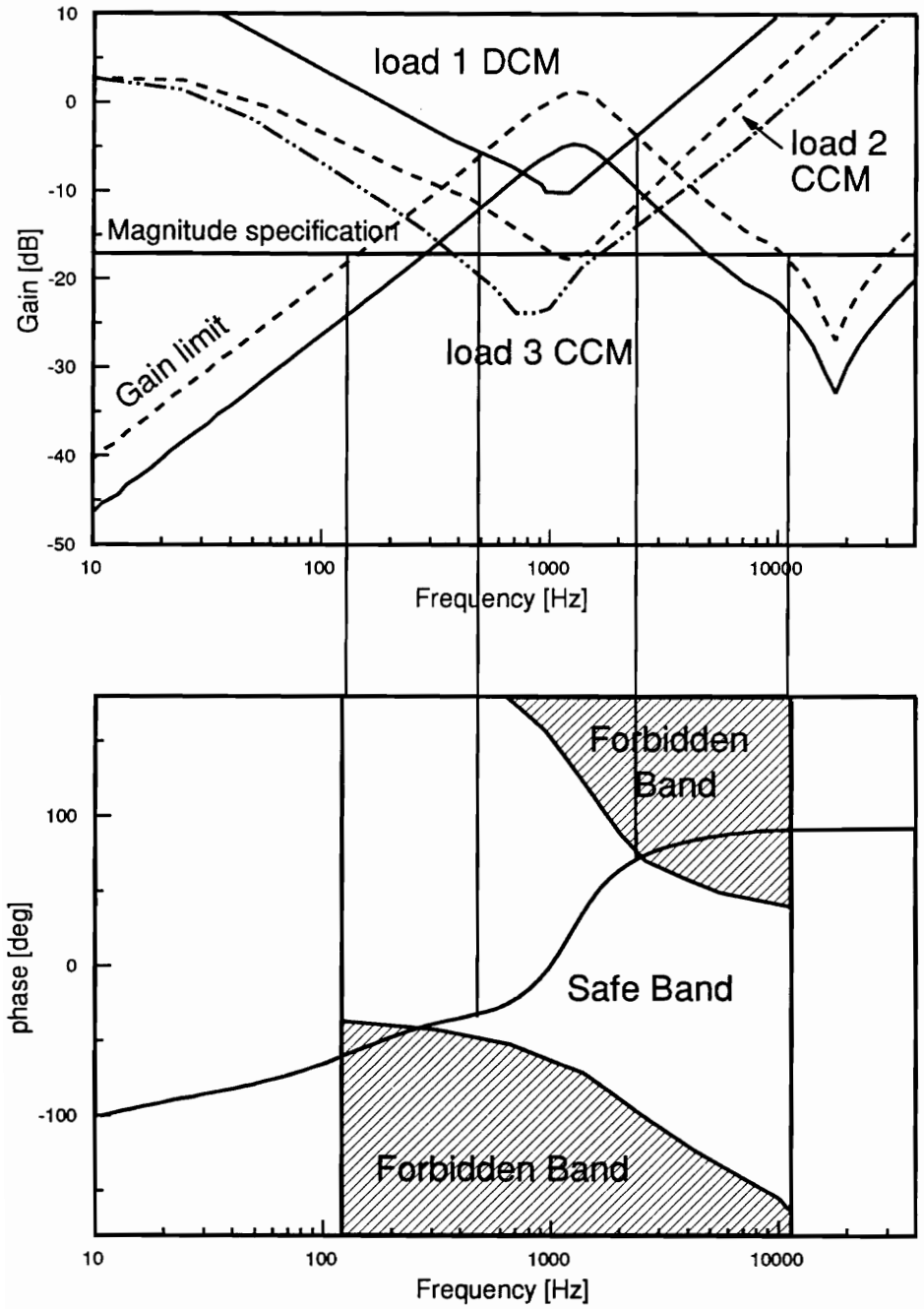


Figure 3.16 Three example loads checked against load impedance specification with magnitude specification

load 1 meets the specification and is acceptable
loads 2 and 3 have magnitude that does not meet the magnitude specification and are therefore not allowed

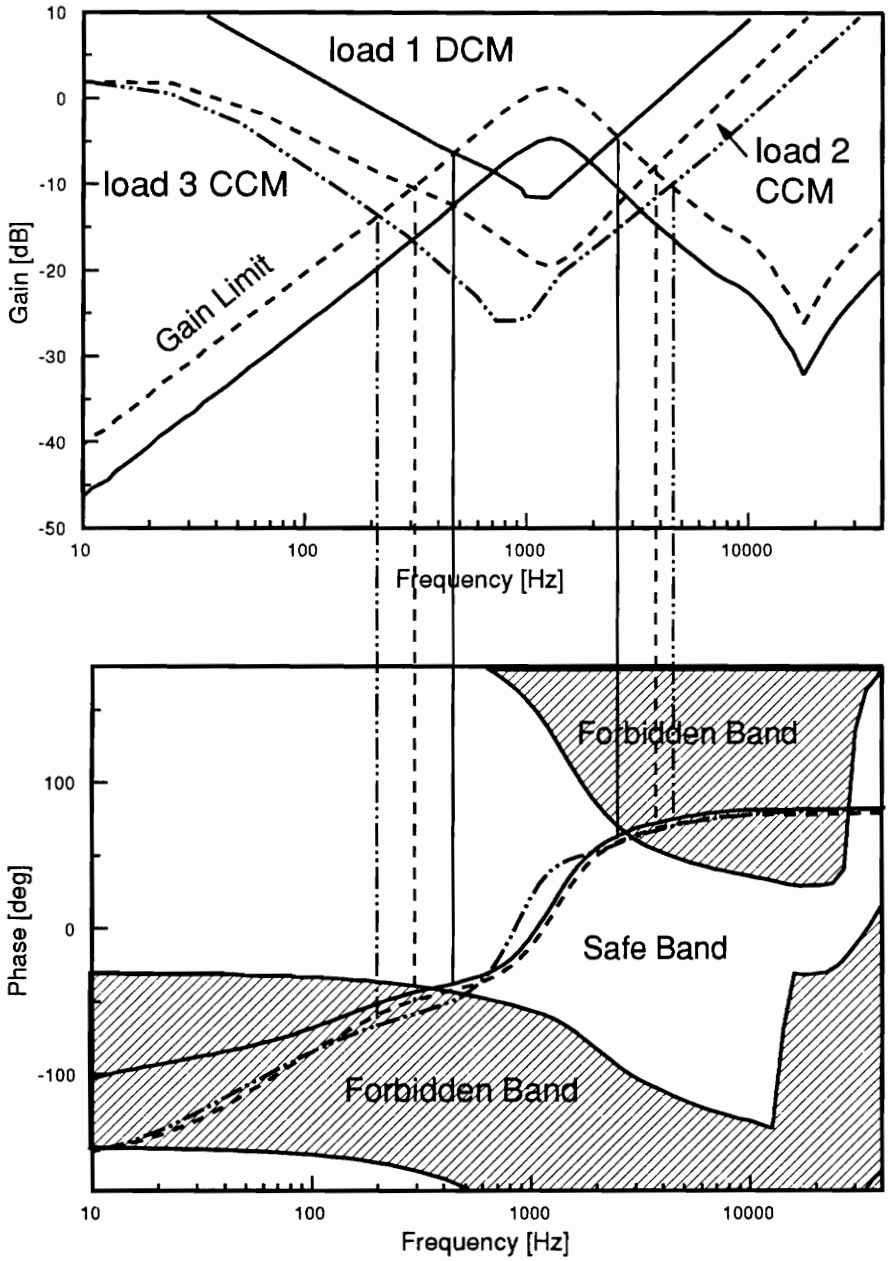


Figure 3.17 Three example loads checked against composite specification valid for all operating modes

load 1 meets the specification and is acceptable
loads 2 and 3 do not meet the phase specification and are therefore not allowed

impedance of all operating conditions. Figure 3.18 shows the input impedance of the three loads compared to the specification which utilizes separate DCM and CCM specifications. It can be seen that the composite specification, which covers all operating conditions, is more restrictive than separate CCM and DCM specifications. In the composite specification, the phase of all three loads must be checked against a phase band which is narrower than that of the separate specifications, for a wider frequency range. In the case of the separate specifications, load 2 does not have to be checked at all, since its magnitude does not fall below the CCM gain limit; loads 1 and 3 need to have their phase checked over a narrower frequency range, against a less restrictive phase specification than if the composite specification is used. The chart below summarizes the results:

Method 1 - Composite specification valid for all operating conditions

Method 2 - Composite specification with magnitude specification

Method 3 - Separate CCM and DCM specifications

	Method 1	Method 2	Method 3
Load 1	Acceptable	Acceptable	Acceptable
Load 2	Unacceptable	Unacceptable	Acceptable
Load 3	Unacceptable	Unacceptable	Acceptable

From this chart, it can be seen that the least restrictive input impedance specification for the Space Power System is the one which uses separate DCM and CCM specifications.

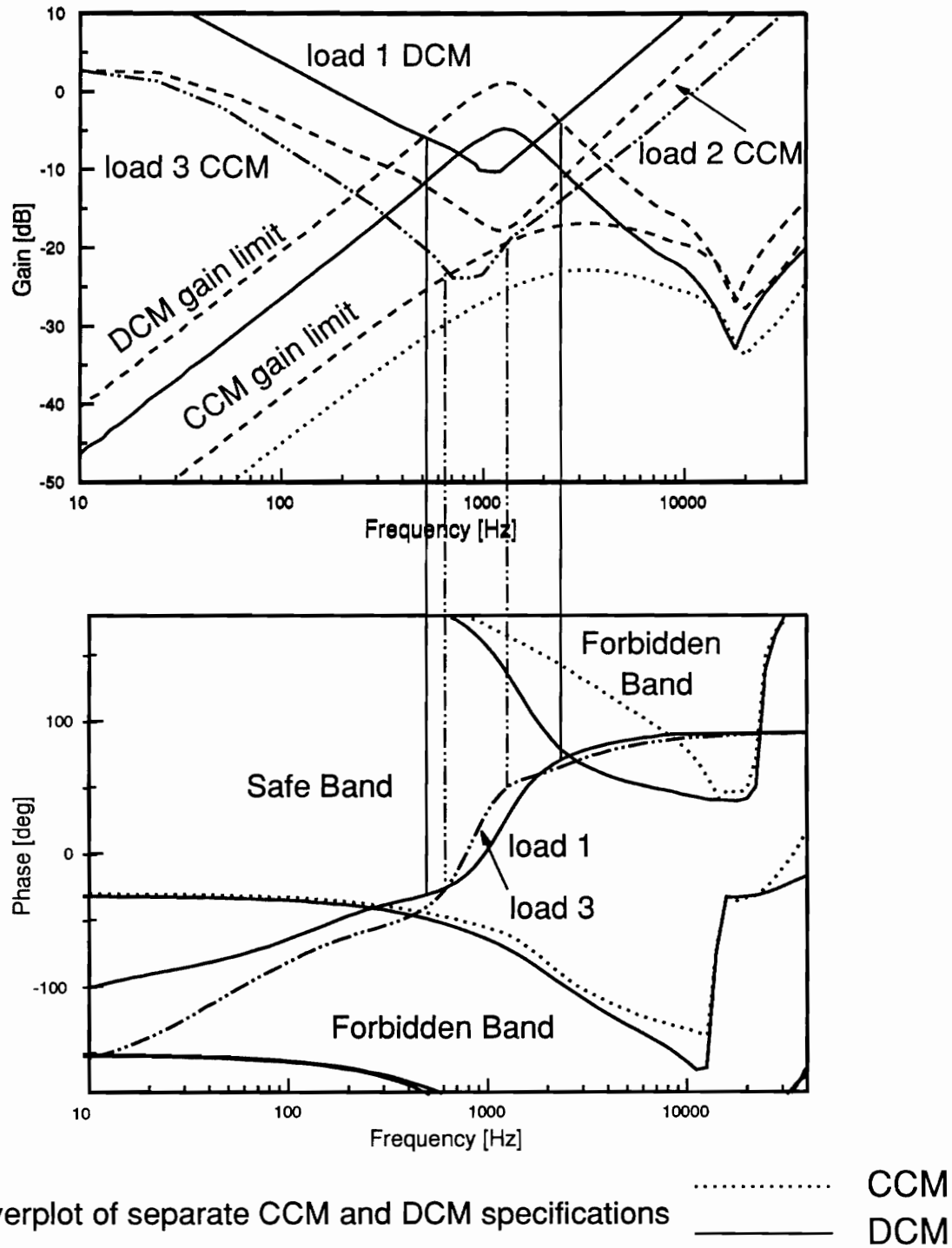


Figure 3.18 Three example loads checked against separate DCM and CCM specifications

loads 1,2 and 3 all meet the specification and are acceptable

3.9 Discussion of Magnitude Specification

A magnitude specification for the load input impedance is not necessary to ensure stability. In the previous section, it was seen that adding a magnitude specification to the Space Power System was not helpful in making the load impedance specification easier to meet. However, in certain cases the use of a magnitude specification may make the phase specification easier to meet. An example system where the magnitude specification makes the load impedance specification less restrictive is shown in Figure 3.19. The figure shows several possible output impedance curves, which are assumed to be the output impedance of a single hypothetical line conditioner at five different operating conditions. The phase specification on the figure is for the case where there is no magnitude specification, and it can be seen that the acceptable band for phase is very narrow. On the figure it can be seen that there is a large variation in the output impedance phase at each frequency. As discussed in Section 3.5 it is known that at each frequency the phase of every operating condition for which impedance overlap is possible must be considered when generating the phase specification for the input impedance of the load. Therefore, if there are many different values of output impedance phase at each frequency (as in Figure 3.19), the phase specification will become very restrictive, and it will be difficult for any load to meet it. A magnitude specification can be used to limit the number of operating conditions for which impedance overlap is possible, and therefore make the phase specification less restrictive. In Figure 3.20, using the same output impedance curves, the phase specification is reformed with the addition of a magnitude specification. This magnitude specification decreases the frequency range in which overlap is possible, and it prevents impedance overlap with the output impedance of three of the five operating conditions. It can be seen that this causes the phase specification to become much less restrictive. The forbidden band for phase is narrower and the magnitude

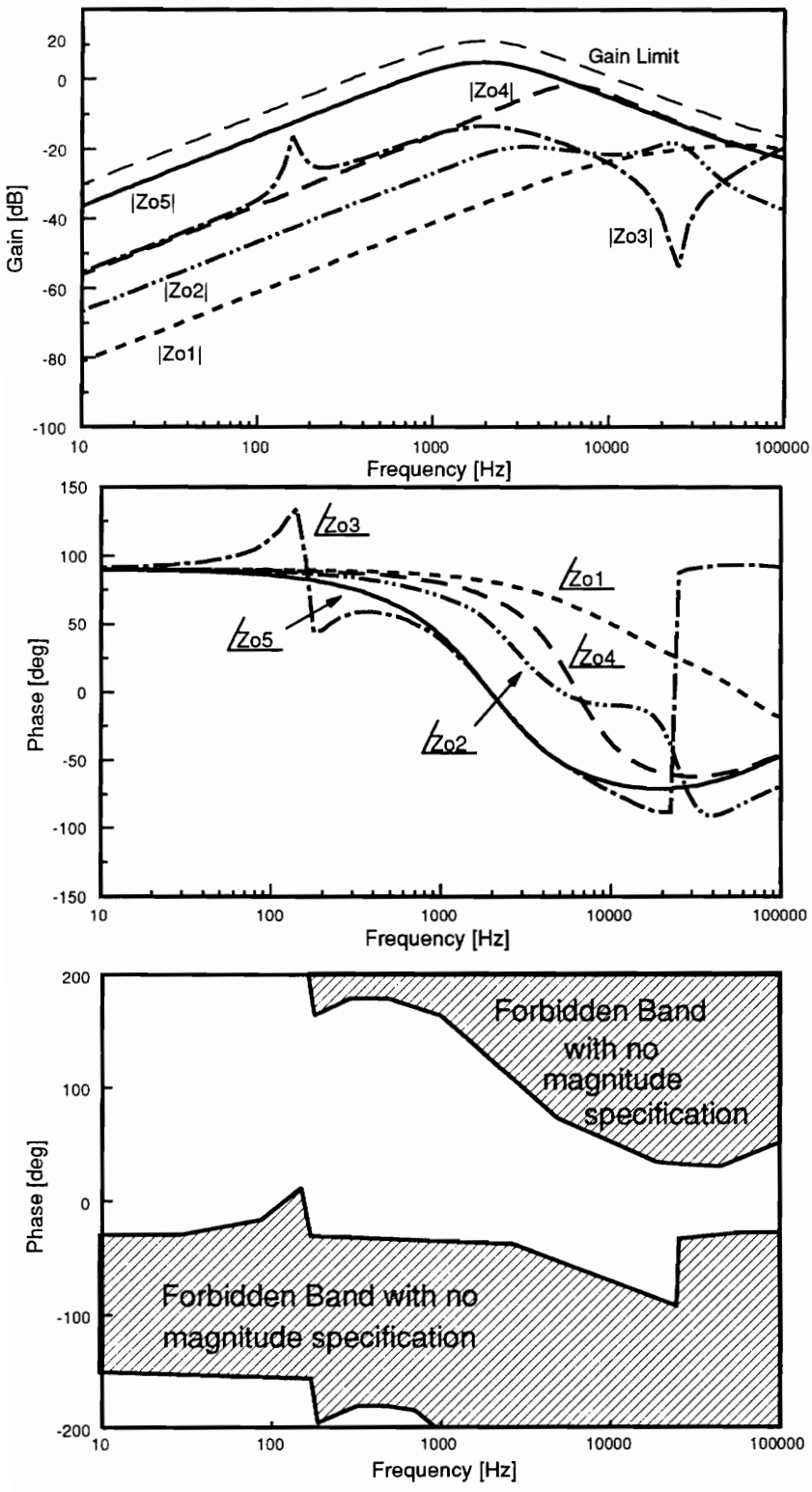


Figure 3.19 Input impedance specification without magnitude specification

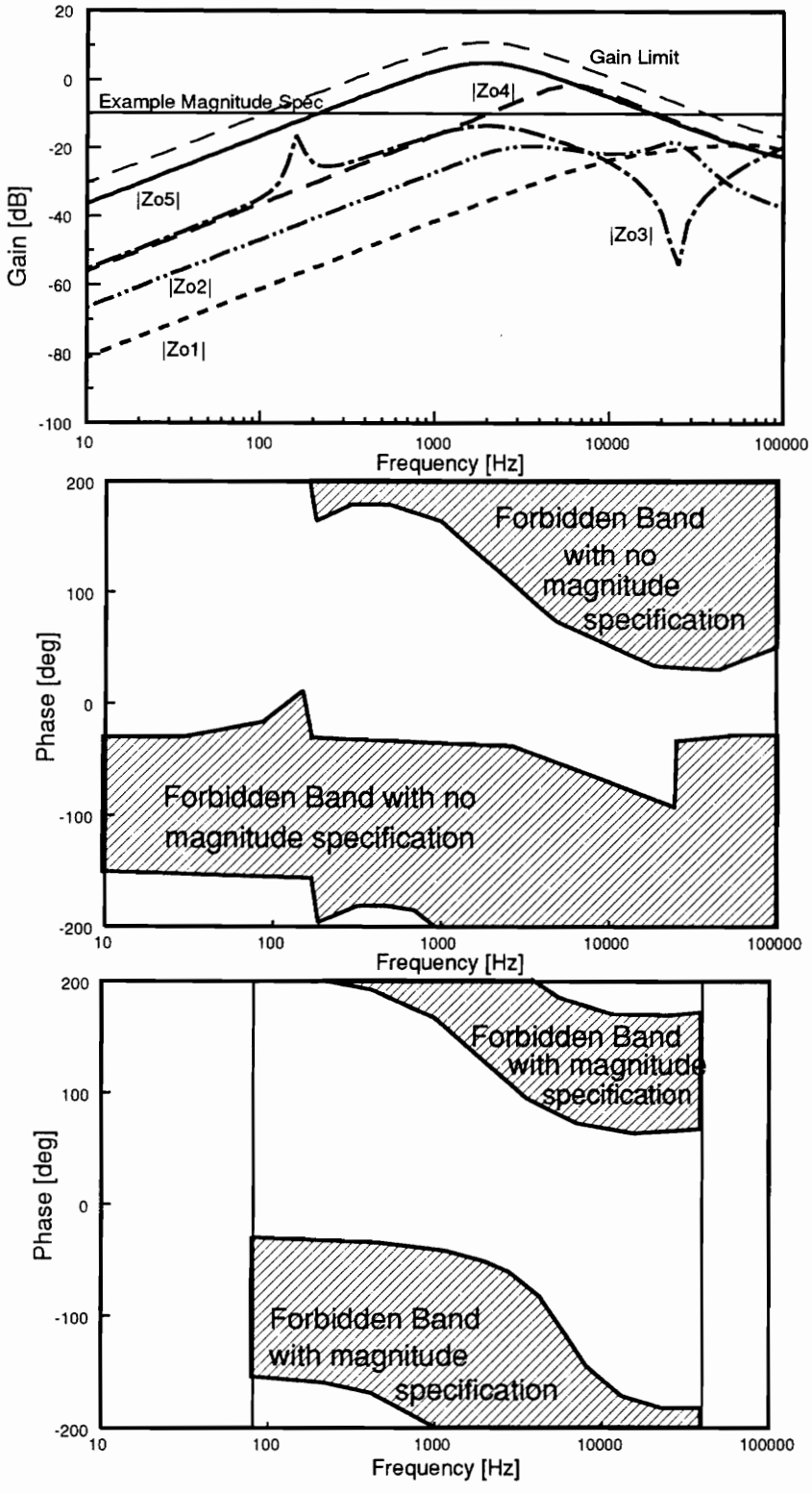


Figure 3.20 Effect of adding magnitude specification on the phase specification

specification prevents interaction from occurring at low frequencies, which has been shown to degrade the system transient response significantly. The conclusion on the magnitude specification is that it simplifies analysis and makes the phase specification more bearable in the case of widely varying output impedances. In the case where output impedance does not vary much with frequency, a magnitude specification is not needed and will not make the phase specification much easier to meet.

3.10 Parallel Modules

Thus far it has been assumed that the input impedance of the entire load subsystem is known and can be checked against the load impedance specification. Very often in a DPS, many parallel load converters are attached to a single line conditioner. It is not possible to measure the input impedance of the load subsystem as a whole until system integration begins. However, it is desirable that each load converter be tested individually before integrating the load subsystem, so that potential problems can be identified early in the design process and changes made.

3.10.1 Phase of Parallel Modules

The first observation which can be made about the input impedance of parallel load converters is that if the phase of the input impedance of the individual modules is between $-90°$ and $90°$, then the phase of the input impedance of the parallel converters is bounded by that of the individual modules. A proof of this is presented, in conjunction with Figure 3.21, which considers the case of two parallel impedances.

Figure 3.21a shows the system being considered. Suppose $-90° \le \Phi_1 \le \Phi_2 \le 90°$, then:

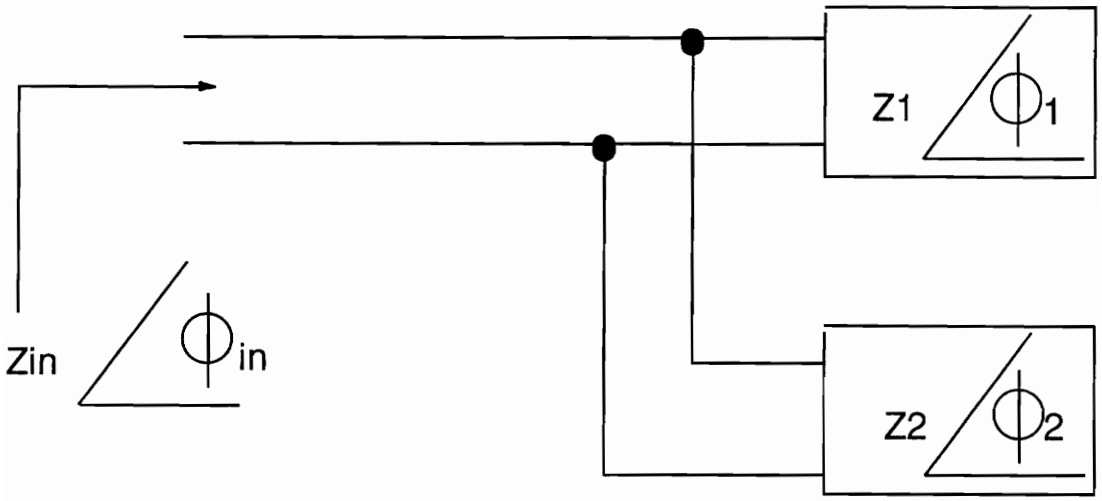


Figure 3.21a Two parallel impedances

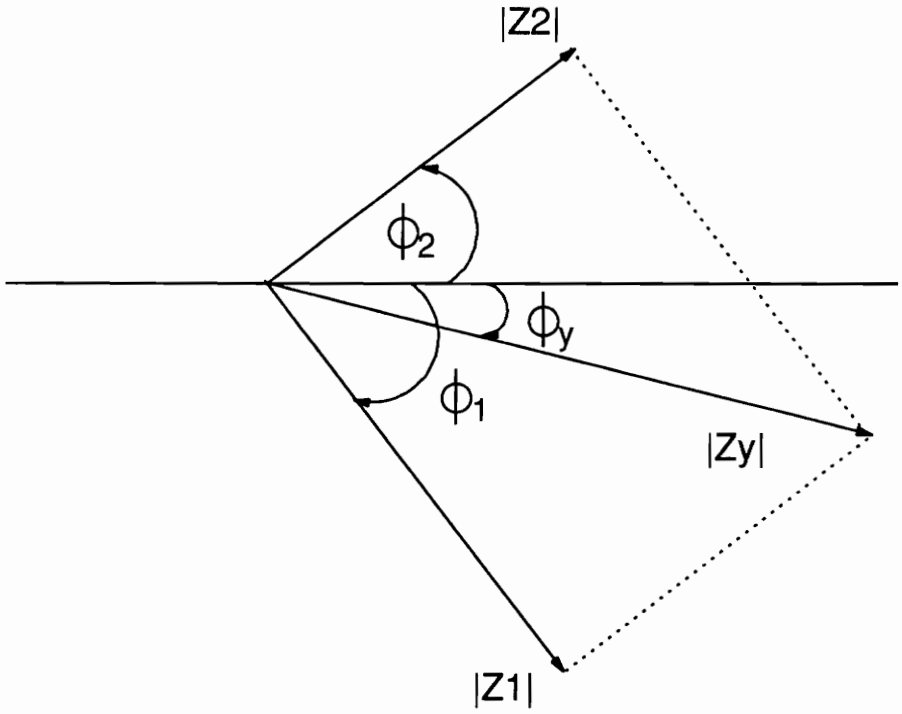


Figure 3.21b Vector addition of Z1 and Z2

$$\overrightarrow{Zin} = \frac{\overrightarrow{Z1} \times \overrightarrow{Z2}}{\overrightarrow{Z1} + \overrightarrow{Z2}} \quad .$$

Let $\overrightarrow{Zy} = \overrightarrow{Z1} + \overrightarrow{Z2}$, which implies:

$$Zin \angle \Phi_{in} = \frac{Z1\,Z2 \angle \Phi_1 + \Phi_2}{Zy \angle \Phi_y}$$

for the phase to be bounded, $\Phi_1 \le \Phi_{in} \le \Phi_2$, which means that:

$$\Phi_1 \le \Phi_1 + \Phi_2 - \Phi_y \le \Phi_2 \text{ , or}$$

$$\Phi_1 \le \Phi_y \quad \text{and} \quad \Phi_y \le \Phi_2$$

but by vector algebra, as shown in Figure 3.21b

$$\Phi_1 \le \Phi_y \le \Phi_2 \text{ , so}$$

$$\Phi_1 \le \Phi_{in} \le \Phi_2.$$

Although the phase of a load converter generally varies from −180° and 90°, the assumption that the phase of the individual modules is between −90° and 90° is a valid assumption for many practical DPS loads in the frequency range for which impedance overlap is likely to occur. An example showing parallel converters with different phases is shown in Figure 3.22. It can be seen that the phase of the parallel combination is always bounded by that of the two individual impedances.

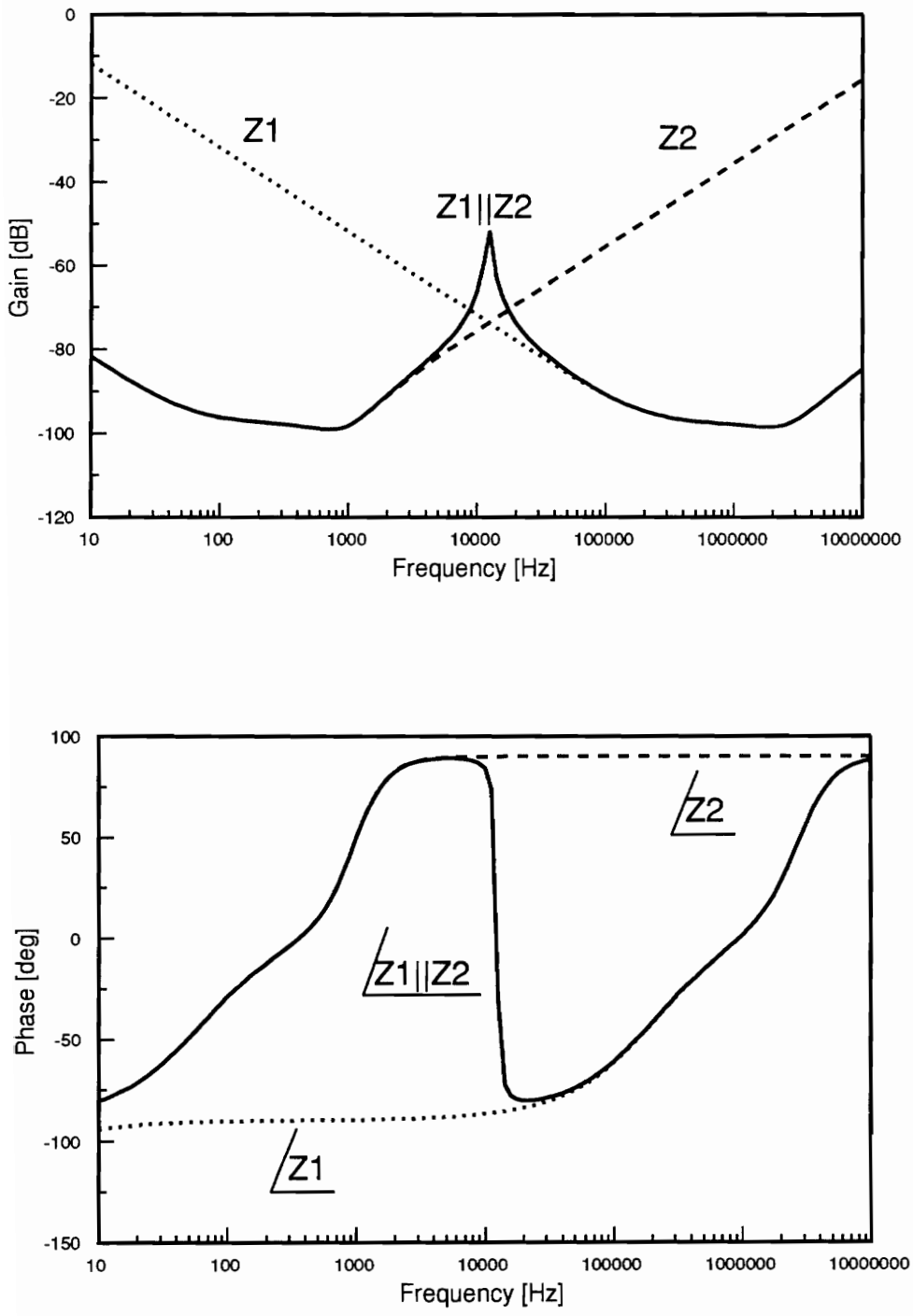


Figure 3.22 Example showing impedances in parallel have bounded phase but not bounded magnitude

3.10.2 Magnitude of Parallel Modules

For the purposes of meeting the impedance specification presented, the worst-case magnitude of input impedance is that with the smallest value of magnitude, since it will stay below the gain limit and need its phase checked over the widest frequency range. Based upon the equations in the previous section, it can be seen that the worst-case (minimum) magnitude of parallel modules is when the modules are identical. In such a case the magnitude of the parallel combination is half that of each individual module.

Upward peaking of the impedance is possible when paralleling impedances. This is true because the impedance $\overrightarrow{zy}$ can go to zero if $\overrightarrow{z1}$ and $\overrightarrow{z2}$ are out of phase and cancel one another. Figure 3.22 shows upward peaking caused by paralleling modules; this does not create any problem as far as meeting a load impedance specification, as long as the individual modules can meet the specification. This is because after paralleling the modules, magnitude is increased, and the phase remains between that of the individual modules.

3.10.3 Conclusions on Parallel Modules

The worst-case for parallel modules is when they are identical. The phase remains the same while the magnitude is decreased by the maximum amount possible. Therefore, individual load modules can be tested against the load input impedance specification in the following manner:

It is assumed that the number of load converters, n, to be attached to the line conditioner is a known quantity. For each load converter that is designed, the magnitude should be shifted down by 20 log (1/n) dB, which is the worst case magnitude when n converters are in parallel. This magnitude should be checked to see at which frequencies it falls below the gain limit, and in these frequency ranges the phase of the input impedance of the converter should be checked to see if it is between −90° and 90° and if

it meets the input impedance phase specification. If all load converters are designed to meet these criteria separately, the load subsystem will meet the specification after integration.

3.11 Summary

In this chapter a forbidden region for the loop gain, T_m, was defined; avoiding the region guarantees that the integrated system is stable, is not conditionally stable, and has minimal performance degradation. A systematic procedure to translate this forbidden region to a phase specification for the load subsystem was introduced, assuming that the source subsystem was well-defined. It was demonstrated that the worst-case system output impedance is not necessarily the operating condition with the worst-case magnitude, and that the output impedance of all operating conditions for which impedance overlap is possible must be considered when forming an input impedance specification for the load subsystem.

Analysis of the Space Power System was performed to demonstrate the ideas presented in the chapter. The concept of the forbidden region was applied to the system, and appropriate methods for defining the phase and magnitude specifications for the load input impedance were discussed. It was found that for the Space Power System, having separate specifications for the CCM and DCM operating modes provided the least restrictive specification for the load to meet. The use of a magnitude specification was examined. It was found that a magnitude specification is not needed to ensure stability, but it can make the phase specification easier to meet in the case of widely varying output impedance phases.

Also, the feasibility of checking individual load converters which are part of the load subsystem was discussed. It was shown that if the input impedance phase remained

between –90° and 90° in the frequency range of overlap, the phase characteristic of the parallel modules can be no worse than that of the individual modules. Based upon this it was shown that by making an adjustment to the magnitude of the input impedance, parallel load converters can be tested individually against the impedance specification.

CHAPTER 4

CONCLUSIONS

This thesis has presented an analysis of the interaction issues present when integrating a DPS. An analysis of the effect of interaction on the source subsystem, load subsystem, and system as a whole has been performed. Methods of forming an input impedance specification for the load subsystem have been introduced, and the feasibility of meeting such a specification has been examined.

Chapter 2 of the thesis showed the possible problems caused by the loading effect in a DPS. It was seen that the impedance ratio, Z_o/Z_{in}, can be viewed as a system loop gain, T_m. From the analysis of this loop gain, it was seen that both stability and performance degradation could be problems in the presence of impedance overlap. The effect of impedance overlap on the system performance was examined, as was the effect of impedance overlap on the source and load subsystems.

Chapter 3 of the thesis presented the concept of a forbidden region for loop gain T_m. It was found that by avoiding the forbidden region on the polar plot, it was possible to avoid significant performance degradation and the possible stability problems caused by impedance overlap. A possible approach for DPS design was outlined, in which an ac unterminated modelling approach was used to design the source subsystem, and then an input impedance specification for the load subsystem was determined using the worst-case output impedance phase.

It was found that formation of the specification was made more complicated because the worst-case output impedance phase does not occur at a single operating condition. A band of output impedance phase which considers all operating conditions needs to be determined in order to properly form the specification. The use of Monte Carlo analysis to find a phase band for the line conditioner output impedance was discussed. Based upon the Monte Carlo analysis, various methods of forming the load input impedance specification were derived and compared.

The use of a magnitude specification to simplify analysis by decreasing the number of operating conditions for which impedance overlap is allowed was discussed. It was found that such a specification is useful when output impedance phase varies widely, to make the phase specification less restrictive. Finally, the use of parallel load converters was examined. It was found that in certain cases individual load converters can be tested against the load impedance specification separately, before system integration, to verify that the system will meet the specification after integration.

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VITA

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