Efficiency Improvement of WCDMA Base Station Transmitters using Class-F power amplifiers

Muthuswamy Venkataramani

Thesis submitted to the faculty of the Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Master of Science
In
Electrical Engineering

Dr. Charles W. Bostian, Chair
Dr. Dennis G. Sweeney
Dr. Sanjay Raman

February 13, 2004
Blacksburg, Virginia

Keywords: WCDMA, power amplifier, class-F, class-AB, linearity, harmonic balance,
Intermodulation distortion, power added efficiency

Efficiency Improvement of WCDMA Base Station Transmitters using Class-F power amplifiers

Muthuswamy Venkataramani

(ABSTRACT)

Universal Mobile Telecommunications Systems (UMTS) is the preferred third generation (3G) communication standard for mobile communications and will provide worldwide coverage, a convenient software technology and very high data rate. The high data rate, especially, requires the use of bandwidth-efficient modulation schemes such as Quadrature Phase Shift Keying (QPSK). But modulation schemes such as QPSK need, in turn, a very linear power from the output of the transmitter power amplifier in order to meet the spectral requirements. A linear power amplifier, traditionally, has very low energy efficiency. Poor energy efficiency directly affects operational costs and causes thermal heating issues in base station transmitters. Thus the power amplifier designer is forced to trade-off between linearity and efficiency. As a result of this trade-off a Class-AB power amplifier is most often used in QPSK based systems. Class-AB power amplifiers provide acceptable linearity at efficiency values around 45-50% typically. This compromise is not a satisfactory solution but is inevitable while using traditional power amplifier design techniques.

This thesis details the use of a Class-F amplifier with carefully chosen bias points and harmonic traps to overcome this problem. Class-F amplifiers are usually considered as very high efficiency (80% or more power-added efficiency) amplifiers where the high efficiency is obtained through the use of harmonic traps (L-C filters or quarter-wavelength transmission lines), which provide suitable terminations (either open or short) for the harmonics generated. By doing this, a square wave drain voltage and a peaked half-sinusoidal drain current out-of-phase by 180º are produced. Since only a drain

voltage or a drain current exists at any given time, the power dissipation is ideally zero resulting in 100% theoretical efficiency. These very high efficiency values are usually associated with poor linearity. However the linearity can be improved to meet the design standards but compromising on efficiency. Even after this is done, efficiencies are usually 10 to 15% greater than a traditional Class AB power amplifier with similar linearity performance. Thus efficiency can be improved without affecting linearity by the use of Class-F power amplifiers.

In order to verify this theory, a Class-AB and a Class-F power amplifier are designed using Motorola's high voltage laterally diffused metal oxide semiconductor (LDMOS) transistor. The choice of bias points and the design of the harmonic traps are very critical for the Class-F performance and hence were designed after careful consideration. The designs were simulated on Agilent's Advanced Design System (ADS) and the simulated results were compared for three different power levels namely, the peak power, 3 dB below peak power and 6 dB below peak power. At all of these power levels it was noted that the Class-F and Class-AB power amplifiers have very similar linearity performance whereas the Class-F power amplifiers show about 10% improvement in efficiency in comparison to the Class-AB power amplifiers.

To my advisor

Dr. Charles Bostian

To my family

Gulo, Venkataramani, Sandhya, Shiva,
Sudhanva and Sudheep

Acknowledgment

Working on this thesis was a very useful, important and memorable experience to me. I would like to thank all those people who made this thesis possible.

First of all, I would like to thank Dr. Charles Bostian, my advisor at the Center for Wireless Telecommunications, Virginia Tech. The knowledge that I gained from his lectures and during personal discussions was invaluable. In addition to his roles as my thesis advisor and professor for radio engineering courses, he has been a very good friend, a father figure, who always had encouraging words for me. I also thank him for giving me various teaching assistantship positions that helped me fund my graduate studies and also served as a very useful experience.

I am grateful to my thesis committee members, Dr. Sanjay Raman and Dr. Dennis Sweeney, for their insightful suggestions towards my thesis. I also thank them for their time spent reviewing my thesis.

I would like to thank Motorola for providing design kits and technical support. I would especially like to thank Bob Keasler, David Shih and Cedric Cassan of Motorola for their support and suggestions.

I would like to thank the staff of CWT, especially, Shelley Johnson, Judy Hood, Kathy McCloud and James Dunson for their help and support.

Friends are a very important part of graduate life and I would like to thank my friends who have been with me through this. I would always relish the time spent with them.

Finally I would like to thank my parents, my sister and brother-in-law for their constant support, love and prayers. I thank them for helping me pursue my academic goals.

Table of Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Background

Universal Mobile Telecommunications Systems (UMTS) is the preferred third generation (3G) communication standard for mobile communications offering potential worldwide coverage and a convenient technology for software and applications developers [1], [2]. The radio technology proposed in UMTS is Wideband CDMA (WCDMA) and the planned frequency range of operation for UMTS is close to 2GHz. WCDMA uses a bandwidth that is four times wider (5 MHz bandwidth) than the conventional CDMA systems that are typically used in second generation networks in North America.

UMTS utilizes a bandwidth-efficient modulation, namely the Quadrature Phase Shift Keying (QPSK) modulation, and therefore is capable of providing higher bit rates per unit of bandwidth. Typically UMTS systems are expected to deliver peak data rates of up to 2.4 Mbps with average data rates of 300 kbps when the user is walking or driving [1]. The data rate increases further when the user is stationary. UMTS is designed to deliver

services which require high bandwidth such as streaming multimedia, large file transfers and video-conferencing.

High data rates, however, demand a linear power amplifier output from the transmitter to conform to transmitted spectrum requirements. A highly linear power amplifier, in turn, has very poor energy efficiency, forcing the power amplifier designer to trade-off between linearity and efficiency.

1.2 Problem

The power amplifiers for existing second generation GSM (Global System for Mobile Communications) transmitters are highly efficient, typically providing efficiencies of 50% or more. However these transmitter designs cannot be applied to UMTS/WCDMA. This is because GSM uses the constant envelope feature of GMSK (Gaussian Minimum Shift Keying) modulation which introduces phase variations only. UMTS on the other hand must maximize spectral efficiency in order to accommodate higher data rate services. A WCDMA system with QPSK modulation is used in UMTS systems to obtain spectral efficiency. In these systems both phase and amplitude variations are introduced by the modulation. The amplitude variation requires a linear output from the transmitter. A conventional linear power amplifier, such as a Class A amplifier, has a very low efficiency (typically 10-35%). This is unacceptable for most applications since efficiency is a major issue directly affecting power consumption, cost, reliability, size of transmitter and talk time. The power amplifiers are thus challenged to amplify complex modulated signals without distortion and at minimum dc power consumption. High linearity and high efficiency thus become contradicting requirements for the power amplifier of a WCMDA system.

1.3 Thesis Outline

A reasonable compromise between linearity and efficiency can be achieved by using a Class AB power amplifier wherein fairly linear amplification can be achieved with an

efficiency of around 45%. However, keeping in mind the advantages of a high efficiency amplifier, many techniques have been proposed to achieve higher efficiencies (50% or more) without additional distortion. In this thesis a Class F power amplifier design is proposed to achieve higher efficiency in comparison to a Class AB power amplifier for a WCDMA based system without compromising linearity. The amplifier will be designed using Motorola's LDMOS transistor model in Agilent's Advanced Design System (ADS) software to operate over the frequency band ranging from 2.11 GHz to 2.17 GHz. Several important parameters such as power added efficiency, dc power consumption, third order intermodulation distortion, AM-PM conversion and third order input intercept point will be examined to assess the efficiency and linearity performance of the power amplifier.

1.4 Thesis Overview

- Chapter 2 discusses the theoretical concepts behind power amplifier design and the various classes of RF power amplifiers.
- Chapter 3 explains the operation of a Class F power amplifier and details the underlying design concepts.
- Chapter 4 describes the actual design of the Class F power amplifier based on simulations using Agilent's ADS. Internal matching of the die model using Motorola's HVIC components is also explained.
- Chapter 5 presents the simulated results and enables a comparative study between the performance of a Class AB and Class F power amplifier.
- Chapter 6 summarizes the thesis by providing conclusions and also suggestions to build on this work.

Chapter 2

RF Power Amplifier Theory

2.1 Introduction

The RF power amplifier (PA), a critical element in transmitter units of communication systems, is expected to provide a suitable output power at a very good gain with high efficiency and linearity. The output power from a PA must be sufficient for reliable transmission. High gain reduces the number of amplifier stages required to deliver the desired output power and hence reduces the size and manufacturing cost. High efficiency improves thermal management, battery lifetime and operational costs. Good linearity is necessary for bandwidth efficient modulation. However these are contrasting requirements and a typical power amplifier design would require a certain level of compromise. There are several types of power amplifiers which differ from each other in terms of linearity, output power or efficiency. This thesis will present a Class F PA design and discuss its performance in comparison to a traditional Class AB amplifier. Parameters which quantify the various aspects of amplifier performance such as 1-dB compression point, input intercept point, intermodulation distortion, power output

capability, power added efficiency and adjacent channel power ratio are discussed in this chapter. In addition the Class AB power amplifier operation is discussed in detail.

2.2 Power Output Capability (C_p)

The power output capability, C_p, is defined as the RF output power produced when the device has a peak drain voltage of 1 volt and a peak drain current of 1 ampere [3]. This is a unit less quantity. If the power amplifier uses two or more transistors, then the number of transistors is included in the denominator.

If P_0 is the RF output power, $I_{d,\,pk}$ is the peak drain current, $V_{d,\,pk}$ is the peak drain voltage and N is the number of transistors, then

$$\mathbf{C_p = \frac{P_0}{N I_{d,pk} V_{d,pk}}} \tag{2.1}$$

Usually the power output capability of a Class A amplifier is the highest since it is operated at the center of the load line allowing room for maximum voltage and current swings. Based on this, another parameter called the power utilization factor (PUF) is defined as the ratio of RF power delivered by a device in a particular mode to the power delivered by operating the device as a Class A amplifier.

2.3 Power Added Efficiency (PAE)

Efficiency or drain efficiency is simply defined as the ratio of output power at the drain to the input power supplied to the drain by the dc supply.

$$\eta_d = \frac{P_0}{P_{dc}} \tag{2.2}$$

Drain efficiency is usually not enough to characterize RF power amplifier performance. This is due to the substantial RF power at the input of the amplifier, especially in amplifiers with low gain. Power added efficiency (PAE) includes the effect of input drive power and is defined as:

$$\mathbf{PAE} = \frac{\mathbf{P_0} - \mathbf{Pdrive}}{\mathbf{P_{dc}}} \tag{2.3}$$

2.4 1-dB compression point ($P_{1\text{-}dB}$)

When a power amplifier is operated in its linear region, the gain is a constant for a given frequency. However when the input signal power is increased, there is a certain point beyond which the gain is seen to decrease. The input 1-dB compression point is defined as the power level for which the input signal is amplified 1 dB less than the linear gain. The 1-dB compression point can be input or output referred and is measured in terms of dBm**.** A rapid decrease in gain will be experienced after the 1-dB compression point is reached. This gain compression is due to the non-linear behavior of the device and hence the 1-dB compression point is a measure of the linear range of operation.

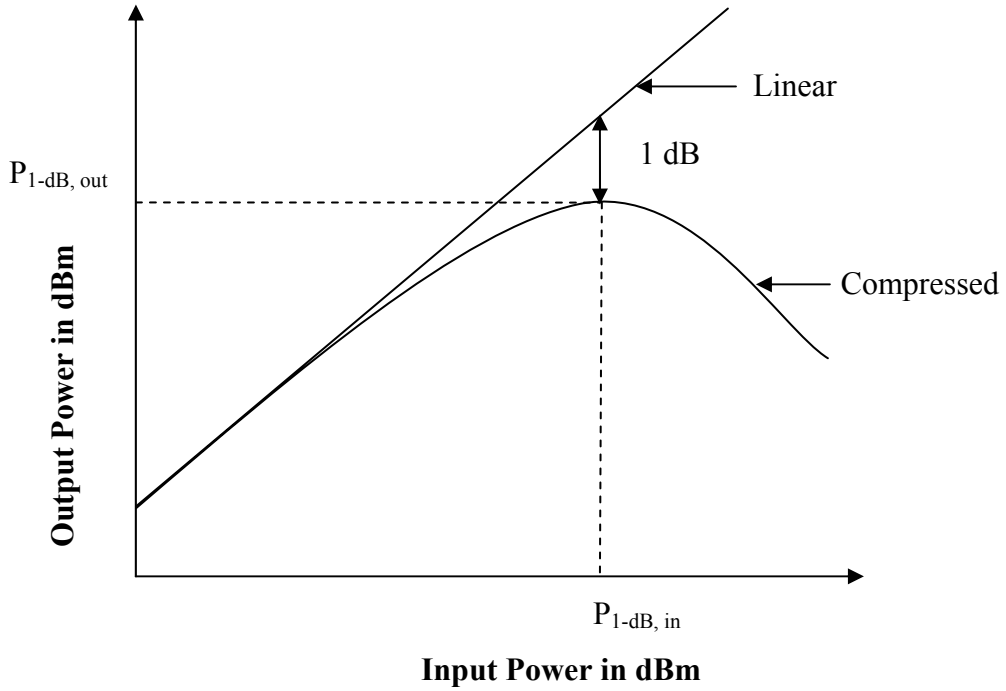

Fig 2.1 **1-dB compression point**

2.5 Intermodulation Distortion (IMD)

Intermodulation distortion is a nonlinear distortion characterized by the appearance, in the output of a device, of frequencies that are linear combinations of the fundamental frequencies and all harmonics present in the input signals [4]. A very common procedure to measure the intermodulation distortion is by means of a two-tone test. In a two-tone test a nonlinear circuit is excited with two closely spaced input sinusoids. This would result in an output spectrum consisting of various intermodulation products in addition to the amplified version of the two fundamental tones and their harmonics. If $\mathbf{f_1}$ and $\mathbf{f_2}$ are the fundamental frequencies then the intermodulation products are seen at frequencies given by

$\mathbf{f_{IMD} = mf_1 \pm nf_2}$

where m and n are integers from 1 to ∞.

The ratio of power in the intermodulation product to the power in one of the fundamental tones is used to quantify intermodulation. Of all the possible intermodulation products usually the third order intermodulation products (at frequencies $\mathbf{2f_1-f_2}$ and $\mathbf{2f_2-f_1}$) are typically the most critical as they have the highest strength. Furthermore they often fall in the receiver pass band making it difficult to filter them out.

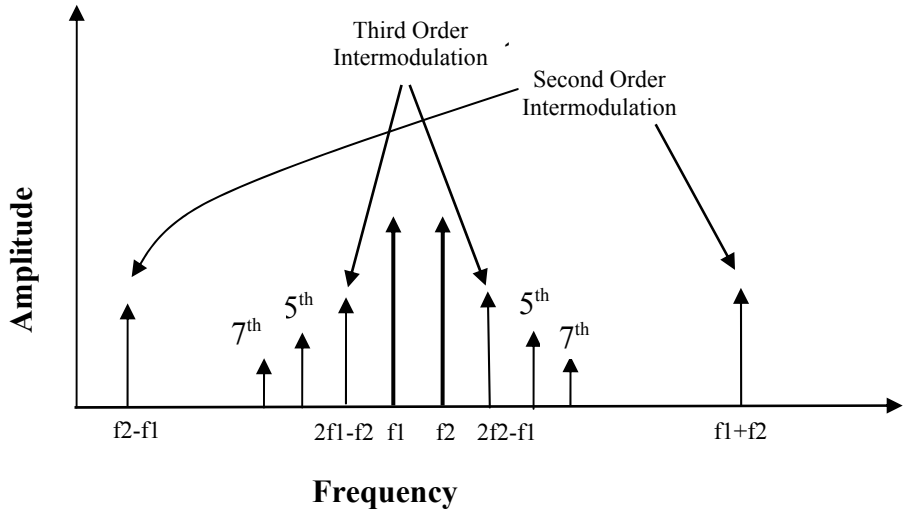

Fig 2.2 **Intermodulation Distortion**

2.6 Adjacent Channel Power Ratio (ACPR)

In many modern communication systems, the RF signal typically has a modulation band that fills a prescribed bandwidth on either side of the carrier frequency. Similarly the intermodulation products also have a bandwidth associated with them. The IM bandwidth is three times the original modulation band limits for third order products, five times the band limits for fifth order products and so on. Thus the frequency band of the intermodulation products from the two tones stretches out, leading to leakage of power in the adjacent channel. This leakage power is referred to as adjacent channel power. The adjacent channel power ratio (ACPR) is the ratio of power in the adjacent channel to the power in the main channel. ACPR values are widely used in the design of power

amplifiers to quantify the effects of intermodulation distortion and hence also serve as a measure of linearity.

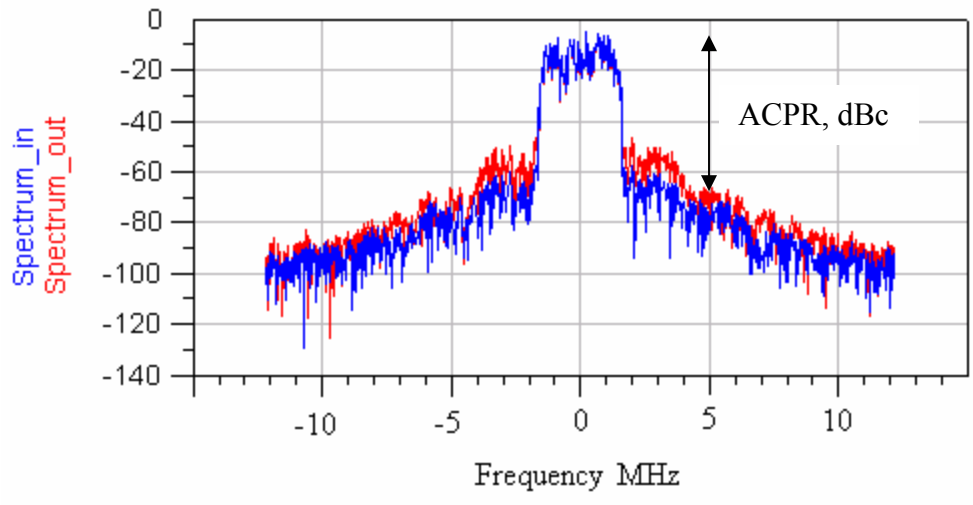

Fig 2.3 **Plot of Adjacent Channel Power**

2.7 Intercept Point (IP)

The intercept point is the point where the slope of the fundamental linear component meets the slope of the intermodulation products on a logarithmic chart of output power versus input power. Intercept point can be input or output referred. Input intercept point represents the input power level for which the fundamental and the intermodulation products have equal amplitude at the output of a nonlinear circuit. In most practical circuits, intermodulation products will never be equal to the fundamental linear term because both amplitudes will compress before reaching this point. In those cases intercept point is measured by a linear extrapolation of the output characteristics for small input amplitudes. Since the third order intermodulation products, among the IM products, are of greatest concern in power amplifier design, the corresponding intercept point called the third order intercept point (IP3) is an important tool to analyze the effects of third order nonlinearities. In fact intercept point serves as a better measure of linearity in

comparison to intermodulation products as it can be specified independent of the input power level [4].

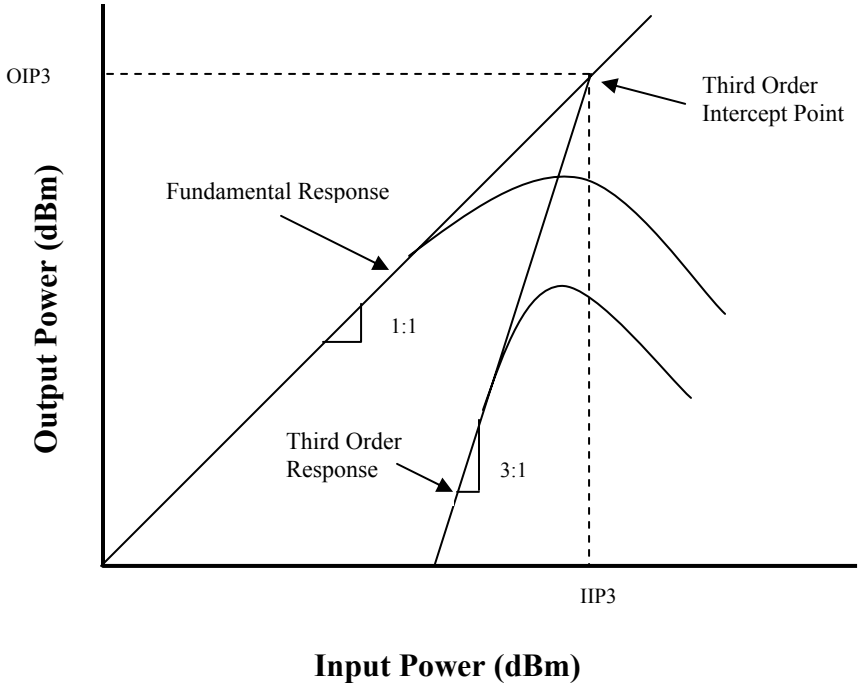

Fig 2.4 **Plot showing Third Order Intercept Point**

2.8 Amplitude Modulation to Phase Modulation (AM-PM) Conversion:

An amplifier driven under strongly nonlinear conditions produces phase distortion in addition to amplitude distortion. The phase distortion is a serious problem in systems with phase modulation such as QPSK. This phase distortion is characterized by AM-PM conversion which is defined as the change in phase of the output signal when the drive level at the input is increased toward and beyond the compression point. The AM-PM effects are usually caused by the storage elements in the circuit like the gate-source junction capacitances and parasitics associated with inductors under nonlinear conditions.

2.9 Power Amplifier Classification

There are several types of power amplifiers and they differ from each other in terms of their linearity, efficiency and power output capability. The first step in designing a power amplifier is to understand the most important design factor and choose the power amplifier type most suited for that purpose. For example, communication systems which require good linearity often use Class A or Class AB architecture whereas those which require good efficiency use a Class C, E or F type power amplifier. In addition there are power amplifier types which satisfy special needs such as a Doherty amplifier which provides high efficiency at backed-off power levels or a Chireix amplifier which gives linear performance using nonlinear components. Class AB power amplifier provides a reasonable trade-off between linearity and efficiency and is the popular power amplifier type for WCDMA applications. In this section the Class AB power amplifier is detailed and other basic power amplifier types are briefly discussed. These discussions based on MOS transistor viewpoint.

2.9.1 Class A:

Class A is the simplest power amplifier type in terms of design and construction. The Class A amplifier has a conduction angle of 2π radians or 360°. Conduction angle refers to the time period for which a device is conducting. Thus a conduction angle of 360º tells us that in Class A operation the device conducts current for the entire input cycle. Class A amplifiers are considered to be the most linear since the transistor is biased in the center of the load line to allow for maximum voltage and current swings without cut-off or saturation. However the problem with Class A amplifiers is their very poor efficiency. This is because the device is draining current at all times which translates to higher power loss. In fact it can be shown that the maximum efficiency achievable from a Class A power amplifier is only 50% [5]. However this is a theoretical number and the actual efficiency is typically much less. In fact commercial Class A amplifiers have efficiency as low as 20%. Hence Class A amplifiers are usually used only in places where linearity

is a stringent requirement and where efficiency can be compromised as in the initial stages of a multi-stage power amplifier.

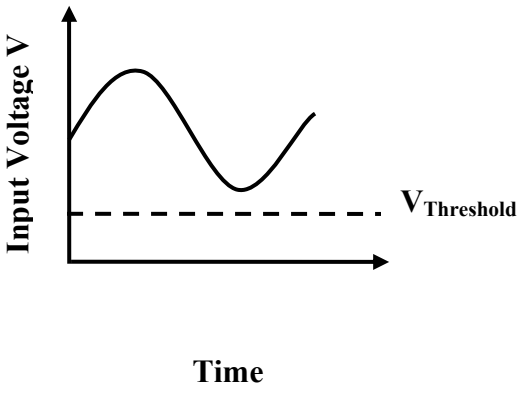

Fig 2.5 **Input signal for Class A**

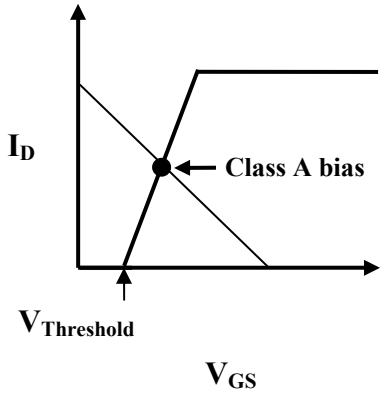

Fig 2.6 **Biasing for Class A**

2.9.2 Class B:

The next class of power amplifiers is Class B. The transistor is biased at the threshold voltage point of the transistor for Class B operation. Hence there is a current flowing at the output of the device only when there is a signal at the input. Moreover the device would conduct current only when the input signal level is greater than the threshold voltage. This occurs for the positive half cycle of the input signal and during the negative half cycle the device remains turned off. Hence the conduction angle for Class B operation is 180º or π radians. Due to this behavior; there is a large saving in the power loss. It can be shown that the maximum theoretical efficiency achievable with Class B operation is about 78.5% [5]. Commercial Class B amplifiers typically have an efficiency of 50-60%. However, the increased efficiency comes at the cost of reduced linearity. The reduction in the output power occurs because the output current flows for only one half cycle of the input signal. The poor linearity is primarily attributed to an effect called the crossover distortion [5]. Whenever the transistor is turned on (at the start of positive half

cycle) and turned off (at the start of negative half cycle) the transistor does not change abruptly from one state to the other. Instead the transition is gradual and nonlinear, and results in an offset voltage. This voltage alters the output waveform (crossover distortion) thereby reducing the linearity. Sometimes a Class B amplifier is realized in "push-pull" configuration. In this configuration the two transistors are driven 180º out-of-phase so that each transistor is conducting for one half cycle of the input signal and turned off for the other half cycle.

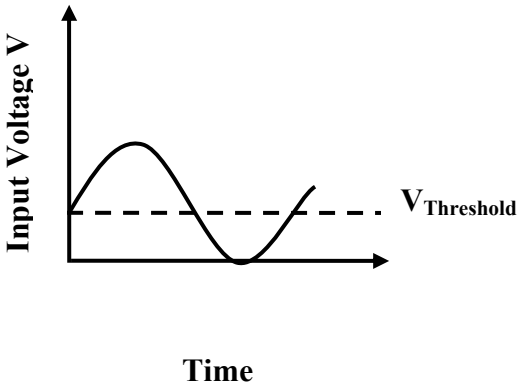

Fig 2.7 **Input signal for Class B**

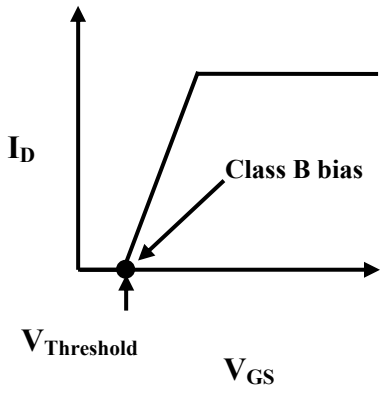

Fig 2.8 **Biasing for Class B**

2.9.3 Class AB:

The crossover distortion effect in Class B amplifiers can be minimized by biasing the gate in such a way so as to produce a small quiescent drain current. This leads to the type of amplifiers called Class AB, where the transistor is biased above the threshold voltage but below the center of the load line. Class AB amplifier operation, as the name suggests, can be considered to be a compromise between Class A and Class B operation. The conduction angle of a Class AB amplifier lies between 180º and 360º. By varying the conduction angle the amplifier can be made to behave more as a Class A or Class B amplifier. Hence the theoretical maximum efficiency of a Class AB amplifier is between

50% and 78.5%. But commercial Class AB amplifiers typically have much lower efficiency in the order of 40-55%. Thus a trade-off between linearity and efficiency can be achieved by simply changing the gate bias. Class AB amplifiers can also be realized in push-pull configurations even though single transistor configuration is preferred for high frequency linear operation.

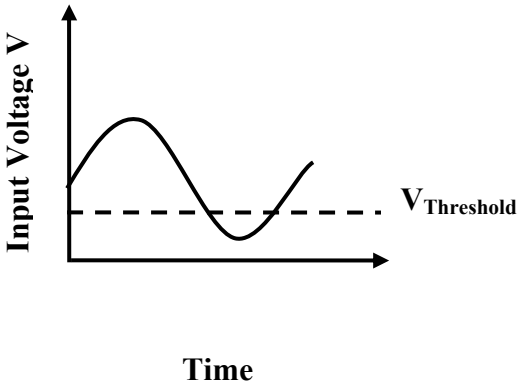

Fig 2.9 **Input signal for Class AB**

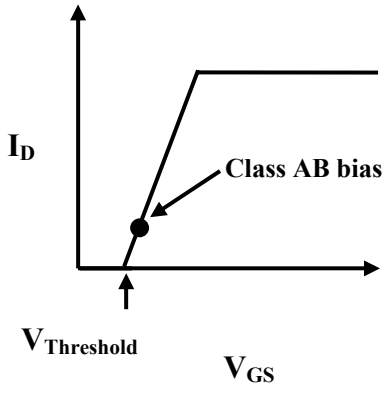

Fig 2.10 **Bias for Class AB**

A practical implementation of a single transistor Class AB is shown in Figure 2.11. In addition to the matching networks and the bias networks, a parallel filter tuned to the fundamental frequency is often used. This filter presents the load impedance to the fundamental component of the output signal and presents a short circuit to all other frequencies. Thus harmonics are shunted to ground, preventing them from reaching the load.

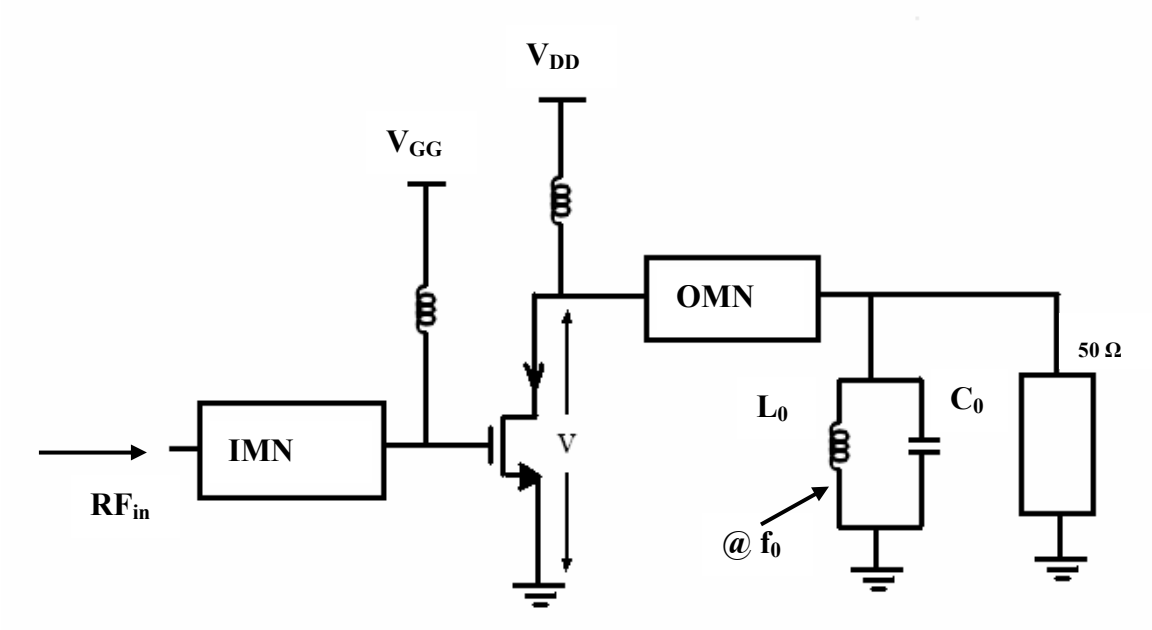

Fig 2.11 **Single transistor Class AB configuration with output harmonic filter**

2.9.4 Class C:

A Class C power amplifier is a non-linear power amplifier used in places where linearity is not a requirement and high efficiency is highly desired. Class C amplifiers are widely used in constant envelope modulation systems where linearity is not required. The transistor is biased below threshold for Class C operation and hence the device conduction angle varies from 0º to 180º. When a voltage signal is applied to the input, the transistor conducts only for the period of time when the input signal is greater than the threshold voltage. The transistor remains switched off at all other times. Since only a portion of the positive input voltage swing takes the device into the amplifying region the output current is a pulsed representation of the input. Due to this pulsed output current the input and output voltages are not linearly related. Thus the amplitude of the power amplifier output is highly distorted. The efficiency of a Class C amplifier depends on the conduction angle. The efficiency increases for decreasing conduction angle. The maximum theoretical efficiency of a Class C power amplifier is 100%. However this is obtainable only for a conduction angle of 0º which means that no signal is applied and

this condition is of no interest. Commercially Class C amplifiers typically show an efficiency of 60% or more.

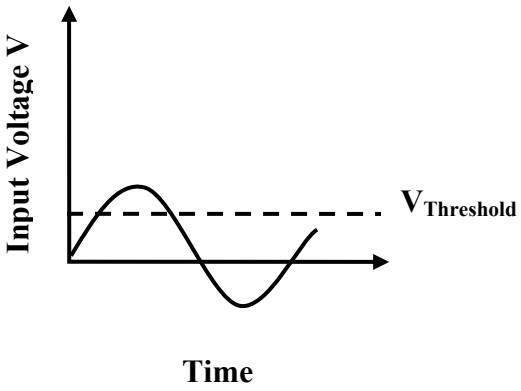

Fig 2.12 **Input signal for Class C**

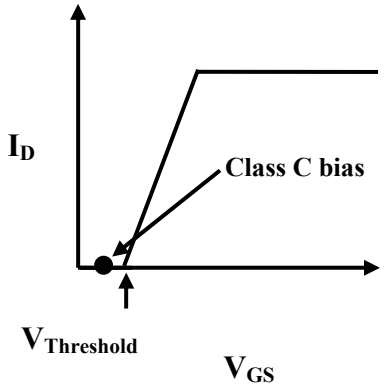

Fig 2.13 **Bias for Class C**

2.9.5 Class E:

Class E power amplifiers are fundamentally different from the other types of power amplifiers discussed before. In the previously described power amplifier classes, it was seen that the operational differences were obtained by the selection of the bias point. However, in a Class E amplifier, only circuit-independent signal guidelines are given (discussed below), and the topology is not as restricted. The idea behind the Class E amplifier is to have non-overlapping output voltage and output current waveforms, and to limit the values of the voltage, current, and the derivative of the voltage with respect to time at the instants when the transition between non-zero currents and non-zero voltages occurs [6]. In [7], the first published work on Class E amplifiers; the important conditions for Class E operation are listed. These conditions are based on the assumption that the transistor acts like a switch for Class E operation. Also the terms “on” state and “off” state are used to describe the time period when the transistor starts conducting and stops conducting respectively. The voltage across the switch must return to zero just before the switch turns “on” and starts conducting current. Similarly the current through the switch

must return to zero just before the switch turns "off". These two conditions avoid the energy dissipation caused by the simultaneous superposition of substantial voltage and current on the switching transistor during transition from "on" to "off" state or "off" to "on" state. Another condition for Class E operation is that the voltage across the switch must return to zero with zero slope (i.e., $dv/dt = 0$). Hence the current through the transistor at the beginning of "on" state is zero. Similarly the current through the transistor must return to zero with zero slope (i.e., $di/dt = 0$) and the voltage across the transistor at the beginning of "off" state is zero. Hence for a deviation in the switching instant from the ideal switching time the corresponding output voltage or current will be very small, and the power lost in the device due to this non-ideality will be relatively small [7]. With all these conditions satisfied, very high efficiencies can be achieved. However it is quite difficult to meet all these requirements in practice. The maximum theoretical efficiency of Class E amplifiers is 100% [3], however efficiency values around 60% are typically achieved.

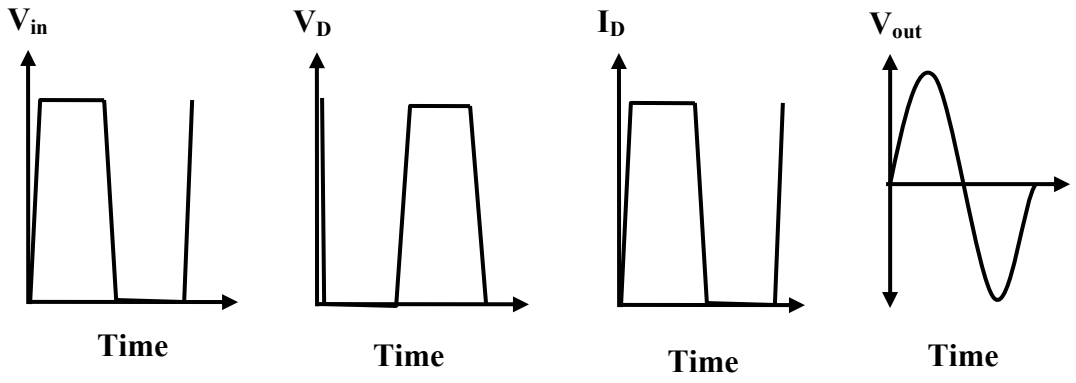

Fig 2.14 **Typical Class E Waveforms**

2.9.6 Class F:

Class-F amplifiers are usually considered as very high efficiency (80% or more power-added efficiency) amplifiers where the high efficiency is obtained through the use of

harmonic traps (L-C filters or quarter-wavelength transmission lines) which provide suitable terminations (either open or short) for the harmonics generated. By doing this, a square wave drain voltage and a peaked half-sinusoidal drain current out-of-phase by 180º are produced. Since only a drain voltage or a drain current exists at any given time, the power dissipation is ideally zero resulting in 100% theoretical efficiency. These very high efficiency values are usually associated with poor linearity. However the linearity can be improved to meet the design standards but compromising on efficiency.

2.10 Conclusion

The important concepts associated with power amplifier design were explained in this chapter. In addition some of the common power amplifier types, used widely commercially, were discussed. The Class F amplifier is described in detail in the next chapter. As mentioned before there are other types of power amplifiers such as the Class D, Class S, Doherty and Chireix Outphasing amplifier that were not discussed here. For a detailed study of the various amplifier classes it is recommended that the reader reviews [4].

Chapter 3

Class F Power Amplifiers

3.1 Introduction

Class F power amplifiers provide major improvement in power added efficiency, output power and gain by loading the device output with appropriate terminations at fundamental and harmonic frequencies. The idea of using harmonic terminations to improve efficiency was first introduced in 1950s [8]. Basically, an amplifier can be made to operate in Class F mode by providing to the device output open-circuit terminations at the odd harmonic frequencies and short-circuit terminations at the even harmonic frequencies of the fundamental component. The resulting ideal drain voltage waveform is a square wave and the ideal drain current is a truncated sinusoid. This results in the reduction of harmonic power since there is no flow of output current for high drain voltage and there is maximum current flow when the drain voltage waveform is at its minimum. Based on this idea, significant research has been done to determine the various factors that affect Class F performance and also the harmonic terminations required for optimum behavior. Snider [9] focused on the optimally loaded and overdriven power amplifier to derive the correct harmonic terminations under ideal conditions. Raab [10] theoretically derived the maximum output power and efficiency that can be achieved using third-harmonic and

fifth-harmonic output peaking. This is especially useful to make a trade-off between efficiency and circuit complexity. Colantonio et al. [11], [12] have derived the importance of harmonic-generating mechanisms and harmonic manipulations for optimizing Class F performance. In this section, Class F operation, the necessary background for designing Class F amplifiers and the various factors affecting Class F performance will be discussed in detail.

3.2 Background

Poor energy efficiency directly affects operational costs and causes thermal heating issues in base station transmitters. To attain high efficiency, the transistor of a Class F amplifier must operate as a closed switch for half the time period and as an open switch for the rest half of the time period. By doing so, the drain voltage will be zero when the transistor is conducting current as a closed switch, and the drain current will be zero when the transistor acts as an open switch holding considerable voltage across it. Thus at any given instant, either the voltage or current at the drain is zero and hence no power is lost in the device.

3.3 Basic Class F operation

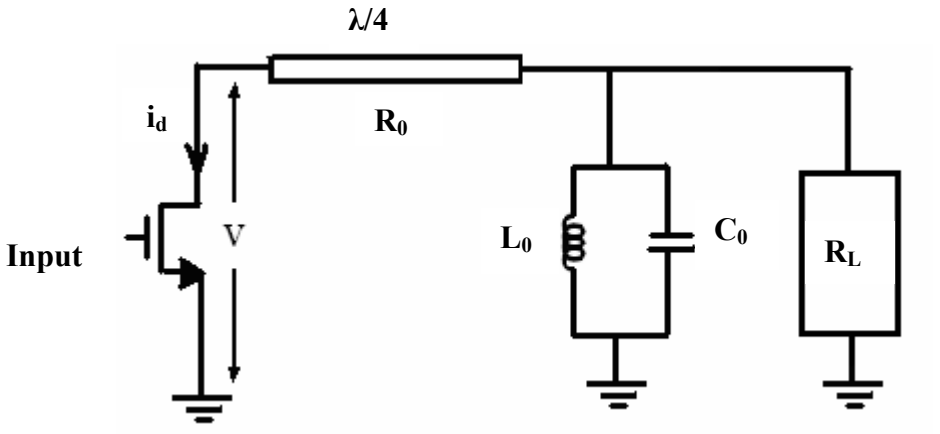

Fig 3.1 **Class F design using quarter-wave transmission line at the output**

Fig 3.1 shows a simple Class F design using a quarter-wave transmission line as discussed in [13]. The load resistor R_L is shunted by a parallel tank circuit that has infinite impedance at the fundamental frequency and zero impedance at all harmonics. Thus the impedance presented to the drain by the transmission line varies with frequency. At the fundamental frequency, the input impedance of the quarter-wave transmission line of characteristic impedance R_0 is:

$$\mathbf{R} = \frac{\mathbf{R_0^2}}{\mathbf{R_L}} \tag{3.1}$$

At even harmonics, the transmission line behaves as if it is half wavelength (or multiples of λ/2) long. Hence the short-circuit for even harmonics at the output is reproduced at the drain. At the odd harmonics, the transmission line behaves as if it is quarter wavelength (or multiples of λ/4) long and translates the short circuit at the output into an open circuit at the drain. The short circuit at even harmonics results in the presence of only the fundamental and odd harmonic voltages at the drain. The DC component of drain voltage, the fundamental voltage and the odd harmonic voltages add up at the drain to produce a square-wave drain voltage. Since the average voltage of the drain must be V_{DD} if there is no DC drop in the RF choke, the square wave voltage swings between 0 and $2V_{DD}$. If the characteristic impedance of the transmission line (R_0) is assumed to be equal to R_L, then R is also equal to R_L. The fundamental-frequency component of the square-wave drain voltage then appears across the load:

$$\mathbf{v_L(t)} = \frac{\mathbf{4V_{DD}}}{\pi}\mathbf{\sin \omega t} \tag{3.2}$$

The load voltage lags the drain voltage by 90º because of the phase shift in the quarter-wave transmission line. The fundamental-frequency current that flows in the load is just the load voltage divided by R:

$$i_L(t) = \frac{4V_{DD}}{\pi R} \sin \omega t \tag{3.3}$$

The odd harmonics in the drain-voltage waveform convert the sine wave into a square-wave, but, since they do not cause current to flow, they consume no power. The output power is produced entirely by the fundamental-frequency current and voltage and is found to be:

$$P_0 = \frac{v_L i_L}{2} = \frac{8V_{DD}^2}{\pi^2 R} \tag{3.4}$$

When the transistor is off, the drain current must be zero. The RF choke passes only dc, so the fundamental-frequency current that flows through the load must also flow through the drain. Since the transmission line is an open circuit to odd harmonics, the drain current must be composed of a fundamental and even harmonics. Furthermore, because the transmission line acts as a short circuit to even harmonics, the drain can draw any amount of even-harmonic current necessary to meet other circuit requirements. This even-harmonic current results in a half-sinusoidal drain current whose peak amplitude is equal to the peak-to-peak amplitude of the output current:

$$i_{DP} = \frac{8V_{DD}}{\pi R} \tag{3.5}$$

The even-harmonic currents circulate through the drain, transmission line, output network, but no power is consumed because they have zero voltage.

3.4 Third Harmonic Peaking Class F PA

In order to reduce the circuit complexity, a class F amplifier is often used in a third harmonic peaking mode. Third harmonic peaking refers to a Class F amplifier with only a harmonic trap for the third harmonic vs. all odd harmonics. In this section the maximum

efficiency and power output capability of a Class F amplifier with third harmonic peaking is derived. It is possible to obtain a higher efficiency with a Class F third harmonic peaking amplifier than in Class B or C amplifiers [3] because the presence of the third harmonic in the collector voltage causes its waveform to flatten. However it should be noted that the third harmonic component should be added 180º out-of-phase with the fundamental to obtain the flattened voltage waveform. This has been shown in [11] and the results are reproduced in Figures 3.2 and 3.3. The in-phase and out-of-phase behavior can be seen clearly at $w_0t = -\pi, 0, \pi, 2\pi$ and so on.

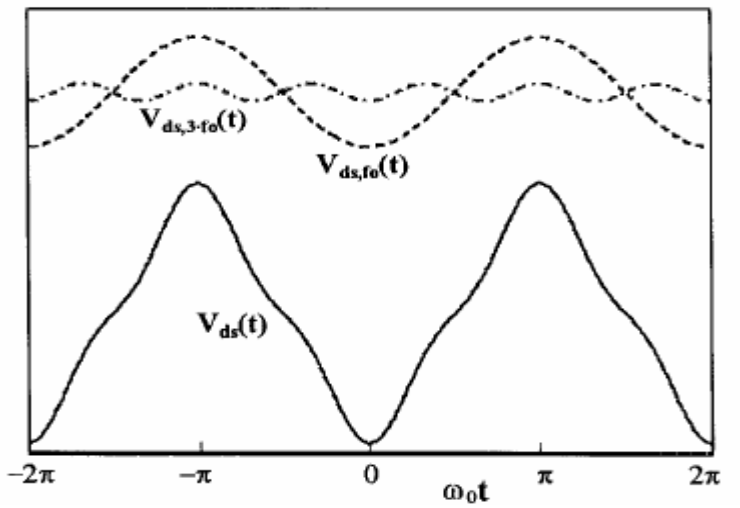

Fig 3.2 **Output voltage when fundamental and third harmonic components are in-phase**

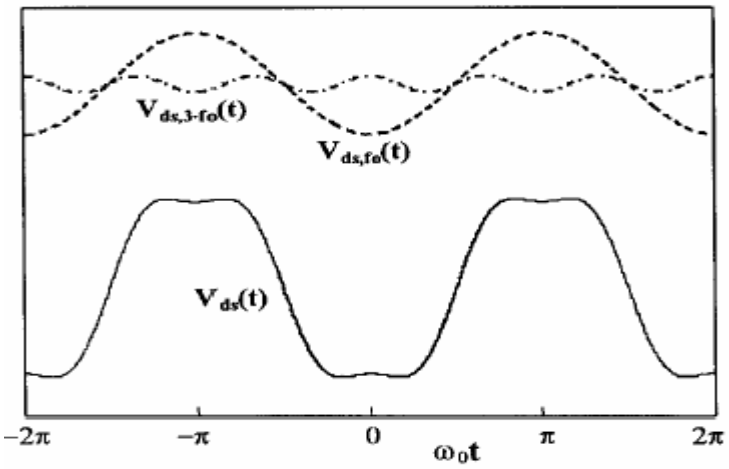

Fig 3.3 **Output voltage when fundamental and third harmonic components are out-of-phase**

The purpose of adding a third harmonic component to the drain voltage is to reduce the negative peak of the voltage waveform, while leaving the magnitude of the fundamental frequency component unaffected [11]. Hence the two voltage components must have opposite signs. Since the third harmonic voltage is obtained by loading the corresponding current component with a resistive termination, proper shaping can be obtained only if the third harmonic current component is negative. In [11] the behavior of the various current components as a function of the conduction angle has been presented. Those results are reproduced in Figure 3.4.

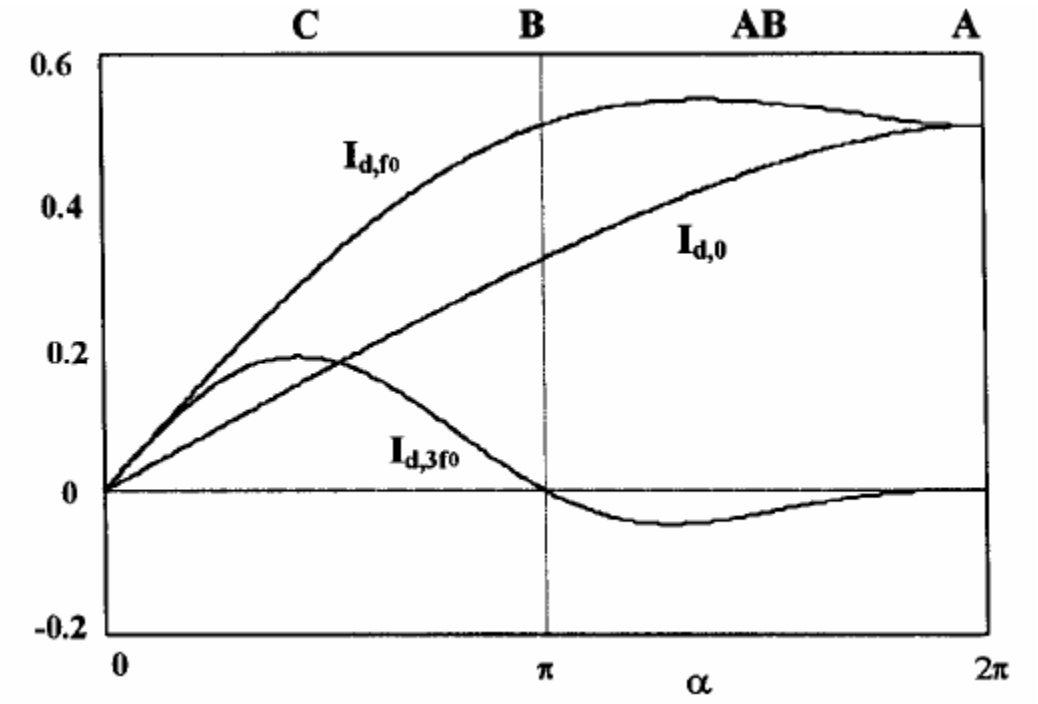

Fig 3.4 **Normalized amplitudes of the drain current harmonic components at DC, f_0 and $3f_0$ as a function of the drain current conduction angle**

From this plot, we see that for proper Class F operation, the transistor must be biased as a Class A, AB or B amplifier. Biasing the transistor below the threshold as in Class C bias would lead to phase issues due to the positive third harmonic current. Usually the Class F transistor is biased in Class B mode as it gives a better efficiency than biased as Class A

or Class B due to the generation of large harmonics. However that would result in a poor linearity. Hence a Class AB bias point was chosen for this design.

The maximum efficiency and the power output capability of a Class F amplifier for Class B bias is derived below. For Class AB bias, the maximum efficiency attainable will be less than this value whereas the power output capability will be more than the corresponding Class B value.

The drain voltage which is the sum of a DC component, the fundamental voltage and the third harmonic voltage can be given as:

$$\mathbf{v(\theta) = V_{dc} + V_0 \cos\theta - V_3 \cos 3\theta = V_{dc} + V_0(\cos\theta - x\cos\theta)} \quad (3.6)$$

where $x > 0$ and is equal to V_3/V_0 and $\theta = \omega t$

The optimal value of x can be found by setting $\frac{\mathbf{dv(\theta)}}{\mathbf{d(\theta)}} = \mathbf{0}$ is found to be 1/9.

When x=1/9, the peak-to-peak voltage swing of $v(\theta)$ is $(16/9)V_0$.

Since the maximum drain voltage swing is $2V_{dc}$, the maximum amplitude of the collector voltage is:

$$V_0 = (9/8)\, V_{dc} \quad (3.7)$$

Thus the peak output power is given by

$$\mathbf{P_0 = \frac{V_0^2}{2R} = \frac{81V_{dc}^2}{128R} = 0.6328\frac{V_{dc}^2}{R}} \quad (3.8)$$

The amplitude of the drain current I_{DM} and the DC current I_{dc} are given as

$$\mathbf{I_{DM} = V_0/R = (9V_{dc}/8R)} \quad (3.9)$$

$$\mathbf{I_{dc} = (2/\pi)\, I_{DM} = (9V_{dc}/4\pi R)} \quad (3.10)$$

Hence the maximum drain efficiency and power output capability are given by

$$\eta = \frac{\mathbf{P_0}}{\mathbf{P_{dc}}} = \frac{\mathbf{P_0}}{\mathbf{V_{dc}I_{dc}}} = \mathbf{88.36\%} \tag{3.11}$$

$$\mathbf{C_p} = \frac{\mathbf{P_0}}{\mathbf{2V_{dc}I_{DM}}} = \mathbf{0.1406} \tag{3.12}$$

We notice that the third harmonic peaking Class F amplifier gives roughly 27% higher output power, 10% higher drain efficiency and has 12% higher power output capability than a Class B amplifier.

3.5 Factors Affecting Class F Performance

Harmonic generating mechanisms along with bias selection play an important role on the feasibility of the Class F scheme. The amplitude and phase of the harmonic drain currents relative to the fundamental currents should meet specific requirements in order to obtain optimum performance. In power amplifiers, at higher drive levels the drain voltage and current are not purely sinusoidal – they exhibit a considerable harmonic content. A higher harmonic content is useful in getting a maximally flat voltage waveform at the expense of linearity.

Harmonics are usually generated by clipping which is generally due to

- forward conduction of the gate-channel junction
- pinch-off of the conducting channel
- gate-drain junction breakdown
- Resistive losses of the device in triode region.

The zero power loss condition in Class F amplifiers is an ideal condition that is never practically achievable. Only a transistor with zero saturation resistance (R_{ON}) can lead to

zero power loss. All practical transistors have a finite saturation resistance which results in power loss and hence reduces the efficiency. In simple terms the efficiency for the finite resistance case can be given as

$$\eta_F = R/(R + 2R_{on}) \tag{3.13}$$

The saturation resistance also decreases the maximum power output.

The effect of the saturation resistance can be reduced by placing 2 transistors in parallel. But this would lower the output impedance as well leading to difficulties in output matching. Another way to reduce R_{ON} is to set the value of R greater than the resistance R_{max} at which maximum power occurs [13]. This improves the efficiency but reduces the output power. A higher value of V_{dd} may also result in a better efficiency but the transistor breakdown voltage would set a limit on this value.

3.6 Conclusion

This chapter presented the necessary background on Class F amplifier operation and explained the critical parameters that affect its design. Based on this knowledge, a Class F amplifier design for WCDMA specifications will be discussed in the next chapter.

Chapter 4

Design and Implementation

4.1 Introduction

The basic operating principle of a Class F power amplifier and the factors that aid or affect the Class F performance were explained earlier. A Class F power amplifier design that meets the WCDMA specifications is described in this section. The Class F amplifier was designed using Motorola's LDMOS (Laterally Diffused Metal Oxide Semiconductor) transistor models and its performance was simulated using ADS. Various procedures involved in the design of the Class F amplifier such as DC simulation, bias point selection, source-pull and load-pull characterization, input and output matching circuit design and the design of suitable harmonic traps are explained.

4.2 Design Specifications

As mentioned earlier, WCDMA requires high linearity to provide bandwidth efficiency. The Class F amplifier was designed to operate in the WCDMA band (2.11 – 2.17 GHz) and was expected to meet the set of specifications listed in Table 4.1.

Operational center frequency	2.14 GHz
Output power	4 W (36 dBm)
PAE at maximum output power (should be higher than similarly biased Class AB)	50% or better
PAE at 6 dB back-off from maximum output power	20% or better
Third order intermodulation products at maximum output power (should be comparable to similarly biased Class AB)	-20 dBc
Third order intermodulation products at 6 dB back-off from maximum output power (should be comparable to similarly biased Class AB)	-30 dBc

Table 4.1 **Design Specifications for WCDMA power amplifier**

4.3 Bias Point Simulation

The first step towards designing the Class F amplifier was to select a suitable bias point for operation. A Class F amplifier can be biased as a Class A, AB, B or C amplifier and then suitable harmonic terminations can be designed to get efficiency higher than what could be achieved originally. It was seen earlier that Class A, AB, B and C amplifiers differ merely by their respective conduction angles. Thus a device can be made to operate under any of these modes by suitable adjusting the gate bias. It was also seen earlier that the Class AB amplifiers are generally used in WCDMA systems in order to provide linear operation at a reasonable efficiency. Hence the Class F power amplifier was biased as a Class AB amplifier. In order to determine the bias point a DC bias point simulation was performed. Fig 4.1 shows the plot of the DC transfer characteristics for the transistor at a drain-source voltage of 26 V. The drain bias voltage value was chosen to be 26 V in order to provide a large output voltage swing and at the same time to ensure that the device is operated below the transistor breakdown voltage of 58 V.

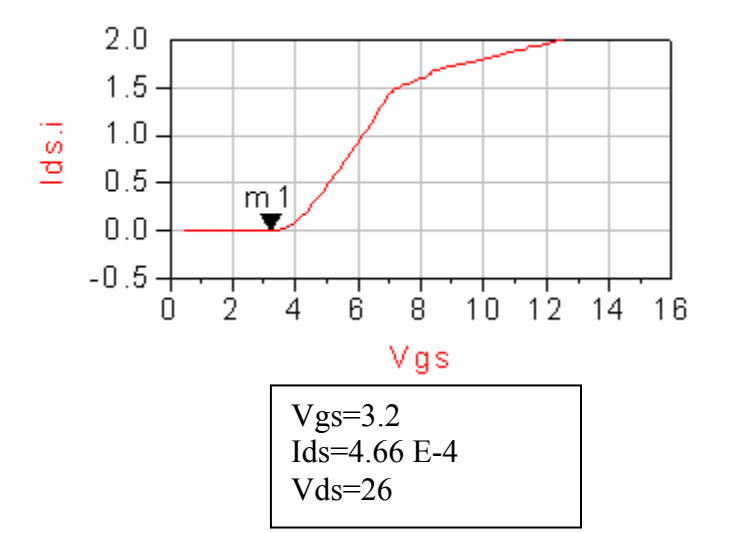

Fig 4.1 **Plot of transistor DC transfer characteristics at Vds = 26 V**

From Figure 4.1, we see that the transistor must be provided with a gate bias voltage between 3.2 V and 5.1 V for Class AB operation. A 3.8 V gate bias voltage was chosen for this design.

4.4 Load Pull and Source Pull

Load pull is a technique wherein the load impedance seen by the device under test (DUT) is varied and the performance of the DUT is simultaneously measured [4]. Similarly in source pull the performance of the DUT for varying source impedances is measured. The measured results are very useful in determining the optimum load and source impedance which the device must see to give the best performance. Load pull, in particular, is commonly used to determine the load impedance required for maximizing efficiency. The input of a power amplifier is usually conjugate matched and the source pull is not always required. However in the design of a Class F power amplifier, it has been shown in [14] that the source pull is useful to investigate the effects of the second harmonic termination and make appropriate corrections to improve the Class F performance. The impedance seen by the device for maximum efficiency, power and gain can be quite different. In such cases the impedances are chosen as per the design requirements. It should be noted

that the impedance values calculated vary with bias. In this design load pull and source pull were performed to obtain maximum efficiency. The results obtained from these simulations shows that the transistor needs to see an impedance of 9.22 + j24.42 ohms at the output and 7.4 + j1.065 ohms at the input as shown in Figure 4.3.

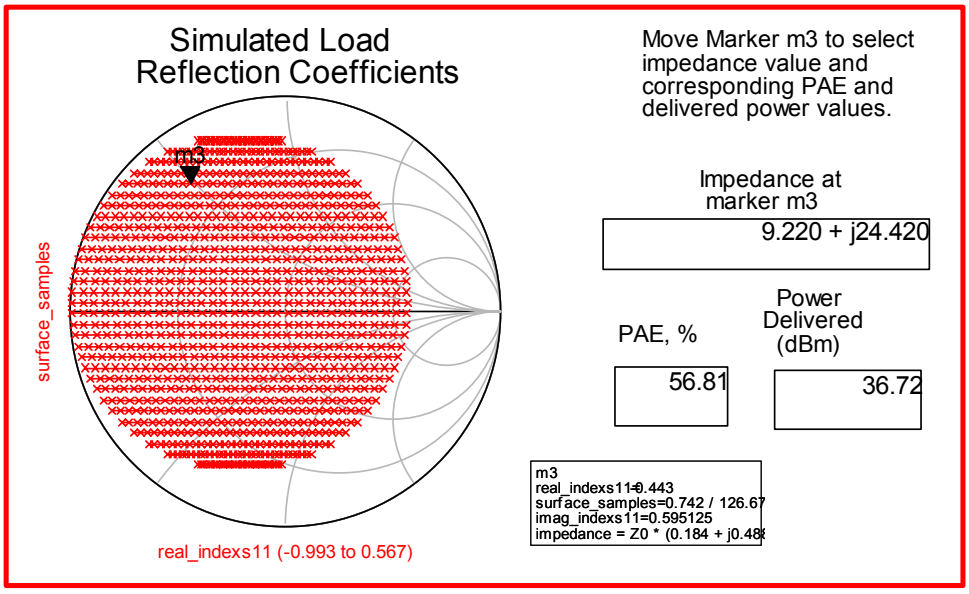

Fig 4.2 **Load Pull Analysis to determine load impedance for maximum efficiency**

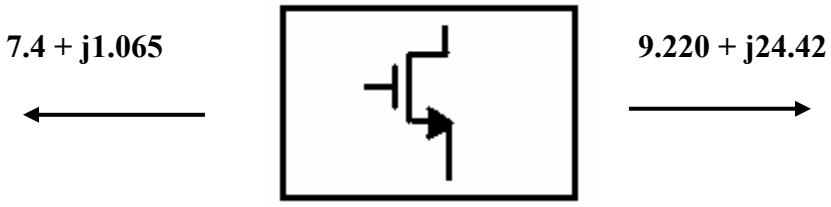

Fig 4.3 **Load and Source Impedance for maximum efficiency**

4.5 Design Architecture

Figure 4.4, shows the basic design architecture of the Class F power amplifier. V_{DD} and V_{GG} provide the required drain and gate bias determined previously from a 26 V supply. The DC bias and Dc blocks are ignored here. The input and output matching networks transform the impedance that the transistor needs to see at their respective sides to 50 ohms. The filter combination L_0C_0 is tuned to the fundamental frequency. It provides very high impedance (ideally an open circuit) for the fundamental frequency and very low impedance (ideally a short circuit) for harmonic frequencies. L_3 and C_3 together form the third harmonic trap. This trap provides high impedance for the third harmonics and allows all other signals to pass through. Due to this the third harmonic voltages gets added out of phase to the fundamental voltage at the drain causing the flattening of the drain voltage waveform. The series filter combination L_2C_2 along with the bypass capacitor bypasses the second harmonics to ground and provides high impedance at other frequencies. This results in short circuit second harmonic current which in turn makes the drain current waveform resemble a peaked half sinusoid.

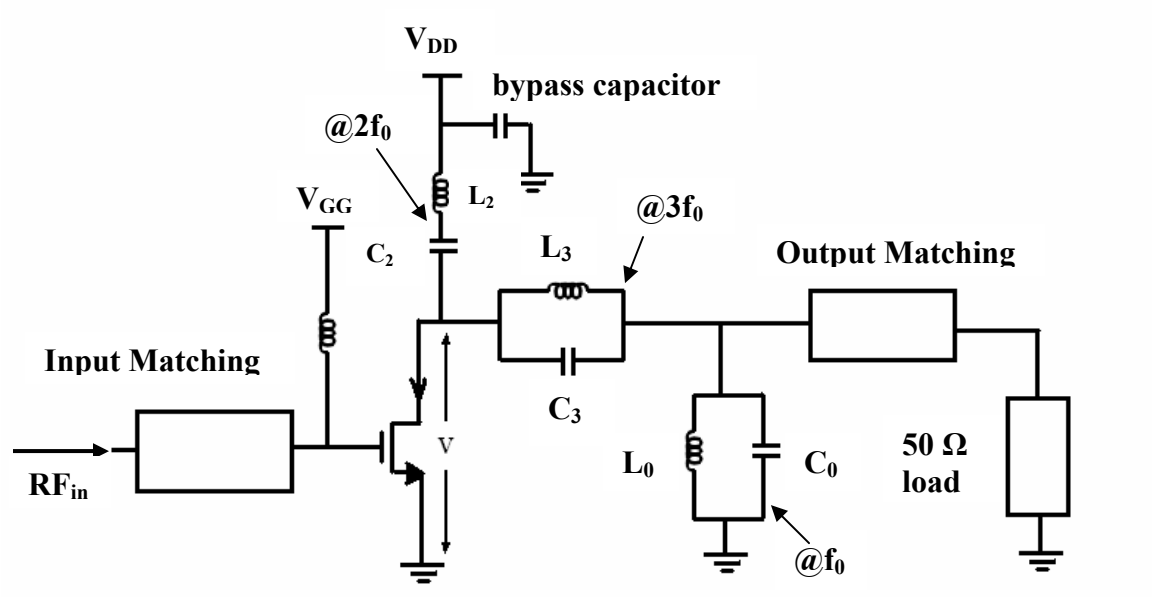

Fig 4.4 **Class F Power Amplifier Design Architecture**

4.6 Input and Output Matching

Input and output matching can be provided using simple discrete element matching network such as an L-network, T-network or pi-network. A pi-network, C12-L6-L7, was used to match from 50 ohms to 7.4+j1.065 ohms. A high pass L-network, L9-C13, was used for output matching from 9.22+j24.42 ohms to 50 ohms. The capacitive element in the output L-network also serves as a DC blocking capacitor.

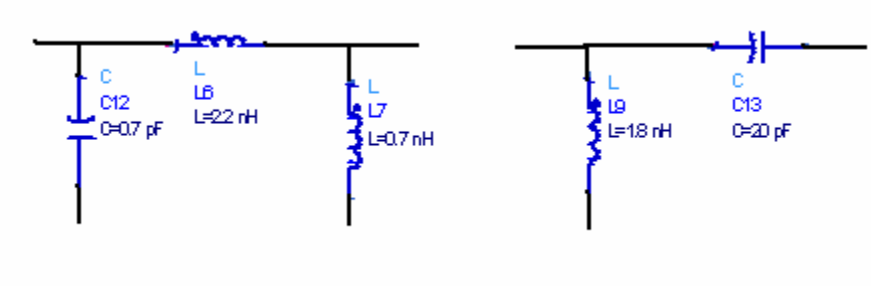

Fig 4.5 **Input and Output Matching Networks**

4.7 Harmonic Terminations

The design of proper harmonic traps is the most crucial and also the most difficult aspect of the design. The third harmonic trap was designed using a parallel L-C filter tuned at the third harmonic frequency of 6.42 GHz. Several combinations of L and C that would resonate at this frequency were designed. Of these, the combination which gives the best performance using as small an inductor as possible was chosen. For the second harmonic trap, a series L-C filter tuned at the second harmonic frequency of 4.28 GHz was initially designed. However, it was noted that there was considerable fourth harmonic current in the circuit, causing power loss. In order to overcome this, a transmission line one quarter-wavelength long at fundamental frequency was tied to the drain of the transistor with its other end bypassed to ground. This was able to provide a very good short circuit at not only the second harmonic frequency but also at the fourth and higher even order frequencies. A similar approach using a quarter-wavelength transmission line to provide an open circuit for odd harmonic frequencies was tried but it was observed that the transmission line was unable to produce a good open circuit. Further, a future work in this

direction would be to realize the harmonic traps on-chip with the output matching done off-chip. A quarter-wavelength line at 2.14 GHz would be too long to fit inside a chip. Hence the third harmonic trap was realized using discrete components. Harmonic traps for the fifth and other higher odd harmonics can be included to improve the performance at the cost of increased circuit complexity. In [10], the trade-off between the number of odd harmonic traps and circuit complexity has been analyzed and it is found that the third harmonic trap is usually enough for acceptable Class F performance. In addition to increasing the circuit complexity, additional harmonic traps may result in loss when realized using practical components. Also at high operational frequencies, it may be impossible to realize the design using practical components. Considering these limitations the selected design scheme for the harmonic traps seems to be the best solution.

4.8 Class F Implementation

The various design blocks of the Class F amplifier were explained in the previous sections. The final design was realized in ADS. The PA uses Motorola's High Voltage Version 4.0 (HV4) 10.2 mm (gate periphery) LDMOS transistor model. Non-ideal inductors with a Q of 20 were used so that the results obtained are close to the performance obtained using commercial inductors. In addition to the Class F design, a Class AB amplifier was also designed. The Class F and Class AB amplifiers use identical transistors, bias points and input and output matching networks. This enables a fair comparison of the two amplifier modes. Figures 4.6 and 4.7 shows the final realization of the Class F and Class AB designs respectively. These designs will be simulated and the results will be analyzed to see if Class F amplifiers can give a linearity performance comparable to that of a Class AB amplifier at higher efficiency.

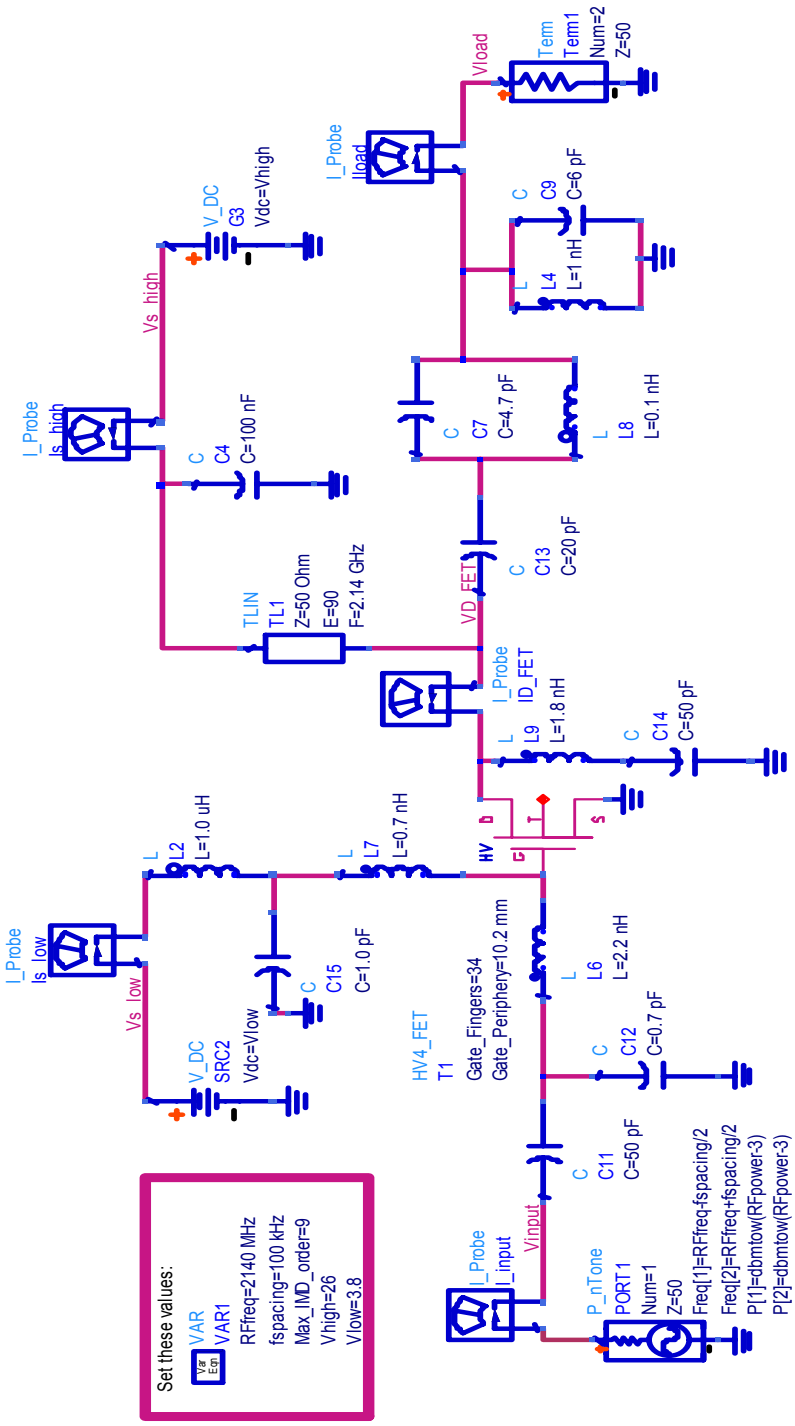

Fig 4.6 **Schematic of the Class F power amplifier Design**

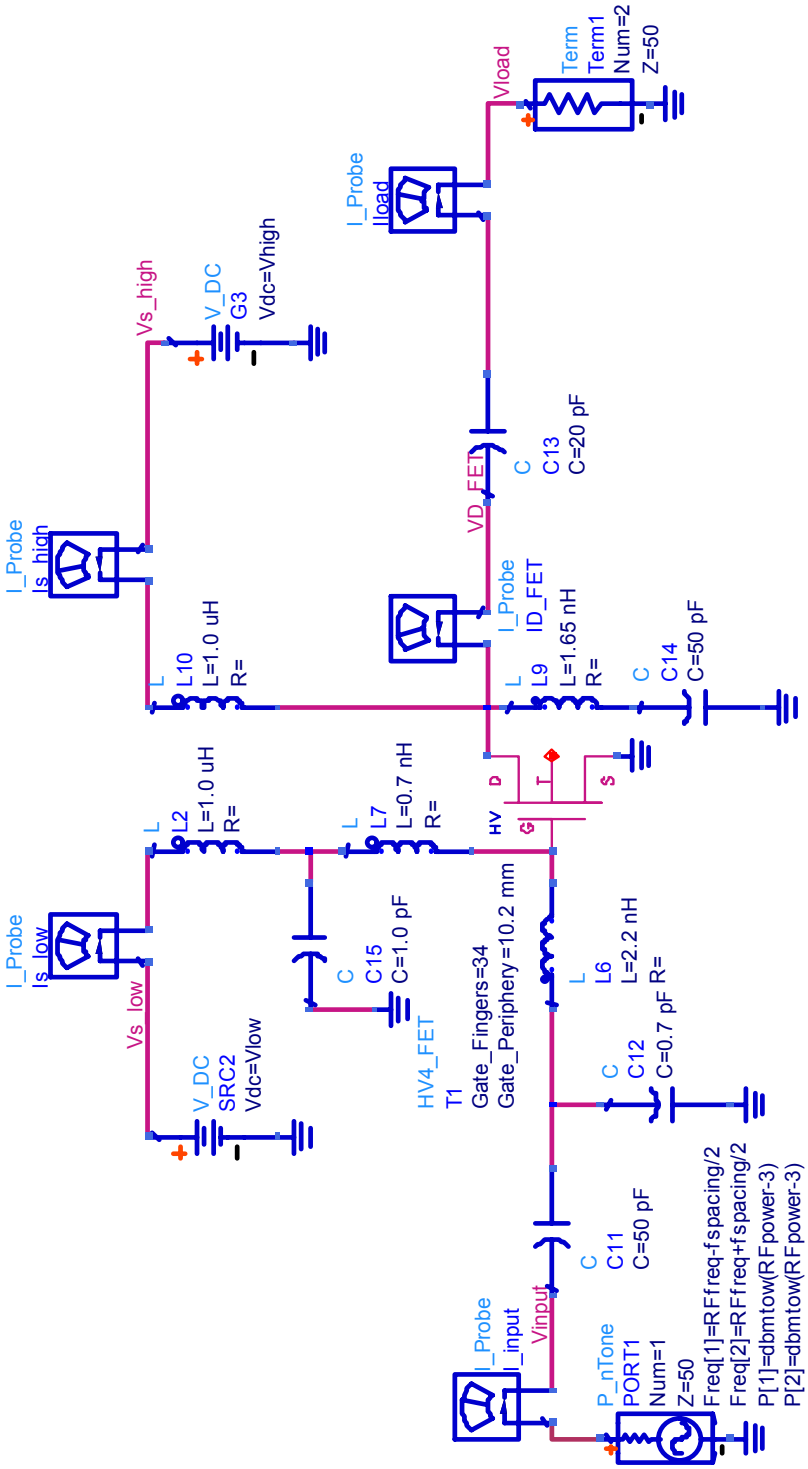

Fig 4.7 **Schematic of Class AB design**

Chapter 5

Results

5.1 Introduction

The Class F amplifier designed earlier was simulated in ADS to evaluate its performance. The designed Class AB amplifier's performance was also measured to see how it compares with the Class F amplifier. This was done by means of single-tone and two-tone harmonic balance simulations. The two-tone test results were compared with the design specifications for WCDMA.

5.2 Bias Point Simulation

As mentioned earlier, bias point simulation was performed in order to bias the transistor in Class AB mode. The results are given in Table 5.1.

Drain-Source Voltage (Vds)	Gate-Source Voltage (Vgs)
26 V	3.8 V

Table 5.1 **Class AB bias voltages**

5.3 Single-tone Simulation

A single-tone simulation was done to plot the voltage and current waveforms at the drain. The resultant waveforms for the Class AB amplifier are given in Figures 5.1 and 5.2 and the waveforms for the Class F amplifier are given in Figures 5.3 and 5.4.

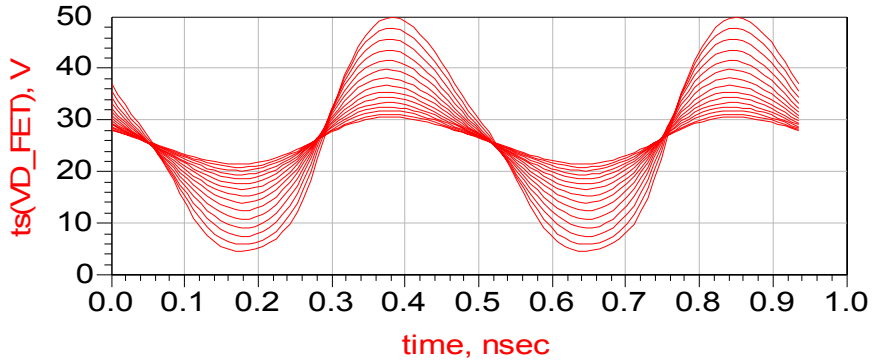

Fig 5.1 **Class AB: Drain Voltage Waveform**

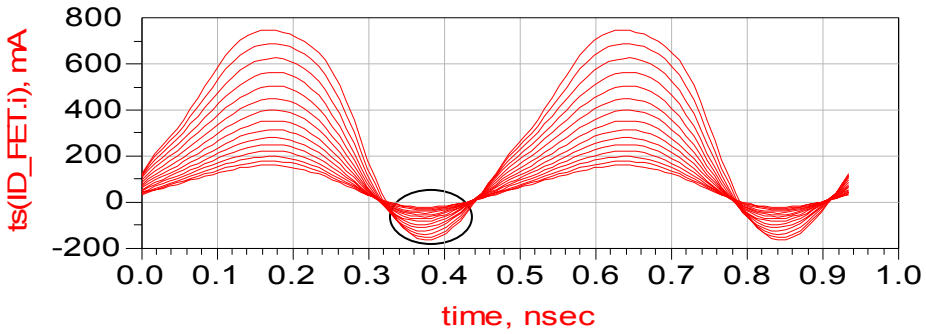

Fig 5.2 **Class AB: Drain Current Waveform**

The drain voltage in Fig 5.1 is a sinusoid swinging from about 3 V to 50 V. The voltage swing is close but slightly less than 2 Vdd just as expected for a Class AB amplifier. The drain current as shown in Fig 5.2 is flowing for more than half the time period. A small quiescent current which is typical of a Class AB mode is also noticed.

Fig 5.3 which corresponds to the drain voltage of the Class F waveform is not exactly a square wave due to the presence of the third harmonic only. Still the addition of the third harmonic flattens out the voltage waveform. This voltage is more prominent when compared with the waveform in Fig 5.1. The voltage waveform can be made to approach a square wave by the addition of higher odd harmonics and by biasing the transistor in deep Class AB or Class B to generate harmonics.

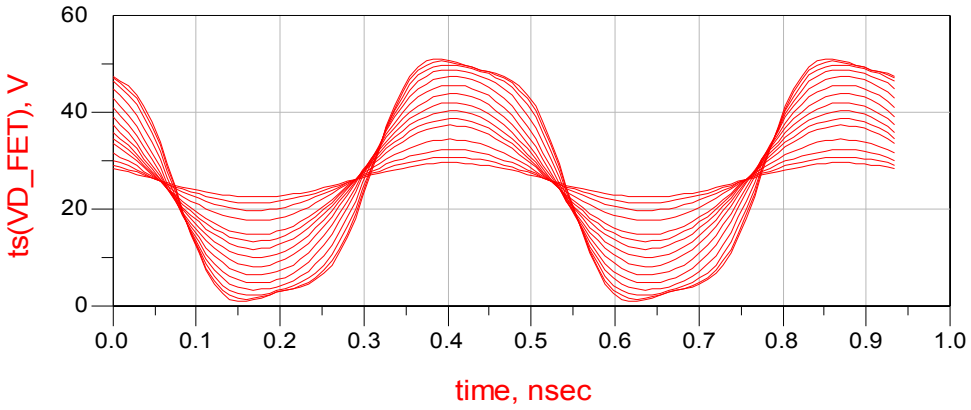

Fig 5.3 **Class F: Drain Voltage Waveform**

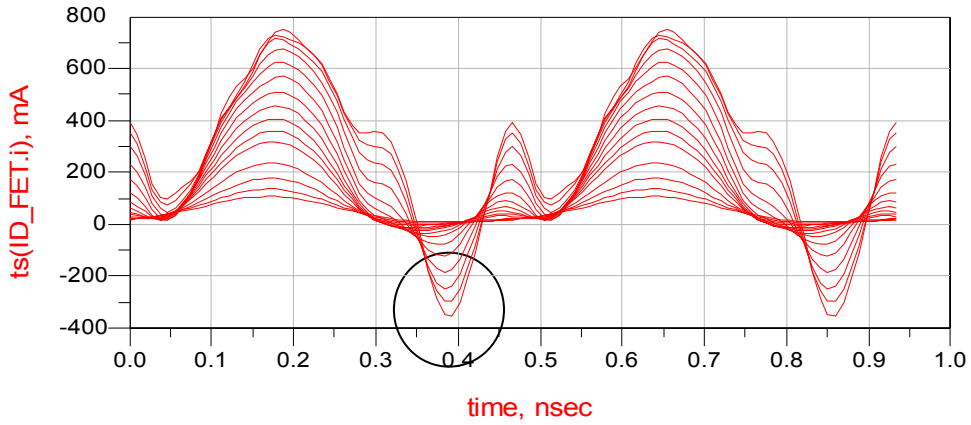

Fig 5.4 **Class F: Drain Current Waveform**

The drain current waveform in Fig 5.4 is a peaked half sinusoidal waveform. It can be seen that the current peaks occur for the period of time when voltage is at its minimum and that the current minimum coincides for maximum voltage values. Hence the power loss is greatly reduced thereby increasing efficiency. The negative transitions of the drain currents for both the Class AB and Class F waveforms are due to the imperfect cancellation of the reactive part at the output of the transistor. This is shown as the circled region in Fig. 5.2 and Fig. 5.4. The output matching network may be adjusted to lessen this effect.

Fig 5.5 shows the AM-PM conversion for the Class F amplifier.

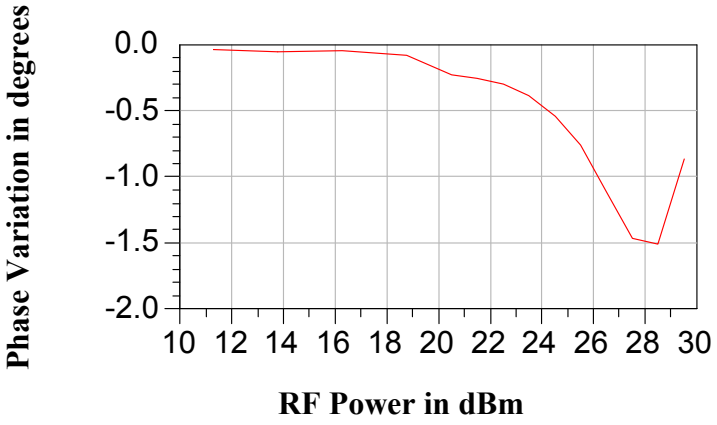

Fig 5.5 **Class F: AM-PM Conversion (deg/dB)**

The AM-PM performance is quite good with a maximum deviation of only 1.5 º/dB corresponding to peak output power. The AM-PM performance indicates the nonlinear behavior of the amplifier. One of the most common effects of AM-PM conversion is the asymmetrical slewing of the intermodulation.

Table 5.2 shows the impedance of the Class F amplifier at the second and the third harmonic frequencies. It is very important for proper Class F operation that the third

harmonic is presented with very high impedance (ideally an open circuit) and the even harmonics are presented with extremely low impedance (ideally a short circuit). The designed circuit is found to present about 4300 ohms at the third harmonic frequency and 0.5 milliohms at the second harmonic frequency. This tells us that the designed harmonic filter circuits are functioning to our expectations.

RF power in dBm	Magnitude of Z3 in Ohms	Magnitude of Z2 in Ohms
28.5	**4355.85**	**5E-4**

Table 5.2 **Class F: Impedance at third and second harmonic frequency**

Tables 5.3 and 5.4 present the second, third, fourth and fifth harmonic levels at the output. The harmonic content at the load must be as low as possible in order to avoid unnecessary power loss and matching issues. The Class F PA due to the harmonic trapping filters presents harmonic content at an extremely low level at the output. In comparison the Class AB PA fares badly. In fact, the second harmonic content is only 15 dB below the useful signal content and the third harmonic content is only 30 dB below carrier.

Second Harmonic dBc	Third Harmonic dBc	Fourth Harmonic dBc	Fifth Harmonic dBc
-104.7	**-85.13**	**-125.1**	**-69.81**

Table 5.3 **Class F: Harmonic levels at the output**

Second Harmonic dBc	Third Harmonic dBc	Fourth Harmonic dBc	Fifth Harmonic dBc
-15.5	**-30.67**	**-32.95**	**-55.86**

Table 5.4 **Class AB: Harmonic levels at the output**

5.4 Two-tone Simulation

Two-tone harmonic balance simulations were performed on the Class F and Class AB designs. Harmonic balance is a frequency-domain analysis technique for simulating distortion in nonlinear circuits. Harmonic balance determines the spectral content of voltages and currents in the circuit. It is very useful to compute intercept point and intermodulation distortion. This is also used to determine the power added efficiency of the amplifier in the presence of interferers. Here the two tone frequencies were chosen to be 2140.05 MHz and 2139.95 MHz. Seventh order harmonic balance simulation was performed to account for all harmonics upto the seventh harmonic. Fig 5.6 is a plot of the output spectrum of the Class F PA.

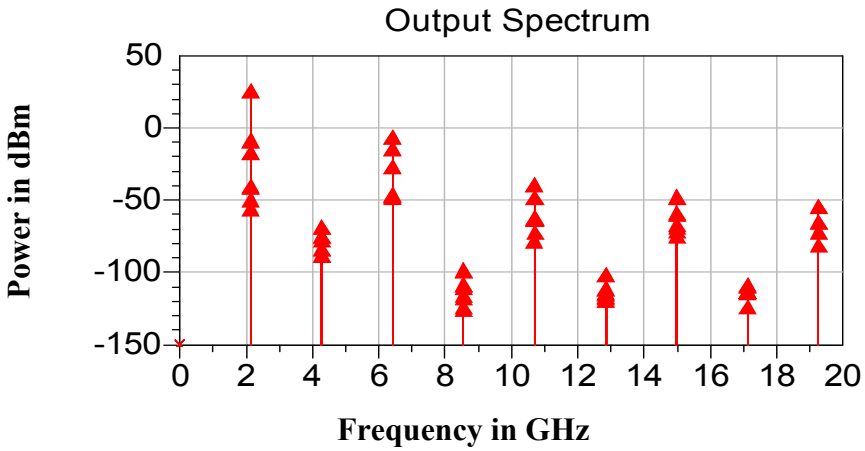

Fig 5.6 **Class F: Output Spectrum**

Fig 5.7 is a zoomed output spectrum of the Class F amplifier. In this plot the third, fifth and seventh order intermodulation products are shown. This plot can also be used to determine the corresponding intercept points.

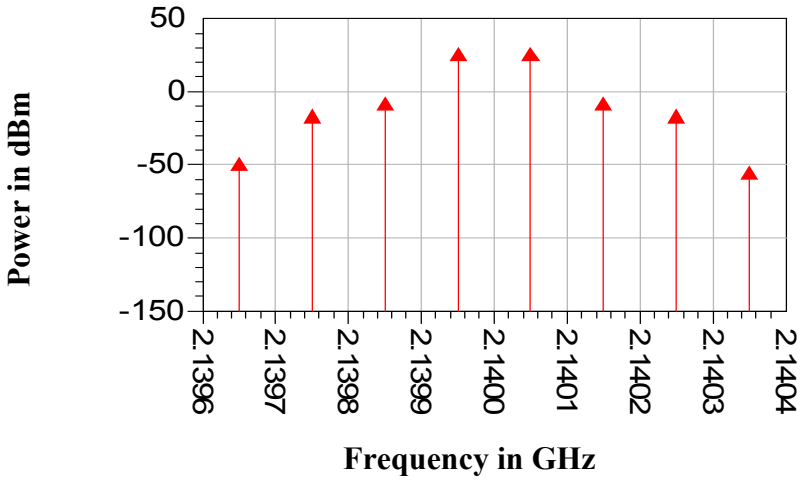

Fig 5.7 **Class F: Zoomed Output Spectrum showing 3rd, 5th and 7th order IMD products**

Figures 5.8 and 5.9 give the signal strength of third order IMD products of the Class F and Class AB amplifiers respectively. It is evident from these plots that the Class F amplifier's linearity performance matches that of the Class AB amplifier. This was a very important design goal and establishes the fact that the linearity of the Class F amplifier is comparable to Class AB linearity when biased in similar fashion.

The value of third order IM products for the Class F PA is almost -22 dBc at peak power and -35.5 dBc at 6 dB back-off from peak power. This meets the design specifications for linearity that was listed earlier.

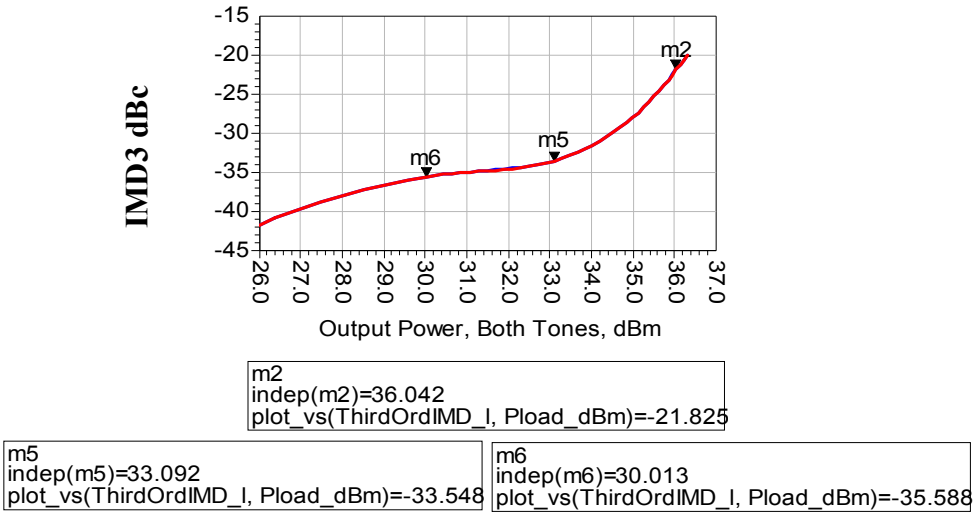

Fig 5.8 **Class F: Plot of third order intermodulation products (dBc)**

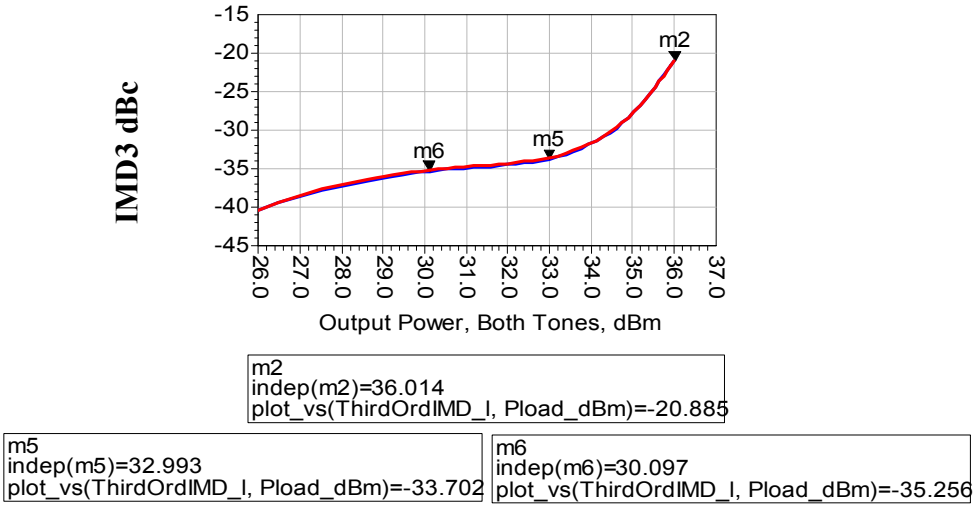

Fig 5.9 **Class AB: Plot of third order intermodulation products (dBc)**

Figures 5.10 and 5.11 show fifth order IMD plots for the two amplifier cases. Once again the performance of the Class F amplifier was found to match the Class AB linearity performance.

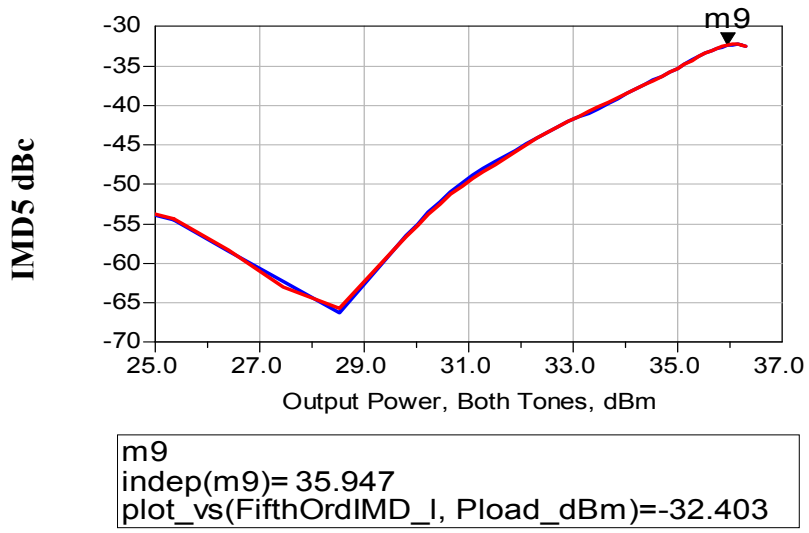

Fig 5.10 **Class F: Plot of fifth order intermodulation products (dBc)**

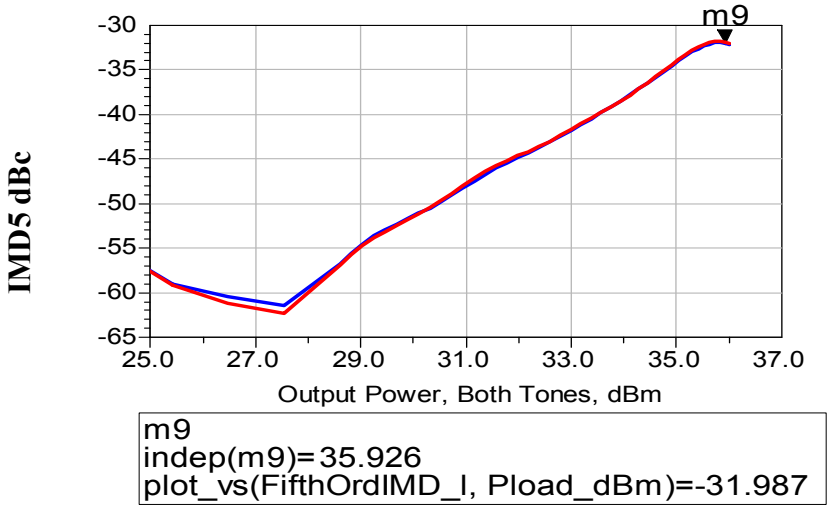

Fig 5.11 **Class AB: Plot of fifth order intermodulation products (dBc)**

Having met the linearity specifications, we shall now determine the power added efficiency of the Class F PA to see if the Class F PA offers a higher efficiency as suggested by the theory and also the design voltage and current waveforms. Figures 5.12 and 5.13 give the PAE plots of the Class F and Class AB amplifiers respectively. The Class F PA shows a marked improvement in efficiency over the Class AB mode. The efficiency of Class F at peak power, 3 dB back-off from peak power and 6 dB back-off from peak power is 60%, 44% and 31% respectively in comparison to 53%, 40% and 27% achieved using a Class AB PA. This is a remarkable improvement from a manufacturing point of view. The important point to note here is that the improved efficiency is obtained without compromising linearity.

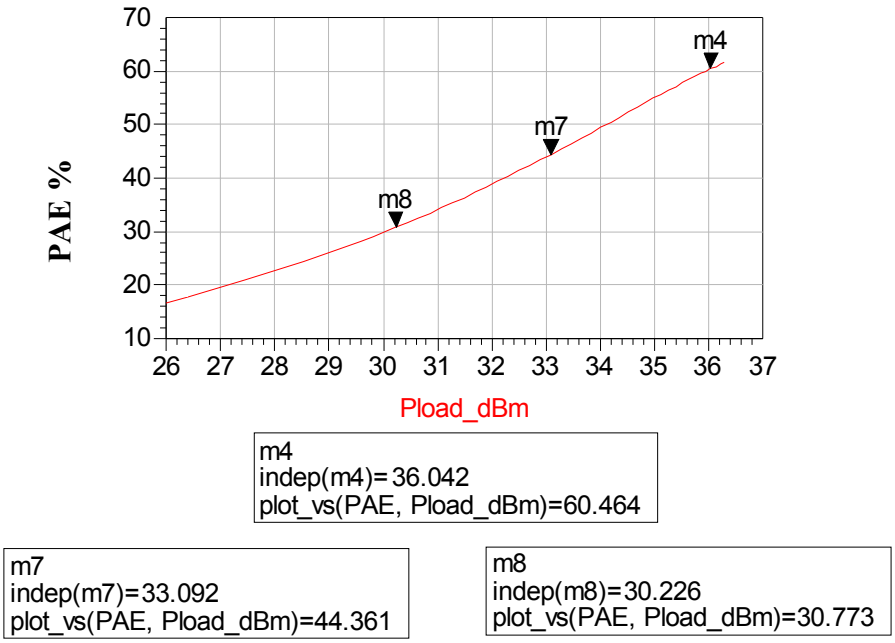

Fig 5.12 **Class F: Plot of PAE (%) vs. Output Power (dBm)**

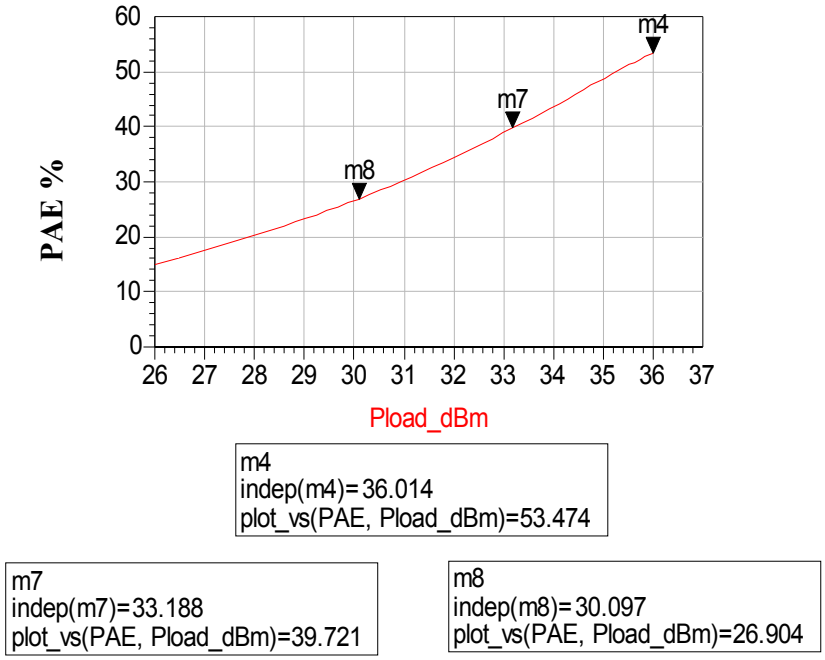

Fig 5.13 **Class AB: Plot of PAE(%) vs. Output Power (dBm)**

The gain plots for Class F and Class AB amplifiers shown in Figures 5.14 and 5.15 respectively show the improvement in gain that is achieved using the Class F design. The Class F gives a gain 1 dB higher than the Class AB counterpart.

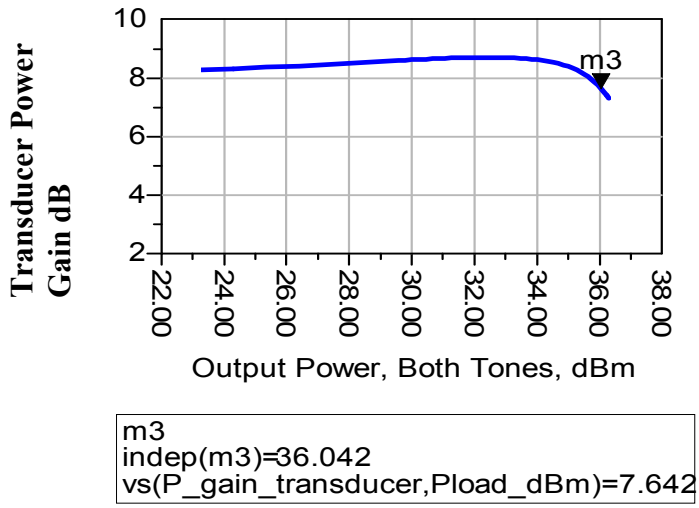

Fig 5.14 **Class F: Plot of Gain (dB) vs. Output Power (dBm)**

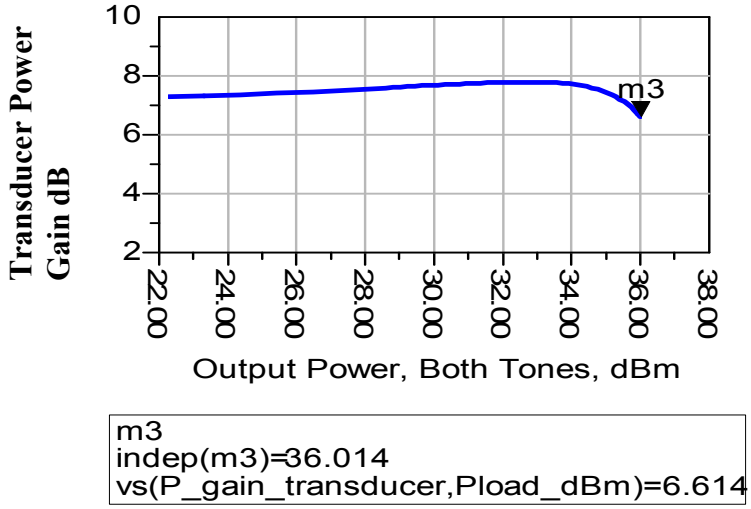

Fig 5.15 **Class AB: Plot of Gain (dB) vs. Output Power (dBm)**

Table 5.5 summarizes the performance of the Class F and Class AB amplifiers.

Performance Parameter	**Class F Performance**	**Class AB Performance**
Input Power P_{in} (dBm)	28.4	29.4
Output Power P_{out} (dBm)	36	36
Gain (dB)	7.6	6.6
Power Added Efficiency @ maximum output power (%)	60.5	53.5
Power Added Efficiency @ 6 dB back-off from maximum output power (%)	30.8	26.9
DC Power P_{dc} (Watts)	6.6	7.5
Thermal Dissipation (Watts)	2.6	3.5
IMD3 @ maximum output power (dBc)	-21.8	-21
IMD3 @ 6 dB back-off from maximum output power (dBc)	-35.6	-35.3
IMD5 @ maximum output power (dBc)	-32.4	-32
IMD5 @ 6 dB back-off from maximum output power (dBc)	-55	-52
IIP3 (dBm)	36.5	36.5

Table 5.5 **Comparison of Class F and Class AB PA performance**

5.5 Conclusion

Various simulations and tests were conducted on the designed Class F PA. A conventional Class AB design was also tested to compare the performance of the Class F PA. The Class F amplifier gives an efficiency of 60%, delivering 36 dBm of power at the output while matching the linearity performance of the Class AB amplifier. Hence a Class F power amplifier is found to be the best design choice for a WCDMA base station power amplifier.

Chapter 6

Conclusions

6.1 Summary

A Class F power amplifier was designed using Motorola's LDMOS transistor model to operate in the WCDMA band. The idea was to use a Class F amplifier biased as a Class AB amplifier. The Class F amplifier would provide a higher efficiency than achievable with a Class AB amplifier. However, as the Class F bias is the same as the Class AB amplifier, linearity is not compromised.

In this thesis, conventional PA types such as Class A, AB, B and C amplifiers and newer high efficiency PA such as the Class E amplifier were discussed. Following this, the operation of a basic Class F power amplifier and the factors affecting its performance was discussed. Later, the third harmonic peaking Class F amplifier was explained and the maximum efficiency, output power and power output capability of the amplifier was derived.

Based on this background, a third harmonic peaking Class F power amplifier was designed. This included the selection of optimum bias points, design of input and output matching networks and the design of appropriate harmonic terminations. A Class AB amplifier was also designed using the same bias and input and output matching. The Class F performance was compared to the performance of this Class AB amplifier.

6.2 Conclusion

The research has proven by means of simulation, the feasibility of using a Class F amplifier for WCDMA applications by achieving an efficiency of 60% with very good linearity. This thesis work provided the opportunity the make some important contributions in this field of research. The idea of using Class F amplifiers to improve efficiency without degrading linearity is relatively new and prior to this there has been no significant published work which focuses on Class F amplifiers for WCDMA applications. However, all of the results published in this thesis were those obtained by means of CAD simulation. Actual performance of the designed amplifier may vary significantly.

6.3 Future Work

This thesis work presents lot of scope for further research and development. It would be worthwhile to explore the following to build on this thesis work.

- Perform adjacent channel power measurements to evaluate the effect of non-linearity on adjacent channels.
- Building the circuit and measuring the actual performance of the power amplifier. Depending on how it compares with the simulated results, modifications should be done to the design to improve its performance. Due to the losses associated with components in real life, the power amplifier design typically requires few trials.
- Realizing the third harmonic and, if possible, the second harmonic traps using on-chip components. Since most of the present day designs focus on single chip solutions, this would be a logical extension. Furthermore, this would also result in significant reduction in costs. However, this may be extremely difficult to realize due to the parasitic effects at high frequencies (especially in the harmonic frequencies).

References

[1] UMTS Forum, http://www.umts-forum.org/

[2] 3G Americas, http://www.3gamericas.org/

[3] M. Albulet, *RF Power Amplifiers*, Noble Publishing, Atlanta, GA, 2001.

[4] S.C. Cripps, *RF Power Amplifiers for Wireless Communications*, Artech House, Norwood, MA, 1999.

[5] H.L. Krauss, C.W. Bostian and F.H. Raab, *Solid State Radio Engineering*, John Wiley & Sons, New York, NY 1980.

[6] R. S. Narayanaswami, Design of a 1.9 GHz, 250 mW CMOS Power Amplifier for DECT, *Master's Thesis Report*, 1998.

[7] N. Sokal and A. Sokal, Class E-A New Class of High-Efficiency Tuned Single Ended Switching Power Amplifiers, *IEEE Journal of Solid State Circuits,* Vol. SC10, June 1975, pp. 168-76.

[8] V.J. Tyler, A new high-efficiency high power amplifier, *Marconi Review,* vol. 21, 1958, pp. 96-109.

[9] D.M. Snider, A theoretical analysis and experimental confirmation of the optimally loaded and overdriven RF power amplifiers, *IEEE Transactions on Electron Devices*, ED-14, 1967, pp. 851-857.

[10] F.H. Raab, Class-F power amplifiers with maximally flat waveforms, *IEEE Transactions on Microwave Theory and Techniques,* Vol. 45, 1997, pp. 2007-2012.

[11] P.Colantonio, F.Giannini, G.Leuzzi, E.Limiti, On the Class-F Power Amplifier Design, *International Journal on RF and Microwave Computer Aided Engineering,* Vol.9, No.2, March 1999, pp.129-149

[12] P.Colantonio, F.Giannini, G.Leuzzi, E.Limiti, Theoretical Facets and Experimental Results of Harmonic Tuned PAs, *International Journal on RF and Microwave Computer Aided Engineering,* Vol.13, June 2003, pp.459-472

[13] F.H. Raab, Introduction to class-F power amplifiers, *RF Design,* Vol.19, May 1996, pp. 79-84.

[14] F. H. Raab, FET power amplifier boosts transmitter efficiency, *Electronics,* Vol. 49, No. 12, pp. 122 - 126, June 10, 1976.

[15] P.Colantonio, A.Ferrero, F.Giannini, E.Limiti and V.Teppati, Harmonic Load/Source Pull Strategies for High Efficiency PA Design, *IEEE MTT Symposium Digest,* 2003, pp. 1807-1810

[16] C. Duvanaud, S. Dietsche, G. Pataut, and J. Obregon, High-efficient Class F GaAs FET amplifiers operating with very low bias voltages for use in mobile telephones at 1.75 GHz, *IEEE Microwave Guided Wave Letters,* Vol. 3, 1993, pp. 268-270.

[17] C. Trask, Class-F Amplifier Loading Networks - A Unified Design Approach, *Proceedings of the 1999 IEEE International Symposium on Microwave Theory and Techniques,* Anaheim, California, June 1999.

Vita

Muthuswamy Venkataramani was born on December 21, 1979 in Madras, India. He obtained his undergraduate degree in Electronics and Instrumentation Engineering from the University of Madras. He then moved to United States of America to pursue his graduate studies. He joined the Electrical Engineering Department at Virginia Tech in Blacksburg, Virginia. During this time, he worked at the Center for Wireless Telecommunications at Virginia Tech as a research assistant, focusing on RF front-end design and power amplifier design. He also served as a teaching assistant for the radio engineering courses taught at Virginia Tech.

He spent the summer of 2002 at Motorola, as an intern, working in their Wireless Infrastructure Systems Division. He was evaluating commercial hybrid couplers for use in base station transmitters.

Muthuswamy will have completed the requirements for the degree of Master of Science in Electrical Engineering in May 2004. After graduation, he will join Motorola's Personal Communications Sector and work in their 3G Product Development Group in Libertyville, Illinois as a Senior RF Engineer.