High Frequency, High Power Density GaN-Based 3D Integrated POL Modules

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Abstract

The non-isolated POL converters are widely used in computers, telecommunication systems, portable electronics, and many other applications. These converters are usually constructed using discrete components, and operated at a lower frequency around 200 ~ 600 kHz to achieve a decent efficiency at the middle of 80's%. The passive components, such as inductors and capacitors, are bulky, and they occupy a considerable foot-print. As the power demands increase for POL converters and the limited real estate of the mother board, the POL converters must be made significantly smaller than what they have demonstrated to date. To achieve these goals, two things have to happen simultaneously. The first is a significant increase in the switching frequency to reduce the size and weight of the inductors and capacitors. The second is to integrate passive components, especially magnetics, with active components to realize the needed power density.

Today, this concept has been demonstrated at a level less than 5A and a power density around 300-700W/in^3 by using silicon-based power semiconductors. This might address the need of small hand-held equipment such as PDAs and smart phones. However, it is far from meeting the needs for applications, such as netbook, notebook, desk-top and server applications where

tens and hundreds of amperes are needed.

After 30 years of silicon MOSFET development, the silicon has approached its theoretical limits. The recently emerged GaN transistors as a possible candidate to replace silicon devices in various power conversion applications. GaN devices are high electron mobility transistors (HEMT) and have higher band-gap, higher electron mobility, and higher electron velocity than silicon devices, and offer the potential benefits for high frequency power conversions. By implementing the GaN device, it is possible to build the POL converter that can achieve high frequency, high power density, and high efficiency at the same time. GaN technology is in its early stage; however, its significant gains are projected in the future. The first generation GaN devices can outperform the state-of-the-art silicon devices with superior FOM and packaging.

The objective of this work is to explore the design of high frequency, high power density 12 V input POL modules with GaN devices and the 3D integration technique. This work discusses the fundamental differences between the enhancement mode and depletion mode GaN transistors, the effect of parasitics on the performance of the high frequency GaN POL, the 3D technique to integrate the active layer with LTCC magnetic substrate, and the thermal design of a high density module using advanced substrates with improved thermal conductivity.

The hardware demonstrators are two 12 V to 1.2 V highly integrated 3D POL modules, the single phase 10 A module and two phase 20 A module, all built with depletion mode GaN transistors and low profile LTCC inductors.

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Table of Contents

List of Figures

List of Tables

Chapter 1. Introduction

1.1. Background of Point of Load (POL) Converters

The Point of Load (POL) converters are becoming more and more common in everyday life; the range of applications is from the small handheld electronics like smart phones, GPS to the laptop and desktop, to the large size systems like telecom and server as shown in Fig. 1.1. These POL converters convert from a 3.3 V, 5 V or 12 V power rail down to a processor core voltage. As the Moore's law predicted, the speed and transistors counts of the processor have grown significantly, the power demands of the processor also have been increased significantly [1][2].

Fig. 1.1: Applications for POL converters.

In 1997, CPES proposed the multi-phase voltage regular (VR) to power the new generation

of microprocessors with improved efficiency, transient performance, and power density [3][4][5]. Today's every processor is powered with one of these multi-phase VR's. The design is scalable with each phase providing a 15-25A current. The number of phases (modules) increased from 1 to 8-10 phases since the microprocessor can demand up to 180A current. These VRs are mostly constructed with discrete components and built on the motherboard. In order to achieve a circuit efficiency at the mid-80's%, the circuit is operated at a lower frequency around 200-600 kHz. The passive components such as inductors and capacitors are bulky. They occupy a considerable foot-print on the motherboard. Fig. 1.2 shows a server motherboard with lots of VRs populated on board. These VRs occupy about 30% of footprint of the motherboard.

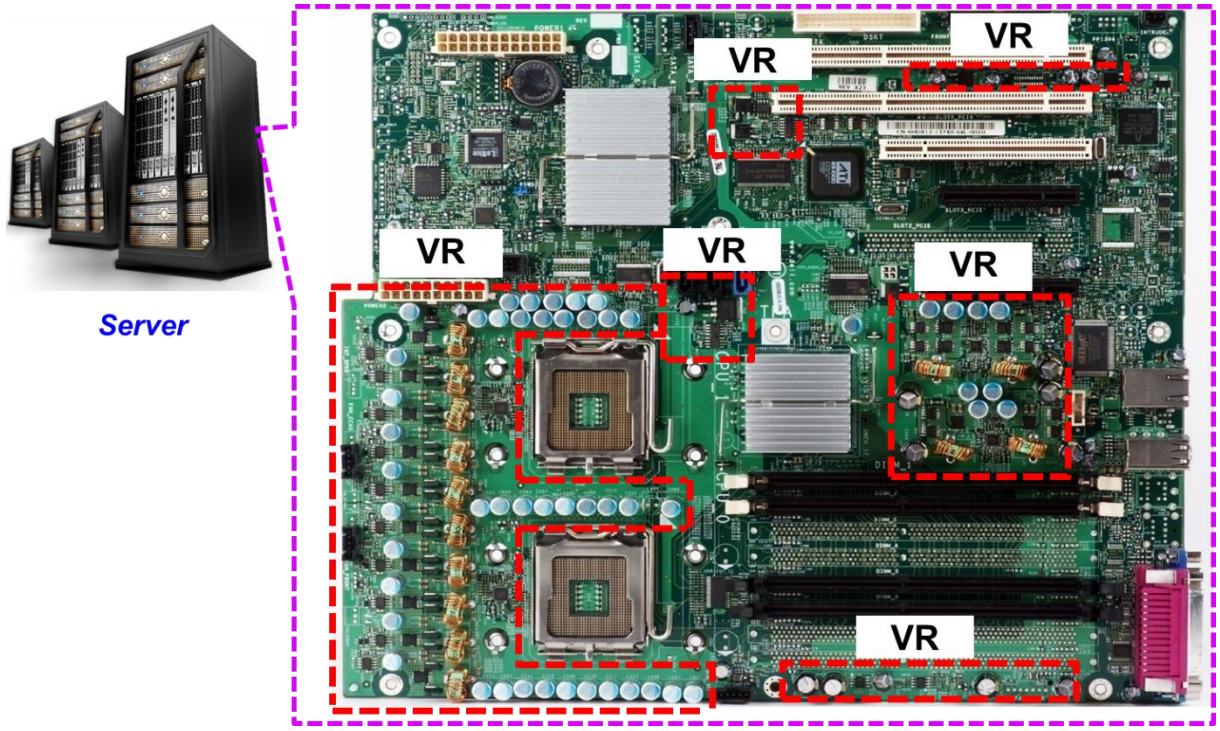


Fig. 1.2: Server motherboard with VRs on board

With the current trend of reducing the size of all forms of portable computing equipment from notebook to netbook, increasing functionalities of PDA and smart phones, as well as the

increasing use of cloud computing instead of a more traditional network based computing, the high power density, high efficiency VRs are demanded.

Recently, the industry leaders such as IBM and Cisco are promoting the idea of replacing these embedded VR solutions with plug-in modules, namely "power blocks" to save the motherboard real estate for other critical functions. Fig. 1.3 shows the power blocks products from GE and Delta Electronics Inc. that cover the current range from 3 A to 40 A. These power blocks contain all necessary power components, such as power MOSFETs and drivers, input/output capacitors, output inductor. They are designed to work with either digital or analog controllers located on the mother board to provide maximum flexibility for system configuration.

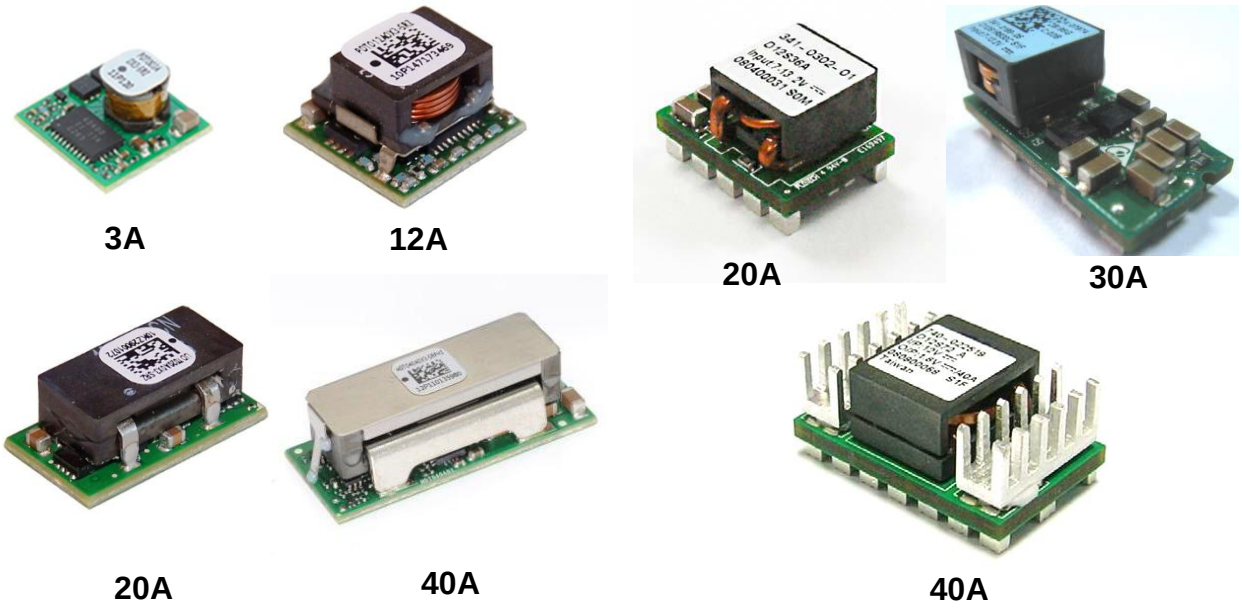


Fig. 1.3: Power blocks from (a) GE and (b) Delta Electronics

However, these power blocks are all working in around 400 KHz ~ 500 kHz range. The magnetic component occupies significant amount of volume, limits the power density. To

address the future demand of high power density power modules, these “power blocks” must be made significantly smaller than they have been demonstrated to date. To achieve these goals two things have to happen simultaneously, one is a significant increase in the switching frequency to reduce the size and weight of the inductors and capacitors. The second is to integrate passive components, especially magnetics, with active components to realize the needed power density [6][7][8][9].

1.2. State-of-the-art POL Modules

Today’s POL modules include three types as shown in Fig. 1.4. The first type is the integrated POL using silicon-based power semiconductors which addresses the need of small hand-held equipment such as PDAs and smart phones. The power density can achieve 700 ~ 1000 W/in^3. However the current is usually less than 6A. The second type is co-packaged POL module using bare dies of power device and driver, packaged with discrete inductor and capacitors. The co-packaged POL converter can provide 5 ~ 20A output current with the power density is around 200 ~ 500 W/in^3. The third type is the discrete POL module which is built with all discrete components on a PCB board. These modules cover the output current range of 5 ~ 40 A with a much lower power density of 50 ~ 200 W/in^3.

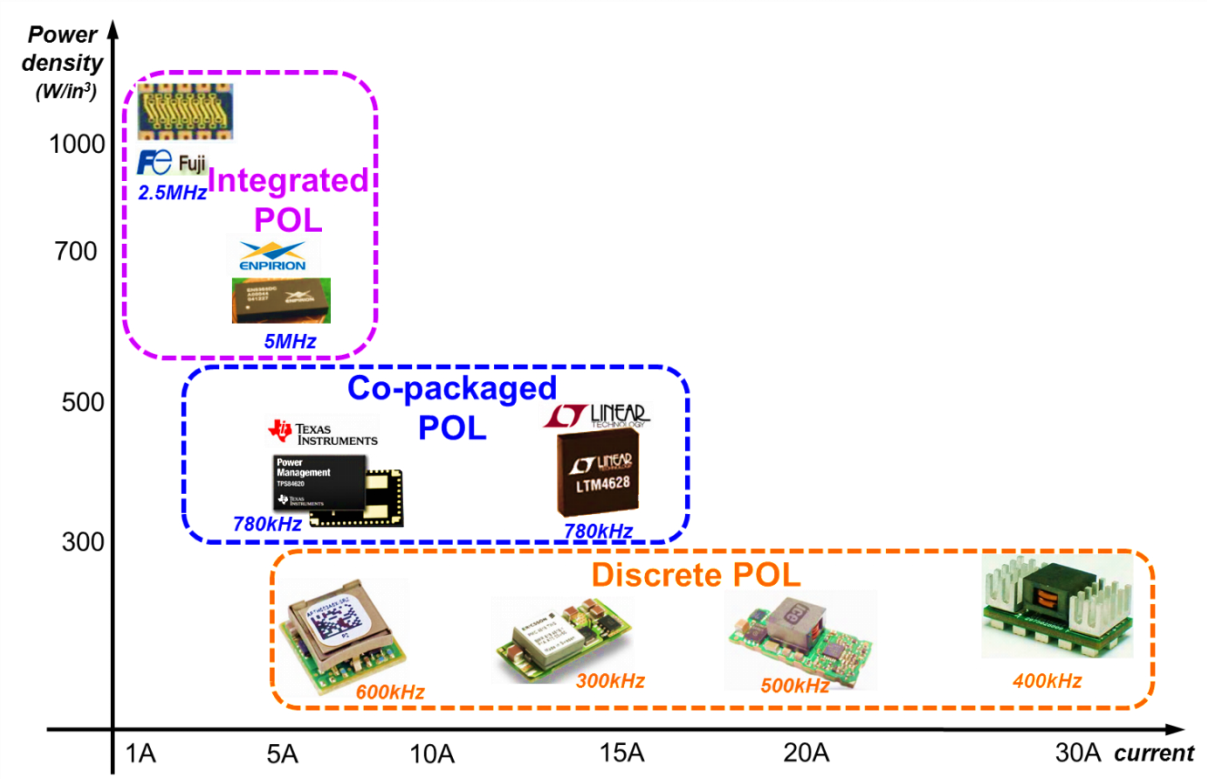


Fig. 1.4: Power densities of today's POL modules

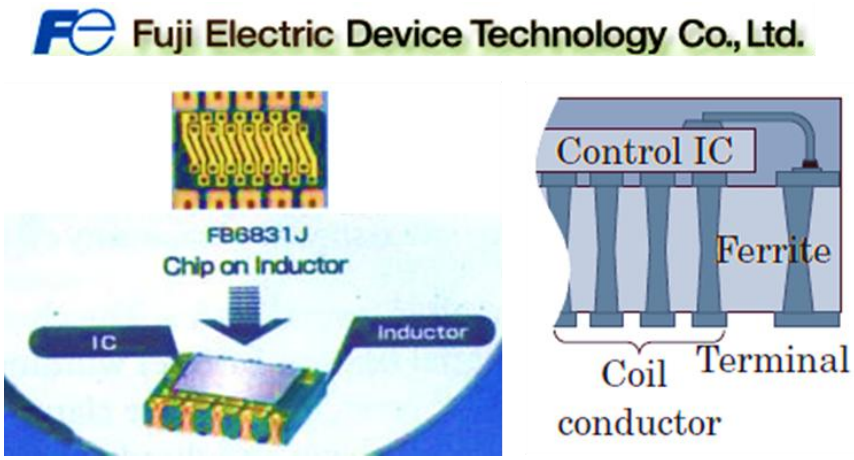
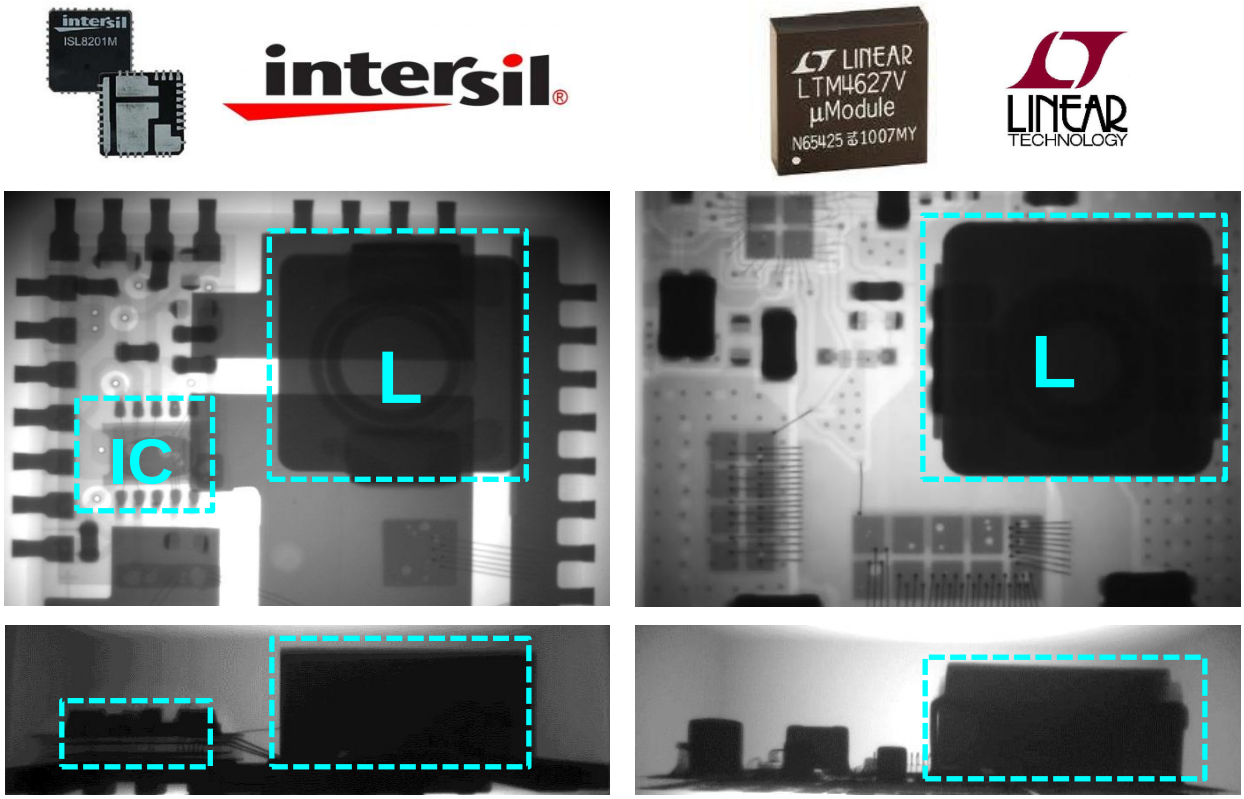


Fig. 1.5: Fuji FB6831J integrated POL module

Fig. 1.5 shows a fully integrated POL module from Fuji Electric Device Technology Co., Ltd., with 5 V input voltage and 500 mA output current [10]. It is built with a silicon control IC on a ferrite inductor. The operation frequency is 2.5 MHz, which makes possible for the inductor to be small enough to be placed on the back of IC as a substrate, which is defined as 3D

integration.



(a) Intersil ISL8201M (b)Linear LTM4627

Fig. 1.6: X-ray images for co-packaged POL modules

Fig. 1.6 shows the X-ray images for two 12 V input co-packaged POL modules with higher output current. Fig. 1.6(a) is Intersil's ISL8201M POL module with 10 A output current, at 600 kHz operation frequency [11]. Fig. 1.6(b) is Linear Technology's LTM4627 POL module with 15 A output current, at 780 kHz maximum operation frequency [12]. In these modules, the active bare dies are wire bonded to the substrate; the discrete inductor is placed next to the silicon dies. The inductor still has large physical size which impacts the module's power density, due to the relative low operation frequency.

At higher current level, the POL modules are usually built with all discrete components and

operating at much lower frequency. Fig. 1.7 shows a 12 V/ 20 A discrete POL module from Delta Electronics, INC [13]. With a 500 kHz operation frequency, it requires a large size inductor; therefore, its power density is less than 200 W/in^3.

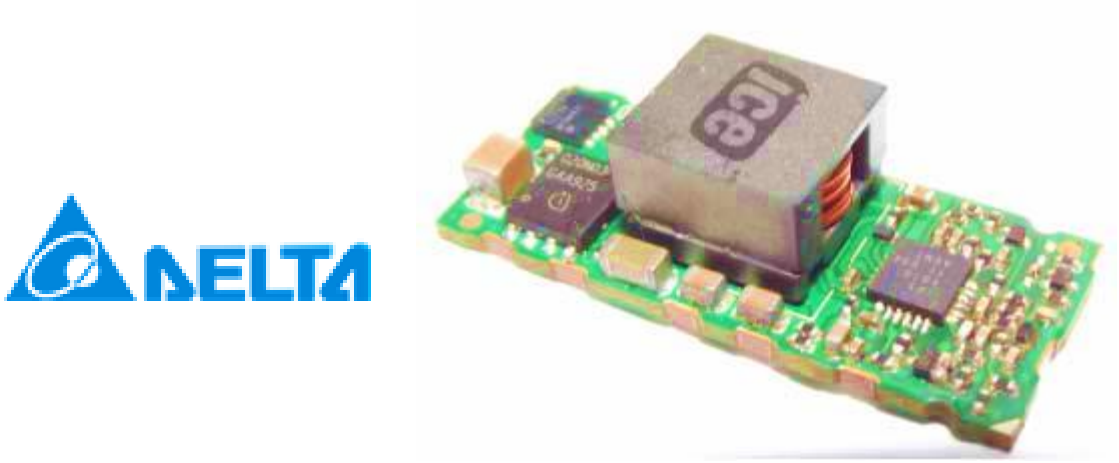


Fig. 1.7: Delta DCL12S0A0S20NFA discrete POL module

In a sum, the integrated POL module has the highest operation frequency, significantly reduces the size of passive components; hence it has the highest power density. However the output current is low. The co-packaged POL module increases the output current; however, the power density suffers from the discrete inductor. The discrete POL module has the highest output current, but the lowest power density because of its all discrete structure.

The objective of this thesis is to design the high current, high efficiency 12 V input POL modules, with 3D integration of the output inductor to increase the power density.

1.3. 3D Integrated POL Module

In order to penetrate the barrier to high power density which can be seen in the co-packaged

modules, in Fig. 1.6(a) and 1.6(b), the modules volume is dominated by the discrete inductor. The 3D integration approach should be considered to improve the module power density [16][17]. As shown in Fig. 1.8, the concept of 3D integration is to integrate the active layer on the low profile inductor substrate to produce a small footprint, low profile vertical structure solution. The 3D integration allows for footprint saving and full space utilization, which significantly increases the converter's power density.

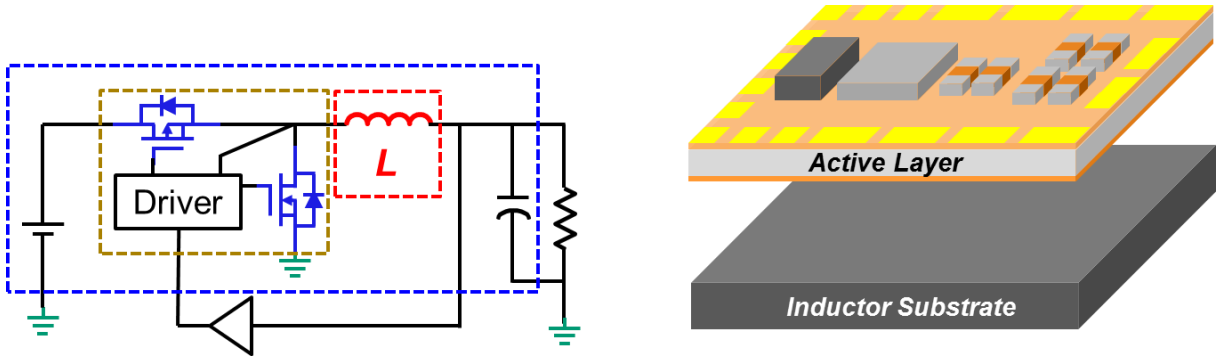


Fig. 1.8: Concept of 3D integration

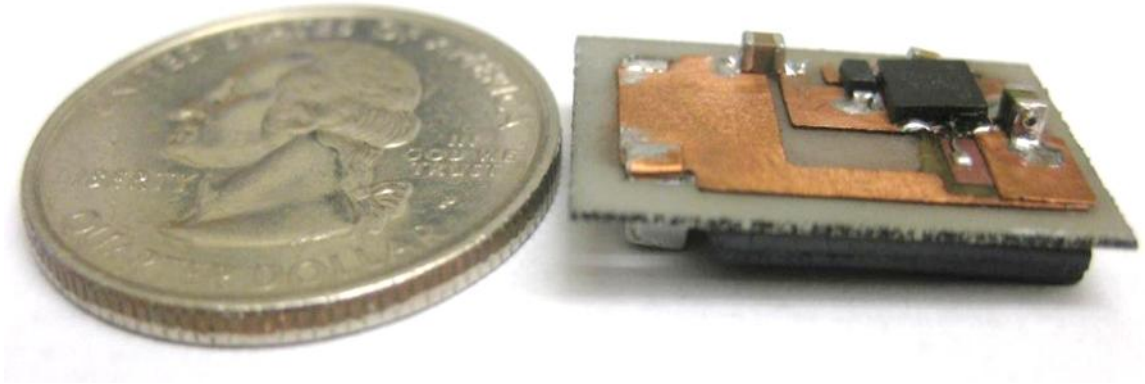
(a) (b)

Fig. 1.9: Industry 3D integrated POL modules from (a) Ti and (b) Enpirion

This 3D integrated concept has been adopted by few industry companies. Fig. 1.9 shows the 3D integrated POL modules from Ti and Enpirion [14][15]. With the 3D integration technique,

these products have high power density. However, the output current of these products are all less than 5 A. Output current level has to be pushed to meet the increasing power demands.

Lots of practices of 3D integrated POL modules have been demonstrated in CPES [16][17]. Fig. 1.10 shows a 3D integrated high power POL module developed in 2004. The active layer was built by MOSFET dies, driver, and control IC that mounted on the AlN substrate. The AlN DBC substrate is employed as the die holder to improve the active stage thermal conductivity and module thermal performance. The LTCC inductor with the silver paste winding is adopted for the low profile inductor substrate. This POL module worked at 1.5 MHz operation frequency. The maximum output current is 15 A for a 5 V to 1.2 V conversion, the power density can achieve 300 W/in^3.

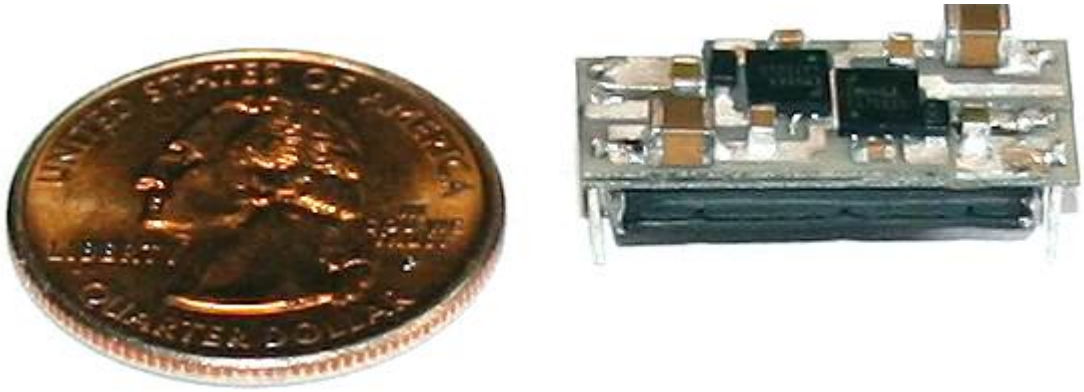


Ref: *Qiang Li, Fred C. Lee, "High Inductance Density Low-Profile Inductor Structure for Integrated POL Converter" APEC 2009.*

Fig. 1.10: CPES 3D integrated POL converter

In 2008, a further improvement in power density was realized by implementing the inverse coupled two phase inductor [18]. The inverse-coupled LTCC inductor can save 50% of the footprint comparing with a non-coupled inductor. With 1.5 MHz operation frequency and 40A output current, this integrated LTCC vertical-flux-coupled inductor POL converter module

achieves 500W/in^3 power density as shown in Fig. 1.11. All these modules have an order of magnitude higher current than the industry products.



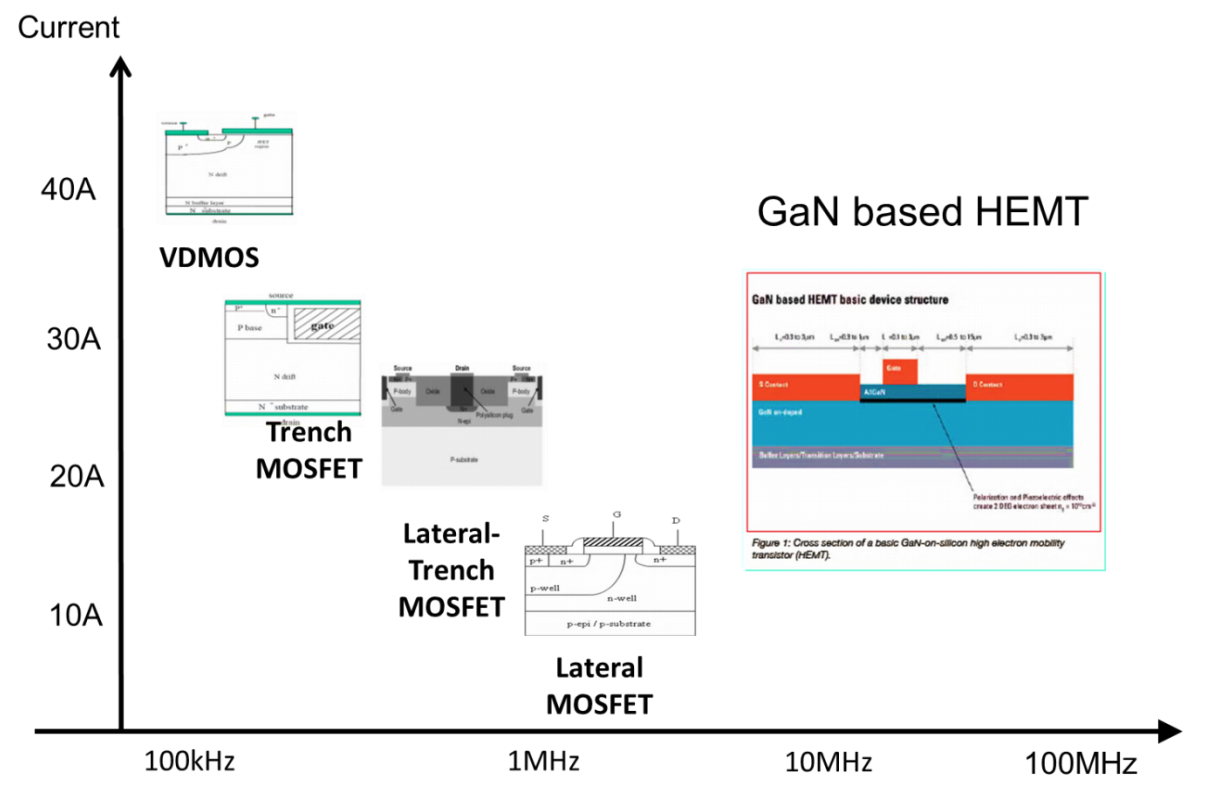
Ref: *Yan Dong, "Investigation of Multiphase Coupled-Inductor Buck Converters in Point-of-Load Applications", PhD. Dissertation, 2009.7*

Fig. 1.11: CPES two phase 3D integrated POL converter with coupled inductor

Although these 3D integrated POL converters improved the output current and power density, the input voltage and the maximum operation frequency were limited by the performance of Silicon devices. In order to keep pushing the operation frequency and power density, new technology has to be adopted to replace the Silicon devices.

1.4. Gallium Nitride (GaN) Transistor

In the past decades, MOSFETs have become the power device of choice for many applications. From planar HEXFETs to Trench FETs and super junction FETs, silicon based MOSFETs have made a dramatic improvement in figures of merit (FOMs) to effectively serve in a variety of applications.



Ref: *Yucheng Ying, "Device selection criteria----based on loss modeling and Figure of Merit", Thesis of MS, 2008.*

Fig. 1.12: Semiconductor device technologies

Fig. 1.12 shows the operation frequency and current range for different power device technologies. The VDMOS is usually used for applications with a voltage greater than 30 V. For the low voltage applications, Trench MOSFET and lateral MOSFET are two widely used silicon devices. For the 30 V applications, the Trench MOSFET is a more popular choice because it is usually operating at less than 600 kHz with 25A current. The lateral MOSFET is more suitable for lower voltage (< 20 V) and lower current (< 10 A) applications and it is capable of running at a higher frequency (> 1 MHz) [19][20]. In 2007, Ti introduced the lateral trench MOSFET where it can be best used at a voltage range from 15V to 25V and a current level similar to a trench MOSFET. Its FOM is almost half of today's best trench MOSFET. This newcomer, lateral-trench

MOSFET has some potential to fill this application gap between lateral and trench devices. However, none of these devices is suitable for higher frequency (>5MHz), higher current, and high buck ratio applications. In order to achieve higher power density with an operating frequency approaching 5-10MHz and a current reaching 20-40A level, a new device has to be developed with a significant improvement in its figure of merit.

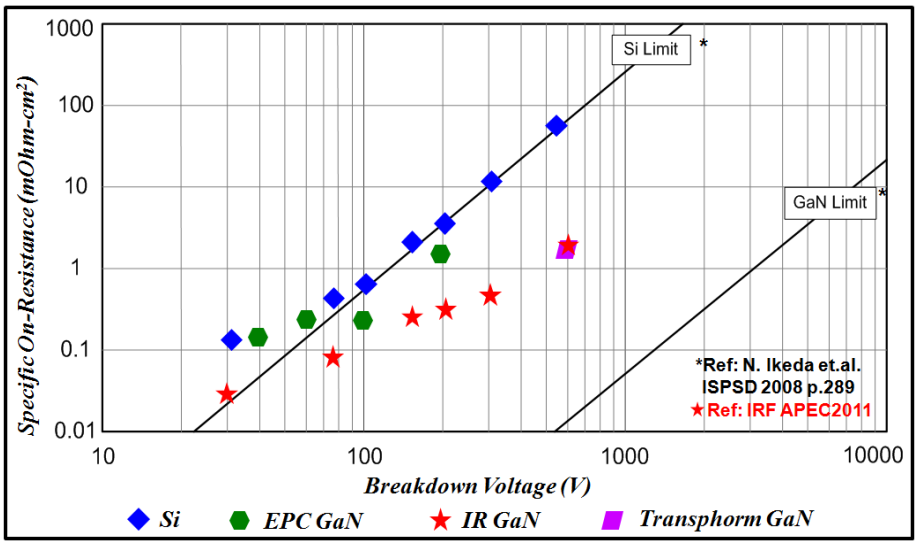
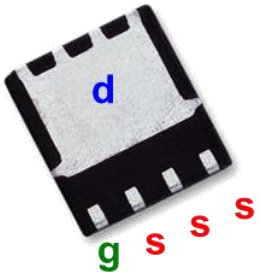


Fig. 1.13. Comparison of Si and GaN specific on resistances.

The recently emerged GaN transistors, as a possible candidate to replace silicon devices in various power conversion applications. GaN devices are high electron mobility transistors (HEMT) and have higher band-gap, higher electron mobility, and higher electron velocity than silicon devices, and offer the potential benefits for high frequency power conversions. By implementing the GaN device, it is possible to build the POL converter that can achieve high frequency, high power density, and high efficiency at the same time. GaN technology is still in its early stage; however, its significant gains are projected in the future as shown in Fig.1.13 [23].

The first generation GaN devices can outperform the state-of-the-art silicon devices with superior FOM and packaging.

Table 1.1: Parameters comparison between GaN and Silicon devices

	 **EPC 1015 40V Enhancement GaN**	 **PowerFLAT 5x6** **40V Silicon**
Rds(on) (mΩ) @Vgs = 5V	3.2	3.1
Qg (nC)	10.5	45
Qgd (nC)	2.2	14
Ciss (pF)	1100	5900
Coss (pF)	575	870
VGS (V)	-5 ~ +6	-20 ~ +20

The parameters for the state-of-the-art ST Microelectronics 40V silicon MOSFET [21] and the first generation 40V enhancements GaN transistor are compared in Table 1.1. Both devices have similar Rds(on). However, the GaN transistor only has ¼ of footprint of Silicon MOSFET. The Qg, Qgd, Ciss, and Coss of GaN transistor are much lower than the Silicon MOSFET; therefore, GaN transistor is suitable for high frequency operation.

1.5. Thesis Outline

This thesis mainly focuses on exploring the high efficiency, high power density POL

modules design. The GaN transistors are utilized to push to high operation frequency, reduce the passive components size; the active layer and LTCC inductor substrate are 3D integrated to improve the power density.

Chapter 1 gives an introduction of the research background.

Chapter 2 gives an introduction of the current GaN technologies, the advantages and limitations of depletion mode and enhancement mode GaN transistors, and considerations of utilizing the GaN transistors in high frequency POL converter design. It also addresses driving the GaN transistors, the dead-time loss for the GaN-based buck converter, the maximum operation frequency, and the impact of the package and layout parasitics.

Chapter 3 discusses the module structure design, the method of reducing layout parasitics, the shield layer implementation, the PCB substrate design, thermal management with advanced DBC substrate, the integration of the low profile LTCC magnetic substrate, and the two phase interleaved module design.

Chapter 4 provides the thermal cycling test and thermal performance evaluation results for the designed GaN POL modules.

Chapter 5 provides a summary of this thesis and proposes some future work.

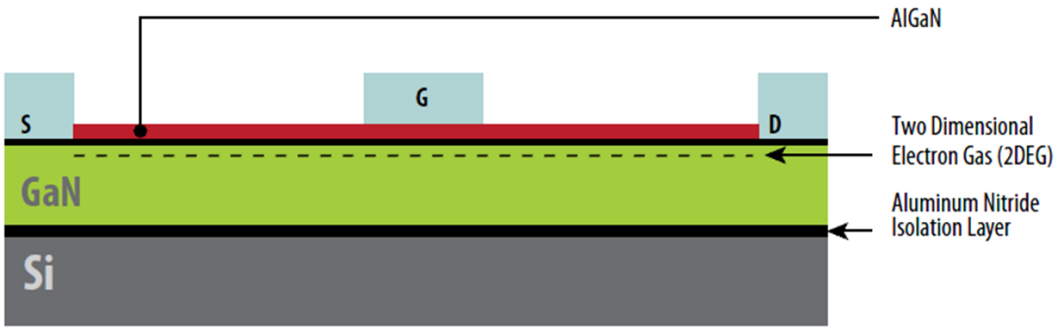
Chapter 2. Utilizing GaN Transistors in High Frequency POL Converter Design

The GaN transistor offers the capability of high frequency operation while maintaining the high efficiency. Currently, for low voltage point of load application, there are two types of GaN transistors available on the market: the depletion mode GaN transistors from International Rectifier (IR) [22], and the enhancement mode GaN transistors from Efficient Power Conversion Corporation (EPC) [23]. This chapter will give an introduction for the current GaN technologies, the advantages and limitations of these two types of GaN transistors, and considerations of utilizing the GaN transistors in high frequency POL converter design. It will also address driving the GaN transistors, the dead-time loss for the GaN-based buck converter, the maximum operation frequency, and the impact of the package and layout parasitics.

2.1. Depletion Mode and Enhancement Mode Low Voltage GaN Transistors

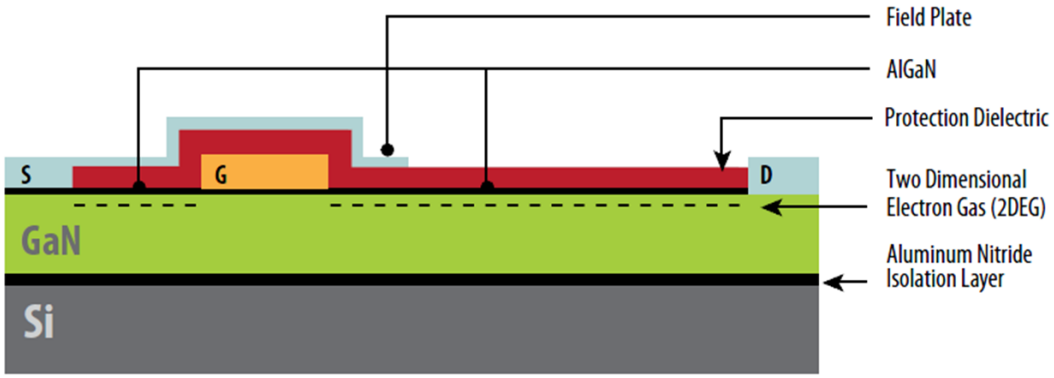
Both of depletion mode and enhancement mode GaN transistors are lateral devices. Fig. 2.1 and Fig.2.2 show the similar structures for these two devices [24]. In both of these two structures, a thin layer of Aluminum Nitride (AlN) is grown on the silicon substrate, and then GaN is grown on the AlN. An ultra-thin AlGaN layer is then grown on top of the highly resistive GaN. The interface between the GaN and AlGaN crystals layers creates a two dimensional electron gas

(2DEG) which is filled with highly mobile and abundant electrons [25]. The conduction channel between source and drain electrodes are formed with the underlying 2DEG. To turn off the channel, the electrons have to be depleted.



***Ref:* EPC "Gallium Nitride GaN Technology Overview"**

Fig.2.1: Structure for depletion mode GaN transistor.



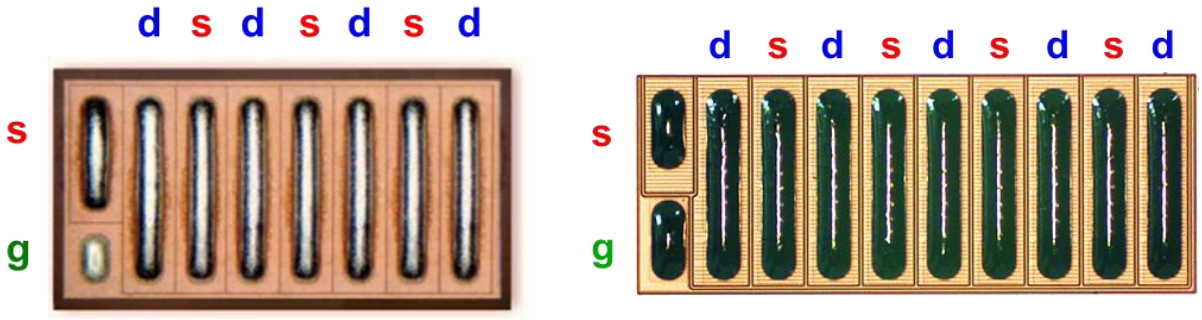
***Ref:* EPC "Gallium Nitride GaN Technology Overview"**

Fig.2.2: Structure for enhancement mode GaN transistor.

In depletion mode GaN transistor, a gate electrode is placed on top of the AlGaN layer in order to deplete the 2DEG. The gate electrode is formed as a Schottky contact to the top surface. When apply a negative voltage to this contact, the Schottky barrier becomes reverse biased and the electrons underneath are depleted. Therefore, in order to turn this device OFF, a negative voltage relative to both drain and source electrodes is needed.

In enhancement mode GaN transistor, the gate electrode is designed to form a depletion region under the gate. Additional layers of metal are added to route the electrons to gate, drain, and source terminals. To turn on the FET, a positive voltage is applied to the gate in the same manner as turning on an n-channel, enhancement mode power MOSFET.

IR's depletion mode and EPC's enhancement mode GaN transistors have the same Linear Grid Array (LGA) package as shown in Fig. 2.3. The device is mounted as the bare die with the underneath metalized bumps. The drain and source pads are interleaved to minimized the parasitics.



(a) (b)

Fig.2.3: LGA package for (a) IR depletion mode and (b) EPC enhancement mode GaN transistors.

The most noticeable difference between these two types of devices is that the enhancement mode GaN is a normally off device; it requires a positive voltage to turn on, whereas the depletion mode GaN is a normally on device; it requires a negative voltage to turn off.

Fig.2.4 shows the I-V curves for IR's 30 V depletion mode and EPC's 40 V enhancement mode GaN transistors. IR's GaN transistor is on with 0 V gate voltage; it needs a negative 3.3 V to turn off with the threshold voltage at -2 V [26]. The $R_{ds(on)}$ of this transistor is 2.5 mΩ, and the

figure of merit (FOM) is 30 mΩ•nC. EPC's 40 V GaN device requires a 5 V gate voltage to fully turn on, and 0V gate voltage to turn off with the threshold voltage at 1.4 V, The $R_{ds(on)}$ of this transistor is 3.2 mΩ, and the FOM is 40 mΩ•nC.

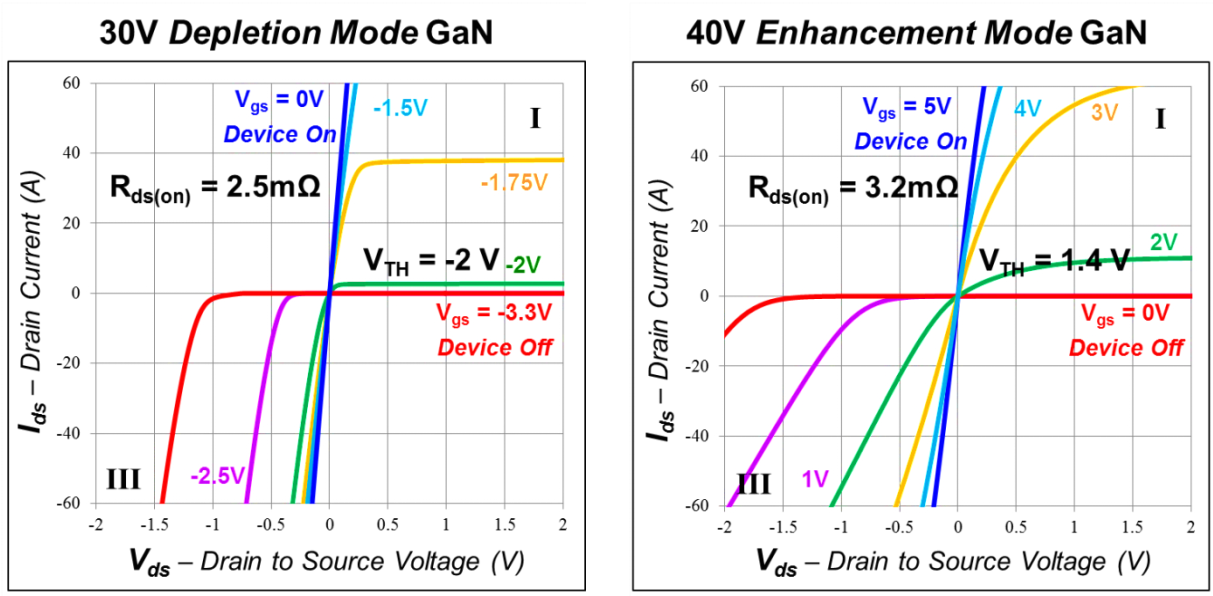


Fig.2.4: I-V characteristics for IR's 30V depletion mode and EPC's 40V enhancement mode GaN transistors.

From the I-V curves of these two devices, a different can be found between GaN transistors and silicon MOSFETs: when these devices working in the third quadrant, GaN transistors have higher reverse voltage than silicon MOSFETs. Usually the reverse voltage for silicon MOSFET is about 0.7 V, which is the forward voltage of body diode, this reverse will not change much with the increasing current. When comparing the depletion mode and enhancement mode GaN transistors, the reverse voltage is about 1.3 V for the depletion mode GaN transistor, it is smaller than enhancement mode GaN, which is about 1.4 V at no load, and 2 V at 10 A.

2.2. Driving GaN Transistors

Fig.2.5 shows the gate driving characteristics for IR's depletion mode transistor and EPC's enhancement mode transistor [27]. EPC's enhancement mode GaN transistor has a distinct property in the device: its maximum gate voltage limit is -5 to 6V. An over of this 6V limit will damage the device. However, this enhancement mode GaN is designed to achieve optimum performance with a gate drive voltage around 5V, which leaves an extremely tight margin for safe operation. Therefore, a careful gate driving design must be considered to limit the drive overshoot for the enhancement mode GaN transistors.

IR's depletion mode transistor has a maximum gate voltage from -10V to 6V. It does not encounter the over voltage issue since it is driven on at 0V, and driven off at -3.3V. There are plenty of margins for tuning on and off. Therefore, depletion mode GaN transistors offer a much safer driving than the enhancement mode GaN transistors.

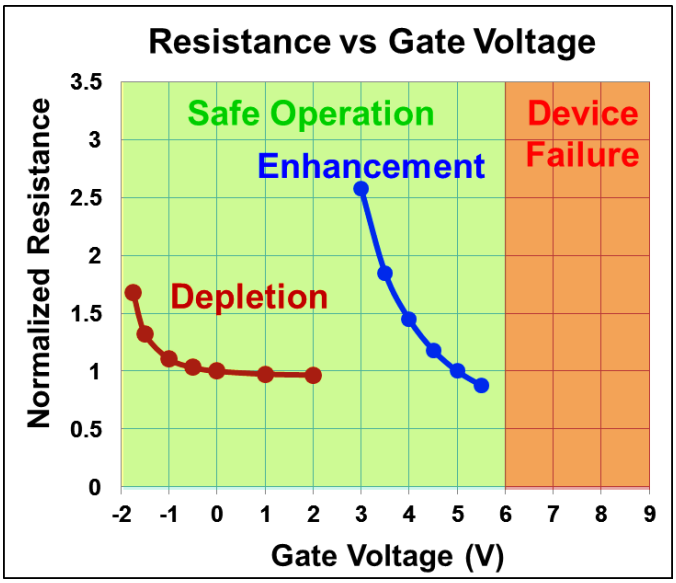


Fig.2.5: Gate driving characteristics of GaN transistors

Since there is an extremely tight margin for enhancement mode GaN transistor to be turned on, specific methods have to be implemented in the driving circuit. First of all, the power supply for the enhancement mode driver should be well regulated. For the silicon MOSFET, since the gate drive voltage is usually +/- 20V, the conventional bias power supply for silicon driver can come from a loosely cross-regulated transformer winding. However, it is not suitable anymore for the enhancement mode GaN transistor [28]. As shown in Fig.2.6, a 5V LDO should be implemented in the power supply circuit which can regulate the supply voltage from an available higher voltage rail, a transformer winding, or directly from the unregulated input voltage.

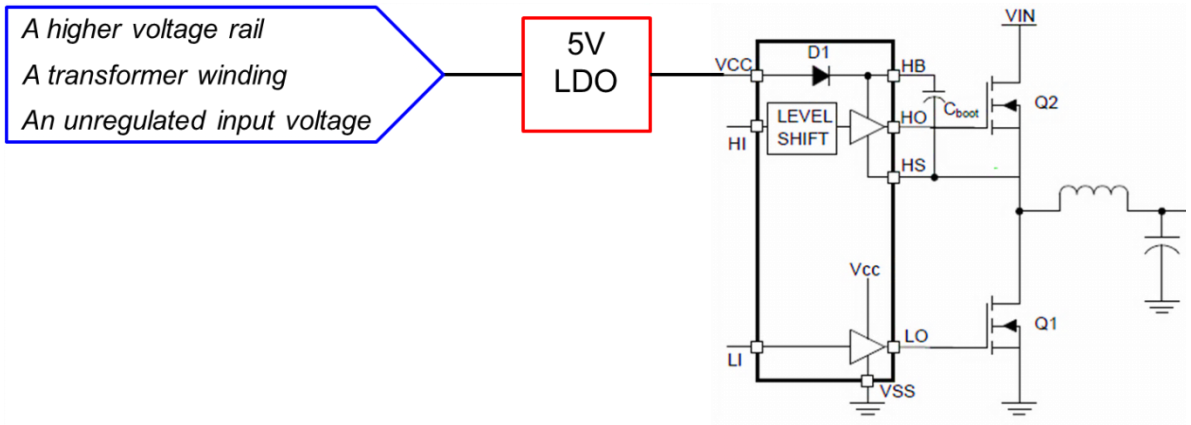


Fig.2.6: Power supply for enhancement mode GaN driver

The power dissipation for the LDO can be calculated from the below equations:

$$I_g = Q_g \times f_S \tag{2.1}$$

$$P_g = (V_{i\_max} - 5V) \times I_g \tag{2.2}$$

Where I_g is gate drive current, Q_g is the total gate charge, f_s is the operation frequency, and V_{i_max} is the input power supply voltage.

When driving enhancement mode GaN transistors, another problem is the high reverse drain-to-source voltage V_{sd}, and the reverse voltage increases with increasing current. When implementing the enhancement mode GaN transistor in a synchronous Buck or half-bridge converters, this high reverse voltage causes a serious problem in driving a high side GaN transistor. Fig. 2.7 shows the conventional gate drive circuit using the bootstrap technique to drive the high side FET in a buck converter. When the low side FET is turned on, the bootstrap capacitor is charged by V_{CC} via the bootstrap diode. Then, the charged bootstrap capacitor serves as the bias supply for the high side driver. This technique works well for driving silicon MOSFET, when this technique is applied to a GaN transistor, the bootstrap capacitor will be charged to a voltage V_{boot} which is mainly determined by:

$$V_{boot} = V_{CC} - V_F + V_{sd\_Q2} \tag{2.3}$$

Where V_{CC} is the driver bias supply voltage, V_F the forward voltage drop on the bootstrap diode, and V_{sd_Q2} is the low side FET reverse drain-to-source voltage. When V_{CC} is 5V, and V_F is 0.7V, since V_{sd_Q2} will increase quickly with the load current, the V_{boot} will also increase quickly to exceed the maximum 6V rating and damage the high side GaN transistor.

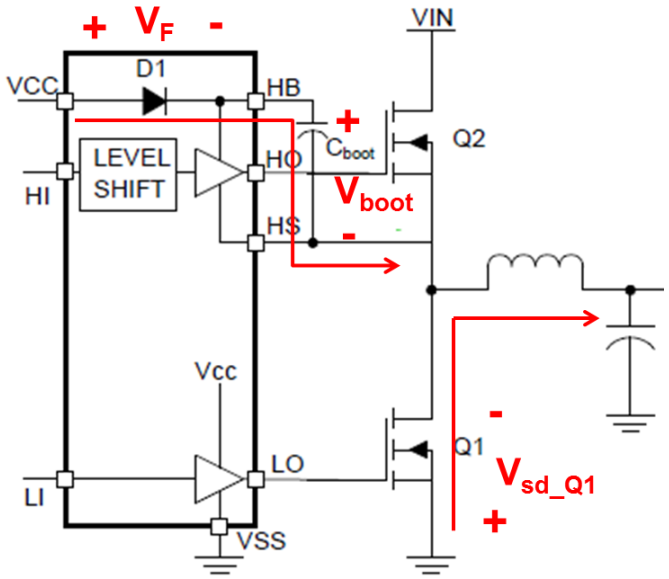


Fig.2.7: Bootstrap capacitor voltage for enhancement mode GaN driver

In some application, an external diode is added to parallel with low side GaN transistor, to reduce the reverse voltage. However, it is not an effective solution to prevent the driving problem, because charging the bootstrap capacitor completes in less than a few tens of nanoseconds. The lead inductance of the diode will significantly reduce its effectiveness of clamping the reverse drain-to-source voltage during this short period.

To overcome all these problems, the gate driver should be designed specifically for the enhancement mode GaN transistors. Fig. 2.8 shows the first released enhancement mode GaN transistor driver by Texas Instruments [29]. It has an internal gate drive voltage clamp block. The high side FET gate voltage is clamped at 5.2V to prevent the over voltage driving. In the meantime, the turn on resisters are built in the driver, to reduce the switching ringing. As shown in Fig. 2.9, increasing the gate resistance will reduce the gate voltage spikes to prevent overvoltage damage, however, the turn on resisters purposely slow down the switching speed.

The turn on time is 10 uS for 1.4 ohm gate resistance; it increases to 20 uS for 2.4 ohm gate resistance. Therefore, the maximum operation frequency is limited by the turn on resister.

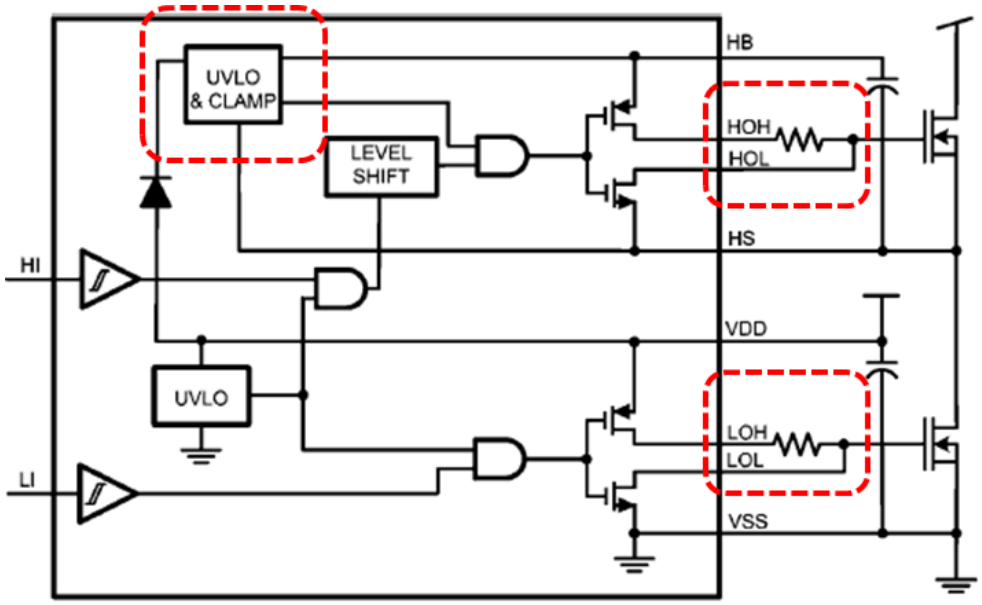
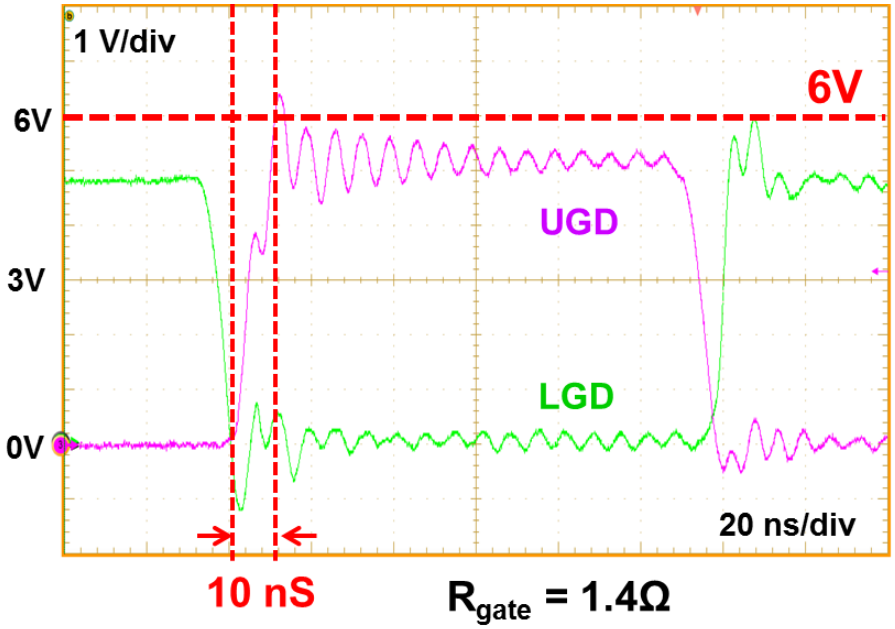


Fig.2.8: LM5113: first released enhancement mode GaN FETs gate driver



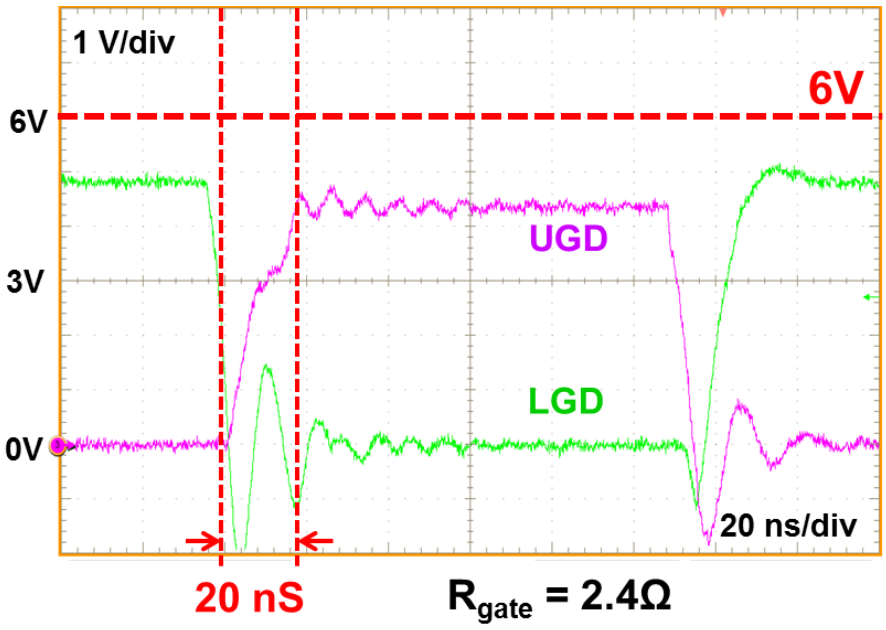


Fig.2.9: Gate signals with different gate resistance

Fig. 2.10 shows the block diagram for the depletion mode GaN driver. Since there is plenty of margins for driving the depletion mode GaN transistor, the driver does not need the voltage clamp block to prevent over voltage driving, neither the turn on resisters to slow down the turn on transition. As shown in Fig. 2.11, the turn on transition time is only 3 uS. The depletion mode GaN transistor switches much faster than the enhancement mode GaN transistor. That means the converter built with depletion mode GaN transistor can operate at higher frequency than the converter built with enhancement GaN transistor.

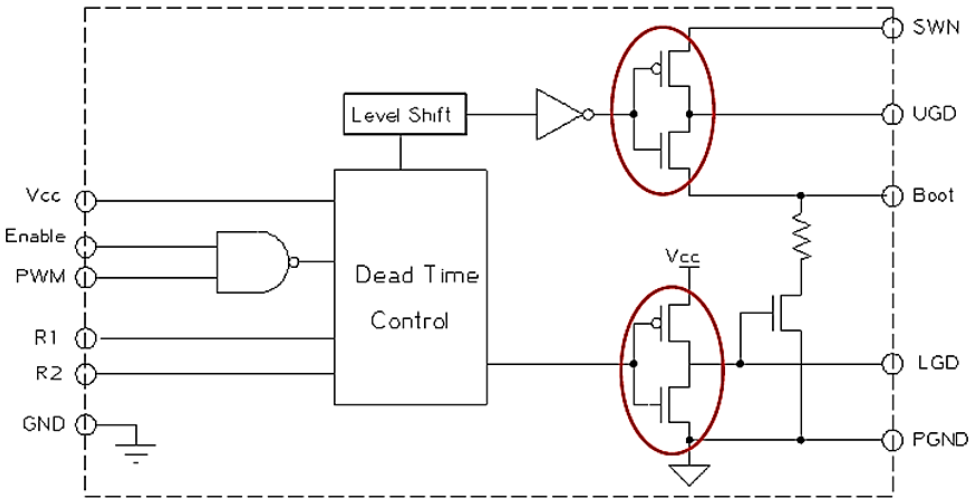


Fig.2.10: Driver block diagram for IR depletion mode GaN transistors

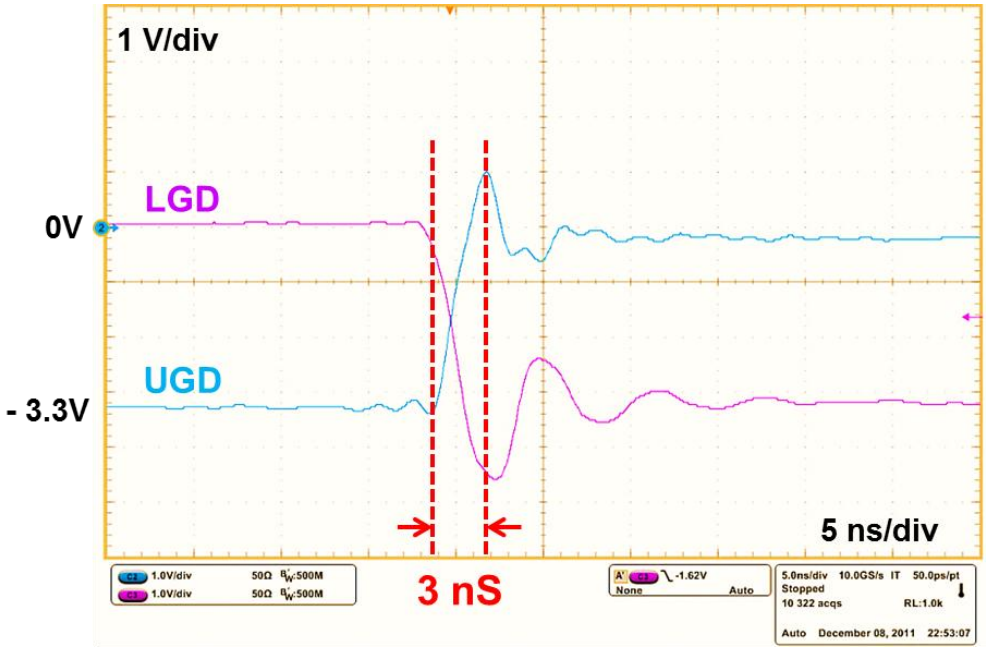


Fig.2.11: Gate drive signals for depletion mode GaN transistors

On the other hand, the depletion mode GaN transistor is a normally on device. When no drive signals applied to top and bottom GaN transistors, both of them are on, the input source is shorted through these two switches. To prevent the short through issue, a switch is usually placed in series of input source as shown in Fig. 2.12. This switch remains off until the drive signals have been applied to the GaN transistors.

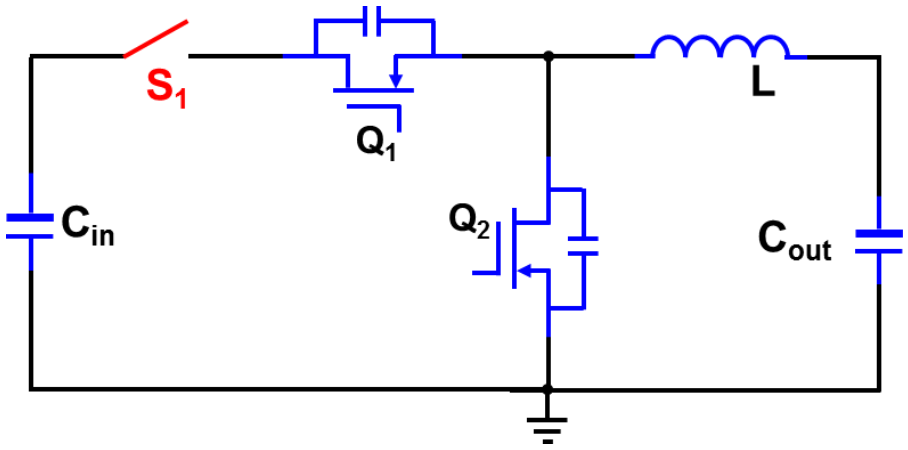


Fig.2.12: Buck circuit with switch in series of input when using depletion mode GaN

The depletion mode GaN transistor requires a negative voltage to turn off. Therefore, both positive and negative bias power supplies are needed for the driver. A level shift circuit is also needed for input PWM signals as shown in Fig. 2.13. This level shift circuit shifts the 0 V ~ 5V input PWM signal to – 3.3 V ~ 0 V then sends it to the driver. The driver generates two complementary upper gate drive (UGD) and lower gate drive (LGD) signals for top and bottom switches as shown in Fig. 2. 14. All these circuit requirements increase the circuit complicity for driving depletion mode GaN transistors.

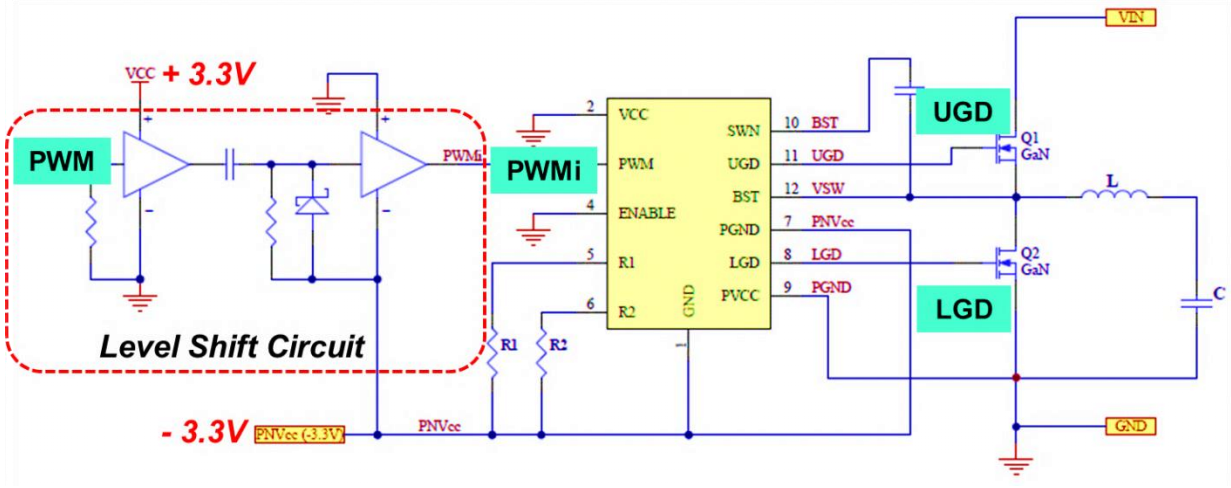


Fig.2.13: Application schematic for depletion mode GaN driver

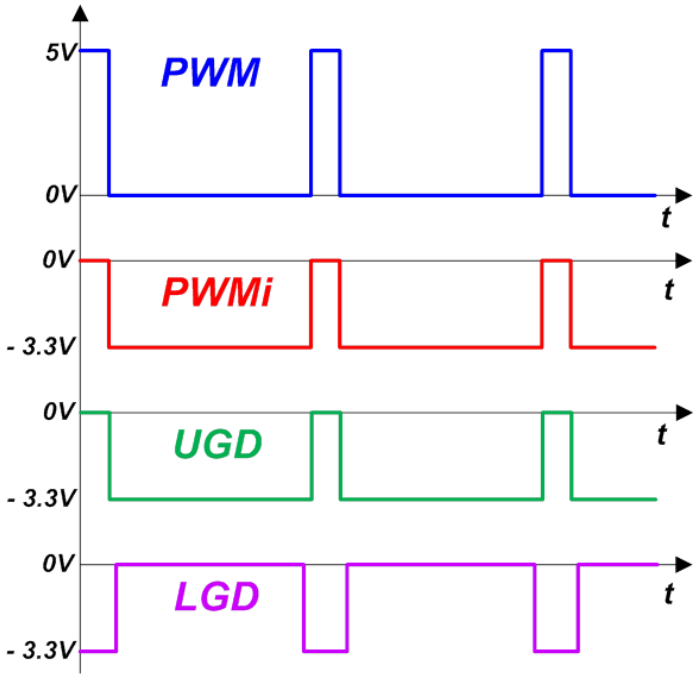


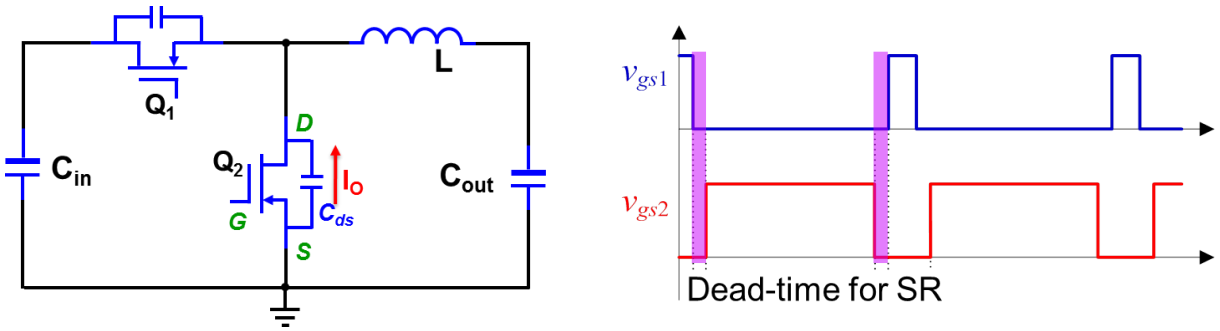
Fig.2.14: Drive signals for depletion mode GaN driver

2.3. Dead-Time Loss when Using GaN Transistor as the Synchronous Rectifier

Although the GaN transistors have similar switching characteristics with silicon MOSFET switches, there are differences between GaN transistors and silicon MOSFETs. One main difference is that a GaN transistor does not have a build-in body-diode. When implementing both of these two devices as the synchronous rectifiers, they are working in the third quadrant during the dead-time. In a synchronous buck converter, the dead time is defined as the transition time when both top and synchronous rectifier devices are turned off. The dead-time is used to prevent the simultaneous turn on for both devices which will cause shoot through that can significantly decrease the efficiency even damage the devices. During the dead-time, the current freewheels through the SR's body diode. The dead-time loss is given by:

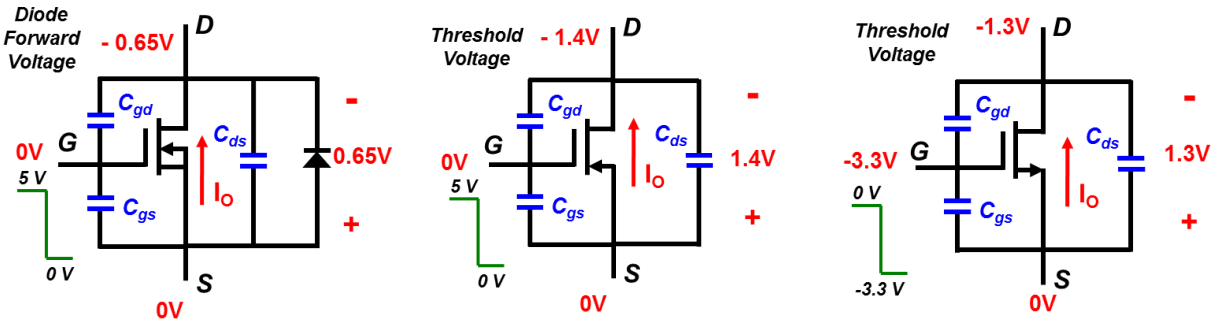
$$P_{DT} = 2 \cdot V_{BD}(I_o) \cdot I_o \cdot t_{DT} \cdot f_S \tag{2.4}$$

Where V_{BD} is the voltage drop across the SR during the dead time, I_O is the output current, t_{DT} is the dead time, and f_S is the operation frequency.



(a) (b)

Fig. 2.15: (a) Synchronous Buck converter, (b) Dead-time for SR

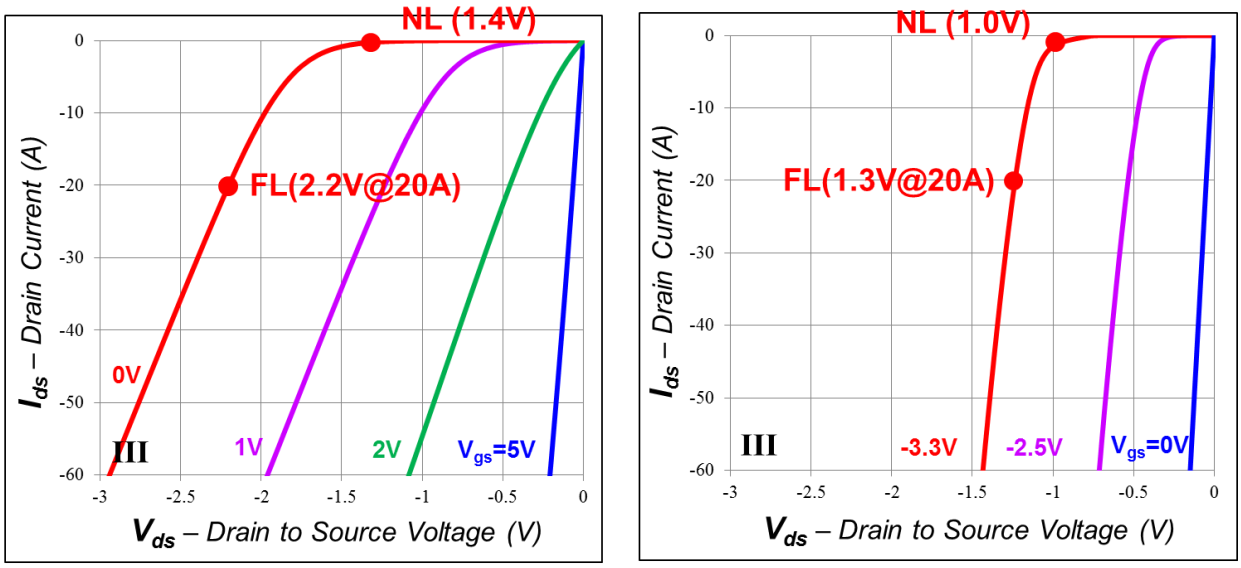


(a) (b) (c)

Fig.2.16: Dead-time operation for (a) silicon MOSFET, (b) enhancement mode GaN transistor, and (c) depletion mode GaN transistor

Fig.2.15 shows a synchronous Buck converter, when the SR works in the dead-time. For the silicon device, the channel is off during the entire dead-time. The reverse current charges the output capacitor first. When the output capacitor voltage is charged to the voltage of the internal body diode, V_{df}, the body diode turns on and conducts the load current as shown in Fig. 2.16(a). The reverse voltage between drain to source is the body-diode forward voltage, which is 0.65 V

at no load, and 0.7 V at 20 A full load.



(a) (b)

Fig.2.17: Third quadrant I-V curves for (a) enhancement mode GaN and (b) depletion mode GaN transistor

However, for a GaN device, operation in the third quadrant is quite different without the body-diode. During the dead-time, the reverse current flows from the source to drain through the output capacitor C_{ds} first, and then build a voltage across output capacitor. Because the GaN transistor is a lateral structure device, it can be driven bi-directionally with a gate voltage on either V_{gs} or V_{gd}. The gate to drain voltage is given by:

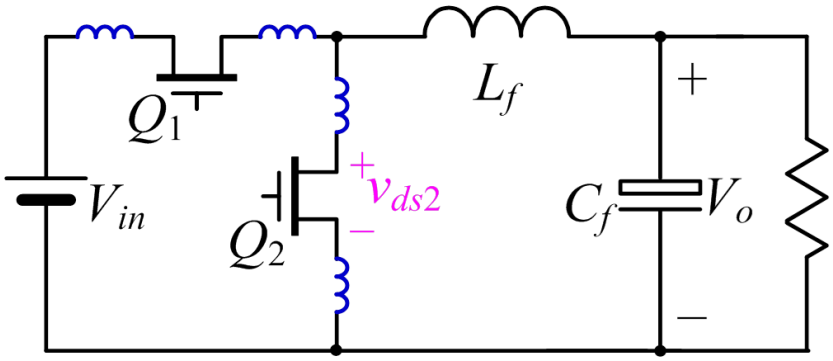
$$V_{gd} = V_{gs} - V_{ds} \tag{2.5}$$

As the source to drain voltage increasing and the channel will turn on at:

$$V_{gd} = V_{th} \tag{2.6}$$

At this time, the GaN channel turns on weakly. This device is working at the third quadrant. As the third quadrant I-V curve shown in Fig.2.17 (a), the voltage between source and drain is

the threshold voltage, which is higher than the silicon device. Furthermore, the dead-time reverse voltage increases with current increasing. For EPC's enhancement mode GaN transistor, the voltage drop is 1.4 V at no load, and 2.2 V at 20 A load, which is about 3 times larger than the silicon device. In the real application, considering the parasitics inductance in the circuit, as shown in Fig.2.18 (a), this reverse voltage during the dead-time is larger than calculated value. It is -2 V during the dead-time when SR turns off and -3 V during the dead-time when SR turns on as shown in Fig.2.18 (b).



V_{in}=12V, V_o=1.8V, f_s=1.2MHz, L_f=150nH, I_o=6A

Fig.2.18 (a) : Buck circuit with parasitic inductance

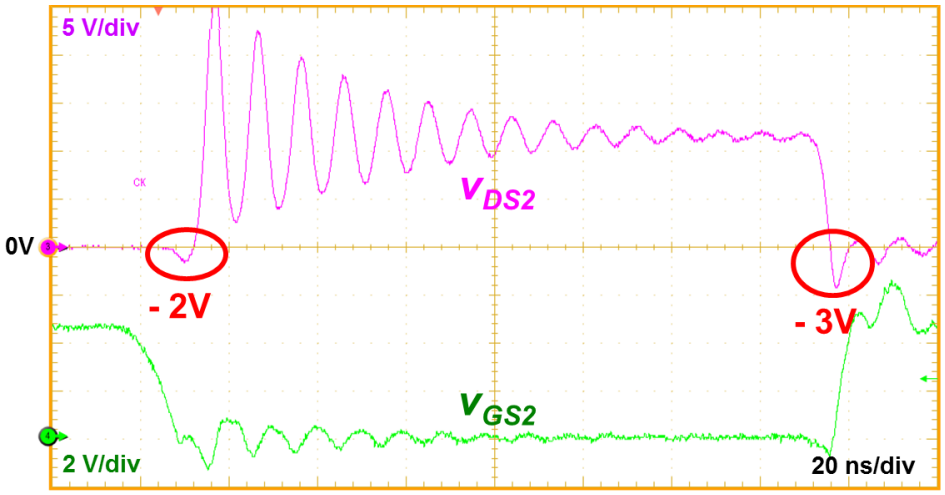
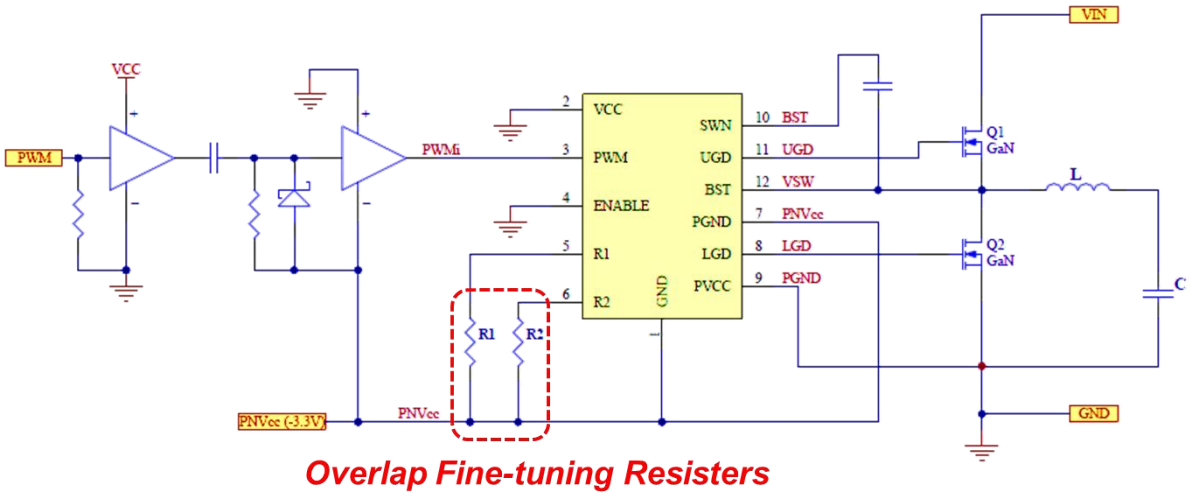


Fig.2.18 (b) : SR dead-time voltage drop

The depletion mode GaN transistor has better dead-time performance than the enhancement mode GaN transistor. As shown in Fig. 2.17 (b), the dead-time reverse voltage for IR's depletion mode GaN transistor is only 1.0V at no load and 1.3V at 20A. However, it is still 1.5 times larger than the silicon device.

In addition, the body-diode of silicon device is a minority carrier, which has a reverse recovery charger during the dead-time; whereas, the GaN transistor does not contain minority carriers during the dead-time, which eliminates the reverse recover charge.

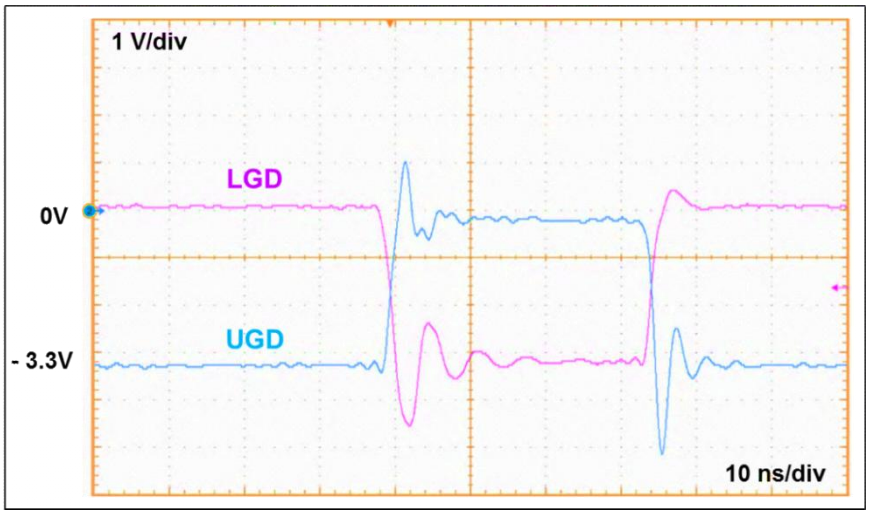
When implementing the GaN transistors in the synchronous POL converter, the dead-time loss needs to be carefully considered. There are three methods have been proposed to reduce the dead-time loss duo to the high reverse voltage. Method one is to overlap the top and bottom drive signals to reduce the transition time. The transition time can be reduced by fine-tuning the gate drive waveforms of top and bottom switches. Fig. 2.19 shows the driving circuit diagram for IR depletion mode GaN-based converter. In this circuit, two resistors R1 and R2 are used to fine-tune the dead-time between upper switch gate signal UGD and the SR gate signal LGD [30]. By fine-tuning these two resistances, the transition time between UGD and LGD is changed.



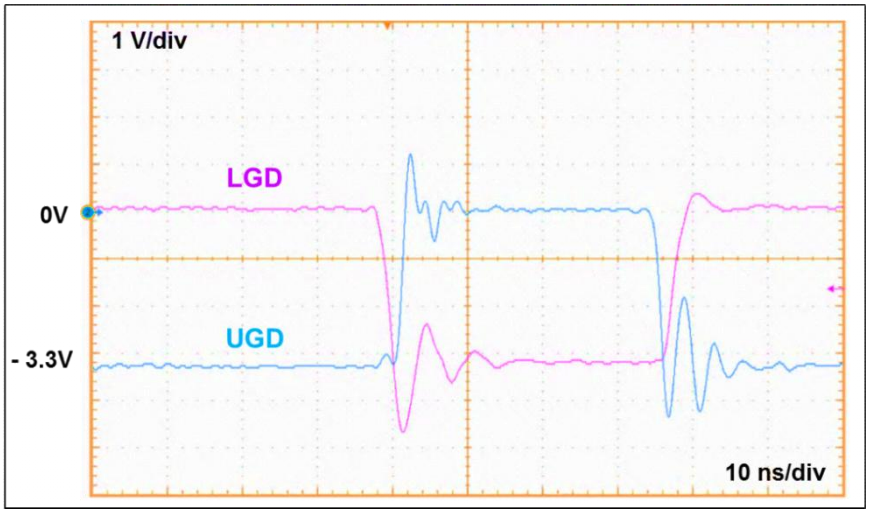
Ref: International Rectifier "10MHz 3.3V GaN Driver" datasheet

Fig. 2.19: Driving circuit diagram with fine-tuning resisters

Furthermore, the top and bottom gate drive signals can be overlapped at where slightly under the threshold voltage as shown in Fig.2.20. In this way, during the dead-time, the actual voltage between drain to source is the threshold voltage minus the gate voltage. Since the gate voltage is fine-tuned at slightly below the threshold voltage, the reverse voltage V_{ds} is reduced to about 0.2 to 0.5V depends on the fine-tuned level. Therefore, the dead-time loss can be significantly reduced.



(a) Overlapped drive signals



(b) Non-overlapped drive signals

Fig.2.20: Overlapped (a) and non-overlapped (b) UGD and LGD gate drive signals

Fig.2.21 shows the efficiency comparison for the IR's depletion mode GaN-based converter with overlapped and non-overlapped drive signals. It can clearly to be seen that with overlapped drive signals, the efficiency can be significantly improved.

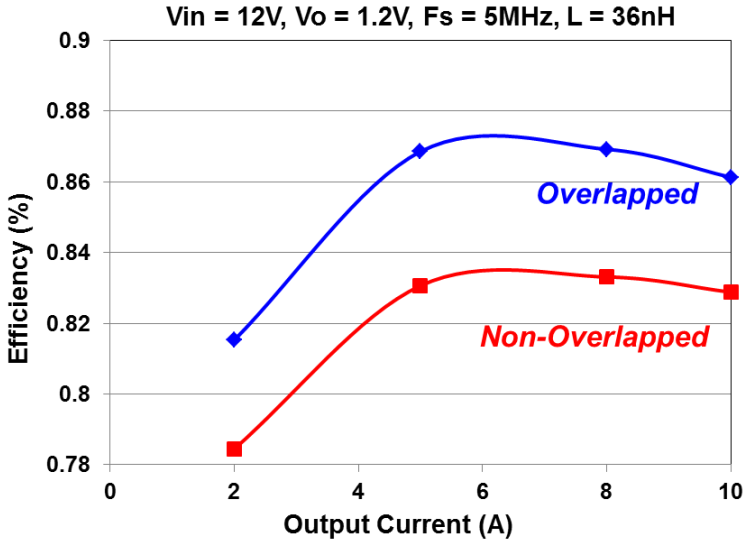


Fig.2.21: Efficiency data for IR depletion mode GaN-based converter with overlapped and non-overlapped drive signals

Although fine-tuning the gate drive signals can reduce the loss, and it is a common method that is adopted by lots of industry companies, there is still concern about the reliability since

these two driving signals are so close to the threshold voltage, the shoot through may occur in the circuit.

The second method that can improve the efficiency but does not have the shoot through concern is paralleling a Schottky diode as shown in Fig. 2.22. In this way, during the dead-time, the reverse current flows through the Schottky diode instead of GaN FET channel; therefore, the forward voltage is limited to around 0.3 to 0.5V; and the efficiency can be increased. Fig. 2.23 shows the efficiency comparison for an enhancement mode GaN-based converter. Without overlapped drive signals, the GaN efficiency is even worse than silicon. With paralleling Schottky diode, the efficiency is improved to about the same level with overlapped drive signal.

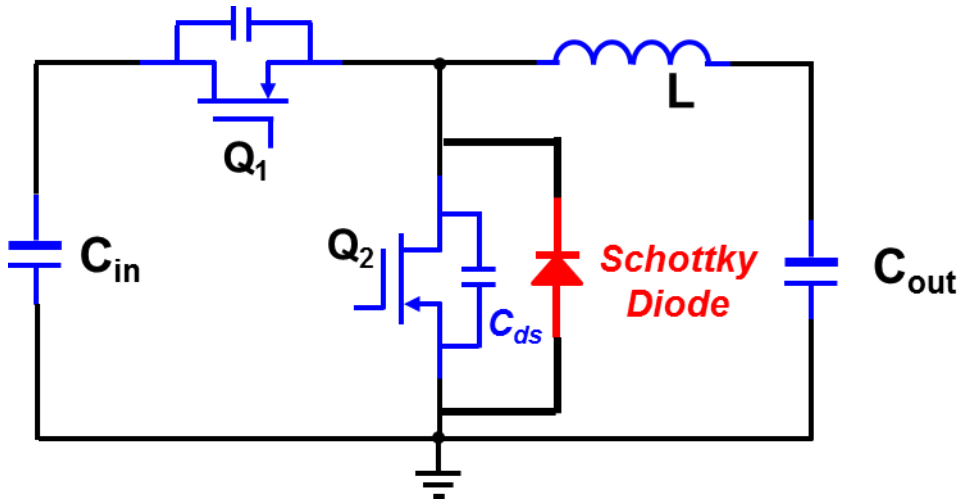
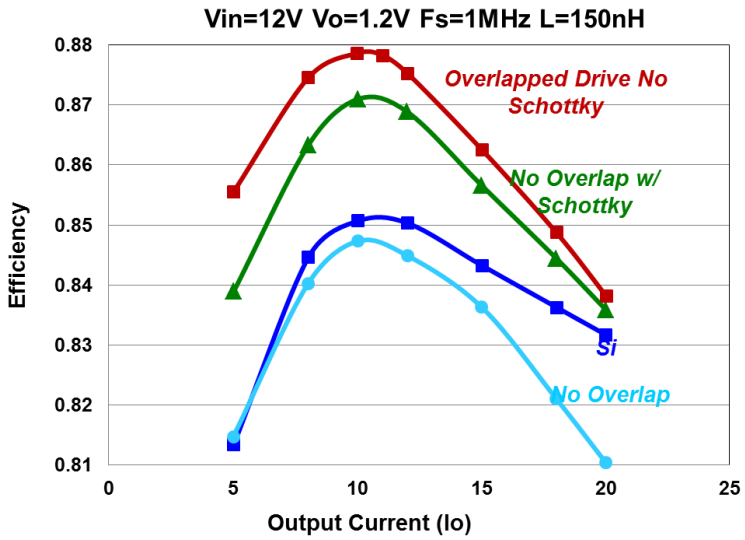


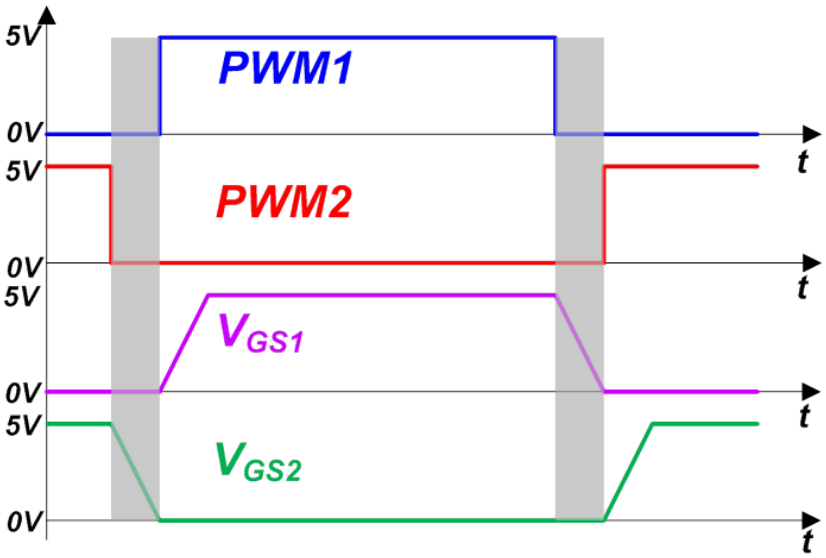
Fig.2.22: GaN transistor paralleled with Schottky diode in Buck circuit



Ref: *David Reusch, "High Frequency, High Power Density Integrated Point of Load and Bus Converters", PhD. Dissertation, 2012.04*

Fig.2.23: Efficiency data for EPC enhancement mode GaN-based converter with overlapped, non-overlapped drive signals, and with Schottky diode.

The third method that can reduce the dead-time loss is creating a step drive signal. Fig. 2.24(a) shows a common drive signals applied to the Buck converter with enhancement mode GaN transistors. The simulation waveforms show that the bottom switch Vds has over 2 V negative voltage during the dead-time.



(a) PWM signals

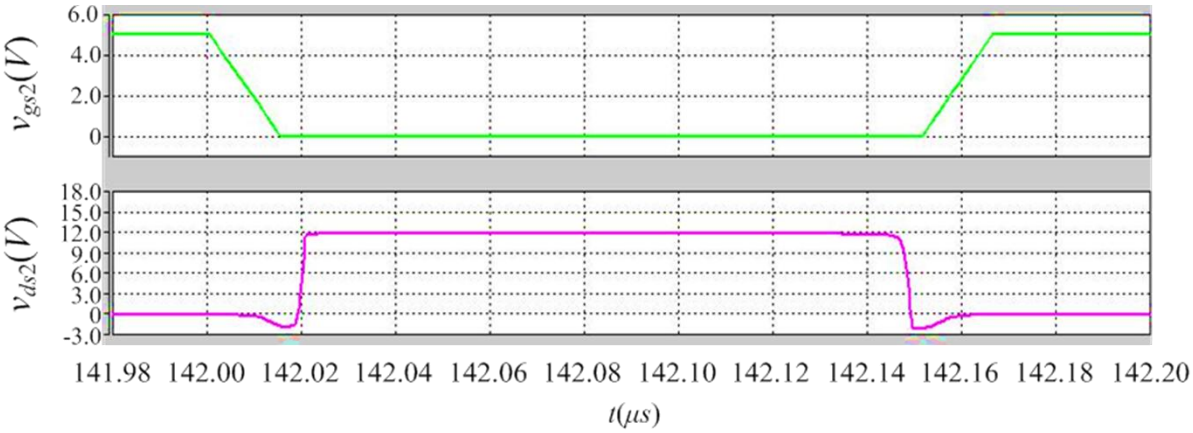
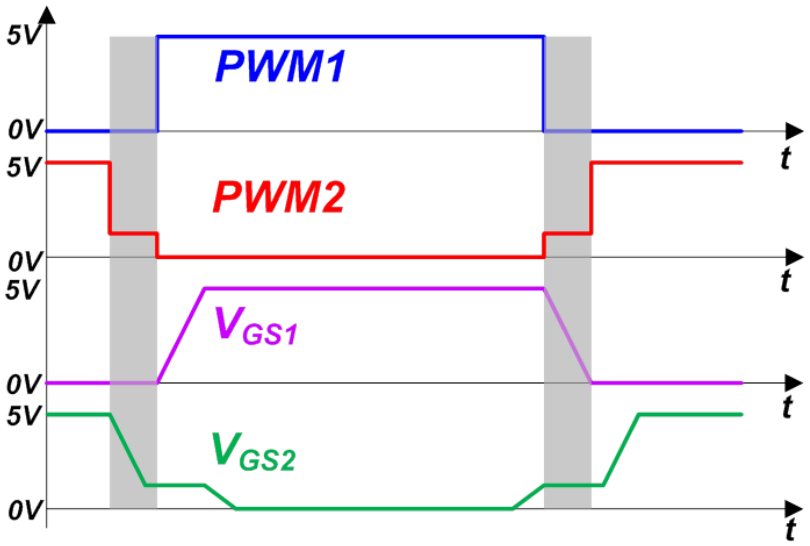


Fig.2.24: Common PWM signals and simulation waveforms for Buck converter with enhancement mode GaN transistors.

Fig. 2.25(a) shows the drive signals with a "step" is added to the SR drive signal during the turn on and turn off dead-time. The step voltage is set slightly lower the threshold voltage. In this way, during the dead-time, instead of 0 V, there is a positive voltage added on Vgs, therefore, the actual Vds voltage is reduced. The Vgs voltage simulation results are shown in Fig. 2.25(b). It can clearly to be seen that, with the step SR drive signal, the Vds voltage is significantly reduced, compared to without step drive signal.



(a) PWM signals

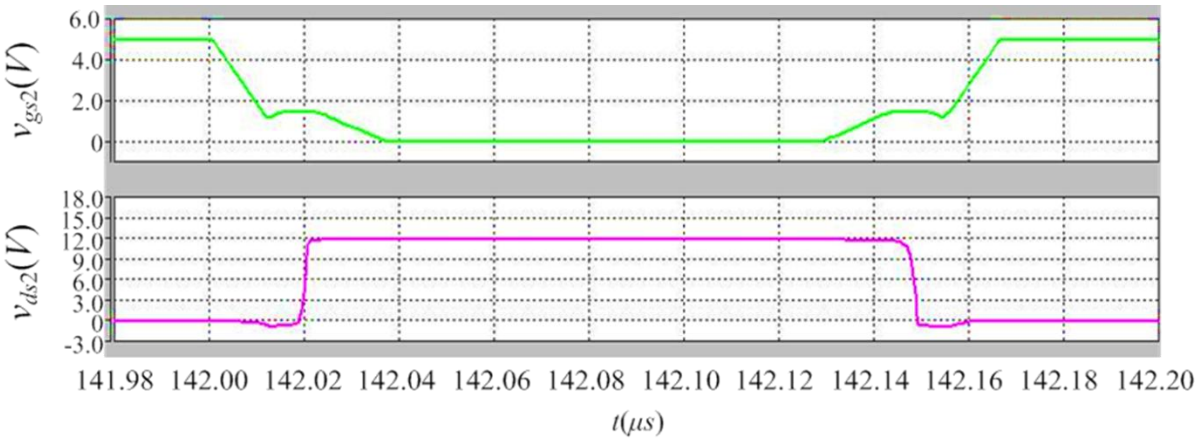


Fig.2.25: Step PWM signals and simulation waveforms for Buck converter with enhancement mode GaN transistors.

The third quadrant I-V curves can explain the reduced reverse voltage with a step drive signal. As shown in Fig. 2.26, for an enhancement mode GaN transistor, its reverse voltage will reach 2.3 V when there is no voltage applied on Vgs. However, with a step on the drive signal, there is a positive voltage applied on Vgs, the reverse voltage can be significantly reduced. With a 1 V voltage, the reverse voltage is reduced to 1.2 V at the same load condition.

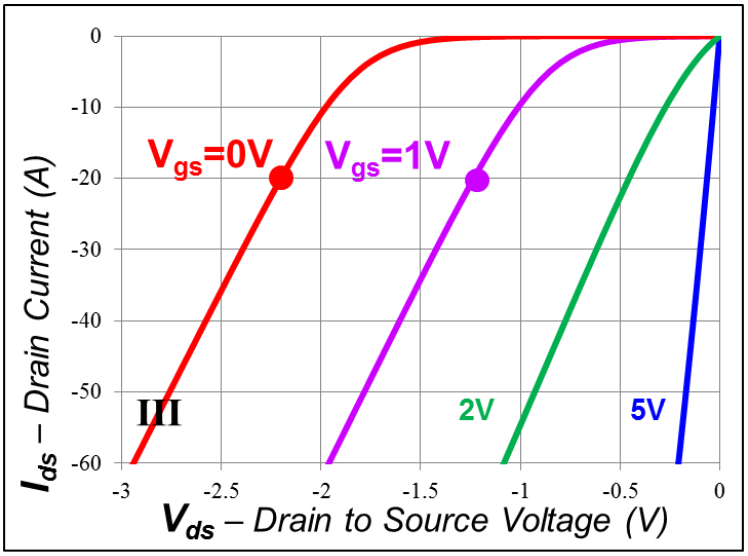


Fig.2.26: Third quadrant I-V curves for enhancement GaN transistor

2.4. Packaging and Layout Parasitics

For the high operation frequency synchronous buck converter, the parasitics in the high frequency power loop and top and bottom switches driving loops are extremely important. The general rules is that the higher of parasitics, the lower converter efficiency. Reducing the parasitics of these loops can significantly improve the converter performance [31][32].

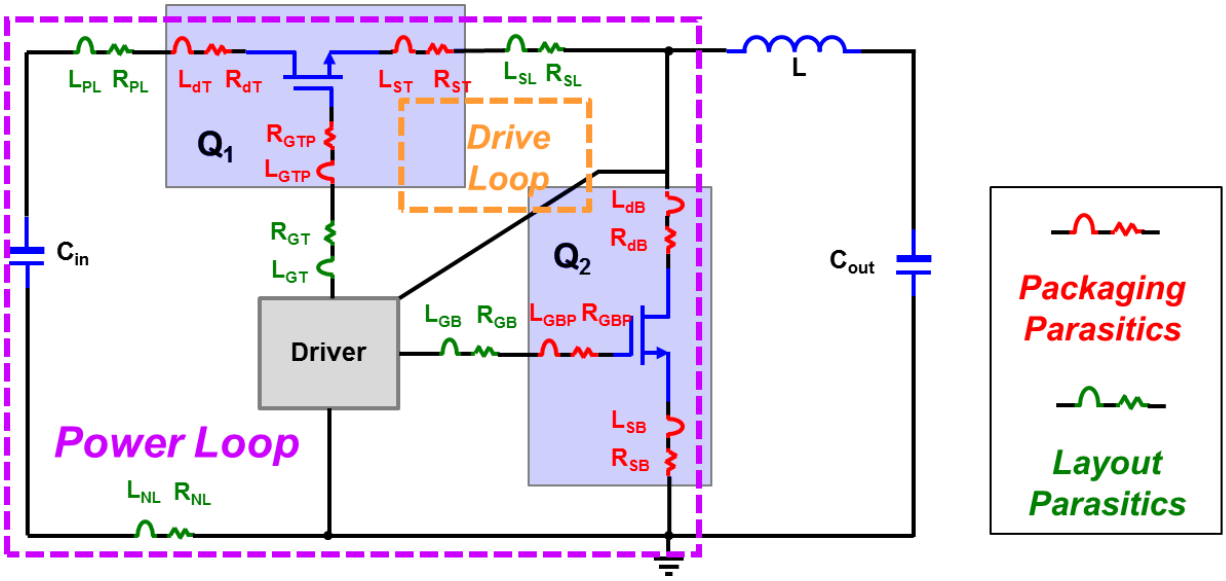


Fig. 2.27: Synchronous buck converter with parasitics

Fig.2. 27 shows a synchronous buck converter considering all the parasitics in the power loop and drive loops. These parasitics come from two parts: the device packaging parasitics, as shown in red in the figure, and the layout parasitics, as shown in green in the figure. A real Buck circuit with two EPC 1015 enhancement mode GaN transistors is analyzed by the finite element analysis (FEA) tool to extract the parasitic inductance and resistance at 1 MHz operation frequency. These parasitics are listed in Table 2.1.

Table 2.1: Circuit parasitics for EPC 1015 GaN FETs based Buck converter @ 1 MHz

L	L_{DT}	L_{ST}	L_{GTP}	L_{DB}	L_{SB}	L_{GTP}	L_{PL}	L_{SL}	L_{NL}	L_{GT}	L_{GB}
(nH)	0.07	0.08	0.07	0.07	0.08	0.07	0.49	0.23	0.47	1.24	1.6
R	R_{dT}	R_{ST}	R_{GTP}	R_{dB}	R_{SB}	R_{GTP}	R_{PL}	R_{SL}	R_{NL}	R_{GT}	R_{GB}
(mΩ)	0.09	0.10	0.12	0.09	0.10	0.12	0.4	0.17	0.59	4.9	3.87

As shown in Fig. 2.28, the power loop parasitic inductances can be lumped into two main parts: L_S and L_{LOOP}. L_S is the common source inductance shared by the drain to source current path and gate driver loop. L_{LOOP} is the high frequency power loop inductance from the positive terminal of the input capacitance, through the top device, synchronous rectifier, and ground loop to the input capacitor negative terminal. The inductances are defined as:

$$L_S = L_{ST} + L_{SL} \tag{2.7}$$

$$L_{LOOP} = L_{PL} + L_{DT} + L_{DB} + L_{SB} + L_{NL} \tag{2.8}$$

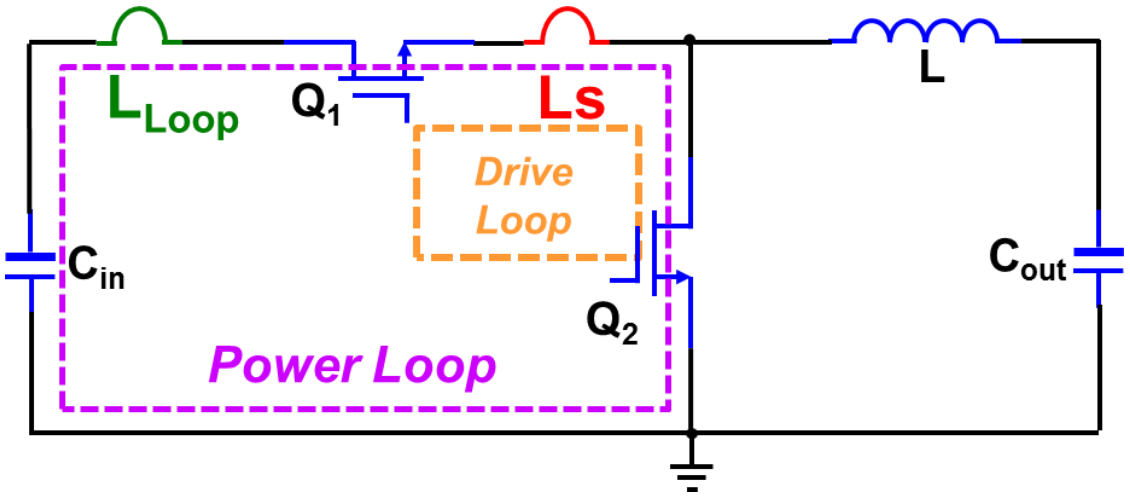


Fig. 2.28: Power loop inductance

Fig. 2.29 shows the impact of L_S and L_{LOOP} on the top side switch turn-on transition. During

the turn on transition, since the drain current is rising, the negative voltages are induced by the positive di_D/dt across L_S and L_{LOOP}. The actual voltage across drain to source of the device is:

$$V_{DS} = V_{IN} - V_{Loop} - V_{LS} = V_{IN} - \frac{di_D}{dt} \cdot L_{Loop} - \frac{di_D}{dt} \cdot L_{Ls} \tag{2.9}$$

Then the device gate driving current is:

$$I_g = \frac{V_{Drive} - V_{gs(on)} - V_{Ls}}{R_g} \tag{2.10}$$

Where V_{drive} is the drive voltage, $V_{gs(on)}$ is gate to source voltage during turn on, and R_g is the total gate resistance.

The induced voltage V_{Loop} and V_{LS} reduce the effective voltage across the drain to source during the turn on transition, reduce the switching loss. However, the common source inductance induced voltage V_{LS} counteracts the driving gate voltage, reduces the available gate charging current. Therefore, the turn on transition speed is limited.

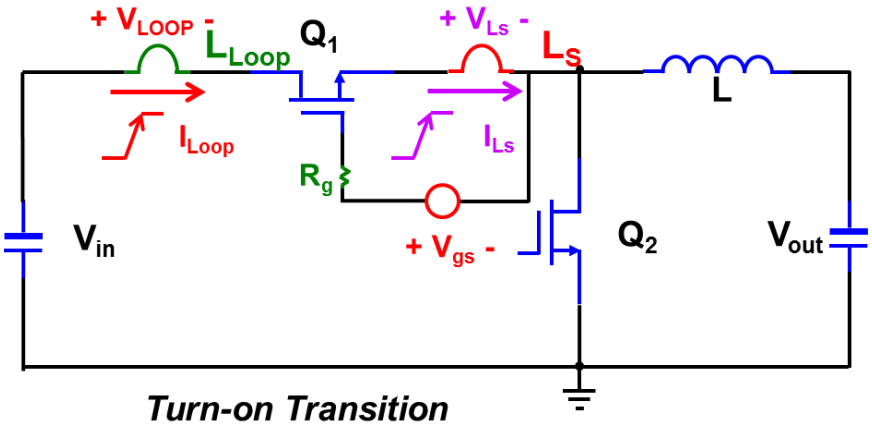


Fig. 2.29: Parasitics impact at turn-on transition

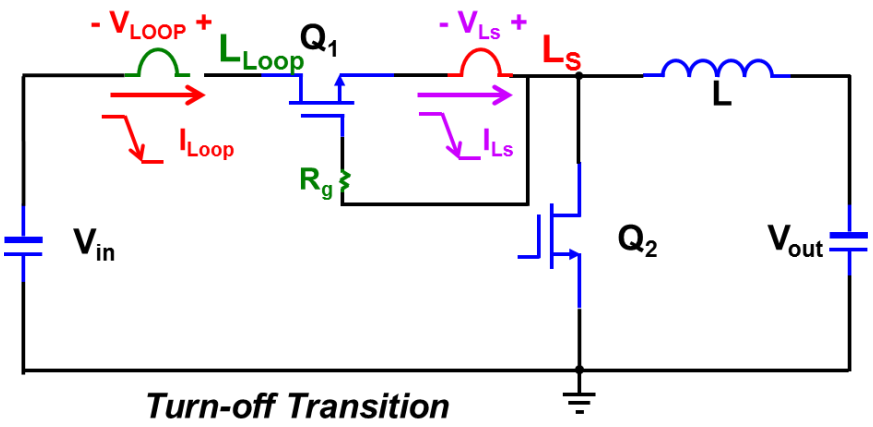


Fig. 2.30: Parasitics impact at turn-off transition

During the turn off transition, shown in Fig. 2.30, the drain current is falling. The positive voltage are induced by the negative di_D/dt across L_S and L_{LOOP}. The actual voltage across drain to source of the device is:

$$V_{DS} = V_{IN} + V_{Loop} + V_{LS} = V_{IN} + \frac{di_D}{dt} \cdot L_{Loop} + \frac{di_D}{dt} \cdot L_{Ls} \tag{2.11}$$

The device gate driving current is:

$$I_g = \frac{-V_{gs(on)} + V_{Ls}}{R_g} = \frac{-V_{gs(on)} + \frac{di_D}{dt} \cdot L_{Ls}}{R_g} \tag{2.12}$$

The induced voltage V_{Loop} and V_{LS} add to the input voltage, increase the effective voltage across the drain to source during the turn off transition, and increase the switching loss. L_S. The common source inductance induced voltage V_{LS} counteracts the driving gate voltage, slows down the device turn off speed, and lengthens the turn off transition time.

As the results, for the synchronous buck converter with small duty cycle, both common source inductance L_S and high frequency power loop inductance L_{LOOP} have negative impacts on turn on and turn off transition, increase the loss. Fig 2.31 gives the simulated power loss at

different L_S and L_{LOOP}. It can be seen than the power loss is creasing with both increasing of L_S and L_{LOOP}. L_S has more impact than L_{LOOP} because L_S carries the drain source current and the gate charging current. Any voltage induced on L_S will show up in the Vgs of switch. Because of the importance of Vgs on the switching performance of the power switch, common source inductance has a significant impact on the system performance [33][34][35][36][37].

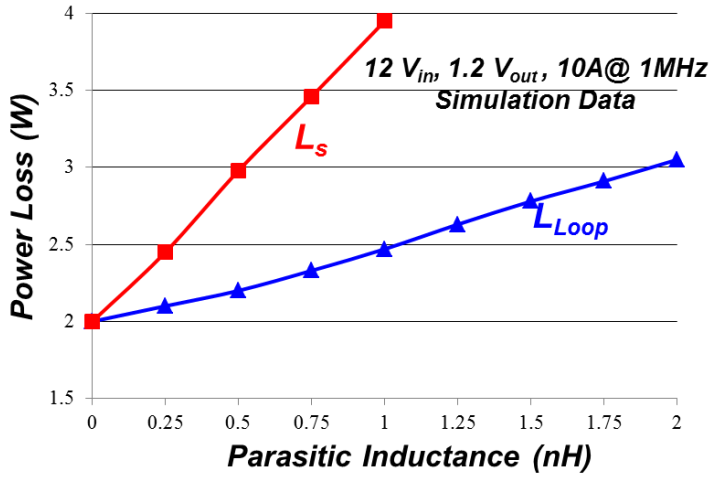
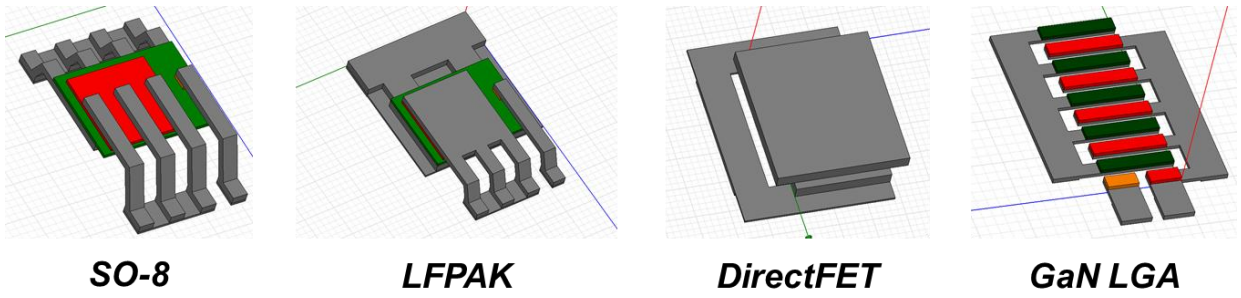


Fig. 2.31: Power loss vs parasitic inductance



Ref: David Reusch, "High Frequency, High Power Density Integrated Point of Load and Bus Converters", PhD. Dissertation, 2012.04

Fig. 2.32: Package evolution for power transistors

When designing the high frequency converter, both the device packaging parasitics and the layout parasitics need to be minimized to achieve good circuit performance. The LGA package, which is adopted by both IR's depletion GaN transistor and EPC's enhancement GaN transistor,

has remarkably low package inductance. Compared with the common low voltage silicon MOSFET package types: SO-8, LFPAK, and DirectFET, as shown in Fig. 2.32, the LGA package has much smaller parasitic inductance and resistance [38]. The low parasitics inductance gives GaN transistors the capability of fast switching at the high frequency operation. The parasitics FEA simulation results for these packages are listed in Table 2.2.

Table 2.2: Devices package parasitics

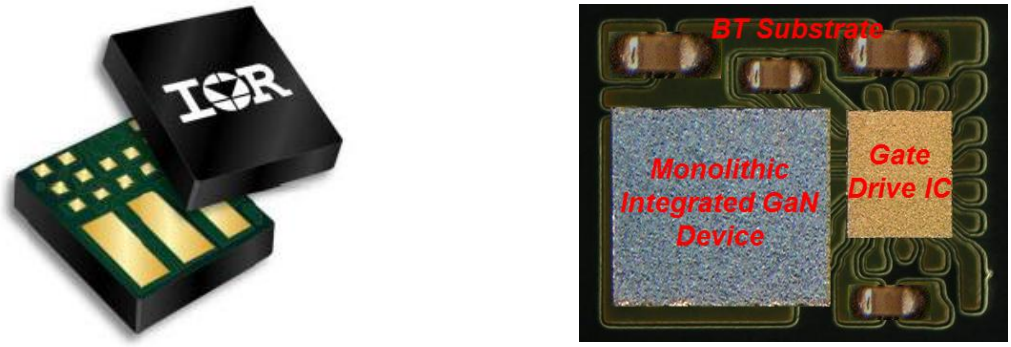
Fs = 1MHz	**L_g (nH)**	**L_d (nH)**	**L_s (nH)**	**R_g (mΩ)**	**R_d (mΩ)**	**R_s (mΩ)**
SO-8	2.06	0.48	0.83	9.44	0.13	0.96
LFPAK	1.64	0.1	0.54	0.73	0.1	0.14
DirectFET	0.09	0.44	0.09	0.22	0.39	0.23
GaN LGA	0.07	0.07	0.08	0.12	0.09	0.1

When implement these GaN transistors in circuit design, since the packaging parasitics have been minimized, the layout parasitics become critical to circuit performance, it has to be minimized as well. The way of minimizing the layout parasitics will be introduced in chapter 3.

2.5. Modular Approach vs Discrete Approach

IR and EPC chose different approaches of launching their GaN devices to the market. In 2010, IR introduced the GaN-based iP2010 integrated power stage device [39], as shown in Fig.2.33 (a). The iP2010 provides a fully optimized, high frequency power stage solution for synchronous buck applications. Inside the module, the 30V top and bottom GaN transistors are monolithic integrated into the same wafer with optimized die size for POL application, a highly

sophisticated, ultra-fast silicon driver IC, and input decoupling capacitors are mounted on a BT-Epoxy material substrate as shown in Fig.2.33 (b). This module can deliver higher efficiency and more than doubled switching frequency of state-of-the-art silicon-based integrated power stage devices. The maximum switching frequency of this module is 3MHz.



(a) (b)

Fig. 2.33: (a) IR GaN-based integrated power stage devices (b) device interior

Different with IR's modular approach, EPC only sells the discrete GaN devices. When designing a GaN-based converter, designer needs to choose the proper top and bottom switches, find the suitable drive IC, design the substrate, and assemble them together to form a module as shown in Fig. 2.34.

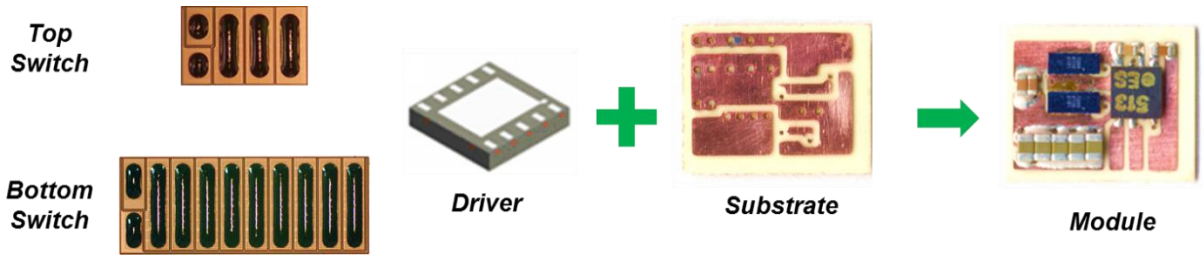


Fig. 2.34: Discrete approach for EPC GaN devices

In this design process, the designer will face several challenges: first of all, in order to get better performance, the layout parasitics have to be minimized. Second, the gate drive signals

need to be carefully fine-tuned to reduce the dead-time loss. Third, since GaN device has smaller die size than silicon MOSFET, proper thermal management has to be implemented into the design. Last, the maximum operation frequency is limited because of gate voltage limit and circuit parasitics.

Because there are so many challenges for the discrete approach, IR chooses the modular approach to achieve the best performance for their products. Instead of provides discrete GaN devices, IR provides the complete power stage module solution to their customer. Inside the module, the parasitics have been minimized, the gate signals have been well fine-tuned, and the thermal performance has been optimized. This approach reduces the burden for the circuit designer.

2.6. Summary

In this chapter, the fundamental characteristics of depletion mode and enhancement mode GaN transistors are introduced. IR's depletion mode GaN transistor offers better figure of merit, much safer driving, and higher operation frequency capability than EPC's enhancement mode GaN transistor. IR's modular approach also provides a better performance, easier solution for the designer than EPC's discrete approach.

Parasitics is critical for high frequency converter design. Both of these two types of GaN transistors utilize the LGA package to reduce packaging parasitics. In the meantime, the circuit layout parasitics have to be minimized as well in order to achieve better performance of the converter.

Chapter 3. 3D-Integrated POL Module Design with Depletion Mode GaN Transistor

The future point of load (POL) converter needs to achieve high power density, high efficiency, high output current, and small size factor. All these demands cannot be satisfied with the conventional technologies. There are limitations in the switch performance, packaging parasitics, layout parasitics, and thermal management that must be addressed to push for higher frequencies and improved power density. To overcome all these limitations, the design of 3D-integrated POL modules utilizing IR's depletion mode GaN transistors will be addressed in this chapter.

The previous chapter addresses the characteristics of depletion mode and enhancement mode GaN transistors. IR's depletion mode GaN transistor offers better figure of merit, much safer driving, and higher operation frequency capability than EPC's enhancement mode GaN transistor. Therefore, IR's depletion mode GaN transistor is chosen in this thesis work to design the high frequency, high power density POL Module.

This chapter will discuss the module structure design, the method of reducing layout parasitics, the shield layer implementation, the PCB substrate design, thermal management with advanced DBC substrate, the integration of the low profile LTCC magnetic substrate, and the two phase interleaved module design.

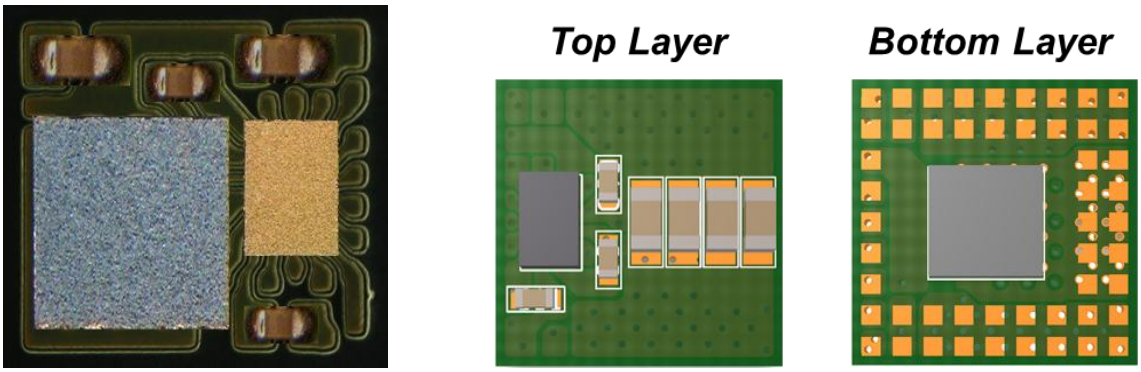
3.1. IR's High Frequency GaN Module

At APEC 2011, IR demonstrated the new iP2008 RvG high frequency GaN module [40]. Compared with the iP2010 and iP2011 GaN module that released in 2010, the maximum operation frequency is increased to 10 MHz. The features comparisons between iP2010 and iP2008 RvG modules are listed in Table 3.1.

Table 3.1: Features comparisons between iP2010 and iP2008 RvG GaN module

	iP2010	**iP2008 RvG**
Maximum Operation Frequency	3 MHz	5 MHz
Maximum Current	30A	10A
GaN Die Size	4.5 X 4.5 mm^2	3 X 3 mm^2
Driver	Up to 3 MHz	Up to 10 MHz

Fig. 3.1 shows IR's iP2010 and new iP2008 RvG GaN modules. The GaN transistor die of iP2008 RvG has been modified for high frequency operation; the die size is reduced to 3 X 3 mm^2 from 4.5 X 4.5 mm^2 of iP2010. The maximum output current is also reduced to 10 A from 30 A of iP2010 because of die size reduction. The silicon gate driver is modified as well to fit maximum 10 MHz driving.



(a) (b)

Fig.3.1: IR's iP2010 (a) and iP2008 RvG (b) GaN modules.

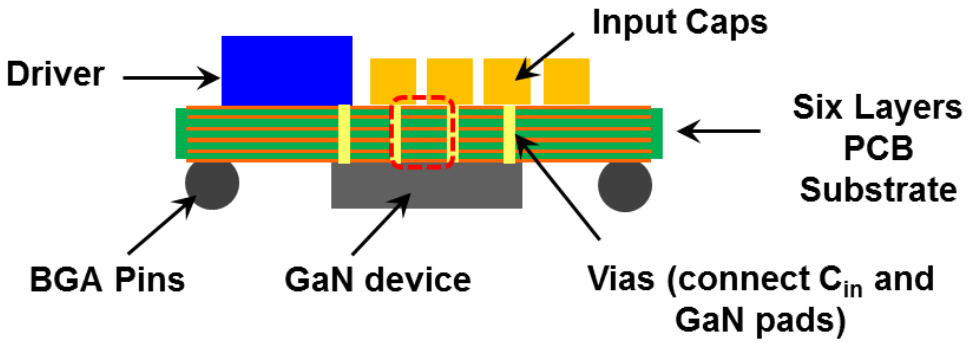


Fig. 3.2: Cross section view of iP2008 RvG Module

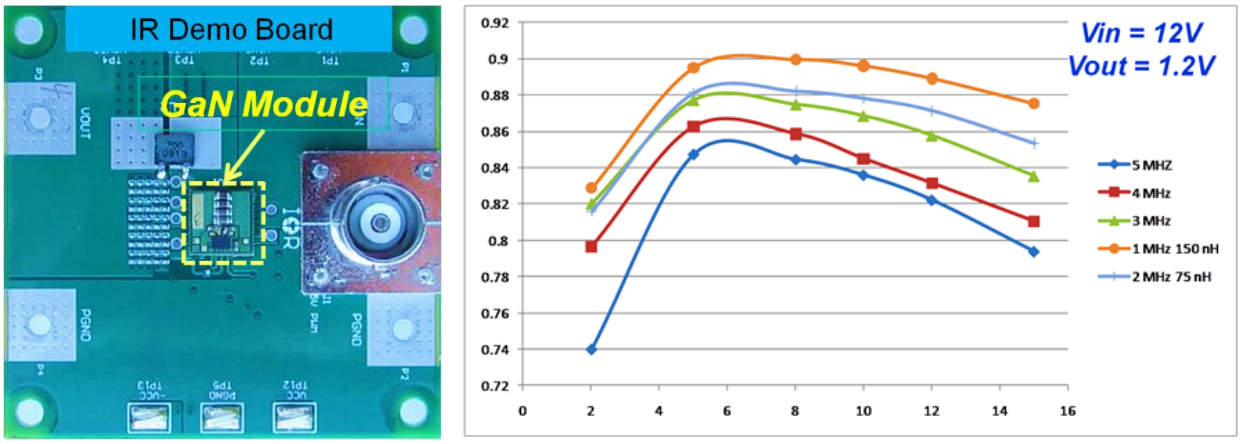
The most noticeable difference is that the structure on the new module is changed. For the previous iP2010 module, the GaN transistors, driver, and capacitors are all on the same side of PCB substrate. This structure has been proved to be adequate for 3 MHz maximum operation frequency. However, in order to push to 10 MHz operation frequency on iP2008 RvG module, this structure needs to be modified. As shown in Fig. 3.2, iP2008 RvG module chooses the double side structure. The driver, input capacitors are placed on the top side of a 6 layer PCB substrate, the BGA input/output pins and GaN transistors are placed on the bottom side. The GaN device is right underneath of input capacitors, connects to the input capacitors and driver by vias. In this structure, the high frequency power loop area is minimized, as shown in the red dash line in Fig. 3.2. The drive loops are minimized as well since the drive connects GaN device's

gate terminals directly by vias. Table 3.2 gives the parasitic inductances and resistances for power loop and drive loops for this double side structure under 1 to 5 MHZ operation frequency, extracted by Ansoft Q3D extractor. It can be found that the power loop inductance is less than 0.1 nH, which is extremely low. Therefore, this double side structure is suitable for high frequency operation.

Table 3.2: Parasitic inductance and resistance for iP2008 RvG module

Operation Frequency	Power Loop		Drive Loop TOP		Drive Loop Bottom	
	L (nH)	R (mΩ)	L (nH)	R (mΩ)	L (nH)	R (mΩ)
1 MHz	0.099	0.262	0.476	3.885	0.314	3.058
2 MHz	0.093	0.332	0.406	4.768	0.261	3.743
3 MHz	0.090	0.392	0.361	5.530	0.224	4.346
4 MHz	0.087	0.445	0.328	6.199	0.197	4.880
5 MHz	0.086	0.493	0.304	6.801	0.176	5.361

Fig. 3.3 (a) shows the iP2008 RvG module assembled on a demo board. This GaN module does not have the output inductor and capacitors, they are assembled on the demo board. Fig. 3.3 (b) shows the efficiencies tested with Coilcraft discrete inductors with 15 A output current at 1 to 5 MHz operation frequency respectively. It can be seen that the efficiency is decreasing with the increasing operation frequency; the peak efficiency is usually at 6 A, and there is significant low efficiency at light load.



(a) (b)

Fig. 3.3 (a): GaN module on demo board, (b) demo board efficiency

3.2. Structure Redesign for Inductor Integration

Although iP2008 RvG module's double side structure has extremely low power loop parasitic inductance, which is critical for high frequency operation as addressed in chapter 2, this module does not have on-board output inductor and output capacitors. The objective of this thesis work is to build a 3D integrated converter, which means the inductor and output capacitor should be integrated into the module. However, IR's double side structure has an issue when assembling the inductor as shown in Fig. 3.4. The top side of the module is occupied by the driver and input capacitors, and there are not at the same level. When place the inductor on top, it is extremely difficult for soldering and is not mechanically stable. Therefore, the double side structure is not suitable for the inductor integration. The structure has to be redesigned.

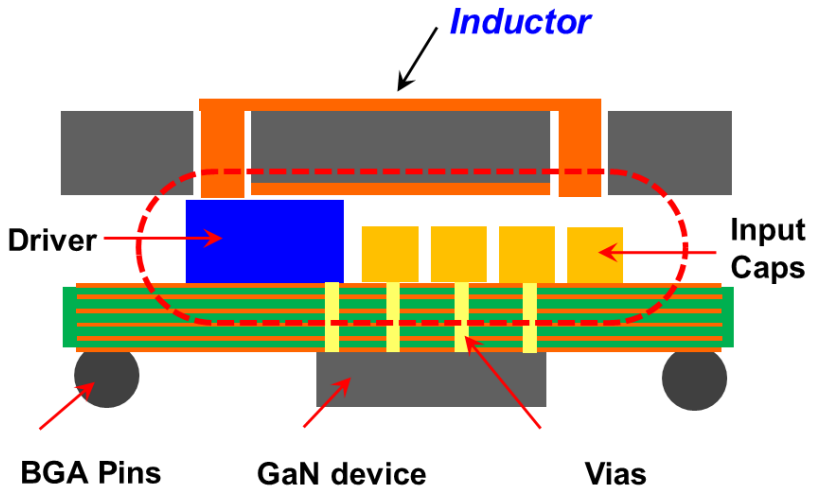


Fig. 3.4: Issue of inductor assembling on double side structure

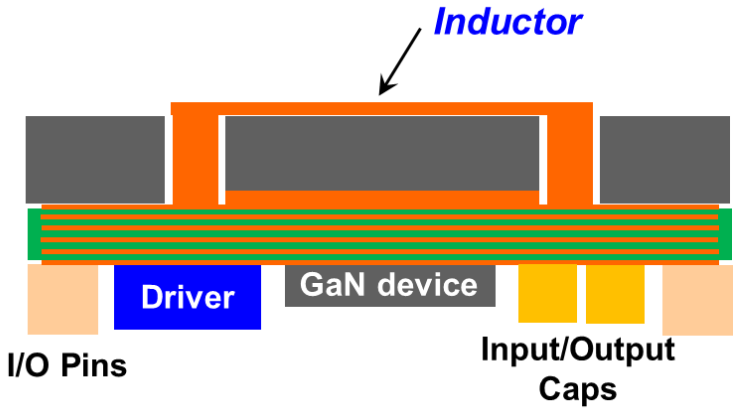
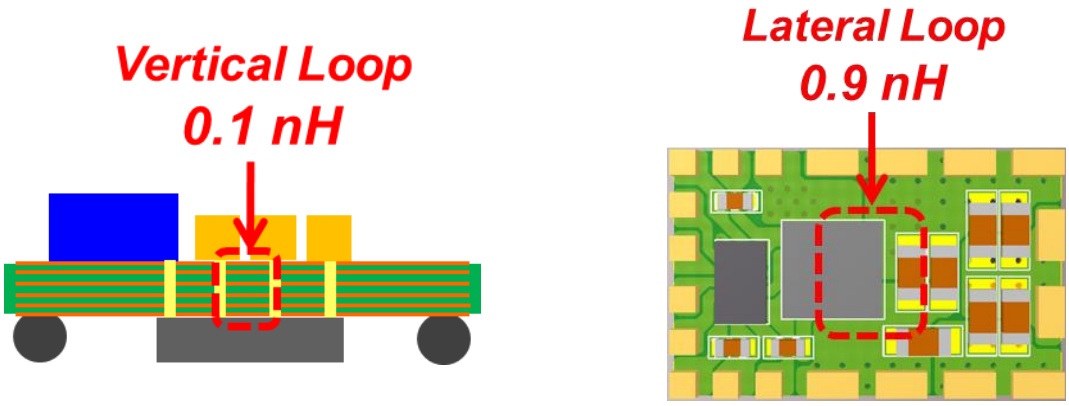


Fig. 3.5: Proposed single side structure

Fig. 3.5 shows the proposed single side structure. In the structure, the driver and input capacitors are moved to the bottom side, the output capacitors are also added into the module. The top side of module is clean and flat now; it is suitable for inductor assembling.

However, after move the input capacitor and driver to the same side of GaN switches, the power loop structure is changed. As shown in Fig. 3.6 (a), the power loop is vertical in the double side stricture. The distance between input capacitors and GaN switches is only the thickness of PCB substrate, which is 0.6 mm. The loop inductance is only 0.1 nH. In the

proposed single side structure, the power loop is a lateral loop. The loop area is increased; the loop inductance is also increased to 0.9 nH.



(a) (b)

Fig. 3.6: Vertical power loop (a) and lateral loop (b)

In order to evaluate the effect of the increased power loop inductance, a simulation model is built as shown in Fig. 3.7. This simulation model comes from two parts: the GaN device model provided by IR and the circuit parasitics extracted by Ansoft 3D.

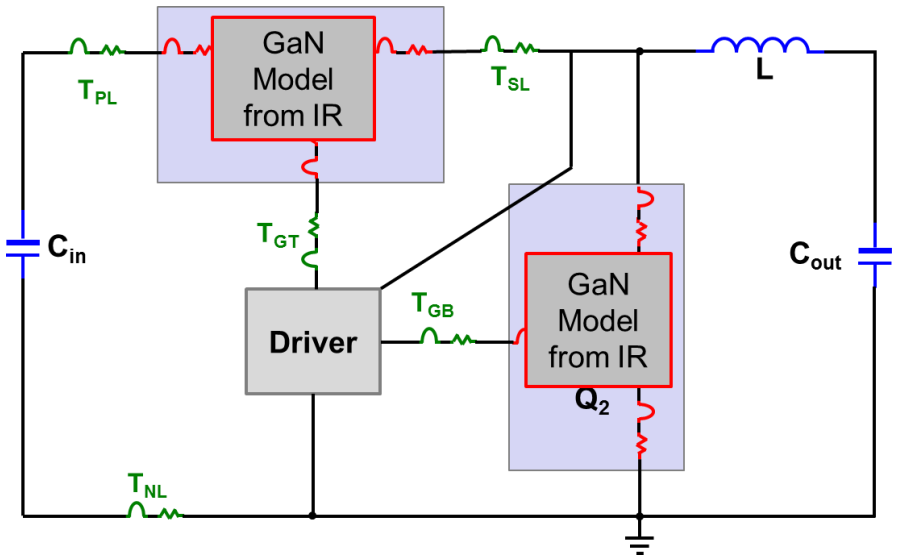


Fig. 3.7: Simulation model

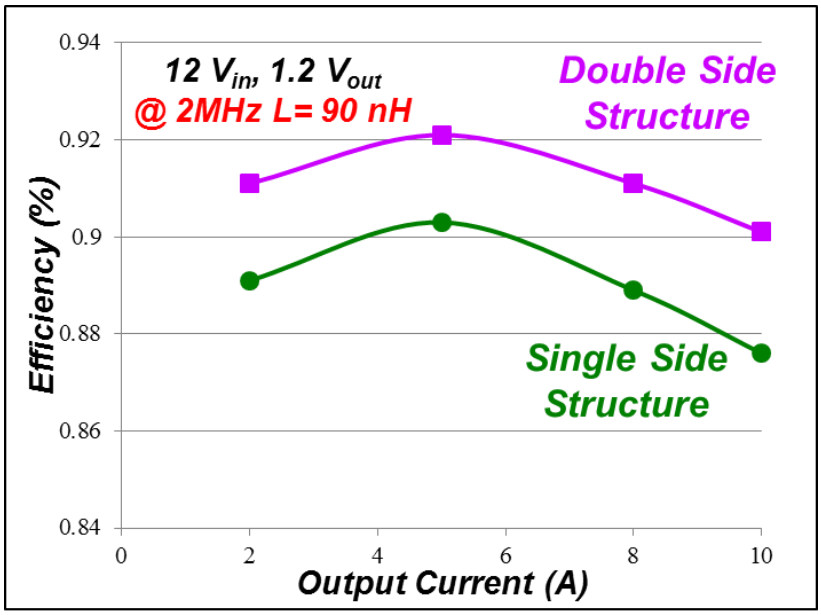


Fig. 3.8: Estimated efficiencies data

After putting the extracted parasitics of double side structure and single side structure into the simulation model, the efficiencies data can be estimated as shown in Fig. 3.8. The result shows that the single side structure has significant lower efficiency than the double side structure duo to the increased power loop inductance. The loop inductance has to be reduced in order to achieve high efficiency.

3.3. Active Layer with PCB Substrate

3.3.1. Implementing Shied Layer to Reduce Loop Inductance

The shield layer has been proved to be an effective method to reduce the loop inductance especially for the POL module with integrated inductor [41]. In previous practice, a POL converter was built with LTCC inductor as the substrate. The silver traces were printed on LTCC inductor, and then the active components were placed on top of LTCC inductor. The test results

showed that this converter had severe ringing caused by parasitic inductance, which was introduced by the mutual coupling between the magnetic core and the active circuit. To reduce the parasitic inductance, one solution is inserting a shield layer between LTCC inductor and the active circuit to block the mutual coupling. Moreover, the eddy current induced in the conductive shield layer further reduces the parasitic inductance. Therefore, a minimum two layers of substrate is needed for active circuit since one layer is used as a shield layer.

Fig. 3.9 shows the concept of reducing loop inductance by implementing a shield layer. The power loop current I generates the flux Φ. After a metal shield layer is inserted underneath the active layer, the flux Φ generates an opposite direction eddy current in the shield layer. This eddy current also generates flux Φ', which cancels with flux Φ. Therefore, the loop inductance can be reduced.

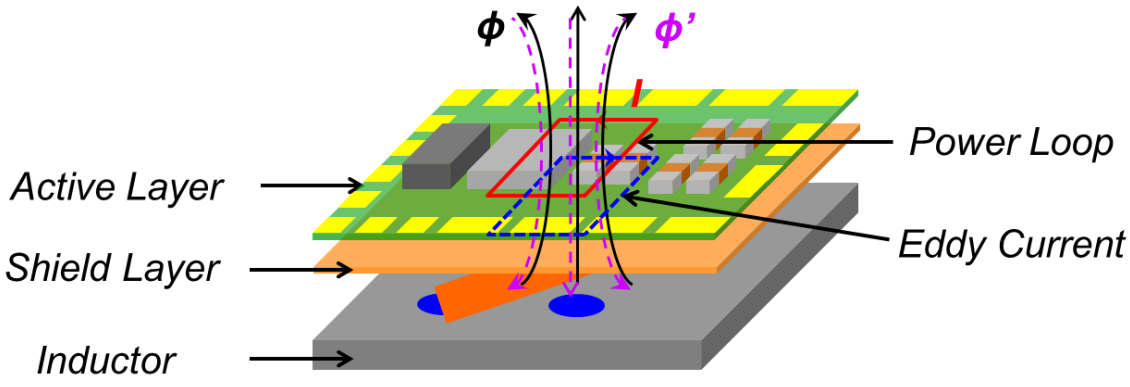
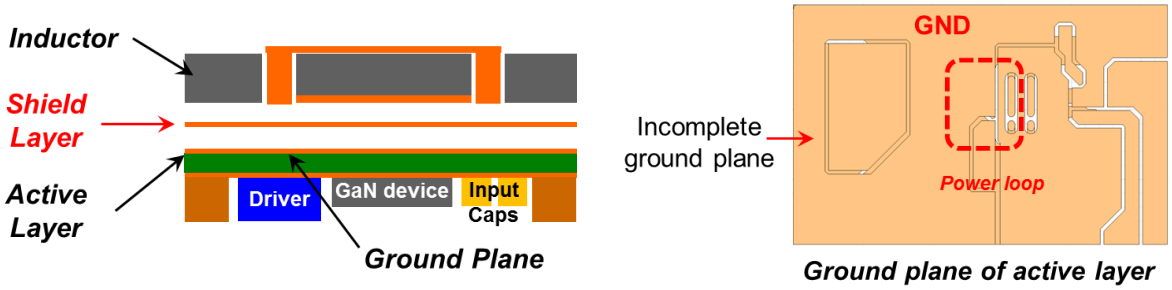


Fig. 3.9: Concept of implementing shield layer

Fig. 3.10 (a) shows the first attempt of implementing the shield layer. The shield layer is inserted between the inductor and the copper layer of active layer substrate, which is a ground plane of the circuit as shown in Fig. 3. 10 (b). Since this ground plane is not well designed in the

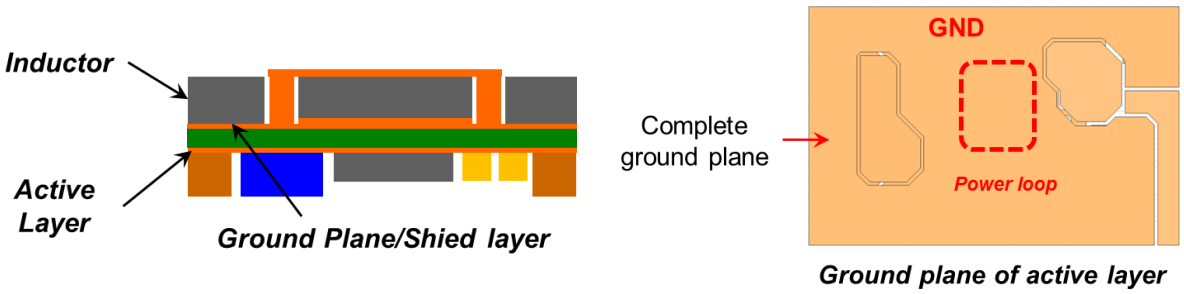
first time, it is incomplete and not able to cover the power loop area, the loop inductance is 0.9 nH without a shield layer. After a shield layer is inserted, the loop inductance can be reduced to 0.57 nH, which is 36.7% of reduction.



(a) (b)

Fig. 3.10: Implementing the shield layer

The inserted shield layer does reduce the loop inductance, and the simulation results show the efficiency is improved. However, since an extra layer of metal is required, it increases the complexity of module integration and the cost. Fig. 3.11 shows another method to implementing the shield layer. A well redesigned complete ground plane as shown in Fig. 3.11(b), which can cover all the power loop area, can serve as the shield layer too. In this way, the system structure is simplified without the additional shield layer as shown in Fig. 3.11 (a), it is easy to integrate the active layer with inductor; the cost is also reduced. Moreover, since the ground plane/shield layer is closer to the active layer, the flux cancelation is more effective.



(a) (b)

Fig. 3.11: Using ground plane as the shield layer

3.3.2. PCB Substrate for Single Phase Module

After moving all the active layer components to the single side and using a ground plane as the active layer, a PCB substrate is designed for the single phase GaN module. Fig. 3.12 shows the structure of a single phase GaN module with PCB substrate. This PCB substrate contains 6 layers of copper: the top layer is the active layer where the components soldered; the middle 1 layer is the well-designed ground plane which serves as the shield layer, the middle 2, 3, and 4 layers are Vin, ground, and Vout respectively for better thermal performance; the bottom layer is also the ground plane and have two pads for inductor connection. The parameters of this PCB substrate are listed in Table 3.3.

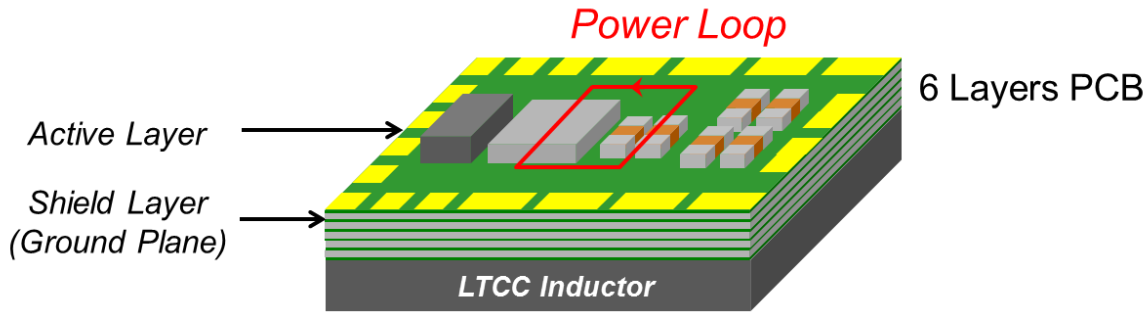


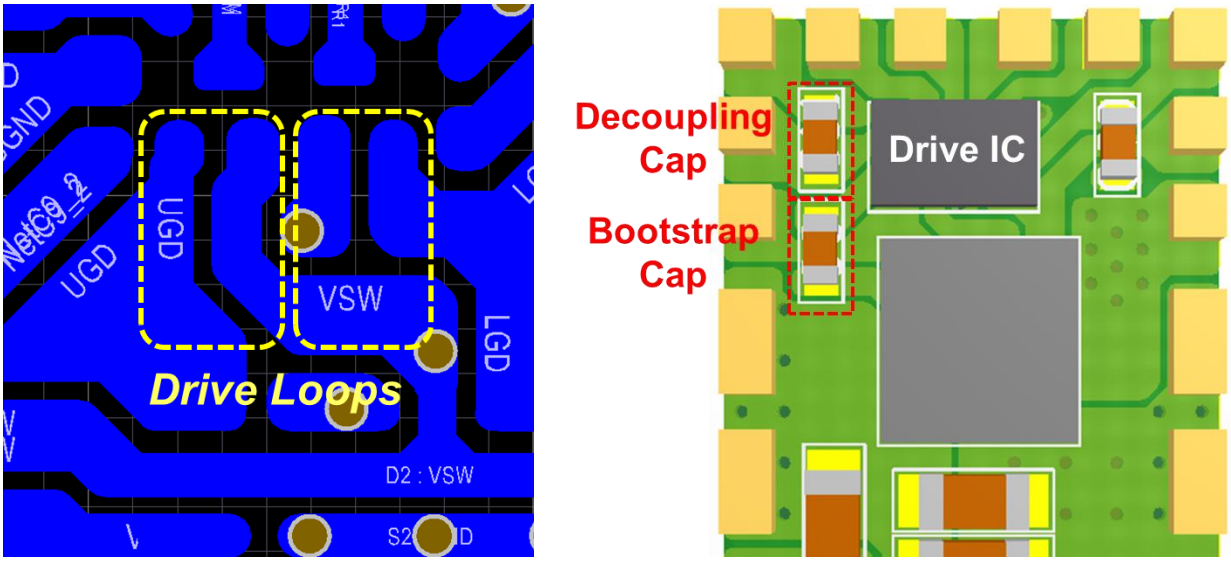
Fig. 3.12: Single phase module with PCB Substrate

Table 3.3: Parameter of single phase PCB substrate.

Layers	6
Copper Thickness	1 oZ
Total Thickness	0.56 mm
Material	BT Epoxy

In this design, the distance between the active layer and shield layer is only 5 mil, therefore, the flux cancelation is effective, and the loop inductance is reduced to 0.18 nH.

Besides the high frequency power loop inductance needs to be minimized, the driving loops are also need to be considered and well designed to minimize the parasitic inductance. Fig. 3.13 shows the PCB layouts for drive loops and the drive IC. As shown in Fig. 3.13 (a), the drive loop traces should be placed side by side to minimize the loop area. The decoupling capacitor and bootstrap capacitor for the drive IC should be placed closely beside the corresponding pins.

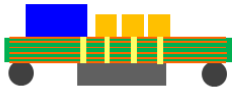
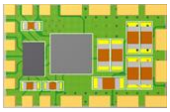


(a) PCB layout for drive loops (b) PCB layout for drive IC

Fig. 3.13: Reducing the drive loop parasitics

The power loop and drive loop parasitics for IR's double side design and CPES' single side design are extracted by Ansoft Q3D and listed in Table 3.4. It can be found that after implementing the shield layer, the loop inductances for CPES' single side design are reduced to be comparable with IR's double side design. The efficiency simulation data also shows that the efficiency of CPES PCB substrate module is very close to IR's module, and is much better than the previous attempt without shield layer as shown in Fig. 3.14. In this way, the easy inductor assembling can be achieved without sacrificing too much efficiency.

Table 3.4: Parasitics comparison for IR and CPES active layers design.

Fs = 2 MHz	Power Loop		Top Drive Loop		Bottom Drive Loop	
	L (nH)	R (mΩ)	L (nH)	R (mΩ)	L (nH)	R (mΩ)
IR 	0.093	0.332	0.406	4.768	0.261	3.743
CPES 	0.183	0.651	0.546	4.448	0.479	3.458

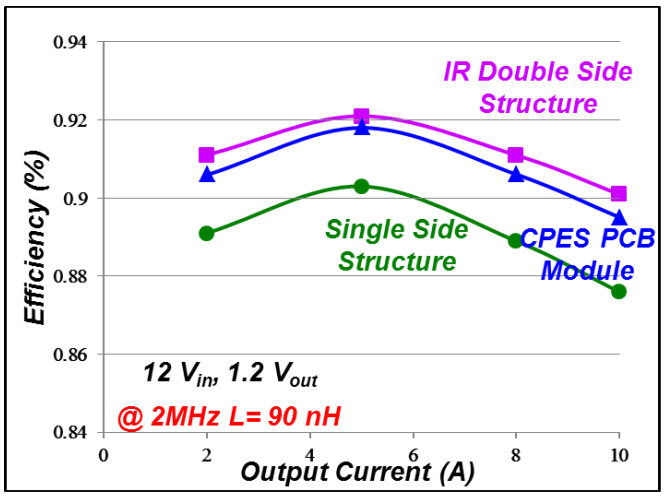


Fig. 3.14: Efficiency simulation data for different substrates design

Fig. 3. 15 shows the final fabricated active layer for the single phase module with the PCB substrate. The dimensions of this PCB substrate are 7.37 mm X 11.68 mm with 85 mm^2 footprint. It also includes 3 X 4.7 uF input capacitors and 4 X 22 uF output capacitors.

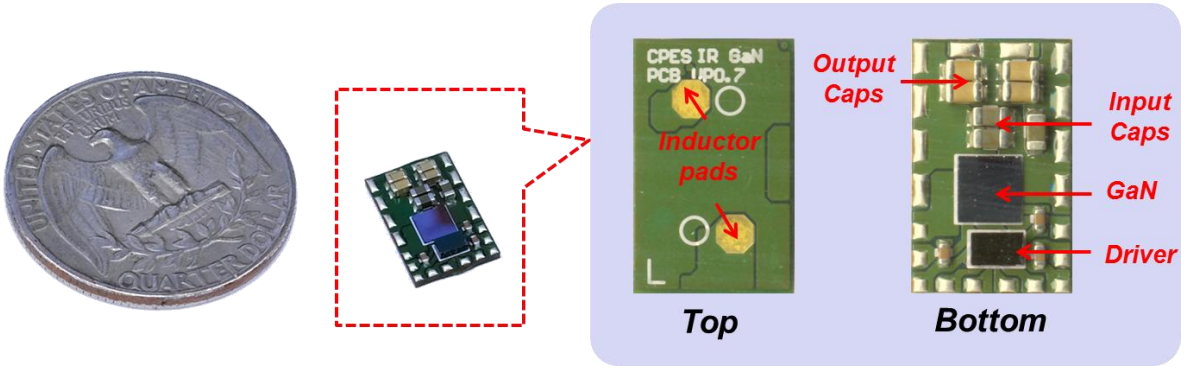


Fig. 3.15: Active layer of single phase module with PCB substrate

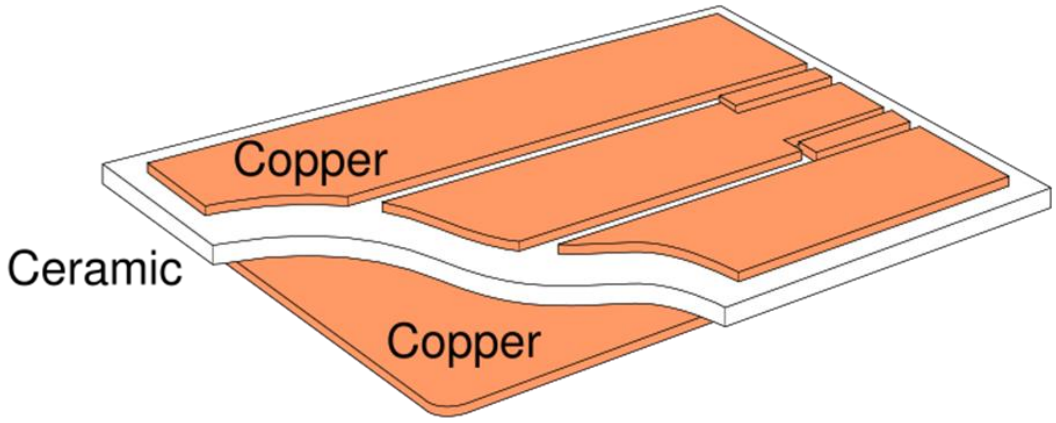
3.4. DBC Substrate Design

3.4.1. Direct Bonded Copper (DBC) Technique

Direct bonded copper (DBC) substrates are commonly used in power modules, because of their good thermal conductivity. They are composed of a ceramic tile with a sheet of copper bonded to one or both sides by a high-temperature oxidation process [42], as shown in Fig. 3.16. The copper layer thickness is usually 5 to 10 Oz. The ceramic materials used in DBC include:

1. Alumina (Al_2O_3), which is widely used because of its low cost. However, it has relative low thermal conductivity (24-28 W/mK).
2. Aluminum nitride (AlN) is more expensive than Alumina, but it has far better thermal conductivity (> 150 W/mK).

3. Beryllium oxide (BeO), which has good thermal performance, but is often avoided because of its toxicity when the powder is ingested or inhaled.



Ref: *Wikipedia, "Power electronic substrate"*

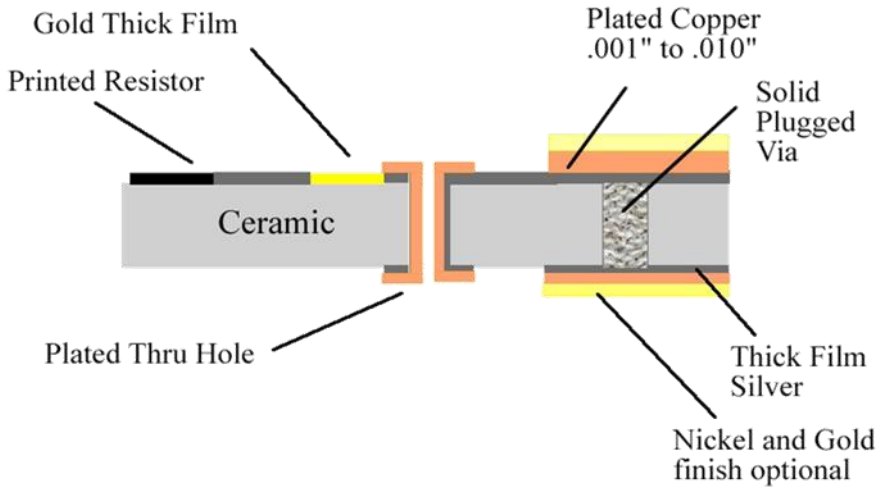
Fig. 3.16: Structure of DBC substrate

The properties of the DBC substrate are [43]:

- Very good thermal conductivity
- Superb thermal cycling stability
- Good heat spreading
- Good mechanical strength, mechanically stable shape
- Excellent electrical insulation
- Good adhesion and corrosion resistant
- Environmentally clean

All the properties bring the advantages to the user for high current loading capability, high power density in module design. However, the IR's GaN transistor in this work has a 15 mil pinch for small package parasitics, and requires 8 mil vias on the pads to reduce the layout parasitics. Furthermore, thin ceramic layer is desirable to place the shield layer more close to the

active layer to reduce the loop inductance. The common DBC technique cannot meet these requirements. The new emerging DBC technique called Direct Plated Copper (DPC) [44] or Plated Copper on Thick films (PCTF) [45] can solve this issue. This new technique is created for better electrical performance and better flexibility because of its fine line capability and solid copper via fill. As shown in Fig. 3.17, the copper is plated to the ceramic substrate instead of being bonded; therefore, the copper layer thickness can be flexible from 1 to 10 mil. The holes can be drilled by laser and filled by mental on the ceramic substrate before the copper plating process; therefore, it is easy to make the vias. The comparison between common DBC technology and new DPC technology is listed in Table 3.5 [46].



Ref: *Remtec, "Core Technology: Plated Copper on Thick films (PCTF ®) Technology"*

Fig. 3.17: Structure of DPC substrate

Table 3.5: Comparison between common DBC and new DPC technology.

	Common DBC Technology	**DPC Technology**
Copper Thickness (Oz)	5 ~ 10	1 ~ 7
Trace Clearance (Mil)	20	3

Ceramic Thickness (Mil)	20 ~ 40	10 ~ 40
Minimum Via Diameter (Mil)	40	3
Via Feasibility	Very Difficult	Can be made and filled easy

3.4.2. DBC Substrate for Single Phase Module

In the previous practice of designing the high power density POL module, the DBC substrate has demonstrated its better thermal performance compared with the common PCB substrate. The maximum temperature can be reduced, and the hot spots can be eliminated [47]. The thermal conductivity for FR4 epoxy, which is the common material for PCB board is 0.27 W/mK. The thermal conductivity for Alumina ceramic substrate of DBC is 24 ~ 28 W/mK, which is 90 times better than FR4. The AlN substrate has a much higher thermal conductivity of over 150 W/mK. In this thesis work, an Alumina DBC substrate is also designed for the GaN module to achieve better thermal performance.

Fig. 3.18 shows the PCB and DBC substrates for the single phase GaN module. These two substrates have the same footprint, same top layer and bottom layer traces layout. However, the DBC substrate only has two layers of copper; the PCB substrate has 6 layers of copper. The parameters of DBC substrate are listed in Table 3.6.

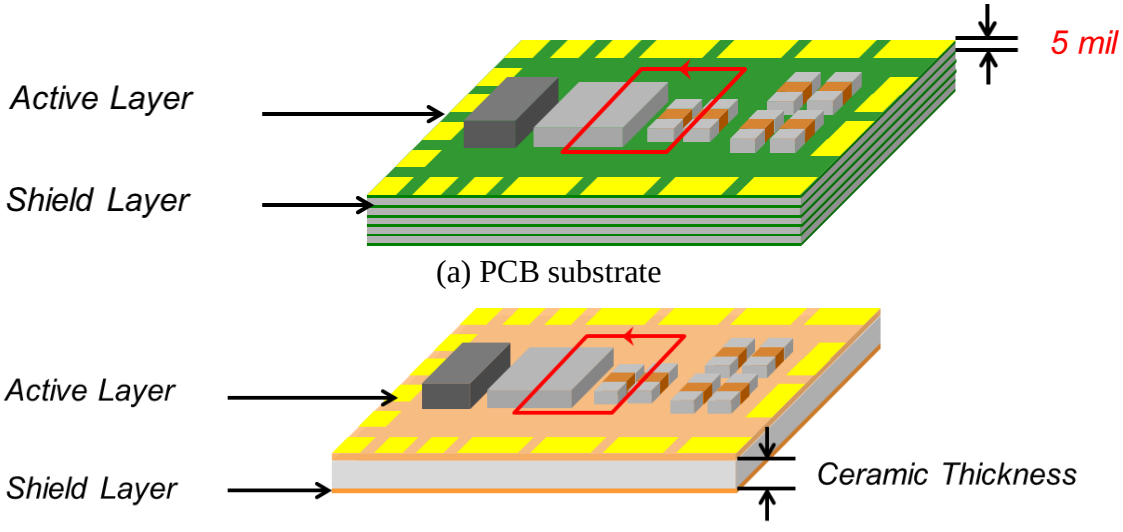
(a) PCB substrate (b) DBC substrate

Fig. 3.18: PCB & DBC substrate for single phase modules

Table 3.6: Parameters of single phase DBC substrate

Layers	2
Copper Thickness	2 oZ
Total Thickness	0.4 mm
Material	Alumina

As shown in Fig. 3.19, for a PCB substrate, the shield layer can be placed very close to the active layer with only 5 mil distance. The loop inductance is only 0.18 nH. For a DBC substrate, since it only has two layers of copper: one layer is for the active layer, and the other layer is for the ground plane/shield. The distance between the active layer and shield layer is the thickness of the ceramic, which is usually 10 ~ 40 mil. For the 40 mil thickness, the loop inductance is 0.57 nH, it is much higher than PCB substrate.



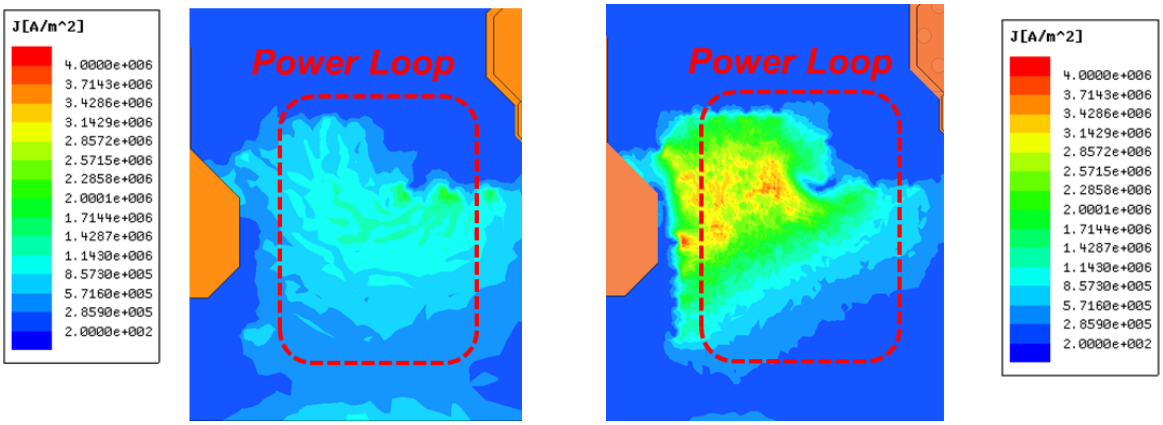
(a) PCB substrate

(b) DBC substrate

Fig. 3.19: Distance between active layer and shield layer for PCB & DBC substrates

In Fig. 3.20, the eddy current FEA simulation results for 40 mils and 10 mil ceramic substrates are compared. It can be seen that the eddy current is much stronger in 10 mil substrate

than in the 40 mil one, which means stronger flux cancellation effect, hence smaller loop inductance. Fig. 3.21 gives the FEA simulation results for loop inductance with different ceramic thicknesses. The results show a clear trend that the loop inductance can be reduced with smaller ceramic thickness. 10 mil of thickness DBC only has half of loop inductance of 20 mil DBC. However, in practical, 10 mil is the minimum thickness for the DBC substrate, less than 10 mil will be too fragile to be fabricated. Therefore, 10 mil DBC substrate is chosen for this thesis work.



(a) 40 mil thickness (b) 10 mil thickness

Fig. 3.20: Eddy current FEA simulation results

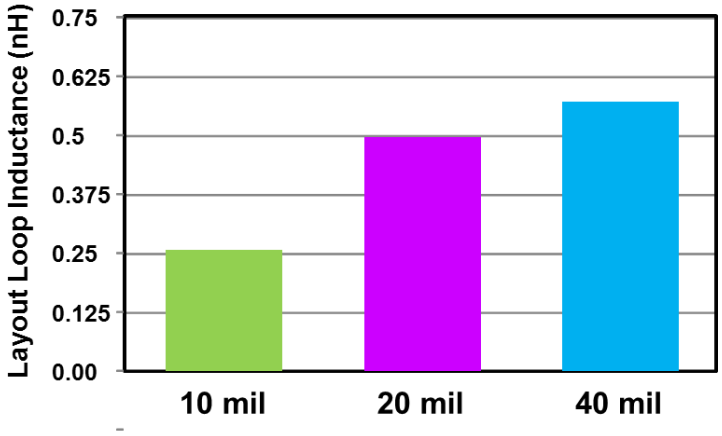
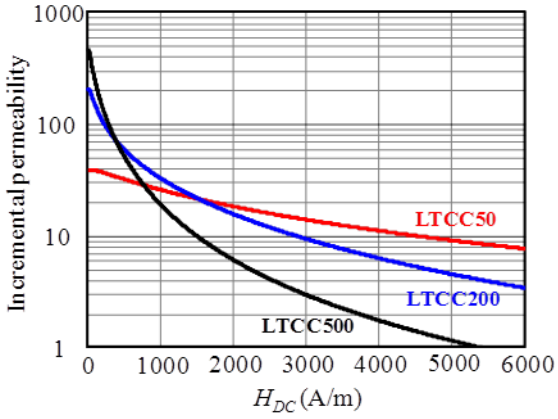


Fig. 3.21: Loop inductance vs ceramic thickness

3.5. Inductor Substrate Design

3.5.1. LTCC Inductor [48]

High operating frequency and integration technique are two main approaches to achieve high power density for the switching mode power supply. The GaN technique provides the capability of multi-MHz operation frequency and high output current. The Low Temperature Co-fire Ceramic (LTCC) technique provides the better performance for high frequency operation and more importantly, the 3D integration capability for POL modules. In the meantime, The LTCC based integration can have good thermal performance, which is critical for high current application. Furthermore, as a thick film technology, it is very easy to use LTCC technology to fabricate a sufficiently thick magnetic core and winding for high output current [48].

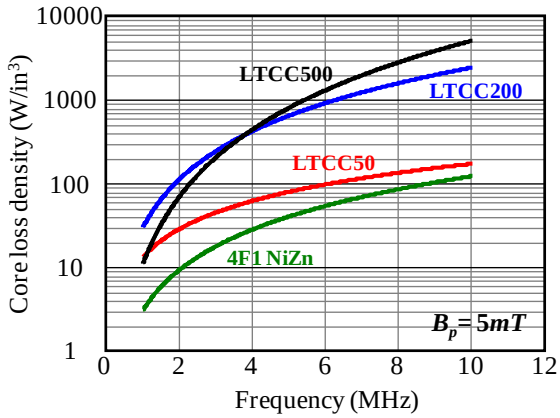


Ref: *Yipeng Su, Qiang Li, and Fred Lee, " Design and Evaluation of High Frequency Inductor Substrate for 3-Dimension Integrated DC/DC Converter,"*

Fig. 3.22: Incremental permeability as a function of HDC for different LTCC materials.

Three different LTCC magnetic materials, 40010, 40011 and 40012, are commercialized in ESL ElectroScience®. They are herein nominated as LTCC50, LTCC200 and LTCC500, in which the numbers represent their initial permeability. The key magnetic properties of the LTCC

materials, such as the permeability and core loss density, are experimentally characterized in [49]. The incremental permeability as a function of DC bias (H_{DC}) for different LTCC materials is shown in Fig. 3.22. For the high current POL application, the H_{DC} of the majority of the core is larger than 1000 A/m. In this DC bias range, the LTCC50 has the largest incremental permeability, which results the smallest inductor size.

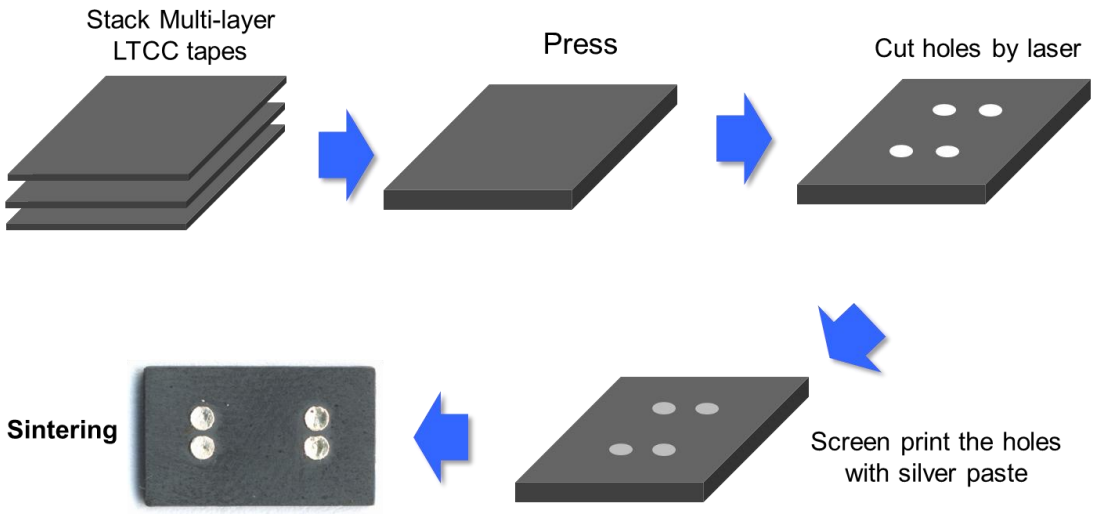


Ref: *Yipeng Su, Qiang Li, and Fred Lee, " Design and Evaluation of High Frequency Inductor Substrate for 3-Dimension Integrated DC/DC Converter,"*

Fig. 3.23: Core loss density comparison for different LTCC materials

Core loss at high operating frequency is another criterion for material selection. The core loss densities of the LTCC materials are compared as Fig. 3.23 in the interested operation frequency range from 1MHz to 10MHz. The core loss density of LTCC50 is one to two orders of magnitude lower than that of LTCC200 and LTCC500 at the same AC flux excursion; it is also close to the NiZn ferrite (4F1) material which in known as a loss density magnetic for high frequency [50]. Therefore, the LTCC50 is selected as the core material to design the inductor in this thesis work, due to its low loss density at high frequency and high incremental permeability at large DC bias condition.

Fig. 3. 24 shows the fabrication process for the LTCC inductor. Since the LTCC magnetic material comes in tape form, the first step is to cut the LTCC green tape to the designed size and stack the needed layers together. After these stacked layers have been pressed, the holes are cut by laser and then screen printed with silver paste. The last step is sintering in the oven with a specified temperature curve [51].



Ref: Yipeng Su, "Inductor Design for GaN POL", PMC Quarter Review, 2011.04

Fig. 3.24: LTCC inductor fabrication process

3.5.2. Inductance Selection

For the Buck converter, the output inductance is determined by:

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I_{PP} \cdot f_S} \cdot D \tag{3.1}$$

Where, Vin is the input voltage, Vout is the output voltage, f_S is the operation frequency, and D is the duty cycle, and ΔI_{PP} is the peak-to-peak ripple current of inductor, assume:

$$\Delta I_{PP} = k \cdot Io \tag{3.2}$$

Where Io is the maximum DC output current, k is the ripple factor. In here it is set to 30%,

60%, 90%, 120%, and 150%.

By the core loss model develop in [52], the core loss for 12V to 1.2V, 10A converter at different peak-to-peak current ripples can be calculated as shown in Fig. 3.25. The module efficiency also can be calculated by the simulation model as shown in Fig. 3.26.

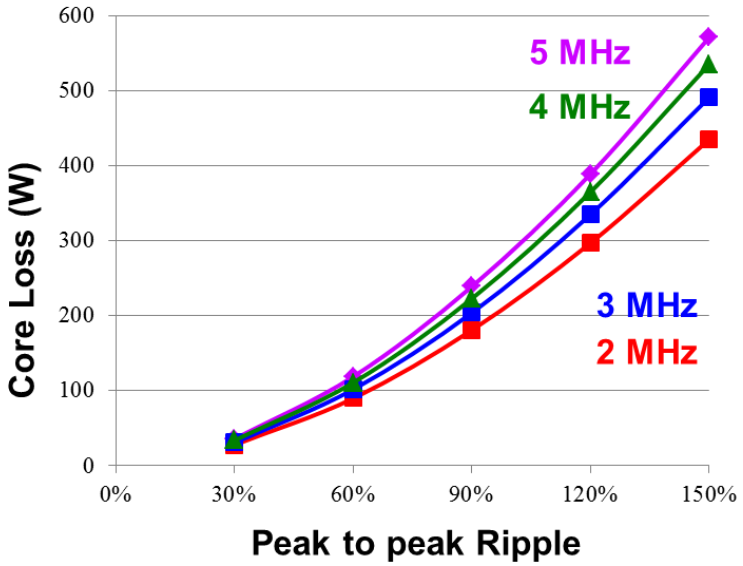


Fig. 3.25: Core loss vs inductor current ripple

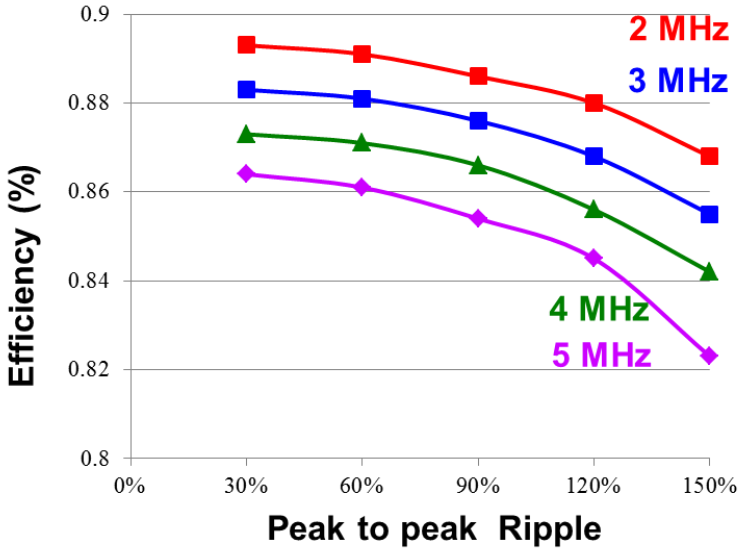


Fig. 3.26: Efficiency vs inductor current ripple

It can be found that the large current ripple will result high core loss and also low efficiency. However, low current ripple means large inductance which requires more layers of LTCC green tape. After the trade-off between efficiency and inductor manufacturability, 60% of the output current ripple is chosen for this thesis work, which results 90 nH, 60 nH, 45 nH, and 36 nH inductance for 2 MHz, 3 MHz, 4 MHz, and 5 MHz operation frequencies respectively, as shown in Fig. 3.27. All these four inductors have same 2 turn structure and same footprints as the active layer. It can be seen that the core thickness and number of LTCC green tape layers are all reduced; hence the total cost is reduced at high frequency.

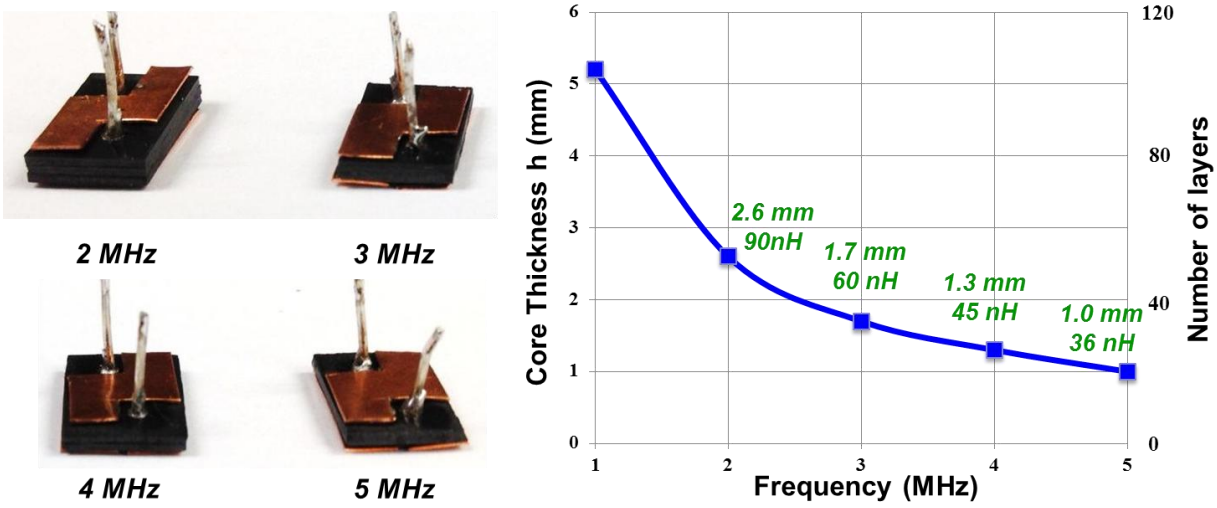


Fig. 3.27: LTCC inductors for single phase module

3.6. Integration Process and Efficiency Evaluation

3.6.1. 3D Integration Process for the Single Phase Modules

After the active layer and LTCC inductor have been designed and fabricated, the next step is to integrate them together to form a module. Fig. 3.28 shows the structure of the final single

phase GaN module. This structure includes three basic parts: the active layer, the passive layer, and the Thermal Interface Material (TIM) in the middle. The active layer is the substrate with the GaN transistors, driver, input/output capacitors, and input/output pins assembled on one side. The passive layer is the LTCC magnetic core with copper trances on both sides.

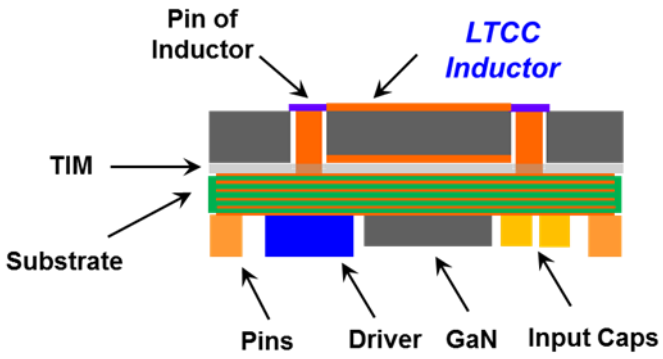


Fig. 3.28: Structure of single phase GaN module

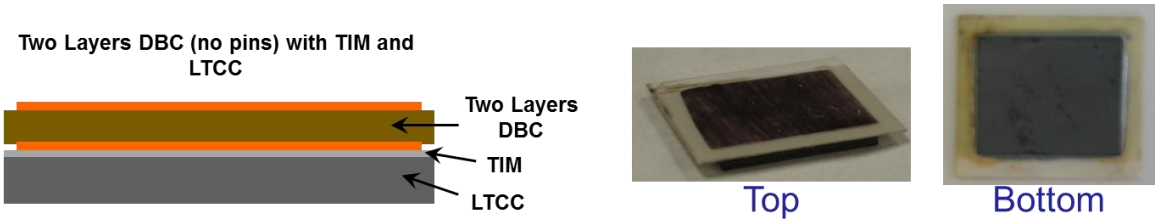
The purpose of the TIM is to provide the electrical isolation between the active copper layer and the inductor copper traces, also to alleviate the stress caused by the different Coefficient of Thermal Expansion (CTE) of DBC substrate and the LTCC inductor. Therefore, this TIM needs to provide the electrical isolation and good thermal conductivity at the same time.

Table 3.7: Thermal interface material candidates

Manufacturer	**Product**	**Thermal Conductivity W/mK**	**Curing**	**Comments**
TechFilm	T2521F4	0.9	60min @ 150C	Excellent Adhesion to Ceramic and Metal
	T2222F4	0.75	60min @ 150C	High Bond Strength for difficult to bond substrates
MasterBond	Supreme10ANHT	3.1	60min@ 150C	Ideal adhesive for bonding dissimilar substrates when high thermal conductivity is needed, readily thermally cyclable

Three TIM candidates from TechFilm [53] and MasterBond [54] are listed in Table 3.7. In

order to find out which one is the best choice, a two layer DBC, the TIM, and LTCC core are assembled for the thermal cycling test as shown in Fig. 3.29. These samples are then cycled from -40 C to 150 C. After 150 cycles, no visual breakdown of any materials, therefore, the Supereme10ANHT from MasterBond is chosen for this thesis for because of its highest thermal conductivity among these three materials.



Ref: *David Gilham, " Integration of GaN POL Module",HDI Quarter Review, 02,2012*

Fig. 3.29: Thermal cycling test for TIM

The fabrication process for the GaN modules includes the following steps as shown in Fig. 3.30: (1) solder the GaN transistors, driver, capacitors, and input/output pins to the substrate; (2) solder two pins on the other side of substrate for inductor assembling; (3) add one TIM layer between the active layer and inductor; (4) put the LTCC inductor on top of TIM layer, the bottom copper trance has been soldered with two filled vias, the other two vias are left open; (5) solder the top copper traces with pins; (6) curing the module at 150 degree C for an hour to solidify the TIM layer. The assembled single phase GaN modules with PCB and DBC substrates are shown in Fig. 3.31. The components layout and Bill of Material (BOM) are listed in Fig. 3. 32 and Table 3.8.

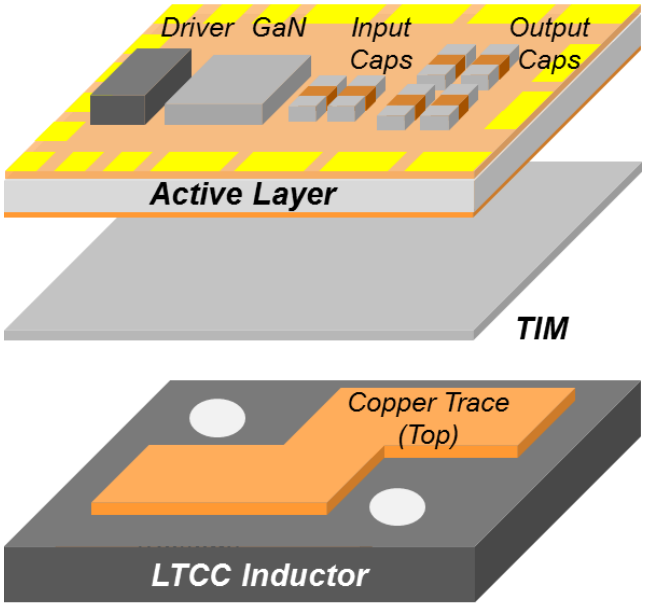
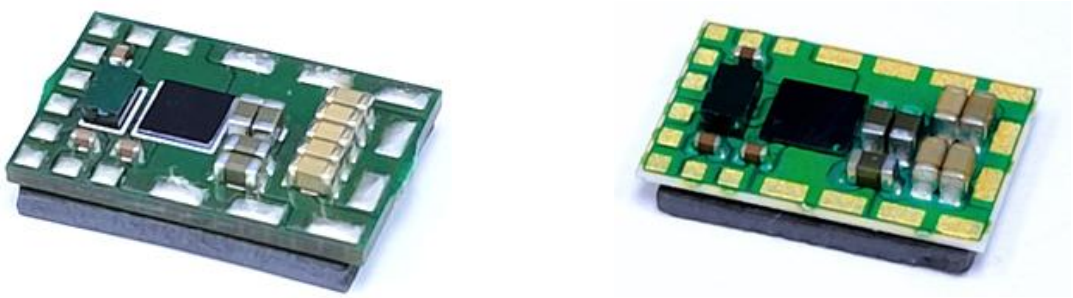


Fig. 3.30: GaN module integration process



(a) PCB module (b) DBC module

Fig. 3.31: Single phase GaN modules

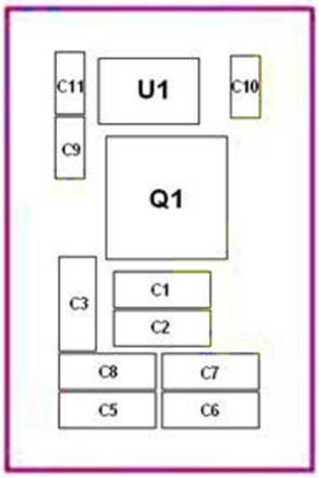


Fig. 3.32: Single phase GaN module components layout

Table 3.8 : Bill of Material for single phase GaN module

Number	Description	Part Number	Quantity	Manufacture
C1,C2,C3	Input Capacitors, 4.7 uF/16V, 0603	EMK107ABJ475	3	TDK
C5,C6,C7,C8	Output Capacitors, 22 uF/4V, 0603	GRM188R60G226ME	4	Murata
C9,C10,C11	Decoupling Capacitors, 0.1 uF/25V, 0402,	CGA2B3X7R1E104K	3	TDK
U1	GaN Driver		1	IR
Q1	Monolithic Integrated GaN Transistors		1	IR
Substrate	PCB Substrate, 6 Layers, 1oZ Copper		1	Metrocircuits
	DBC Substrate, 2 Layers, 2oZ Copper		1	REMTEC
TIM	Thermal Interface Material	Supreme10ANHT	1	MasterBond
Inductor	LTCC 50 Magnetic Material		1	CPES
Pin	Input/Output Copper Pins		20	METAL PROCESSING

3.6.2. Single Phase Modules Efficiency Evaluation

Fig. 3.33 shows the single phase GaN module mounted on the test board for the efficiency evaluation. Two resistors are also mounted on the test board to fine-tune the overlap time for drive signals to achieve the best efficiency.

Fig. 3.34 shows the efficiency data for single phase PCB module with 12 V input/1.2 V output, 10 A output current conversion. This module is tested at 2 MHz, 3 MHz, 4 MHz, and 5 MHz operation frequencies with designed inductance as marked in the pictures. In order to find out the efficiency and temperature of higher output current, this module is also tested at 15A output current as shown in Fig. 3.35.

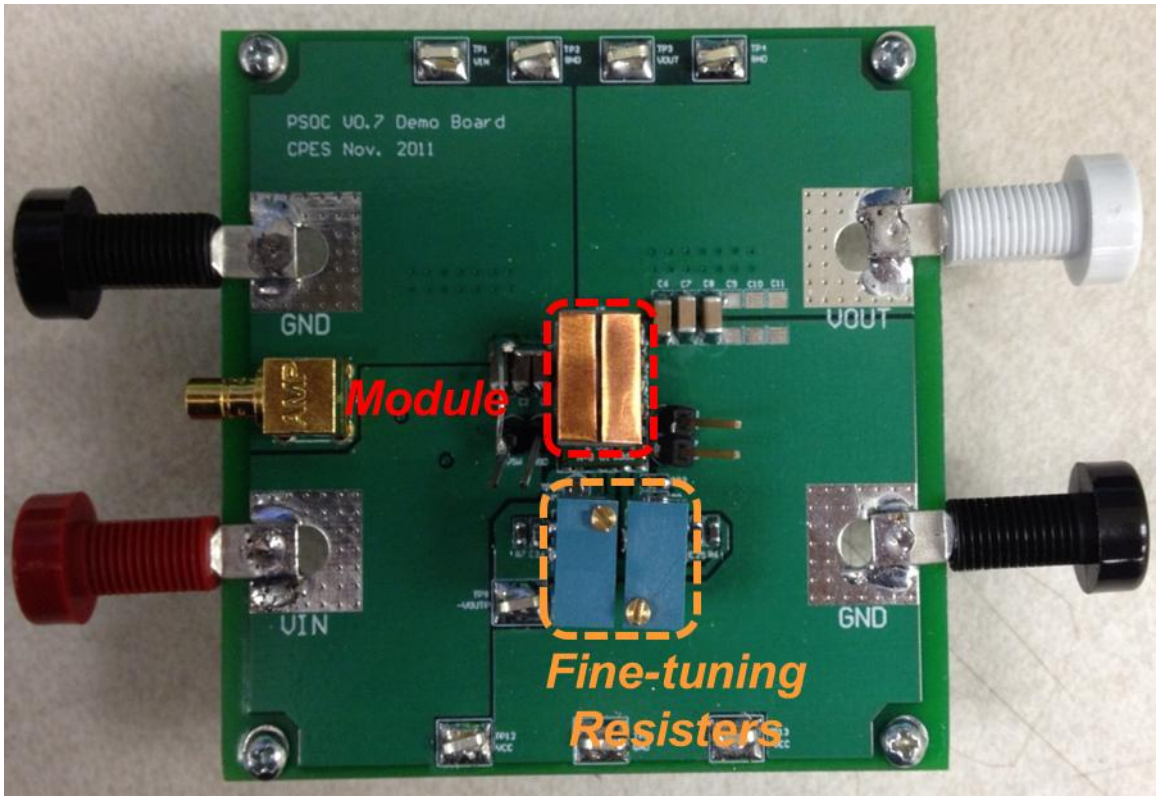


Fig. 3.33: Single phase GaN module with test board

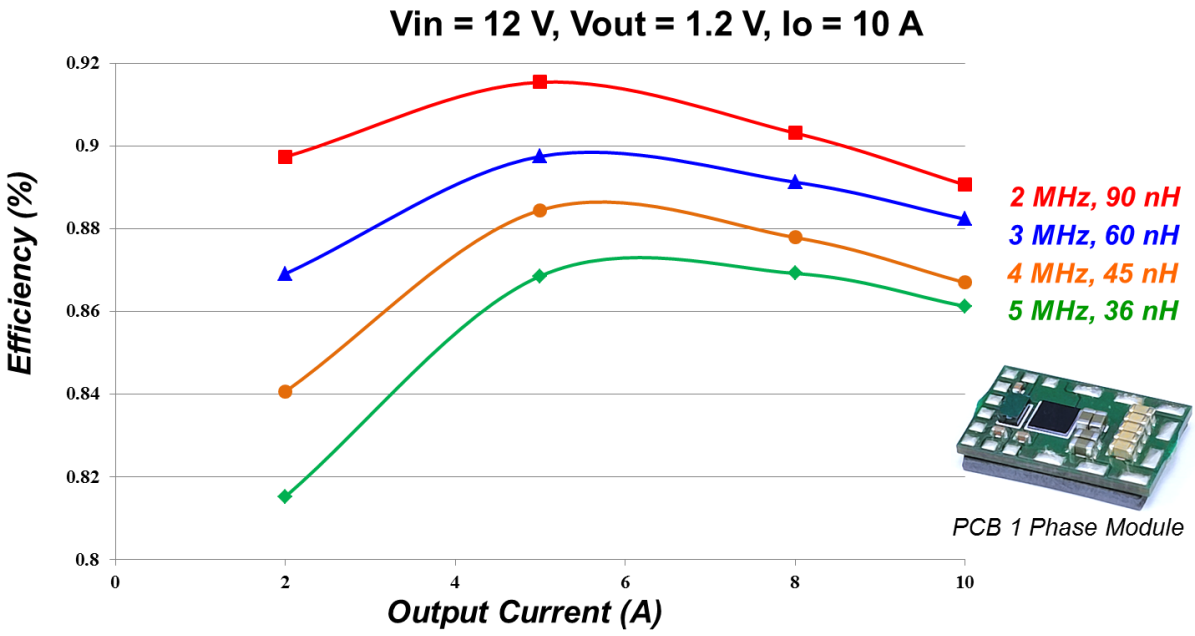


Fig. 3.34: PCB module 1.2V/10A efficiency data

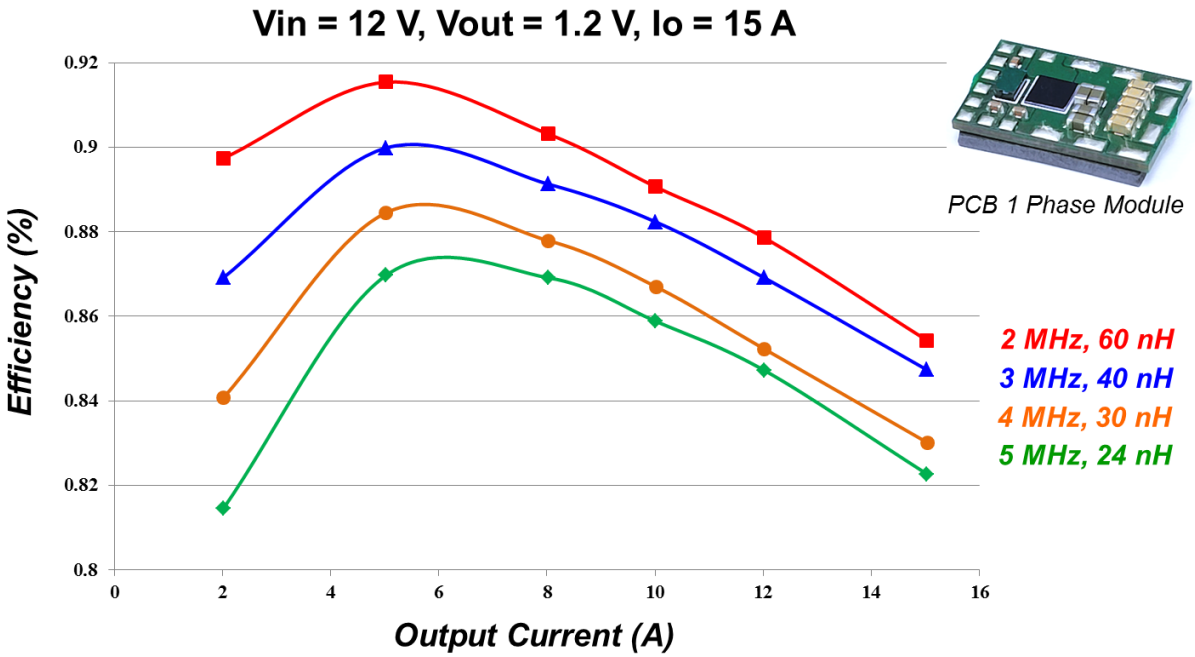


Fig. 3.35: PCB module 1.2V/15A efficiency data

Since the latest Intel VRM 12.5 specification has modified the VRM input voltage from 1.2 V to 1.8V, the 1.8V output efficiency is also tested as shown in Fig. 3. 36.

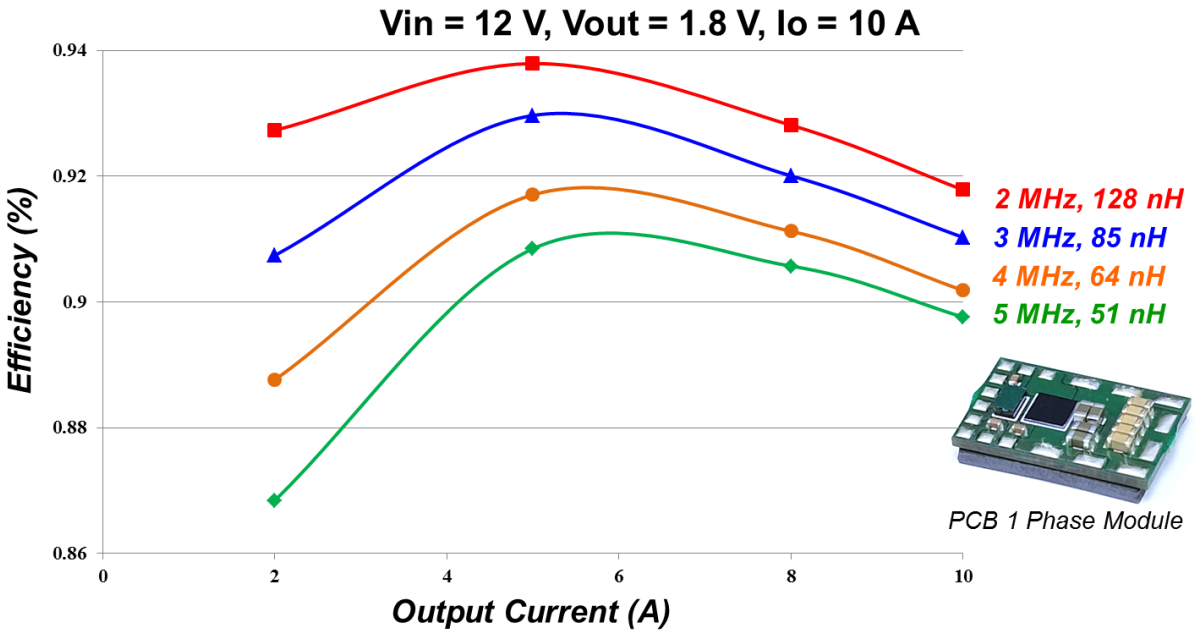


Fig. 3.36: PCB module 1.8V/10A efficiency data

The GaN modules with DBC substrate are also tested at the same condition, the efficiency data are shown in Fig. 3. 37, Fig. 3.38, and Fig. 3.39.

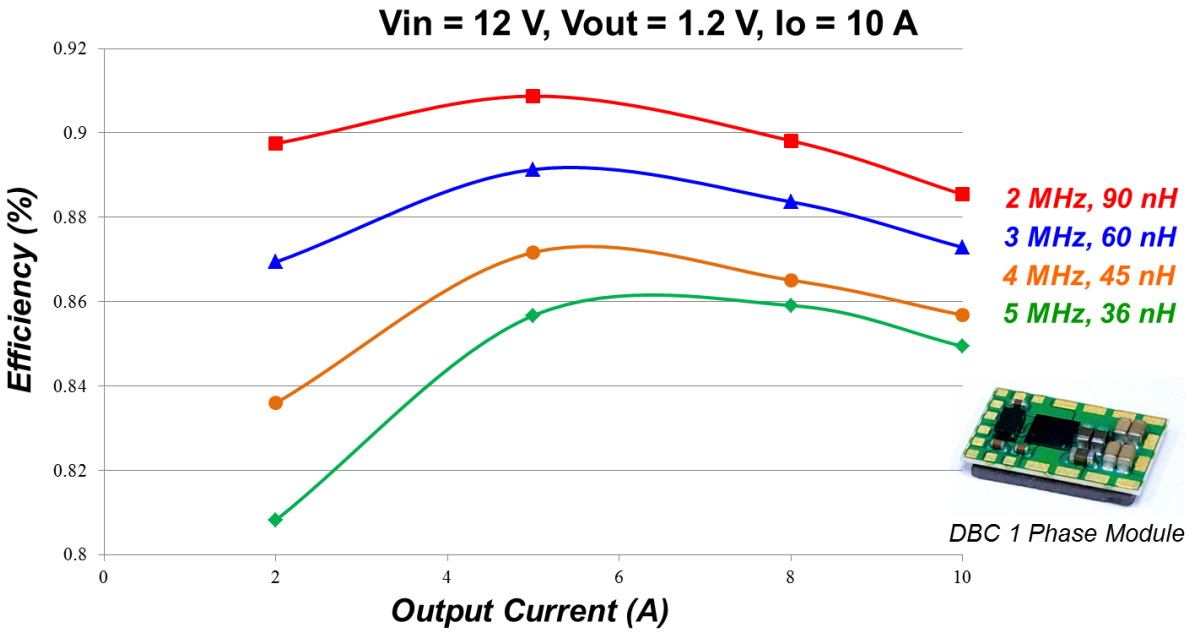


Fig. 3.37: DBC module 1.2V/10A efficiency data

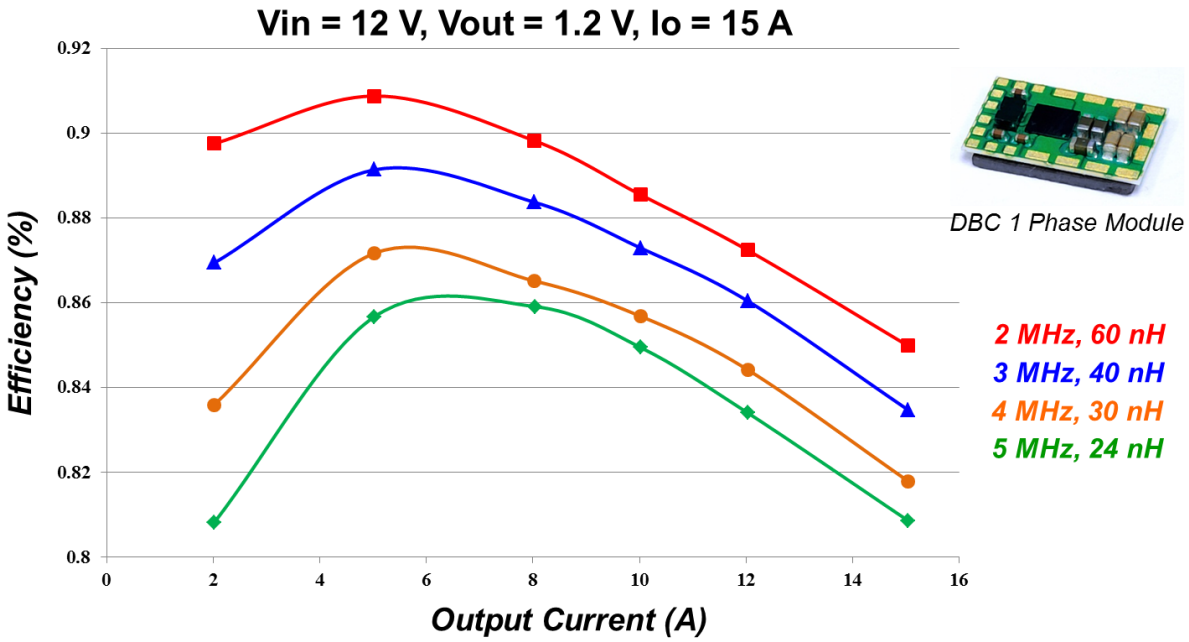


Fig. 3.38: DBC module 1.2V/15A efficiency data

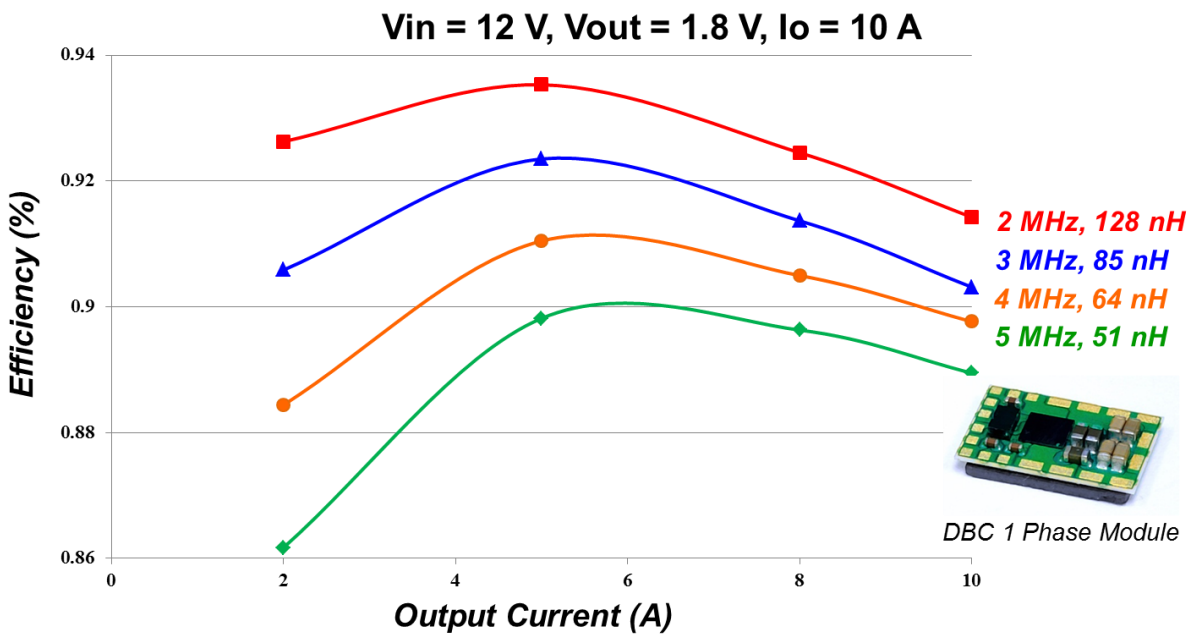
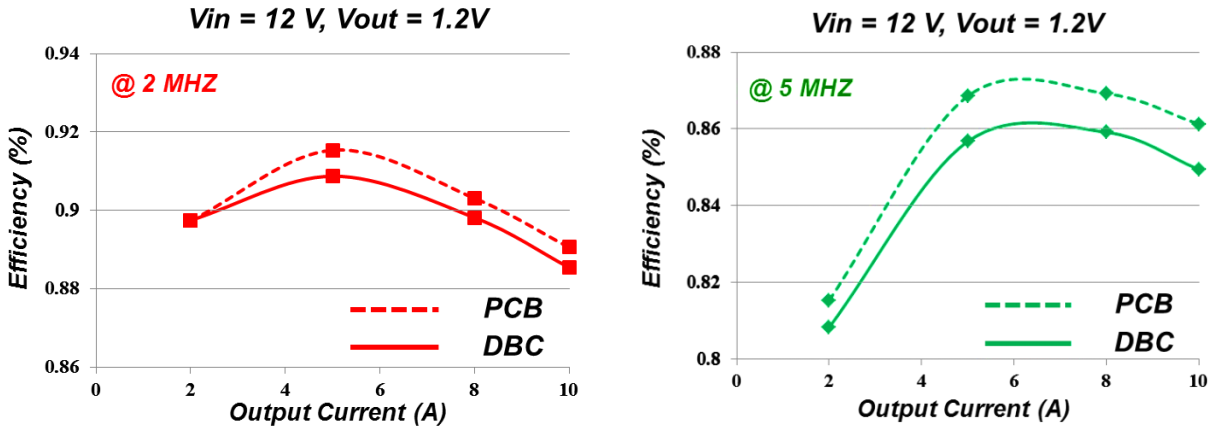


Fig. 3.39: DBC module 1.8V/10A efficiency data

The testing data show both PCB and DBC GaN modules have good efficiencies at any operation frequencies. The GaN modules can achieve about 89% efficiency for 1.2 V/ 10A at 2 MHz frequency. Even at 5 MHz frequency, the efficiency still can achieve 85% ~ 86%, it is at the same level with the industry products that are working at lower than MHz frequency.

Comparing the efficiency data for DBC and PCB modules, as shown in Fig. 3.40, it can be found that the PCB module has higher efficiency than the DBC module. At 2 MHz operation frequency, PCB module has 0.5% higher efficiency than DBC module; at 5 MHz operation frequency, PCB module has 1% higher efficiency than DBC module. The efficiencies difference is caused by the different power loop inductances. As prior elaborate, the PCB substrate has 0.18 nH loop inductance, lower than 0.25 nH for the DBC substrate. Therefore, PCB module has higher efficiency than DBC module, especially at higher operation frequency.



(a) @ 2 MHz (b) @ 5 MHz

Fig. 3.40: Efficiency comparison for DBC & PCB modules

The thermal performance of PCB and DBC modules are also compared as listed in Table 3.9. At low power loss, both PCB and DBC modules have good thermal performance; the DBC has slightly lower temperature than PCB module. At high power loss, the DBC module shows significant better thermal than PCB module even with higher loss.

Table 3.9: Components temperature for PCB and DBC GaN modules

	PCB Module		DBC Module	
	Io = 10 A Ploss = 2.2 W	Io = 15 A Ploss = 3.26 W	Io = 10 A Ploss = 2.35 W	Io = 10 A Ploss = 3.37 W
T_{GaN} (℃)	67.5	97	63.3	82.9
T_{Driver} (℃)	54.5	76.1	51.5	72
Vin = 12V, Vout = 1.2V, Fs = 5MHz, TA = 21 ℃, No Air Flow				

3.7. Two Phase GaN Modules Design

3.7.1. Two Phase Coupled Inductor [51]

Two phase interleaved structure has been demonstrated the benefits of pushing high output current and high power density. In order to push the output current to a higher level, the two phase modules with both PCB and DBC substrates are also designed in this thesis work.

Instead of building two separate inductors for the two phase interleaved POL converter, the inversed coupled LTCC inductor substrate is used. The structure of LTCC coupled inductor is illustrated in Fig. 3.41. Two windings are embedded in one LTCC core, so their flux is magnetically coupled together. With the marked current direction, the inversed coupling between the two inductors is realized, which means the flux lines created by the currents of different inductors are in reversed direction. Compared with the single phase non-coupled LTCC inductor, the inversed coupled LTCC inductor has two significant benefits. First, the equivalent transient inductance, which impacts the transient speed of the converter, becomes smaller than the equivalent steady state inductance, which determines the steady state current ripple of the converter. So the high efficiency and fast transient can be achieved at the same time [55]. Secondly, most of the DC flux in the core is cancelled by the inversed coupling. The core of LTCC coupled inductor is working at much lower DC bias condition than that of single phase inductor is [48]. Fig. 3.42(a) shows the DC flux distribution of the single phase non-coupled inductor with 15 A DC bias current. It can be seen that the H_{DC} value of majority of the core is larger than 2000 A/m. If two single phase inductors are inversed coupled together with 0.35

coupling coefficient and the DC bias current in each phase is still kept as 15 A, the DC operating point of the core can be reduced to around 1000 A/m as shown in Fig. 3.42 (b). The coupling effect can be enhanced by decreasing the distance between two inductors (i.e. d_L). It is illustrated in Fig. 3.42 (c) the coupling coefficient is increased to 0.6 with d_L=0.4 mm, which results the DC operating point of the core is reduced to several hundred A/m. In Fig. 3.41, the solid line is the direction of the inductor current and the dash line represents the flux line in the core.

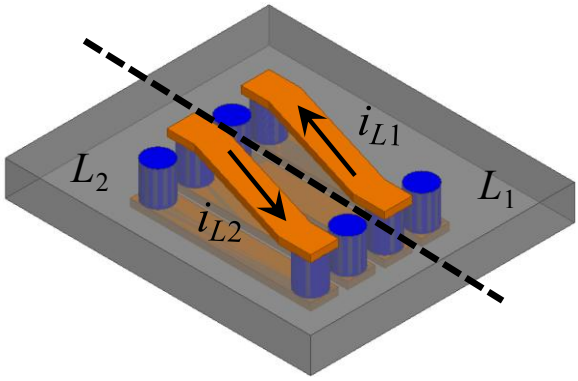
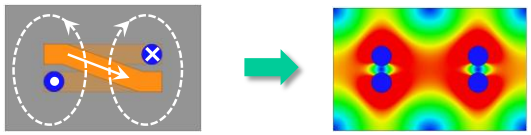


Fig. 3.41. Inversed coupled LTCC inductor structure



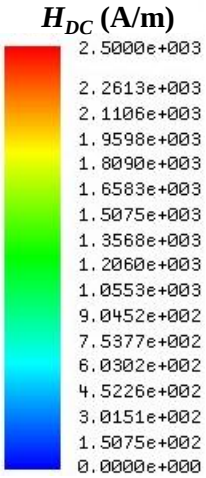


Fig. 3.42(a). DC flux distribution of single-phase inductor with 15 A DC bias

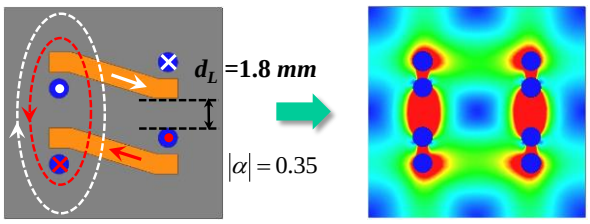


Fig. 3.42(b). DC flux distribution of coupled inductor with 15 A DC bias in each phase (d_L=1.8 *mm* and $|\alpha|$=0.35)

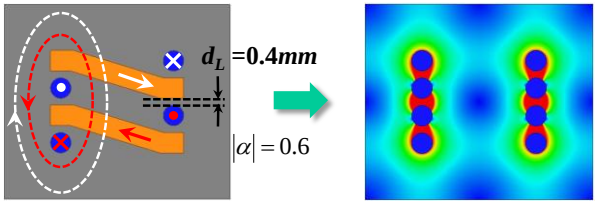


Fig. 3.42(c). DC flux distribution of coupled inductor with 15 A DC bias in each phase (d_L=0.4 *mm* and $|\alpha|$=0.6)

Because of the nonlinear B-H curve of the LTCC magnetic material as prior illustrated in Fig. 3.22, the incremental permeability at low DC bias is larger than that at high DC bias condition. Compared with single-phase inductor, the core volume of the coupled inductor therefore can be further reduced due to the larger permeability.

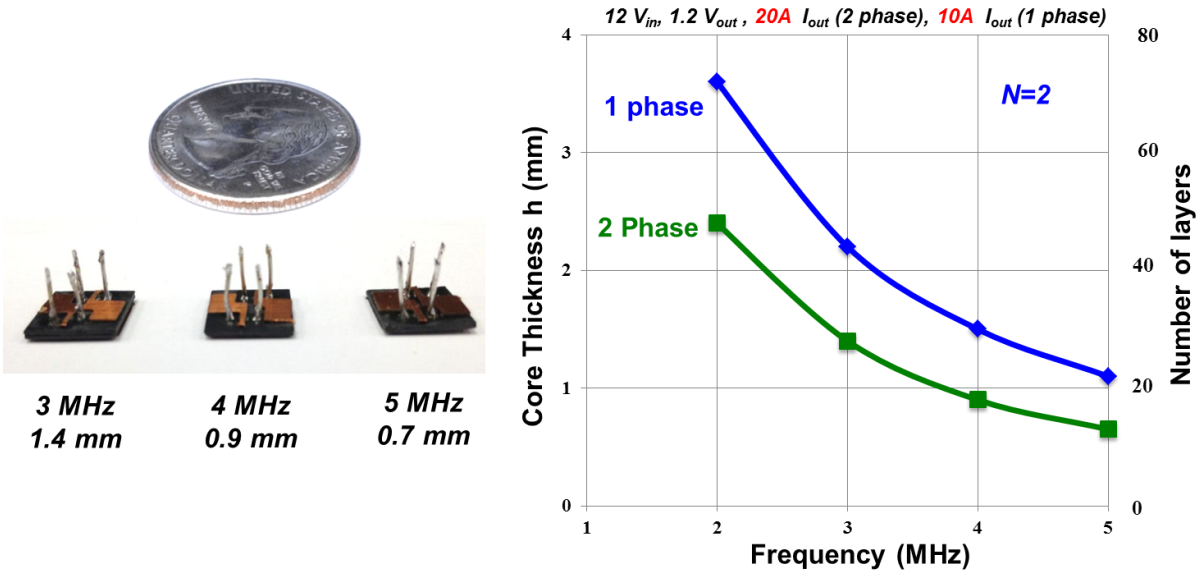


Fig. 3.43: Two phase coupled LTCC inductors

Fig. 3.43 shows the two phase coupled inductors for 3 MHz, 4 MHz, and 5 MHz operation frequency. The steady state inductances are kept same as the single phase module. Because of flux cancellation effect and the non-linear incremental permeability of LTCC material, the core thickness and number of green layers can be reduced for coupled inductor; hence the module

power density can be further increased.

3.7.2. Two Phase Modules with PCB and DBC Substrates

Fig. 3.44 shows the final fabricated two phase module with the PCB and DBC substrates. The dimensions of the substrates are 11.43 mm X 13.21 mm with 150 mm^2 footprint. It also includes 6 X 4.7 uF input capacitors and 4 X 22 uF output capacitors. Compared with the single phase module, the volume is increased 76%, but the output current is increased 100%. The power densities of single phase and two phase modules are shown in Fig. 3. 45. With the benefits or coupled inductor, the two phase module can achieve almost 1000W/in^3 power density.

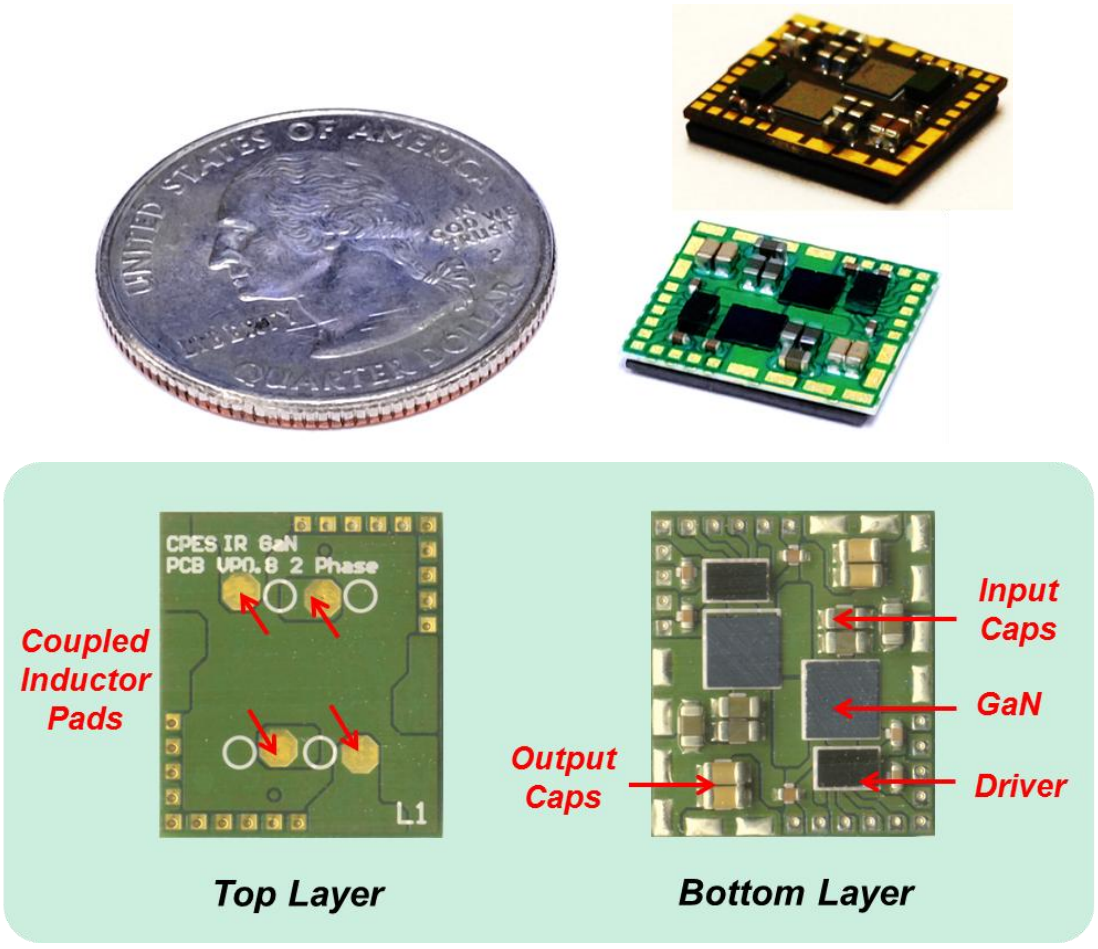


Fig. 3.44: Two phase PCB and DBC GaN modules

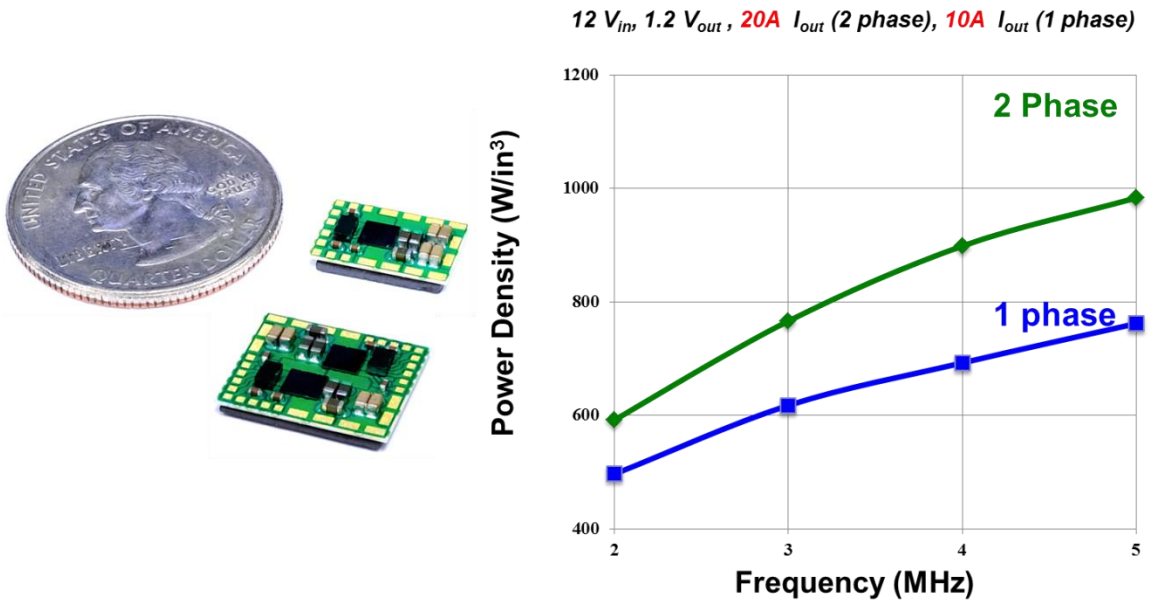


Fig. 3.45: Power densities for single phase and two phase modules

The components layout and BOM are listed in Fig. 3. 46 and Table 3.10.

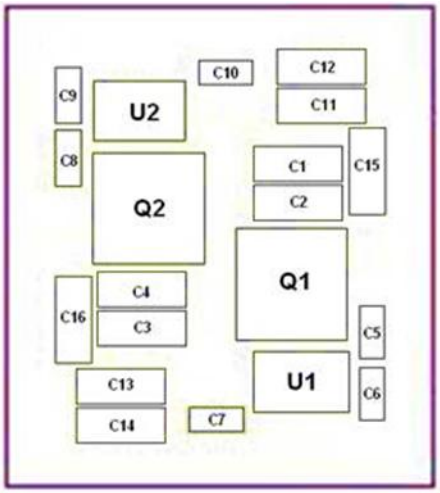


Fig. 3.46: Two phase GaN modules component layout

Table 3.10: Bill of Material for two phase GaN module

	Description	Part Number	Quantity	Manufacture
C1,C2,C3,C4,C15,C16	Input Capacitors, 4.7 uF/16V, 0603	EMK107ABJ475	6	TDK
C11,C12,C13,C14	Output Capacitors, 22 uF/4V, 0603	GRM188R60G226ME	4	Murata

C5,C6,C7,C8,C9,C10	Decoupling Capacitors, 0.1 uF/25V, 0402,	CGA2B3X7R1E104K	6	TDK
U1,U2	GaN Driver		2	IR
Q1,Q2	Monolithic Integrated GaN Transistors		2	IR
Substrate	PCB Substrate, 6 Layers, 1oZ Copper		1	Metrocircuits
	DBC Substrate, 2 Layers, 2oZ Copper		1	REMTEC
TIM	Thermal Interface Material	Supreme10ANHT	1	MasterBond
Inductor	LTCC 50 Magnetic Material		1	CPES
Pin	Input/Output Copper Pins		32	METAL PROCESSING

Same as single phase modules, the two phase modules are also mounted on the test board for efficiency test as shown in Fig. 3.47. The efficiency data for PCB and DBC two phase modules are shown in Fig. 3. 48 and Fig. 3.49. Since the layout of two phase module is very similar to the single phase module, the loop inductances of two phase module are also same as single phase module. Therefore, the two phase PCB module has 0.5% to 1% higher efficiency than DBC module because of its smaller loop inductance.

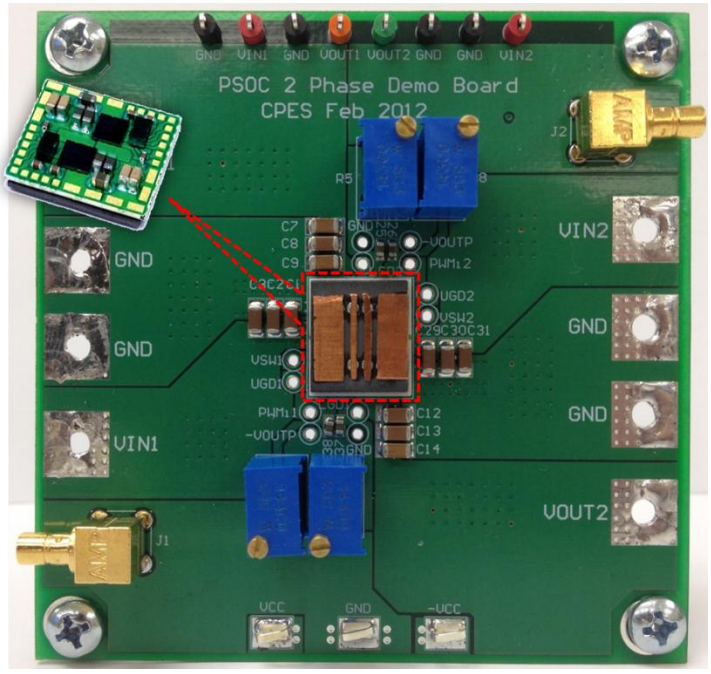


Fig. 3.47: Two phase PCB module with test board

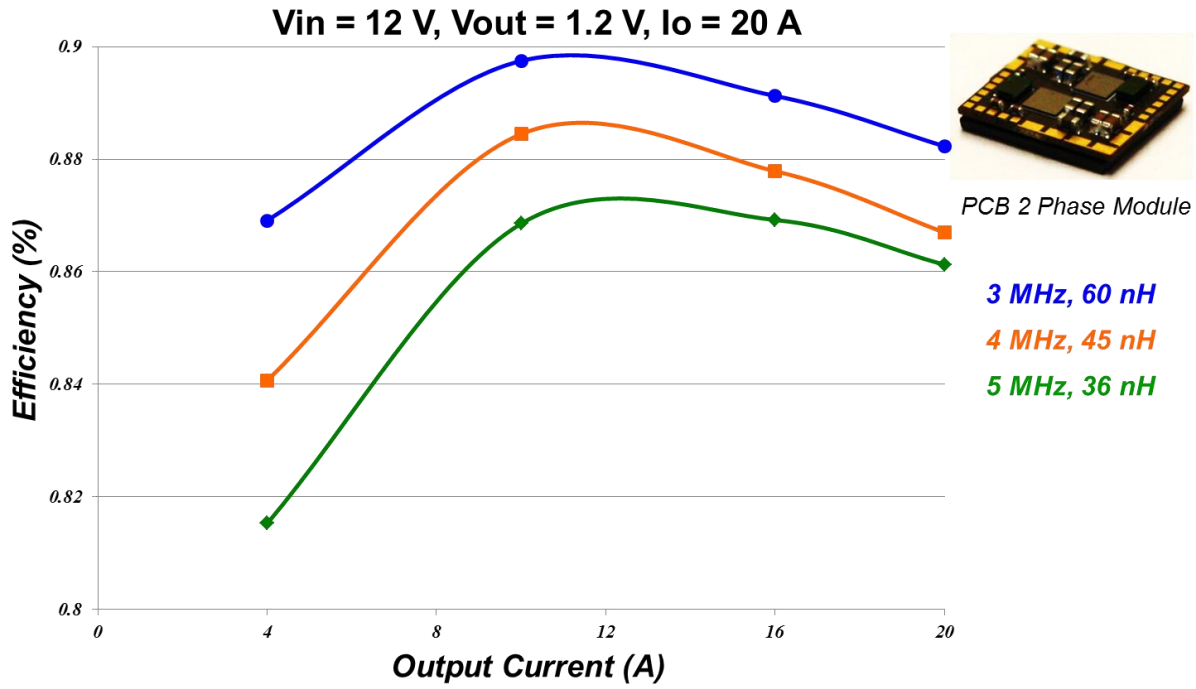


Fig. 3.48: Efficiency for two phase PCB module

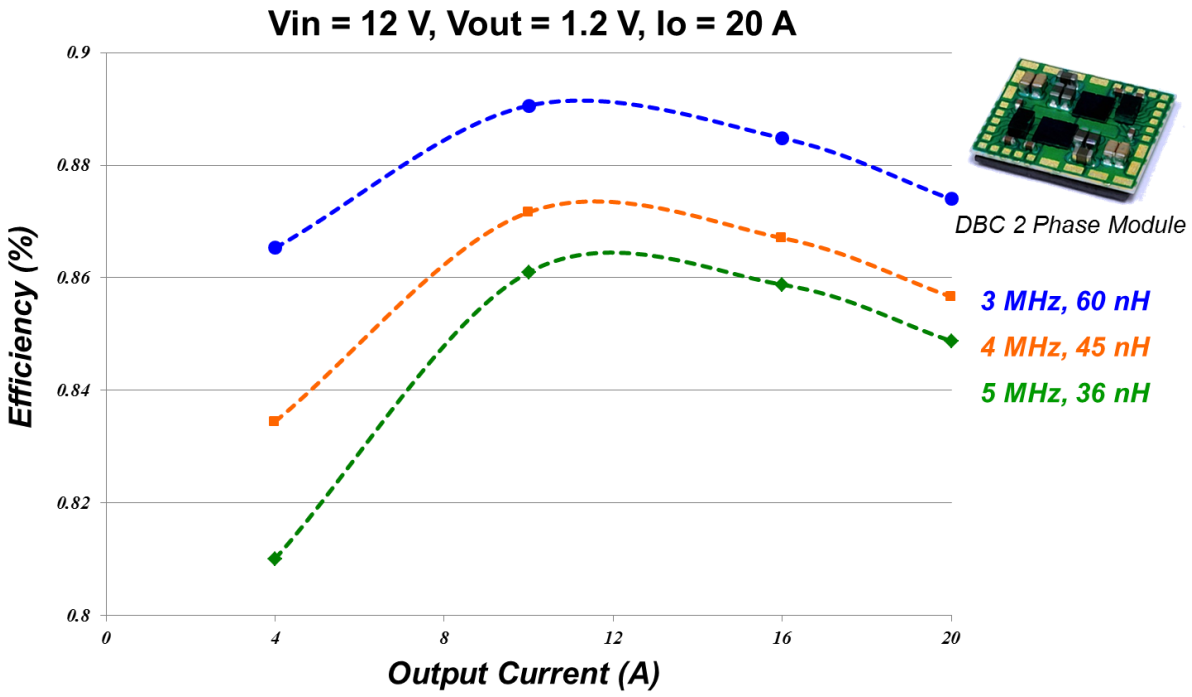


Fig. 3.49: Efficiency for two phase DBC module

The efficiency data for single phase module and two phase module are also compared as

shown in Fig. 3.50. The orange curve is the efficiency for a 20 A two phase module, the red curve is the efficiency for a 10 A single phase module. If divide the current of two phase module by two to get the same current as single phase and redraw the efficiency curve as the blue one, it can be found that the blue curve and red curve are almost overlapped, which means the two phase module and single phase module have the same efficiency. The two phase modules achieve higher power density but do not scarify the efficiency.

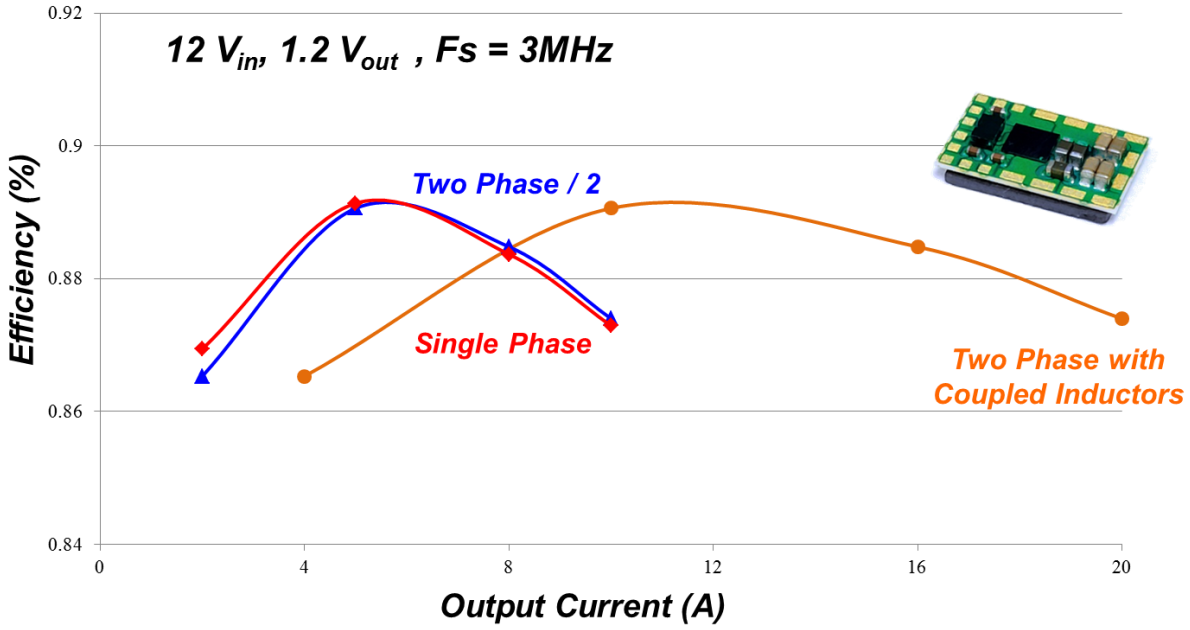


Fig. 3.50: Efficiency comparison for single phase and two phase modules

Chapter 4. Thermal Cycling and Thermal Performance Evaluation for GaN POL Modules

This chapter will discuss the module thermal cycling and thermal performance evaluation. The GaN module is tested with -40 C to +150 C thermal cycling to assess the soldering and integration quality; the components temperatures are measured at full load condition and then the thermal model is calculated.

4.1. Thermal Cycling Assessment for GaN Modules

The thermal cycling test is conducted to determine the ability of components and solder interconnects to withstand mechanical stresses induced by alternating high- and low-temperature extremes. Permanent changes in electrical and/or physical characteristics can result from these mechanical stresses [56].

The JEDEC JESD22-A104D test condition M standard is adopted for the thermal cycling test. The minimum and maximum temperature and tolerances are listed in Table 4.1:

Table 4.1: Temperature cycling test conditions

Test Condition*	Nominal $T_{s(min)}$(°C) with Tolerances	Nominal $T_{s(max)}$(°C) with Tolerances
A	-55(+0, -10)	+85(+10, -0)
B	-55(+0, -10)	+125(+15, -0)
C	-65(+0, -10)	+150(+15, -0)
G	-40(+0, -10)	+125(+15, -0)
H	-55(+0, -10)	+150(+15, -0)
I	-40(+0, -10)	+115(+15, -0)
J	-0(+0, -10)	+100(+15, -0)
K	-0(+0, -10)	+125(+15, -0)
L	-55(+0, -10)	+110(+15, -0)
M	-40(+0, -10)	+150(+15, -0)
N	-40(+0, -10)	+85(+10, -0)

The actual test setups are shown in Fig. 4.1. The tested GaN module is soldered on the test board, then the test board is placed on top of a hotplate, and the hotplate is placed in the thermal chamber. The temperature of thermal chamber is set at -40 ℃ to meet the minimum temperature requirement. The temperature of the hot plate is controlled by the temperature controller placed outside of the chamber. The hot plate is turned on to heat the module when the high temperature is required.

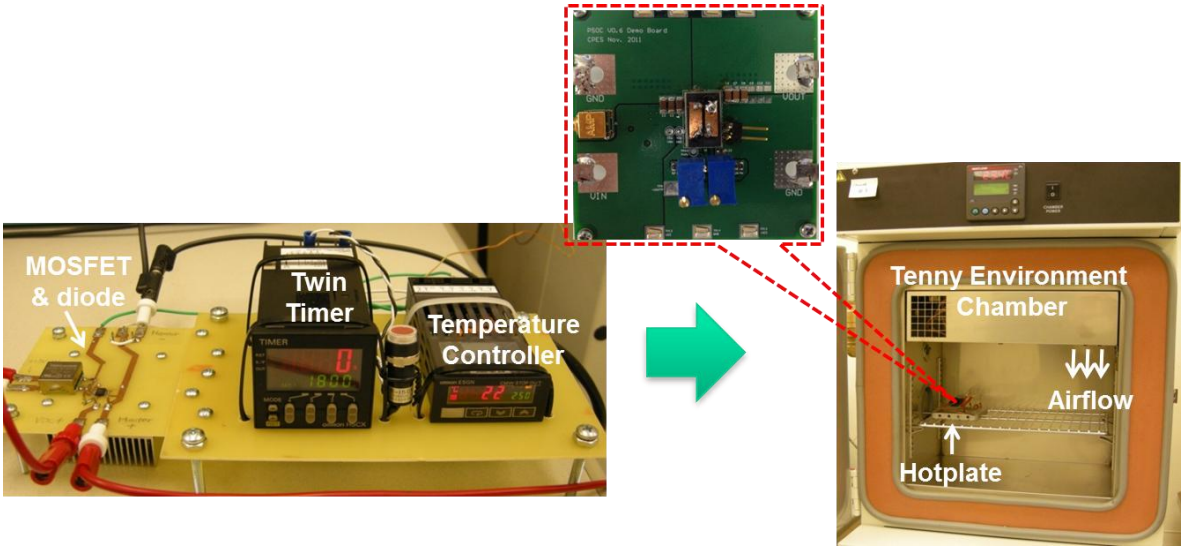
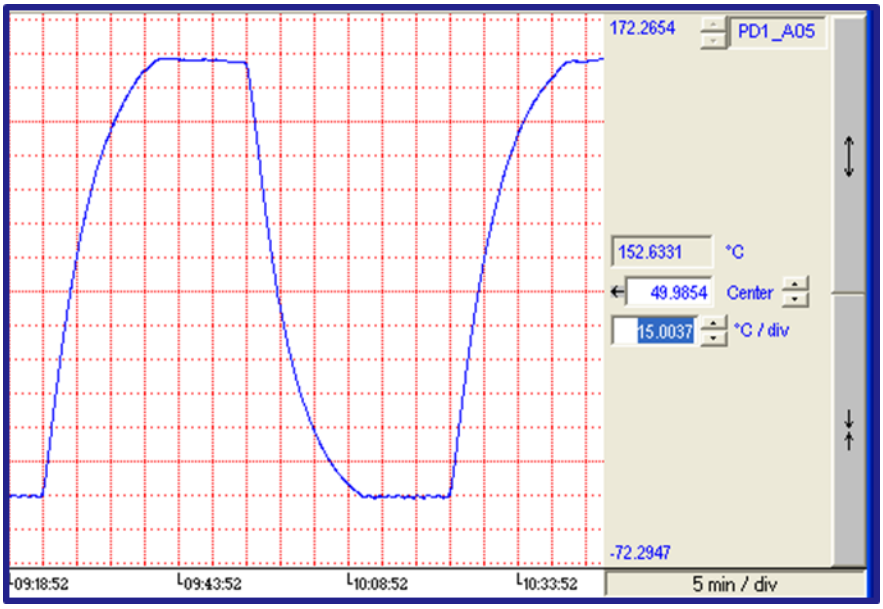


Fig. 4.1: Thermal cycling test setup



Ref: *David Gilham, " Integration of GaN POL Module",HDI Quarter Review, 02,2012*

Fig. 4.2: Measured temperature profile

Fig. 4.2 shows the measured temperature profile by thermal coupler. The comparison between the actual measurement and JEDEC standard are listed in Table 4.2. It can be seen that the profile falls within the standard.

Table 4.2: Temperature comparison for JEDEC standard and actual measurement

Test Conditions	**JEDEC Standard**	**Actual Measurement**
Nominal Temp (min) ℃	-40 (+0,-10)	-41.05
Nominal Temp (max) ℃	+150 (+15,-0)	154.6
Cycles per Hour	1-3	1
Dwell Time Upper (minutes)	5-15	12.5
Dwell Time Lower (minutes)	5-15	12.5
Ramp Rate Heating ℃/min	10-14	11.1
Ramp Rate Cooling ℃/min	10-14	11.1

A DBC GaN module is placed into the chamber and cycled with measured temperature

profile. After 50 temperature cycles, there is no visible crack or defect can be observed on the GaN module. The efficiencies also are tested for before and after the thermal cycling test, as shown in Fig. 4. 3. It can be seen that there is no change of efficiency after 50 cycles. Therefore, the GaN modules have good quality.

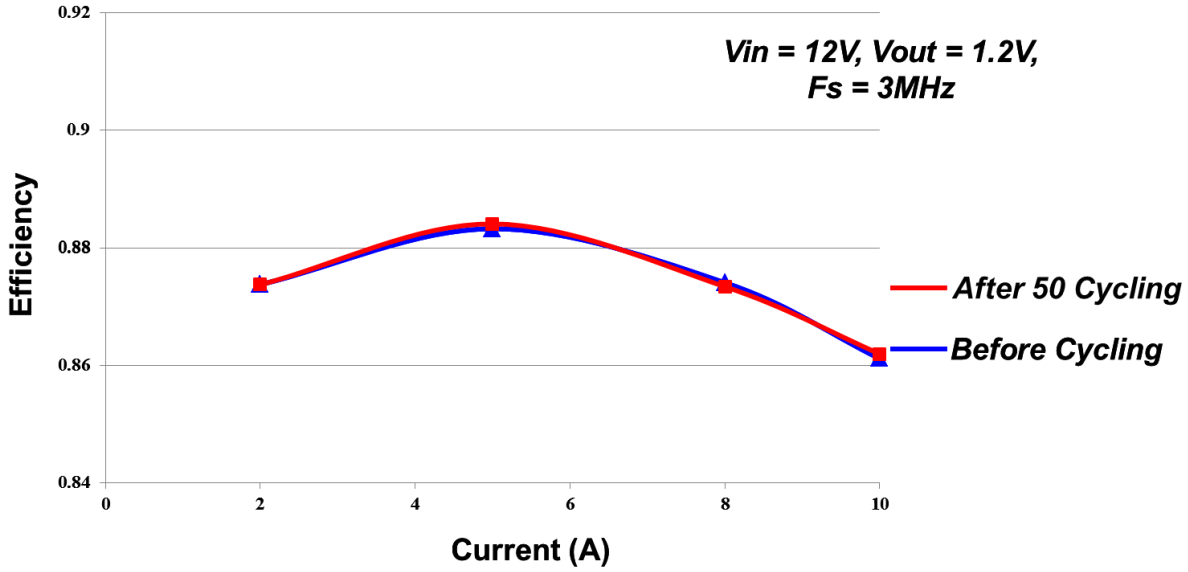


Fig. 4. 3: The efficiency test for before and after thermal cycling

4.2. Thermal Evaluation for GaN Modules

In order to evaluate the thermal performance of these GaN modules, the JEDEC standards JESD51-7 and JESD51-12 are adopted for the evaluation [57][58]. Both PCB and DBC substrates modules are tested and compared, the temperatures of GaN devices are measured by the thermal coupler, the temperatures of testing board are measured by thermal camera, and the junction-to-ambient ($R_{\theta JA}$) is calculated based on measure data as well.

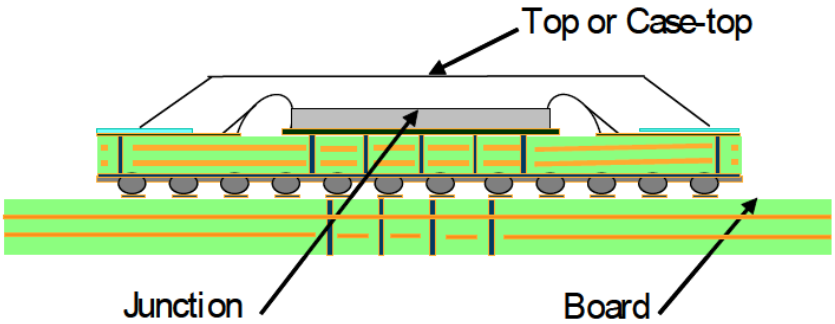
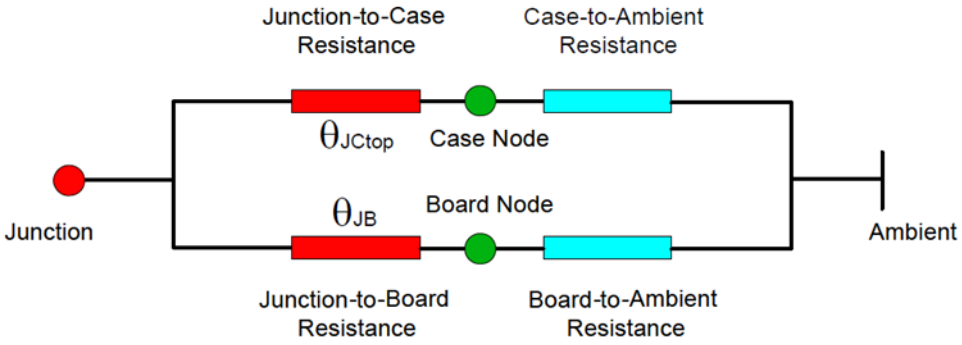


Fig. 4.4: Typical temperature location designations



Ref: *JEDEC Standard JESD51-12*

Fig. 4.5: Equivalent thermal resistance diagram of the two-resistor model on a PCB

Fig. 4.4 shows the temperature measurement locations used to determine the thermal values. When these thermal values are measured, a simple two-resistor model can be calculated as shown in Fig. 4.5. There are two thermal paths from junction to ambient: from junction to testing board, then board to ambient; and from junction to module case, then from case to ambient. For the module with a small top surface without the heat sink, the top thermal path can be ignored; only junction-to-board resistance $R_{\theta JB}$, and board-to-ambient resistance $R_{\theta BA}$ need be calculated in this test.

The measurement of the junction-to-ambient ($R_{\theta JA}$) thermal characteristics of a small package module has historically been carried out using a number of test fixturing methods. The most prominent fixturing method is the soldering of the packaged devices to a PCB board. The

characteristics of the test PCBs can have a dramatic (>60%) impact on the measured $R_{\theta JA}$. It is desirable to have an industry-wide standard for the design of PCB test boards to minimize discrepancies in measured values between companies, due to this wide variability.

JESD51-7 and JESD51-12 standards define the test PCB board geometry and trace layout. Trace layers and layer thicknesses are defined in Fig. 4.6 along with relative dielectric thicknesses between the layers. The test PCB is made of FR-4 material. The finished thickness of the PCB is 1.60 mm +/- 10%.

Ref: *JEDEC Standard JESD51-7*

Fig. 4.6: Cross section of multi-layer PCB showing trace and dielectric thicknesses

Based on the JEDEC specifications, the thermal evaluation boards are designed for both single phase and two phase modules. Since the PCB and DBC GaN modules have the same footprint and are pin-to-pin compatible, both PCB and DBC substrates modules can be tested on the same board.

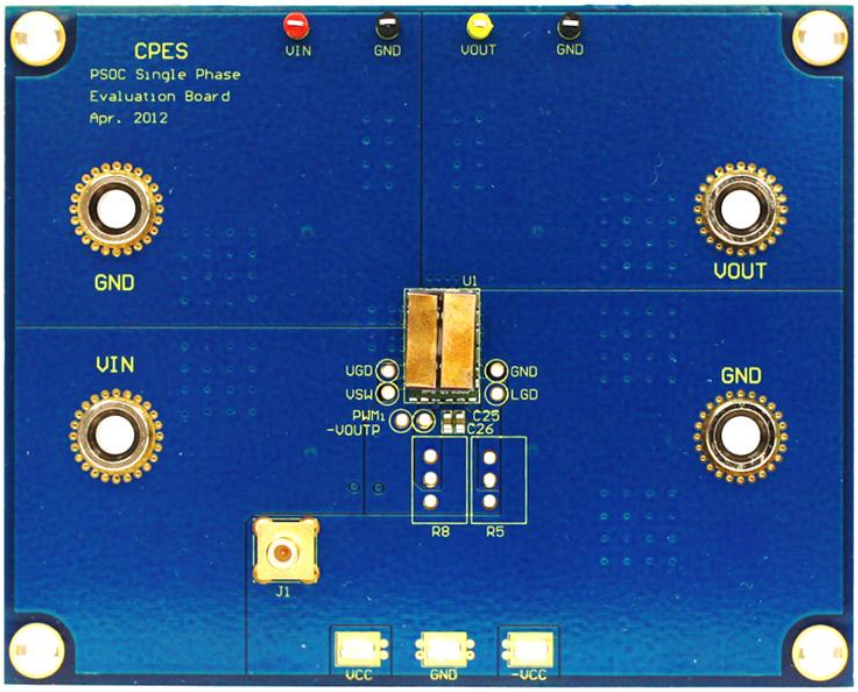
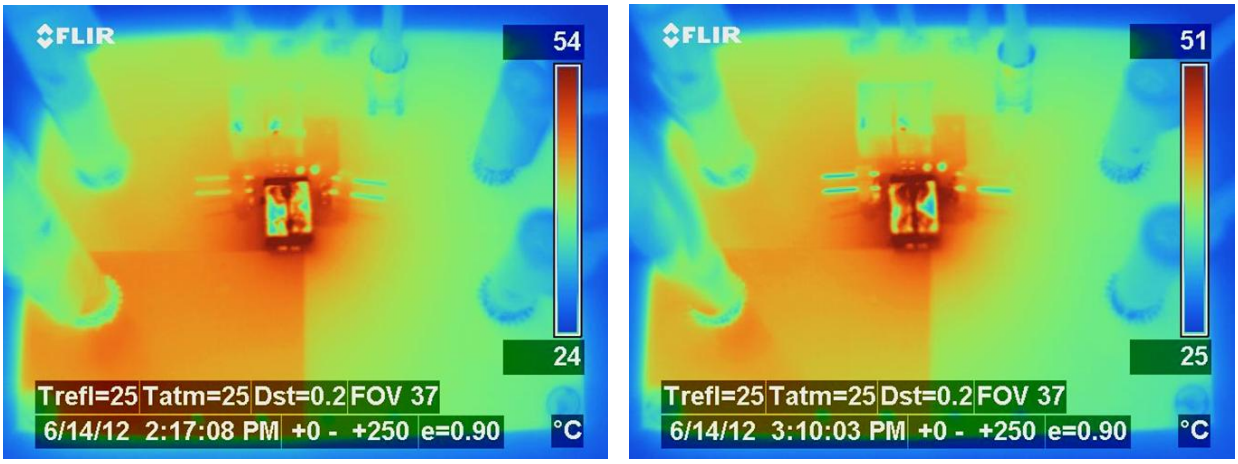


Fig. 4.7: Single phase module mounted on thermal evaluation board

Fig. 4.7 shows the single phase module mounted on the thermal evaluation board. As shown in Fig. 4.8, both PCB and DBC modules are tested at 12 V input, 1.2 V output, 10 A current, 5 MHz operation frequency, 21 ℃ ambient temperature without airflow. The temperature of GaN transistor, which is the hottest point of the module, is measured by thermal coupler. For PCB substrate module, the temperature of GaN is 67.5 ℃ at 2.2 W power loss; for DBC substrate module, the temperature of GaN is 63.3℃ at 2.35 W power loss.



(a) PCB Module (b) DBC Module

Fig. 4.8: Thermal images for single phase PCB and DBC modules

Fig. 4.9 shows the two phase modules mounted on the thermal evaluation boards. In Fig. 4.10, both PCB and DBC modules are tested at 12 V input, 1.2 V output, 20 A current, 5 MHz operation frequency, 23 ℃ ambient temperature without airflow. For PCB substrate module, the temperature of GaN is 113 ℃ at 4.8 W power loss; for DBC substrate module, the temperature of GaN is 93℃ at 5.2 W power loss.

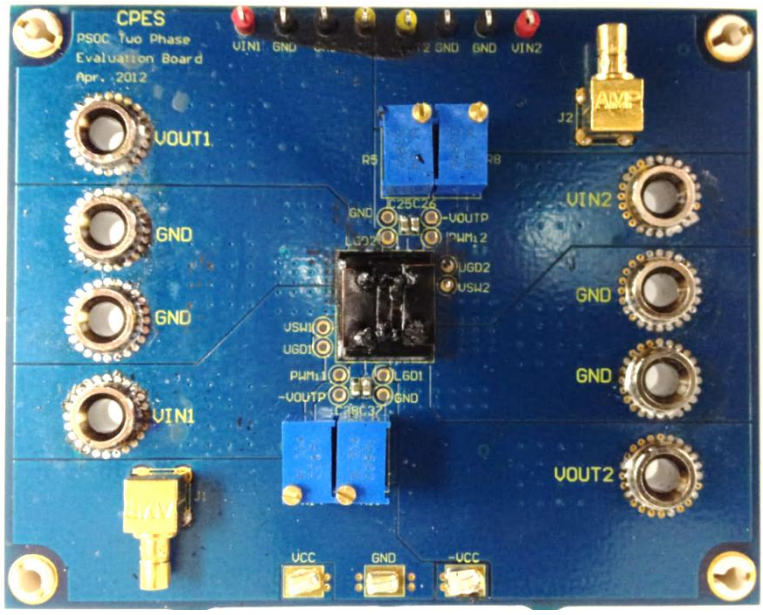
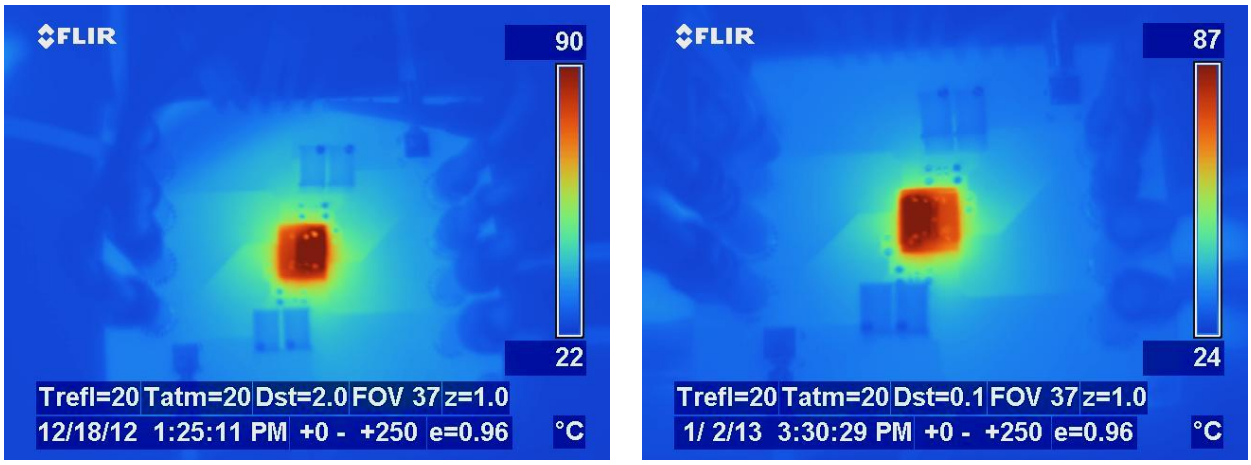


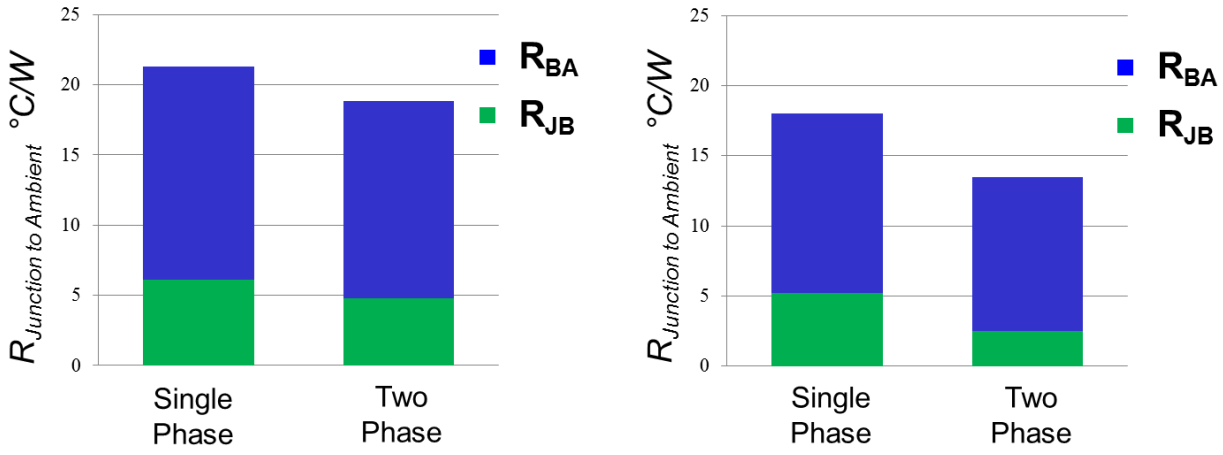
Fig. 4.9: Two phase module mounted on thermal evaluation board



(a) PCB 2 Phase Module (b) DBC 2 Phase Module

Fig.4.10: Thermal images for two phase PCB and DBC modules

The thermal resistances can be calculated based on measured temperature data. Fig.4.11 shows the thermal resistance data for PCB and DBC substrates modules. It can be found that: 1, DBC substrate has smaller thermal resistance than PCB substrate, even with higher power loss; 2, two phase module has smaller thermal resistance than single phase module.



(a) PCB Modules (b) DBC Modules

Fig. 4.11: Thermal resistances for PCB and DBC substrates

Chapter 5. Conclusion and Future Work

5.1. Conclusion

The emerging GaN transistors enable multi-MHz high power density, high efficiency POL converter with high current capability. In this thesis, the design of a high frequency, high power density 3D integrated GaN-based POL module is introduced. This thesis also explores the enhancement mode and depletion mode GaN devices and their characteristics. The impact of parasitics on switching loss is quantified; exploring the contributions of the common source and high frequency loop inductance on switching loss. With the improvements of the GaN device packaging reducing the parasitic inductances, design of the module becomes the main barrier to higher efficiencies and frequencies. Reduction of the high frequency power loop size can offer significant inductance improvements and provide a smaller design footprint. As power density is increased in the module, the thermal design becomes a critical aspect to consider and is often the bottleneck in power handling capability. The use of high thermal conductive alumina DBC substrates to improve thermal performance with better heat distribution is demonstrated. The impact of switching from a traditional multi-layer PCB to a two layer DBC has major implications on the module design to achieve good electrical performance. The impact of the shield plane on electrical performance is considered.

The final demonstrations are single phase and two phase modules with both PCB and DBC substrates that can operate at up to 5MHz. These modules can achieve 3 to 5 times of the power

density and the best of efficiency as the commercial modules. Fig. 5.1 and Fig. 5.2 shows the power density and efficiency achievements of the industry products and CPES GaN module. With the GaN transistor, LTCC inductor substrate, careful circuit design, and 3D integration technique, the GaN POL modules can achieve the highest power density and highest efficient with operating at the highest frequency.

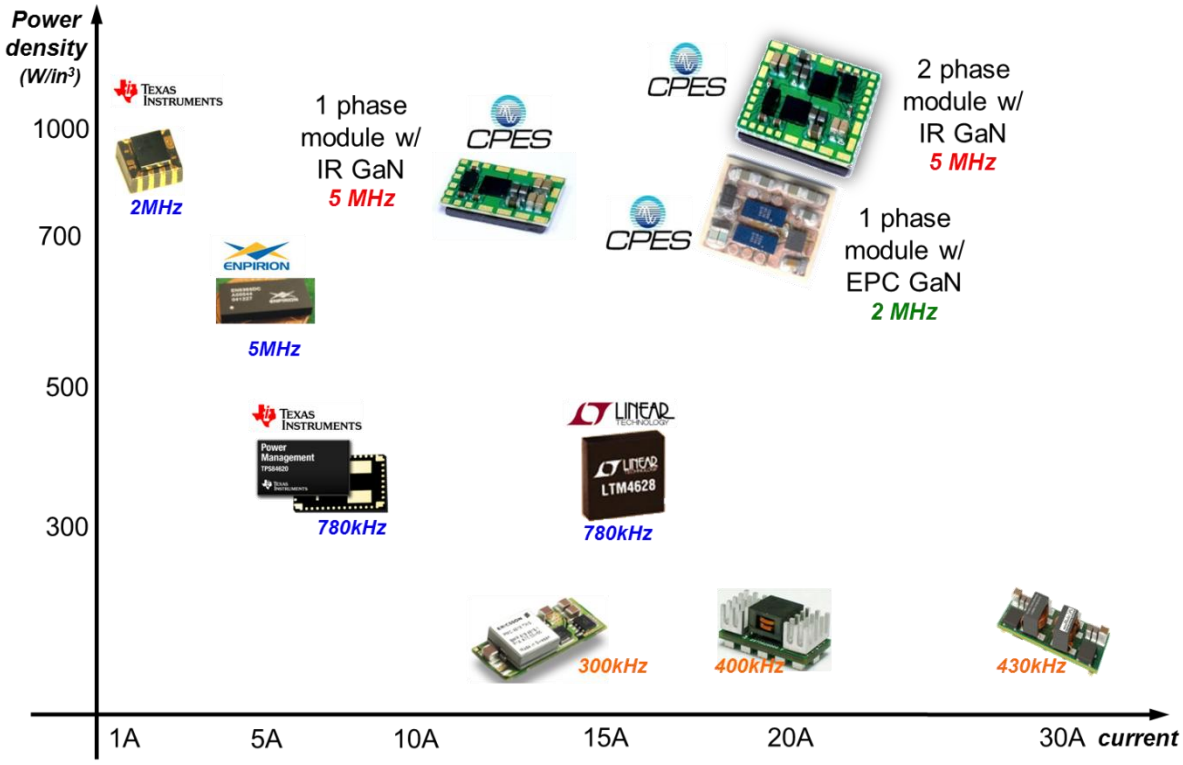


Fig. 5.1: Power density achievement

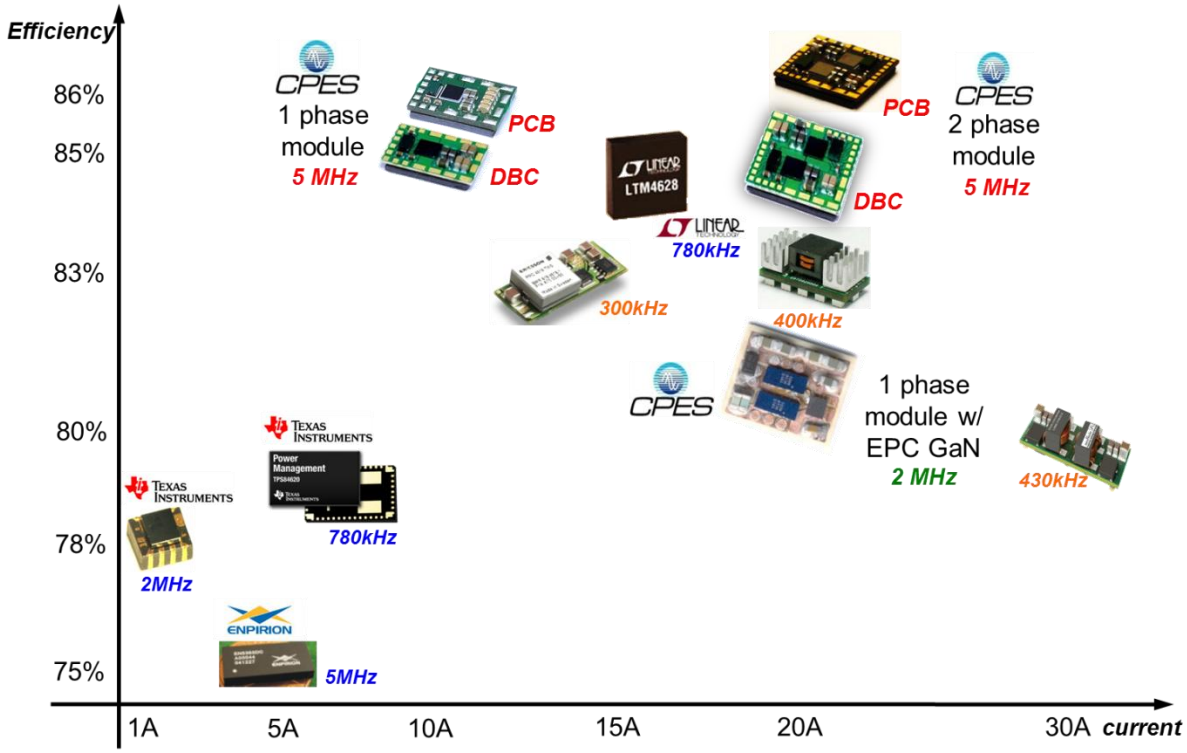


Fig. 5. 2: Efficiency achievement (Vout = 1.2 V)

This thesis work is also a part of APRA-E "Power Supplies on a Chip (PSOC)" project (DE-AR00000106). In this project, Mr. Yipeng Su is in charge of inductors design; Mr. David Gilham and Dr. Wenli Zhang are in charge of LTTC inductors fabrication; Dr. Mingkai Mu is in charge of magnetic material characterization; Dr. David Reusch is in charge of POL module design with EPC's enhancement mode GaN transistors. My work are focusing on POL module design with IR depletion mode GaN transistors, include:

1. single phase module design with PCB substrate;
2. single phase module design with DBC substrate;
3. two phase modules design with both PCB and DBC substrates;
4. extract package and layout parasitics;

5. build the simulation model for GaN module to predict the efficiency;
6. design the evaluation boards for GaN POL modules;
7. evaluate the module efficiency;
8. evaluate the module thermal performance;
9. perform thermal cycling test for GaN modules.

5.2. Future Work

Although the GaN module achieved the highest power density and the highest efficiency, it still has room to be improved. With the new emerging super low profile capacitor technique, the two side structure is considerable with easy inductor assembling and low loop inductance. The efficiency can be further increased. The LTCC inductor also can be placed in the middle of PCB substrate to further simplify the integration process and increase the power density.

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