Design and Analysis of a Low-Power Low-Voltage Quadrature LO Generation Circuit for Wireless Applications

by

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ABSTRACT

The competitive market of wireless communication devices demands low power and low cost RF solutions. A quadrature local oscillator (LO) is an essential building block for most transceivers. As the CMOS technology scales deeper into the nanometer regime, design of a low-power low-voltage quadrature LO still poses a challenge for RF designers.

This dissertation investigates a new quadrature LO topology featuring a transformer-based voltage controlled oscillator (VCO) stacked with a divide-by-two for low-power low-voltage wireless applications. The transformer-based VCO core adopts the Armstrong VCO configuration to mitigate the small voltage headroom and the noise coupling. The LO operating conditions, including the start-up condition, the oscillation frequency, the voltage swing and the current consumption are derived based upon a linearized small-signal model. Both linear time-invariant (LTI) and linear time-variant (LTV) models are utilized to analyze the phase noise of the proposed LO. The results indicate that the quality factor of the primary coil and the mutual inductance between the primary and the secondary coils play an important role in the trade-off between power and noise. The guidelines for determining the parameters of a transformer are developed.

The proposed LO was fabricated in 65 nm CMOS technology and its die size is about 0.28 mm^2. The measurement results show that the LO can work at 1 V supply voltage, and its operation is robust to process and temperature variations. In high linearity mode, the LO consumes about 2.6 mW of power typically, and the measured phase noise is -140.3 dBc/Hz at 10 MHz offset frequency. The LO frequency is tunable from 1.35 GHz to 1.75 GHz through a combination of a varactor and an 8-bit switched capacitor bank. The proposed LO compares favorably to the existing reported LOs in terms of the figure of merit (*FoM*). More importantly, high start-up gain, low power consumption and

low voltage operation are achieved simultaneously in the proposed topology. However, it also leads to higher design complexity.

The contributions of this work can be summarized as 1) proposal of a new quadrature LO topology that is suitable for low-power low-voltage wireless applications, 2) an in-depth circuit analysis as well as design method development, 3) implementation of a fully integrated LO in 65 nm CMOS technology for GPS applications, 4) demonstration of high performance for the design through measurement results. The possible future improvements include the transformer optimization and the method of circuit analysis.

I dedicate this achievement to my husband Wei Shen

It would not have been possible without your support, encouragement and love. Thank you for staying with me all the way.

Also to my lovely daughter Meadow Shen

You are truly our precious and the most wonderful gift given to us.

Also to my parents Mr. Xipeng Wang and Ms. Xiue Wei

I know you truly believe that I am the best from the bottom of your hearts; and I want you to know that you are the most wonderful parents.

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Chapter 1 Introduction

After a brief introduction of wireless technology and transceiver architectures, this chapter states the motivation of the proposed research. The research focuses on the design, analysis and implementation of a low-power low-voltage quadrature signal generator for wireless applications, which stacks a transformer-based VCO and a divide-by-two. Then, it describes the research goals and challenges followed by the technical contributions of the dissertation.

1.1. Motivation

Wireless technology has evolved rapidly over the past decades. It has affect dramatically the lifestyle of people throughout the world. There are numerous wireless applications and services available nowadays, such as cellular/mobile service, wireless local area network (WLAN), Global Positioning System (GPS), satellite television, and so forth. Various wireless standards have been established globally that specify details and constrains for wireless systems such as the operating frequency, modulation type, multiple access techniques, timing, sensitivity and output power level.

Advanced Mobile Phone System (AMPS) is the earliest cellular technology that used Frequency Division Multiple Access (FDMA) and analog frequency modulation (FM). In the 1990s, Global System for Mobile Communications (GSM) and IS-95 Code Division Multiple Access (CDMA) are introduced and considered as second generation (2G) cellular technologies. GSM uses Time Division Multiple Access (TDMA) and is widely deployed in Europe and Asia, while CDMA is more dominant in the United States. To implement both voice and data services, a few standards have been developed, such as General Packet Radio Services (GPRS), Enhanced Data rates for GSM Evolution (EDGE) and IS-95B, which are considered as second and a half generation (2.5G). The destinies of the evolution of GSM and IS-95 to third generation (3G) technology are Universal Mobile Telecommunication Systems (UMTS)/Wideband CDMA (WCDMA) and CDMA2000, respectively [1-1]. As the demand for multimedia service grows tremendously, the migration to fourth generation(4G) standards (a data rate of up to 100

Mbps for high mobility and up to 1 Gbps for low mobility [1-2]) is well undergoing. Worldwide Interoperability for Microwave Access (WiMAX) and Long Term Evolution (LTE) are the two 4G technologies commercially deployed. Along with the well-established cellular standards, numerous complementary technologies have also evolved, such as Bluetooth, WLAN/Wi-Fi (IEEE 802.11), Radio Frequency Identification (RFID) and Near-Field Communication (NFC).

GPS is a satellite navigation system that is operated and controlled by the U. S. Department of Defense (DoD). It was originally invented for military use in the 1970s, and has been freely accessible to civilian users worldwide since 1993. The satellites transmit the signals at two frequencies, 1575.42 MHz (L1) and 1227.60 MHz (L2). A CDMA spread-spectrum technique is used in the satellite network. Besides the United States GPS, there are some other satellite navigation systems, such as Russian GLONASS, European Galileo, and China's Beidou (Compass).

As the competition in the market of the wireless communication devices becomes more intense, there is a growing demand to provide the products with increasingly higher performance, lower power and lower cost. A fully integrated transceiver using low-cost complementary metal oxide semiconductor (CMOS) technology is the appropriate choice for the demand. A considerable research effort has been made to develop CMOS wireless single chip transceivers [1-3]-[1-8].

Superheterodyne, Zero-IF (or Homodyne) and Low-IF have historically been the most commonly used receiver architectures. Due to its superior sensitivity and selectivity, Superheterodyne has been the architecture of choice for decades. However, it requires high-frequency high-performance filters that are difficult to integrate. Alternatively, Zero-IF and Low-IF receivers are gaining more and more popularity for its ease of integration and low cost.

Fig. 1-1 shows a general zero-IF receiver. An RF signal is directly converted down to the baseband. A low-pass filter is then employed to suppress the nearby interferers and select the desired channel. To separate the two sidebands, the zero-IF receiver incorporates quadrature mixing. Despite its apparent simplicity, the zero IF receiver is susceptible to DC offset, I/Q mismatch, even-order distortion and flicker noise [1-9].

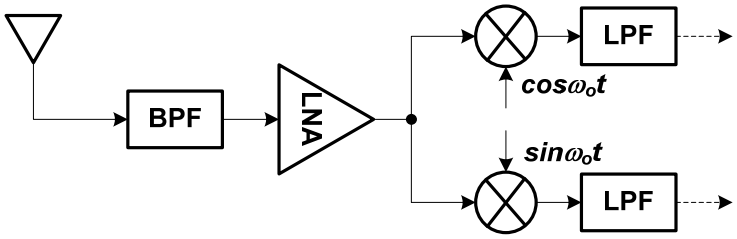


Fig. 1-1 A general Zero-IF receiver

In a low-IF receiver, an RF signal is converted down to a low intermediate frequency (IF), typically a few MHz. The image rejection is accomplished through on-chip quadrature mixing. Since the dc component can be removed by bandpass filters, the DC offset, the LO leakage and the flicker noise are much less serious. One of the drawbacks of the low-IF receiver is the limited image rejection due to the on-chip matching. An example of a low-IF receiver is illustrated in Fig. 1-2 [1-10].

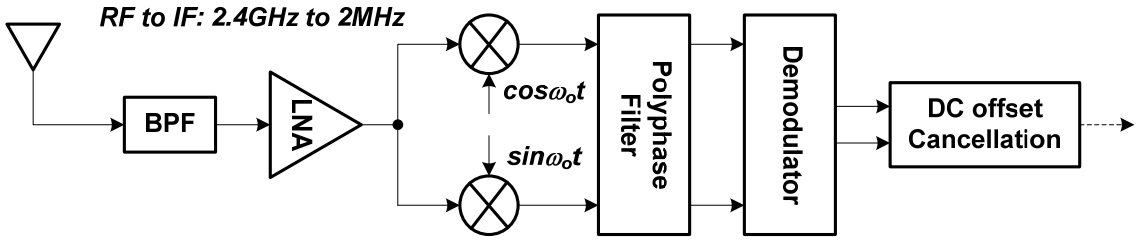


Fig. 1-2 An example of a Low-IF receiver architecture

In both zero-IF and low-IF topologies, an RF local oscillator (LO) that can generate precise quadrature signals is an essential building block. Generally, the LO is one of the power hungry blocks in a transceiver, as it needs to provide low phase noise and minimum I/Q imbalance required for many RF systems. The thriving market of portable wireless devices demands low power and low cost. However, as the CMOS technology scales deeper into the nanometer regime, design of a low-power low-voltage quadrature LO becomes more and more challenging.

1.2. Research Goal and Challenges

The goals of this dissertation research are to explore a new circuit topology to generate quadrature signals for low-power and low-voltage wireless applications, to have an in-depth analysis on the circuit operation principle and the noise mechanism, to

understand all the design tradeoffs and give the insightful guidelines, and to demonstrate the design feasibility with measurement results of a test chip.

Inspired by the current re-use technique, we propose a transformer-based VCO stacked with a divide-by-two for low power quadrature LO generation [1-11], [1-12]. The challenges encountered during the research include:

- *Low voltage operation is one of the design constraints, which makes it difficult to come up with a suitable circuit topology that stacks the divide-by-two on top of the VCO.*
- *Since the VCO and the divider are closely coupled to each other, the impact of the divider to the VCO operation condition, such as voltage swing, current consumption and phase noise should be considered when analyzing VCO performance.*
- *The proposed VCO utilizes a multiple-port transformer. As compared to the conventional VCOs based on an LC (inductor and capacitor) tank, the proposed one is much more complicated in design optimization, transformer modeling as well as simulation convergence.*

The solutions for overcoming the above challenges are essentially the technical contributions of the proposed dissertation research and are described in this dissertation. An Armstrong transformer-based configuration is adopted in the proposed LO architecture, which enables low-voltage operation of the VCO. The impact of the divide-by-two on the signal swing, current consumption and phase noise of the VCO are analyzed mathematically with some approximate models. The design guidelines on the transformer parameter selection and layout optimization are provided in details. Also, a physical lumped model is generated based on the S-parameter model of the transformer over a wide frequency range, which can be used readily in the simulation with good accuracy.

1.3. Dissertation Organization

This dissertation presents design, analysis and implementation of a low-power low-voltage quadrature LO generator through stacking a transformer-based VCO and a divide-by-two. The organization of the dissertation is as follows.

Chapter 2 describes the general oscillator theory and the definition of key design parameters. A number of conventional oscillator topologies, including crystal, ring, Armstrong, Colpitts and Hartley oscillators, are covered. A varactor-based voltage-controlled oscillator and an injection-locked oscillator are also presented. Then three quadrature LO generation schemes, a single VCO followed by a divide-by-two, quadrature VCO and combination of a single VCO and a polyphase filter, are reviewed and compared. The limitations of the existing LOs in the literature are summarized.

Chapter 3 presents the proposed quadrature LO in details. It explains how the low-voltage operation is achieved by using a transformer-based Armstrong VCO in the proposed topology. The VCO start-up condition, the oscillation frequency and the VCO amplitude are derived based upon a linearized small-signal model. Both a linear time-invariant (LTI) and a linear time-variant (LTV) frequency-domain approaches are utilized to analyze the phase noise performance. The theoretical analysis indicates that the mutual inductance and the quality factor of the primary coil play an important role in the trade-off between power and noise. The guidelines on how to determine the transformer parameters and layout configurations are provided.

To validate the proposed LO topology, we designed and fabricated the circuit in 65 nm CMOS technology for GPS receiver. Chapter 4 reviews the design specifications first. Then the circuit implementations of various sub-blocks of the LO are described and some simulation results are provided. The measurement shows that the LO operates robustly under 1 V supply voltage, covers a frequency range roughly from 1.35 GHz to 1.75 GHz. In high linearity mode, the LO typically consumes about 2.6 mW of power, and the measured phase noise is -140.3 dBc/Hz at 10 MHz offset frequency.

Finally, Chapter 5 draws conclusions of the proposed research. Future work is suggested based on the problems encountered and research findings throughout the course of the research.

Chapter 2 Background

This chapter provides background for the proposed research and it starts with the general oscillation theory, modeling approaches and definition of key design parameters. Then, it describes various conventional oscillator topologies, along with detailed circuit analysis and design methodologies. A quadrature signal generator can be viewed as a multi-phase oscillator. The approaches to generate quadrature I/Q signals are reviewed. Advantages and limitations of the different architectures in terms of area, complexity, power and noise are discussed. Finally, existing low-power techniques adopted for VCOs and quadrature LOs are discussed, and challenges for low-power design are summarized.

2.1. General Oscillation Theory

An oscillator is a circuit that can continuously produce a periodic output signal without any input signal. Such a circuit or system has to meet certain criteria to sustain steady oscillation. Generally, the start-up condition and the oscillation frequency of an oscillator can be determined by examining the conditions in which the criteria are met.

There are two different ways to view an oscillator: a two-port model based on positive feedback and a one-port model based on negative resistance [2-1]. Even though the two approaches are fundamentally equivalent to each other, it is more convenient to use one model over the other for a specific oscillator. For instance, it is more convenient to analyze the ring oscillator using the positive feedback model. Alternatively, the negative resistance approach is commonly adopted to model resonator-based oscillators such as an LC oscillator.

2.1.1. Feedback Model of an Oscillator

An oscillator can be modeled mathematically as a linear positive feedback system, as shown in Fig. 2-1, where A(s) represents the loop gain. Then the overall transfer function from the input X(s) to the output Y(s) is

$$\frac{Y(s)}{X(s)} = \frac{A(s)}{1-A(s)} \quad (2\text{-}1)$$

From the control theory, the circuit is unstable if it has poles in the right half of the S-plane, and it is marginally stable if the poles are located on the imaginary axis. The unstable system produces an expanding transient waveform when subject to an initial excitation. Any noise in the circuit and/or coupled from the power supply or the substrate can provide such an excitation that initiates the oscillation build-up. As the signal becomes large, the nonlinearity in the circuit limits the growth of the signal. The well-known Barkhausen's criteria state that the circuit will sustain the steady-state oscillation only at frequencies for which:

1) The magnitude of the loop gain, |A(s)|, must be equal to unity;

2) The total phase shift around the loop, ∠A(s), must be equal to zero or integer multiple of 2π.

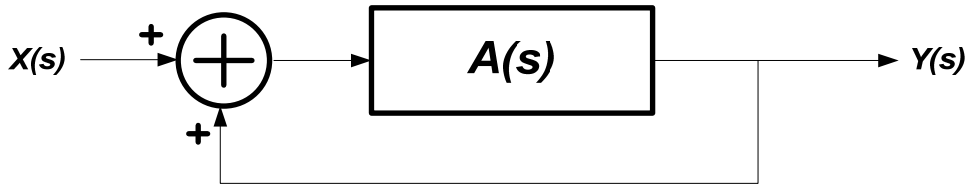


Fig. 2-1 Feedback model of an oscillator

It should be emphasized that Barkhausen's criteria are *necessary but not sufficient conditions* for oscillation [2-2]. For example, a 6-stage single-ended ring oscillator will latch up even if the total phase shift around the loop is 2π, and the loop gain is sufficient. However, it is usually convenient to use Barkhausen's criteria to find the oscillation conditions provided that the oscillation does exist.

2.1.2. Negative-Resistance Model of an Oscillator

The one-port model based on negative-resistance is shown in Fig. 2-2. The oscillator is viewed as two one-port networks connected in parallel. One is a lossy resonator, the other one is an active circuit. The resonator can be modeled as a parallel combination of an inductor L, a capacitor C and a resistor R_p. The role of the active circuit is to replenish the energy dissipated in the resonator by providing an equivalent negative resistance of R_p. As a result, the steady-state oscillation is sustained. The negative-resistance model has been widely used in the design of LC oscillators.

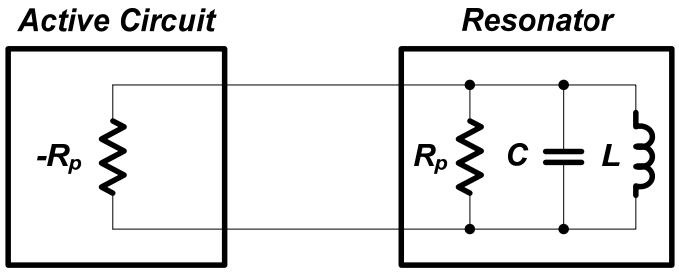


Fig. 2-2 Negative-resistance model of an oscillator

2.2. Key Oscillator Design Parameters

2.2.1. Phase Noise

An ideal oscillator produces a sinusoidal time-domain waveform of a constant amplitude and a constant frequency, which translates into a single tone in frequency domain. However, in reality both the amplitude and the frequency of the oscillator are inevitably disturbed by the internal and or the external noise sources. The perturbation in the amplitude is negligible for most cases. Contrarily, the random deviation of the frequency is of great concern for practical RF transceivers. The spectrum of an ideal oscillator and that of a real one are shown in Fig. 2-3, respectively. With the existence of the phase noise, the spectrum exhibits the noise "skirt" around the carrier signal.

Fig. 2-3 Spectrums of ideal and real oscillators

Phase noise $L\{f_m\}$, as shown in Fig. 2-4, is defined as the noise spectral power in a 1 Hz bandwidth at a certain offset frequency f_m from the carrier relative to the power of the fundamental signal, typically expressed in unit of dBc/Hz [2-1]. The spectral impurity of the oscillator has various negative impact in RF communication systems. For a receiver, poor phase noise can result in "reciprocal mixing". It may also raise the noise floor of the receiver, and degrade the noise figure. For a transmitter, poor phase noise can

cause the noise being transmitted with the wanted signal, which may lead to interference with other frequency bands and degrade signal-to-noise ratio (SNR).

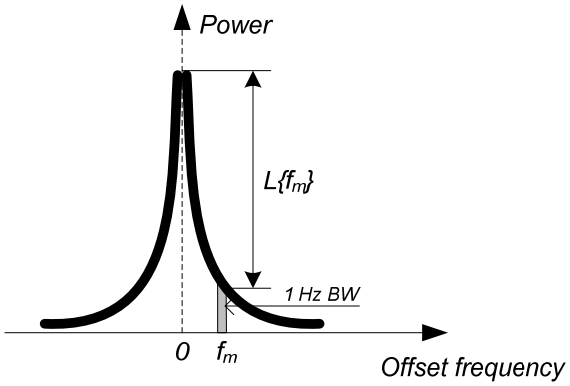


Fig. 2-4 Illustration of phase noise definition

2.2.2. Characteristics of Frequency Tuning

A local oscillator (LO) used in RF systems generally needs to support a certain frequency tuning range. The tuning sensitivity, also called the gain of the oscillator, measures the amount of change in the oscillation frequency that results from the change of control voltage or current. Intuitively, the wider the frequency tuning range, the higher the tuning sensitivity. However, a high sensitivity is very undesirable as it makes the frequency tuning circuit sensitive to the noise and hence degrades the phase noise. This issue is typically addressed by dividing the tuning range into multiple discrete frequency bands with sufficient overlap between adjacent bands. Then a wide enough tuning range and a low tuning sensitivity can be achieved simultaneously.

2.2.3. Q of the Oscillator

Q or quality factor of the oscillator is defined as the ratio of the energy stored to the energy dissipated per cycle, which can be written as

$$\mathrm{Q} = 2\pi \frac{\text{Energy Stored}}{\text{Energy Dissipated per cycle}} = 2\pi f_o \frac{Energy\ Stored}{Power\ Loss} \tag{2-2}$$

A resonator usually has a bandpass characteristics. The Q can also be defined as the resonant frequency divided by the 3dB bandwidth. The Q of a simple RLC resonator is

$$\mathrm{Q} = \frac{R_p}{\omega \mathrm{L}} = R_p \omega C \tag{2-3}$$

where R_p is a parallel equivalent resistor, representing the loss of the resonator.

The active devices for practical oscillators also add to the resonator loss, which lowers the quality factor, particularly when the signal swing is large that pushes the devices into the triode region. The term "loaded Q" refers to this scenario to differentiate it from the inherent Q of the resonator.

2.3. Conventional Oscillator Topologies

Many different types of oscillators have been developed over the past few decades. Depending on the output waveform, they can be grouped into two categories: harmonic oscillators and relaxation oscillators [2-3]. The oscillators that generate sinusoidal or nearly so waveforms with a definite frequency are classified as harmonic oscillators, and the ones that produce non-sinusoidal outputs are termed as relaxation oscillators. A few common oscillator topologies are reviewed in the following, which are crystal oscillator, ring oscillator, Armstrong oscillator, Hartley oscillator, Colpitts oscillator and cross-coupled LC oscillator.

2.3.1. Crystal Oscillator

Crystal oscillators are widely used as the stable clock sources for frequency synthesizers in communication systems. A quartz crystal oscillator relies on the piezo-electric effect to work, which is known as the linear electromechanical interaction between the electrical and the mechanical states in the crystal [2-4]. It behaves like a very high Q resonator when placed into an electronic circuit. An equivalent model of the crystal oscillator is shown in Fig. 2-5, where R, L and C represent the characteristics of the crystal itself, and C_o is the capacitance between the electrodes. There are two possible resonance modes. One is a series resonance from L and C, which results in a very low impedance at the resonant frequency. The other one is a parallel resonance from L, C and C_o, which has a very high impedance at the resonant frequency. Normally the difference between the two resonant frequencies is quite small, as C_o is much larger than C. Since the oscillation frequency of the crystal oscillator drifts over temperature, a temperature compensated crystal oscillator (TCXO) is normally used as a very high precision frequency source.

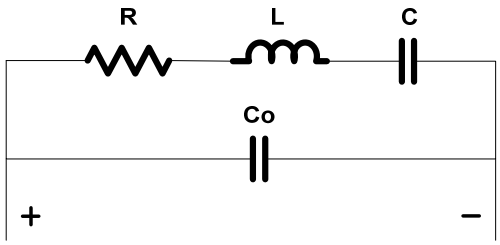


Fig. 2-5 Equivalent circuit of a quartz crystal oscillator

2.3.2. Ring Oscillator

A ring oscillator is composed of a number of delay stages. It is one type of the relaxation oscillators. According to Barkhausen's criteria, a single-ended inverter based ring oscillator should have at least three delay stages as the phase shift per stage is less than 180º. Fig. 2-6 shows a block diagram of a typical three-stage single-ended ring oscillator.

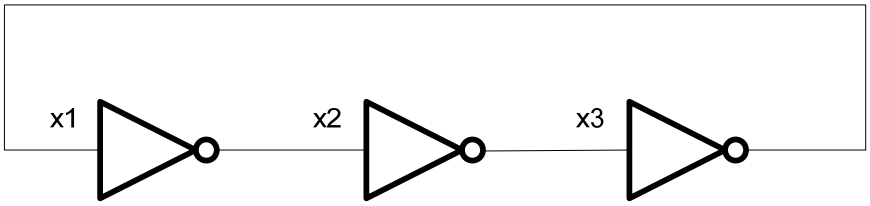


Fig. 2-6 Block diagram of a three-stage single-ended ring oscillator

If an even number of delay stages are connected in a ring, then the circuit will latch up due to the positive feedback near zero frequency. Therefore, a single-ended ring oscillator must have an "odd" number of stages to avoid latch-up. However, a differential ring oscillator can utilize an even number of stages by simply configuring one stage as an non-inverting stage. A block diagram of a typical four-stage differential ring oscillator is illustrated in Fig. 2-7.

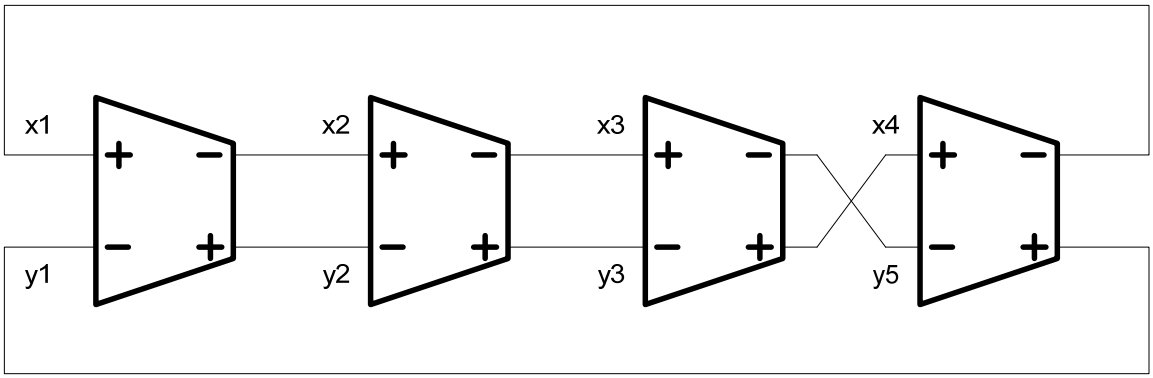


Fig. 2-7 Block diagram of a four-stage differential ring oscillator

It is assumed that each delay stage has a transfer function of

$$T_{delay\_stage} = -\frac{A}{1+\frac{s}{\omega_{3dB}}} \tag{2-4}$$

where A is the small-signal DC gain, and ω_{3dB} is the *-3dB* bandwidth. Then the loop gain of a three-stage oscillator is equal to

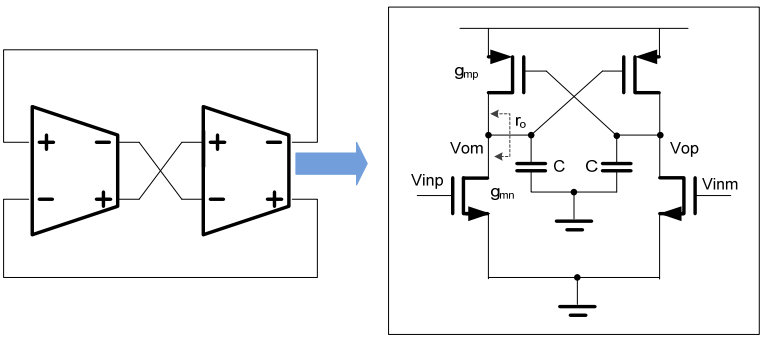
$$T_{gain\_3stage} = -\frac{A^3}{\left(1+\frac{s}{\omega_{3dB}}\right)^3} \tag{2-5}$$

From Barkhausen's criteria, the oscillator oscillates at the frequency of $\sqrt{3}\omega_{3dB}$ provided $A \geq 2$. Similarly, the loop gain of a four-stage oscillator can be written as

$$T_{gain\_4stage} = -\frac{A^4}{\left(1+\frac{s}{\omega_{3dB}}\right)^4} \tag{2-6}$$

When $A \geq \sqrt{2}$, the oscillator oscillates at the frequency of ω_{3dB}. However, if the common-mode level of the differential signals is either too high or too low, the circuit can still latch up. A start-up circuit (for example, two weak inverters) is thereby necessary.

The delay cell is typically implemented as a differential amplifier with either resistive load or diode connected PMOS load. The frequency tuning can be achieved by varying the bias current of the cell. Depending on the circuit topology, the transfer function of the delay cell could be different from (2-4). For example, the delay cell presented in [2-5] consists of a cross-coupled latch, which results in a pole on the right half plane. Therefore, the ring oscillator can oscillate even with only two stages, which is shown in Fig. 2-8.



Two complex-conjugate poles:

$$S_{1,2} = \frac{g_{mp}r_o - 1}{r_o C} \pm j\, g_{mn}/C$$

Oscillation condition:

$$g_{mp}r_o - 1 > 0$$

Fig. 2-8 A two-stage ring oscillator design example

The oscillator becomes nonlinear when operating in the large-signal regime. The steady-state oscillation frequency is governed by the number of the stages N and the delay per stage T_d as

$$f_{osc} = \frac{1}{2NT_d} \tag{2-7}$$

which is different from what is predicted from a small-signal model. The waveforms at the internal nodes of a four-stage differential ring oscillator is demonstrated in Fig. 2-9. Apparently, the ring oscillator with even number of delay stages can provide quadrature signals.

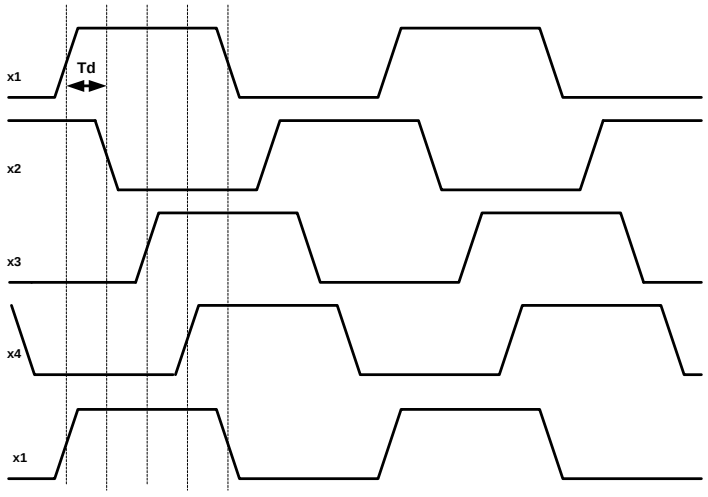


Fig. 2-9 Waveforms at the nodes of the four-stage differential ring oscillator

The phase noise and jitter performance of ring oscillators have been analyzed mathematically in [2-6]-[2-8]. For the same power consumption, the ring oscillator is much noisier but also more compact than its LC oscillator counterpart. The strategies for a low noise ring oscillator design are summarized as follows [2-6]-[2-8]:

- Use as high a supply voltage as possible;
- Burn as much current as the budge allows;
- Use low threshold device;
- Choose the longest practical channel;
- Use cross-coupled loads for a fast rail-to-rail switching;
- Get rid of NMOS bias current source.

By injecting a clean reference clock into a ring oscillator periodically, the low-frequency phase noise of the oscillator can be improved significantly [2-9]. However, it is challenging to apply this technique in a fractional-N frequency synthesizer.

2.3.3. Armstrong Oscillator

The Armstrong oscillator [2-10] utilizes two inductors connected at the gate and the drain of an NMOS device, which is shown in Fig. 2-10. The oscillation is sustained by the magnetic coupling between the two inductors. The capacitor C can be resonated with either the gate inductor L_g (which is the case shown here) or the drain inductor L_d to form the main tank.

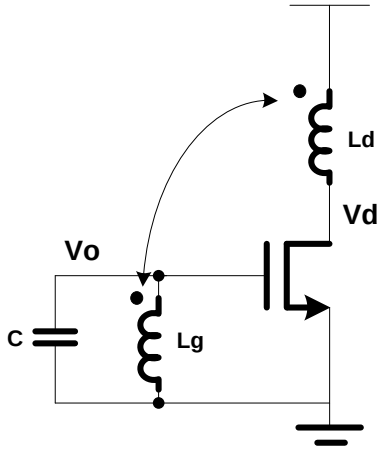


Fig. 2-10 A conventional single-ended Armstrong oscillator

The circuit analysis of the Armstrong oscillator is omitted here as it is provided in details in Chapter 3. The start-up condition of the oscillator in Fig 2.10 can be derived as

$$g_m \omega Q M > 1 \qquad (2\text{-}8)$$

where Q represents the quality factor of the resonator, and M is the mutual inductance between L_g and L_d. The oscillation frequency is approximately equal to

$$f_o = \frac{1}{2\pi\sqrt{L_g C}} \tag{2-9}$$

2.3.4. Colpitts Oscillator

A Colpitts oscillator incorporates one inductor and two capacitors. The feedback signal is taken from a capacitor divider. The common-drain configuration is illustrated in Fig. 2-11, where the LC tank is resonated at the gate of the NMOS device, and the feedback signal is applied to the source.

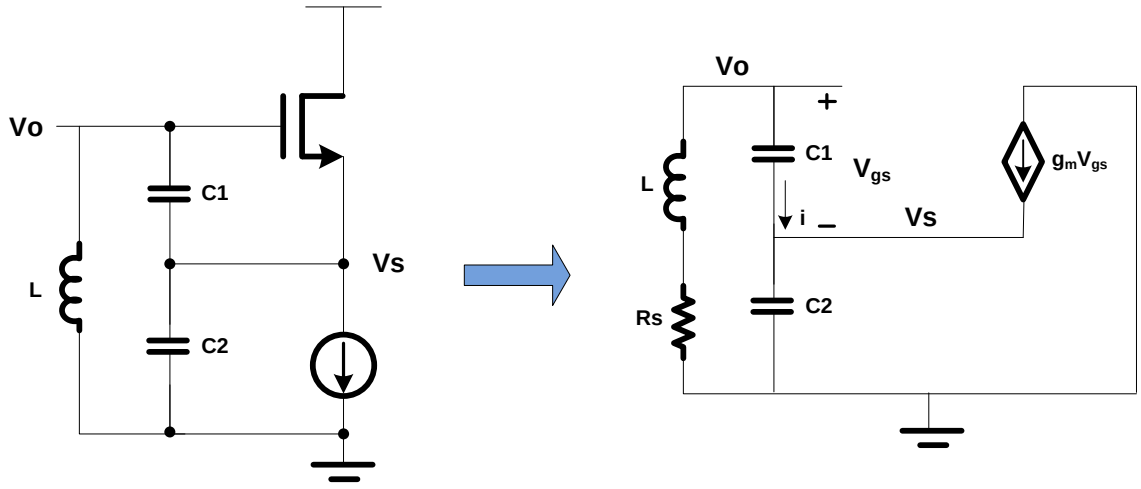


Fig. 2-11 A conventional single-ended Colpitts oscillator and its small-signal model

From the small-signal model shown in the same figure, we can obtain the following equations:

$$i + g_m(V_o - V_s) = V_s \cdot sC_2 \tag{2-10}$$

$$i = (V_o - V_s) \cdot sC_1 \tag{2-11}$$

Then the impedance seen by the inductor can be calculated as:

$$Z = \frac{V_o}{i} = \frac{1}{sC_1} + \frac{1}{sC_2} - \frac{g_m}{\omega^2 C_1 C_2} \tag{2-12}$$

Clearly, there is a negative resistance of $-g_m/\omega^2 C_1 C_2$ in series with the capacitors. The circuit will oscillate when the negative resistance is greater than R_s, which models the loss of the tank. So the start-up condition of the Colpitts oscillator in Fig. 2-11 is

$$\frac{g_m Q}{\omega(C_1+C_2)} > 1 \tag{2-13}$$

where Q is the quality factor of the resonator. From (2-12), the oscillation frequency is determined by the inductance and the equivalent capacitance of C_1 and C_2 in series, which is approximately equal to

$$f_o = \frac{1}{2\pi\sqrt{L\frac{C_1 C_2}{C_1+C_2}}} \tag{2-14}$$

The required g_m is minimum when $C_1 = C_2$, which yields

$$g_m > \frac{4}{Q\omega L} \tag{2-15}$$

The single-ended Colpitts oscillator can be extended to the differential topology for better common-mode rejection. It has been widely used in RF systems due to the superior phase noise performance. However, it suffers from a poor start-up gain and also the capacitive divider limits the tuning range. Some g_m-boosting techniques have been published to overcome the disadvantages [2-11], [2-12].

2.3.5. Hartley Oscillator

A Hartley oscillator is essentially equivalent to the Colpitts oscillator in terms of the circuit topology. The only difference is the roles of L and C are exchanged. Fig. 2-12 shows a conventional single-ended Hartley oscillator, which employs one capacitor and two inductors. The feedback signal is taken from an inductor divider. However, it is not easy to bias the NMOS device as the inductors provide both ac and dc paths. The two inductors L_1 and L_2 are generally coupled with each other, though it is not necessary.

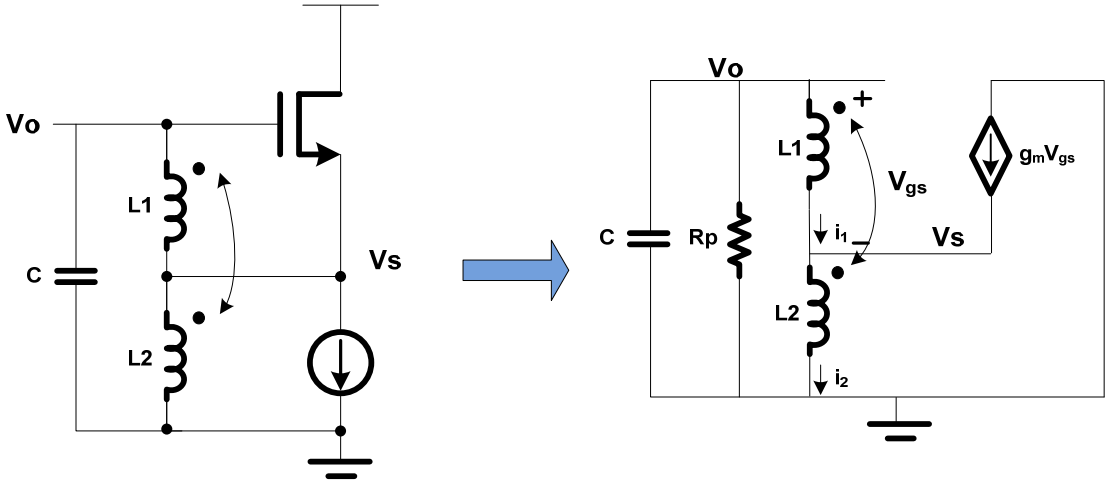


Fig. 2-12 A conventional single-ended Hartley oscillator

Again the oscillation conditions can be analyzed based on the small-signal model in Fig. 2-12. From Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL), we can write down the following equations:

$$V_o - V_s = i_1 \cdot sL_1 + i_2 \cdot sM \tag{2-16}$$

$$V_s = i_2 \cdot sL_2 + i_1 \cdot sM \quad (2\text{-}17)$$

$$i_2 = i_1 + g_m \cdot (V_o - V_s) \quad (2\text{-}18)$$

where M is the mutual inductance between L_1 and L_2. Then the impedance seen by the capacitor C and the parallel resistor R_p can be derived as

$$Z = \frac{V_o}{i_1} \approx s(L_1 + L_2 + 2M) - g_m\omega^2(L_1 + M)(L_2 + M) \quad (2\text{-}19)$$

Thus, there is a negative resistance of $-g_m\omega^2(L_1 + M)(L_2 + M)$ in series with the inductors. The oscillation is sustained when the tank loss is completely compensated by this negative resistance. The start-up conditions of the Hartley oscillation shown in Fig. 2-12 becomes

$$\frac{g_m Q\omega(L_1+M)(L_2+M)}{L_1+L_2+2M} > 1 \quad (2\text{-}20)$$

And the oscillation frequency is approximately equal to

$$f_o = \frac{1}{2\pi\sqrt{(L_1+L_2+2M)C}} \quad (2\text{-}21)$$

The required g_m is minimum when $L_1 + M = L_2 + M$, which yields

$$g_m > \frac{4}{Q\omega L} \quad (2\text{-}22)$$

where L is the total equivalent inductance, equal to the sum of L_1, L_2 and $2M$.

Similar to the Colpitts oscillator, the Hartley oscillator exhibits excellent phase noise performance, but poor start-up gain. This type of oscillator is actually rarely used as compared to other LC oscillators.

2.3.6. Cross-Coupled LC Oscillator

A cross-coupled LC oscillator is the most popular one as it is easy to start up and also has good phase noise performance. A conventional differential NMOS cross-coupled LC oscillator is shown in Fig. 2-13. The NMOS cross-coupled pair provides negative resistance to the LC resonator to compensate the loss.

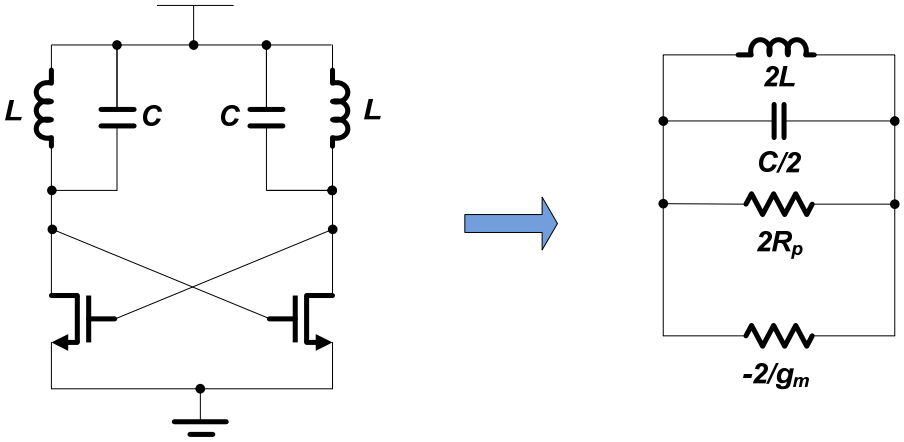


Fig. 2-13 A conventional differential CMOS cross-coupled LC oscillator and its small-signal model

It is rather straightforward to analyze the oscillation conditions using the one-port negative-resistance model. As shown in Fig. 2-13, the cross-coupled pair acts as a differential negative resistance of $-2/g_m$ to the tank. So the start-up condition is

$$g_m > \frac{1}{Q\omega L} \tag{2-23}$$

And the oscillation frequency is approximately equal to

$$f_o = \frac{1}{2\pi\sqrt{LC}} \tag{2-24}$$

Comparing (2-23) with (2-15) and (2-22), we can see that the minimum required g_m for the Colpitts and the Hartley oscillators are four times larger than that for the NMOS-only cross-coupled oscillator. This clearly demonstrates an important advantage of the cross-coupled oscillator over the other types of the oscillators.

2.4. Voltage-Controlled Oscillator (VCO)

A voltage-controlled oscillator (VCO) refers to an oscillator whose output frequency is varied in response to an input voltage. Varactor that has variable capacitance depending on the voltage is widely used as a tuning element in many LC VCOs. For CMOS technologies, on-chip varacators are typically implemented as reverse-biased diode varactors or MOS varactors in either depletion-inversion regime or accumulation-depletion regime [2-13], [2-14]. MOS varactors gain more popularity over the diode ones for wider tuning range and lower parasitic resistance especially when more advanced technology is adopted.

A cross-section view of an inversion-mode MOS (I-MOS) varactor is shown in Fig. 2-14. The operation is similar to a standard PMOS transistor with the drain and the source being tied up. When $|V_{gs}| >> |V_{th}|$, an inversion channel of mobile holes is formed under the gate oxide, and the transistor operates in the inversion region. The MOS capacitance is equal to the gate oxide capacitance C_{ox}. As $|V_{gs}|$ decreases below the threshold voltage, a depletion layer made of ionized donor atoms is created at the gate oxide surface, which can be viewed as a variable depletion capacitor C_{dep} connected to C_{ox} in series. Consequently, the total MOS capacitance decreases to $C_{ox}C_{dep}/(C_{ox}+C_{dep})$.

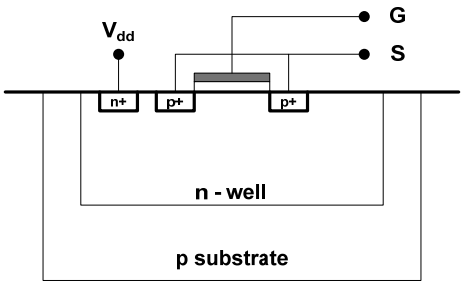


Fig. 2-14 A cross-section of an inversion-mode varactor

Alternatively, an accumulation-mode MOS (A-MOS) varactor exhibits superior performance as compared to the diode varactor and the I-MOS varactor [2-14]. A cross-section view of a typical A-MOS varactor is shown in Fig. 2-15. The structure is similar to a standard NMOS transistor except that it is fabricated in an n-well instead of a p substrate. When $|V_{gs}| >> |V_{th}|$, the electrons provided by the n^+ region are accumulated at the gate oxide interface and form an accumulation layer. The total MOS capacitance is simply determined by the gate oxide capacitance C_{ox}. As $|V_{gs}|$ decreases, the surface is less accumulated and eventually undergoes depletion. As a result, the total MOS capacitance reduces from C_{ox} to $C_{ox}C_{dep}/(C_{ox}+C_{dep})$.

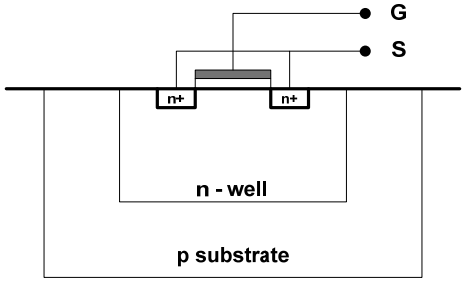


Fig. 2-15 A cross-section of an accumulation-mode varactor

The frequency tuning sensitivity of an LC VCO with a MOS varactor is directly dependent on the C-V characteristics of the varactor as

$$f_o(V) = \frac{1}{2\pi\sqrt{L(C+C_{var}(V)}} \tag{2-25}$$

$$K_{VCO}|_{V=V_{tune}} = \frac{df_o(V)}{dV}\Big|_{V=V_{tune}} = -2\pi^2 {f_{osc}}^3 L \frac{dC_{var}(V)}{dV}\Big|_{V=V_{tune}} \tag{2-26}$$

where f_{osc} is the oscillation frequency when $V = V_{tune}$, and C_{var} is the capacitance of the varactor. Typically, K_{vco} varies a lot over the tuning voltage due to a highly non-linear *C-V* curve of the varactor.

2.5. Injection-Locked Oscillator (ILO)

When a harmonic LC oscillator is disturbed by an injected signal at a frequency close to its free-running frequency, injection locking or injection pulling can occur depending on the strength of the injected signal [2-15], [2-16]. This phenomena is intentionally utilized in an injection-locked oscillator (ILO).

Fig. 2-16 shows a conceptual injection-locked oscillator, which includes an RLC resonant tank, an ideal inverting stage and a common-source amplifier. Ignoring parasitics, the self-resonant frequency ω_o of the tank is equal to $1/\sqrt{LC}$. When the oscillator is oscillating at ω_o, the total phase shift around the loop is 360º, and V_o and I_o are in phase all the time. Suppose an external current I_{inj} at a frequency of ω_{inj} is injected to the tank. Then the net current I_T flowing into the tank is no longer in phase with V_o. Under certain conditions, the oscillator is locked to the frequency of ω_{inj}. The vector diagram drawn in the same figure illustrates the phase and the magnitude relationships among I_o, I_{inj} and I_T, where θ is the phase difference between I_{inj} and I_o and φ is the phase difference between I_T and I_o.

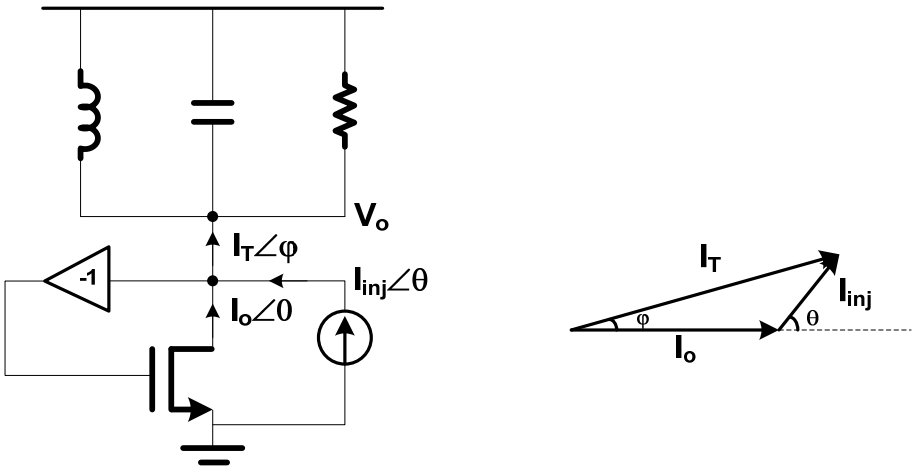


Fig. 2-16 Conceptual view of an injection-locked oscillator

In the steady state, since V_o and I_o are always in phase, the tank must introduce $-\varphi$ to validate the condition. The amplitude and the phase of the tank impedance over the frequency are plotted in Fig. 2-17.

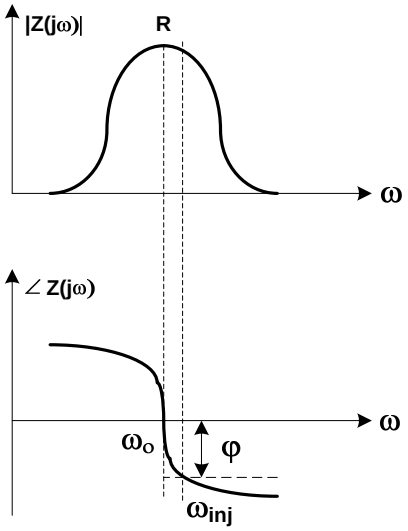


Fig. 2-17 Magnitude and phase of the tank impedance over the frequency

The following conditions are satisfied simultaneously in the steady state:

$$\tan\varphi = \frac{I_{inj}\cdot\sin\theta}{I_o + I_{inj}\cdot\cos\theta} \tag{2-27}$$

$$\tan\varphi \approx \frac{2Q}{\omega_o}(\omega_o - \omega_{inj}) \tag{2-28}$$

where Q is the quality factor of the tank. Two possible solutions, θ and 180^o-θ, exist for the same φ, I_{inj} and ω_{inj}. However, it was proved that only one solution with the higher amplitude of I_T is stable [2-17]. Therefore, θ reaches the maximum at

$$\varphi_{max} = arcsin\frac{I_{inj}}{I_o} \tag{2-29}$$

and

$$\theta_{max} = 90^{\circ} + \varphi_{max} \tag{2-30}$$

The locking range of the ILO is

$$Locking\ Rang = 2\left|\omega_o - \omega_{inj}\right| = \frac{\omega_o}{2Q}\frac{I_{inj}}{\sqrt{(I_o)^2-(I_{inj})^2}} \tag{2-31}$$

From (2-31), both the Q and the injection strength affect the locking range of the ILO. A small Q and large injection current are desirable for a wide locking range.

2.6. Quadrature LO Signal Generators

A quadrature LO signal generator is an important building block for many RF transceivers. With In-phase (I) and Quadrature (Q) signals, the local oscillator can drive a mixer to select higher or lower sidebands or extract the information on either side of the spectrum. Design of a low-noise, low-power, and compact LO that can generate quadrature signals at several GHz, using aggressively scaled down CMOS technology, is still a challenge to RF designers.

Many different quadrature LO topologies have been explored over the years, such as a single VCO followed by a divide-by-two, two coupled VCOs under injection locking, or so-called quadrature VCO (QVCO), a singe VCO combined with a poly-phase filter and an even-stage ring oscillator. Since an LC oscillator tends to be the best choice for high performance oscillators, the LC oscillator is assumed in the following unless stated otherwise.

2.6.1. Single VCO followed by a divide-by-two

The most popular scheme to generate quadrature signals is use of a VCO running at twice the LO frequency followed by a divide-by-two [2-18]-[2-20]. The block diagram of a differential VCO driving a latch-based divider for quadrature generation is shown in Fig. 2-18. The two VCO output signals, V_{vcop} and V_{vcom}, are 180º out of phase. One latch

toggles on a rising edge of V_{vcop}, the other on a rising edge of V_{vcom}, or a falling edge of V_{vcop}. If V_{vcop} and V_{vcom} have 50% duty cycle, $I_p(I_m)$ and $Q_p(Q_m)$ are 90º out of phase.

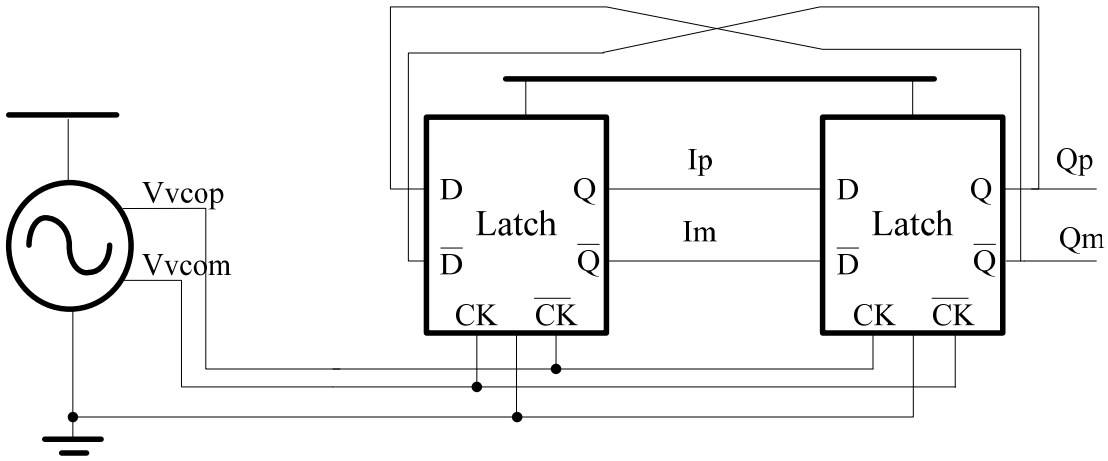


Fig. 2-18 A block diagram of a differential VCO driving a latch-based divider

The divider can be implemented in numerous ways. It is crucial to select an appropriate topology to meet specific design objectives. The current mode logic (CML) divider is the most widely used topology due to its high operation frequency and wide input frequency range. The CMOS logic based topologies, such as sense amplifier-based or true single-phase clock (TSPC) flip-flops [2-21], are suitable for medium frequency and low power applications. Miller divider [2-22] and injection-locked divider [2-23] are good candidates for very high frequency applications, which are shown in Fig. 2-19.

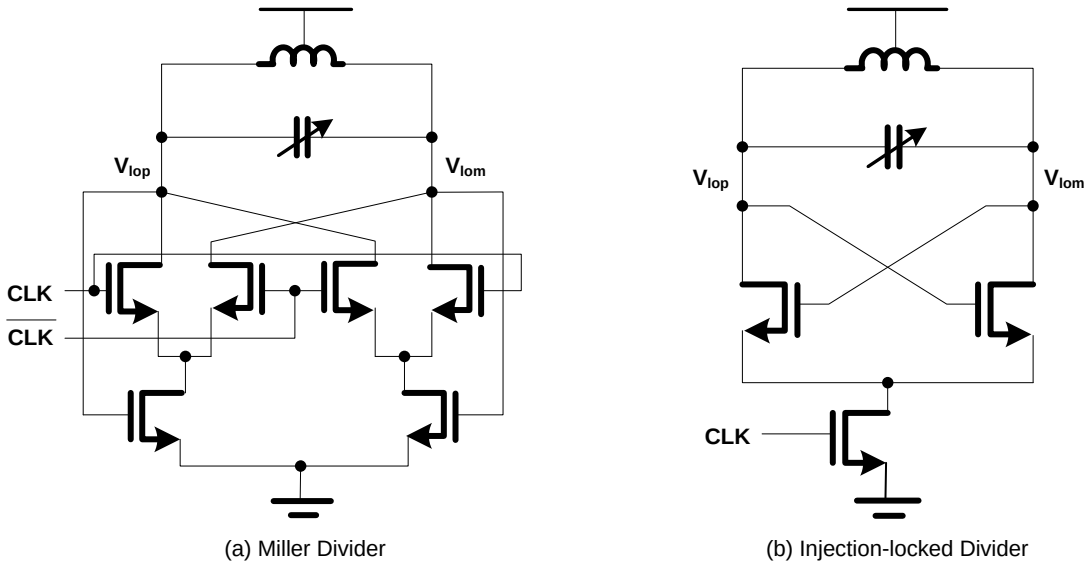


Fig. 2-19 Miller divider and injection-locked divider

The advantage of a "VCO followed by a divide-by-two" approach is small die area due to the small size of passive components necessary for the VCO running at twice the LO frequency. However, the primary concern is large power consumption, especially when the divider operates at a very high frequency. In addition, a non-50% duty cycle of the input signal causes I and Q phase imbalance.

2.6.2. Quadrature VCO (QVCO)

A quadrature LC oscillator was first proposed by Rofougaran et al. in 1996, in [2-24]. Since then many researchers have followed to seek better understandings or improved designs [2-17], [2-25]-[2-30]. A conventional QVCO is shown in Fig. 2-20. It includes two identical LC oscillators, which are injection-locked to each other at a common frequency. The relative size of the coupling transistors determines the injection strength, which is normally large.

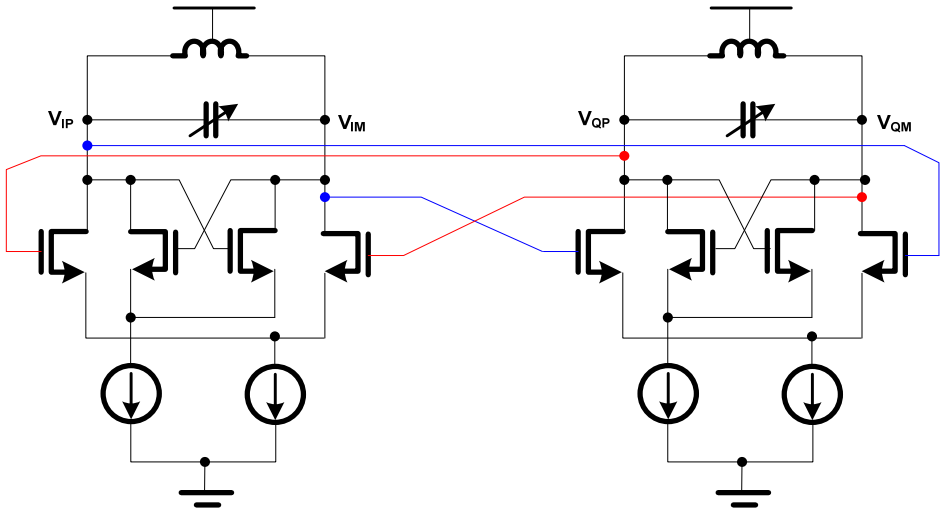


Fig. 2-20 A conventional quadrature LC VCO

The operation conditions of the QVCO can be analyzed based on a linearized model, which is shown in Fig. 2-21. It is assumed that the two cores match perfectly, and the transconductance of the coupling transistor G_m is real, or equivalently, the differential injection current is in phase with the differential voltage applied to the gate.

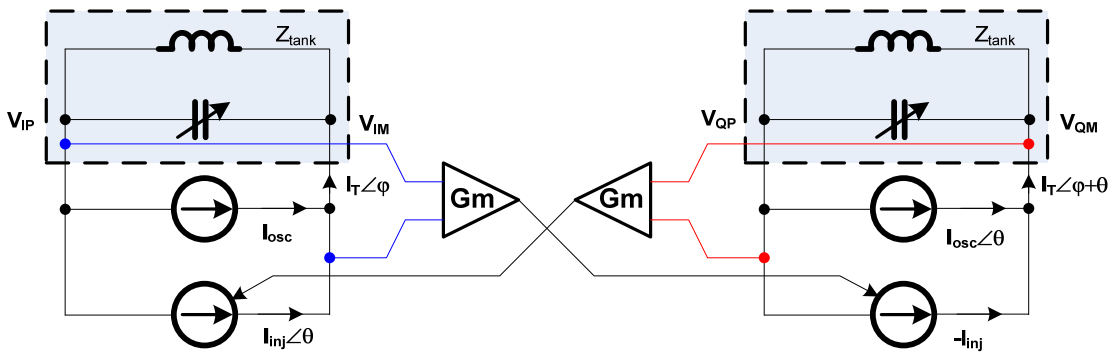


Fig. 2-21 Linearized model of a QVCO

In the steady state, the two LC tanks oscillate at the same frequency. At the output nodes, we can write the following KCL equations:

$$I_{osc} + I_{inj}e^{j\theta} = I_T e^{j\varphi} \quad (2\text{-}32)$$

$$I_{osc}e^{j\theta} - I_{inj} = I_T e^{j(\varphi+\theta)} \quad (2\text{-}33)$$

$$\Rightarrow I_{inj}\left(1 + e^{j2\theta}\right) = 0$$

Since the injection current is non-zero, then the solutions are

$$\theta = \pm 90° \quad (2\text{-}34)$$

which means the two oscillators produce quadrature outputs. However, there exist two modes, corresponding to two different oscillation frequencies, ω_1 and ω_2. Both of them are stable solutions. $V_{QP}(V_{QM})$ could be either 90º lead or lag to $V_{IP}(V_{IM})$. The vector diagram and the tank impedance are illustrated in Fig. 2-22. Bimodal oscillation is an unwanted behavior, as the frequency ambiguity may lead to very poor phase noise, and the phase ambiguity can cause the output of the following complex mixers unpredictable. In practical implementation, the tank impedance around the self-resonant frequency is asymmetry, or $|Z(j\omega_1)| \neq |Z(j\omega_2)|$, the higher frequency mode is normally sustained due to a higher amplitude [2-17]. Nevertheless, there is still possibility that bimodal oscillation could happen due to the variations of process, temperature and device mismatch. A few design or calibration approaches were explored to address this problem in [2-29], [2-30].

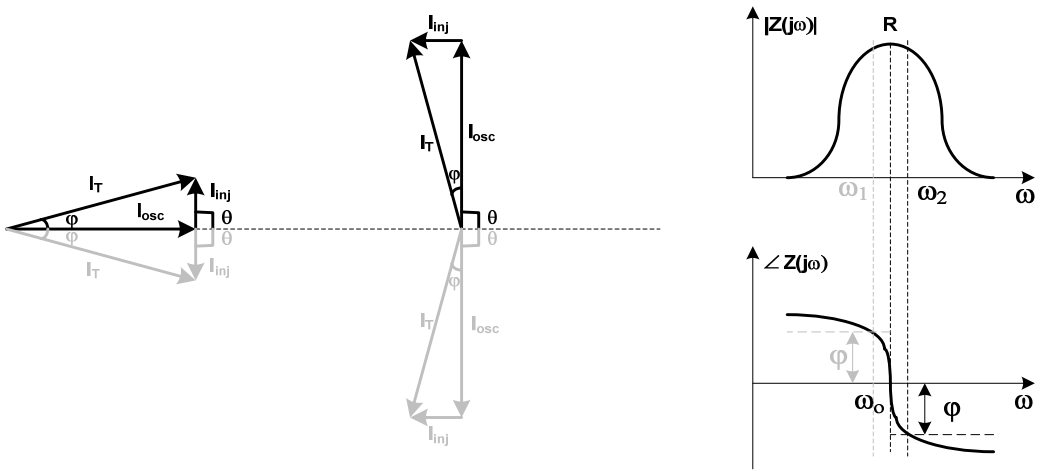


Fig. 2-22 Vector diagram and tank impedance of a QVCO

Mismatch between the two oscillators causes the *I/Q* imbalance. To minimize the phase error arising from mismatch, it is desirable to lower the *Q* of the tank and strengthen the injection current. However, those measures increase the phase noise. Introducing an approximate 90º phase shift in the coupling path can desensitize the output phase to mismatch and lower the phase noise [2-17].

The advantages of using a QVCO to generate quadrature signals are relatively low power consumption and high output swing. But two LC cores occupy large die area, the circuit potentially suffers from bimodal oscillation, and the design of *Q* and coupling factor involves tradeoff between phase noise and phase error.

2.6.3. Single VCO with a poly-phase filter

A simple technique to generate quadrature signals is use of an RC-CR network as shown in Fig. 2-13. It consists of a low-pass filter and a high-pass filter. The two outputs have 90º phase difference at all the frequencies, but the same amplitude at only one frequency of $1/(2\pi RC)$. Thus it is only suitable for narrow band application. Moreover, it is very susceptible to process and temperature variations.

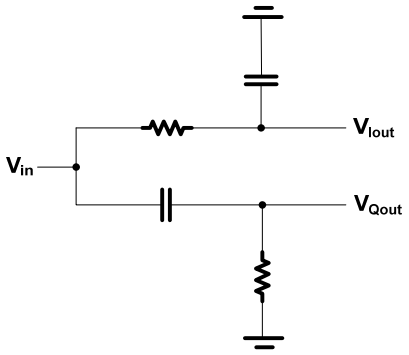


Fig. 2-23 an RC-CR network

Alternatively, a series of asymmetric polyphase filters (PPFs) developed by Gingell [2-31] are commonly used for generation of quadrature signals. Fig. 2-24 shows two different circuit implementations of the PPF. It can be seen that the PPF can be viewed as an n-stage RC network. Each stage consists of four identical resistors and four identical capacitors. Although the difference between Type-I and Type-II PPFs is only the input configuration, it has significant impact on the performance [2-32].

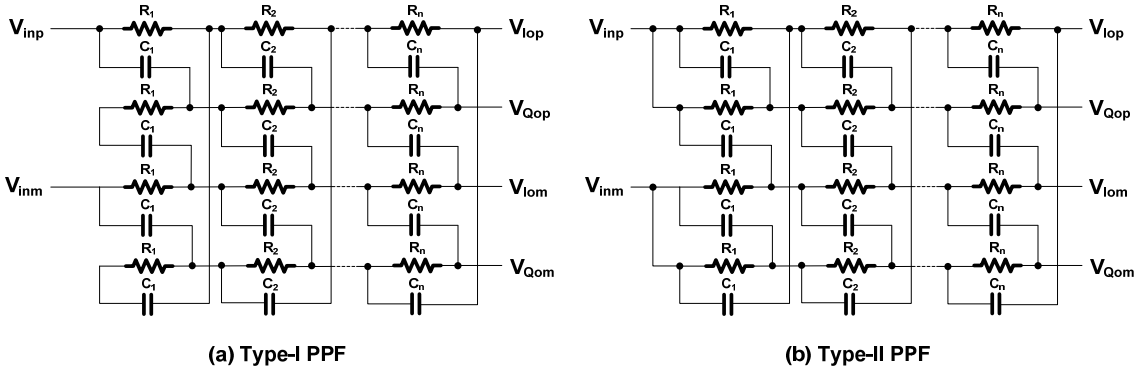


Fig. 2-24 Two types of circuit implementation of PPFs

For Type-I PPFs, the phase difference between *I* and *Q* outputs is equal to 90º at all frequencies, regardless of the *R* and *C* values and the load impedance. The amplitude balance is achieved only at each RC pole. Increase of the network stages broadens the effective bandwidth. For Type-II PPFs, *I* and *Q* outputs have the same amplitude at all frequencies, but the phase difference is 90º only at each RC pole. Similarly, the bandwidth can be extended by increasing the number of RC-CR network stages.

The advantage of using passive PPFs to generate quadrature signals is simple design, as only resistors and capacitors are used. However, in practical implementations, it has several disadvantages that limit its wide applications:

- **Signal Loss**. Theoretically, each stage of the passive PPF has 3 dB insertion loss. The parasitic capacitors and resistors make the signal loss even worse. Thus, a buffer or amplifier is usually needed to compensate the signal attenuation. Those buffers can consume large power for high-order PPFs .
- **Component Variation**. The values of the on-chip passive components have large process and temperature variations. Therefore, the bandwidth of the PPF needs to be sufficiently wide, so that the band of interest can be covered under all the conditions. Consequently, a high-order PPF is normally required.
- **Layout Dependency**. A good matching between I and Q channels requires large layouts of resistors and the capacitors, which inevitably increases the die area.

To mitigate some of the issues mentioned above, active polyphase filters were proposed in [2-33], [2-34]. The passive resistors are replaced with the transconductance stages. The advantages of the active PPFs compared to the passive ones include the possibility of filter calibrations, tuning and signal amplification [2-34]. However, they are obtained at the expense of increased circuit complexity, power consumption and phase noise.

2.7. Low-Power VCOs and Quadrature LOs

Various low power techniques developed for existing VCOs and quadrature LOs can be classified basically into two categories: ***low voltage operation*** and ***bias current reuse*** [2-35]-[2-43]. The power consumption of a circuit is the current multiplied by the supply voltage. Therefore, if a circuit can operate at lower supply voltage with the same current (***low voltage operation***), or if it can use less current with the same supply (***bias current reuse***), the power consumption can be reduced.

2.7.1. Low Voltage Operation

Low supply voltage imposes several challenges for VCO designs [2-44]. First, the maximum VCO voltage swing is limited by the supply voltage. The reduced supply for conventional VCOs operating in the voltage limited region leads to a smaller VCO swing, which degrades the phase noise performance according to Leeson's equation [2-45]. Second, the reduced supply limits the voltage headroom so that the tail current source is usually removed. The bias current and the start-up gain for a self-biased circuit, such as a CMOS cross-coupled VCO, are susceptible to process and temperature variations. A few techniques were proposed to overcome the shortcoming.

a) Inductive Feedback (Transformer Feedback)

Kwok and Luong demonstrated that a transformer feedback (TF) VCO can operate at a supply below the threshold voltage in [2-35]. As shown in Fig. 2-25, the primary and secondary coils of the transformer are connected to the drain and the source terminals of transistor, respectively. The drain voltage could be higher than the supply voltage with use of the drain inductor, and the source voltage could be lower than the ground level with the source inductor. It is an interesting design, but it lacks insightful analysis and explicit design guidelines in [2-35].

To gain a better understanding on how the circuit works, we can analyze it using its half-circuit shown in Fig. 2-25. The primary coil L_d resonates with C to form the main tank. The drain current i_s, or the current flowing into the secondary coil L_s, is approximately equal to V_G/R_d, as the currents in L_d and C cancel each other. The magnitude of the current flowing into the primary coil i_p, is about Q_p times larger than that of i_s, where Q_p represents the quality factor of the primary coil. Since Q_p is typically high, $|i_p|>>|i_s|$. Then the source voltage, $-V_s$, can be derived as:

$$-V_s = i_s \cdot (sL_s + R_s) + i_p \cdot sM \approx i_p \cdot sM \quad (2\text{-}35)$$

where M is the mutual inductance between L_d and L_s. And the drain voltage, $-V_G$, is:

$$-V_G = i_p \cdot sL_d + i_s \cdot sM \approx i_p \cdot sL_d \quad (2\text{-}36)$$

(2-35) and (2-36) indicate that the drain and the source voltages are in phase. Therefore, the VCO swing can be enhanced effectively. The oscillation frequency is mainly determined by the primary inductance and the capacitance as:

$$f_o \approx \frac{1}{2\pi\sqrt{L_d C}} \tag{2-37}$$

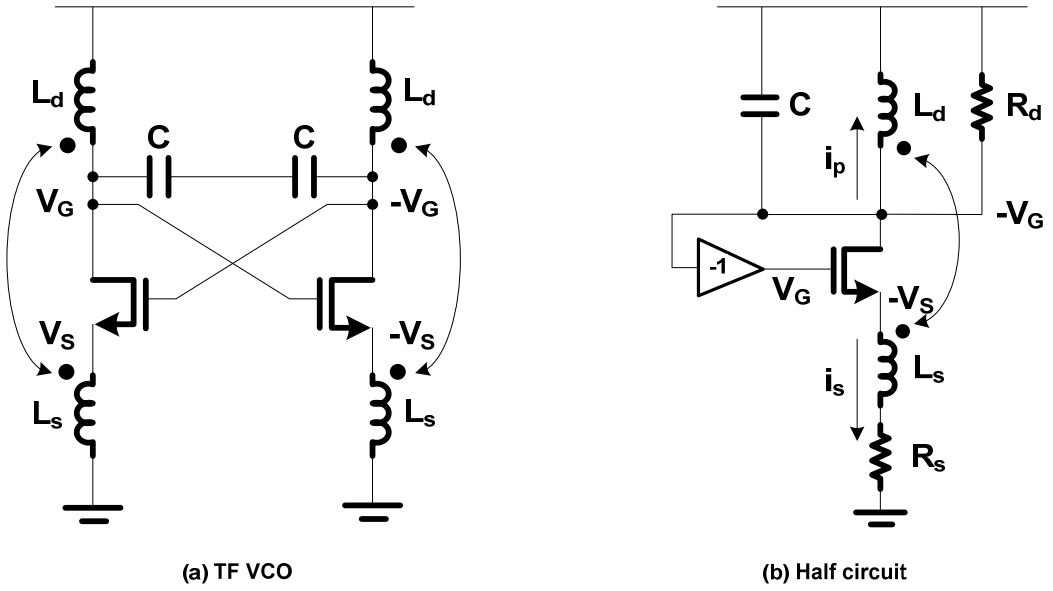


Fig. 2-25 A transformer-feedback VCO for ultra-low-voltage operation [2-35]

A CMOS version of transformer feedback VCO was presented in [2-36]. With a three-coil transformer, the maximum VCO swing is extended beyond the supply limit.

b) Capacitive Feedback

Wang proposed capacitive feedback (CF) technique to improve the signal swing [2-37]. Hsieh and Lu demonstrated that the VCO can operate at a reduce supply voltage by utilizing capacitive feedback as shown in Fig. 2-26 [2-38]. Their circuit is similar to the one in Fig. 2-25, except that the positive feedback is realized through capacitive coupling instead of magnetic coupling.

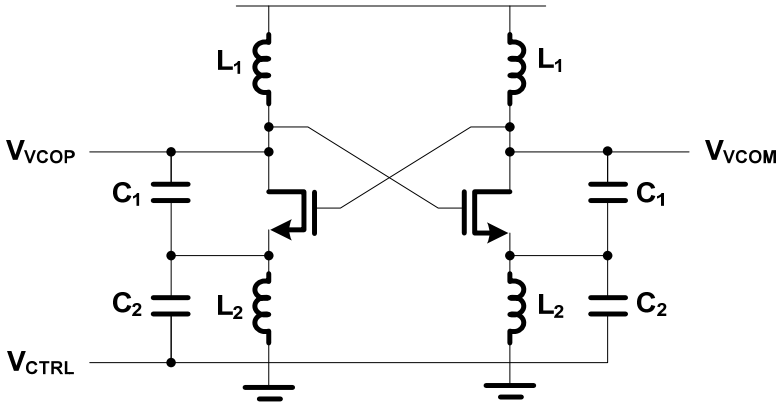


Fig. 2-26 A capacitive-feedback VCO for ultra-low-voltage operation [2-38]

With the inductors L_1 and L_2, and the feedback loop formed by C_1 and C_2, the drain voltage can swing above the supply voltage and the source voltage can swing below the ground potential. As a result, the VCO amplitude is enhanced. However, selection of C_1 and C_2 involves a tradeoff between the frequency tuning range and the power consumption.

c) Forward Body Bias (FBB)

The threshold voltage of a MOS transistor is a function of the bulk voltage. This is called body effect that can be quantified by the following equation [2-46]:

$$V_t = V_{t0} + \gamma(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F}) \quad (2\text{-}38)$$

where V_{t0} is the threshold voltage when the bulk-to-source voltage V_{BS} is zero, ϕ_F and γ are physical parameters. Thus, the effective threshold voltage can be reduced by applying a forward bias voltage to the body. With the FBB technique, the VCO can operate at a supply voltage as low as 0.4 V in [2-38].

d) Gate Bias

A conventional cross-coupled CMOS VCO requires (V_{gsp}+V_{gsn}) of the supply voltage for proper bias. Deng et al. reported that the CMOS VCO can operate at a supply voltage of 0.5 V by employing ac-coupled differential pairs [2-39]. Fig. 2-27 shows the schematic of an ac-coupled differential pair with an independent gate bias. The drawbacks of the gate bias are signal attenuation due to the capacitive divider, and extra noise contribution from the resistors. As a matter of fact, the drain voltages for the circuit in [2-39] should be well defined to ensure that all the transistors are in saturation region.

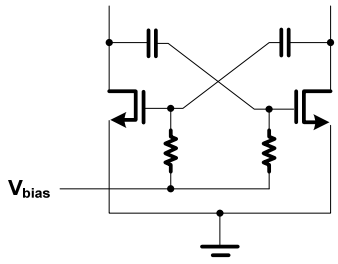


Fig. 2-27 An ac-coupled differential pair with independent gate bias

2.7.2. Current Reuse

A straightforward way of sharing bias current among multiple blocks is stacking them up under the same supply. It is essentially equivalent to lower the supply voltage of each individual block. So all the design challenges for low-voltage operation remain. Furthermore, the VCO phase noise may be degraded due to the weak isolation and/or the loading effect. A few different circuit topologies based on the current reuse technique have been published in [2-40]-[2-43].

a) Stacking VCO and Divide-by-two

Park and Cho proposed to stack a divide-by-two on top of a CMOS LC VCO as shown in Fig 2-28 [2-40]. The cross-coupled PMOSs are shared by the VCO and the divider, which reduces the number of the transistors. However, there are still four transistors stacked up, it requires a minimum supply voltage of 1.8 V for robust operation and good phase noise performance.

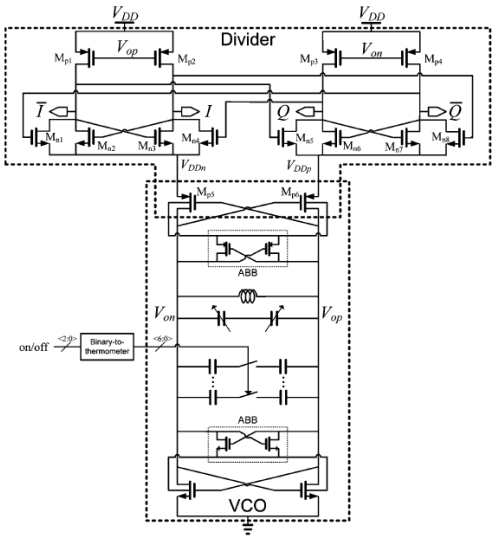


Fig. 2-28 Proposed VCO and divide-by-two in [2-40]

Another current reusing VCO and divide-by-two topology was proposed in [2-41] and shown in Fig. 2-29. An NMOS-only LC VCO is stacked on the top of a divide-by-two. The VCO differential output voltages are applied to the divider through ac-coupling capacitors. A big capacitor C_{AC} is added between the VCO and the divider to provide solid ac ground. Similarly, the circuit needs a 1.8 V supply to operate.

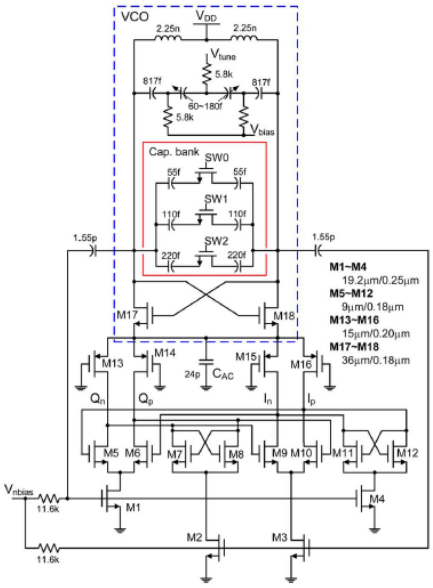


Fig. 2-29 Proposed VCO and divide-by-two in [2-41]

Leung and Luong successfully lowered the supply to 1 V by utilizing a transformer-feedback VCO in a common-drain configuration in [2-42]. The schematic of the circuit is shown in Fig. 2-30. Two additional negative *gm* cells are utilized to boost the quality factors of the primary and the secondary tanks. The switched capacitor bank is connected at the secondary coil, and the varactors are at the primary coil. However, the operation principle of the circuit is not well analyzed in the paper. Though the drain voltage can swing below the ground level, the effective supply voltage is actually reduced as the drain and the source voltages are in phase, which is different from the transformer-based VCO in [2-35]. The small signal analysis provided in the paper is based on the assumption that the self-resonant frequency of the secondary tank is much higher than that of the primary tank, which may not be valid in real implementation, as the switched capacitor bank is normally large than the varactors. For a comparative study to be presented in Section 3.2.1, we have derived the start-up gain of their circuit as:

$$g_m \omega Q_p M \left(1 - \frac{M}{L_p}\right) > 1 \qquad (2\text{-}39)$$

where g_m is the transconductance of the NMOS transistor, Q_p the quality factor of the primary coil, L_p the primary inductance and M the mutual inductance.

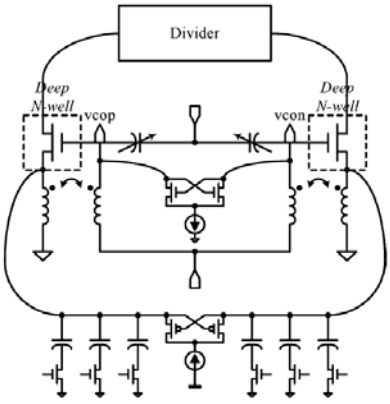


Fig. 2-30 Proposed VCO and divide-by-two in [2-42]

b) Stacking LNA, Mixer and LO

Cheng et al. proposed a low-power GPS receiver by merging the LNA, the quadrature mixer and the quadrature LO in a single current-reuse stacked topology as shown in Fig. 2-31 [2-43]. A gate-modulated NMOS-only quadrature VCO is utilized for low voltage operation. The overall power consumption of the receiver is very low. However, the receiver noise figure and the linearity can be hardly optimized due to the fact that the LNA, the mixer and the QVCO have to use the same amount of the bias current.

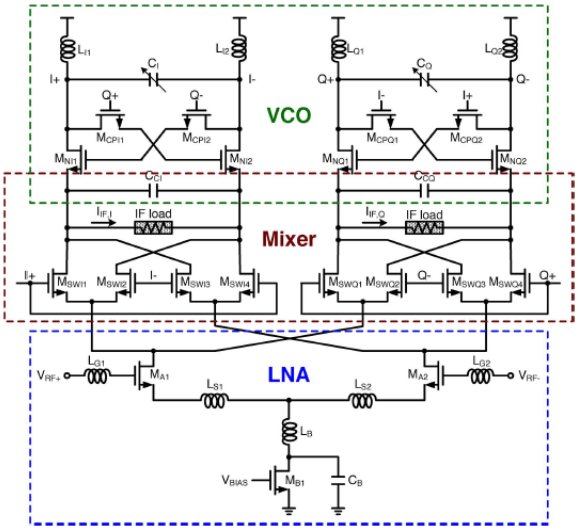


Fig. 2-31 Double-balance quadrature LNA, mixer and VCO in [2-43]

2.7.3. Limitations of existing designs

The supply voltage across the chip is normally unified, and its minimum value is set by all the blocks, not just the VCO. Therefore, even though the VCO can operate at lower supply voltage, the power for the VCO alone cannot be reduced. Hence, it is more feasible to achieve low power with a current reuse technique. However, the existing published works have some limitations. First, the minimum supply voltage is too high when stacking many transistors in one branch [2-40], [2-41]. A transformer-feedback VCO stacked with a divide-by-two can operate at low supply voltage. But the circuit requires two additional cross-coupled pairs and current sources to boost the start-up gain, which increases the circuit complexity and power consumption [2-42]. More importantly, the detailed analysis on the circuit, the optimization strategy and the systematic design methodology are missing.

2.7.4. Proposed Research

We propose to explore a new quadrature LO generation circuit suitable for low-power and low-voltage wireless applications, and have an in-depth understanding on the circuit behavior in this research. The proposed LO stacks a transformer-based VCO and a divide-by-two [2-47], which can achieve high VCO start-up gain, low voltage operation and low power consumption simultaneously. The Armstrong VCO configuration adopted in the design mitigates the small voltage headroom and the noise coupling encountered in the current reused topology. Also, the operation conditions and the phase noise of the LO are analyzed comprehensively based upon some approximate models. The details will be covered in the following chapter.

2.8. Summary

In this chapter, background on the oscillators which are relevant to the proposed research is provided. Two classical models to analyze an oscillator are described: one is a two-port model based on positive feedback, and the other one a one-port model based on negative resistance. Key oscillator design parameters include phase noise, tuning range and quality factor.

A few conventional oscillator topologies are described. Each one has its own pros and cons. In general, crystal oscillators are used as reference clock sources in frequency synthesizers for high frequency-stability. Ring oscillators are very compact, but rarely used in high-performance synthesizers due to the poor phase noise and the high power consumption. Traditional Amstrong, Colpitts and Hartley oscillators are not very popular these days, but proven useful for some applications. Cross-coupled LC voltage-controlled oscillators are the most widely used ones owing to the low phase noise, the wide tuning range, and the good start-up behavior. Injection-locked oscillators have been employed for frequency division, or multi-phase generation such as quadrature VCO.

There are basically three schemes to generate quadrature signals. The most common approach is use of a VCO running at twice the LO frequency followed by a divide-by-two stage. It requires relatively small die area due to the small size of passive components. However, it usually consumes large power for a high frequency. Another approach is use of two identical VCOs running at the LO frequency coupled to each other with the 90° phase shift. It dissipates relatively small power, but two LC cores occupy large die area, and bimodal oscillation could happen if not handled properly. The third approach is combination of a single phase VCO and a polyphase filter. A high-order RC filter is usually required to generate accurate quadrature signals. However, this also leads to a large die area. Also, a voltage limiter is often placed at the output to minimize the amplitude mismatch, but it increases the power consumption and contributes the phase noise due to the AM-to-PM conversion.

The existing low power techniques utilized in the VCOs and the quadrature LOs can be categorized into two groups: low-voltage operation and current reuse. The advantages as well as the limitations of the previous works have been identified and summarized. This research work aims to improve the existing low-power LO designs by investigating a new circuit topology and providing a systematic design methodology.

Chapter 3 Analysis and Design of a Low-Power Low-Voltage Quadrature LO

Since a quadrature LO generation circuit is usually a highly power hungry block in a transceiver, it is crucial to design a power-efficient LO for a given supply voltage, which scales down in deep sub-micron technology. A new quadrature LO topology of stacking a transformer-based VCO and a divide-by-two is thereby investigated for the dissertation research. Both analytical and measurement results show the effectiveness of the proposed configuration in low-power wireless applications.

This chapter begins with a brief review of a conventional LO, which is used to explain the proposed scheme and its analysis. The proposed LO adopts the Armstrong transformer-based VCO configuration in stead of an LC tank. The magnetically cross-coupled differential pair for loss compensation takes only small voltage headroom. The main resonant tank is placed between the gates of the differential pair, while the divide-by-two is driven by the drain current. Hence, the divide-by-two is isolated from the resonator to minimize the noise coupling between the divider and the VCO core. The start-up condition, the oscillation frequency and the VCO amplitude of the proposed LO are analyzed using a linearized small-signal model. In order to understand the noise mechanism and to quantify the noise, both a linear time-invariant (LTI) model and a linear time-variant (LTV) model are used to estimate the VCO phase noise contributions of the resonant tank, the VCO differential pair, and the divide-by-two. The results show that a high quality factor of the primary inductor is always preferable, and the mutual inductance between the primary and the secondary coils plays an important role in the design tradeoffs among start-up gain, power and noise. The mathematical equations are derived and verified with the simulations. Finally, the guidelines on the transformer parametric and layout designs are discussed.

The proposed LO was designed and fabricated in TSMC CMOS 65 nm technology for GPS receiver. The specifications, the circuit implementations and the measurement results will be provided in details in the following chapter.

3.1. Description of the Proposed LO and Its Operation

A conventional quadrature LO architecture is illustrated in Fig. 3-1. A CMOS LC-tank VCO oscillates at twice the LO frequency, and the differential VCO signals are then fed to the following divide-by-two. The current mode logic (CML) based divide-by-two is shown in the figure, which is generally preferable for high-frequency and low-noise applications. The divide-by-two has two latches, each one consisting of two sense devices, one cross-coupled pair for regeneration, and two pull-up resistors. When one latch senses the current state, the other one stores the previous state. The power consumption of the divide-by-two with quadrature differential outputs depends on the operating frequency, the output load condition, and the phase noise requirement. In some circumstances, a divide-by-two consumes more power than the VCO.

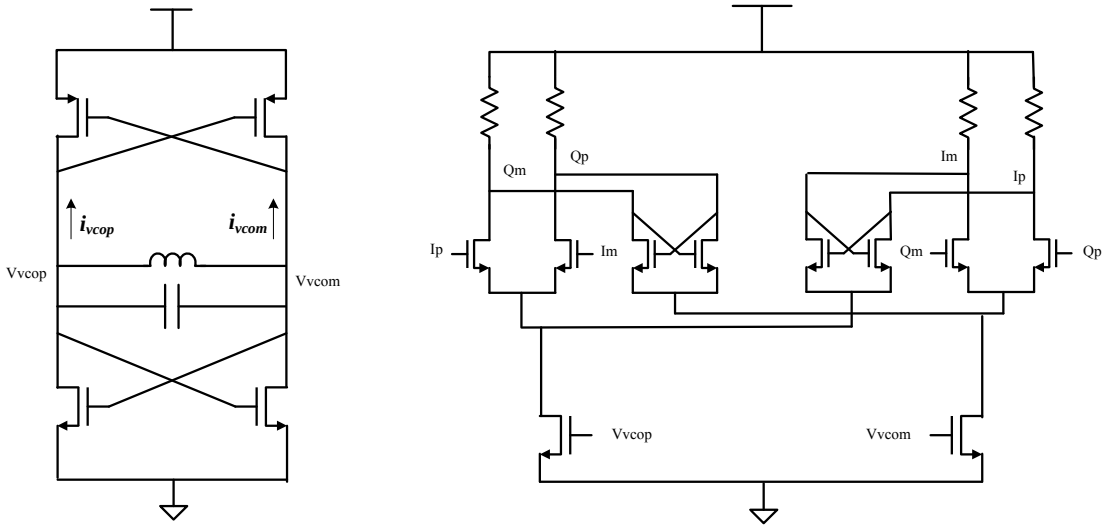


Fig. 3-1 A conventional LO architecture

It can be observed that the currents flowing in both the VCO and the divide-by-two have the same fundamental frequency, which is the VCO oscillation frequency. This prominent feature makes it possible that the VCO current directly drives the downstream divide-by-two, if their bias currents are chosen the same. One possible LO topology based on the above scheme is illustrated in Fig. 3-2. The PMOS pair of the VCO and the NMOS input pair of the divider are removed in the stacked LO topology. As the VCO current drives the latches of the divide-by-two directly, the overall power consumption can be reduced by this current reuse technique.

However, there are two primary design concerns for the candidate LO topology. First, there is a potential noise coupling from the divider to the VCO. The divider is directly seen by the resonant tank of the VCO, which may degrade the quality factor of the tank, and thus the phase noise performance. Second. there is a possible headroom issue due to stacking a larger number of devices. The required supply voltage is ($2V_{th}$ + $2V_{dsat}$ + IR) to bias the LO shown in Fig. 3-2, where V_{dsat} is the overdrive voltage of the transistor. Since the VCO is vulnerable to the supply noise, it is often necessary to add an on-chip regulator to improve supply isolation. The on-chip regulator pushes the internal operating voltage even lower than the external power supply.

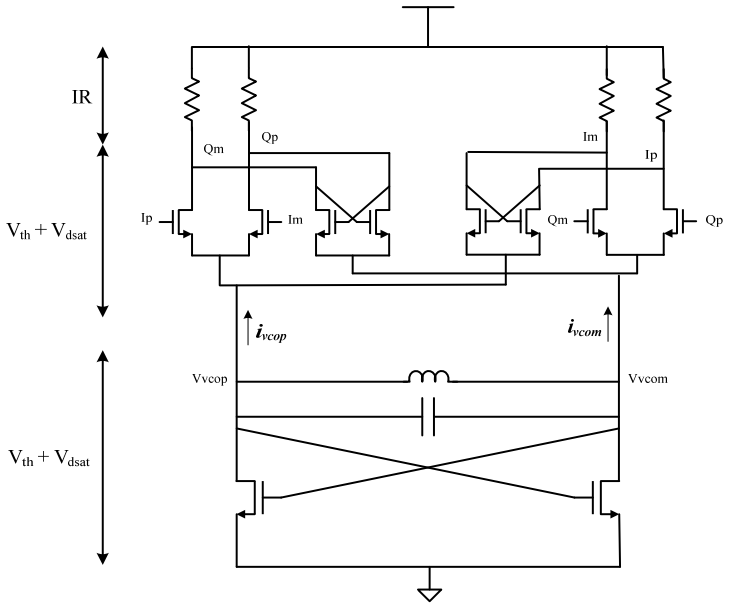


Fig. 3-2 Candidate LO topology stacking an LC VCO and a CML divide-by-two

The magnetic coupling (rather than the direct feedback) as demonstrated in Armstrong oscillator offers an effective solution to the above two problems [3-1]. Fig. 3-3 shows the proposed LO circuit based on the magnetic coupling. The transformer-based VCO has two identical transformers, one is formed by L_{p1} and L_{s1}, and the other by L_{p2} and L_{s2}. The magnetic coupling between the primary and the secondary coils provides a negative equivalent resistance to the resonant tank, and thus sustains the oscillation. The resonant tank is connected between the gates of the VCO differential pair, including two primary coils (L_{p1} and L_{p2}) and the capacitor. The two secondary coils (L_{s1} and L_{s2}) pass the current of the VCO to the divide-by-two. It can be seen that the divider does not load

the resonant tank directly, it would have little impact on the Q of the resonant tank. The required supply voltage for the propose LO is reduced to (V_{th} + $2V_{dsat}$ + IR). The inductively cross-coupled VCO differential pair operates at a very low voltage and needs only one V_{dsat}. It converts the VCO voltage signals to the current signals that drive the divide-by-two. The bias current reuse technique reduces the power consumption of the LO. In addition to the power efficiency, the proposed LO has lower supply sensitivity compared to the conventional self-biased CMOS VCO, since the resonant tank is located at the gates of the differential pair that is biased at a supply insensitive voltage.

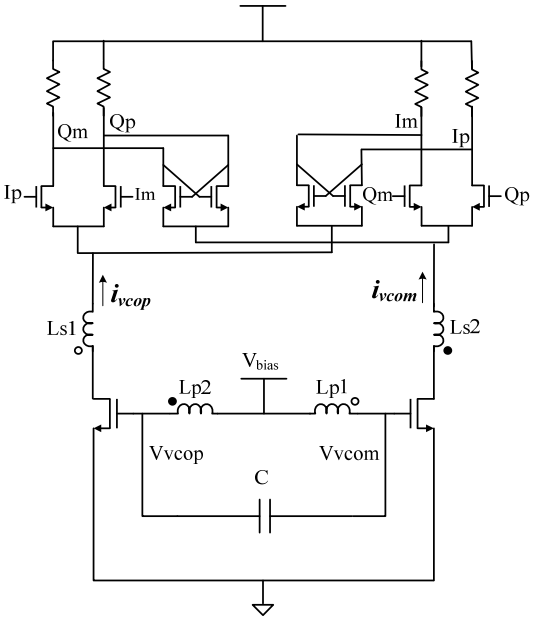


Fig. 3-3 Proposed LO topology stacking a transformer-based VCO and a CML divide-by-two

3.2. Detailed Circuit Analysis Based Upon a Linearized Small-Signal Model

Analysis of the proposed LO is rather complicated than the conventional one, as the VCO utilizes the magnetic coupling feedback to sustain the oscillation and it is stacked with the divider-by-two. In order to justify the idea and to guide the design, we need to have a solid understanding of the operation conditions of the proposed LO.

The proposed differential LO can be analyzed using its half circuit and a small-signal model shown in Fig. 3-4 and Fig. 3-5, respectively. The parameters in the figures are defined as follows.

L_p (L_s) : the primary (secondary) inductance,

R_{lp} (R_{ls}) : the series equivalent resistance of L_p (L_s),

M : the mutual inductance between the primary and the secondary coils,

C : the total capacitance at the resonator including the capacitance of the switchable capacitor bank, the capacitance of the varactor, and the gate-to-source parasitic capacitance of the transistor, (In the half circuit, the equivalent single-ended capacitance is $2C$.)

i_p (i_s) : the current flowing into L_p (L_s),

Z_{load} : the load impedance seen from the secondary coil to the divide-by-two,

g_m (R_{ds}) : the transconductance (output resistance) of the NMOS transistor,

C_{gd} (C_{db}) : the gate-to-drain (drain-to-bulk) parasitic capacitance of the NMOS transistor,

V_1 (V_2) : the gate (drain) voltage of the NMOS transistor,

Z_{in} : the impedance seen by the capacitor $2C$,

Z_{tank} : the impedance of the resonant tank, and

Z_{ls} : the impedance seen from the drain to the secondary coil.

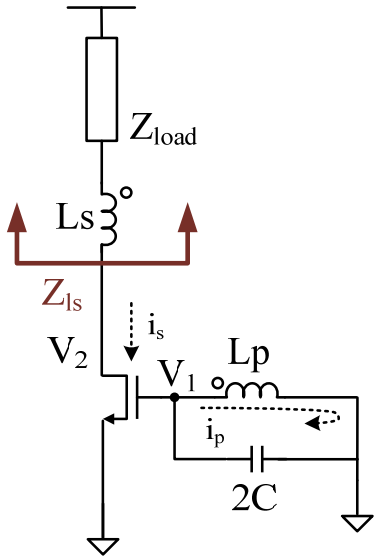


Fig. 3-4 Half circuit of the proposed LO

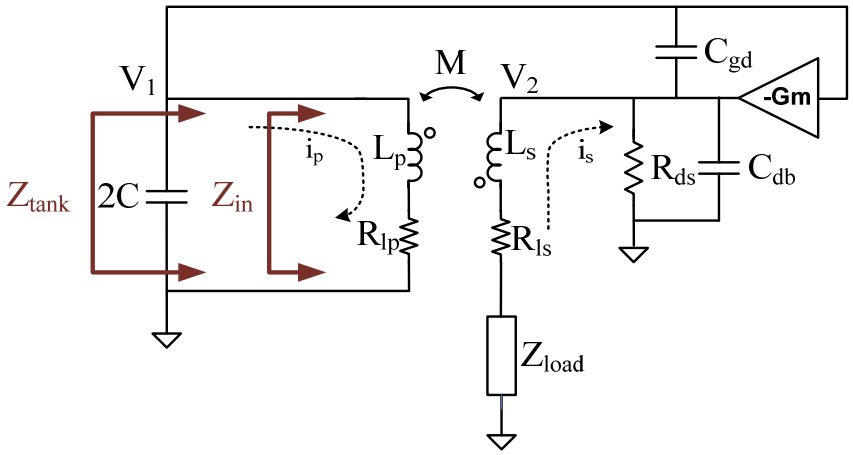


Fig. 3-5 Linearized small-signal model of the proposed LO

3.2.1. Start-up Condition

From the equivalent circuit shown in Fig. 3-5, we can obtain the following equations based on Kirchhoff's voltage law and current law:

$$V_1 = i_p \cdot sL_p + i_p \cdot R_{lp} + i_s \cdot sM \tag{3-1}$$

$$V_2 = -i_s \cdot sL_s - i_s \cdot R_{ls} - i_p \cdot sM - i_s \cdot Z_{load} \tag{3-2}$$

$$i_s = -V_1 \cdot (-g_m) + \frac{V_2}{R_{ds}} + V_2 \cdot sC_{db} - (V_1 - V_2) \cdot sC_{gd} \tag{3-3}$$

The impedance seen by $2C$ can be derived as the following:

$$V_1 = \frac{(R_{lp}+sL_p)\cdot(1+{}^{B}/_{A})-{}^{(sM)^2}/_{A}}{1-sM\cdot(g_m-sC_{gd})+{}^{B}/_{A}} \cdot i_p$$

$$Z_{in} = \frac{V_1}{i_p} = \frac{(R_{lp}+sL_p)\cdot(1+{}^{B}/_{A})-{}^{(sM)^2}/_{A}}{1-sM\cdot(g_m-sC_{gd})+{}^{B}/_{A}} \tag{3-4}$$

$$A = \frac{1}{s(C_{gd}+C_{db})+{}^{1}/_{R_{ds}}}$$

$$B = sL_s + R_{ls} + Z_{load}$$

where A stands for the parallel impedance of R_{ds}, C_{gs} and C_{db}, and B stands for the series impedance of R_{ls}, C_{ls} and Z_{load}. Typically, $|A| >> 1$ and $|A|$ is much larger than $|B|$, or $|B/A| << 1$. Then, (3-4) can be simplified as

$$Z_{in} \approx \frac{R_{lp}+sL_p}{1-sM\cdot g_m} \tag{3-5}$$

The impedance of the resonant tank can be expressed as:

$$Z_{tank} = Z_{in} || {}^{1}/_{\omega 2C} = \frac{R_{lp}+sL_p}{1+s(2CR_{lp}-g_mM)+s^2 2CL_p} = \frac{R_{lp}+sL_p}{1-\omega^2 2CL_p+s(2CR_{lp}-g_mM)} \tag{3-6}$$

The real part of Z_{tank} is

$$R_e(Z_{tank}) = \frac{R_{lp} - \omega^2 L_p g_m M}{(1-\omega^2 2CL_p)^2 + (2CR_{lp} - g_m M)^2} \quad (3\text{-}7)$$

And the imaginary part of Z_{tank} is

$$I_m(Z_{tank}) = \frac{L_p - \omega^2 2CL_p^2 - 2CR_{lp}^2 - g_m M R_{lp}}{(1-\omega^2 2CL_p)^2 + (2CR_{lp} - g_m M)^2} \quad (3\text{-}8)$$

The proposed LO is guaranteed to oscillate when the real part of Z_{tank} becomes negative. So the start-up condition is

$$R_{lp} - \omega^2 L_p g_m M < 0$$

$$\Rightarrow g_m \omega Q_p M > 1 \quad (3\text{-}9)$$

where Q_p represents the quality factor of the primary coil, which is approximately equal to $\omega L_p/R_{lp}$. (3-9) indicates that the transformer should maximize the product of M and Q_p to boost the VCO start-up gain.

For comparative study, let's examine the start-up condition for a conventional VCO. A CMOS cross-coupled VCO usually has larger effective transconductance due to the extra PMOS pair than a NMOS-only VCO for the same bias current and hence larger start-up gain. From a linearized small-signal model of the conventional CMOS VCO shown in Fig. 3-6, we can derive the start-up condition similarly as

$$\frac{(g_{mn}+g_{mp})}{2} > \frac{1}{R_{ind}} = \frac{1}{\omega L Q_{ind}}$$

$$\Rightarrow \frac{(g_{mn}+g_{mp})\omega L Q_{ind}}{2} > 1 \quad (3\text{-}10)$$

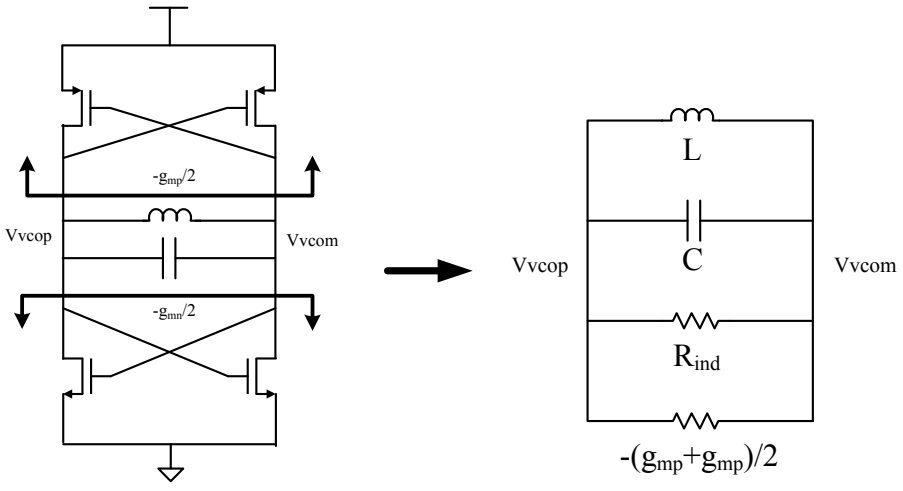


Fig. 3-6 Linearized small-signal model of the conventional CMOS VCO

Thus, if M is chosen similar to L for the proposed VCO, then its start-up gain becomes comparable to the conventional CMOS cross-coupled VCO with the same oscillation frequency and the quality factor. Looking back at (2-39), which is the start-up condition of the LO presented in [2-42], we can see that the proposed LO has a higher start-up gain than that LO.

3.2.2. Oscillation Frequency

The oscillation occurs at the frequency, where the real and the imaginary parts of Z_{tank} become zero and infinite, respectively. So the oscillation frequency can be calculated as

$$\begin{cases} R_{lp} - \omega_o^2 L_p g_m M = 0 \\ \left(1 - \omega^2 2CL_p\right)^2 + \left(2CR_{lp} - g_m M\right)^2 = 0 \end{cases}$$

$$\Rightarrow \omega_o = {1}\Big/{\sqrt{2L_pC}} \tag{3-11}$$

The frequency is simply determined by the primary inductor and the capacitors in the resonant tank.

3.2.3. Voltage Swing and Current Consumption

To gain more insight into the circuit, we ignore R_{ds}, C_{gd} and C_{db}, which is generally a valid approximation. Also, Q_p is normally larger than 10, so that $V_1 \approx i_p sL_p$. Then the induced voltage on the primary inductor due to the magnetic coupling can be written as:

$$i_s \cdot sM \approx V_1 g_m \cdot sM \approx i_p \cdot sL_p g_m \cdot sM = -i_p \omega^2 L_p M g_m \tag{3-12}$$

The mutual inductance acts as a negative resistance of $\omega^2 L_p M g_m$ to the primary coil, which cancels out the loss in the tank and thus sustains the oscillation. If the negative resistance is larger than R_{lp}, the VCO is guaranteed to start oscillating.

Looking at the secondary coil, we can write the induced voltage due to the magnetic coupling as:

$$i_p \cdot sM = \frac{V_1}{sL_p} sM = \frac{i_s/g_m}{sL_p} sM = i_s \cdot {\omega M^2 Q_p}\Big/{L_p} \tag{3-13}$$

The mutual inductance acts as a positive resistance of $\omega M^2 Q_p / L_p$ to the secondary coil. This equivalent resistance can be re-written as:

$$\frac{\omega M^2 Q_p}{L_p} = 2\omega Q_p k_{ps}^2 L_s \quad (3\text{-}14)$$

where k_{ps} represents the coupling coefficient between the primary and the secondary coils. For the half circuit, L_p represents only half of the total primary inductance, so there is a factor of 2 in (3-14). For a reasonable design, $k_{ps} > 0.5$, $Q_p > 10$, so that the following conditions hold true, $\omega_o M^2 Q_p/L_p >> \omega_o L_s$ and $\omega_o M^2 Q_p/L_p >> R_{ls}$. Therefore the impedance looking from the drain into the secondary coil is

$$Z_{ls} = sL_s + R_{ls} + Z_{load} + \omega M^2 Q_p/L_p \approx Z_{load} + \omega M^2 Q_p/L_p \quad (3\text{-}15)$$

In the steady-state, the VCO differential voltage signals generated by the resonant tank are converted to the differential current signals by the differential pair. When the VCO voltage signals are small, as the gate voltage of the differential pair increases, the drain current rises as well. This operation region is called current-limited region. When the gate voltage reaches a certain level, the current is clipped at its peak value determined by the supply and the impedance from the drain to the supply. This clipped region is called supply-limited region [3-3]. It is generally efficient to design the proposed LO in the supply-limited region for good signal swings. Fig. 3-7 illustrates steady-state time-domain waveforms of V_1 and i_s in the supply-limited region, and Fig. 3-8 shows i_s-V_1 characteristics in the current-limited and the supply-limited operation regions. V_1 is a nearly-sinusoidal voltage with a repetition frequency of f_o determined by the resonant tank. The current i_s has a waveform close to a square wave, which is composed of the fundamental and the odd harmonic frequency terms. The current flowing into the secondary coil is coupled to the resonator through the mutual inductance. The higher-order harmonics are filtered out by the resonator. The fundamental flows through the primary coil to determine the VCO differential voltage swing.

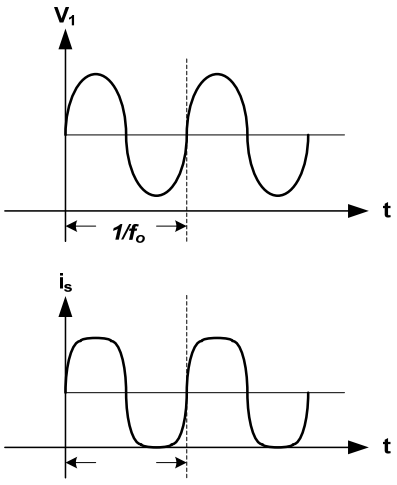


Fig. 3-7 Steady-state time-domain waveforms of V_1 and i_s

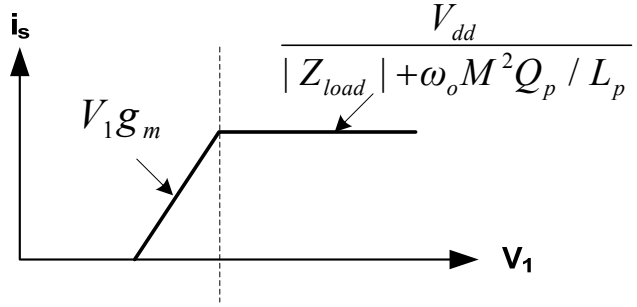


Fig. 3-8 i_s-V_1 characteristics in current-limited and supply-limited operation regions

When the LO reaches the steady-state in oscillation, the magnetic coupling between the primary and the secondary coils completely compensates the tank loss to hold the following condition:

$$I_p \cdot R_{lp} + I_s \cdot sM = 0 \quad (3\text{-}16)$$

where I_p and I_s are the amplitudes of the fundamental spectrums of i_p and i_s, respectively. Then the differential voltage across the resonant tank is expressed as:

$$V_{VCO} = I_p \cdot 2sL_p = I_s \cdot 2\omega_o M Q_p \quad (3\text{-}17)$$

Equation (3-17) indicates that the larger the mutual inductance and the quality factor of the primary coil are, the smaller the current consumption is for the same VCO swing. For comparison, the differential voltage across the tank of a conventional NMOS VCO can be written as $V_{VCO} = I_s \cdot R_p = I_s \cdot \omega_o LQ$ [3-9]. If M is larger than $L/2$ for the proposed LO, then its current consumption is lower than the conventional VCO followed by a divide-by-two

for the same oscillation frequency and the quality factor. Thus, the proposed LO is more power efficient with a large M especially when the power consumption of the divide-by-two is high possibly due to a stringent far-offset phase noise requirement.

For the sake of simplicity, we assume that the current waveform flowing through the secondary coil is an ideal square wave toggling between 0 and I_{pk} in the supply-limited region. The amplitude of the fundamental spectrum of the current is

$$I_s = \frac{4}{\pi}\frac{I_{pk}}{2} = \frac{2}{\pi}\frac{V_{dd}}{|Z_{load}|+{\omega_o M^2 Q_p}/{L_p}} \tag{3-18}$$

Then, the VCO differential amplitude becomes

$$V_{VCO} = \frac{4}{\pi}\frac{V_{dd}}{|Z_{load}|/{\omega_o M Q_p}+{M}/{L_p}} \le \frac{2V_{dd}}{\pi}\sqrt{\frac{\omega_o L_p Q_p}{|Z_{load}|}} \tag{3-19}$$

(3-18) and (3-19) demonstrate the interaction between the VCO and the divider. A smaller load impedance looking into the divider results in a larger VCO amplitude, but at the cost of larger current consumption. It is always favorable to maximize Q_p, as it leads to a higher VCO swing with no power penalty. As the mutual inductance M increases, the drain current reduces, and so does the divider output swing. Therefore, the mutual inductance should not be too large. The relationship between the mutual inductance M and the VCO amplitude V_{VCO} from (3-19) is shown in Fig. 3-9, and the largest VCO swing is achieved for

$$M = M_{opt} = L_p\sqrt{\frac{|Z_{load}|}{\omega_o Q_p L_p}} \tag{3-20}$$

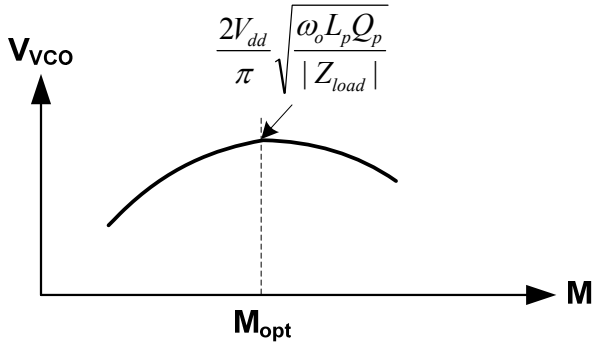


Fig. 3-9 Mutual inductance versus VCO differential amplitude in the supply-limited region

3.3. VCO Phase Noise Estimation

The noise mechanism of electrical oscillators has been investigated over many years. Leeson's equation [3-2] is one of the pioneer works to provide insights on the oscillator design. Based on a linear time-invariant (LTI) model, Craninckx and Steyaert derived a general formula of the phase noise of an LC tuned oscillator in [3-5], which is essentially similar to Leeson's heuristic equation. However, the accuracy of the LTI based method is limited because it ignores the nonlinearity and the time variation presented in real oscillators. In fact, frequency translation or modulation resulting from the nonlinearity can occur. Therefore, the approaches that can appropriately capture the time-varying and large-signal nature of the devices have gained more and more popularity, which include an impulse sensitivity function (ISF) based approach proposed by Hajimiri and Lee in [3-3], [3-4], a perturbation projection vector (PPV) based analysis published in [3-6]-[3-8] and a phasor-based method presented in [3-9]-[3-12].

Noise of an oscillator can be viewed as a perturbation superimposed on the fundamental oscillation signal. The perturbation is usually much smaller in amplitude than the steady-state carrier tone. Thus, despite the nonlinearity nature of the oscillator system, the noise-to-phase transfer function can be approximately treated as linear [3-13]. The phase response of an oscillator to the noise current impulse is time dependent. For instance, if the impulse is injected when the voltage reaches its peak value, the amplitude is perturbed immediately, but the timing of the zero crossing does not change, and there is no phase shift. On the other hand, if the impulse happens at the zero crossing, then it causes the maximum phase shift, but minimum amplitude perturbation. So the phase response to the noise is time variant regardless of how small the injected noise current is. Therefore, it is reasonable to analyze the phase noise based on a linear time-variant (LTV) model.

Hajimiri and Lee have developed a general model to quantitatively predict the phase noise of different types of oscillators [3-4]. They introduced a so-called impulse sensitivity function to measure the phase sensitivity to a current perturbation injected at a particular time. The ISF is generally determined through extensive simulations. The model further assumes that the noise in the oscillator is cyclostationary and can be treated

as the product of a stationary white noise source and a periodic function. The model is applicable to any type of oscillators, such as LC oscillators and ring-based ones. It is widely accepted for its accurate prediction at least for cases where the injected noise is stationary. However, it is more like a simulation-aided approach.

The works presented in [3-6]-[3-8] involve extensive mathematical treatments, and are considered to be the most accurate, rigorous and generic treatment of noises in oscillators, and hence is favorable for simulation tools, like Agilent's GoldenGate. However, it does not provide useful insights and intuitions to designers for improving their circuit.

The phasor-based approach proposed in [3-9]-[3-12] treats the phase noise generation mechanism in the frequency domain. It offers an alternative perspective and provides more important insights from the designer's point of view, although it is practical only for quasi-sinusoidal LC oscillators. The basic assumptions for this approach are similar to those of the ISF based approach. It is assumed that there exists a large-signal steady-state solution in the oscillator that is disturbed by the small-signal noise sources. All the noise sources are considered stationary or cyclostationary with respect to the oscillation frequency. As a matter of fact, the phasor-based and ISF based approaches are essentially equivalent. One should expect the two approaches yield the same results, which was verified in [3-11].

Both the LTI and the LTV models are utilized to analyze the phase noise performance of the proposed LO in the following sections. Through the analysis, we can gain better understanding on the noise mechanism for the proposed LO, which allows us to optimize the circuit performance. We also compare the strengths and weaknesses of the two approaches through the analysis of the proposed LO.

3.3.1. An LTI Model based Phase Noise Analysis

An LTI model of the proposed LO with all noise sources is shown in Fig. 3-10, where v_{n1} and v_{n2} represent the noise generated by R_{lp} and R_{ls}, respectively, i_{n1} the noise by the VCO differential pair and i_{n2} the noise by the divider Z_{load}. It is built from the small-signal half-circuit model shown in Fig. 3-5 with only the noise sources added.

Please note that the parasitic capacitances associated with the differential pair are ignored for sake of simplicity.

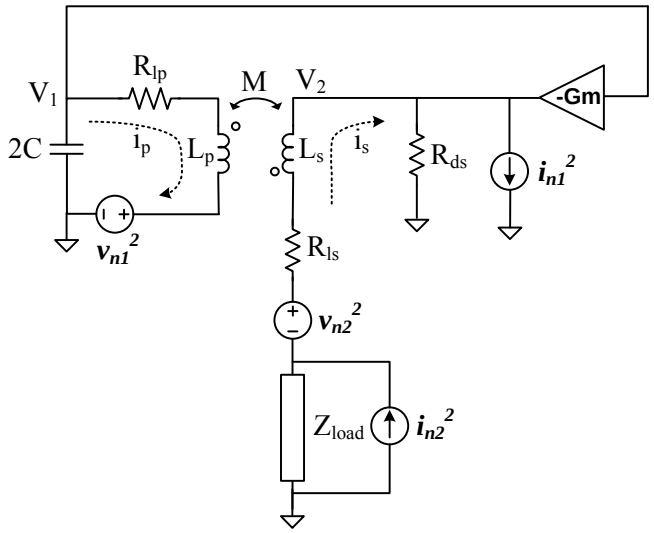


Fig. 3-10 An LTI Model of the proposed LO with all the noise sources

a) Noise contribution of v_{n1}

The noise transfer function from the noise source v_{n1} to V_1 can be calculated as:

$$V_1 = -V_1 s2C \cdot \left(R_{lp} + sL_p\right) + V_1 g_m \cdot sM + v_{n1}$$

$$\Rightarrow T^2_{n,R_{lp}}(s) \doteq \frac{V^2_{n,1}}{v^2_{n1}} = \left(\frac{1}{1+s\left(2CR_{lp}-Mg_m\right)+s^2 2CL_p}\right)^2 \quad (3\text{-}21)$$

The inverse of the noise transfer function is defined as:

$$H_{n,R_{lp}}(s) \doteq \frac{1}{T_{n,R_{lp}}} = 1 + s\left(2CR_{lp} - Mg_m\right) + s^2 2CL_p \quad (3\text{-}22)$$

At the frequency close to oscillation frequency, $\omega = \Delta\omega + \omega_o$,

$$H_{n,R_{lp}}(j\omega) = H_{n,R_{lp}}(j\omega_o) + \Delta\omega \cdot \left.\frac{dH_{n,R_{lp}}}{d\omega}\right|_{\omega=\omega_o}$$

$$= -\Delta\omega \cdot 2\omega_o 2CL_p = -2\frac{\Delta\omega}{\omega_o} \quad (3\text{-}23)$$

Then the noise power at the VCO output can be written as:

$$V^2_{n,o}(\Delta\omega) = 4kT(2R_{lp}) \cdot \left(\frac{\omega_o}{2\Delta\omega}\right)^2 \quad (3\text{-}24)$$

where k is Boltzmann constant, T the temperature and $\Delta\omega$ the offset frequency from ω_o. The noise can be decomposed equally into an amplitude-modulation (AM) component and a phase-modulation (PM) component. The AM component is removed by the

amplitude limiting mechanism of the oscillator. Thus the phase noise, defined as the noise power to the carrier signal power ratio, can be calculated as

$$L(\Delta\omega) = \frac{V_{n,o}^2(\Delta\omega)/2}{V_{VCO}^2/_2} = \frac{2}{V_{VCO}^2} kTR_{lp}\left(\frac{\omega_o}{\Delta\omega}\right)^2 \tag{3-25}$$

As Q_p increases, R_{lp} decreases and V_{VCO} increases. Therefore, to reduce the noise contribution of the resonant tank, we should maximize Q_p. Also, if M is chosen to be M_{opt}, V_{VCO} can be maximized. Therefore, in order to reduce the noise contribution of the resonant tank, we should maximize Q_p and use a mutual inductance close to M_{opt} when designing a transformer.

b) Noise contribution of i_{n1}

The noise transfer function from the noise source i_{n1} to V_1 can be calculated as:

$$\begin{cases} V_1 = -V_1 s2C \cdot (R_{lp} + sL_p) + sM \cdot \left(V_1 g_m + i_{n1} + \frac{V_2}{R_{ds}}\right) \\ V_2 = -(R_{ls} + Z_{load} + sL_s) \cdot \left(V_1 g_m + i_{n1} + \frac{V_2}{R_{ds}}\right) + V_1 s2C \cdot sM \end{cases}$$

$$\Rightarrow T_{n,g_m}^2(s) \doteq \frac{V_{n,1}^2}{i_{n1}^2} \approx \left(\frac{sM}{1+s(2CR_{lp}-Mg_m)+s^2 2CL_p}\right)^2 \tag{3-26}$$

The inverse of the noise transfer function is defined as:

$$H_{n,g_m}(s) \doteq \frac{1}{T_{n,g_m}} = \frac{1}{sM} + \frac{2CR_{lp}-Mg_m}{M} + \frac{s2CL_p}{M} \tag{3-27}$$

At the frequency close to oscillation frequency,

$$H_{n,g_m}(j\omega) = H_{n,g_m}(j\omega_o) + \Delta\omega \cdot \left.\frac{dH_{n,g_m}}{d\omega}\right|_{\omega=\omega_o}$$

$$= \Delta\omega \cdot 2j\frac{2CL_p}{M} = \frac{\Delta\omega}{\omega_o} \cdot 2j\frac{1}{\omega_o M} \tag{3-28}$$

Then the noise power at the VCO output can be written as:

$$V_{n,o}^2(\Delta\omega) = 4kT(2g_m)\gamma \cdot \left(\frac{\omega_o^2 M}{2\Delta\omega}\right)^2 = \frac{2kT\gamma\omega_o M}{Q_p} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \tag{3-29}$$

where γ represents the noise coefficient of an NMOS transistor [3-10]. Then the phase noise due to the differential pair can be expressed as:

$$L(\Delta\omega) = \frac{V_{n,o}^2(\Delta\omega)/2}{V_{VCO}^2/_2} = \frac{2kT\omega_o M\gamma}{V_{VCO}^2 Q_p} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \tag{3-30}$$

Substituting (3-17) and (3-18) into (3-30), the phase noise $L(\Delta\omega)$ can be rewritten as a function of M. And it is minimum when

$$M = L_p\sqrt{\frac{|Z_{load}|}{3\omega_o Q_p L_p}} = \frac{M_{opt}}{\sqrt{3}} \approx 0.58M_{opt} \tag{3-31}$$

Equation (3-31) requires the mutual inductance M to be smaller than M_{opt} to minimize the noise contribution of the VCO differential pair.

c) Noise contribution of v_{n2}

The noise transfer function from the noise source v_{n2} to V_1 can be calculated as:

$$\begin{cases} V_1 = -V_1 \cdot s2C \cdot \left(R_{lp} + sL_p\right) + sM \cdot \left(\frac{V_2}{R_{ds}} + V_1 g_m\right) \\ V_2 = -(R_{ls} + Z_{load} + sL_s) \cdot \left(\frac{V_2}{R_{ds}} + V_1 g_m\right) + V_1 s2C \cdot sM + v_{n2} \end{cases}$$

$$\Rightarrow T^2_{n,R_{ls}}(s) \doteq \frac{V^2_{n,1}}{v^2_{n2}}$$

$$= \left(\frac{1}{\frac{\left(1+s2CR_{lp}+s^2 2CL_p\right)(Z_{load}+R_{ds}+R_{ls}+sL_s)}{sM} - g_m R_{ds} - s^2 2CM}\right)^2 \tag{3-32}$$

The inverse of the noise transfer function is defined as:

$$H_{n,R_{ls}}(s) \doteq \frac{1}{T_{n,R_{ls}}}$$

$$= \frac{\left(1+s2CR_{lp}+s^2 2CL_p\right)(Z_{load}+R_{ds}+R_{ls}+sL_s)}{sM} - g_m R_{ds} - s^2 2CM \tag{3-33}$$

At the frequency close to oscillation frequency,

$$H_{n,R_{ls}}(j\omega) = H_{n,R_{ls}}(j\omega_o) + \Delta\omega \cdot \left.\frac{dH_{n,R_{ls}}}{d\omega}\right|_{\omega=\omega_o}$$

$$\approx \frac{M}{L_p} + g_m(Z_{load} + R_{ls} + j\omega_o L_s) + \Delta\omega \cdot j\frac{4CL_p R_{ds}}{M} \tag{3-34}$$

Comparing to the equation (3-23), we can see that

$$\left|H_{n,R_{ls}}(j\omega)\right| \gg \left|H_{n,R_{lp}}(j\omega)\right| \tag{3-35}$$

Therefore, the noise contribution of v_{n2} is negligible.

d) Noise contribution of i_{n2}

Similarly, the inverse of the noise transfer function from noise source i_{n2} to V_1 is

$$\left|H_{n,Z_{load}}(j\omega)\right| \gg \left|H_{n,g_m}(j\omega)\right| \tag{3-36}$$

So the noise contribution of i_{n2} can also be ignored. Intuitively, since the divide-by-two does not load the resonant tank directly for the proposed LO, the noise contribution of the divider to the VCO is insignificant as compared to those of the resonator and the VCO differential pair.

The VCO phase noise considering all the noise sources can be written as:

$$L(\Delta\omega) = \left(\frac{2}{V_{VCO}^2} kTR_{lp} + \frac{2kT\omega_o M\gamma}{V_{VCO}^2 Q_p}\right) \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \quad (3\text{-}37)$$

(3-37) indicates that to minimize the VCO phase noise, one should generally maximize the Q of the primary inductor, increase the VCO swing and reduce the mutual inductance.

3.3.2. An LTV Model based Phase Noise Analysis

Among the different LTV methodologies, a phasor-based approach is adopted to analyze the proposed LO with an emphasis on the thermally induced noise, as it relies more on the circuit analysis and physical noise mechanism.

A noise spectrum of an oscillator can be approximately represented by a large number of sinusoidals whose frequencies are distributed over the range of interest and whose phase is random. Consider a pair of sidebands at a particular offset frequency of ω_m around a large carrier as shown in Fig. 3-11. If the sum of the sidebands is orthogonal to the carrier, then the phase modulation (PM) occurs. Alternatively, if the sum is co-linear at all times with the carrier, the amplitude modulation (AM) results. A single-side band (SSB) noise around the carrier can always be decomposed into equal PM and AM sidebands, which is shown in Fig. 3-12.

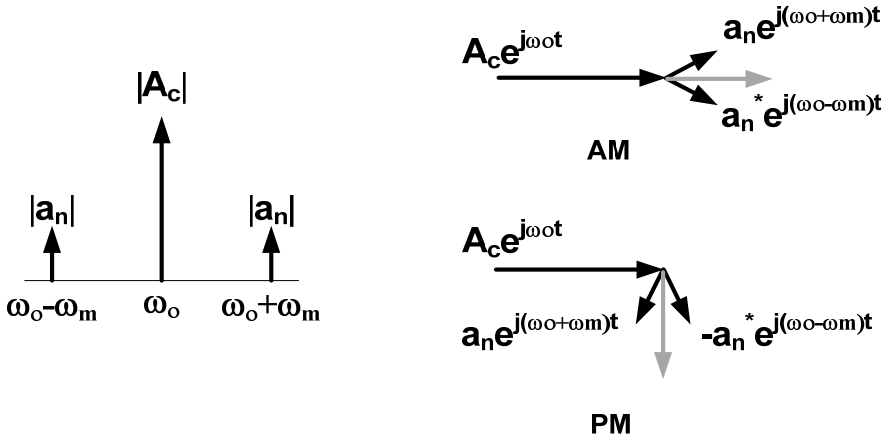


Fig. 3-11 Amplitude modulation (AM) and phase modulation (PM) sidebands

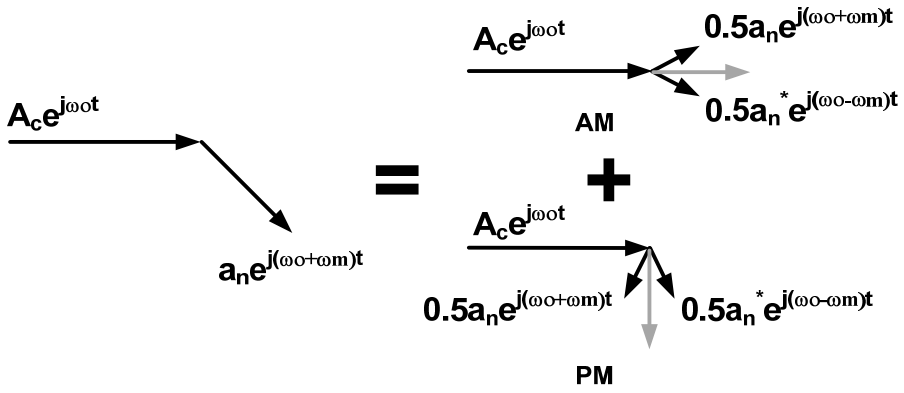


Fig. 3-12 A single sideband decomposed into AM and PM sidebands

In the phasor-based approach, it is assumed that there is a steady-state solution to the circuit that consists of a fundamental tone and a series of sideband noise tones with unknown coefficients. The coefficients can be determined using circuit equations in steady state. Once the coefficients are known, the phase noise can be calculated easily.

a) Noise contribution of the resonant tank

As shown in Fig. 3-13, the resonant tank can be modeled as a capacitor in parallel with a lossy inductor and a voltage source representing the induced voltage $V_{ind}(t)$.

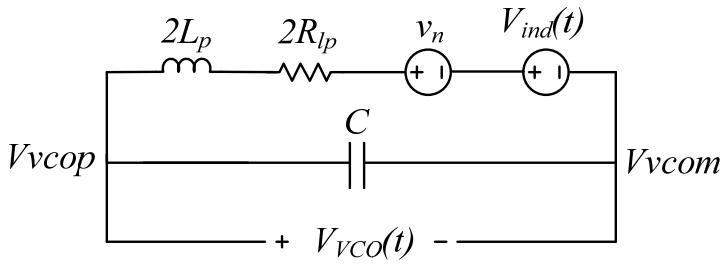


Fig. 3-13 A lossy resonant tank model

It is assume that in the steady state the differential voltage across the resonant tank is:

$$V_{VCO}(t) = V_{VCO}e^{j\omega_o t} + \left(ae^{j\omega_+ t} - a^* e^{j\omega_- t}\right) + \left(be^{j\omega_+ t} + b^* e^{j\omega_- t}\right) \quad (3\text{-}38)$$

where a and b are the unknown coefficients of PM and AM sidebands, located at $\omega_+ = \omega_o + \Delta\omega$, $\omega_- = \omega_o - \Delta\omega$, and $\Delta\omega$ is the offset frequency. Note that a^* (b^*) denotes the complex conjugate of a (b). The differential pair of the VCO converts the VCO output voltage to the drain current, which induces a voltage on the primary coil through the magnetic coupling. It has been proved in [3-9] that the input PM carrier-to-sidebands

ratio is preserved at the output of a memory-less narrow-band nonlinear circuit, and the output does not contain AM. So the induced voltage for the resonant tank can be written as

$$V_{ind}(t) = V_{ind}\left[e^{j\omega_o t} + \frac{1}{V_{VCO}}\left(ae^{j\omega_+ t} - a^* e^{j\omega_- t}\right)\right] \tag{3-39}$$

At ω_o:

$$V_{VCO} = \frac{V_{ind}}{2R_{lp}+j\omega_o 2L_p+{}^{1}/_{j\omega_o C}}\frac{1}{j\omega_o C} = \frac{V_{ind}Q_p}{j} \tag{3-40}$$

At ω_+:

$$a + b = \left(a\frac{j}{Q_p} + v_n\right)\frac{{}^{1}/_{j\omega_+ C}}{2R_{lp}+j\omega_+ 2L_p+{}^{1}/_{j\omega_+ C}} \tag{3-41}$$

where v_n is the noise voltage of R_{lp} that models the loss of the resonant tank. In this analysis, a single component of the noise voltage located at ω_+ is assumed.

At ω_-:

$$-a^* + b^* = -a^*\frac{j}{Q_p}\frac{{}^{1}/_{j\omega_- C}}{2R_{lp}+j\omega_- 2L_p+{}^{1}/_{j\omega_- C}}$$

$$\Rightarrow -a + b = -a\frac{j}{Q_p}\frac{{}^{1}/_{j\omega_- C}}{2R_{lp}-j\omega_- 2L_p-{}^{1}/_{\omega_- C}} \tag{3-42}$$

Subtracting (3-42) from (3-41)

$$2a = \left(a\frac{j}{Q_p} + v_n\right)\frac{1}{(2R_{lp}+j\omega_+ 2L_p)j\omega_+ C+1} + a\frac{j}{Q_p}\frac{1}{(2R_{lp}-j\omega_- 2L_p)j\omega_- C-1} \tag{3-43}$$

With some approximation,

$$a = v_n\frac{\omega_o}{4\Delta\omega} \tag{3-44}$$

Then the phase noise due to the resonator loss is

$$L(\Delta\omega) = \frac{2a^2}{{}^{V_{VCO}^2}/_2} = \frac{2}{V_{VCO}^2}kTR_{lp}\left(\frac{\omega_o}{\Delta\omega}\right)^2 \tag{3-45}$$

Note that (3-45) is the same as (3-25). Since no frequency translation occurs and the noise of the resistor is white noise, it is expected that the two different approaches would yield the same results.

b) Noise contribution of the VCO differential pair

In the steady state, the VCO differential pair can operate in all possible regions (cutoff, saturation and triode regions). We consider the noise contribution only in the saturation region. For simplicity, the time-varying transconductance of the differential pair is modeled as a series of pulses with a pulse width equal to the duration t_W in the saturation region and an interval of $1/2f_o$ as shown in Fig. 3-14 (a). The spectrum of the transconductance is approximated as a series of pulses at DC and even harmonics of the oscillation frequency with constant amplitude up to $1/t_w$, as shown in Fig. 3-14 (b).

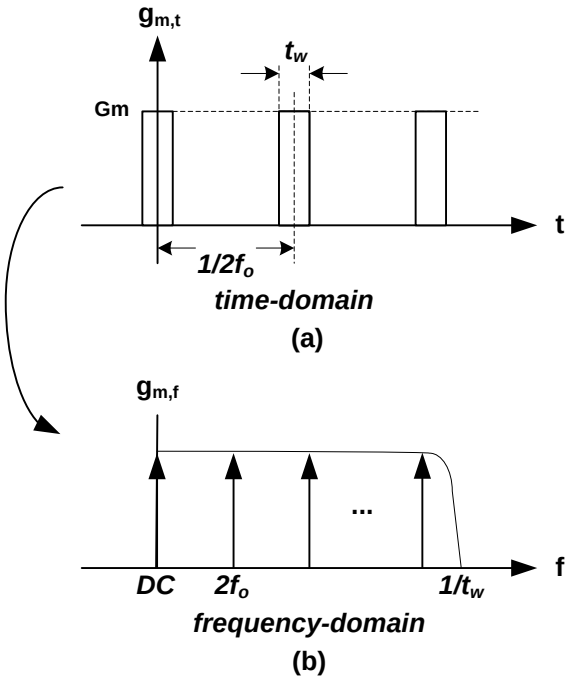


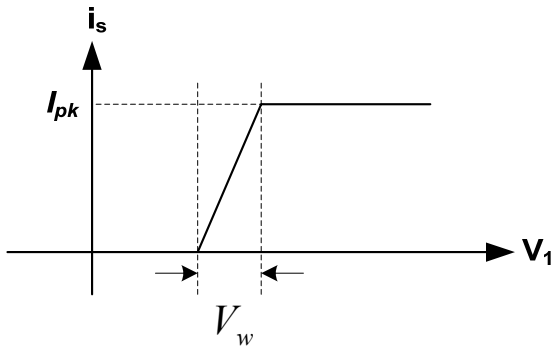
Fig. 3-14 Approximate time-domain and frequency-domain waveforms of the transconductance of the differential pair

We assume that the tranconductance of the VCO differential pair in the saturation region is constant, as shown in Fig. 3-15, where V_w is the gate voltage change during t_w. Then the constant transconductance G_m can be estimated as

$$G_m = \frac{di_s}{dV_1} = \frac{I_{pk}}{V_w} = \frac{I_{pk}}{t_w(V_{VCO}/2)\omega_o} = \frac{2I_{pk}}{V_{VCO}\omega_o t_w} \tag{3-46}$$

From Fig. 3-14 (a), the DC value of the transconductance is obtained as:

$$g_{m,DC} = G_m \frac{t_w}{1/2f_o} \tag{3-47}$$



Assume: $V_1 = \frac{V_{VCO}}{2}\sin(\omega_o t)$

$$\frac{V_w}{t_w} = \left.\frac{dV_1}{dt}\right|_{t=0} = \frac{V_{VCO}}{2}\omega_o \cos(\omega_o t)\Big|_{t=0} = \frac{V_{VCO}}{2}\omega_o$$

Fig. 3-15 Constant Gm in the saturation region

Then all the frequency domain impulses have an amplitude of $g_{m,DC}$. Since the noise current of the differential pair is a multiplication of the noise voltage at the gate and the transconductance, convolution of the white thermal noise of the transistor and the frequency domain impulses of the transconductance produces the noise current spectrum, which is shown in Fig. 3-16. The noise current can be calculated as the sum of the square of the frequency domain envelope times the thermal noise voltage:

$$i_{s,n}^2 = v_n^2 g_{m,DC}^2 N_{pulse} N_{dev} = \frac{4kT\gamma}{G_m} \cdot g_{m,DC}^2 \cdot \frac{1/t_w}{2f_o} \cdot 2 = 16kT\gamma \frac{I_{pk}}{\pi V_{VCO}} \tag{3-48}$$

where N_{pulse} is the number of the pulses, N_{dev} the number of the devices and γ the channel noise coefficient of an NMOS transistor. The noise current is seen by the resonant tank through the magnetic coupling. The induced noise voltage is

$$v_{gm,n}^2 = 2{i_{s,n}}^2 \cdot (\omega_o M)^2 \tag{3-49}$$

Referring to (3-44) and (3-45), we can calculate the phase noise contributed by the differential pair as

$$L(\Delta\omega) = \frac{4v_{gm,n}^2}{V_{VCO}^2}\left(\frac{\omega_o}{4\Delta\omega}\right)^2 = \frac{8kT\gamma I_{pk}}{\pi V_{VCO}^3}\left(\frac{\omega_o^2 M}{\Delta\omega}\right)^2 \tag{3-50}$$

Substituting (3-17) and (3-18) into (3-50) results in

$$L(\Delta\omega) = \frac{2kT\gamma\omega_o M}{Q_p V_{VCO}^2} \cdot \left(\frac{\omega_o}{\Delta\omega}\right)^2 \tag{3-51}$$

Again, (3-51) is the same as (3-30). So we would expect that the optimum mutual inductance for the minimum phase noise contribution of the differential pair is about $0.58M_{opt}$. It is interesting that the time-variant model gives the same result as the time-invariant model. As a matter of fact, the assumptions made in the time-variant model make this happen.

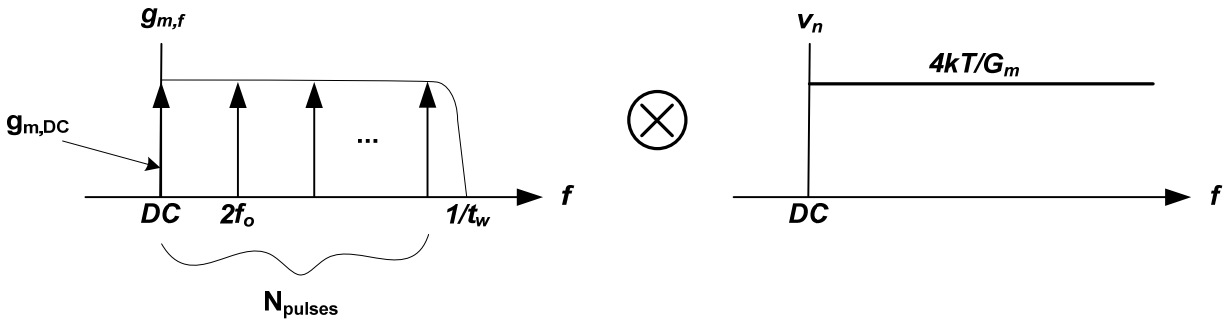


Fig. 3-16 Calculation of the noise current of the differential pair

c) Noise contribution of the divider

The divider noise is mostly coupled to the resonant tank when the differential pair of the VCO is in the deep triode region. Switching of the differential pair translates the noise of the divider into the sidebands around the carrier through mixing process, which results in the phase noise of the VCO, as shown in Fig. 3-17. Specifically, the noise around DC is mixed up into the AM sidebands around the carrier, and hence has no impact. Instead the noise at all the even harmonics can be translated into the PM sidebands around the fundamental tone.

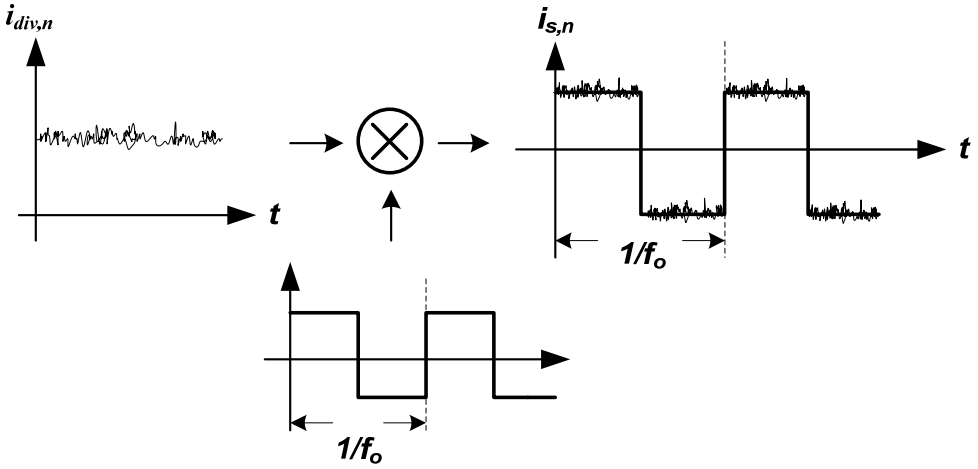


Fig. 3-17 The divider noise current mixed with a square wave

Assume that the noise current source caused by the divider around the second harmonic is $i_{div,n}sin(2\omega_o+\Delta\omega)t$, then the noise current after mixing with a square-wave is

$$i_{s,n} = i_{div,n}\sin(2\omega_o + \Delta\omega)t \cdot \frac{2}{\pi}\left(\sin\omega_o t + \frac{1}{3}\sin 3\omega_o t + \cdots\right)$$

$$= \frac{i_{div,n}}{\pi}\left[\cos(\omega_o + \Delta\omega)t + \frac{1}{3}\cos(\omega_o - \Delta\omega)t + \cdots\right]$$

$$= \frac{i_{div,n}}{\pi}\left\{\frac{2}{3}[\cos(\omega_o + \Delta\omega)t + \cos(\omega_o - \Delta\omega)t] + \frac{1}{3}[\cos(\omega_o + \Delta\omega)t - \cos(\omega_o - \Delta\omega)t] + \cdots\right\} \quad (3\text{-}52)$$

where $cos(\omega_o+\Delta\omega)t+cos(\omega_o-\Delta\omega)t$ are the PM sidebands, modulating the phase of the signal tone $sin\omega_o t$, and $cos(\omega_o+\Delta\omega)t-cos(\omega_o-\Delta\omega)t$ are the AM sidebands, modulating the amplitude of the signal tone. The total noise current power is a sum of the noise current power at all the even harmonics. Then the phase noise contributed by the divider is

$$L(\Delta\omega) = \frac{i_{div,n}^2}{4}\left(\frac{\omega_o M}{V_{VCO}}\right)^2\left(\frac{\omega_o}{2\Delta\omega}\right)^2 = \frac{kTA}{R_{div}}\left(\frac{\omega_o M}{V_{VCO}}\right)^2\left(\frac{\omega_o}{2\Delta\omega}\right)^2 \quad (3\text{-}53)$$

where R_{div} is an equivalent resistance of the divider seen by the secondary coils, and A is a noise factor of the divider. Generally, a smaller mutual inductance is more favorable to reduce the phase noise contributed by the divider.

The total phase noise is the sum of individual noises given in (3-45), (3-50) and (3-53), and is as follows.

$$L(\Delta\omega) = \left(\frac{2kTR_{lp}}{V_{VCO}^2} + \frac{8kT\gamma I_{pk}\omega_o^2 M^2}{\pi V_{VCO}^3} + \frac{kTA\omega_o^2 M^2}{4R_{div}V_{VCO}^2}\right)\left(\frac{\omega_o}{\Delta\omega}\right)^2 \quad (3\text{-}54)$$

Comparing (3-37) and (3-54), we can see that the noise due to the divide-by-two cannot be captured properly in the LTI model. However, both of the two approaches point out that the transformer of the proposed LO should have a high quality factor Q_p and a relatively low mutual inductance M to lower the total phase noise. Therefore, the LTI based approach has limited power in predicting the phase noise even though it does provide some important design insights.

In the above analysis, we ignore the flicker noise, which generally dominates the close-in phase noise of the VCO. The mechanisms of the flicker noise up-conversion include the frequency modulation of the harmonic content of the current flowing into the differential pair [3-10] and the AM-to-FM conversion through the varactor and the junction capacitors associated with the transistors[3-12].

Now, let's revisit (3-1), the induced voltage $i_s \cdot j\omega M$ produces the current circulating in the resonant tank. It is assumed that the current i_s is close to a square wave, so rich in harmonics. For simplicity, we ignore all the high-order harmonics and only consider the harmonic contents at f_o and $3f_o$. The gate voltage $V_1(t)$ to the induced voltage $V_{ind}(t)$ gain can be calculated as

$$\left.\frac{V_1(t)}{V_{ind}(t)}\right|_{f=f_o} = \frac{1/s2C}{\frac{1}{s2C}+sL_p+R_p} = \frac{1}{s2CR_p} = \frac{Q_p}{j} \tag{3-55}$$

$$\left.\frac{V_1(t)}{V_{ind}(t)}\right|_{f=3f_o} = \frac{1/s2C}{\frac{1}{s2C}+sL_p+R_p} = \frac{1}{1-9+j3/Q_p} \approx -\frac{1}{8} \tag{3-56}$$

Then the gate voltage at the differential pair can be written as:

$$V_1(t) = \frac{2}{\pi}\mathrm{I_{pk}}\omega\mathrm{MQ_p}\cos(\omega t) + \frac{2}{3\pi}\mathrm{I_{pk}}3\omega\mathrm{M}\frac{1}{8}\sin(3\omega\mathrm{t}) \tag{3-57}$$

We can see that even though the harmonic voltage is much smaller than the fundamental tone, the two voltages are not in-phase but in quadrature. As a result, the zero crossings of the fundamental tone are shifted due to the harmonics, as shown in Fig. 3-18. If the harmonic level is modulated by the noise, it will cause frequency modulation (FM) that is one of the flicker induced phase noise sources.

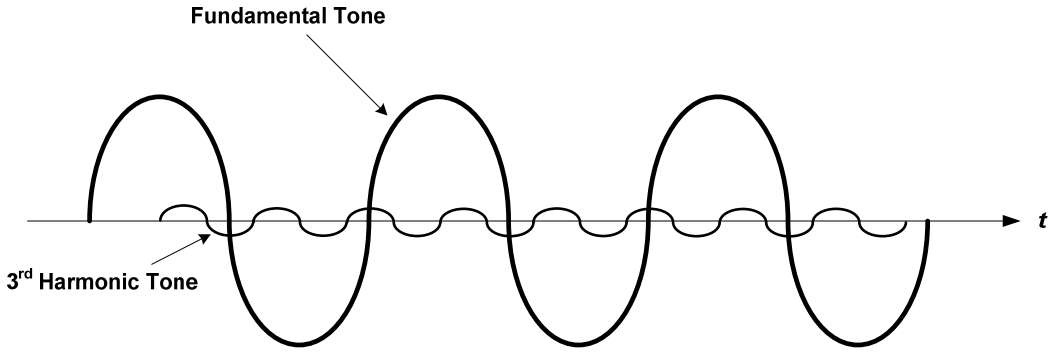


Fig. 3-18 Calculation of the noise current of the differential pair

This frequency modulation behavior due to the harmonics can be modeled as an equivalent capacitor added in parallel to the resonant tank. The capacitance value is a function of the harmonic level normalized to the fundamental.

Nonlinearity of the varactor C-V characteristics is another source of the flicker induced phase noise. The effective capacitance in the resonant tank is expressed as: $C_{eff} = C_o - 0.5C_2$, where C_o is the timing average total capacitance and C_2 the second order Fourier coefficient of the nonlinear varactor [3-12]. The effective capacitance depends on the bias voltage of the varactor as well as the VCO amplitude, and hence any perturbation on the VCO amplitude due to the noise can cause the fluctuation on C_{eff} and on the oscillation frequency. This process is so-called AM-to-PM conversion. Therefore, a linear tuning curve is highly desirable for minimizing the low-frequency flicker noise converted to the in-band phase noise.

For the conventional NMOS-only VCO, the varactor has one side connected to the power supply. In the presence of the varactor nonlinearity, the low frequency fluctuation on the supply line can modulate the effective capacitance, and hence degrades the phase noise. However, for the proposed transformer-based VCO, the varactor is biased at a voltage normally generated from a bandgap reference. Therefore, it is more immune to the supply noise.

3.4. Transformer Design Guidelines

Design of a transformer is not trivial as there are many parameters involved. But most of the strategies that have been used for on-chip inductor optimization can also be applied to the transformer. Here are a few guidelines for the transformer design based on the equations derived in the previous section:

1. Primary inductance. It is mainly determined by the oscillation frequency and the tuning range. In general, it should be maximized for low-power applications [3-14].
2. Quality factor of the primary inductor. It should be maximized for a high start-up gain, low power consumption, and low phase noise.
3. Secondary inductance. It is determined by the target mutual inductance.
4. Quality factor of the secondary inductor. It does not matter unless extremely low. As a rule of thumb, the series equivalent resistance of the secondary coil should be smaller than $Z_{load}/10$ for not affecting the voltage headroom.
5. Mutual inductance. It depends on the design objective. If low power (noise) is the primary objective, a relatively high (low) mutual inductance is desirable.
6. Magnetic coupling between the primary and the secondary coils. It is determined by the target mutual inductance.
7. Magnetic coupling between two secondary coils. It usually does not affect the performance and could be either positive or negative depending on the layout.

8. Capacitive coupling between the primary and the secondary coils. It impairs the isolation between the VCO and the divider, and causes the noise coupled to the resonant tank. Thus, it should be minimized.
9. Layout symmetry. A center tap is required to deliver the bias voltage to the resonant tank. A perfectly symmetric layout around the center-tap line is important for a differential VCO.

In order to verify the validity of the equations, we have performed parametric simulations to check the impact of *M* on the start-up time, the LO current consumption, the VCO swing, and the LO phase noise. The start-up time is defined as the time for the VCO to reach from zero to 90 percent of the full swing, as shown in Fig. 3-19.

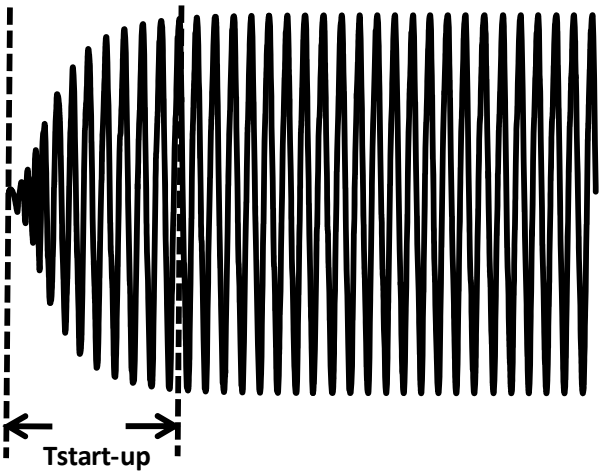


Fig. 3-19 Definition of the start-up time

The simulation results are given in Fig. 3-20 through Fig. 3-23. Fig. 3-20 shows that a larger mutual inductance results in a shorter start-up time, which matches with the prediction in (3-9).

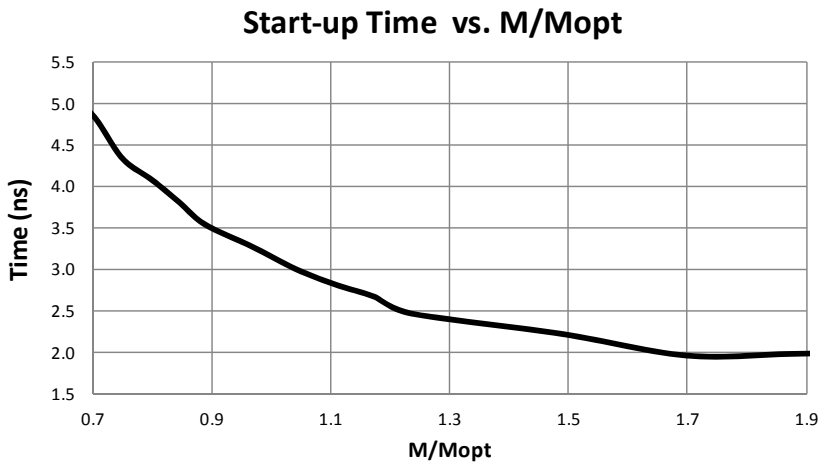


Fig. 3-20 Start-up time versus M/M_{opt}

Fig. 3-21 confirms (3-17), which predicts that a larger mutual inductance leads to a lower current. (14) gives the fundamental spectrum of the current, which matches reasonably well with the average current.

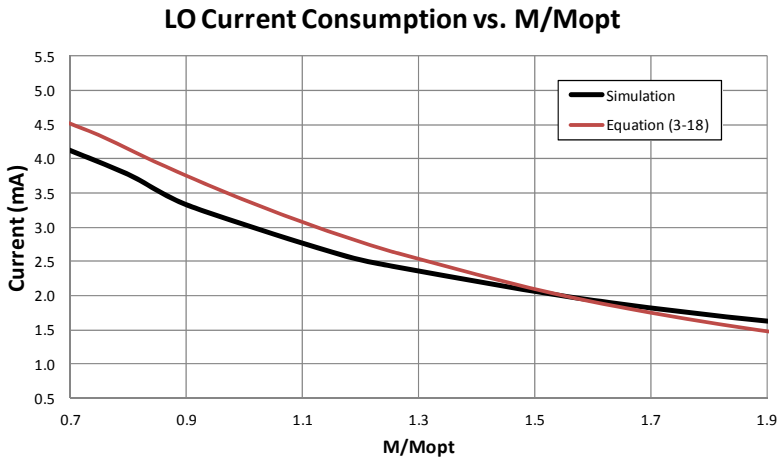


Fig. 3-21 LO current versus M/M_{opt}

Fig. 3-22 indicates that the VCO swing is maximum at $M/M_{opt} \approx 1$, as predicted in (3-19) and (3-20). The discrepancy between the simulation and the analytical results becomes larger for larger M/M_{opt}, as the parasitics ignored in the analysis become more significant.

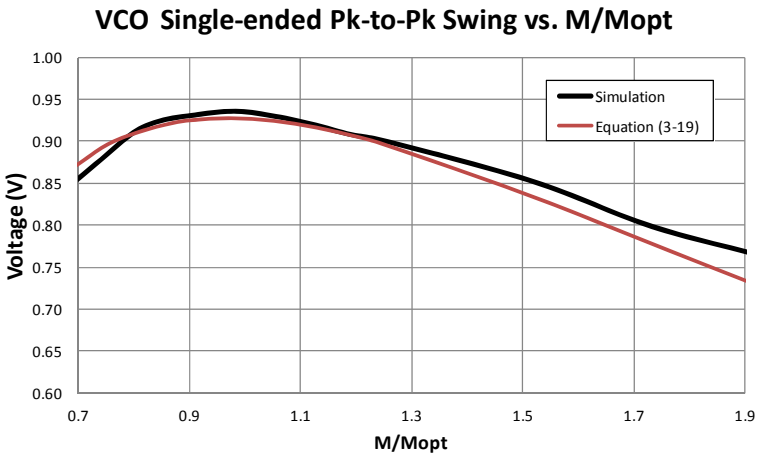


Fig. 3-22 VCO swing versus M/M_{opt}

Fig. 3-23 shows the LO phase noise with respect to M/M_{opt}. According to (3-54), the first term is minimum at $M/M_{opt} \approx 1$, and the second term is minimum at $M/M_{opt} \approx 0.58$. The resonant tank and the differential pair are the dominant noise contributors for small M in the particular design, and hence the minimum phase noise is achieved for M/M_{opt} in between 0.58 and 1. Fig. 3-23 shows the value is about 0.75.

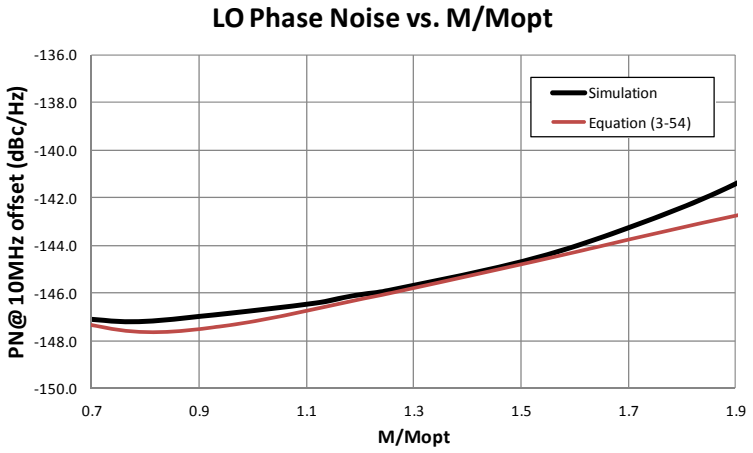
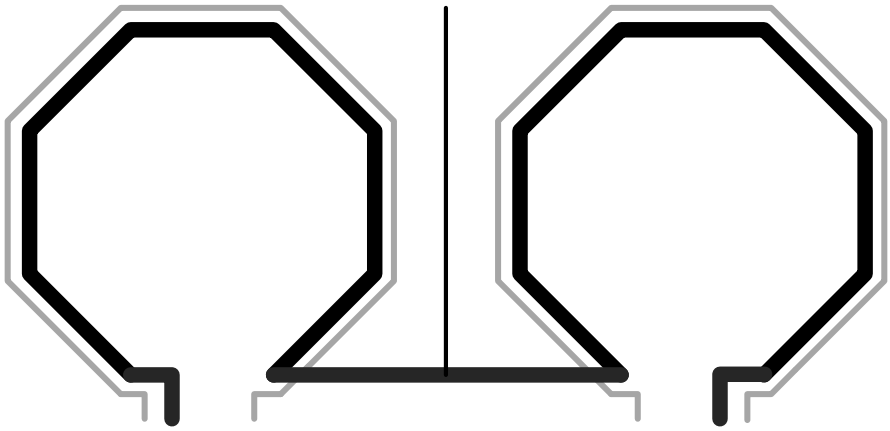


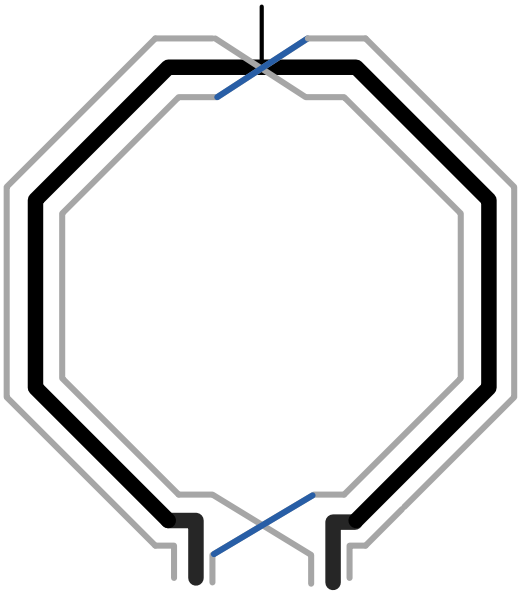
Fig. 3-23 LO phase noise versus M/M_{opt}

There are two possible transformer configurations suitable for the proposed LO as shown in Fig. 3-24. Configuration I has two identical single-ended transformers placed side-by-side. The two primary coils are connected in series at the center. Since the magnetic fields generated by the primary coils try to cancel each other, a certain distance

between two cores is required to minimize the effect. Configuration II is a single-core structure having one differential primary coil coupled with two secondary coils closely. Each configuration has its advantages and disadvantages. Configuration I leads to a simpler layout than Configuration II, but a larger area due to use of two cores. The layout for Configuration II could be complicated, if a large number of turns is needed for higher mutual inductance. However, it is compact. More importantly, it can achieve higher Q for the primary coil owing to enhanced magnetic coupling.



Configuration I: Dual-Core



Configuration II: Single-Core

Fig. 3-24 Possible transformer configurations

3.5. Summary

In this chapter, a low-power low-voltage quadrature signal generation circuit of stacking a transformer-based VCO and a CML divide-by-two is presented. The operation theories of the proposed LO are analyzed comprehensively based on a linearized small-signal model. Both the LTI and the LTV models are exploited to quantify the VCO phase noise. The validity of theoretical analysis is then verified through the simulations. The mathematical equations offer important insights for design optimization of the proposed LO. The mutual inductance between the primary and the secondary coils of the transformer turns out to be one of the key parameters. In general, the higher the mutual inductance, the lower the power, but also the worse the phase noise performance. The quality factor of the primary inductance should always be maximized. Beyond the low-power feature, the proposed LO also has inherently lower power supply sensitivity compared to the conventional LO. Finally, the design guidelines and layout choices of the transformer are summarized.

Chapter 4 Circuit Implementation and Measurement Results

The quadrature LO proposed in Chapter 3 was designed and fabricated in TSMC CMOS 65 nm technology for a global positioning system (GPS) receiver. As one of the key building blocks in the frequency synthesizer, the quadrature LO drives the mixers as well as the prescaler on the feedback path of the synthesizer. All the practical aspects have been considered in the LO design.

This chapter reviews the design specifications and describes the topology selections and the circuit implementations of the proposed VCO transformer, the switchable capacitor bank, the frequency-drift temperature compensation, the peak detector, the voltage regulator and the LO buffers in great details. Then various measurements results, including the LO phase noise and its variations over supply, process and temperature, the frequency tuning range, the reference spur are provided with some explanations. Finally, the performance of the proposed LO is compared against the recently published LOs using the well-known FoM and FoM_T [4-1].

4.1. Design Specifications

The proposed low-power quadrature LO generation circuitry is intended to be used in a GPS receiver that operates concurrently with the cellular transceivers due to the mandatory support of E911 (Enhanced 911) service in wireless handsets [4-2]. To maximize the power efficiency, the GPS receiver operates either in a high-linearity mode or in a low-linearity mode depending on the detected transmitting power level. Therefore, the LO also needs to be designed to support both operation modes. In the high linearity mode, the phase noise requirement of the LO is very stringent due to the strong jammer, while the power consumption should be minimized in the low linearity mode. Table 4-1 summarizes the design specifications of the quadrature LO.

Table 4-1 Quadrature LO Design Specifications

Parameter	Specification
Technology	TSMC CMOS 65 nm
Power Supply	External: 1.2 V; Internal: 1V (at voltage regulator output)
Frequency Tuning Range	1567 MHz – 1590 MHz
LO Phases	Q leads I by 90 degree
Integrated Phase Noise (from 1 KHz to 10 MHz)	< -23 dBc
LO Phase Noise @ 96 MHz	< -137 dBc/Hz (Low Linearity Mode) < -154 dBc/Hz (High Linearity Mode)
RSB	< -23 dBc
Power Consumption	As low as possible for low linearity mode

4.2. Quadrature LO Design Implementation

Fig. 4-1 shows a classical type II fractional-N frequency synthesizer consisting of a phase frequency detector (PFD), a charge pump (CP), a low pass filter, a pulse-swallow prescaler, an N counter, a delta-sigma modulator, and a quadrature generation circuit proposed in Chapter 3. The LO buffer drives the mixers as well as the prescaler on the feedback of the synthesizer. The complete quadrature LO generation circuit includes a transformer-based VCO stacked with a divide-by-two, a switchable capacitor bank, a frequency-drift temperature compensation circuit, a peak detector for adaptive gain control, a voltage regulator, and LO buffers.

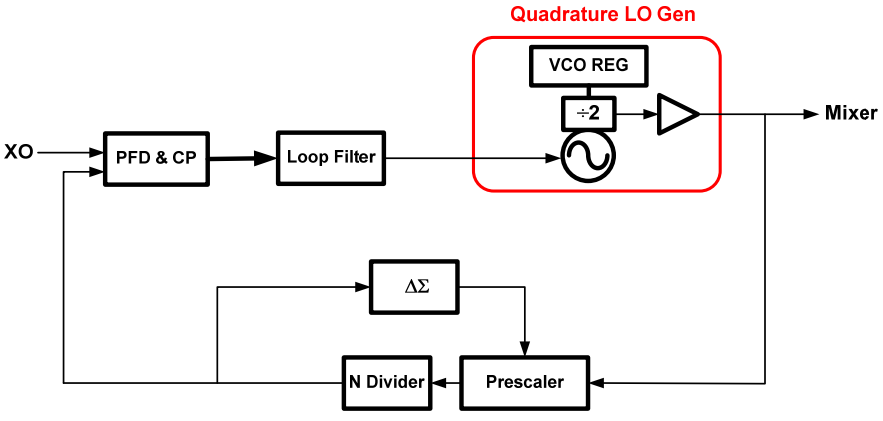


Fig. 4-1 Block diagram of a fractional-N frequency synthesizer

4.2.1. Transformed-Based VCO

The primary design objective of the LO is to reduce the power consumption. The stringent far-offset phase noise specification generally requires large current of the divide-by-two and the following buffers for the conventional LO. The proposed LO is thus very suitable for the target application.

To justify the topology selection, both the conventional LO in Fig. 3-1 and the proposed one in Fig. 3-3 have been designed for the target specifications. A performance comparison based on the schematic-level simulations is shown Table 4-2.

Table 4-2 LO Performance Comparison (Proposed vs. Conventional)

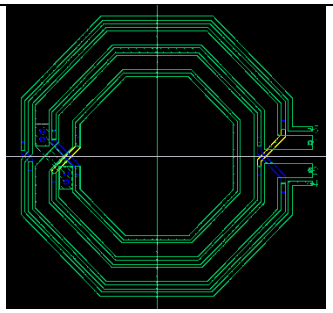
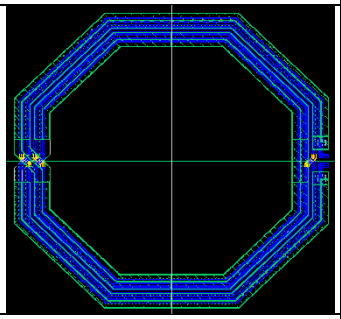
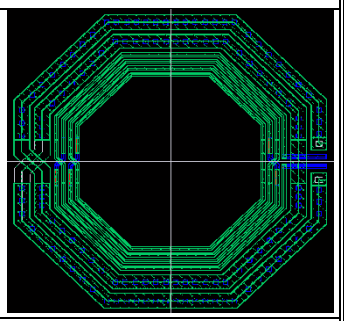
Parameter	Proposed LO	Conventional LO
Transformer/Inductor	L_p: 1.3 nH Q_p: 13.5 L_s: 3.5 nH Q_s: 5 M: 1.5 nH	L: 2.6 nH Q: 15
LO frequency	1.7 GHz	1.7 GHz
Supply Voltage	1 V	1 V
Current Consumption (VCO + Divider)	**1.8 mA**	**2.5 mA**
LO Phase Noise @ 96 MHz offset Frequency (worst case)	-154.2 dBc/Hz	-154.4 dBc/Hz
LO Single-ended Peak-to-peak Swing	1 V	1 V
VCO Start-up Time	2.5 ns	3.5 ns

It can be noticed that the two designs have very similar performance in terms of the operation frequency, the far-offset phase noise, the LO output swing. However, the current consumption of the proposed LO is about 30% lower than that of the conventional LO. Also it has shorter start-up time, or equivalently, larger start-up gain.

The quadrature LO needs to support two operation modes: high linearity (low noise) and low linearity (low power), in one design. The different criteria lead to the different design optimizations and tradeoffs. For low power consumption, a larger mutual inductance M, a larger load impedance Z_{load} of the divide-by-two, a smaller g_m of the VCO differential pair and smaller LO buffers are generally preferable. However, the design choices go in completely opposite direction for low noise. Therefore, the resistive load of the divider, the gate bias of the differential pair, and the LO buffers are all made programmable to accommodate the different scenarios.

As the primary design objective is to lower the power consumption, and the phase noise is of secondary concern, a relatively high mutual inductance with a dual-core configuration is chosen for the transformer-based VCO. Several different transformer structures for a dual-core configuration were designed and compared using PeakView tool from Lorentz Solution. The transformer layouts and their electromagnetic (EM) performances are summarized in Table 4-3.

Table 4-3 Transformer Layout and EM Performance Comparison

	INTERLEAVED	**STACKED**	**TAPPED**
Layout			
L_p **(nH)**	0.98	1.28	1.16
Q_p	15.5	12.4	15.9
L_s **(nH)**	3.94	5.93	4.06
Q_s	5.66	2.27	8.57
k	0.78	0.92	0.55

It can be observed that among the three transformer structures, the stacked one has the highest coupling factor k but lowest Q_p, the tapped one has the highest Q_p but the lowest k, the interleaved structure has the best overall performance and thus is selected in the LO design.

The magnetic coupling between the two transformers' coils are negative for the dual-core configuration, so the magnetic field becomes weaker as the two cores are getting closer to each other. Another study for transformers in dual-core configuration was conducted to evaluate the isolation. The results are shown in Fig. 4-2, where $k_{pp,}$ k_{ss} and $k_{ps,}$ represent the coupling factors between the two primary coils, the two secondary coils, the primary and the secondary coils in different transformers, respectively. It can be seen that in order to keep all the coupling factors less than 0.01, the center-to-center distance between the two transformer cores should be larger than 300 um.

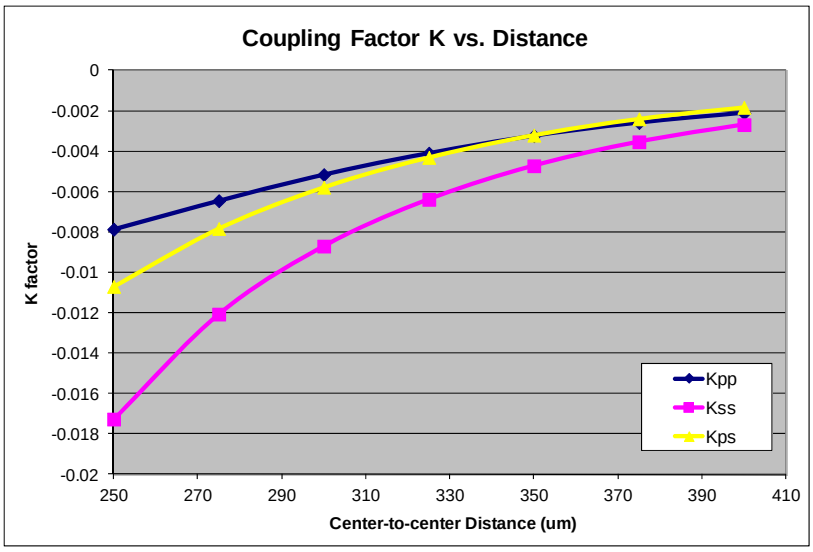


Fig. 4-2 Coupling factors versus center-to-center distance

The final layout of the dual-core transformer is shown in Fig. 4-3. Each transformer core is implemented with a 2-turn primary coil and a 4-turn secondary coil in an interleaved structure. The primary coil uses thick M5 layer with a metal width of 12 um, and the secondary coil uses AP layer with a metal width of 3 um. The overall area is 540 um x 260 um = 0.14 mm^2, and the center-to-center distance is 330 um.

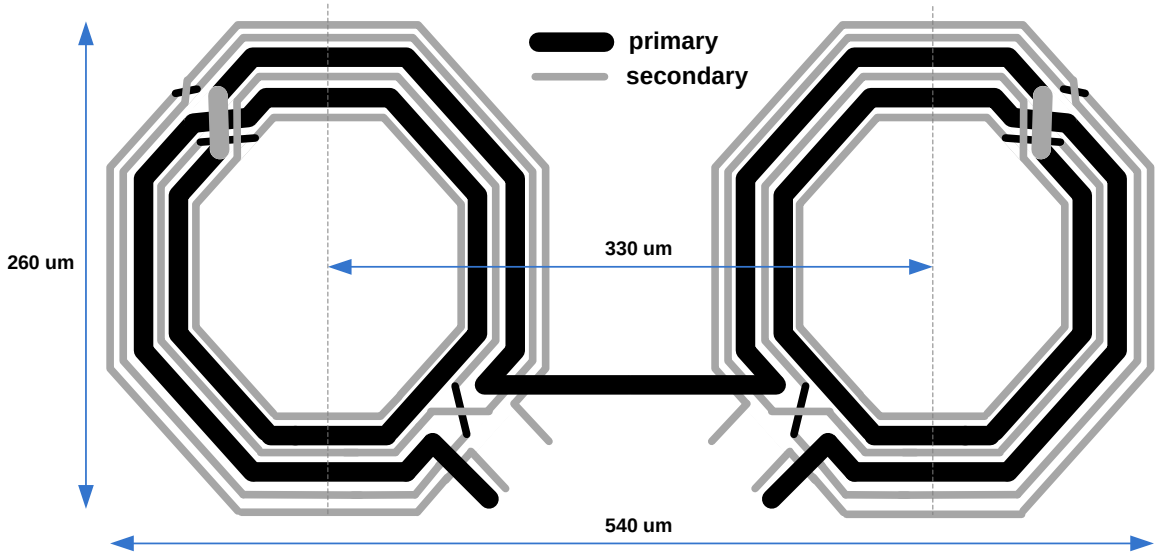


Fig. 4-3 Dual-core transformer layout

The transformer is simulated using Ansoft's 3-D finite element solver HFSS. The key parameters are plotted in Fig. 4-4. At the frequency of around 3.2 GHz, the differential primary inductance (or, the total equivalent inductance of the two primary

coils in series) is 2.6 nH and Q_p is 13.5. The single-ended secondary inductance is 5.2 nH and Q_s is 4.5. The coupling factor between the primary and the secondary coils is 0.76 and the mutual inductance is 1.98 nH.

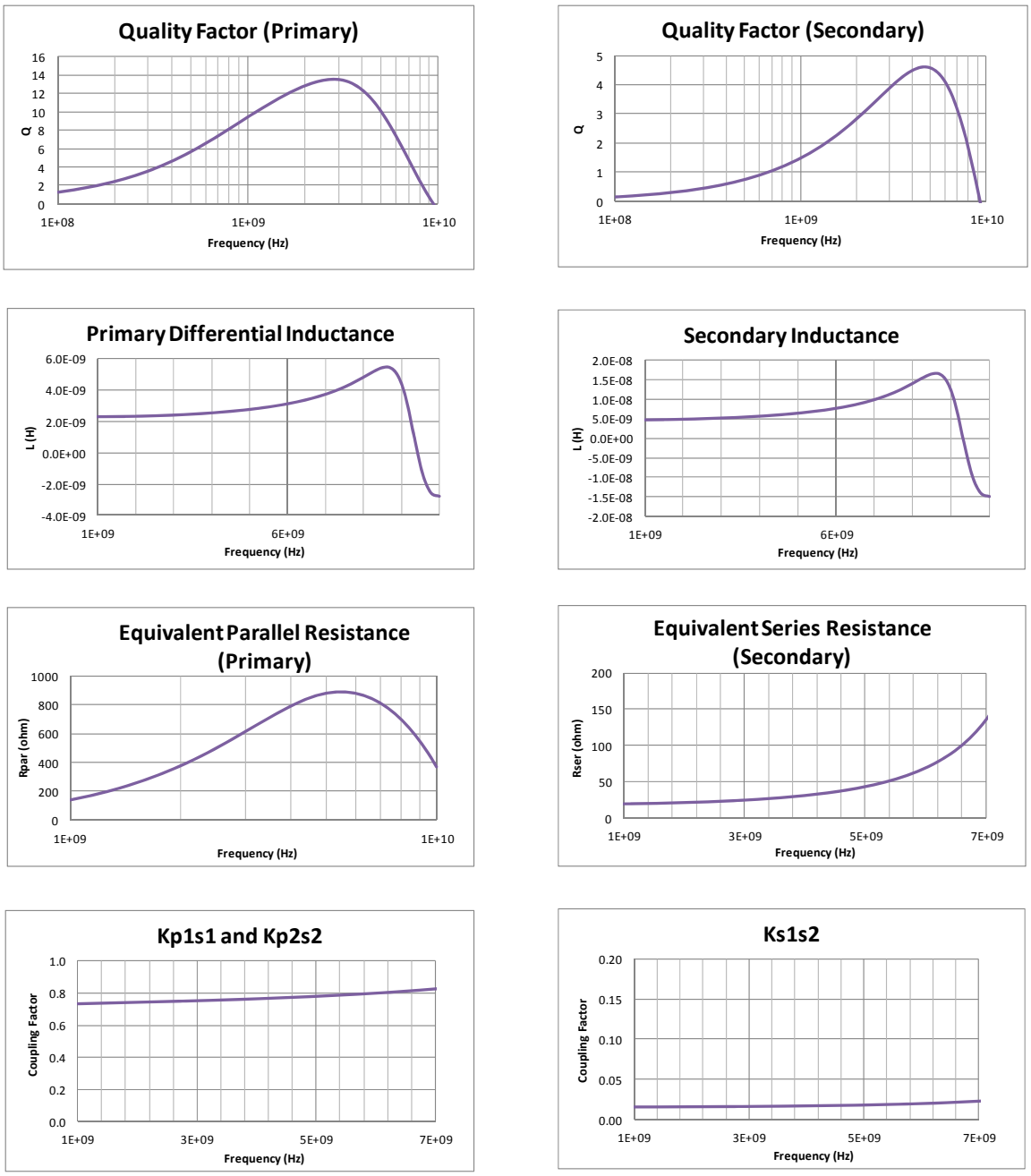


Fig. 4-4 Key parameters of the transformer

A physical-based lumped-model is also generated for simulation purpose. The model includes the self and the mutual inductances, the terminal-to-substrate parasitic

capacitance, the terminal-to-terminal parasitic capacitance, the winding-to-winding parasitic capacitance, the winding and the substrate losses due to the ohmic, skin and proximity effects.

4.2.2. Switchable Capacitor Bank

In order to guarantee the frequency coverage over various conditions as well as keep K_{vco} relatively small for low frequency tuning sensitivity, a combination of varactors and an 8-bit weighted capacitor array with a switch for each capacitor bank [4-2] are used to resonate with the inductor. The oscillation frequency is coarsely tuned using the weighted capacitor array, and then finely tuned by the varactors. A schematic of the 8-bit switchable capacitor array and the varactors are illustrated in Fig. 4-5. When *CT<i>* is 0, the switch is turned on and the NMOS transistor behaves as a resistor. The two associated capacitors on the bank are connected to the LC tank through the NMOS. When *CT<i>* is 1, the switch is turned off to open the path. The tradeoff is the on-resistance of the switch should be very low for not degrading the *Q* of the capacitor bank. On the other hand, the parasitic capacitance of the NMOS switch should be small enough for not affecting the tuning range.

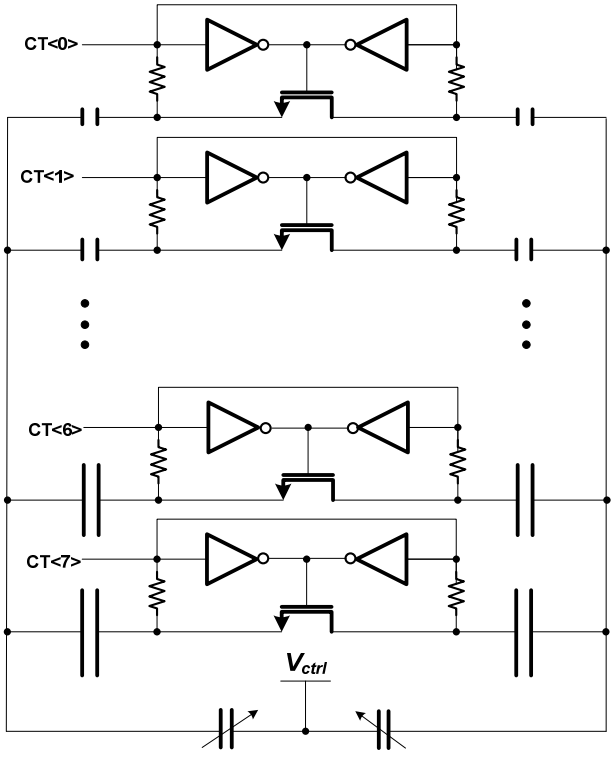


Fig. 4-5 Schematic of the switchable capacitor bank and the varactors

The coarse tuning capacitor bank needs to be calibrated each time before enabling the synthesizer analog loop. The calibration procedure based on a binary search algorism is described as follows:

1. Set the control voltage of the VCO to be a fixed voltage, usually half of the supply, by a voltage generator;

Then, starting from the most significant bit of the coarse tuning code,

2. Set the bit to be one;
3. Estimate the VCO frequency f_{est} using an on-chip RF digital counter;
4. Make a decision
   - Stop here, if $f_{est} = f_{target}$;
   - Set the bit to be 0, if $f_{est} > f_{target}$, and then repeat step 2,3 and 4 for the less significant bit;
   - Set the bit to be 1, if $f_{est} < f_{target}$, and then repeat step 2,3 and 4 for the less significant bit;
5. Go back to step 2 unless it is the least significant bit (LSB).

The resolution and the accuracy of the digital counter causes the error in the VCO frequency during the coarse tuning process. The accuracy can be improved by increasing the calibration time, which is not an issue for GPS applications.

An ideal frequency tuning characteristic is shown in Fig. 4-6. The control voltage variation ΔV_{ctrl} can be roughly estimated as the frequency offset Δf_{offset} divided by K_{vco}. The frequency offset can be introduced by the discrete coarse-tuning frequency step, the bank selection error, and the frequency drift over temperature. A large ΔV_{ctrl} can possibly cause the synthesizer loop unlock. To minimize Δf_{offset} due to the discrete coarse-tuning frequency step, it is important to determine the LSB capacitance to the varactor capacitance ratio carefully for the sufficient frequency overlap between two adjacent coarse tuning curves. A frequency-drift temperature compensation circuit is normally required to reduce the frequency variation over temperature.

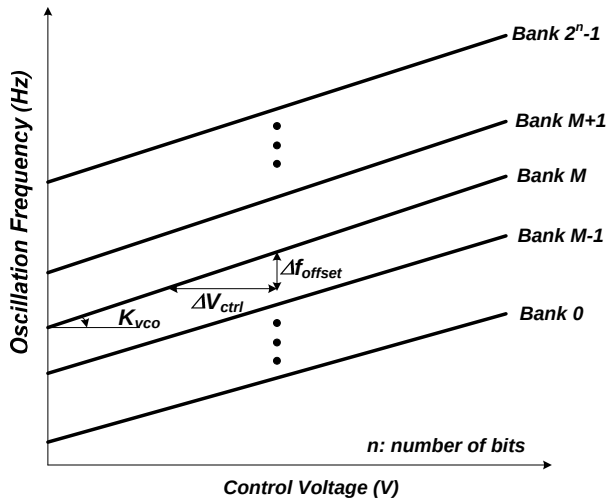


Fig. 4-6 An ideal frequency tuning curve with multiple banks

4.2.3. Frequency-drift Temperature Compensation

The VCO frequency drift over temperature poses a potential problem to a GPS system where the synthesizer must remain in lock over entire temperature range and can not be re-locked. One possible remedy is to enlarge the varactor to accommodate the frequency drift range, however, it increases the tuning sensitivity and hence the phase noise coupled through the control voltage. Therefore, it is indispensable to compensate the temperature variation without increasing K_{vco}.

The VCO oscillation frequency is mainly determined by the inductance and the effective capacitance in the resonant tank. The temperature dependence of an inductor is normally negligible. Contrarily, the effective capacitance is sensitive to the temperature, such as the reverse-biased junction capacitors of the transistors [4-3]. Although several different temperature compensation circuits have been reported in [4-3]-[4-5], the basic idea is the same: use of a temperature dependent voltage to bias the varactors.

The block diagram of the temperature compensation circuit implemented in this design is shown in Fig. 4-7. A temperature dependent voltage V_b is generated by multiplying a PTAT (proportional to absolute temperature) bias current I_{ptat} and a resistor $R1$. Since the larger the voltage temperature coefficient T_c, the smaller the extra varactor needed. A simple common-source amplifier is thus added to amplify T_c. To minimize the process variation of V_{temp}, a diode-connected NMOS transistor is used as the load of the

amplifier. Also, an RC filter with a pole at a frequency below 1 kHz is employed to reduce the noise contribution of the bias generation circuit.

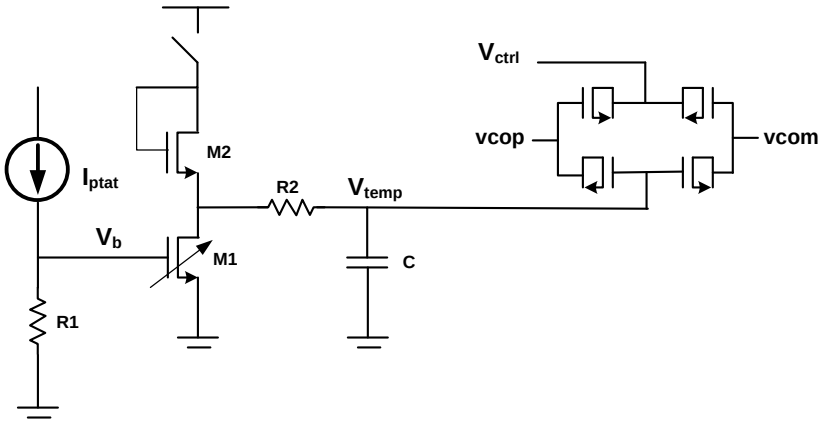


Fig. 4-7 Block diagram of a frequency-drift temperature compensation circuit

4.2.4. Adaptive Amplitude Control (AAC) with Peak Detector

Due to large process and temperature variations, it is difficult to optimize the design over all the conditions. For instance, a large bias current or a high supply voltage is usually necessary to ensure a robust start-up of the VCO and meet the phase noise specification under slow process and hot temperature conditions. Consequently, the power may not be optimal at typical and fast process corners. It is thereby desirable to implement a tracking loop to control the operation conditions intelligently. A few adaptive-amplitude control (AAC) techniques for the VCOs have been presented in [4-6]-[4-8]. By utilizing the AAC, the start-up, the power and the phase noise of the VCO can be kept at a more or less optimal level over all the conditions. However, the stability, the area and power overhead, and the extra noise contributions from the AAC circuit are the things that need to be considered.

The block diagram of an adaptive amplitude control circuit implemented in this design is shown in Fig. 4-8. The VCO output amplitude is sensed by a peak detector (PD) and then fed into a comparator. If the amplitude is higher than the reference voltage V_{ref}, then the PD output signal *pd_out* becomes high; otherwise, the *pd_out* goes low. V_{ref} can be programmed by a control signal V_{ref}*_Rsel*. A digital finite state machine (FSM) records the *pd_out* and generates the control signals *Rsel* to the VCO regulator.

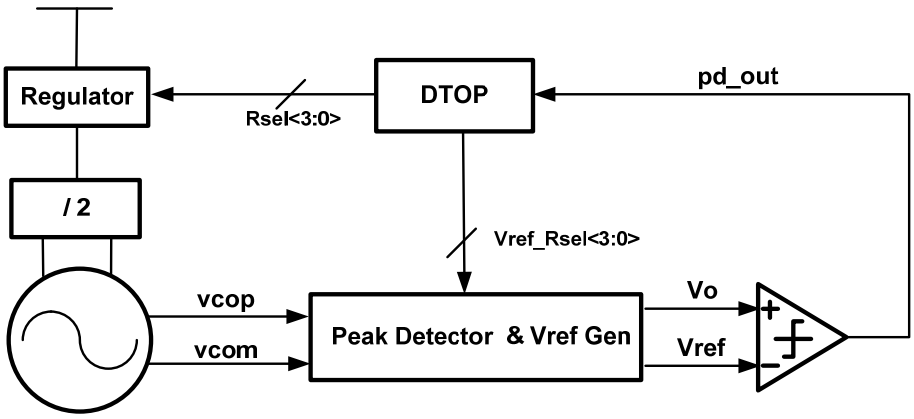


Fig. 4-8 Block diagram of a frequency-drift temperature compensation circuit

The calibration procedure is as follows:

1. Enable the VCO and the PD, set *Rsel<3:0>* = {default code};
2. Set V_{ref}*_Rsel<3:0>* = {code 1};
3. Record the PD output as pd_out1;
4. Set V_{ref}*_Rsel<3:0>* = {code 2};
5. Record the PD output as pd_out2;
6. Set *Rsel<3:0>* = {specific code based on pd_ou1 and pd_ou2};
7. Disable the PD;

The PD is enabled only during the calibration mode. Since this is an open-loop control, there is no instability concern. Also, there is no extra power and noise contribution from the AAC circuit.

The schematic of the peak detector and the reference voltage generator is shown in Fig. 4-9, where V_{inp} and V_{inm} are the differential VCO output signals. The PD works as a full-wave rectifier. The two differential signals charge the capacitor *C1* alternatively, with each one for half of the VCO clock cycle. The charging action continues until the "peak" value is reached at the capacitor, which is

$$V_{dc} = \frac{2}{\pi} V_{VCO} \tag{4-1}$$

where V_{VCO} represents the VCO differential amplitude. As shown in Fig. 4-9, a replica bias scheme is used for the reference voltage generator. So the DC voltages of V_{ref} and V_o can track well over process and temperature.

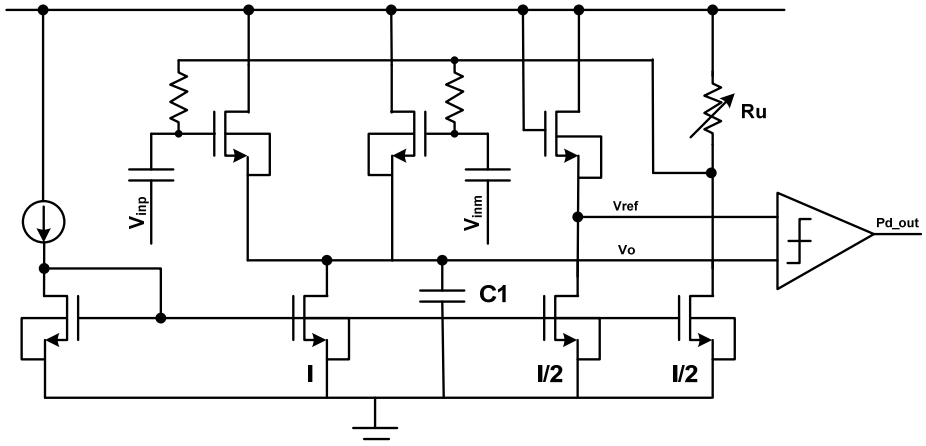


Fig. 4-9 Schematic of the peak detector and the reference voltage generator

4.2.5. Voltage Regulator

An on-chip regulator with high power supply rejection ratio (PSRR) is critical to achieve a low-noise VCO. The main challenge of the regulator design is to maintain a low supply sensitivity over a wide bandwidth while keeping the dropout voltage low and the loop stable. The dropout voltage refers to the difference between the external supply and the internal supply generated by the regulator. The advantage of a low dropout voltage is higher efficiency. A conventional PMOS-based low dropout (LDO) regulator with RC compensation is shown in Fig. 4-10.

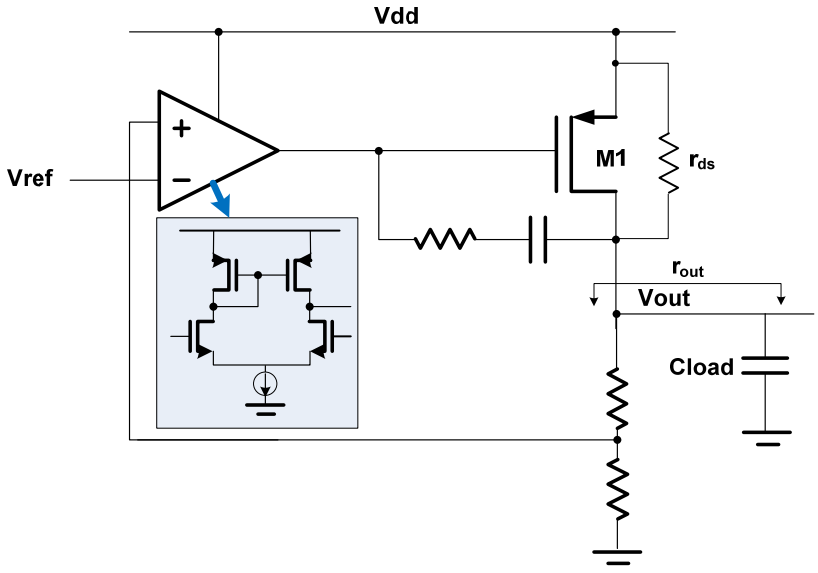


Fig. 4-10 Conventional LDO with RC compensation

In this topology, a PMOS transistor M1 is used as an output stage. Its gate voltage should follow the supply perturbation to produce a constant output voltage V_{out}. An operational transconductance amplifier (OTA) allowing the direct feedthrough of the supply ripple to the output is thus desirable for a high PSRR. Assume that A_1 and p_1 are the DC gain and the dominant pole of the OTA, A_2 and p_2 are the DC gain and the dominant pole of the output common-source amplifier, A_{vdd} is the resistive divider ratio from V_{out} to V_{dd}, equal to $r_{out}/(r_{ds} + r_{out})$. Generally, p_1 is made much smaller than p_2 with a miller C or RC compensation. Then V_{out} can be approximately written as:

$$V_{out} = \frac{V_{dd}A_{vdd}/(1+s/p_2)}{1+A_1A_2/[(1+s/p_1)(1+s/p_2)]} \tag{4-2}$$

Therefore, the PSRR of the conventional LDO is:

$$PSRR \triangleq \frac{\text{def}}{V_{dd}} \approx \begin{cases} A_{vdd}/A_1A_2 & DC \\ \dfrac{A_{vdd}(1+\frac{s}{p_1})}{A_1A_2} & p_1 \sim UGF \\ A_{vdd} & at\ UGF \\ \dfrac{A_{vdd}}{1+s/p_2} & > p_2 \end{cases} \tag{4-3}$$

where *UGF* represents the unit gain frequency at which the PSRR is small. For a stable loop, *UFG* should be between p_1 and p_2. Since the loop normally has two closely spaced poles, a compensation is required to stabilize it. The LDO in Fig. 4-10 uses a Miller RC compensation. However, the stability is achieved at the cost of a lower open-loop gain. Several different compensation techniques have been presented in [4-9]-[4-11]. A replica biased regulator topology proposed in [4-9] is shown below.

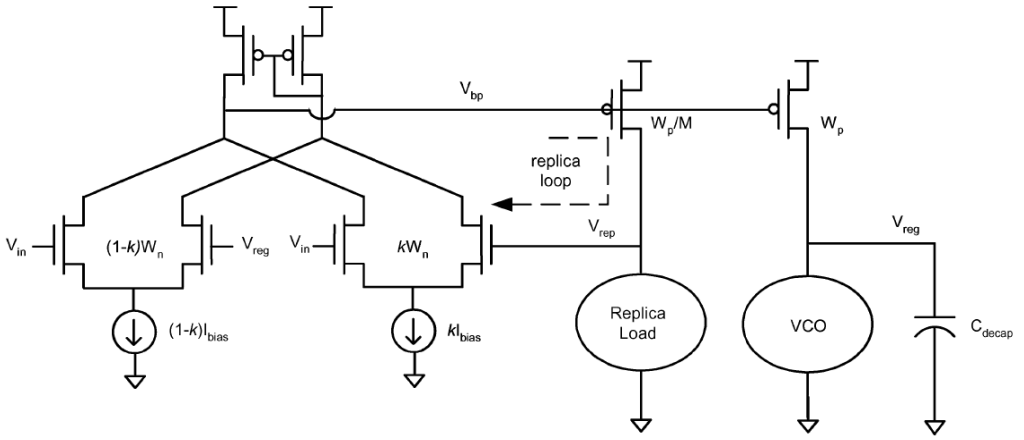


Fig. 4-11 Replica compensated regulator [4-9]

The key idea is by introducing a secondary replica feedback loop, the effective pole of the OTA is pushed out far from the pole of the output stage, so the main loop can be stabilized without narrowing the open-loop bandwidth. In other words, the high-frequency PSRR is improved. Assume that $(1-k)A_1$ is the DC gain of the OTA in the main loop, kA_1 is the DC gain of the OTA in the replica loop, p_1 is the dominant pole of the OTA, A_2, p_2 and A_{vdd}, are the DC gain, the dominant pole and the divider ratio of the main output stage, respectively, A_{22}, p_{22} and A_{vdd2}, are the DC gain, the dominant pole and the divider ratio of the replica output stage, respectively. Note that $A_2 = A_{22}$ and $A_{vdd} = A_{vdd2}$ if the replica load matches the main load perfectly, also $p_{22} >> p_2$ as the capacitor attached to the replica load is much smaller. The PSRR can be derived from the following equations:

$$\begin{cases} \frac{-V_{out}\cdot(1-k)A_1 - V_{rep}\cdot kA_1}{1+s/p_1} = V_{bp} \\ \frac{V_{dd}A_{dd}+V_{bp}A_2}{1+s/p_2} = V_{out} \\ \frac{V_{dd}A_{dd2}+V_{bp}A_{22}}{1+s/p_{22}} = V_{rep} \end{cases} \tag{4-4}$$

Then V_{out} can be written as:

$$V_{out} = \frac{\frac{V_{dd}A_{dd}}{1+s/p_2}}{1+\frac{(1-k)A_1A_2}{(1+s/p_1)(1+s/p_2)}+\frac{kA_1A_2}{(1+s/p_1)(1+s/p_{22})}} \tag{4-5}$$

Therefore, the PSRR can be expressed as:

$$PSRR \approx \begin{cases} A_{vdd}/A_1A_2 & DC \\ \frac{A_{vdd}(1+\frac{s}{p_1})}{A_1A_2(1+k\frac{s}{p_1})} & p_1(p_2) \sim UGF \\ \frac{A_{vdd}}{1+s/p_2} & > UGF \end{cases} \tag{4-6}$$

The replica biased regulator has the same DC gain but a higher unit gain frequency as compared to the conventional LDO. So the PSRR is improved for high frequencies. In this topology, a relatively large loading capacitor is normally required to form a low dominant pole (p_2) at the output stage. However, it is limited by the die area. Also, the performance highly depends on the matching between the main load and the replica load.

The conventional LDO does not use a standard NMOS transistor as the output stage because of the high dropout voltage. The availability of the native device in this

design makes the conventional LDO with an NMOS output stage a viable topology. The schematic is shown in Fig. 4-12 4-12.

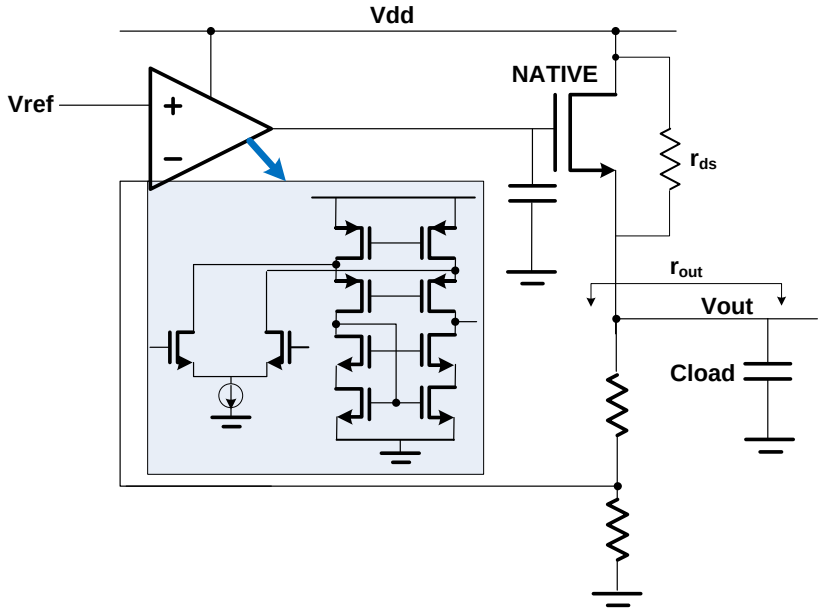


Fig. 4-12 Native-NMOS LDO regulator

The loop stability can be maintained easily as the output impedance of the output stage is low, so that its dominant pole is far away from the pole of the OTA. The output stage is a source follower, and hence it is important to keep the gate voltage of the NMOS transistor clean. A folded-cascode OTA that does not allow the direct feedthrough from the supply to the OTA output is thereby desirable. Assume that A_1 and p_1 are the DC gain and the dominant pole of the OTA, A_2 is the product of the transconductance of the native NMOS and the equivalent resistance (r_{ds} // r_{load}) at the output node (Note that it is *NOT* the gain of the source follower, and A_2 >>1), p_2 is the dominant pole of the output stage, which is equal to $(1+A_2)/[C_{load}\cdot(r_{ds}$ // $r_{load})]$, usually much larger than p_1, A_{vdd} is the resistive divider ratio from V_{out} to V_{dd}, equal to $r_{out}/(r_{ds} + r_{out})$. Then V_{out} can be approximately written as:

$$V_{out} = \frac{\frac{V_{dd}\cdot A_{vdd}}{(1+A_2)(1+s/p_2)}}{1+\frac{A_1}{(1+s/p_1)}\cdot\frac{A_2}{(1+A_2)(1+s/p_2)}} \tag{4-7}$$

Therefore, the PSRR of the NMOS LDO is:

$$PSRR \triangleq^{\text{def}} \frac{V_{out}}{V_{dd}} \approx \begin{cases} A_{vdd}/A_1A_2 & DC \\ \frac{A_{vdd}(1+\frac{s}{p_1})}{A_1A_2} & p_1 \sim UGF \\ \frac{A_{vdd}}{A_2} & at\ UGF \\ \frac{A_{vdd}}{1+s/p_2} & > p_2 \end{cases} \quad (4\text{-}8)$$

Apparently the NMOS LDO has higher PSRR at the high frequencies as compared to its PMOS counterpart. All of the three different regulators have been designed with the same loading condition and the power budget. A performance comparison based on the simulation results is shown in Table 4-4.

Table 4-4 Regulator performance comparison

Topology	PSRR (dB)						Noise (dB)			PM (°)	C_{load} (pF)
	10k	100k	1.6M	3.2M	19.2M	100M	1k	10k	100k		
PMOS LDO	-63	-43	-19	-13	0.3	-4.4	-144	-151	-153	69	20
NMOS LDO	-78	-60	-36	-31	-21	-28	-144	-151	-151	71	20
Replica PMOS	-64	-53	-33	-29	-13	-14	-135	-145	-151	59	20

It can be seen that the NMOS LDO has the best overall performance among the three, in terms of the PSRR, the noise and the loop stability (or phase margin). Therefore, it is chosen for this design.

4.2.6. LO Buffers

Due to the large LO signal swing required by the following passive mixers, an amplification stage or LO buffer is necessary for this design. An ac-coupled self-biased CMOS buffer in Fig. 4-13 is commonly used for its simplicity and ease of design. However, the small-signal gain of the buffer is very sensitive to process, temperature and supply (PVT) variations, especially at low supply voltage. To ensure sufficient gain even in the worst condition (low temperature and slow process), a g_m-tuned bias scheme is designed for the ac-coupled LO buffer, where the NMOS transistor and the PMOS transistor are biased at different levels. The schematic of the LO buffer with the bias generation circuit is shown in Fig. 4-14.

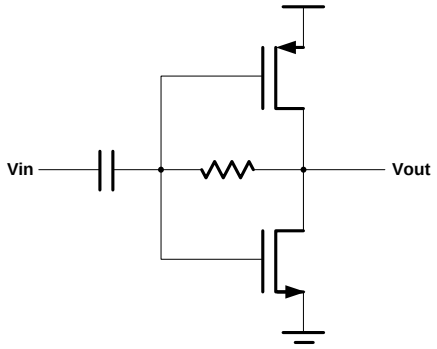


Fig. 4-13 An ac-coupled self-biased CMOS buffer

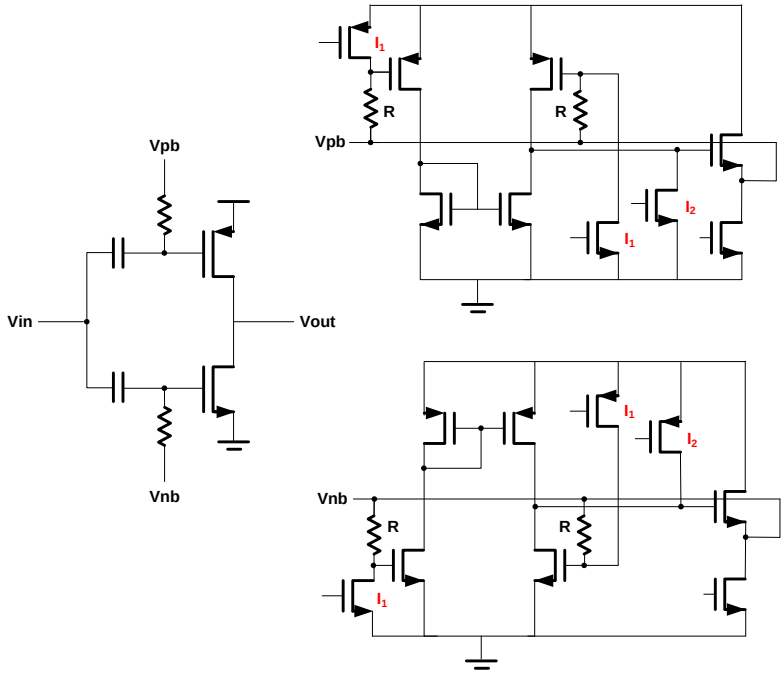


Fig. 4-14 An ac-coupled CMOS buffer with g_m-tuned bias

Assume that there is no channel length modulation effect, I_1 is generated from the bandgap reference voltage divided by a resistor, and I_2 from the bandgap reference voltage divided by a tuned resistor, then the transconductances of the PMOS and the NMOS transistors can be written as:

$$2I_1Rg_{mp} = I_2 \quad \text{and} \quad 2I_1Rg_{mn} = I_2 \tag{4-9}$$

Since the variation of R is compensated by I_1, g_{mp} and g_{mn} are constant at all the conditions. Following the ac-coupled g_m-tuned buffer, a simple CMOS inverter is used as a 2nd stage buffer to further improve the driving capability.

4.2.7. A Complete Schematic of the LO Generation Circuitry

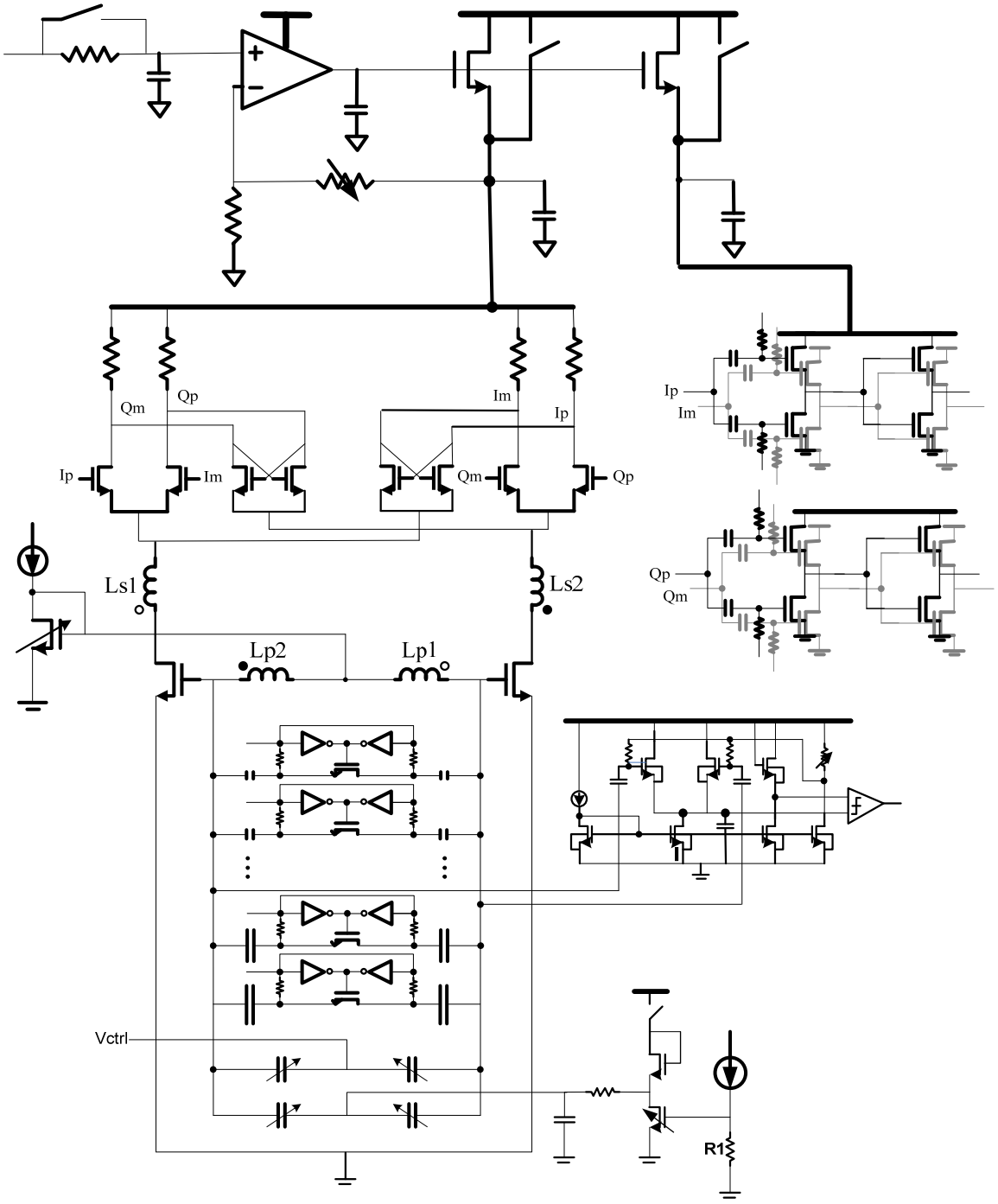


Fig. 4-15 A complete schematic of the LO generation circuitry

4.3. Simulation Results

The LO generator was laid out and fabricated in CMOS 65 nm technology. Extensive post layout simulations were performed to check the circuit performance under various conditions. A few important simulation results, which cannot be measured directly, are shown below.

a) VCO, divider and LO output signal amplitudes

The top waveform in Fig. 4-16 is the output of the divide-by-two, the middle one is the output of the LO buffer, and the VCO output signal is shown at the bottom.

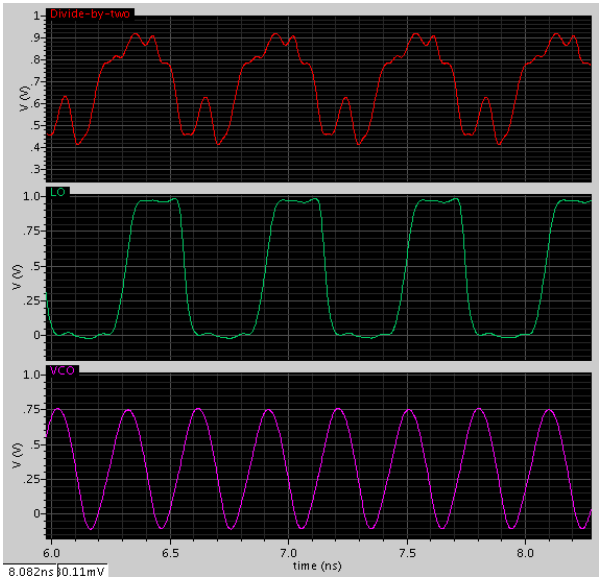


Fig. 4-16 Transient waveforms of VCO, divide-by-two and LO output signals

b) Supply sensitivity

Fig. 4-17 shows the PSRR of the regulator. The curve in red is the PSRR when the output voltage of the regulator is equal to 1.16 V, or the dropout voltage is 40 mV (V_{dd} = 1.2 V). The curve in green is the PSRR for the output voltage equal to 1 V. The simulation results demonstrate that the regulator can provide decent PSRR over wide frequency range as long as the dropout voltage is kept larger than 200 mV. Fig. 4-18 illustrates the supply sensitivity of the LO frequency, K_{vdd}, over process variations. In the simulation, the output voltage of the regulator is about 1 V. The result shows that K_{vdd} is less than 1 MHz/V if the supply voltage is larger than 1.15 V.

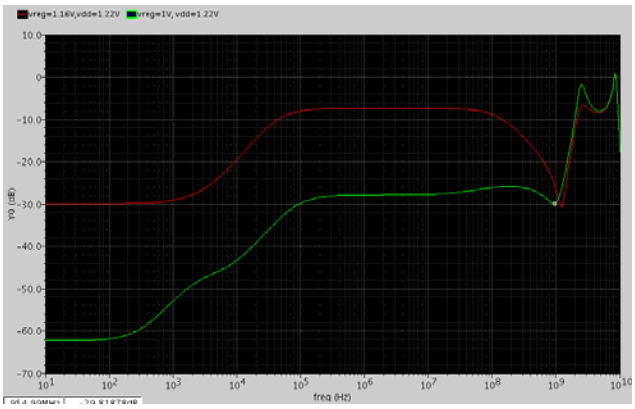


Fig. 4-17 Simulated PSRR for V_{reg} = 1.16 V and V_{reg} = 1V

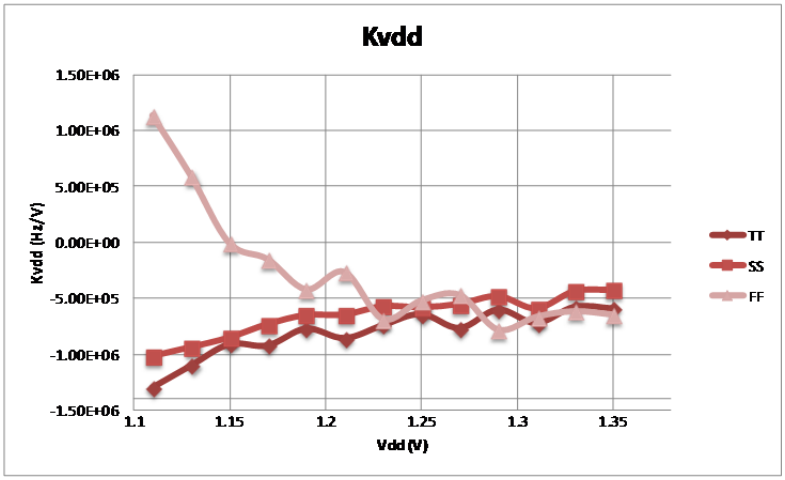


Fig. 4-18 Simulated LO supply sensitivity K_{vdd}

c) I and Q Mismatch

The relationship between the residual sideband (RSB) and I/Q mismatch can be described as follows:

$$\text{RSB (dBc)} = 10\log_{10}\frac{1+A^2-2A\cos\theta}{1+A^2+2A\cos\theta} \qquad (4\text{-}10)$$

where A is the voltage ratio between I and Q amplitudes and θ is the phase deviation from quadrature between I and Q. The higher the absolute value of RSB, the better the I and Q matching. Monte Carlo simulations with 100 runs were performed to check I and Q phase mismatch, amplitude mismatch and RSB in low linearity mode. The results are shown in Fig. 4-19, Fig. 4-20 and Fig. 4-21, respectively. Fig. 4-19 shows that the worst phase mismatch can be more than 5 degree, which translates into an RSB of -27 dBc even

without any amplitude mismatch. Therefore, the phase mismatch is a dominant factor to determine the RSB.

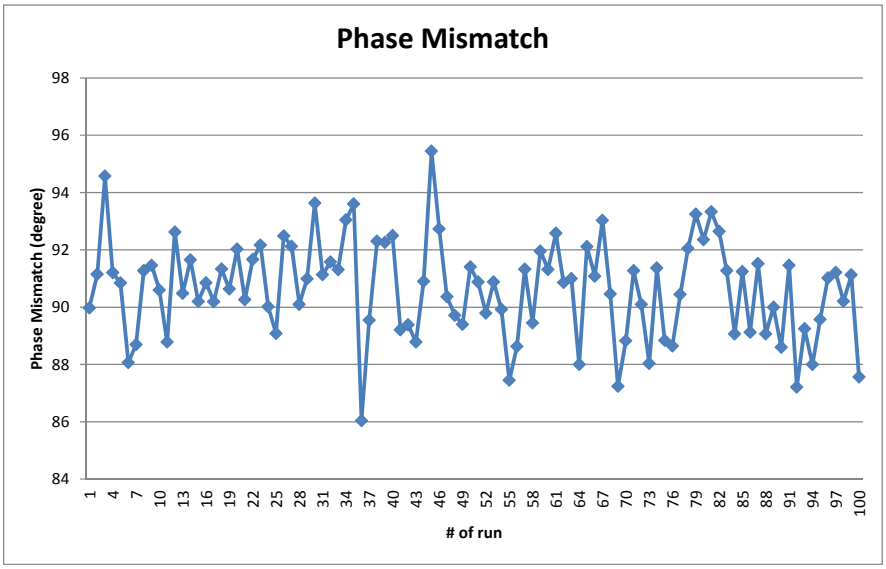


Fig. 4-19 I and Q phase mismatch in low linearity mode

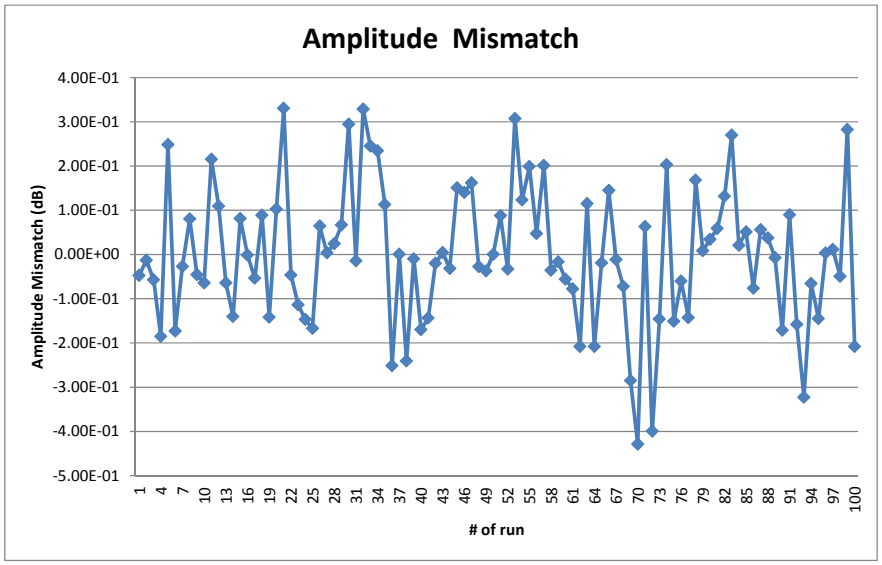


Fig. 4-20 I and Q amplitude mismatch in low linearity mode

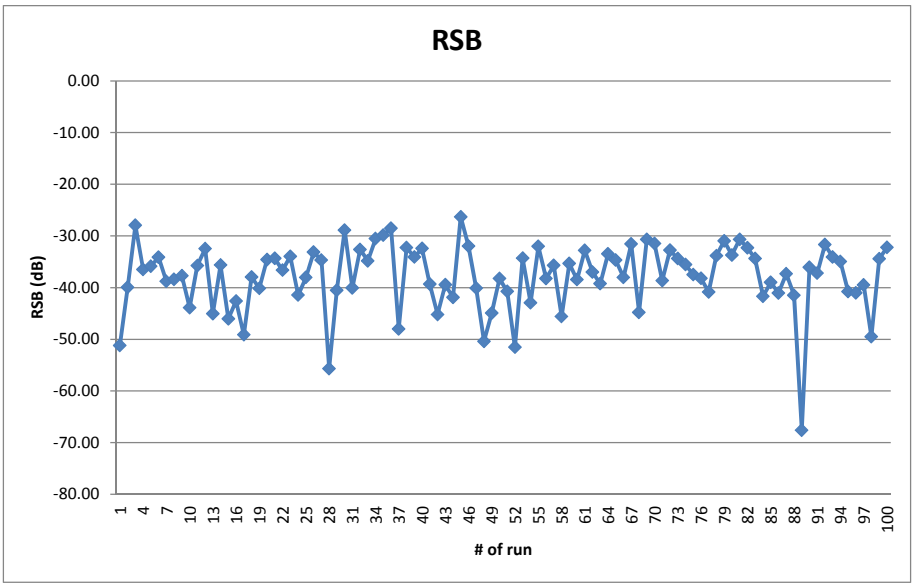


Fig. 4-21 RSB in low linearity mode

4.4. Measurement Results

The entire GPS receiver including the LO generation circuitry was fabricated in TSMC 65 nm CMOS technology. The chip microphotograph is shown in Fig. 4-22.

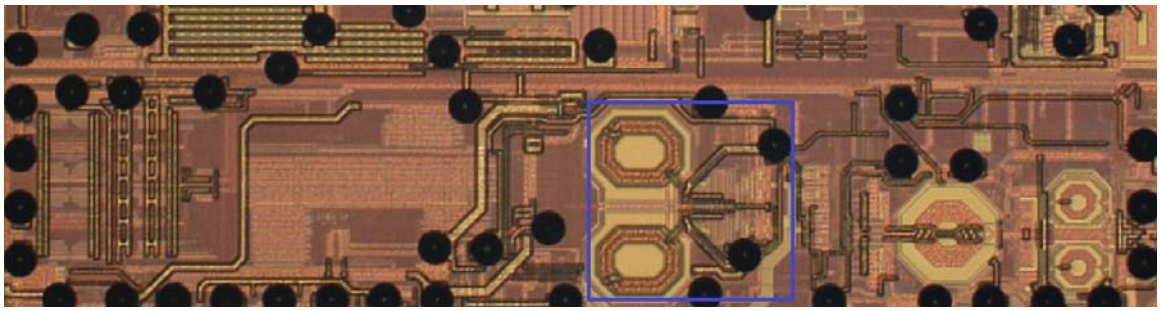


Fig. 4-22 Chip microphotograph of the LO generation circuitry

Fig. 4-23 shows the measured LO spectrum when the frequency synthesizer is in lock. The measured LO frequency is 1588.74 MHz. The reference spurious level is about -77.4 dBc.

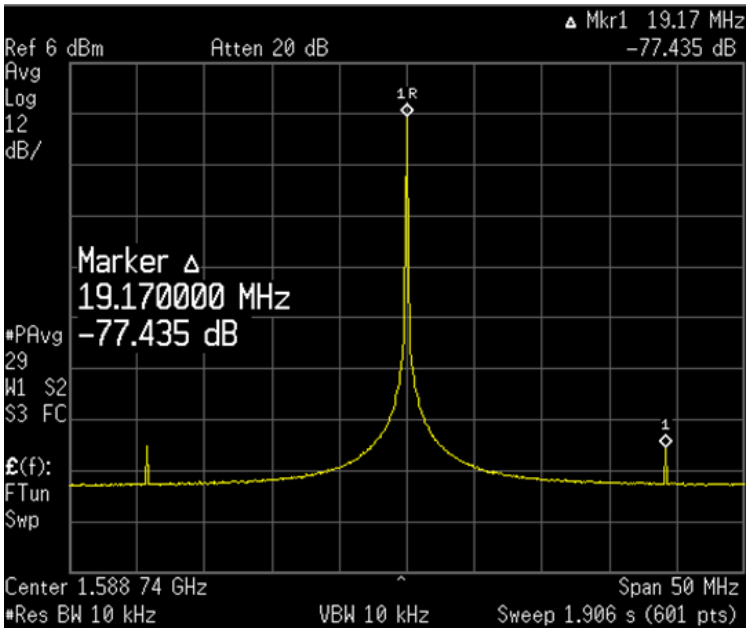


Fig. 4-23 Measured the LO spectrum

Fig. 4-24 demonstrates the VCO coarse tuning calibration and the synthesizer close-loop settling behavior. It can be observed that during the calibration the frequency jumps up an down, and eventually settles to the closest bank.

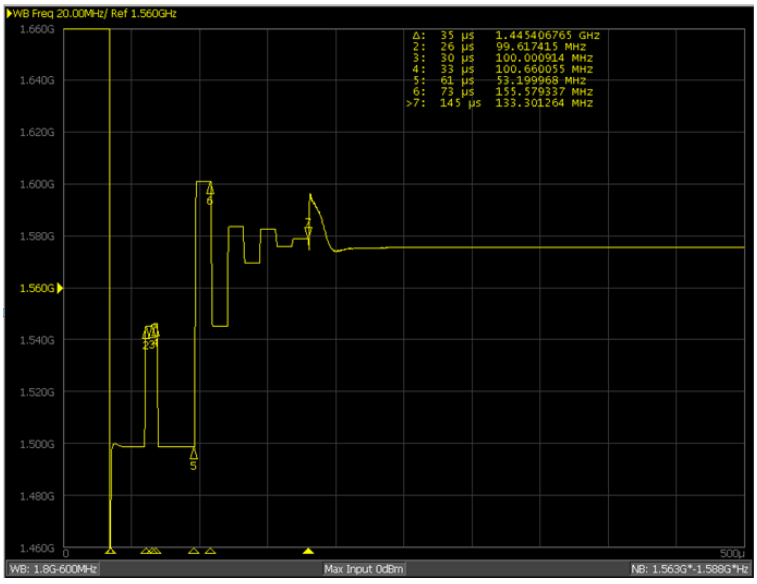


Fig. 4-24 Measured the LO frequency during the calibration and normal operation

Fig. 4-25 illustrates the measured single side-band (SSB) integrated phase noise (IPN) of the synthesizer, which is about -29 dBc. It meets the design specification (-23 dBc) with plenty of margin. The loop bandwidth of the synthesizer is about 45 KHz.

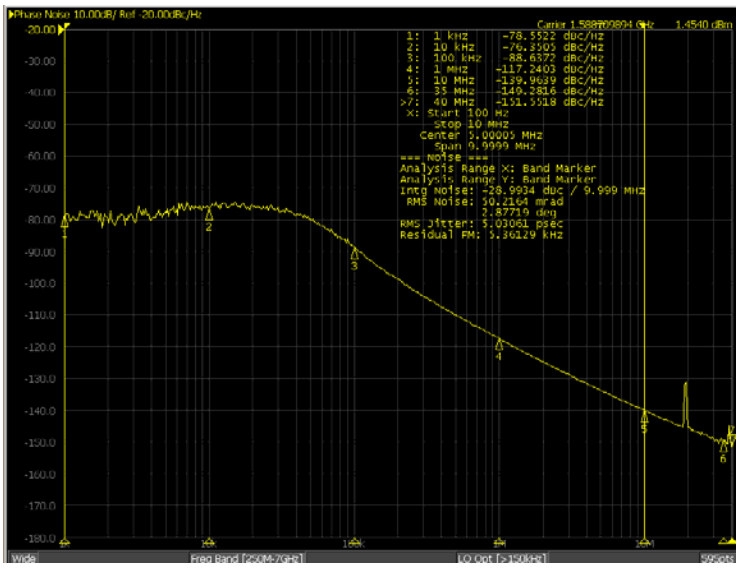


Fig. 4-25 Measured the single side-band integrated phase noise (IPN)

The transformer-based VCO stacked with the divide-by-two operates at an internal supply voltage of 1 V, and consumes 2.6 mW in high linearity mode, and about 2 mW in low linearity mode. The power consumption of the LO can be reduced further by lowering the supply, but the phase noise performance becomes worse as shown in Fig. 4-26.

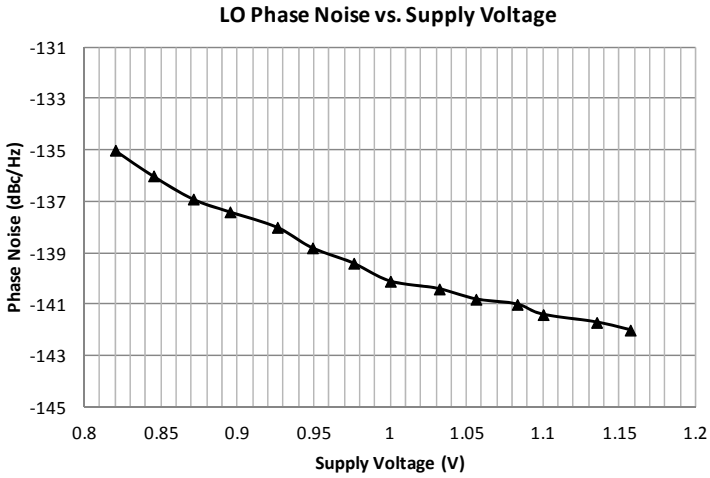


Fig. 4-26 Measured LO phase noise versus the supply voltage in high linearity mode

In high linearity mode, the measured LO phase noise at the carrier frequency of around 1.6 GHz is shown in Fig. 4-27. The phase noise is -140.4 dBc/Hz at 10 MHz offset frequency and -151.5 dBc/Hz at 35 MHz offset frequency.

Fig. 4-27 Measured LO phase noise in high linearity mode

In low linearity mode, the measured LO phase noise is shown in Fig. 4-28. The phase noise is -138 dBc/Hz at 10 MHz offset frequency and -145 dBc/Hz at 40 MHz offset frequency.

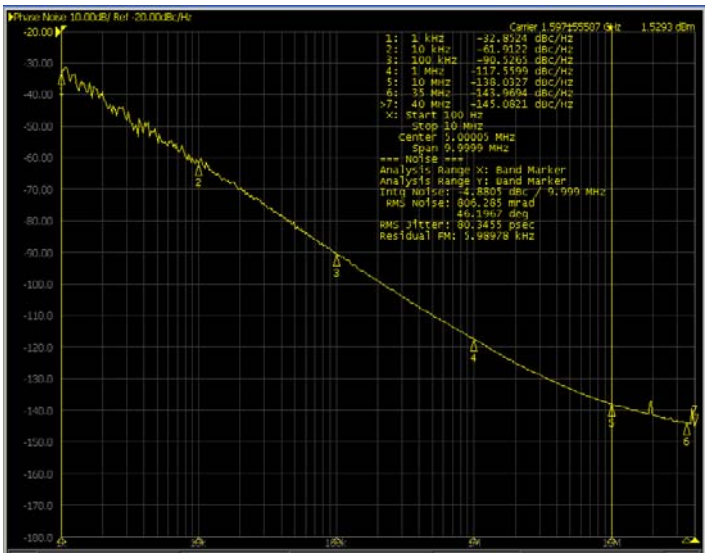


Fig. 4-28 Measured LO phase noise in low linearity mode

To verify the robustness of the proposed LO, the chips were tested under various conditions. The measured LO phase noise over the process (SS: slow process, TT: typical process and FF: fast process) corners and the temperature (LT: low temperature, RT: room temperature and HT: high temperature) variations is shown in Fig. 4-29. The worst performance happens at the corner of slow process and high temperature. Even at this

corner, we observed that the VCO could start up vigorously at the lowest possible voltage (= 0.82 V) of the on-chip regulator.

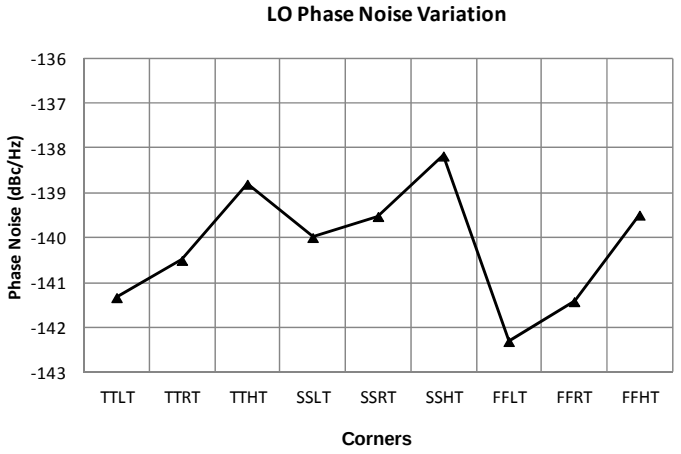


Fig. 4-29 Measured LO phase noise over the process and temperature variation

The measured LO frequency tuning range is roughly from 1.35 GHz to 1.75 GHz or about 26 percent as illustrated in Fig. 4-30. To ensure a sufficient overlap, the tuning curve is intentionally designed as being non-monotonic. The discrete coarse tuning characteristic and the LO gain K_{lo} are shown in Fig. 4-31 and Fig. 4-32, respectively. From the lowest coarse tuning capacitor bank to the highest capacitor bank, K_{lo} varies from 30 MHz/V to 90 MHz/V roughly. K_{lo} is about 60 MHz/V at the LO frequency of 1.6 GHz.

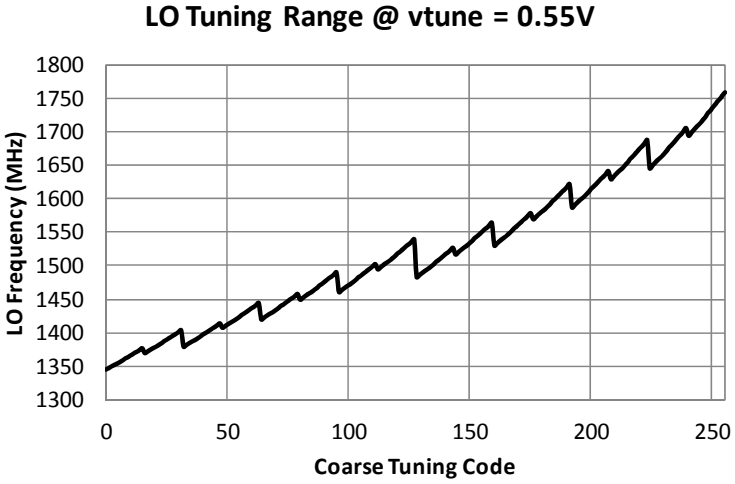


Fig. 4-30 Measured LO frequency tuning range

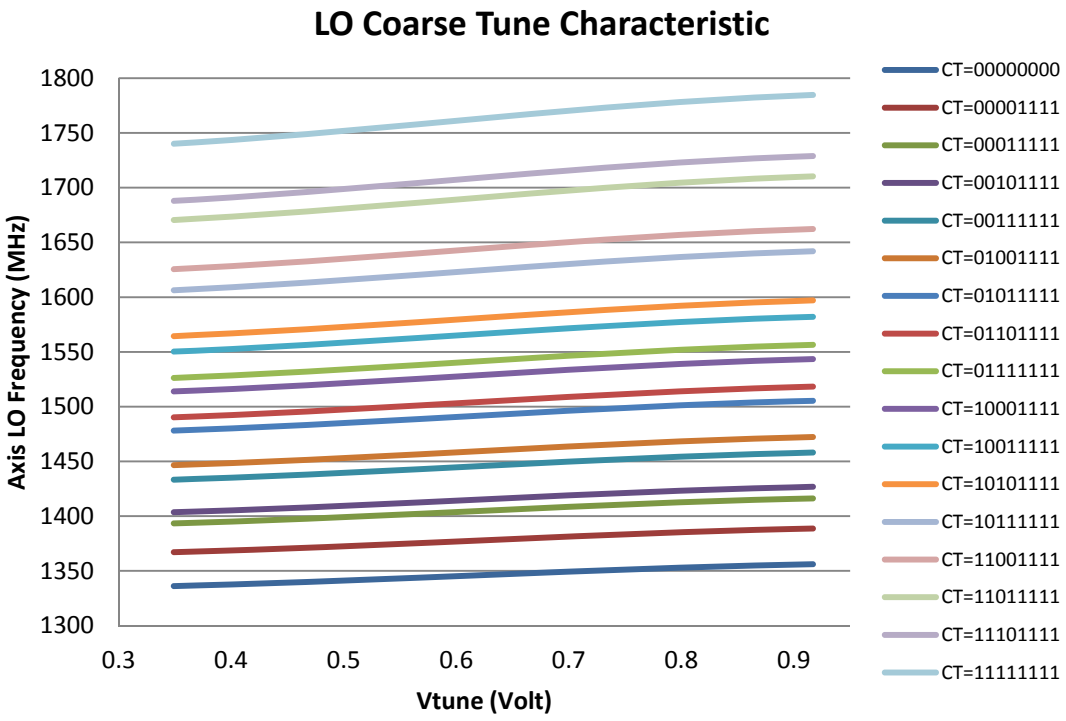


Fig. 4-31 Measured LO coarse tuning characteristic

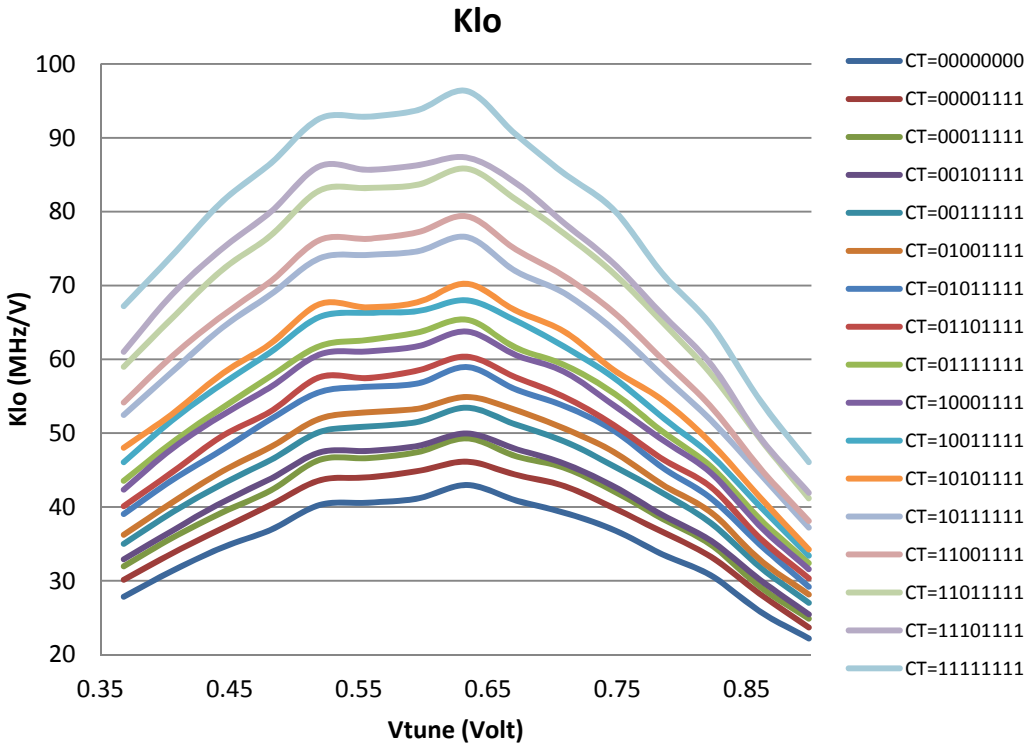


Fig. 4-32 Measured LO Gain K_{lo}

The performance of the temperature compensation circuitry is shown in Fig. 4-33. When the temperature varies from -30 ºC to 110 ºC, the LO frequency drifts more than 10 MHz without the temperature compensation (TC). After the TC circuit is enabled, the LO frequency drift reduces to less than 2 MHz for the same temperature range.

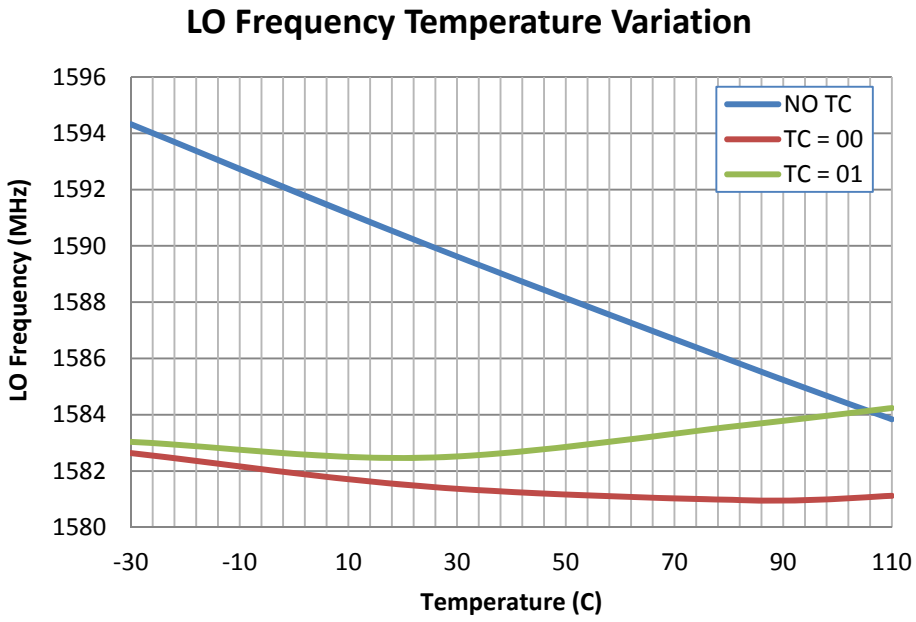


Fig. 4-33 Measured LO frequency drift w/ and w/o temperature compensation

Table 4-5 shows the variation of the control voltage applied to the varactors with and without the TC. The voltage variation is as high as 252 mV without the TC. It is reduced to 28 mV with the TC.

Table 4-5 Control voltage variation w/ and w/o temperature compensation

Process	**TT**		**SS**		**FF**	
Vctrl	*No TC*	*TC (01)*	*No TC*	*TC (01)*	*No TC*	*TC (01)*
110	0.515	0.493	0.527	0.519	0.568	0.558
-30	0.29	0.493	0.275	0.51	0.421	0.586
ΔV	-0.225	0	-0.252	-0.009	-0.147	0.028

4.5. Performance Comparison

Table 4-6 compares the performance of the proposed quadrature LO against the existing recent LOs. The figure of merit (*FoM*) in the table is defined as

$$FoM = 10log\left[\left(\frac{\omega_o}{\Delta\omega}\right)^2 \frac{1}{L(\Delta\omega)\cdot P}\right] \quad (4\text{-}10)$$

where $L(\Delta\omega)$ is the phase noise at $\Delta\omega$, and P the power consumption in mW. The modified *FoM* (FoM_T) [4-12] is included to take the tuning range into consideration and given below.

$$FoM_T = 10log\left[\left(\frac{\omega_o}{\Delta\omega}\cdot\frac{TuningRange(\%)}{10}\right)^2 \frac{1}{L(\Delta\omega)\cdot P}\right] \quad (4\text{-}11)$$

Although a fair comparison is difficult due to different technologies, operating conditions, and design objectives, the proposed LO achieves the lowest power consumption and the highest FoM_T among the recently reported quadrature LOs.

Table 4-6 LO performance comparison

Ref.	Tech. (CMOS)	V_{DD} (V)	Power (mW)	LO Freq (GHz)	Tune. Range (%)	Phase Noise (dBc/Hz)	FoM (dB)	FoM_T (dB)
[4-13]	0.18 µm	1.8	4.32	1.58	6	-121.5 @ 1 MHz	179	175
[4-14]	0.18 µm	1	5.17	2.18	23	-140.5 @ 20 MHz*	180	187
[4-15]	0.18 µm	1.8	3.06	1.57	13.7	-120 @ 1 MHz	180	182
[4-16]	65 nm	0.65	8.71	5.49	28.6	-113.3 @ 1 MHz	179	188
this work	65 nm	1	2.6	1.6	26	-140.3 @ 10 MHz	180	189

***** *phase noise at a carrier frequency of 4.36 GHz ($2f_{LO}$)*

4.6. Summary

In this chapter, a quadrature LO generation circuit design based on the proposed topology in Chapter 3 is described in details. A simulation test bench has been created to justify the design choice. As compared with the conventional LO that has a CMOS VCO followed by a divide-by-two, the transformer-based VCO combined with a divide-by-two in one branch achieves higher start-up gain and less power consumption for a similar oscillation frequency and far-offset phase noise performance. A dual-core transformer in

an interleaved structure is adopted for low power. All critical parameters of the transformer are extracted in a wide frequency range to increase the simulation accuracy. The bias voltage of the VCO differential pair and the resistive load of the divider are made programmable to optimize for the two different operation modes: low linearity (low power) and high linearity (low noise). An 8-bit switchable coarse tuning capacitor array in parallel with the varactors is utilized to cover the required tuning range with a low gain, or low sensitivity. Additional varactor pair biased at a temperature dependent voltage is employed to compensate the LO frequency drift over temperature. An native NMOS based LDO shows better PSRR at high frequencies than the conventional PMOS based LDO, and thus used to provide a clean supply to the LO. The regulator output voltage level is set during the calibration based on the VCO amplitude detected by a peak detector. The LO buffer amplifies the divider output signals and provides almost rail-to-rail LO signals to the passive mixers.

The entire GPS receiver including an LNA, a mixer, a frequency synthesizer, an LO and baseband filters is fabricated in TSMC 65 nm CMOS technology. The measured LO signal spectrum shows that the reference spurious tone is about 77.4 dB lower than the main tone. The synthesizer SSB IPN is -29 dBc. The LO phase noise is -140.3 dBc/Hz at 10 MHz offset frequency in high linearity mode, and is about 2 dB worse in low linearity mode. The typical power consumptions of the VCO stacked with the divider are 2.6 mW and 2 mW, in the high linearity and the low linearity modes, respectively. The LO frequency is tunable from 1.35 GHz up to 1.75 GHz. With the temperature compensation, the LO frequency drift is less than 2 MHz as the temperature varies from -30 ºC to 110 ºC. The proposed LO compares favorably to the recently reported LOs.

Chapter 5 Conclusions and Future Works

5.1. Conclusions

In this dissertation, a transformer-based VCO stacked with a divide-by-two for quadrature signal generation is proposed. The LO was designed and implemented in 65 nm CMOS technology. The measurement results demonstrate that the proposed LO is suitable for low-power low-voltage wireless applications. Achievements and contributions of the dissertation research are as follows.

A new quadrature LO topology. A VCO stacked with a divide-by-two to share the bias current is proposed for low power LO generation, which adopts the Armstrong transformer-based VCO configuration for low-voltage operation. The differential pair is cross-coupled through the mutual inductance between the primary and the secondary coils, and hence it can operate at very low voltage. The resonant tank is connected between the gates of the differential pair, and the CML divide-by-two is driven by the drain current. Thus, a good isolation between the resonator and the divider is maintained, which minimizes the noise coupling.

An in-depth circuit analysis. Based upon a linearized small-signal model, the important circuit parameters, such as the VCO start-up gain, the oscillation frequency, the voltage swing and the current consumption of the proposed LO are derived quantitatively. The design tradeoffs can be understood clearly through the analysis. To estimate the phase noise performance, both the LTI and the LTV models are used to calculate the noise contributions of the resonant tank, the VCO differential pair and the divide-by-two. The mathematical equations are validated by the simulations. The results indicate that the quality factor of the primary coil and the mutual inductance between the primary and the secondary coils are two critical parameters. It is always desirable to have a high Q, but determination of the mutual inductance involves tradeoffs among the start-up gain, the signal swing, the current consumption and the phase noise.

Transformer design guidelines. A guideline on how to determine the parameters of a transformer is provided. The parameters include the primary and the secondary inductances, the mutual inductance, the quality factors, and the parasitic capacitance.

There are two possible layout configurations: dual cores and single differential core. The two options are compared in terms of the area, the complexity, and the quality factor of the primary coil.

Implementation of a complete LO. The proposed quadrature LO is designed for a GPS receiver. The primary goal is to lower the power consumption. Thus, a dual-core transformer structure is selected. To facilitate the simulation convergence, a broad-band lumped model of the transformer is generated from a s-parameter file. An 8-bit switchable capacitor bank in parallel with the varactors is utilized to cover the required tuning range with a low K_{vco}. Extra varactors biased at a temperature dependent voltage are added to compensate the frequency drift over temperature. A native NMOS based LDO provides good isolation from a noisy supply over a wide bandwidth. During the initial calibration, a peak detector is enabled to control the supply voltage. Also, a two-stage LO buffer is inserted to ensure the following stages get sufficient LO signal swings.

Demonstration of a working test chip with good measurement results. The test chip including a full receiver chain and an LO was fabricated in TSMC 65 nm CMOS technology and is fully functional. The LO operates robustly over process and temperature variations at an internal supply voltage of 1 V. The measured LO phase noise is -140.3 dBc/Hz at 10 MHz offset frequency for high linearity mode, and the typical power consumption is 2.6 mW. The tuning range of the LO is about 26 percent, roughly from 1.35 GHz to 1.75 GHz. The temperature compensation circuit helps reducing the control voltage variation from 252 mV to less than 30 mV. Also, when the synthesizer is in lock, the measured reference spurious tone at the LO output is about -77.4 dB with respect to the signal tone, and the integrated phase noise of the synthesizer is -29 dBc.

5.2. Future Works

The proposed LO generation circuit indeed achieves low power consumption and is able to operate at a low voltage. However, there are still some interesting works that are worth further exploration.

5.2.1. Optimizing the transformer design

Optimization of the transformer design is important for the proposed LO. As described in section 3.4, there are two possible transformer layout structures: one configuration is based on dual cores, which was implemented in the test chip, the other one is based on a single core. It is relatively easy to increase the secondary inductance for the dual-core structure. However, the required secondary inductance is lower for the single-core configuration, due to the fact that it is coupled to the whole primary coil, not half of it as is in the dual-core case. The single-core configuration also leads to a higher quality factor of the primary coil with a compact layout. Therefore, it could be a better choice for the proposed LO. Another LO using a single-core transformer was designed in TSMC 65 nm CMOS technology and taped out recently. The simulation shows that the LO consumes slightly higher current but achieves lower phase noise performance. Further research is necessary to compare the two transformer configurations and offer improved guidelines to optimize the design.

5.2.2. Improving the circuit analysis method

The linearized small-signal model yields good results for start-up analysis. When the LO enters large-signal operation mode, the circuit behavior is governed by the nonlinearity of the devices. In Chapter 3, the large-signal analysis is based on the assumption that the LO is in the voltage-limited region, and the current produced by the differential pair toggles between the peak value and 0 with a square-wave shape. Also, in the phase noise analysis, the noise contribution from the divider is calculated based on the assumption that the VCO differential pair works as ideal switches. However, those simplified assumptions incur a disagreement between the analytical results and the simulations ones. Moreover, as the mutual inductance increases, some parasitics of the differential pair cannot be ignored any longer, which makes the nonlinearity even worse. Therefore, it is necessary to further improve the methods for analyzing the proposed LO to gain more accurate prediction.

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