A SiC-Based Liquid-Cooled Electric Vehicle Traction Inverter Operating at High Ambient Temperature

Chi ZHANG, Srdjan SRDIC, Srdjan LUKIC, Keyao SUN, Jun WANG, and Rolando BURGOS

***Abstract*—This paper describes the design process of a high-power-density 100 kW (34 kW/L) traction inverter for electric vehicles, operating at an ambient temperature of 105 °C. A detailed thermal analysis is performed based on the thermal behavior of the switching devices, and the results are used to estimate the semiconductor device junction temperature and to determine the requirements of the cooling system to achieve the target power level. A high-temperature gate drive board aiming for reliable system operation in electric vehicles is developed. An overcurrent protection scheme based on parasitic inductance between the power source and the Kelvin source of the power module has been implemented. A dc-link decoupling snubber circuit is designed numerically based on a detailed forth-order high-frequency equivalent circuit of a double pulse test circuit. The approach to optimize the snubber circuit, not only for the voltage spike suppression but also for good thermal performance, is proposed. Finally, a hardware prototype with SiC power modules has been built and tested at 60 kW continuous power and 100 kW for 20 seconds at 105 °C ambient temperature and 65 °C inlet coolant temperature.**

***Index Terms*—Electric vehicles, high power density, high temperature, SiC, traction inverter.**

I. Introduction

MODERN power electronics converters are widely used in electric vehicles (EVs) to drive electrical machines and to provide different voltage levels from the EV battery [1]. Recently, silicon carbide (SiC) power semiconductors have been recognized as an attractive alternative to silicon devices. Compared with traditional Si-based power converters, the SiC-based converters have the potential for reliable operation at higher junction temperatures, higher switching frequencies, higher efficiency, and higher power density [2]. SiC semiconductors are capable of operating at significantly higher operating temperatures of over 400 °C theoretically, with practical limitations typically at 175 °C [3]. The higher operating junction temperature of SiC semiconductors allows for a larger temperature difference between the semiconductor junction and the coolant, thus dissipating heat more effectively.

Beyond thermal management of the switching devices, the maximum ambient operating temperature of the inverter is often limited by the maximum allowable temperatures of the system components, such as capacitors and auxiliary power supplies. The design of a 120 °C ambient temperature forced air-cooled automotive inverter using SiC JFETs was proposed in [4]. An optimized active cooling using a Peltier cooling element helps the inverter to operate at a very high ambient temperature. However, this was possible only at the expense of significantly higher complexity and reduced efficiency and power density of the overall inverter, and the volume needed for the active cooling of the signal electronics made up 20% of the overall inverter volume.

Compared to the air-cooled system, liquid-cooled systems are more attractive due to their compact design and low total (junction-to-coolant) thermal resistance as a result of the lower thermal resistance of the cold plates compared to the heatsinks. In [5], the authors report a design and experimental verification of a 200-kVA traction inverter using 900 V SiC power modules with 2.5 mΩ on-resistance. A 250-kW inverter, based on 1200-V SiC modules and achieving gravimetric power density of 15.6 kW/kg is presented in [6]. A compact 110 kVA, 140 °C ambient temperature, 105 °C liquid-cooled, SiC traction inverter with the volumetric and gravimetric power density of 23.1 kVA/L and 16.8 kVA/kg, respectively, is reported in [7]. Unfortunately, the majority of components in this system were not able to operate at 140 °C ambient, and an additional air cooling was required to keep the temperature inside the enclosure below 105 °C. In [8] and [9], a 30-kVA inverter is designed and evaluated for 180 °C ambient temperature operation. However, the switching devices in this system require a complicated cooling system design to dissipate the heat to the coolant, thus the high power density was not the priority in this design. A high-power density 100 kW SiC traction inverter with 1 kV dc-link and a printed circuit board (PCB) busbar optimized to achieve low characteristic impedance, symmetrical commutation loop, and low loop inductance, is presented in [10].

In a high-power inverter system, gate drivers play a significant role to drive the high-power modules while withstanding high ambient temperature. Because of the high cost of power

Manuscript received October 22, 2021; revised December 28, 2021; accepted January 21, 2022. Date of publication June 30, 2022; date of current version June 16, 2022.

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Digital Object Identifier 10.24295/CPSSTPEA.2022.00015

modules and safety considerations, the protection circuit design is always a critical part of gate drivers. In recent years, many short-circuit (SC) protection methods were specifically designed for high current SiC MOSFET power modules. PCB integrated Rogowski coil [11] and current mirror [12], [13] techniques have also proved to be effective for SC protection. The Rogowski current sensor-based scheme specifically has been shown to be superior to DeSat protection as it has been demonstrated to reduce energy dissipation during SC events and is much less temperature-sensitive [14]. However, this type of scheme increases gate-drive circuit complexity as it requires a PCB-winding-based Rogowski coil. Similarly, the current-mirror scheme relies on a special semiconductor die structure to measure the current through the main power semiconductor [12], [13]. To address these shortcomings, we have adopted a gate-driver protection scheme for SiC high current power module which can not only detect a short circuit fault within 80 ns, but can also detect a relatively slow overcurrent event that could generate excessive heat and damage the system.

The snubber circuits (typically in form of decoupling capacitors) placed close to the switching devices (power modules) are normally used to suppress the overvoltage spikes and ringing during turn-off transients of the switching devices. The decoupling capacitors are easy to implement and do not reduce the switching speed. The effect of decoupling capacitors is analyzed in the frequency domain and quantifiable results independent of the device's switching speed are derived in [15]. By carefully designing the snubber capacitance, the snubber can also improve the electromagnetic interference (EMI) in voltage source converters [16]. An RC snubber is also easy to apply and can provide an effective level of ringing suppression. In [17], an analytical technique based on the root locus method for designing an RC snubber for converters with phase-leg configurations is proposed. The authors proposed to neglect the loop inductance from the switching device to the snubber circuit to reduce a fourth-order equation representing the system to a third-order equation. However, the neglected loop inductance is exactly what causes the voltage spike during the transient, which significantly reduces the usability of the analysis. In addition, the analyses and designs in [15]–[17] are performed only for voltage spike suppression or EMI improvement, and there was no discussion about the thermal performance of the snubber circuits. Actually, the non-optimal thermal performance of the passive components (mainly capacitors) can become a significant limiting factor and even lead to loss of the switching devices and system failure.

The development and design of a high-power-density (34 kW/L) 100 kW EV traction inverter for 105 °C ambient temperature operation is presented in this paper. A detailed thermal analysis is performed based on the thermal behavior of the switching devices, and the results are used to estimate the semiconductor device junction temperature and to determine the requirements of the cooling system to achieve the target power level. In addition, we have implemented a gate-driver protection scheme that uses fewer simple and low-cost components compared to other methods and does not require any special technique during the manufacture of the module. The additional advantages of the proposed method include no temperature dependency, wide sensing bandwidth, and current range, very fast response speed, and high sensor density. Using the adopted approach, a compact, low-profile (90 mm × 65 mm × 8 mm) gate driver with embedded overcurrent protection is designed for a wide operating temperature range up to 105 °C.

TABLE I
THE INVERTER BASIC REQUIREMENTS

Requirement	Target value
Continuous power	60 kW
Peak power for 20 seconds	100 kW
Input dc voltage	400 V
Switching frequency	40 kHz
Peak efficiency	97%
Cooling system	Liquid
Inlet coolant temperature	65 °C
Ambient operating temperature	105 °C

A practical snubber optimization approach is evaluated for both voltage spike suppression and thermal performance improvements. The design method is especially improved for snubber circuits that are subjected to high thermal stress caused by high-frequency ripple currents carried by the snubber. The thermal properties of snubber circuits are carefully evaluated in the system using fast-switching SiC devices and operating at elevated ambient temperatures.

Finally, a hardware prototype with SiC power modules has been built and tested at 60 kW continuous power and 100 kW for 20 seconds at 105 °C ambient temperature and 65 °C inlet coolant temperature to verify the proposed inverter system.

The rest of the paper is organized as follows. The inverter component selection and their arrangement to achieve high power density are discussed in Section II. The design and optimization of the snubber circuit are presented in Section III. The design of a high-temperature gate driver for SiC power modules is presented in Section IV, and the overall system layout in Section V. The system thermal modeling and design are discussed in Section VI. The theoretical findings are verified using a laboratory prototype of the inverter, as presented in Section VII, and Section VIII concludes the paper.

II. THE SYSTEM REQUIREMENTS AND COMPONENT SELECTION

The basic requirements for the inverter presented in this paper are listed in Table I.

The inverter is required to operate at 105 °C ambient temperature and should be capable of delivering 60 kW continuously and 100 kW for 20 seconds. By using a conventional 65 °C coolant, the developed inverter can be easily implemented in most existing hybrid electric vehicles (HEVs) without any modification to the vehicle cooling system. The 40 kHz switching frequency was selected to support the use of

high power density electrical machines with higher rotational speeds and lower inductances while minimizing the loss-producing harmonies components in the resulting current waveform [18].

A. Power Semiconductors

During the steady-state operation, the RMS current values of all six switches are the same when conventional symmetric modulation schemes are applied. Ignoring deadtime and influences from the parasitics in the system, the RMS current of each switch can be expressed as

$$I_{\mathrm{s,rms}} = \frac{I_{\mathrm{ph,rms}}}{\sqrt{2}}. \tag{1}$$

The relationship between the real output power P_{out} of the three-phase inverter and RMS phase current I_{ph} is

$$P_{\mathrm{out}} = 3 \cdot V_{\mathrm{ph,rms}} \cdot I_{\mathrm{ph,rms}} \cdot \cos\theta, \tag{2}$$

where $V_{\mathrm{ph,rms}}$ denotes the RMS value of the output phase voltage and $\cos\theta$ represents the power factor. Conventionally, space-vector control or pulse width modulation with third harmonic injection achieves a maximum modulation index, $m_{\max} = 2/\sqrt{3}$ without overmodulation. Therefore, the maximum phase voltage will be

$$V_{\mathrm{ph,rms}} = m_{\max} \cdot \frac{V_{\mathrm{dc}}}{2\sqrt{2}} = \frac{V_{\mathrm{dc}}}{\sqrt{6}}, \tag{3}$$

where V_{dc} refers to the input dc-link voltage of the inverter.

To supply the peak 100 kW output power at 400 V dc-link voltage, a minimum phase current $I_{\mathrm{ph,rms,min}}$ is calculated as well as minimum switch current $I_{\mathrm{s,rms,min}}$:

$$I_{\mathrm{ph,rms,min}} = \frac{\sqrt{2}P_{\mathrm{out}}}{\sqrt{3}V_{\mathrm{dc}}\cos\theta} = 240\ \mathrm{A}, \tag{4}$$

$$I_{\mathrm{s,rms,min}} = \frac{P_{\mathrm{out}}}{\sqrt{3}V_{\mathrm{dc}}\cos\theta} = 170\ \mathrm{A}, \tag{5}$$

with $\cos\theta = 0.85$ based on the requirement for a conventional high-speed permanent magnet synchronous (PMSM) machine [4].

Considering the high current requirement at peak power, the discrete power semiconductor devices are not preferred in this design because of their low current capability per device and the potential complexities of connecting several devices in parallel.

The SiC half-bridge module CAS325M12HM2 from Wolfspeed was selected for the system because of its high current capability, low-profile design, and low module parasitic inductance. Each 3.6 mΩ MOSFET in the module is made with seven 25 mΩ 1200 V MOSFET dies in parallel, with six 1200 V SiC Schottky barrier diode dies in parallel, which results in 256 A continuous drain current capability for each switch at case temperature of 125 °C and junction temperature of 175 °C.

B. Dc-Link Capacitors

The dc-link capacitors are selected based on the required capacitance, rated dc voltage, maximum allowable current ripple, and maximum allowable operating temperature.

Ceramic capacitors typically have very low equivalent series resistance (ESR) and equivalent series inductance (ESL), which are required by the application. However, these capacitors have very low capacitance per device due to their thick dielectric (paraelectric), leading to a high number of capacitors required to achieve the needed capacitance. Stacking many capacitors in parallel can significantly increase the system cost and can potentially reduce the reliability due to possible cracks induced by the thermal stress of these capacitors.

The ESR and ESL of the electrolytic capacitors are usually significantly higher than those of ceramic capacitors or film capacitors, which will reduce their filtering capability at high frequencies when used as dc-link capacitors and cause higher power losses. In addition, if electrolytic capacitors are selected, the system lifetime could be significantly reduced at elevated temperatures.

The film capacitors have a long lifetime, high capacitance per device, and low ESR and ESL due to their inherent geometry. Sigma Technologies, Delphi, and GE are currently developing film capacitors capable of up to 140 °C temperature operation [19]. Meanwhile, 200 °C capacitors are enabled based on polyphenylene sulfide (PPS) torelina film [20]. However, all these capacitors are still in development and not available on the market.

On the other hand, Panasonic and TDK EPCOS provide automotive-grade packaged film capacitors, which can be operated at 105 °C ambient temperature continuously. However, these capacitors are usually optimized for low switching frequency (5–10 kHz) inverters and have much higher capacitance than required, which results in a large volume of the capacitor bank. In addition, the capacitors packaged in one capacitor bank are not feasible for very compact designs, where a special capacitor shape is desired to minimize the overall inverter volume. Therefore, using discrete film capacitors instead of prepackaged capacitor banks can significantly increase the power density of the designed inverter.

Finally, the TDK B32776P metalized polypropylene dc-link film capacitors for 125 °C operations are selected for this inverter system because of their relatively high capacitance, good self-healing properties, low losses with high current capability, and high reliability [21]. The RMS value of the total capacitor current, $I_{\mathrm{rms,cap}}$, which is the most critical parameter for this application, can be calculated as

$$I_{\mathrm{rms,cap}} = \frac{\sqrt{2}P_{\mathrm{out}}}{\sqrt{3}V_{\mathrm{dc}}\cos\theta}\sqrt{2m\left[\frac{\sqrt{3}}{4\pi} + \left(\frac{\sqrt{3}}{\pi} - \frac{9m}{16}\right)\cos^2\theta\right]} = 142.73\ \mathrm{A}, \tag{6}$$

where m is the PWM modulation index and $\cos\theta$ is the power factor of the electric machine [22]. For $\cos\theta = 0.85$, $m = 0.66$, sixteen 12 μF/700 V capacitors B32776P7126K000 in parallel,

with a total capacitance of 192 μF, a continuous operating voltage of 600 V at 105 °C, and a total ripple current capability of 143 A at 105 °C are selected. The ESR of each capacitor is approximately 5.3 mΩ and it is almost constant for frequencies higher than 10 kHz. The total volume of the selected capacitors is approximately 0.55 L.

The temperature rise of the selected capacitors due to the ESR losses can derate the ripple current capability and cause the capacitor failure. Therefore, the maximum temperature rise needs to be determined before using the capacitors in the system. The dissipated power, P_{dis} (mW) is

$$P_{dis} = ESR \cdot \left(\frac{I_{rms,cap}}{16} \right)^2 = 422 \text{ mW}. \quad (7)$$

The temperature rise is defined with equivalent heat coefficient G = 58 mW/°C, which is related to the capacitor package.

$$\Delta T = \frac{P_{dis}}{G} = 7.28 \text{ °C} \quad (8)$$

Due to the derating at high temperature, the maximum allowed temperature rise is calculated as

$$\Delta T_{max} = \lambda^2 \cdot \Delta T_{85\,°C} = 7.35 \text{ °C}, \quad (9)$$

where λ = 0.7 for 105 °C operations and $\Delta T_{85\,°C}$ = 15 °C [21]. Based on this result, the capacitors can safely operate at 105 °C for 100 kW with no extra cooling required.

C. Busbar Design

The typical busbar system for a three-phase inverter system comprises a dc busbar and an ac busbar. The dc busbar connects the EV battery to the dc-link capacitors and then to the power semiconductor devices, while the ac busbar carries the output ac current from the power semiconductor devices to the electric motor. The minimum current of the ac busbar is already determined by (4) as $I_{busbar,ac} = I_{ph,rms}$ = 240 A, and the current of the dc busbar is determined by (5) as $I_{busbar,dc} = I_{s,rms}$ = 170 A. Considering these high current-carrying requirements and the required wide operating temperature range from −40 °C to 105 °C, the copper sheet busbar is preferred over the multilayer PCB approach in this case. Since the high-frequency snubber circuit and gate drivers need to be mounted above the power modules, the dc-link capacitors can be placed beside the module and the cold plate. This arrangement requires two horizontal copper sheets for the dc busbar, as illustrated in Fig. 1.

To optimally utilize the available space, both the dc input interface and ac output interface are arranged on the same side of the dc-link capacitors. Both the dc and the ac busbar must be machined and bent to the desired shape. The thickness of the ac and dc busbar is 4.76 mm and 2.36 mm, respectively, resulting in a total busbar volume of approximately 0.16 L.

The dc busbar loop inductance was first estimated by

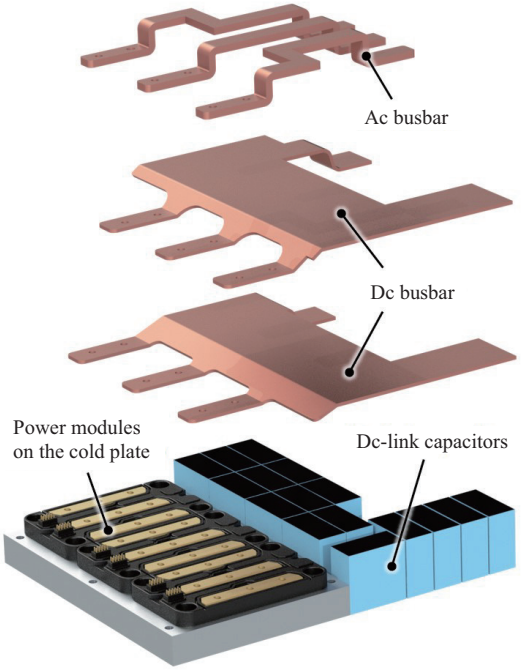

Fig. 1. Exploded view of the busbar system, power modules, and the cold plate.

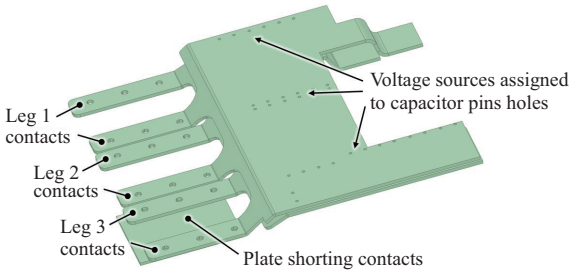

Fig. 2. The dc busbar geometry is simulated in the Q3D extractor.

simulations in Ansys Q3D Extractor and then verified using transient switching waveforms from double-pulse tests. For the Q3D Extractor simulations, the copper contacts on the module side were shorted with a copper plate and voltage sources and sinks are assigned to the holes for the capacitor pins on the top and the bottom plate, respectfully, as illustrated in Fig. 2.

The loop inductance test results are summarized in Table II. One of the drawbacks of the laminated busbars (both with copper sheets and the PCB-based ones) is their asymmetry, as illustrated in Table II. Namely, different devices (modules) "see" different current commutation loop inductances. This causes slightly different switching behavior of different power devices (modules) in the inverter.

The obtained loop inductance values are typical for this type of busbar and are acceptable for the inverters based on Si IGBTs. If SiC MOSFETs are used, the loop inductance of more than 20 nH is unacceptable and will cause significant overvoltage spikes during the MOSFET turn-off transient, as illustrated by the double-pulse test waveforms in Fig. 3. Therefore, a local snubber circuit needs to be used to reduce these spikes

TABLE II
THE LOOP INDUCTANCE TEST RESULTS

Leg	Q3D simulation /nH	Double-pulse test /nH
Leg 1	23.3	26
Leg 2	25.4	28
Leg 3	26.5	29

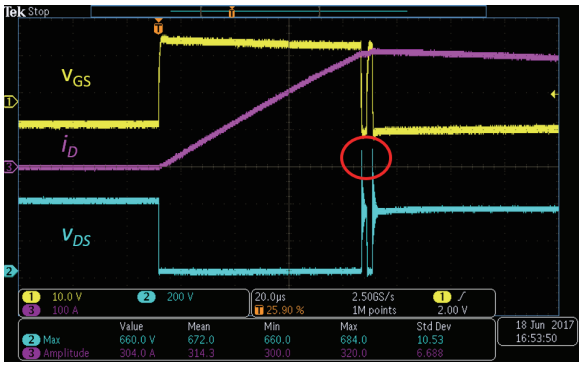

Fig. 3. Overvoltage spike of 684 V (75% overshot) at 300 A drain current and a dc-link voltage of 390 V: (yellow) gate-source voltage, (magenta) drain current, (cyan) drain-source voltage.

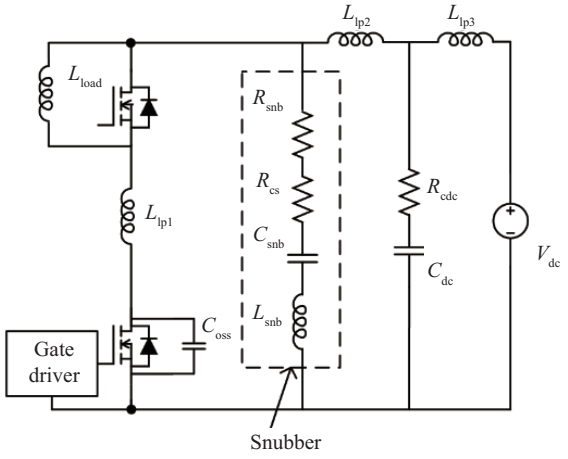

Fig. 4. Circuit diagram of a double-pulse circuit with decoupling snubber circuit.

when SiC MOSFETs are used as power semiconductor devices.

III. SNUBBER DESIGN

Fig. 4 shows a circuit diagram of a double-pulse-test setup with a decoupling snubber circuit, which is used to evaluate the performance of different snubber circuit designs. The gate driver provides necessary double pulse gating signals to the bottom switch. The load inductor L_{load} provides initial drain-source current, I_0. The L_{lp1} represents the total loop stray inductance of the device package and the connections to the snubber circuit. L_{lp2} represents the total stray loop inductance from the snubber circuit to the bulk dc-link capacitors (R_{cdc} and C_{dc}), while L_{lp3} refers to the total stray loop inductance from bulk dc-link capacitors to the dc source, V_{dc}. The ESR

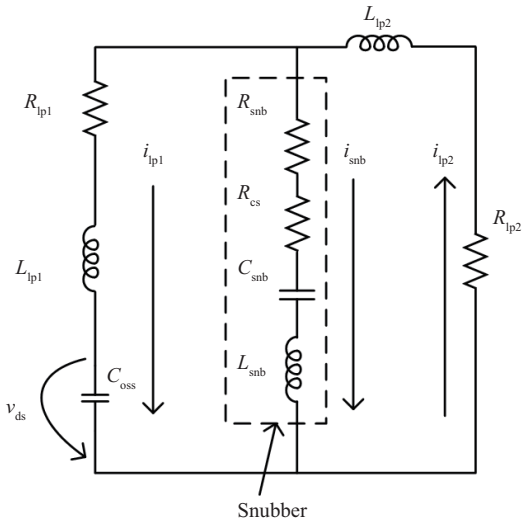

Fig. 5. High-frequency equivalent circuit of the double pulse test circuit.

of the decoupling capacitor, R_{cs}, models the power dissipation in the capacitor. The output capacitor of the device, C_{oss}, will be treated as a constant value during the transient because it usually becomes saturated and less sensitive to the drain-source voltage at high bias voltage. The R_{snb} represents the extra resistor of the snubber circuit and will be regarded as zero when only a capacitor, C_{snb}, is applied in the snubber circuit. The derived high-frequency equivalent circuit of the double pulse circuit is shown in Fig. 5, where the load inductor is treated as an open circuit due to its significantly higher inductance compared to the other loop inductances. The bulk dc-link capacitor is treated as a short circuit due to its significantly higher capacitance compared to the other capacitances in the circuit, and the dc source loop is neglected because its loop inductance L_{lp3} is significantly higher than the other two loop inductances in the circuit. In addition, the R_{lp1} is introduced to represent the loop resistance from the device to the snubber circuit (and it is mostly coming from the upper-side diode), and the R_{lp2} is introduced to represent the loop resistance from the snubber circuit to dc-link capacitors.

The equations in the time domain are then derived to describe this high-frequency equivalent circuit, and finally, their *s*-domain representations (10) to (13) are derived by using Laplace transform. The V_{ds} (s) is obtained by solving (10) to (13) and expressed as (14), where the denominator D(s) is a fourth-order expression shown in (15).

$$I_{lp2}(s) = I_{lp1}(s) + I_{snb}(s) \tag{10}$$

$$V_{ds} = I_{lp1} / (sC_{oss}) \tag{11}$$

$$V_{ds}(s) = (R_{snb} + R_{cs}) I_{snb}(s) + I_{snb}(s) / (sC_{snb}) + sL_{snb} I_{snb}(s) - L_{lp1}[sI_{lp1}(s) - I_0] - R_{lp1} I_{lp1}(s) \tag{12}$$

$$V_{ds}(s) = -R_{lp2} I_{lp2}(s) - L_{lp2}[sI_{lp2}(s) - I_0] - L_{lp1}[sI_{lp1}(s) - I_0] - R_{lp1} I_{lp1}(s) \tag{13}$$

TABLE III
KEY PARAMETERS EXTRACTED FROM A 100 KW TRACTION INVERTER PROTOTYPE

Description	Value	Description	Value
L_{lp1}	6 nH	R_{lp1}	50 mΩ
L_{lp2}	19 nH	R_{lp2}	50 mΩ
L_{snb}	0.1 nH	R_{cs}	50 mΩ
I_0	400 A	C_{oss}	2 nF

$$V_{ds}(s) = N(s)/D(s) \tag{14}$$

$$\begin{cases} D(s) = a\cdot s^4 + b\cdot s^3 + c\cdot s^2 + d\cdot s + 1 \\ a = C_{oss}C_{snb}L_{snb}L_{lp1} + C_{oss}C_{snb}L_{lp2}L_{snb} + C_{oss}C_{snb}L_{lp2}L_{lp1} \\ b = (R_{snb}+R_{cs})C_{oss}C_{snb}L_{lp1} + R_{lp2}C_{oss}C_{snb}L_{snb} + \\ \quad R_{lp2}C_{oss}C_{snb}L_{lp1} + R_{lp2}C_sC_{snb}L_{lp2} \\ c = C_{snb}L_{snb} + C_{oss}L_{lp1} + C_{snb}L_{lp2} + C_sL_{lp2} + \\ \quad C_sC_{snb}R_{bulk}(R_{snb}+R_{cs}) \\ d = C_{snb}(R_{snb}+R_{cs}) + C_{snb}R_{bulk} + C_sR_{bulk} \end{cases} \tag{15}$$

Table III lists the parameters of the double pulse test circuit based on the proposed busbar design. By importing the parameters into (10) to (13) and sweeping the snubber resistance, we can evaluate the performance of the snubber circuit.

The snubber capacitance is first selected to be 100 times higher than the C_{oss} value to obtain the best voltage spike suppression performance since the snubber will absorb the majority of the energy and very little energy will be transferred to the device output capacitance [23]. Due to the small value of Coss in most conventional SiC devices, it is usually affordable to implement such a snubber capacitor in terms of both cost and space in the system. Therefore, the 200 nF snubber capacitor is found to be a good compromise between the performance and the cost/space requirements for this application.

The relationship between a voltage spike and the snubber resistance is illustrated in the top plot of Fig. 6, where the percentage is calculated by comparing the voltage spike with the snubber circuit to the voltage spike without any snubber circuit. For example, 35% voltage spike reduction (65% of the voltage spike without snubber) can be obtained with 0.1 Ω snubber resistance. The bottom plot shows the energy dissipated in the snubber capacitor E_{rcs} and the energy dissipated on the snubber resistor E_{rsnb} under different snubber resistance. The graphs reveal that larger snubber resistance results in lower power dissipation in the snubber capacitor but it also reduces the suppression of the overvoltage spike. The optimal region is where the snubber resistance can satisfy both the overvoltage spike suppression and the snubber loss reduction requirements. In our case, the optimization targets are more than 15% overvoltage spike reduction and less than 1 W loss on the snubber capacitor. This region is highlighted in the plot and C_{snb} = 200 nF and R_{snb} = 4.7 Ω are selected as final values for the snubber. The detailed optimization procedure

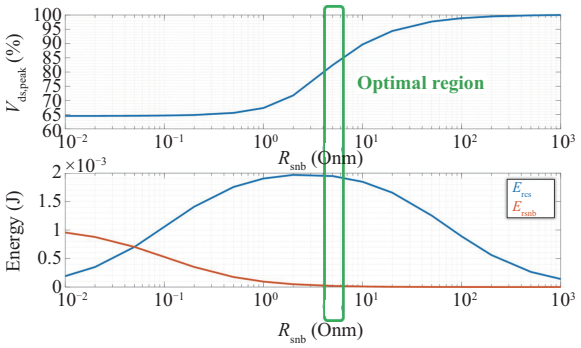

Fig. 6. Top plot: overvoltage spike in the percentage of voltage spike without snubber circuit vs. added snubber resistance R_{snb}. Bottom plot: (red trace) energy dissipated in the snubber capacitor, (blue trace) energy dissipated in the snubber resistor, versus added snubber resistance R_{snb}.

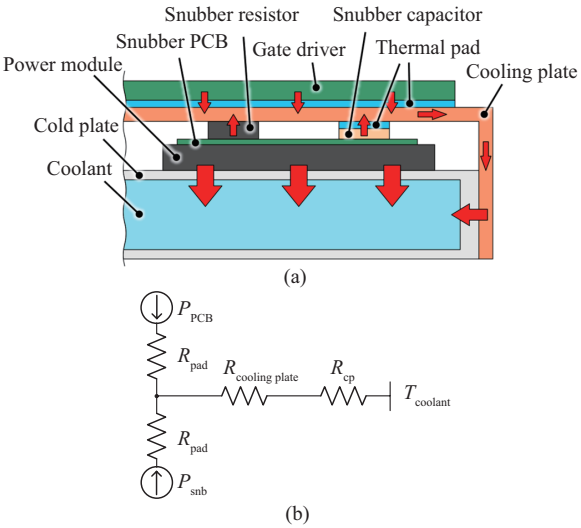

Fig. 7. (a) Heat flow through the copper cooling plate and (b) the equivalent thermal circuit.

can be found in [23].

With this snubber, the voltage spike has been suppressed to 568 V at 400 V dc-link voltage and 380 A output peak current. To keep the temperature of the snubber components at the acceptable level when the inverter operates at full power, an additional copper cooling plate that has a good thermal connection with the cold plate is installed, as illustrated in Fig. 7(a). This copper plate serves as a heat pipe and helps to cool the gate driver board as well. The equivalent thermal circuit is illustrated in Fig. 7(b), where P_{PCB} represents the lumped loss from the gate driver PCB, such as gate driver chip and power supply, and P_{snb} is the loss from the snubber circuit. With the cooling plate installed, the measured temperature of the snubber capacitors and resistors was less than 110 °C at 105 °C ambient at full output power.

IV. HIGH-TEMPERATURE GATE DRIVER

The prototype of the realized high-temperature gate driver is shown in Fig. 8. The required voltage potentials for protection

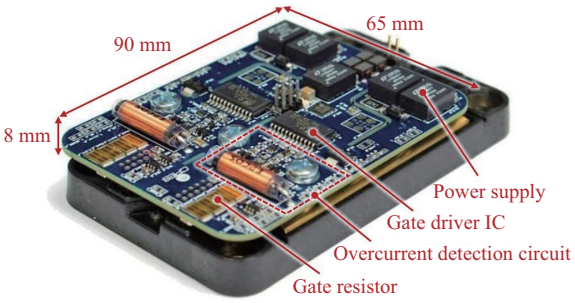

Fig. 8. The prototype of the high-temperature gate driver is assembled with the MOSFET module.

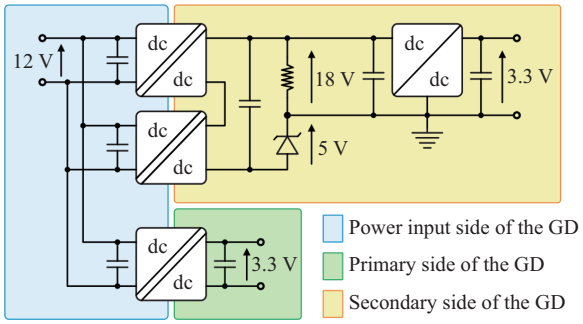

Fig. 9. The high-temperature gate driver power supply architecture.

are introduced to the gate driver via spacers and screws between the gate driver and busbar of the MOSFET module. Therefore, no cable connections are required, which simplifies the assembly procedure. The design and analysis of the most important functional blocks of the high-temperature gate driver are given in the following paragraphs.

A. Gate Driver Power Supply

The architecture of the power supplies of the developed gate driver is shown in Fig. 9. The gate driver is supplied by a 12 V external source. For the primary side of the gate driver, an isolated 3.3 V is generated to power the MCU and gate driver IC. For the secondary side, 18 V / −5 V driving voltages are generated by two isolated power supplies in an input-parallel-output-series (IPOS) connection. Also, 3.3 V is generated by a non-isolated dc/dc converter from +18 V to provide power for the overcurrent detection circuit. This isolation structure protects the primary side driving signals from being polluted by the secondary side high dv/dt switching node.

For the proposed gate driver, the main isolated power supplies are used to generate 23 V from the input. After that, a Zener diode is used to generate a stable negative voltage. The input voltage, output voltage, output power, efficiency, and size are the basic requirements that should be met for the proper design of the isolated dc/dc converter. In addition, the isolation capacitance of the converter should also be small enough to limit the common mode current generated by the high dv/dt switching node. The LTM8067 is selected as the isolated power supply because of the following reasons.

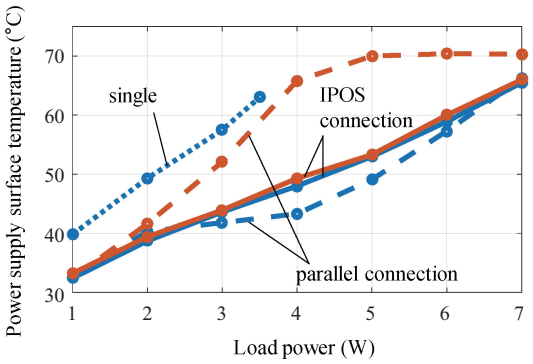

Fig. 10. Power supply surface temperature under different load power and different connections.

First, it has a significantly higher power density compared to the other isolated dc/dc converters with similar power and isolation voltage levels, which enables a low-profile, compact gate driver design. Second, its maximum allowed internal operating temperature is 125 °C, which enables the high-temperature operation of the gate driver. Third, the power supply has adjustable output voltage which could be tuned by changing the feedback resistor. Being able to adjust the output voltage helps the power supply to have good scalability. Direct paralleling of converters for higher power levels can cause the current imbalance problem. However, if the output voltage is adjustable, the power supplies can be connected in IPOS connection so that there will be no current sharing problem. This is especially useful considering an application with a higher power or higher ambient temperature where the power capability of the converter is derated. Fig. 10 shows the surface temperature of the converter measured by thermocouple with load power increasing in three different cases: single power supply, two power supplies in parallel, and two power supplies in IPOS connection. From the test result, IPOS has a much better current balancing compared to parallel-connected structures and has a much lower temperature increase compared to the single power supply under the same load. Therefore, the IPOS connection can help the dc/dc converter to operate under high temperatures.

B. Overcurrent Protection Circuit

The protection circuit design is another critical part of the gate driver because of the high cost of power modules and safety considerations. An overcurrent detection scheme based on the parasitic inductance of the SiC MOSFET power module is shown in Fig. 11, [24]. Assuming the impedance of the R_s and C_s branch is much higher than the impedance of the parasitic inductance branch, the transfer function from the switching current i_d to the voltage v_o across the capacitor C_s will be

$$G(s)=\frac{-v_o(s)}{i_d(s)}=\frac{L_p\cdot s}{R_sC_s\cdot s+1}=\frac{L_p}{R_sC_s}\cdot\frac{R_sC_s\cdot s}{R_sC_s\cdot s+1}\approx\frac{L_p}{R_sC_s}, \tag{16}$$

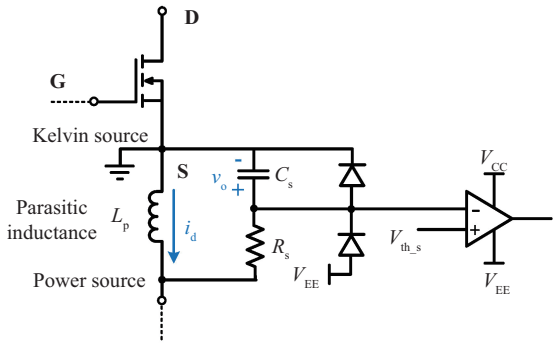

Fig. 11. Short-circuit detection scheme based on utilizing parasitic inductance of the SiC MOSFET module.

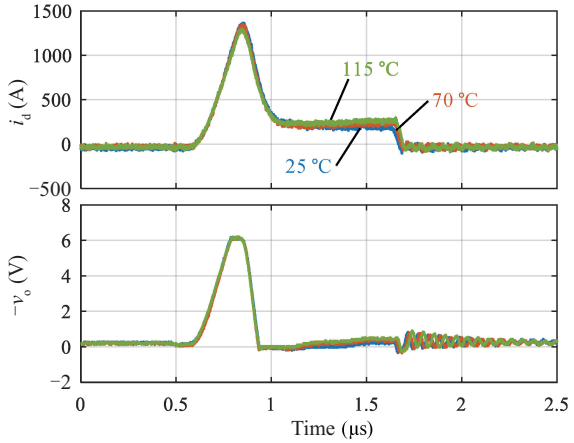

Fig. 12. Short-circuit current i_d and its detection voltage $-v_o$ under different junction temperatures.

which means that the switch current i_d is in direct proportion with signal v_o. As shown in Fig. 12, the short-circuit (both top and bottom switches are ON) starts from 0.6 μs and the proposed protection circuit eliminates the short-circuit current within a duration of 1.1 μs. In addition, the protection circuit has low thermal sensitivity which helps the protection to be operational even at high operating temperatures. During the short-circuit, the detection signal v_o of the short-circuit current i_d is invariable under different module temperatures. In the end, it should also be noted that the labeled tolerance of components is much smaller than the end-of-life tolerance. The tolerance can come from the assembly, storage, moisture, thermal drift, etc. The worst-case analysis is therefore important to make sure the circuit can still operate under the worst-case conditions from components tolerance perspective. Assuming n% tolerance of R_s and C_s, the detected current will have the worst-case tolerance of approximately 2n% (valid for tolerance within 10%) which is acceptable for short-circuit detection. After adding a filter inductor, the circuit can also be used to detect overload fault without being disturbed by transient overshoot during turn-on and turn-off events. The details of the protection circuit and its design process are explained in [24].

The capacitor C_s in the overcurrent detection circuit should be a class I capacitor with ultra-stable C0G/NP0 class I dielectric

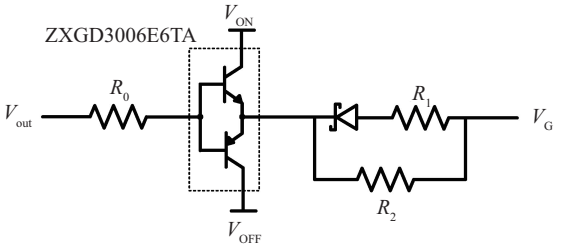

Fig. 13. Current booster and gate resistors.

to ensure reliable operation at a wide operating temperature range. For the diodes in the driver circuits, the leakage current of reverse biased diodes operating at a high temperature can be significantly higher than that at room temperature, which needs to be taken into account when diode power losses are calculated.

C. Gate Driver IC

The STGAP1AS is selected to be the main driver IC of the gate driver board. As an isolated gate driver IC, it has functionalities of UVLO, OVLO, soft turn-off (two-level-turn-off), and active Miller clamp. STM32L052K8U3TR is used as the MCU to program the gate driver IC through the JTAG connection. The MCU helps to set proper UVLO, OVLO voltage levels, protection threshold voltage, and enable soft turn-off, etc. Both the gate driver IC and the MCU can work under the ambient temperature from −40 °C to 125 °C which meets the high-temperature requirement of the gate driver.

D. Current Booster and Gate Resistor

Current boosters and gate resistors between the output of the gate driver IC V_{out} and the driving voltage V_G are shown in Fig. 13. The gate driver IC has a 5 A gate driving capability which cannot drive the MOSFET fast enough to minimize the switching loss. Therefore, current boosters are implemented to increase the gate driving capability. Current booster chip ZXGD3006E6TA works as a bipolar transistor, which has low voltage drop and thus low power losses. Each current booster can supply a maximum of 10 A driving current. Based on the required driving current (determined by different switching speeds), different numbers of current boosters can be implemented in parallel to increase the driving capability. The gate resistor structure includes a Schottky diode, a turn-on resistor, and a turn-off resistor. The diode is conducting only during turn-off. Therefore, the equivalent turn-on resistor is R_2 while the turn-off resistor is $R_1 \| R_2$. A smaller turn-off resistor can help the driving system to achieve a higher turn-off speed.

The current booster chip can work under the ambient temperature of −55 °C to 155 °C which meets the temperature requirement. For the gate resistor under high temperature, the power loss can be roughly estimated as

$$P_{loss} = Q_G \cdot V_{GS} \cdot f_{sw}, \tag{17}$$

where Q_G is the gate charge, V_{GS} is the gate driving voltage, and

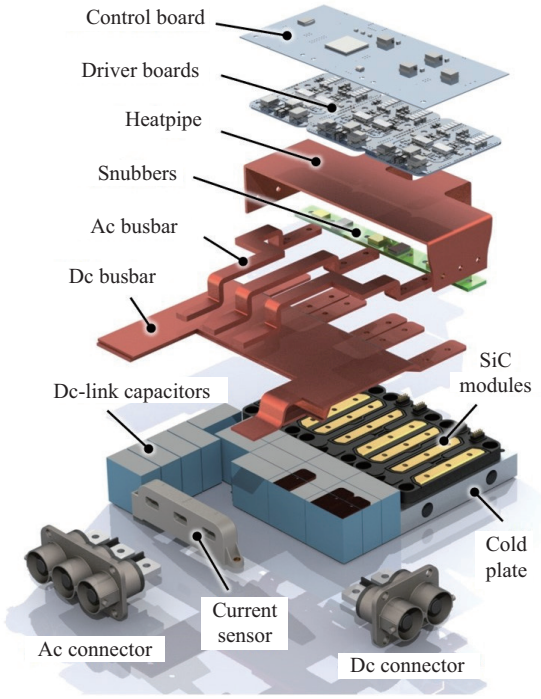

Fig. 14. Exploded view of the proposed inverter.

f_{sw} is the switching frequency. The resistor's power derating at high ambient temperature also needs to be taken into account. For example, if the allowed resistor power dissipation at 105 °C is 40% of the power rating, the power rating should be selected to be 2.5 times the gate resistor loss so that the gate resistor can safely operate at 105 °C.

V. System Layout

The inverter layout is illustrated in Fig. 14. Unlike the inverter systems with the PCB busbars, where the current sensors are compact and typically soldered directly on the PCB, the system with the copper busbar usually comes with bulky panel-mounting current sensors for three-phase current measurement. This can substantially increase the overall inverter volume, which is not acceptable in automotive applications. The requirement for high-current measurements at high ambient temperature is another obstacle when it comes to selecting the current sensors. The sensors need to be rated for high-temperature operation and need to be qualified for automotive applications. An AEC-Q100 qualified HAH3DR 700-S03/SP2 current sensor from LEM is finally selected for this application because of its capability to operate up to 125 °C, measuring range up to 700 A, and very compact design for sensing three-phase currents with a single unit. This open-loop Hall effect transducer has 98% accuracy and a frequency bandwidth of 40 kHz. The total volume of the selected current sensor is 0.05 L.

The Amphenol Industrial PowerLok Series connectors are selected as input and output power connectors, because of their compact design, easy busbar-type mounting, up to 500 A continuous current ability (300 A version is used in this application), 1000 V rated voltage, and up to 125 °C temperature operation. The total volume of the selected power connectors is 0.2 L. By arranging the dc-link capacitors in a specific shape, the current sensor and power connectors can be placed close to the output connector, while keeping the total design as compact as possible, as illustrated in Fig. 15.

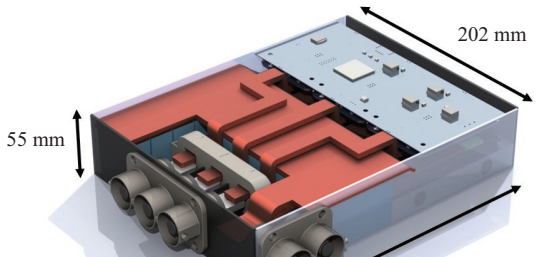

Fig. 15. Compact inverter design with a total volume of 2.9 L.

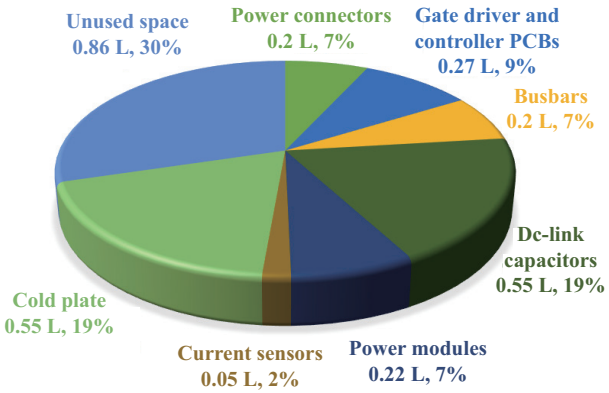

Fig. 16. Inverter volume distribution by subsystems.

The final inverter volume distribution is shown in Fig. 16. The selected dc-link capacitors take only 19% of the total volume and the proposed arrangement leads to only 30% of unused space, which is significantly lower than 67% in the case of the inverter from [5]. When operating at peak 100 kW output power, the power density exceeds 34 kW/L.

VI. System Thermal Modeling and Performance Analysis

The design of the power electronic converter system should ensure that the power device junction temperature never exceeds the preset limit during the converter operation. In other words, the thermal operating points of the system should be designed to be in a safe and optimum range, which is mainly determined by the power losses in the power semiconductor devices and the properties of the cooling system. A comprehensive system thermal model is required to determine the total losses in the system, the cooling system requirements to achieve target power, and to be able to predict the system thermal performance.

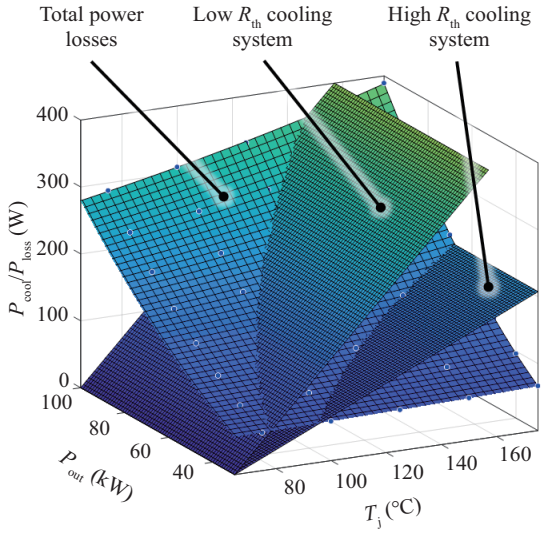

Fig. 17. The possible thermal operating points are defined by the intersection of the power losses surface (the curved surface) and the cooling system characteristics (the flat surfaces).

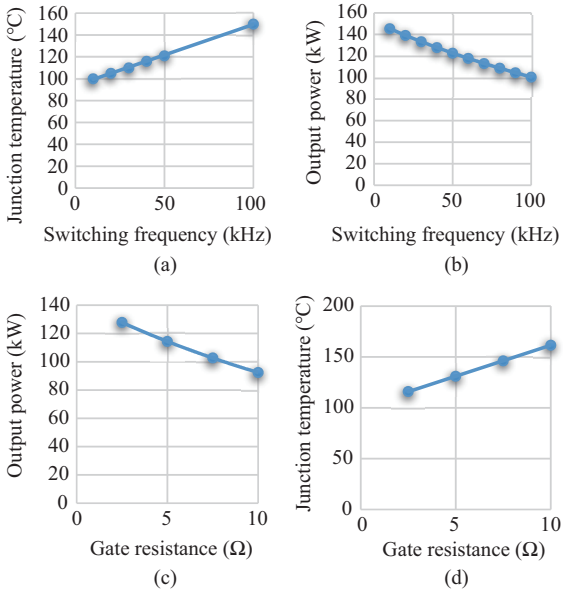

Fig. 18. Design parameters relationships based on the proposed thermal model: (a) T_j vs. f_{sw} given P_{out} = 100 kW and R_g = 2.5 Ω. (b) P_{out} vs. f_{sw} given T_j = 150 °C and R_g = 2.5 Ω. (c) P_{out} vs. R_g given T_j = 150 °C and f_{sw} = 40 kHz. (d) T_j vs. R_g given P_{out} = 100 kW and f_{sw} = 40 kHz.

A. Inverter Thermal Model

The majority of power losses in the inverter system occur in power semiconductor devices and can be divided into switching losses which occur during the switching transients and practically do not depend on the device junction temperature and the conduction losses which are highly dependent on the junction temperature.

The selected MOSFETs module power losses characterization is obtained from the double pulse test and conduction losses test. The double pulse test is performed with the proposed busbar layout to obtain the actual switching losses in the real prototype. In the conduction losses test, the selected module is placed in the thermal chamber and the $R_{ds,on}$ is measured at different junction temperatures. Based on these results, a thermal model of the MOSFETs is created in PLECS to simulate the inverter power losses.

The simulations have been done at output power ranging from 30 kW to 100 kW, and junction temperature ranging from 25 °C to 175 °C, with a fixed switching frequency of 40 kHz. The results are imported into MATLAB and presented as a power losses surface by applying MATLAB's polynomial curve fitting tool. The cooling system performance can be illustrated in the same coordinate system by a flat surface, as illustrated in Fig. 17. The two flat surfaces in Fig. 17 correspond to two different total thermal resistances at the same coolant temperature. The intersection of cooling power surface and power losses surface defines the possible thermal operating points. The intersection shows that a better cooling system corresponds to lower junction temperature at the same output power or higher output power at the same junction temperature.

The inverter power losses P_{loss}, which are defined as a function of junction temperature T_j, output power $P_{out,}$ and switching frequency f_{sw}, are equal to the sum of conduction losses and switching losses (18). On the other hand, cooling power P_{cool} can be defined as a function of junction temperature, input coolant temperature $T_{coolant}$ (ambient temperature for an air-cooled system), and total thermal resistance $R_{th,total}$ (19). These two powers are the same in the steady-state and the junction temperature can be determined from (20) when the coolant temperature and the total thermal resistance are known.

$$P_{loss}\left(T_j, P_{out}, f_{sw}\right) = P_{switching}\left(T_j, P_{out}, f_{sw}\right) + P_{conduction}\left(T_j, P_{out}, f_{sw}\right) \quad (18)$$

$$P_{cool} = \left(T_j - T_{coolant}\right) / R_{th,total} \quad (19)$$

$$P_{cool}\left(T_j, T_{coolant}, R_{th,totoal}\right) = P_{loss}\left(T_j, P_{out}, f_{sw}\right) \quad (20)$$

By applying polynomial curve fitting in MATLAB, the power losses function P_{loss} can be fitted as a polynomial function, where junction temperature T_j, output power P_{out} and switching frequency f_{sw} are variables.

Assuming $R_{th,total}$ = 0.15 °C/W and $T_{coolant}$ = 65 °C are given in the system, various relationships between other design parameters are analyzed according to (18) to (20) and some important results are illustrated in Fig. 18. As can be seen in Fig. 18(a), the junction temperature increases from 100 °C to 150 °C when the switching frequency is increased from 10 kHz to 100 kHz, given P_{out} = 100 kW and R_g = 2.5 Ω, which reveals the maximum allowable switching frequency is 100 kHz under this condition. The maximum output power is decreasing when the switching frequency increases, as illustrated in Fig. 18(b). Increasing the gate resistance R_g can either reduce the maximum power or increase the junction temperature by increasing the switching losses, as shown in Fig. 18(c) and (d), respectively.

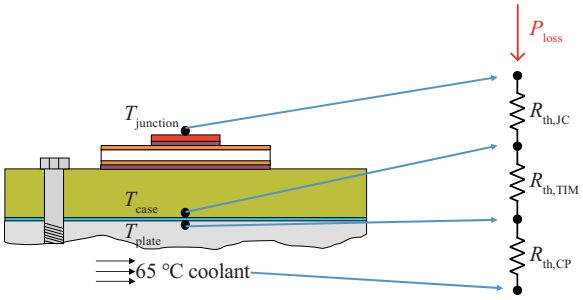

Fig. 19. A practical inverter thermal model.

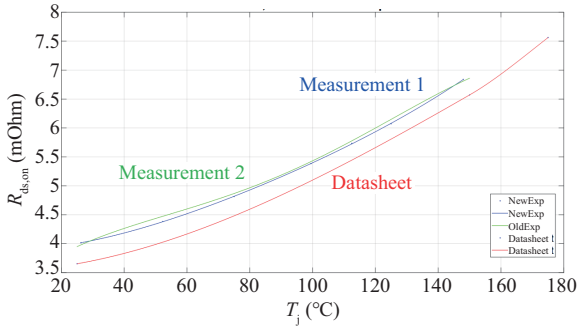

Fig. 20. MOSFETs module $R_{ds,on}$ at different junction temperature (green and blue curves are two measurements results while red curve comes from datasheet).

Similarly, to keep the junction temperature below 150 °C (having 25 °C margin), the maximum allowable total thermal resistance from junction to the coolant is determined to be 0.23 °C/W to achieve 100 kW output power at $R_g = 2.5\ \Omega$ and $T_{coolant} = 65$ °C.

1) Thermal Interface Material Considerations

A practical thermal model of the inverter is illustrated in Fig. 19. The total thermal resistance is the sum of MOSFETs junction-to-case thermal resistance $R_{th,jc}$, thermal interface material (TIM) thermal resistance $R_{th,TIM}$, and cold plate thermal resistance $R_{th,cp}$ (21). Since the junction-to-case resistance is given by the module package, it is important to carefully test and select the optimal TIM and the cold plate to achieve the required total thermal resistance of 0.23 °C/W.

$$R_{th,total} = R_{th,jc} + R_{th,TIM} + R_{th,cp} \quad (21)$$

The TIM is tested and selected based on the following procedure. First, the $R_{ds,on}$ of a specified module (CAS325M 12HM2 from Wolfspeed) is measured at different temperatures (ranging from 25 °C to 150 °C) to obtain the relationship between the conduction resistance and junction temperature, as illustrated in Fig. 20.

The measured resistance is about 0.3 mΩ higher than the curve from the module datasheet (red curve), which is mainly because the measured resistance includes connection resistance on the module level, whereas the datasheet provides only the resistance on the chip (die) level. Second, the characterized

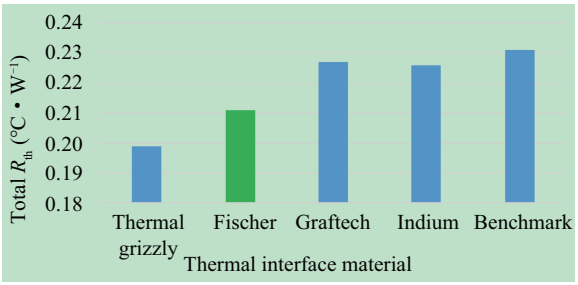

Fig. 21. Total thermal resistance in the test setup with forced-air heatsink for different thermal interface materials

module is placed on a cold plate or a heatsink if a liquid cooling system is not available and conducts sufficient dc current, e.g., 300 A for the selected module to generate substantial conduction losses. The drain-source voltage is then measured in the steady-state condition (after reaching thermal equilibrium). Finally, the total thermal resistance can be evaluated using (22), where I_D represents the drain-source current (300 A), P_{loss} is the total conduction losses and the junction temperature T_j can be found based on the relationship in Fig. 20. Because the other two thermal resistances are constant, the smaller the total thermal resistance is, the better the TIM is.

$$R_{th,i} = \left(T_{j,i} - T_a\right) \Big/ P_{loss,i},\ P_{loss,i} = V_{ds,i} \cdot I_D = R_{ds,on,i} \cdot I_D^{\,2} \quad (22)$$

Thermal Grizzly Kryonaut, Fischer WLPK, Graftech HT-C3200, and Indium Heat-Spring are selected to be the TIM candidates due to their high thermal conductivity and availability in the market. Wakefield 126 thermal grease is used as a Benchmark TIM. The proposed thermal resistance test was performed with a heatsink as the liquid cooling system was not available at the initial design stage. The Thermal Grizzly Kryonaut shows the best performance with only 0.2 °C/W total thermal resistance from junction to air. However, silicone-based thermal grease has the tendency for the oil to physically migrate and separate from the solids, especially under high pressure. And silicone thermal grease can dry out after extensive thermal cycling. Therefore, the silicone-based Kryonaut is not suitable for this high-temperature inverter design. The Fischer grease has the second-lowest thermal resistance, and it is selected as the TIM in the prototype. The relatively poor performance of Graftech and indium sheets probably results from relatively small maximum allowable module mounting pressure compared to the required high contacting pressure aiming to achieve very small thermal resistance. Fig. 21 summarizes the testing results. The thermal resistances of different cold plates are compared similarly as for the TIMs and 007-MXQ-01 from Maxq Technology is finally selected due to its compact design and small thermal resistance.

2) Experimental Validation of the Developed Thermal Model

After selecting the thermal interface material and the cold plate, the total thermal resistance from junction to coolant is then obtained by performing the high-power conduction losses test. The three modules are connected in series with

TABLE IV
HIGH-POWER CONDUCTION LOSS TEST FOR TOTAL THERMAL RESISTANCE

I_d /A	V_{ds} /mV	$R_{ds,on}$ /mΩ	T_j /°C	T_{inlet} /°C	P_{loss} /W	$R_{th,total}$ /(°C • W^{-1})
199.03	902	4.53	60.85	35.5	179.5	0.141
249.78	1296	5.19	91.39	42.9	323.3	0.15
297.8	1772	5.95	120.56	37.2	527.7	0.158

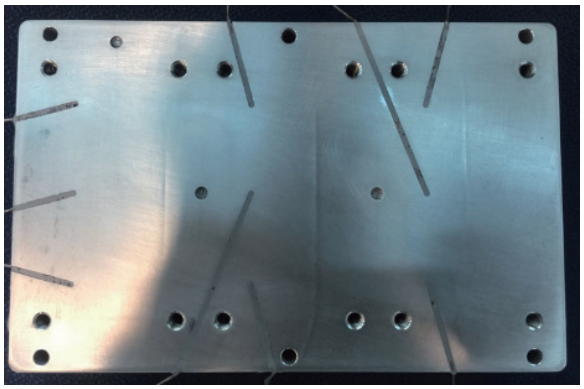

Fig. 22. The nine thermocouples were implemented in the cold plate for thermal measurements.

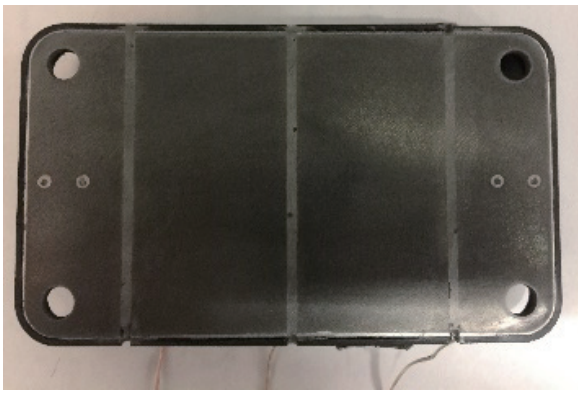

Fig. 23. The nine thermocouples were implemented in the module base plate for thermal measurements.

thick copper bars and all six MOSFETs gates are connected to constant positive voltage (+20 V). The series drain-source current is set to be 200, 250, and 300 A in three different conduction tests, and the results are summarized in Table IV. The total thermal resistance is slightly different for different drain currents and the average thermal resistance was approximately 0.15 °C/W. To make sure that all devices operate with the junction temperature which is below the maximum allowable junction temperature, a total thermal resistance of 0.16 °C/W is used for junction temperature estimations and other system thermal performance evaluations.

To confirm the thermal model illustrated in Fig. 19 and more importantly to make sure all the components can safely operate at 105 °C ambient temperature, the thermocouples (TC) are implemented in the system to monitor the temperature of critical points during the high-power tests. Nine 1-mm deep slots are machined on the cold plate and nine thermocouples are inserted into the slots. The tips of these TCs are placed exactly vertically below the MOSFET dies to measure the hottest points on the cold plate surface. By applying high thermal conductivity epoxy, the thermocouples can permanently stay in the cold plate, as shown in Fig. 22. Another nine thermocouples are also implemented on the surface of the baseplate of the MOSFETs modules by the same approach, as shown in Fig. 23. Three modules are then mounted on the cold plate with the selected TIM.

By performing the proposed conduction losses test and using (23) each interface layer temperature and their thermal resistances can be obtained as listed in Table V. The T_{case} represents the average thermocouple reading in the module base plate, T_{plate} is the average thermocouple reading in the cold plate, $R_{th,JC}$ is thermal resistance from junction to case, $R_{th,TIM}$ is the TIM thermal resistance and $R_{th,CP}$ is the thermal resistance from cold plate surface to coolant. The obtained results verify the proposed thermal model and validate the thermal resistance testing approach.

TABLE V
HIGH-POWER CONDUCTION LOSS TEST FOR EACH INTERFACE THERMAL RESISTANCE

Position	Temperature /°C	Parameter	Value /(°C • W^{-1})
Junction	94	$R_{th,JC}$	0.08
Baseplate	70	$R_{th,TIM}$	0.03
Clod plate	60	$R_{th,CP}$	0.05
Coolant inlet	45	$R_{th,total}$	0.16

$$\begin{cases} R_{th,\,JC} = \dfrac{T_j - T_{case}}{P_{loss}} \\ R_{th,\,TIM} = \dfrac{T_{case} - T_{plate}}{P_{loss}} \\ R_{th,\,CP} = \dfrac{T_{plate} - T_{coolant}}{P_{loss}} \end{cases} \tag{23}$$

VII. EXPERIMENTAL RESULTS

A. Test Platform

The 100-kW three-phase inverter prototype was assembled and placed in a thermal chamber, as shown in Fig. 24. The dc-link capacitors are soldered directly to the busbar and the necessary insulation is achieved using Kapton tape. The

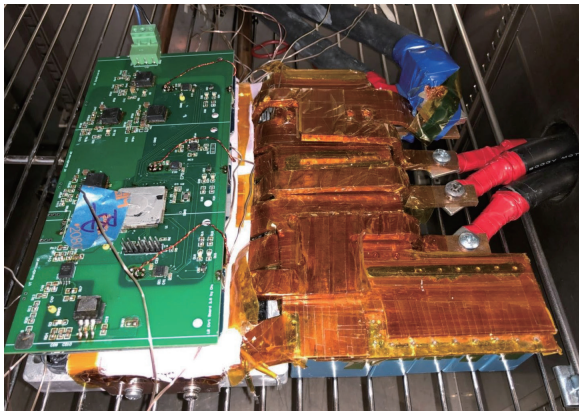

Fig. 24. The inverter prototype in the thermal chamber.

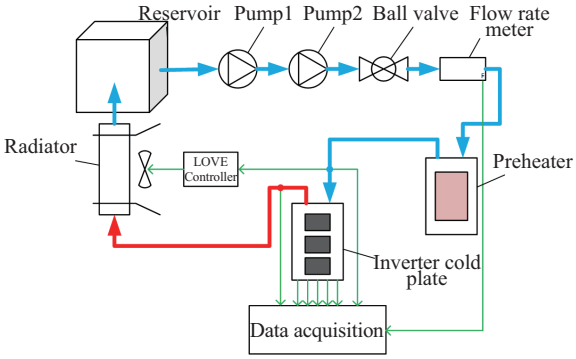

Fig. 25. Block diagram of the implemented liquid cooling system.

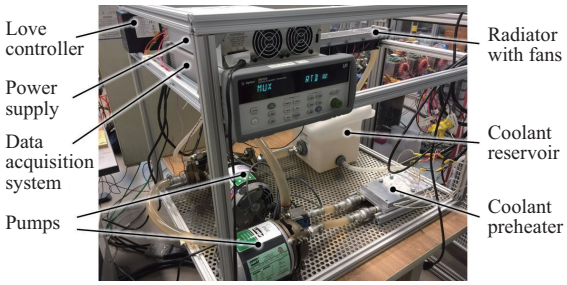

Fig. 26. The assembled cooling system.

additional thermocouples are implemented on the surface of the critical components (such as digital controller and dc/dc converters) on the gate driver and control board to monitor their temperature. The thermal conductive paste WLPK from Fischer Elektronik was used as the thermal interface between the MOSFET modules and the cold plate. The total thermal resistance from the junction to the coolant inlet was 0.16 °C/W. The inverter prototype was tested with an RL load. Two resistive load banks were connected in parallel to provide 100 kW resistive load at rated line-to-line ac output voltage, and two parallel-connected three-phase 250 A inductors are used as the inductive part of the load.

The liquid cooling system using a water-glycol mixture was assembled according to the diagram shown in Fig. 25.

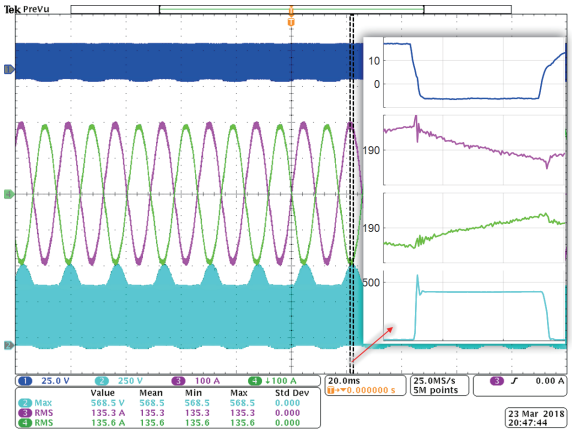

Fig. 27. Phase current (green & magenta), the corresponding bottom switch drain-source voltage (cyan blue), and its gate drive signal (dark blue), at 100 kW output power.

The assembled cooling system is shown in Fig. 26. Two pumps were connected in series to provide sufficient pressure difference. The mechanical valve controlled the flow rate at the rated 10 L/min. A preheater, which is made using a cold plate with integrated cartridge heaters, was used to preheat the coolant to the required temperature. The inlet and outlet coolant temperatures were measured by two thermocouples, and their pressure difference was monitored by a pressure transducer. An air-cooled radiator from TOYOTA Prius with seven dc-powered fans was used to dissipate the heat to the ambient. The love controller 4B-63-LV was used to regulate the inlet coolant temperature within 1 °C error.

B. Measurement Results

The inverter prototype was tested at 60 kW for an hour (the inverter reaches thermal equilibrium in 30 minutes) and then at 100 kW for 20 seconds at 105 °C ambient temperature. Fig. 27 shows the phase current, the corresponding bottom switch drain-source voltage, and the corresponding gate drive signal, recorded at 100 kW output power. Because of the current probe range limitation, the phase current is first split by using two conductors in parallel and then measured with two current probes (one of which was measuring the negative value of the current and hence the opposing current waveforms). The phase current is the sum of these two measurements and its RMS value was equal to 270 A. The drain-source overvoltage spikes of 568.5 V (which is a 42% voltage overshoot) were acceptable.

The achieved efficiency at 100 kW output power was 97%, as illustrated in Fig. 28. The temperature measurement results, obtained using data acquisition system 34972A from Agilent technologies, are shown in Fig. 29. When the output power increases from 60 kW to 100 kW, the temperatures of the inlet, outlet, module base plate, and cold plate reach their new steady state in less than 5 seconds. This is because the modules and cold plate have a relatively small thermal capacity, considering the power losses. Therefore, even 20 seconds of operation at

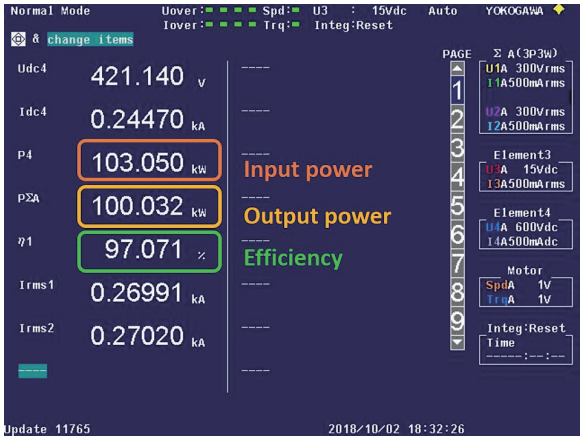

Fig. 28. The efficiency of the system at 100 kW output power.

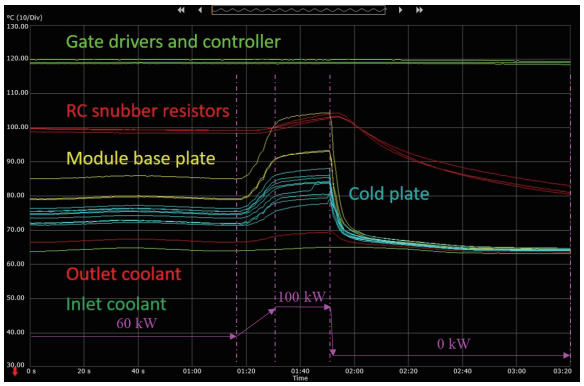

Fig. 29. The temperature measurements on the inverter prototype during the output power transition from 60 kW to 100 kW.

TABLE VI
THE TEMPERATURE MEASUREMENTS AT 100 KW OUTPUT POWER

Component	Maximum temperature /°C
Gate drivers	120
Digital controller	120
Snubber resistors	104
Baseplate	93 (104 °C outlier)
Cold plate	88
Inlet coolant	65
Outlet coolant	69

100 kW is sufficient to be considered as continuous operation for the modules and the whole cooling system.

If we disregard the outlier temperature measurement, which comes from one of the three thermocouples implemented in the middle module baseplate, the maximum temperatures at 100 kW output power are summarized in Table VI. The junction temperature can be calculated using (24), where the single switch power loss is 503 W from efficiency measurements.

$$T_j = R_{\text{th,total}} \cdot P_{\text{loss}} + T_{\text{avg,coolant}} = 145\ ^\circ\text{C} \tag{24}$$

VIII. CONCLUSION

This paper has presented a design of a high-power-density (34 kW/L) SiC-based 100 kW EV traction inverter which operates at 105 °C ambient temperature. The detailed thermal analysis is performed based on the thermal behavior of the switching devices to estimate the semiconductor device junction temperature and to determine the requirements of the cooling system to achieve the target power level. The methodology for the design and test of the cooling system including thermal interface material is proposed and then validated by implementing the thermocouples in the critical positions of the system. The inverter prototype is built and tested up to 100 kW at 105 °C ambient temperature. Both electrical and thermal experimental measurements confirm the safe operation of the proposed inverter.

REFERENCES

[1] C. C. Chan, "The state of the art of electric, hybrid, and fuel cell vehicles," in *Proceedings of the IEEE*, vol. 95, no. 4, pp. 704–718, Apr. 2007.

[2] J. Milln, P. Godignon, X. Perpi, A. Prez-Toms, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," in *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[3] M. Nakanishi, K. Hayashi, A. Enomoto, M. Hayashiguchi, M. Ando, K. Ino, C. Felgemacher, A. Mashaly, and G. Richard, "Automotive traction inverter utilizing sic power module," in *Proceedings of PCIM Europe 2018; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, Jun. 2018, pp. 1–6.

[4] B. Wrzecionko, D. Bortis, and J. W. Kolar, "A 120 °C ambient temperature forced air-cooled normally-off SiC JFET automotive inverter system," in *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2345–2358, May 2014.

[5] K. Olejniczak, T. McNutt, D. Simco, A. Wijenayake, T. Flint, B. Passmore, R. Shaw, D. Martin, A. Curbow, J. Casady, and B. Hull, "A 200 kVA electric vehicle traction drive inverter having enhanced performance over its entire operating region," in *Proceedings of 2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Oct. 2017, pp. 335–341.

[6] A. H. Wijenayake, K. J. Olejniczak, and D. Simco, "Design of a 250 kW, 1200 V SiC MOSFET based three-phase inverter by considering a subsystem level design optimization approach", in *Proceedings of 2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 939-946.

[7] K. Olejniczak, T. Flint, D. Simco, S. Storkov, B. McGee, R. Shaw, B. Passmore, K. George, A. Curbow, and T. McNutt, "A compact 110 kVA, 140 ℃ ambient, 105 ℃ liquid cooled, all-SiC inverter for electric vehicle traction drives," in *Proceedings of 2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2017, pp. 735–742.

[8] F. Qi, M.Wang, and L. Xu, "Investigation and review of challenges in a high-temperature 30-kva three-phase inverter using SiC mosfets," in *IEEE Transactions on Industry Applications*, vol. 54, no. 3, pp. 2483–2491, May 2018.

[9] F. Qi, M. Wang, L. Xu, B. Zhao, Z. Zhou, and X. Ren, "Design and evaluation of 30 kVA inverter using SiC mosfet for 180 ℃ ambient temperature operation," in *Proceedings of 2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2016, pp. 2912–2918.

[10] L. Yang, Y. Luo, R. S. K. Moorthy, D. Rahman, W. Yu, and I. Husain, "Design and test of a planarized high power density 100 kW SiC traction inverter with 1 kV dc-link," in *Proceedings of 2018 IEEE Energy Conversion Congress and Exposition (ECCE),* Portland, OR, 2018, pp. 3864–3871.

[11] J. Wang, Z. Shen, C. DiMarino, R. Burgos, and D. Boroyevich, "Gate driver design for 1.7 kV SiC MOSFET module with Rogowski current

sensor for short circuit protection," in *Proceedings of 2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2016, pp. 516–523.

[12] K. Fink, A. Volke, W.Wei, E.Wiesner, and E. Thal, "Gate-driver with full protection for SiC-MOSFET modules," in *Proceedings of PCIM Asia 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2016, pp. 1–7.

[13] E.Wiesner, E. Thal, A.Volke, and K. Fink, "Advanced protection for large current full SiC-modules," in *Proceedings of PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2016, pp. 1–5.

[14] S. Mocevic, J. Wang, R. Burgos, D. Booyevich, C. Stancu, M. Jaksic, and B.Pleaslee, "Comparison between desaturation sensing and Rogowski coil current sensing for short circuit protection of 1.2 kV, 300 a SiC MOSFET module," in *Proceedings of 2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 2666–2672.

[15] Z. Chen, D. Boroyevich, P. Mattavelli, and K. Ngo, "A frequency-domain study on the effect of dc-link decoupling capacitors," in *Proceedings of 2013 IEEE Energy Conversion Congress and Exposition,* Denver, CO, 2013, pp. 1886–1893.

[16] Q. Liu, S. Wang, A. C. Baisden, F. Wang, and D. Boroyevich, "EMI suppression in voltage source converters by utilizing dc-link decoupling capacitors," in *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1417–1428, Jul. 2007.

[17] K. Yatsugi, K. Nomura, and Y. Hattori, "Analytical technique for designing an RC snubber circuit for ringing suppression in a phase-leg configuration," in *IEEE Transactions on Power Electronics*, DOI 10.1109/TPEL.2017.2731421.

[18] E. Sulaiman, T. Kosaka, and N. Matsui, "A novel hybrid excitation flux switching synchronous machine for a high-speed hybrid electric vehicle applications," in *Proceedings of 2011 International Conference on Electrical Machines and Systems*, Aug. 2011, pp. 1–6.

[19] R. Taylor, B. Balachandran, D. Tan, and A. Yializis, "DC-link capacitors, a summary of the work performed under DoE programs DE-EE-00006433, DE-EE-00006438, and DE-AC02-06CH11357," Delphi, Argonne, GE, Sigma and the U.S. Department of Energy Vehicle Technologies Office, Mar. 2018.

[20] Torelina Introduction [online]. Available: https://www.toray.jp/films/en/products/torelina/index.html

[21] *Metallized Polypropylene Film Capacitors (MKP) Series/Type: B32774P ... B32778P*, TDK Electronics AG, Jun. 2018.

[22] J. W. Kolar and S. D. Round, "Analytical calculation of the RMS current stress on the dc-link capacitor of voltage-PWM converter systems," in *IEE Proceedings - Electric Power Applications*, vol. 153, no. 4, pp. 535–543, Jul. 2006.

[23] C. Zhang, S. Srdic, and S. Lukic, "Optimization of dc-link decoupling snubber circuit for SiC-based EV traction inverters," in *Proceedings of 2019 IEEE Energy Conversion Congress and Exposition (ECCE),* Baltimore, MD, USA, 2019, pp. 6810–6814.

[24] K. Sun, J. Wang, R. Burgos, and D. Boroyevich, "Design, analysis, and discussion of short circuit and overload gate-driver dual-protection scheme for 1.2-kV, 400-A SiC MOSFET modules," in *IEEE Transactions on Power Electronics*, vol. 35, no. 3, pp. 3054–3068, Mar. 2020.

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