

# Chapter 7. Conclusions and Recommendations

## 7.1 Conclusions

The following original contributions have been made in the study of the effects of the input PFC on various VSD systems:

- (i) Inclusion of the input PFC to SRM-, PMBDC- and DCM-based VSD systems has been proposed for appliance applications and its performance has been verified with experiment, analysis and simulation.
- (ii) Operational modes of the proposed VSD systems have been identified and analytical derivations are made for each mode. Based on this, the system equations and design procedures are systematically derived to evaluate the drive system performances with and without an input PFC preregulator.
- (iii) The comparison of drive performance with PFC preregulator shows its overall system efficiency is consistently lower than that without an input PFC. This decrease in efficiency has to be weighted against the advantages of the near sinusoidal current from utility, high power factor and reduction of input current harmonics of the input PF-corrected drive system. It is recommended for integration of input PFC with a clear understanding that it will lower the overall system efficiency.
- (iv) The efficiency prediction of the proposed VSD systems has been carried out with derived loss models. The loss models are derived by summation of all losses of major power components in PFC preregulators and VSD systems. The derived loss models are unique to the given VA ratings of PFC preregulators and VSD systems. Therefore the derived loss models are not directly applicable to other VSDs with different configurations. However the procedure to derive the VA ratings and loss expressions can be referred to derive the loss models of other types of VSDs.
- (v) C-dump converter for use with the PMBDC has been identified to give a high reliability and phase independent operation. The application of a C-dump converter to PMBDC drive is novel. The identified topology lends itself to the four-quadrant operation, compact packaging, low number of power supplies and gate drives requirements, making it a low cost drive system for the PMBDC motor. Modes of operation for this motor drive and its design are derived and experimentally verified. The proposed drive is efficient for most of the desired speed ranges in appliance VSD applications.
- (vi) UMD concept has been proposed and illustrated with the C-dump converter based SRM drive system. Various topologies for UMD have been analyzed and experimentally verified. Overall system performance and efficiency have been

experimentally and analytically evaluated and found to be acceptable for many applications.

## **7.2 Recommendations for Future Study**

For future study in the area of the input PF-corrected VSD system, the following issues should be studied,

- (i) Development of a precise dynamic model of an input PF-corrected VSD system to predict its dynamic behavior,
- (ii) Investigation of the interaction between the front-end PFC preregulator and converter for the VSD system to prevent any undesirable effects. Especially the study of the regeneration effect on PFC preregulator when a VSD system operates in the regenerative mode, and
- (iii) A study on the single-stage input PFC topology including a PWM converter or inverter function for the VSD system to improve the overall system efficiency and reliability.