A Constant ON-Time 3-Level Buck Converter for Low Power Applications

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ABSTRACT

Smart cameras operate mostly in sleep mode, which is light load for power supplies. Typical buck converter applications have low efficiency under the light load condition, primarily from their power stage and control being optimized for heavy load. The battery life of a smart camera can be extended through improvement of the light load efficiency of the buck converter. This thesis research investigated the first stage converter of a car black box to provide power to a microprocessor, camera, and several other peripherals. The input voltage of the converter is 12 V, and the output voltage is 5 V with the load range being 20 mA (100 mW) to 1000 mA (5000 mW). The primary design objective of the converter is to improve light load efficiency.

A valley current mode controlled 3-level buck converter proposed by Reusch was adopted for the converter in this thesis. A 3-level buck converter has two more MOSFETs and one more capacitor than a synchronous buck converter. Q1 and Q2 are considered the top MOSFETs, while Q3 and Q4 are the synchronous ones. The extra capacitor is used as a second power source to supply the load, which is connected between the source of Q1 and the drain of Q2 and the source of Q3 and the drain of Q4. The methods considered to improve light load efficiency are: PFM (pulse frequency modulation) control scheme with DCM (discontinuous conduction mode) and use of Schottky diodes in lieu of the synchronous MOSFETs, Q3 and Q4. The 3-level buck converter operates in CCM for heavy load above 330 mA and DCM for light load below 330 mA. The first method uses a COT (constant on-time) valley current mode controller that has a built in inductor current zero-crossing detector. COT is used to implement PFM, while the zero-crossing detector allows for DCM. The increase in efficiency comes from reducing the switching frequency as the load decreases by minimizing switching and gate driving loss. The second method uses an external current sense amplifier and a comparator to detect when to shut down the gate drivers for Q3 and Q4. Schottky diodes in parallel with Q3 and Q4

carry the load current when the MOSFETs are off. This increases the efficiency through a reduction in switching loss, gate driving loss, and gate driver power consumption.

The proposed converter is prototyped using discrete components. LTC3833 is used as the COT valley current mode controller, which is the center of the control scheme. The efficiency of the 3-level buck converter was measured and ranges from 82% to 95% at 100 mW and 5000 mW, respectively. The transient response of the converter shows no overshoot due to a 500 mA load step up or down, and the output voltage ripple is 30 mV. The majority of the loss comes from the external components, which include a D FF (D flip-flop), AND gate, OR gate, current sense chip, comparator, and four gate drivers. The proposed converter was compared to two off-the-shelf synchronous buck converters. The proposed converter has good efficiency and performance when compared to the other converters, despite the fact that the converter is realized using discrete components.

To my parents, sister and brothers

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Chapter 1

Introduction

1.1 Motivation

Event data recorders, often called car black boxes, are being installed in most American cars today. The device collects information such as speed, accelerator position, brake position, etcetera of during a crash and the prior moment. As of September 1st 2014, the National Highway Traffic Safety Administration mandates every car to be equipped with a car black box [1].

The car black box proposed by the Korean Advanced Institute of Science and Technology (KAIST) team in Korea records video of the front and rear view of the car. The car black box is mostly in sleep mode while waiting for detection of an event. Upon detection of an event, it wakes up and starts to record. Since a car black box is powered by the car battery and mostly in sleep mode, high efficiency for light load is important, especially when the engine is turned off. The proposed research in this thesis is to improve light load efficiency of a power converter, targeting the black box developed by the KAIST team.

1.2 Scope of the Proposed Research

DC-to-DC buck converters are used to convert the car battery voltage down to lower DC voltages necessary for the black box. A two stage approach is usually taken to efficiently step a 12 V input voltage down to lower voltages. The first stage steps the battery voltage down to a regulated 5 V for USB hosts and a camera. The second stage steps down the 5 V to various DC voltages.

A traditional synchronous buck converter can be used for both the first and second stage.

One major difference between the two stages is the breakdown voltage required for the MOSFETs. The breakdown voltage of a MOSFET used in a buck converter is typically two times the input voltage, which prevents overshoot, ringing and others from damaging the device [2]. Therefore, the first stage requires the breakdown voltage of about 30 V, considering the maximum car battery voltage of 14.2 V. Low voltage devices typically have better characteristics, such as low on-resistance and gate charge, which improves the light load efficiency. The proposed research is to improve light load efficiency of the first stage converter, specifically a 12 V to 5 V DC/DC converter, through adoption of a 3-level buck converter configuration that enables use of devices with a lower breakdown voltage.

The proposed 3-level buck converter uses research by Reusch as the starting point [3]. The 3-level buck converter has four phases of operation, in which the inductor and output capacitor are charged twice within one switching period. It has two additional MOSFETs and an extra capacitor compared to a traditional buck. The main advantages of the 3-level buck converter are the ability to use low voltage devices and smaller passive values compared to a traditional buck at the same frequency.

The 3-level buck converter designed in [3] adopts a constant frequency control method. This control method is efficient for heavy load, but light load efficiency suffers significantly. This is essentially due to the converter connecting the input voltage source to the load more often than necessary for light load. It wastes power in the form of conduction loss, gate driving loss, and switching loss to result in low efficiency.

Zhou proposed several methods to improve light load efficiency of buck converters [4]. Among the methods, a hybrid control approach adopts PFM (pulse frequency modulation) in DCM (discontinuous conduction mode) that reduces the switching frequency proportional to the load. Reducing the switching frequency decreases the amount of conduction, switching, and gate driving losses. The converter only connects the input source to the load only when it is necessary, which is inherently more efficient for light load.

A 3-level buck converter was investigated that adopts the control approach to improve light load efficiency. The 3-level buck converter utilizes constant on-time (COT) control in PFM, with DCM being implemented by detecting the point when the inductor current reaches zero. The reduction in switching frequency as the load decreases leads to less loss and higher

efficiency when compared to CCM (continuous conduction mode).

1.3 Technical Contributions of the Proposed Research

The first stage buck converter targeted for the KAIST car black box was designed and prototyped. The major design objective of the converter is high efficiency at light load. Technical contributions of the proposed research are as follows.

First, the power stage of the converter was successfully designed to meet the objective, high efficiency in light load, for the target application. The MOSFET selection was discussed in detail, and the power stage was optimized iteratively through simulation and performance measurement of prototypes.

Second, the control loop was successfully designed to meet the same objective, and it adopts COT valley current mode control and DCM. An off-the-shelf synchronous buck controller was selected as the core of the control loop. The gate signals, generated by the controller, are passed through a series of digital gates to generate the appropriate driving signal for each MOSFET in the 3-level buck converter. The control loop was simulated in LTspice to ensure proper operation.

Third, the proposed converter is prototyped using discrete components and an existing controller to demonstrate the control scheme and design. The prototype demonstrates correct operation of the control scheme such that the switching frequency reduces with the load current in light load. It also demonstrates correct operation of the DCM, which shuts down the synchronous MOSFETs when the inductor current touches zero. Performance of the converter was measured using the final prototype. The efficiency is significantly improved when compared with the CCM mode adopted in Reusch's converter and other comparable buck converters.

1.4 Organization of the Thesis

The organization of the thesis is as follows. Chapter 2 provides background and preliminaries for the proposed research work. This chapter discusses requirements for the proposed buck converter and reviews the traditional buck converter topology, methods to

improve the efficiency of buck converters, and a 3-level buck converter including its advantages and disadvantages. Chapter 3 introduces the proposed 3-level buck converter and describes the operation of the controller. The control method is described in detail to explain how the proposed converter aims to improve light load efficiency. PFM with DCM, specifically COT valley current mode control, is utilized to improve light load efficiency by reducing the overall switching frequency as the load current drops. Chapter 4 presents measured results of the prototype to show the efficiency and performance of the converter. Measured results include load transients and efficiency for the entire load range. Lastly, Chapter 5 draws conclusions on the proposed controller design.

Chapter 2

Preliminaries

This chapter provides preliminary information and previous research activities that are necessary to understand the proposed 3-level buck converter and the contributions of this thesis research. Section 2.1 provides the characteristics of a typical power supply and the requirements set forth for the proposed design. Section 2.2 describes how a synchronous buck converter operates. Section 2.3 reviews a 3-level buck converter design. Section 2.4 describes Constant On-Time (COT) control method adopted in the proposed converter and its advantages and disadvantages. Section 2.5 summarizes the chapter.

2.1 Design Requirements

The target black box is power by the 12 V lead acid car battery. Figure 2.1 shows a block diagram for the power stage. The first stage converts a car battery voltage to a regulated 5 V, and the second stage steps down the 5 V to various lower voltages. The proposed converter aims for the first stage 12 V to 5 V step down.

The car black box operates mostly in sleep mode, or light load, while waiting for detection of any event. A black box should not deplete the battery when the car is parked, where the light load sleep mode is the primary operating condition. This leads the major design objective of the proposed converter to be high efficiency in light load.

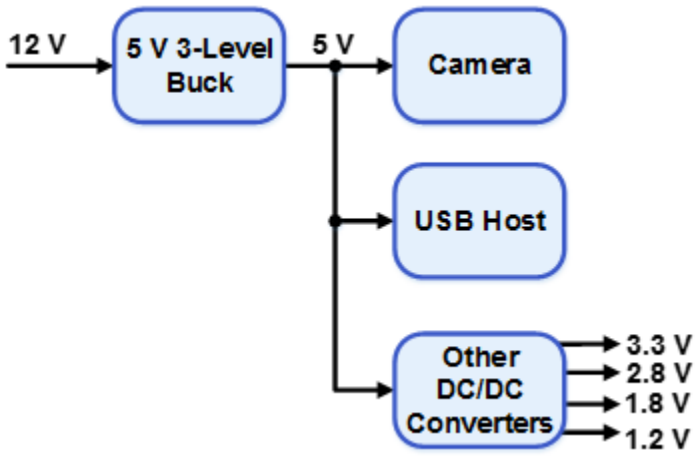


Figure 2.1 Power block diagram for Car Black Box.

2.2 Buck Converter

Voltage regulators can be realized using a linear regulator or a switching power supply, with the latter being more efficient and commonly used. A typical topology to step down a voltage is a buck converter. The output voltage is the average value of the period, in which the input is connected through the switch. An asynchronous buck converter is shown in Figure 2.2. This topology has one active and one passive switch. When the input switch is closed, the inductor and output capacitor are charged and the load current is supplied by the input. The inductor and output capacitor supply the load when the switch is open.

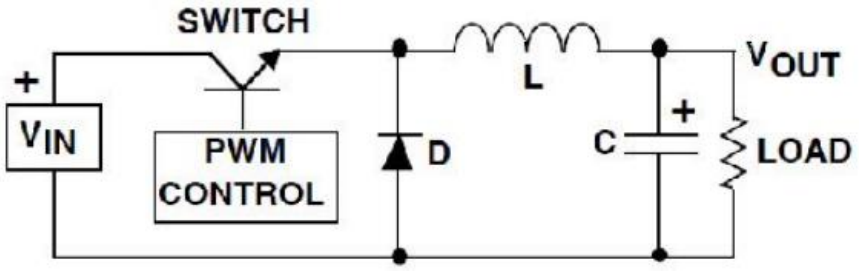


Figure 2.2 Asynchronous buck converter from E. V. Mehta and E. P. Malik, "Comparison between Asynchronous and Synchronous Buck Converter Topology," *International Journal of Applied Engineering Research*, vol. 7, no. 11, 2012. Used under fair use, 2015.

Replacing the diode with a MOSFET improves the heavy load efficiency of the converter due to the reduction in conduction loss. This topology shown below in Figure 2.3 is called a synchronous buck converter.

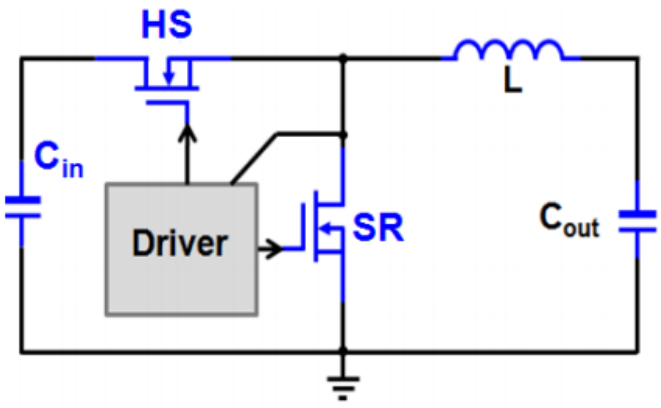


Figure 2.3 Synchronous buck converter D. Reusch, *High Frequency, High Power Density Integrated Point of Load and Bus Converters,* Ph.D. dissertation, ECE, Virginia Tech, Blacksburg, VA, 2012. Used under fair use, 2015.

There are two operation modes for a converter, continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The inductor current always flows in CCM, where it can be in the positive and negative direction in a synchronous buck converter. The inductor current in DCM can only flow in the positive direction. When it reaches zero, it is not allowed to flow in the negative direction because it is blocked. DCM is naturally realized using an asynchronous buck converter due to the diode blocking the inductor current from reversing direction; whereas, a synchronous buck converter must shut down the bottom MOSFET when the inductor current reaches zero.

There are several design criteria that must be met when designing a switching power supply. The most important are the converter's ability to regulate the output voltage with a change on the input voltage and/or an increase in load current, which is called line and load regulation, respectively. The following design is performed at full load when the converter is operating in CCM. The duty cycle, D, of the converter determines how long switch one should be turned on in the switching period. The ideal value for D being calculated below [5]:

$$D = \frac{V_{out}}{V_{in}}$$

The next major design step is calculating the amount of inductance needed based on the maximum output current and allowable current ripple. Below is the calculation for inductance [5]:

$$L = \frac{(V_{in} - V_o) \cdot D}{I_{o_{max}} \cdot \Delta i_L \cdot f_s}$$

where V_{in} is the input voltage, V_o is the output voltage, f_s is the switching frequency, $I_{o_{max}}$ is the maximum load current, and Δi_L is the peak to peak inductor current ripple percentage. The inductor current ripple is typically designed to be between 20 – 40% of the maximum load current to minimize the conduction loss [6].

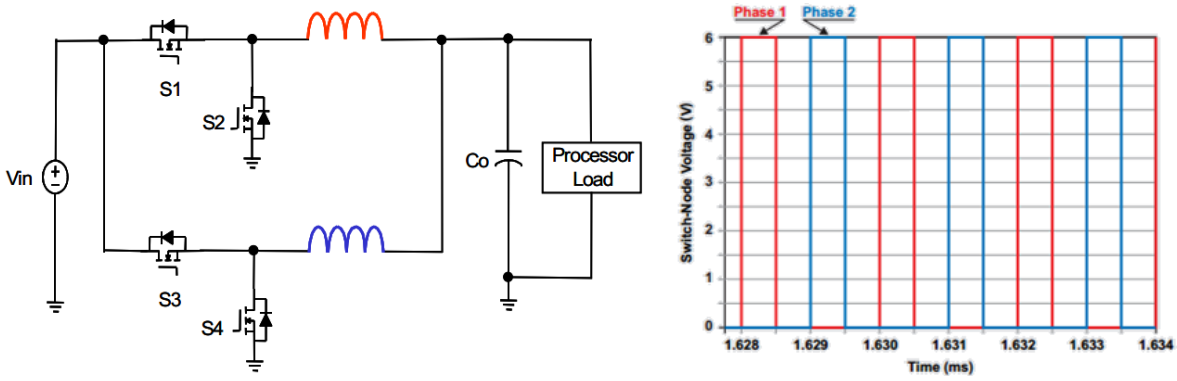
The output capacitance is obtained based on the inductor current ripple, switching frequency, and maximum allowable output voltage ripple. The capacitance calculation is as follows [5]:

$$C = \frac{\Delta I_L}{8 \cdot \Delta V_o \cdot f_s}$$

Lastly, it is important to select the proper active devices. The breakdown voltage of a MOSFET is defined as the maximum allowable voltage stress on V_{DS}. Using a device that has a breakdown voltage rating of two times the input allows for overshoot on V_{DS} to not damage the device [7]. The breakdown voltage of each MOSFET of a buck converter must be two times the input voltage because when each switch is on, the other switch sees the input voltage to ground from its drain to source (V_{DS}). The on resistance ($R_{DS_{on}}$) and gate charge (Q_g) are the next factors to consider when selecting a device. Generally, as $R_{DS_{on}}$ goes down, Q_g goes up and vice versa. The conduction loss of a converter increases with a larger $R_{DS_{on}}$. Gate charge loss increases with a larger Q_g. As the load decreases, Q_g becomes more important than $R_{DS_{on}}$ because it becomes the dominant factor compared to the relatively small conduction loss.

The required inductance and capacitance can be reduced with two buck converters in parallel, which is called a two-phase buck converter [8]. Figure 2.4 shows a two-phase buck converter and its timing diagram. The timing diagram shows that switch S3 is driven 180 degrees out of phase of switch S1. This causes the inductor current waveforms to be interleaved which then makes the output ripple frequency effectively two times the switching frequency of MOSFETs. This allows the input to supply power to the load twice within one switching period. This greatly reduces the current ripple and the amount of inductance and capacitance needed to maintain the proper output voltage [8]. More phases can be put in parallel to further reduce the required load current ability of each phase. One limitation is when the duty cycle is very small,

the current ripple cancellation is poor which increases the output ripple [8].



(a) (b)

Figure 2.4 (a) Multi-phase buck converter schematic from P. Xu, Multiphase Voltage Regulator Modules with Magnetic Integration to Power Microprocessors, Ph.D. dissertation, ECE, Virginia Tech, Blacksburg, VA, 2002. (b) Timing diagram for two phase buck from D. Baba, *Benefits of a multiphase buck converter*, Texas Instruments Application Note, 2012. Used under fair use, 2015.

Typically, synchronous buck converters adopt pulse width modulation (PWM), where the width of the pulse that drives the top and bottom MOSFETs is adjusted. PWM is usually accompanied with a constant frequency control, which is efficient under heavy load, but the efficiency suffers in the light load [9]. The conduction loss P_{cond} decreases with load because it is primarily dependent on $R_{DS_{on}}$ of the MOSFETs and the load current, as shown in Figure 2.5 [9]. The gate driving and switching loss denoted as P_{sw} in the figure are constant throughout the entire load range. The fixed loss denoted as P_{fixed} includes chip supply power and other unavoidable power dissipation, and it cannot be adjusted. PFM can be used to reduce the switching loss and improve efficiency as described in the following [10].

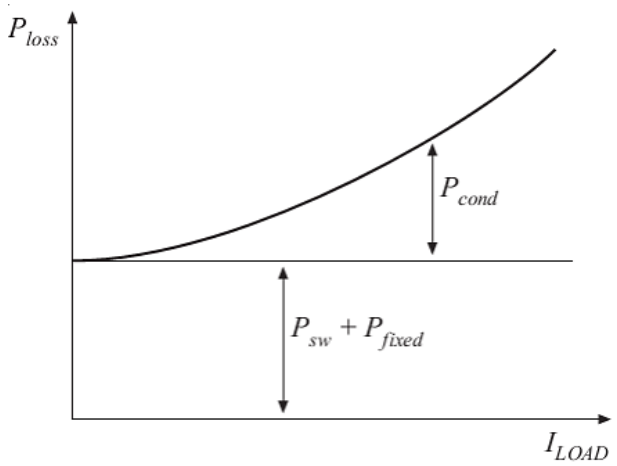


Figure 2.5 Constant frequency control loss breakdown from P. Vivek, *Extending Efficiency in a DC/DC converter with automatic mode switching from PFM to PWM*, M.S. Thesis, ECE, Arizon Statue University, Phoenix, AZ, 2014. Used under fair use, 2015.

2.2.1 Approach to Improve Efficiency

As the load decreases, PFM reduces the switching frequency to minimize gate driving loss to improve light load efficiency [9]. Figure 2.6 shows how the gate driving and switching loss is reduced as the load decreases under PFM, which increases the efficiency. The disadvantage of this technique is the output voltage ripple increases [9]. The controller can be used to mitigate it by monitoring the output voltage ripple in DCM. The proposed converter adopts a technique to trigger the top MOSFET when the output voltage ripple exceeds a certain threshold.

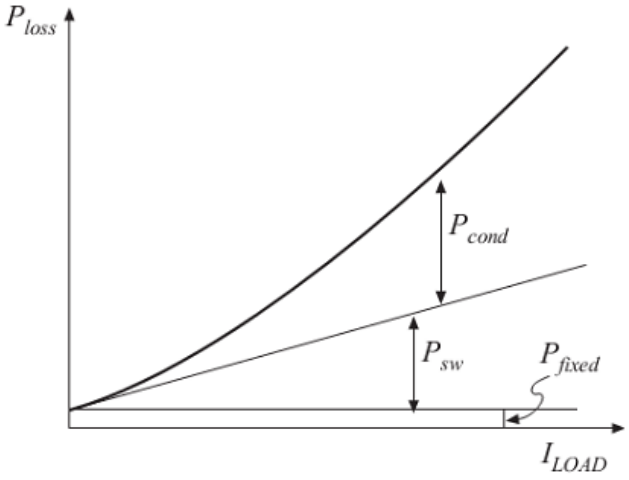


Figure 2.6 PFM control loss breakdown from P. Vivek, *Extending Efficiency in a DC/DC converter with automatic mode switching from PFM to PWM*, M.S. Thesis, ECE, Arizon Statue University, Phoenix, AZ, 2014. Used under fair use, 2015.

2.2.2 Breakdown Voltage

MOSFET breakdown voltage needed in a synchronous buck converter and its impact on efficiency are discussed in this section. A major drawback of a synchronous buck converter is the inability to use low voltage devices. Low voltage devices refer to MOSFETs with low breakdown voltages. Devices with low breakdown voltages generally have lower values of $R_{DS_{on}}$, Q_g, and Miller capacitance. Miller capacitance is between the gate and drain of a MOSFET and must be charged or discharged to turn the device on or off, respectively. Decreasing these three values leads to higher efficiency through faster turn on and off time, lower conduction loss, and lower switching loss. The breakdown voltage required for each MOSFET of a converter is generally two times the input voltage to allow for overshoot and ringing seen across V_{DS} [7].

2.2.3 Zhou's Approaches

Zhou highlights major drawbacks in light load efficiency with the synchronous buck converter topology [4]. Zhou attempted to improve the efficiency by introducing four different methods of switching the synchronous MOSFET when the inductor current begins to flow in the reverse direction. Three of Zhou's attempts to improve light load efficiency will be discussed in this section. Zhou's first approach uses a Schottky diode in parallel with the bottom MOSFET [4]. Figure 2.7 shows the schematic of the proposed converter, which operates in constant switching frequency or PWM. The bottom MOSFET is shut down completely when the average load current decreases below a threshold value. The inductor current flows through the Schottky diode, which effectively becomes an asynchronous buck converter. The threshold value is based on the inductor value by determining when the inductor current begins to reverse in direction. The threshold value is considered the critical duty cycle and is where the efficiency begins to reduce significantly. Shutting down the bottom MOSFET reduces the driving loss of the converter. Figure 2.8 compares the efficiency between normal CCM operation and DCM operation with the Schottky diode.

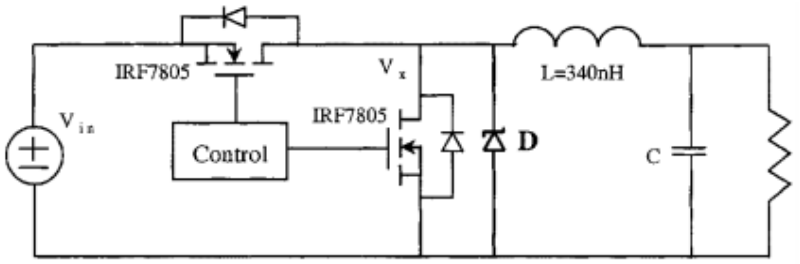


Figure 2.7 Schematic of the proposed converter from X. Zhou, M. Donati, L. Amoroso, and F. C. Lee, "Improved Light-Load Efficiency for Synchronous Rectifier Voltage Regulator Module," in *IEEE Transactions on Power Electronics, Vol. 15, No. 5, pp. 826-834*, 2000. Used under fair use, 2015.

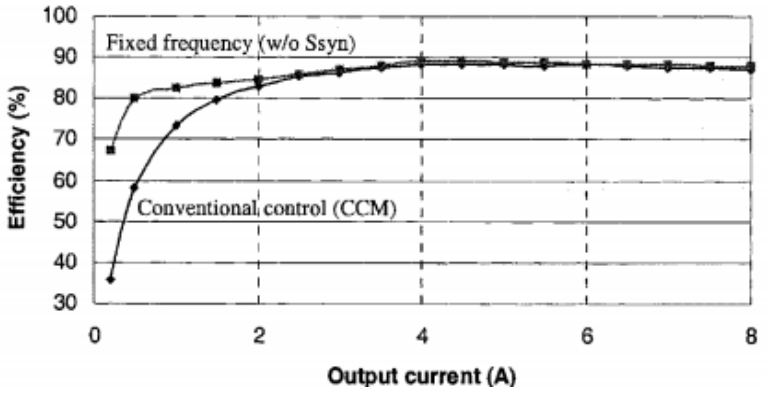


Figure 2.8 Efficiency of CCM and Schottky diode DCM (w/o Ssyn) from X. Zhou, M. Donati, L. Amoroso, and F. C. Lee, "Improved Light-Load Efficiency for Synchronous Rectifier Voltage Regulator Module," in *IEEE Transactions on Power Electronics, Vol. 15, No. 5, pp. 826-834*, 2000. Used under fair use, 2015.

The second one, called a hybrid technique, further improves the light load efficiency [4]. Like the first approach, the hybrid mode operates at the constant frequency above the critical load current. As the load decreases below the critical load current, the synchronous rectifier is shut down and the parallel Schottky diode carries the load current. Differing from the first method, the switching frequency decreases according to the load current. Figure 2.9 shows improvement of the light load efficiency for the hybrid method, owing to reduction of the switching frequency and DCM operation. The converter achieves much higher efficiency in the light load case than the conventional CCM and the first Schottky diode DCM approach.

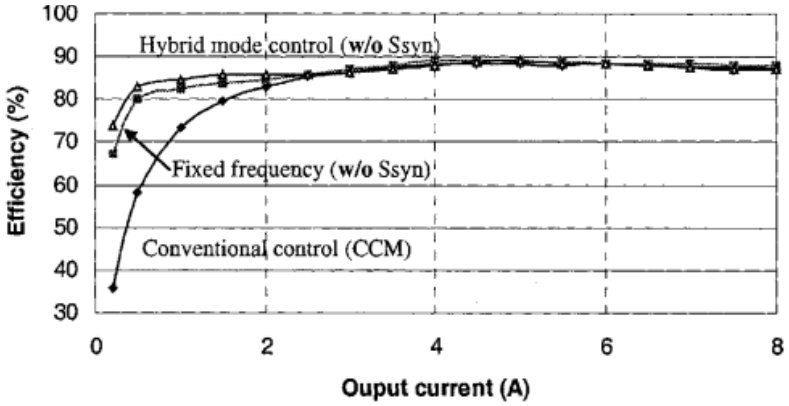


Figure 2.9 Efficiency curve from X. Zhou, M. Donati, L. Amoroso, and F. C. Lee, "Improved Light-Load Efficiency for Synchronous Rectifier Voltage Regulator Module," in *IEEE Transactions on Power Electronics, Vol. 15, No. 5, pp. 826-834*, 2000. Used under fair use, 2015.

The approach is then further improved by determining when the inductor current will reach zero, at which point the synchronous MOSFET is turned off. The synchronous MOSFET will turn on again after the top MOSFET turns off, repeating the same process. The approach adopts PFM and eliminates the loss due to the forward drop of the Schottky diode. Figure 2.10 shows the efficiency of the third approach annotated as “hybrid mode control (w/ Ssyn)” compared to CCM and the hybrid diode approaches. Figure 2.10 demonstrates that shutting down the synchronous MOSFET instead of using a diode is more efficient. The converter of the car black box application stays in the sleep mode or light mode mostly, making high efficiency in this case is important. The 3-level buck converter will adopt PFM, DCM, and the paralleled Schottky diode method introduced in this paper.

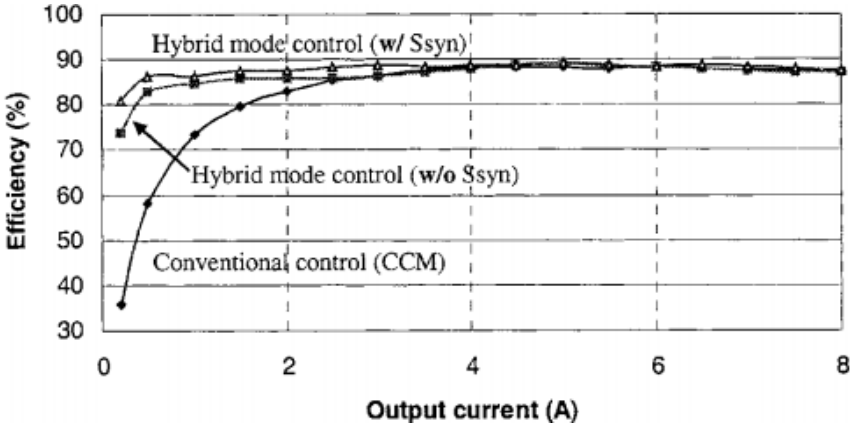


Figure 2.10 Efficiency of the hybrid MOSFET (w/ Ssyn) and hybrid Schottky diode (w/o Ssyn) method from X. Zhou, M. Donati, L. Amoroso, and F. C. Lee, "Improved Light-Load Efficiency for Synchronous Rectifier Voltage Regulator Module," in *IEEE Transactions on Power Electronics, Vol. 15, No. 5, pp. 826-834*, 2000. Used under fair use, 2015.

2.2.4 Shortcomings

The primary shortcoming of Zhou's approaches is the inability to use low voltage devices. Low voltage devices improve the overall efficiency by decreasing $R_{DS_{on}}$, Q_g, and Miller capacitance. It is the major driving factor for the proposed converter to adopt a 3-level buck converter.

2.3 3-Level Buck Converrter

The 3-Level Buck converter topology adopted for this thesis research was also used by Reusch [3]. The proposed converter used Reusch's valley current mode control as the starting point. The converter was designed as a voltage regulator to step 12 V down to 1.8 V and is capable of supplying the load with 15 A. The converter achieves 88% efficient under a load of 8.5 A (or 15.3 W) [3].

2.3.1 Reusch Valley Current Mode 3-Level Buck Converter

Reusch designed a valley current mode controlled 3-level buck converter in [3]. The 3-level buck converter is shown in Figure 2.11. The topology has two extra MOSFETs and one extra capacitor compared to the traditional buck converter. The additional "flying capacitor" floats between two switch nodes. The timing diagram in the figure shows that MOSFET Q1 and Q2 are driven 180 degrees out of phase. The flying capacitor repeats charging and discharging each switching period. The flying capacitor acts as a second source while being discharged, making the effective output ripple frequency two times the MOSFET switching frequency.

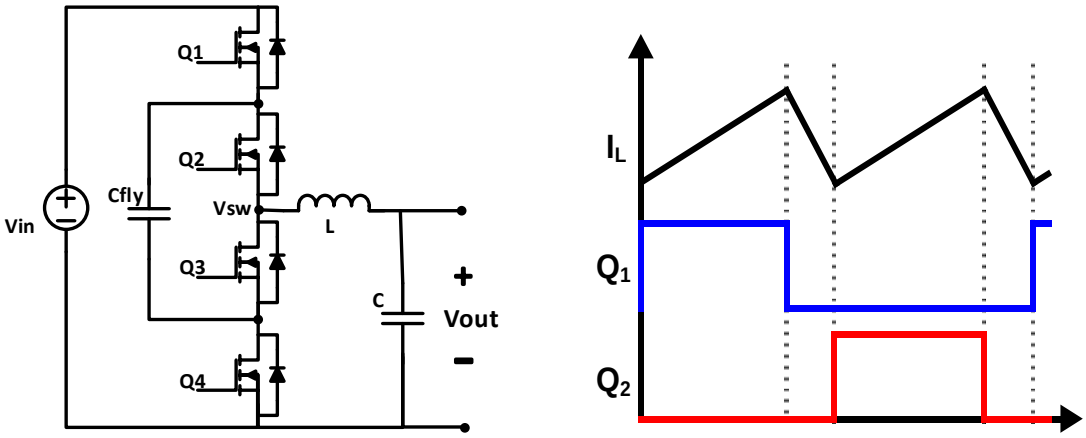
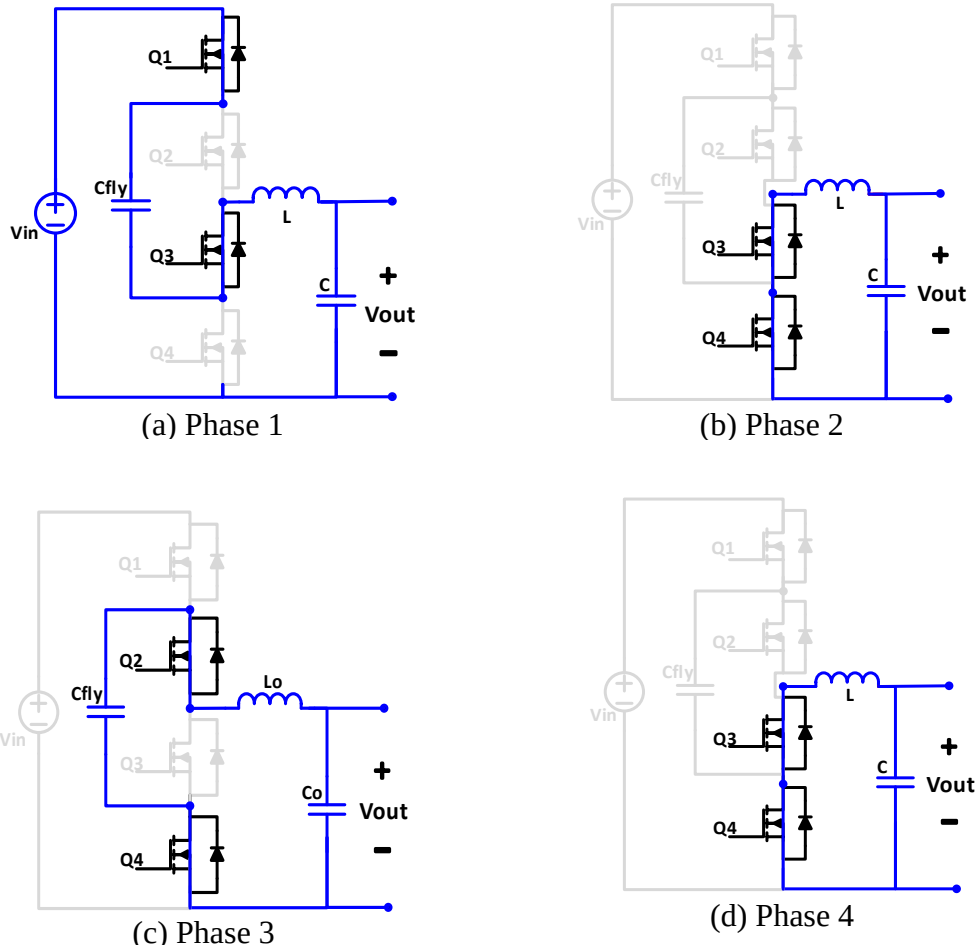


Figure 2.11 3-Level Buck Converter schematic and timing diagram.

The 3-level buck converter's four modes of operation shown in Figure 2.12 are explained by the following. Phase 1 occurs when Q1 and Q3 are turned on. It charges the flying capacitor, inductor, and output capacitor as well as supplying the load. During Phase 2, Q3 and Q4 are turned on. This allows the converter to act like a synchronous buck converter by supplying the load with the inductor and output capacitor. During Phase 3, Q2 and Q4 are turned on. The energy stored in the flying capacitor charges the inductor and output capacitor as well as supplying the load. Phase 4 has the same configuration as Phase 2.

The energy sources, the voltage source V_{in} and the flying capacitor, are each connected to the load once within a switching period, causing the output ripple frequency to double. Additionally, charging the inductor twice within one switching period reduces the inductance and output capacitance necessary for the same amount of ripple. It is discussed further in Section 2.4.2.



(a) Phase 1 (b) Phase 2

(c) Phase 3 (d) Phase 4

Figure 2.12 Four phases of operation a) Phase 1, b) Phase 2, c) Phase 3, d) Phase 4.

The 3-level buck converter design adopts valley current mode and constant frequency control. The valley current mode control compares the inductor current to a valley threshold, which is generated from the output voltage error amplifier. When the trough of the inductor current reaches the valley threshold, either Q1 or Q2 is turned on. The constant frequency clock turns the top MOSFET Q1 or Q2 off to keep the switching frequency constant. The timing diagram for the control and the schematic are shown in Figure 2.13.

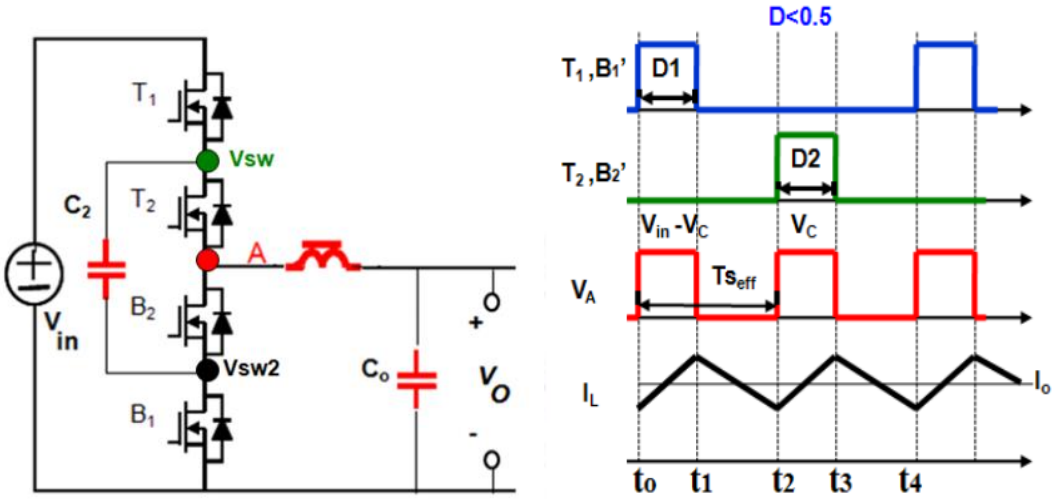


Figure 2.13 3-level buck converter schematic and timing diagram from D. Reusch, *High Frequency, High Power Density Integrated Point of Load and Bus Converters*, Ph.D. dissertation, ECE, Virginia Tech, Blacksburg, VA, 2012. Used under fair use, 2015.

Valley current mode control allows for natural balancing of the flying capacitor voltage to one-half the input voltage V_{in}. Figure 2.14 and Figure 2.15 illustrate how the flying capacitor voltage naturally balances due to the valley current threshold. Figure 2.14 shows the case where the flying capacitor voltage is less than 0.5 V_{in}. Phase 1 starts at time t_0 and the inductor current rises at a large slope due to the voltage at node A being higher than 0.5 V_{in}. It enters Phase 2 with the clock tick at t_1 and the inductor current begins to decrease. This time period is longer than the balanced case of $0.5V_{in}$ due to the inductor current being charged to a higher value. At t_2, the inductor current reaches the valley threshold to enter Phase 3. The flying capacitor starts to charge the inductor again until the next clock tick at t_3. This period is shorter than $t_0 - t_1$ due to the increased amount the inductor discharges from time $t_1 - t_2$. Thus, the inductor is charged less than the previous period of $t_0 - t_1$, to result in the flying capacitor discharging less. The time for Phase 4 during $t_3 - t_4$ is shorter than that for Phase 2 during $t_1 - t_2$ due to a smaller amount of inductor current charge, resulting in the current reaching the valley threshold

sooner. The process of charging the flying capacitor longer than discharging it increases the capacitor voltage so that it reaches 0.5 V_{in}. The flying capacitor voltage balances at the point when the inductor current charging slope is the same for time $t_0 - t_1$ and $t_2 - t_3$ [3]. The process actually balances the inductor current, naturally causing the flying capacitor voltage to settle at one-half the input.

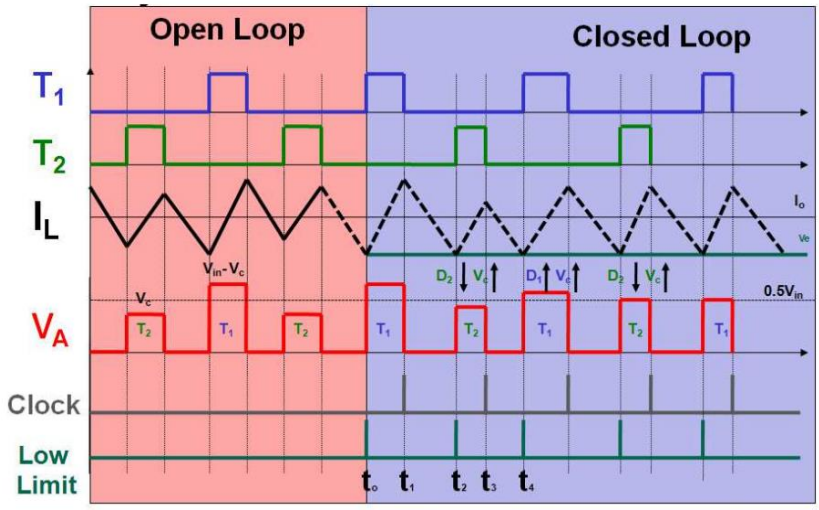


Figure 2.14 Inductor current balancing due to valley threshold when $V_c < 0.5 \cdot V_{in}$ from D. Reusch, *High Frequency, High Power Density Integrated Point of Load and Bus Converters*, Ph.D. dissertation, ECE, Virginia Tech, Blacksburg, VA, 2012. Used under fair use, 2015.

Figure 2.15 illustrates the case where the flying capacitor voltage higher than 0.5 V_{in}. The process is opposite to the previous case. The flying capacitor is discharged for a longer period of time than it being charged, which reduces the voltage toward 0.5 V_{in}. It is imperative that the flying capacitor balances at 0.5 V_{in}, so that maximum drain to source voltage of each MOSFET is 0.5 V_{in} to allow for use of low voltage devices [3].

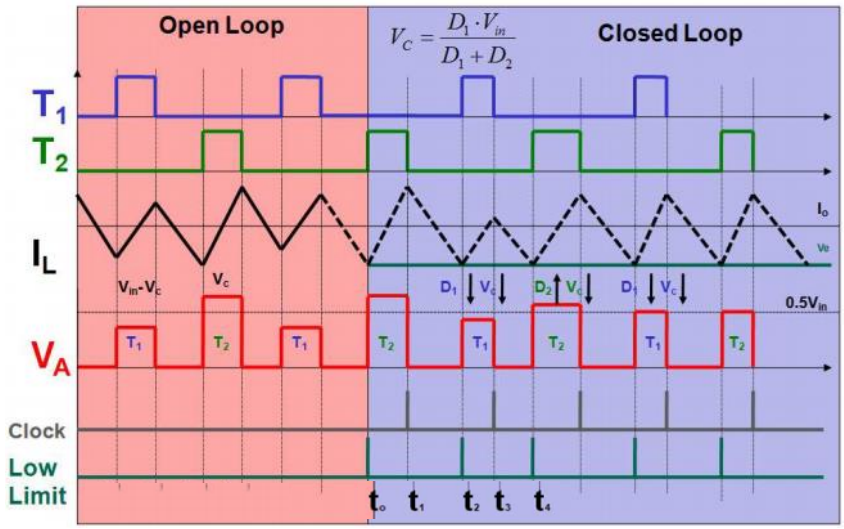


Figure 2.15 Inductor current balancing due to valley threshold when $V_c > 0.5 \cdot V_{in}$ from D. Reusch, *High Frequency, High Power Density Integrated Point of Load and Bus Converters*, Ph.D. dissertation, ECE, Virginia Tech, Blacksburg, VA, 2012. Used under fair use, 2015.

2.3.2 Low Voltage Devices

There are several factors that make using a 3-level buck converter advantageous. The biggest advantage is use of low voltage devices due to the flying capacitor being balanced at one half of the input voltage. Balancing the capacitor at one half the input voltage prevents V_{DS} of each MOSFET from exceeding one-half of the input voltage, enabling the breakdown voltage of each device to be equal to the input voltage. A low break down device has a figure of merit (FOM). FOM is the product of the $R_{DS_{on}}$ and Q_g of a MOSFET as shown, for some examples, in Figure 2.16 from [3]. Generally, the smaller the FOM, the higher the efficiency a converter can achieve.

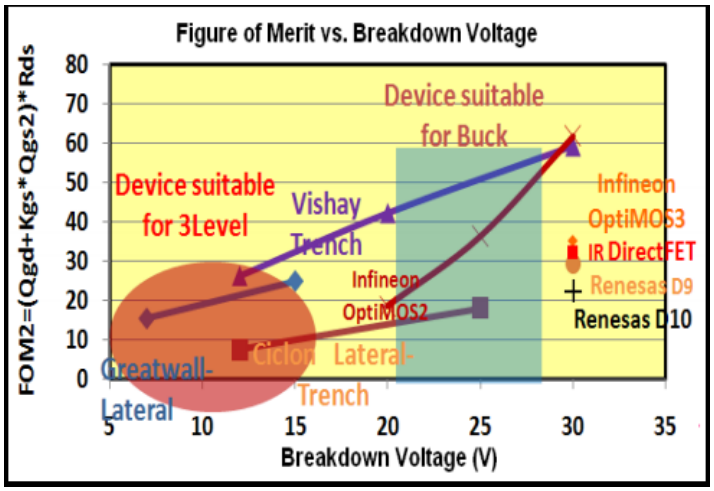


Figure 2.16 MOSFET FOM versus breakdown voltage from D. Reusch, *High Frequency, High Power Density Integrated Point of Load and Bus Converters*, Ph.D. dissertation, ECE, Virginia Tech, Blacksburg, VA, 2012. Used under fair use, 2015.

The efficiency of the 3-level buck converter is better than a traditional buck converter, for most of the load range. For example, Figure 2.17 shows the 3-level buck proposed by Reusch has an efficiency of 88% at 8.5 A compared to the traditional buck's 85%. Both converters in the figure switch at 2 MHz, but the effective output ripple frequency of the 3-level buck converter is 4 MHz. The increase in output ripple frequency allows for the inductance to be reduced from 250 nH for the traditional buck to 150 nH for the 3-level buck converter [3].

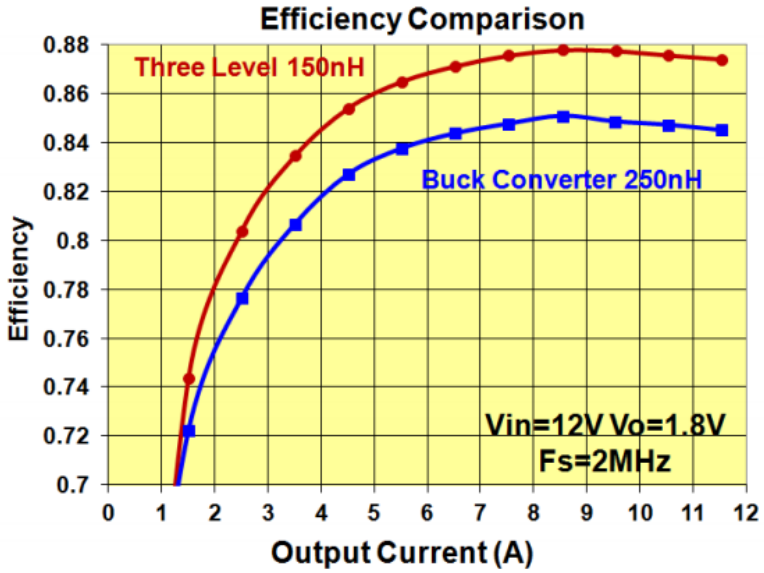


Figure 2.17 Efficiency comparison of traditional buck versus 3-level buck converter from D. Reusch, *High Frequency, High Power Density Integrated Point of Load and Bus Converters*, Ph.D. dissertation, ECE, Virginia Tech, Blacksburg, VA, 2012. Used under fair use, 2015.

2.3.3 Component Design

The components used in a 3-level buck converter are designed differently than a synchronous buck converter. The only condition considered for the designed 3-level converter is the duty cycle of less than 50%. The inductor is charged during Phase 1 and 3 of each switching period. (Refer to Section 2.3.1) It effectively doubles the output voltage ripple frequency. The inductor is designed as follows from [3].

$$L = \frac{V_{in} \cdot (0.5 - D) \cdot D}{\Delta i_L \cdot f_s} \qquad D < 0.5$$

where V_{in} is the input voltage, D is the duty cycle, L is the inductance, Δi_L is the inductor current ripple, and f_s is the switching frequency. The inductor ripple current is obtained under the assumption that the flying capacitor voltage is one-half the input voltage. Figure 2.18 compares the normalized inductance value for a 3-level buck and traditional buck converter for the same switching frequency. It can be seen that the 3-level buck converter requires smaller inductance for any duty cycle than a synchronous buck converter. The maximum normalized value is 0.25 at a duty cycle of 25% for the 3-level buck converter, while it is three times larger for a synchronous buck converter.

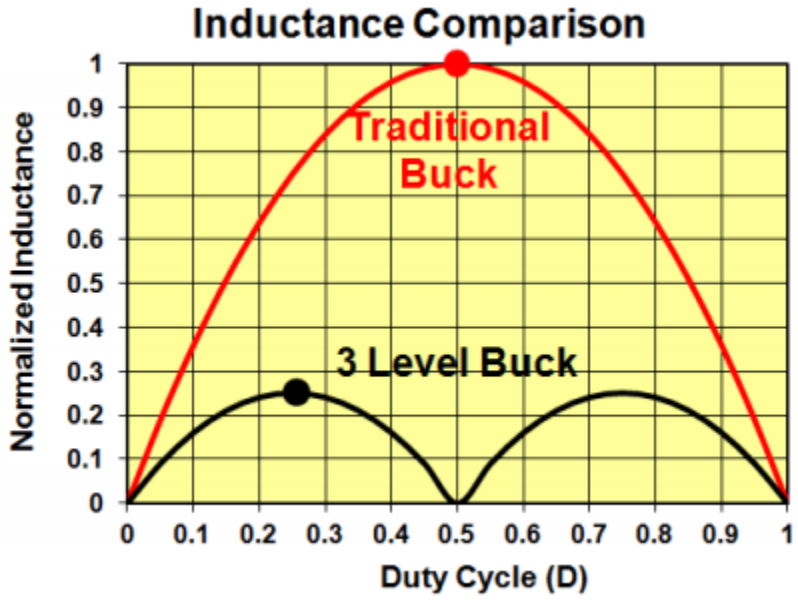


Figure 2.18 Inductance of a 3-level buck versus a traditional buck converters from D. Reusch, *High Frequency, High Power Density Integrated Point of Load and Bus Converters*, Ph.D. dissertation, ECE, Virginia Tech, Blacksburg, VA, 2012. Used under fair use, 2015.

The decrease in inductance comes from an energy source being connected to the load twice in one switching period. It also reduces the output capacitance. The output capacitance is obtained as follows [3].

$$\Delta V_o = \frac{\Delta i_L}{16 \cdot C \cdot f_s}$$

Compared to the traditional buck converter in Section 2.2, the output capacitance is reduced to one half. Smaller inductance and capacitance for the 3-level converter is highly advantageous for many applications, in which the footprint of the device is critical. However, the addition of the flying capacitor does use extra space. The flying capacitor value is obtained below from [3].

$$C_{fly} = \frac{D \cdot I_o}{\Delta v_{fly} \cdot f_s}$$

2.3.4 Shortcomings

The control scheme proposed by Reusch suffers from poor light load efficiency [3]. It is caused by adoption of constant frequency control and CCM. Constant frequency control connects the input source to the load more frequently than necessary to regulate the output voltage in light load. It wastes power in the form of conduction, switching, and gate driving losses. The inductor current is continuous in CCM, which results in larger conduction loss that causes poor light load efficiency.

2.4 Chapter summary

This chapter highlights several topics related to the proposed work. The first section describes the application, design criteria, and baseline efficiency that must be surpassed. The second section discusses the traditional buck converter followed by approaches to improve efficiency proposed by Zhou [4]. The third section discusses the two primary buck converter control methods, PWM and PFM, as well as their strengths and shortcomings. The fourth section reviews the valley current mode controlled 3-level buck converter proposed by Reusch [3]. The primary focus of the proposed converter is to address the shortcomings of the 3-level buck converter.

Chapter 3

Proposed 3-Level Buck Converter

Most converters are designed to achieve high efficiency under heavy load, which leads to overall high efficiency of converters. In contrast, the proposed 3-level buck converter intends to improve efficiency under the light load condition. High efficiency under light load is important because car black boxes are mostly in idle mode until an event is detected. In addition, black boxes are powered by the car battery when the vehicle is parked. The light load efficiency for the proposed converter is improved through PFM with a COT controller. The entire converter was designed and prototyped with discrete components on a PCB.

3.1 Specification of the Proposed Converter

The specifications of the target power stage are shown in Table 1. The 3-level buck converter is designed to regulate the output voltage at 5 V, with an input of 12 V. The load current ranges from 20 mA to 1000 mA, with a maximum output ripple of 30 mV.

Table 1 First Stage Buck Converter Specifications

Specification	Requirement
Input / output voltage	12 V / 5V
Minimum / maximum load current	20 mA / 1000 mA
Maximum output voltage ripple	30 mV

3.2 Block Diagram of the Proposed Converter

The proposed 3-level buck converter extends Reusch's CCM valley current mode control design to improve light load efficiency [3]. Reusch's converter achieves high efficiency

under the heavy load case, while taking advantage of low voltage devices. The availability to increase the light load efficiency for Reusch's converter is the focus of this thesis research. PFM is the driving factor behind light load efficiency improvements in this design. PFM reduces the switching frequency as the load demand decreases, so long as it operates in DCM. Specifically, COT valley current mode control is used.

The block diagram of the 3-level buck converter is shown in Figure 3.1. The power stage block consists of the gate drivers, MOSFETs, and inductor. The COT controller generates signals necessary for the control, while keeping the converter stable. The COT control block generates a top gate (D) and bottom gate (D') signal to drive the MOSFETs. The load current sensor block senses the load current, which is passed to the diode mode selector to decide whether to shut down the two synchronous MOSFETs Q3 and Q4 or not. When Q3 and Q4 are shut down, parallel Schottky diodes carry the load current. The diode mode selector was selected solely on power consumption. Its speed is not important because any transition delay between DCM and CCM only momentarily degrades the efficiency. On the contrary, using a fast device allows the converter to operate in the ideal operating mode at all times at the cost of lower overall efficiency. It is more important that the overall efficiency be higher than the momentary span of lower efficiency.

The gate driving signal generator block generates the gate signals for MOSFETs, Q1 through Q4, of the power stage. It consists of digital chips, which were selected based on switching speed, propagation delay, maximum supply voltage, and power consumption. Four gate drivers were used to properly drive each MOSFET with the designed control scheme. Reusch used a driving method in [3], where two complimentary gate drivers were used. One gate driver is referenced to ground in his method and the other floated between ground and the switch node between Q3 and Q4. It was a clever method of driving four MOSFETs with only two gate drivers, but it is not applicable for the proposed converter. This is explained further in Appendix A.

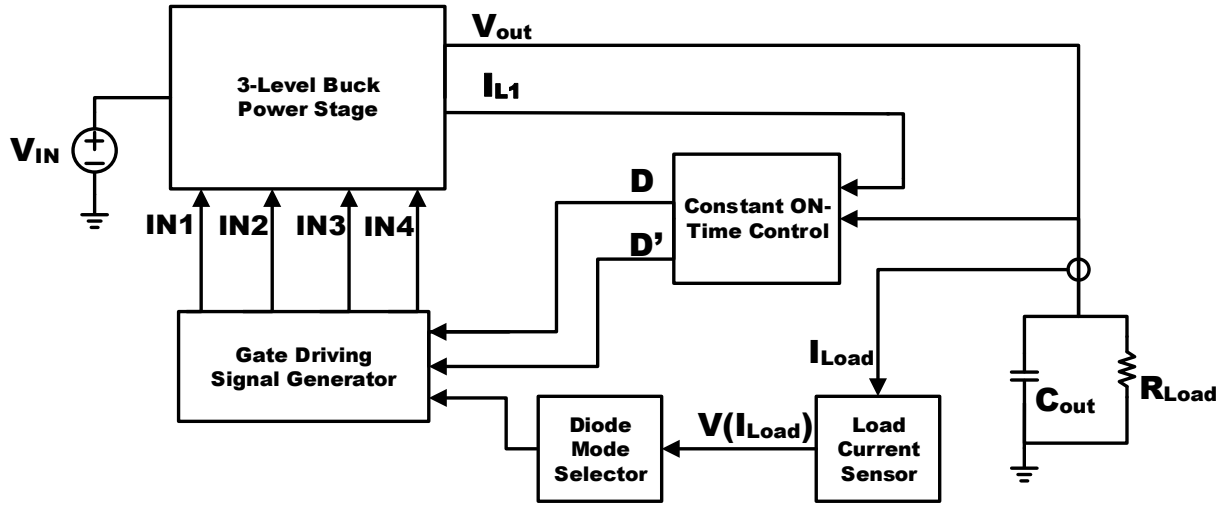


Figure 3.1 Block diagram of 3-level buck converter with control logic.

3.3 Power Stage

3.3.1 Circuit Diagram

DCM in a typical converter is realized using a diode as the bottom switch or shutting down the bottom MOSFET when the inductor current reaches zero. In either case, the inductor current is not able to flow in the reverse direction. This is important because when the inductor current reverses in direction, the output capacitor is the device supplying the power, which causes the stored energy to be wasted. DCM reduces waste and improves efficiency by only using energy in the output capacitor to supply the load.

Figure 3.2 shows the circuit diagram of the power stage of the proposed 3-level buck converter. The proposed 3-level buck converter implements DCM in the light load condition by shutting down the synchronous MOSFETs, Q3 and Q4, when the inductor current reaches zero. DCM is also realized in the very light load condition by indefinitely disabling Q3 and Q4 and allowing Schottky diodes in parallel with each MOSFET to conduct the load current in the forward direction and block it in the reverse. The implementation of DCM makes the proposed converter different from Reusch's converter [3]. The light load efficiency of Reusch's converter is poor in comparison to heavy load because it operates in CCM and continuously switches at a constant frequency independent of the load.

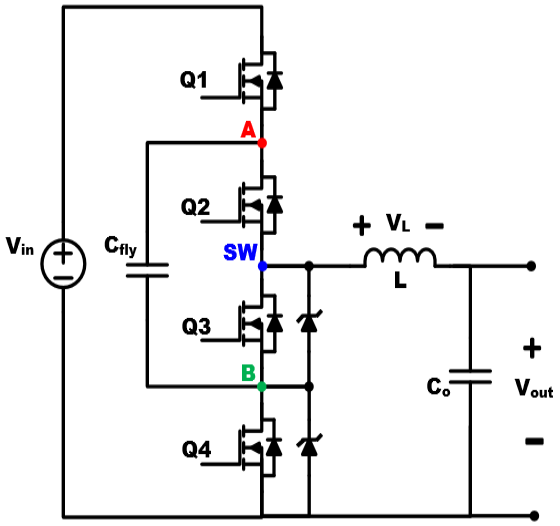


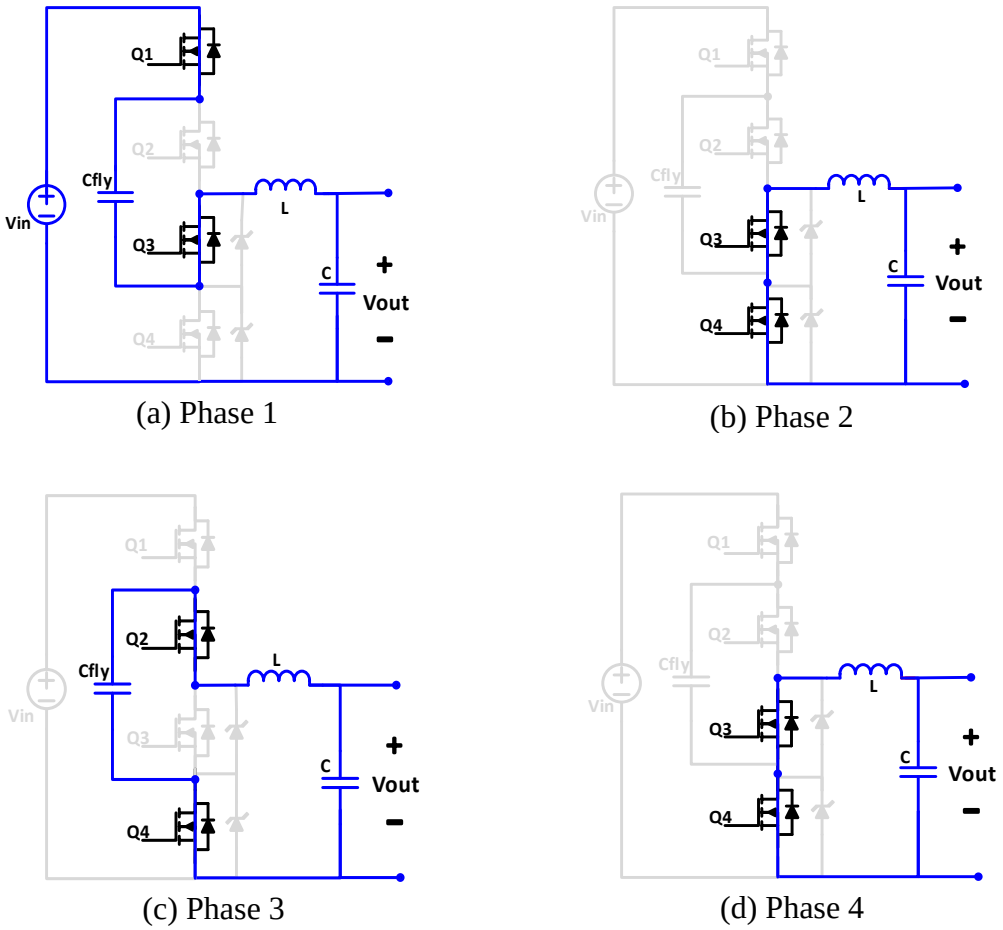
Figure 3.2 Circuit Diagram of the Power Stage of the Proposed Converter.

The power stage was designed based on the heavy load operating condition while maintaining high light load efficiency. The MOSFETs were selected from a wide range of discrete components. Texas Instruments (TI) NexFETs have good device characteristics in terms of low overall gate charge as well as on resistance. The perfect device for the 3-level buck converter would be a low voltage device, whose breakdown voltage of the MOSFET is small. After performing the survey, a 30 V device CSD16301Q2 was chosen from TI because it had the best characteristics despite its breakdown voltage being larger than necessary. More about device selection is discussed later in this chapter.

3.3.2 Phases Operation

Section 2.3.1 discusses the four phases of operation in detail. Figure 3.3 shows the four phases of operation for the proposed topology. During Phase 1, Q1 and Q3 are on to allow the input source to charge the flying capacitor, inductor, and output capacitor. Phase 2 uses the synchronous MOSFETs Q3 and Q4 to discharge the inductor to supply the load. Phase 3 operates like phase 1 in terms of charging the passive components. Q2 and Q4 are turned on to allow the flying capacitor to charge the inductor and output capacitor. Phase 4 repeats phase 2. Once phase 4 is complete, the switching period is over and cycle begins again. Under the light load condition, Q3 and Q4 are shut down when the inductor current touches zero in Phase 2 and Phase 4. They are turned back on again after Phase 1 or Phase 2 ends. The very light load

condition shuts down Q3 and Q4 indefinitely in all phases, where Schottky diodes will carry the load current.



(a) Phase 1 (b) Phase 2

(c) Phase 3 (d) Phase 4

Figure 3.3 Four Phases of operation (a) Phase 1, (b) Phase 2, (c) Phase 3, (d) Phase 4.

3.4 Control Block Diagram of the Controller

The control circuit comprises of three blocks: the controller, gate signal generation, and diode mode selector. The controller implements PFM through COT valley current mode control in DCM. The control scheme was originally tested in SIMPLIS using ideal components. The control loop consisted of a COT generator, output voltage error amplifier, inductor current sensing, and inductor current zero crossing detector. The original control method was implemented in SIMPLIS to prove the concept and allow for simulations in a different program to commence. The COT controller selected is LTC3833 from Linear Technology. After this device was selected, the entire control loop operation was tested in Linear Technology's

simulation program LTspice. The LTspice simulation included the controller, gate logic, gate drivers, and diode mode selector.

3.4.1 Contoller Design

The controller's switching frequency is based on the desired output ripple frequency of the converter. The controller senses the inductor current through the differential voltage across a sense resistor, which is compared to the reference valley current voltage generated from the error of the voltage feedback. The reference valley voltage is obtained from the error amplifier, internal to the controller, by monitoring the output voltage. Under a load step, the converter either increases or decreases the switching frequency to meet the load demand.

The inductor and the output capacitor of the 3-level buck converter are selected based on an output voltage ripple frequency of 400 kHz. Therefore, the controller's steady state switching frequency is 400 KHz and is set by the frequency set resistor in the COT control block in Figure 3.4. It is important to select the proper sense resistor so that the maximum allowable differential voltage of the controller is not exceeded. The last step is to design the compensation network. In variable frequency control, or PFM, the sample and hold effect is eliminated. Therefore, COT control double poles have little impact at half the switching frequency. The bandwidth of the control loop was designed to not exceed one-third the switching frequency following that presented by Yan [11]. This allows a proper gain and phase margin for the controller, which makes it stable.

The controller generates the COT signal for the MOSFETs and is shown in Figure 3.4. The controller was designed and verified through simulation with SIMPLIS simulation tool. The controller circuit for the simulation and simulation results are given in Appendix B. The COT valley current mode controller, LTC3833, from Linear Technology, was selected because of its wide switching frequency range [12]. The control loop is slightly different than the SIMPLIS simulation because of the addition of a very light load operation mode. This method was introduced in [4] as a way to improve light load efficiency. The very light load mode shuts down the gate driver for Q3 and Q4 and paralleled Schottky diodes carry the load current to allow for further increase in efficiency. The control scheme is implemented with one COT controller (LTC3833), one D FF (74AC11074DR), one AND chip (CD74HC08PW), one OR chip (74HCT32PW), one current sense chip (LT6105), one low power comparator (LTC1440),

and four gate drivers (LTC4440-5). The control loop design was simulated and tested in LTspice to verify its operation. A block diagram of the control loop is shown below in Figure 3.4.

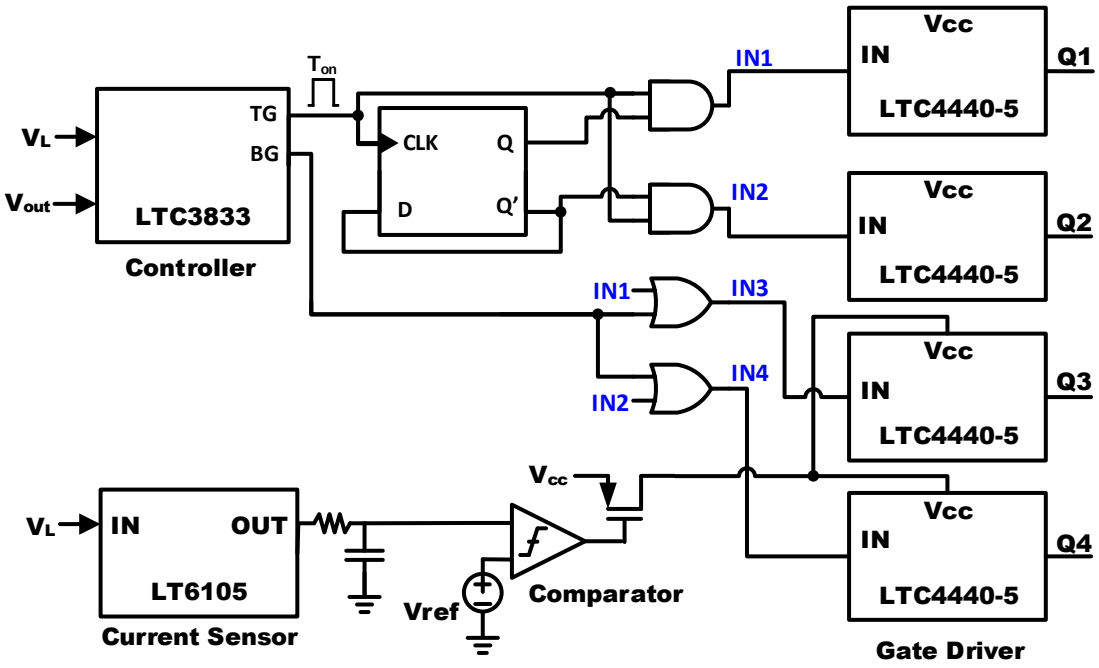


Figure 3.4 Control loop of the prototyped converter.

The controller generates the COT signal for the top and synchronous MOSFETs and is shown in Figure 3.4. Since Q1 and Q2 must be driven 180 degrees out of phase, a D FF is used to alternate the on-time signal between each gate. The D FF is setup as a toggle [13] that changes its state at the rising edge of the COT one-shot. The on-time from the COT controller and the output of the D FF are ANDed together to create the proper driving signals for Q1 and Q2, which are then passed to their respective gate drivers. The bottom gate signal from the COT controller is passed through the AND gate to delay the signal, so that it does not overlap with the on-time. This is important because the gate drivers are individual and do not have any built in dead time. Therefore, the dead time from the COT controller is used to make sure shoot-through does not occur. The ANDed bottom gate signal is then ORed with the driving signal for Q1 and Q2. The driving signal for Q3 is the OR of Q1 and bottom gate, while Q4 is the OR of Q2 and the bottom gate signal. DCM is implemented by using the bottom gate signal from the controller which allows for Q3 and Q4 to be turned off when the inductor current reaches zero.

It is important to note that the AND chip was picked first and a similar OR gate was selected to ensure that they had the same propagation delay time [14] [15].

The driving signals applied to the gate drivers are level shifted by the driver according to the source of the driven MOSFET. The LTC4440-5 gate driver is a single MOSFET driver that uses a bootstrap capacitor to level shift the gate signal above the MOSFET source to turn the device on [16]. Since each MOSFET is driven by its own gate driver, dead time is implemented on the input side of the driver.

The current sense and comparator chips were selected primarily based on power consumption. These chips operate throughout the entire load range, but only help improve the efficiency when the load current becomes small. Therefore, its speed is not important because the converter still operates correctly regardless of how fast the devices respond. LT6105 is a micropower, precision current sense amplifier that is capable of 100 V/V gain from the input differential voltage to the output voltage [17]. It is responsible for taking the differential voltage seen across the current sense resistor and applying a gain allowing for it to be compared to a reference. The output of the current sense chip is passed through a RC lowpass filter to obtain the average value of the load current. The filtered load current information is given to the LTC1440 comparator, which is an ultra-low power comparator that has a built in reference and hysteresis [18]. The comparator disables Q3 and Q4's gate driver when the load current voltage is below the reference voltage. The gate drivers are disabled by turning off a P-MOS switch in series between the power supply and the supply pin of the chip.

3.4.2 Operation under Three Different Load Conditions

This section describes different operation modes for the converter under three different load conditions, heavy load, light load, and very light load. Heavy load causes the device to operate under CCM, while light load and very light operation are under DCM. The very light load condition shuts down the gate driver for Q3 and Q4 to allow a Schottky diodes to conduct the load current while operating in DCM.

A. Heavy Load

The 3-level buck converter operates in CCM when the load current is above 330 mA and the input voltage is 12 V. All four MOSFETs, Q1 – Q4, are switching during this mode of

operation. Figure 3.5 shows a timing diagram of each gate driver input and output in CCM under the heavy load case. The inductor current ripple is designed under CCM to be 660 mA peak to peak with an input of 12 V at a maximum load current of 1 A and switching frequency of 400 kHz. The inductor current does not flow in reverse in this mode because the ripple is 330 mA. Thus, the transition point between CCM and DCM is at an average load current of 330 mA. DCM is used to turn off Q3 and Q4 within the switching period to improve efficiency by preventing the inductor current from flowing in the reverse direction. CCM operation allows for the switching frequency of 400 kHz to maintain the output voltage and load current.

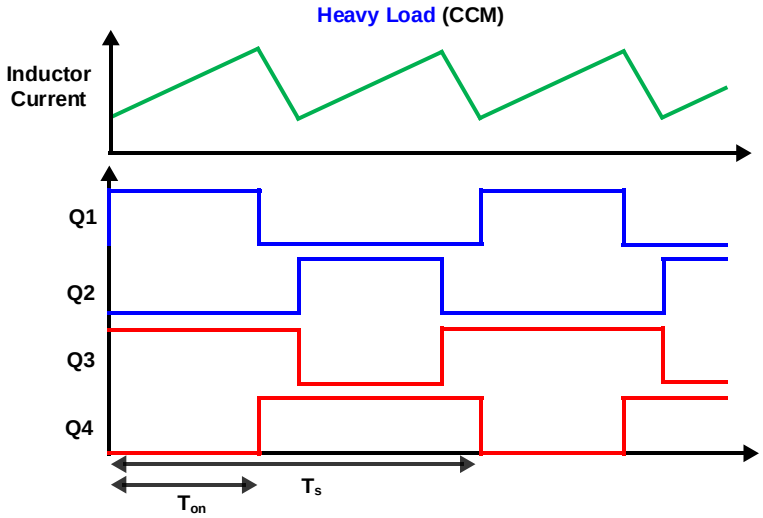


Figure 3.5 Heavy load timing diagram.

B. Light Load

The light load current ranges from 12 mA to 330 mA, where the converter is operating in DCM. The converter enters DCM by turning off Q3 and Q4 when the inductor current reaches zero. The Schottky diodes in parallel with Q3 and Q4 are not used in this load range. The next gate signal for Q1 or Q2 is generated when the output voltage droops below a voltage threshold within the controller. DCM delays the next switching cycle until the output capacitor cannot supply the load any more. This allows the switching frequency to decrease and the efficiency to increase. The increase in efficiency comes from the reduction in gate driving and conduction loss. Figure 3.6 shows a timing diagram of each gate driver input and output in DCM.

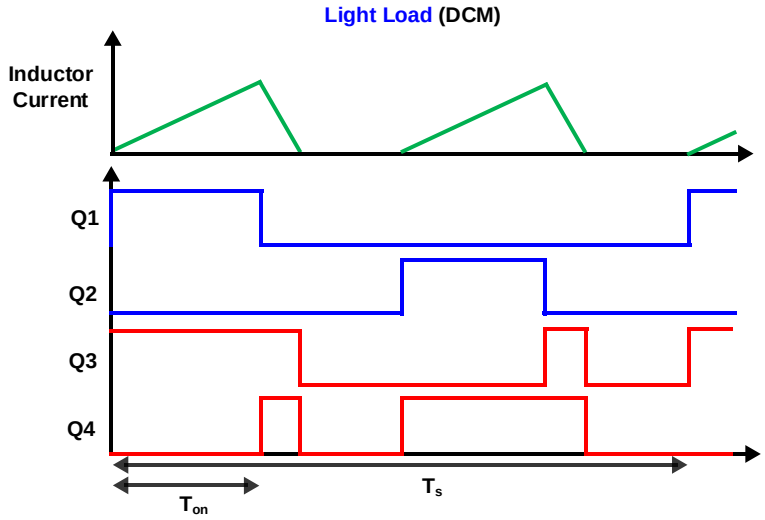


Figure 3.6 Light load timing diagram.

C. Very Light Load

The diode mode selector is used for the very light load case and shuts down the bottom two MOSFETs completely when the load current falls below 12 mA. The bottom MOSFETs are shut down by turning off the supply voltage of gate drivers for Q3 and Q4. The Schottky diodes in parallel with Q3 and Q4 conduct the load current and prevent the inductor current from reversing in direction. The efficiency is able to improve further than the previous mode of DCM because the gate driver loss of Q3 and Q4 are eliminated. Similar to the light load case, the next switching period is determined by the output voltage droop. The main difference between the two light load modes of operation is that Q3 and Q4 never switch in very light load; whereas in the light load, Q3 and Q4 switch and are turned off only when the inductor current reaches zero. The reason for not switching the synchronous gates is the ability to reduce the gate charge and gate driver loss, which is much greater than the added conduction loss from the forward drop of the diode. Figure 3.7 shows a timing diagram for the converter operating under the very light load case. The discrete realization of the diode mode selector circuit is not ideal due to the large amount of power still being consumed by the two other gate drivers and the controller. To increase the efficiency under very light load, the controller need to shut down all unnecessary functions other than monitoring the output voltage.

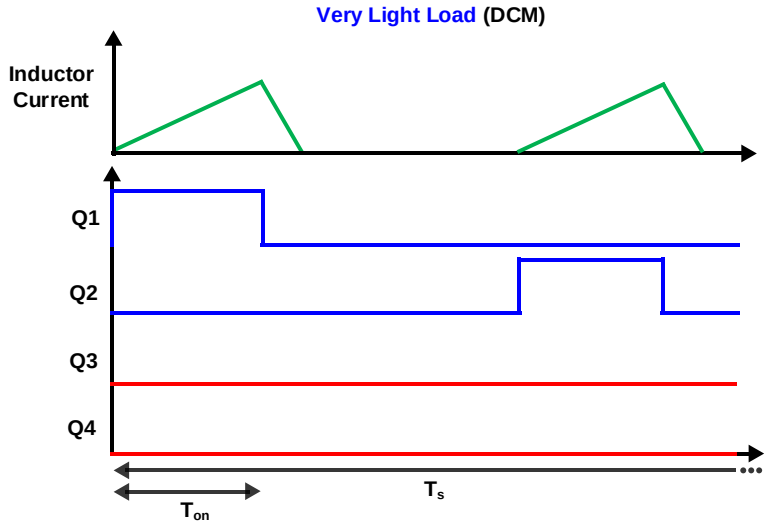


Figure 3.7 Very light load timing diagram.

3.4.3 Bandwidth of the Controller

The control loop should provide stability as well as fast response to load changes. The bandwidth of the control loop indicates how quickly the device can respond to a transient. The LTC3833 controller adopts a Type 3 voltage compensator, which is external to the controller chip itself. LTpowerCAD II is used to design the resistor and capacitor network that, in conjunction with the error amplifier, acts as the compensator for the LTC3833 controller [19]. The program allows for the compensator to be designed based on the input voltage, output voltage, load current, inductor, current sense resistor, output capacitance, and switching frequency. In LTpowerCAD II, the converter topology for the LTC3833 controller is a traditional buck, which makes the compensator design different for the proposed control loop. The input voltage for the proposed controller is the flying capacitor voltage, due to the inductor being charged with a maximum voltage of one-half the input voltage. Also, the controller switching frequency is set to two times the actual switching frequency because the output ripple frequency is doubled. Designing in this manner allows the compensator to be calculated based on what the controller is actually sensing when the converter is running.

Figure 3.8 shows the bandwidth of the converter from LTpowerCAD II. The bandwidth of the control loop is made much lower than the switching frequency of the converter. The phase margin of the converter was designed to be greater than 45 degrees and the gain margin to

be larger than 10 dB, which allows for greater stability. The unit gain bandwidth of the converter is 43.65 kHz with a phase margin of 67.68 degrees and a gain margin of 20 dB.

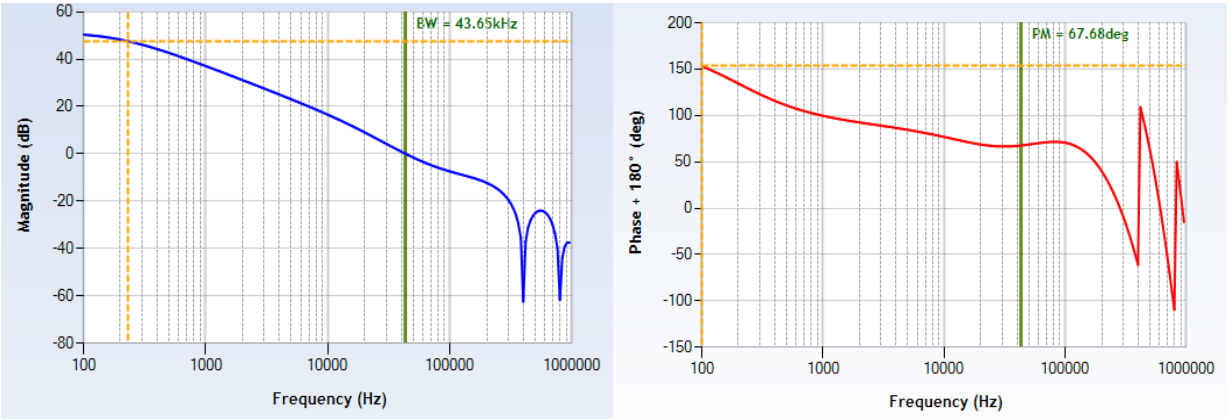


Figure 3.8 Control loop bandwidth of converter from LTpowerCAD II.

3.4.4 Gate Driving Circuit

Figure 3.9 shows the gate driving circuit and the power stage of the 3-level buck converter. Like a typical buck converter, the gate driving circuit for the 3-level buck converter uses gate drivers with bootstrap capacitors to drive the MOSFETs. The bootstrap capacitor is necessary only for the top three gates, Q1 – Q3, as the bottom Q4 is referenced to ground. Q2 and Q3 bootstrap capacitors are charged with a 5 V supply. Q1 bootstrap capacitor is charged using Q2 capacitor, because the two capacitors are connected in parallel when Q2 is on. Figure 3.10 shows how Q1 bootstrap capacitor is charged when Q2 is switched on.

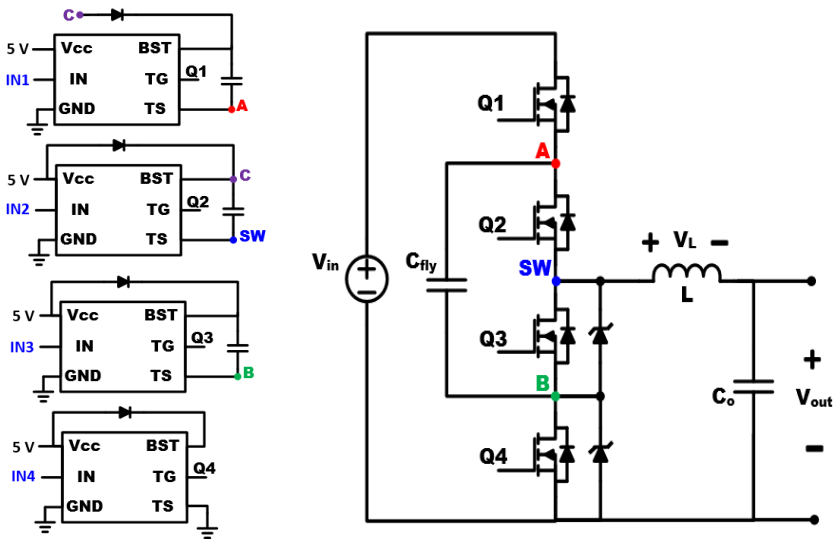


Figure 3.9 3-level buck converter gate drivers and the power stage.

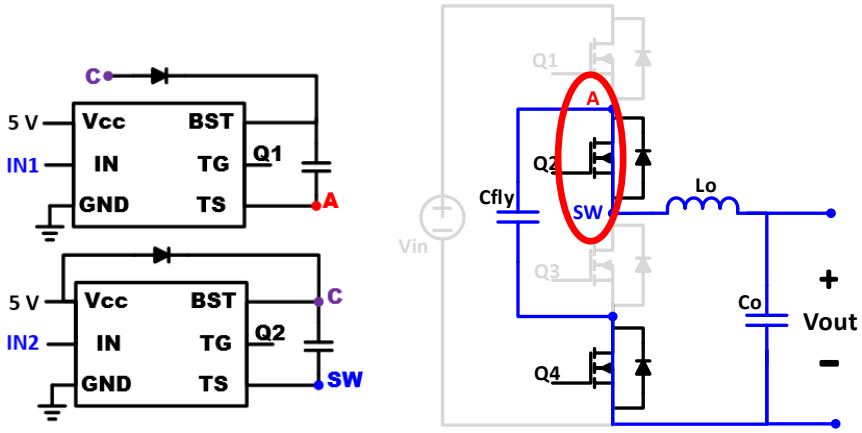


Figure 3.10 Node A and SW are connected, allowing Q1 bootstrap capacitor to charge.

The only drawback to the design is that the converter should start in CCM to charge the bootstrap capacitor for Q2 properly. For further understanding, assume the output capacitor is initially completely discharged. Consider the load is light where the converter operates in DCM mode, and the bottom MOSFETs, Q3 and Q4, are disabled. The supply voltage charging the bootstrap capacitors must be higher than 5 V for a short period of time upon start up if Q3 and Q4 are shut off. This is because the bootstrap Q2 capacitor is charged through the inductor and output capacitor. Because the output capacitor starts completely discharged, it begins to charge through the bootstrap capacitor path for Q2. When the output fully charges, the bootstrap capacitor has no charge on it due to the output voltage and supply voltage for the capacitor being equal to 5 V. Thus, Q2 never fully turns on to allow for Q1's bootstrap capacitor to

charge and the converter fails to operate properly because the input power is never utilized. Now, consider the converter being able to start under CCM. By allowing the converter to switch Q3 and Q4, the bootstrap capacitor for Q2 is able to charge through the synchronous MOSFETs to ground. The converter is then able to transition between CCM and DCM because the bootstrap capacitors are fully charged and the nominal 5 V supply can be used.

3.5 Component Design and Selection

An important design process is selecting components of the power stage including MOSFETs, an inductor, an output capacitor, and a flying capactor. The inductor and capacitor values usually are chosen considering the worst case situation which is the highest input voltage and load current. However, the proposed converter aims to achieve high efficiency under light load when the car engine is turned off. Therefore the design is done at the input voltage of 12 V. The converter's components are designed based on operation in CCM at the worst case load condition of 1 A at a switching frequency of 200 kHz. The major difference between the traditional design for a buck covnerter is that the inductor current ripple for the proposed design is 66%, which is larger than the suggested value of 20-40% stated in Section 2.2. The switching frequency of 200 kHz was set to a similar value of the buck converter selected by KAIST, which is used for the ACT4070B buck converter [20], to allow for a fair comparison.

The inductor value is chosen based on the load current it is desired for the converter to switch between CCM and DCM operations. A smaller inductor value makes the converter enter DCM earlier, which increases the output voltage ripple with the same capacitance. Thus, it is necessary to increase the output capacitance to meet the specification for the output ripple. The inductance is obtained according to Equation 3.3.1 suggested by Reusch in [3].

$$L = \frac{V_{in} \cdot (0.5 - D) \cdot D}{\Delta i_L \cdot f_s} \qquad D < 0.5 \tag{3.3.1}$$

where $V_{in} = 12$ V, $V_{out} = 5$ V, $D = \frac{V_{out}}{V_{in}} = 0.416$, $f_s = 200$ kHz, $\Delta i_L = 66\% \cdot I_o = 660$ mA.

The inductance is 3.3 µH based on ripple current of 660 mA which makes the critical load current 330 mA. The critical load current is defined as the point the inductor curent begins to go negative, which is when the converter should begin to enter DCM. The closest inductor selected from Coilcraft (EPL7040-332MEB) is 3.3 µH with a DCR of 15 mΩ [21]. The large inductor

current ripple of 660 mA was chosen, so that the converter enters DCM.

Next, the output capacitance value was selected based on of the inductor current ripple and obtained as in Equation 3.3.2 [3].

$$C_{out} = \frac{\Delta i_L}{16 \cdot f_s \cdot \Delta v_o} \tag{3.3.2}$$

where $f_s = 200\ \text{kHz}$, $\Delta i_L = 0.66 \cdot I_o = 660\ \text{mA}$, and $\Delta v_o = 30\ \text{mV}$. The value calculated is $C_{out} = 6.8\ \mu\text{F}$. This value was tuned using LTspice to make sure the voltage ripple of 30 mV lies within specification in DCM. The value found to best suit the device was $C_{out} = 120\ \mu\text{F}$. The large value for C_{out} is necessary to keep the output voltage ripple within specification when the switching frequency reduced to its minimum of 5 kHz. The flying capacitor value is obtained next from Equation 3.3.3 [3].

$$C_{fly} = \frac{D \cdot I_o}{\Delta v_{fly} \cdot f_s} \tag{3.3.3}$$

where $f_s = 200\ \text{kHz}$, $D = \frac{V_{out}}{V_{in}} = 0.416$, $I_o = 1000\ \text{mA}$, and $\Delta v_{fly} = 50\ \text{mV}$. The capacitor value is $C_{fly} = 28.2\ \mu\text{F}$. The flying capacitor should be ceramic to reduce the ESR, which will allow for less conduction loss and higher efficiency. Three ceramic capacitors of 10 μF in parallel are used for the proposed design to reduce the ESR and RMS current each capacitor sees.

A main advantage of the 3-level buck is the ability to use low breakdown voltage devices. For this application, the necessary breakdown voltage of each MOSFET is equal to the input voltage of 14.2 V. After a survey of off-the-shelf MOSFETs, Texas Instruments NexFETs is the most suitable for the current level of 1 A required for this application. In order to choose the most suitble device for the application, the FOM for MOSFETs, shown in Equation 3.3.4, is used to select a few candidates. The FOM is product of the MOSFET on-resistance $(R_{DS_{on}})$ and gate charge (Q_g) [22].

$$\text{FOM} = R_{DS_{on}} \cdot Q_g \tag{3.3.4}$$

Three TI MOSFET candidates, with a breakdown voltage between 20 and 30 V, are identified based on each FOM and listed in Table 2.

Table 2 MOSFET Survey of TI NexFETs [23] [24] [25].

Name	V_{BR}	Q_{gd}	C_{oss}	$R_{DS_{on}}$(@5V)	Q_g(@5V)	FOM $\left(R_{DS_{on}} \cdot Q_g\right)$
CSD17571Q2	30 V	0.6 nC	101 pF	23 mΩ	2.6 nC	59.8 mΩ · nC
CSD15571Q2	20 V	0.66 nC	184 pF	15 mΩ	2.8 nC	42 mΩ · nC
CSD16301Q2	**25 V**	**0.4 nC**	**165 pF**	**23 mΩ**	**2.2 nC**	**50.6 mΩ · nC**

Generally, a low FOM is a good starting point to narrow down MOSFET candidates, but the lowest FOM does not always achive the highest overall efficiency. There is a tradeoff between conduction and gate driving loss that must be considered based on the application. A device with a lower gate charge reduces the amount of power dissipated during charging and discharging the gate, which is shown in the Equation 3.3.5 [22].

$$P_g = V_{gs} \cdot Q_g \cdot f_s \tag{3.3.5}$$

where V_{gs} is the gate to source voltage applied by the gate driver. It is advantageous to have a lower Q_g under light load because the converter loss is primarily dominated by gate driving loss and not conduction losses. The opposite is true under heavy load. The 3-level buck converter has four phases of operation, but only two phases, Phase 1 and Phase 2 shown in Figure 3.3, need to be considered. A device with a low on-resistance reduces the amount of conduction loss and is shown in Equation 3.3.6 and 3.3.7 [22].

$$P_{cond_{Q1Q3}} = I_o^2 \cdot 2 \cdot R_{DS_{on}} \tag{3.3.6}$$

$$P_{cond_{Q3Q4}} = I_o^2 \cdot 2 \cdot R_{DS_{on}} \tag{3.3.7}$$

where $P_{cond_{Q1Q3}}$ is the power dissipated when Q1 and Q3 are on during Phase 1 in Figure 3.3 and $P_{cond_{Q3Q4}}$ is the power dissipated when Q3 and Q4 are on under Phase 2. Q2 is not considered in the conduction loss calculations because it is on during Phase 3, which is identical to Phase 1 with the use of the flying capacitor as the power source. In addition to the above two losses, several other losses should also be considered to determine which MOSFETs to use. Switching loss, reverse recovery loss, and C_{oss} loss are all important and increase with switching frequency. Switching loss is the loss generated by the load current continuing to flow through the MOSFET while the device turns off. C_{oss} comes from the capacitance across V_{DS}

charging when the device turns off. Body diode conduction loss is also important to consider and primarily depends on dead time; however, dead time was not adjustable in the proposed design so it will not be considered. The power for those losses are expressed as follows [22].

$$P_{sw} = \frac{V_{off} \cdot I_o \cdot f_s}{2} \cdot \frac{Q_g}{I_{driver}} \tag{3.3.8}$$

$$P_{C_{oss}} = \frac{C_{oss} \cdot V_{off}^2 \cdot f_s}{2} \tag{3.3.9}$$

$$P_{Qrr} = Q_{rr} \cdot f_s * V_{off} \tag{3.3.10}$$

The most practical way to select MOSFETs is a loss breakdown comparison. Figure 3.11 shows calculated values for the loss breakdown for each MOSFET under heavy load in CCM. Q_{rr} loss, which is the body diode reverse recovery loss, is not considered for each MOSFET because a Schottky diode is in parallel with Q3 and Q4 that causes this loss to be constant across all operating conditions.

Figure 3.11 shows the losses each MOSFET will see in CCM and at a load current of 750 mA.

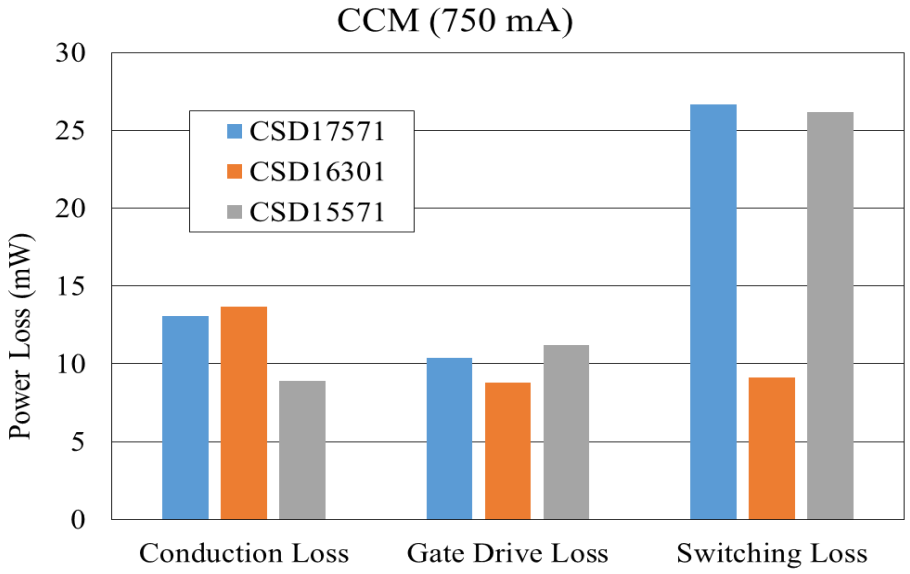


Figure 3.11 CCM loss breakdown of each MOSFET.

Figure 3.12 shows the loss of each MOSFET in DCM and at a load current of 100 mA. CSD16301 has the least amount of loss and will yield the highest efficiency under this load condtion.

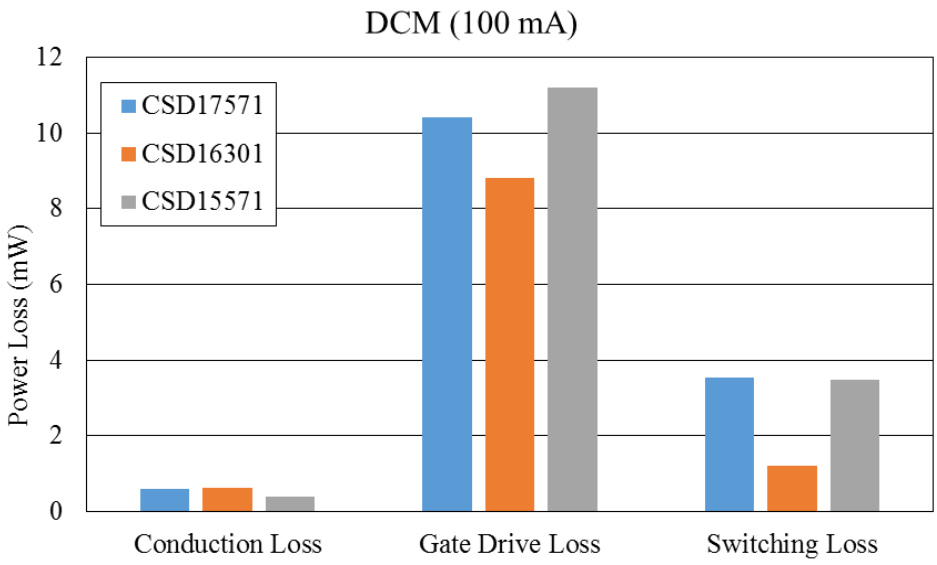


Figure 3.12 DCM MOSFET Loss at 100 mA.

CSD16301Q2 MOSFET achieves the highest efficiency under light load and is selected for the proposed converter.

3.6 Chapter Summary

This chapter describes the controller design for the 3-level buck converter. It explains how the converter operates through the entire load range. SIMPLIS simulation verifies the operation of the controller using COT valley current mode control and DCM. The power stage of the converter is designed to achieve optimal performance under light load with input voltage of 12 V. It also describes various trade-offs involved in the design process.

Chapter 4

Experimental Results

This chapter describes experimental results of the proposed 3-level buck converter. There are several iterations of efficiency measurements to show how the efficiency changes in CCM, DCM, and with the diode method implemented. All output ripples under different loads are within specification. The transient response of the device is tested to show that the converter is stable.

4.1 Measurement Setup

4.1.1 Measurement Setup

Each device was supplied with the appropriate voltage from power supplies. The digital chips (such as D FF, AND, OR in Figure 3.4) and the gate drivers (LTC4440-5) were powered with a 5 V supply. The controller (LTC3833) is also supplied with 5 V, which allows proper pulse skipping. Details on LTC3833 are discussed in Appendix C.

The PCB of the proposed 3-level buck converter was laid out in Eagle schematic editor, and populated with surface mounted discrete components. The prototype is shown in Figure 4.1.

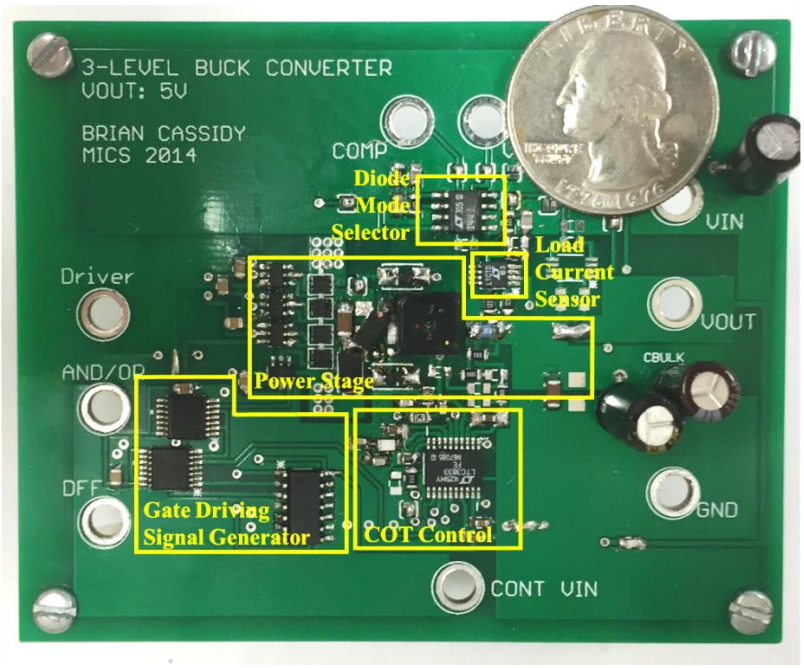


Figure 4.1 Prototype of the Proposed Converter. Photos by author.

Six digital multi-meters (Agilent 34401A) were used to measure the current into the power stage, load, controller, digital gates, diode mode selector, and gate drivers. A linear regulated, two-quadrant power supply (Hameg HM8143) was used to supply power to the power stage as well as sink the current from the load. The electronic load has the ability to adjust the load by 1 mA up to a maximum load of 2000 mA [26]. Two triple output DC power supplies (Agilent E3631A) were used to supply power to the gate drivers, digital chips, diode mode selector, and controller. A four channel, isolated oscilloscope (Tektronix TPS 2024B) was used to measure the output voltage ripple, inductor current ripple, flying capacitor voltage, and gate drive signals. Figure 4.2 shows the efficiency measurement test setup.

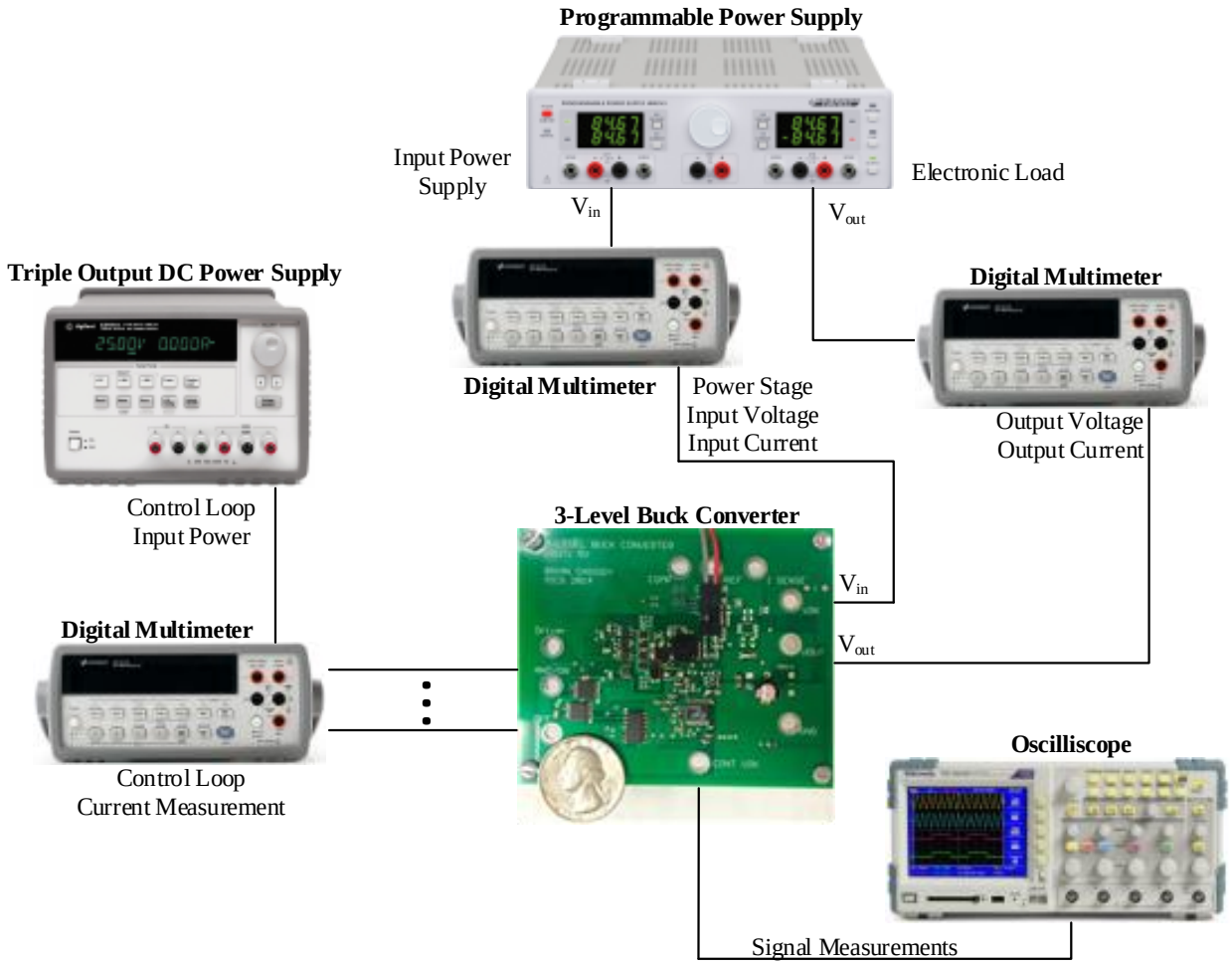


Figure 4.2 Efficiency measurement test setup. Agilent E3631A from http://www.testequipmentdepot.com/usedequipment/images/e3631a.jpg, 2015. Tektronix TPS2024B from http://www2.tek.com/cmsreplive/psrep/img/13304/A003_0395-L.jpg, 2015. Hameg HM8143 from http://www.rohde-schwarz.com/en/product/hm8143-productstartpage_63493-43458.html, 2015. Agilent 34401A from http://www.testunlimited.com/productdetail.aspx?product_id=117, 2015. Used under fair use, 2015.

Figure 4.3 shows the test setup for the load transient test. A triple output DC power supply (Agilent E3631A) was used to supply the control loop with 5 V and the power stage with 12 V. An electronic load (Transistor Devices RBL488 100-120-800) was used under constant current pulse mode to generate the required load step [27]. A four-channel isolated oscilloscope (Tektronix TPS2024B) was used to observe the inductor current as the load changes. A four-channel oscilloscope (Tektronix MSO5000) was used to observe the output voltage overshoot and undershoot as well as the monitoring the switching frequency with each load step.

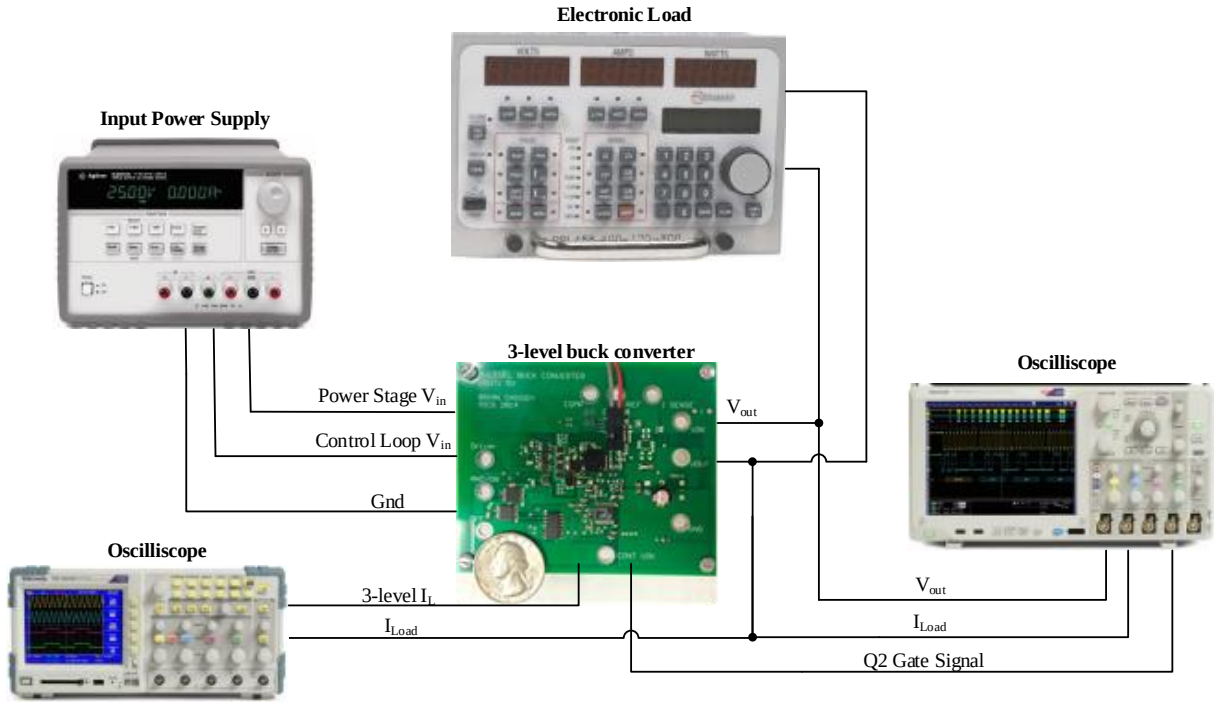


Figure 4.3 Load transient test setup. Agilent E3631A from http://www.testequipmentdepot.com/usedequipment/images/e3631a.jpg, 2015. Tektronix TPS2024B from http://www2.tek.com/cmsreplive/psrep/img/13304/A003_0395-L.jpg, 2015. Agilent 34401A from http://www.testunlimited.com/productdetail.aspx?product_id=117, 2015. Tektronix MSO5000 from http://www.tek.com/oscilloscope/mso5000-dpo5000, 2015. Transistor Devices RBL488 100-120-800 from https://accusrc.com/product.php?id=7284, 2015. Used under fair use, 2015.

4.2 Measurement Results

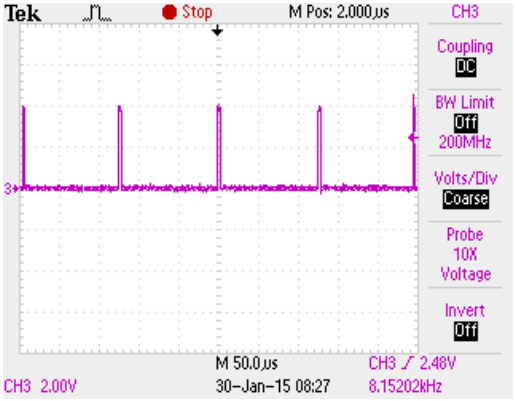
This section presents the measured efficiency across the entire load range as well as the loss breakdown. The subsection for transient waveforms shows how the switching frequency changes under DCM and stays constant under CCM. It also shows the output voltage ripple under the two operating conditions. The transient response of the converter is shown to display the overshoot and undershoot of the output voltage due to a load step. The subsection for efficiency shows efficiency curves under CCM, and DCM with/without Schottky diodes. The last subsection shows the loss breakdown.

4.2.1 Transient Waveforms

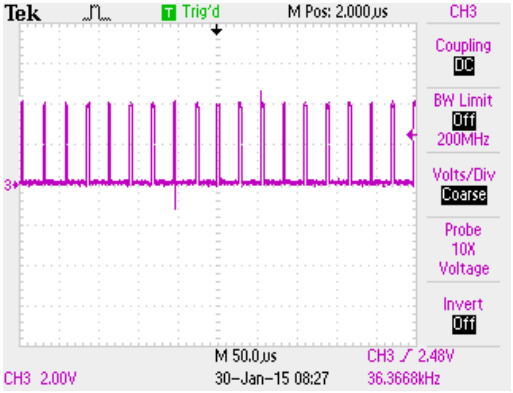
4.2.1.1 Light Load

The light load of the converter ranges from 20 mA to 330 mA, in which the converter operates in DCM. The 3-level buck converter is designed to enter DCM when the load current drops below 330 mA or the output power below 1650 mW. The switching frequency of the converter reduces as the load current decreases in DCM. Figure 4.4 shows the switching frequency change as the load changes.

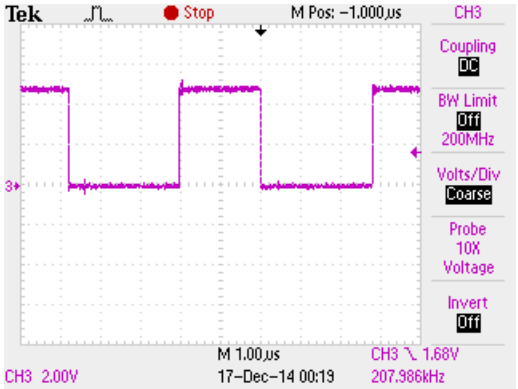
(a) f_s = 5.7 kHz, I_o = 10 mA



(b) f_s = 11 kHz, I_o = 20 mA



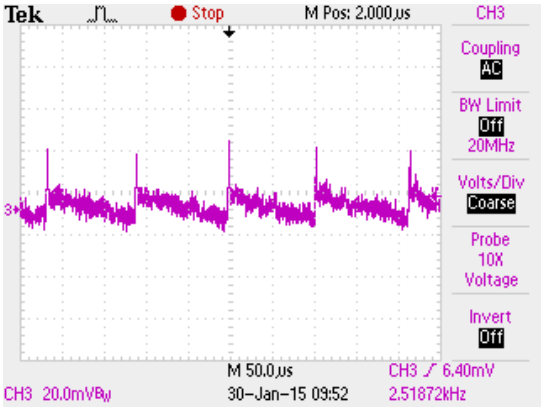
(b) f_s = 49 kHz, I_o = 100 mA



(b) f_s = 207 kHz, I_o = 350 mA

Figure 4.4 Switching frequency versus load current under light load.

The output voltage ripple at 10 mA is shown in Figure 4.5. Light load incurs a larger output ripple than heavy load, and the output ripple should be within the specification of 30 mV for light load. The output ripple frequency in the figure is two times the switching frequency, which verifies the correct operation.

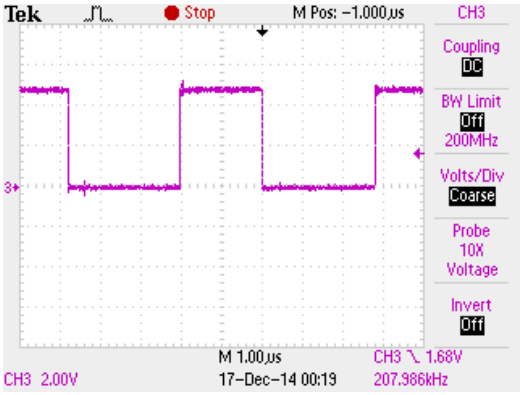


(a) $V_r = 30$ mV, $f_o = 11.2$ kHz, $I_o = 10$ mA

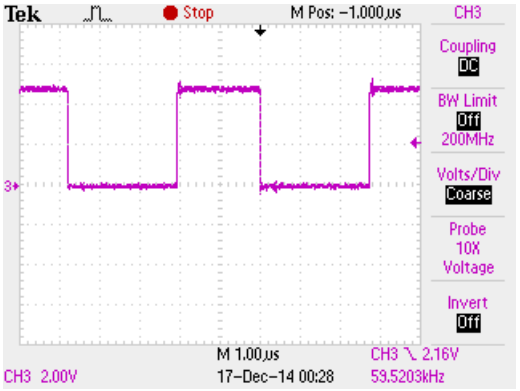
Figure 4.5 Output ripple voltage, frequency, and load current load current under light load.

4.2.1.2 Heavy Load

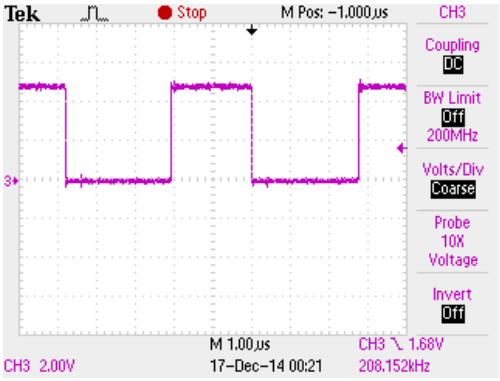
The heavy load for the converter ranges from 330 mA to 1000 mA, in which the converter operates in CCM. The 3-level buck converter is designed to enter CCM when the load current reaches above 330 mA or the output power in 1650 mW. At this point, the switching frequency of the converter remains at 200 kHz with an output ripple frequency of 400 kHz. Figure 4.6 shows how the switching frequency does not change the load changes.



(a) f_s = 208 kHz, I_o = 350 mA



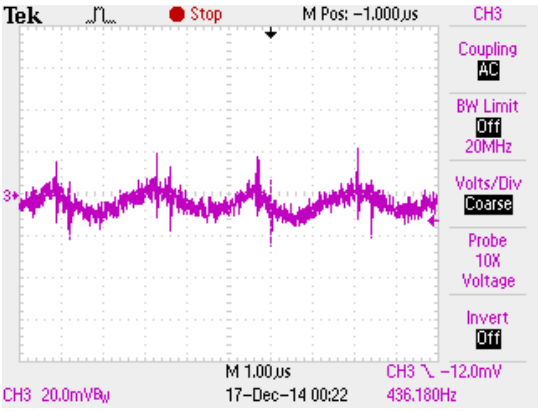
(b) f_s = 208 kHz, I_o = 750 mA



(c) f_s = 208 kHz, I_o = 1000 mA

Figure 4.6 Switching frequency versus load current under heavy load.

The output voltage ripple at maximum load is shown in Figure 4.7. The converter has the same output voltage ripple of 20 mV in CCM under heavy load because the switching frequency remains the same.



(c) V_r = 20 mV, f_o = 416 kHz, I_o = 1000 mA

Figure 4.7 Output ripple voltage under maximum load.

4.2.1.3 Load Trasient Performance

Figure 4.8 and Figure 4.9 show the transient response of the 3-level buck converter with a load step up from 100 mA to 500 mA. Figure 4.8 shows the load current, output voltage, and the gate signal for Q1. The gate signal of Q1 is displayed to show the switching frequency changing with the load step. The yellow line in Figure 4.8 is the load current, which changes from 100 mA to 500 mA in 68 µs. The blue line shows the output voltage ripple. There is no undershoot in the output voltage because the converter is able to assume the change in current. The load step is too slow to cause the converter to become overloaded. The output voltage ripple is greater than 30 mV causing it to fail to meet the specification under transient operation. Therefore, it requires future investigation to ensure the ripple does not damage any devices or improve the design to meet the specification. The purple line is the gate signal for Q1, which shows the switching frequency increases as the load increases. Figure 4.9 shows the load current and inductor current. The yellow line in Figure 4.9 shows the load current, which changes from 100 mA to 500 mA. The purple line shows the inductor current, which switches from DCM to CCM as the load current increases.

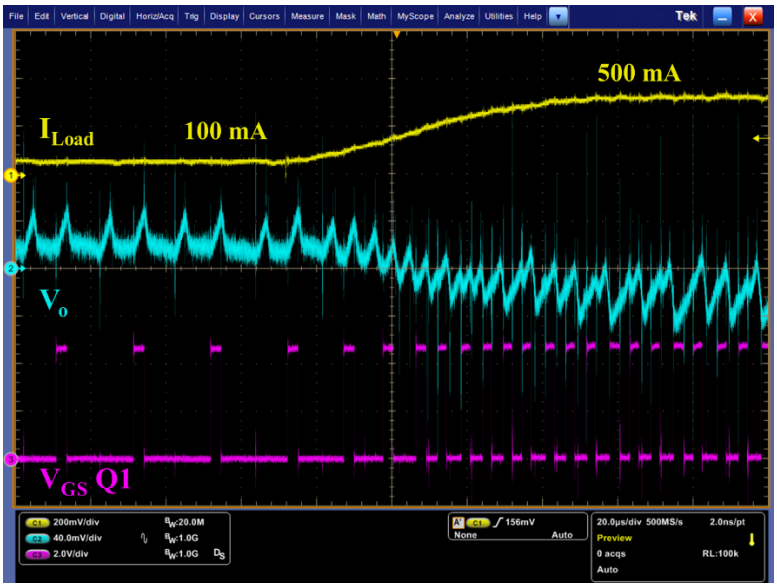


Figure 4.8 Output voltage and Q1 gate signal due to load step up.

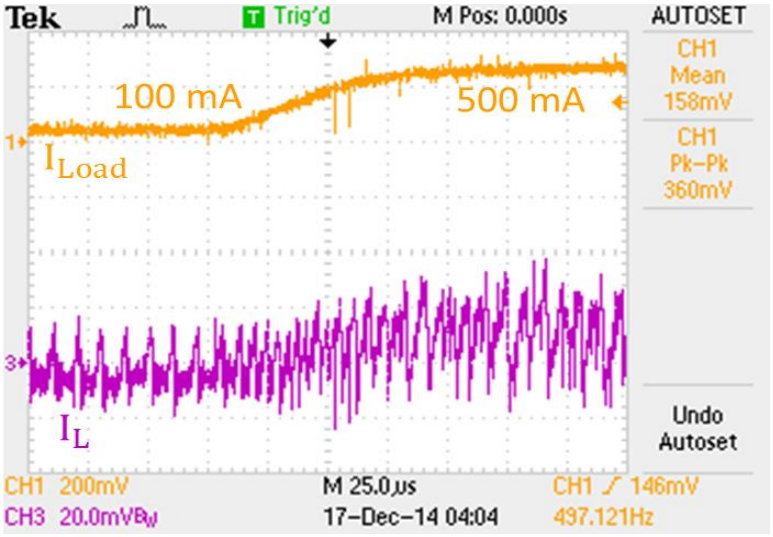


Figure 4.9 Inductor current change due to load step.

Figure 4.10 and Figure 4.11 show the transient response of the 3-level buck converter with a load step down from 500 mA to 100 mA. Figure 4.10 shows the load current, output voltage, and the gate signal for Q1. The gate signal of Q1 is displayed to show how the switching frequency changes with the load step down. The load current, shown by the yellow line in Figure 4.10, changes from 500 mA to 100 mA in 68 µs. The blue line shows the output voltage ripple. It is evident that there is no overshoot in the output voltage because the converter is able to assume the change in current. The load step is too slow to cause too much energy to be stored in the output capacitor. The purple line is the gate signal for Q1, which shows the switching frequency change as the load decreases. Figure 4.11 shows the load current and inductor current. The yellow line in Figure 4.11 shows the load current changing from 500 mA to 100 mA. The purple line shows the inductor current as it switches from CCM to DCM with the load current decrease.

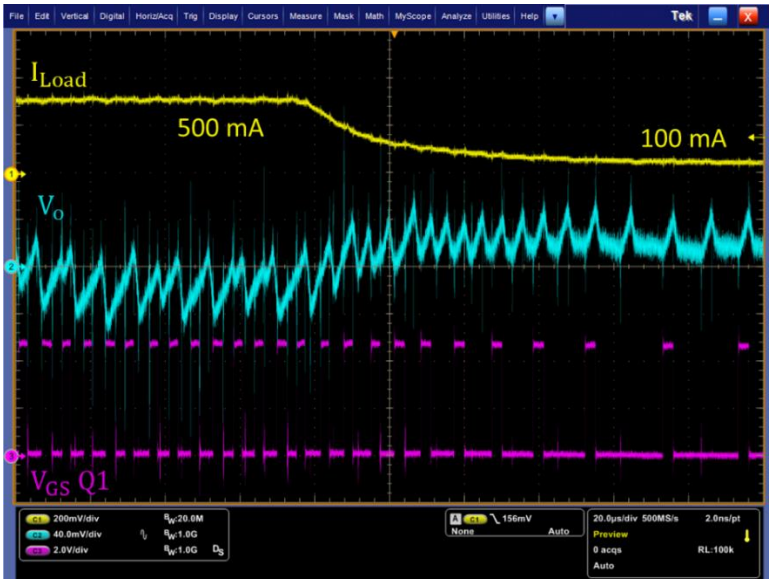


Figure 4.10 Output voltage and Q1 gate signal due to load step down.

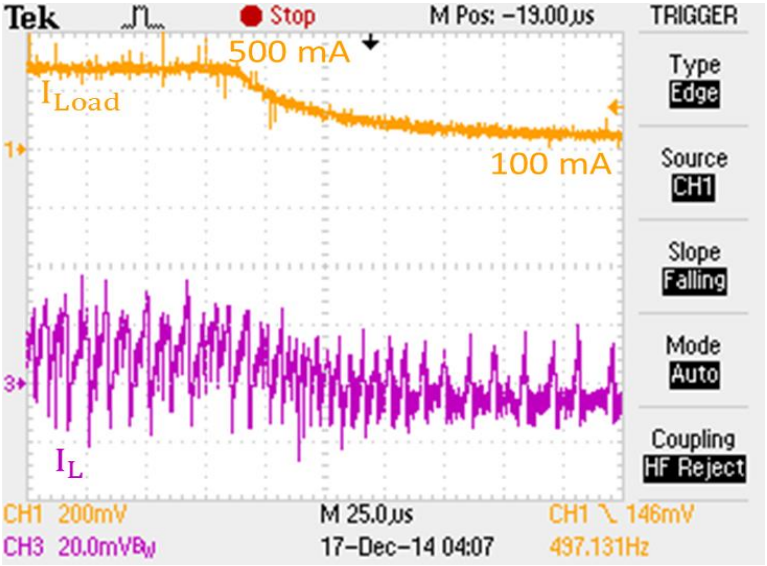


Figure 4.11 Inductor current change due to load step down.

4.2.2 Efficiency

The overall efficiency of the converter was measured under the input voltage of 12 V when the car is turned off. Note that a car black box should be most efficient under the off mode to prevent it from depleting the car battery. The load range tested covers above and below the required test load range of 20 mA to 1000 mA, which includes 1 mA to 1650 mA. There are several efficiency graphs that show the improvement in efficiency with the change in operating

mode. The converter switches between CCM and DCM depending on the load, with a very light load mode implementing DCM by shutting down Q3 and Q4 and using Schottky diodes.

First, the efficiency of the converter was measured when it operated in CCM for the entire load range of 20 mA to 1000 mA. The controller was forced to operate in CCM by tying the MODE pin to the input voltage [28]. Figure 4.12 shows the CCM efficiency increasing from 46 % at 20 mA (or 100 mW) to 95% at 1000 mA (or 5000 mW) and then drops off to 93.7% at 1650 mA (or 8250 mW). The converter shows poor efficiency in CCM under light load, which further motivates the adoption DCM in light load.

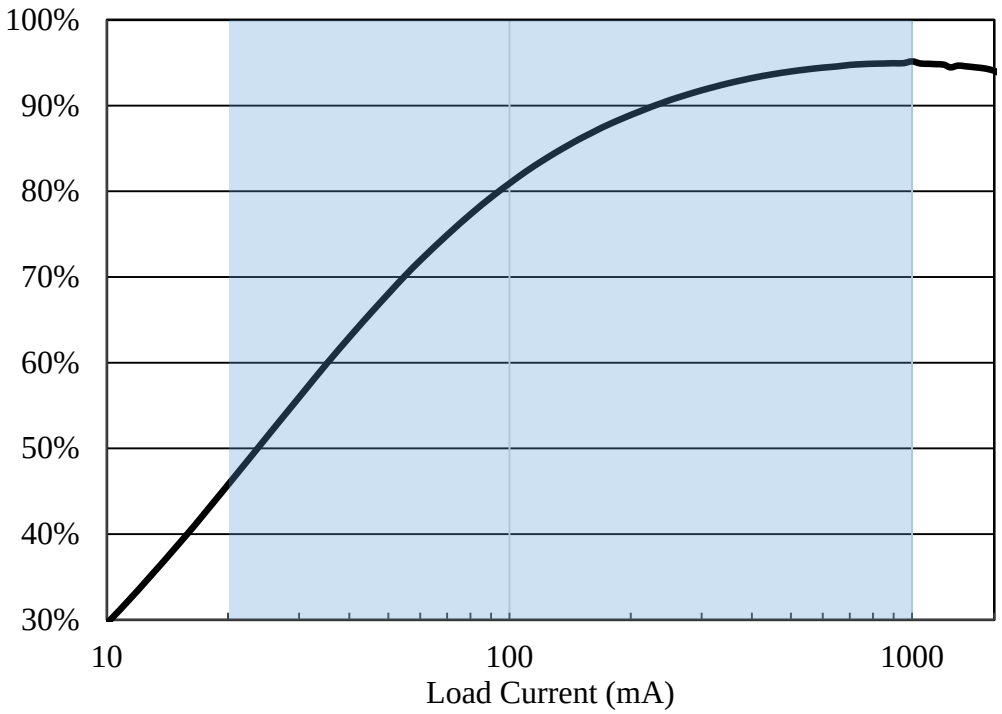


Figure 4.12 CCM efficiency versus load current.

As explained above, it is necessary to operate the converter in DCM under light load and CCM under heavy load. DCM is implemented using the inductor current sense comparator internal to the controller to determine the zero crossing. The DCM threshold can be adjusted by changing the inductor value. A larger inductor causes the converter to enter DCM at a smaller load. The inductor was designed for a 66% current ripple at full load of 1000 mA, allowing the converter to enter DCM at 330 mA. Refer to Section 3.4.2 part B about the controller design to operate the converter in such manner.

Figure 4.13 shows the efficiency of the converter under two operation modes, DCM under light load and CCM under heavy load. The efficiency in DCM increases drastically at low current load when compared with CCM only, where the increase is gradual at higher load current. For example, the efficiency at 30 mA of load current is 57% in CCM and 85% in DCM, which is a 28% increase. The increase at 100 mA of load current is from 81% in CCM to 92% in DCM, which is an 11% increase. The 85% efficiency bar is shifted from 140 mA in CCM down to 30 mA in DCM. When the operation mode switches from DCM to CCM at load current of 330 mA, the efficiency drops by 0.5%.

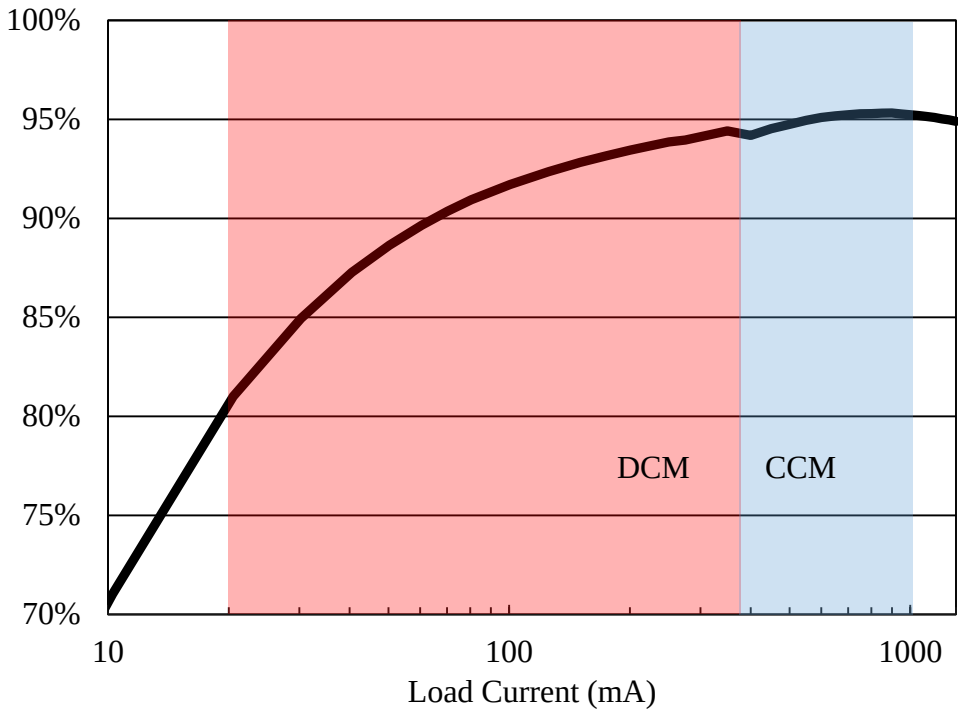


Figure 4.13 Light load DCM and CCM efficiency versus load current.

The proposed converter configuration in the DCM mode described above turns off synchronous MOSFETs, Q3 and Q4, when the inductor current touches zero. It is called zero-diode configuration in this section. As explained in Section 3.3.1 part B, it is possible to shut off only Q4 completely while switching Q3, called one-diode configuration. In such a case, the inductor current flows through the Schottky diode in parallel with Q4. The two-diode configuration shuts down both Q3 and Q4. (Refer to Section 3.3.1 for details.) Figure 4.14 shows the efficiency under the very light load case for the three different configurations. The zero-diode configuration achieves higher efficiency for the load current above 12 mA. One-

diode and two-diode configurations perform better over zero-diode configuration below 12 mA, and the difference increases as the load current decreases. The difference in efficiency between one-diode and two-diode configurations is approximately 1-2%. Overall, the no-diode configuration adopted for the proposed converter achieves higher efficiency than the other two configurations for the minimum target load current of 20 mA. When the load is under 20 mA, one- or two-diode configuration may be considered.

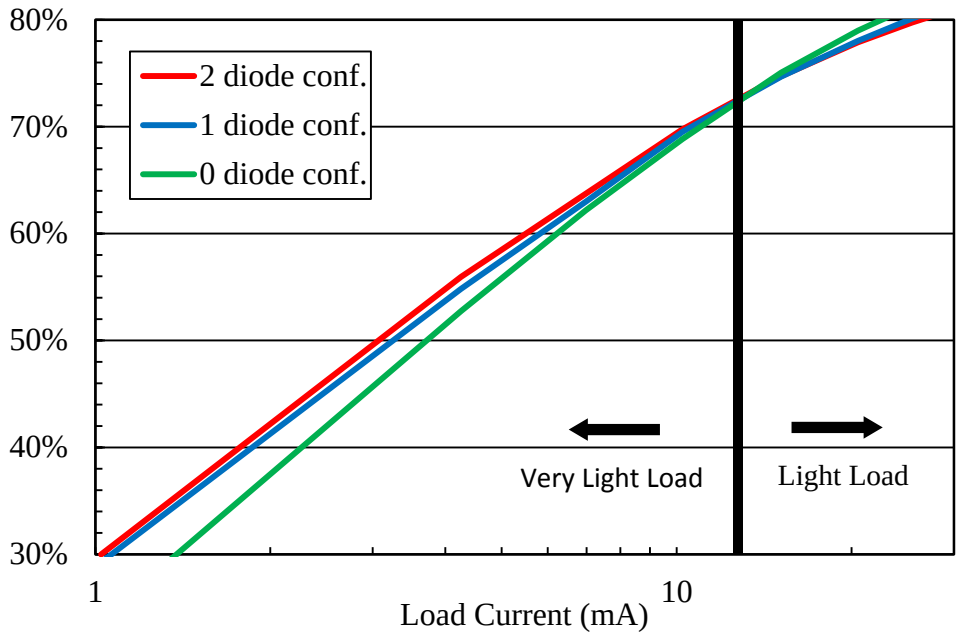


Figure 4.14 Very light load DCM efficiency versus load current.

Figure 4.15 shows the maximum achievable efficiency across the entire load range from 1 mA to a 1650 mA, when all the three configurations, zero-, one-, and two-diode, are incorporated. The shaded area in green is the target load range of the car black box. The figure shows that the efficiency ranges from 30% at 1 mA (5 mW) to maximum 95% at 1000 mA (5000 mW), with the efficiency being larger than 90% above 100 mA (500 mW).

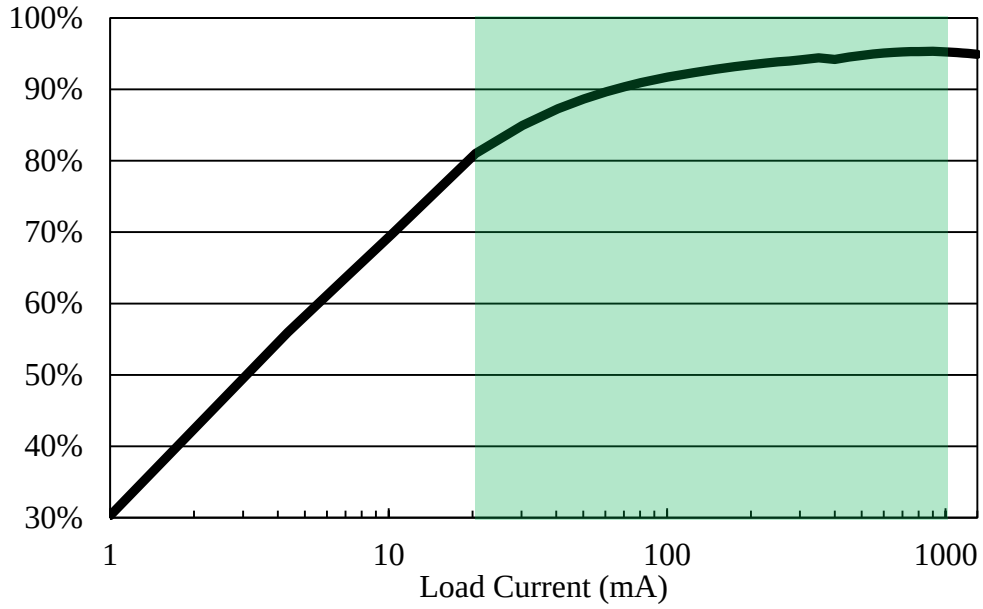


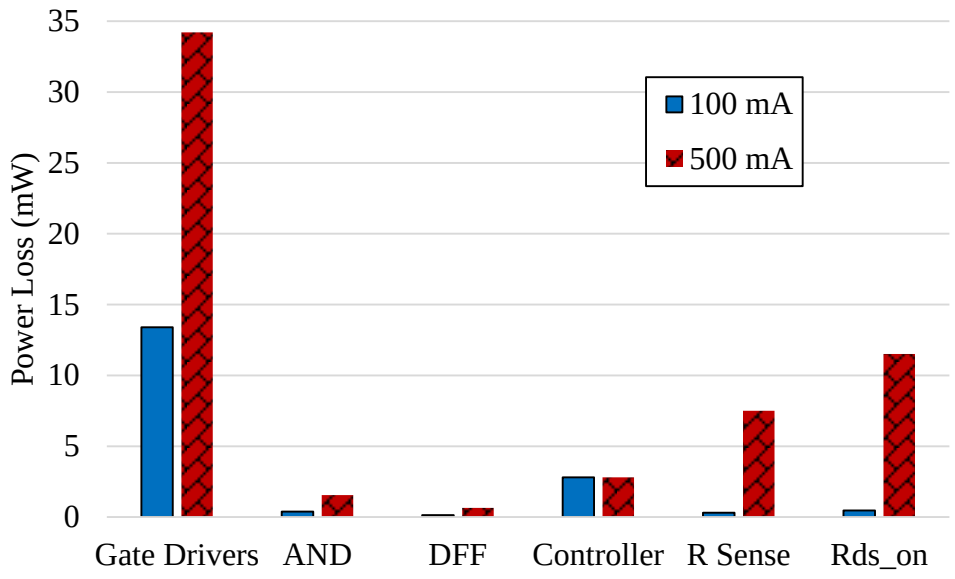
Figure 4.15 Ideal efficiency over load range 1 mA to 1650 mA.

4.2.3 Loss Breakdown

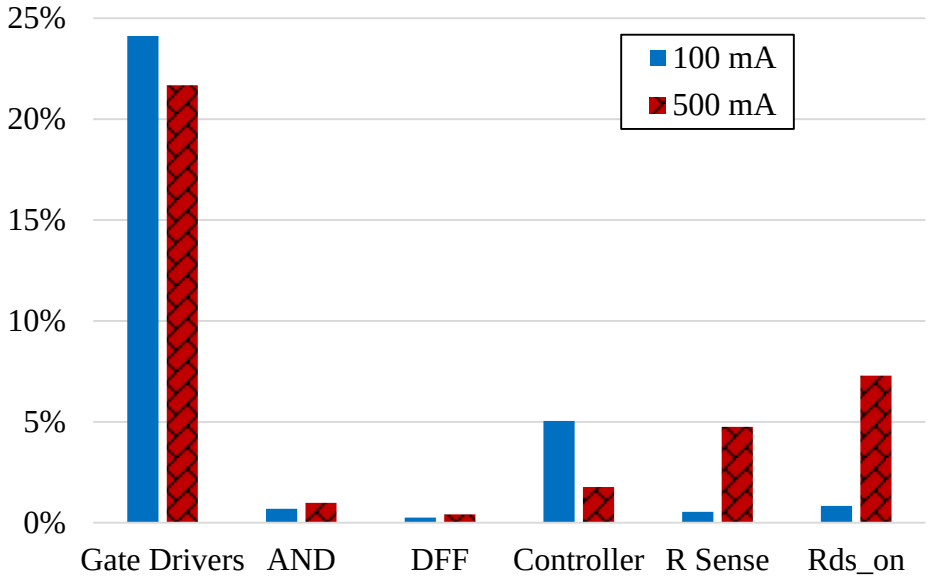
This section covers the loss breakdown at two different loads currents, 100 mA (or 500 mW) and 500 mA (or 2500 mW). The loss breakdown is considered at two different loads to show how much power each part consumes in relation to the total loss. The components considered for the loss breakdown are the four MOSFETs, the four gate drivers, one AND gate, 1 D FF, 1 OR gate, one controller, and the current sense resistor. (Refer to Section 3.4.1 for the parts.)

Figure 4.16 shows the loss breakdown of each component at two different load currents, 100 mA and 500 mA. The total power loss is 55 mW under the load current of 100 mA and 158 mW under the load current of 500 mA. The four gate drivers consume 13.4 mW (24%) while the one controller consumes 2.8 mW (5%) for the light load. The total power dissipated by the gate drivers and controller account for 29% of the total loss at 500 mW. When the load current increases to 500 mA (or 2500 mW), the power consumption of the gate drivers increase to 34.2 mW, but its loss percentage is reduced to 21.7%. This is due to the increase in switching frequency. In contrast, the power dissipation of the controller remains the same 2.8 mW (with the reduced loss percentage being 1.8%). The controller power consumption does not increase with the increase in the switching frequency because of the bypass of LDO (Low-dropout

regulator). The output voltage is used to power the gate driver and other parts internal to the controller through a pin called EXTVcc. This is explained further in Appendix D. The power losses can be improved by reducing the number of gate drivers. The ideal option would be integrating them into the controller to avoid having to use four additional parts.



(a) Power loss of each type of components.



(b) Percentage of losses for each type of components.

Figure 4.16 Breakdown of losses.

4.3 Efficiency Comparison

This section compares the performance of existing off-the-shelf buck converter ICs with the proposed 3-level buck converter. In general, the comparison favors off-the-shelf ICs because MOSFETs for commercial ICs can be designed for the specific load conditions. In addition, unnecessary functions can be shut down to improve light load efficiency.

4.3.1 Comparison with Active-Semi ACT4070B

This section compares the proposed converter with Active-Semi ACT4070B buck converter IC chosen by the KAIST team for the car black box. Figure 4.17 shows the efficiency curve of ACT4070B. The efficiency under 12 V input ranges from 65% at 100 mW to 93% at 5 W, with the peak efficiency being 94% at 4 W [20]. The proposed 3-level buck converter achieves higher efficiency than ACT4070B by 14% at light load and 2% at full load. The 3-level buck also has an efficiency of 90% at 500 mW compared to 85% for ACT4070B [20]. ACT4070B adopts an asynchronous topology, which operates in DCM below 300 mA. This helps ACT4070B to improve the light load efficiency. Above 300 mA, the 3-level buck converter and ACT4070B buck converter have similar efficiency curves, with the 3-level being more efficient on average by approximately 2%. The 3-level buck's higher efficiency is attributed to less conduction losses and is explained next.

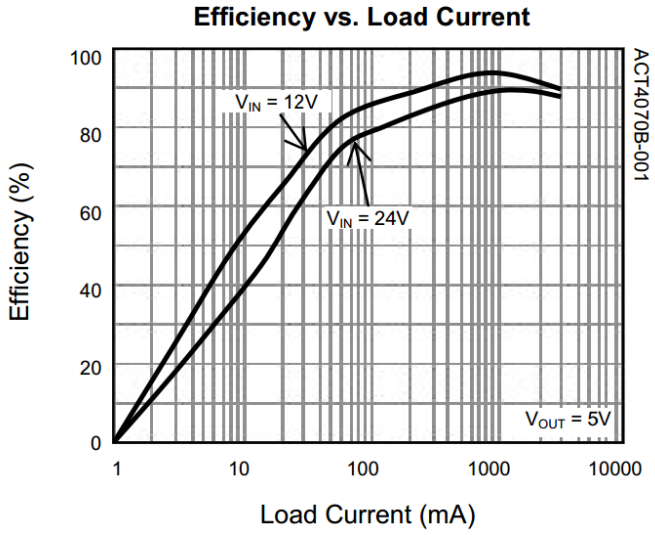
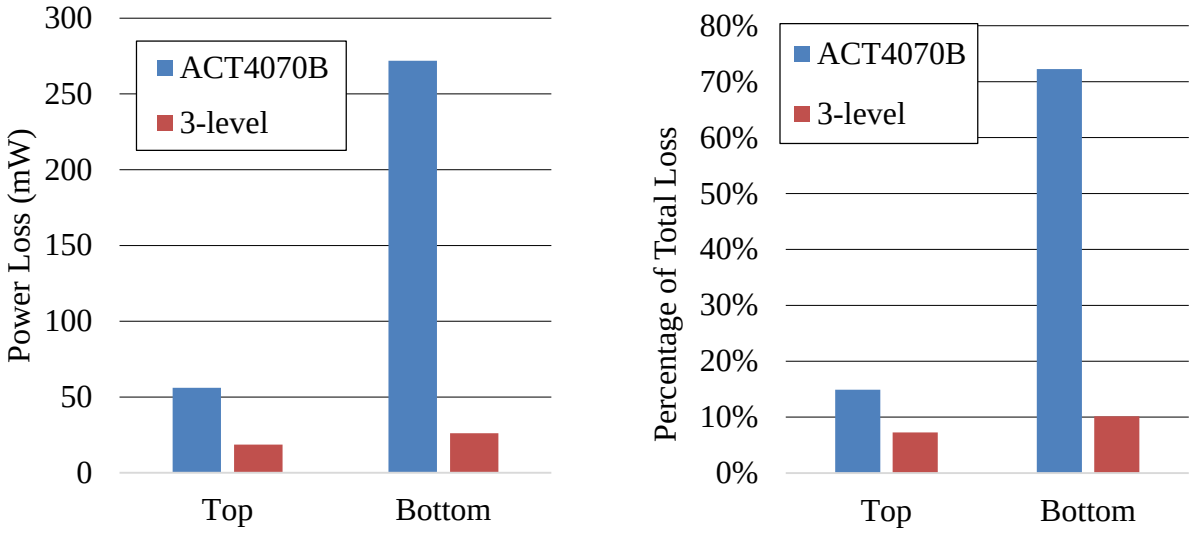


Figure 4.17 ACT4070B efficiency versus load current from A. Semi, "Wide Input 3A Step Down Conveter," ACT4070B datasheet, 2013. [Online]. Available: http://www.active-semi.com/sheets/ACT4070B_Datasheet.pdf. [Accessed 15- May- 2014]. Used under fair use, 2015.

The $R_{DS_{on}}$ of the top and bottom switches for ACT4070B is 130 mΩ and 7.9 Ω, respectively [20]. The bottom switch is used only to charge the bootstrap capacitor for the top gate, while a Schottky diode, with a forward voltage of 0.35, is used to carry the load current [28]. Figure 4.18 shows the power consumed by each switch throughout one switching cycle under the full load condition of 1 A. ACT4070B switches consume 327 mW or 87.2% of the total power lost compared to 44.7 mW or 17.5% for the 3-level buck. The Schottky diode used in the ACT4070B buck converter consumes the most power of 271 mW or 72.3% of the total power lost. The switches of the proposed 3-level buck converter consume significantly less power, but suffer much larger loss implementing the control and gate driving. Overall, the 3-level buck converter is more efficient and shows feasibility for further efficiency improvement.



(a) Power loss (b) Percentage loss

Figure 4.18 3-level buck vs. ACT4070B power loss comparison.

4.3.2 Comparison with Linear Technology LTC3646

This section compares the proposed 3-level buck converter with LTC3646, which has high light load efficiency owing to adoption of burst mode and integrated MOSFETs. LTC3646 is capable of handling a maximum input voltage of 40 V [29]; therefore requiring each MOSFET to have a breakdown voltage of 80 V. This possibly skews the data because the devices used in the proposed converter are not integrated and designed optimally for the car black box application.

Figure 4.19 shows the efficiency curve of LTC3646. The efficiency under 12 V input ranges from 88% at 100 mW to 93% at 5 W, with the peak efficiency being 95% at 4 W [29]. The proposed 3-level buck converter achieves lower efficiency than LTC3646 by 7% at light load and the same efficiecny at full load. The 3-level buck also has an efficiency of 90% at 500 mW compared to 88% for LTC3646 [29]. Above 300 mA, the 3-level buck converter and LTC3646 buck converter have a similar trend in efficiency, with the 3-level being more efficient on average by approximately 1%. However, it does show that the integrated MOSFETs have very good characteristics considering their high breakdown voltage.

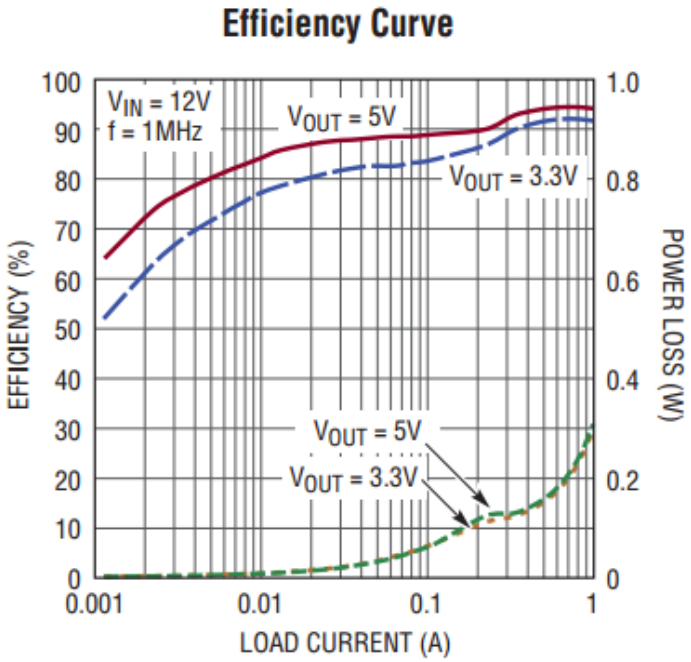
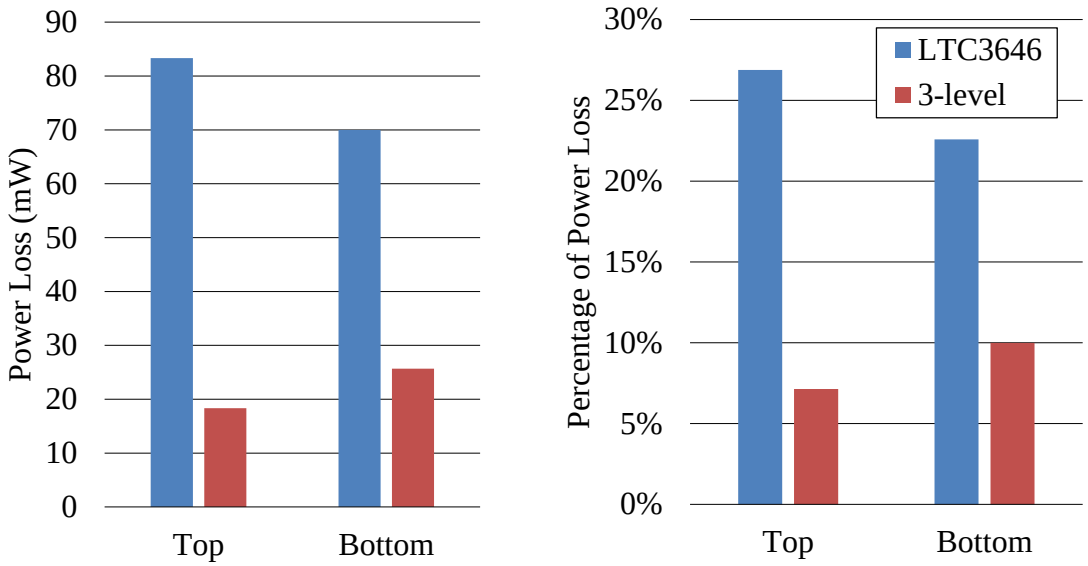


Figure 4.19 Efficiency vs load current from L. Technology, "40V, 1A Synchronous Step-Down Converter," LTC3646 datasheet. [Online]. Available: http://cds.linear.com/docs/en/datasheet/36461fb.pdf. [Accessed 10- Dec- 2014]. Used under fair use 2015.

LTC3646 uses integrated MOSFETs inside of the chip. The only necessary external components are bypass, output and input capacitors, a voltage divider, and an inductor. The approximated gate charge for the MOSFETs is 2.5 nC each and 5 nC in total [29]. $R_{DS_{on}}$ for the main switch is 200 mΩ and the synchronous switch is 120 mΩ. Figure 4.3.1.4 compares the conduction loss of the integrated switches with the proposed 3-level buck converter switches at full load of 1000 mA or 5000 mW. Figure 4.20 shows the power consumed by each switch through on switching cycle under full load, for LTC3646 and the 3-level buck converter. LTC3646 switches consume 158 mW or 49.7% of the total power lost compared to 44.7 mW or

17.5% for the 3-level buck. Therefore, 50.5% of the loss for LTC3646 comes from the inductor DCR and the internal parts of the chip, which is far less than the 3-level buck. The 3-level buck has 82.9% of its loss coming from the inductor DCR, gate drivers, controller and external control logic. At full load, the 3-level inductor DCR accounts for 24 mW or 9.3% of the total loss, bringing the gate drivers, controller, and control logic loss to 73.6%. At full load, the 3-level buck converter is more efficient at 95.1% compared to LTC3646 at approximately 94%. Overall, the 3-level buck converter shows feasibility to further improve the efficiency through an integrated circuit, possibly higher efficiency than that of LTC3646.



(a) Power loss (b) Percentage loss

Figure 4.20 3-level buck vs. LTC3646 power loss comparison.

4.4 Chapter Summary

The first part of this chapter describes performance of the prototype of the proposed converter. The peak efficiency of the converter is 95% at 1 A with the light load efficiency being 79% at 20 mA. The second part compares the efficiency of the proposed converter with off-the-shelf buck converters, ACT4070B and LT3646. The comparisons show that a promising way to increase the overall efficiency of the proposed converter is to integrate the control loop, gate drivers, and MOSFETs on the same IC as well as designing the MOSFETs for the specific application.

Chapter 5

Conclusion

Smart cameras operate mostly in sleep mode, which is light load for power supplies. Typical buck converter applications have low efficiency under the light load condition, primarily from their power stage and control being optimized for heavy load. The battery life of a smart camera can be extended through improvement of the light load efficiency of the buck converter. This thesis research investigated the first stage converter of a car black box to provide power to a microprocessor, camera, and several other peripherals. The input voltage of the converter is 12 V, and the output voltage is 5 V with the load range being 20 mA (100 mW) to 1000 mA (5000 mW). The primary design objective of the converter is to improve light load efficiency.

The proposed 3-level buck converter uses research by Reusch as the starting point for this thesis. A 3-level buck converter has two more MOSFETs and one more capacitor than a synchronous buck converter. Q1 and Q2 are considered the top MOSFETs, while Q3 and Q4 are the synchronous ones. The extra capacitor is used as a second power source to supply the load, which is connected between the source of Q1 and the drain of Q2 and the source of Q3 and the drain of Q4. The methods considered to improve light load efficiency are: PFM control scheme with DCM and use of Schottky diodes in lieu of the synchronous MOSFETs, Q3 and Q4. The 3-level buck converter operates in CCM for heavy load above 330 mA and DCM for light load below 330 mA. The first method uses a COT valley current mode controller that has a built in inductor current zero-crossing detector. COT is used to implement PFM, while the zero-crossing detector allows for DCM. The increase in efficiency comes from reducing the switching frequency as the load decreases by minimizing switching and gate driving loss. The second method uses an external current sense amplifier and a comparator to detect when to shut down the gate drivers for Q3 and Q4. Schottky diodes in parallel with Q3 and Q4 carry the load

current when the MOSFETs are off. This increases the efficiency through a reduction in switching loss, gate driving loss, and gate driver power consumption.

The proposed converter is prototyped using discrete components. LTC3833 is used as the COT valley current mode controller, which is the center of the control scheme. The efficiency of the 3-level buck converter was measured and ranges from 82% to 95% at 100 mW and 5000 mW, respectively. The transient response of the converter shows no overshoot due to a 500 mA load step up or down, and the output voltage ripple is 30 mV. The majority of the loss comes from the external components, which include a D FF, AND gate, OR gate, current sense chip, comparator, and four gate drivers. The proposed converter was compared to two off-the-shelf synchronous buck converters. The proposed converter has good efficiency and performance when compared to the other converters, despite the fact that the converter is realized using discrete components.

Future research areas to improve upon for the 3-level buck converter are listed below.

- Design and integration of MOSFETs would have a large impact on efficiency because of the ability to carefully choose the optimum gate charge and on resistance.
- Integration of the control scheme and gate drivers into one chip. Currently, the controller is designed for a synchronous buck converter and has gate drivers built in, which makes the total gate driver count in the proposed converter equal to six. By integrating the control scheme for a 3-level buck converter, two of the unnecessary gate drivers can be eliminated. Additionally, the digital chips can be designed for the exact number of gates needed. Lastly, the very light load detection circuit can be implemented with less parts because the current sense amplifier used for the COT control can be used.
- Elimination of the current sense resistor through use of DCR current sensing. The current prototype does not implement DCR current sensing because of the external current sense IC for detection of the very light load case. At full load, DCR could improve the efficiency by 0.6%.

The above items are left for future research in 3-level buck converter designs for low power applications.

Appendix

Additional Information

A. Previous Gate Driving Method

Reusch used the gate driving method shown in Figure A.1 from [3], which proved not to work for the very light load method implemented in the proposed converter. Under very light load, the gate drivers for Q3 and Q4 and Schottky diodes in parallel with the MOSFETs carry the load current, shown in Figure A.2. When the converter is operating in the very light load using the driving method presented by Reusch, the bootstrap capacitor powering the floating gate driver will not be able to charge with a 5 V supply.

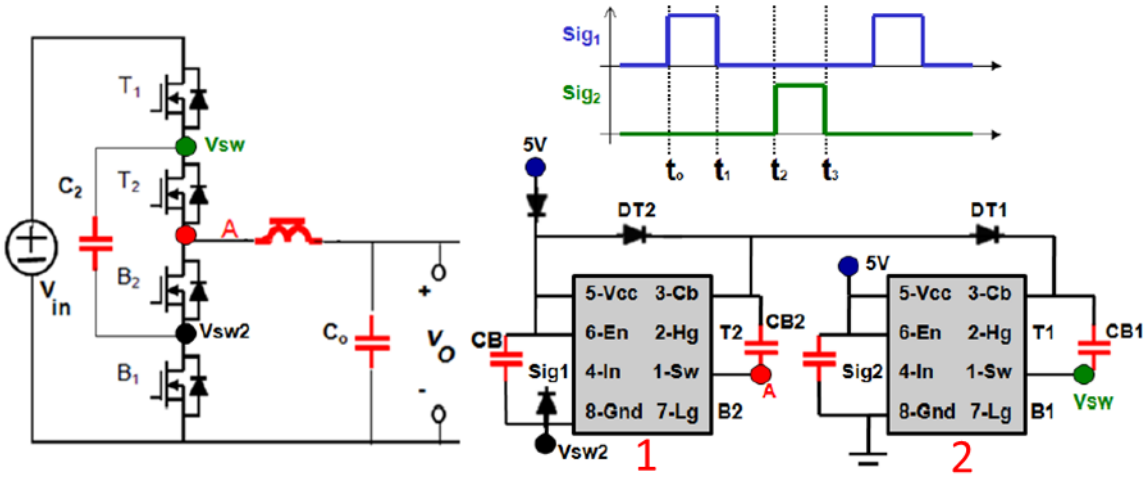


Figure A.1 Reusch gate driving method from D. Reusch, *High Frequency, High Power Density Integrated Point of Load and Bus Converters*, Ph.D. dissertation, ECE, Virginia Tech, Blacksburg, VA, 2012. Used under fair use, 2015.

Initially, when gate driver 2 is enabled, CB is able to charge through B2, A, and the output. This allows gate driver 1 to float between switch node Vsw2 and A. However, when the

output is regulated at 5 V, the charge on CB will slowly deplete until the voltage is not large enough to keep gate driver 1 on. This is because CB is not able to charge through the switch node. Under CCM, CB would charge through B1. Figure A.2 shows the converter topology when operating in DCM. B1 is replaced with a Schottky diode, inhibiting CB from charging. This causes the gate driver to shut down momentarily and the output voltage begins to droop. When the output voltage drops to 3 V, CB is able to then charge again in the same fashion. The output voltage is regulated at 5 V momentarily until the same process reoccurs.

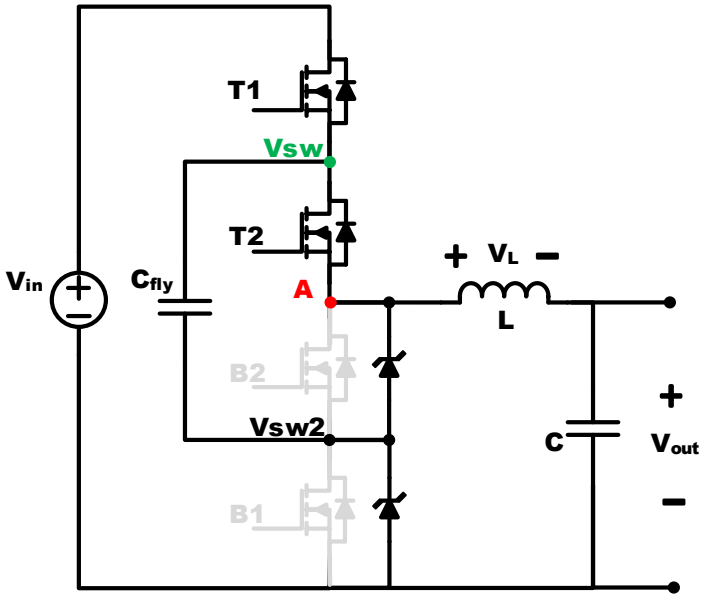


Figure A.2 Very light load schematic

This phenomenon prevents the use of the driving topology presented by Reusch in [3]. The new topology used was introduced in Section 3.4.4.

B. Control Loop Design

The first step to designing the 3-level buck converter was to simulate all of the switching components in their ideal case in SIMPLIS. The simulation used ideal switches as the MOSFETs, ideal inductors and capacitors, and an ideal voltage source. The control method was COT that utilized DCM to allow for the switching frequency to reduce. The main purpose of the simulation was to ensure the flying capacitor balanced at one-half the input voltage, the output voltage regulated, the inductor current was balanced, the converter was stable, and the switching frequency reduced as the load decreased. The four major blocks were the gate driving signal generator, the output voltage compensator, the constant on-time valley current mode control, and the inductor current zero crossing detector. The zero crossing zero detector control block was in charge of detecting the inductor current zero crossing and turning off Q3 and Q4 to allow the converter to enter DCM. The simulation showed that the switching frequency would decrease with the load. The constant on-time valley current mode control block generated the on pulse for Q1 and Q2. The flying capacitor was able to balance naturally using valley current mode detection because this control method forced the inductor current to balance [3]. The voltage compensator block was in charge of generating the output voltage error information to be used for the valley inductor current threshold as well as increasing the bandwidth of the control loop to allow for faster transient response. Lastly, the gate driving signal generator block was in charge of creating the proper gate signal for each MOSFET through a series of digital gates. Figure B.1 shows the SIMPLIS schematic.

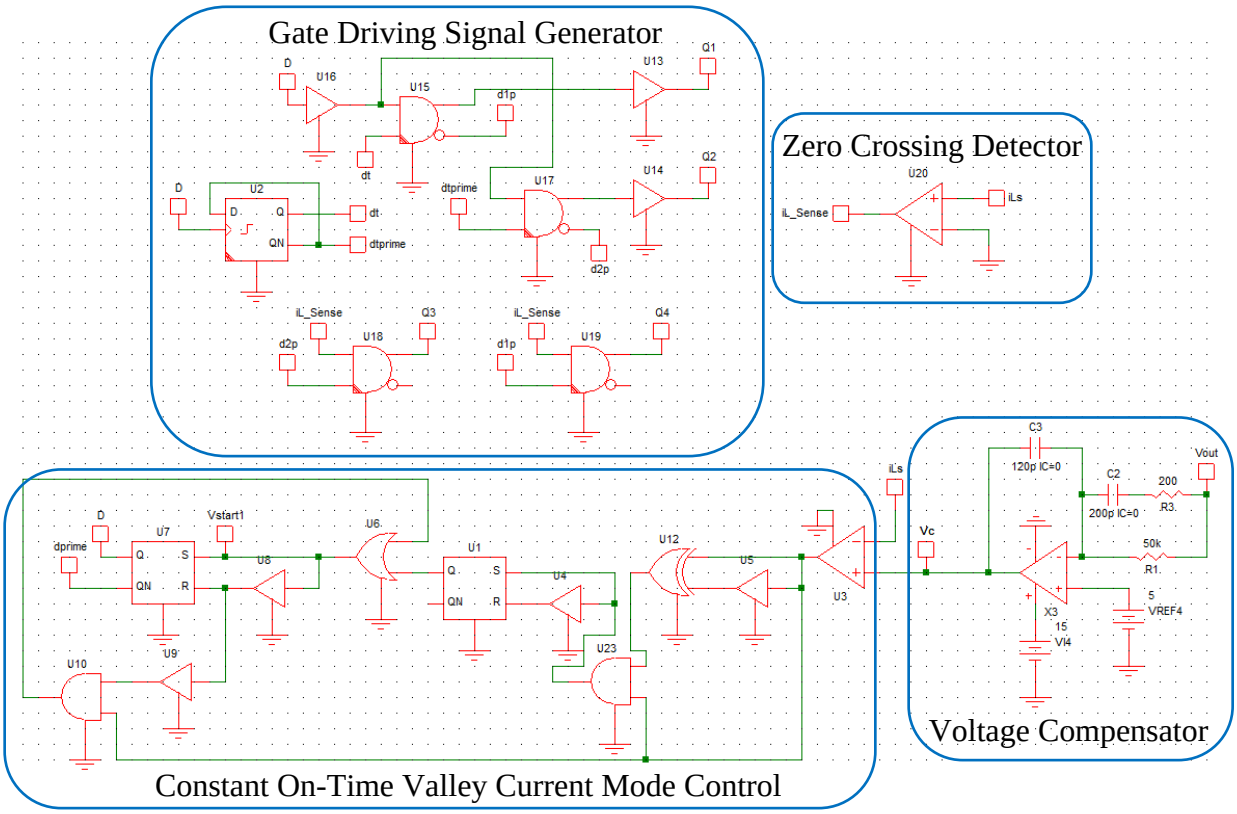


Figure B.1 SIMPLIS Schematic

Figure B.2 shows the flying capacitor balancing at one-half the input voltage. It is necessary for the flying capacitor to balance at one-half the input voltage to reduce the stress each MOSFET sees as well as allowing the inductor to charge the same amount during each cycle [3].

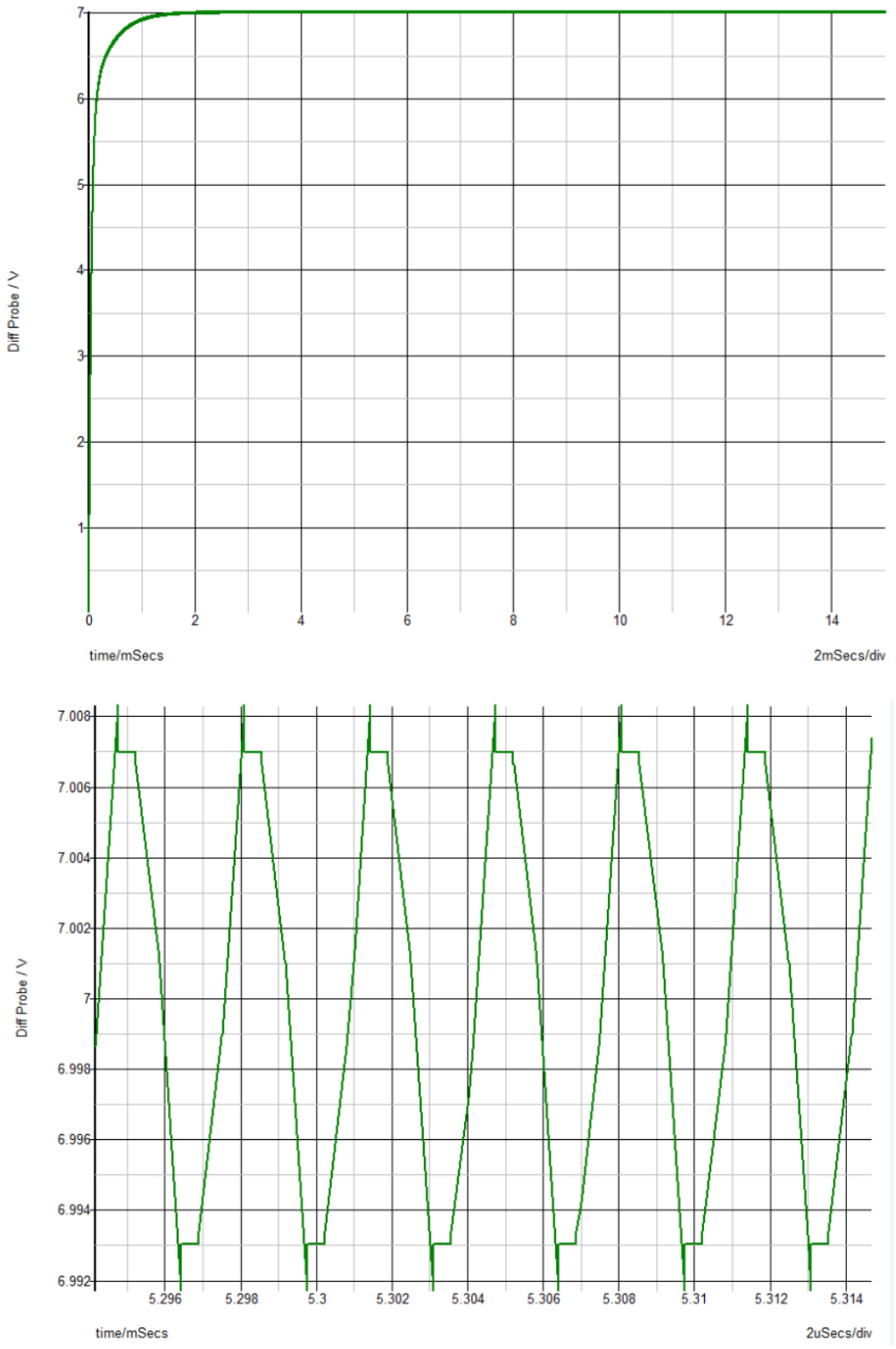


Figure B.2 Flying capacitor balancing at one-half Vin (14 V).

C. Pulse Skipping

LTC3833 COT valley current mode controller has the ability to pulse skip as the load decreases [12]. The pulse skipping method allows the switching frequency to reduce proportionate to the load. LTC3833 is designed for use in a synchronous buck converter application. The proposed 3-level buck converter design causes some issues when trying to power the controller. Figure C.1 shows a typical application for LTC3833, where the pin "Vin" is tied to the input voltage source and the drain of the top MOSFET. The minimum on-time of the controller will depend on whether the converter is in DCM or CCM; however, it is smaller for high step-down ratios, per the datasheet [12].

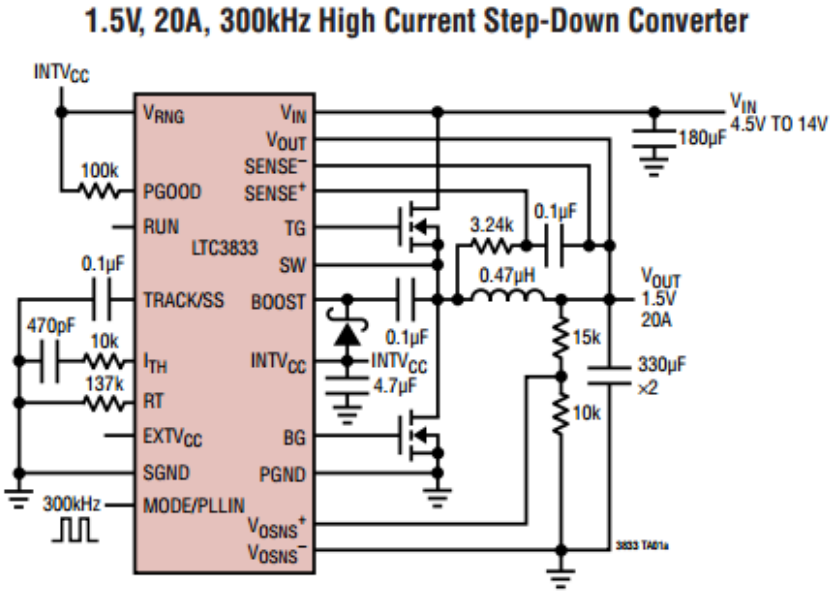


Figure C.1 LTC3833 Pin Label from L. Technology, "Fast Accurate Step-Down DC/DC Contoller with Differential Output Sensing," LTC3833 datasheet. [Online]. Available: http://cds.linear.com/docs/en/datasheet/3833f.pdf. [Accessed 10- Jun- 2014]. Used under fair use, 2015.

The on-time for the top MOSFET in CCM is shown below [12]. With a set switching frequency, it is evident that the on time decreases as the input voltage increases and vice versa.

$$t_{ON} = \frac{V_{out}}{V_{in} * f_s}$$

For the proposed converter, the Vin pin and the drain of the top MOSFET Q1 is separated to allow a different voltage to be supplied to the controller than the power stage.

When Vin is tied to 12 V and the converter is operating in DCM, the controller enters a burst mode. The burst mode is defined as the switching frequency of the converter increasing to 1 MHz for a short period and then shutting down all gates for a short period. When the load is 200 mA, the converter is in DCM switches continuously at 1 MHz causing the efficiency to decrease dramatically from the CCM case. Figure C. shows the burst mode behavior of the converter at 50 mA. It is clear that the converter is switching very quickly for 1.2 ms and then not at all for 1.8 ms. The previous two examples cause a large decrease in efficiency, worse than if the converter were to operate in CCM throughout the entire load range.

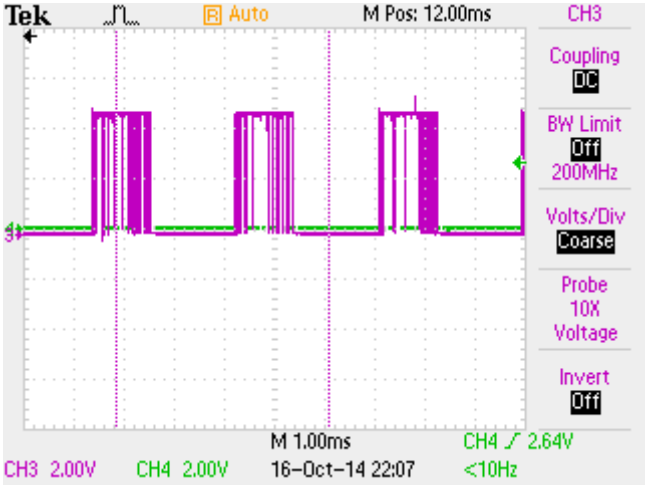


Figure C.2 Example of burst mode.

The datasheet does not explicitly discuss how the on time can be calculated for DCM mode of operation. Thus, it was difficult to determine why the converter was not behaving in the proper fashion. It was found through prototype testing that reducing the input voltage to the controller allowed it to pulse skip in a more normal fashion that enabled the switching frequency to reduce. The controller began to perform normal when the input voltage was reduced to 10 V and as low as 5 V. Since the digital chips and gate drivers use a 5 V supply, the input to the controller was also supplied with 5 V. Figure C.3 shows proper operation of the controller and that the on time of the top gate to be 2.5 µs for a load current of 100 mA. This trend continues throughout the entire range the converter is operating in DCM. It can be seen that the switching frequency reduces to 50 kHz and the controller is not operating in a burst mode fashion.

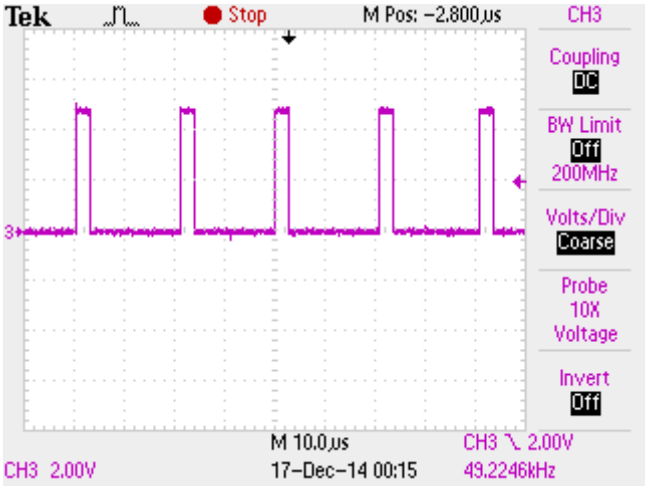


Figure C.3 Proper operation of the controller with 5 V input.

D. EXTVcc

LTC3833 has a built in LDO that reduces the input voltage of the controller to 5.3 V, which is available on the INTVcc pin [12]. This voltage is used to supply the top and bottom gate driver of the controller as well as the bootstrap capacitor for the top gate. For the proposed converter, a bootstrap capacitor is not used for the controller because the gate signal does not have to be level shifted. For applications with an output voltage larger than 4.6 V and smaller than 6 V, the output can be attached to the EXTVcc pin [12]. This shorts EXTVcc to INTVcc and shuts down the internal LDO. If Vin is less than 5.3 V, Vin and INTVcc can be tied together to disable the LDO, preventing dropout [12]. Appendix C discusses why 5 V was used to power the controller; however, the PCB was designed before this was determined.

The current state of the prototype yields the highest efficiency when the output is connected to EXTVcc. This allows the internal LDO to be shut down and the power be derived from the 12 V input to the power stage. This is more efficient than supplying power through the LDO, which will have a large dropout due to the input voltage being 5.

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