Power Module with Series-connected MOSFETs in Flip-chip Configuration

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Thesis submitted to the Faculty of the
Virginia Polytechnic Institute and State University
In partial fulfillment of the requirements for the degree of
Master of Science
in
Electrical Engineering

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August 23, 2010

Blacksburg, Virginia

Keywords: Power module, Series-connected power MOSFETs

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Abstract

Power module design is needed for high system performance and reliability, especially in terms of high efficiency and high power density. Low parasitic impedance and thermal management is desired for the lower power loss and device stress.

For power module with high efficiency and improved breakdown voltage, this thesis proposes a novel series-connected power MOSFETs module. Three IRF7832 MOSFETs (30 V breakdown voltage) in series are simulated in a chopper circuit. The drain-source voltage sharing in switching off-mode shows that the devices can share voltage within their breakdown ranges. The switching characteristics are studied, and the switching energy losses without parasitic inductance and with 5 nH parasitic inductances are 203.38 μJ and 316.49 μJ, respectively. The critical parasitic inductance is the one connecting the source of the upper MOSFET and the drain of the middle MOSFET. The switching energy loss due to critical parasitic inductance is about 44.4% of the total switching energy loss. The layout is designed for the double-substrates direct-bond module and wire-bonded module using direct-bond-copper (DBC) substrate. Based on layout dimensions and packaging materials, the packaging module's parasitic parameters are obtained using Ansoft® Q3D extractor. Using parasitic inductance values from simulation, the switching energy losses of direct-bond module and wire-bonded module are 296.18 μJ and 238.99 μJ, respectively. Thermal management is then studied using Ansoft® ePhysics. The MOSFET junction-to-air thermal resistances of the double-substrate direct-bond module and the single-substrate wire-bonded module are 33°C/W and 82°C/W, respectively. Hence, by comparing the direct-bond module with a wire-bonded power module, direct-bond module shows lower parasitic impedances and better thermal management.

To test the breakdown voltage of series-connected power MOSFETs module, three TI DualCool^{TM} N-channel NexFET Power MOSFETs (25 V breakdown voltage) in series are assembled using flip-chip direct-bond technology. Three samples are assembled and the breakdown voltages are measured by using high-power curve tracer as 76 V, 82 V, and 72 V. The more accurate method for testing breakdown voltages by digital voltmeter obtains 77.51 V, 82.31 V, and 73.06 V. The series-connected power MOSFETs module shows compact volume, low parasitic impedances, thermal resistances and improved breakdown voltage. This power module has strong potential for use in applications that require minimized packaging size and parasitic inductance for high voltage, high switching frequency, and high efficiency.

Acknowledgements

I would like to thank my advisor, Dr. Khai. D. T. Ngo, for his kindly help in this research. This work could not have been finished without his guidance, support and time.

I would like to thank Dr. G. Q. Lu to be my committee co-chair and Dr. Kathleen Meehan to be my committee member. Their suggestions and help in my study are greatly appreciated.

The colleagues at CPES also give me a lot help for my stay here. I would like to thank Xiao Cao, Li Jiang, Ruxi Wang, Wei Zhang, Dong Dong, ZiJian Wang, Daocheng Huang, Li Jiang, Shuilin Tian, Mingkai Mu, Haoran Wu, Jin Li, Pengju Kong, Fang Luo, Zheng Chen, YiYing Yao, Jayashree Seshadri, Kewei Xiao, Zheyuan Tan for their help, discussions and friendships.

I also would like to thank CPES administrative staff: Teresa Shaw, Trish Rose, Marianne Hawthorne and Doug Sterk for their help and support.

Finally I would like to thank my parents for their constant love and support.

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Chapter 1: Background and Introduction

This chapter gives a basic background in power electronic packaging modules, power device packaging technology and the motivation for and an introduction to this research.

1.1. Power electronic packaging module

Power electronics are now driven by challenging requirements, such as volume, power density, operation temperature, and cost [1]. The packaging of power electronics is a critical factor to performance and reliability of power electronics systems. For a traditional power multi-chip module, the devices are mounted on the substrates via a large solder area. The wire bonds are used to connect the upper device contacts because of the maturity of the wire-bonding process. However, the wire bond is known to be the main cause of failure of discrete devices under high-voltage, high-current applications due to the parasitic stray inductances. The wire-bonded module also sets space limits to the integration depth of power electronic systems. The two-dimensional packaging structure also places limits on heat dissipation capability. A standard chip and wire module is shown in Fig. 1.1.

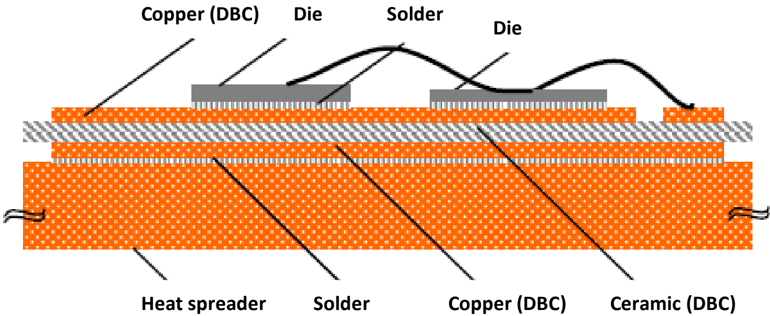

Fig. 1.1. A standard power chip and wire module [1].

For better thermal management and system performance, three-dimensional (3D) packaging aims at integration of entire modules and driver circuits into a compact stacked layer structure. The 3D modules include a metal post-interconnected parallel-plate structure (MPIPPS), flip-chip-on-flex (FCOF), stacked solder bumping (SSB), dimple-array interconnect (DAI) and double-side cooled direct solder interconnect, all developed at CPES [2]. The module is fabricated based on the soldering process, and the devices are sandwiched between two circuit substrates, such as direct-bond-copper (DBC) substrates. The devices are attached to the bottom substrate with solder using a conventional solder die-attach processes. 3D modules are built as stacked assemblies with a second interconnection layer on top of the devices, and a flexible substrate or a second DBC can be soldered on the die, leading to a multilayer assembly. A half-bridge flip-chip-on-flex integrated power module is shown in Fig. 1.2.

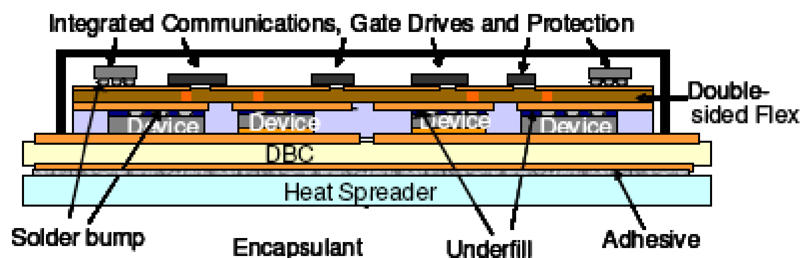

Fig. 1.2. A half-bridge flip chip on flex integrated power module [2].

Other 3D packaging modules include an embedded power assembly developed by CPES [3] and planar power polymer packaging (P4) developed by GE [4]. These are termed thin-film-based processes because of the method on deposition of the copper conductive layer. This study focuses on the packaging module based on the soldering process.

In short, the 3D packaging approach has several advantages compared to 2D packaging: (1) higher power density due to the compact layout; (2) less parasitic stray inductance, providing improved switching behavior and reduced overvoltage; (3) compact integration of control electronic components on the power assembly; and (4) improved heat paths and significantly reduced thermal resistance [5].

1.2. Power MOSFET packaging technology

The semiconductor's package has three basic functions: It connects the die to the external circuit, it removes heat generated in the device, and it protects the die from contamination such as dust and moisture. A traditional package comprises three basic components: lead frames, bond wires, and a molding compound, as shown in Fig. 1.3 [6].

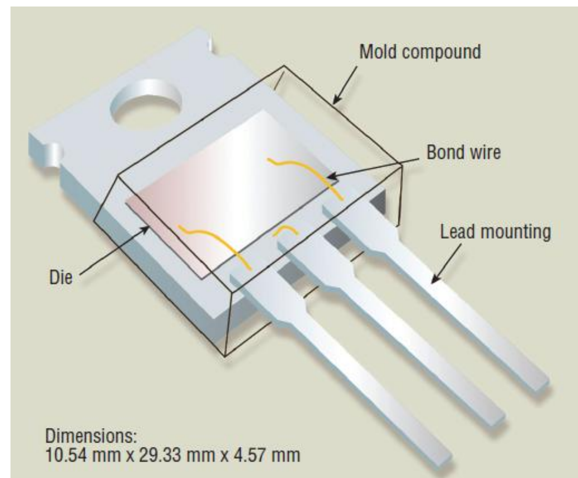

Fig. 1.3 A traditional device package [6].

Packaging is becoming a limiting factor for device high speed performance and thermal management. Package resistance can affect power and current capability. Current requirements have increased greatly in the past years. For processor applications, current requirements have increased beyond 100 A. The molding compound protects the semiconductor from contaminants as it conducts heat away from the die. Common power semiconductors use an epoxy-molding compound, with thermal conductivity k in the range of 0.9 to 1 W/mK. Metal can be considered to replace epoxy packages. The package's thermal conductivity often limits the device's current rating in high-power applications. Thus it is currently a trend to reduce the package related losses and improve thermal management.

In recent years, the SO-8 package and its descendants have dominated miniature power packaging. SO-8 packages improve thermal performance by providing a shorter thermal path. Instead of using thin wire bonds, thermally-enhanced SO-8 packages are used to mount the die on a copper pad with connections to the leads. Currently, the state-of-the-art technologies are DirectFET^{TM} from International Rectifier and DualCool^{TM} from Texas Instruments.

The DirectFET^{TM} is design to (1) reduce the electrical resistance of the package to a level insignificant relative to the MOSFET drain-source on-resistance; (2) reduce both junction-to-board and junction-to-topside thermal impedance of the package for dual-sided cooling applications; (3) facilitate the board layout and paralleling of the devices; and (4) to enable the use of existing surface mount assembly lines [7]. DirectFET^{TM} package and a cross section of the DirectFET^{TM} are shown in Fig. 1.4.

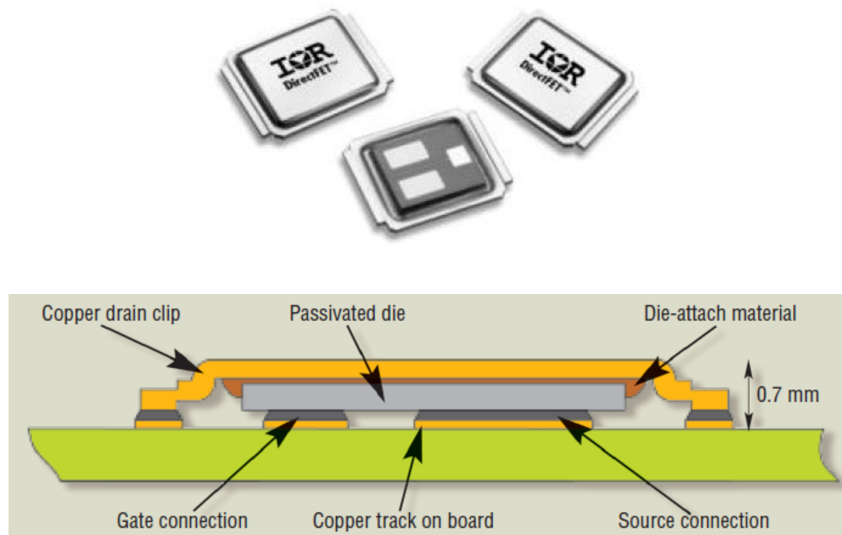

Fig. 1.4. DirectFET^{TM} package (above) and a cross section of DirectFET^{TM} Technology (bottom) [6].

The drain connection is made from the back of the die to the board through the use of a copper “can” into which the die has been bonded. The facilitator is a proprietary passivation system developed by International Rectifier. This passivation is applied to a wafer that has a solderable top metal stack rather than the aluminum top commonly used in wire-bonded devices. It is then

patterned to open out solderable areas on the surface of the die for the source and the gate connections. This allows the shape of the solder joints between the silicon and the circuit board to be closely controlled. The DirectFET™ can greatly reduce the conduction path through the package. Compared to the SO-8 package, DirectFET™ technology eliminates conduction paths in series with the silicon die. The direct coupling of the silicon to the board leads to a lower thermal resistance. The thermal resistance from the MOSFET to the top of the package is 3 ℃/W rather than the 25 ℃/W for an SO-8. By using dual-sided cooling, the junction-to-air thermal resistance can be less than 12 ℃/W.

The DualCool™ package design was developed by Texas Instruments and commercialized in 2010. In the DualCool™ package, the backside electrode of MOSFET die is attached to the lead frame of the package with solder and a copper clip is soldered to the topside electrode. The structure diagram of a DualCool™ package device is shown in Fig. 1.5 [8].

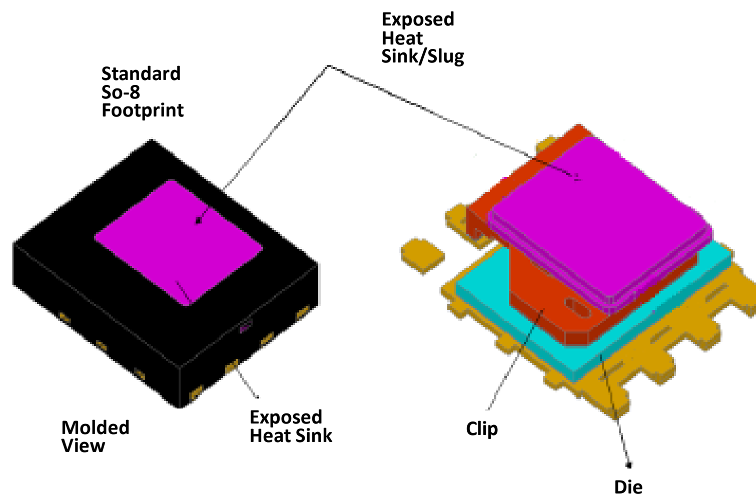

Fig. 1.5. Structure diagram of a DualCool™ device [8].

The DualCool™ package enables heat conduction to the top surface of the package through a high thermal-conductivity path, that reduces the junction-to-top thermal resistance by more than a factor of ten compared to the standard packages. The junction-to-top thermal resistance can be as low as 1 ℃/W.

1.3. Power module applications

In a power electronic converter system, higher power density and higher efficiency are desired for cost and space reduction. When reducing the volume of the converter, a high operating frequency can decrease the volume of the passive components. The high operating frequency leads to high switching losses, especially at the higher power levels. In order to avoid the degrading of the switching frequency at the higher power levels, a device with high blocking voltage and fast switching operation is required [9]. For sharing the voltages, the SiC JFETs connected in series are discussed in [10]. A compact high-voltage converter based on SiC JFETs is designed in [9]. The increasing power ratings of converters also need higher current. Current sharing in paralleled IGBT is discussed in [11]. The parasitic parameters have a large impact on the power systems' performance. Modeling and measurements of parasitic parameters for integrated power electronics modules is studied in [12], while the packaging parasitic inductance modeling in flip-chip flex-circuit packaging is studied in [13]. The use of double-side packaged IGBTs to improve thermal and switching characteristics is studied in [14], the current sharing between a wire-bonded module and a planar power module is compared in [15], and switching characteristic of the power packaging module using solder bump technology is investigated in [16]. There are many works in this field in addition to those mentioned here.

1.4. Focus of the thesis

Based on the above, a power module design is needed for high system performance and reliability, especially in terms of high efficiency and high power density. Low parasitic impedance is desired for the power loss and device current/voltage stress. Thermal management is also an important issue. A lower device temperature improves the device switching behavior and reduces power loss.

This study explores a voltage-sharing power MOSFET module. By series-connecting several low-voltage-rating devices, the breakdown voltage can be improved to be higher than in one device. In order to drive series-connected MOSFETs, a novel switch topology is proposed, and

then the power module is designed. The parasitic impedance and thermal resistance are simulated based on the layout dimensions and materials. Wire-bonded module and direct-bond module are compared. Finally, the direct-bond power module is assembled. A TI DualCool™ N-channel NexFET power MOSFET is used here because of its low junction-to-air thermal resistance. Flip-chip direct-bond technology is used to sandwich the MOSFET between two DBC substrates. Hence, low parasitic impedance and low thermal resistance are achieved, and a high breakdown voltage is obtained. In short, the advantages of our power module are: (1) compact size; (2) low parasitic impedances and (3) low thermal resistance. In future work the gate drive will be built and switching behavior will be tested.

1.5. Organization of the thesis

Chapter 1 introduces the state of art power packaging module and power MOSFET package. In addition, the power modules applications are introduced.

Chapter 2 proposes a series-connected power MOSFETs topology. This chapter analyzes the voltage-sharing in switch off-mode among the three series-connected power MOSFETs. The switching behaviors and energy losses are studied with and without parasitic inductances.

Chapter 3 presents parasite impedance extraction of the three series-connected power MOSFETs modules using Ansoft® Q3D extractor. A direct-bond module and a wire-bonded module are compared in terms of parasitic impedance. Also Chapter 3 presents thermal analysis of the three series-connected power MOSFETs modules using Ansoft® ePhysics. A double-substrate direct-bond module and a single-substrate direct-bond module are compared in terms of thermal resistance.

Chapter 4 presents the assembly process and the breakdown voltage testing of the three series-connected power MOSFETs module.

Chapter 5 gives the conclusion of the thesis. Contributions, problems and future works are also presented.

1.6. Conclusions

Power electronics module provides electrical interconnection, mechanical support, heat dissipation and protections of the devices. The optimal module design can improve the system's performance and reliability. This study proposes a series-connected power MOSFETs topology to improve the breakdown voltage, and the module is assembled using flip-chip direct-bond technology. This chapter provides basic background in power electronic packaging modules, power device packaging technology and the motivation for and introduction to this research on a series-connected power MOSFET module. The next chapter will introduce the proposed series-connected MOSFETs switch topology.

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Chapter 2: Series-connected Power MOSFETs Switch Topology

This chapter proposes a switch topology with series-connected MOSFETs. The switch is simulated in a chopper circuit in Synopsys Saber® Sketch [1], with a concentration on voltage sharing in the off-mode. The switching behavior and energy loss are investigated with and without parasitic inductances, and the most critical parasitic inductor parameter is identified. In addition, the wire-bonded module and direct-bond module are compared in terms of switching energy loss.

2.1. Proposed three series-connected MOSFETs switch topology

This work is to find how to successfully series-connect three MOSFETs together instead of using one MOSFET in a switching-mode power supply. The motivation for using a series-connected MOSFETs switch is to reduce the voltage stress on the MOSFETs and thus improve the breakdown voltage. Three series-connected MOSFETs will have a lower energy loss than one single MOSFET due to the lower off-mode voltage. Hence the module's thermal management and system performance will be improved. However, the system can become complex due to the extra diodes required, and there is also extra energy loss on the resistors. Therefore this thesis proposes a novel switch topology with three series-connected MOSFETs, which is shown in a chopper circuit in Fig. 2.1.

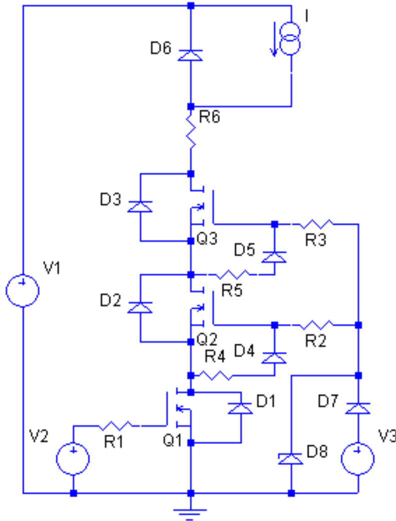

Fig. 2.1. Schematic of three series-connected MOSFETs in a chopper circuit.

In Fig. 2.1, V1 is a pulse voltage and provides low-side gate control of the switch. V3 is a DC voltage. When gate voltage V2 is higher than the threshold voltage, Q1 turns on; then the drain voltage of Q1 decreases to zero. The Q2 gate-source voltage consequently increases under V3, and Q2 turns on. Then the drain voltage of Q2 decreases to zero. The Q3 gate-source voltage consequently increases under V3, and Q3 turns on. Current can go through the three series-connected MOSFETs switch and the turn-on process is finished. The turn-on processes are shown in Fig. 2.2.

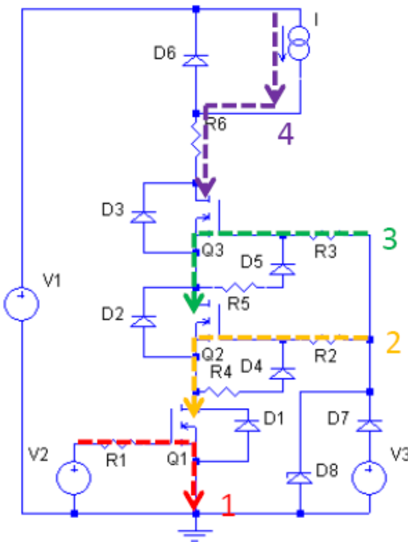

Fig. 2.2. Turn-on processes of three series-connected MOSFETs in a chopper circuit schematic.

When Q1 is turned off, the source voltage of Q2 is increased. By diode D4, the gate voltage of Q2 is increased. When the Q2 gate-source voltage is lower than the threshold voltage, Q2 is turned off. Then the Q3 source voltage is increased. By diode D5, the gate-source voltage of Q3 is increased. When the Q3 gate source voltage is lower than the threshold voltage, Q3 is turned off and the three series-connected MOSFETs switch turn-off process is finished. In the turn-off process, R1, R2, and R3 are used to limit the Q1, Q2, and Q3 turn-on currents, respectively. R4 and R2 are used to limit the Q2 turn-off current. R5 and R3 are used to limit the Q3 turn-off current. R4 and R5 cannot be too large or the gate-source voltage will be too low. If R2 and R3 are too large, the Q2 and Q3 turn on speed will be degraded. D1 to D3 are used to help switch off-mode voltage-sharing among the MOSFETs. The D7 and Zener D8 diodes provide protection for DC voltage V3. The turn-off processes are shown in Fig. 2.3.

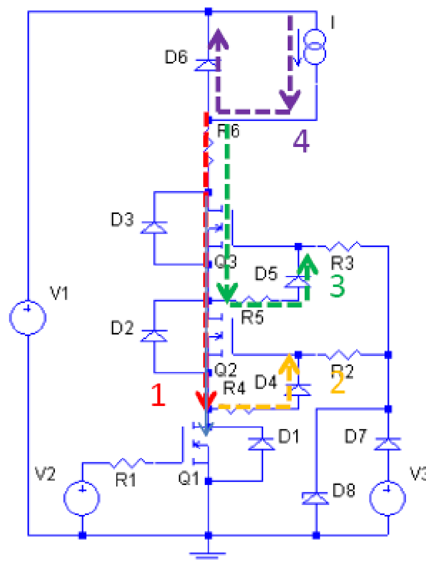

Fig. 2.3. Turn-off process of three series-connected MOSFETs in a chopper circuit schematic.

The package parasitic inductances are critical in the switching current and voltage slew rate, overshoot and ringing, and energy loss [2]. The circuit with parasitic inductance is shown in Fig.

2.4. The switching characteristics and energy loss need be compared with and without parasitic inductances.

Fig. 2.4. Schematic of three series-connected MOSFETs with parasitic inductances in a chopper circuit.

2.2. Three series-connected MOSFETs switch simulation

Saber® Sketch is used to perform the simulation. The circuit schematic with parasitic inductances is shown in Fig 2.5.

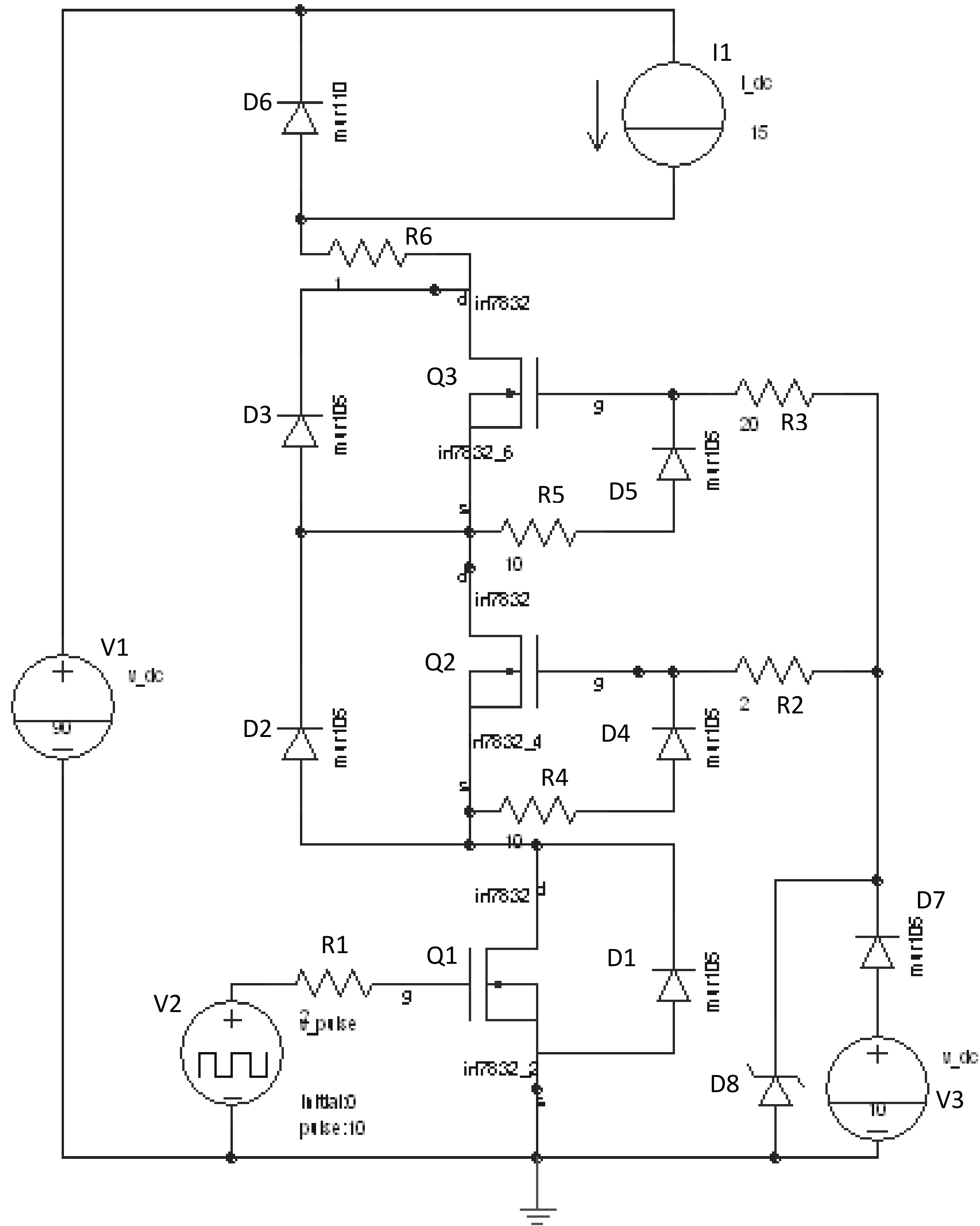

Fig. 2.5. Schematic of three series-connected MOSFETs without parasitic inductances in a chopper circuit in Saber® Sketch.

The devices and circuit specifications used in the simulation are summarized in the Table 2.1. Resistance R1 is 2 Ω, R2 is 5 Ω, R3 is 20 Ω, R4 and R5 are 8 Ω, and R6 is 1 Ω. Parasitic

inductances can be added to the terminals of the MOSFET and interconnections of the MOSFETs.

Table 2.1 Circuit specifications and device parameters for Fig. 2.5

Symbol	Component	Specifications
Q1, 2, 3	MOSFET: IRF7832	Drain source breakdown voltage: 30 V Continuous drain current: 16 A Threshold voltage: 2 V Gate-source voltage: ±20 V Qg: 34 nC gfs: 77 S Cgs: 3860 pF Cgd: 540 pF
D1,2, 3, 4,5,7	Diode: Mur105	Breakdown voltage: 50 V Average rectified forward current: 1 A
D6	Diode: Mur1510	Breakdown voltage: 100 V Average rectified forward current: 15 A
D8	Zener diode:BZX79-F10	Zener Voltage: 10 V Reverse leakage current: 7.5 A
V1	Input DC voltage	10-90 VDC
I1	DC Current	15 A
V2	Gate pulse voltage	10 V magnitude 100 k Freq, 50% duty cycle
V3	DC voltage	10 VDC

2.2.1. Voltage sharing in switch off-mode

To investigate the voltage sharing in the switch off-mode, the input voltage is changed from 30 V to 90 V. The three series-connected MOSFETs' switching off-mode drain-source voltage waveforms under the 90 V input voltage are shown in Fig. 2.6. The 90 V voltage is shared evenly among the three MOSFETs. Fig. 2.7 shows the three series-connected MOSFETs' drain-source voltages in switching off-mode from 10 V to 90 V input voltage. Fig. 2.8 shows the three series-connected MOSFETs' gate-source voltages for Q2 and Q3 in switching off-mode from 10 V to 90 V input voltage.

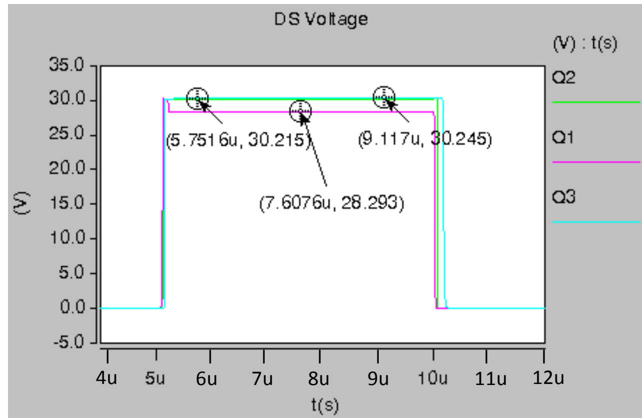

Fig. 2.6. Switching off-mode drain-source voltage waveforms of three series-connected MOSFETs without parasitic inductances under 90 V input voltage (circuit schematic in Fig. 2.5).

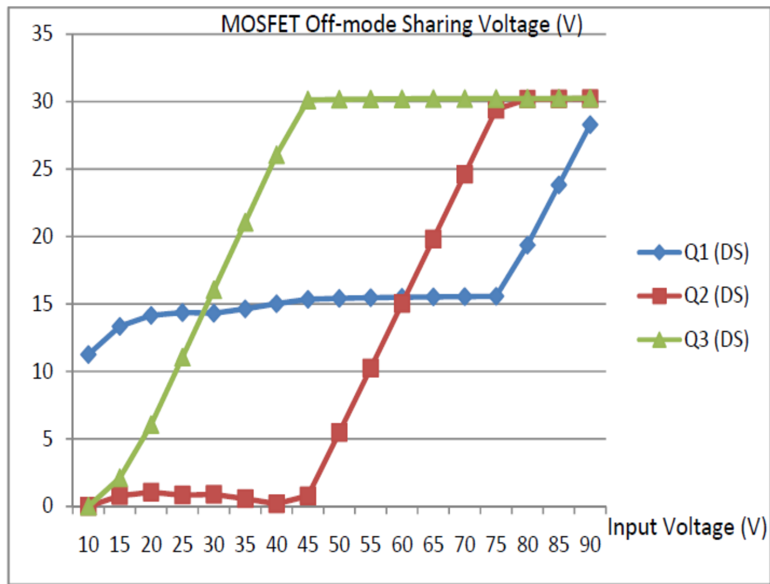

Fig. 2.7. Switching off-mode drain-source voltages of three series-connected MOSFETs without parasitic inductances under 10-90 V input voltages.

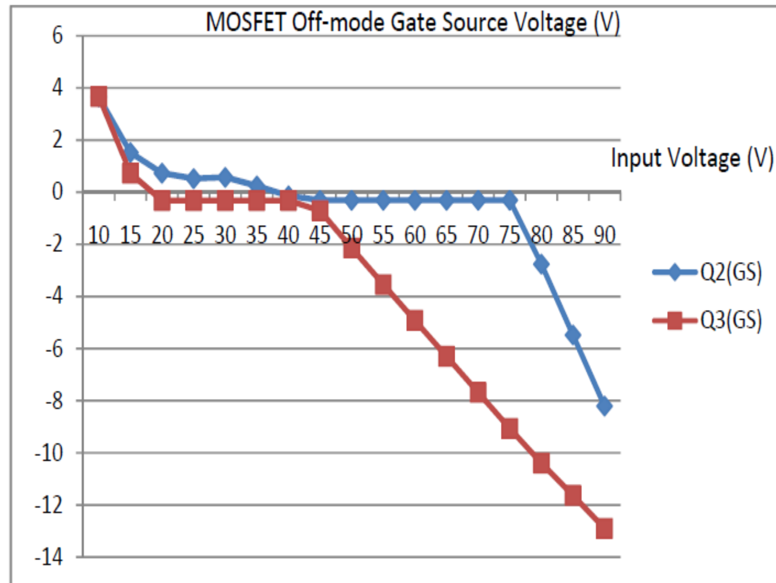

Fig. 2.8. Switching off-mode gate-source voltages of three series-connected MOSFETs without parasitic inductances under 10-90 V input voltages.

In Fig. 2.7, Q3 first goes up with Q1 to share the voltage in the lower voltage range. With an increase of the input voltage, Q2 goes up to help share the voltage. Q3 will reach its breakdown voltage first. Then Q2 reaches its breakdown voltage. Finally Q1 reaches its breakdown voltage, and mostly stays at half of the breakdown voltage. In Fig. 2.8, the Q2 and Q3 gate-source voltages decrease because of voltage sharing with the resistors. The Q1 gate-source voltage is always zero.

2.2.2. Switching characteristic and energy loss

Next, the MOSFET switching characteristic and energy loss are investigated under 90 V input. The first simulation uses a model without parasitic inductances, and the second simulation uses 5 nH as the parasitic inductance. The energy losses and parasitic inductance values of the wire-bonded and direct-bond module are obtained using the Ansoft® Q3D extractor simulation shown in the next chapter. The turn-on and turn-off transition waveforms of the gate-source voltages under 90 V input voltage without parasitic inductances are shown in Fig. 2.9. The turn-on and turn-

off sequences go from Q1, to Q2 to Q3. The turn-on and turn-off transition waveforms of the drain-source voltage under 90 V input voltage without parasitic inductances are shown in Fig. 2.10. The turn-on and turn-off transition waveforms of the drain-source currents under 90 V input voltage without parasitic inductances are shown in Fig. 2.11. The overshoot of the turn-on drain-source current of Q1, Q2 and Q3 is 32 A.

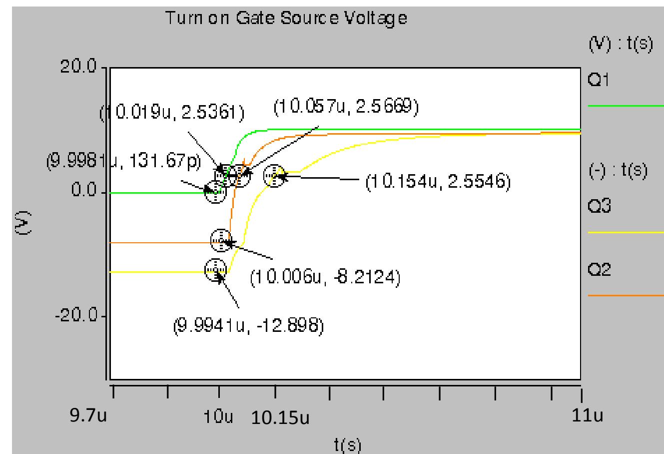

Fig. 2.9.a. Turn-on transition waveforms of gate-source voltage of three series-connected MOSFETs under 90 V input voltage without parasitic inductances (circuit schematic in Fig. 2.5).

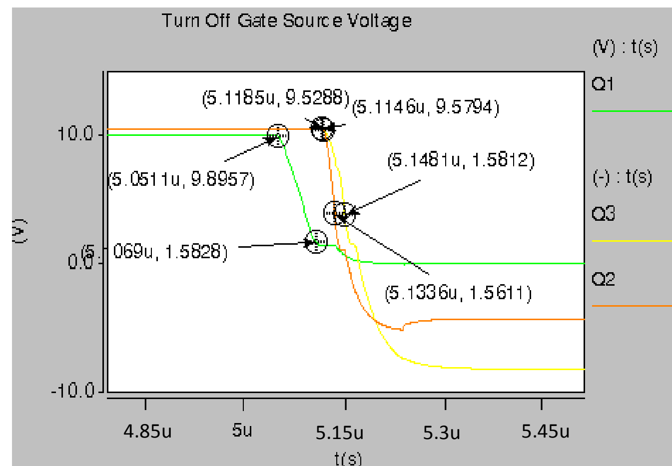

Fig. 2.9.b. Turn-off transition waveforms of gate-source voltage of three series-connected MOSFETs under 90 V input voltage without parasitic inductances (circuit schematic in Fig. 2.5).

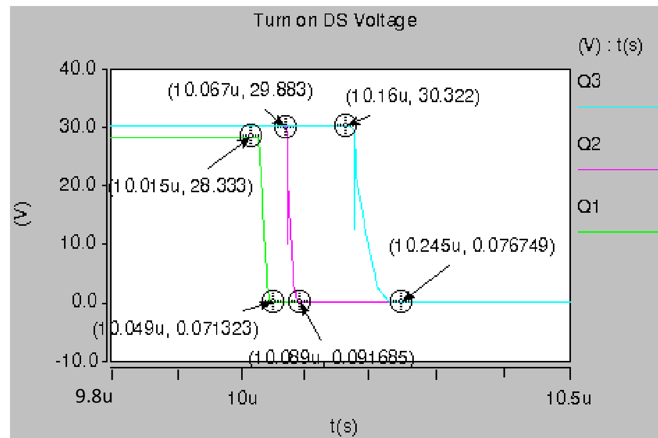

Fig. 2.10.a. Turn-on transition waveforms of drain-source voltage of three series-connected MOSFETs under 90 V input voltage without parasitic inductances (circuit schematic in Fig. 2.5).

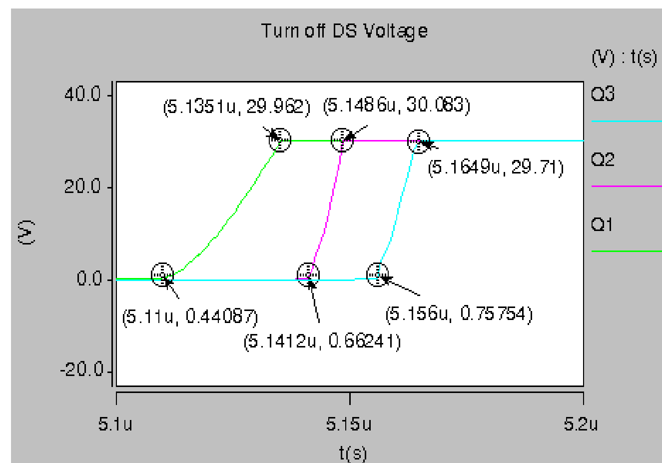

Fig. 2.10.b. Turn-off transition waveforms of drain-source voltage of three series-connected MOSFETs under 90 V input voltage without parasitic inductances (circuit schematic in Fig. 2.5).

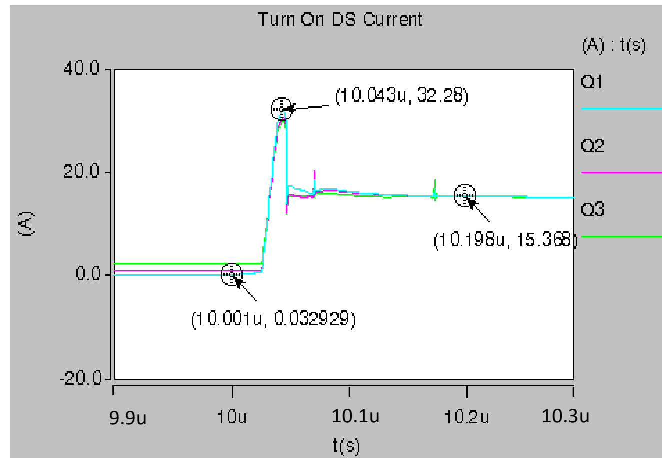

Fig. 2.11.a. Turn-on transition waveforms of drain-source current of three series-connected MOSFETs under 90 V input voltage without parasitic inductances (circuit schematic in Fig. 2.5).

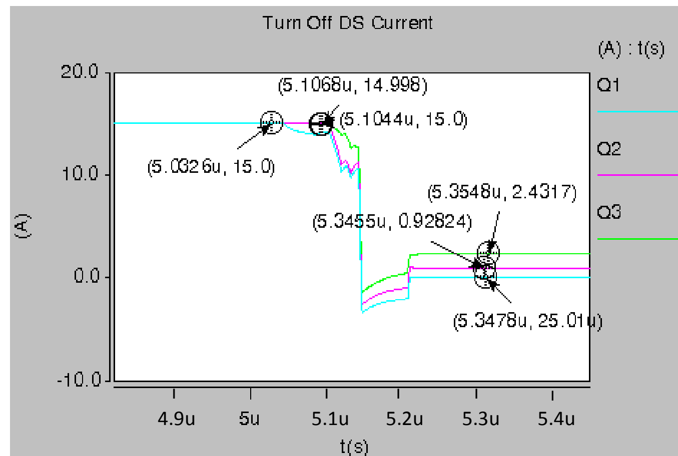

Fig. 2.11.b. Turn-off transition waveforms of drain-source current of three series-connected MOSFETs under 90 V input voltage without parasitic inductances (circuit schematic in Fig. 2.5).

The second simulation uses 5 nH as the parasitic inductance at the drain, source of the MOSFETs, and the interconnections between the MOSFETs. The turn-on and turn-off transition waveforms of the gate-source voltage under 90 V input voltage with 5 nH parasitic inductances are shown in Fig. 2.12. The turn-on and turn-off transition waveforms of the drain-source voltage under 90 V input voltage with 5 nH parasitic inductances are shown in Fig. 2.13. The overshoot of the turn-on drain-source voltage of Q3 is 65 V. The snubber circuit or soft

switching need be considered for Q3. The turn-on and turn-off transition waveforms of the drain-source current under 90 V input voltage with 5 nH parasitic inductances are shown in Fig. 2.14. The turn-on drain-source overshoot current of Q1, Q2 and Q3 is 25 A. There are small drain-source voltage and current oscillations at the end of the turn-off process.

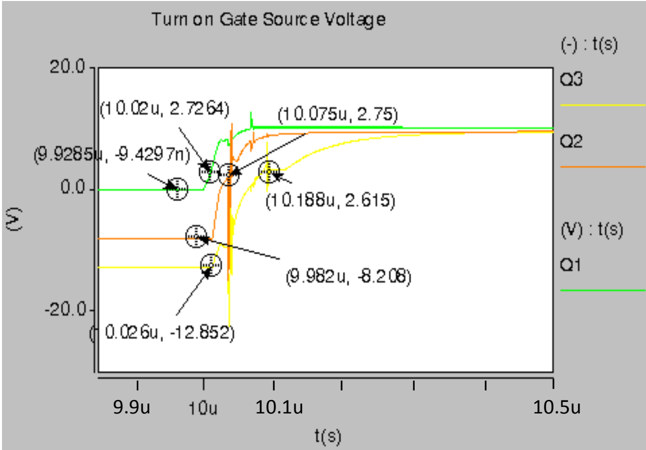

Fig. 2.12.a. Turn-on transition waveforms of gate-source voltage of three series-connected MOSFETs under 90 V input voltage with 5 nH parasitic inductances (circuit schematic in Fig. 2.4).

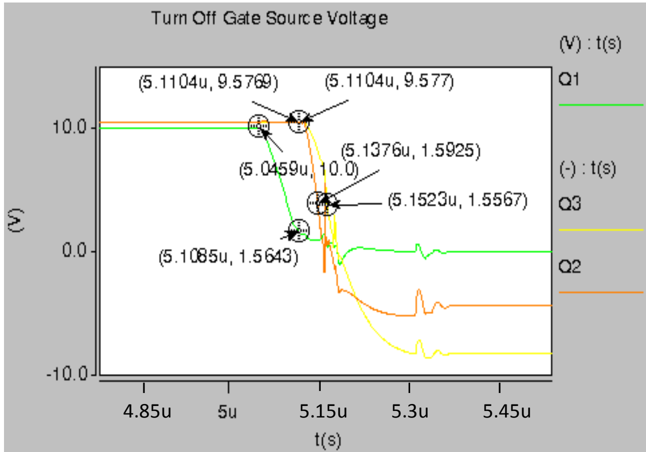

Fig. 2.12.b. Turn-off transition waveforms of gate-source voltage of three series-connected MOSFETs under 90 V input voltage with 5 nH parasitic inductances (circuit schematic in Fig. 2.4).

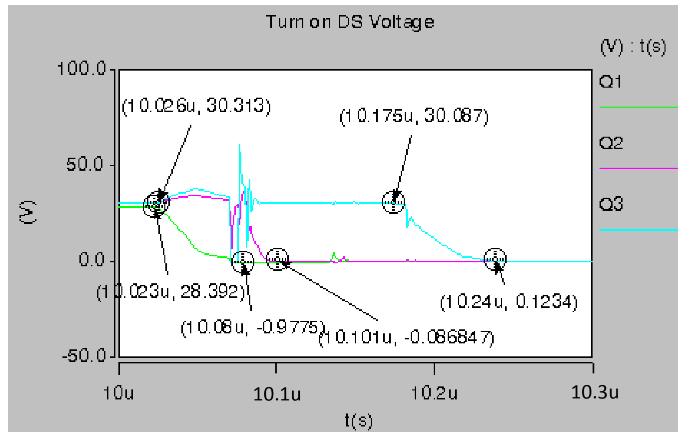

Fig. 2.13.a. Turn-on transition waveforms of drain-source voltage of three series-connected MOSFETs under 90 V input voltage with 5 nH parasitic inductances (circuit schematic in Fig. 2.4).

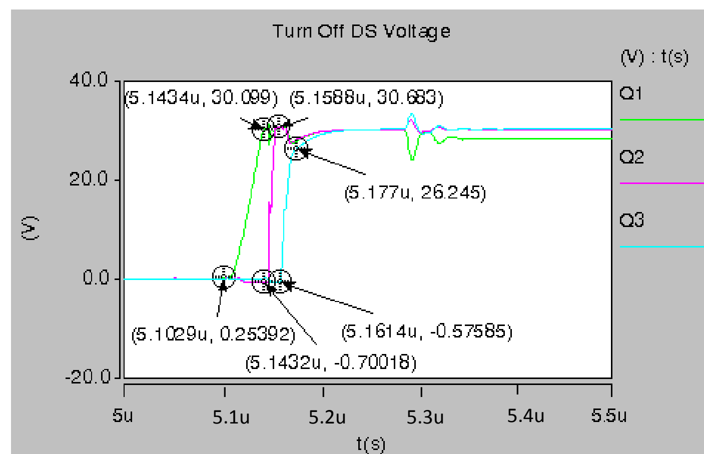

Fig. 2.13.b. Turn-off transition waveforms of drain-source voltage of three series-connected MOSFETs under 90 V input voltage with 5 nH parasitic inductances (circuit schematic in Fig. 2.4).

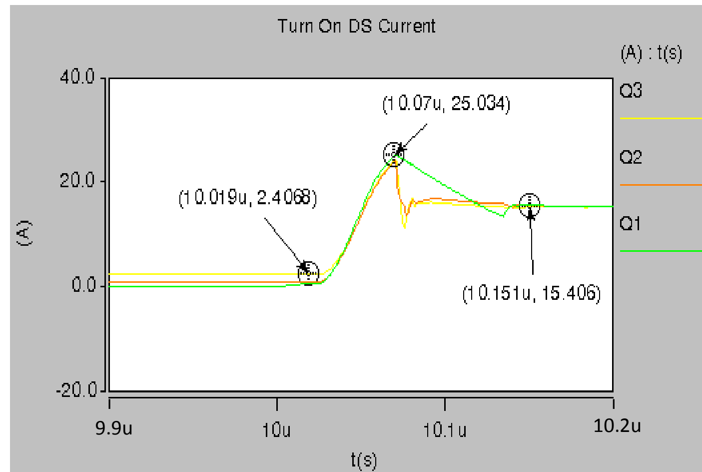

Fig. 2.14.a. Turn-on transition waveforms of drain-source current of three series-connected MOSFETs under 90 V input voltage with 5 nH parasitic inductances (circuit schematic in Fig. 2.4).

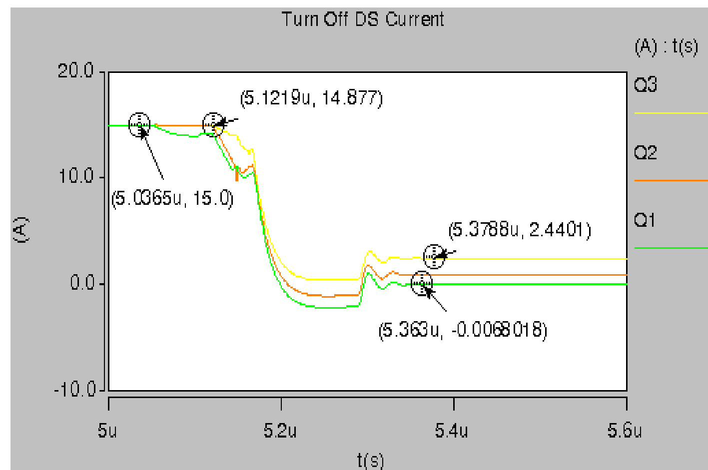

Fig. 2.14.b. Turn-off transition waveforms of drain-source current of three series-connected MOSFETs under 90 V input voltage with 5 nH parasitic inductances (circuit schematic in Fig. 2.4).

The three series-connected MOSFETs switching energy losses with and without 5nH parasitic inductances are summarized in Table 2.2 and Table 2.3.

Table 2.2 Switching energy losses of three series-connected MOSFETs without parasitic inductance (circuit schematic in Fig. 2.5)

Energy loss (μJ)	**Turn-off**	**Turn-on**	**Total**
Q1	32.27	25.44	57.71
Q2	16.81	31.93	48.74
Q3	7.83	89.1	96.93
Total	56.91	146.47	203.38

Table 2.3 Switching energy losses of three series-connected MOSFETs with 5 nH parasitic inductances (circuit schematic in Fig. 2.4)

Energy loss (μJ)	**Turn-off**	**Turn-on**	**Total**
Q1	46.43	34.19	80.62
Q2	41.15	48.64	89.79
Q3	51.23	94.85	146.08
Total	138.81	177.68	316.49

Based on the calculations, the parasitic inductances cause energy loss during switching. The turn-on and turn-off energy loss increase as the parasitic inductance increases. The Q2–Q3 interconnection parasitic inductance value is the most critical parameter, which mostly impacts the Q3 turn-off energy loss by contributing about 44.4% of the total switching energy loss. The energy losses with 5 nH Q2-Q3 interconnection parasitic inductance are shown in Table 2.4.

Table 2.4 Switching energy losses of three series-connected MOSFETs with 5 nH Q2-Q3 interconnection parasitic inductance (circuit schematic in Fig. 2.4)

Energy loss (μJ)	**Turn-off**	**Turn-on**	**Total**
Q1	33.19	27.06	60.25
Q2	33.32	34.38	67.7
Q3	29.97	95.73	125.7
Total	96.48	157.17	253.65

The energy losses are calculated for the wire-bonded module and direct-bond module, and shown in Table 2.5 and Table 2.6, respectively. The parasitic inductances are obtained from the

simulations performed in Chapter 3. These simulations show that the direct-bond module has lower energy loss than the wire-bonded module.

Table 2.5 Switching energy losses of three series-connected MOSFETs wire-bonded module (circuit schematic in Fig. 2.4)

Energy loss (μJ)	**Turn-off**	**Turn-on**	**Total**
Q1	42.09	33.93	76.02
Q2	39.41	44.61	84.02
Q3	42.84	93.3	136.14
Total	124.34	171.84	296.18

Table 2.6 Switching energy losses of three series-connected MOSFETs direct-bond module (circuit schematic in Fig. 2.4)

Energy loss (μJ)	**Turn-off**	**Turn-on**	**Total**
Q1	33.39	29.94	63.33
Q2	33.85	22.82	56.67
Q3	25.59	93.4	118.99
Total	92.83	146.16	238.99

2.3. Conclusions

This chapter presents the topology to perform series-connected power MOSFETs switching. The switch was simulated in a chopper circuit. The MOSFETs off-mode voltage sharing was investigated and switching behaviors and energy losses were studied with and without parasitic inductances. The parasitic inductances introduced significant energy loss. For the three series-connected MOSFETs, the most critical parasitic inductor parameter is identified as that of the Q2-Q3 interconnection, and the wire-bonded module and direct-bond module were compared in terms of switching energy loss. The following chapter introduces methods to obtain the parasitic parameters in module layout using Ansoft® Q3D extractor, and to perform thermal analysis using Ansoft® ePhysics.

2.4. References

[1] Synopsys Saber, Version 4, Synopsys Inc., Mountain View, CA, 2010.

[2] Y. Xiao, H. Shah, T. P. Chow and R. J. Gutmann, "Analytical modeling and experimental evaluation of interconnect parasitic inductance on MOSFET switching characteristics", in *Proc. Applied Power Electronics Conference and Exposition*, 2004, pp. 516-521.

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Chapter 3: Power Module Parasitic Parameter Extraction and Thermal Analysis

This chapter introduces the extraction of parasitic parameters and thermal analysis of power module. The layout parasitic parameters and junction temperature are critical for the system performance and reliability. Double-substrate direct-bond by flip-chip technology will be introduced and used in the module assembly in later chapters. The double-substrate direct-bond module is compact and with better thermal management than single-substrate direct-bond module. A DualCool™ device makes this module much easier to assemble with low parasitic impedance and thermal resistance. For the comparisons, a wire-bonded module is also modeled. Ansoft® Q3D extractor will be used for extracting the capacitance, inductance and resistance of the conductors in the module [1]. Ansoft® ePhysics will be used for obtaining the module temperature under power loads [2].

3.1. Parasitic parameter extraction of power module

Ansoft® Q3D extractor is used to characterize the structural impedance of the three dimensional interconnector structures and impedance matrices based on the theory of partial element equivalent circuit (PEEC) [3]. The processes include a three dimensional representation of the structure, material characteristic of the object, and source excitation. Then the impedance matrices are generated. The multi-pole solver [4] is used to simulate the electrical fields and from which capacitances are computed; while the conduction solver is used to simulate the electrical current from which resistances and inductances are computed.

In Ansoft® Q3D, an approximate method is used to compute the parasitic resistance and inductance. All AC currents are assumed to be surface currents obtained from DC solutions as follows. And AC resistances are corrected for skin effect [5].

From DC solution, the magnetic field intensity $\vec{H}$ is calculated as:

$$\vec{A} = \frac{\mu_0}{4\pi} \iiint \frac{\vec{J}}{r} dV \tag{3.1}$$

$$\vec{H} = \frac{1}{\mu_0} \nabla \times \vec{A} \tag{3.2}$$

where $\vec{A}$ is magnetic vector potential (*Wb/m*), $\vec{J}$ is current density vector (A/m^2), *r* is distance, *V* is volume, and μ_0 is permeability of free space ($4\pi 10^{-7} H/m$).

For AC current, the surface magnetic field is calculated as:

$$\vec{H} \cdot \hat{n} = 0 \tag{3.3}$$

where $\hat{n}$ is the vector normal to surface.

At high frequencies, the magnetic field is tangential to the surface of a good conductor. The surface current density is calculated as:

$$\vec{K} = \hat{n} \times \vec{H} \tag{3.4}$$

The magnetic vector potential as high frequency is calculated as:

$$\vec{A}_i = \frac{\mu_0}{4\pi} \iint \frac{\vec{K}_i}{|r|} d\Omega \tag{3.5}$$

AC inductance matrix elements are calculated as:

$$L_{ij} = \iiint \vec{A}_i \cdot \vec{K}_j dV \tag{3.6}$$

Equivalent current density based on skin depth δ is calculated as:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \tag{3.7}$$

$$\vec{J} = \frac{\vec{K}}{\delta} \tag{3.8}$$

The electric field and the power are calculated as:

$$\vec{E} = \frac{\vec{J}}{\sigma} \tag{3.9}$$

$$P = \vec{E} \cdot \vec{J} = \frac{\vec{J} \cdot \vec{J}}{\sigma} = I^2 R \tag{3.10}$$

The AC resistance is calculated as:

$$R = \frac{P}{I^2} \tag{3.11}$$

The AC inductances and AC resistances can be obtained based on equations (3.6) and (3.11), respectively.

3.1.1. Parasitic parameter extraction of three series-connected MOSFETs in a direct-bond module

The layout of packaging interconnector and substrate are modeled in 3D, as shown in Fig 3.1. The interconnector and substrate are set with the materials. The layout parameter and material conductivity are shown in Table 3.1. Then the simulated current net is constructed and the source and sink are specified. As the final step in the solution setup, the capacitance, the DC resistance/ inductance and the AC resistance/inductance are selected to solve. The solver residual is 1e-05 and the solution frequency is 100 MHz.

Table 3.1 Layout parameters of direct-bond module with the three series-connected MOSFETs

	Thickness (mil)	**Size (mil×mil)**	**Conductivity (1/Ω×m)**
Silicon die	10	160×180	0
Solder	2	Same as top substance	7E6
Al_2O_3	25	590×1110	0
Copper (DBC substrate)	8	590×1110	5.8E7

The three-dimensional layout of the direct-bond module with three series-connected MOSFETs is shown in Fig. 3.1. The substrates and die layout dimensions are shown in Table 3.1. The

source and sink for each section of the conductors in the substrates are shown in Fig. 3.2 and Fig. 3.3. The area within the green line in Fig. 3.2 is the Q3-Q2 interconnector pad. The area within the yellow line in Fig. 3.2 is the Q2 gate pad. The area within the red line in Fig. 3.2 is the Q1 source pad. The area within the green line in Fig. 3.3 is the Q2-Q1 interconnector pad. The area within the yellow line in Fig. 3.3 is the Q3 gate pad. The area within the red line in Fig. 3.3 is the Q1 gate pad. The area within the blue line in Fig. 3.3 is the Q3 drain pad. Based on the layout of the conductive materials and non-conductive materials, the nets for the conductor are constructed on conductive materials. In this case, copper is the conductive net. For simulation, the sink and source are defined at the surface areas of the conductors. Hence the conductors' impedances are obtained for both DC and AC conditions.

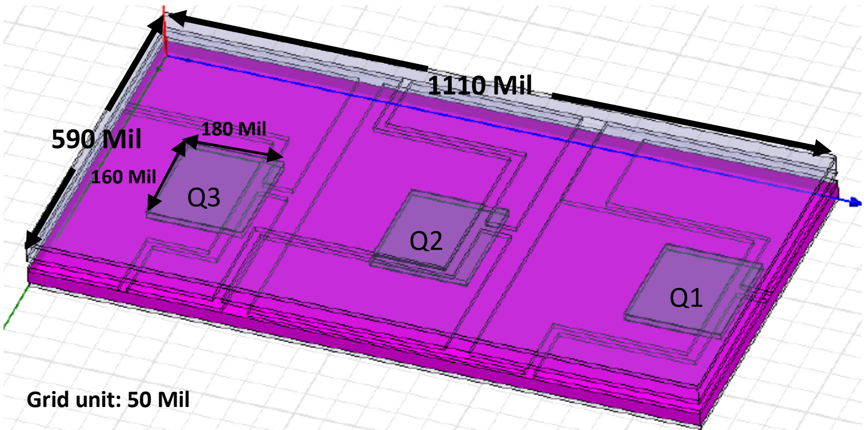
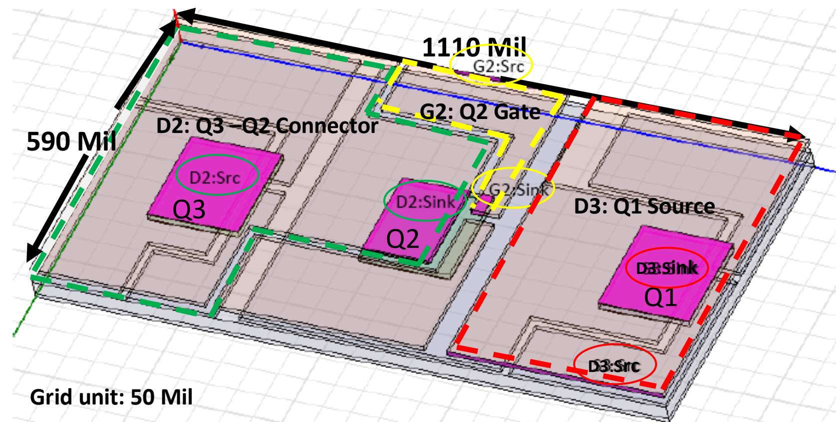


Fig. 3.1. Layout of the three series-connected MOSFETs direct-bond module (layout dimensions in Table 3.1) in Ansoft® Q3D extractor.



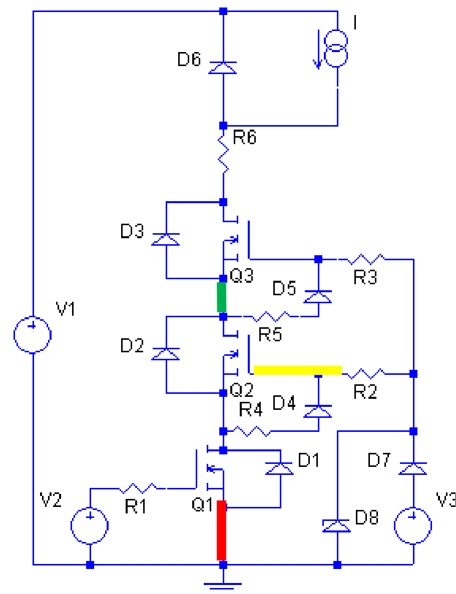
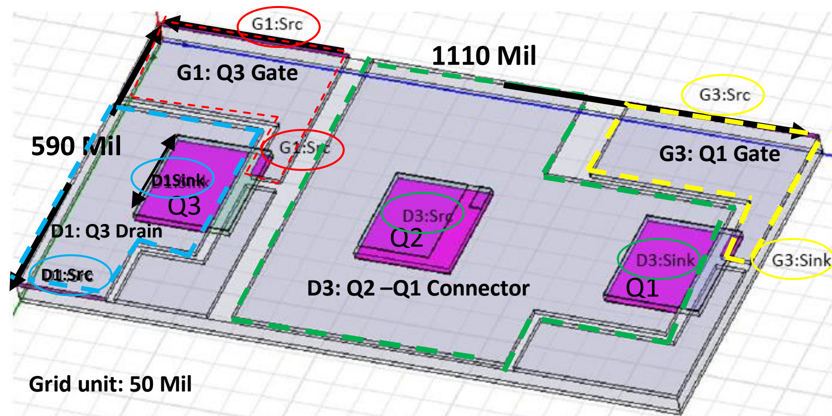


Fig. 3.2. Layout of the three series-connected MOSFETs direct-bond module top substrate pads (layout dimensions in Table 3.1) in Ansoft® Q3D extractor (above) and substrate pad positions in circuit schematic (below).



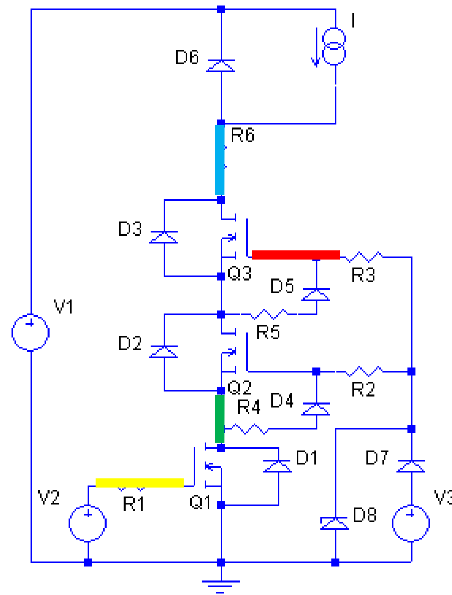


Fig. 3.3. Layout of the three series-connected MOSFETs direct-bond module bottom substrate pads (layout dimensions in Table 3.1) in Ansoft® Q3D extractor (above) and substrate pad positions in circuit schematic (below).

The parasitic capacitances are shown in Table 3.2. The DC resistance and AC resistance are shown in Table 3.3 and Table 3.4, respectively. The DC and AC inductance are shown in Table 3.5 and Table 3.6, respectively. D1, D2, S3, D3, G1, G2, and G3 are the names of the pads on the layout. In Tables 3.3 - 3.6, the diagonal elements are self-resistances/inductances. The other

elements are mutual resistances/inductances. The sign (+/-) in the partial mutual resistances/inductances represents the relative orientation of the segment currents.

Table 3.2 Capacitance matrix of the three series-connected MOSFETs direct-bond module

Capacitance Matrix (pF)							
	D1	**D2**	**S3**	**D3**	**G1**	**G3**	**G2**
D1	15.374	-7.057	-1.49E-05	-0.0028324	-0.0939	-4.69E-05	-0.0003339
D2	-7.057	41.36	-0.00071	-6.5131	-1.3111	-0.00109	-0.10397
S3	-1.49E-05	-0.00071	30.065	-7.2587	-1.43E-05	-1.2815	-0.0005486
D3	-0.0028	-6.5131	-7.2587	45.277	-0.0030	-0.085197	-0.97964
G1	-0.0938	-1.3111	-1.43E-05	-0.0030244	7.0623	0	0
G3	-4.69E-05	-0.00109	-1.2815	-0.085197	0	6.8566	0
G2	-0.0003	-0.10397	-0.00055	-0.97964	0	0	5.0325

Table 3.3 DC resistance matrix of the three series-connected MOSFETs direct-bond module

DC Resistance Matrix (mΩ)							
	D1	**D2**	**S3**	**D3**	**G1**	**G3**	**G2**
D1	0.11901	0	0	0	0	0	0
D2	0	0.076432	0	0	0	0	0
S3	0	0	0.048512	0	0	0	0
D3	0	0	0	0.080212	0	0	0
G1	0	0	0	0	0.27177	0	0
G3	0	0	0	0	0	0.28312	0
G2	0	0	0	0	0	0	0.35064

Table 3.4 AC resistance matrix of the three series-connected MOSFETs direct-bond module

AC Resistance Matrix (mΩ)							
	D1	**D2**	**S3**	**D3**	**G1**	**G3**	**G2**
D1	3.5745	0.22308	-0.03311	0.022958	-0.05748	0.043804	0.02376
D2	0.22308	2.5917	-0.02032	0.19276	0.13154	0.010933	0.13665
S3	-0.0331	-0.02032	1.6351	0.17206	0.010714	-0.04361	-0.07562
D3	0.02296	0.19276	0.17206	2.8761	0.028264	0.080746	0.16777
G1	-0.0575	0.13154	0.010714	0.028264	6.4158	-0.04233	0.041628
G3	0.0438	0.010933	-0.04361	0.080746	-0.04233	6.3806	-0.00261
G2	0.02376	0.13665	-0.07562	0.16777	0.041628	-0.00261	7.9528

Table 3.5 DC inductance matrix of the three series-connected MOSFETs direct-bond module

DC Inductance Matrix (nH)							
	D1	**D2**	**S3**	**D3**	**G1**	**G3**	**G2**
D1	1.9332	0.20457	0.1493	0.095601	-0.32215	-0.1236	-0.19824
D2	0.20457	1.826	0.056236	0.54089	0.13408	0.10071	0.20684
S3	0.1493	0.056236	1.1487	0.35994	-0.17435	-0.31459	-0.3268
D3	0.0956	0.54089	0.35994	2.2244	0.086935	0.23036	0.075084
G1	-0.3222	0.13408	-0.17435	0.086935	2.9355	0.2428	0.46942
G3	-0.1236	0.10071	-0.31459	0.23036	0.2428	2.9931	0.47006
G2	-0.1982	0.20684	-0.3268	0.075084	0.46942	0.47006	3.2692

Table 3.6 AC inductance matrix of the three series-connected MOSFETs direct-bond module

AC Inductance Matrix(nH)							
	D1	**D2**	**S3**	**D3**	**G1**	**G3**	**G2**
D1	1.3653	0.18087	0.19344	0.12435	-0.2833	-0.1577	-0.23165
D2	0.18087	1.3399	0.092564	0.57185	0.09887	0.09992	0.2217
S3	0.19344	0.09256	0.89866	0.33579	-0.1989	-0.2233	-0.28534
D3	0.12435	0.57185	0.33579	1.791	0.05501	0.37406	0.049668
G1	-0.2833	0.09887	-0.19888	0.05501	1.6786	0.27245	0.47969
G3	-0.1577	0.09992	-0.22326	0.37406	0.27245	1.7827	0.48524
G2	-0.2317	0.2217	-0.28534	0.04967	0.47969	0.48524	1.7317

3.1.2. Parasitic parameter extraction of three series-connected MOSFETs in a wire-bonded module

A three-dimensional layout of the wire-bonded module with three series-connected MOSFETs in Ansoft® Q3D is shown in Fig. 3.4. The substrate and die layout dimension is shown in Table 3.1. The aluminum wire radius is used as 5 mil. The conduction pads with source and sink, and corresponding positions in the circuit schematic are shown in Fig. 3.5 and Fig. 3.6. The dotted lines in Fig. 3.5 and Fig. 3.6 represent the wire bonds.

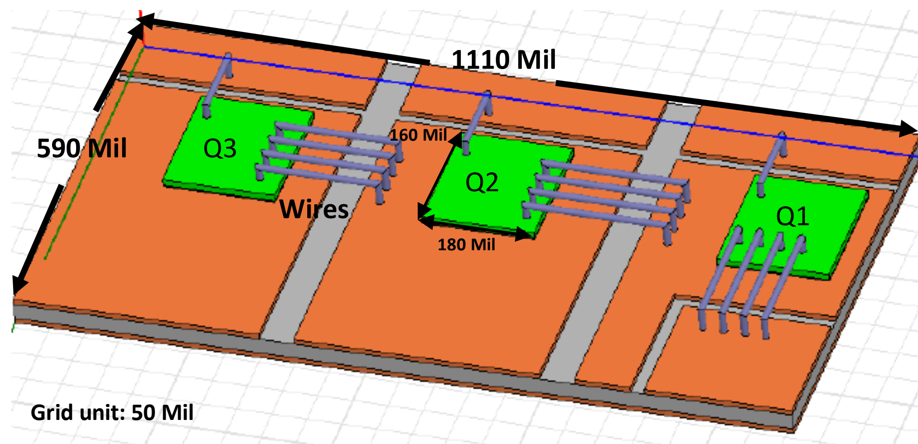
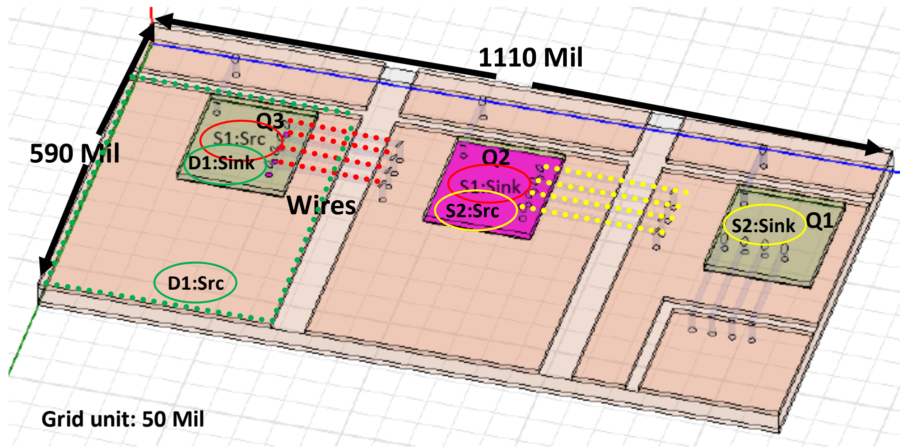


Fig. 3.4. Layout of the three series-connected MOSFETs wire-bonded module (layout dimensions in Table 3.1) in Ansoft® Q3D extractor.

Fig. 3.5. Layout of the three series-connected MOSFETs wire-bonded module substrate pads and wires (layout dimensions in Table 3.1) in Ansoft® Q3D extractor (above) and substrate pad and wire positions in circuit schematic (below).



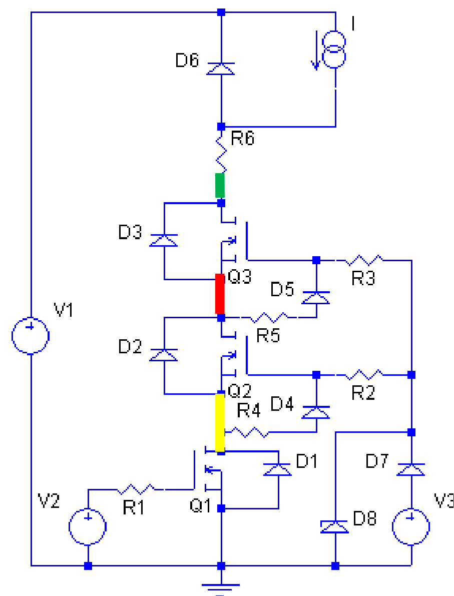


Fig. 3.6. Layout of the three series-connected MOSFETs wire-bonded module substrate pads and wires (layout dimensions in Table 3.1) in Ansoft® Q3D extractor (above) and substrate pad and wire positions in circuit schematic (below).

The parasitic capacitances are shown in Table 3.7. The DC resistance and AC resistance are shown in Table 3.8 and Table 3.9, respectively. The DC and AC inductances are shown in Table 3.10 and Table 3.11, respectively. G1, G2, G3, S1, S2, S3 and D1 are the names of the pads or wires of the layout. In Table 3.8 - 3.11, the diagonal elements are self-resistances/inductances.

Others are mutual resistances/inductances. The sign (+/-) in the partial mutual resistances/inductances accounts for the relative orientation of the segment currents.

Table 3.7 Capacitance matrix of the three series-connected MOSFETs wire-bonded module

Capacitance Matrix(pF)							
	G1	**G2**	**G3**	**S1**	**S2**	**S3**	**D1**
G1	3.9417	-0.01763	-0.00142	-0.01478	-0.00234	-0.00109	-0.31461
G2	-0.0176	4.0257	-0.01766	-0.31396	-0.01362	-0.00195	-0.00762
G3	-0.0014	-0.01766	3.522	-0.00759	-0.29966	-0.0063	-0.00226
S1	-0.0148	-0.31396	-0.00759	17.357	-0.50898	-0.01234	-0.48104
S2	-0.0023	-0.01362	-0.29966	-0.50898	11.461	-0.67602	-0.00583
S3	-0.0011	-0.00195	-0.0063	-0.01234	-0.67602	4.4774	-0.00323
D1	-0.3146	-0.00762	-0.00226	-0.48104	-0.00583	-0.00323 Q1	16.539

Table 3.8 DC resistance matrix of the three series-connected MOSFETs wire-bonded module

DC Resistance Matrix(mΩ)							
	G1	**G2**	**G3**	**S1**	**S2**	**S3**	**D1**
G1	1.9756	0	0	0	0	0	0
G2	0	1.9773	0	0	0	0	0
G3	0	0	1.9760	0	0	0	0
S1	0	0	0	0.7459	0	0	0
S2	0	0	0	0	0.84888	0	0
S3	0	0	0	0	0	0.77333	0
D1	0	0	0	0	0	0	0.074087

Table 3.9 AC resistance matrix of the three series-connected MOSFETs wire-bonded module

AC Resistance Matrix(mΩ)							
	G1	**G2**	**G2**	**S1**	**S2**	**S3**	**D1**
G1	17.187	-0.0489	-0.0325	0.073934	0.003636	-0.03972	-0.23022
G2	-0.0489	17.178	0.06924	-0.23073	0.076855	-0.02757	0.016678
G3	-0.0325	0.06924	17.18	0.00468	-0.0384	-0.00725	0.00937
S1	0.073934	-0.23073	0.00468	7.9234	0.18694	0.069583	0.21687
S2	0.003636	0.076855	-0.0384	0.18694	9.3965	0.2892	0.081282
S3	-0.03972	-0.02757	-0.00725	0.069583	0.2892	8.9917	0.12653
D1	-0.23022	0.016678	0.00937	0.21687	0.081282	0.12653	2.0988

Table 3.10 DC inductance matrix of the three series-connected MOSFETs wire-bonded module

DC Inductance Matrix(nH)							
	G1	**G2**	**G3**	**S1**	**S2**	**S3**	**D1**
G1	2.7876	0.22802	0.22659	-0.03399	-0.01391	0.15634	-0.41297
G2	0.22802	2.7984	-0.0273	-0.03207	-0.05207	0.24638	-0.28936
G3	0.22659	-0.0273	2.798	-0.0289	-0.0248	0.26931	-0.2467
S1	-0.034	-0.03207	-0.0289	2.7038	0.53604	0.000852	0.013128
S2	-0.0139	-0.05207	-0.0248	0.53604	3.2977	0.005182	0.026349
S3	0.15634	0.24638	0.26931	0.000852	0.005182	3.4368	-0.29206
D1	-0.413	-0.28936	-0.2467	0.013128	0.026349	-0.29206	2.0809

Table 3.11 AC inductance matrix of the three series-connected MOSFETs wire-bonded module

AC Inductance Matrix(nH)							
	G1	**G2**	**G3**	**S1**	**S2**	**S3**	**D1**
G1	2.377	0.27784	0.27632	-0.08713	-0.01995	0.19877	-0.44313
G2	0.27784	2.3456	-0.0692	-0.03172	-0.10257	0.30216	-0.33822
G3	0.27632	-0.0692	2.365	-0.0592	-0.0938	0.2892	-0.3352
S1	-0.0871	-0.03172	-0.0592	2.2529	0.4961	-0.03614	-0.02328
S2	-0.02	-0.10257	-0.0938	0.4961	2.7275	-0.09387	0.006519
S3	0.19877	0.30216	0.2892	-0.03614	-0.09387	2.9313	-0.37429
D1	-0.4431	-0.33822	-0.3352	-0.02328	0.006519	-0.37429	1.8526

3.1.3. Equivalent circuit model from Ansoft® Q3D extractor

After extracting the parameters, Ansoft® Q3D extractor constructs an equivalent circuit of the model [1]. The methods of construction depend on whether the conductors have one source or multiple sources. In this case only a single-source conductor is applied. For all conductors which have just one source terminal and one sink terminal, the system creates a balanced circuit to model the transmission structure. The impedance of the circuit is the same regardless of the direction of the current flow. A two-conductor transmission structure is shown in Fig. 3.7. Each conductor has one source and one sink. The current goes from source to sink.

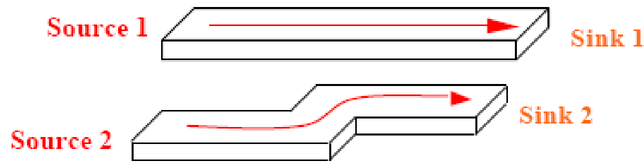


Fig. 3.7. Two conductor transmission structures [1].

The parameter matrices of inductances, resistances, and capacitances for this model are:

$$\begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{22} \end{bmatrix} \begin{bmatrix} R_{11} & 0 \\ 0 & R_{22} \end{bmatrix} \begin{bmatrix} C_{11} & C_{12} \\ C_{12} & C_{22} \end{bmatrix} \quad (3.12)$$

The mutual resistance between them is 0. The mutual capacitance C_{12} is used directly as a circuit element. The self-capacitances of each conductor, C_{11} and C_{22}, are used to compute the capacitances between the conductor and ground, C_{10} and C_{20}.

$$\begin{cases} C_{10} = C_{11} - C_{12} \\ C_{20} = C_{22} - C_{12} \end{cases} \quad (3.13)$$

To create a balanced circuit, each inductance or resistance matrix entry is divided into two series inductors or resistors, as shown in Fig. 3.8.

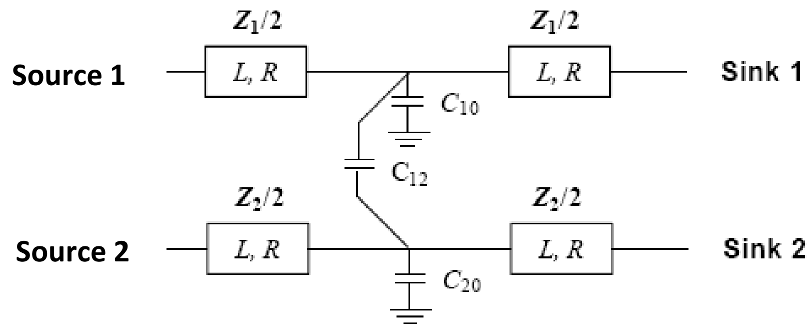


Fig. 3.8. Balanced circuit model [1].

The voltage on the Z elements is calculated as:

$$V_i = L_{i1}\frac{di_1}{dt} + L_{i2}\frac{di_2}{dt} + \cdots + L_{ii}\frac{di_i}{dt} + \cdots + L_{in}\frac{di_n}{dt} + R_{i1}i_{i1} + R_{i2}i_{i2} + \cdots + R_{ii}i_i + \cdots + R_{in}i_n \quad (3.14)$$

which becomes

$$V_i = L_{ii}\frac{d}{dt}\left[i_1\frac{L_{i1}}{L_{ii}} + i_2\frac{L_{i2}}{L_{ii}} + \cdots + i_{ii} + \cdots + i_n\frac{L_{in}}{L_{ii}}\right] + R_{ii}\left[i_1\frac{R_{i1}}{R_{ii}} + i_2\frac{R_{i2}}{R_{ii}} + \cdots + i_{ii} + \cdots + i_n\frac{R_{in}}{R_{ii}}\right] \quad (3.15)$$

From equation (3.15), circuit model using controlled current sources is shown in Fig. 3.9.

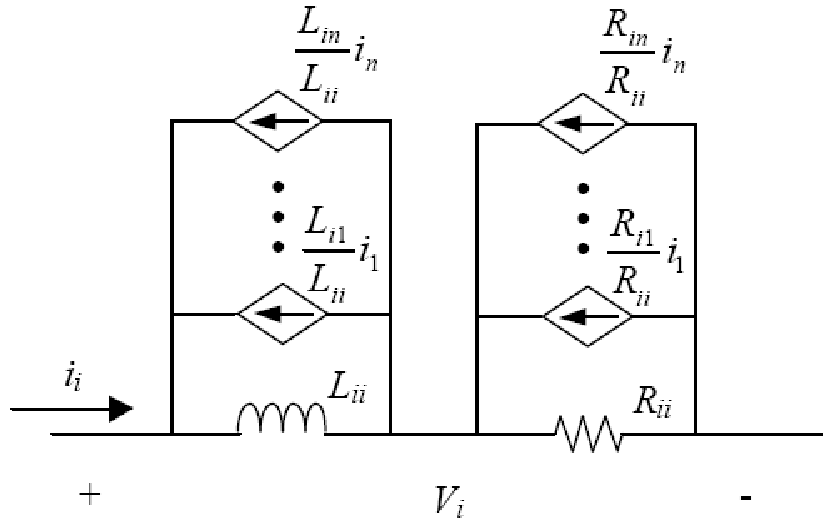


Fig. 3.9. Circuit model using controlled current sources [1].

Ansoft® Q3D extractor can export equivalent circuit for the netlist files into PSpice or Saber. Then simulations can be executed with the extracted parameters. For the parasitic parameters used in the circuit simulation, the mutual inductances are much smaller than the self-inductances, and thus are neglected [6]. The self-drain and self-source inductances are critical values for the switching energy loss discussed in Chapter 2. The self-resistances and self-inductances from Tables 3.3, 3.5, 3.8, and 3.10 are summarized in Tables 3.12 and 3.13.

Table 3.12 Self-resistances of the three series-connected MOSFETs direct-bond module and wire-bonded module

Resistance (mΩ)	Direct-bond module	Wire-bonded module
Q 1 Gate resistance	0.27177	1.9756
Q 2 Gate resistance	0.35064	1.9773
Q 3 Gate resistance	0.28312	1.9760
Q 1 Source resistance	0.048512	0.074087
Q 1– Q2 resistance	0.080212	0.7459
Q 2 – Q3 resistance	0.076432	0.84888
Q3 Drain resistance	0.11901	0.77333

Table 3.13 Self-inductances of the three series-connected MOSFETs direct-bond module and wire-bonded module

Inductance (nH)	Direct-bond module	Wire-bonded module
Q 1 Gate inductance	2.9355	2.7876
Q 2 Gate inductance	3.2692	2.7984
Q 3 Gate inductance	2.9931	2.798
Q 1 Source inductance	1.9332	3.4368
Q 1– Q2 inductance	1.826	3.2977
Q 2 – Q3 inductance	1.1487	2.7038
Q3 Drain inductance	2.2244	2.0809

Based on the above tables, it concludes that the wire-bonded module has a higher self-resistance value than the direct-bond module. For the gate inductance, the wire-bonded module has similar values to the direct-bond module. For the drain and source inductances, the direct-bond module has lower values than the wire-bonded module. The direct-bond module has lower switching energy loss than the wire-bonded module, as shown in Chapter 2.

3.2. Thermal analysis of power module

Thermal energy is transferred in three ways: conduction, convection and radiation. In conduction transfer, thermal energy is transferred through a stationary medium by a vibratory motion of atoms and molecules. In convection transfer, the thermal energy is converted through mass movement around the heat-generating object. In radiation transfer, the thermal energy is

converted into electromagnetic radiation, which can be absorbed by the surrounding environments. For a power electronic packaging module, the conduction and convection are the main means of thermal energy transfer. The most important package design parameters are power dissipation and operation temperature. The maximum silicon device junction temperature for most applications is usually 125 ℃. When selecting packaging materials, the thermal conductivity is the most important design parameter. Thermal conductivity is a measurement of how conductive a material is on transferring thermal energy. The CTE (coefficient of thermal expansion) of a material is a measure of how much the material expands and contracts during heating and cooling. The CTEs of the materials in the packaging are expected to match to reduce the stresses between materials. In short, the design goal is to select of materials with excellent thermal conductivity and CTE closely matched to the power devices. Direct-bond-copper (DBC) is commonly used as a substrate due to its good performance in thermal conductivity and CTE [7].

The effectiveness of which the heat is transferred through a material is measured by the thermal conductivity k. Thermal conductivity is measured in watts per meter per Kelvin (W/mK). The rate of heat transfer is defined in the following equation:

$$q_{conduction} = -kA\frac{\Delta T}{\Delta x} \tag{3.16}$$

where A is the cross-sectional area through which the heat is conducted, and ΔT is the temperature difference between the two surfaces separated by a distance Δx.

Convection uses the motion of fluids to transfer heat. The convection coefficient is the measure of how effectively a fluid transfers heat by convection, and is determined by factors such as the fluid density, viscosity and velocity. It is measured in W/m^2K. The rate of heat transfer from a surface by convection is given by the following equation:

$$q_{convection} = -CA(T - T_a) \tag{3.17}$$

where A is the surface of object, C is convection coefficient, T is the surface temperature, and T_a is the ambient temperature.

Radiative heat transfer occurs when the emitted radiation strikes another body and is absorbed. The amount of radiation emitted by an object is given by the following equation:

$$q_{emitted} = \varepsilon\sigma A T^4 \tag{3.18}$$

where A is the surface area, T is the temperature of the surface, σ is the Stefan-Boltzmann constant ($5.67\times10^{-8} W/m^2K^4$), and ε is the emissivity of material.

In thermal analysis, the boundary condition is to define properties with the convection and radiation of the object in the model. The four types of convection and radiation boundary conditions are basic convection and radiation, forced convection with radiation, free horizontal convection with radiation, and free vertical convection with radiation. The basic convection and radiation are used here. These are evaluated based on the following equation:

$$(-k)\nabla T \cdot n = C(T - T_a) + \varepsilon\sigma(T^4 - T_R^4) \tag{3.19}$$

where n is the surface unit normal, and T_R is the radiation reference temperature. The other symbols are same as equations 3.16 - 3.18.

Ansoft® ePhysics is used to obtain the power MOSFET module temperature under different power loads in simulation. The 3D layout parameters of the power MOSFET module are shown in Table 3.14.

Table 3.14 Layout parameters of power MOSFET module for thermal simulation

	Thickness (mil)	**Size (mil×mil)**
Silicon die	10	160×180
Solder	2	Same as top substance
Copper clip	10	160×210
Copper Spreader	2	140×190
Copper top sink	4	110×130
Copper lead frame	10	200×240
Copper (Top DBC)	8	590×1110
Al_2O_3	25	590×1110
Copper (Bottom DBC)	8	590×1110

The layout for one power MOSFET module is shown in Fig. 3.10.

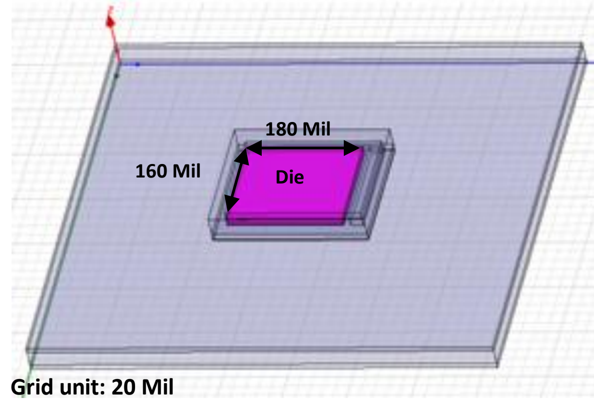


Fig. 3.10. Power MOSFET module 3D layout (dimensions in Table 3.14) in Ansoft® ePhysics.

Then, the layouts of the interconnector and substrate are set with the materials. The materials' thermal conductivity is shown in Table 3.15.

Table 3.15 Power MOSFET module material thermal conductivity

Material	Thermal Conductivity (W/m· K)
Copper	400
Al_2O_3	35
Silicon	148
Solder	48
Air	0.026

Finally, the die is set as the power load and all the surfaces of the devices and DBC substrates are set as the convection and radiation boundary. The convection coefficient is set as 10 W/°cm², the ambient temperature and radiation reference temperature as 30℃, and radiation emissivity as 0.7. The power MOSFET module material thermal conductivity is shown in Table 3.15. The substrate and die layout dimensions are shown in Table 3.1. The temperature models of the double-substrate direct-bond module and single-substrate direct-bond module in Ansoft® ePhsyics are shown in Fig. 3.11 and Fig. 3.12, respectively.

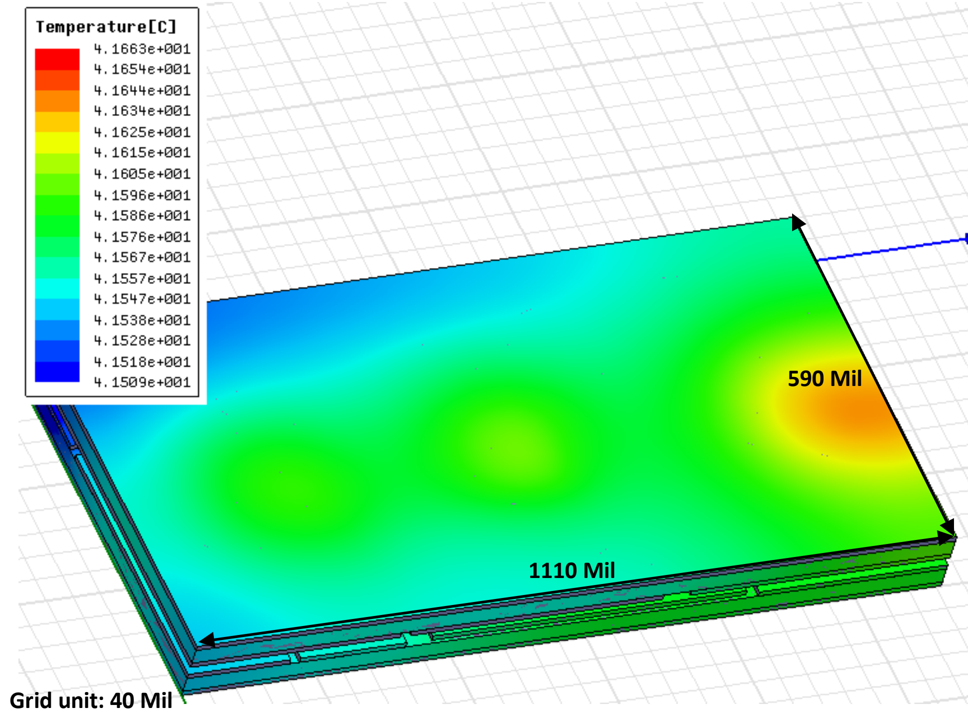


Fig. 3.11. Temperature model of the double-substrate direct-bond module (layout dimensions in Table 3.14) in Ansoft® ePhysics.

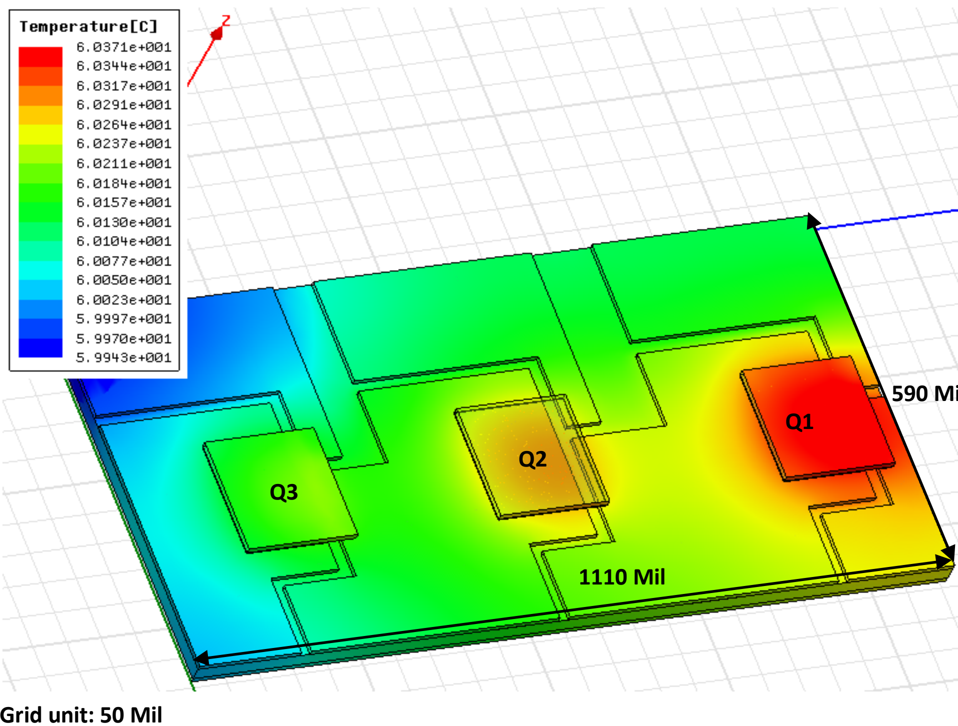


Fig. 3.12. Temperature model of the single-substrate direct-bond module (layout dimensions in Table 3.14) in Ansoft® ePhysics.

The die junction temperatures in the double-substrate direct-bond module and single-substrate direct-bond module under device power losses are shown in Table 3.16. The junction-to-air thermal resistances for the double-substrate module and single substrate module are 33 ℃/W and 82 ℃/W, respectively. The double-substrate direct-bond module has significantly lower thermal resistance than the single-substrate direct-bond module.

Table 3.16 Junction temperatures of the double-substrate direct-bond module and single-substrate direct-bond module under power loss

Power loss on each device	**Junction Temp (℃) in the double-substrate direct-bond module**	**Junction Temp (℃) in the single-substrate direct bond-module**
0.1W	41.737	60.371
0.3W	64.111	113.48
0.5W	84.925	158.28
0.7W	104.44	196.26
1W	131.54	-
1.5W	170.64	-

3.3. Conclusions

This chapter introduces methods for extracting parasitic parameters. The parasitic resistances, inductances and capacitances of the double-substrate direct-bond module and wire-bonded module were obtained using Ansoft® Q3D extractor. The results show that the double-substrate direct-bond module has lower parasitic values than the wire-bonded module. The thermal analysis of double-substrate direct-bond module and single-substrate direct-bond module were simulated in Ansoft® ePhysics. The die-to-air thermal resistances of the double-substrate direct-bond module and single-substrate direct-bond module were found to be 33 ℃/W and 82 ℃/W, respectively. Hence, the double-substrate direct-bond module has lower parasitic impedance and lower thermal resistance than the single-substrate direct-bond module. The double-substrate direct-bond module is assembled in the next chapter.

3.4. References

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[2] *ePhysics Online Help*, Version 2, Ansoft Corporation, Pittsburgh, PA, 2007.

[3] J. Ekman, "Experimental verification of PEEC based electric field simulations," in *proc. IEEE Int. Symposium on Electromagnetic Compatibility*, vol. 1, 2001, pp. 351-355.

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Chapter 4: Power Module with Three Series-connected MOSFETs Assembly

This chapter introduces the materials selection, power MOSFET module packaging procedure, testing and experimental results for the three series-connected power MOSFET module. DualCool^{TM} N-channel NexFET power MOSFETs from Texas Instruments are used as the devices, and direct-bond-copper (DBC) is used as the substrate. A reflow process is used to solder the devices on the substrates. Three modules are assembled, and the breakdown voltages of the modules are tested.

4.1. Selection of materials

MOSFET

A DualCool^{TM} N-channel NexFET power MOSFET from Texas Instruments is used. The DualCool^{TM} package has an SON of 5X6mm, and is optimized for two-sided cooling, and 5 V gate drive, with ultralow Qg and Qgd, and low thermal resistance. A diagram of the top view and bottom view is shown in Fig. 4.1. In the diagram, S denotes the source and D denotes the drain. The product summary of CSD16325Q5C is shown in Table 4.1.

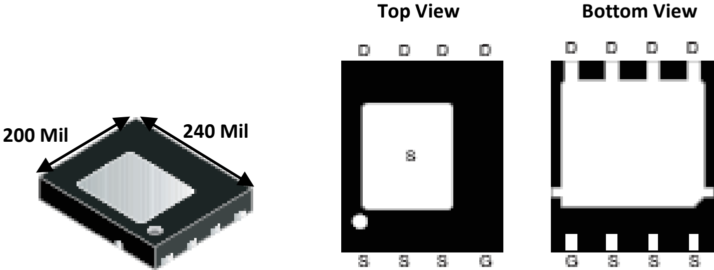


Fig. 4.1. DualCool^{TM} N-channel NexFET power MOSFET diagram.

Table 4.1 Product summary of CSD16325Q5C [1]

<table>
<tr><td>V_{DS}</td><td>Drain-to-source voltage</td><td colspan="2">25</td><td>V</td></tr>
<tr><td>Q_g</td><td>Gate charge total (4.5V)</td><td colspan="2">18</td><td>nC</td></tr>
<tr><td>Q_{gd}</td><td>Gate charge gate-to-drain</td><td colspan="2">3.5</td><td>nC</td></tr>
<tr><td rowspan="3">$R_{DS(on)}$</td><td rowspan="3">Drain-to-source on resistance</td><td>V_{GS}=3 V</td><td>2.1</td><td>mΩ</td></tr>
<tr><td>V_{GS}=4.5 V</td><td>1.7</td><td>mΩ</td></tr>
<tr><td>V_{GS}=8 V</td><td>1.5</td><td>mΩ</td></tr>
<tr><td>$V_{GS(th)}$</td><td>Threshold voltage</td><td colspan="2">1.1</td><td>V</td></tr>
</table>

Substrate

Direct-bond-copper (DBC) is used as the substrate for the interconnection for the devices. DBC has three layers with two copper layers as the outside layers and one layer of electrically insulated sandwich-bonded ceramic as the middle layer. The DBC materials and thicknesses are shown in Fig. 4.2.

Fig. 4.2. Top view and side view of the DBC substrate.

DBC is manufactured at temperatures as high as 1070 ℃ in an inert atmosphere. The copper oxides forms a eutectic melt that wets and cools to form a strong bond between the copper and the ceramic. There is no solder or any other bonding materials between the copper and the ceramic surface. The ceramic used as the insulating materials include Al_2O_3, AlN, Si_3N_4 and BeO [2]. Aluminum oxide was used here because it is easily available in the marketplace and in the lab.

DBC offers many advantages for power electronics packaging: The copper and ceramic bonded together have a coefficient of thermal expansion (CTE), that is much lower than the copper and

close to that of the ceramic. Thus a large-area chip can be soldered onto the copper layer without risking stress damage. The copper is a high-purity, oxygen-free-high-conductivity (OFHC) type. The copper traces can have very low resistance that handles large current of more than 100 A. The thick layer of the copper pad is effective for spreading heat throughout the power device.

Solder material

The top and bottom layers of the DBC were made with interconnection patterns to connect the devices. The layers also work as heat spreaders and electrical shields. The external expensive heat sink can be eliminated.

A precision reflow machine was used to solder the device onto the substrate. Low temperature solder was used because it is easy to reflow, and the low temperature needed eliminates the risk of overheating the devices during the soldering. An SnPb eutectic solder paste was used here. The specifications are in Table 4.2 as follows [3].

Table 4.2 Specifications of the SnPb eutectic solder paste

Alloy	SN63/PB37
Melting point	183°C
Particle size	Type 3 per J-STD-006
Power shape	Sphere
Halide content	9.5±0.5wt%
Viscosity	200-500ppm
Flux type	Resin flux ROLO J-STD-004

For handling and storage, solder paste should be stored at 0-10 ℃. The shelf life is six months from the production date, and the paste should be kept out of direct sunlight.

4.2. Design, fabrication of substrate and assembly

AutoCAD is used for the layout of the substrate. The layout of top substrate interconnection pads and the pad positions in the circuit schematic are shown in Fig. 4.3. The layout of bottom substrate interconnection pads and the pad positions in the circuit schematic are shown in Fig. 4.4. The opposite side of the connecting substrate is a plane copper without a pattern, as shown in Fig. 4.5. The brown color denotes copper and white color denotes exposed ceramic. For testing breakdown voltage, the MOSFET gate and source terminals should be shorted together. So P2 and P4, P5 and P7, and P8 and P10 were shorted together in the assembly process.

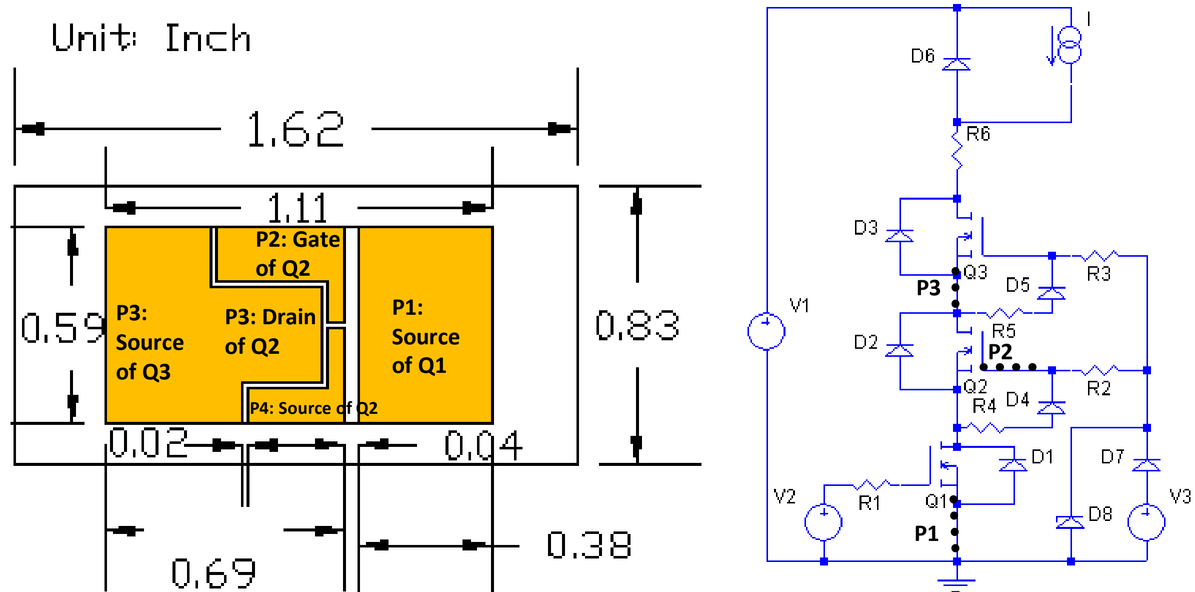


Fig. 4.3. Layout of top substrate pads (left) and pad positions in circuit schematic (right).

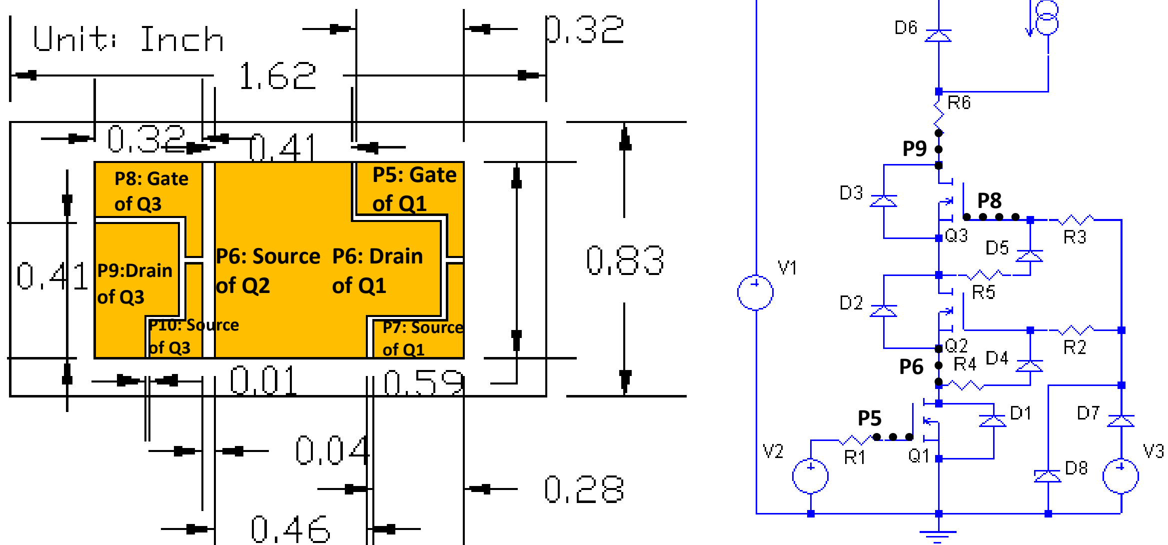


Fig. 4.4. Layout of bottom substrate pads (left) and pad positions in circuit schematic (right).

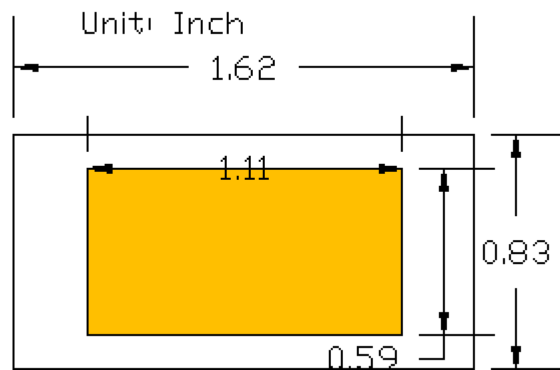


Fig. 4.5. Layout of opposite side of substrate pads.

Kapton® tape is used to transfer the AutoCAD layout to the DBC substrate. The Kapton tape used was 2.5 mils thick polyimide Kapton®. Kapton® has high temperature processing capabilities. A soft rubber roller was used to apply Kapton® tape to the DBC panel and to press and push the tape evenly and avoid air bubbles between the tape and the DBC.

Then a laser cutting machine is used to cut the pattern on the Kapton® tape. The laser cutting machine used is made by Resonetics Micormaching Technology, Nashua, NH, USA, and is shown in Fig. 4.6.

Fig. 4.6. Laser cutting machine.

For cutting the tape, the process parameters, pulse spacing, laser power and pulse number were set as 0.002 inch, 5 W and 10, respectively, to ensure high-dimension resolution. The DBC panel was attached to the work station using double-sided tape to prevent the panel moving. Then laser cutting was performed on the Kapton® tape for the layout pattern. After laser cutting, the DBC substrates are shown in Figure 4.7. Then the unnecessary parts were removed**.** The DBC substrates after being stripped of the tape are shown in Figure 4.8.

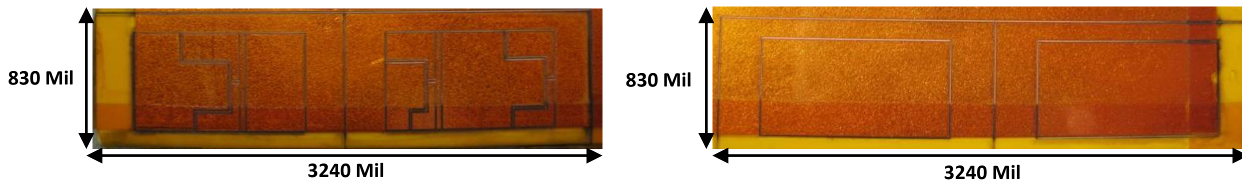


Fig. 4.7. DBC substrates after laser cutting on tape: substrate pads (left) and opposite of substrate pads (right).

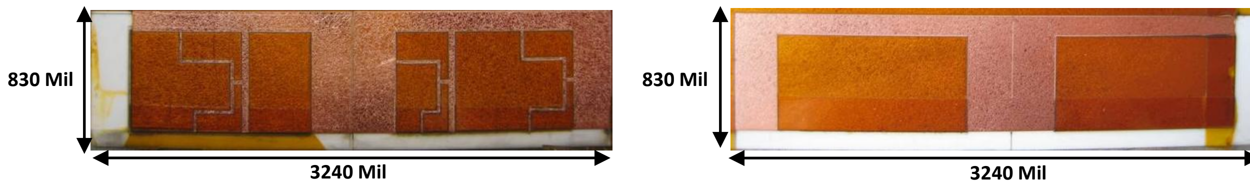


Fig.4.8. BDC substrates after being stripped of tape: substrate pads (left) and opposite of substrate pads (right).

The exposed copper was then etched away. The etching machine is a BTD-201B, bench-top developer made by Kepro Circuit Systems Inc, Fenton, MO, USA. The etching solution is ferric chloride ($FeCl_3$). The BTD-201B is shown in Fig. 4.9.

Fig. 4.9. Kepro BTD-201B etching machine.

The DBC panel was put in the machine and solution was pressure-sprayed onto the DBC panel. The unmasked copper was etched away by chemical reaction. It takes about one hour for etching copper with thickness of 8 mil. When the etching is finished, the DBC panel was rinsed in the water to remove the etching solution residue. Then a laser cutting process was used to cut the DBC panel as the substrate. The laser pulse spacing was 0.0006 inch. The laser power was 38 W, and the power number was 300. The DBC panel was attached to the work station using double-sided tape to prevent the panel moving. The DBC substrates after etching and cutting are shown in Fig. 4.10.

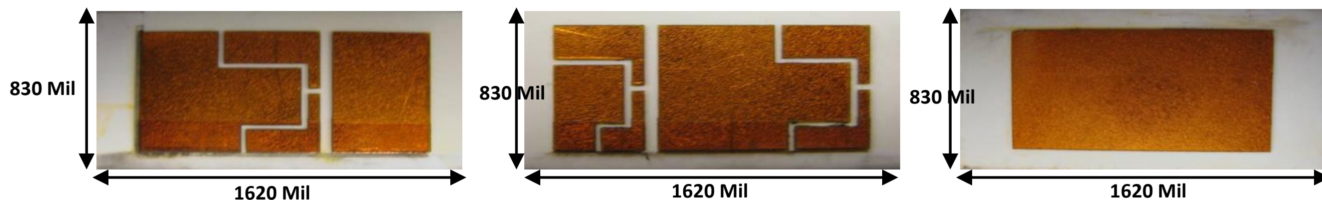
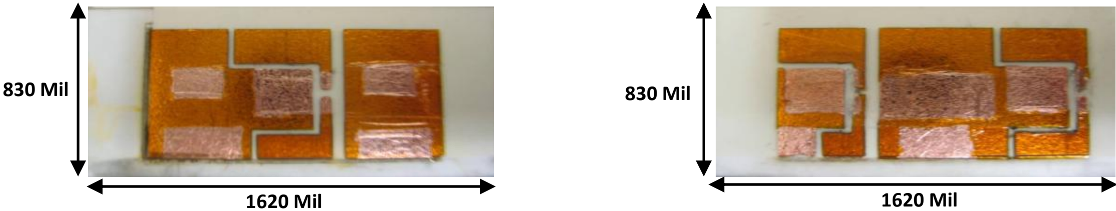


Fig. 4.10. DBC substrates after etching and laser cutting: top substrate pads (left), bottom substrate pads (center) and opposite of substrate pads (right).

The Kapton® tape on the DBC panel was cut for the solder paste area to prevent the solder from overflowing onto the substrate. The DBC substrates after cutting the solder paste areas are shown in Figure 4.11.



4.11. DBC substrates after cutting solder paste areas: top substrate pads (left) and bottom substrate pads (right).

The solder paste was printed on the exposed copper area. To easily solder the two substrates together, the MOSFETs are soldered on the substrates separately. For testing, the copper foil needs to be soldered on the edge of the DBC substrate. The reflow process was used for the soldering. The goal of the reflow process is to heat the substrate, and to melt the solder without overheating and damaging the devices. The reflow process consists of four zones: pre-heat zone, pre-reflow zone, reflow zone and cool-down zone. The reflow profile is shown in Fig. 4.12 [3]. A Sikama conduction belt oven was used in this process, as shown in Fig. 4.13. The belt speed was set as 6 inch/min.

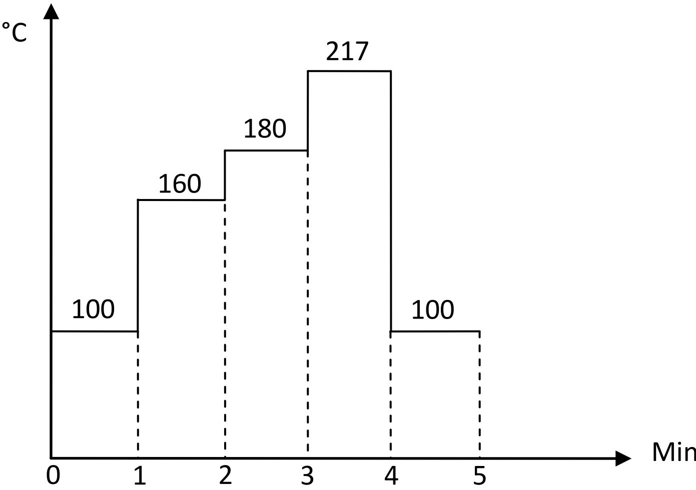


Fig.4.12. Reflow profile for soldering MOSFET.

Fig. 4.13. Sikama conduction belt oven.

After reflow, the MOSFETs and testing foil were soldered onto the DBC panel, as shown in Fig. 4.14.

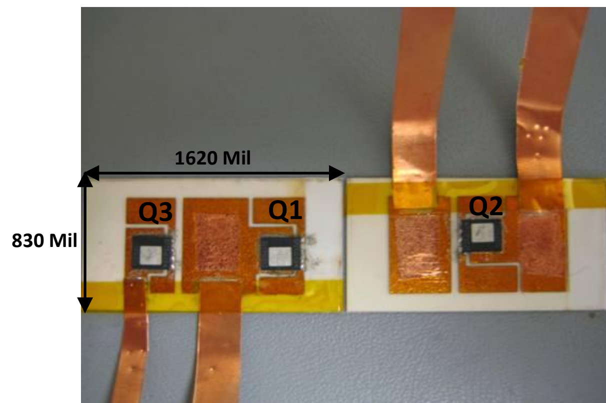


Fig. 4.14. MOSFETs with the copper foils soldered on the DBC substrates.

Finally, the two DBC substrates with the MOSFETs were soldered together by a second reflow. The solder paste and reflow profile used are the same as the first process. In order to keep the devices fixed on the substrate, Kapton® tape was used to hold these two substrates together, as

shown in Fig. 4.15. Otherwise, the devices would move around during the reflow process. Three samples were assembled, as shown in Fig. 4.16.

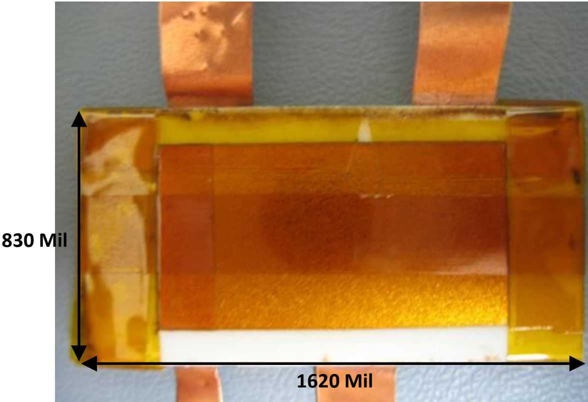


Fig. 4.15. Three series-connected MOSFETs sandwiched between two DBC substrates.

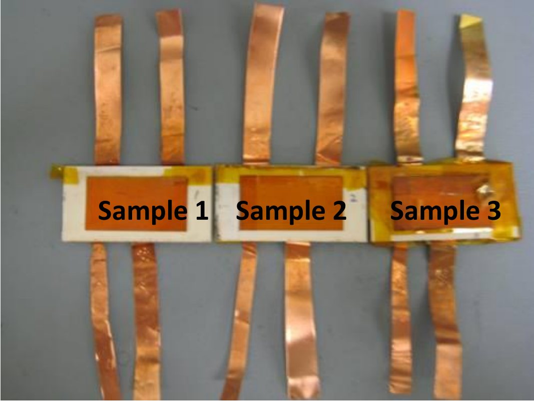


Fig. 4.16. Three samples of three series-connected MOSFETs module.

4.3. Electrical characterization

A Tektronic 371 high-power curve tracer was used to test of the breakdown voltage of the power modules, as shown in Fig. 4.17 (left). The testing circuit schematic is shown in Fig. 4.17 (right).

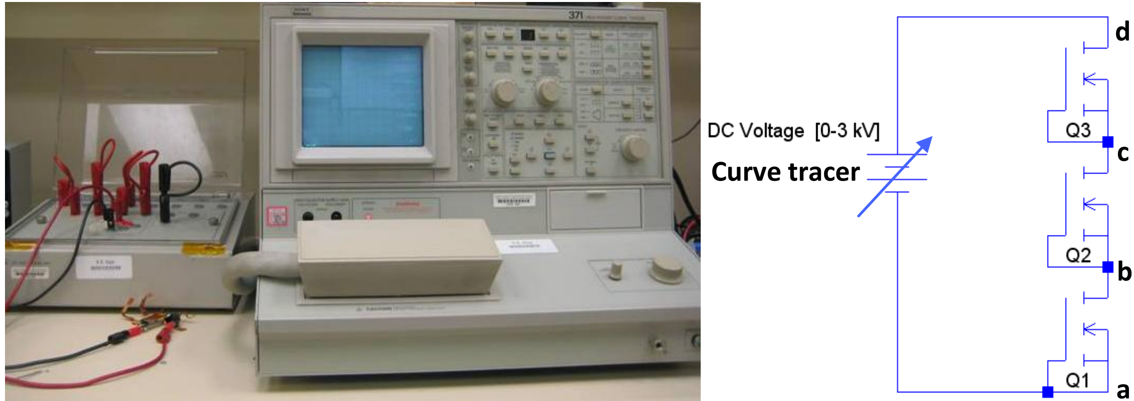


Fig. 4.17. Tektronic 371 high-power curve tracer (left) and schematic of three series-connected MOSFETs breakdown voltage testing circuit (right).

For testing the modules' breakdown voltage, the MOSFET gate and source terminals were shorted together in the solder reflow process. Three series-connected MOSFETs module and breakdown voltage testing setup using curve tracer are shown in Fig. 4.18. Referring to Fig. 4.17 (right), label "a" denotes source of Q1, label "b" denotes source of Q2, label "c" denotes source of Q3, and label "d" denotes drain of Q3. The curve tracer is set as high voltage with 3 kV and peak power with 3 W. In the measurement, the collector supply voltage was increased from 0 V gradually. And the breakdown voltage was obtained as the drain-source current at 250 μA [1, 4].

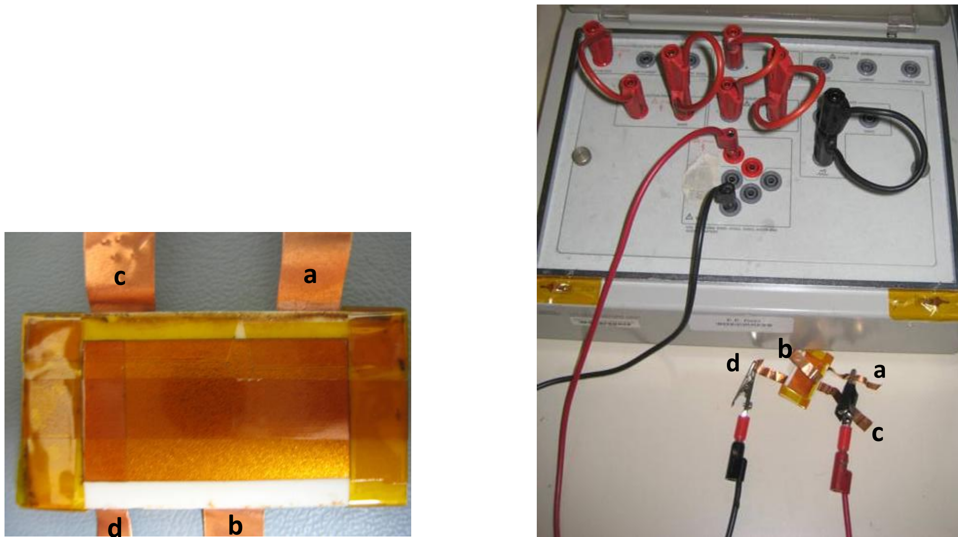


Fig. 4.18. Three series-connected MOSFETs module (left) and breakdown voltage testing setup using curve tracer (right).

Breakdown voltages were measured for one MOSFET, two series-connected MOSFETs of Sample 1 and three series-connected MOSFETs of Sample 1, 2 and 3. The results are shown in Fig. 4.19 – 4.23.

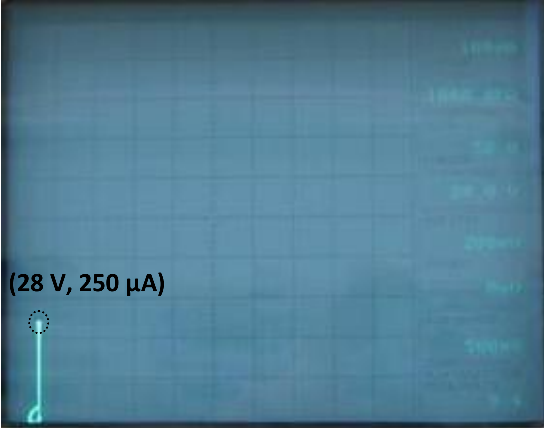


Fig. 4.19. One MOSFET (testing between “a” and “b”) of Sample 1 with 28 V breakdown voltage.

Fig. 4.20. Two series-connected MOSFETs (testing between “a” and “c”) of Sample 1 with 55 V breakdown voltage.

Fig. 4.21. Three series-connected MOSFETs (testing between "a" and "d") with 76 V breakdown voltage Sample 1.

Fig. 4.22. Three series-connected MOSFETs (testing between "a" and "d") with 82 V breakdown voltage Sample 2.

Fig. 4.23. Three series-connected MOSFETs (testing between “a” and “d”) with 72 V breakdown voltage Sample 3.

The measurement results of individual MOSFET breakdown voltage and three series-connected MOSFETs breakdown voltage are shown in Table 4.3. The summations of individual MOSFET breakdown voltage are shown in Table 4.3, also. The summations of individual MOSFET breakdown voltage are closed to the measurement results of series-connected MOSFETs breakdown voltage.

Table 4.3 MOSFET breakdown voltage measurement results of the three samples using high-power curve tracer

Breakdown voltage (V)	Sample 1	Sample 2	Sample 3
Measurement of Q1	28	28	28
Measurement of Q2	28	28	28
Measurement of Q3	21	28	17
Summation of Q1, Q2, Q3	77	84	73
Measurement of Q1-Q3	76	82	72

The second testing method using digital voltmeter (DVM) was measured by series connecting a resistor (333 kΩ, 0.25 W) to the MOSFETs module. The testing circuit schematic is shown as Fig. 4.24. With drain-source current of 250 μA, the voltage drop at the resistor is 83.3 V. By adding resistor voltage with three 25 V MOSFET breakdown voltage, the total voltage is 158.3 V. The rating of voltage supply should at least beyond this value. The power supply used is the Sorensen DCR 600-4.5B with the maximum 800 V output voltage, as shown in Fig. 4.25. The

digital voltage and current meter used is the Tektronix DMM 4020 5-1/2 digital multimeter, as shown in Fig. 4.26. The testing circuit setup is shown in Fig. 4.27. Referring to Fig. 4.24, label “a” denotes source of Q1, label “b” denotes source of Q2, label “c” denotes source of Q3, and label “d” denotes drain of Q3.

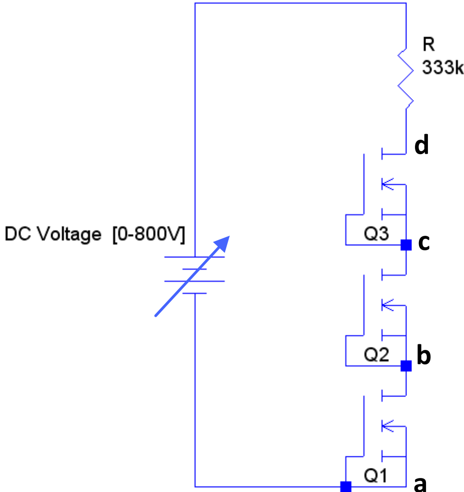


Fig. 4.24. Schematic of three series-connected MOSFETs breakdown voltage testing circuit.

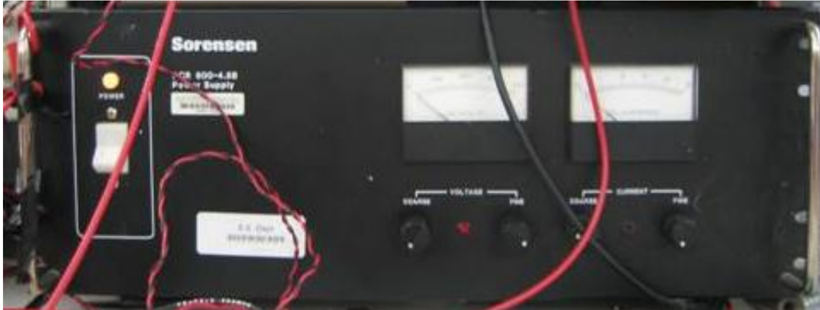


Fig. 4.25. Sorensen DCR 600-4.5B power supply.

Fig. 4.26. Tektronix DMM 4020 5-1/2 digital multimeter.

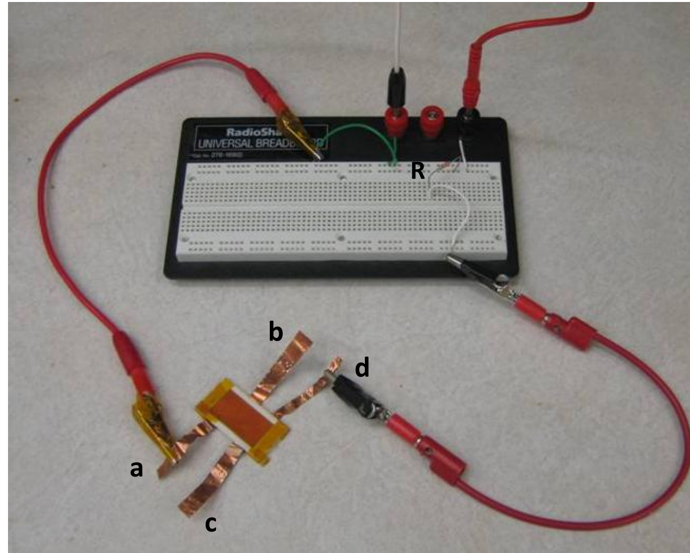


Fig. 4.27. Three series-connected MOSFETs breakdown voltage testing circuit setup using digital voltmeter (DVM).

In the measurement, the power supply voltage was increased from 0 V gradually, and the breakdown voltage was obtained with the drain-source current at 250 μA [1, 4]. The measurement results of one MOSFET breakdown voltage and three series-connected MOSFETs breakdown voltage are shown in Table 4.4. The summations of individual MOSFET breakdown voltage are shown in Table 4.4, also. The summations of individual MOSFET are closed to the measurement results of series-connected MOSFETs. Compared with the results using high-power curve tracer, this method is more accurate, as well as being easier to set up.

Table 4.4 MOSFET breakdown voltage measurement results of the three samples using digital voltmeter (DVM)

Breakdown voltage (V)	Sample 1	Sample 2	Sample 3
Measurement of Q1	27.54	27.42	27.16
Measurement of Q2	27.42	27.48	27.40
Measurement of Q3	22.88	27.49	18.94
Summation of Q1, Q2, Q3	77.84	82.39	73.50
Measurement of Q1-Q3	77.51	82.31	73.06

4.4. Conclusions

This chapter introduces the assembly process of the three series-connected power MOSFETs module. The TI DualCool^{TM} N-channel NexFET power MOSFET was chosen as the device. DBC was used as the substrate, and Kapton® tape was used as the mask for the pad etching. Three samples were assembled by laser cutting, etching, and solder reflow. Testing with a high-power curve tracer, the breakdown voltages were found to be 76 V, 82 V, and 72 V. The breakdown voltages found by using digital voltmeter (DVM) were 77.51 V, 82.31 V, and 73.06 V. The next chapter will summaries this research and introduces possible future work.

4.5. References

[1] *CSD16325Q5C data sheet*, Texas Instruments, 2010.

[2] *GMBH, Direct Copper Bonded Substrates for Semiconductor Power Devices*, Curamik Electronics, Tech. Rep., 1997.

[3] *SnPb eutectic solder paste datasheet,* Manncorp Inc., Available: http://www.smtsolderpaste.com

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Chapter 5: Conclusions and Future Works

This research introduces series-connected power MOSFETs modules to improve breakdown voltage. A novel switch topology of three series-connected MOSFETs is proposed, and the series-connected three IRF7832 MOSFETs (30V breakdown voltage) are simulated in a chopper circuit and the switching behaviors are studied. The drain-source voltage sharing in switching off-mode shows that the MOSFETs can share voltage within their breakdown ranges. Based on the simulations, the switching energy losses without parasitic inductance and with 5 nH parasitic inductances are 203.38 μJ and 316.49 μJ, respectively. The critical parasitic inductance is identified as the interconnector of Q2 and Q3, which is about 44.4% of the total energy loss. The packaging parasitic impedances of a direct-bond module and a wire-bonded module are studied using Ansoft® Q3D extractor. The results show that the direct-bond module can provide lower parasitic impedances. The switching energy losses of the direct-bond module and the wire-bonded module are 296.18 μJ and 238.99 μJ, respectively, that shows that the direct-bond module has the lower switching energy loss than the wire-bonded module. The thermal management of a double-substrate direct-bond module and a single-substrate direct-bond module is studied using Ansoft® ePhysics. Based on thermal simulations, the MOSFET junction-to-air thermal resistances of the double-substrate direct-bond module and the single-substrate wire-bonded module are 33°C/W and 82°C/W, respectively. The double-substrate direct-bond module provides significantly lower thermal resistance than the single-substrate direct-bond module.

The three series-connected power MOSFETs module are assembled and the breakdown voltages are measured. Three series-connected TI DualCool^{TM} Power MOSFETs (25 V breakdown voltage) are sandwiched in the double DBC substrates by flip-chip technology. By using high-power curve tracer, the breakdown voltages of the three samples are found to be 76 V, 82 V, and 72 V. The breakdown voltages of the three samples found by using digital voltmeter (DVM) are 77.51 V, 82.31 V, and 73.06 V. The series-connected MOSFETs module shows improved breakdown voltage.

For future work, a driver circuit needs to be built in the power module and tested. The performance of the power module should be studied in terms of voltage sharing, switching

behavior and energy loss. The series-connected multiple devices switching characteristics can be compared with one device switch. And series-connected high-voltage MOSFETs and IGBTs can be studied. The applications of voltage sharing switch need to be specified and tested.