4 CONCLUSIONS

The most important space vector modulation schemes were analyzed for a three-leg and a four-leg voltage source inverters. The analysis was performed over the complete range of modulation index, and for both balanced and and unbalanced load conditions in the case of the four-leg inverter. Two types of unbalance were considered, namely the load power unbalance and load power factor unbalance. The results of the analysis are summarized below.

1. There is always a trade off to be observed between the total harmonic distortion and switching loss. This could be translated as a trade off between the size of the heat sink and of the filter used, although sometimes the choice could be affected by the other factors.

2. The performance of the four-leg converter with respect to both switching loss and THD is found to deteriorate with unbalance. The design of the filter inductor must be done for the worst case unbalance situation to avoid problems like saturation and excessive heating.

3. The performance of three-leg and four-leg voltage source inverters with respect to various modulation schemes is found to be similar. However, the THD of a four leg inverter is higher compared to a three leg inverter, assuming both are operating under identical conditions. This is because the phase voltage at the output of the inverter is pulsed rectangular in the case of a four-leg inverter, whereas in a three-leg inverter the equivalent phase voltage waveform is stepped.

4. The scheme with symmetric switching (SVM2 - three leg & Scheme1 - four leg) is recommended at low switching frequencies because switching losses then become

insignificant. Since this scheme requires larger number of switching states it is usually associated with larger programmable logic device needed for the digital modulator implementation.

5. The scheme where the highest current is not switched (SVM4 - three leg & Scheme2 - four leg) is recommended at high switching frequencies, especially at high load power factors. This is the only scheme where the choice of switching state vectors is dependent on load. This is usually associated with additional coding inside the digital signal processor (DSP) and is practical only when currents are sensed anyway for other reasons.

6. The scheme with the minimum number of switchings (SVM3 - three-leg & Scheme3 - four-leg) is recommended for high switching frequencies and low load power factors. Since this scheme is associated with minimum number of switching state vectors it usually requires minimum logic device space occupation and lesser coding inside the processor compared to the other schemes, but it results in high THD and high current ripple.

Scope for further work

Analysis performed assumed ideal elements. Performing a similar analysis using real elements would be useful. Formal proofs and derivations of all the concepts developed would be challenging. Also the analysis of unbalance based on sequence components (negative and zero) would be interesting.