INSULATED GATE TRANSISTORS. CHARACTERISTICS AND APPLICATION TO MOTOR CONTROL.

by

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(ABSTRACT)

A detailed study of a MOS-Bipolar power semiconductor known as the IGT or COMFET or GEMFET was undertaken. The major disadvantage of the device was identified as latching and the effect of various factors affecting latching were determined. The experiments performed determined susceptibility to latch under various conditions of temperature, rate of rise of gate-source voltage and rate of fall of drain-source voltage.

A 340V, 10A three phase GEMFET bridge inverter using a pulse width modulation scheme to drive a permanent magnet brushless dc motor was sucessfully fabricated. The simplicity of the gate drive circuit and the low cost of the device make the IGT ideal for motor drive applications.

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TABLE OF CONTENTS

TABLE OF CONTENTS (CONT'D)

LIST OF FIGURES

LIST OF FIGURES (CONT'D)

LIST OF FIGURES (CONT'D)

LIST OF FIGURES (CONT'D)

LIST OF TABLES

CHAPTER I.

INTRODUCTION.

The Insulated Gate Transistor (IGT) is a new power switching semiconductor device which was invented in late 1982 [1]. This four layered, three terminal, normally off device is a hybrid between a bipolar junction transistor and a power MOSFET. The input current requirement of the Insulated Gate Transistor, like that of a conventional FET device, is small. The output characteristics of the IGT resemble a bipolar device, where minority carriers as well as majority carriers are used to keep the device conduction resistance low. From a user's point of view, this means that the drive requirements of the Insulated Gate Transistor are very simple while the conduction voltage drop of the device is low.

The new power device is now being manufactured by various leading semiconductor companies, each of whom refer to the device by a different name and circuit symbol. The names are:

1) INSULATED GATE TRANSISTOR (IGT) by GENERAL ELECTRIC [2].

2) CONDUCTIVITY MODULATED FIELD EFFECT TRANSISTOR (COMFET) by RCA [3]. and

3) GAIN ENHANCED MOSFET (GEMFET) by MOTOROLA [4].

The various circuit symbols used to represent the device are shown in Figure 1.1. Figure 1.1.a. shows the circuit symbol of an IGT. while Figures 1.1.b. and 1.1.c. show the symbols for a COMFET and a GEMFET respectively.

In this thesis, the name IGT will be used to describe the entire class of these devices and the circuit symbol of Figure 1.1.a will be used in circuit diagrams. The MOSFET terminology (drain, gate and source) will be used to describe the three equivalent terminals on the IGT.

The IGT is similar in structure to a power MOSFET and the technology used in its manufacture is an offshoot of VLSI fabrication. Thousands of IGT cells arranged in a simple geometrical pattern comprise one IGT chip. The processes used in the manufacture of the IGT are also similar to that of a power MOSFET. The starting material for the IGT, however is a p^+ doped silicon wafer instead of the n^+ wafer used for power MOSFETs. Similarities in structure also translate to roughly equal costs in the manufacture of a power IGT and a MOSFET of the same die size.

Power IGTs rated 500 V and 30 A are currently being commercially manufactured. Devices with voltage ratings of over one kV and current ratings up to 100 A are

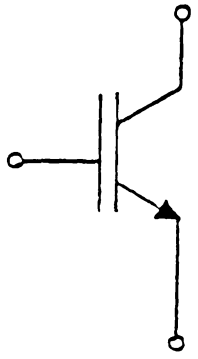


Fig. 1.1.a.

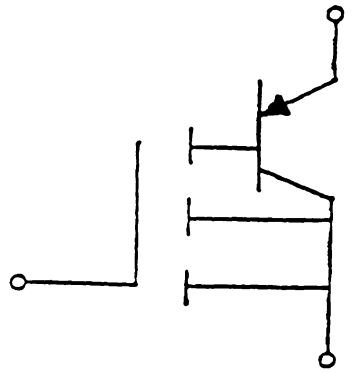


Fig. 1.1.b.

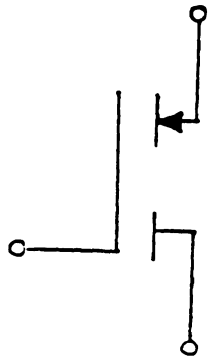


Fig. 1.1.c.

Figure 1.1: The various circuit symbols used for Insulated Gate Transistors.

likely to be available in the future.

This thesis is divided into six chapters. The first two chapters consist of a compilation and evaluation of published results. The next three chapters describe the studies made to evaluate the device. Chapter II discusses the structure and equivalent circuit of the device and describes its operation in detail. Experiments performed to illustrate the operation of the IGT are also discussed. A comparison with the conventional power MOSFET is also given in Chapter II. Chapter III describes the experiments performed to learn the properties of the IGT. Device latching was identified as the most serious disadvantage of this device. The experiments performed examined the effects of device temperature, rate of fall of gate-source voltage and rate of rise of drain-source voltage on the susceptibility of the IGT to latch. Experiments were performed on RCA COMFETs and GE IGTs and the effect of a combination of these factors on the latching current levels was determined. The results of a study of latching during the paralleling of Insulated Gate Transistors is also given in Chapter III. Chapters IV and V provide an in-depth discussion of an important application of this device, namely its use in a three phase bridge inverter controlling a permanent magnet brushless d.c. motor. Chapter IV

describes the gate drive circuit while Chapter V discusses the power circuit. The use of IGT inverters for the PWM control of d.c. motors is discussed. A conclusion giving an overall assessment of the device and suggesting some areas of future development in this field can be found in Chapter VI.

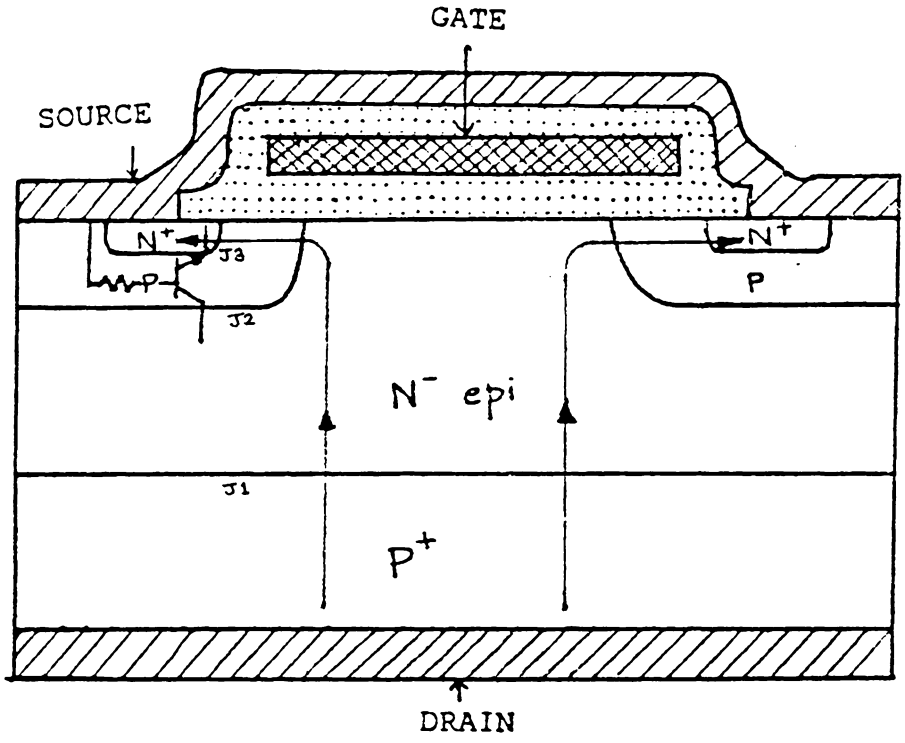
CHAPTER II.

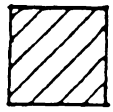
OPERATING PRINCIPLE OF INSULATED GATE TRANSISTORS.

The IGT, being a relatively new device, is still not very well known to many power electronics engineers. This chapter discusses the operating principles of the IGT. Section 2.1 discusses the device structure of the IGT. The operation of the device in the various modes of switching is explained in detail in Section 2.2. A comparison of the IGT with the power MOSFET is given in Section 2.3.

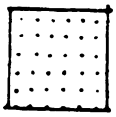
2.1. IGT STRUCTURE AND EQUIVALENT CIRCUIT

The simplified structure of the IGT presented in Figure 2.1 shows it to be very similar to that of a conventional power MOSFET. The one major difference is that the n^+ substrate has been replaced by a p^+ doped substrate. In the forward blocking mode (drain-source voltage being positive and no gate-source voltage impressed.), the junction J2 provides the voltage blocking capability. In the reverse blocking mode, junctions J3 and J1 are reverse biased with the junction J1 providing most of the voltage blocking capability.

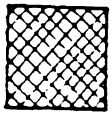




METAL (ALUMINUM)



DIELECTRIC (SiO_2)



POLYSILICON

Figure 2.1: Simplified cross-section of an IGT.

A better insight into the structure of the IGT is provided by the equivalent circuit shown in Figure 2.2. The p-n-p transistor and the parasitic n-p-n transistor are positioned back-to-back in a positive feedback configuration, similar to an SCR device. However the SCR action is deliberately suppressed in the device design to avoid loss of gate control. In other words it is a parasitic effect which is not used for normal current conduction. It is well known in SCR physics that when the sum of the current gain alpha parameters of the two transistors equals one, the parasitic SCR latches. Therefore in the device design, the alpha of the n-p-n transistor is kept deliberately low under all operating conditions. This is accomplished by overlapping source metalization which introduces the bulk distribution resistance R_S in the emitter.

2.2. DEVICE OPERATION.

Consider the cross-sectional structure of the device as shown in Figure 2.1. The operation of the IGT may be explained, with the help of Figure 2.1, by considering each of the following five cases:

1) The device in its forward blocking state.

2) The device in its forward conducting state.

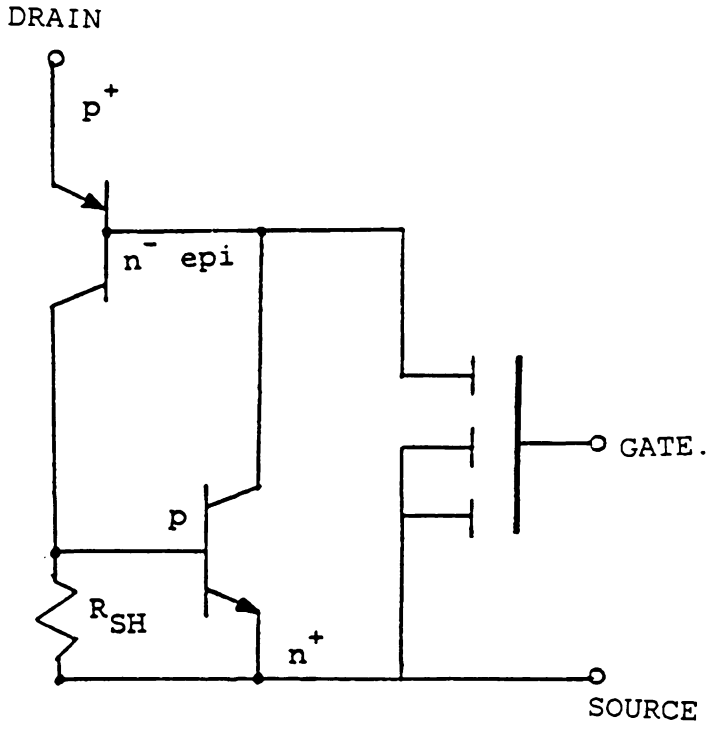


Figure 2.2: The transistor equivalent circuit of the Insulated Gate Transistor of Figure 2.1.

3) The device in its reverse blocking state.

4) The device during turn-on.

5) The device during turn-off.

2.2.1. THE IGT IN ITS FORWARD BLOCKING MODE.

When the gate source voltage is below the threshold voltage and the drain voltage of the IGT is positive with respect to the source, the device is said to be in its forward blocking mode. Only a small forward leakage current flows through the device. The junction J2 between the n^- epitaxial region and the p^+ doped base region is reverse biased. A potential barrier is formed in the junction. The current flow is prevented, similar to a reverse biased diode.

Figure 2.3 gives a typical doping density profile of an IGT [3]. The doping density and thickness of the n^--p^+ regions determine the device voltage blocking capability. The device design is similar to that of a conventional MOSFET n^--p^+ junction. The n^- region is lightly doped and has a thickness large enough to support the depletion region when the device is in the forward blocking mode.

The space charge region is almost entirely in the n^- epi region and, therefore, the epitaxial layer supports high

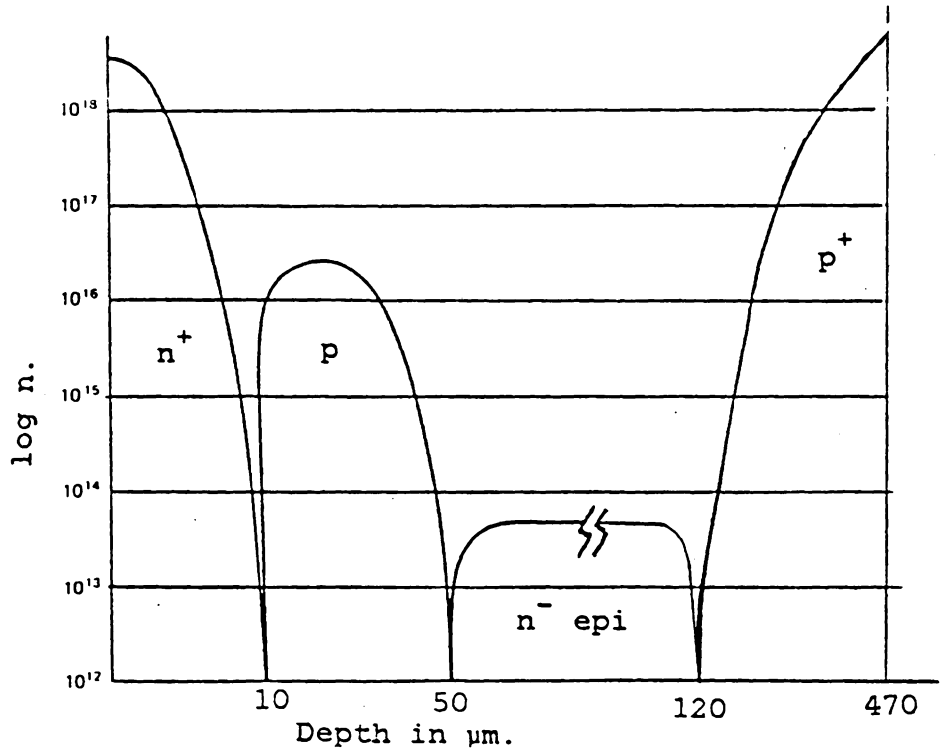


Figure 2.3: A typical doping profile of a 400V IGT.

voltages. The n^- epitaxial layer has, typically, a doping density of around 10^{14} atoms/cm^3 for a 450 V IGT. The value of the leakage currents flowing under full voltage conditions for a 450 V device will typically be less than 1 mA at room temperature. This is approximately equal to that of a power MOSFET of the same voltage rating. As the temperature of the device is increased to 100°C, the leakage current may increase to ten times its value at room temperature.

The resistance of the n^- region mentioned above is the cause of the high voltage on resistance of the conventional power MOSFET. But in the IGT, conductivity modulation of the n^- region will reduce the conduction as, explained in the next section.

2.2.2. THE DEVICE IN ITS FORWARD CONDUCTION STATE.

When the MOS gate of the device is given a positive bias with respect to the source and the drain is positive with respect to the source, then the device is in its on-state. The forward gate-source voltage inverts the p doped base region immediately below the oxide layer. The device behaves like a p-i-n diode with the junction J1 between the p^+ doped drain region and the n^- epi region being forward

biased. The highly resistive n^- region is heavily conductivity modulated by injected holes and this causes a low conduction drop. This is the reason for the very high current densities that the IGT can sustain without causing a large voltage drop.

The conduction voltage of the device mainly comprises the forward bias voltage of the junction J1 and the voltage drop due to the ohmic resistance of the epitaxial layer, the channel resistance and the metallization resistance. The ohmic resistance of the inverted p-base depends on the doping density of the p region, the thickness of the oxide layer and the gate voltage necessary for strong inversion. The highly resistive n^- epitaxial region contributes little to the total drop because of conductivity modulation, as explained earlier. Compared to a power MOSFET, this is the most significant factor, especially at high voltages. Figure 2.4 shows the relative chip areas of an RCA COMFET and an IRF conventional MOSFET of approximately the same rating. It can be seen that the conventional FET occupies a much larger area.

We may explain the conduction voltage of the IGT with the help of the transistor equivalent circuit as shown in Figure 2.2.

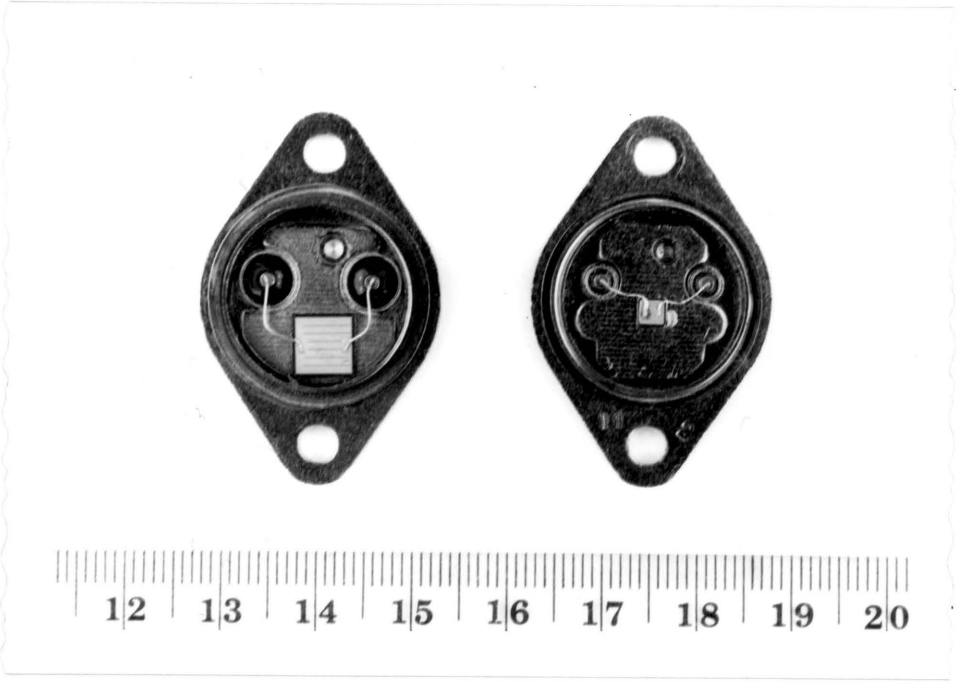


Figure 2.4: Photograph showing the chip areas of an IGT (TA9437B) and a power MOSFET (IRF 352) of ratings 400V and 10A.

The voltage of the IGT in its conduction state, is the sum of the forward bias voltage of the junction J1 and the on-state saturation voltage of the parasitic n-p-n transistor. The thickness of the epitaxial region in the IGT is approximately the same as that of a power MOSFET of similar voltage rating. The conduction voltage of the epitaxial layer is less than that of a comparable MOSFET because the injection of minority carriers into the epitaxial layer results in a high conductivity modulation region.

Figures 2.5.a. and 2.5.b. show the static characteristics of an RCA TA9437A COMFET. The oscillograph shows that the output characteristics of an IGT are rather similar to that of a conventional power MOSFET. The IGT will be in its forward state only when the drain voltage of the device exceeds the source voltage by the forward voltage drop of junction J1. This results in a shift of the output characteristic curves of the IGT to the right by a voltage of approximately 0.7 V. This can be clearly seen in Figure 2.5.b. Thus the conduction voltage of the IGT is approximately an order of magnitude less than the present day power MOSFETs and is about equal to that of a power bipolar transistor.

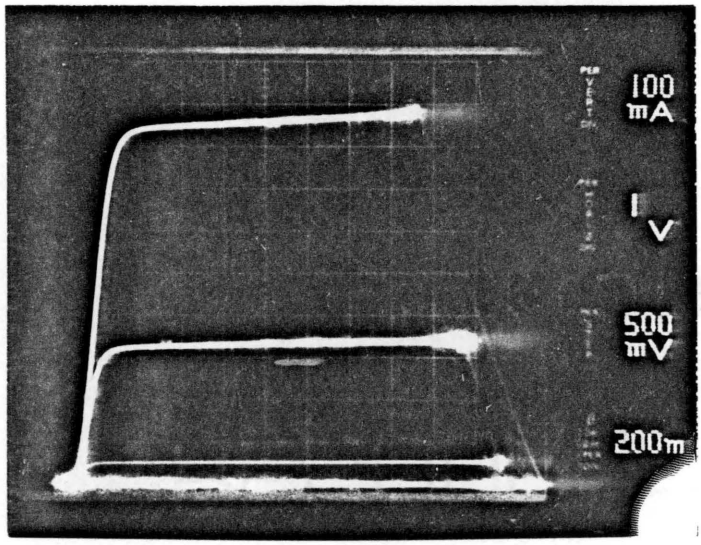
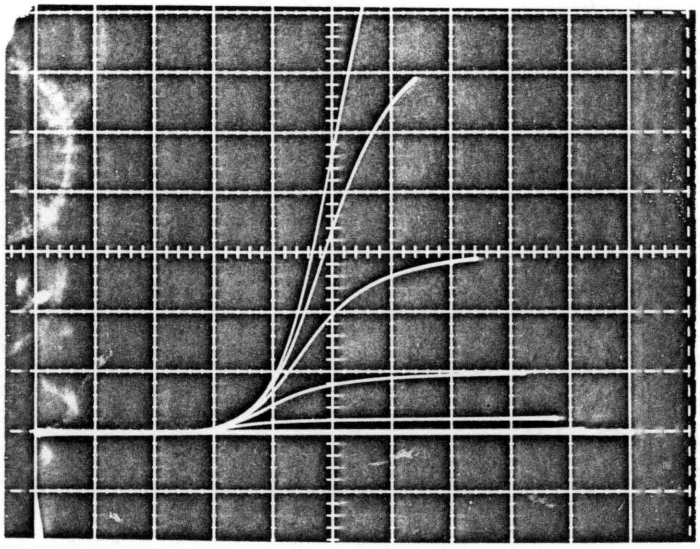


Figure 2.5.a: Oscillograph of the static characteristics of an RCA TA9437B COMFET.



Vert. 100mA/div

Hor. 200mV/div

per step 200mV

g_m 0.5/div

Figure 2.5.b: Oscillograph of the static characteristics of an RCA TA9437B COMFET showing the 0.7V turn on drain-source voltage.

2.2.3. THE IGT IN ITS REVERSE BLOCKING MODE

Unlike the power MOSFET, the IGT has an inherent reverse voltage blocking capability. If a reverse voltage is applied between the drain and source terminals, the junction J1 between the n^- epitaxial region and the p^+ drain region becomes reverse biased. The reverse voltage is also dropped across the high resistivity n^- region because the space charge region exists mainly in the lightly doped epitaxial region.

However, the reverse blocking voltage of an IGT is however less than the forward blocking capability of the device. This is because the open base breakdown voltage of the heavily doped p-base of the n-p-n transistor (shown in the equivalent circuit of Figure 2.2) breaks down at values between 15% and 30% of the forward breakdown voltage of the IGT. In motor control applications, the reverse blocking capability should be high enough to prevent damage due to reverse voltages during the recovery time of the anti-parallel fast recovery diode. Most of the applications for which the IGT has been targeted, however, need reverse conducting capability.

2.2.4. TURN-ON PROCESS IN AN IGT

The turn-on process in an IGT can be considered to be a combination of the rise times of a power MOSFET and a p-i-n diode. Turn-on delay time is caused by the combination of the delay caused by the polysilicon MOS gate to charge the input capacitance and the forward recovery time of a p-i-n diode. The rise time is caused essentially by the rise time of a p-i-n diode. The rise time of the IGT is also of the order of a few tenths of a microsecond.

The oscillographs of Figure 2.6 and Figure 2.7. show the voltage and current waveforms during turn-on in an IGT.

2.2.5. TURN OFF PROCESS IN AN IGT

The turn-off process in an IGT is very unique. The IGT shows significant turn-off delay (storage) times and fall times.

The storage times in an IGT are caused by the rate of discharge of the gate-source capacitance and also by the minority carrier saturation mechanism similar to that of a power bipolar transistor. The storage time depends on the type of load being switched and the value of the gate-source resistance. The high value of gate-source resistance in IGT drive circuits causes slow discharge of the gate capacitance and hence causes large device storage times. During the

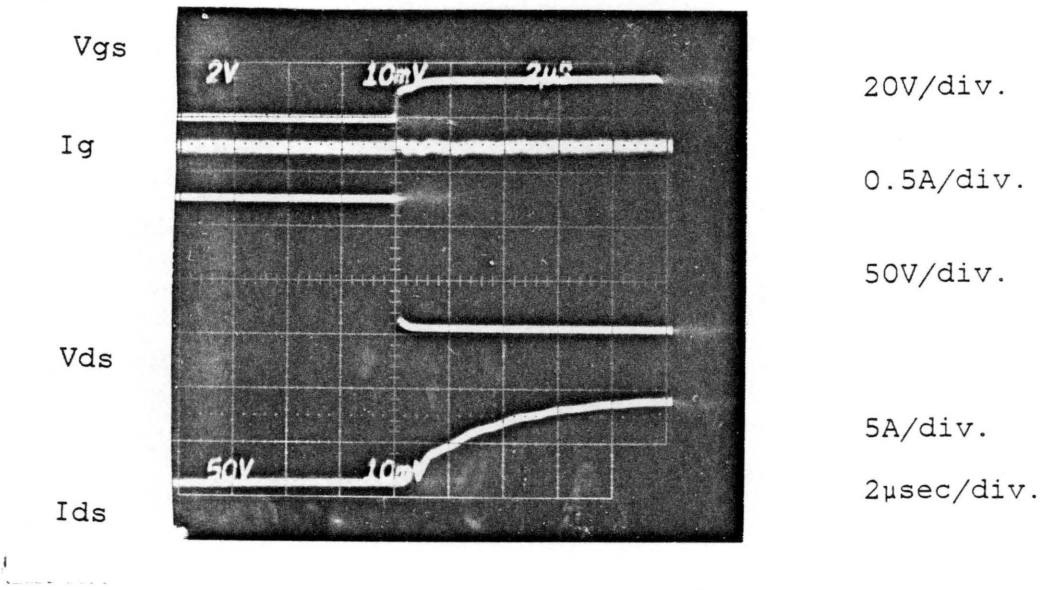
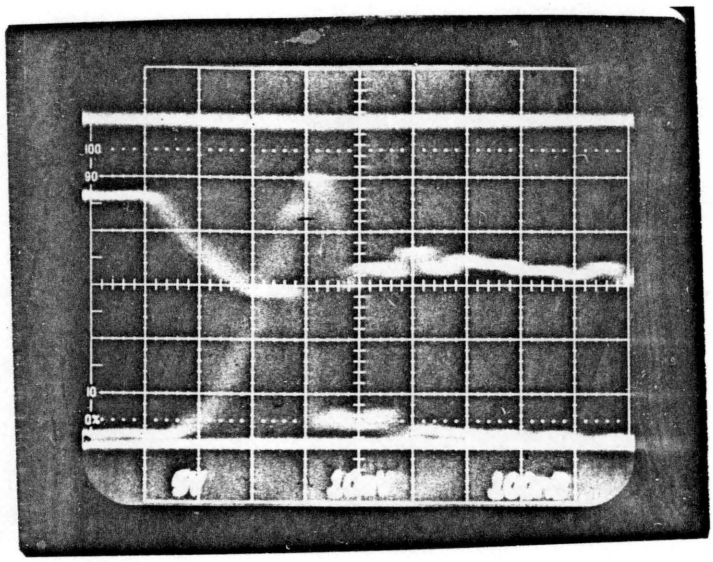


Figure 2.6: Oscillograph of the drain and gate voltages and currents during turn-on in a RCA TA9437B.



V_{DS} 50V/div.

I_D 2A/div.

V_{GS} 10V/div.

50 ns/div.

Figure 2.7: Oscillograph showing an expanded view of the turn-on characteristics of an RCA TA9437B COMFET switching a discontinuous inductive current.

storage time, the process of recombination in the n^- epitaxial region begins.

The turn-off fall time is divided into two phases, termed t_{f1} and t_{f2} in Figure 2.8. t_{f1} is related to the injection phase and t_{f2} represents the recombination phase. These will be explained below:

a) The Injection Phase.

The time interval t_{f1} begins with the removal of the inversion layer in the p-base. The electron concentration in the n^- epitaxial layer region is high. This results in the injection of electrons into the p^+ substrate region while a corresponding hole current will flow into the p-base region. The injection of the holes stops with the formation of a depletion region between the n^+ source and the p-base. This time interval forms a small fraction of the total device fall time. The larger the current at turn-off, the smaller the time taken for injection. Thus the IGT is one device in which the turn-off time decreases marginally when the magnitude of the current increases.

b) The Recombination Phase.

The second phase is a rather long recombination phase in which the current through the device tails to a very low

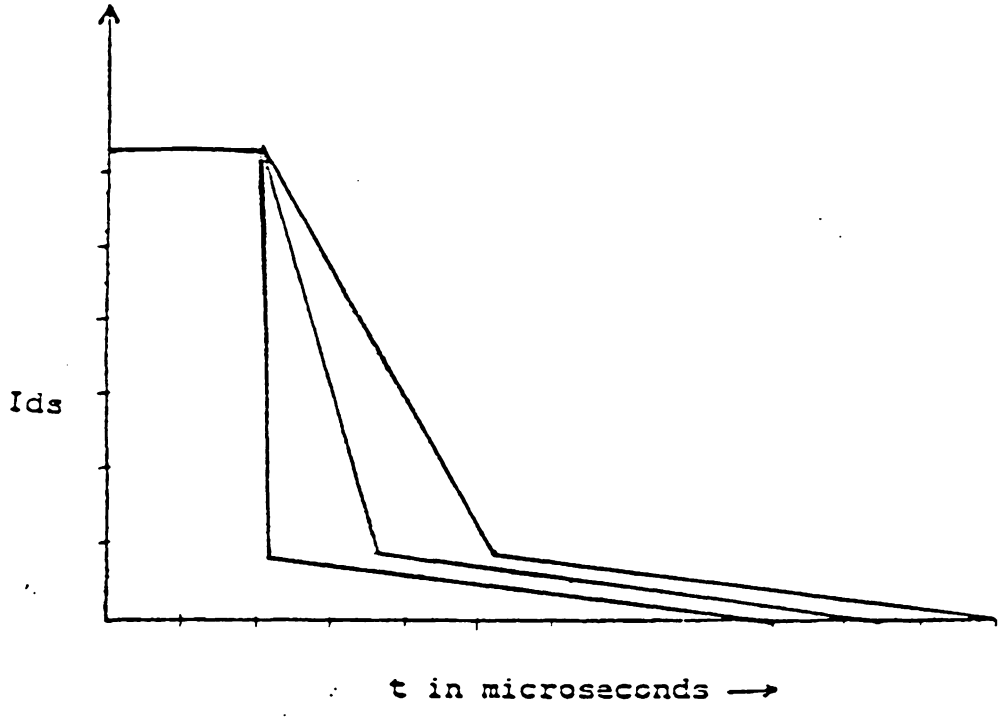


Figure 2.8: Diagram showing the division of the fall time into t_{f1} and t_{f2}.

value. During this phase, the plasma of electrons and holes left in the n^- epitaxial layer decays due to recombination. This time interval is independent of the gate-source resistance and is dependent only on the device design. Long recombination lifetimes imply long minority carrier lifetimes in the n^- region. This phase contributes greatly to increased power dissipation in the device, since during this time the device blocks a high voltage, while at the same time, the current through the device is significant.

The turn-off times vary with device design and with the gate-source resistance. Figures 2.9 to 2.11 show the turn-off voltages and currents of the three different IGTs commercially available.

While low turn-off times are necessary to reduce device losses and temperature, very rapid discharge of the gate-source capacitance will lead to a dv/dt turn-on of the parasitic p-n-p-n structure resulting in device latching, as will be explained in Chapter III.

The creation of direct and indirect recombination centers in the substrate-epitaxial layer junction J1 in Fig. 2.1 reduces the fall times significantly. The recombination centers may be either indirect recombination centers achieved by gold or platinum doping or direct recombination

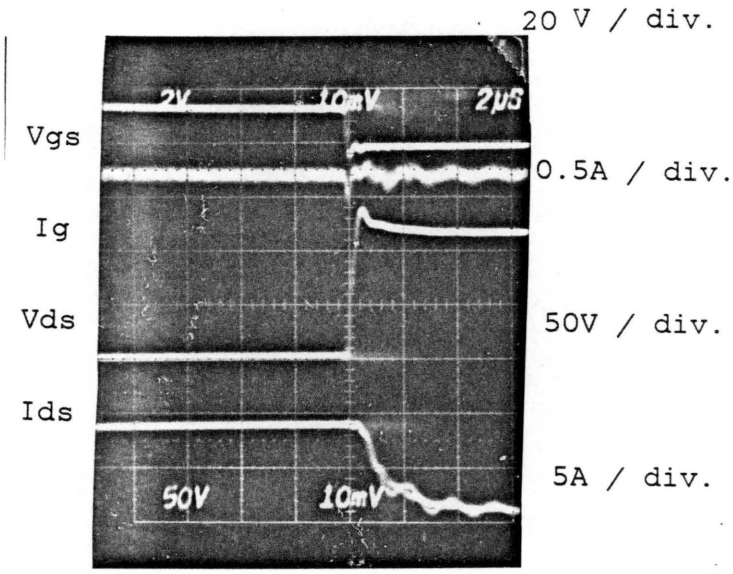
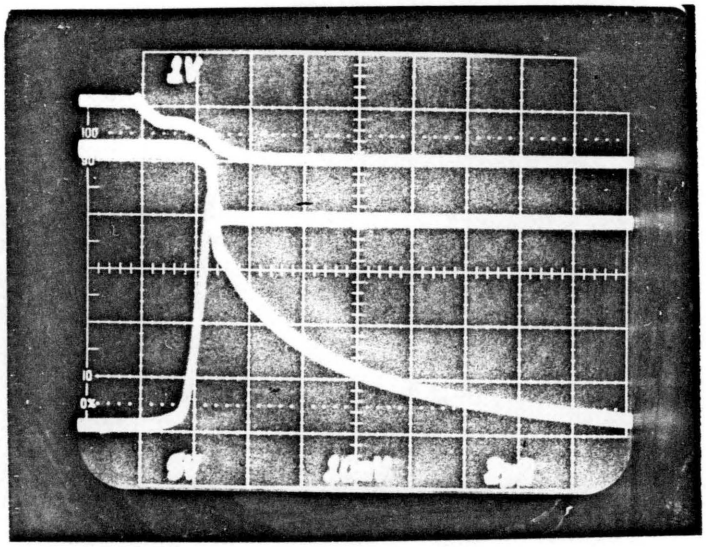


Figure 2.9: Oscillograph showing the drain and gate currents and voltages of an RCA TA9437B COMFET at turn-off.

Note: R_{GS}= 1 kΩ. Case temperature = 29°C. No snubber was used.



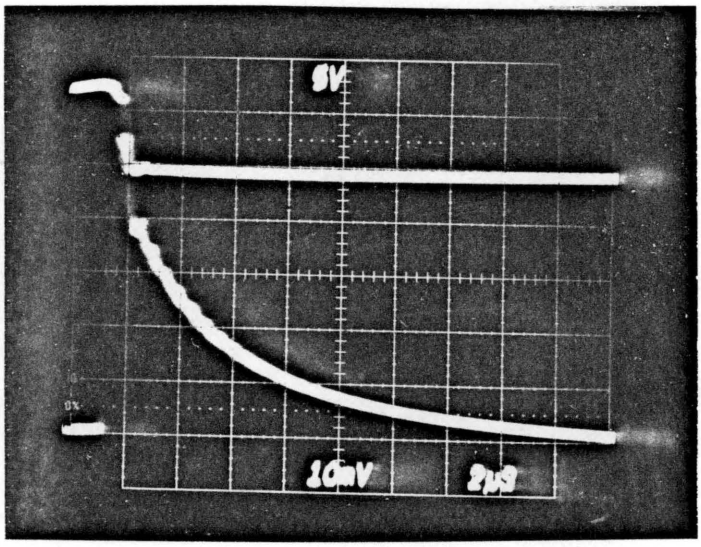
V_{GS} 10V/div.

V_{DS} 50V/div.

I_D 2A/div.

2μs /div.

Figure 2.10: Oscillograph showing the turn-off characteristics of a GE D94FR4 IGT with R_{GS}= 1kΩ. Load Inductance = 8.9mH.



V_{DS} 50V/div.

I_D 1A/div.

2µs /div.

Figure 2.11: Oscillograph showing the turn-off characteristics of a Motorola MGM20N50 GEMFET with R_{GS}= 1 kΩ.

Note: Load Inductance = 8.9mH. Device temperature = 37°C.

centers created by the use of electron or fast neutron irradiation. A ten fold reduction of switching speed is possible with irradiated devices. IGT turn-off times as low as 100 ns have already been reported in laboratory devices [5]. The price to pay is increased conduction resistance and device cost.

2.3. COMPARISON WITH THE CONVENTIONAL POWER MOSFET.

Table 2.1 compares the IGT with a conventional power MOSFET of similar voltage and current ratings. An RCA TA9437B COMFET and an IRF 352 MOSFET are used for the comparison. From Table 2.1 we can make the following observations:

1) Comparison of conduction voltages shows that the conduction voltage of the power MOSFET is higher than that of the IGT even though the IGT has a smaller chip area.The conduction losses in an IGT are considerably less than that of a comparable power MOSFET.The reason for the low on-state voltage is the conductivity modulation in the n^- epitaxial region.

2) Comparison of the device capacitances shows that the input, output and Miller capacitances of the MOSFET are

several times that of the IGT. From the comparison of input capacitances we can infer that the IGT is easier to drive than a power MOSFET and is much more suitable to be driven directly from logic integrated circuits.

3) Both the turn-on delay time and rise times of the IGT are larger than those of an equivalent power MOSFET but the difference does not adversely affect device performance. The storage and fall times of the IGT are a serious disadvantage, being many times those for an equivalent power MOSFET and result in large switching losses.

4) A significant feature in the comparison table is the great saving in chip area enjoyed by the IGT over the MOSFET. Smaller chip areas translate to smaller cost per device and also better device yields if the manufacturing processes are similar.

TABLE 2.1: COMPARISON BETWEEN AN IGT AND A POWER MOSFET OF SIMILAR RATINGS (400V AND 10A).

DEVICE CHARACTERISTIC	RCA TA9437B	IRF 352
CONDUCTION MECHANISM	BIPOLAR	UNIPOLAR
EXHIBITS LATCHING?	YES	NO
BREAKDOWN V_{DSS}	400V	400V
I_D MAX	10A	10A
$V_{DS\ ON}$ at 5A.	1.5V	2V
$V_{DS\ ON}$ at 10A.	2V	4V
INPUT CAPACITANCE	650pF	4000pF
OUTPUT CAPACITANCE	230pF	600pF
REVERSE TRANSF. CAP.	60pF	200pF

DEVICE CHARACTERISTIC	RCA TA9437B	IRF 352
TURN ON DELAY TIME	500ns	60ns
TURN ON RISE TIME	500ns	150ns
TURN OFF DELAY TIME	500ns	400ns
TURN OFF FALL TIME	3000ns	150ns
CHIP AREA	$0.09cm^2$	$0.36cm^2$
MAX. SWITCH. FREQ.	20kHz	200kHz

Table 2.2 compares an IGT with a conventional MOSFET of the same chip areas [4]. A Motorola MGM20N45 IGT and a MOTOROLA MGM4N50 MOSFET are used for comparison. The conclusions drawn from the table are presented below.

1) One of the most striking features of this comparison table is that the current-carrying capacity of the IGT is five times that of the MOSFET. This shows that the IGT has the potential to operate at significantly higher current densities than the power MOSFET.

2) The input capacitances of the two devices are of the same order of magnitude. The turn-on delay times and rise times of the devices are also approximately equal. The storage time and fall time of the IGT are however many times that of an equivalent power MOSFET.

3) At 100°C The conduction voltage of the IGT at 10 A is one half that of the power MOSFET operating at a drain current of 2 A. The low on resistance of the IGT is, thus, a significant advantage, especially at high temperatures.

4) The turn-on delay time and the rise time of the IGT are similar to those of the MOSFET. The very large fall time of the IGT leads to large switching losses in the IGT.

Therefore, from Tables 2.1 and 2.2, we can infer that the IGT is best suited for frequencies below 20 kHz, high current densities and applications involving large duty cycles. Large fall times are a major disadvantage of the IGT. Another disadvantage is the susceptibility to latch, especially at higher temperatures. This is described in detail in the next chapter.

TABLE 2.2: COMPARISON BETWEEN AN IGT AND A POWER MOSFET OF THE SAME CHIP AREA.

DEVICE CHARACTERISTIC	GEMFET MGM20N50	MOSFET MTM4N50
BREAKDOWN V_{DSS}	400V	400V
I_D MAX CONTINUOUS	20A	4A
I_D MAX PULSED	30A	10A
SIDE OF SQUARE CHIP	150mils	150mils
INPUT CAPACITANCE	950pF	1200pF
OUTPUT CAPACITANCE	150pF	100pF
REVERSE TRANSF. CAP.	60pF	80pF

DEVICE CHARACTERISTIC	GEMFET MGM20N50	MOSFET MTM4N50
STATIC ON-RESISTANCE	0.27Ω at 10A	1.5Ω at 2A
$V_{DS(ON)}$ at 100°C	3V at 10A	6V at 2A
TURN ON DELAY TIME	75ns	50ns
TURN ON RISE TIME	150ns	100ns
TURN OFF DELAY TIME	4000ns	200ns
TURN OFF FALL TIME	10000ns	100ns

CHAPTER III

LATCHING CHARACTERISTICS OF INSULATED GATE TRANSISTORS.

Latching in the IGT is the tendency of the device to remain in its low impedance state, regardless of the gate voltage. One of the most important drawbacks of using the the IGT family of devices is their tendency to latch under certain conditions. Latching is, in many circuit applications, very dangerous and could lead to catastrophic short circuits. This phenomenon has not been well understood and no systematic study of the factors contributing to latching has been reported.

In this chapter, experiments were conducted to study the latching properties of IGTs. In Section 3.1, theoretical expressions were derived for the current level necessary to cause device latch . Section 3.2 describes the efforts to determine all the factors leading to device latching and also reports the results of the experiments to determine the variation of latching current with each of these factors. Section 3.3 lists the various steps taken by manufacturers to decrease the susceptibility of the devices to latch. The results of a study of latching of paralleled devices is given in Section 3.4. Section 3.5 discusses latching in

resonant converters. A summary of the practical means to avoid latching, pointing out the constraints involved in IGT circuit design and discussing the tradeoffs involved in fast switching are discussed in Section 3.6.

3.1. THEORY OF LATCHING.

Latching in the IGT is caused by an increase in the sum of the current gain parameter, alpha of the p-n-p transistor and the parasitic n-p-n transistor till they equal unity.

The theory of conditions leading to device latchup in the IGT has been developed and is given below :

Consider the currents in Figure 2.1. Represent the drain current as I_D, the source current I_S and the current through the ideal MOSFET as I_M.

Current through (n-p-n transistor and shunt)= $I_S - I_M$

Replace the n-p-n transistor and shunt resistance by an equivalent n-p-n transistor with its current gain alpha parameter = α'.

$$\alpha'_{npn} = \alpha_{npn} x \{ I_{npn} / (I_{npn} + I_{shunt}) \} \qquad (1)$$

Therefore the lower the shunt resistance, the lower will be the alpha parameter of the equivalent transistor. Applying to each of the transistors, the KCL we get:

$$I_C=(-\alpha)xI_E + I_{CBO} \qquad (p\text{-}n\text{-}p) \qquad (2)$$

$$I_C=(\alpha)xI_E + I_{CBO} \qquad (n\text{-}p\text{-}n) \qquad (3)$$

$$I_D= (\alpha_{pnp})xI_D+I_M+(\alpha'_{npn})x(I_S-I_M) + I'_{CBO\ npn} + I_{CBO\ pnp} \qquad (4)$$

Since $I_D=I_S$,

$$I_D=(\alpha_{pnp}+\alpha'_{npn})xI_D + I_Mx(1-\alpha'_{npn}) + I'_{CBO\ npn} + I_{CBO\ pnp} \qquad (5)$$

$$I_D= - \frac{\{I_Mx(1-\alpha_{npn}) + I'_{CBO\ npn} + I_{CBO\ pnp}\}}{1-\alpha_{pnp}-\alpha'_{npn}} - \qquad (6)$$

Therefore when the sum $(\alpha_{pnp}+\alpha'_{npn})$ approaches unity, the value of I_D increases greatly and device latching occurs [6].

3.2. FACTORS CAUSING LATCHING

A study of latching in IGTs was undertaken to determine the causes of latching and the relative importance of each cause.

For a given load, four factors were identified as the

causes for latching in IGTs :

1) Excessively high current magnitudes.

2) Excessively high temperatures.

3) High rate of rise of drain-source voltage and

4) High rate of fall of gate-source voltage.

Experiments were performed to determine the effect of the variation of latching current level with the device case temperature, the rate of fall of gate-source voltage and the rate of rise of drain-source voltage. The theory and experiments on the effects of each of the factors on the latching current are discussed below in separate subsections.

3.2.1. HIGH CURRENT LEVELS

3.2.1.1. THEORY OF LATCHING DUE TO HIGH CURRENT LEVELS.

The alpha parameter of a transistor is directly proportional to the collector-emitter current through the transistor. Consider the equivalent circuit of Figure 2.1. An increase in the current through the IGT will result in an increase in the alpha parameters of both the transistors,especially that of the p-n-p transistor. The device thus latches.

3.2.1.2. RESULTS OF LATCHING DUE TO HIGH CURRENT LEVELS.

Figure 3.1 shows the static characteristic of the IGT at the time of latching. After latching occurs, the saturation characteristics seen on the right side of Figure 3.1 are replaced by the low impedance characteristic seen in the left side of Figure 3.1. The oscillograph shows that latching occurs due to excessively high currents and not due to any phenomenon associated with device temperature or turn-off. High currents through the IGT force the dc alphas of the device to increase enough to cause latching. Latching therefore occured before the device was turned off.

3.2.2. HIGH DEVICE TEMPERATURES.

3.2.2.1. THEORY OF DEPENDENCE OF LATCHING ON TEMPERATURE.

High temperature is another very important factor that causes device latching in the IGT. Consider Equation 3.5 developed in Section 3.1. Again, an increase in the temperature of the device results in an increase in the alpha parameters of both the transistors and this causes latching in the device.

3.2.2.2. EXPERIMENTAL SETUP

A series of experiments were carried out with RCA

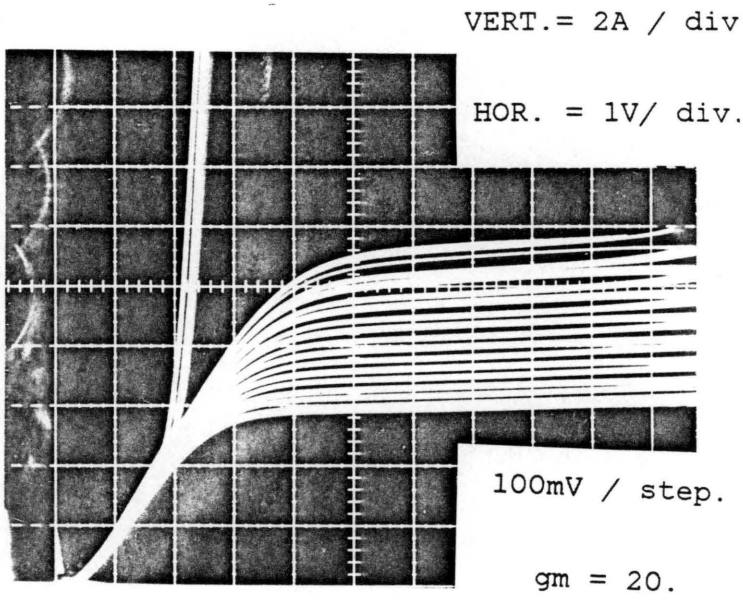


Figure 3.1: Oscillograph of the static characteristics of an IGT at the time of latching. The device used is a TA9437B COMFET.

COMFETs, GE IGTs and Motorola GEMFETs in order to learn more about the effect of temperature on device latching.

All experiments used a setup shown in Figure 3.2.a. The gate drive used is shown in Figure 3.2.b. A load consisted of a resistive and an inductive part. This was provided by 200 W power resistors totalling 10Ωs in series with a brushless dc motor (inductance of 1.8 mH and resistance of 0.7Ω). An IRF 16FL60S02 Fast Recovery Diode was used to clamp the voltage across the IGT to the supply voltage. An astable multivibrator provided a square wave pulse of 50% duty cycle at a frequency of 2 kHz. A buffer inverter was used to increase the current capability of the drive circuit. The device temperature was altered by passing continuous current through the IGT and the temperature of the IGT at the case of the TO 3 package (drain terminal) was measured. A small heat sink was used to control the rate of change of device temperature. Drain voltage was provided by a linear power supply with a maximum current capability of about 33 A. The temperature measured is correct to 0.5°C. The current was measured using an oscilloscope. Experiments were performed on the GE IGT, the RCA COMFET and the MOTOROLA GEMFET. The results of experiments on the GE IGT and the RCA COMFET are given in Figures 3.3 and 3.4. The GEMFET was found not to latch even

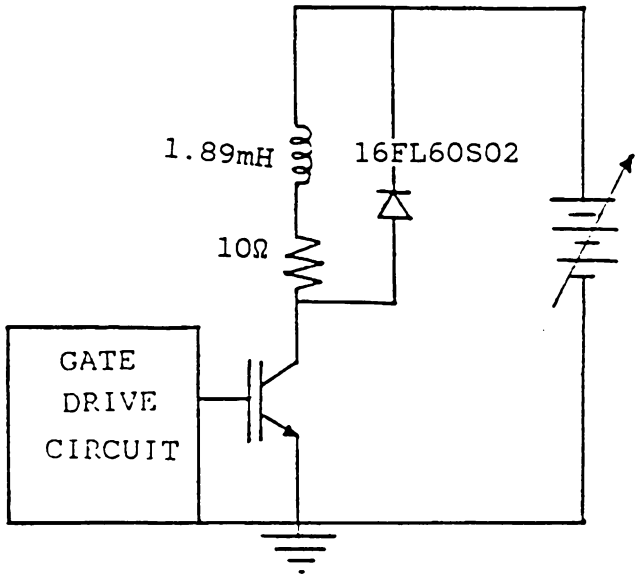


Figure 3.2.a: Diagram of the circuit used for the experiments on latching.

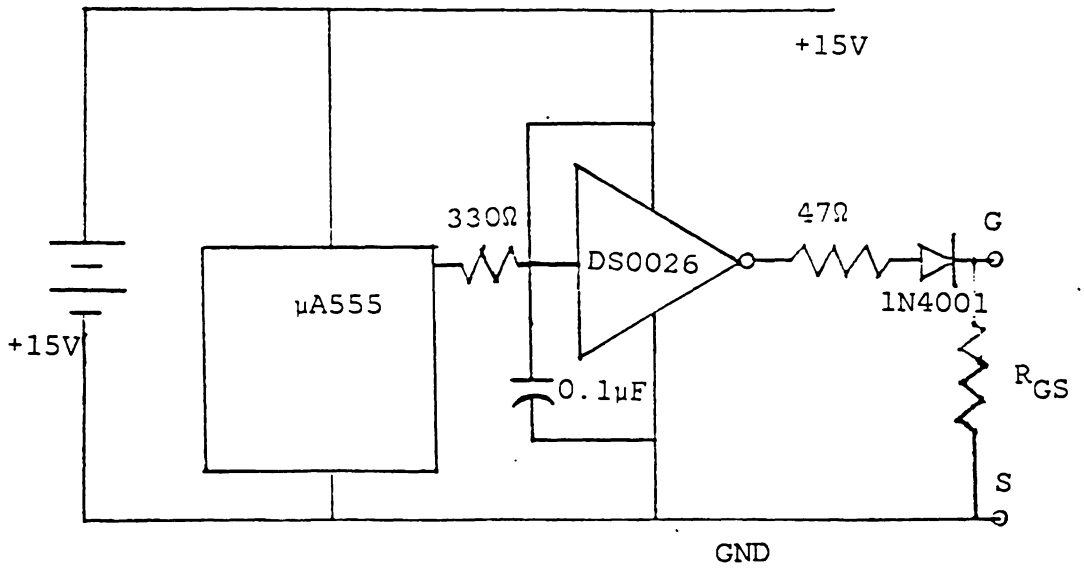


Figure 3.2.b: Gate drive circuit diagram for the circuit of Figure 3.2.a.

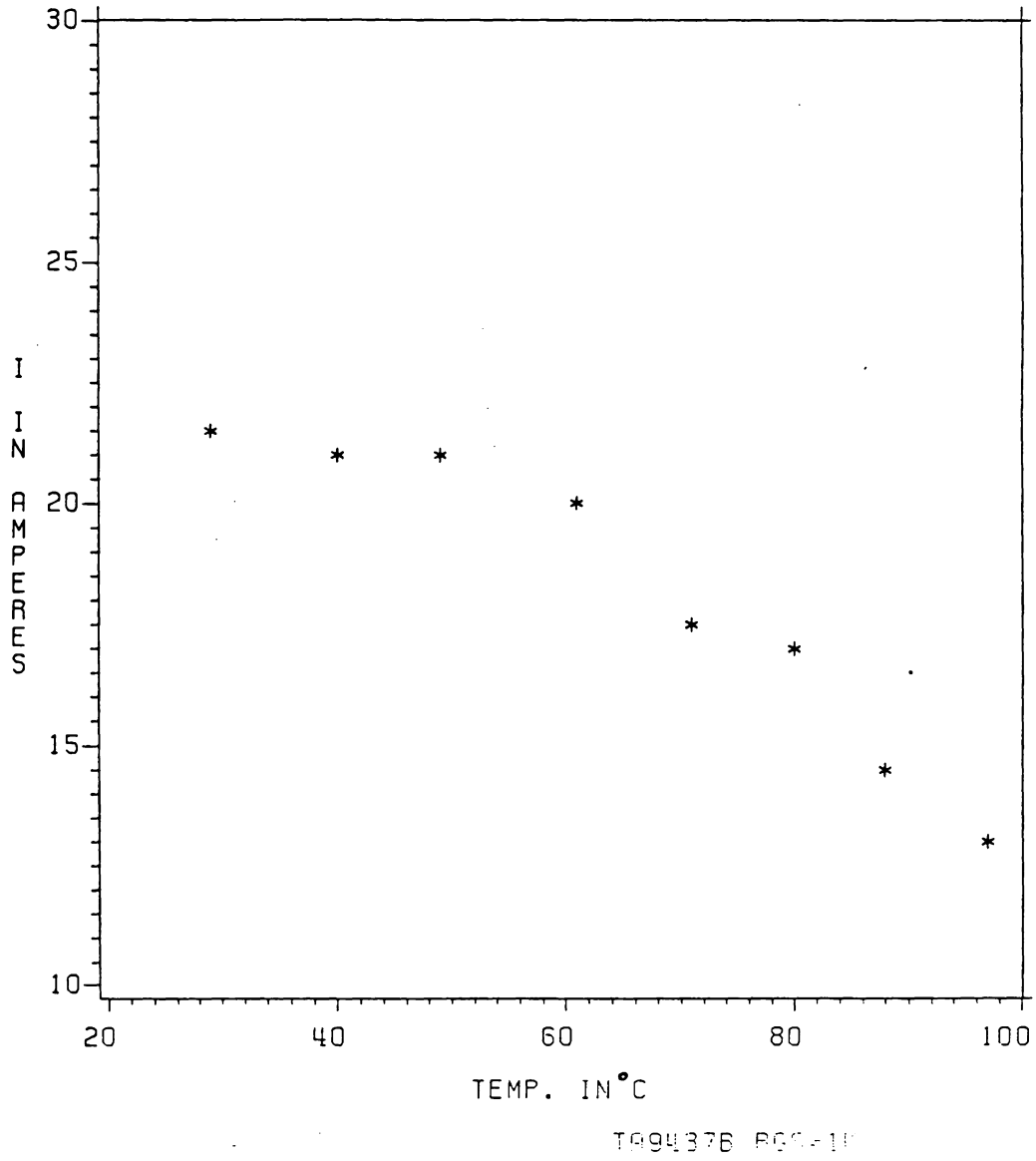


Figure 3.3: Variation of latch-free current with device temperature in a COMFET. R_{GS} = 1K No snubber capacitance used.

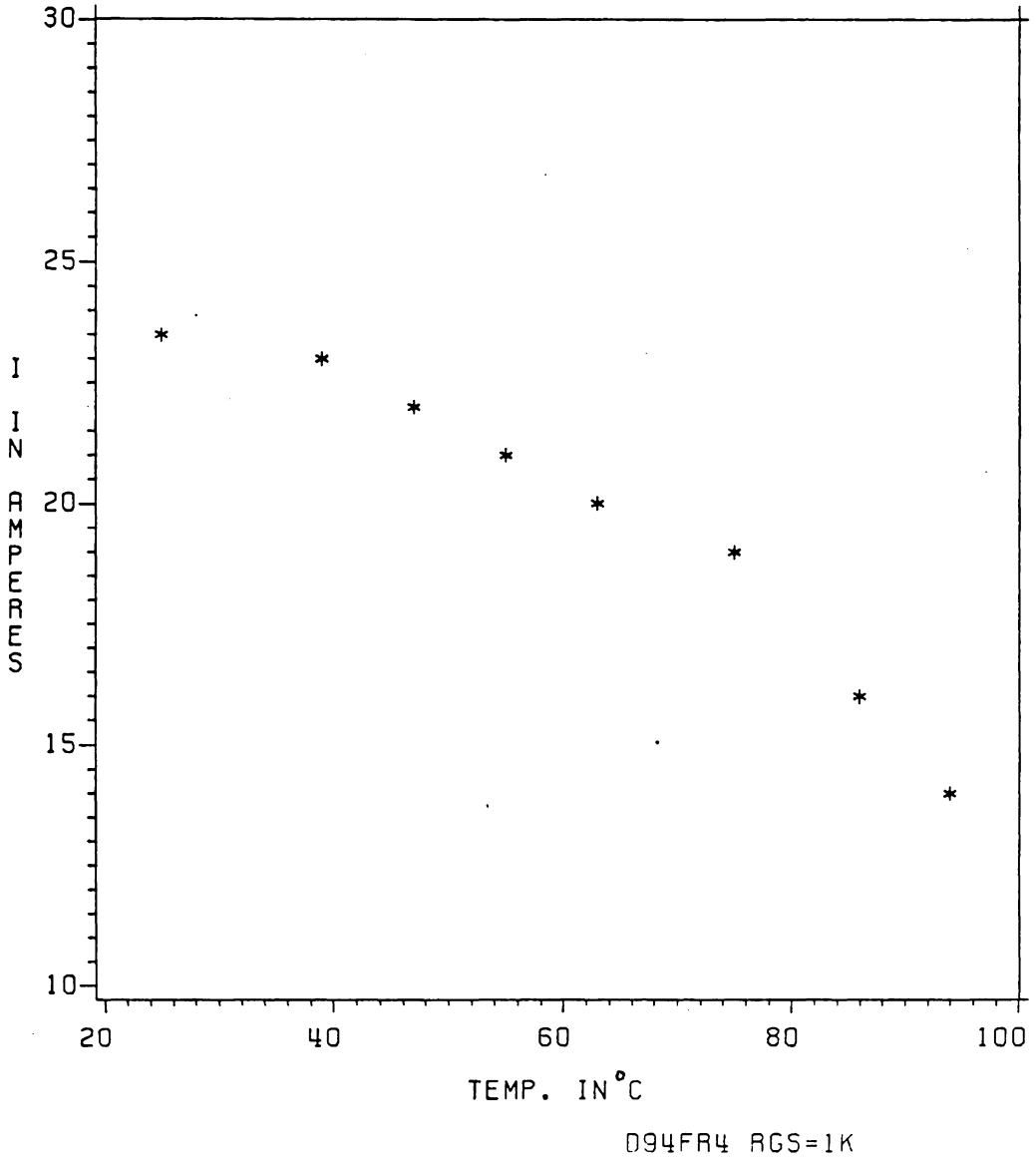


Figure 3.4: Variation of latch-free current with device temperature in an IGT. R_{GS}= 1K. No snubber capacitance used.

at 30 A and 89°C.

A second set of temperature measurements examined the effect of high temperatures together with the rate of fall of gate-source voltage and also the rate of change of rise of drain-source voltage. These tests were made on the GE IGT and the RCA COMFET. The device temperatures for these tests was maintained at around 80°C. The results of these tests can be found in Figures 3.5 to 3.8.

3.2.2.3. RESULTS OF THE VARIATION WITH TEMPERATURE.

The latching current level is very strongly dependent on the device temperature. The higher the temperature of the device, the lower the latching current level. As we move from 25°C to about 85°C, the current level is nearly halved.

The relationship between latch-free current level and temperature is almost linear and monotonic. The strong dependence of the latching current on temperature is a major disadvantage of the use of IGTs. This tells us that even though these devices are rated up to 150°C the IGTs show very poor high temperature characteristics due to the possibility of latching. Excellent heat sinking is necessary for high current operation. The variation of device latching current does not depend on the speed of switching of the device and both the devices, the slow GE

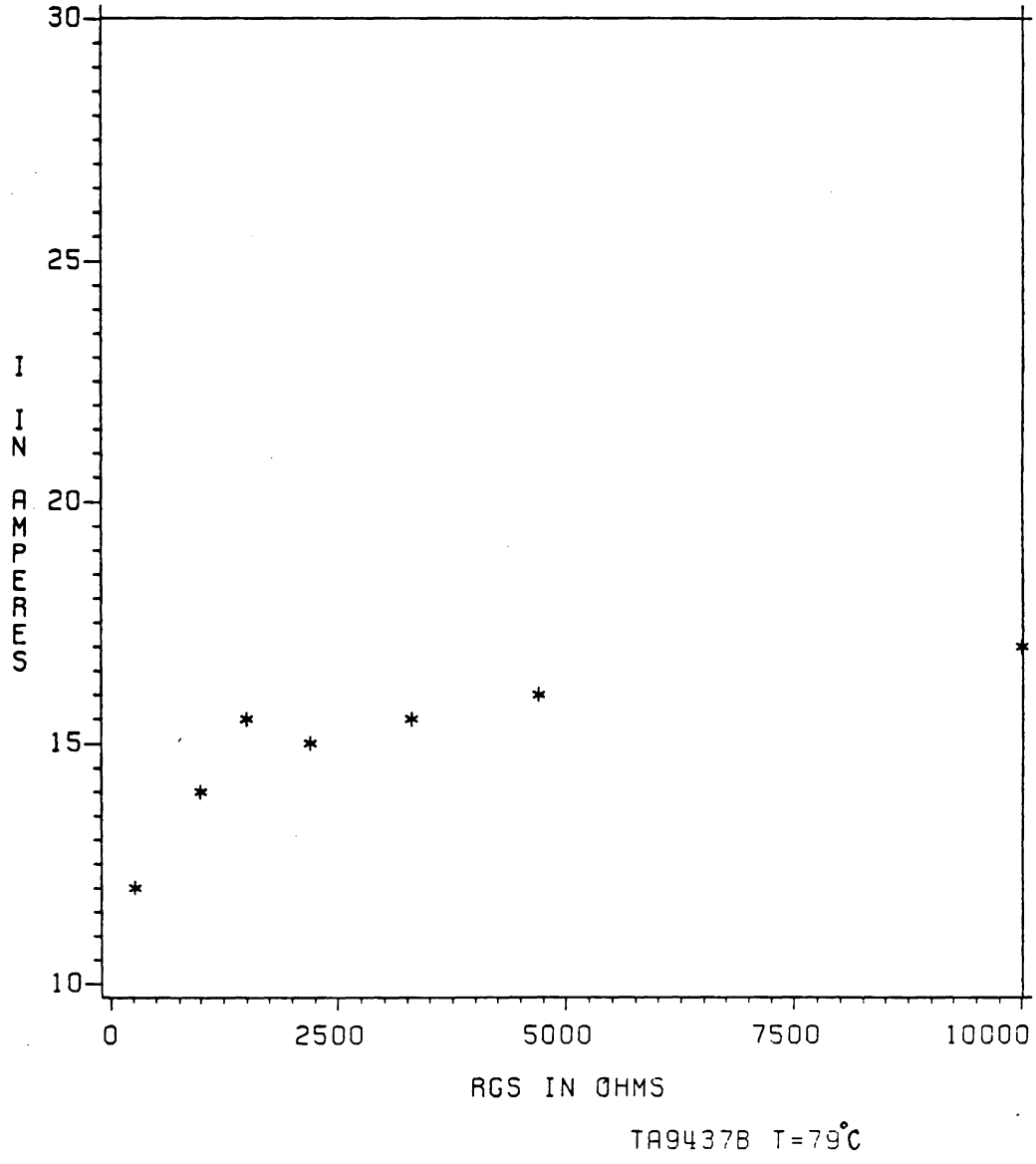


Figure 3.5: Variation of latch-free current in a COMFET with the gate-source resistance

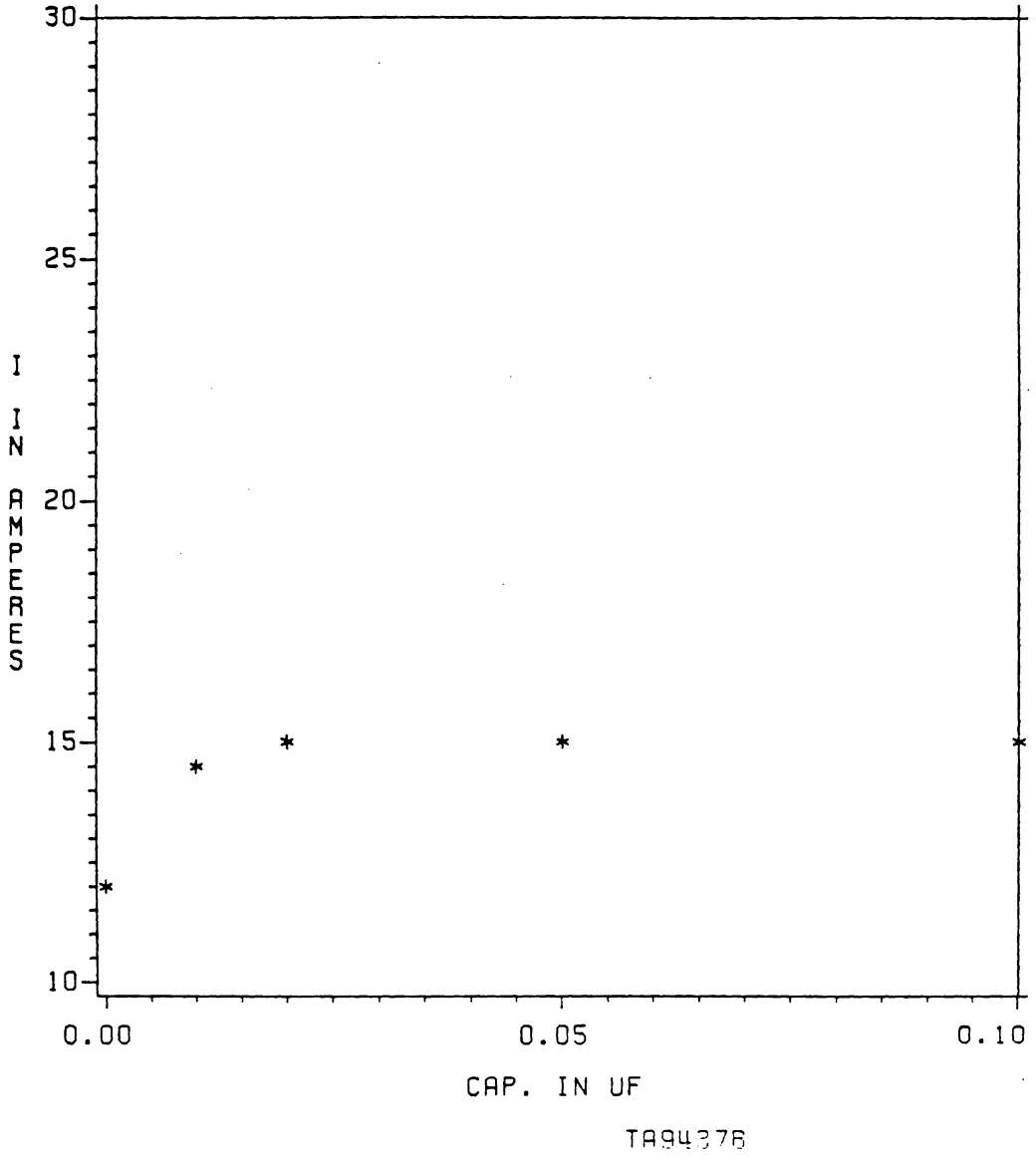


Figure 3.6: Variation of latch-free current in a COMFET with the snubber capacitance across the device. Temperature = 78 C.

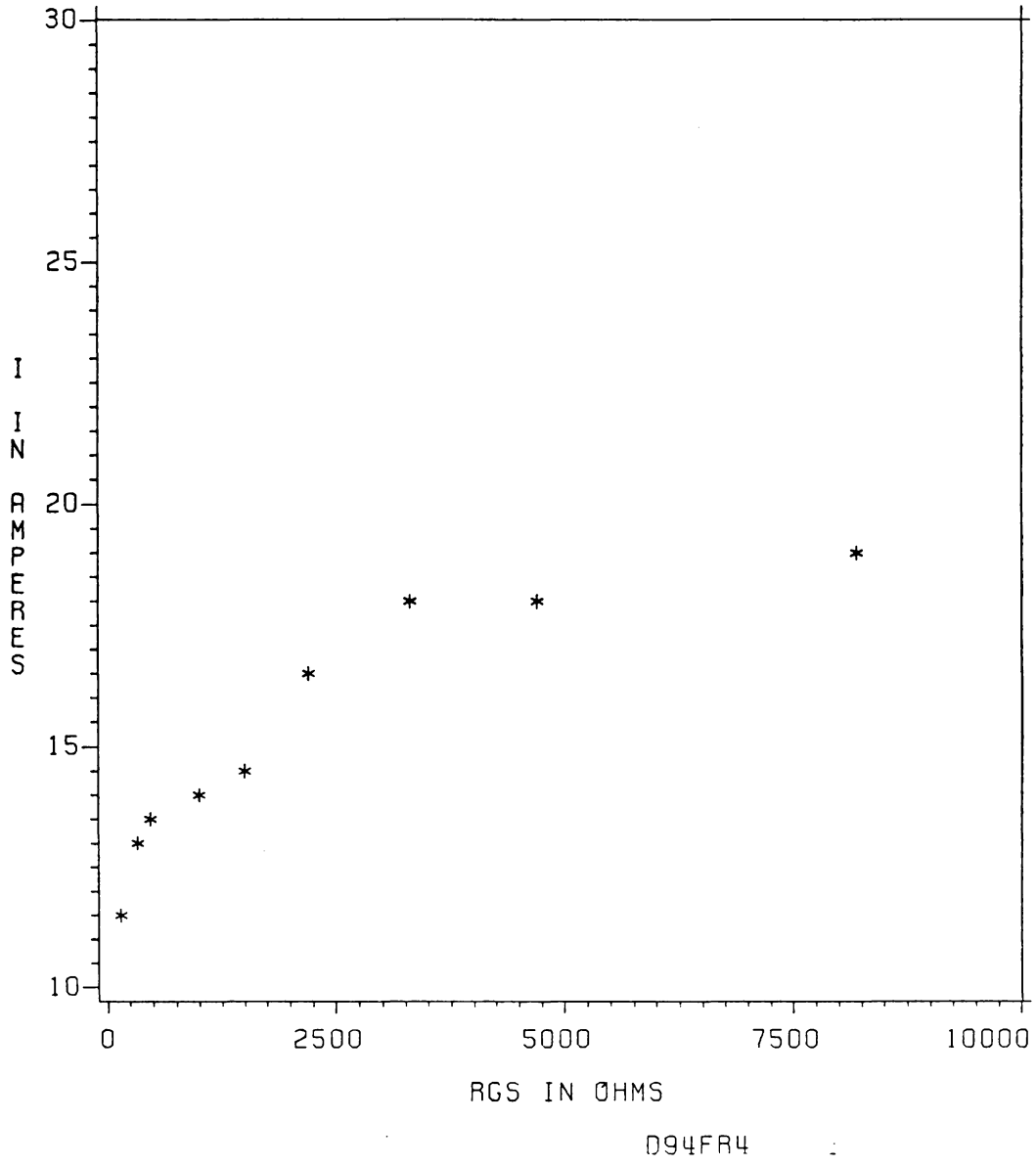


Figure 3.7: Variation of latch-free current in an IGT with the gate-source resistance of the device. Temperature = 80°C.

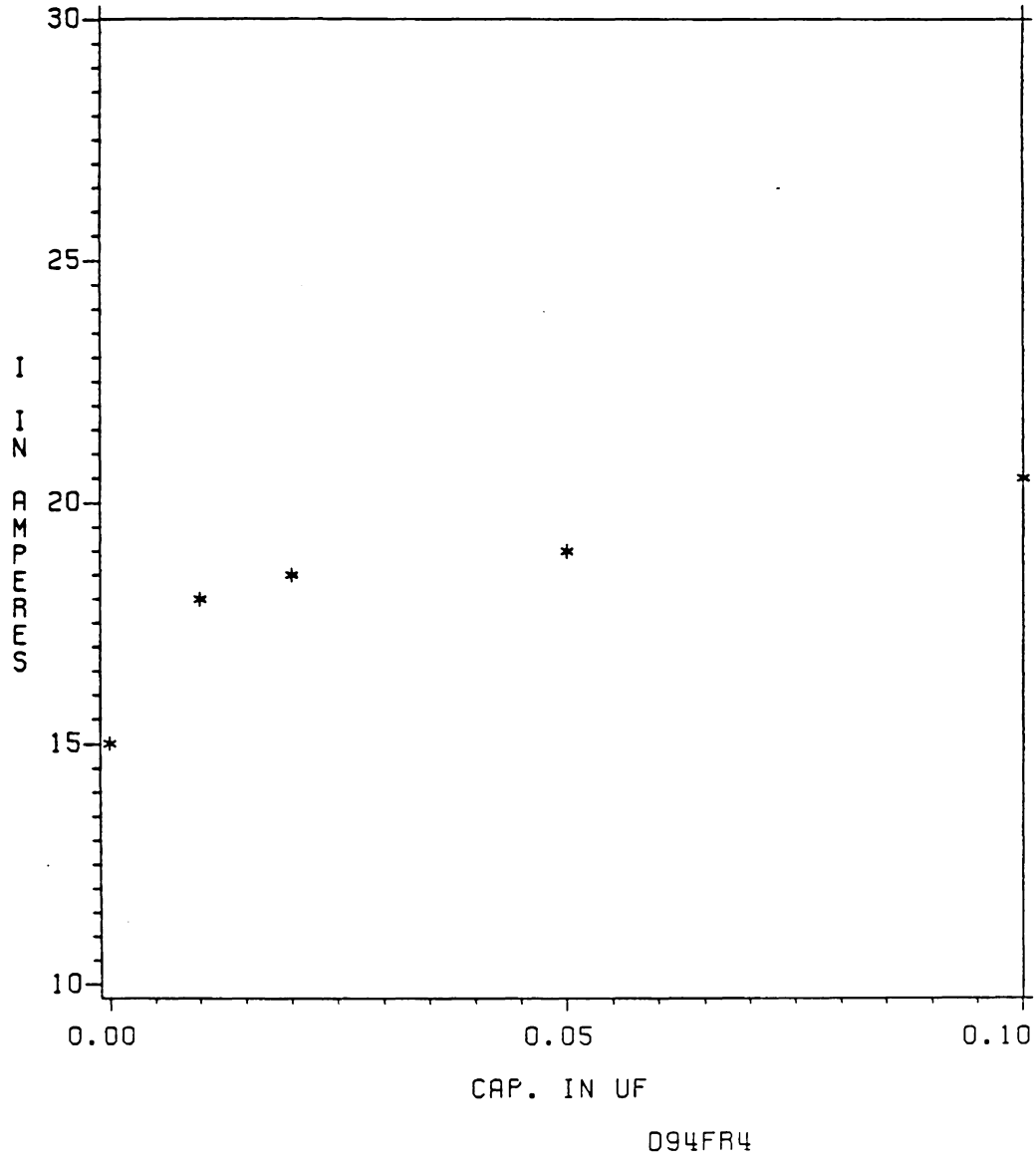


Figure 3.8: Variation of latch-free current in an IGT with the snubber capacitance across the device. Temperature = 78 C.

D94FR4 and the fast switching RCA TA9437B have very similar temperature characteristics.

The tests on the effect of a combination of two of the three factors causing latching showed that the device temperature is the dominant cause of latching.

3.2.3. HIGH RATE OF RISE OF DRAIN SOURCE VOLTAGE.

3.2.3.1. THEORY OF LATCHING DUE TO RATE OF RISE OF V_{DS}.

The equivalent circuit of the IGT shown in Figure 3.9 includes a depletion layer capacitance between the collectors and the bases of the two transistor equivalent structures [7]. This capacitance is charged when the IGT is in the off state and discharged during device turn-on. The charging of the capacitor is through the p-n-p transistor. A very high rate of rise of drain source voltage will lead to a current inrush through the p-n-p structure, increasing momentarily, the current gain of the structure. Even a momentary increase in the instantaneous alpha parameter of the p-n-p transistor can cause a regenerative process that leads to the current latching. The latching process in the IGT begins when the sum of the ac alphas of the two transistor equivalent structures equals unity and continues till the sum of the two dc alphas of the transistors reaches

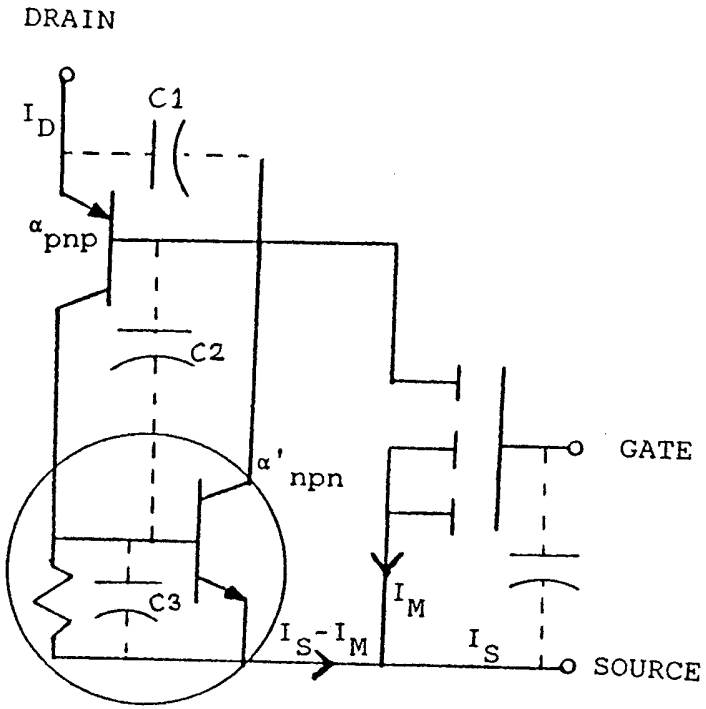


Figure 3.9: Transistor equivalent circuit of an IGT showing the internal junction capacitances.

one. A quantitative explanation in terms of the equivalent circuit can be given with the help of Figure 3.9.

Of the three capacitances C_1, C_2 and C_3 in Figure 3.9, capacitances C_1 and C_3 are diffusion types while C_2 is a depletion capacitance. C_2 is much larger than (C_1+C_2). Therefore we may consider only C_2. The capacitance C_2 gives rise to a current = $C_2(dv/dt)$.

$$I_D = \frac{\{I_M x(1-\alpha_{npn}) + I'_{CBO\ npn} + I_{CBO\ pnp} + C_2(dv/dt)\}}{1-\alpha_{pnp}-\alpha'_{npn}} \qquad (7)$$

The higher the rate of change of voltage across the capacitance C_2 the greater is the current and a higher current level further increases the alpha parameters in the two transistor.

3.2.3.2. EXPERIMENTS ON RATE OF RISE OF DRAIN VOLTAGE.

The diagram of the circuit used for the experiments is the same as Figures 3.2.a. and 3.2.b. Tests were carried out on the GE D94FR4 and also the RCA TA9437 COMFETs. The gate-source resistance used in these experiments was 1 kΩ. The results of these experiments comprise Figures 3.10 and 3.11. The MOTOROLA MGM20N50 GEMFET did not exhibit any latching at all up to 30 A even when no snubber was used. A snubber circuit was used to vary the rate of rise of

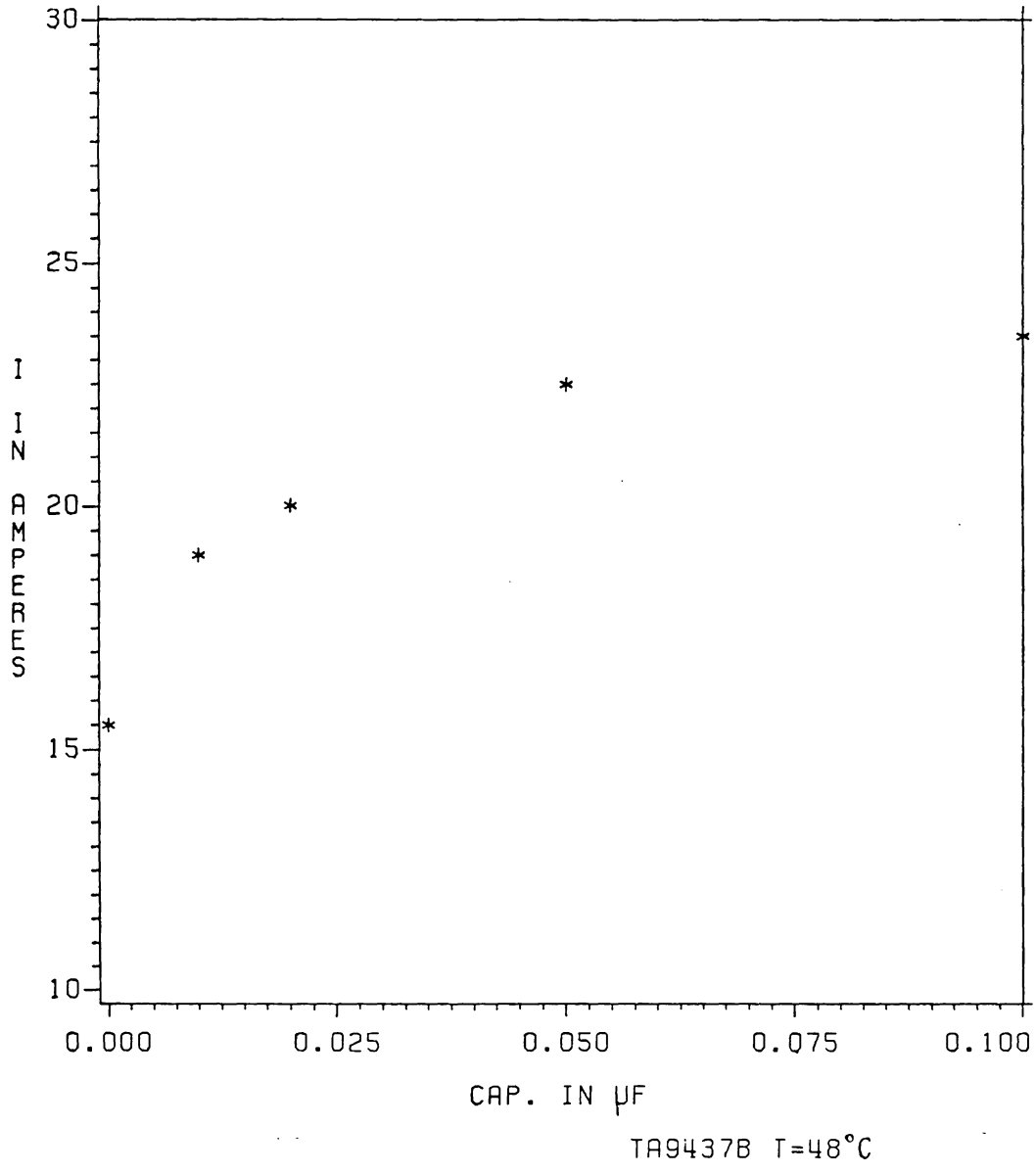


Figure 3.10.a: Variation of latch-free current in a COMFET with the snubber capacitance. R_{GS} = 1K.

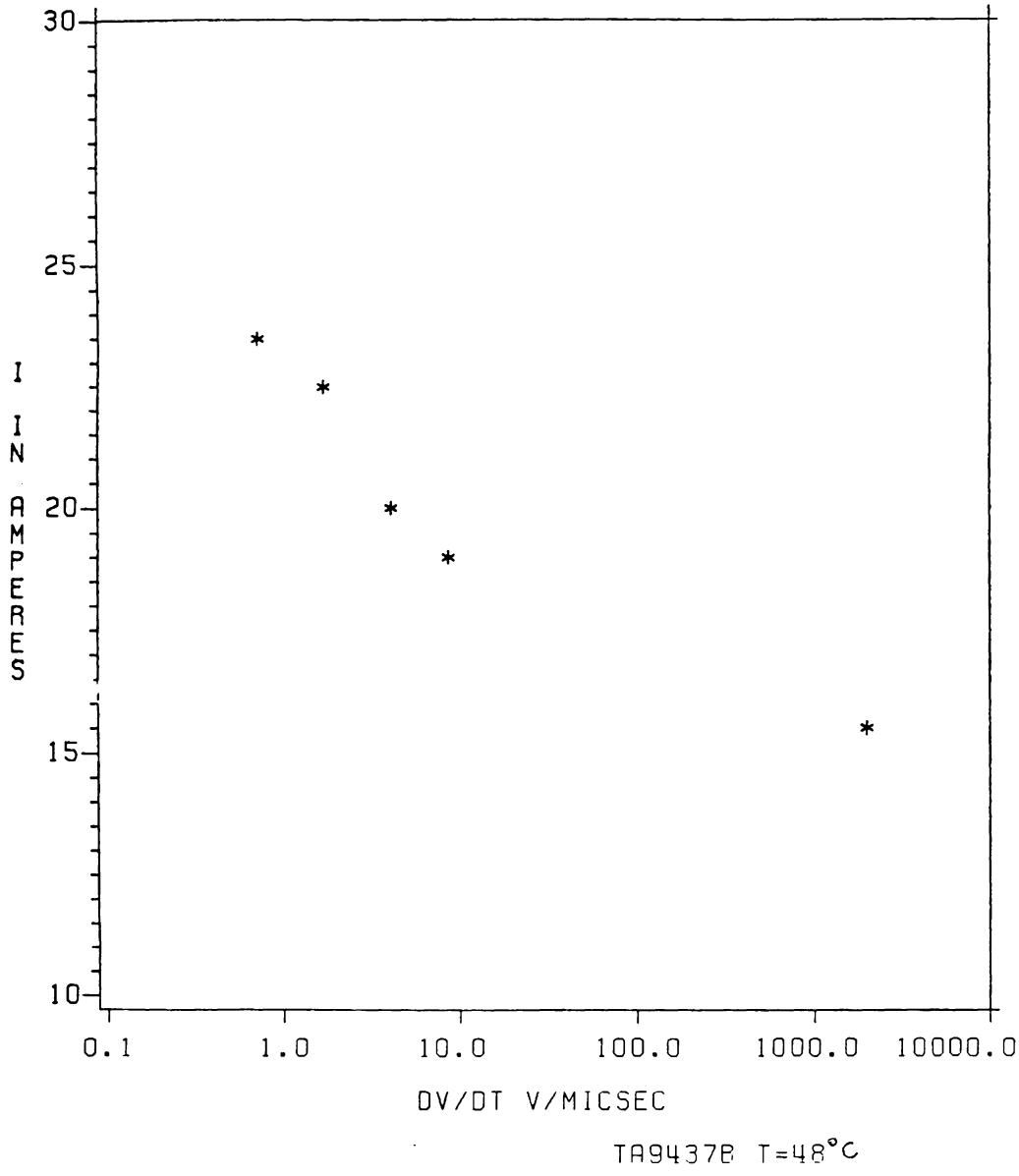


Figure 3.10.b: Variation of latch-free current in a COMFET with the rate of rise of drain-source voltage. R_{GS} = 1K.

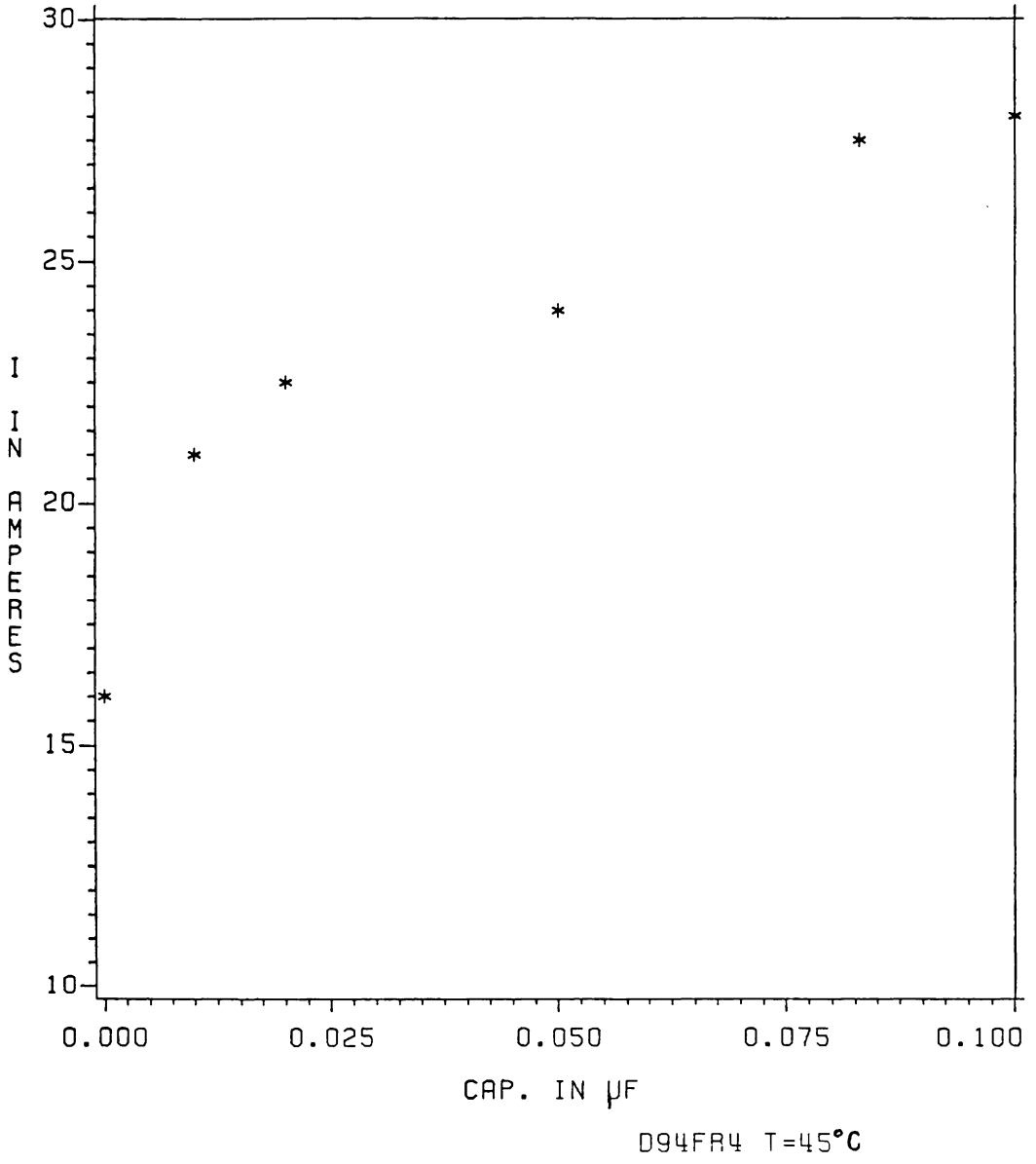


Figure 3.11.a: Variation of latch-free current in an IGT with snubber capacitance. R_{GS} = 1K.

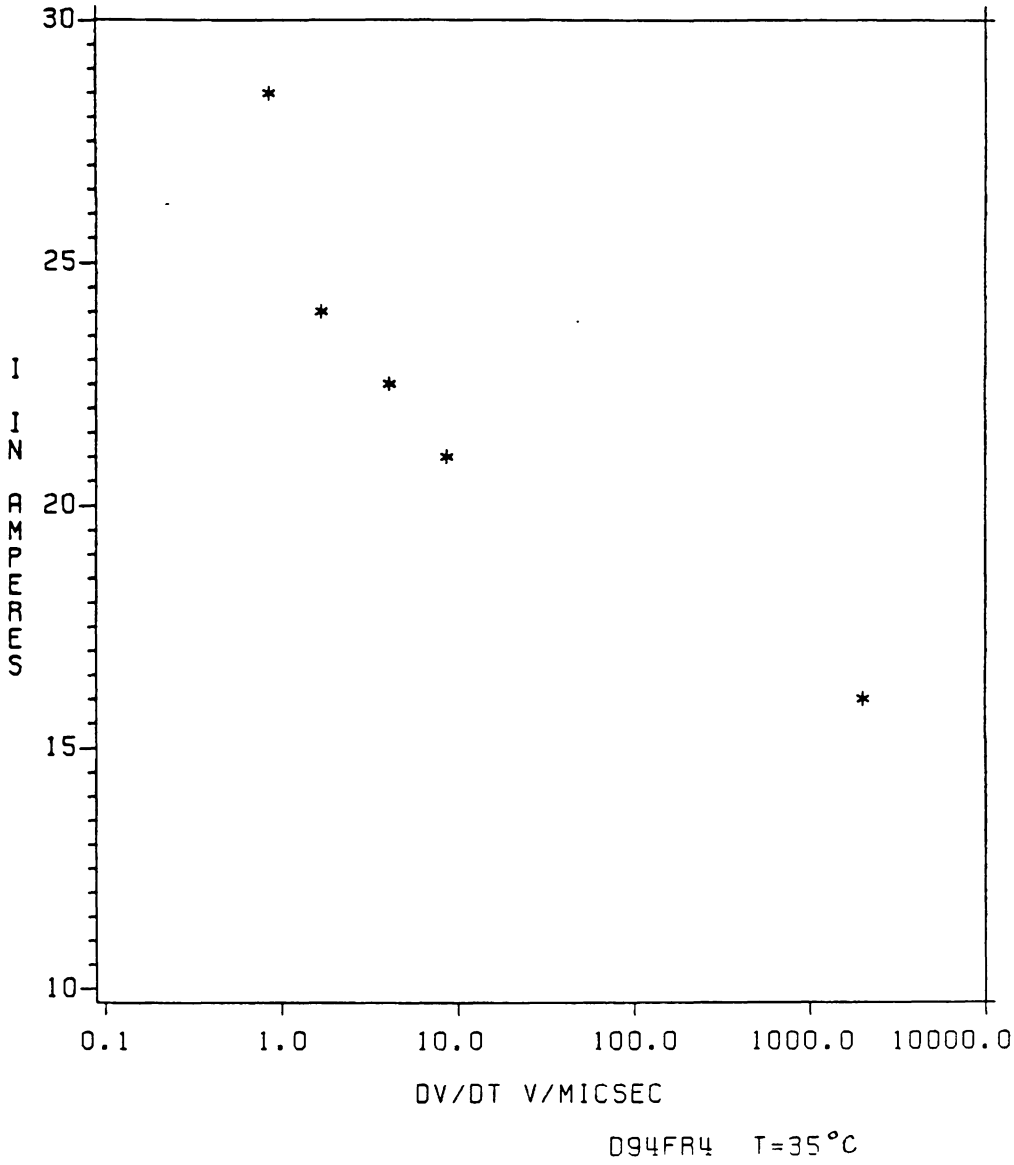


Figure 3.11.b: Variation of latch-free current in an IGT with the rate of rise of drain-source voltage. R_{GS} = 1K.

drain-source voltage at turn-off. The snubber capacitance was varied in a simple RCD circuit. The larger the capacitance, the slower is the rate of rise of drain-source voltage. The temperature of the IGT under test was kept constant by using a large heat sink and also by using a small fan to maintain the temperature at about 45°C. The snubber capacitances were SPRAGUE 6PS-S series 600V capacitors and the diodes were 1N5627 diodes.

3.2.3.3. RESULTS OF RATE OF RISE OF DRAIN VOLTAGE.

The variation of latching current with snubber capacitance varied significantly between the IGT and the COMFET tested. Both the devices showed a considerable increase in the current latching level with a snubber than without a snubber. The increase in latching current in the D94FR4 is greater than that in the faster TA9437B. As with the SCR, the use of a snubber network tends not only to decrease the rate of rise of drain source voltage but also to decrease the device turn-off losses in the IGT. The increase in latching current due to the addition of a snubber capacitance is significant.

3.2.4. HIGH RATE OF FALL OF GATE-SOURCE VOLTAGE

3.2.4.1. THEORY OF LATCHING DUE TO RATE OF FALL OF V_{GS}.

During this kind of latching, the charging of the depletion capacitance causes the increase in the ac alphas of the two transistors, leading to latching in the IGT. The latching current level depends on the depletion capacitance C2 in Figure 3.9, the time taken for the plasma in junction J1 in Figure 2.1 to recombine and the delay between the turn-off in the various paralleled cells comprising the device. Consider turn-off in a single IGT cell. The MOSFET shunts current away from the depletion capacitance. Very fast turn-off of the power MOSFET in the equivalent circuit would mean that the rest of the current flows through the p-n-p transistor and then to the depletion capacitance. The increase in the ac alpha parameter of the equivalent p-n-p transistor causes that cell to latch. Latching of one cell has a positive feedback effect with the other cells also latching. This phenomenon depends on the plasma recombination time t_{f2} and this kind of latching can be found when switching resistive as well as inductive loads.

3.2.4.2. EXPERIMENTS ON RATE OF FALL OF GATE-SOURCE VOLTAGE.

The circuit used for the experiments determining the

variation of the latching current with the rate of fall of gate-source voltage.The circuit used for the experiments is the same as Figures 3.2.a. and 3.2.b and the circuit has been described in 3.2.2.2. The experiments performed used a gate-source turn-off resistance to alter the rate of fall of gate-source voltage.No negative bias voltage was applied during turn-off. Experiments were performed on the RCA TA9437B COMFET and the GE D94FR4 IGT. The results of these tests are given in Figures 3.12 and 3.13. No snubber circuit was used during these tests. A large heat sink and a small fan was used to keep the temperature of the device constant.

3.2.4.3. RESULTS ON CURRENT AND THE RATE OF FALL OF V_{GS}.

The manner in which the gate-source resistance causes a variation in the latch-free maximum switching current level can be seen in Figures 3.12 and 3.13. As can be seen from these figures, the gate-source resistance affects the latching current levels in different devices in very different ways. Here we see that the current level is not as strongly a linear function of the gate-source resistance as it is a function of temperature.

3.3. DEVICE DESIGN TO PREVENT DEVICE LATCHING.

During the past year significant progress was made in

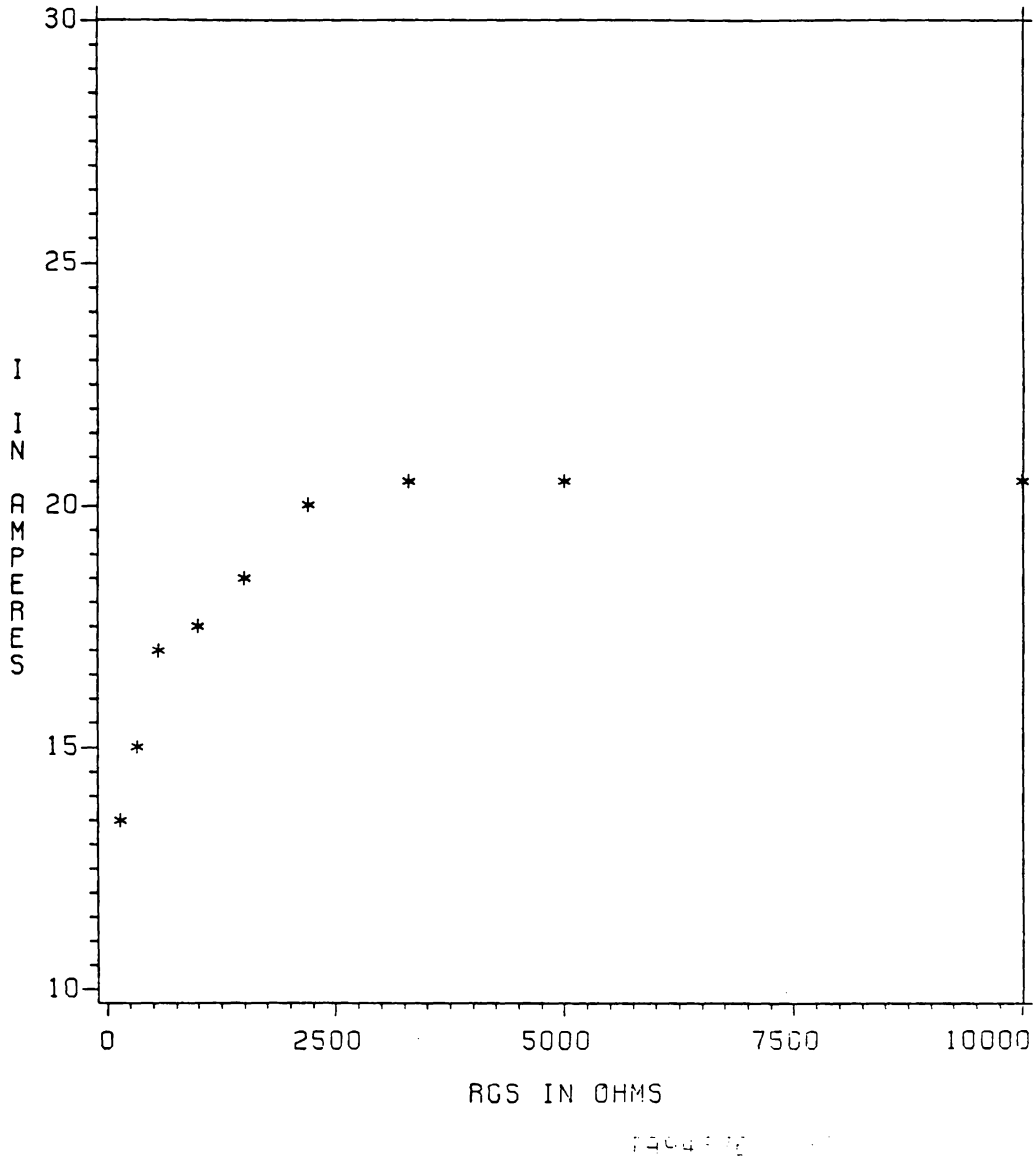


Figure 3.12.a: Variation of latch-free current in a COMFET with gate-source resistance. No snubber capacitance used.

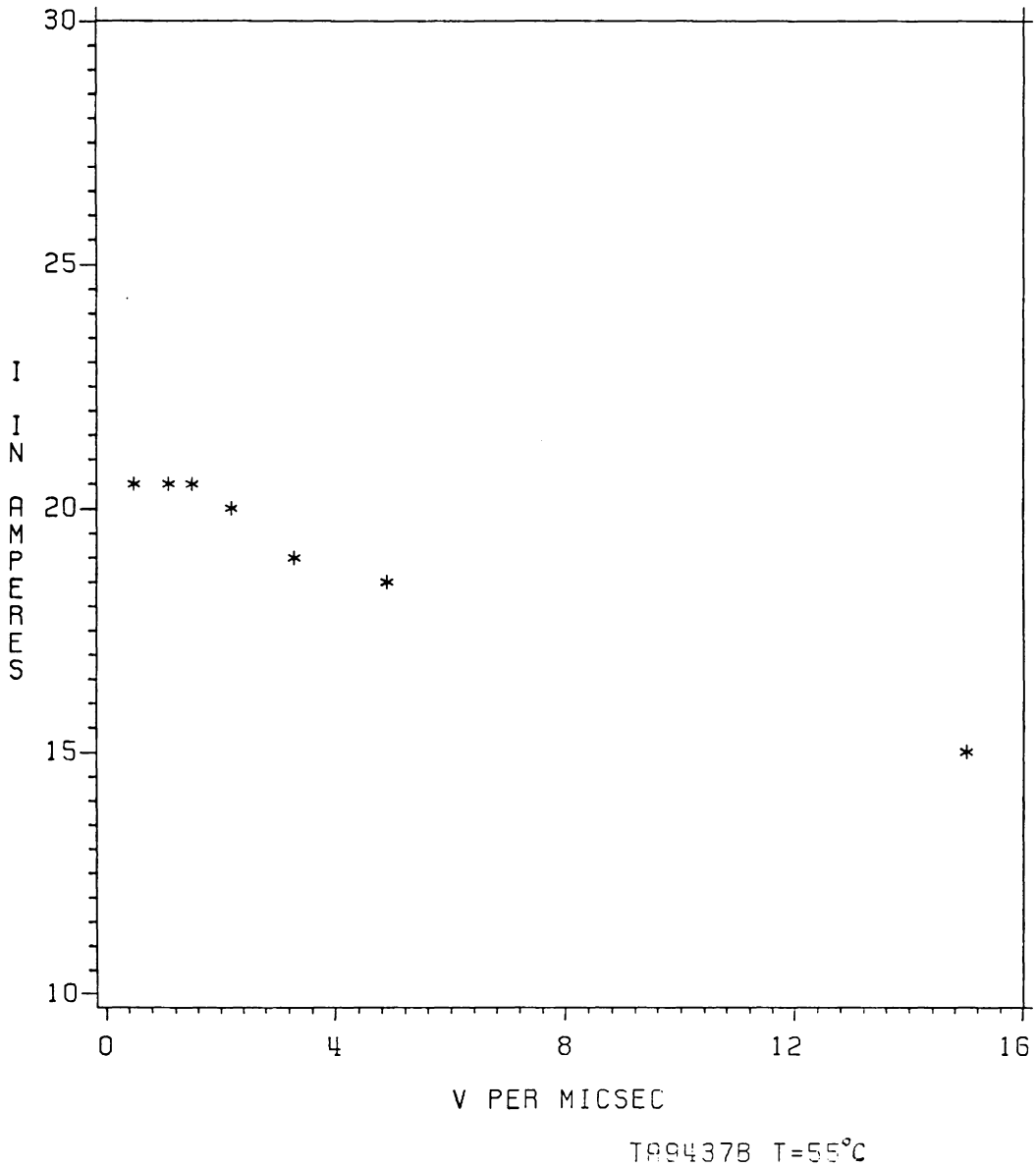


Figure 3.12.b: Variation of latch-free current in a COMFET with the rate of fall of gate-source resistance. No snubber capacitance used.

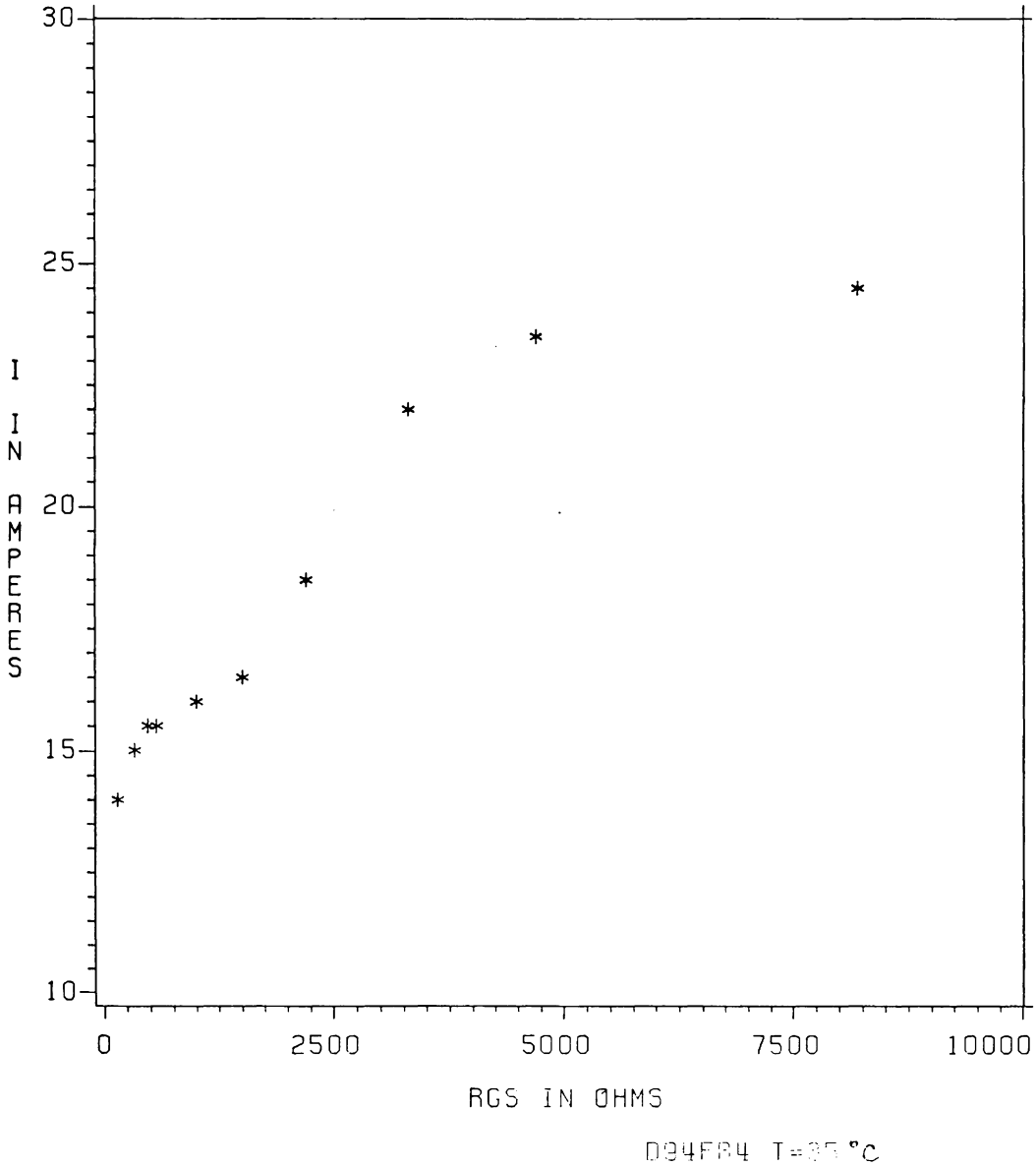


Figure 3.13.a: Variation of latch-free current in an IGT with gate-source voltage No snubber capacitance used.

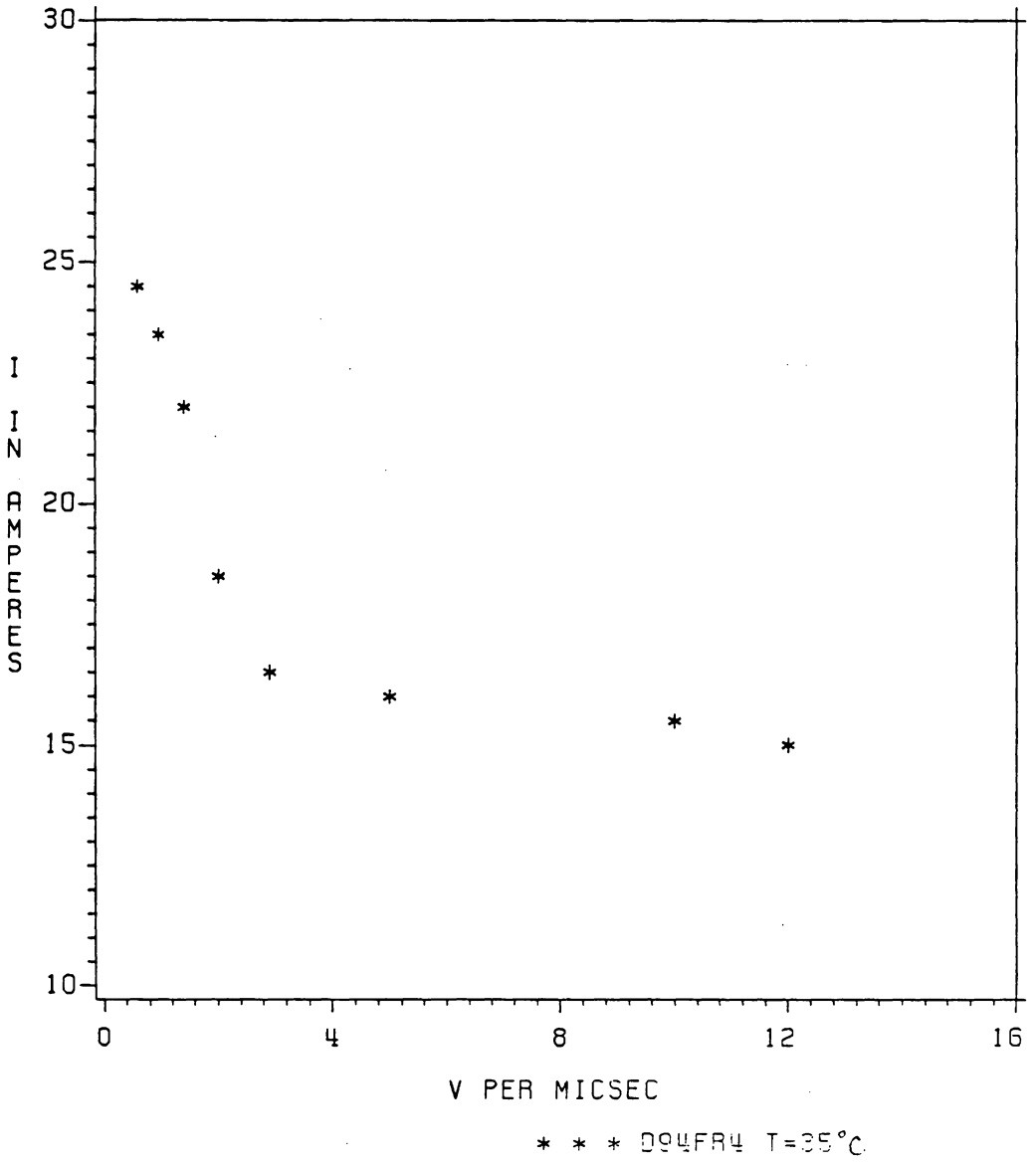


Figure 3.13.b: Variation of latch-free current in an IGT with the rate of fall of gate-source voltage . No snubber capacitance used.

the attempts by devices manufacturers to improve latch-free performance in IGTs. The IGT devices fabricated in manufacturers' laboratories in 1983 had a latching current rating of about 100 A/cm^2 [1,2]. Laboratory Devices that had latching current densities over 1000 A/ cm^2. were reported by Baliga et al. [5]. Some of the methods to decrease latching currents are described in the following sections.

3.3.1. DECREASING THE LATERAL RESISTANCE OF THE P BASE.

The method of decreasing the gain of the n-p-n transistor is the use of a shunt resistance connecting the gate and source terminals, similar to that used in a power MOSFET. Extending the metalization at the source over the p-base region is implemented with power MOSFET technology. Consider the Figures 2.1 and 2.2. Decreasing the shunt resistance would mean increasing the lateral conductance of the p-base. This allows a higher current flow in the p-base before the emitter-base junction is forward biased in excess of 0.7 V required to obtain electron injection from the emitter, which causes regenerative latchup [8]. A highly doped p- region will decrease the lateral resistance of the p-base. One disadvantage of the scheme is that the heavier the doping of the p-base the higher the threshold voltage and the smaller the width of the the inverted region. The

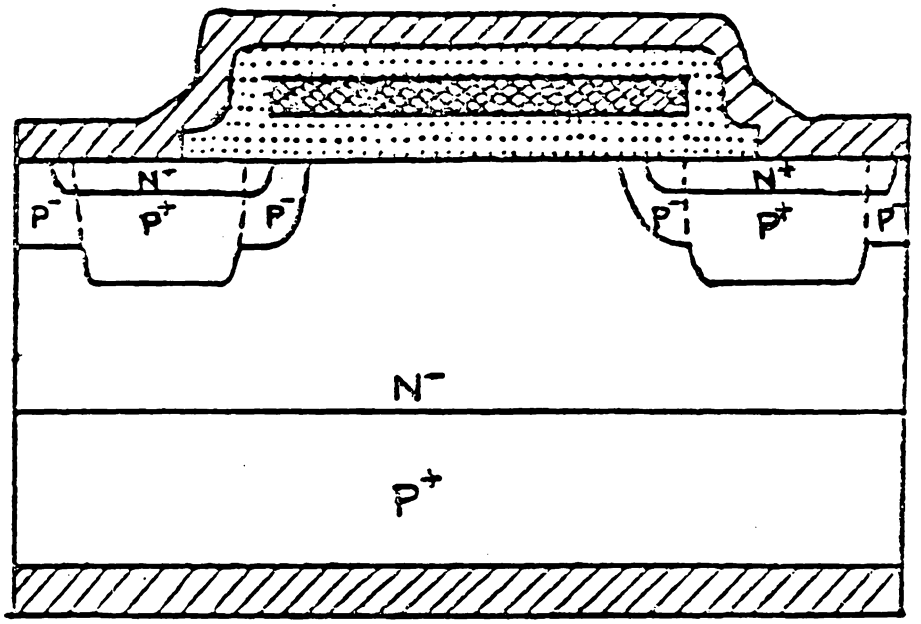
manner by which the disadvantage is overcome is explained in the following subsection.

3.3.2. THE USE OF HIGHLY DOPED P+ REGIONS IN THE P BASE.

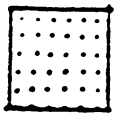
Consider the variation in the structure of the IGT shown in Figure 3.14. In order to suppress latchup of the parasitic transistor, it is necessary to increase the conductivity of the p base under the n+ source. This allows higher lateral current in the p base before the source-p base junction J3 in Figure 3.14 is forward biased in excess of 0.7 V. This is achieved by the heavily doped centers of the p base region. At the same time, the lightly doped p- regions in the extremities of the p base help keep the threshold voltage of the IGT low [8,9]. The device latching current level was found to increase by about 250% as a result of this variation in device design.

3.3.3. DECREASE OF THE LENGTH OF THE SOURCE REGION.

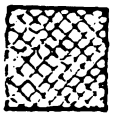
Decreasing the length of the highly doped n+ source region causes an almost linear rise in the latch-free current level [4]. By decreasing the length of the source region the value of R_{SH}, the lateral resistance of the p- base region is reduced. The current flowing into the



METAL (ALUMINUM)



DIELECTRIC (SiO_2)



POLYSILICON

Figure 3.14: The structure of an IGT with a nonuniformally doped p-base region.

parasitic n-p-n transistor is decreased, causing an increase in the latch free current level. Baliga [5] has shown that a decrease of emitter length from 30 microns to 8 microns increases the latching current density from 200 A/cm^2 to 1000 A/cm^2. Finer resolution processing results in higher latching current levels.This is one method of increasing the current latching level without compromising on the device conduction resistance.

3.3.4. DECREASE SUBSTRATE DOPING DENSITY.

The decrease in the doping density of the substrate from a p+ substrate to a p- substrate. The effect of the reduction in doping density of the starting substrate is to reduce the emitter injection efficiency and therefore the gain of the p-n-p transistor. This result was first reported by A.M.Goodman [9]. Large decreases in the substrate doping will result in a smaller number of holes injected into the p+ substrate, lesser conductivity modulation and hence higher conduction resistances. Therefore there is a limit below which we cannot decrease the doping density of the substrate.

The manner in which the circuit designer may use the data obtained on device latching is given in Section 3.6.

3.3.5. DECREASING TURN OFF TIME BY IRRADIATION.

Latching due to rapid discharge of gate-source capacitance occurs primarily because among all the paralleled cells comprising the device, if a few are turned off very rapidly, the plasma of charged carriers, especially in the turn-off time t_{f2} , causes one or two cells to lose gate control, thus starting the process of latching. In general, rapid recombination of the plasma results in lessening the likelihood of latching. Irradiation techniques developed for improving the recovery time of high current diodes have been successfully used to make IGTs with low turn-off times [10]. The low fall time is achieved at the expense of higher conduction voltage drop, but the device still has conduction voltages smaller than that of equivalent power MOSFETs having similar current densities. One interesting result of the IGT irradiation tests is that fast and slow IGTs could be made with the same device design and device frequency could be adjusted for the application.

3.3.6. OPTIMIZATION OF THE GEOMETRY OF DIFFUSED REGIONS.

It has been found that latching caused by the rate of rise of drain-source voltage is dependant on the geometry of the diffused regions. These techniques, which were first developed to combat dv/dt failure in power MOSFETs, are used

to decrease the chances of latchup due to high rate of rise of drain-source voltage.

3.4. LATCHING DURING PARALLELING OF IGTS.

The understanding of the behaviour of paralleling of power devices is important for enhanced current applications and for reliable packaging of a number of paralleled power devices.

Care should be taken during paralleling to have good thermal coupling between devices and make the leads as short and as symmetrical as possible. Gate coupling between the devices should be just large enough to prevent unnecessary gate circuit oscillations.

Experiments with paralleling showed that the most serious problem experienced is latching, especially at turn-off. Table 3.1 shows a list of all the possible causes of imbalances in IGTs and its effect on latching [11].

The variation of the IGT show that temperature coefficient of resistance is negative for current, levels up to 60% of the rated current density. Beyond this current density, the temperature coefficient is positive. A positive temperature coefficient of resistance is very useful in the paralleling of devices as this has a negative feedback effect on the static current through the paralleled devices.

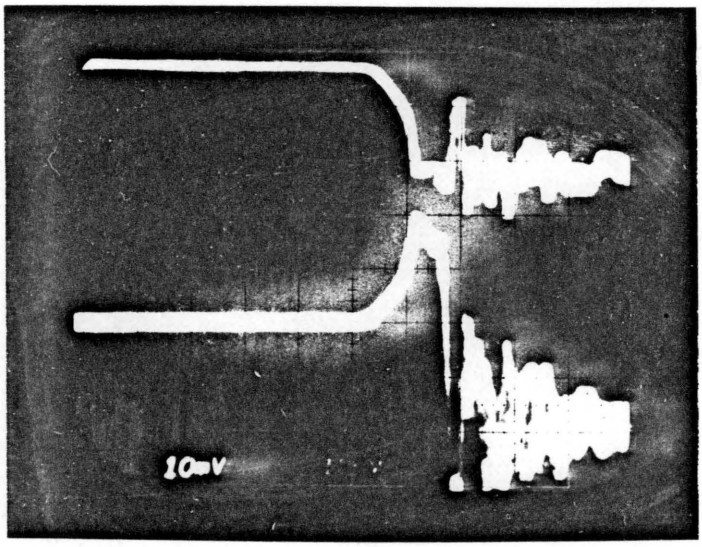
TABLE 3.1: THE EFFECT OF IMBALANCES ON LATCHING IN PARALLELED DEVICES

IMBALANCE GENERATOR	CURRENT DIFFERENTIAL	TIME OF IMBALANCE	IMPORTANCE (LATCH)
IMBALANCES DUE TO DEVICE CHARACTERISTICS.			
$V_{DS(ON)}$	STEADY STATE	CONDUCTION	MAJOR.
G_F	DYNAMIC	TURN-OFF	MINOR.
$V_{(THR)}$	DYNAMIC	TURN-OFF	MAJOR.
C_{GS}	NONE		
C_{GD}	NONE		
POWER CIRCUIT.			
L_D	DYNAMIC	TURN-OFF	MAJOR.
L_S	DYNAMIC	TURN-ON TURN-OFF	MAJOR.

IMBALANCE GENERATOR	CURRENT DIFFERENTIAL	TIME OF IMBALANCE	IMPORTANCE (LATCH)
GATE DRIVE CIRCUIT.			
R_{GG}	DYNAMIC	TURN-ON	MAJOR.
		TURN-OFF	
R_{GS}	DYNAMIC	TURN-ON	MAJOR.
		TURN-OFF	
DIODE T_{rec}	DYNAMIC		MINOR.

The major problem in paralleling devices, latching, occurs during turn-off. During the turning off of two paralleled devices, if one of the devices turns off faster than the other, then, all the current through the combination will go through the second device, tending to cause that device to latch. Once a device latches, it loses gate control and the paralleled combination ceases to operate as a switch. In a conventional power MOSFET, even though current balance may occur at turn-off, it occurs only for a short period of time (turn-off time). No latching occurs and therefore the problem of current imbalances is more serious in the IGT than in the MOSFET. Figure 3.15 shows the currents at turn off through two paralleled devices, showing a peak when one device is faster than the other.

It may be concluded that, while the very small gate drive power requirements really help us design simpler and less expensive gate drive circuits, the negative temperature coefficient of resistance, the higher switching losses and, especially the possibility of latchup are very severe disadvantages which must be overcome. However, the high current densities possible with IGTs can reduce the number of IGTs to be paralleled. The paralleling of more than two devices causes an increase in the susceptibility to latchup.



I_D 2A/div.

I_D 2A/div.

200ns /div.

FIGURE 3.15: Oscillograph showing turn off current waveforms in two paralleled devices. The devices switched are TA9437A COMFETs.

3.5. THE USE OF THE IGT IN RESONANT CONVERTERS.

The IGT is very well suited for applications requiring zero current turn-off. The device can withstand current levels up to three times its current rating without causing device damage. The IGTs latch at high current levels but a low current level restores gate control to the IGT. The IGTs commercially available today however, may not be switched at frequencies above 50 kHz since some time is required for the plasma of charge carriers in the n^--p^+ junction J1 in Figure 2.1. The value of t_q for the IGT is not specified in IGT device data sheets but this can be taken to be equal to the turn-off fall time t_{f2}. The property of the IGT to block reverse voltages may also be very useful in some resonant converter topologies.

The development of fast IGTs will make the IGT very suitable for high frequency resonant converter applications. The IGTs commercially available today are most suited for resonant applications below 10 kHz, as in welding unit power supplies and semiconductor furnace power supplies. The advent of high power, high frequency IGTs make the device very attractive for resonant converters.

3.6. INFERENCES FROM EXPERIMENTS ON LATCHING.

Several conclusions can be drawn from the experiments performed on the latching current levels. These inferences are listed in the following sections.

3.6.1. MAXIMUM CONTINUOUS CURRENT DEPENDS ON LATCHING.

The high current latching level would mean that the maximum current through the device will always depend, not on the power dissipated in the IGT but on the latching current levels.

3.6.2. DEVICE TEMPERATURE IS DOMINANT CAUSE OF LATCHING.

Device design cannot inherently alter the dependence of the device temperature on the latching current level. The effect of temperature on the latching current is greater than that of any other factor causing latching. The strong dependence of the latching current on high device temperature limit would mean that thermal design of IGT circuits is very important. This also means that the maximum device operating temperature of the IGT will be about 125°C compared to nearly 200°C for a conventional power MOSFET.

3.6.3. THE EFFECT OF RATE OF RISE OF DRAIN-SOURCE VOLTAGE.

From a user's point of view the high rate of rise of drain source voltage latching would mean that snubbers may be used to increase the latch-free operating current. It is hoped that the next generation of IGTs will have their susceptibility to the rate of rise of drain-source voltage greatly reduced by better device design.

3.6.4. THE EFFECT OF RATE OF FALL OF GATE-SOURCE VOLTAGE.

A gate-source turn-off resistance of at least 500Ω is recommended to prevent device latching. This problem was found to be a much more serious in the slower devices than in the faster devices.

3.6.5. DIFFICULTIES IN PARALLELING.

The negative and positive temperature coefficients of resistance mean that if we allow for the factor of safety applied by the user to select a device, the device will have a negative temperature coefficient of resistance. Thus the major advantage in paralleling enjoyed by power MOSFETs is absent in IGTs. Device paralleling in IGTs is is rather difficult with latching being the major problem.

3.6.6. SUITABILITY FOR HIGH FREQUENCY RESONANT CIRCUITS.

Fast switching IGTs are very well suited for handling high peak currents and have a lower conduction resistance than the power MOSFET. The time necessary for the plasma to recombine would mean that high frequency resonant circuits are difficult with most of the IGTs of today. The IGT is very well suited for low frequency applications that require natural commutation.

3.6.7. THE TRADEOFF BETWEEN FALL TIME AND LATCHING CURRENT.

The value of the gate-source resistance chosen represents a tradeoff between the device fall time and the current latching level. A high gate source resistance will mean large fall times and consequently increased turn-off losses.

A very low turn-off gate resistance in an IGT results, not only in dv/dt latching, but also in higher gate currents. The IGTs available today show fall times between 1 and 12 μs. The second generation of faster IGTs devices may be commercially available soon and these fast switching IGTs could be used up to 50 kHz [12]. However, most motor control applications do not require switching above 20 kHz and turn-off times of around 0.5 μs and latch-free operation at 1.5 times the rated current upto 150°C are suitable.

CHAPTER IV.

GATE DRIVE CIRCUITRY FOR THE IGT.

In this chapter the gate drive circuitry used to drive the IGT is discussed in detail. The chapter is divided into three sections. The first section, Section 4.1 describes the constraints and the features unique to IGT gate drive circuits. Section 4.2 discusses the operation of and part selection for the optically isolated IGT gate drive circuits developed for use in bridge circuits. The experimental results for the circuits are given in Section 4.3.

4.1. GATE CIRCUIT FEATURES AND DESIGN CONSTRAINTS.

The drive circuit of the IGT must have the following features:

1) It must deliver a positive voltage of +10V to +15V during the on-state of the IGT for turning the device on.

2) The gate-source voltage during the off state need be zero volts. Reverse biasing the IGT may be necessary in very noisy environments to prevent false triggering.

3) The turn-off time of the gate circuit must be small enough to avoid large turn-off losses, but, at the same time, this cannot be too fast, since the latching current

level reduces as the turn-off time is reduced, as described in the previous chapter. Therefore there exists a trade-off in determining the turn-off resistance of the gate circuit.

4) Significant dead time must be provided in the gate drive circuitry in certain power circuits like the bridge inverter where overlap conduction must be avoided.

5) The IGT requires a large gate-source resistance to prevent device latchup. This means that the device gate cannot be easily held at a reverse voltage during the forward blocking mode in order to prevent false triggering. The IGT is susceptible to noise because of the large turn-off resistances.

In addition, a few of the important IGT gate drive design aspects are listed in the following sections.

4.1.1. NEED FOR DIFFERING TURN ON AND TURN OFF RESISTANCES.

Care should be taken in the design of IGT gate drive circuits to avoid device latching. The IGT can, like the power MOSFET, be turned on in a few tenths of a microsecond. The turn-off of the IGT however, should be slow. Fast turn-off of the device results in latching of the power IGT, as explained in Chapter III. The resulting loss of gate control is very critical especially in motor control and

other totempole configurations. Consider the Figure 4.1. The turn-on impedance of the gate drive circuit, R_{GG}, must be low but the turn-off impedance as seen by the device, R_{GS}, must be high enough to prevent latching. Two types of drive systems were used in order to evaluate the drive system best suited for the three phase bridge.

4.1.2. SUSCEPTIBILITY TO DAMAGE BY STATIC.

The small gate capacitance of the IGT would mean that the device is more sensitive to damage due to electrostatic charge stored at the gate terminal. External gate-source resistances of under 50 kΩ can be used to avoid gate oxide damage.

4.2. ISOLATED GATE DRIVE CIRCUIT IMPLEMENTATION.

Two isolated gate drive circuits were built for IGTs in a totempole configuration. The two circuits differed only in the voltage and power output levels and hence the components selected. The two gate circuits are shown in Figures 4.2 and 4.3.

The aim of the gate drive design was to keep the drive circuitry as simple and inexpensive as possible. Consequently it was decided to incorporate a gate drive without drain-source voltage sensing. In addition it is

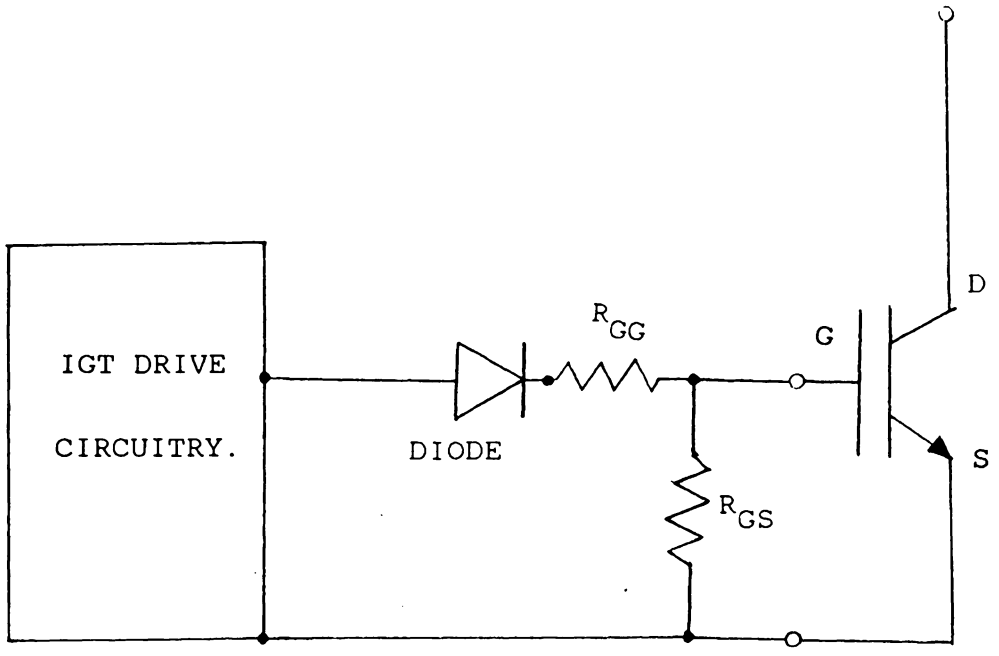


Figure 4.1: Diagram showing the differing IGT turn on and turn off resistance. R_{GG} shows the turn on resistance and R_{GS} the turn off resistance.

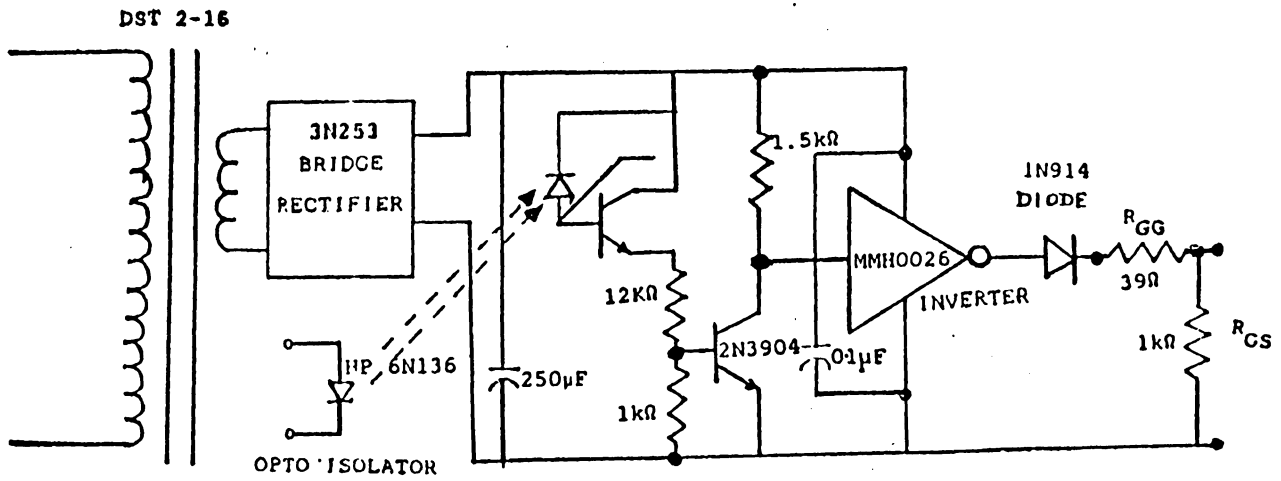


Figure 4.2: Circuit diagram of an IGT gate drive used in the three phase bridge inverter.

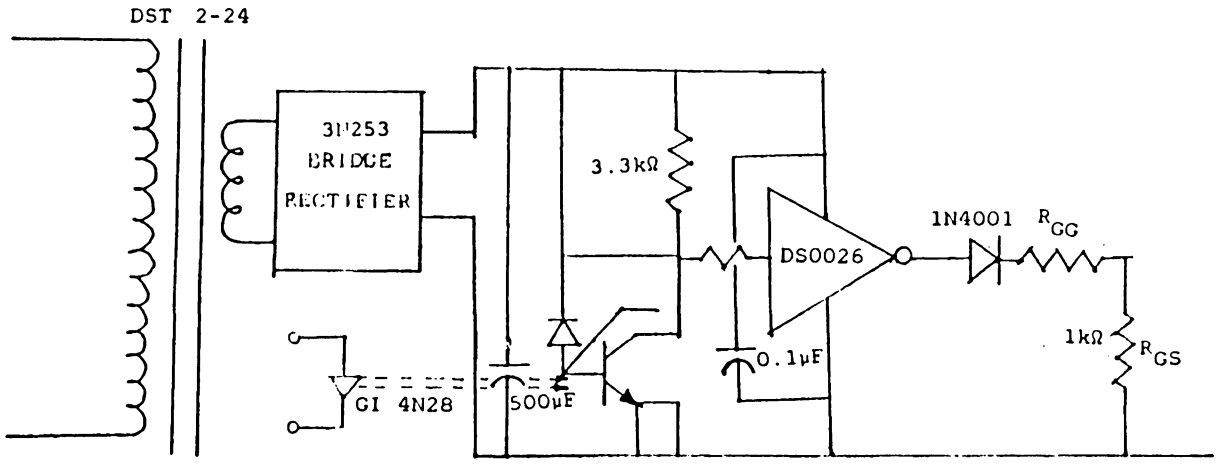


Figure 4.3: Circuit diagram of a higher voltage gate drive circuit used in the three phase bridge inverter.

necessary to make the drive circuitry fail safe so that no IGT can be turned on in case there is a time difference between the turning on of the gate drive power supply and the logic power supply.

The operation of the gate drive circuit is explained in Subsection 4.2.1 and Subsection 4.2.2 discusses the selection of components.

4.2.1. OPERATION OF THE GATE DRIVE CIRCUIT.

Since the two circuits of Figures 4.2 and 4.3 operate in a similar fashion, the operation of the circuit in Figure 4.2 alone will be discussed in Subsection 4.2.1. The method of operation of the circuit of Figure 4.3 is as follows:

When no current flows through the input diode of the optical isolator, the voltage at the collector of the output transistor in the optical isolator remains at the supply voltage. The voltage at the input to the MMH0026 chip is high and therefore the output of the driver chip is held low. No current flows through the diode to charge the input capacitance of the IGT. No IGT gate-source voltage is impressed and the IGT is in its off state.

When the output of the logic circuitry is pulled low, current flows through the input diode of the optical isolator. The light emitted from the LED in the optical

isolator provides the base current in the photo-transistor turning the device on. The collector voltage of the optical isolator falls from around 15V to less than 1V. This forces the input to the clock driver chip low and hence the output of the MMH0026 is high. The gate-source voltage of the IGT is about +15V.

At the time of the turn-off, the diode prevents the gate capacitance of the IGT from discharging through the MMH0026 chip. The discharge of the gate capacitance is through the gate source resistance R_{GS}.

4.2.2. COMPONENT SELECTION.

The gate drive circuit shown in Figures 4.2 and 4.3 can be divided into six parts: the gate power supply circuit, the opto-coupler, interface circuitry, driver chip, the small signal diode and the gate resistances. In addition, the In addition, an alternative for the driver chip is also discussed.

4.2.2.1. GATE POWER SUPPLY.

Inexpensive center-tapped (Signal Transformer DST 2-16 and DST 2-24) transformers are used with primaries in series and secondaries in parallel. The continuous current rating of the transformer secondaries is 90mA. The bridge rectifier

used is the popular MDA 200 (3N253) chip.

4.2.2.2. OPTICAL ISOLATOR.

The optical isolator used in Figure 4.2, the HP 6N136 is an unshielded Gallium Arsenide transistor output device. It has a bandwidth of 2 MHz and a dc current transfer ratio of 19%. The optical isolator chosen for the circuit in Figure 4.3 is the GI 4N28. This opto-coupler is less expensive and has an output transistor with a collector current rating of 100mA and a V_{CE} rating of 30V. The GI 4N28 is a slower device than the HP 6N136.

4.2.2.3. INTERFACE CIRCUIT.

The interface circuit connecting the output of the optical isolator to the inverting buffer in Figure 4.2 consists of a 2N3904 signal level transistor and appropriate resistances. Careful selection of the voltage divider resistors reduces the fall time at the collector of the 2N3904 transistor to less than 0.3 μs. The delay time introduced in the circuit, which is around 2 μs, is not of much importance.

The circuit of Figure 4.3 does not need any interface circuitry. No interface circuitry is needed if the CD4050 (or CD4049) chip is used to drive the IGT.

4.2.2.4. USE OF THE MMH0026 DRIVER CHIP.

The MMH0026 clock driver chosen is a powerful bipolar driver which can output up to 1.5 A of current [13]. The fall times at the output of this inverting buffer integrated circuit are less than 0.3 μs. A 0.1 μF capacitor is used to keep the supply voltage to the inverting buffer constant. An alternate choice of a driver chip is given below.

4.2.2.5. USE OF A CD 4050 DRIVER CHIP.

The small input capacitance of the IGT would mean that many inexpensive and readily available integrated circuit driver chips may be used to drive the power IGT. The high threshold voltage means that the driver chips would have to be a high voltage CMOS (CD 4000 series) integrated circuit chip.

All the six gates of the 4049 chip are paralleled for the highest possible power rating. It should be noted that the output current levels of the CD 4000 series is a strong function of the dc supply voltage (V_{DD}-V_{SS}). The driver chip must therefore be driven as close to the +15V rails as possible so as to maximize gate current and thus decrease turn-on time. The rated maximum output currents possible with the CMOS buffer chips is only around 200mA [14]. The

predominantly low frequency use of the IGT would mean that the turn-on rise time of the IGT is not critical. Thus for many applications, the CD 4049/4050 signal level buffer chip may be sufficient to drive the power IGT.

4.2.2.6. DIODE FOR DECOUPLING TURN OFF CIRCUIT.

The small signal diode used decouples the drive circuit during the turn-off period of the device [2]. The diode used in the circuit of Figure 4.2 is a 1N914 small signal diode. The 1N4001 diode used in Figure 4.3. has a a higher power rating than the 1N914. The diode causes a voltage drop of about 0.8V.

4.2.2.7. THE GATE RESISTANCES.

By using a gate-source resistance R_{GS} and the diode we may slow down the rate of fall of gate-source voltage. An alternate value for the gate-source resistance for MGM20N50 GEMFETs is 3.3 KΩ. The resulting increase in fall time is small but the dead time separating the conduction times between two devices in totempole configuration must be increased to at least 75 μs.

The larger turn-on gate resistance of 56Ω in Figure 4.3 is used in order to decrease oscillations from the larger input capacitances of IGTs with higher current

ratings.

4.3. RESULTS AND OBSERVATIONS.

Photographs of the two boards implementing the isolated gate drive circuits shown in Figures 4.2 and 4.3 are shown in Figures 4.4 and 4.5 respectively. For the circuit of Figure 4.3, the variation in the rate of fall of gate-source voltage caused by the diode can be seen in Figure 4.6. While the voltage at the output of the MMH0026 driver chip falls from 15V to 0V in about 50 ns, the rate of fall of the voltage at the gate is greater than 1 μs.

Consider the oscillographs shown in Figure 4.7. These demonstrate the effect of various values of the gate resistance R_{GG} of Figure 4.3, when the gate of the IGT is impressed with a voltage V_{GS} of 15V. Figure 4.7.a shows that with an R_{GG} of 56Ω we have an overdamped system with no oscillations. Figure 4.7.b shows that if the gate resistance is 39Ω, the maximum gate voltage just stays at 15V. Figure 4.7.c shows that if the gate resistance is reduced to 10Ω, the oscillations in the gate voltage reach up to 19 V. A lower value of the gate resistance was found to destroy the GEMFET. Values of the gate resistance R_{GG} between 30Ω and 50Ω, while adding little to the gate resistance, help decrease the rate of rise of gate-source

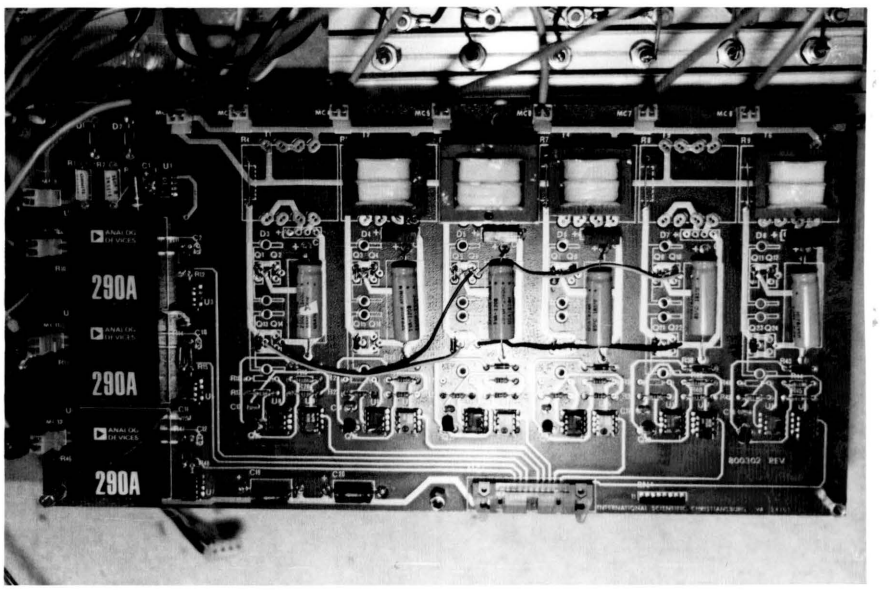


Figure 4.4: Photograph of the gate drive circuit board implementing the circuit of Figure 4.2. The printed circuit board contains six gate drive circuits and the current feedback circuitry for the three phases.

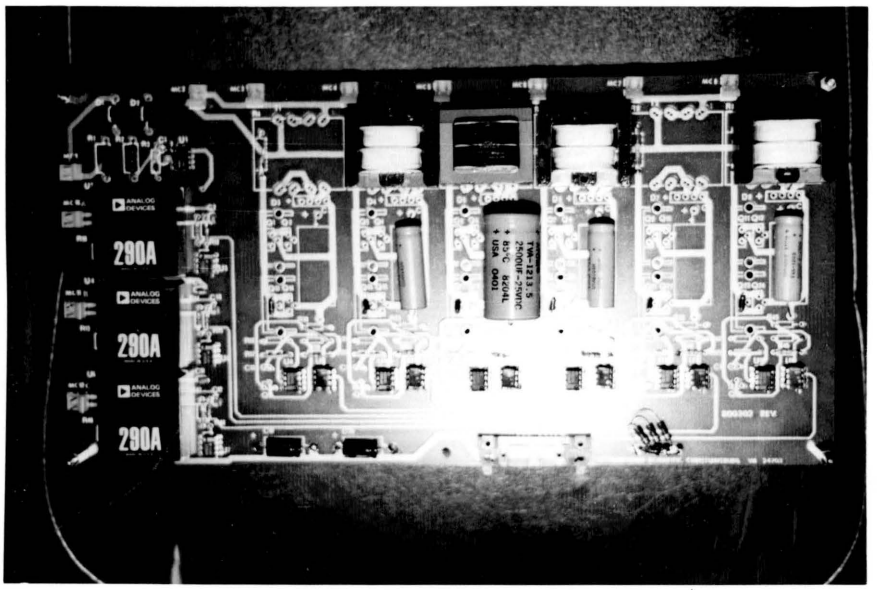
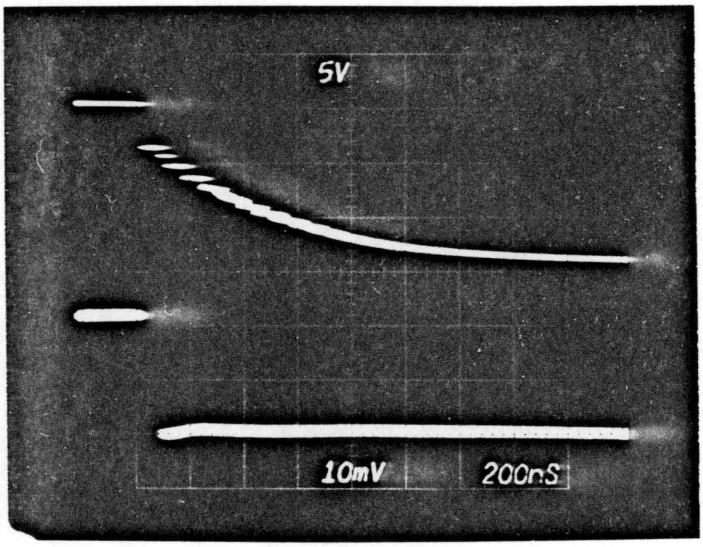


Figure 4.5: Photograph of the gate drive circuit board implementing the circuit of Figure 4.3. The printed circuit board contains six gate drive circuits and the current feedback circuitry for the three phases.

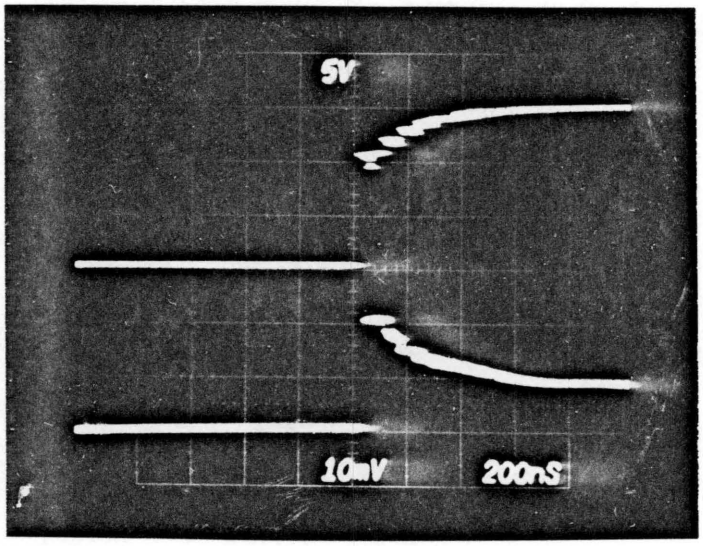


V_{GS} 5V/div.

I_{DR} 20mA/div.

200ns /div.

Figure 4.6: Oscillograph showing the effect of the diode and a gate-source resistance of 1KΩ on the fall of gate voltage. The lower waveform shows the current output by the MMH0026 driver. The IGT switching is an RCA TA9437B device.

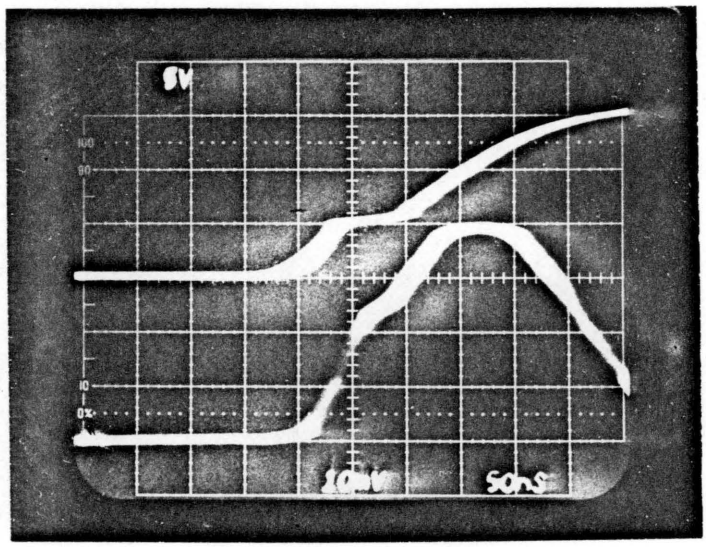


V_{GS} 5V/div.

I_G 50mA/div.

200ns /div.

Figure 4.7.a: Oscillograph showing gate waveforms when a turn on gate resistance of 56Ω is used. The device switched is a TA9437A COMFET.

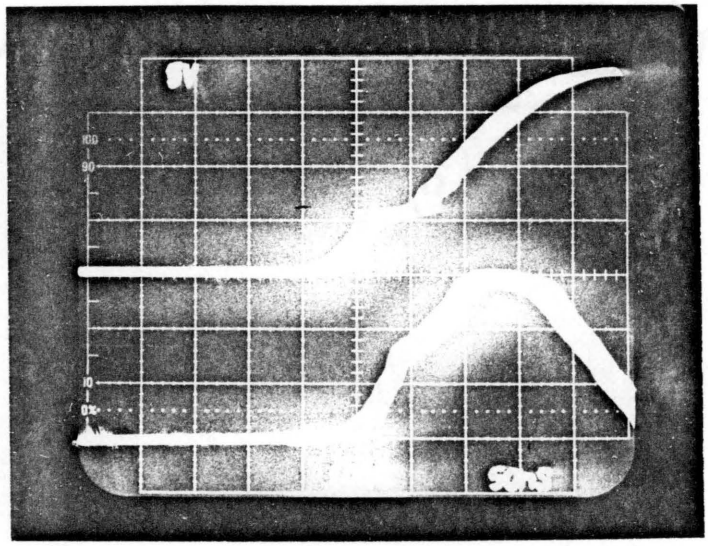


V_{GS} 5V/div.

I_G 50mA/div.

50ns /div.

Figure 4.7.b: Oscillograph showing gate waveforms when a turn on gate resistance of 39Ω is used. The device switched is a TA9437A COMFET.



V_{GS} 5V/div.

I_G 50mA/div.

50ns /div.

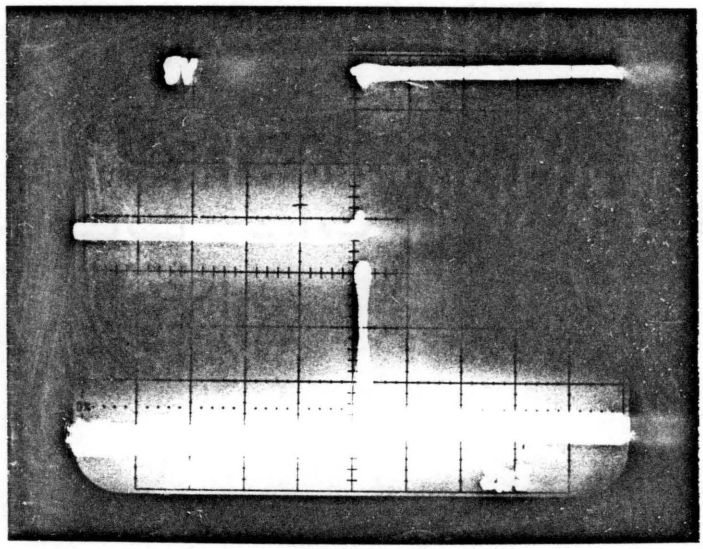
Figure 4.7.c: Oscillograph showing gate waveforms when a turn on gate resistance of 10 ohms is used.

Note: The device switched is a TA9437A COMFET.

voltage.

One interesting observation that can be made from Figures 4.7.b and 4.7.c. is that the input capacitance of the IGT is not constant but varies like that of the power MOSFET, resulting in the flat portion of the gate voltage seen in upper trace of Figures 4.7.b and 4.7.c [15]. Figure 4.8 shows the gate voltage and current waveforms when the IGT is driven by a CD 4049 CMOS inverting buffer integrated circuit chip.

The gate drive circuit of the IGT been shown to be very simple and inexpensive. However, care should be taken to minimize the chances of latchup. The small drive requirements of the IGT makes the device uniquely suited for gate drive integration. The gate drive circuit was successfully used to drive a three phase bridge inverter in a motor drive circuit as will be discussed in the following chapter.



V_{GS} 5V/div.

I_G 50mA/div.

2µs /div.

Figure 4.8: Oscillograph showing gate waveforms when a CD 4049 is used to drive a TA 9437A COMFET.

CHAPTER V

MOTOR DRIVE CIRCUIT USING INSULATED GATE TRANSISTORS.

IGTs were used to build a three phase bridge inverter controlling a permanent magnet brushless dc motor. This chapter provides a detailed description of the three phase bridge amplifier used. Section 5.1 discusses the advantages of the IGT for motor control applications. A description of the inverter circuit built is given in Section 5.2. Section 5.3 discusses the experimental results and observations made from the motor control system of Section 5.2.

5.1. EVALUATION OF THE IGT FOR MOTOR CONTROL APPLICATIONS.

The advantages that make the IGT suitable for motor control are given below in subsection 5.1.1. while the disadvantages of the IGT are listed in subsection 5.1.2.

5.1.1. ADVANTAGES OF THE IGT.

1) VERY SIMPLE GATE DRIVE CIRCUITRY.

The drive circuitry for the IGT was shown in Chapter IV to be very simple and inexpensive. The smaller chip area of the IGT means that the input capacitance of the device is significantly smaller than that of an equivalent power

MOSFET. The input current necessary at device turn-on is reduced. Therefore the gate drive circuitry can be very simple.

2) LOW CONDUCTION LOSSES.

Because of conductivity modulation in the lightly doped n^- region, the voltage drop in an IGT is significantly smaller than that in a power MOSFET. The increase in the voltage drop in an IGT at high temperatures is less than that in a corresponding power MOSFET.

3) LOW DEVICE COST.

The chip area of the IGT is about one fourth of that of a power MOSFET of similar ratings. This translates to lower cost per device and also better yields per processed wafer.The simplicity of the gate drive circuit will also result in additional savings.

5.1.2. DISADVANTAGES OF THE IGT.

1) SUSCEPTIBILITY TO LATCH.

Most motor control applications need high starting currents. The tendency of the IGT to latch at high current levels is a severe disadvantage,which gets worse at high temperatures. The IGT has inherently a large surge current

capability since the conduction mode of the IGT is similar to that of a diode. Were it not for the possibility of latching, the device would be ideal for motor control, because large surge current capability is normally required in a motor drive circuit. Future research should overcome the latching problem and enhance the surge current capability of the IGT.

2) SLOW DEVICE TURN-OFF.

The long turn-off times of the power IGT result in large switching power losses. The switching frequencies used in motor control are, in general, low. Therefore this is not a serious problem.

3) NO INHERENT FEEDBACK DIODE.

The structure of the IGT prevents reverse conduction. Difficulties in packaging are a disadvantage to incorporating a discrete anti-parallel diode in the package.

The power losses at various frequencies for a slow IGT (D94FR4), a fast IGT (TA9437B), and a common power MOSFET are compared in Table 5.1. From Table 5.1 we may conclude that a fast IGT is best suited for uses below about 20 kHz and for use at high duty cycles.The IGT is therefore well suited for motor control applications.

TABLE 5.1: COMPARISON OF TOTAL POWER LOSSES

BETWEEN AN IGT AND A MOSFET OF SIMILAR RATINGS.

FREQUENCY (Hz.)	FAST IGT RCA TA9437B (Watts)	MOSFET IRF 352 (Watts)
0	10.000	20.000
100	10.114	20.017
250	10.285	20.043
500	10.570	20.085
750	10.854	20.128
1000	11.139	20.170
1500	11.709	20.255
2500	12.848	20.425
3000	13.417	20.510
5000	15.695	20.850

FREQUENCY	FAST IGT RCA TA9437B	MOSFET IRF 352
7500	18.543	21.275
10000	21.390	21.700
11000	23.668	21.870
12000	27.085	21.700
15000	27.085	22.040
20000	32.780	23.400

	FAST IGT RCA TA9437B	MOSFET IRF 352
CHIP AREA	$0.09cm^2$	$0.36cm^2$

Note: Duty cycle was assumed to be 50%. Losses during device off time were equal and small enough to be neglected. The calculations are for a device switching 340V and 10A at 25 degrees Celsius.

5.2. THE THREE PHASE BRIDGE INVERTER CIRCUIT.

Figure 5.1 shows the circuit diagram for a commonly used three phase bridge inverter for motor drive applications. The six power switching devices used were MGM 20N50 GEMFETs. The input voltage is 340V DC and the load is a three phase permanent magnet brushless dc motor. The feedback resistances, R_S, are used to control the current in the motor.

Subsection 5.2.1 discusses some aspects of the control circuit used to drive the bridge inverter. Subsection 5.2.2 describes the power circuit.

5.2.1. THE CONTROL CIRCUITRY.

A comprehensive description of the control circuitry used is beyond the scope of this thesis. A brief explanation of the important aspects is presented with the help of the diagram of Figure 5.2 [16]. Voltage across the current sampling resistor R_S passes through isolation and inverting buffer amplifiers and is added to a sine wave request generated by a PROM. The resulting wave is converted into pulses. The anti-coincidence circuitry introduces a dead time to prevent overlap of the conduction time between two IGTs. A short description of the pwm and the dead time

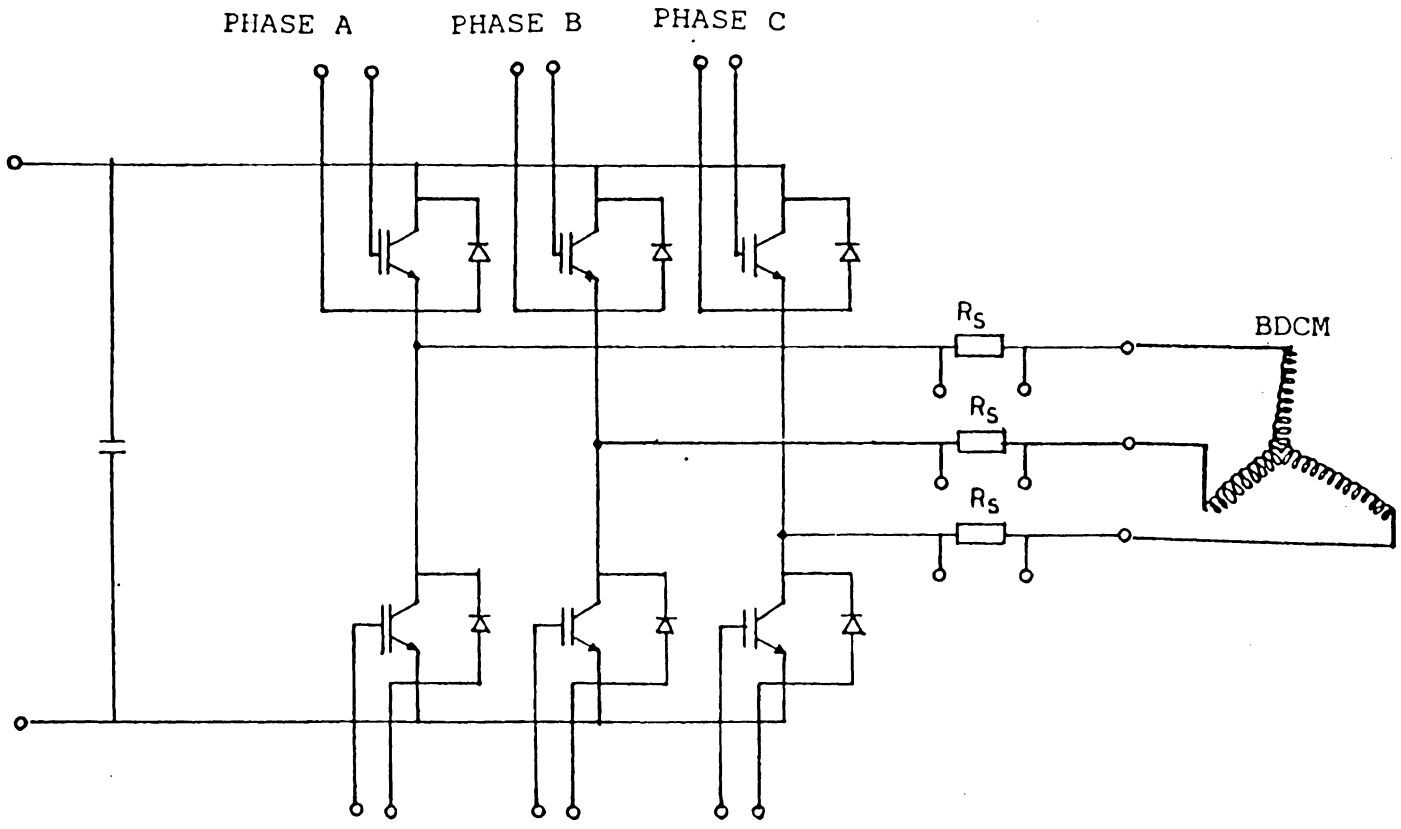


Figure 5.1: A circuit diagram of the GEMFET based three phase bridge used to drive a brushless dc motor.

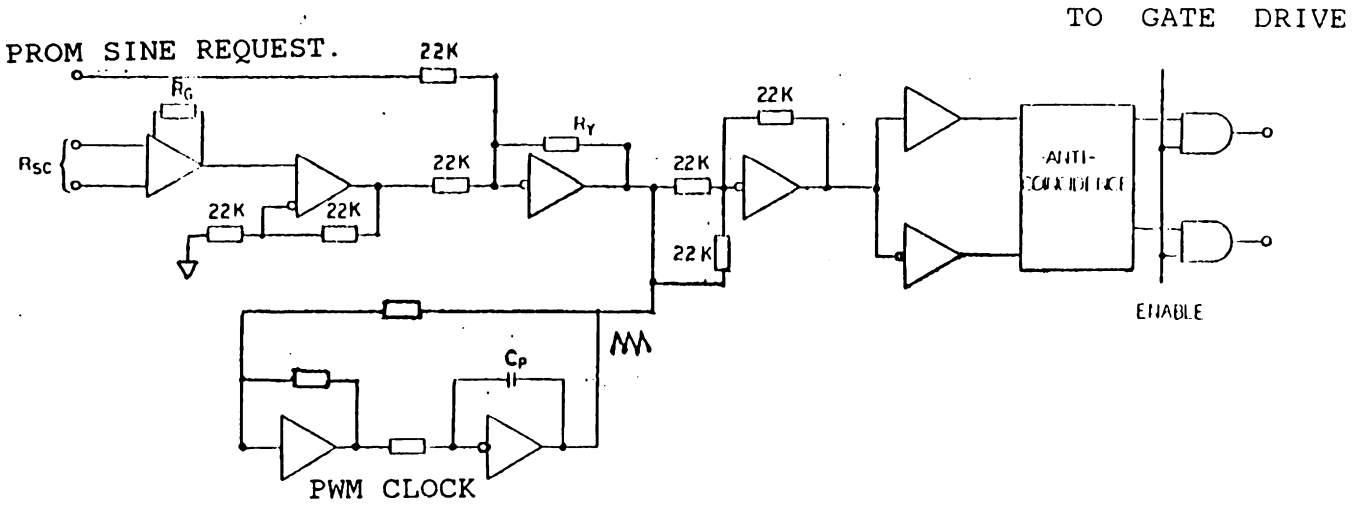


Figure 5.2: A simplified schematic of the logic circuit used for pwm control of a brushless dc motor.

circuits is given below.

5.2.1.1. THE PWM SCHEME.

The principle of operation of the pulse width modulation scheme, as applied to two devices in a totempole configuration is shown in Figure 5.3. The amplitude of the resultant sine wave is proportional to the width and the phase of the pulses. In the scheme implemented, the number of pulses per half cycle is fixed, with the width of these pulses varying. The frequency of the pulse width modulator clock was reduced to 2.5 kHz because higher frequencies tended to cause excessive device heating in the IGT.

5.2.1.2. DEAD TIME IMPLEMENTATION.

The storage and the large fall times of the GEMFET devices, especially at high temperatures, and the susceptibility of the IGT to latch necessitates a very conservative choice of the dead time between the switching off of one IGT in a totempole and the turn-on of the other device. The dead time is digitally implemented with a high frequency clock and a storage flip-flop. The dead time used in the circuit implemented was about 52 μs. One consequence of a large dead times is cross-over distortion in the current waveform.

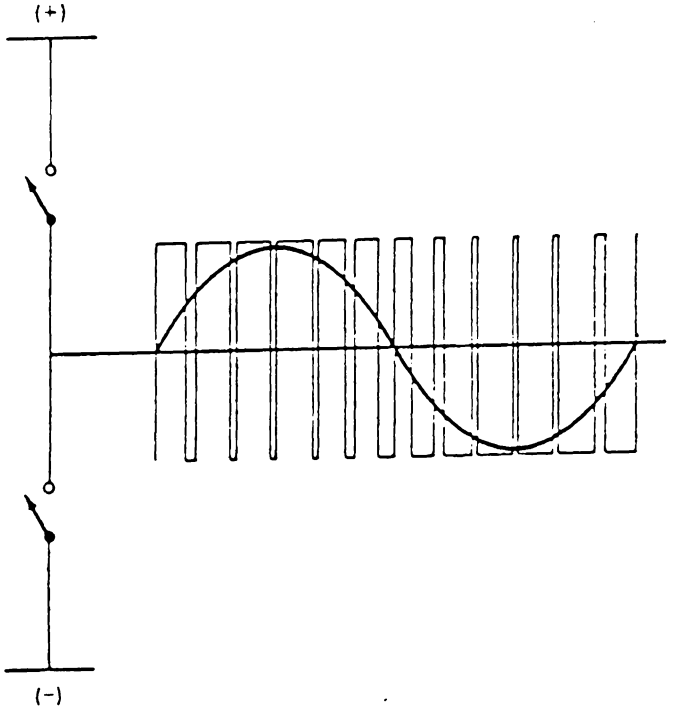


Figure 5.3: Diagram showing the pulse width modulated switching of two devices in a totempole configuration.

5.2.2. THE POWER CIRCUIT.

Two parts of the power circuit shown in Figure 5.1 will be discussed in this section - the reasons for not using the snubber circuits and the anti-parallel diodes used.

No snubbers were used in the power circuit since they increase size, parts count and cost. There also exists the possibility of interaction between the snubber circuit and the switching IGT. As a result of snubberless operation, the MGM20N50 GEMFETs had to be derated so that the maximum current through each device was 10 A.

When a power IGT switches highly inductive currents, as in motor circuits, the collapsing magnetic field induces a counter emf that could exceed the breakdown voltage of the power IGT. In order to avoid this situation, fast recovery diodes are used between device source and drain, providing a path for the inductive current to flow in the opposite direction. The diodes used were 600 V, 15 A IRF 16FL60S02 Fast Recovery Diodes with a recovery time of 200 nanoseconds. The GEMFET can withstand reverse voltages of over 50V during the recovery time of the Fast Recovery Diodes.

5.3. RESULTS AND OBSERVATIONS.

Figure 5.4 is a photograph of the GEMFET three phase bridge circuit shown in Figure 5.1. The six GEMFET devices comprising three totempole circuits were placed in line on an aluminum heat sink of thickness 0.25 inches. The steady state device temperature for the motor running under a light load with the supply voltage at 340V was recorded at 42°C.

The photograph of Figure 5.5 shows the entire IGT motor drive system developed. The foreground shows from left to right, the bridge inverter, the current feedback resistors and the input filter capacitance. The printed circuit boards seen are the logic board and the gate drive board below it. The logic power supply is seen in the background to the right.

5.3.1. MOTOR CURRENTS.

In order to test the power circuit alone, a three phase PROM based sine wave generator was used to generate the current request. The current request voltage and the current per phase are shown in Figure 5.6. The twelve pole motor used had an inductance of 5.8 mH per phase and a resistance of 2.1 Ω per phase.

Two observations are made about the motor currents. The phase current is not perfectly sinusoidal. The

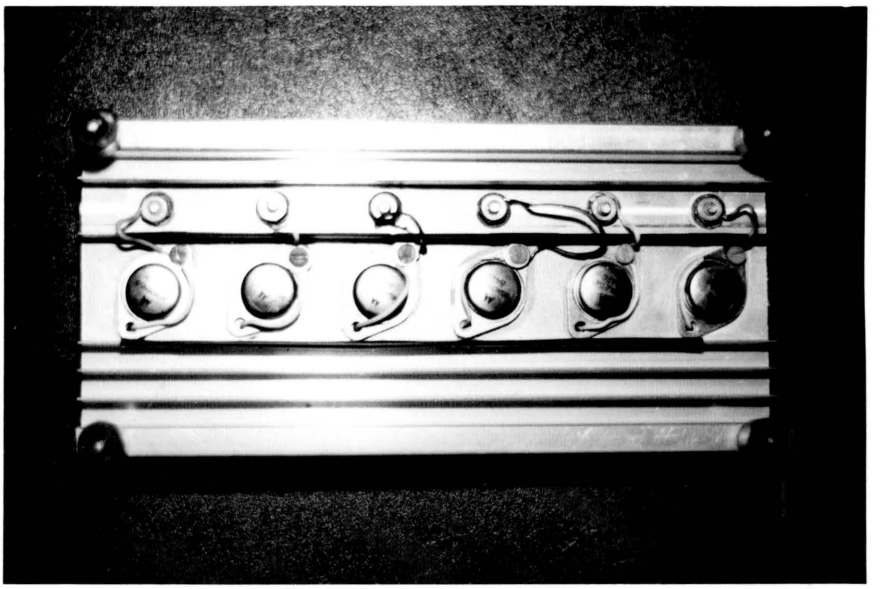


Figure 5.4.a: Photograph of the power circuit of the IGT motor control system.

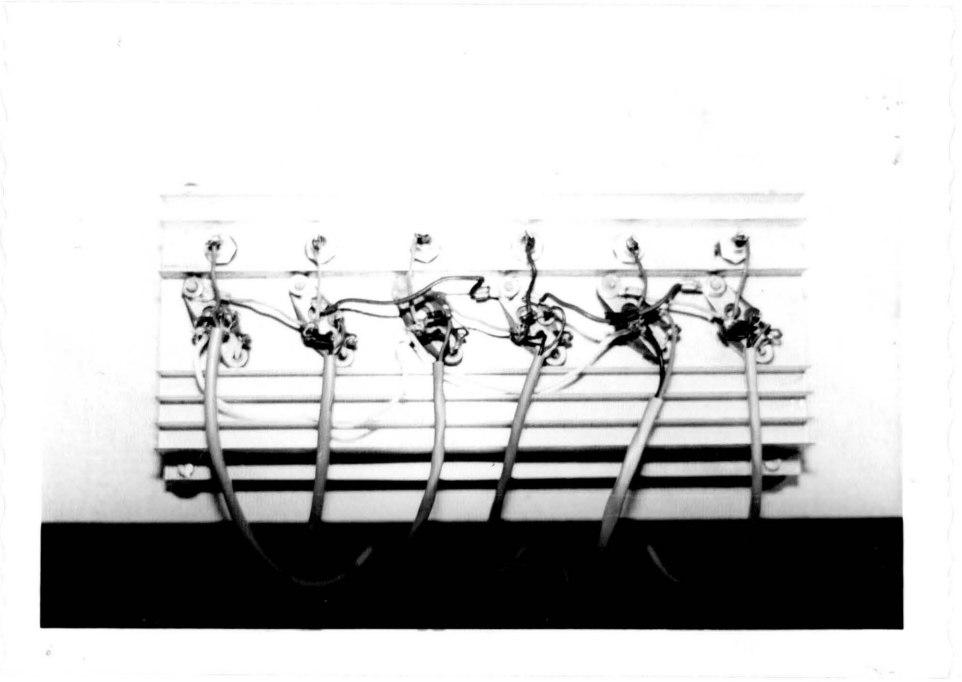


Figure 5.4.b: Photograph of the power circuit of the IGT motor control system.

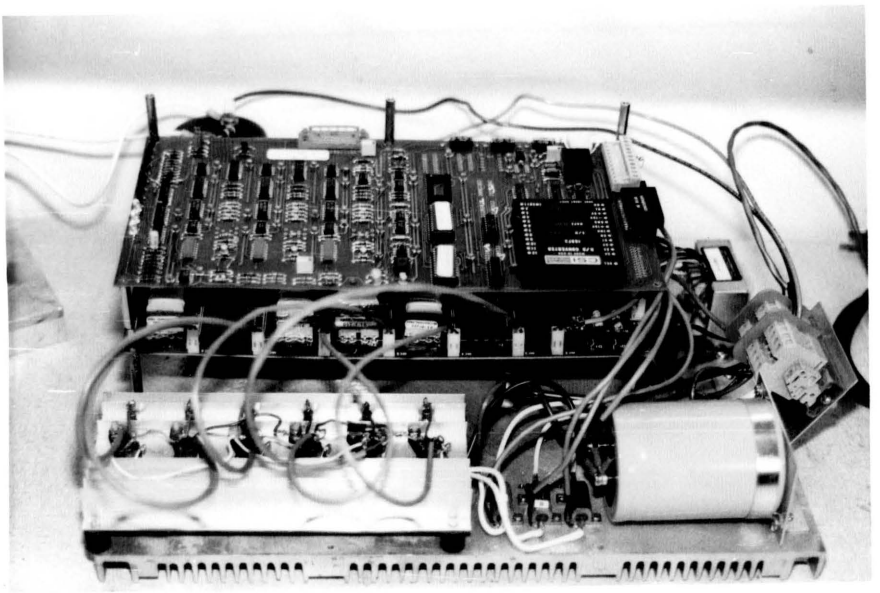
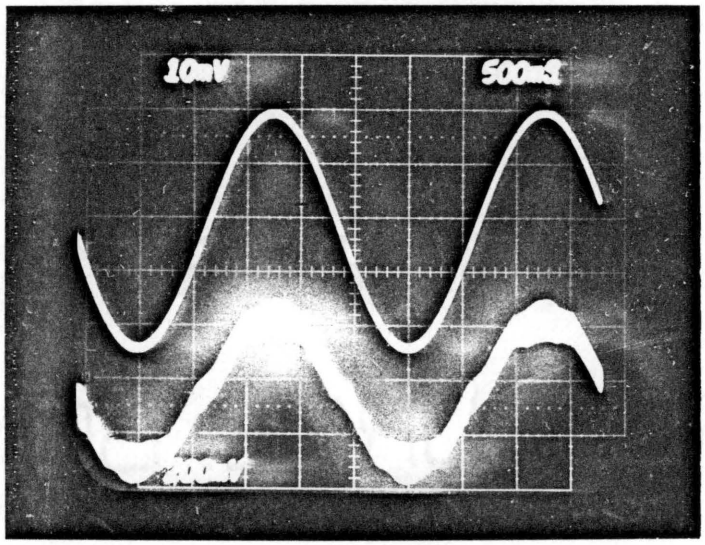


Figure 5.5: Photograph of the IGT based pwm motor control system.



I_{req} 2V/div.

I_{ph} 1A/div.

500 ms/div.

Figure 5.6: Oscillograph showing current requested and current per phase in the three phase GEMFET bridge inverter.

Note: pwm frequency = 1.8 kHz.

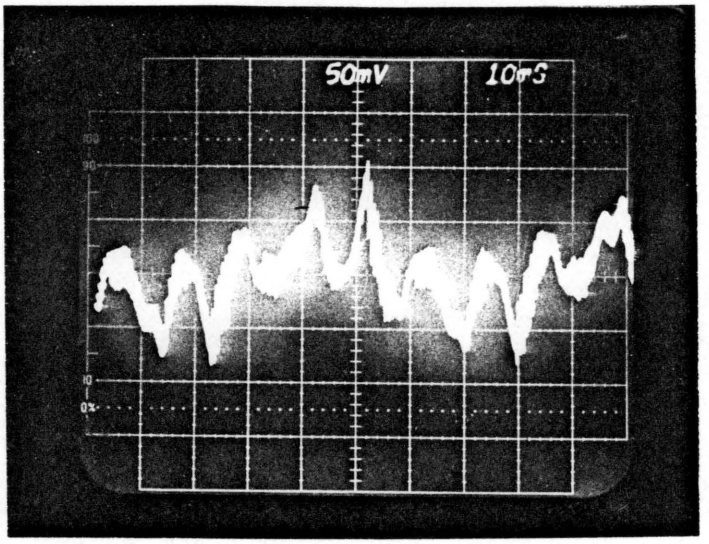
I_{req} is the current requested by the PROM.

I_{ph} is the current in the corresponding phase.

distortion introduced is similar to the cross-over distortion in a Class C amplifier and is due to the large dead time. The second observation is that the current per phase has a large ripple.

The no load phase current in the twelve pole motor is shown in Figure 5.7.a. Figure 5.7.b. shows an expanded view of the motor current waveform at the center of Figure 5.7.a. The magnitude of the current ripple is directly proportional to the low pulse width modulation frequency and is inversely proportional to the inductance of the motor.

The motor controlled by the GEMFET amplifier was then replaced by a high inductance, thirty pole permanent magnet motor. This motor had an inductance per phase of 110 mH and a resistance per phase of 13Ω. The current waveforms at various loads, with a pulse width modulation frequency of 2.5 kHz is shown in the oscillographs of Figure 5.8. Figure 5.8.a shows the operation of the motor at no load. Figure 5.8.b shows the operation under a light load. Figure 5.8.c shows the phase current under a heavy load. The upper trace in Figures 5.8.a and 5.8.b shows the current per phase. The current request of the corresponding phase is shown in the middle trace. The bottom trace shows the current feedback voltage in the same phase. There is a 180 degree phase shift between the phase current and the feedback voltage. Figure



I_{ph} 0.5A/div.

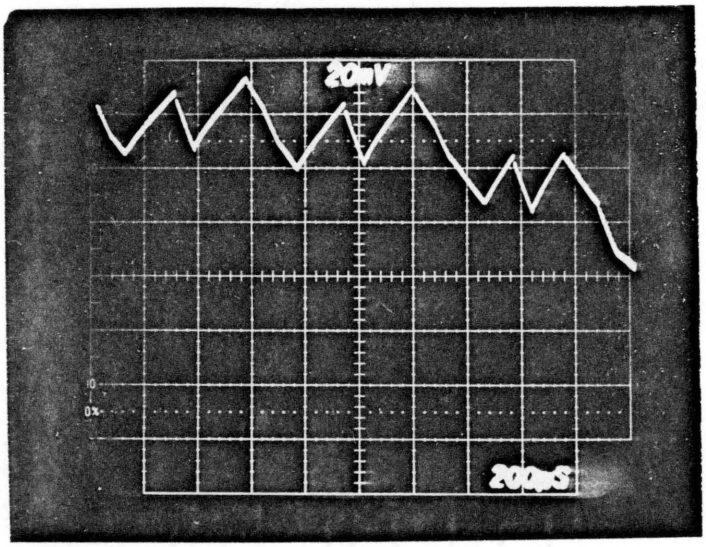
10 ms/div.

Figure 5.7.a: Oscillograph showing no load current per phase in a 12 pole brushless dc motor.

Note: pwm frequency = 1.8 kHz.

Bus Voltage to the GEMFET inverter = 250V.

I_{ph} is the current per phase.



I_{ph} 0.2A/div.

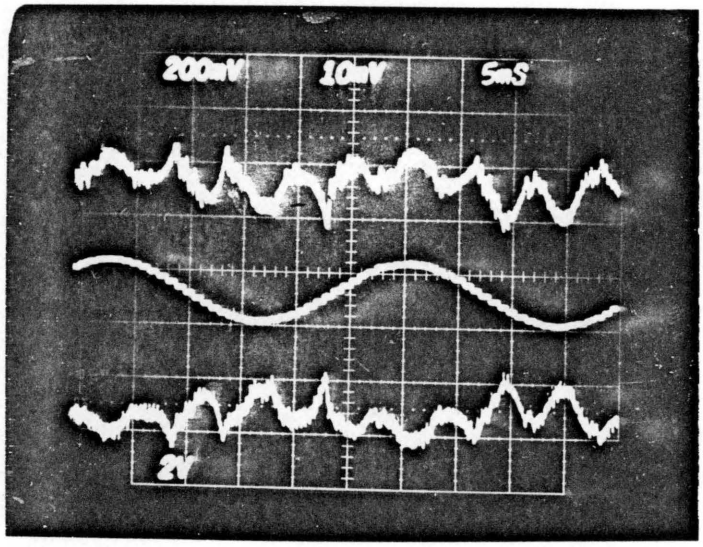
200µs/div.

Figure 5.7.b: Oscillograph showing an expanded view of the current in Figure 5.7.a.

Note: pwm frequency = 1.8 kHz.

Bus Voltage to the GEMFET inverter = 250V.

IGT case temperature = 31°C.



I_{ph} 0.5A/div.

I_{req} 20V/div.

I_{fb} 2V/div.

5 ms/div.

Figure 5.8.a: Oscillograph showing current per phase with the 30 pole brushless dc motor under no load.

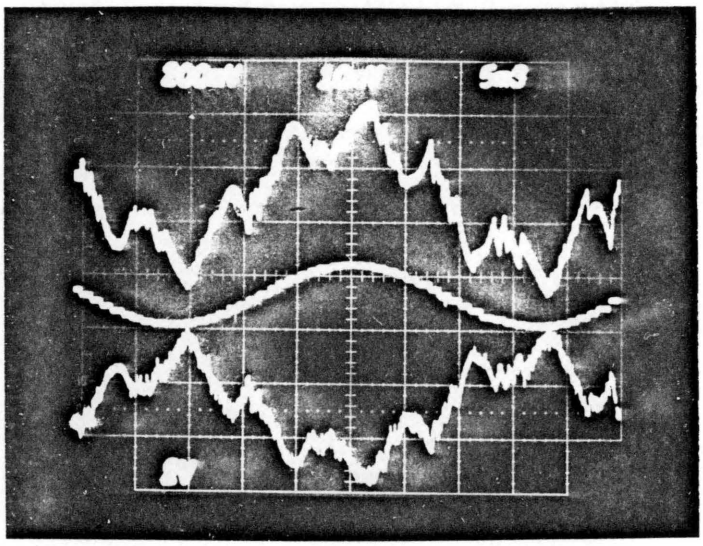
Note: pwm frequency = 2.5 kHz.

Bus Voltage to the GEMFET inverter = 340V.

I_{ph} is the current per phase.

I_{req} is the current request voltage.

I_{fb} is the feedback voltage proportional to the current I_{ph}.



I_{ph} 0.5A/div.

I_{req} 20V/div.

I_{fb} 2V/div.

5 ms/div.

Figure 5.8.b: Oscillograph showing current per phase with the 30 pole brushless dc motor at light load.

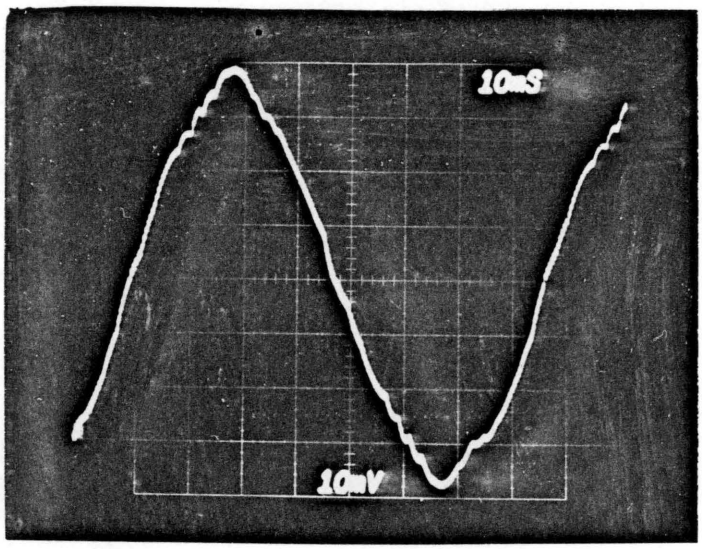
Note: pwm frequency = 2.5 kHz.

Bus Voltage to the GEMFET inverter = 340V.

I_{ph} is the current per phase.

I_{req} is the current request voltage.

I_{fb} is the feedback voltage proportional to the current I_{ph}.



I_{ph} 20V/div.

10 ms/div.

Figure 5.8.c: Oscillograph showing current per phase with the 30 pole motor under a heavy load.

Note: pwm frequency = 2.5 kHz.

Bus Voltage to the GEMFET inverter = 340V.

5.8.c shows how, under a heavy load, the phase current becomes more sinusoidal.

5.3.2. DEVICE LOSSES.

Baliga [12,13] showed the variation of the conduction resistances of IGTs with differing fall times, considering both device design and the effect of irradiation. If we increase the device irradiation , the fall time decreases and the conduction resistance of the device increases.

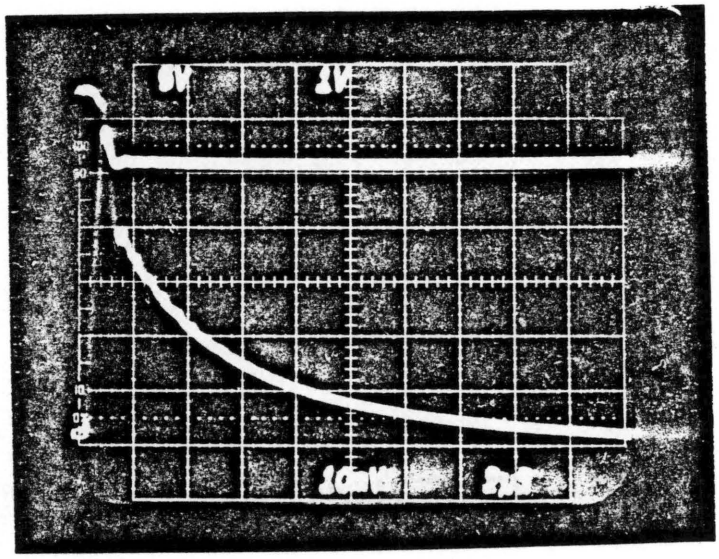
Figure 5.9 shows the current and voltage waveforms of one of the six IGTs in the three phase bridge inverter. Consider the power losses in the IGT three phase bridge circuit built. The assumptions made are:

1) The average duty cycle is approximated to be 48%. The duty cycle may be approximated as the sum of the device on time and the turn-off (storage) time.

2) Turn-on losses may not be neglected in pwm schemes.

3) Empirical expressions derived in [8] are used to determine the turn-on and turn-off losses in the GEMFET. The fall times of the GEMFET in circuit were seen to be approximately as follows:

rise time= 150ns and fall time is t_{f1}=5μs and t_{f2}=10μs.



V_{DS} 50V/div.

I_{DS} 1A/div.

2μs/div.

Figure 5.9: Oscillograph of the turn off current waveform in one GEMFET in the three phase bridge inverter.

Note: pwm frequency = 1.8 kHz.

Bus Voltage = 150V.

GEMFET case temperature = 32°C.

4) Each device switches 340V and 10A.

5) Gate Drive losses may be neglected.

Therefore the losses in each device can be calculated as follows:

Conduction losses = $(V_{DS(sat)} x I_{DM} x (t_c + t_d))/T$

= (2.7x10x0.48) W

= 12.96 W

Off State losses = $(V_{DD} x I_{DS(off)} x (T - t_1))/T$

= $340 x\ 10^{-5} x 0.52$

= 0.01768.

Turn-on losses = $(V_{DD} x I_{DM} x f x t_r)/6$

= $(340x10x2.5x10^{3}x150x10^{-9})/6$

= 0.000056667xf W.

Turn-off losses = $(V_{DD} x I_{DM} x f) x ((T_{f1}/5.5) + (T_{f2}/21.5))$

= $(340x10xf) x (0.9090909x10^{-6} + 0.465116x10^{-6})$

= 0.0046723xf

Total Power = 12.97768 + 0.0046723xf

= 12.98 + 0.00467xf

TABLE 5.2: TOTAL POWER LOSSES PER DEVICE.

MGM20N50 GEMFETS IN THE MOTOR DRIVE CIRCUIT.

FREQUENCY (Hz.)	IGT MGM 20N50 (Watts)
0	12.98
100	13.45
250	14.15
500	15.32
750	16.48
1000	17.65
1500	19.99
2500	24.66
3000	26.99
5000	36.33

FREQUENCY (Hz.)	IGT MGM 20N50 (Watts)
7500	48.01
10000	59.68
15000	83.03
20000	106.38

CHAPTER VI.

CONCLUSIONS.

This chapter is divided into two parts. Section 6.1 discusses the conclusions drawn from the fabrication of the IGT based motor control circuit. Section 6.2 describes the future research work in this area and variations to the N-channel IGT that are likely in the near future.

6.1. CONCLUSIONS.

Since the invention of the IGT in late 1982, most of the literature ,has consisted of descriptions of particular device structure of different ratings and characteristics. These papers have stressed device design and manufacturing techniques [5,8,9]. The contributions made in this thesis, in the author's view, are the following:

1) The compilation of a consistent theory for the device structure, its operation and an explanation of the basic characteristics of the device. Although some of the theory is not new in itself, this concise explanation of device theory can be better understood by the average power electronics engineer.

2) An in-depth investigation of the latching characteristics of the IGT, which is a unique and inconvenient characteristic of the IGT. The application information obtained enables the user to estimate the limitations of the device.

3) The design of a gate drive circuit and the implementation in a prototype three phase bridge inverter for brushless dc motor application. As far as the author knows, this is the first IGT motor drive system reported.

Several conclusions were drawn from this investigation:

1) Because of the inherently slow turn-off time of the IGT available today, the upper limit for system operation is about 2.5 kHz for the slow IGTs. This is acceptable for many motor drive applications. Other applications such as switching power supplies need devices with significantly smaller fall times. However, with device design, the turn-off speed can be significantly increased at the expense of conduction voltage drop. It is expected that this is one of the directions of future development.

2) From a user's point of view, the IGT device characteristics exhibit several conflicting constraints. The designer has to choose a low value of the gate-source

resistance such that the latching current level is high but the turn-off is not too slow. Large values of the gate-source resistance improve the latching level but slow down the switching speed and cause large turn-off losses. A high impedance also creates a gate voltage spike in the gate circuit of one device in a totempole configuration when the other device is switched off.

3) From the package point of view, it is convenient to have a totempole power module with anti-parallel diodes.

4) Latching is a weakness in motor drive circuits but a distinct advantage in resonant converters and other uses with zero current turn-off.

6.2. FUTURE DEVELOPMENTS.

The IGT is still in its infancy. More developments can be expected in the future. Some of these developments are discussed in the following subsections.

6.2.1. THE ASYMMETRIC IGT.

Figure 6.1 shows the structure of the asymmetrical IGT. The concept of extending the concept of an asymmetric structure to the IGT has been demonstrated recently by B.J.Baliga et al [17]. The major difference between an

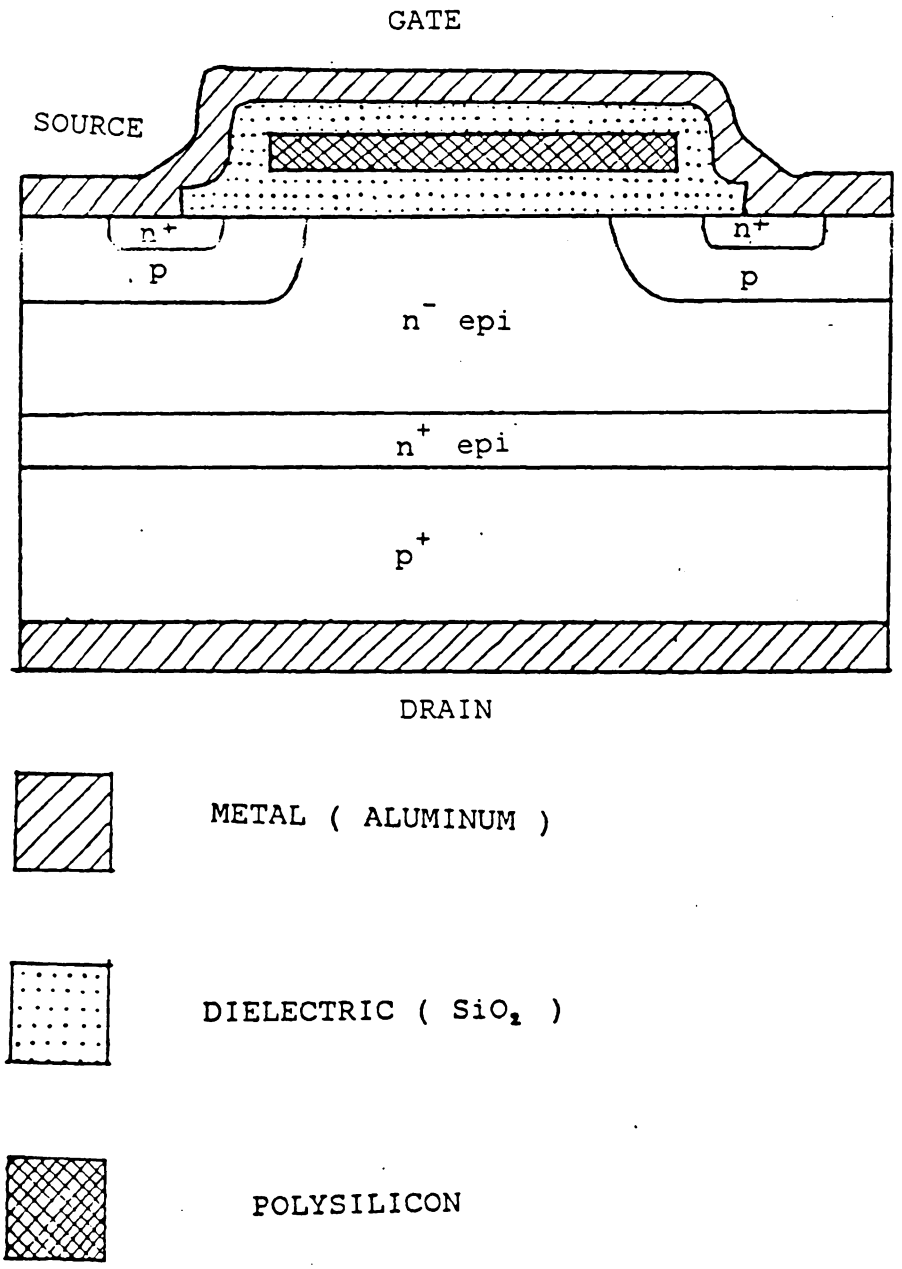
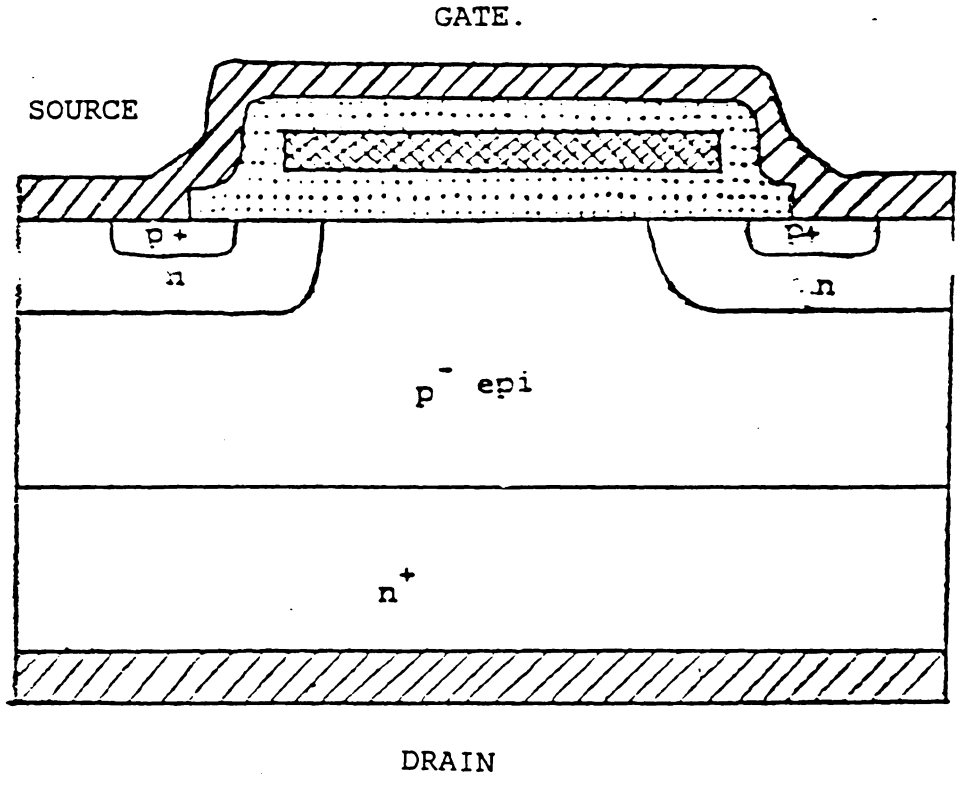


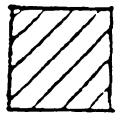
Figure 6.1: The structure of the asymmetrical IGT.

asymmetrical IGT and a conventional IGT is that the former has no reverse voltage blocking capability but can be designed to achieve faster speed and lower conduction voltage drop. This is achieved by replacing the n^- region in the IGT with n^+ and n^- regions. This results in a significant decrease in the thickness of the epitaxial base region required to support the device operating voltages. This decreases the forward voltage drop during current conduction and also allows the use of a lower lifetime in the base region, which increases the switching speed of the IGTs. Because of the n^+-p junction, the device reverse blocking capability is drastically reduced. However, for most applications, an anti-parallel diode is necessary anyway.

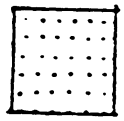
6.2.2. P CHANNEL IGTs.

The structure of a p channel IGT is given in Figure 6.2. The structure of the p-channel IGT is the complementary to to that of the n-channel device. The starting substrate is n doped. The IGT is the only gate controlled device that has a p-channel equivalent which is not inferior to the n channel device. Bipolar p-n-p transistors are slower than similar n-p-n transistors and the on resistance of p channel power MOSFETs are higher than their n channel counterparts.





METAL (ALUMINUM)



DIELECTRIC (SiO_2)

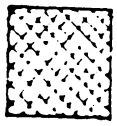


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Figure 6.2: The structure of a P channel IGT.

The p channel IGT, like the n-channel IGT, displays p-i-n diode characteristics in the on-state and does not suffer from the same weakness as the p channel power MOSFET. The development of the p channel IGT means that a complementary pair enables the designer to have a non-isolated gate drive which further simplify the gate circuit, especially for motor drive circuits. At present, however, no manufacturer makes p channel IGTs.

6.2.3. THE INTEGRATED GATE DRIVE CHIP.

The purpose of integration of the drive circuitry with the power device is to facilitate control from TTL or CMOS logic, simplify electronics, reduce system size and cost, and increase system reliability.

The IGT is very well suited for drive circuit integration. The small drive requirements are a major advantage. Another important factor is that the gate-source external resistors may also be incorporated within the package to decrease the chances of device latching. The gate-source zener diode is relatively easy to implement into the circuit. The problem of gate circuit inductance could be greatly reduced.

The structure of the IGT, seen in Figure 2.1 is very similar to a DMOS conventional MOSFET. Two power IC

technologies that have been developed recently seem very promising: The Bipolar-DMOS-FET technology and the junction isolated CMOS-DMOS technology. The inherent advantages of the high voltage capability, ruggedness and lower power consumption make the CMOS/DMOS technology best suited for an IGT integrated gate drive chip. The power integrated circuits available today include The DMOS-CMOS power IC MPC2005 from Motorola has 60% of its chip area occupied by a MOS-SCR which is similar in structure to an IGT and which can block voltages up to 150 V [12] Power ICs with 440 V, 25 A power IGT chips integrated directly into the IC chip are likely to be commercially available in the near future.

The development of p-channel IGTs will further help create integrated systems using power IC technology. For the purposes of motor control, the packaging of a p channel and an n channel device and their antiparallel diodes to form one leg of a three phase bridge inverter, is very attractive from the point of view of the user.

6.2.4. INCREASES IN VOLTAGE, CURRENT AND SPEED.

The conduction mechanism of the IGT makes it very well suited for a high voltage applications. As the voltage rating of the device goes up, the improvement over the MOSFET in terms of the chip area becomes even more

pronounced. At present, 1000 V power MOSFETs can conduct up to only about 1 A. IGTs with ratings up to 1 kV and 10 A and also 400 V and 50 A are likely in the near future. Devices with higher continuous current ratings of up to 50 A are also likely in the next few years. The most significant improvements, however, are likely in the fall times of the IGT and 400 V, 10 A devices with fall times of under 250 μs will be available in the near future.

The IGT represents the first device to combine the advantages of bipolar transistors and power MOSFETs. This trend of combining MOS and bipolar in monolithic structures is likely to continue [12] and advances in technology can be expected. The trend to mix technologies with logic and driver devices will continue in the years ahead.

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