Low-Power mm-Wave Frequency Quadrupler Using Deep Class-C Doublers

Meysam Sohani Darban, Dong Sam Ha, Jeffrey Sean Walling
Bradly Department of Electrical and Computer Engineering,
Virginia Polytechnic Institute and State University, Virginia, United States
{meysam97, ha, jswalling}@vt.edu

***Abstract* — In this paper, a low-power mm-wave frequency quadrupler is introduced. The proposed quadrupler comprises two push-push frequency doublers operating in deep class-C mode to ensure minimal static power consumption. The quadrupler is fabricated in the 22-nm FD-SOI process technology and uses an area of $0.5 \times 0.41\,\mathrm{mm}^2$. It generates a ≈ 60 GHz signal with a P_{out} of -10 dBm from a 15 GHz input signal and provides $10.8\,\mathrm{GHz}$ output bandwidth (18% fractional bandwidth). Its low power consumption and wide bandwidth make it attractive for many operations in the $60\,\mathrm{GHz}$ spectrum, including advanced communication with a high data rate. Operating from $54.9 - 65.7$ GHz, its total power consumption is $12\ mW$, which includes the output pad driver; however, the core frequency quadrupler consumes only $5\ m$W due to deep class-C operation.**

***Keywords* — Class-C, frequency multiplier, low-power, mm-Wave, quadrupler.**

I. Introduction

As the transition frequency of transistors (f_T) has increased with continued scaling of the feature sizes in CMOS technology, primarily due to shorter-channel lengths and reduced parasitic capacitance, it is possible to realize efficient circuits that operate into mm-wave frequencies. Operating in these frequency bands leads to higher available bandwidth and increased spatial resolution. This can be exploited in communications applications (e.g., mm-wave connectivity), imaging, and radar applications [1], [2].

Generating a high-frequency signal from a local frequency synthesizer with low power consumption, low phase noise, and high range of operation is one of the primary challenges faced by operation in the mm-wave frequency bands. For optimal performance, the synthesizer should produce a signal with low phase noise and be capable of adjusting the carrier signal's frequency over an expected range with acceptable resolution. One solution to this problem is to generate a signal at a lower frequency using a phase-locked loop (PLL) and subsequently increase the fundamental frequency using a frequency multiplier. This method allows the synthesizer to operate at a lower frequency, where better performance (e.g., reduced power, lower phase noise, and increased resolution) is expected [3].

Many recent examples of frequency multipliers have been demonstrated, especially by a multiplication factor of four called a "quadrupler." Reference [4] presented a 2-stage multiplication, using quadrature signals at its input. A single-stage quadrupler from a single-ended input was shown in [5]. A primary challenge to the design of multipliers is that their power consumption is often high, which contradicts the justification for their usage (i.e., to reduce the system's total power). In addition, utilizing quadrature signals for either the input or internal stages can lead to reduced bandwidth. This paper presents a low-power frequency quadrupler consisting of two cascaded doublers in deep class-C operation to decrease the static power. Avoiding mid-stage amplifiers or I/Q passive structures provides wide ($\approx$ 11 GHz) -3dB saturated output power bandwidth. The paper is organized as follows. Section II presents the concept and architecture of the proposed quadrupler. This is followed by measurement results in Section III. Finally, conclusions are presented in Section IV.

II. A mm-Wave Frequency quadrupler

In this section, basic concepts in frequency multiplication are presented, along with details of the proposed frequency quadrupling method that results in low power consumption and wide bandwidth. Additionally, the architecture of the proposed circuit and design considerations are presented.

A. Frequency Multiplication Concepts

There are two primary methods for generating integer frequency multiplication: *1)* Mixing a signal with either itself or one of its harmonics, and *2)* Exploiting device nonlinearity to generate harmonics. In either case, a filter is generally applied to select the desired output frequency product that is produced. Mixer-based frequency multipliers can be complex to design in fine-line CMOS owing to reduced voltage supplies and poor switching performance at higher frequencies (e.g., increased effective on-resistance, R_{on}, and slow-edge rates), typically resulting in higher power consumption.

A mixer-based multiplier cannot provide a multiplication factor > 2 unless a strong higher-order harmonic of the input can be self-mixed with the fundamental or a separate circuit is used to generate a higher frequency for mixing with the input. In either of these cases, increased power consumption, mainly when operating at high frequency, is inevitable.

The nonlinear method has a flaw at high frequency that makes it practically impossible to realize multiplication factors > 2. High-order harmonics generated by nonlinearity rarely provide enough output power to be used in the system, and the available power at the harmonic typically reduces as the order of the harmonic is increased. Consider Fig. 1 (a),

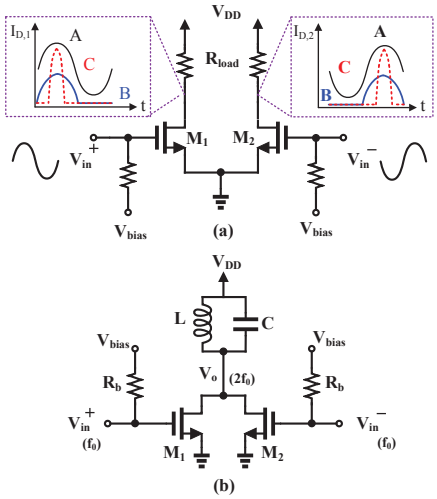


Fig. 1. (a) Demonstration of drain currents for three different classes of operation in differential amplifier, (b) Schematic of frequency doubler.

where MOSFETs act as amplifiers in a differential mode. If V_{bias} is higher than MOSFET's threshold voltage (V_{th}), they will act as a linear (class-A) amplifier. However, changing V_{bias} to be closer to V_{th} pushes the device into a nonlinear (class-AB, -B, -C) mode by enabling the drain current to be periodically cut off. Due to this behavior, the output current contains higher-order harmonics at integer multiples of the input frequency dependent on the gate bias and the input power.

For an optimal even-harmonic generation, the gate bias and input power would be such that the drain current waveform is a half-rectified sine wave. In this case, the 2^{nd} harmonic current amplitude would ideally be -7dB lower than the fundamental, and the 4^{th} harmonic current would be -21dB lower. It is expected that the performance when implemented in transistors will be worse than ideal; hence, such structures are not feasible, even considering their simplicity in implementation.

B. Push-Push Frequency Doubler

The circuit shown in Fig. 1(b) is a push-push circuit, where V_{in}^{+} and V_{in}^{-} are differential input signals. By driving transistors M_1 and M_2 into the nonlinear operation mode, we can realize a drain current that contains many odd- and even-harmonics. Equation 1 describes the drain current of either transistor as a function of the gate-to-source voltage, where α_N represents a proportionality coefficient dependent on the gate bias and input power.

$$i_{out} = \alpha_1.V_{gs} + \alpha_2.V_{gs}^2 + \alpha_3.V_{gs}^3 + \alpha_4.V_{gs}^4 + ... \quad (1)$$

By applying a sinusoidal signal as V_{GS} and $-V_{GS}$ to the respective inputs of the push-push circuit, harmonics in the output currents are realized. The drain currents for each transistor are as follows:

$$i_{D,M1} = \alpha_1.sin(\omega t) + \alpha_2.sin^2(\omega t) + \alpha_3.sin^3(\omega t) + \alpha_4.sin^4(\omega t) + ... \quad (2)$$

$$i_{D,M2} = -\alpha_1.sin(\omega t) + \alpha_2.sin^2(\omega t) - \alpha_3.sin^3(\omega t) + \alpha_4.sin^4(\omega t) + ... \quad (3)$$

As shown in Eqs. 2 and 3, the odd harmonics of the drain current are out of phase with each other, while the even harmonics are in phase. Hence, adding $i_{D,1}$ with $i_{D,2}$ in the shared drain node suppresses the fundamental and all odd harmonics and selects the even harmonics. In an ideal case, the second harmonic appears with twice the input amplitude, while the higher-order harmonic amplitudes are reduced proportionally as their order increases. Ideally, only the 2^{nd} harmonic should be present in the output for a doubler circuit. To select the 2^{nd} tone, the LC-tank shown in Fig. 1(b) is tuned to resonate at $2 \times f_0$, where f_0 is the fundamental frequency at the input to the doubler [6].

If V_{bias} in Fig. 1 (b) is set to a value less than V_{th}, the transistors will operate in the deep class-C mode. This reduces their static current at the expense of reducing the power available at the 2^{nd} harmonic and increases the power at other harmonics (due to sub-optimal wave shapes). Using a load-pull simulation in the design procedure can result in a more optimal power delivery.

C. Quadrupler Circuit

As discussed in Section II-A, generating the 4^{th} harmonic from the nonlinear behavior of the transistor is impractical. Meanwhile, it is seen that a relatively strong second harmonic can be achieved with a push-push doubler (Fig. 1 (b)). Hence, a cascade of two push-push doublers is chosen in the proposed implementation, yielding a frequency quadrupler.

The schematic of the proposed quadrupler is shown in Fig. 2. The proposed circuit consists of a transformer balun at the input, followed by a cascade of two push-push doublers and an output buffer to drive the signal off-chip for measurement. Note that a more optimal buffer could be realized if not for measurement using 50 Ω instrumentation. The goal of the proposed work was to realize an efficient, low-power multiplication; hence, no input or interstage amplifiers were used in the design.

To provide for single-ended input and output, a transformer balun is used at the input to simultaneously achieve an input match while also passing the DC bias to the input gates. The transformer-based matching network, with the primary and secondary inductance of 142 and 132 pH at 15 GHz, is designed to match the 50 Ω of the input probe with the input of the first doubler stage. Note that the input and output are matched to 50 Ω only for measurement purposes; in a complete system, efficiency could be improved by conjugately matching the input directly to the preceding stages' output.

The first stage doubles the 15 GHz input frequency to 30 GHz. In prior work, an interstage amplifier was used to boost the signal before input to the succeeding stage [7]. However, to decrease the power consumption, this work presents a passive balun as the 2^{nd} harmonic load, as well as an interstage balun. The interstage balun is optimized to

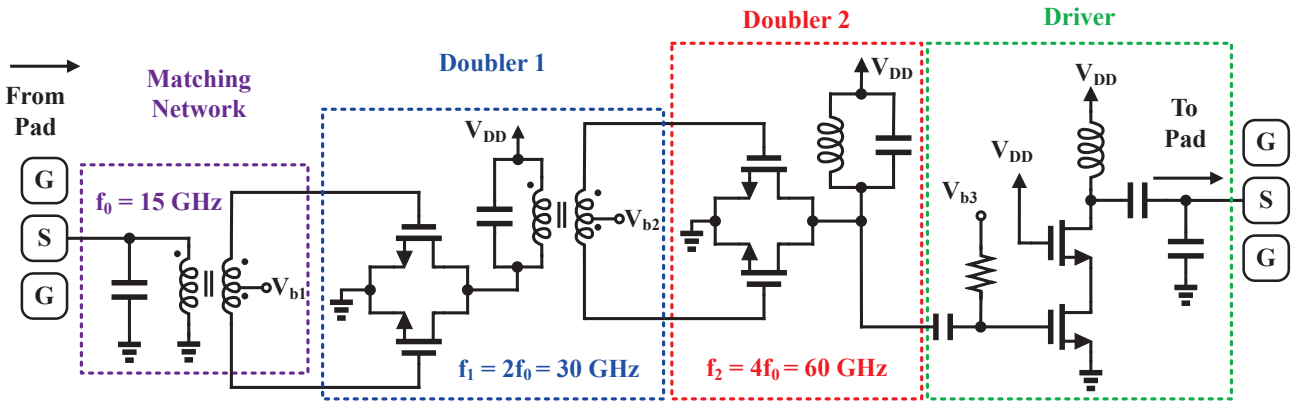
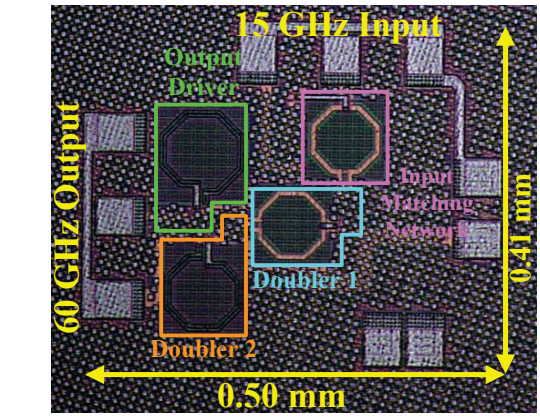
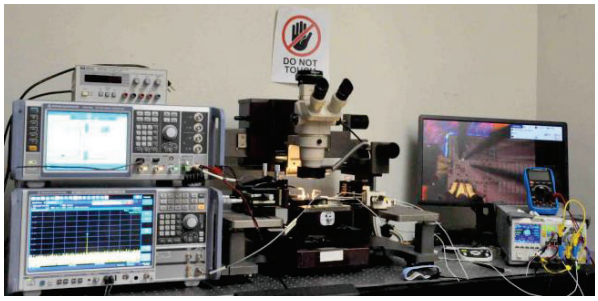


Fig. 2. Schematic of proposed low-power quadrapuler.



(a)



(b)

Fig. 3. (a) Microphotograph of the fabricated circuit, (b) Measurement setup.

provide maximal voltage swing at the second-stage doubler's input.

To maintain single-ended I/O, the second stage doubler is terminated with a high-Q shunt inductor, optimized to provide maximum voltage swing at the second stage's output and good harmonic rejection at the output. A class-A driver comprises the third stage, which is to drive the output pad. By using deep class-C operation for the doublers and using passive baluns at the input and interstage instead of active circuits, low power consumption is achieved.

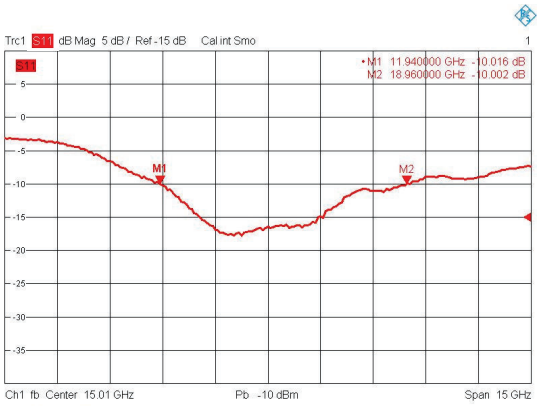


Fig. 4. Measured input reflection coefficient.

III. Measurement and Results

The proposed circuit was fabricated using 22-nm FD-SOI process technology with 9 metal layers, including an ultra-thick metal layer. The die photo is shown in Fig. 3 (a). The total occupied area (including pads) is 0.5×0.41 mm^2. The measurement setup for testing the circuit is shown in Fig. 3 (b). The input signal is generated using a Rohde & Schwarz (R&S) SMW200A signal generator, and the output is measured using an R&S FSW spectrum analyzer.

The input match is characterized. Fig. 4 shows the measured S_{11}. The input match is maintained at $S_{11} < -10dB$ across ≈ 7 GHz bandwidth from 12-19 GHz. Next, the input frequency is swept to measure the output power as a function of frequency. Fig. 5 shows the output power of the quadrupler circuit at different output frequencies. The -3 dB bandwidth of the quadrupler is 10.8 GHz, resulting in an 18% fractional bandwidth.

Fig. 6 shows the measured output power characteristic versus the input power at a frequency of 60 GHz. This is compared to the simulation result in the same figure. We were unable to measure the harmonic power due to a lack of appropriate probe extenders; hence we also provided simulation results of the output harmonics. The proposed multiplier provides a worst-case harmonic rejection of -22.5

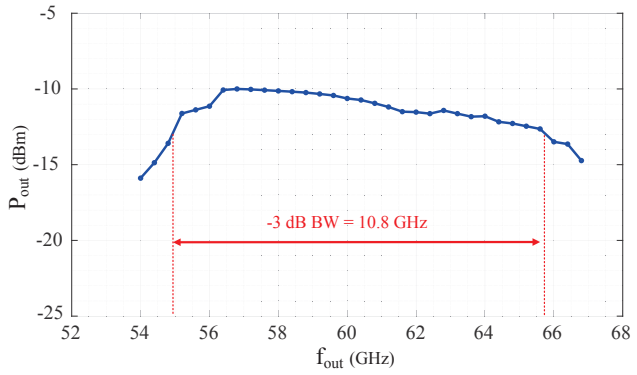


Fig. 5. Measured output power of the quadrupler over frequencies, indicating 10.8 GHz bandwidth.

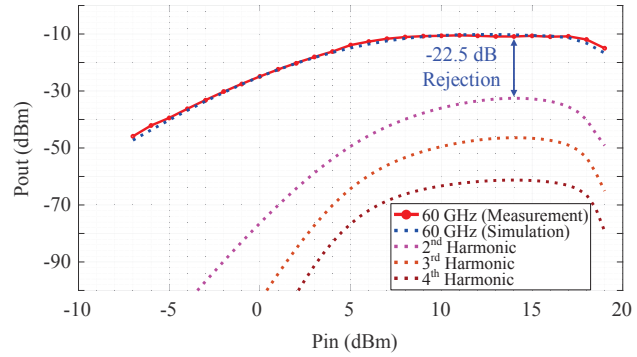


Fig. 6. Measured output power at 60 GHz and simulated harmonics' power by adjusting input power.

dBC at the second harmonic rejection at its single-ended output. This occurs in deep saturation, as is shown in Fig. 6.

The first doubler operates in deep class-C mode. Hence, its behavior causes the characteristic to saturate at $P_{in} \approx 10\,\mathrm{dBm}$. The quadrupler operates from a 1.2 V supply, and its total power consumption is 12 mW. The breakdown of the power consumption is indicated in the pie chart of Fig. 7. All circuits on the chip share a common DC supply; hence, simulation results were used to provide a breakdown of the individual components of DC power. As expected, most of the power consumption is due to the output pad driver, which consumes 58% of the power. Due to the relatively low-quality factor of the transformers, the first doubler consumes more power than the second. As expected, due to the deep class-C operation of the doublers, the power consumption of these blocks is low compared to previous work shown in Table 1.

IV. Conclusion

A low-power mm-wave frequency quadrupler is designed and fabricated using 22 nm FDX-SOI technology for operation in the 60 GHz spectrum. It achieves 18% fractional bandwidth and power consumption of $\approx$ 5 mW when eliminating the pad driver. It is suitable for frequency generation in many applications, including mm-Wave communications and radar. The circuit is a double-double architecture, which consists of two doubler stages, and each stage is optimized

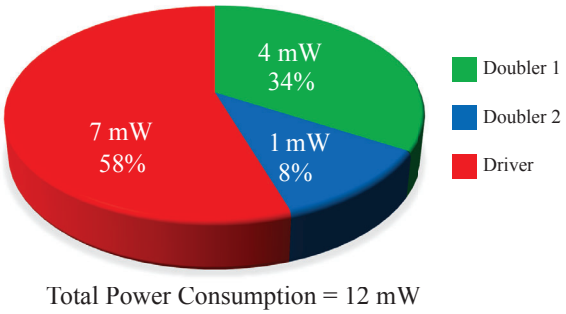


Fig. 7. Power breakdown of the entire system.

Table 1. Comparison of state-of-the-art frequency quadruplers

	This Work	[4]	[5]	[7]	[8]
Technology	**22nm FD-SOI**	22nm FD-SOI	40nm CMOS	0.1μm SiGe	22nm FD-SOI
f_{out} (GHz)	**54.9 - 65.7**	70 - 81	65 -75	70 - 110	32 - 42
BW %	**18**	12.9	13.6	44	22
P_{DC} (mW)	**5** / 12*	70	5.08/11.38*	170	12 / 20
P_{out} (dBm)	**-10**	3.1	-0.2	3	-4
BW / P_{DC} (GHz/mW)	**2.16**	0.75	1.79	0.23	0.825
Area (mm^2)	**0.2**	0.38	0.28	1.9	0.21

*Include driver.

to operate at the lowest amount of power by using deep class-C modes. Removing interstage amplifiers and utilizing passive load-pulled loads to optimize the performance achieves frequency quadrupling with low power consumption.

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