Topology and Control Investigation of Soft-Switching DC-DC Converters for DC Transformer (DCX) Applications

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Abstract

With the development of electric vehicle (EV) charging systems, energy storage systems (ESS), data center power supplies, and solid-state transformer (SST) systems, the fixed-ratio isolated DC-DC converter, namely the DC transformer (DCX), has gained significant popularity. Similar to the passive AC transformer, DCX can bidirectionally convey DC power with very high efficiency. Due to zero-voltage switching (ZVS) and a small root mean square (RMS) current, the open-loop CLLC resonant converter operating at the resonant frequency is a promising candidate for DCX with a constant voltage transfer ratio.

In **Chapter 2**, to solve unsmooth bidirectional power flow and current distortion in the traditional CLLC-DCX with synchronization rectification (SR) modulation, a dual-active-synchronization (DAS) modulation is adopted with identical driving signals on both sides. First, the switching transition of this modulation is thoroughly analyzed considering the large switch's output capacitances. After comparing different transitions, a so-called sync-ZVS transition is more desirable with ZVS, has no deadtime conduction loss, and almost has load-independent voltage gain. An axis and center symmetric (ACS) method is proposed to achieve this switching transition. Based on this method, an overall design procedure of CLLC-DCX with DAS modulation is also proposed.

However, designing a high-power and high-frequency transformer for CLLC-DCX presents significant challenges due to the trade-off between thermal management, leakage inductance minimization, and insulation requirements. To overcome this trade-off between power rating and operation frequency, a scalable electronic-embedded transformer (EET) with a low-voltage bridge integrated into the transformer windings is proposed in **Chapter 3**. The EET addresses the challenge through simple open-loop control and natural current sharing, enabling easy parallel connection and scaling to different power ratings. Based on this concept, a bidirectional, EET-based DC transformer (EET-DCX) is proposed to solve the transformer-level paralleling and resonant point shift issues in traditional LLC-DCX designs. By employing the embedded full bridge, the EET-DCX effectively cancels out the impedance of the leakage inductance, ensuring optimal operation at any frequency. Additionally, the EET-DCX retains the inherent advantages of the LLC-DCX, such as load-independent voltage gain, simple open-loop control, full-load range ZVS, and low circulating current. Leveraging these advantages, the proposed EET-DCX solution has the potential to push the boundaries of transformer performance to the MHz operation frequency range with hundreds of kilowatts of power capability.

Moreover, to address the significant RMS current problem of the CLLC-DCX, a trapezoidal current modulation is also proposed in **Chapter 3**. Compared to the CLLC-DCX with a sinusoidal current, an EET-DCX with a trapezoidal current can reduce the total conduction loss by up to 23%. This total conduction loss includes semiconductor loss on both high-voltage and low-voltage bridges and transformer winding loss.

In light of this EET concept, another resonant commutation (RC) EET-DCX is proposed to streamline the circuit. First, it replaces the embedded full bridge with a low-voltage bidirectional AC switch. Second, it introduces a resonant current commutation to realize a quasi-trapezoidal

transformer current with a smaller RMS value. Compared to the triangular current produced by the original EET-DCX, the RMS current can be decreased by 15%. By incorporating only one embedded bidirectional AC switch, the high-frequency transformer leakage inductance impedance is fully neutralized. As a result, the rated power of the proposed RC EET-DCX can be readily scaled up through transformer-level parallelism. Furthermore, the RC EET-DCX maintains the benefits of a typical LLC/CLLC-DCX, including load-independent voltage gain, full load range ZVS, and low circulating current.

However, either in EET-DCX or RC EET-DCX, the trapezoidal current modulation will increase the voltage stress on the low-voltage full bridge or bidirectional AC switch, especially when the leakage inductance is large and variable, such as in the high-power wireless charging application. To address this trade-off between RMS current and voltage stress, this paper proposes the concept of a hybrid resonant-type EET-DCX with a series resonant capacitor. Following this concept, two specific topologies, hybrid EET-DCX and hybrid RC EET-DCX, are proposed. The main difference between these topologies is that the former adopts a full bridge. In a hybrid RC EET-DCX, a resonant current commutation scheme is developed. Among these topologies, since the passive capacitor can mainly cancel the leakage inductance impedance, the full bridge or AC switch only needs to handle the remaining impedance. Thus, the voltage stress on active components can be dramatically decreased. Additionally, these two proposed topologies can retain all the advantages of previous EET-DCX designs, including natural current sharing, load-independent voltage gain, simple open-loop control, and full-load range ZVS. The comparison between these two topologies is thoroughly studied. Finally, a 12-kW DCX testbench is built to verify all the analysis and performance in **Chapter 3**.

If output voltage regulation is required, DCX can cooperate with other voltage regulators to realize

high conversion efficiency and power density. In **Chapter 4**, two DCX applications are implemented: an 18-kW 98.8% peak efficiency EV battery charger with partial power processing and a 50-kW symmetric 3-level buck-boost converter with common-mode (CM) noise reduction.

In the first battery charger, a large portion of the power is handled by an 18 kW CLLC-DCX, and the remaining partial power goes through a 3-phase interleaved buck converter. The proposed switching transition optimization in **Chapter 2** is adopted in the 18-kW CLLC-DCX to realize 98.8% peak efficiency.

To handle the step-up and step-down cases at the same time, a symmetric 3-level buck-boost converter with coupled inductors is also studied as a post regulator. With symmetric topology and quadrangle current control, the converter can achieve a CM noise reduction and full load range ZVS with a small RMS current. To further optimize the performance and simplify the control, a mid-point bridging with a better CM noise reduction and a split capacitor voltage auto-balance is implemented. A 50-kW prototype is built to verify the above analysis.

To summarize, **Chapter 2** first proposes a switching transition optimization for CLLC-DCX. Later, to address the intrinsic trade-off between transformer rating power and frequency, an EET concept and its corresponding soft-switching DCX family are found in **Chapter 3**. Finally, to handle voltage regulation, two examples for practical applications are studied in **Chapter 4 —**one is an 18-kW partial power converter, and the other is a 50-kW 3-L buck-boost converter. Finally, Chapter 5 will draw conclusions and illustrate future work.

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General Audience Abstract

With the development of electric vehicle (EV) charging systems, energy storage systems (ESS), data center power supply, and solid-state transformer (SST) systems, the fixed-ratio isolated dc-dc converter, namely dc transformer (DCX), has gained significant popularity. However, designing a high-performance DCX still has many challenges, such as large dead time loss, poor current sharing, and sensitivity to parameter tolerance.

Firstly, the state-of-the-art resonant CLLC-DCX is optimized in **Chapter 2.** With an optimal switching frequency and dead time, both the primary and secondary sides of zero voltage switching (ZVS) can begin and finish simultaneously, which means dead time loss caused by current through the body diode can be eliminated. Therefore, the efficiency of CLLC-DCX can be improved. However, designing a high-power and high-frequency CLLC-DCX transformer still presents significant challenges due to the trade-off between thermal management, leakage inductance minimization, and insulation requirements.

To overcome this trade-off, in **Chapter 3**, a scalable electronic-embedded transformer (EET) concept with a low-voltage bridge integrated into the transformer windings is proposed. The EET addresses the challenge through its simple open-loop control and natural current sharing, enabling easy parallel connection and scaling to different power ratings. In light of this EET concept, a new

family of soft-switching DCXs is proposed for different applications, such as high-power wireless charging systems. All these EET-based DCXs retain the merits of typical CLLC-DCX, such as small circulating current ringing, small turn-off current, full load range ZVS, and load-independent gain.

After realizing a desirable design for DCX, **Chapter 4** presents two DCX applications with voltage regulation. Firstly, an 18 kW 98.8% peak efficiency battery charger is designed with partial power processing. Most of the power will go through an optimized DCX, and the remaining small portion of power will go through a 3-phase interleaved buck converter. On the other hand, DCX can also be adopted as a front-end or rear-end converter in a typical two-state DC-DC converter. As for another stage, a non-isolated DC-DC converter with a large output range can be used to handle voltage regulation. Following this structure, a 50-kW symmetric 3-L buck-boost converter with coupled inductors and reduced common emission is proposed.

To summarize, the state-of-the-art CLLC-DCX is optimized in **Chapter 2**. Afterward, a new concept of EET-DCX and its corresponding DCX family is proposed in **Chapter 3**. After obtaining an optimized DCX, two practical applications with DCX are implemented in **Chapter 4**. Finally, **Chapter 5** will draw conclusions and illustrate future work.

To My Family:

My parents, Yunfei Cao, and Xiaodong Yao

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Table of Contents

Chapter 1 Introduction 1

1.1 Bidirectional DC-DC Converter 1

1.1.1 Electrical Vehicle (EV) Applications 2

1.1.2 Data Center Applications 3

1.2 Concept of DC Transformer (DCX) 4

1.2.1 What is a DCX? 4

1.2.2 DCX Applications 5

1.2.3 State-of-the-Art DCX Topologies 6

1.3 Challenges in CLLC-DCX Design 8

1.3.1 Switching Transition Noise 8

1.3.2 Deadtime Loss 9

1.3.3 Design Trade-off for High-Frequency and High-Power Transformer 9

1.3.4 Large rms Current with LLC-DCX 12

1.3.5 Current Sharing Issue 12

1.4 Dissertation Outline 14

Chapter 2 CLLC-DCX Modeling, Control, and Optimization 15

2.1 Introduction 15

2.2 Comprehensive Analysis for Dual-Active-Synchronization (DAS) 17

2.2.1 Simplified CLLC-DCX Circuit 17
2.2.2 DAS Operation Principle 20
2.2.3 “Sync-ZVS” Transition 25
2.3 “SYNC-ZVS” Switching Transition Design 26
2.3.1 Splitting Magnetizing Currents Approximation 26
2.3.2 Current Decomposition 27
2.3.3 Proposed “Axis and Center Symmetric” (ACS) Method 30
2.3.4 Load Independence and Power Boundary 34
2.3.5 Sensitivity Study on Parasitic Output Capacitance 35
2.4 Efficiency Optimization 39
2.4.1 Conduction Loss 39
2.4.2 Switching Loss 39
2.4.3 Proposed Optimization Procedure 40
2.5 Hardware Prototype and Experimental Results 42
2.5.1 Prototype Implementation 42
2.5.2 Experimental Results of *DCX I* 44
2.5.3 Experimental Results of *DCX II* 47
2.5.4 Experimental Results of *DCX III* 49
2.5.5 Efficiency 52
2.6 Conclusion 54

Chapter 3 Electronic-Embedded Transformer (EET), A New Concept for Scalable High-Frequency High-Power DCX 55

3.1 Introduction 55

3.2 The Foundation of EET-DCX 58

3.2.1 Operation Principle of Traditional LLC-DCX 58

3.2.2 Operation Principle of EET-DCX 60

3.2.3 Natural Current Sharing of EET-DCX 67

3.2.4 Soft Switching Analysis of EET-DCX 74

3.2.5 Hardware Implementation and Verification 79

3.3 Trapezoidal Current Modulation 93

3.3.1 Operation Principle 93

3.3.2 Re-analysis for ZVS and Current Sharing 97

3.3.3 Experimental Validation 100

3.4 Resonant Commutation (RC) EET-DCX 103

3.4.1 Operation Principle of RC EET-DCX 103

3.4.2 Robust Load-Independent Voltage Gain 106

3.4.3 Steady State of RC EET-DCX 109

3.4.4 Comparison with LLC-DCX and Typical EET-DCX 112

3.4.5 Sensitivity Study on Current Sharing 115

3.4.6 Hardware and Implementation 127

3.5 Hybrid EET-DCX, A New Family of Soft-switching DCX 137
3.5.1 Circuit Diagram and Definitions 139
3.5.2 Hybrid EET-DCX 141
3.5.3 Hybrid RC EET-DCX 149
3.5.4 Analytical Comparison 161
3.5.5 Experimental Verification 171
3.6 Conclusion 186
Chapter 4 DCX with Regulation and Implementation 187
4.1 Introduction 187
4.2 18 kW Bidirectional Charger with Partial Power Processing 188
4.2.1 Partial Power Converter Design Procedure 189
4.2.2 Parameters Design 191
4.2.3 AC Loop Inductance and Resistance Minimization 202
4.2.4 Hardware Prototype and Experimental Results 212
4.3 Three-level Buck-boost Converter with Common-Mode Noise Suppression 221
4.3.1 Proposed 3-L Buck-Boost Converter 222
4.3.2 Simplified Close-loop Control 234
4.3.3 Decoupled Active Balance Control 240
4.3.4 A 50 kW 3-L Buck-Boost Converter Prototype 247
4.4 Capacitor Voltage Auto-Balance with Mid-points Interconnection 264

4.4.1 Circuit Operation Principle 265

4.4.2 Midpoints Bridging Impact on CM Emissions 266

4.4.3 Midpoints Bridging Impact on Voltage Balance 269

4.4.4 Experimental Validation 271

4.5 Conclusion 275

Chapter 5 Conclusions and Future Work 277

5.1 Contributions 277

5.2 Future Work 278

References 279

List of Figures

Fig. 1-1. Applications of bidirectional dc/dc converter.....1

Fig. 1-2. Global EV sales in the past seven years, from 2016 to 2023.....2

Fig. 1-3. The energy trends related to data centers from 2010 to 2030.....3

Fig. 1-4. The concept of DC transformer (DCX).....4

Fig. 1-5. Three DCX applications: (a) two-stage DC-DC converter, (b) two-stage AC-DC converter, (c) partial power converter. The DCX diagram follows Fig. 1-4, and more applications can be found in Chapter 4.....5

Fig. 1-6. State-of-the-art topologies for DCX: (a) dual active bridge (DAB) converter, (b) resonant LLC/CLLC converter with active rectifier. 6

Fig. 1-7. The detailed circuit diagram of CLLC-DCX with magnetizing inductance and parasitic capacitors on both sides: $C_{oss,HV}$ and $C_{oss,LV}$. The symbols will remain the same as Fig. 2-1 in Chapter 2.....8

Fig. 1-8. Current waveforms of a typical CLLC-DCX in [12]: (a) typical waveforms, (b) experimental waveforms with an optimal switching transition, (c) experimental waveforms with non-optimized switching transition. Detailed parameters and results can be found in Fig. 2-16 and Fig. 2-17.....8

Fig. 1-9. Three state-of-the-art single transformer designs for LLC-DCX [11], [34], [35].....10

Fig. 1-10. State-of-the-art transformer's frequency versus (a) power density, (b) rating power [11], [34], [35]. Three transformer sizes and parameters can be found in Fig. 1-9. 10

Fig. 1-11. Trade-off triangle for CLLC-DCX transformer.....11

Fig. 1-12. Comparison of sinusoidal and square current waveforms.....12

Fig. 1-13. Parallel schemes: (a) converter-level parallel and (b) transformer-level parallel.....12

Fig. 2-1. Bidirectional CLLC-DCX operated with "dual-active-synchronization" (DAS) modulation.....18

Fig. 2-2. (a) Simplified CLLC-DCX circuit diagram. The LV side is referred to as the HV side with the voltage transfer ratio of the transformer *n*. (b) Current and voltage waveforms of the CLLC-DCX with DAS modulation. 18

Fig. 2-3. Equivalent circuits during the different operation modes. (a) Resonant Pulse "RP". (b) ZVS at HV and LV side "ZHL". (c) ZVS at HV side plus "ZHV+". (d) ZVS at HV side minus "ZHV-" (e) ZVS at LV side plus "ZLV+". (f) ZVS at LV side minus "ZLV-". 21

Fig. 2-4. The classification of seven ZVS transition types during t_1 to t_2. *Type IV* is defined as "Sync ZVS" transition without deadtime conduction loss $P_{dt,los}$. Corresponding waveforms are plotted in Fig. 2-5. 23

Fig. 2-5. Current and voltage waveforms of seven ZVS transition types: (a)-(g) *Type I-VII*. *Type IV* is defined as a "Sync-ZVS" transition without Q_{loss} and Pdt $_{loss}$. The classification can be found in Fig. 2-4. 23

Fig. 2-6. The Splitting magnetizing currents at zero load: (a) $i_{m,HV}$. (b) $i_{m,TLV}$. 26

Fig. 2-7. Currents decomposition: (a) total currents i_{HV} and i_{TLV}. (b) resonant current i_r (c) splitting magnetizing currents $i_{m,HV}$ and $i_{m,TLV}$. The equivalent circuit during the deadtime can be found in Fig. 2-8. 28

Fig. 2-8. Simplified equivalent circuit for "ZHL" mode during the deadtime t_1 to t_2. 28

Fig. 2-9. Proposed ACS method: (a) *case* 1, and (b) *case* 2. 31

Fig. 2-10. Simulated voltages $v_{ds,HV}$, $v_{ds,TLV}$, and current ir with proposed "Axial and Central Symmetry" method at different loads: (a) *case* 1, and (b) *case* 2. The simulation parameters can be found in Table 2-1...33

Fig. 2-11. (a) Relationship between desired f_s and t_d with different $C_{oss,eq}$. (b) Relationship between L_m and t_d with different $C_{oss,eq}$. The resonant frequency f_r is fixed at 600 kHz, and the max output power is 25 kW. 36

Fig. 2-12. Simulated voltages $v_{ds,HV}$, $v_{ds,TLV}$ in c*ase* 2 when equivalent switch output capacitance $C_{oss,eq}$ has a +5% tolerance. (a) t_d=158 ns, (b) t_d=166 ns. The simulated.....37

Fig. 2-13. Proposed optimization procedure for CLLC-DCX. A specific example can be found in Fig. 2-15. ..41

Fig. 2-14. Three 18 kW CLLC-DCX prototypes (a) *DCX I,* (b) *DCX II* and *III*. The related circuit parameters can be found in Table 2-2.....43

Fig. 2-15. Efficiency optimization for *DCX I*. Total loss is composed of both conduction and switching loss. The optimization follows the procedure in Fig. 2-13.....43

Fig. 2-16. Simulation and experimental results of *DCX I* with "Sync-ZVS" transition. (a) Voltage waveforms. (b) Current waveforms. (c) Zoomed-in voltage waveforms (d) Zoomed-in current waveforms. The CLLC-DCX operates at 18 kW with $f_{s,opt}$ as 455 kHz. The related circuit parameters can be found in Table 2-2.....45

Fig. 2-17. Simulation and experimental results of *DCX I* with *Type II* ZVS transition. (a) Voltage waveforms. (b) Current waveforms. (c) Zoomed-in voltage waveforms (d) Zoomed-in current waveforms. The

CLLC-DCX operates at 18 kW with 482 kHz. The related circuit parameters can be found in Table 2-2. 46

Fig. 2-18. Steady-state waveforms of *DCX I* at 11 kW with "Sync-ZVS" transition at 455 kHz. The related circuit parameters can be found in Table 2-2. 47

Fig. 2-19. Steady-state waveforms of *DCX II* at 15 kW: (a) "Sync-ZVS" transition at 442 kHz, (b) almost "Sync-ZVS" transition at 460 kHz, (c) *Type III* ZVS transition at 490 kHz, (d) *Type VI* ZVS transition at 400 kHz. The results match the analysis and waveforms in Fig. 2-5. 49

Fig. 2-20. Experimental results of *DCX III* at 15 kW (a) Load changing test from 15 kW to zero load (b) static waveforms at 15 kW (c) static waveforms at 7 kW (d) static waveforms at no load. The related voltage gain measurement was plotted in Fig. 2-21. 51

Fig. 2-21. Experimental voltage gain of *DCX III* from 15 kW to zero load. Input voltage $V_{DC,HV}$ remains constant at 750 V during load changing. The corresponding testing results can be found in Fig. 2-20. 51

Fig. 2-22. The efficiency of *DCX I* with "Sync-ZVS" and *Type II* transition. The corresponding testing waveforms can be found in Fig. 2-16 and Fig. 2-17. 53

Fig. 2-23. Loss breakdown of *DCX I* with "Sync-ZVS" and *Type II* transition at 18 kW. 53

Fig. 2-24. Loss distribution of *DCX I* at 18 kW: (a) "Sync-ZVS," (b) *Type II*. 53

Fig. 3-1. Circuit diagram of LLC-DCX and its corresponding waveforms. 59

Fig. 3-2. Circuit diagram of proposed EET-DCX with one EET unit. 60

Fig. 3-3. Equivalent circuits and their corresponding waveforms: (a) whole EET-DCX, (b) only HV bridge part, and (c) only LV bridge part. The simplified circuit diagram is derived from Fig. 3-2. 61

Fig. 3-4. Steady-state waveforms of EET-DCX under different load conditions. The solid line current waveforms represent a certain load case, which can be found in Fig. 3-3. 64

Fig. 3-5. Proposed EET-DCX with multiple transformers paralleled: (a) circuit diagram, (b) simplified equivalent circuit. The equivalent circuit diagram for parallel units was derived from Fig. 3-2. 68

Fig. 3-6. LLC-DCX with multiple transformers paralleled: (a) circuit diagram, (b) simplified equivalent circuit. 69

Fig. 3-7. Resonant tank impedance Z_{tank} with a tolerance of L_k:(a) amplitude of Z_{tank} (b) variation of Z_{tank}. 70

Fig. 3-8. Simulated currents and voltages of the proposed EET-DCX 72

Fig. 3-9. Simulated currents and voltages of the LLC-DCX. The corresponding parameters can be found in Table 3-1.....72

Fig. 3-10. Equivalent circuit of EET-DCX with the consideration of semiconductor output capacitance. The original simplified equivalent circuit can be found in Fig. 3-2. 75

Fig. 3-11. Simulated currents and voltages of the LLC-DCX. The parameters are listed in Table 3-2. 75

Fig. 3-12. ZVS analysis for LV bridge of EET-DCX. The current will go through the body diodes during the deadtime, as shown in Fig. 3-11.....76

Fig. 3-13. Scalable and modular ZVS design with two split external inductances. The multiple-units parallel diagram can be modified by the unit diagram shown in Fig. 3-10. 78

Fig. 3-14. The 300 kHz experimental results of *EET-DCX I* with only one EET unit: (a) 12 kW, (b) 8 kW, (c) 4 kW. The corresponding circuit parameters can be found in Table 3-3. 80

Fig. 3-15. A 12 kW 500 kHz *EET-DCX II* prototype with four EET units plugged in: (a) whole converter, (b) details of each 3 kW EET unit. The corresponding circuit parameters can be found in 82

Fig. 3-16. Impedance analyzer measurement results for one EET unit are shown in Fig. 3-15(b).....83

Fig. 3-17. The 6 kW 500 kHz experimental results for *EET-DCX II* with only two EET units paralleled: (a) currents stacked, (b) currents overlapped. The corresponding circuit parameters can be found in...84

Fig. 3-18. The 12 kW 500 kHz experimental results of *EET-DCX II* with four EET units paralleled: (a) currents stacked, (b) currents overlapped. The corresponding circuit parameters can be found in 85

Fig. 3-19. Dynamic experimental results for *EET-DCX II*: (a) whole procedure, (b) start-up, (c) load changing from 12 kW full load to half load 6 kW, (d) shut down. The corresponding circuit parameters can be found in 87

Fig. 3-20. Experimental results of 12 kW EET-DCX with 400 kHz. The corresponding circuit parameters can be found in 87

Fig. 3-21. The setup for robustness current sharing test for *EET-DCX II*. An extra air core inductance was adopted to add a tolerance of over 100%. 90

Fig. 3-22. Impedance analyzer measurement results for the air core inductance. The prototype with air core inductance can be found in Fig. 3-21. 90

Fig. 3-23. The 12 kW 500 kHz experimental results of *EET-DCX II* after adding air core inductance to EET 1 unit: (a) currents stacked, (b) currents overlapped. 91

Fig. 3-24. Thermal simulation for each modular EET unit. 92

Fig. 3-25. Thermal results of *EET-DCX II* under 12 kW 500 kHz with four EET units paralleled. 92

Fig. 3-26. The measured efficiency of *EET-DCX II* with different output power. The prototype can be found in Fig. 3-15. 92

Fig. 3-27. Simplified EET-DCX circuit and related v_C waveforms. (b) previous triangular current modulation in [26], (c) proposed trapezoidal current modulation. 94

Fig. 3-28. Normalized transformer current i_T/I_{in} with different k. A certain case is shown in Fig. 3-27. 94

Fig. 3-29. (a) Transformer rms current $I_{T,rms}$, and (b) floating capacitor voltage V_b. 94

Fig. 3-30. ZVS analysis for LV bridge of EET-DCX with trapezoidal modulation. The related circuit diagram can be found in Fig. 3-27. 98

Fig. 3-31. Transformer-level parallel: (a) circuit diagram, (b) equivalent circuit. The parallel circuit diagram can be modified from the single unit diagram shown in Fig. 3-27. 98

Fig. 3-32. Simulated waveforms: (a) currents and voltages in a large scale of 1 ms, (b) currents when the transient L_{k2} doubled, (c) good current sharing after transient. 99

Fig. 3-33. Experimental results for each EET unit at full load 3 kW: (a) LLC-DCX configuration. LV bridge was shorted, and a resonant capacitor was added. (b) k=0.5, previous triangular current modulation in [26], (c) k=0.4, (d) k=0.3. The prototype can be found in Fig. 3-15. 101

Fig. 3-34. Experimental results for current sharing at full load 12 kW with 4 EET units paralleled: (a) k=0.2, f_s=250 kHz with stacked waveforms, (b) k=0.2, f_s=250 kHz with overlapped waveforms, (c) k=0.2, f_s=200 kHz with stacked waveforms. The prototype can be found in Fig. 3-15. 102

Fig. 3-35. EET-DCX Efficiency with different k. The prototype can be found in Fig. 3-15. 102

Fig. 3-36. Circuit diagram of the proposed RC EET-DCX. 104

Fig. 3-37. Voltage and current waveforms of the proposed RC EET-DCX are shown in Fig. 3-36. 104

Fig. 3-38. The whole procedure of the robust load-independent voltage gain: (a) whole RC EET-DCX, (b) only HV bridge part, and (c) only LV bridge part. The original circuit diagram can be found in Fig. 3-36. 107

Fig. 3-39. Steady-state waveforms of RC EET-DCX under different loads. A certain load case can be found in Fig. 3-38. 110

Fig. 3-40. RC EET-DCX normalized transformer current i_T/I_{in} with different k. 113

Fig. 3-41. Normalized current and voltage of the proposed RC EET-DCX: (a) normalized transformer rms current $I_{T,rms}$ based on input dc current I_{in}, (b) normalized peak voltage $V_{rc,peak}$ based on k=0.5 case. When k=0.5, the proposed RC EET-DCX will be a traditional CLLC-DCX. The corresponding time-domain current waveforms with different k can be found in Fig. 3-41. 113

Fig. 3-42. Transformer-level parallel solution with LLC or EET or proposed RC EET unit: (a) circuit diagrams, (b) simplified equivalent circuits. The circuit diagram with multiple units was derived from the single unit diagram shown in Fig. 3-38. 116

Fig. 3-43. Impact of the tolerance on leakage inductance L_k. 118

Fig. 3-44. Simulated currents and voltages of the proposed RC EET-DCX with the tolerance on leakage inductance. 120

Fig. 3-45. Phase shift tolerance impact on single transformer RC EET-DCX. 122

Fig. 3-46. Single transformer RC EET-DCX's normalized rms current with phase shift tolerance. 122

Fig. 3-47. Phasor diagram of the current sharing analysis with the phase shift tolerance. 125

Fig. 3-48. Simulated current sharing results of the proposed RC EET-DCX with the tolerance on phase shift. 125

Fig. 3-49. A 12 kW DCX prototype with four configurable transformer units paralleled (a) whole converter, (b) detailed design of the proposed RC EET unit and EET unit. 128

Fig. 3-50. The experimental results of RC EET-DCX with four paralleled transformers (k=0.26 to give a small margin for current commutation): (a) 12 kW full load with split current, (b) 12 kW full load with overlapped current, (c) 6 kW half load with split current, (d) 6 kW half load with overlapped current. 131

Fig. 3-51. The experimental results of RC EET-DCX with no margin (k=0.22) and large margin (k=0.30) design (a) 12 kW full load with no margin k=0.22, (b) 6 kW half load with no margin k=0.22, (c) 12 kW full load with large margin k=0.30, (d) 6 kW half load with large margin k=0.30. 133

Fig. 3-52. Load changing results of the proposed 12 kW RC EET-DCX from 12 kW to 6 kW. 133

Fig. 3-53. The full load 12 kW experimental results of the typical EET-DCX with (a) split current and (b) overlapped current. 135

Fig. 3-54. The measured efficiency of *EET-DCX II* with different output power. 135

Fig. 3-55. Scalable DCX structure with different topologies, including proposed EET-DCXs family. 138

Fig. 3-56. Proposed two resonant-type hybrid topologies: (a) hybrid EET-DCX and (b) hybrid RC EET-DCX. 138

Fig. 3-57. (a) simplified hybrid EET-DCX circuit and related v_C waveforms. (b) typical EET-DCX without C_r (f_n=0) in [26] and [56], (c) Proposed resonant-type hybrid EET-DCX ($f_n \neq 0$). 142

Fig. 3-58. Normalized transformer current i_T/I_{in} with different k and different f_n: (a) f_n=0, (b) f_n=0.5, (c) f_n=0.8, and (d) f_n=1. 143

Fig. 3-59. Hybrid EET-DCX: (a) Normalized transformer rms current I_{rms}/I_{in}, and (b) normalized floating capacitor voltage V_b/V_b(0.5,0). 148

Fig. 3-60. (a) simplified hybrid RC EET-DCX circuit and related v_C waveforms, (b) typical RC EET-DCX without C_r (f_n=0), and (c) Proposed hybrid RC EET-DCX ($f_n \neq 0$). 150

Fig. 3-61. Normalized hybrid RC EET-DCX transformer current i_T/I_{in} with different k and different f_n: (a) f_n=0, (b) f_n=0.5, (c) f_n=0.8, and (d) f_n=1. 151

Fig. 3-62. Numerical solution of f_{rcn} with different k and f_n. 157

Fig. 3-63. Hybrid RC EET-DCX: (a) Normalized transformer rms current $I_{rms,rc}/I_{in}$, and (b) normalized floating capacitor voltage $V_{b,rc}/V_b$(0.5,0). 157

Fig. 3-64. Design procedures for hybrid EET-DCX and hybrid RC EET-DCX. 160

Fig. 3-65. Normalized rms current based on I_{in} with different k and f_n: (a) 3-D plot, (b) 2-D projection for hybrid EET-DCX, and (c) hybrid RC EET-DCX. 162

Fig. 3-66. Current waveforms for both hybrid EET-DCX and hybrid RC EET-DCX with k=0.5, f_n=0.5 162

Fig. 3-67. Normalized voltage stress based V_b(0.5, 0) with different k and f_n: (a) hybrid EET-DCX, (b) hybrid RC EET-DCX. 164

Fig. 3-68. Transformer-level parallel setup for hybrid EET-DCX, hybrid RC EET-DCX, and LLC-DCX. 165

Fig. 3-69. Simulated current sharing results of hybrid EET-DCX with two transformers paralleled when k=0.2. The corresponding parameters are listed in Table 3-7. 168

Fig. 3-70. The Fourier spectrum of hybrid EET-DCX current i_{T1} and i_{T2} based on f_s=500 kHz. The time-domain current waveforms can be found in Fig. 3-69. 168

Fig. 3-71. Simulated current sharing results of hybrid RC EET-DCX with two transformers paralleled when k=0.2. The corresponding parameters are listed in Table 3-7. 169

Fig. 3-72. The Fourier spectrum of hybrid RC EET-DCX current i_{T1} and i_{T2} based on f_s=500 kHz. The time-domain current waveforms can be found in Fig. 3-69.....169

Fig. 3-73. Simulated current sharing results of LLC-DCX with two parallel transformers. The corresponding parameters are listed in Table 3-7. 170

Fig. 3-74. Two 12 kW DCX prototypes with four configurable transformer units paralleled: (a) whole converter, (b) detailed design of the hybrid EET and hybrid RC EET. The corresponding parameters are listed in Table 3-8. 172

Fig. 3-75. The full load 12 kW experimental results (f_s=250 kHz) of the hybrid EET-DCX with different k when f_n=0 (without resonant capacitor C_r): (a) k=0.5, (b) k=0.3, (c) k=0.15. The corresponding parameters are listed in Table 3-8.....174

Fig. 3-76. Corresponding current sharing performance after overlapping the split currents in Fig. 21: (a) k=0.5, (b) k=0.3, (c) k=0.15. The corresponding parameters are listed in Table 3-8.....175

Fig. 3-77. The full load 12 kW experimental results of the hybrid EET-DCX with different k when f_n=0.8 (with resonant capacitor C_r): (a) k=0.4, (b) k=0.3, (c) k=0.15. The corresponding parameters are listed in Table 3-8.....176

Fig. 3-78. The half load 6 kW experimental results of the hybrid EET-DCX with k=0.15: (a) split currents, (b) overlapped currents. The corresponding parameters are listed in Table 3-8. 177

Fig. 3-79. Corresponding current sharing performance after overlapping the split currents in Fig. 21: (a) k=0.5, (b) k=0.3, (c) k=0.15. The corresponding parameters are listed in Table 3-8.....177

Fig. 3-80. Full load 12 kW and half load 6 kW testing with f_n=0.6 and k=0.2: (a) full load with split currents, (b) full load with overlapped currents, (c) half load with split currents. The corresponding parameters are listed in Table 3-8. 179

Fig. 3-81. Full load 12 kW results with f_n=0.4: (a) k=0.3 with split currents, (b) k=0.3 with overlapped currents, and (c) k=0.2 with split currents. The corresponding parameters are listed in Table 3-8. 180

Fig. 3-82. Experimental results for hybrid RC EET-DCX without C_r (f_n=0) when k=0.2: (a) full load (3 kW per unit), (b) half load (1.5 kW per unit). The corresponding parameters are listed in Table 3-8. 182

Fig. 3-83. Experimental results for hybrid RC EET-DCX with C_r (f_n=0.6) when k=0.2: (a) full load (3 kW per unit), (b) half load (1.5 kW per unit). The corresponding parameters are listed in Table 3-8. 183

Fig. 3-84. Measured efficiency of hybrid EET-DCX with different f_n and different k: (a) f_n=0, (b) f_n=0.8, (c) f_n=0.6, and (d) f_n=0.4. The corresponding testing results are shown in Fig. 3-75 to Fig. 3-81.....184

Fig. 3-85. Measured efficiency of hybrid RC EET-DCX with different f_n. The corresponding testing results are shown in Fig. 3-75. 184

Fig. 4-1. Bi-directional Resonant Isolated IPOS PP Converter. 189

Fig. 4-2. Proposed Design Procedure for PP Converter. The circuit diagram can be found in Fig. 4-1. 190

Fig. 4-3. Four potential candidates for post regulator. 193

Fig. 4-4. Two turns ratio design (a) N_{MP} = 5:2, N_{PP} = 5:1 (b) N_{MP} = 2:1, N_{PP} = 10:1. The turns ratio can be found in the circuit diagram as shown in Fig. 4-3. 193

Fig. 4-5. Two turns ratio design with different topologies: (a) post-regulator loss, (b) partial power ratio, (c) rms value of i_{PP}, and (d) total partial power loop loss. 195

Fig. 4-6. Modification of post-regulator. 196

Fig. 4-7. Post-regulator loss with different phase numbers. An example of 3 phase interleaved buck converter is shown in Fig. 4-6. 196

Fig. 4-8. Final design of the PP converter. The simplified circuit diagram can be found in Fig. 4-1. 197

Fig. 4-9. Decoupling Procedure for DCXs (a) Equivalent ZVS circuit during dead time (b) after simplification (c) after decoupling. The whole circuit diagram is shown in Fig. 4-8. 198

Fig. 4-10. Relationship between MP DCX Loss and magnetizing inductance with different switch parallel numbers, (a) sweep m_1, (b) sweep m_2. 201

Fig. 4-11. Simulated voltage and current waveforms of the MP DCX at 18 kW together with the corresponding gate control signals ($L_{m,MP}$ =20 µH and t_d =100 ns). The related parameters are listed in Table 4-3..201

Fig. 4-12. Relationship between PP DCX loss and battery voltage with different parallel numbers. 202

Fig. 4-13. Proposed 2-D flux cancelation method for 650 V GaN-based full-bridge layout. 204

Fig. 4-14. Cross-section of other three possible layouts for 650 V GaN-based full-bridge: (a) method 1, (b) method 2, and (c) method 3. The proposed method for comparison can be found in Fig. 4-13.....206

Fig. 4-15. Q3D simulation results for surface loss density: (a) proposed 2-D flux cancelation method, (b) method 1, (c) method 2, (d) method 3. The corresponding layout methods can be found in Fig. 4-13 and Fig. 4-14. 207

Fig. 4-16. Winding structures: (a) non-interleaved, (b) maximum interleaved.....209

Fig. 4-17. The relationship between transformer losses and primary turns. The corresponding winding structures with different configurations can be found in Fig. 4-18. 210

Fig. 4-18. Six potential winding topologies for planar E core. The loss breakdown with these structures is shown in Fig. 4-17.....210

Fig. 4-19. FEA simulation results for transformer losses and leakage inductance with six potential topologies in Fig. 4-18. 210

Fig. 4-20. The proposed "intra-leaving" PSPS structure is where the positions of S_1 and S_2 alternate with each turn within a layer, as opposed to interleaved, which only alternates winding positions between layers. 211

Fig. 4-21. 18 kW PP converter prototype operated in 500 kHz. The circuit parameters are listed in Table 4-6. 213

Fig. 4-22. Current sharing results between S_1 and S_2 windings at 18 kW: (a) without Intra-leaving and (b) with intra-leaving. The circuit parameters are listed in Table 4-6. 215

Fig. 4-23. Steady-state waveforms of the PP converter at 18 kW when d = 0.....215

Fig. 4-24. Thermal results for MP DCX secondary side at 18kW. 216

Fig. 4-25. Forward operation from V_{bus} to V_{bat}: (a) dynamic voltage regulation (b) output 450 V at 25 kW when d = 1 (c) output 413 V at 21 kW when d = 0.5 (d) output 431 V at 23 kW when d = 0.75. The circuit parameters are listed in Table 4-6. 217

Fig. 4-26. Reverse operation from V_{bat} to V_{bus} when d = 0.5 at 16 kW. 217

Fig. 4-27. Efficiency of the PP converter with respect to output power determined with Keysight PA 2203A power analyzer.....219

Fig. 4-28. Loss breakdown with different battery voltage at 18 kW. The calculation is based on the circuit parameters listed in Table 4-6. 220

Fig. 4-29. (a) The circuit diagram of a typical four-switch buck-boost (FSBB) converter, (b) the corresponding inductor current i_L with a quadrangle control. 223

Fig. 4-30. Proposed 3-L buck-boost converter: (a) with separate inductor, (b) with coupled inductors, (c) simplified equivalent circuit, (d) DM and CM equivalent circuits. The proposed 3-L circuit diagram can be derived from the original FSBB shown in Fig. 4-29. 226

Fig. 4-31. The equivalent circuit diagrams of four basic modes: (a) *Mode I* (t_1-t_2), (b) *Mode II* (t_2-t_3), (c) *Mode III* (t_3-t_4), (d) *Mode IV* (t_4-t_5). The original circuit diagram is shown in Fig. 4-30. 226

Fig. 4-32. The corresponding waveforms of the 3-L buck-boost converter: (a) step-down case when $V_{in}>V_{out}$, (b) unit-gain case when $V_{in}=V_{out}$, (c) step-up case when $V_{in}<V_{out}$. The circuit diagram is shown in Fig. 4-30. 227

Fig. 4-33. The relationship between (a) $P_{max,ZVS}$ with different L_{DM} and V_{out}, (b) $P_{max,ZVS}$ and L_{DM}, and (c) $P_{max,ZVS}$ and V_{out}. 231

Fig. 4-34. Inductance current waveforms with different load conditions: (a) step-down, (b) unit-gain, (c) step-up. 232

Fig. 4-35. The relationship between marginal power P_{mar} and output voltage V_{out}. The corresponding current waveforms, including marginal power case, can be found in Fig. 4-34. 232

Fig. 4-36. The minimum rms current calculation blocks for quadrangle control FSBB converter: (a) the traditional calculation, (b)the simplified calculation. 235

Fig. 4-37. The relationship between marginal power P_{mar} and output voltage V_{out}. The original current waveforms can be found in Fig. 4-29(b) with k=0. 235

Fig. 4-38. The flowchart of the simplified minimum rms current calculation 235

Fig. 4-39. The inductor current i_L with different ZVS factor k: (a) V_{in}=900V, V_{out}=1 kV, P=50 kW, and (b) V_{in}=900 V, V_{out}= V, P=40.5 kW. 238

Fig. 4-40. The relationship between I_{ZVS} and k under different load conditions and output voltages: (a) before normalization, (b) after normalization. The time-domain current waveforms are shown in Fig. 4-39. 238

Fig. 4-41. Close-loop control diagram with simplified minimum rms current calculation block. The simplified minimum RMS calculation block can be found in Fig. 4-36(b). 239

Fig. 4-42. Circuit diagram of the 3-L buck-boost converter with decoupled balance control. 241

Fig. 4-43. The corresponding waveforms of the gate signals, inductor current i_L, and inductor voltage V_L. The circuit diagram can be found in Fig. 4-42. 241

Fig. 4-44. Decoupled active balance control: (a) input side, (b) output side. The circuit diagram after introducing balance control is shown in Fig. 4-42. 243

Fig. 4-45. Decoupled active balance control: (a) input side, (b) output side. The closed-loop control diagram can be found in Fig. 4-41. 245

Fig. 4-46. Simulation results for the decoupled active balance control under 45 kW unit gain case (900 V to 900 V). The parameters in the simulation are listed in Table 4-8. 246

Fig. 4-47. 50 kW 3-L buck-boost converter prototype with planar coupled inductors: (a) whole power stage, (b) heavy copper coupled inductors. The circuit parameters are listed in Table 4-9. 248

Fig. 4-48. Diagrams of the experimental setups: (a) proposed 3-L buck-boost converter, (b) typical FSBB converter. The prototype can be found in Fig. 4-47. 248

Fig. 4-49. Experimental results of the 3-L buck-boost converter with decoupled balance control: (a) V_{out}=1 kV, (b) V_{out}=900 V, (c) V_{out}=800 V, (d) V_{out}=500 V. The circuit parameters are listed in Table 4-9. 251

Fig. 4-50. Testing results of the 3-L buck-boost converter without decoupled balance control: (a) V_{out}=1 kV, (b) V_{out}=900 V, (c) V_{out}=800 V, (d) V_{out}=500 V. The circuit parameters are listed in Table 4-9. 252

Fig. 4-51. Testing results of the typical FSBB converter: (a) V_{out}=900 V, (b) V_{out}=800 V, (c) V_{out}=500 V. The circuit parameters are listed in Table 4-9. 253

Fig. 4-52. Measured CM current results under different cases: (a) V_{out}=900 V, (b) V_{out}=800 V, (c) V_{out}=500 V. 254

Fig. 4-53. Dynamic close-loop experimental results: (a) soft start-up, (b) output voltage regulation. The circuit parameters are listed in Table 4-9. 255

Fig. 4-54. Experimental results (V_{out}=900 V, P=45.5 kW t_d=600 ns) without decoupled active balance control: (a) large scale voltage and current waveforms, (b) zoomed $v_{ds,2}$ and $v_{ds,3}$ during hard switching

transition. (c) zoomed $v_{ds,6}$ and $v_{ds,7}$ during soft-switching transition. The circuit parameters are listed in Table 4-9. 257

Fig. 4-55. Experimental results (V_{out}=1 kV, P=50 kW t_d=600 ns) with decoupled active balance control: (a) large scale voltage and current waveforms, (b) zoomed $v_{ds,6}$ and $v_{ds,7}$ during hard switching transition. (c) zoomed $v_{ds,6}$ and $v_{ds,7}$ during soft-switching transition. The circuit parameters are listed in Table 4-9. 258

Fig. 4-56. Experimental results with different "ZVS factor" k under V_{out}=900 V, P=45 kW, t_d=600 ns: (a) k=0.2, (b) k=0.3, (c) k=0.4 (d) k=0.5. The circuit parameters are listed in Table 4-9. 259

Fig. 4-57. Thermal testing results for the planar coupled inductor under 50 kW step-up case (900 V to 1 kV). 260

Fig. 4-58. The efficiency of the 3-L buck-boost converter and 2-L FSBB with different output voltage. The 2-L FSBB cannot run at 1 kV because the SiC MOSFETs rating is only 1.2 kV.....261

Fig. 4-59. Loss breakdown of the 3-L buck-boost converter at 50 kw with different output voltages. The calculation was based on the parameters in Table 4-9. 261

Fig. 4-60. Proposed 3-L buck-boost converter and its operating principle (a) circuit diagram, (b) driving signals and i_L waveforms with quadrangle modulation, (c) four operating modes. 265

Fig. 4-61. CM and DM equivalent circuits. The original circuit diagram can be found in Fig. 4-60. 267

Fig. 4-62. CM lump model with parasitics, LISN, and load. The simplified circuit without the consideration of parasitic parameters is shown in Fig. 4-61. 267

Fig. 4-63. Automatic dc-link voltage balance with input-output mid-points connected: (a) equivalent circuit with the consideration of leakage inductance, (b) equivalent circuit with perfect coupling, (c) terminal voltages v_{AC}, v_{BD} and buck-boost inductor current waveforms.....269

Fig. 4-64. SiC-based converter prototype and its measurement setups: (a) 50 kW prototype, (b) test setup for proposed 3-L buck-boost converter, (c) test setup for conventional 2-L FSBB. 272

Fig. 4-65. Experimental results under V_{out}= 1 kV P=50 kW (a) without midpoint connection and without balance control, (b) without midpoint connection and with balance control, (c) with midpoint connection and natural voltage balance. The circuit parameters are listed in Table 4-11. 273

Fig. 4-66. Experimental results with bridged midpoints under V_{out}=900 V P=45 kW: (a) N_T: N_B=7:8, (b) N_T: N_B=8:7. The circuit parameters are listed in Table 4-11. 274

Fig. 4-67. Leakage inductance impact on midpoint voltage balance. The circuit parameters are listed in Table 4-11. 274

Fig. 4-68. CM noise measurement results under V_{out}=900 V 45.5 kW. The circuit parameters are listed in Table 4-11. 276

Fig. 4-69. Extended midpoint interconnection topologies: symmetric 3-L buck or boost converter with coupled inductor. 276

List of Tables

Table 1-1 Technical Specifications of State-of-the-Art DC Fast Chargers **2**

Table 2-1 Simulation Parameters of Two Cases **34**

Table 2-2 The Parameters of Three Prototypes Including Parasitics **42**

Table 3-1 The Parameters of Three Prototypes **71**

Table 3-2 ZVS SIMULATION PARAMETERS OF EET-DCX **75**

Table 3-3 The Parameters of *EET-DCX I* with One EET Unit **80**

Table 3-4 The Parameters of *EET-DCX II* with Four EET Unit **82**

Table 3-5 Current Sharing Simulation Parameters **120**

Table 3-6 Parameters of RC EET-DCX with Four EET Units **128**

Table 3-7 Current Sharing Simulation Parameters **165**

Table 3-8 Parameters of RC EET-DCX with Four EET Units **171**

Table 4-1 Design Specifications of the Battery Charger **193**

Table 4-2 Parameters of Two Turns Ratios Design **195**

Table 4-3 Optimization Results of MP and PP DCX **201**

Table 4-4 Q3D Results of Parasitic Parameters **206**

Table 4-5 Current Sharing Performance and Coupling Coefficient **211**

Table 4-6 Technical Details of Implemented PP Converter **213**

Table 4-7 Specifications of the Proposed 3-L Buck-Boost Converter **230**

Table 4-8 Balancing Effect of Four Intermediate Operation Modes **243**

Table 4-9 Technical Details of 3-L Buck-Boost Converter **249**

Table 4-10 Comparison of Proposed 3-L Buck-Boost Converter and 2-L FSBB **262**

Table 4-11 Specifications of the Proposed 3-L Buck-Boost Converter **272**

Nomenclature

In Chapter 2

$C_{oss,HV(LV)}$	parasitic output capacitance on the HV (LV) side
n	transformer turns ratio
L_m	magnetizing inductance
$L_{r,HV(LV)}$	split leakage inductance on the HV (LV) side
$C_{r,HV(LV)}$	resonant capacitors on the HV (LV) side
$V_{DC,HV(LV)}$	DC bus voltage on the HV (LV) side
f_r	resonant frequency
$v_{AB(CD)}$	terminal AC voltage on the HV (LV) side
$v_{ds,HV(LV)}$	drain to source voltage on the HV (LV) side
$v_{Cr,HV(LV)}$	voltage across the resonant capacitor $C_{r,HV(LV)}$
i_m	magnetizing current
I_m	the peak value of the magnetizing current
t_d	dead time
Q_{mag}	the electric charge provided by magnetizing current during the dead time
T_s	switching period
f_s	switching frequency
$i_{HV(LV)}$	resonant current through the HV (LV) side
Q_{loss}	unused part of Q_{mag} during deadtime
$P_{dt,loss}$	deadtime loss
V_f	forward voltage of the body diode
$i_{m,HV(LV)}$	split magnetizing current on the HV (LV) side

i_r	resonant current dedicated to transferring real power
Q_r	the electric charge caused by i_r
$L_{r,eq}$	equivalent resonant inductance
$C_{oss,eq}$	equivalent parasitic output capacitance
T_{ring}	deadtime ringing period
f_{ring}	deadtime ringing frequency
I_{ring}	the current amplitude of the ringing current during deadtime
P	output power
$I_{rms,HV(LV)}$	rms current on the HV (LV) side
P_{cond}	conduction loss
$R_{ds,HV(LV)}$	on-state resistance for HV (LV) switch
P_{sw}	switching loss
P_{total}	total semiconductor loss
$t_{d,opt}$	optimized deadtime
$L_{m,opt}$	optimized magnetizing inductance
$f_{s,opt}$	optimized switching frequency

In Chapter 3

$V_{in(out)}$	input (output) DC voltage
$I_{in(out)}$	input (output) DC current
L_k	leakage inductance
C_r	resonant capacitor
$v_{pri(sec)}$	AC terminal voltage on the primary (secondary) side
v_{Cr}	the voltage across the resonant capacitor
i_m	magnetizing current
$C_{oss,total}$	the total output capacitance
$i_{pri(sec)}$	transformer current on the primary (secondary) side
C_b	floating DC capacitor
V_b	floating DC voltage across C_b
v_C	output AC voltage of the integrated LV full bridge
i_T	transformer current after ignoring the magnetizing current
$i_{T,I}$	current components with only HV bridge excitations
$i_{T,II}$	current components with only LV bridge excitations
$P_{T,I}$	power delivered to the receiving side by the current $i_{T,I}$
$P_{T,II}$	power delivered to the receiving side by the current $i_{T,II}$
N	parallel units number
v_{AB}	the terminal voltage across "*A*" and "*B*" in current-sharing analysis
R_w	winding resistance
$t_{d,LV}$	LV bridge dead time
$L_{pri(sec)}$	split external inductance on the primary (secondary) side

$t_{d,opt}$	optimized deadtime
i_{total}	total transformer current with four parallel units
L_{air}	inductance of the air core inductor
r_{air}	parasitic resistance of the air core inductor
I_{peak}	transformer peak current
$I_{T,rms}$	transformer rms current
k	duty of the LV bridge output AC voltage v_C
$C_{o1(2)}$	two symmetric parallel capacitors of a bidirectional AC switch
v_{rc}	resonant voltage across bidirectional AC switch
$V_{rc,peak}$	peak resonant voltage across bidirectional AC switch
f_{rc}	resonant commutation frequency
$i_{T,rc}$	transformer current of RC EET-DCX
m	tolerance on leakage inductance
$v_{rc,m}$	resonant voltage with leakage inductance tolerance
$f_{rc,m}$	resonant commutation frequency with leakage inductance tolerance
$i_{T,m}$	transformer current with leakage inductance tolerance
φ	phase shift tolerance
$v_{rc,\varphi}$	resonant voltage across bidirectional AC switch with phase shift tolerance
$i_{T,\varphi}$	transformer current with phase shift tolerance
$v_{rc,\varphi}$	resonant voltage across bidirectional AC switch with phase shift tolerance
f_n	normalized resonant frequency
f_{rcn}	normalized resonant commutation frequency

In Chapter 4

V_{bat}	battery voltage
V_r	regulator output voltage
V_{MP}	the output voltage of MP DCX
P_{MP}	majority power transferred by the majority power (MP) DCX
P_{PP}	partial power transferred by the partial power (PP) DCX
i_{MP}	resonant current through MP DCX
i_{PP}	resonant current through PP DCX
N_{MP}	turns ratios of MP DCX transformer
N_{PP}	turns ratios of PP DCX transformer
$L_{m,MP}$	magnetizing inductance of MP DCX transformer
$L_{m,PP}$	magnetizing inductance of PP DCX transformer
$v_{ds,bus}$	drain to source voltage on the DC bus side
$v_{ds,MP}$	drain to source voltage on the MP DCX side
$v_{ds,PP}$	drain to source voltage on the PP DCX side
$C_{oss,bus}$	parasitic output capacitance on the DC bus side
$C_{oss,MP}$	parasitic output capacitance on the MP DCX side
$C_{oss,PP}$	parasitic output capacitance on the PP DCX side
$P_{cond,MP}$	conduction loss of MP DCX
$P_{sw,MP}$	switching loss of MP DCX
m_1	switch parallel number on DC bus side full bridge
m_2	switch parallel number on MP DCX side full bridge
E	the total energy of the transformer

H	magnetic field strength
I_{ZVS}	required ZVS current
i_L	inductor current
$P_{max,ZVS}$	the maximum power that the FSBB converter could achieve ZVS
L	the inductance of the four-switch buck-boost converter
D_1	the duty cycle for half bridge $S_{1,2}$
D_2	the duty cycle for half bridge $S_{3,4}$
φ	phase shift between D_1 and D_2
i_L	current through inductor L
L_{DM}	differential mode (DM) inductance
L_{CM}	common mode (CM) inductance
L_s	self-inductance
M	mutual inductance
N	turns number of the coupled inductors
i_{CM}	DM current
i_{DM}	CM current
$m_{I\text{-}IV}$	the current slope of *Mode I-IV*
P_{mar}	marginal power
$V_{iT(B)}$	input side split capacitor voltage on the top (bottom) side
$V_{oT(B)}$	output side split capacitor voltage on the top (bottom) side
ΔD_1	duty difference on D_1
ΔD_2	duty difference on D_2

Chapter 1

Introduction

1.1 Bidirectional DC-DC Converter

With the fast development of electric vehicles (EV) [1]–[5], energy storage systems (ESS) [6]–[9], and data center applications [10]–[14], DC power systems are becoming more and more popular [15]–[17]. As shown in **Fig. 1-1**, a bidirectional DC-DC converter can be widely adopted in low-voltage DC(LVDC), medium-voltage DC (MVDC), and high-voltage DC(HVDC) systems. As a bridge between two DC power systems, a bidirectional DC-DC converter interfaces two different or same-level DC buses with high efficiency. For instance, in the application of a solid-state transformer (SST), a bidirectional DC-DC converter can connect an MVDC bus to an LVDC bus that has different voltage levels. With another LVDC-to-LVDC converter, the DC power can be directly used by photovoltaic (PV) systems, energy storage systems, EV charging systems, and data center power supplies.

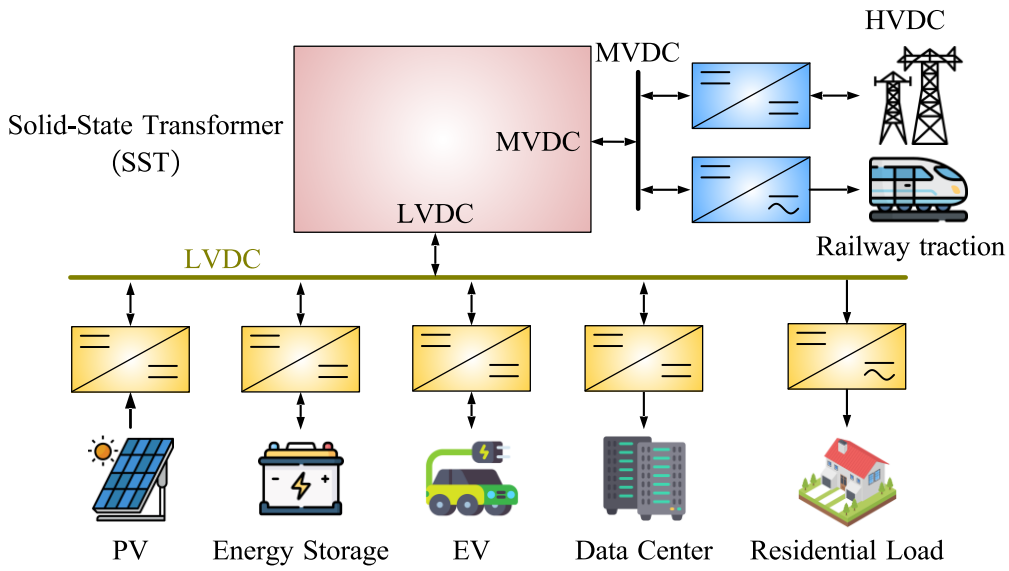


Fig. 1-1. Applications of bidirectional dc/dc converter.

1.1.1 Electrical Vehicle (EV) Applications

Due to the shortage of traditional fossil energy, EVs are emerging and playing a significant role in renewable energy. **Fig. 1-2** shows the global EV sales in the past seven years [18]. The growth has been extremely fast in the past three years, from 2021 to 2023. Compared with traditional cars, EVs have many merits, such as being more eco-friendly, having less noise and smoother motion, being more cost-effective, and lower maintenance. However, since the birth of EVs, charging station limitations and smaller driving ranges are always the main concerns for the consumer. Thanks to the development of fast-charging technology, more and more ultra-fast charging stations have been invented and built [19], as listed in **Table 1-1**. When the rating power increases from 50 kW to 350 kW, the charging time for a 200-mile range is reduced dramatically from 72 minutes

TABLE 1-1 TECHNICAL SPECIFICATIONS OF STATE-OF-THE-ART DC FAST CHARGERS

Manufacturer Model	ABB Terra 53	PHIHONG Integrated	Tesla Supercharger	EVTEC Espresso	ABB Terra HP
Power	50 kW	120 kW	135 kW	150 kW	350 kW
Input Voltage	480 Vac	380 Vac 480 Vac	380-480 Vac	400 Vac	400 Vac
Output Voltage	200-500 V 50-500 V	200-750 V	50-410 V	170-500 V	150-920 V
Output Current	120 A	240 A	330 A	300 A	375 A
Peak Efficiency	94%	93.5%	91%	93%	95%
Volume	758 L	591 L	1047 L	1581 L	1894 L
Weight	400 kg	240 kg	600 kg	400 kg	1340 kg
Time to add 200 miles	72 min	30min	27 min	24 min	10 min

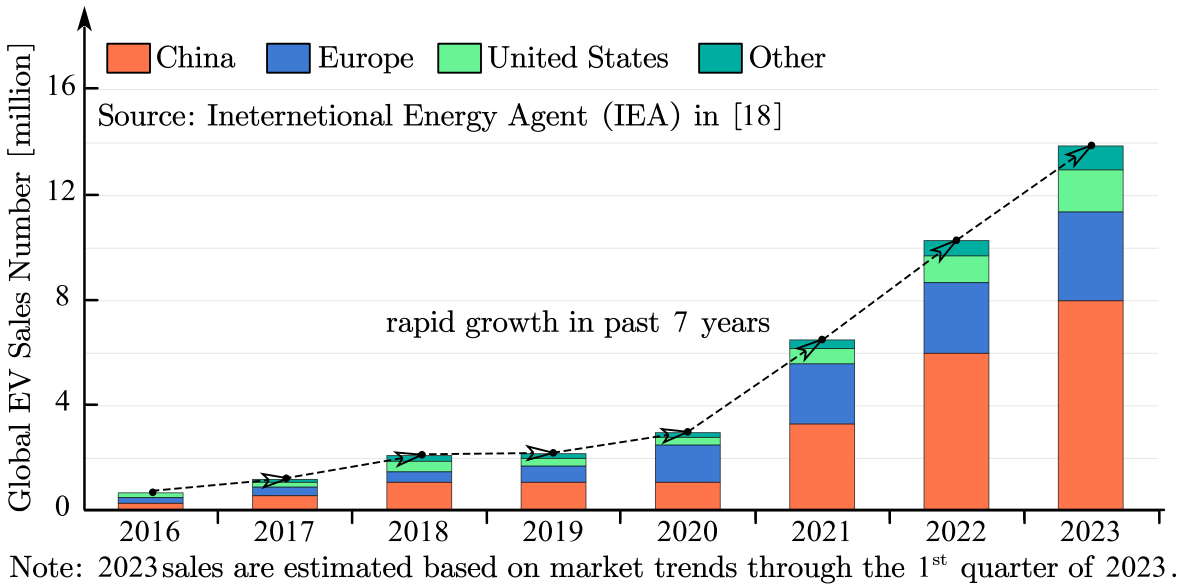


Fig. 1-2. Global EV sales in the past seven years, from 2016 to 2023.

to 10 minutes. In the process of scaling up EV charging power, a scalable and modular bidirectional DC-DC converter is desirable. Thus, the EV charging system is a high-potential application for a bidirectional DC-DC converter. If the systems have the same voltage level DC bus, increasing the output current is the most effective method to push the maximum charging power. In this case, building a high-power and high-density DC-DC converter should be very important.

1.1.2 Data Center Applications

Besides EV applications**,** data centers are playing a pivotal role in facilitating the seamless function of modern technology in the digital age. **Fig. 1-3** shows the energy trends related to the data center [20]. The data center industry has experienced substantial growth over the past decade and contributes significantly to global energy consumption. Due to the popularity of data center applications, high-end tasks can be implemented remotely with cloud calculation. In this case, the energy trends of networks have also increased in the past ten years. The prediction for the next ten years is that usage will be at least double what it is now. Many phenomena have unveiled that the artificial intelligence (AI) era is coming, and it will establish a new demand for power transfer, especially for DC-DC power supplies specified from 400 V to 48 V and 48 V to 1 V.

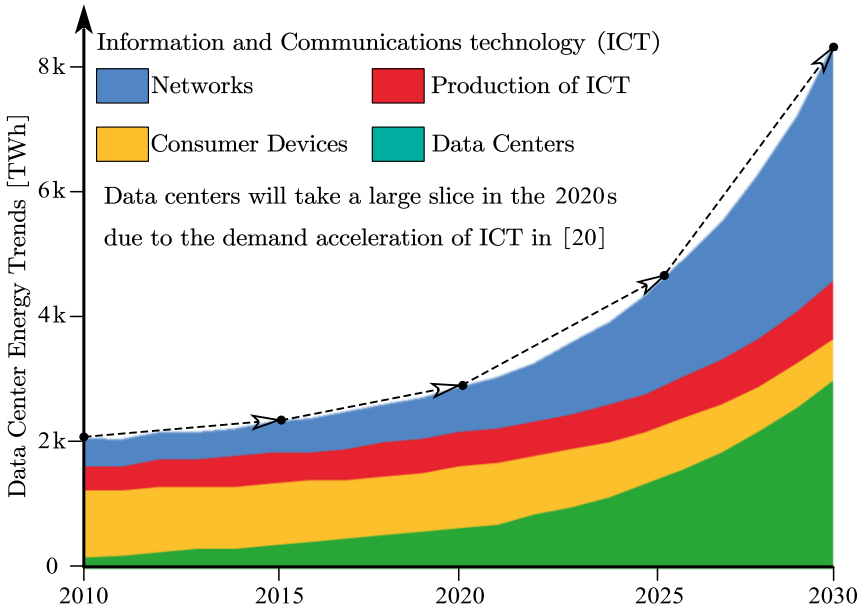


Fig. 1-3. The energy trends related to data centers from 2010 to 2030.

1.2 Concept of DC Transformer (DCX)

1.2.1 What is a DCX?

After the introduction of EV charging systems and data center power supplies, the fixed-ratio DC-DC converter, namely the DC transformer (DCX), has been widely adopted because it can bridge 2 DC buses with very high conversion efficiency. The concept and classification of DCX are both shown in **Fig. 1-4**. Since a traditional AC high-frequency transformer (HFT) can only convey AC power, two additional active full bridges are employed as one inverter and one rectifier. With the development of wide-bandgap semiconductors, such as gallium nitride (GaN) [21], [22] and silicon carbide (SiC) [23]–[25], the switching frequency for a high power converter (over 10s kW) can be pushed over 500 kHz [26]–[31]. Then, the functions of an ideal DCX provide galvanic isolation, transferring the DC power bidirectionally, achieving a high conversion efficiency, and realizing a load-independent voltage gain with simple open-loop control. Similar to a passive 4-terminal AC transformer, the DC voltage conversion ratio of an ideal DCX is only determined by the turns ratio.

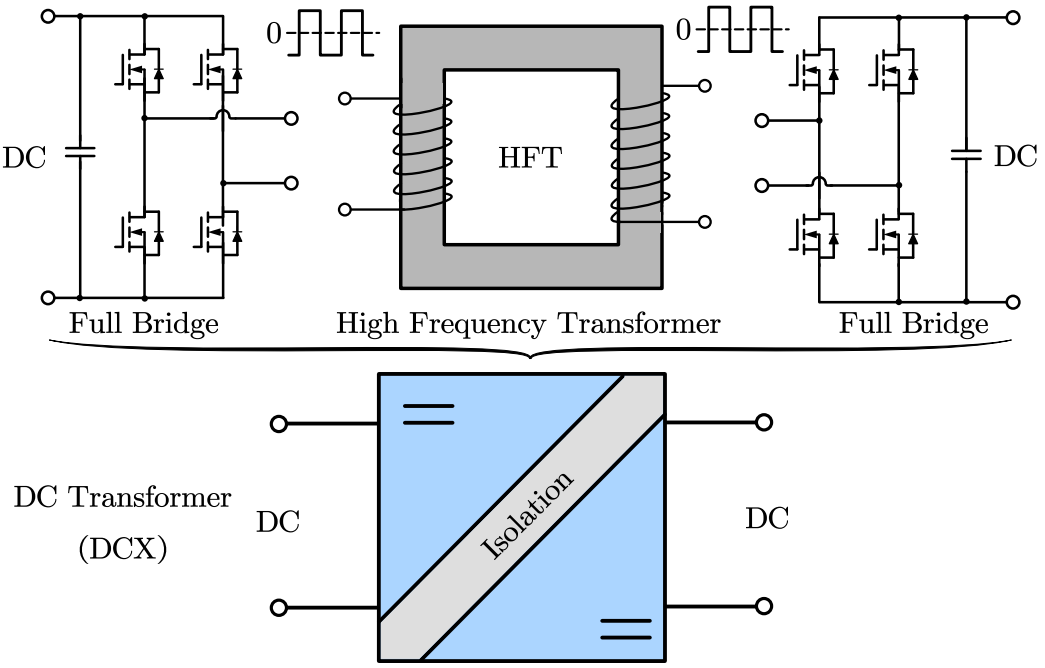


Fig. 1-4. The concept of DC transformer (DCX).

1.2.2 DCX Applications

As shown in **Fig. 1-5**, without requiring any close-loop control, a DCX can provide galvanic isolation and a load-independent constant voltage gain in many applications, such as a 2-stage DC-DC converter, a 2-stage AC-DC converter, and a partial power processing converter. As shown in **Fig. 1-5(a)**, the output regulation in 2-stage DC-DC converter can be handled by rear-end post DC-DC regulator. In the 2-stage AC-DC converter depicted in **Fig. 1-5(b)**, the rear-end AC-DC converter can process the voltage first. Finally, in a partial power converter, as shown in **Fig. 1-5(c)**, the output regulation can be realized by an input-parallel-output-series (IPOS) DC regulator. If the regulation range is not wide, such as in EV charging systems, partial power processing is a promising solution because the majority of power will only go through the DCX directly, and only partial power will be processed by the DC regulator. Furthermore, the topology selection for the DC regulator can follow the isolation requirements. If galvanic isolation is not required, a traditional buck converter can be the regulator with a good dynamic response as a "Sigma" converter [32].

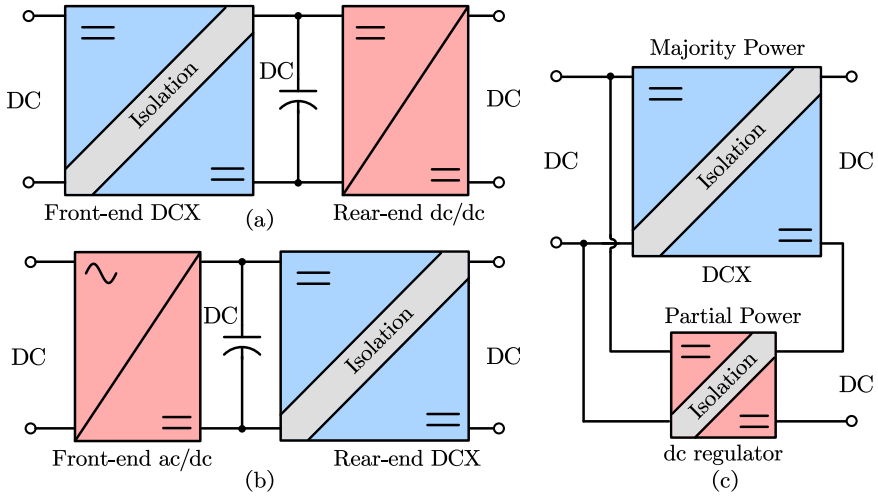


Fig. 1-5. Three DCX applications: (a) two-stage DC-DC converter, (b) two-stage AC-DC converter, (c) partial power converter. The DCX diagram follows Fig. 1-4, and more applications can be found in Chapter 4.

1.2.3 State-of-the-Art DCX Topologies

With the requirement of bidirectional power flow, traditional unidirectional topologies such as the phase-shift full-bridge converter and resonant LLC converter with a passive rectifier are not suitable. As shown in **Fig. 1-6**, with an active secondary side, dual active bridge (DAB) converters and resonant LLC/CLLC converters with active rectifiers are two popular candidates. Both of these topologies have a total of 8 switches and are capable of bidirectional power transfer.

Without consideration of parasitic parameters and dead time, the ideal voltage and corresponding current waveforms of the DAB converter are plotted in **Fig. 1-6(a)**. Several downsides of the DAB converter can be found below.

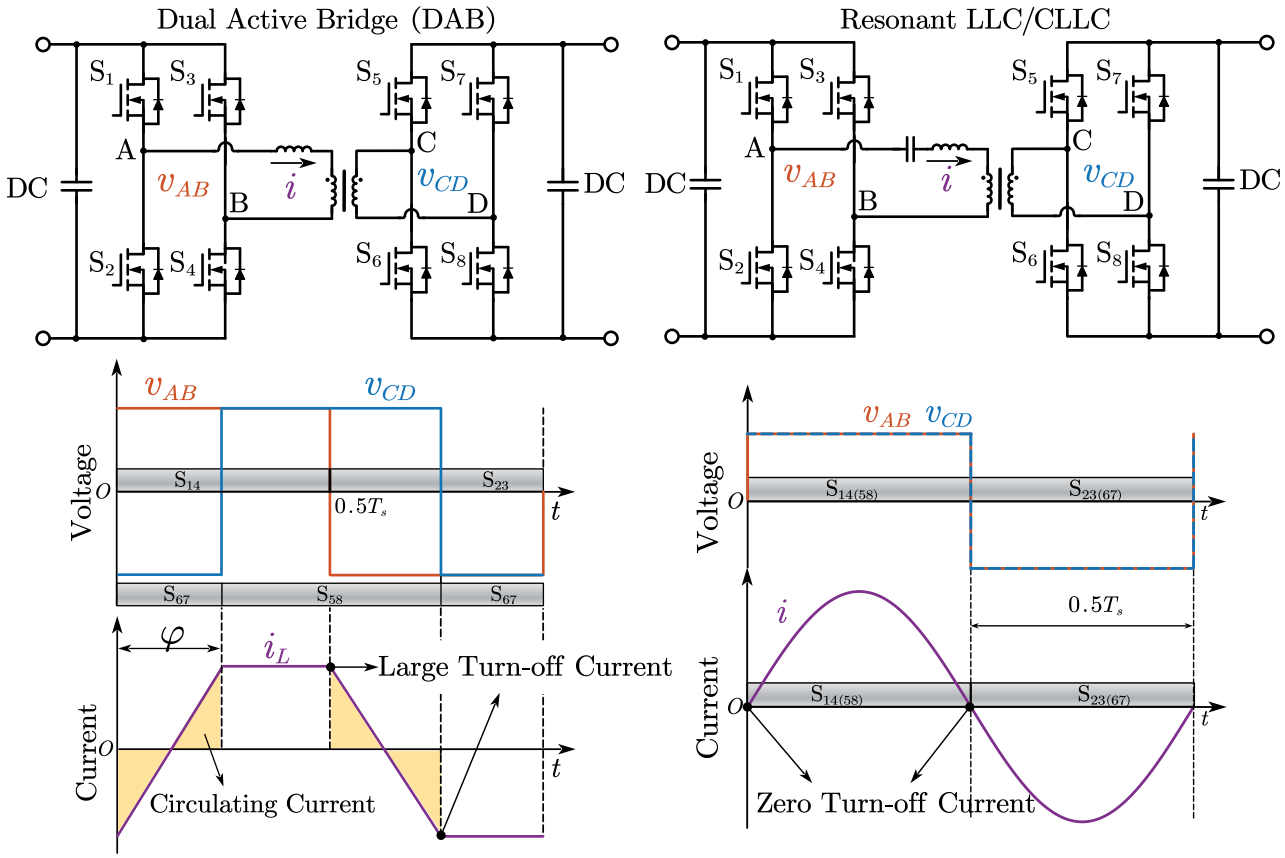


Fig. 1-6. State-of-the-art topologies for DCX: (a) dual active bridge (DAB) converter, (b) resonant LLC/CLLC converter with active rectifier.

1. Large turn-off current

Due to the phase-shift between the primary(v_{AB}) and secondary side(v_{CD}) terminal voltage, the turn-off current is equal to the peak current, as shown in Fig. 1-6(a), which will lead to large switching loss, especially on a high-frequency application.

2. Load-dependent voltage gain

The voltage conversion gain for the DAB converter is related to the load condition, which means the phase shift angle needs a feedback control to maintain a constant voltage gain.

3. No ZVS at light load

ZVS is realized by the circulating current in the DAB converter. However, under light load, the circulating current might not be enough to achieve the ZVS during the dead time.

4. Large circulating current

The circulating current shown in **Fig. 1-6(a)** cannot transfer the real power because of the phase shift between v_{AB} and v_{CD}. However, this current will increase the RMS current and cause a higher conduction loss on the transformer and both sides' full bridges. The inductance between v_{AB} and v_{CD} can be designed to be very small to decrease the circulating current when DAB operates in DCX mode. However, based on the operation principle of DAB, a very small inductance requires a very small phase shift, which means the control will be more difficult. Compared with a DAB converter, the LLC/CLLC series resonant converter (SRC) shown in **Fig. 1-6(b)** is more desirable because it has a lower circulating current and full ZVS. Furthermore, when the SRC works at (or slightly below) the resonant frequency, it can provide a constant voltage gain without requiring any closed-loop voltage control.

1.3 Challenges in CLLC-DCX Design

1.3.1 Switching Transition Noise

The first challenge for CLLC-DCX design is the switching transition noise because of the converter's parasitic parameters, such as the semiconductor's output capacitance [12]. **Fig. 1-7** depicts a detailed CLLC-DCX circuit diagram with the magnetizing inductance and parasitic capacitors on both sides. Unlike the ideal pure sinusoidal current waveform in **Fig. 1-6(b)**, the typical current waveforms for CLLC-DCX are depicted in **Fig. 1-8(a)** [12]. Due to the resonance between leakage inductance L_k and $C_{oss,HV}$/$C_{oss,LV}$, current ringing can be found during the dead time on both primary current i_{HV} and secondary current i_{LV}.

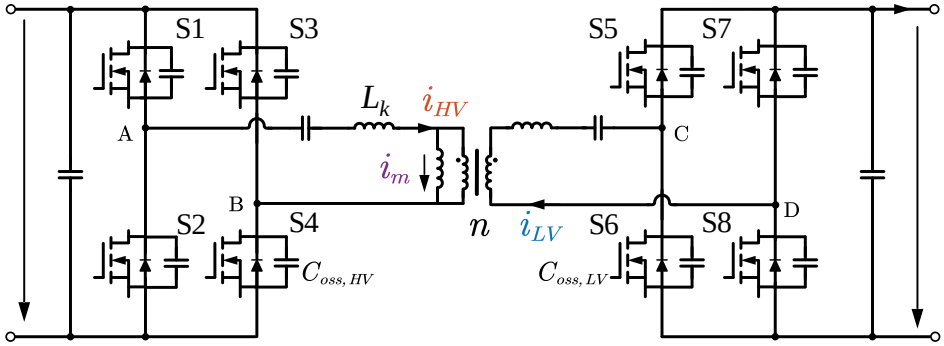
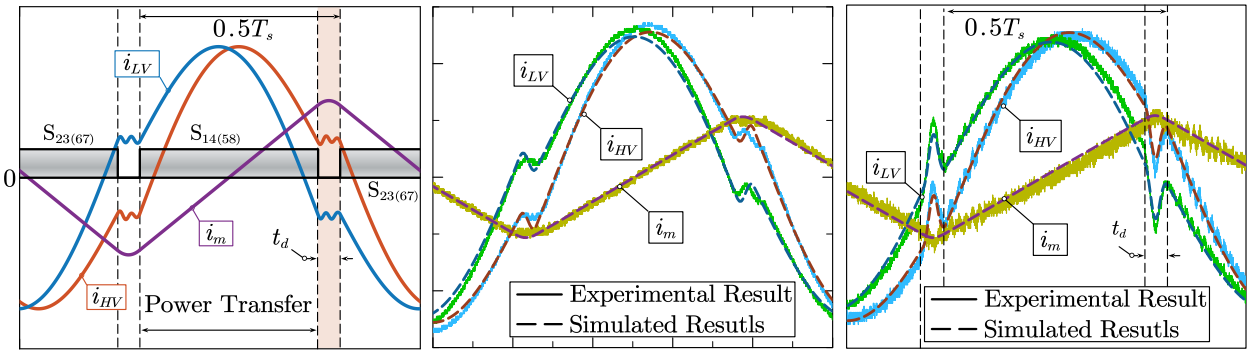


Fig. 1-7. The detailed circuit diagram of CLLC-DCX with magnetizing inductance and parasitic capacitors on both sides: $C_{oss,HV}$ and $C_{oss,LV}$. The symbols will remain the same as Fig. 2-1 in Chapter 2.



(a) (b) (c)

Fig. 1-8. Current waveforms of a typical CLLC-DCX in [12]: (a) typical waveforms, (b) experimental waveforms with an optimal switching transition, (c) experimental waveforms with non-optimized switching transition. Detailed parameters and results can be found in Fig. 2-16 and Fig. 2-17.

If the switching transition is well-designed, the current ringing during dead time can be minimized, as shown in **Fig. 1-8(b)**. However, without a general optimization procedure, the large current spike will cause poor efficiency, and the load-independent voltage gain might be lost.

1.3.2 Deadtime Loss

The deadtime loss in CLLC-DCX is defined as the power loss when the current goes through the MOSFET body diode during the dead time. In particular, WBG semiconductors are typically used for the achievement of high-frequency and high-power density. However, they have a higher forward voltage drop in the third quadrant, which brings a sizable conduction loss during dead time [12], [33]. Therefore, a comprehensive analysis of the ZVS/ZCS mechanism of CLLC-DCX that considers non-ideal current ringing and conduction loss during deadtime is desired.

1.3.3 Design Trade-off for High-Frequency and High-Power Transformer

The third challenge is the high-frequency and high-power transformer design. It is well-known that increasing frequency is an intrinsic method to push the power density because it can reduce the maximum flux density. Three state-of-the-art transformers for LLC/CLLC-DCX are shown in **Fig. 1-9** with different switching frequency and rated power [11], [34], [35]. From left to right, it can be easily found that when the switching frequency increases from 10 kHz to 48 kHz and then to 500 kHz, the corresponding transformer's power density also increases from 62 W/in3 to 156 W/in3 and then to 530 W/in^3. These power density data are also plotted in **Fig. 1-10(a)**. However, in the meantime, the rated power of the transformer in Fig. 1-10(b) reduces from 100 kW to 25 kW and then to 15 kW, which means there is a trade-off between the transformer's frequency and rated power.

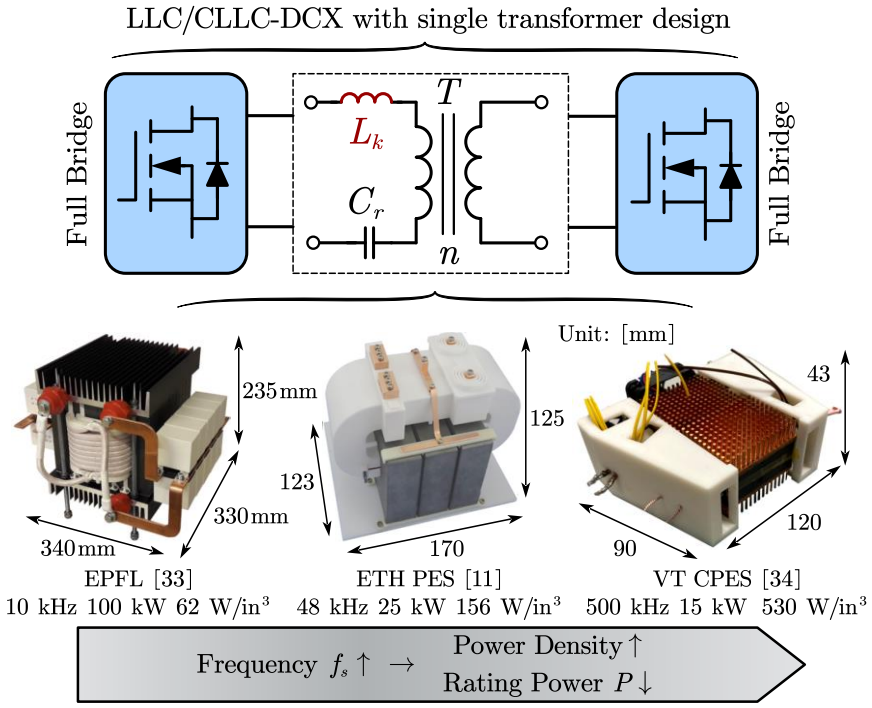


Fig. 1-9. Three state-of-the-art single transformer designs for LLC-DCX [11], [34], [35].

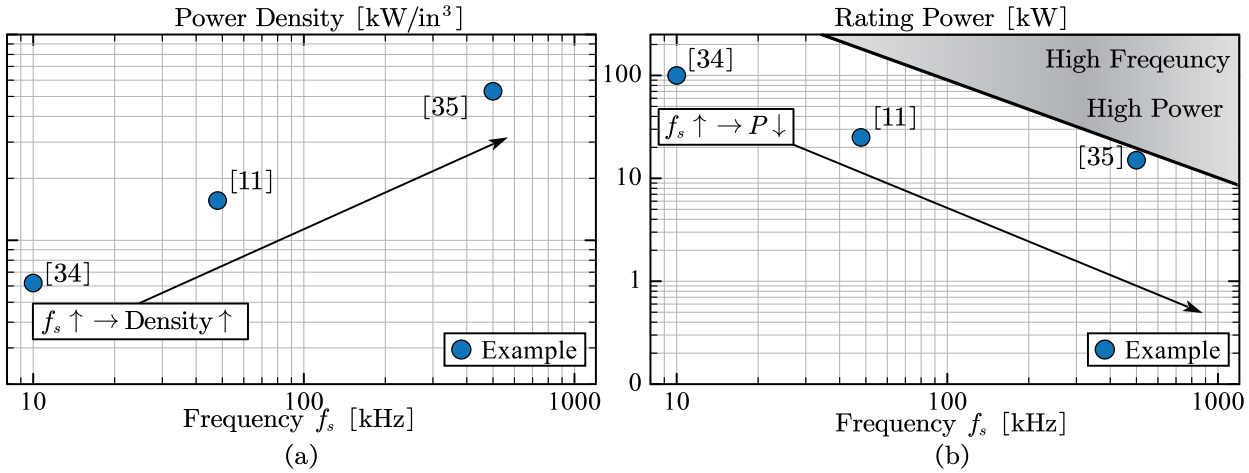


Fig. 1-10. State-of-the-art transformer's frequency versus (a) power density, (b) rating power [11], [34], [35]**. Three transformer sizes and parameters can be found in Fig. 1-9**.

Fig. 1-11 shows this trade-off triangle for high-frequency (> a few hundred kHz) transformers with a high power rating and high efficiency. An overall high-density design remains the biggest challenge.

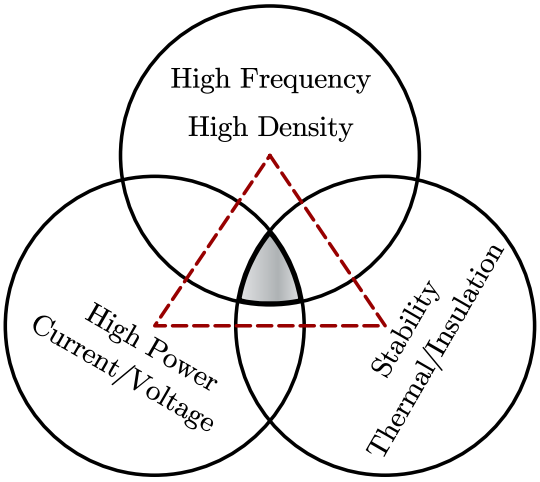


Fig. 1-11. Trade-off triangle for CLLC-DCX transformer.

1. Minimization of leakage inductance and thermal management performance

As mentioned previously, the high-frequency transformer requires the leakage inductance to be minimized so that the voltage drop on the winding can be reduced in order to deliver more power. This inevitably leads to the adoption of an interleaving configuration of winding and compact magnetic core structure to maximize magnetic coupling. However, the shrinking of the geometry size of the transformer will exacerbate the thermal issue due to a smaller heat transfer surface, which limits the power rating of the transformer and enlarges the cooling system. When the operation frequency of the transformer is higher, such design challenges become worse due to the smaller skin depth of the winding.

2. Insulation requirement and compact design

When a high-frequency transformer has a small size, the insulation design is another challenge in medium and high-voltage applications. Solid dielectric materials should be between the primary and secondary sides to reinforce the insulation level. However, these solid insulation materials will increase the thermal resistance from winding to the ambient, further limiting the total power rating of the transformer. To sum up, in the single transformer design, high-frequency and high power are inherently a trade-off, as shown in **Fig. 1-11**.

1.3.4 Large rms Current with LLC-DCX

In the resonant LLC/CLLC-DCX, the sinusoidal current has the merit of zero turn-off current if the magnetizing current is ignored. However, as shown in **Fig. 1-12**, the square waveform current will have a smaller RMS value compared to the sinusoidal waveform. However, referring to the circuit diagram in **Fig. 1-7**, the square current will suffer from a large turn-off current when switches S1 and S4, or S2 and S3, are turned off.

1.3.5 Current Sharing Issue

Parallel connection is an effective method for increasing total rating power. Compared to the traditional converter-level parallel connection in **Fig. 1-13(a)**, the transformer-level parallel solution shown in **Fig. 1-13(b)** is more desirable. This is because the single full power rating sending/receiving converter enables high-density integration and low costs due to a smaller number of gate drivers and auxiliary components.

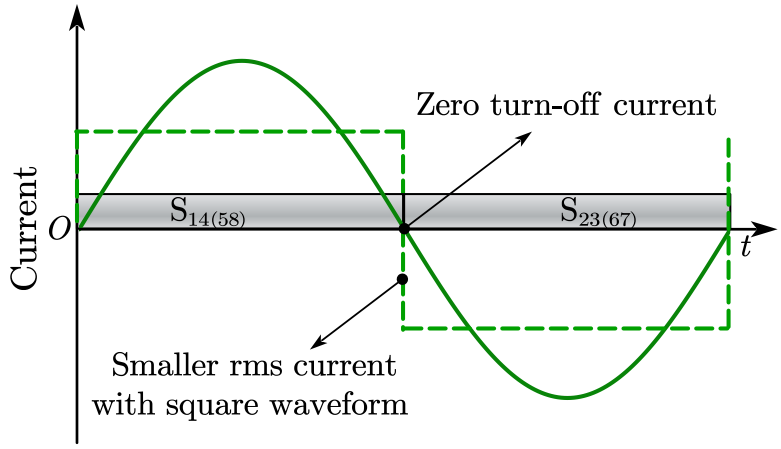


Fig. 1-12. Comparison of sinusoidal and square current waveforms.

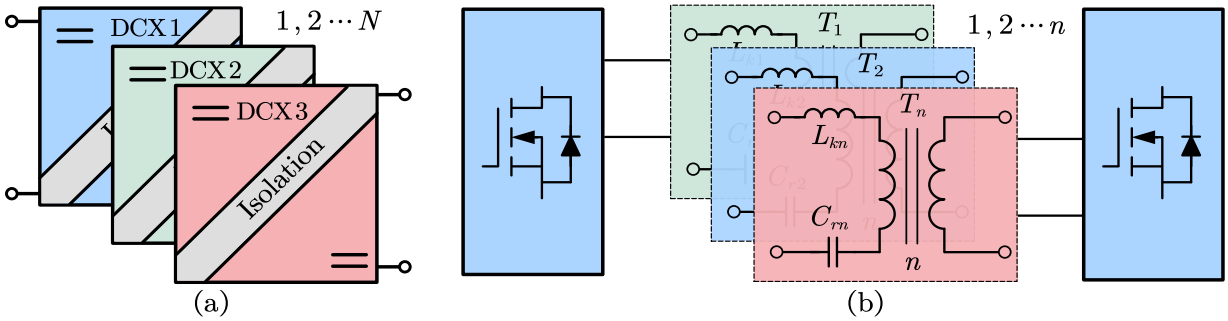


Fig. 1-13. Parallel schemes: (a) converter-level parallel and (b) transformer-level parallel.

However, the current sharing among parallel transformers is determined by the loop impedance of each transformer, which is mostly from the total leakage inductance of the transformer in the high-frequency range. As each transformer leakage inductance is already minimized, any small inductance mismatch, easily introduced by the tolerances from manufacturing, installation, and terminations, can cause a significant current-sharing mismatch.

To sum up, the first two issues, such as switching transition noise, and deadtime loss, will be solved by a switching transition optimization for CLLC-DCX discussed in **Chapter 2**. The remaining three issues, such as high-frequency and high-power transformer design, large rms current, and poor current sharing, will be solved by the EET concept discussed in **Chapter 3**.

1.4 Dissertation Outline

Chapter 1 discusses the background of the DCX, including its topologies, control, and applications. The state-of-the-art DCX topologies are introduced, and the remaining challenges are identified.

Chapter 2 presents the modeling, control, and switching transition optimization for resonant CLLC-DCX. With a generic optimization procedure, both sides' full bridge in CLLC-DCX can start and finish the ZVS at the same time. Thus, deadtime loss can be eliminated, and the current ringing during deadtime can be minimized.

Chapter 3 proposes a new concept of an EET to tackle the intrinsic transformer design trade-off between high-power and high-frequency. With simple open-loop control, a scalable EET-DCX is proposed to realize transformer-level parallel with robust current sharing and trapezoidal current (smaller RMS current). In light of this concept, a family of DCX topologies is proposed, including RC EET-DCX, hybrid EET-DCX, and hybrid RC EET-DCX. All these DCXs retain the benefits from a typical CLLC-DCX, such as full load range ZVS and load-independent gain.

Chapter 4 presents two DCX applications for voltage regulation. Firstly, an 18 kW 98.8% peak efficiency EV charger is designed and implemented with partial power processing. The optimization method in **Chapter 2** was adopted in the main power loop CLLC-DCX design. Later, as the post-regulator for DCX, a symmetric 3-L buck-boost converter with coupled inductors is proposed for CM noise reduction. Furthermore, after bridging the midpoints, the automatic voltage balance on the split capacitor can be realized, and better CM noise reduction can be obtained.

Chapter 5 concludes the dissertation and discusses future work.

Chapter 2

CLLC-DCX Modeling, Control, and Optimization

2.1 Introduction

This chapter starts with a brief introduction to the traditional CLLC-DCX. To reduce the conduction loss caused by the current through the body diode during the deadtime (so-called deadtime loss), synchronous rectification (SR) can be adopted [36]–[38]. However, if the DCX works in the bidirectional application, the power flow direction cannot be changed smoothly because SR makes the driver logic different for inverter and rectifier bridges [39]. In addition, open-loop DCX with SR control is problematic when considering semiconductor output capacitances, such as oscillations, current distortions, and load-dependent voltage gain [40]. In [41], a method based on sensing the resonant AC currents was proposed to obtain a smooth power direction transition. However, obtaining the resonant current is challenging in high-frequency applications because it requires the extra high bandwidth current sensor and related processing circuits, which increases the cost and reduces the power density.

To address these problems, a natural bidirectional modulation has been adopted [40], [42]–[45], which applies identical driving signals to the primary and secondary sides, as shown in **Fig. 2-2**. Since this modulation has many different names in the literature, such as “dual-active control” in [43], “active rectification” in [40], and “sync turn-on and turn-off modulation” in [45], this paper names it “dual-active-synchronization” (DAS) modulation for the simplicity. In [40], [42]–[45], the ZVS mechanism with DAS modulation was given only under the ideal case, without consideration of the deadtime current ringing caused by semiconductor output capacitance or the splitting magnetizing currents caused by identical gate signals. For example, this current ringing

during deadtime may lead to the failure of ZVS. In addition, most of the research on CLLC-DCX with DAS modulation only focuses on the realization of ZVS [40], [42]–[45] and ignores the possible additional conduction losses compared to SR. In particular, WBG semiconductors are usually used for the achievement of high frequency and high-power density. However, they have a higher forward voltage drop in the third quadrant, which brings a sizable conduction loss during dead time [46]–[52]. Therefore, a comprehensive analysis of the ZVS/ZCS mechanism of DAS control for CLLC-DCX (considering non-ideal current ringing and conduction loss during deadtime) is desired.

This chapter is organized as follows. **Section 2.2** presents a comprehensive switching transition analysis for open-loop CLLC-DCX with DAS modulation, including seven possible ZVS transition types, corresponding soft-switching realization, and deadtime conduction loss. Among these types, one optimal "Sync-ZVS" transition is proposed with advantages of minimum deadtime, load-independent voltage gain, and no deadtime conduction loss. To realize this "Sync-ZVS" transition in the full load range, **Section 2.3** proposes an "Axis and Center Symmetric" (ACS) method based on current decomposition. Following this method, an overall design procedure for open-loop CLLC-DCX with DAS modulation is proposed. Finally, the proposed "Sync-ZVS" transition and "ACS" method are both verified by three 18kW CLLC-DCX prototypes with DAS modulation, which all operate around 500 kHz and have 98.7% peak efficiency.

2.2 Comprehensive Analysis for Dual-Active-Synchronization (DAS)

2.2.1 Simplified CLLC-DCX Circuit

The CLLC-DCX circuit in **Fig. 2-1** operates with DAS modulation, where switches S_1, S_4, S_5, and S_8 share the same gate signal (50% duty cycle). The semiconductor output capacitance of both HV and LV sides is represented with a linearized charge-equivalent capacitance $C_{oss,HV}$ and $C_{oss,LV}$ [53]. The transformer equivalent circuit is described as an ideal transformer, with a turns ratio n, a magnetizing inductance L_m, and two split leakage inductances $L_{r,HV}$ and $L_{r,LV}$. The turns ratio n is selected according to the voltage transfer ratio between two DC buses, $V_{DC,HV}$, and $V_{DC,LV}$. Afterward, to achieve the desired resonant frequency f_r, the resonant capacitors $C_{r,HV}$ and $C_{r,LV}$ are selected as

$$C_{r,HV(LV)} = \frac{1}{4\pi^2 L_{r,HV(LV)} f_r^2} \tag{2.1}$$

To simplify the circuit and allow a direct comparison between the HV and LV sides, the complete LV side circuit is referred to as the HV side with the transformer turns ratio n. The simplified CLLC-DCX circuit is shown in **Fig. 2-2(a),** and the transformed parameters can be given as

$$\begin{cases} V_{DC,TLV} = n \cdot V_{DC,LV} \\ v_{TCD} = n \cdot v_{CD} \\ v_{ds,TLV} = n \cdot v_{ds,LV} \\ v_{Cr,TLV} = n \cdot v_{Cr,LV} \end{cases} \tag{2.2}$$

$$I_{TLV} = \frac{I_{LV}}{n} \tag{2.3}$$

$$C_{oss,TLV} = \frac{C_{oss,LV}}{n^2} \tag{2.4}$$

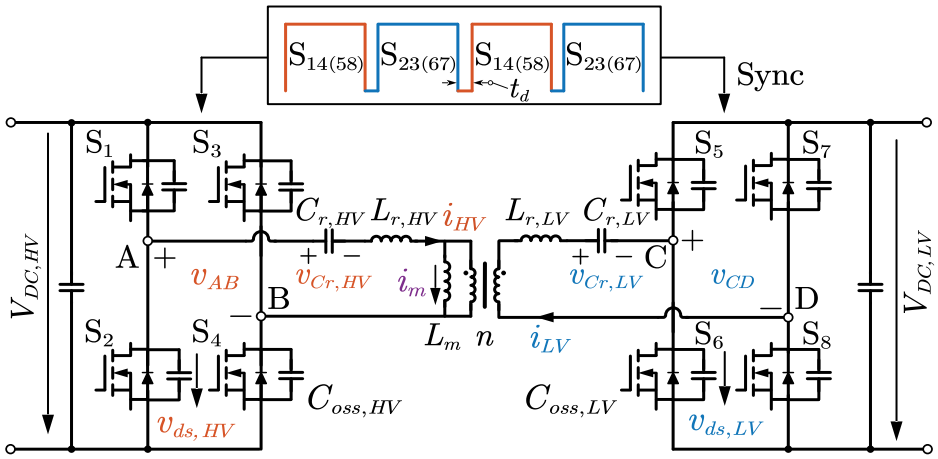
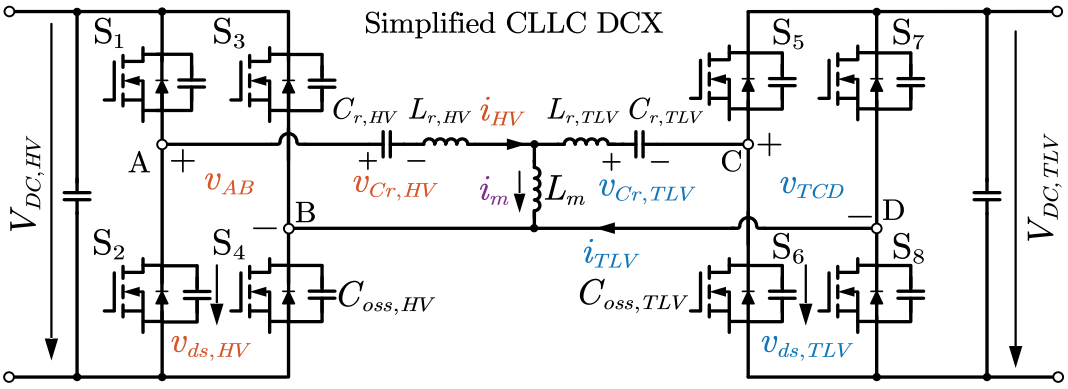
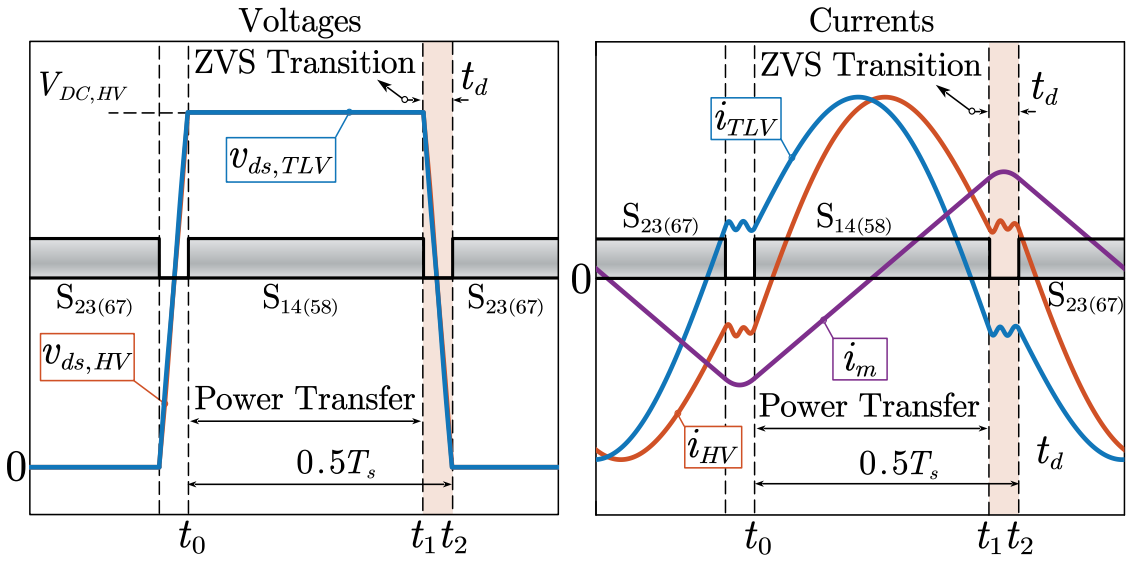


Fig. 2-1. Bidirectional CLLC-DCX operated with "dual-active-synchronization" (DAS) modulation.



(a)



(b)

Fig. 2-2. (a) Simplified CLLC-DCX circuit diagram. The LV side is referred to as the HV side with the voltage transfer ratio of the transformer *n*. (b) Current and voltage waveforms of the CLLC-DCX with DAS modulation.

Where v_{CD} is the voltage across two switching nodes of the bridge; $v_{ds,LV}$ is the drain to source voltage across the switch and $v_{Cr,LV}$ is the voltage across the resonant capacitor $C_{r,LV}$. The current i_{LV} is the resonant current through the transformer at the LV side.

The magnetizing current i_m during the deadtime t_d can be assumed to be constant and equal to its peak value I_m.

$$C_{r,HV(LV)} = \frac{1}{4\pi^2 L_{r,HV(LV)} f_r^2} \tag{2.5}$$

Where f_s is the switching frequency, and Im should be large enough to discharge the semiconductor output capacitance Coss, HV, and Coss,TLV during the dead time t_d to ensure the ZVS turn-on. This limitation can be expressed as

$$Q_{mag} = I_m \cdot t_d \geq Q_{ZVS} = 2V_{DC,HV}(C_{oss,HV} + C_{oss,TLV}) \tag{2.6}$$

Where Q_{mag} is the electric charge provided by magnetizing current during the dead time, and Q_{ZVS} is the total electric charge needed in the ZVS transition. To satisfy the ZVS criteria during dead time t_d and achieve minimum conduction loss [42]-[44], the magnetizing inductance L_m and t_d should meet the following requirements.

$$L_m = \frac{t_d}{8f_s \cdot (C_{oss,HV} + C_{oss,TLV})} \tag{2.7}$$

2.2.2 DAS Operation Principle

Since the power flow direction in CLLC-DCX is determined by the outside situation, for simplicity, the following analysis will focus on the direction from the HV side to the LV side. With the consideration of semiconductor output capacitances, the schematic view of the current and voltage waveforms of the CLLC-DCX are depicted in **Fig. 2-2(b)**. The switching period T_s ($1/f_s$) can be decomposed into two main intervals — the "Power Transfer" interval (t0-t1) and the "ZVS Transition" interval (t_1-t_2). In the "Power Transfer" interval from t_0 to t_1, the real power is transferred with Resonant Pulse (RP) mode, as shown in **Fig. 2-3(a)**. In this interval, the HV and TLV sides are both connected to the resonant tank; as for the "ZVS Transition" interval from t_1 to t_2, five possible operation modes with their equivalent circuits are shown in **Fig. 2-3(b)-(f)**. Regardless of the HV or TLV side, the side where ZVS occurs will be cut out of the resonant tank because the resonant current on that side will be fully used to discharge the semiconductor output capacitors. The reference current direction for i_{HV} and i_{TLV} are represented by black arrows. Each operation mode of the CLLC-DCX with DAS modulation is explained as follows.

1. *Resonant Pulse (RP)* — In **Fig. 2-3(a)**, the HV and LV bridge voltages v_{AB} and v_{TCD} cancel each other, and the resonant tank is excited by the initial voltage on resonant capacitances. This will generate sinusoidal resonant currents i_{HV} and i_{TLV} at the resonant frequency f_r, which is used to transfer the real power.

2. *ZVS at HV and LV Side* (*ZHL*) — In **Fig. 2-3(b)**, before the ZVS completion of both sides, if $i_{HV}>0$ and $i_{TLV}<0$, i_{HV} and i_{TLV} will discharge $C_{oss,HV}$ and $C_{oss,TLV}$, respectively. In this mode, both sides of ZVS are conducted at the same time.

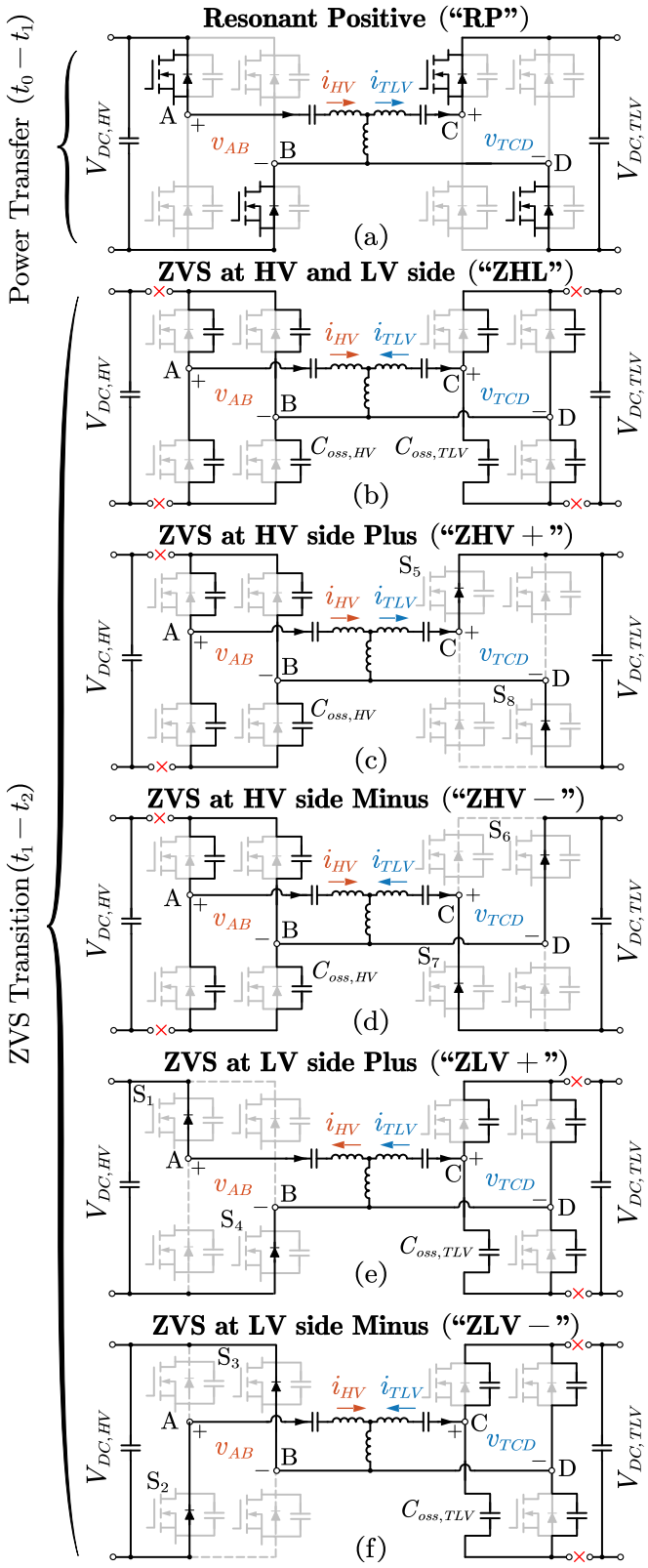


Fig. 2-3. Equivalent circuits during the different operation modes. (a) Resonant Pulse "RP". (b) ZVS at HV and LV side "ZHL". (c) ZVS at HV side plus "ZHV+". (d) ZVS at HV side minus "ZHV-" (e) ZVS at LV side plus "ZLV+". (f) ZVS at LV side minus "ZLV-".

3. *ZVS at HV Side Plus* (ZHV+) — In **Fig. 2-3(c)**, before the ZVS completion of both sides, if $i_{HV}>0$ and $i_{TLV}>0$, i_{HV} will discharge $C_{oss,\,HV}$, and i_{LV} will go through the body diodes of S5 and S8. Therefore, ZVS is only conducted at the HV side, and v_{TCD} is clamped to $+V_{DC,TLV}$.

4. *ZVS at HV Side Minus* (ZHV-) — In **Fig. 2-3(d)**, after achieving the ZVS at LV side, if $i_{HV}>0$ and $i_{TLV}<0$, i_{HV} will discharge $C_{oss,HV}$, and i_{LV} will go through the body diodes of S_6 and S_7. Therefore, ZVS is only conducted at the HV side, and v_{TCD} is clamped to $-V_{DC,TLV}$.

5. *ZVS at LV Side Plus* (ZLV+) — In **Fig. 2-3(e)**, before the ZVS completion of both sides, if $i_{HV}<0$ and $i_{TLV}<0$, i_{LV} will discharge $C_{oss,TLV}$, and i_{HV} will go through the body diodes of S_1 and S_4. In this mode, ZVS is only conducted at the LV side, and v_{HV} is clamped to $+V_{DC,HV}$.

6. *ZVS at LV Side Minus* (ZLV-) — In **Fig. 2-3(f)**, after achieving ZVS at the HV side, if $i_{HV}>0$ and $i_{TLV}<0$, i_{LV} will discharge $C_{oss,TLV}$, and i_{HV} will go through the body diodes of S_3 and S_4. Thus, ZVS is only conducted at the HV side, and v_{TCD} is clamped to $-V_{DC,HV}$.

According to different combinations of these five modes during t_1 to t_2, seven possible ZVS transition types *I-VII* are classified in **Fig. 2-4**. The zoomed voltage ($v_{ds,HV}$ and $v_{ds,TLV}$) and current (i_{HV}, i_{TLV}, and i_m) waveforms of these ZVS transition types are depicted in **Fig. 2-5**. As shown in **Fig. 2-4**, according to the polarity of currents i_{HV} and i_{TLV} at t_1, CLLC-DCX might enter "ZHV+," "ZHL," and "ZLV+," respectively. If $i_{HV}(t_1) > 0$ and $i_{TLV}(t_1) > 0$, CLLC-DCX will operate in "ZHV+" mode first because positive i_{TLV} will clamp $v_{ds,TLV}$ to $+V_{DC,TLV}$ as shown in **Fig. 2-5(a)** and **(b)**. Since i_{TLV} goes through the body diodes at t_1, the LV side has ZCS. When i_{TLV} decreases to zero, the converter will enter "ZHL" mode and both $v_{ds,HV(TLV)}$ will fall. If $v_{ds,HV}$ drops to zero first, CLLC-DCX will work in "ZLV-" mode. This mode sequence, "ZHV+" → "ZHL" → "ZLV-" is defined as a *Type I* transition.

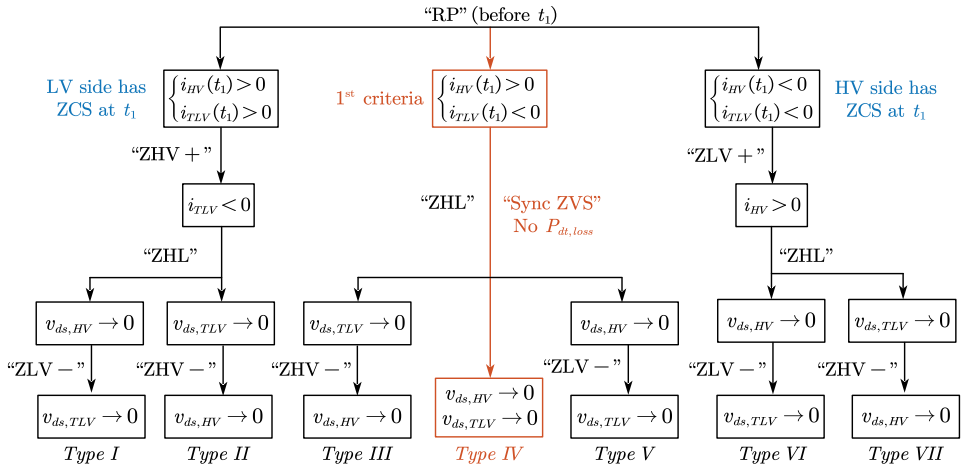


Fig. 2-4. The classification of seven ZVS transition types during t_1 to t_2. *Type IV* is defined as "Sync ZVS" transition without deadtime conduction loss $P_{dt,los}$. Corresponding waveforms are plotted in Fig. 2-5.

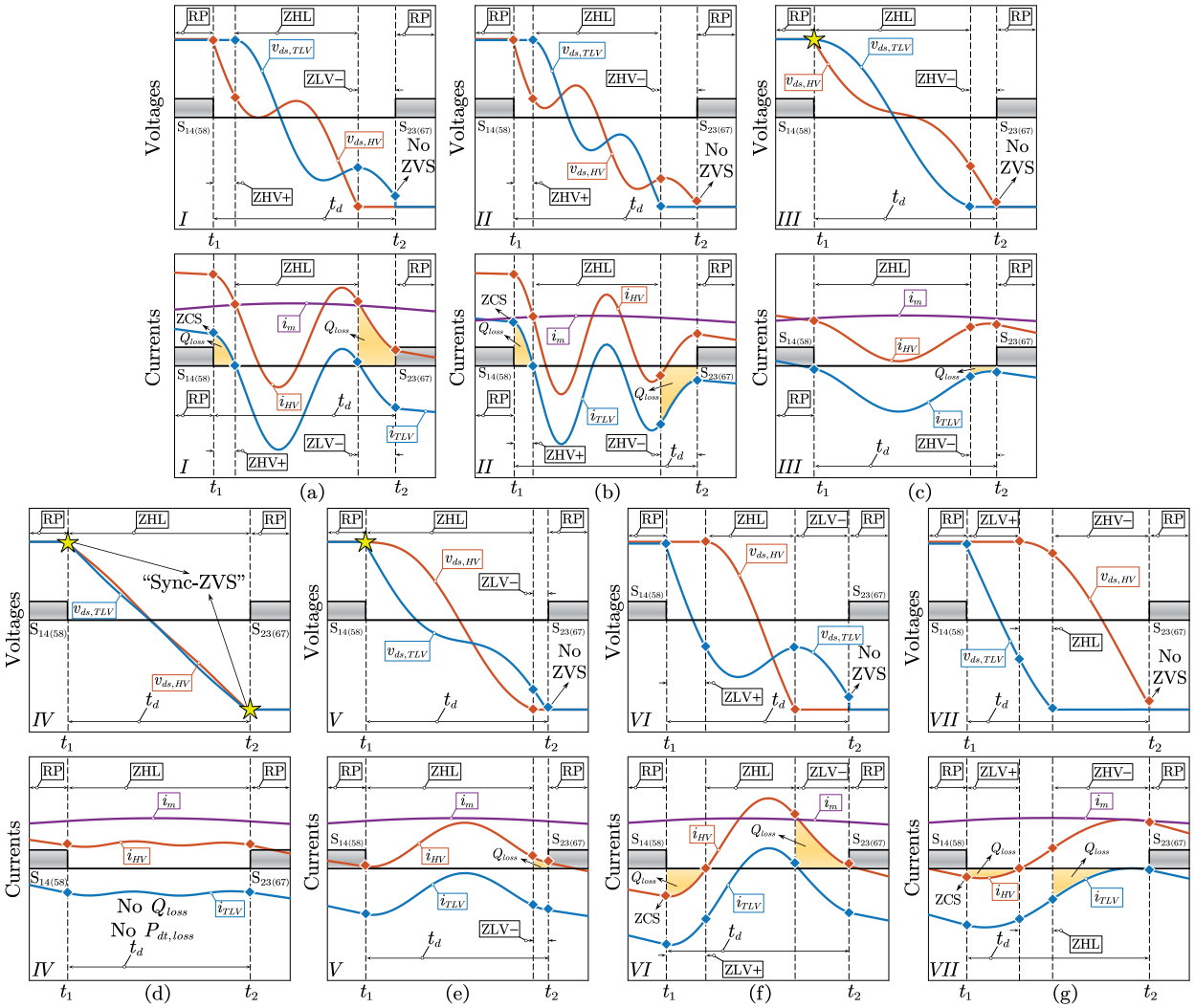


Fig. 2-5. Current and voltage waveforms of seven ZVS transition types: (a)-(g) *Type I-VII*. *Type IV* is defined as a "Sync-ZVS" transition without Q_{loss} and Pdt $_{loss}$. The classification can be found in Fig. 2-4.

On the other hand, if $v_{ds,TLV}$ falls to zero before $v_{ds,HV}$, the converter will enter "ZHV-" mode, and the mode sequence will change to "ZHV+"→"ZHL"→ "ZHV-." This sequence is defined as *Type II*. Following a similar analysis, the mode sequences of the other five types can be found in **Fig. 2-4** and **Fig. 2-5**.

Among these seven transition types, only *Type IV* transition in **Fig. 2-5(d)** can achieve both sides ZVS with minimum t_d because the result from Eq. (2.7) has the assumption that electric charge Q_{mag} in Eq. (2.6) is fully used to realize the ZVS at both sides. However, except for *Type IV*, a part of Q_{mag} in all other six types is not used to discharge the semiconductor output capacitance. The unused part of Q_{mag} is defined as Q_{loss} and will exist in "ZLV+", "ZLV+", "ZHV+" and "ZHV-" modes as shown in **Fig. 2-5**. In addition to causing ZVS failure, this Q_{loss} will lead to the deadtime conduction loss $P_{dt,loss}$ which can be expressed as

$$P_{dt,loss} = Q_{loss} \cdot V_f \cdot f_s \tag{2.8}$$

Where V_f is the forward voltage of the MOSFET body diode. It should be noted that WBG semiconductors (higher V_f) and high switching frequency f_s (hundreds of kHz) are usually adopted for high efficiency and density. This higher V_f and f_s will cause a sizable deadtime conduction loss $P_{dt,loss}$.

2.2.3 "Sync-ZVS" Transition

In order to eliminate $P_{dt,loss}$, CLLC-DCX is required to always operate in *Type IV* transition without Q_{loss}. As shown in **Fig. 2-5(d)**, since both sides of ZVS in the Type IV transition will begin and finish at the same time, this transition type is defined as the "Sync-ZVS" transition. Without the consideration of stray resistance, this "Sync-ZVS" transition has a unit voltage gain because it only has "RP" and "ZHL" modes, as shown in **Fig. 2-3(a)** and **(b)**. The input and output side are both connected (t_0-t_1) or disconnected (t_1-t_2) with the resonant tank simultaneously.

As shown in **Fig. 2-5(c)-(e)**, for ensuring that both sides of ZVS can start at the same time, the first criteria of the "Sync-ZVS" transition require the polarities of currents i_{HV} and i_{TLV} at t_1.

$$P_{dt,loss} = Q_{loss} \cdot V_f \cdot f_s \tag{2.9}$$

After following this criterion, CLLC-DCX might operate in Type III, IV ("Sync-ZVS"), or V. If both sides of ZVS can also finish at the same time, "Sync-ZVS" is achieved. Thus, the next section will discuss how to complete both the HV and LV sides of ZVS simultaneously. The next section will verify this theory with an 18 kW CLLC-DCX prototype.

2.3 “SYNC-ZVS” Switching Transition Design

2.3.1 Splitting Magnetizing Currents Approximation

With DAS modulation, the total magnetizing current i_m is provided by both sides. **Fig. 2-6** depicts the splitting magnetizing currents $i_{m,HV}$ and $i_{m,TLV}$ at zero load. During the deadtime, $i_{m,HV(TLV)}$ could be approximated as constant values $I_{m,HV(TLV)}$ and follow the distribution of $C_{oss,HV}$ and $C_{oss,TLV}$.

$$\begin{cases} I_{m,HV} = \dfrac{C_{oss,HV}}{C_{oss,HV} + C_{oss,TLV}} I_m \\ I_{m,TLV} = -\dfrac{C_{oss,TLV}}{C_{oss,HV} + C_{oss,TLV}} I_m \end{cases} \tag{2.10}$$

Where I_m can be derived from Eq. (2.5). To describe the imbalance between $L_{r,HV}$ and $L_{r,TLV}$, the imbalance factor “k” is defined as $L_{r,HV}/L_{r,TLV}$. As shown in **Fig. 2-6**, although the difference of k will cause some distortions on splitting magnetizing currents during t_0 to t_1, $i_{m,HV}$ and $i_{m,TLV}$ can still be approximated as constants during the deadtime t_d.

At zero load, the electric charge $Q_{m,HV}$ and $Q_{m,TLV}$ in **Fig. 2-6** can be derived as

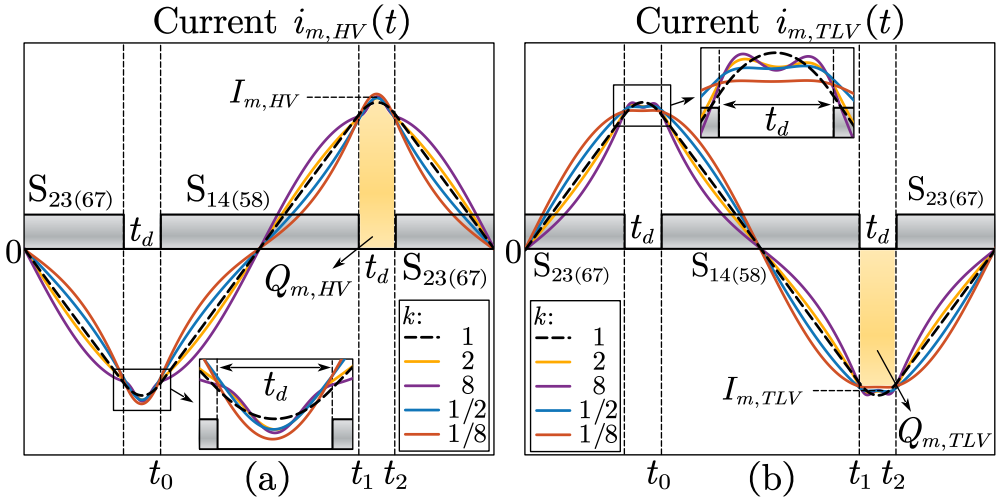


Fig. 2-6. The Splitting magnetizing currents at zero load: (a) $i_{m,HV}$. (b) $i_{m,TLV}$.

$$Q_{m,HV(TLV)} = |I_{m,HV(TLV)}| \cdot t_d \tag{2.11}$$

From Eq. (2.10) and (2.11), $Q_{m,HV(TLV)}$ meet the requirement as

$$Q_{m,HV}/Q_{m,TLV} = C_{oss,HV}/C_{oss,TLV} \tag{2.12}$$

Since Eq. (2.12) can guarantee that both HV and LV sides complete the ZVS transition at the same time, the "Sync-ZVS" transition is naturally achieved at no load condition.

2.3.2 Current Decomposition

Fig. 2-7(a) depicts the total currents i_{HV} and i_{TLV} with a certain load, which can be decomposed into two distinct parts: the resonant circuit i_r dedicated to transferring real power, as shown in **Fig. 2-7(b)**, and the splitting magnetizing currents $i_{m,HV}$ and $i_{m,TLV}$ dedicated to realizing the ZVS at both sides as shown in **Fig. 2-7(c)**.

$$\begin{cases} i_{HV}(t) = i_r(t) + i_{m,HV}(t) \\ i_{TLV}(t) = i_r(t) + i_{m,TLV}(t) \end{cases} \tag{2.13}$$

As shown in **Fig. 2-7(b)**, both HV and LV sides share the same resonant current i_r. During t_0 to t_1, i_r transfers the real power from the HV side to the LV side. As for deadtime from t_1 to t_2, i_r represents the AC current ringing generated by resonance between leakage inductances and parasitic output capacitances. Since only "ZHL" mode will exist during the deadtime (t_1-t_2) with "Sync-ZVS" transition, the equivalent circuit of "ZHL" mode in **Fig. 2-3(b)** is simplified and decomposed as shown in **Fig. 2-8**. The resonant current i_r during t_1 to t_2 can be expressed as

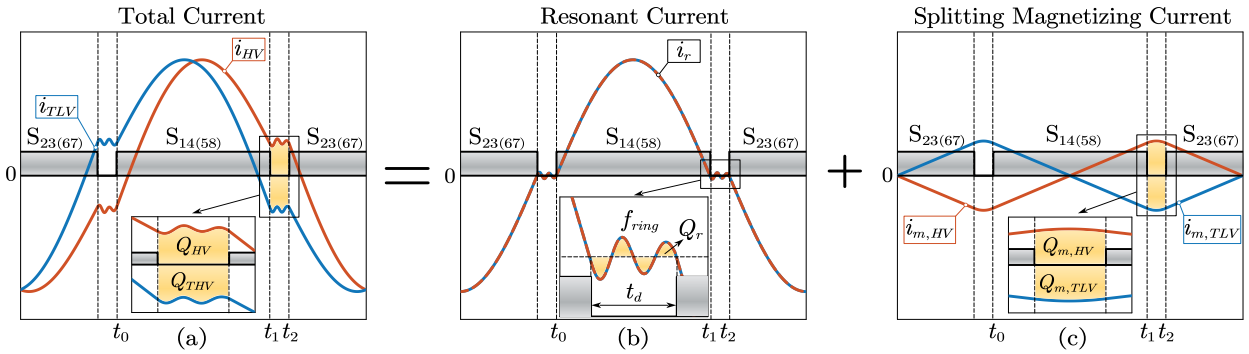


Fig. 2-7. Currents decomposition: (a) total currents i_{HV} and i_{TLV}. (b) resonant current i_r (c) splitting magnetizing currents $i_{m,HV}$ and $i_{m,TLV}$. The equivalent circuit during the deadtime can be found in Fig. 2-8.

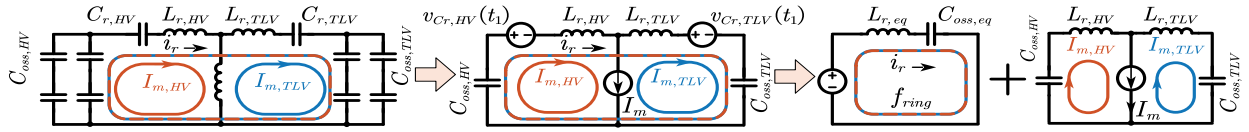


Fig. 2-8. Simplified equivalent circuit for "ZHL" mode during the deadtime t_1 to t_2.

$$i_r(t) = A\sin(2\pi f_{ring}(t - t_1)) + B\cos(2\pi f_{ring}(t - t_1)) \tag{2.14}$$

Where the current ringing frequency f_{ring}, terms "A" and "B" can be given as

$$\begin{aligned} f_{ring} &= 1/\left(2\pi\sqrt{L_{r,eq}C_{oss,eq}}\right) \\ A &= (v_{Cr,HV}(t_1) + v_{Cr,TLV}(t_1))/\sqrt{L_{r,eq}/C_{oss,eq}} \\ B &= i_{HV}(t_1) - I_{m,HV} = i_{TLV}(t_1) - I_{m,TLV} \end{aligned} \tag{2.15}$$

As shown in **Fig. 2-8**, the equivalent resonant inductance $L_{r,eq}$ and parasitic output capacitance $C_{oss,eq}$ can be derived as

$$\begin{aligned} L_{r,eq} &= L_{r,HV} + L_{r,TLV} \\ C_{oss,eq} &= C_{oss,HV} \cdot C_{oss,TLV}/(C_{oss,HV} + C_{oss,TLV}) \end{aligned} \tag{2.16}$$

During the deadtime (t_1-t_2), the current ringing i_r from Eq. (2.14) will result in the electric charge Q_r as shown in **Fig. 2-7(b)**.

$$Q_r = \int_{t1}^{t2} i_r(t)\,dt \tag{2.17}$$

As depicted in **Fig. 2-7(c)**, the splitting magnetizing currents $i_{m,HV}$, and $i_{m,TLV}$ can achieve the "Sync-ZVS" transition naturally at zero load without i_r because $Q_{m,HV}$, and $Q_{m,TLV}$ can meet the requirement from Eq. (2.12).

However, if i_r is required to transfer the real power, Q_r from Eq. (2.17) will have an impact on the ZVS transition, and the total electric charge at HV side Q_{HV} and LV side Q_{TLV} can be expressed as

$$\begin{cases} Q_{HV} = Q_{m,HV} + Q_r \\ Q_{TLV} = Q_{m,TLV} - Q_r \end{cases} \tag{2.18}$$

To achieve the "Sync-ZVS" transition, the electric charge Q_r from Eq. (2.17) should be eliminated, and thus Q_{HV} and Q_{TLV} can meet a requirement similar to Eq. (2.12).

$$Q_{HV}/Q_{TLV} = C_{oss,HV}/C_{oss,TLV} \tag{2.19}$$

Once the ratio between Q_{HV} and Q_{TLV} can follow Eq. (2.19), the CLLC-DCX can finish both HV and LV sides ZVS at the same time. Therefore, the second design criteria of the "Sync-ZVS" transition can be summarized as

$$Q_r = 0 \tag{2.20}$$

2.3.3 Proposed "Axis and Center Symmetric" (ACS) Method

To meet the second design criteria from Eq. (2.20) and achieve the "Sync-ZVS" transition, an "Axis and Center Symmetric" (ACS) method is proposed as shown in **Fig. 2-9**. By adjusting the switching frequency f_s with a per-determined f_r and t_d, the value of resonant current i_r at t_1 and t_2 can be designed as

$$i_r(t_1) = -i_r(t_2) \tag{2.21}$$

Due to the sinusoidal waveform of i_r from Eq. (2.14), Eq. (2.21) ensures that the waveform of i_r is centrosymmetric from t_1 to t_2. On the other hand, based on the operation principle of the CLLC resonant converter, i_r should meet the requirements as

$$i_r(t) = -i_r(t + 0.5T_s) \tag{2.22}$$

Therefore, from Eq. (2.21) and (2.22), the currents $i_r(t_0)$ and $i_r(t_2)$ have a relationship as

$$i_r(t_0) = -i_r(t_0 + 0.5T_s) = -i_r(t_2) \tag{2.23}$$

From Eq. (2.21) and (2.23), the relationship between currents $i_r(t_0)$ and $i_r(t_1)$ can be derived as

$$i_r(t_0) = i_r(t_1) \tag{2.24}$$

From Eq. (2.24), the waveform of i_r is axisymmetric from t_0 to t_1. It can be easily proved that only when i_r is axisymmetric during t_0 to t_1 and centrosymmetric during t_1 to t_2, the electric charge Q_r from Eq. (2.17) can be eliminated. Thus, the "Sync-ZVS" transition can be achieved with the ACS method.

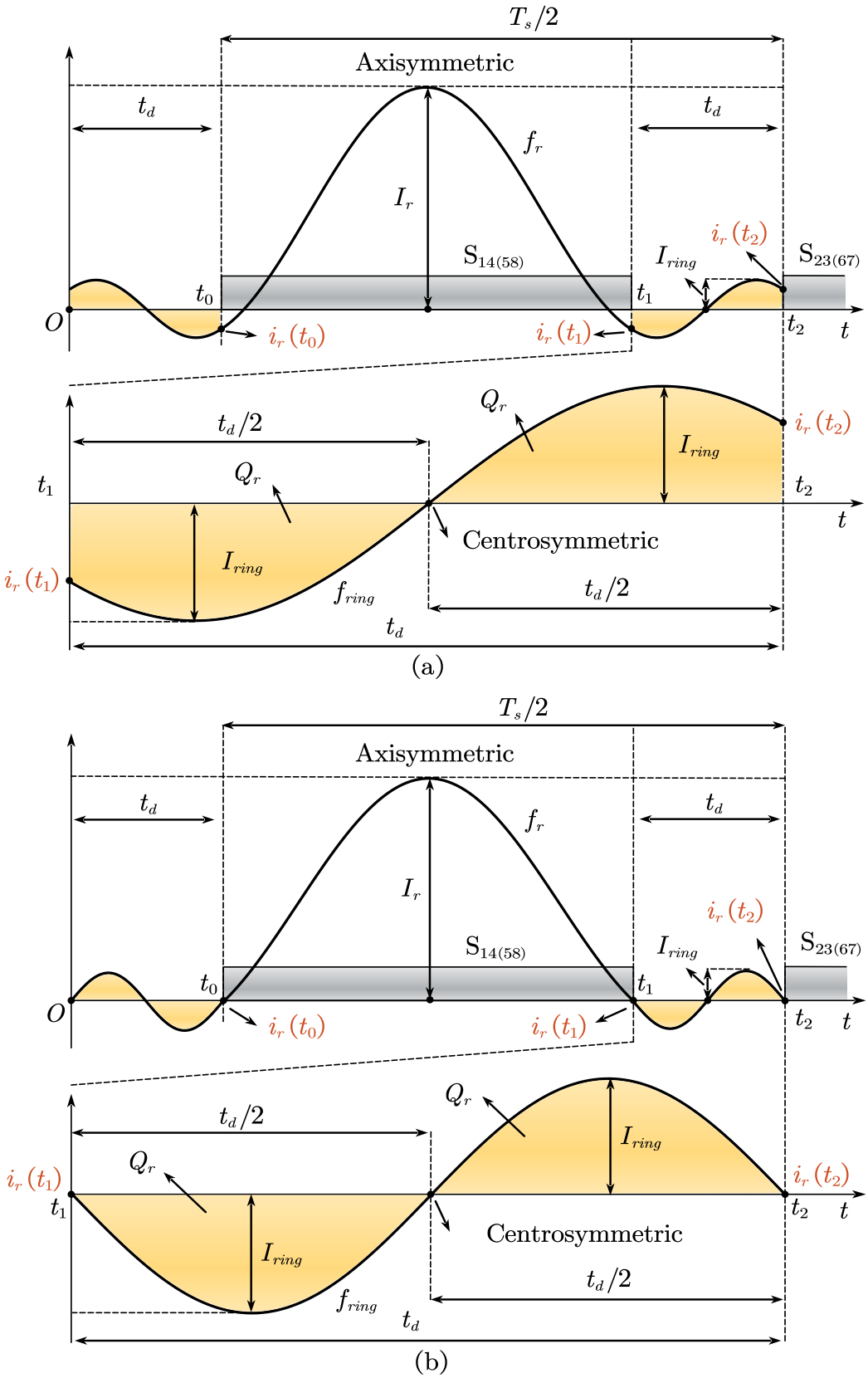


Fig. 2-9. Proposed ACS method: (a) *case* 1, and (b) *case* 2.

According to whether t_d is divisible by the current ringing period T_{ring} ($1/f_{ring}$) from Eq. (2.15), two cases are defined as

$$\begin{cases} case\ 1: & \frac{t_d}{T_{ring}} \neq 1, 2, ... \\ case\ 2: & \frac{t_d}{T_{ring}} = 1, 2, ... \end{cases} \tag{2.25}$$

As shown in **Fig. 2-9(a)** and **(b)**, from Eq. (2.25), *case* 1 and *case* 2 are depicted with the "ACS" method, respectively.

From Eq. (2.14), (2.21), and (2.24), the desired switching frequency f_s can be derived with f_r and t_d.

$$f_s(f_r, t_d) = \begin{cases} \dfrac{0.5\pi f_r}{\cos^{-1}\left(-\dfrac{f_r}{f_{ring}}\dfrac{\sin(\pi f_{ring} t_d)}{|\cos(\pi f_{ring} t_d)|}\right) + \pi f_r t_d} & case\ 1 \\ \dfrac{0.5\pi f_r}{0.5\pi + \pi f_r t_d} & case\ 2 \end{cases} \tag{2.26}$$

Where f_{ring} is pre-determined by $L_{r,eq}$ and $C_{oss,eq}$ from Eq. (2.15).

After obtaining f_s, the corresponding L_m can be determined by Eq. (2.7). However, Eq. (2.7) exaggerates the value of L_m because magnetizing current i_m will not increase with the slope of $V_{DC,HV}/L_m$ during the deadtime t_d. Therefore, Eq. (2.7) should be revised as

$$L_m = \frac{(1 - 2f_s t_d)}{8f_s \cdot (C_{oss,HV} + C_{oss,TLV})} \cdot t_d \tag{2.27}$$

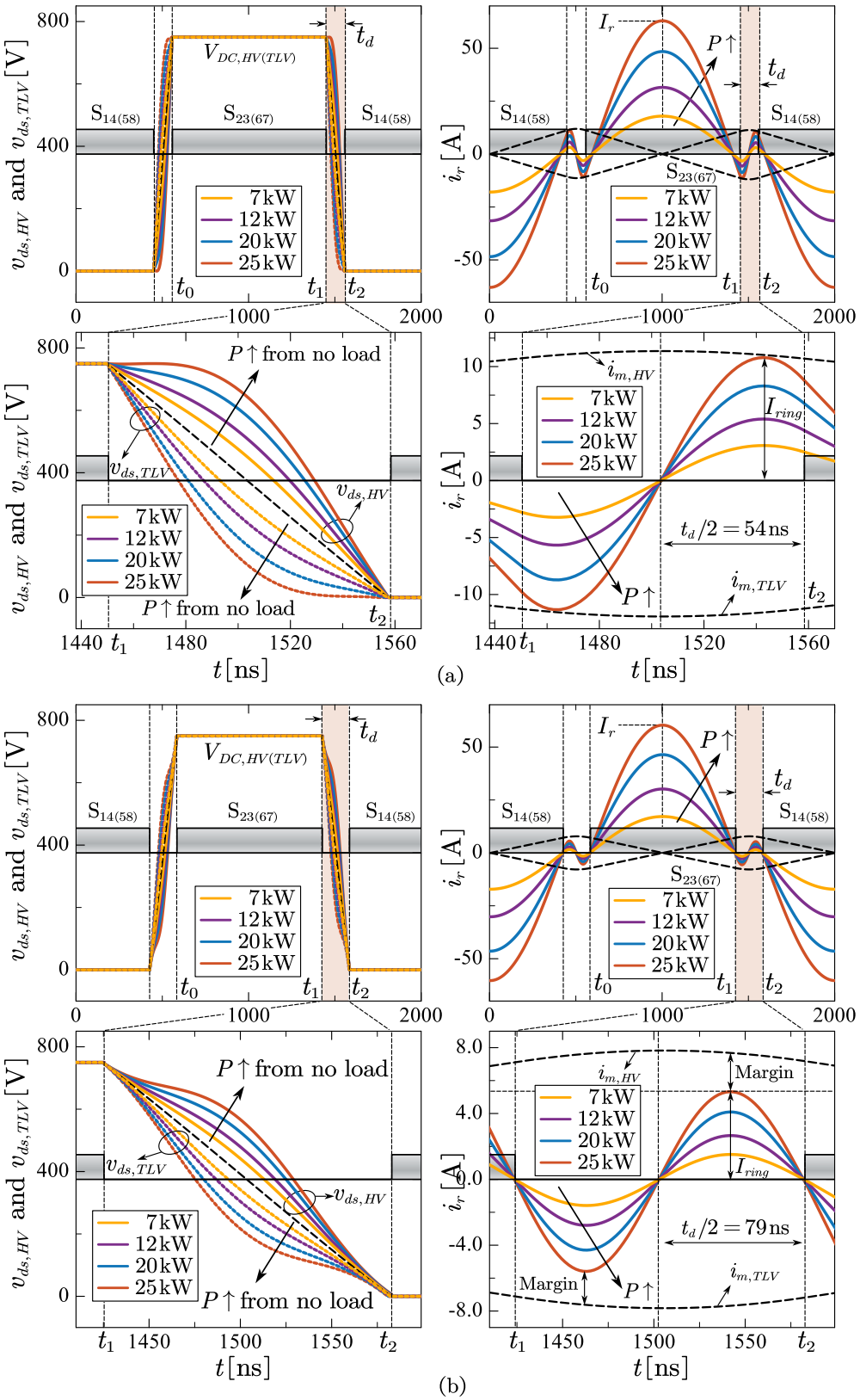


Fig. 2-10. Simulated voltages $v_{ds,HV}$, $v_{ds,TLV}$, and current ir with proposed "Axial and Central Symmetry" method at different loads: (a) *case* 1, and (b) *case* 2. The simulation parameters can be found in Table 2-1.

Table 2-1 SIMULATION PARAMETERS OF TWO CASES

	Case 1	*Case* 2
$V_{DC,HV}$ and $V_{DC,TLV}$	750 V / 750 V	750 V / 750 V
P	25 kW	25 kW
$C_{oss,HV}$ and $C_{oss,TLV}$	0.8 nF / 0.8 nF	0.8 nF / 0.8 nF
$C_{oss,eq}$	0.4 nF	0.4 nF
$C_{r,HV}$ and $C_{r,TLV}$	88 nF / 88 nF	88 nF / 88 nF
$L_{r,HV}$ and $L_{r,TLV}$	800 nH / 800 nH	800 nH / 800 nH
f_s and f_r	491 kHz / 600 kHz	504 kHz / 600 kHz
t_d and T_{ring}	108 ns /158 ns	158 ns /158 ns
L_m	15.6 µH	20.6 µH

2.3.4 Load Independence and Power Boundary

Since the desirable f_s from Eq. (2.26) is independent of output power P, the proposed ACS method can achieve a "Sync-ZVS" transition in the full load range. **Fig. 2-10** depicts the simulated voltages $v_{ds,HV}$, $v_{ds,TLV}$, and current i_r waveforms with the ACS method under different loads. The simulation parameters of *case* 1 and *case* 2 are listed in **Table 2-1**. For both cases, the resonant frequency f_r is fixed as 600 kHz. The difference between these cases is t_d and corresponding f_s and L_m. With different t_d, the desirable switching frequency f_s and magnetizing inductance L_m in these two cases can be calculated from Eq. (2.26) and (2.27), respectively. With pre-determined f_r, t_d, and f_s, the peak value of current ringing I_{ring} can be expressed by output power P.

$$I_{ring}(P)=\begin{cases}\dfrac{\pi^2 f_r^{\,2} P\sqrt{L_{r,eq}C_{oss,eq}}}{V_{DC,HV} f_s\left|\cos(\pi f_{ring} t_d)\right|} & case\ 1\\[2ex] \dfrac{\pi^2 f_r^{\,2} P\sqrt{L_{r,eq}C_{oss,eq}}}{V_{DC,HV} f_s} & case\ 2\end{cases} \tag{2.28}$$

Where $L_{r,eq}$ and $C_{oss,eq}$ are determined from Eq. (2.16).

As shown in **Fig. 2-10**, the peak current ringing I_{ring} from Eq. (2.28) is proportional to output power P. When the output power P increases from zero load, the impact of current ringing i_r on the ZVS transition is more obvious, and the curvature of voltages $v_{ds,HV}$, and $v_{ds,TLV}$ will increase. Since the second design criteria from Eq. (2.20) can be achieved, the proposed ACS method can realize the "Sync-ZVS" transition in the full load range.

There is a maximum power boundary in the ACS method, which requires that Iring at maximum power Pmax should be smaller than splitting magnetizing currents $i_{m,HV}$, and $i_{m,TLV}$. From Eq. (2.10), the boundary can be expressed as

$$I_{ring}(P_{\max}) \leqslant \min\left(\frac{C_{oss,HV}}{C_{oss,HV}+C_{oss,TLV}} I_m, \frac{C_{oss,TLV}}{C_{oss,HV}+C_{oss,TLV}} I_m\right) \tag{2.29}$$

If I_{ring} exceeds this boundary during the dead time, the current ringing might change the polarity of i_{LV} or i_{TLV} from Eq. (2.14). Thus, the first design criteria from Eq. (2.9) will be violated, and the "Sync-ZVS" transition will be lost.

2.3.5 Sensitivity Study on Parasitic Output Capacitance

From Eq. (2.26) and (2.27), the relationship between f_s (L_m) and t_d with different $C_{oss,eq}$ are depicted in **Fig. 2-11(a)** and **(b)**, respectively. *Case* 2 with different $C_{oss,eq}$ are highlighted in these two figures. As shown in **Fig. 2-10(b)**, when t_d is equal to 158 ns, CLLC-DCX will work in *case* 2 with 0.4 nF $C_{oss,eq}$. The range of t_d is limited by the maximum output power (25 kW) from Eq. (2.28) and (2.29). For example, when t_d is equal to 108 ns, the peak current I_{ring} almost touches the maximum power boundary, as shown in **Fig. 2-10(a)**.

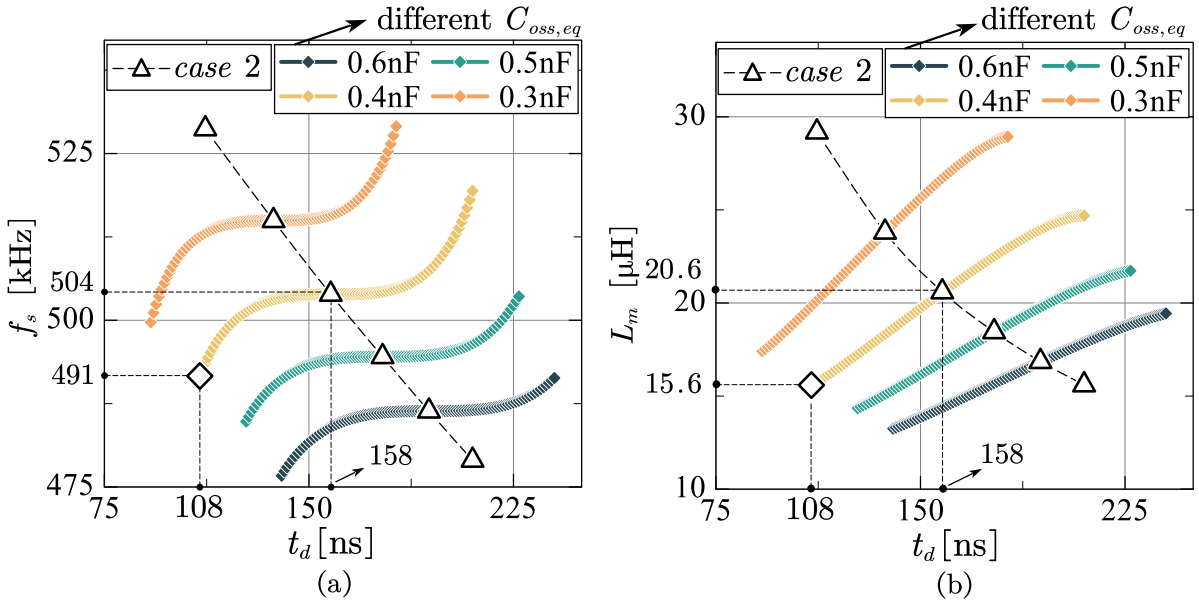


Fig. 2-11. (a) Relationship between desired f_s and t_d with different $C_{oss,eq}$. (b) Relationship between L_m and t_d with different $C_{oss,eq}$. The resonant frequency f_r is fixed at 600 kHz, and the max output power is 25 kW.

As shown in **Fig. 2-11(a)**, the desired f_s is always smaller than the resonant frequency f_r (600 kHz), as listed in **Table 2-1**. When the equivalent switch output capacitance $C_{oss,eq}$ from Eq. (2.16) increases, the desired switching frequency f_s will decrease and further away from fixed f_r as 600 kHz.

As for the desired L_m in **Fig. 2-11(b)**, when $C_{oss,eq}$ increases, the desired L_m will decrease because a larger magnetizing current is required to achieve ZVS with a determined dead time.

Although $C_{oss,eq}$ is mostly temperature insensitive, its value still might have a small measurement tolerance, resulting in a small tolerance on f_{ring}. Considering $C_{oss,eq}$ has a +5% tolerance in *case* 2, the new simulated voltages $v_{ds,HV}$, and $v_{ds,TLV}$ with calculated t_d (158 ns) are shown in **Fig. 2-12(a)**. Since $C_{oss,eq}$ increases by 5%, the pre-determined t_d is not large enough to achieve the full ZVS. For example, the values of $v_{ds,HV}$, and $v_{ds,TLV}$ at t_2 are both very small (less than 5 V) but not equal to zero. Therefore, the turn-on switching losses with partial ZVS will be very small.

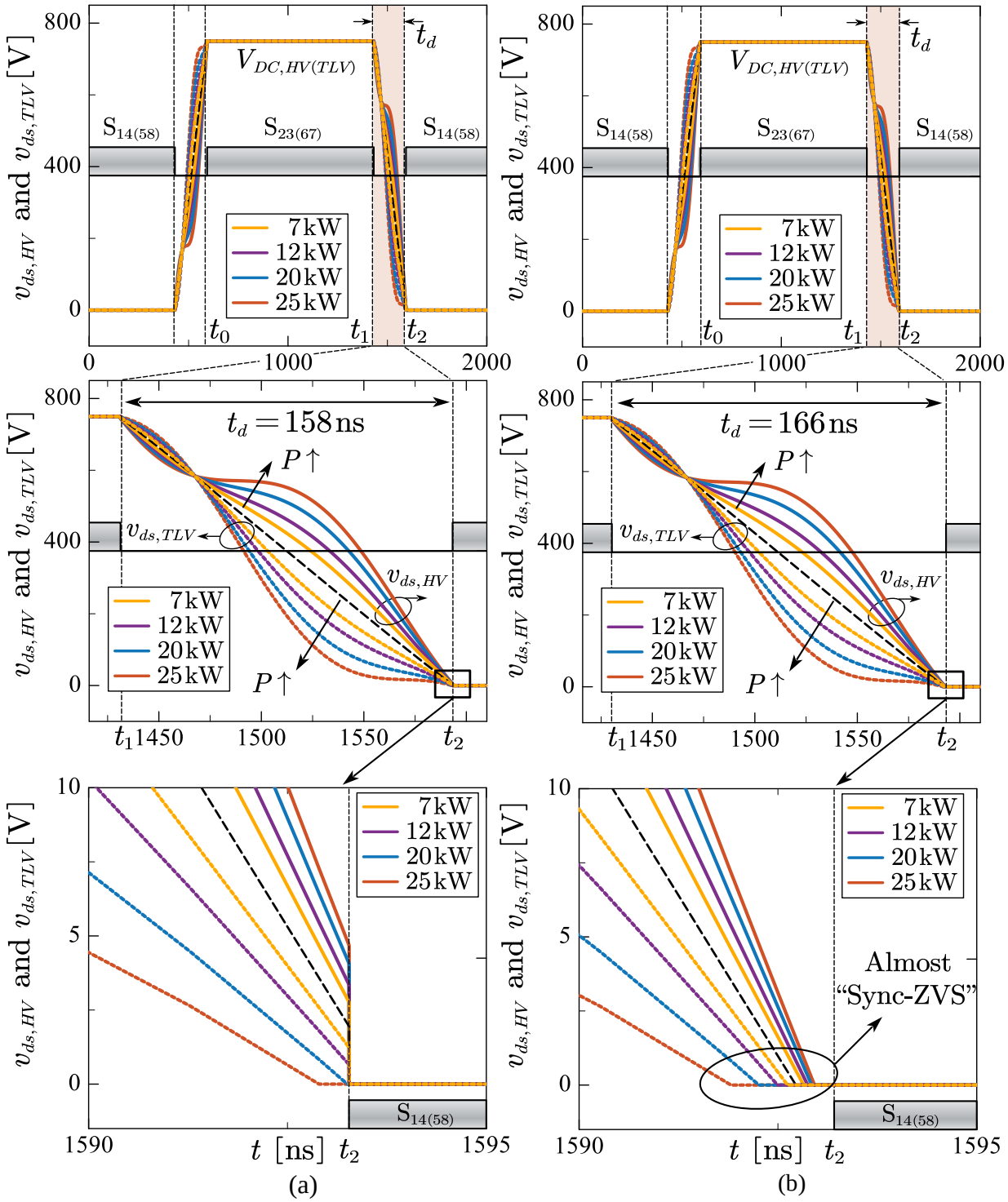


Fig. 2-12. Simulated voltages $v_{ds,HV}$, $v_{ds,TLV}$ in *case* 2 when equivalent switch output capacitance $C_{oss,eq}$ has a +5% tolerance. (a) t_d=158 ns, (b) t_d=166 ns. The simulated

To ensure the full ZVS operation, a small margin for t_d will be given in the real implementation. If a 5% margin of t_d (t_d = 166 ns) is given, the simulated voltages $v_{ds,HV}$ and $v_{ds,TLV}$ are depicted in **Fig. 2-12(b)**. Since both $v_{ds,HV}$, and $v_{ds,TLV}$ will decrease to 0 V before t_2, both HV and TLV sides can achieve the full ZVS. It should be noted that although CLLC-DCX operates in *Type III* as shown in **Fig. 2-5(c)**, in which the TLV side will complete the ZVS prior to HV side, the deadtime loss $P_{dt.loss}$ will be ignorable because the end time difference for both sides ZVS is only about 1 ns. Thus, the HV and TLV sides almost complete ZVS at the same time, which means the "Sync-ZVS" transition has almost reached. Therefore, it can be concluded that the proposed ACS method is robust with a small parasitic output capacitance tolerance.

2.4 Efficiency Optimization

2.4.1 Conduction Loss

Due to the current decomposition from Eq. (2.13), the rms currents $I_{rms,HV}$, and $I_{rms,TLV}$ can be derived as

$$\begin{cases} I_{rms,HV} = \sqrt{\frac{2}{T_s}\int_{t_0}^{t_2} (i_r(t) + i_{m,HV}(t))} \\ I_{rms,TLV} = \sqrt{\frac{2}{T_s}\int_{t_0}^{t_2} (i_r(t) + i_{m,TLV}(t))} \end{cases} \tag{2.30}$$

Where T_s ($1/f_s$) is calculated from Eq. (2.26). After obtaining the rms currents on both sides, the conduction loss P_{cond} can be given as

$$P_{cond} = 2 \cdot (I_{rms,HV}{}^2 R_{ds,HV} + I_{rms,TLV}{}^2 R_{ds,TLV}) \tag{2.31}$$

Where $R_{ds,HV}$ and $R_{ds,TLV}$, are the on-state resistances for HV and LV sides switch.

2.4.2 Switching Loss

As shown in **Fig. 2-5(d)**, switching loss of the "Sync-ZVS" transition will occur at both HV and LV sides because turn-off currents $i_{HV}(t_1)$ and $i_{TLV}(t_1)$ are not equal to zero. The total switching loss P_{sw} on both sides can be derived as

$$P_{sw} = \frac{V_{DC,HV}}{V_{ds,ref}} \left(E_{off,HV}(i_{HV}(t_1)) + E_{off,TLV}(i_{TLV}(t_1))\right) f_s \tag{2.32}$$

Where $V_{ds,ref}$ is the reference drain-source voltage, and $E_{off,HV(TLV)}$ is the turn-off energy per switching cycle at HV and LV side switches with a given turn-off current.

2.4.3 Proposed Optimization Procedure

From Eq. (2.31) and (2.32), the total semiconductor loss, including conduction loss and switching loss, can be expressed as

$$P_{total} = P_{cond} + P_{sw} \tag{2.33}$$

To design a high-efficiency CLLC-DCX with "Sync-ZVS" transition in the full load range, an overall optimization procedure including four steps is proposed in **Fig. 2-13** and listed below.

Step 1 — According to V_{HV} and V_{LV} on both sides, transformer turns ratio n can be selected. With this turns ratio n, all parameters at the LV side are transformed to the HV side from Eq. (2.2)-(2.4) for calculation simplicity.

Step 2 — With the consideration of the total power density, the optimal resonant frequency $f_{r,opt}$ is determined. After the design and fabrication of the transformer, the resonant inductances $L_{r,HV(TLV)}$ on both sides are determined by the leakage inductance. With pre-determined $f_{r,opt}$, and $L_{r,HV(TLV)}$, the resonant capacitances $C_{r,HV(TLV)}$ on both sides can be calculated from Eq. (2.1).

Step 3 — Substituting the $f_{r,opt}$ from *step 2* to Eq. (2.26) and (2.27) can derive the relationship between f_s (L_m) and t_d. The range of t_d is determined from Eq. (2.29) with the maximum output power, P_{max}.

Step 4 — In order to optimize the efficiency, the total loss P_{total} from Eq. (2.33) is swept with t_d. The optimal $t_{d,opt}$ in the range from step 3 can be determined to obtain the minimum loss. The corresponding optimal $f_{s,opt}$ and $L_{m,opt}$ can be derived from Eq. (2.26) and (2.27). An example of this procedure will be given in the next Section.

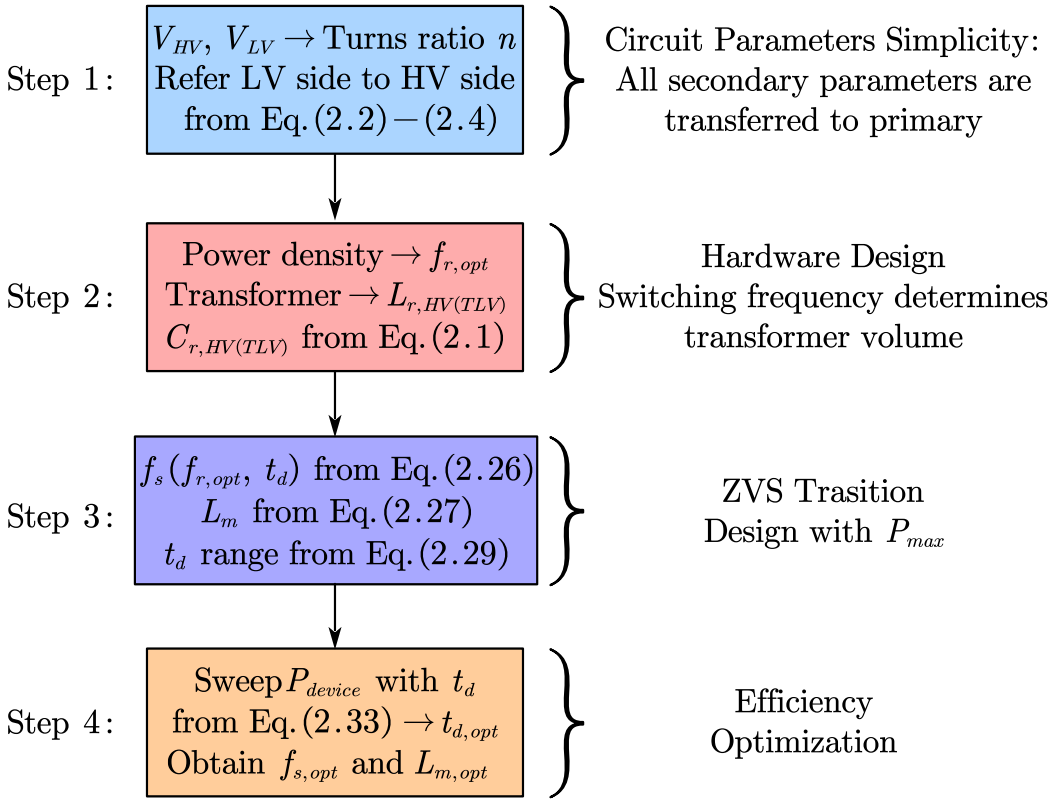


Fig. 2-13. Proposed optimization procedure for CLLC-DCX. A specific example can be found in Fig. 2-15.

2.5 Hardware Prototype and Experimental Results

2.5.1 Prototype Implementation

As shown in **Fig. 2-14**, three 18 kW CLLC-DCX prototypes (*DCX I*, *II*, and *III*) with similar power density, 150 W/in3, were built to verify the proposed "Sync-ZVS" transition and ACS method. The parameters of these prototypes are listed in **Table 2-2**. A 2:1 transformer, as shown in **Fig. 2-14(a)**, is shared with *DCX I* and *II*, and a 1:1 transformer, as shown in **Fig. 2-14(b)**, is adopted by *DCX III*. Compared with *DCX II*, *DCX III* only replaces 650 V SiC MOSFET with 1.2 kV because $V_{DC,LV}$ becomes 750 V. Following the optimization procedure in **Fig. 2-13**, the optimal resonant frequency, $f_{r,opt}$ for *DCX I-III*, which is first determined to 500 kHz with the consideration of power density and efficiency. Take *DCX I* as an example; the optimal dead time $t_{d,opt}$ is determined as 120 ns by sweeping P_{total} with t_d, as shown in **Fig. 2-15**. The range of t_d is derived from Eq. (2.29). From Eq. (2.26) and (2.27), the corresponding $f_{s,opt}$, and $L_{m,opt}$ can be determined to be 455 kHz and 26.8 μH. Following the same procedure, $t_{d,opt}$, $f_{s,opt}$, and $L_{m,opt}$ for *DCX II* and *III* can be obtained, respectively.

Table 2-2 THE PARAMETERS OF THREE PROTOTYPES INCLUDING PARASITICS

	DCX I	*DCX II*	*DCX III*
$V_{DC,HV}$ and $V_{DC,LV}$	750 V/375 V	750 V/375 V	750 V/750 V
P_{max}	18 kW	18 kW	18 kW
$f_{r,opt}$	500 kHz	500 kHz	500 kHz
Turns ratio n	2:1	2:1	1:1
$C_{oss,HV}$	2 × 418 pF	2 × 418 pF	2 × 418 pF
HV Switch	2 × C3M0016120	2 × C3M0016120	2 × C3M0016120
$C_{oss,LV}$	4 x 276 pF	1800 pF	2 x 418 pF
LV Switch	4 x GS66516T	UF3SC065007K4S	2 × C3M0016120
$C_{r,HV}$ and $C_{r,LV}$	138 nF/560 nF	138 nF/560 nF	110 nF/110 nF
$L_{r,HV}$ and $L_{r,LV}$	730 nH/181 nH	730 nH/181 nH	784 nH/795 nH
$f_{s,opt}$	455 kHz	442 kHz	433 kHz
$t_{d,opt}$	120 ns	142 ns	196 ns
$L_{m,opt}$	26.8 μH	25.4 μH	28.5 μH

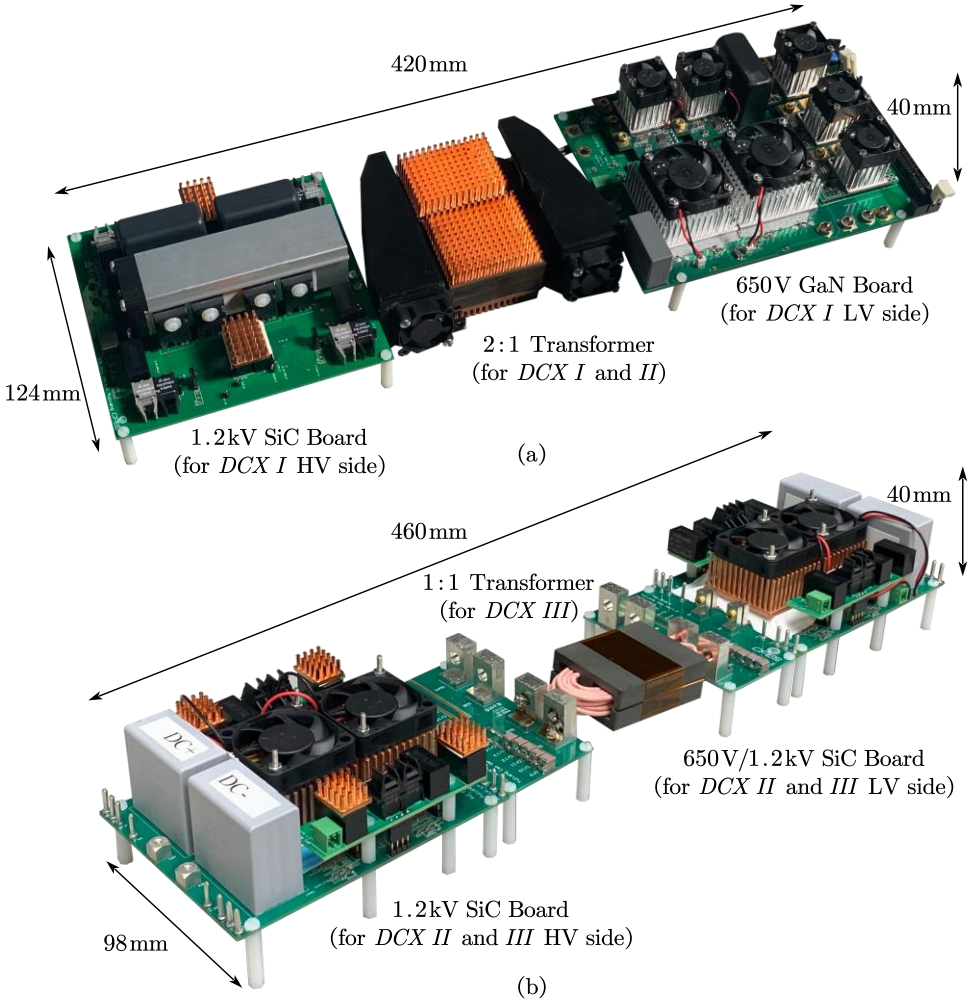


Fig. 2-14. Three 18 kW CLLC-DCX prototypes (a) *DCX I*, (b) *DCX II* and *III*. The related circuit parameters can be found in Table 2-2.

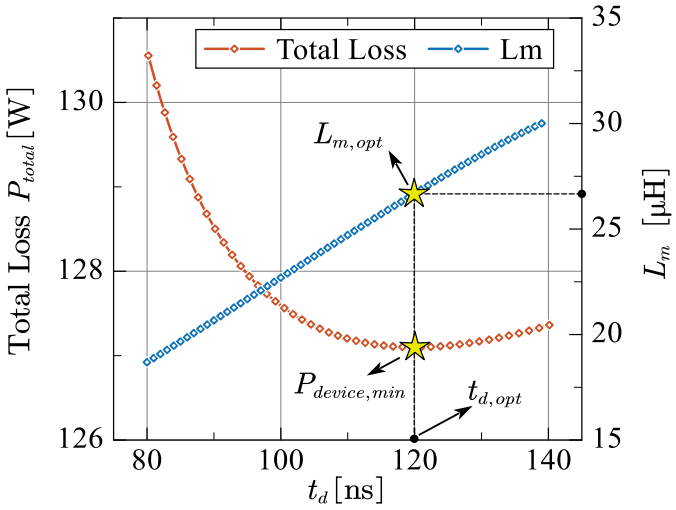


Fig. 2-15. Efficiency optimization for *DCX I*. Total loss is composed of both conduction and switching loss. The optimization follows the procedure in Fig. 2-13.

2.5.2 Experimental Results of *DCX I*

Fig. 2-16 plots and overlaps the simulation and experimental results of *DCX I* during one switching period at 18 kW. **Fig. 2-16(a)** shows $v_{ds,HV}$, and $v_{ds,LV}$ of both sides, whereas **Fig. 2-16(b)** depicts the critical resonant currents i_{HV}, i_{LV}, and magnetizing current i_m. **Fig. 2-16(c)** and **(d)** are the zoomed-in voltage and current waveforms around the deadtime region (1400 - 1700 ns). It can be observed that $v_{ds,HV}$, and $v_{ds,LV}$ transitions start and finish at the same time, which implies the realization of the "Sync-ZVS" transition. This is because the current polarity meets the initial condition requirement, and the ACS method is applied.

In the second test, the f_s is increased to 482 kHz, and *DCX I* will operate in *Type II* ZVS transition, as shown in **Fig. 2-17**. The key difference from the previous one is that the secondary side voltage $v_{ds,LV}$, starts the voltage drop later but reaches zero in advance. As explained earlier, this working mode introduces larger deadtime loss $P_{dt,loss}$ as shown in **Fig. 2-17(c)** and the efficiency lower than the "Sync-ZVS" design.

In order to verify the almost load-independent characteristic of the proposed design, the steady-state waveforms of *DCX I* at 11 kW are shown in **Fig. 2-18**.

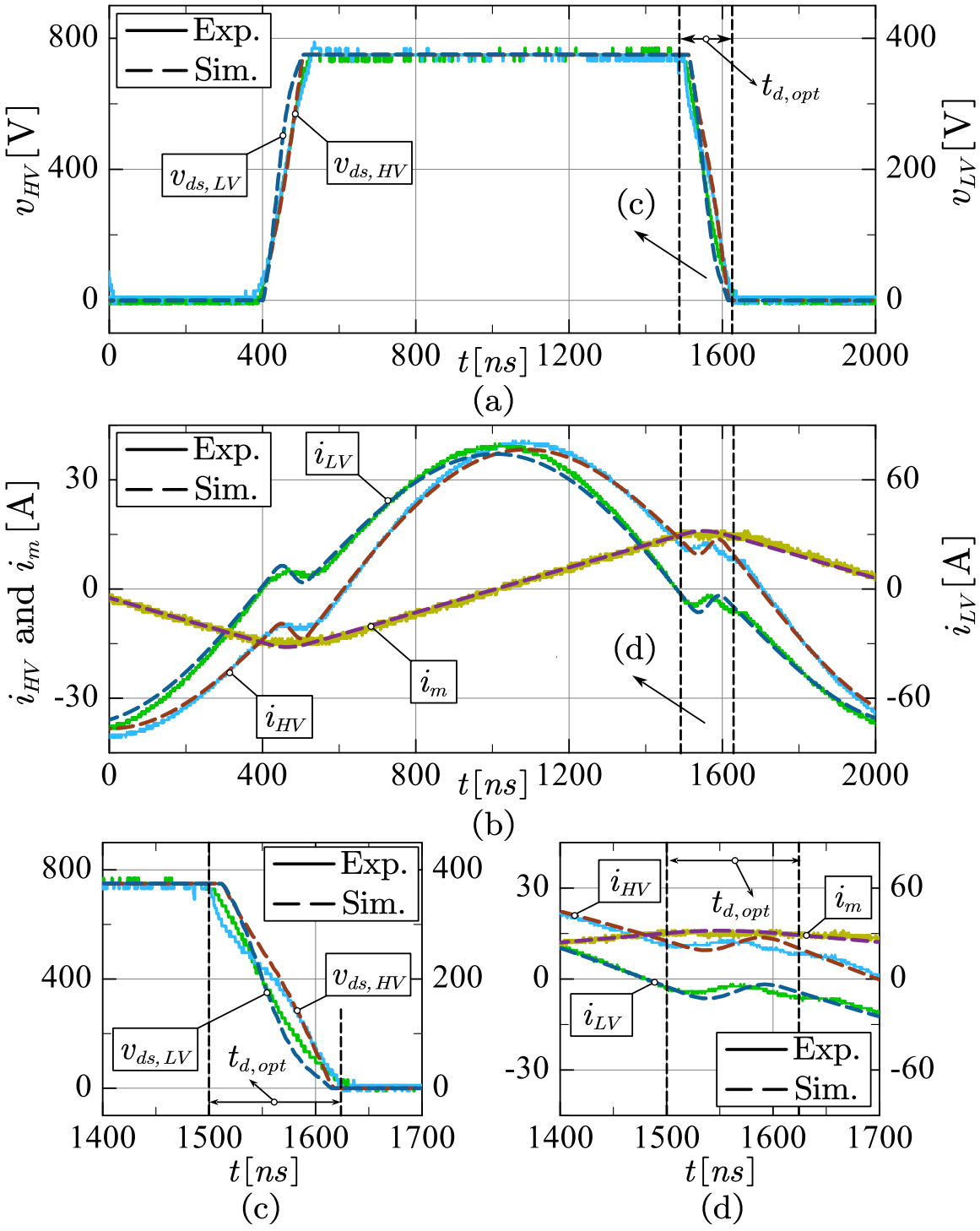


Fig. 2-16. Simulation and experimental results of *DCX I* with "Sync-ZVS" transition. (a) Voltage waveforms. (b) Current waveforms. (c) Zoomed-in voltage waveforms (d) Zoomed-in current waveforms. The CLLC-DCX operates at 18 kW with $f_{s,opt}$ as 455 kHz. The related circuit parameters can be found in Table 2-2.

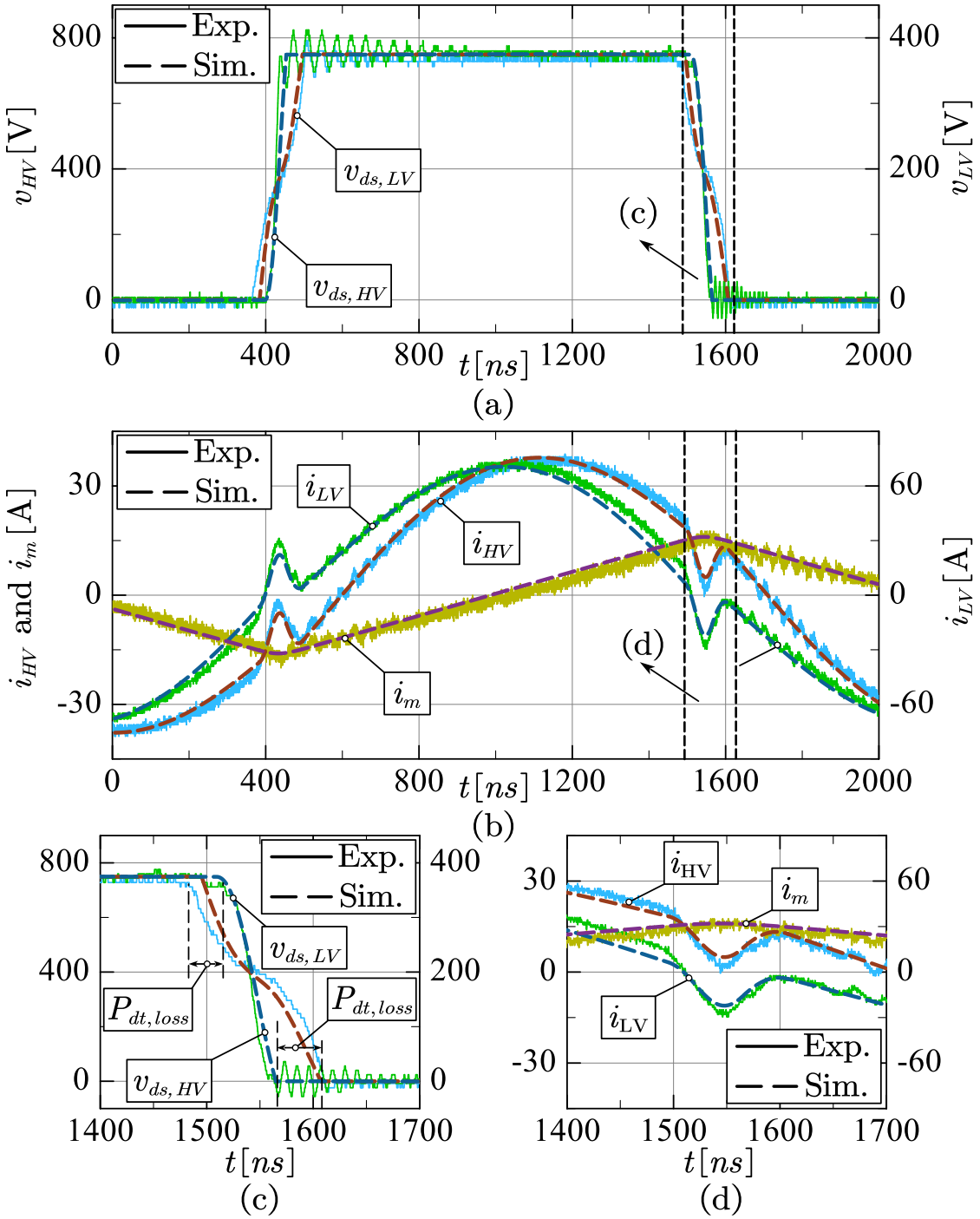


Fig. 2-17. Simulation and experimental results of *DCX I* with *Type II* ZVS transition. (a) Voltage waveforms. (b) Current waveforms. (c) Zoomed-in voltage waveforms (d) Zoomed-in current waveforms. The CLLC-DCX operates at 18 kW with 482 kHz. The related circuit parameters can be found in Table 2-2.

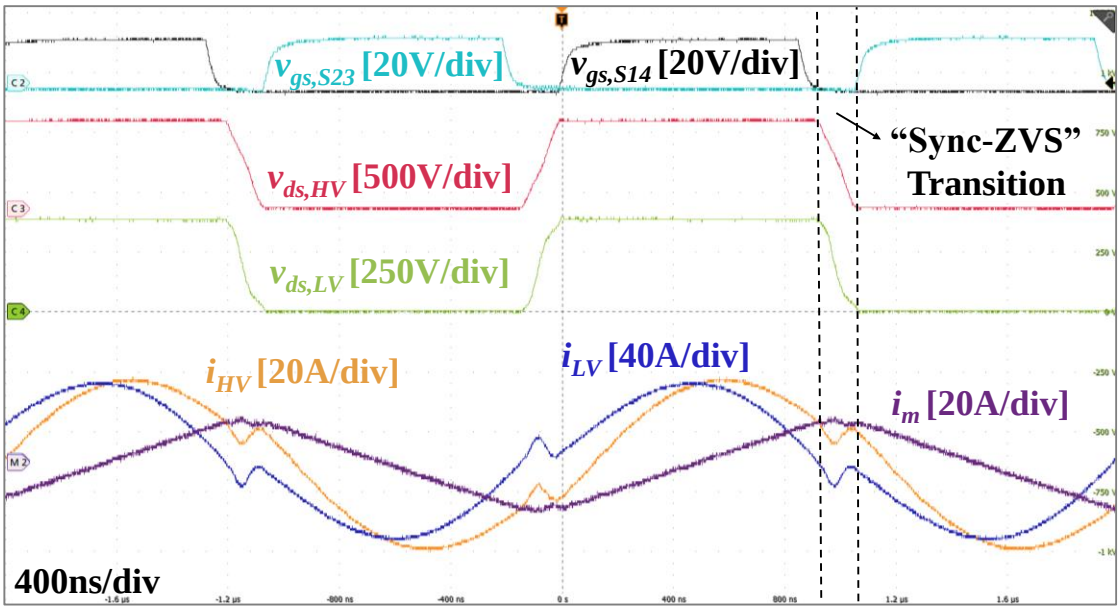


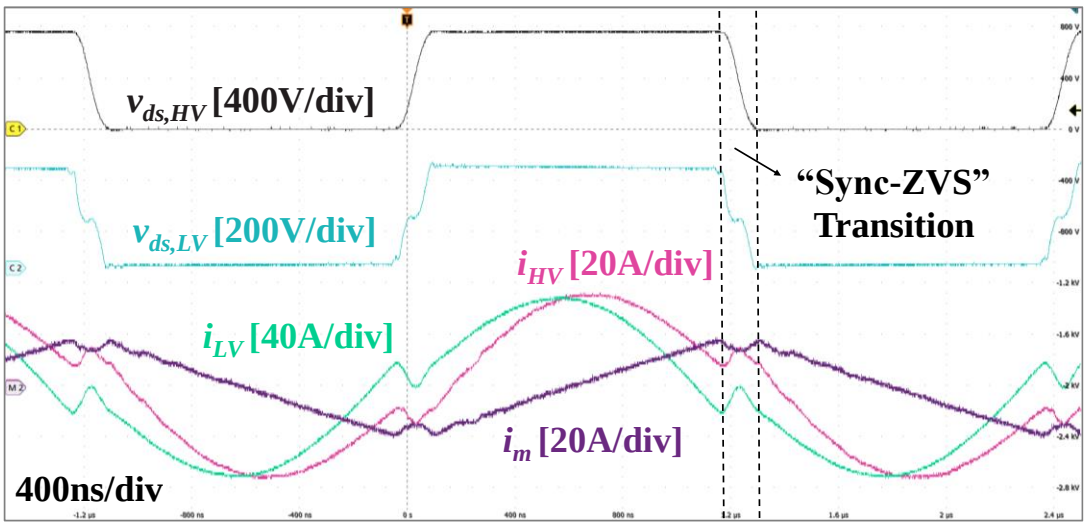
Fig. 2-18. Steady-state waveforms of *DCX I* at 11 kW with "Sync-ZVS" transition at 455 kHz. The related circuit parameters can be found in Table 2-2.

2.5.3 Experimental Results of *DCX II*

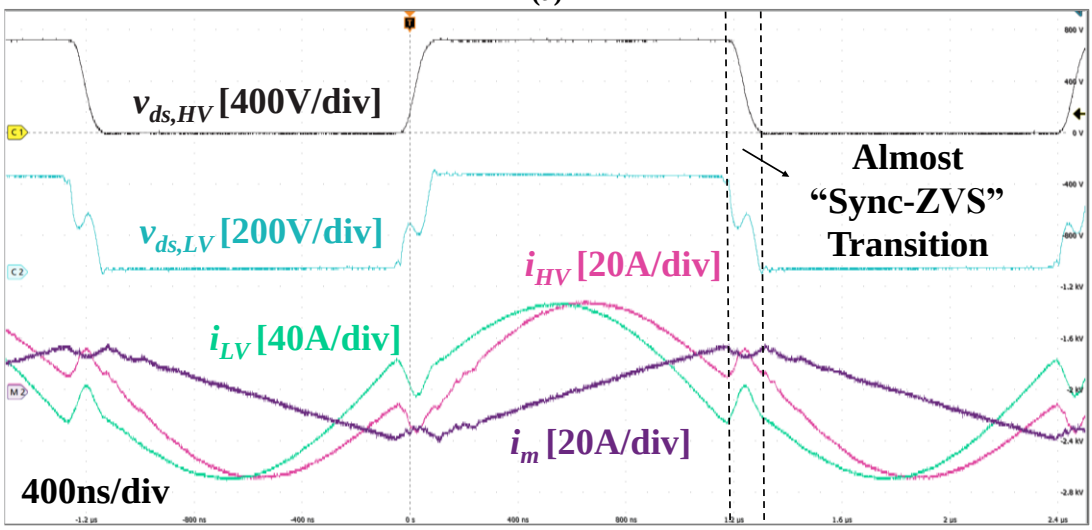
As shown in **Fig. 2-19**, the experimental results of *DCX II* with three ZVS transition types are depicted at 15 kW. In **Fig. 2-19(a)**, the "Sync-ZVS" transition is achieved in DCX II with the proposed ACS method and desirable $t_{d,opt}$, $f_{s,opt}$ as listed in **Table 2-2**. Similar to *DCX I*, HV and LV sides begin and end the ZVS transition at the same time.

Considering a small variation of $f_{s,opt}$ occurs, **Fig. 2-19(b)** shows the experimental results when f_s changes to 460 kHz from 442 kHz. Except for the slightly larger ringing current than **Fig. 2-19(a)**, the "Sync-ZVS" transition has almost been achieved at 462 kHz. Therefore, this small f_s variation experimental result can reflect the robustness of the proposed ACS method.

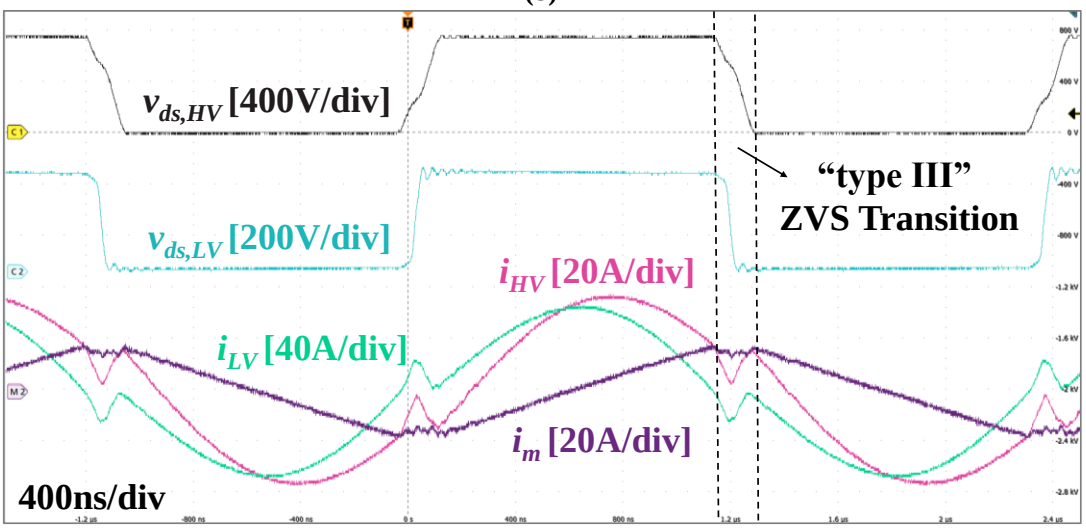
When the switching frequency f_s deviates further to 490 kHz and 400 kHz without a proper design, *DCX II* will operate in *Type III* and *VI* ZVS transition, as shown in **Fig. 2-19(c)** and **(d)**, respectively. The results match the analysis and waveforms in **Fig. 2-5**.


$v_{ds,HV}$ [400V/div]
$v_{ds,LV}$ [200V/div]
i_{HV} [20A/div]
i_{LV} [40A/div]
i_m [20A/div]
"Sync-ZVS" Transition
400ns/div

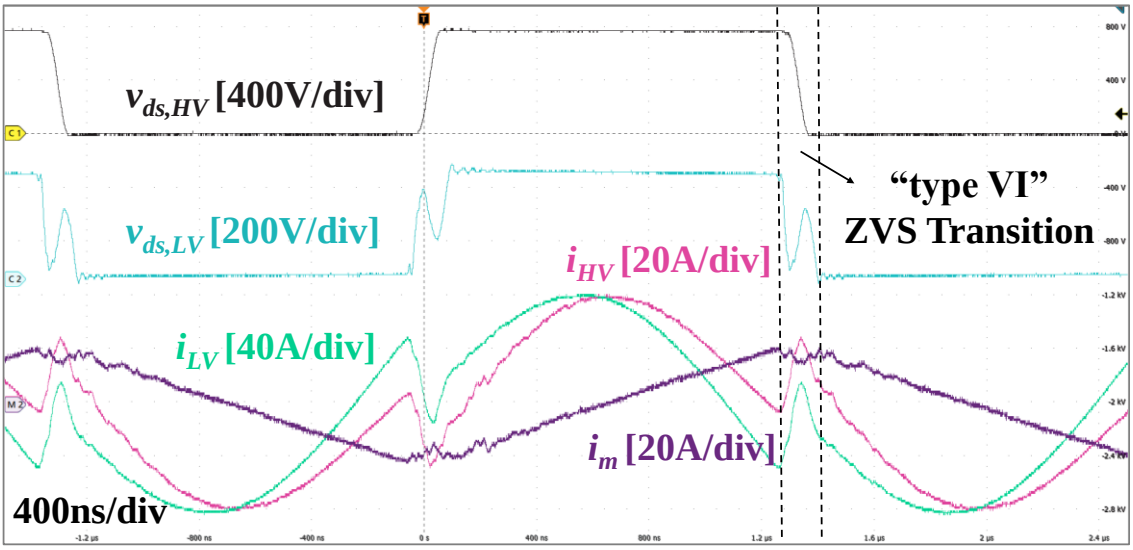
(a)


$v_{ds,HV}$ [400V/div]
$v_{ds,LV}$ [200V/div]
i_{HV} [20A/div]
i_{LV} [40A/div]
i_m [20A/div]
Almost "Sync-ZVS" Transition
400ns/div

(b)


$v_{ds,HV}$ [400V/div]
$v_{ds,LV}$ [200V/div]
i_{HV} [20A/div]
i_{LV} [40A/div]
i_m [20A/div]
"type III" ZVS Transition
400ns/div

(c)



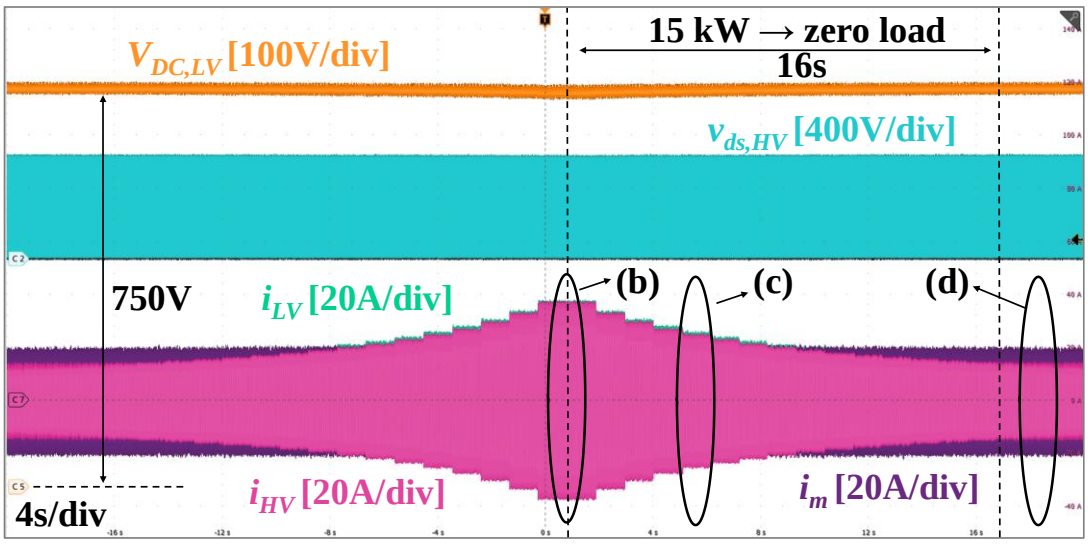
(d)

Fig. 2-19. Steady-state waveforms of *DCX II* at 15 kW: (a) "Sync-ZVS" transition at 442 kHz, (b) almost "Sync-ZVS" transition at 460 kHz, (c) *Type III* ZVS transition at 490 kHz, (d) *Type VI* ZVS transition at 400 kHz. The results match the analysis and waveforms in Fig. 2-5.

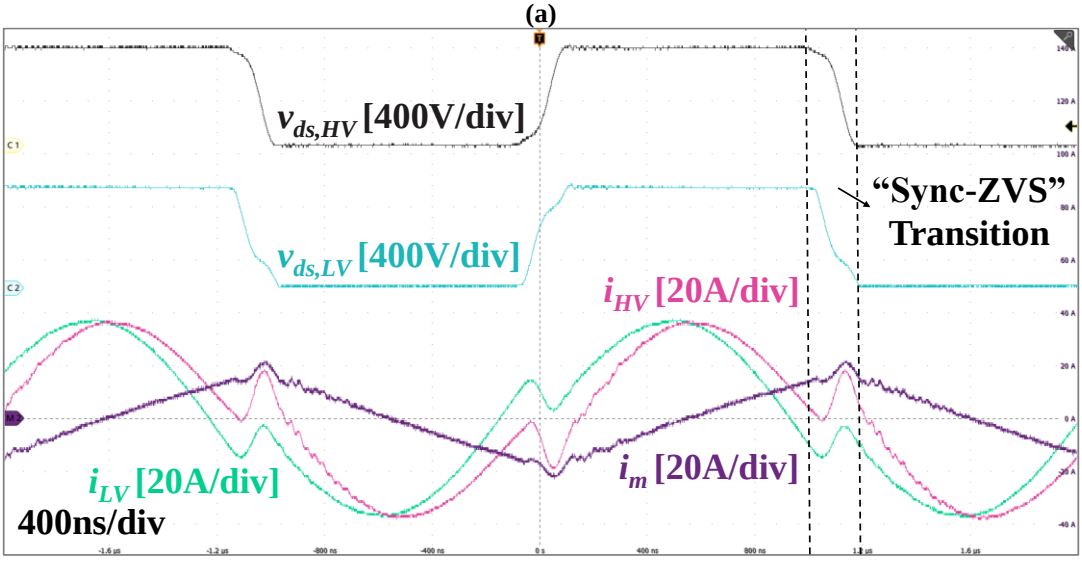
2.5.4 Experimental Results of *DCX III*

In order to validate the dynamic performance of the DCX, the load resistance is changed continuously, as shown in **Fig. 2-20(a)**. When the load decreases from 15 kW to zero load, the output voltage $V_{DC,LV}$ remains almost constant at 750 V. The corresponding voltage gain of *DCX III* with different load conditions is depicted in **Fig. 2-21**. Since the voltage gain is almost constant (less than 0.6% deviation), the almost load-independent voltage gain is verified.

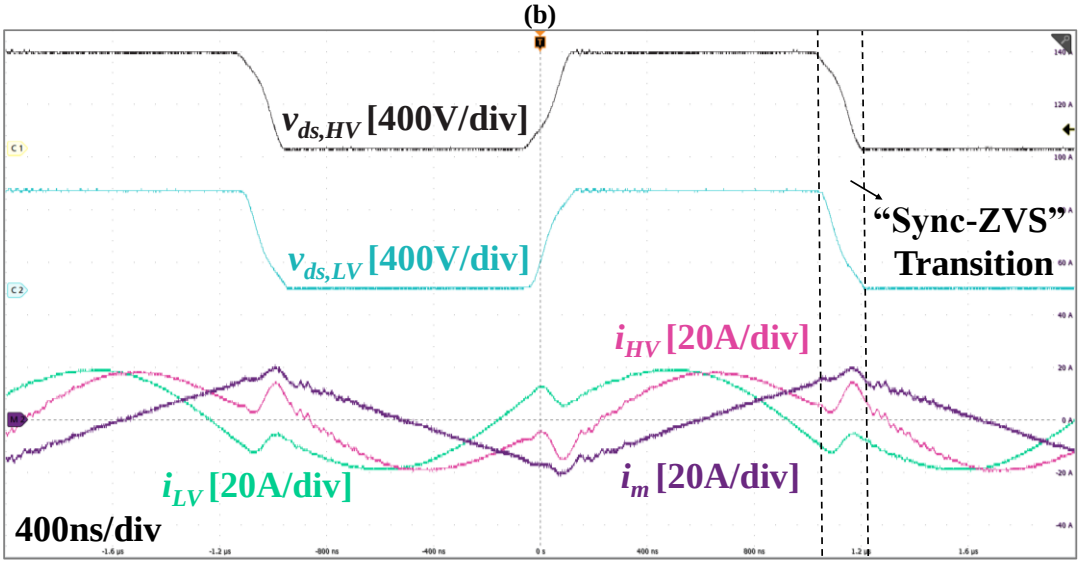
Furthermore, three cases under different loads (15 kW, 8 kW, and zero loads) are zoomed in, as shown in **Fig. 2-20(b)-(d)**. The "Sync-ZVS" transition has been realized in all three of these cases.


$V_{DC,LV}$ [100V/div]
15 kW → zero load
16s
$v_{ds,HV}$ [400V/div]
750V
i_{LV} [20A/div]
(b)
(c)
(d)
i_{HV} [20A/div]
i_m [20A/div]
4s/div

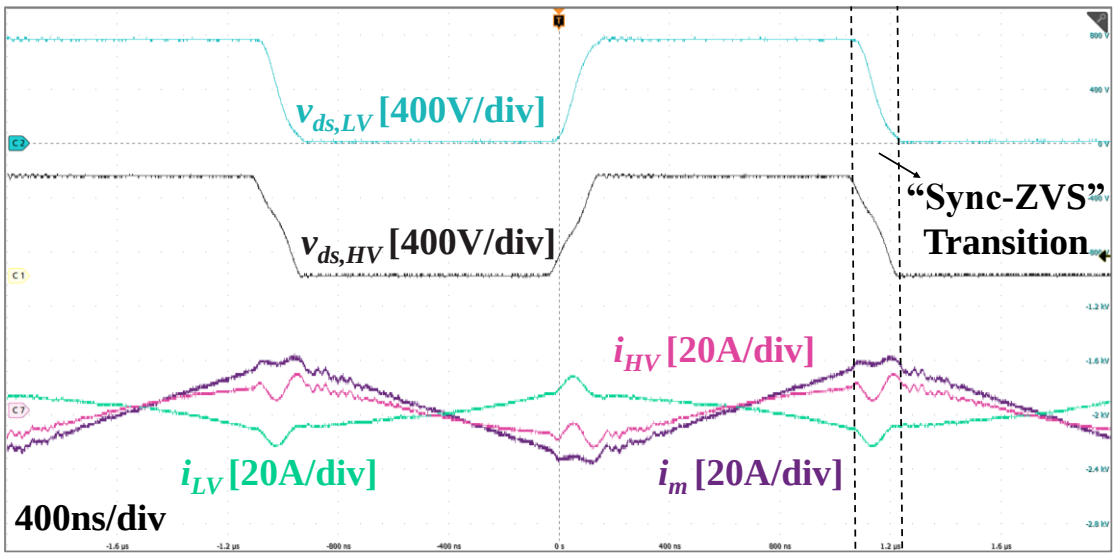
(a)


$v_{ds,HV}$ [400V/div]
"Sync-ZVS" Transition
$v_{ds,LV}$ [400V/div]
i_{HV} [20A/div]
i_{LV} [20A/div]
i_m [20A/div]
400ns/div

(b)


$v_{ds,HV}$ [400V/div]
"Sync-ZVS" Transition
$v_{ds,LV}$ [400V/div]
i_{HV} [20A/div]
i_{LV} [20A/div]
i_m [20A/div]
400ns/div

(c)



(d)

Fig. 2-20. Experimental results of *DCX III* at 15 kW (a) Load changing test from 15 kW to zero load (b) static waveforms at 15 kW (c) static waveforms at 7 kW (d) static waveforms at no load. The related voltage gain measurement was plotted in Fig. 2-21.

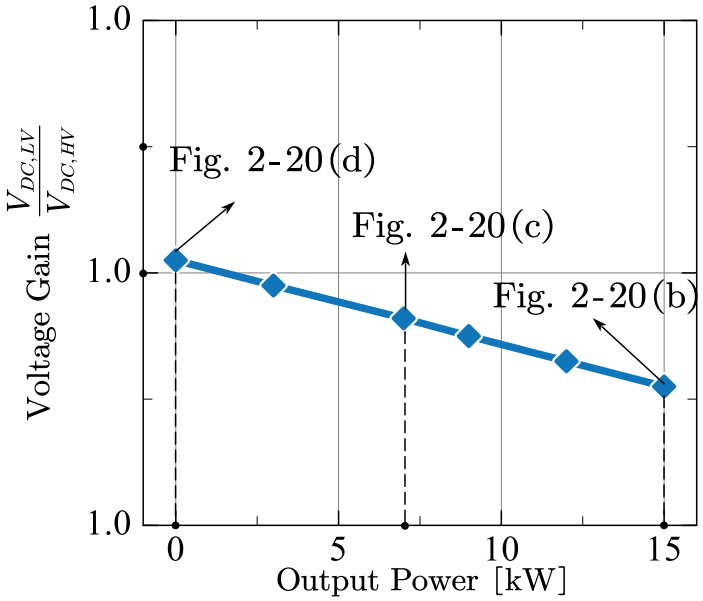


Fig. 2-21. Experimental voltage gain of *DCX III* from 15 kW to zero load. Input voltage $V_{DC,HV}$ remains constant at 750 V during load changing. The corresponding testing results can be found in Fig. 2-20.

2.5.5 Efficiency

With the consideration of auxiliary losses such as gate driving losses, controller losses, and cooling fans losses, the conversion efficiency of *DCX I* with "Sync-ZVS" and *Type II* transition were both measured with Keysight PA 2203A power analyzer as shown in **Fig. 2-22**. Compared with *Type II* transition, the "Sync-ZVS" transition has higher efficiency in the full load range due to no deadtime conduction loss $P_{dt,loss}$. At 18 kW, the efficiencies of "Sync-ZVS" and *Type II* transition are 98.7% and 98.3%, respectively. At 8 kW, compared with the *Type II* transition, the "Sync-ZVS" transition has a 0.8% efficiency improvement.

In addition, the loss breakdown and loss distribution of *DCX I* at 18 kW are plotted in **Fig. 2-23** and **Fig. 2-24**, respectively. As shown in **Fig. 2-23**, the conduction loss P_{cond} with *Type II* transition is significantly larger than the "Sync-ZVS" transition because deadtime loss $P_{dt,loss}$ is included in conduction loss P_{cond}. The winding loss P_{wind} with *Type II* transition is larger than the "Sync-ZVS" transition because a larger current spike during the dead time in **Fig. 2-17** will increase the rms value of currents through the transformer. More details about the *DCX I* transformer loss analysis can be found in [54], [55]. As for the switching loss P_{sw}, core loss P_{core}, and auxiliary loss P_{aux}, these losses are very close between "Sync-ZVS" and *Type II* transition. The slight difference between them is caused by a small switching frequency difference.

The increasing P_{cond} can also be reflected in **Fig. 2-24**. The weight of P_{cond} in *Type II* is 6.4% greater than the "Sync-ZVS" transition.

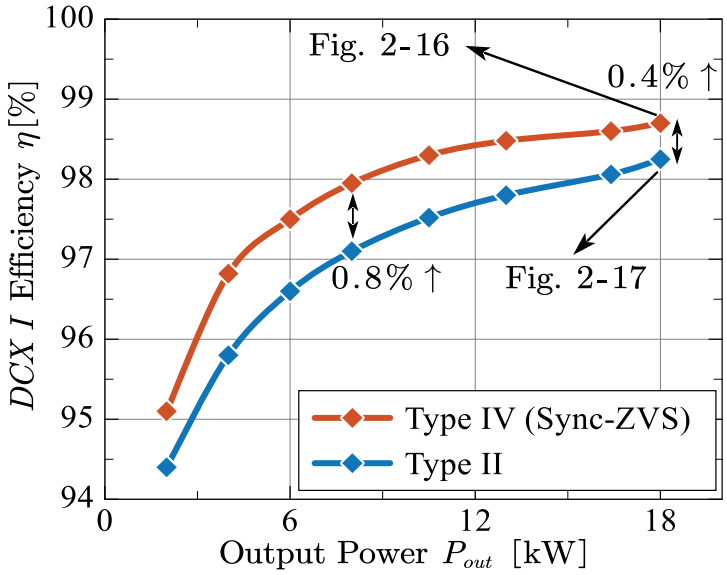


Fig. 2-22. The efficiency of *DCX I* with "Sync-ZVS" and *Type II* transition. The corresponding testing waveforms can be found in Fig. 2-16 and Fig. 2-17.

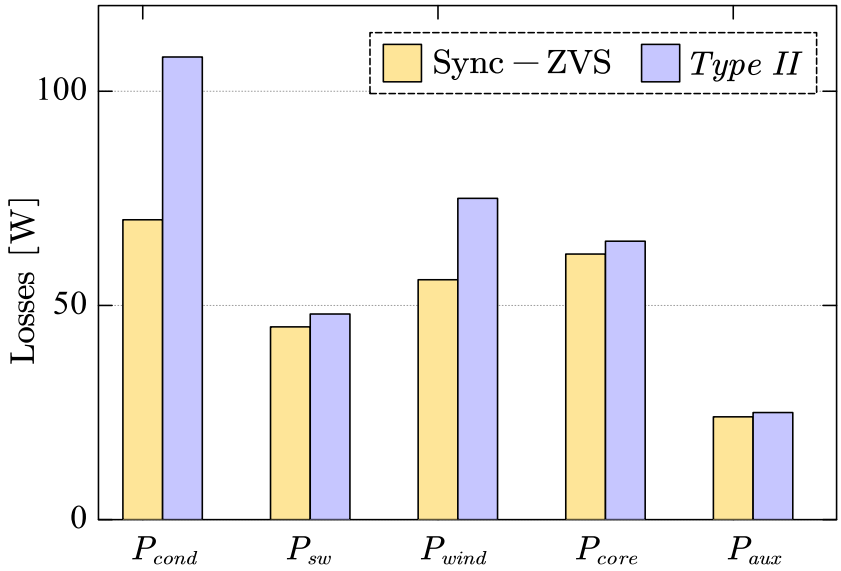


Fig. 2-23. Loss breakdown of *DCX I* with "Sync-ZVS" and *Type II* transition at 18 kW.

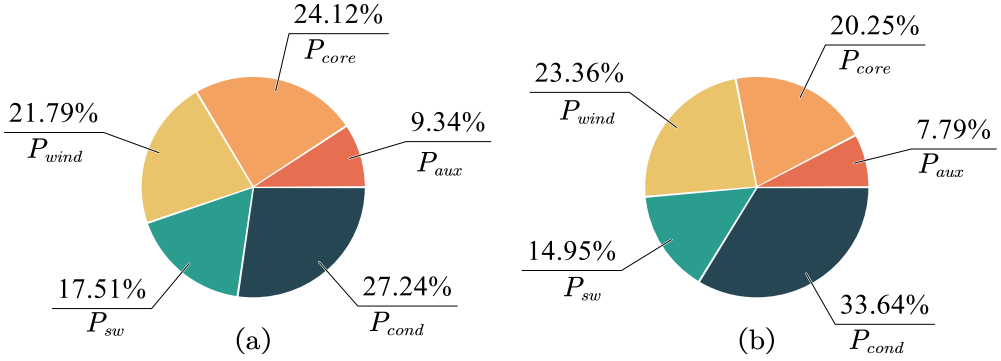


Fig. 2-24. Loss distribution of *DCX I* at 18 kW: (a) "Sync-ZVS," (b) *Type II*.

2.6 Conclusion

In this chapter, a comprehensive switching transient analysis for open-loop CLLC-DCX with DAS modulation is presented. Among seven ZVS transition types, one desirable “Sync-ZVS” transition is identified with the merits of minimum dead time, almost load-independent voltage gain, and no deadtime conduction loss. In order to achieve this “Sync-ZVS” transition in the full load range, the ACS method was proposed based on the current decomposition. Following this method, an overall design procedure for open-loop CLLC-DCX with DAS modulation was proposed to achieve high efficiency.

Finally, the proposed “Sync-ZVS” transition and “ACS” method are both verified by three 18 kW CLLC-DCX prototypes with DAS modulation, which all operate around 500 kHz and have 98.7% peak efficiency. The proposed method has great potential to improve the performance of DCX used in EV charging systems and solid-state transformers.

Chapter 3

Electronic-Embedded Transformer (EET), A New Concept for Scalable High-Frequency High-Power DCX

3.1 Introduction

In the previous chapter, the switching transition of CLLC-DCX has been optimized and realized high efficiency. However, resonant CLLC-DCX has two remaining challenges: one is a trade-off in high-frequency and high-power transformer design, and the other is the relatively large rms current with sinusoidal current [56].

To break the transformer design trade-off between power rating and operation frequency, a scalable electronic-embedded transformer (EET) is proposed in **Section 3.2** with a low voltage bridge integrated into the transformer windings. Due to the simple open-loop control and natural current sharing, multiple EET units can be easily connected in parallel and scaled up to different power ratings. According to this concept, an EET-based DC transformer (EET-DCX) is proposed to solve the transformer-level paralleling and resonant point shift issues in the traditional LLC-DCX. With the help of the embedded full bridge, the impedance of the leakage inductance can be canceled completely, and thus, the EET-DCX can always work optimally at any frequency. In the meantime, EET-DCX also keeps the intrinsic merits of the LLC-DCX, such as load-independent voltage gain, simple open-loop control, full load range ZVS, and low circulating current. Benefits from these advantages, the proposed EET-DCX solution may push the transformer boundary to MHz and tens or even hundreds of kW. Finally, a 12 kW 500 kHz EET-DCX with four planar EET units was built to verify all the merits.

Afterward, **Section 3.2.2** proposes a trapezoidal current modulation for EET-DCX to reduce the rms current. Through the implementation of trapezoidal current modulation, EET-DCX can effectively reduce the rms current by 15% and 11% when compared to triangular current EET-DCX and sinusoidal current CLLC-DCX, respectively. Consequently, this modulation scheme contributes to a noteworthy reduction of total conduction loss, encompassing both semiconductor and transformer winding losses, by 28% and 23%. Notably, the proposed trapezoidal current modulation retains all the advantages of previous EET-DCX designs, including natural current sharing, optimal operation at any frequency, load-independent voltage gain, simple open-loop control, and full load range zero voltage switching (ZVS).

In light of this EET concept, **Section 3.3.1** presents two significant modifications. First, it replaces the complete full bridge with a low-voltage bidirectional AC switch. Second, it introduces a resonant commutation (RC) to realize a quasi-trapezoidal transformer current with a smaller rms value. In addition to streamlining the circuit, the proposed RC EET-DCX retains all the advantages of the original EET-DCX, including simple open-loop control and natural current sharing. By incorporating only one embedded bidirectional AC switch, the impedance of the high-frequency transformer leakage inductance is fully neutralized. As a result, the rated power of the proposed RC EET-DCX can be readily scaled up through transformer-level parallelism. Furthermore, the RC EET-DCX maintains the benefits of typical LLC/CLLC-DCX, including load-independent voltage gain, full load range zero voltage switching (ZVS), and low circulating current. To verify the aforementioned benefits, a 12 kW RC EET-DCX with four planar RC EET units was built and tested.

However, either in EET-DCX or RC EET-DCX, the trapezoidal current modulation will increase the voltage stress on the low-voltage full bridge or bidirectional AC switch, especially when the

leakage inductance is large and variable, such as in the high-power wireless charging application. To address this trade-off between rms current and voltage stress, **Section 3.4.1** proposed the concept of a hybrid resonant-type EET-DCX with a series resonant capacitor. Following this concept, two specific topologies named hybrid EET-DCX and hybrid resonant commutation (RC) EET-DCX were proposed. The main difference between these two topologies is the former adopted a full bridge, and the latter utilized only one bidirectional AC switch. Since the leakage inductance impedance can be mainly canceled by the passive capacitor, the full bridge or AC switch only needs to handle the remaining part. Thus, the voltage stress on active components can be dramatically decreased.

In addition, these two proposed topologies can both retain all the advantages of previous EET-DCX designs, including natural current sharing, load-independent voltage gain, simple open-loop control, and full-load range zero voltage switching (ZVS). The comparison between these two topologies was thoroughly studied. Finally, two 12-kW prototypes were built to verify the analysis and performance.

To summarize, this EET concept and its derivative scalable DCX family can be seen as a potential alternative in DCX applications.

3.2 The Foundation of EET-DCX

3.2.1 Operation Principle of Traditional LLC-DCX

To better understand the proposed EET and the corresponding EET-DCX, the operation principle of the traditional LLC-DCX is illustrated first. **Fig. 3-1** depicts the circuit diagram of the LLC-DCX and its corresponding voltage and current waveforms. The transformer turns ratio N is assumed to be 1:1, and the input voltage V_{in} should be equal to V_{out} at the full load range. Due to the resonance between resonant capacitor C_r and transformer leakage inductance L_k, both primary and secondary side currents i_{pri} and i_{sec} through the transformer are sinusoidal waveforms. The resonant frequency f_r of LLC-DCX can be given as

$$f_r = 1/\left(2\pi\sqrt{L_k C_r}\right) \tag{3.1}$$

If the parasitic output capacitances and deadtime are not considered, the full bridge output voltages v_{pri} and v_{sec} across jumping nodes are 50% duty square waveforms. Due to the DCX operation, the switching frequency f_s is equal to the resonant frequency f_r, which means the resonant capacitor C_r can completely cancel the impedance of L_k. Therefore, the total power loop impedance will be close to zero. Without the consideration of magnetizing current i_m, the resonant currents i_{pri} and i_{sec} are in phase with v_{pri} and v_{sec}, and the maximum real power can be transferred from the input to the output side. Therefore, LLC-DCX could achieve high efficiency. At a resonant point, the sinusoidal resonant capacitor voltage v_{Cr} will have a 90-degree phase delay with v_{pri} or v_{sec}. As for the advantage of soft switching, the magnetizing current i_m can be used to realize the full load range ZVS. As explained in [31], [33], the magnetizing current i_m can be assumed to be constant during the deadtime, and its peak value I_m can be given as

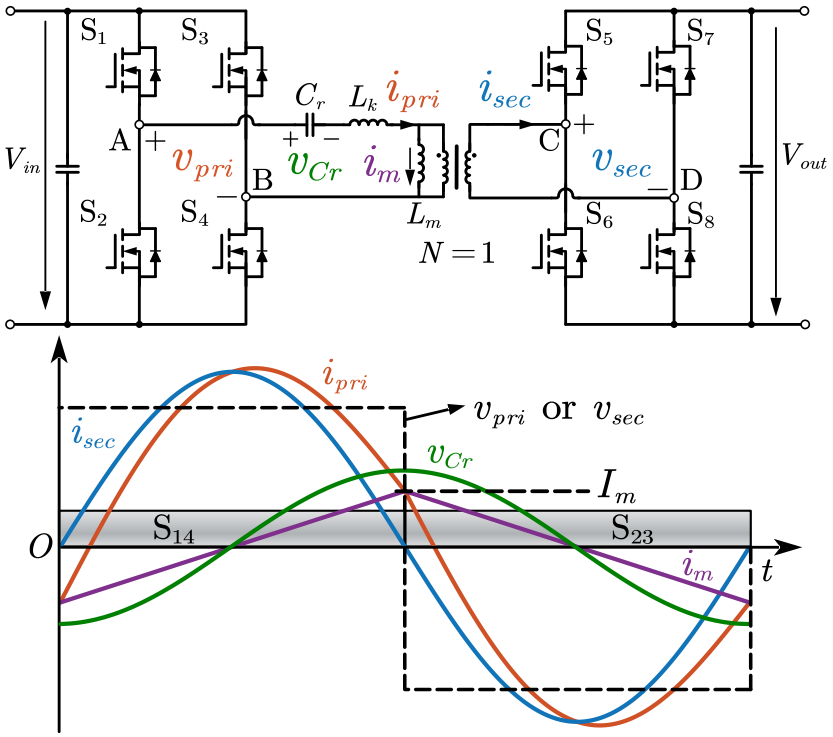


Fig. 3-1. Circuit diagram of LLC-DCX and its corresponding waveforms.

$$I_m = V_{in}/(4L_m f_s) \tag{3.2}$$

The peak current I_m should be large enough to charge and discharge the total output capacitance $C_{oss,total}$ during the dead time t_d to ensure the ZVS turn-on. To satisfy the ZVS criteria and achieve minimum conduction loss [17]-[19], the magnetizing inductance L_m and t_d should meet the following requirements.

$$L_m = t_d/(2f_s C_{oss,total}) \tag{3.3}$$

However, since the resonant tank impedance is very close to zero, a small tolerance of resonant tank parameters (C_r or L_r) or switching frequency f_s will increase the total power loop impedance dramatically. Therefore, the resonant point of LLC-DCX is very sensitive to these parameters. If LLC-DCX cannot work at its resonant point (f_s=f_r), it will lose a constant load-independent voltage gain and suffer from efficiency deterioration.

3.2.2 Operation Principle of EET-DCX

In order to solve the aforementioned problems of LLC-DCX with an integrated LV bridge, the concept of EET is proposed in **Fig. 3-2**. With the addition of two HV bridges, the circuit diagram of EET-DCX can also be found. Following the symbols of LLC-DCX, V_{in} and V_{out} are the input and output voltages, and v_{pri} and v_{sec} are two HV bridge output voltages on the primary and secondary sides. Different from LLC-DCX, the resonant capacitor C_r shown in **Fig. 3-1** has been replaced by an LV bridge with a floating DC capacitor C_b in EET-DCX. V_b is the floating DC voltage across C_b, and its amplitude will be discussed and derived later. Later, v_C is the LV bridge output voltage with the amplitude of V_b. As for the currents, i_{pri} and i_{sec} are the transformer currents through the primary and secondary sides, respectively. The magnetizing current i_m is provided by magnetizing inductance L_m. L_k is the leakage inductances of the transformer. To simplify the operation principle of EET-DCX, i_m and the mechanism of ZVS are ignored first and will be discussed in *Section IV*. Without the consideration of L_m, the simplified equivalent circuit of EET-DCX is shown in **Fig. 3-3(a)**, which includes three square waveform voltage sources: v_{pri}, v_{sec}, and v_C. The amplitudes of these three voltage sources are V_{in}, V_{out}, and V_b, respectively. Due to the ignorance of i_m, the current through the transformer is simplified as i_T.

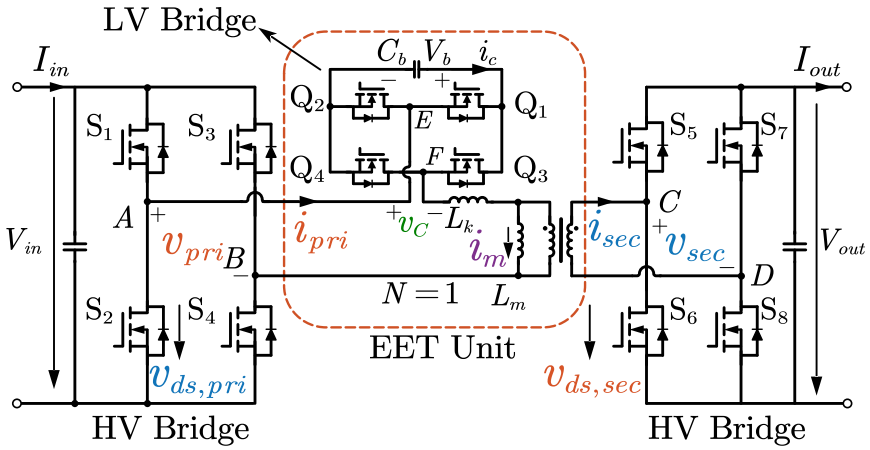


Fig. 3-2. Circuit diagram of proposed EET-DCX with one EET unit.

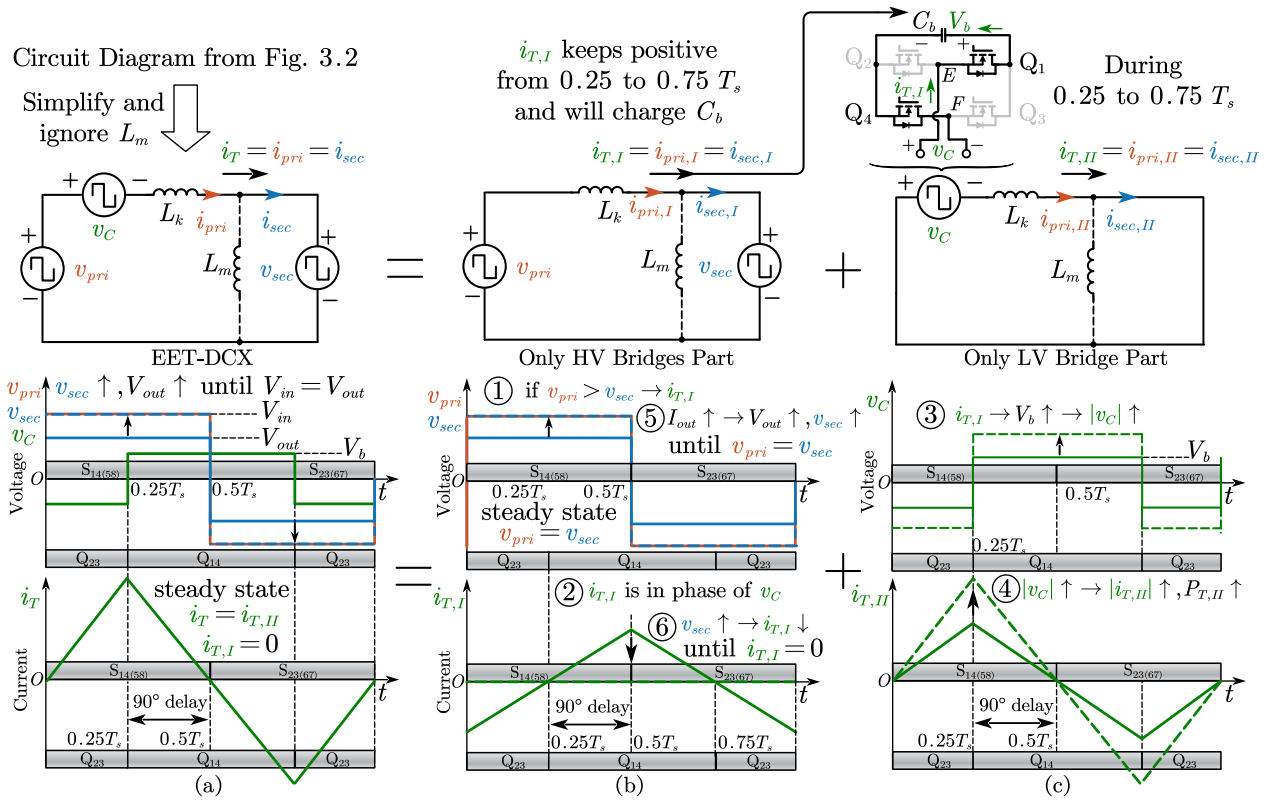


Fig. 3-3. Equivalent circuits and their corresponding waveforms: (a) whole EET-DCX, (b) only HV bridge part, and (c) only LV bridge part. The simplified circuit diagram is derived from Fig. 3-2.

$$i_T = i_{pri} = i_{sec} \tag{3.4}$$

Similar to LLC-DCX, since primary and secondary HV bridges have the same driving signals for switches $S_{1\text{-}4}$ and $S_{5\text{-}8}$, the first constraint is that v_{pri} is in phase with v_{sec}. The LV bridge $Q_{1\text{-}4}$ has a 90-degree phase delay driving signals with two HV bridges. Therefore, the second constraint is that v_C has a 90-degree phase delay with v_{pri} or v_{sec}. In addition, the third constraint is that the ripple on V_{in}, V_{out}, and V_b can be ignored. With these three constraints, the waveforms of v_{pri}, v_{sec}, and v_C are plotted in **Fig. 3-3(a)**. Based on the superposition principle, the equivalent circuit in **Fig. 3-3(a)** can be decomposed into two parts — the HV bridge part and the LV bridge part shown in **Fig. 3-3(b)** and **(c)**, respectively. Later, $i_{T,I}$, and $i_{T,II}$ are the current components with only HV bridge excitations (v_{pri} and v_{pri}) or LV bridge excitations (v_C).

$$i_T = i_{T,I} + i_{T,II} \tag{3.5}$$

With a certain load, the operation principle of EET-DCX can be explained in six steps as follows.

***Step* 1:** Assuming V_{in} is larger than V_{out}, as shown in **Fig. 3-3**, the voltage difference (V_{in}-V_{out}) will be applied to L_k directly, and the triangular current $i_{T,I}$ in **Fig. 3-3(b)** can be expressed in (**3.6**).

$$i_{T,I}(t) = \begin{cases} -\dfrac{V_{in} - V_{out}}{4L_k f_s} + \dfrac{V_{in} - V_{out}}{L_k} \cdot t & t \in [0,\ 0.5T_s] \\ \dfrac{3(V_{in} - V_{out})}{4L_k f_s} - \dfrac{V_{in} - V_{out}}{L_k} \cdot t & t \in [0.5T_s,\ T_s] \end{cases} \tag{3.6}$$

The power $P_{T,I}$ delivered to the receiving side by the current $i_{T,I}$ can be given as

$$P_{T,I} = \int_0^{T_s} v_{sec}(t) \cdot i_{T,I}(t) \tag{3.7}$$

As shown in **Fig. 3-3(b)**, since v_{sec} always has a 90-degree phase difference from $i_{T,I}$, no power can be transferred by $i_{T,I}$.

***Step* 2:** Since the current $i_{T,I}$ in **Fig. 3-3(b)** is in phase with the voltage v_C in **Fig. 3-3(c)**, it will always charge the floating capacitor C_b of the LV bridge. For example, from 0.25 to 0.75 T_s, the current $i_{T,I}$ is positive as shown in **Fig. 3-3(b)**, and at the same time, LV bridge switches Q_1 and Q_4 are turned on as shown in **Fig. 3-3(c)**. As for another half period from 0.75 to 1.25 T_s, negative $i_{T,I}$ will still charge C_b through ON switches Q_2 and Q_3. To sum up, if V_{in} is larger than V_{out}, current $i_{T,I}$ will always charge C_b and increase V_b during the whole period.

***Step* 3:** With the increase of V_b, the amplitude of v_C will also increase, as shown in **Fig. 3-3(c)**.

$$i_{T,I} \rightarrow V_b \uparrow \rightarrow |v_C| \uparrow \tag{3.8}$$

***Step* 4:** As shown in **Fig. 3-3(c)**, with only one voltage source excitation v_C, current $i_{T,II}$ is triangular and can be derived as

$$i_{T,II} = \begin{cases} \dfrac{V_b}{L_k} \cdot t & t \in [-0.25T_s,\ 0.25T_s] \\ \dfrac{V_b}{2L_k f_s} - \dfrac{V_b}{L_k} \cdot t & t \in [0.25T_s,\ 0.75T_s] \end{cases} \tag{3.9}$$

With an increase of V_b from (3.8), the amplitude of current $i_{T,II}$ will become larger from (3.9). On the other hand, the power $P_{T,II}$ delivered to the receiving side by $i_{T,II}$ can be given as

$$P_{T,II} = \int_0^{T_s} v_{sec}(t) \cdot i_{T,II}(t) \tag{3.10}$$

Since v_{sec} always keeps in phase with $i_{T,II}$, with a larger $i_{T,II}$, more real power $P_{T,II}$ will be delivered to the receiving side.

***Step* 5:** if the receiving power increases with a certain load, the corresponding output voltage V_{out} will increase until V_{out} is equal to V_{in}.

$$I_{out} \uparrow \rightarrow V_{out} \uparrow, |v_{sec}| \uparrow \ \text{until}\ V_{out} = V_{in} \tag{3.11}$$

***Step* 6:** Meanwhile, assuming V_{in} is constant, an increasing V_{out} will lead to a smaller current $i_{T,I}$ from (3.6) until V_{out} is equal to V_{in}.

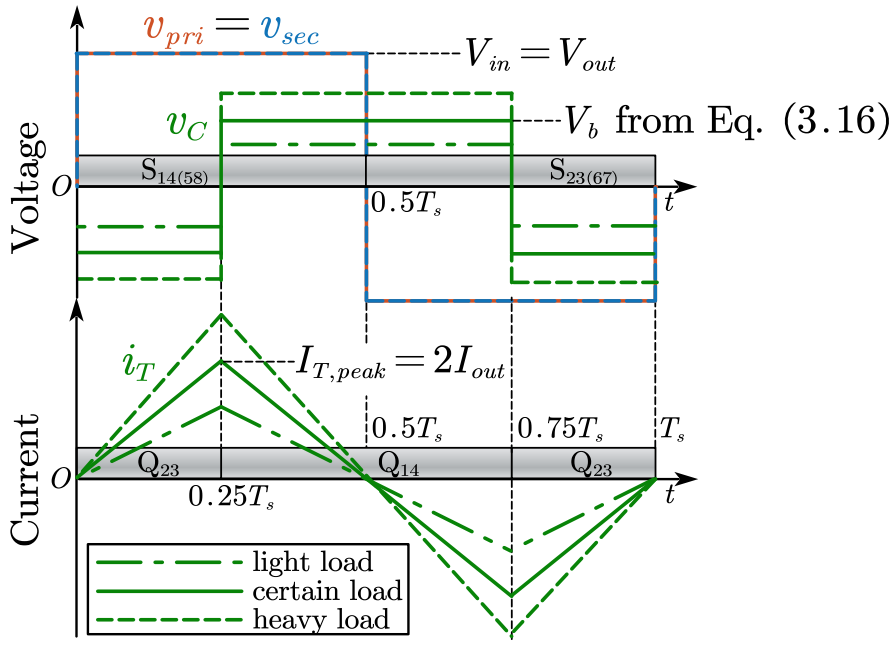


Fig. 3-4. Steady-state waveforms of EET-DCX under different load conditions. The solid line current waveforms represent a certain load case, which can be found in Fig. 3-3.

To sum up, the whole mechanism of EET-DCX can be expressed as (3.12). When V_{out} is equal to V_{in}, current $i_{T,I}$ will be equal to zero, and the DC voltage V_b should remain constant, which means the EET-DCX has entered the steady state. Previous analysis from ***Steps* 1-6** is based on V_{in} is larger than V_{out}. On the contrary, if V_{in} is smaller than V_{out}, with a similar analysis, $i_{T,II}$ will discharge the floating DC capacitor C_b and cause the output current I_{out} to drop. With a certain load, a smaller output current I_{out} will decrease output voltage V_{out} until V_{in} is equal to V_{out}.

$$\begin{cases} V_{in} > V_{out} & i_{T,II} \rightarrow V_b \uparrow \rightarrow I_{out} \uparrow \rightarrow V_{out} \uparrow \\ V_{in} = V_{out} & i_{T,II} = 0 \rightarrow V_b,\ I_{out},\ V_{out}\ \text{const} \rightarrow \text{steady state} \\ V_{in} < V_{out} & i_{T,II} \rightarrow V_b \downarrow \rightarrow I_{out} \downarrow \rightarrow V_{out} \downarrow \end{cases} \tag{3.12}$$

At the steady state, assuming the transformer ratio is 1:1, the input voltage V_{in} should be the same as the output voltage V_{out} based on the analysis in (3.12).

$$V_{in} = V_{out} \tag{3.13}$$

Due to the identical driving signals for both primary and secondary HV bridges, v_{pri} and v_{sec} should have the same amplitude and phase.

$$v_{pri} = v_{sec} \tag{3.14}$$

As for the current i_T, component $i_{T,I}$ should be equal to 0 at the steady state; otherwise, this current will continue charging or discharging floating DC capacitor C_b. Therefore, the current i_T in the steady state should be equal to $i_{T,II}$. This steady state is a stable equilibrium point. Therefore, no control is needed.

$$\begin{cases} i_{T,I} = 0 \\ i_T = i_{T,II} \end{cases} \tag{3.15}$$

Fig. 3-4 shows the steady state waveforms of EET-DCX with different loads. Since i_T is in the phase of v_{pri} or v_{sec} at the steady state, this current is dedicated to transferring the real power. With different output power P, the amplitude of i_T (i_T=$i_{T,II}$) will be regulated via V_b from (3.8). Since I_{out} is equal to $0.5I_{T,peak}$ as shown in **Fig. 3-4**, the steady-state value of voltage V_b can be derived as

$$V_b = 8 f_s P L_k / V_{in(out)} \tag{3.16}$$

From (3.16), the floating voltage V_b applied on the LV bridge is proportional with f_s, P, L_k, and $1/V_{in(out)}$.

$$V_b \propto f_s,\ P,\ L_k, 1/V_{in(out)} \tag{3.17}$$

With a pre-determined $V_{in(out)}$, P, and f_s, minimization of L_k is very critical because it can reduce the voltage stress on the LV bridge. With lower voltage rating GaN FETs, the LV bridge can be easily embedded into the high-frequency transformer. For example, if $V_{in(out)}$ is 1 kV, P is 10 kW, f_s is 500 kHz, and L_k is 300 nH, the voltage V_b can be derived as only 12 V from (3.16).

To sum up, since v_{pri} is equal to v_{sec} at the steady state, the LV bridge output voltage v_C is directly applied to L_k, which means the voltage drop on L_k is completely canceled by this embedded LV bridge output. Besides keeping the merits of LLC-DCX, such as load-independent voltage gain, EET-DCX does not require resonant point tuning and can always operate optimally at any switching frequency.

3.2.3 Natural Current Sharing of EET-DCX

In order to scale up the rating power, the transformer-level parallel is more desirable than the converter-level parallel because of the higher power density. **Fig. 3-5(a)** depicts the circuit diagrams of the EET-DCX with multiple parallel EETs. After transforming all EET parameters from the secondary side to the primary side, the corresponding equivalent circuits can be simplified, as shown in **Fig. 3-5(b)**. The loop resistances on each EET are $r_{w1\text{-}N}$, which include the winding resistance, ON resistance of the LV bridge GaN FETs, and printed circuit board (PCB) trace stray resistance. All the LV bridges in EETs and two HV bridges are replaced by square voltage sources $v_{C1\text{-}N}$, v_{pri}, and v_{sec}. Based on Kirchoff's voltage law (KVL), the terminal voltage v_{AB} can be given as

$$v_{AB} = \underbrace{jwL_{kN} \cdot i_{TN} + v_{CN}}_{\text{completely cancelled as } 0} + r_{wN} \cdot i_{TN} \quad (N = 1, 2, 3...) \tag{3.18}$$

According to the previous analysis in *Section II Part C*, the voltage drop on $L_{k1\text{-}N}$ will be completely canceled by corresponding voltages $v_{C1\text{-}N}$ in the steady state. Thus, the total voltage drops across each EET transformer can be given as

$$v_{AB} = r_{wN} \cdot i_{TN} \quad (N = 1, 2, 3...) \tag{3.19}$$

From (3.19), the current distribution between each EET can be given as

$$i_{T1} : i_{T2} : \cdots : i_{TN} = \frac{1}{r_{w1}} : \frac{1}{r_{w2}} : \cdots : \frac{1}{r_{wN}} \quad (N = 1, 2, 3...) \tag{3.20}$$

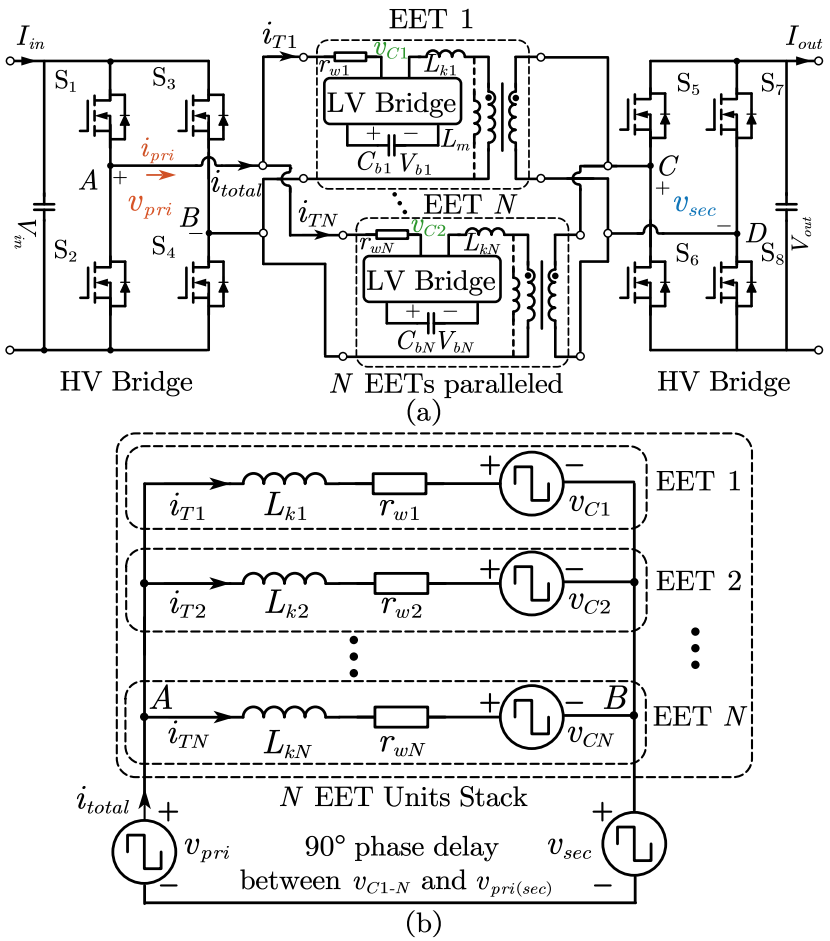


Fig. 3-5. Proposed EET-DCX with multiple transformers paralleled: (a) circuit diagram, (b) simplified equivalent circuit. The equivalent circuit diagram for parallel units was derived from Fig. 3-2.

From (3.20), the current sharing performance of EET-DCX is decoupled from leakage inductances $L_{k1\text{-}N}$ and is only related to the resistances $r_{w1\text{-}N}$. Therefore, EET-DCX will have a natural and stable current sharing performance as the current sharing can always be achieved due to the positive temperature coefficient of resistances. Also, the distribution of $v_{C1\text{-}N}$ can be derived from (3.18), (3.19), and (3.20).

$$v_{C1}:v_{C2}:\ \cdots\ :v_{CN}=\frac{L_{k1}}{r_{w1}}:\frac{L_{k2}}{r_{w2}}:\ \cdots\ :\frac{L_{kN}}{r_{wN}}\quad (N=1,2,3\ldots) \tag{3.21}$$

From (3.21), the floating capacitor dc voltages $V_{b1\text{-}N}$ across $C_{b1\text{-}N}$ are proportional to the leakage inductance $L_{k1\text{-}N}$.

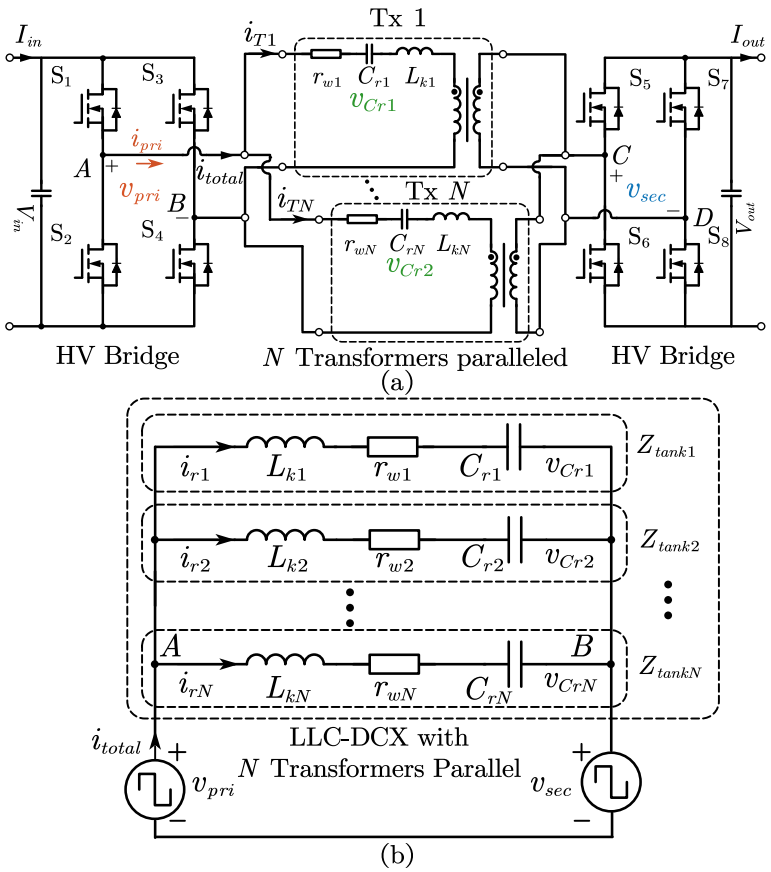


Fig. 3-6. LLC-DCX with multiple transformers paralleled: (a) circuit diagram, (b) simplified equivalent circuit.

It should be noted that if resistances $r_{w1\text{-}N}$ are not considered, the EET-DCX shown in **Fig. 3-5** should have an ideal load-independent voltage gain, which means V_{in} is exactly equal to V_{out}. However, in reality, due to a very small $r_{w1\text{-}N}$, the input voltage V_{in} will be slightly higher than V_{out}. This phenomenon will exist in both EET-DCX and LLC-DCX. However, since the loop resistances $r_{w1\text{-}N}$ are very small, usually on the mΩ level, this voltage drop can be ignored.

Similar to the EET-DCX in **Fig. 3-5**, **Fig. 3-6(a)** and **(b)** depict the circuit diagram and simplified equivalent circuit for LLC-DCX with N transformers paralleled. $i_{r1\text{-}N}$ are the resonant currents through each transformer, and each transformer has its own resonant tank, including resonant capacitor $C_{r1\text{-}N}$ and leakage inductance $L_{k1\text{-}N}$. The impedance of each transformer resonant tank is Z_{tankN} and can be given as

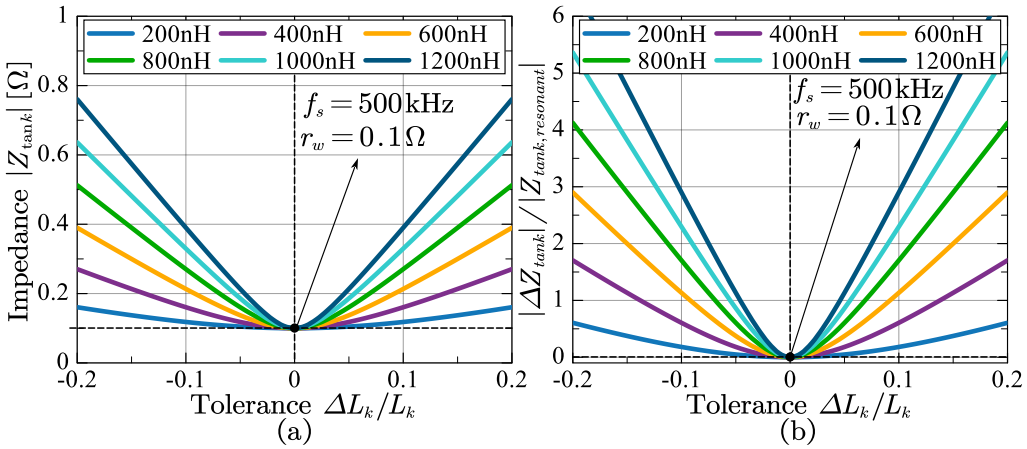


Fig. 3-7. Resonant tank impedance Z_{tank} with a tolerance of L_k:(a) amplitude of Z_{tank} (b) variation of Z_{tank}.

$$Z_{tankN} = R_{wN} + j\omega L_{kN} + 1/(j\omega C_{rN}) \quad (N = 1, 2, 3\ldots) \tag{3.22}$$

From (3.22), the current distribution between each resonant branch can be derived as

$$i_{r1} : i_{r2} : \cdots : i_{rN} = \frac{1}{|Z_{tank1}|} : \frac{1}{|Z_{tank2}|} : \cdots : \frac{1}{|Z_{tankN}|} \quad (N = 1, 2, 3\ldots) \tag{3.23}$$

When all the resonant tanks have the same resonant frequency, the current sharing should be as good as EET-DCX from (3.22) because the voltage drop of $L_{k1\text{-}N}$ will be fully canceled by the resonant capacitor $C_{r1\text{-}N}$. However, if there is a small tolerance on the $C_{r1\text{-}N}$ or $L_{k1\text{-}N}$, the current sharing will deteriorate obviously due to a drastic impedance change on $Z_{tank1\text{-}N}$. For instance, **Fig. 3-7(a)** and **(b)** show the amplitude and variation of Z_{tank} with a tolerance of L_k, respectively. With a fixed switching frequency f_s=500 kHz, the leakage inductance L_k was swept from 200 to 800 nH with a tolerance from -20 % to +20 %. With zero tolerance, the resonant frequency f_r is also set to 500 kHz. Thus, the resonant capacitor C_r can be calculated from (3.1). The loop resistance r_w is assumed to have a typical value of 100 mΩ. If there is no tolerance on L_k, the total impedance Z_{tank} should be equal to r_w as 100 mΩ. However, if there is a tolerance on L_k, the impedance of Z_{tank} will increase dramatically. When L_k is equal to 600 nH and the tolerance is ±10%, the impedance

variation of Z_{tank} will exceed 110%. Due to this large variation, the current sharing performance of LLC-DCX will deteriorate.

To visualize this poor current sharing performance, a simulation was implemented for the comparison between LLC-DCX and the proposed EET-DCX. The current sharing simulation for both EET-DCX and LLC-DCX are depicted in **Fig. 3-8** and **Fig. 3-9**, respectively. For both EET-DCX and LLC-DCX, four transformers are paralleled to simulate the current sharing performance. The simulation parameters are listed in **Table 3-1**. Without the consideration of tolerance, the values of L_k and r_w are set as 600 nH and 100 mΩ.

Following the simplified equivalent circuit of EET-DCX shown in **Fig. 3-5(a)**, the currents through four EETs are $i_{T1\text{-}4}$, and the LV bridge output voltages are $v_{C1\text{-}4}$. As shown in **Fig. 3-8**, before adding tolerance, the current sharing is good, and the amplitudes of $v_{C1\text{-}4}$ are all equal to 35.5 V from (3.16). After about 0.5 μs, +5%, +10%, and +20% tolerances were added to L_{k2}, L_{k3}, and L_{k4}, respectively. At the beginning of the tolerances introduction, currents $i_{T1(234)}$ through 4 EETs will have a small difference because of the circuit transients. Based on the previous analysis, each EET can fully compensate for these tolerances by regulating the amplitudes of $v_{C1(234)}$ automatically. When the EET-DCX enters the steady state again, all the currents $i_{T1\text{-}4}$ overlap again, which means the natural current-sharing mechanism has been verified. With different tolerances on L_k (L_{k1}=L_k, L_{k2}=1.05L_k, L_{k3}=1.1L_k, L_{k4}=1.2L_k), the amplitudes of $v_{C1\text{-}4}$ will regulate automatically to cancel the impedances of $L_{k1\text{-}4}$ from (3.16).

Table 3-1 THE PARAMETERS OF THREE PROTOTYPES

Variable	Value	Variable	Value
Input voltage V_{in}	300 V	Output voltage V_{out}	300 V
Parallel number N	4	Loop resistance r_w	100 mΩ
Rating power P	18 kW	Switching frequency f_s	500 kHz
Leakage inductance L_k	600 nH	Resonant capacitance C_r	168 nF

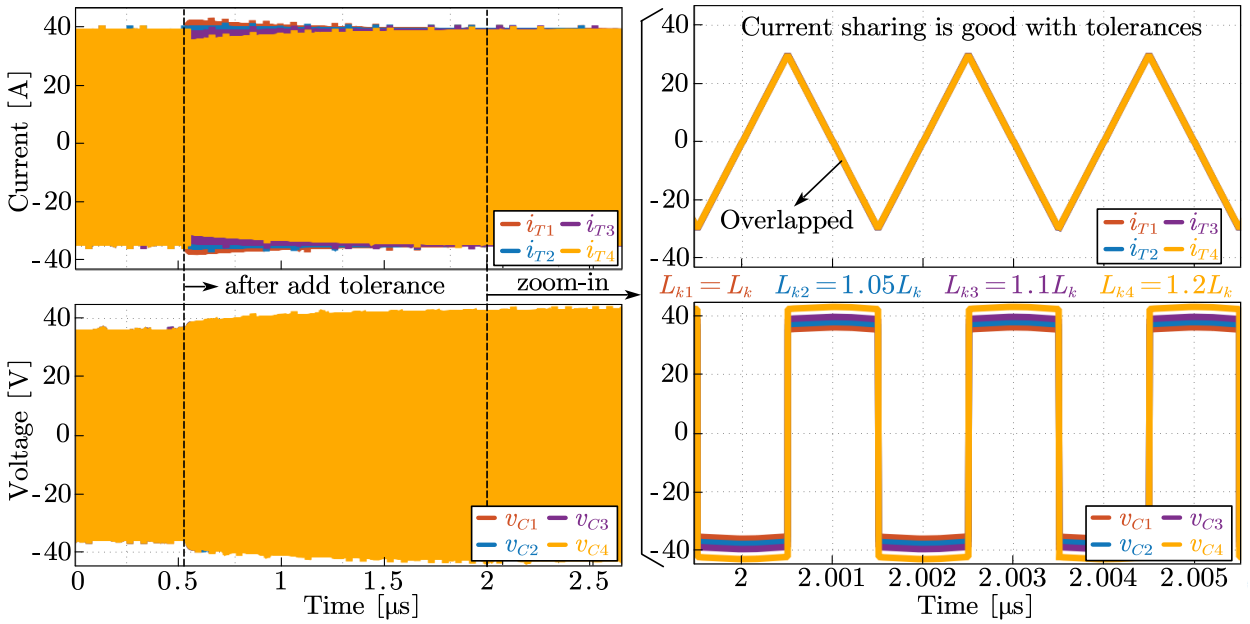


Fig. 3-8. Simulated currents and voltages of the proposed EET-DCX.

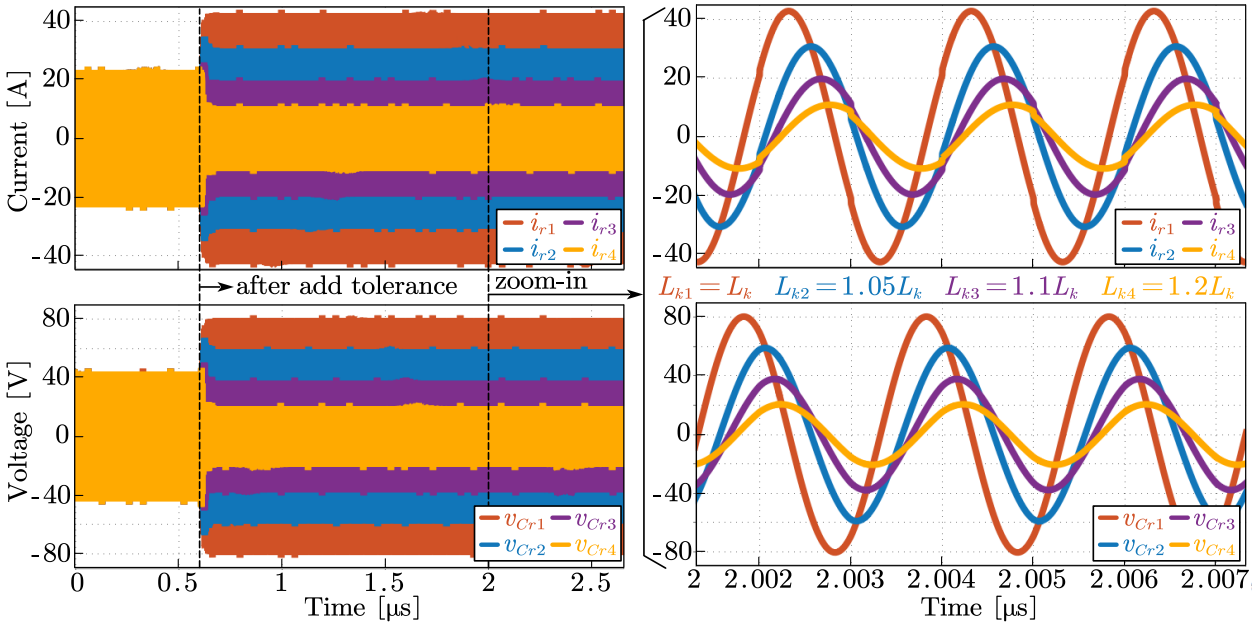


Fig. 3-9. Simulated currents and voltages of the LLC-DCX. The corresponding parameters can be found in Table 3-1.

As for the LLC-DCX with four parallel transformers, the current sharing simulation is depicted in **Fig. 3-9**. Suppose there are some tolerances on the leakage inductances $L_{k1\text{-}4}$. Following the EET-DCX equivalent circuits shown in **Fig. 3-6(b)**, the simulated transformer resonant currents $i_{r1\text{-}4}$ and resonant capacitance voltages $v_{Cr1\text{-}4}$ are depicted. The simulated parameters also can be found in **Table 3-1**. All simulated parameters, such as the input voltage V_{in}, output voltage V_{out}, rating power P, leakage inductance L_k, switching frequency f_s, and loop resistance r_w, remain the same as the EET-DCX simulation shown in **Fig. 3-8**.

Based on the analysis in **Fig. 3-7**, the current sharing performance of LLC-DCX is very sensitive to resonant tank parameters. Same as the EET-DCX, after around 0.6 μs, +5%, +10%, and +20% tolerances were added to L_{k2}, L_{k3}, and L_{k4}, respectively. As shown in **Fig. 3-9**, after adding the tolerance, current sharing becomes poor because the resonant tank impedance will increase drastically even with a very small tolerance of L_k. Most of the current will go through L_{k1} because that branch has the lowest impedance. In addition, since the resonant point shifts away with these tolerances, the phases of $i_{r1\text{-}4}$ are also different from each other.

3.2.4 Soft Switching Analysis of EET-DCX

To simplify the operation principle of EET-DCX, magnetizing inductance and deadtime are neglected in the previous analysis. In this section, detailed soft switching analysis for both HV and LV bridges will be provided.

With the consideration of HV bridges' output capacitances $C_{oss,pri}$, and $C_{oss,sec}$ on both sides, **Fig. 3-10** redraws the circuit diagram of EET-DCX. The circuit diagram of the LV bridge is simplified first and will be explained later. Similar to LLC-DCX, the ZVS for HV bridges of EET-DCX relies on the magnetizing inductance L_m from (3.3). L_m can provide a circulating magnetizing current i_m to charge and discharge the total output capacitance $C_{oss,total}$ during the deadtime t_d. With a 1:1 turns ratio, the $C_{oss,total}$ in (3.3) can be derived as

$$C_{oss,total} = C_{oss,pri} + C_{oss,sec} \tag{3.24}$$

Fig. 3-11 shows the ZVS simulation for HV bridges of EET-DCX, and all the parameters are listed in **Table 3-2**. The input voltage V_{in} and the output voltage V_{out} are both 400 V, and the rating power is 12 kW. The transformer leakage inductance L_k is 1460 nH, and the magnetizing inductance L_m is 25 μH. With a determined L_m, deadtime t_d can be derived from (3.3). After considering i_m, the relationship between i_{pri}, i_{sec}, and i_m can be given as

$$i_m = i_{pri} - i_{sec} \tag{3.25}$$

As shown in **Fig. 3-11**, before the switches $S_{23(67)}$ turn on, both $v_{ds,pri}$ and $v_{ds,sec}$ have fallen down to zero, which means the ZVS for HV bridges is obtained.

Table 3-2 ZVS SIMULATION PARAMETERS OF EET-DCX

Variable	Value	Variable	Value
Input voltage V_{in}	300 V	Output voltage V_{out}	300 V
Parallel number N	4	Loop resistance r_w	100 mΩ
Rating power P	18 kW	Switching frequency f_s	500 kHz
Leakage inductance L_k	600 nH	Resonant capacitance C_r	168 nF

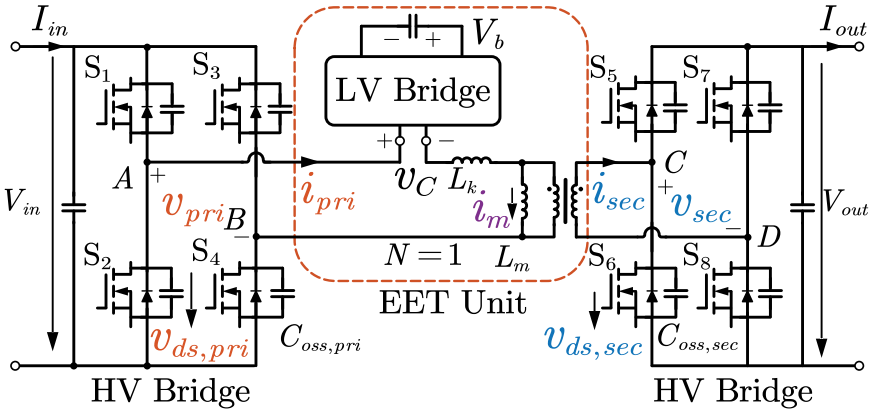


Fig. 3-10. Equivalent circuit of EET-DCX with the consideration of semiconductor output capacitance. The original simplified equivalent circuit can be found in Fig. 3-2.

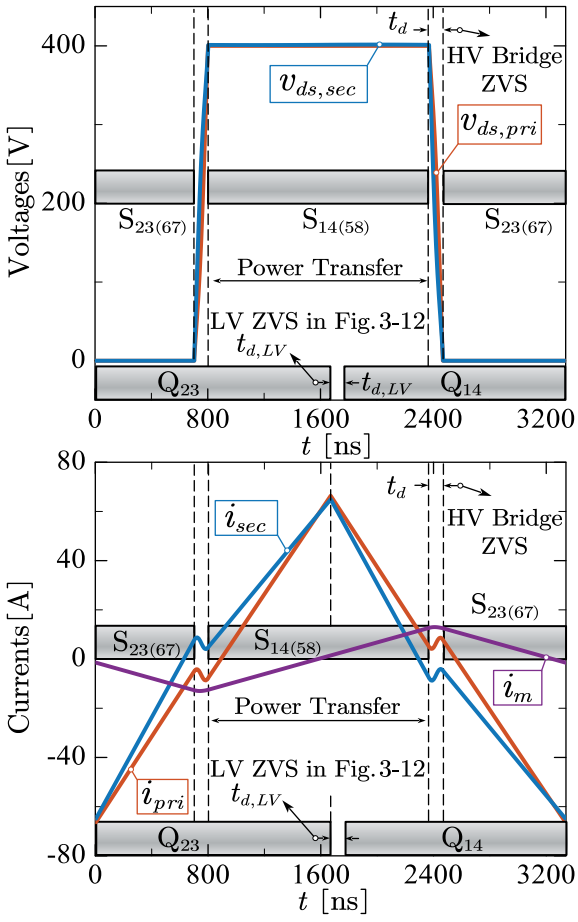


Fig. 3-11. Simulated currents and voltages of the LLC-DCX. The parameters are listed in Table 3-2.

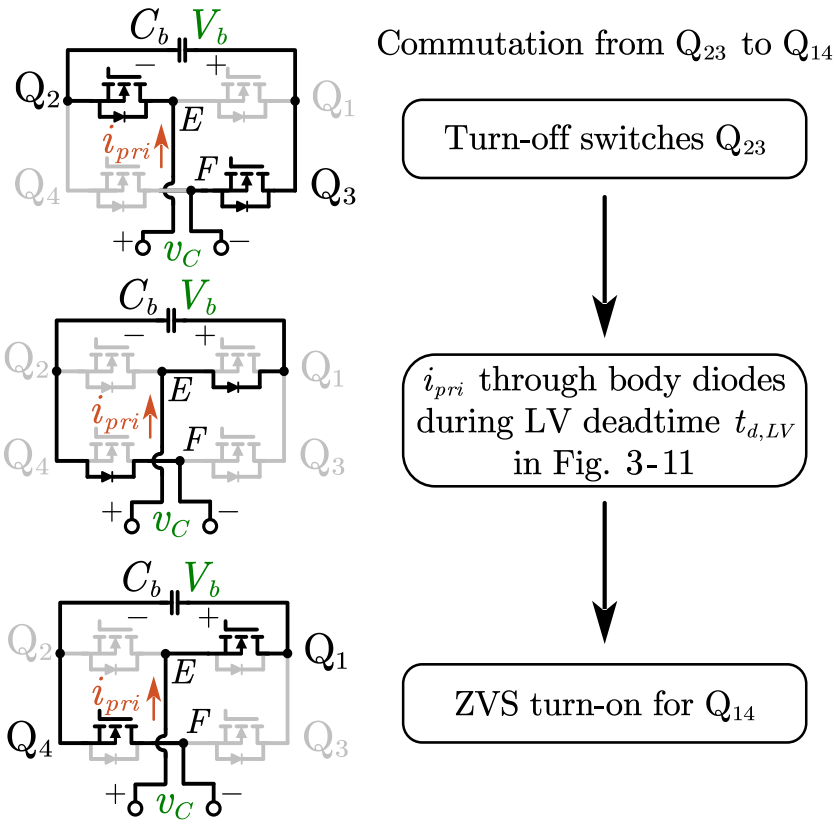


Fig. 3-12. ZVS analysis for LV bridge of EET-DCX. The current will go through the body diodes during the deadtime, as shown in Fig. 3-11.

For a simple ZVS explanation of HV bridges, the LV bridge part was simplified in **Fig. 3-10**. To illustrate the ZVS mechanism of the LV bridge, the detailed equivalent circuits of the LV bridge are plotted in **Fig. 3-12**. The corresponding driving signals $Q_{1\text{-}4}$ and the current waveform i_{pri} can be found in **Fig. 3-11**.

Since the LV driving signals $Q_{1\text{-}4}$ have a 90-degree delay with HV bridges driving signals $S_{1\text{-}4(5\text{-}8)}$, the current i_{pri} will reach its peak value when the LV bridge switches $Q_{1\text{-}4}$ turn on/off. Therefore, during the switch transition of the LV bridge, the polarity of i_{pri} will not change. For example, as shown in **Fig. 3-11**, for the commutation from Q_{23} to Q_{14}, i_{pri} will keep as positive during a very short deadtime $t_{d,LV}$. Before switches Q_{23} turn off, the current i_{pri} will go through the channels of Q_{23}, as shown in **Fig. 3-12**. When switches Q_{23} turn off, positive current i_{pri} will go through the

body diodes of Q_{14}. Similar to the synchronous rectification (SR), after i_{pri} goes through the body diodes of Q_{23}, natural ZVS can be obtained by turning on switches Q_{14}. The same ZVS analysis can be applied to switches Q_{23} in another half period, which means all switches of the LV bridge can achieve the natural ZVS similar to SR operation.

As shown in **Fig. 3-11**, during the LV bridge dead time $t_{d,LV}$, current i_{pri} keeps as the peak value, and the voltage V_b across the LV bridge is very small with a minimized L_k from (3.16). Therefore, the output capacitance of LV bridge switches can be ignored. Moreover, the dead time $t_{d,LV}$ for LV bridge can be optimized and shortened to reduce the dead time conduction loss.

As shown in **Fig. 3-11** and **Fig. 3-12**, the triangular current i_{pri} will charge and discharge the dc capacitance C_b alternately; the ripple $\Delta V_b/V_b$ on C_b can be derived from (3.15).

$$\Delta V_b/V_b = 1/(32 f_s^2 C_b L_k) \tag{3.26}$$

To meet the voltage ripple requirement, the capacitance value of C_b can be selected from (3.26).

In order to achieve the transformer-level parallel and scale up the total power, **Fig. 3-13** shows a scalable and modular design of EET-DCX with two split external inductances, L_{pri} and L_{sec}, on the primary and secondary sides, respectively. If there are N EETs stacked in parallel, the magnetizing current should be equally provided by each EET unit, which means the design of L_m is dependent on the total unit number N. If the demand of the total power increases, more EETs will be stacked. Therefore, the magnetizing inductance L_m in each EET unit should be redesigned according to the updated total parallel number. However, this is not desirable for a modular and scalable design because the transformer airgap design is related to the number of paralleled EETs.

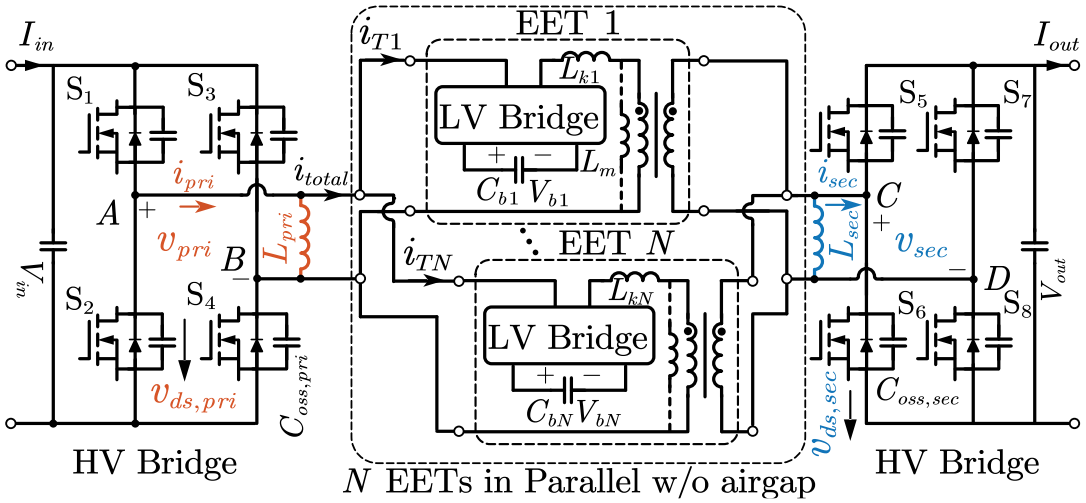


Fig. 3-13. Scalable and modular ZVS design with two split external inductances. The multiple-units parallel diagram can be modified by the unit diagram shown in Fig. 3-10.

As shown in **Fig. 3-13**, with the help of L_{pri} and L_{sec}, both primary and secondary side HV bridges can realize the ZVS without the air gap and the corresponding L_m. The current through each EET $i_{T1\text{-}N}$ can be dedicated to transferring the real power. From (3.3), the value of L_{pri} and L_{sec} can be given as

$$L_{pri(sec)} = t_d / (2 f_s C_{oss,pri(sec)}) \tag{3.27}$$

As for each modular EET unit design, the air gap of the transformer can be eliminated, and L_m for each EET unit will be much larger than L_{pri} or L_{sec}. With different parallel numbers N, the values of L_{pri} and L_{sec} are both fixed since they are dedicated to realizing the HV bridges ZVS. Although two extra inductances, L_{pri} and L_{sec}, are required, a modular EET design can be achieved, and the current through each EET can be reduced.

3.2.5 Hardware Implementation and Verification

Two 12 kW EET-DCX prototypes were built in this section. The first prototype, *EET-DCX I*, has only one EET unit and was used to verify the basic operation principle and ZVS analysis. To verify the natural current-sharing performance, optimal operation at any frequency, and load-independent voltage gain, another modular prototype, EET-DCX II, was built with four paralleled EET units. This section will mainly focus on the *EET-DCX II* with a modular design because more details of *EET-DCX I* can be found in the authors' previous conference paper [30].

1) *EET-DCX I* with One EET Unit

Fig. 3-14(a)-(c) shows the experimental results of EET-DCX I under 12 kW, 8 kW, and 4 kW. The parameters of *EET-DCX I* are listed in **Table 3-3**. Following the circuit diagram in **Fig. 3-10**, the gate signal $v_{gs,S2}$, drain-source voltages $v_{ds,pri(sec)}$, transformer currents $i_{pri(sec)}$, and i_m are all measured. As shown in **Fig. 3-14**, before $v_{gs,S2}$ turns on, both $v_{ds,pri(sec)}$ have dropped to zero, which means ZVS has been achieved on both sides. When the *EET-DCX I* operates under different power from 4 kW to 12 kW, i_{pri} and i_{sec} are both triangular waveforms in phase of the drain-source voltages $v_{ds,pri}$ and $v_{ds,sec}$. Among these three cases, only the amplitudes of currents $i_{pri(sec)}$ are different because larger $i_{pri(sec)}$ can transfer more real power under heavy load, which can verify the analysis in **Fig. 3-4**.

As for the magnetizing current i_m, which is dedicated to realizing ZVS, it keeps constant in the full load range. The design requirement for magnetizing inductance L_m is the same as LLC-DCX. Based on the experimental results of *EET-DCX I* in **Fig. 3-14**, the ZVS analysis in the last section can be verified.

Table 3-3 THE PARAMETERS OF *EET-DCX I* WITH ONE EET UNIT

Variable	Value	Variable	Value
$V_{in(out)}$	400 V	C_b	20 µF
P	12 kW	f_s	300 kHz
L_k	1450 nH	L_m	18 µH
$C_{oss,pri(sec)}$	418 pF × 2	$C_{oss,LV}$	1790 pF
HV Bridge	C3M0016120k × 2	LV Switch	EPC 2021

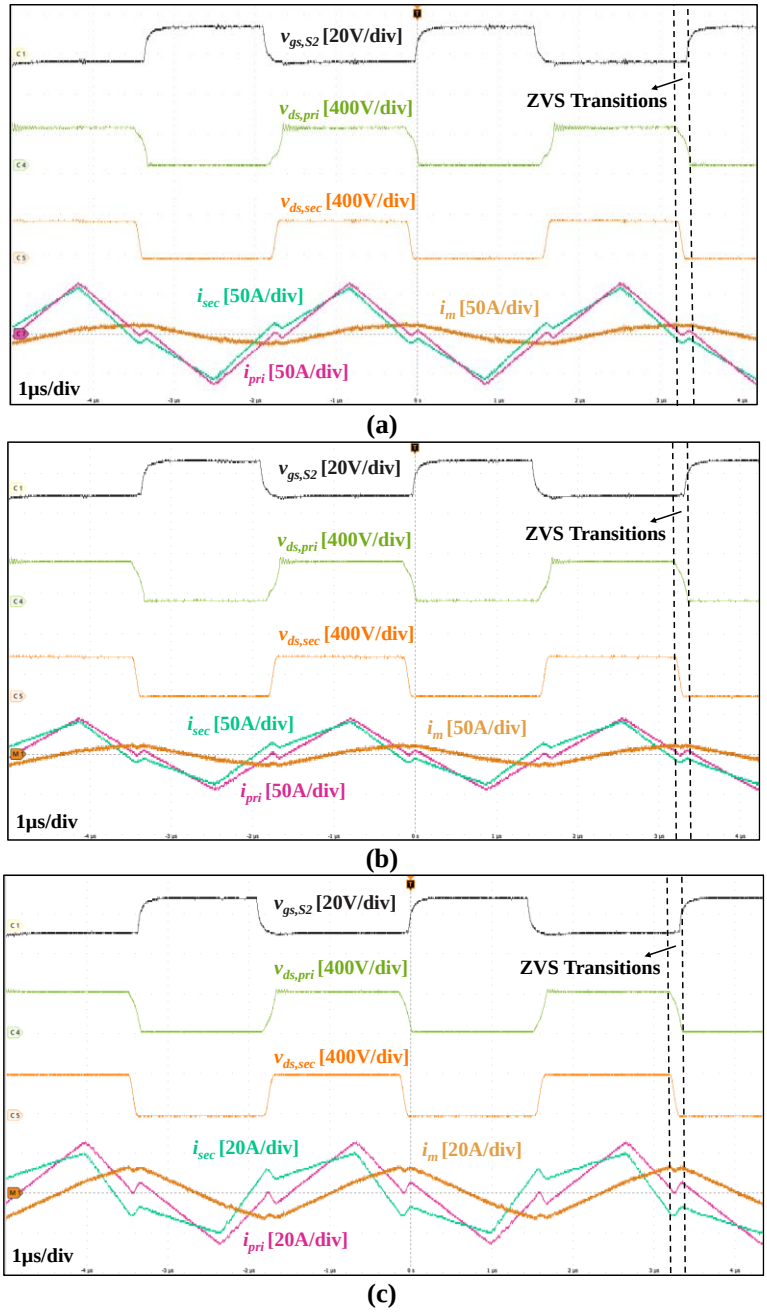


Fig. 3-14. The 300 kHz experimental results of *EET-DCX I* with only one EET unit: (a) 12 kW, (b) 8 kW, (c) 4 kW. The corresponding circuit parameters can be found in Table 3-3.

2) *EET-DCX II* with Four EET Unit

To verify the current sharing performance with multiple paralleled EETs, a 12 kW 500 kHz *EET-DCX II* was built with four EET units, as shown in **Fig. 3-15**. The corresponding parameters of this prototype can be found in

Table 3-4. As shown in **Fig. 3-15(a)**, the whole EET-DCX includes two HV bridges and four paralleled EET units. **Fig. 3-15(b)** shows the detailed hardware design of each modular EET unit. The LV bridge with GaN FETs and drivers has been integrated into the PCB-based windings. V_{in} and V_{out} are both 300 V, and the output rating power is 12 kW, which means each modular EET will handle 3 kW. Due to f_s=500 kHz, high-frequency material *DMR51* from *DMEGC* was selected. To shorten the winding trace and reduce the winding loss, low-profile "ER" core *ECW64A18* was selected, as shown in **Fig. 3-15(b)**. From (3.16) and (3.17), L_k should be minimized to reduce the voltage V_b across the LV bridge. Therefore, PCB winding and interleaving techniques have been adopted. After shorting the secondary terminals of the EET unit and measuring the primary terminals, parasitic parameters L_k and winding resistance r_w can be obtained as 172 nH and 125 mΩ, respectively. The sweep measurement results from the impedance analyzer can be found in **Fig. 3-16**. Following the modular design, as shown in **Fig. 3-13**, external inductances $L_{pri(sec)}$ are adopted to provide circulating current, and no air gap is required for each EET unit. As for the current measurement, the Rogowski coil current probe was adopted. **Fig. 3-17(a)** first shows the current sharing results with only two EET units plugged in, which means the total power is 6 kW (3 kW for each EET unit). Following the annotations in **Fig. 3-13**, $i_{T1\text{-}4}$ are currents through each EET unit and i_{total} is the sum of these four currents.

$$i_{total} = i_{T1} + i_{T2} + i_{T3} + i_{T4} \tag{3.28}$$

Table 3-4 THE PARAMETERS OF *EET-DCX II* WITH FOUR EET UNIT

Variable	Value	Variable	Value
$V_{in(out)}$	300 V	C_b	20 µF
P	12 kW	f_s	500 kHz
L_k	172 nH	$L_{pri(sec)}$	15 µH
ER Core	ECW64A18	Core Material	DMR51
$C_{oss,pri(sec)}$	418 pF × 2	$C_{oss,LV}$	1310 pF
HV Bridge	C3M0016120k × 2	LV Switch	EPC 2029

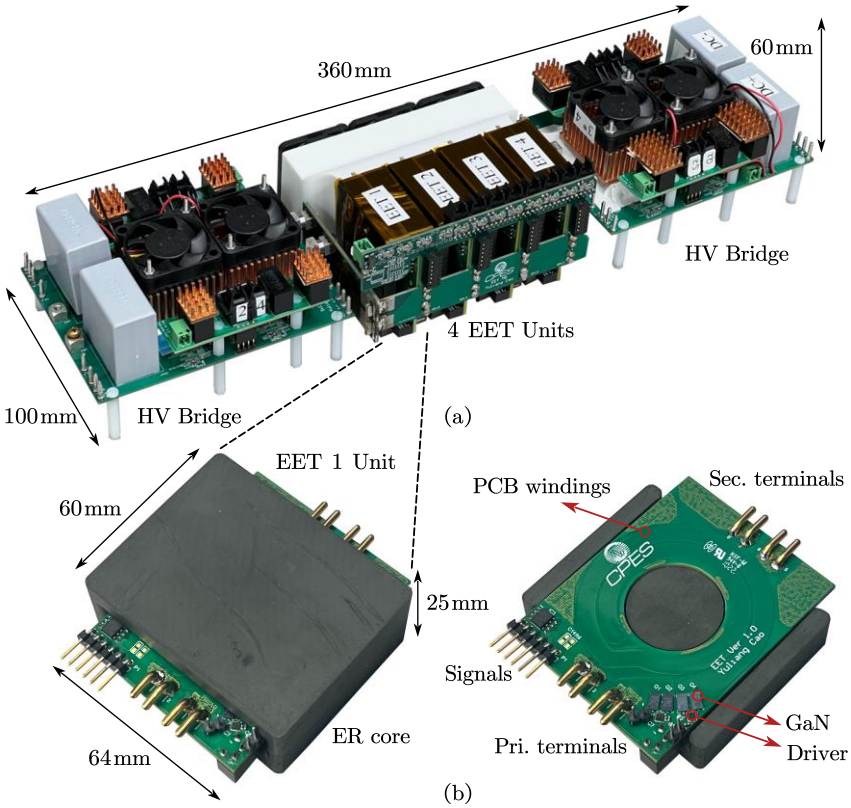


Fig. 3-15. A 12 kW 500 kHz *EET-DCX II* prototype with four EET units plugged in: (a) whole converter, (b) details of each 3 kW EET unit. The corresponding circuit parameters can be found in

Table 3-4**.**

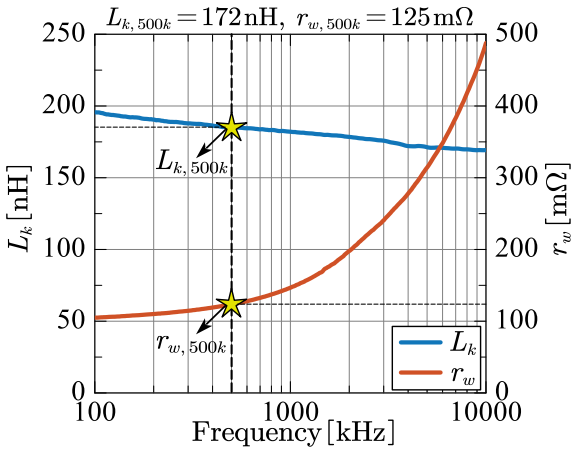
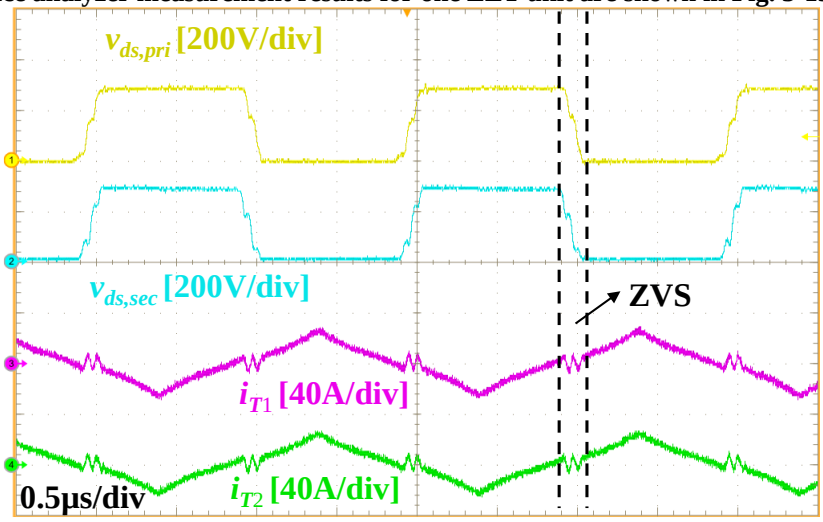
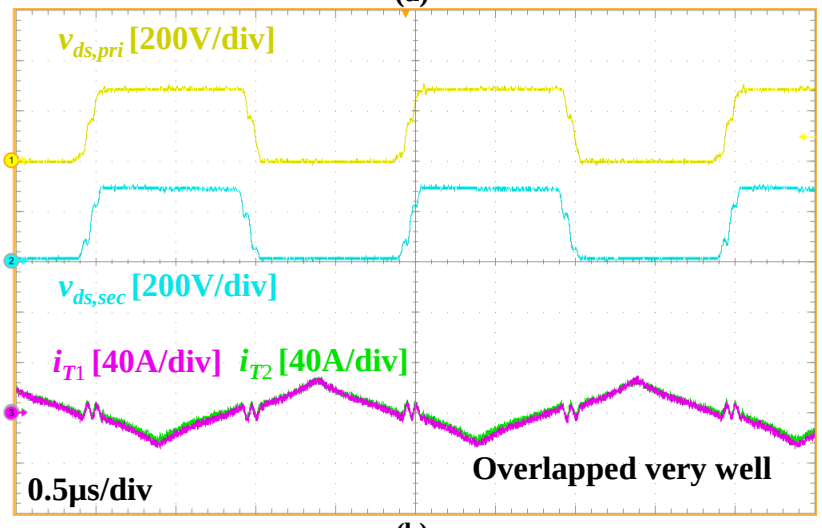


Fig. 3-16. Impedance analyzer measurement results for one EET unit are shown in Fig. 3-15(b).



(a)

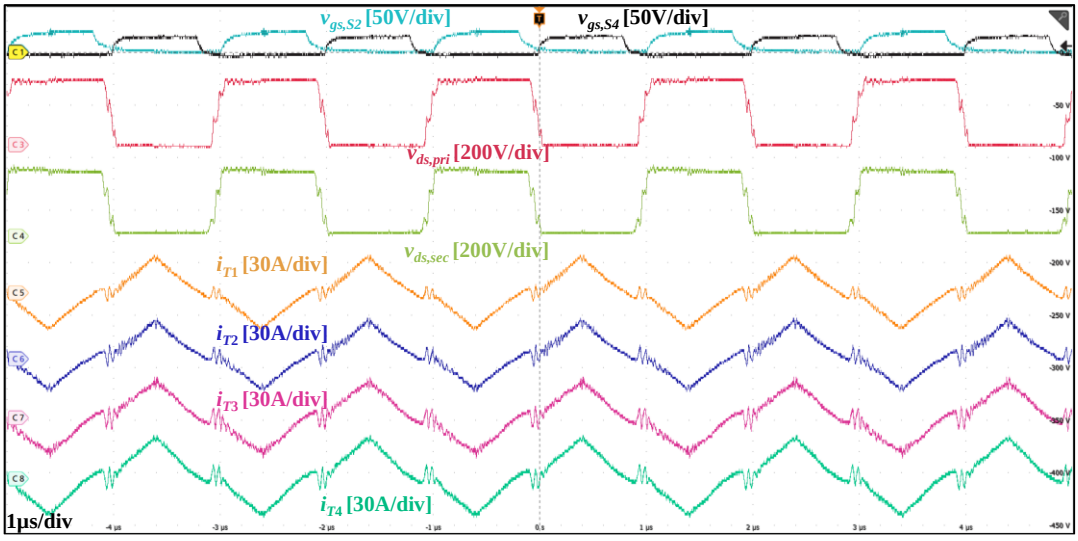


(b)

Fig. 3-17. The 6 kW 500 kHz experimental results for *EET-DCX II* with only two EET units paralleled: (a) currents stacked, (b) currents overlapped. The corresponding circuit parameters can be found in

Table 3-4.

As shown in **Fig. 3-18(b)**, currents i_{T1} and i_{T2} overlapped very well, indicating a good current sharing. **Fig. 3-18(a)** shows the 12 kW 500 kHz experimental results of *EET-DCX II* with all four EET units plugged in. Similarly, the current sharing performance among $i_{T1\text{-}4}$ remains ideal because these four currents overlap well, as shown in **Fig. 3-18(b)**. In addition, ZVS during the dead time can also be verified because both side's drain-source voltages, $v_{ds,pri}$, and $v_{ds,sec}$, are dropped to zero before gate signals turn on.



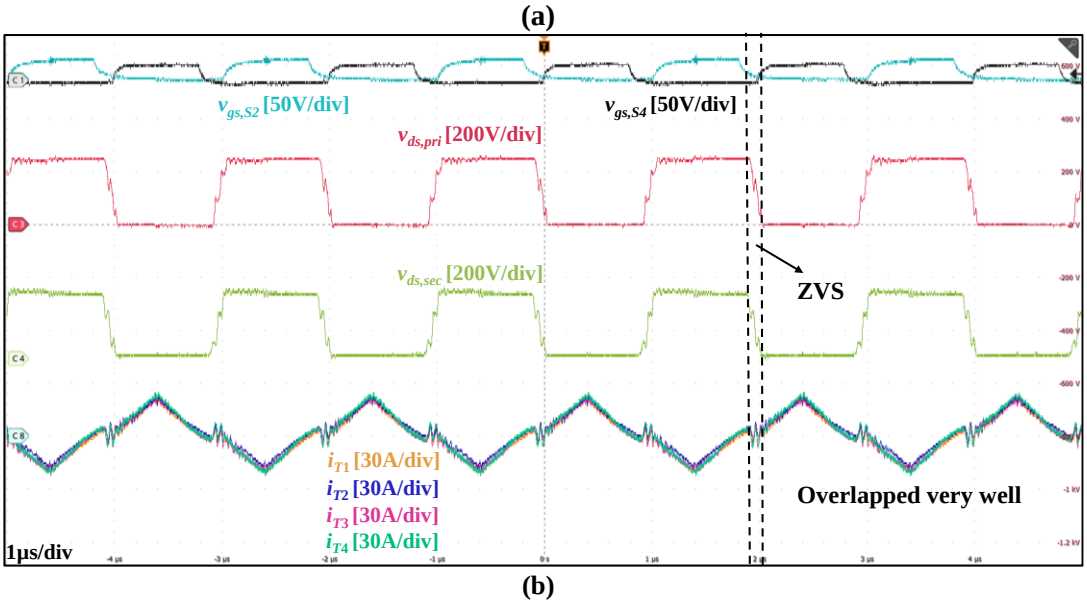
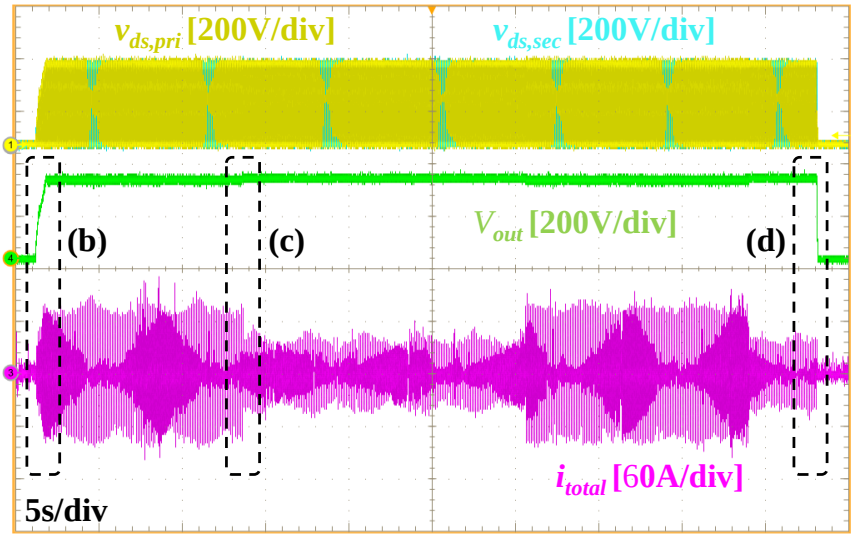


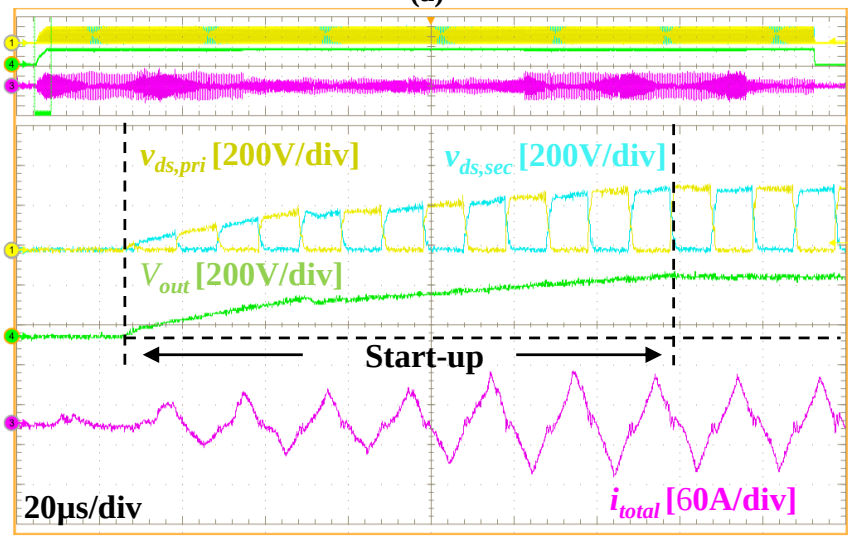
Fig. 3-18. The 12 kW 500 kHz experimental results of *EET-DCX II* with four EET units paralleled: (a) currents stacked, (b) currents overlapped. The corresponding circuit parameters can be found in

Table 3-4.

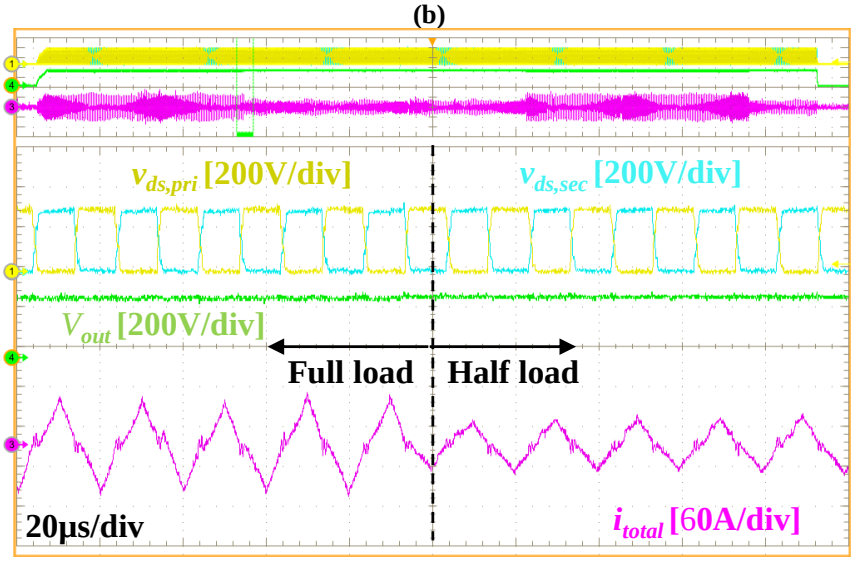
Fig. 3-19(a) depicts a whole dynamic experimental result including start-up, load changing, and shutdown. As for the startup of *EET-DCX II* in **Fig. 3-19(b)**, the total current i_{total} keeps increasing when V_{out} increases from 0 to 300 V. The detailed waveforms are shown in **Fig. 3-19(c)** when the load suddenly jumps from 12 kW (full power) to 6 kW (half load), the amplitude of i_{total} will also decrease to half. Finally, the shutdown is shown in **Fig. 3-19(d)**.


$v_{ds,pri}$ [200V/div]
$v_{ds,sec}$ [200V/div]
(b)
(c)
V_{out} [200V/div]
(d)
i_{total} [60A/div]
5s/div

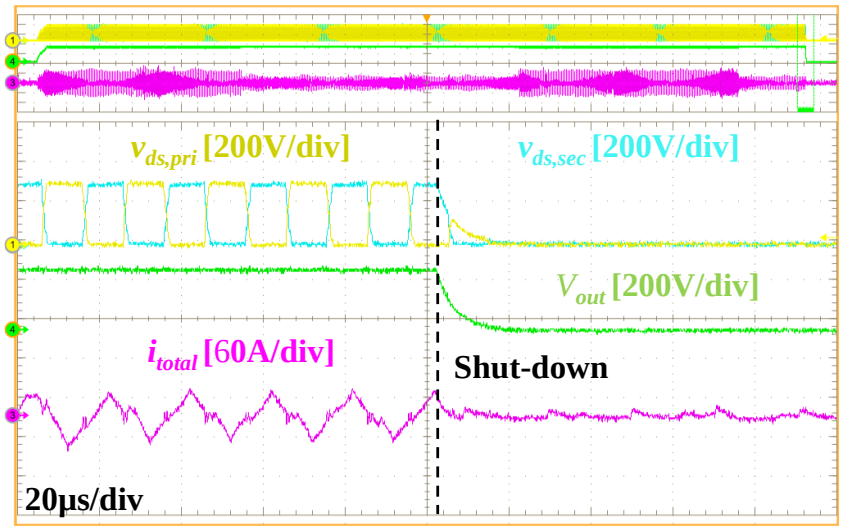
(a)


$v_{ds,pri}$ [200V/div]
$v_{ds,sec}$ [200V/div]
V_{out} [200V/div]
Start-up
i_{total} [60A/div]
20µs/div

(b)


$v_{ds,pri}$ [200V/div]
$v_{ds,sec}$ [200V/div]
V_{out} [200V/div]
Full load
Half load
i_{total} [60A/div]
20µs/div

(c)



(d)

Fig. 3-19. Dynamic experimental results for *EET-DCX II*: (a) whole procedure, (b) start-up, (c) load changing from 12 kW full load to half load 6 kW, (d) shut down. The corresponding circuit parameters can be found in

Table 3-4.

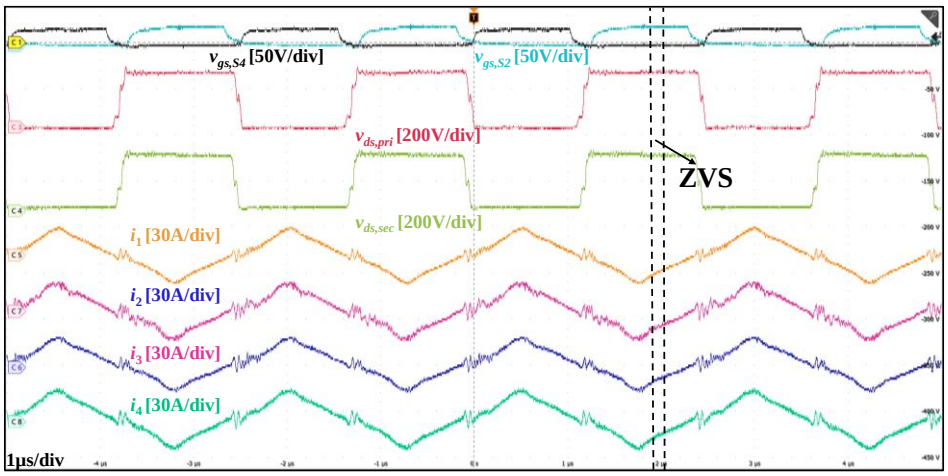


Fig. 3-20. Experimental results of 12 kW EET-DCX with 400 kHz. The corresponding circuit parameters can be found in

Table 3-4.

When the input side turns off, the output voltage V_{out} drops from 300 to 0 V. From this dynamic experimental result, the load-independent voltage gain can also be verified because V_{out} keeps constant at 300 V when the load changes from 12 kW to 6 kW or changes back.

Moreover, to verify that EET-DCX can work at any frequency optimally, the switching frequency f_s has been changed from 500 kHz to 400 kHz, as shown in **Fig. 3-20**. Compared with the 500 kHz results in **Fig. 3-18**, only f_s is different. As shown in **Fig. 3-20**, the triangular currents $i_{T1\text{-}4}$ have a good current sharing and keep in phase of the voltages $v_{pri(sec)}$.

3) Robust Current Sharing Verification

To verify the robustness of the open-loop natural current sharing performance of the *EET-DCX II*, an extra air core inductance was implemented to generate some tolerance on leakage inductance L_k. As shown in **Fig. 3-21**, an extra air core inductor was connected in series to the terminal of the "*EET 1*" unit. All four EET unit currents $i_{T1\text{-}4}$ are measured by Rogowski coil probes. The inductance L_{air} and resistance r_{air} of this air core inductor were both measured by an impedance analyzer and can be found in **Fig. 3-22**. At 500 kHz, L_{air} is 211 nH, and the resistance r_{air} is 7.3 m**Ω**. Compared with the EET unit's inherent L_k=172 nH shown in **Fig. 3-16**, around 122% tolerance was introduced to the "*EET 1*" unit. After a series with this air core inductance, **Fig. 3-23** shows the 500 kHz, 12 kW experimental results with four EET units paralleled again. Even though with a 122% tolerance, the ideal current sharing performance is still retained. As mentioned before, the proposed EET-DCX will automatically cancel the impedance of L_k by regulating the voltage across the LV bridge. Since the LV bridge has been embedded in the EET unit and completely covered by the ER core, as shown in **Fig. 3-15(b)**, it's very difficult to measure the LV output voltage v_C or DC voltage V_b. However, according to the current waveforms $i_{T1\text{-}4}$ and measured L_k, voltage V_b across the LV bridge can be derived from (3.16). Based on the parameters in

Table 3-4, V_b is about 10 V.

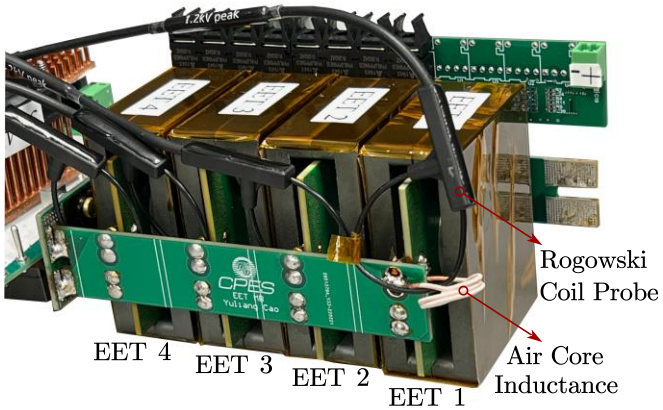


Fig. 3-21. The setup for robustness current sharing test for *EET-DCX II*. An extra air core inductance was adopted to add a tolerance of over 100%.

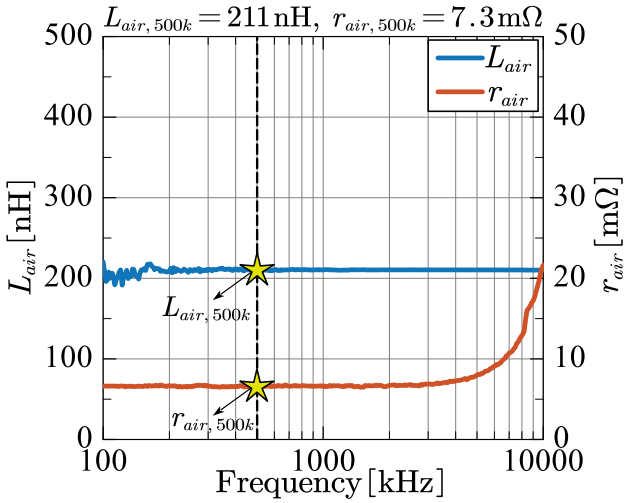
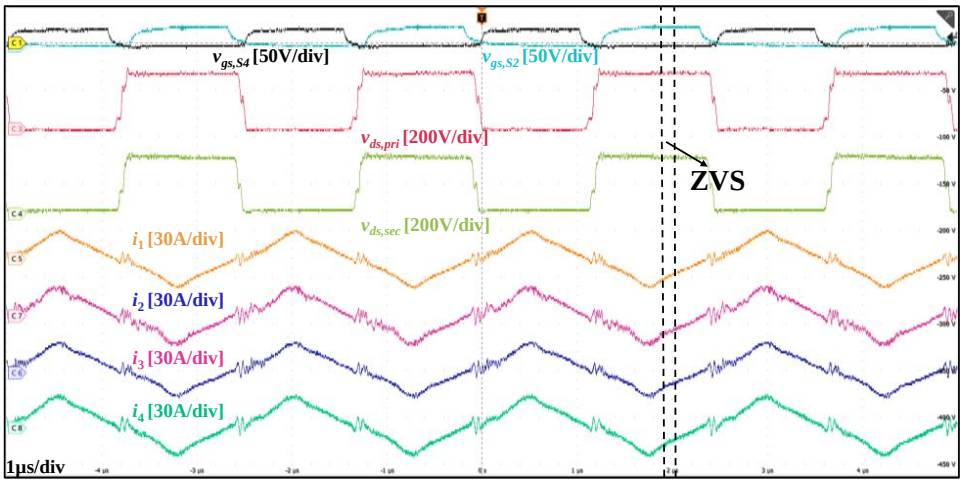
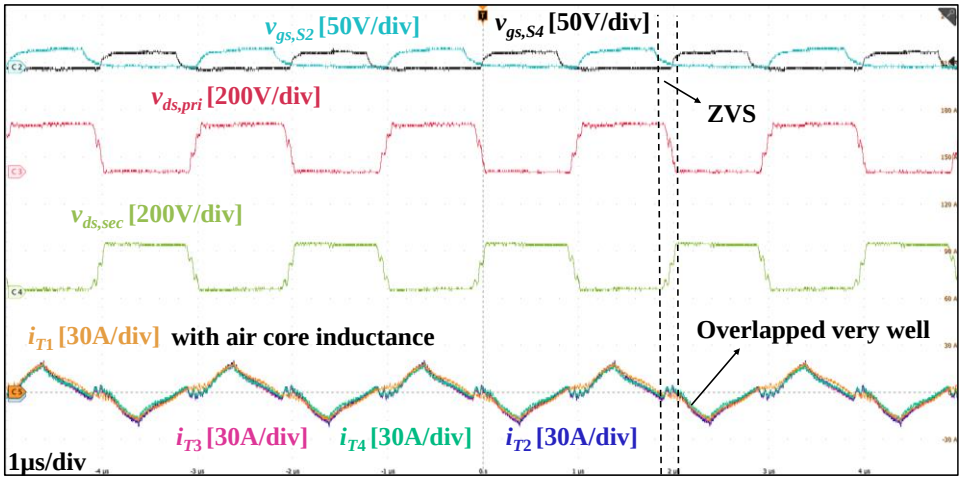


Fig. 3-22. Impedance analyzer measurement results for the air core inductance. The prototype with air core inductance can be found in Fig. 3-21.



(a)



(b)

Fig. 3-23. The 12 kW 500 kHz experimental results of *EET-DCX II* after adding air core inductance to EET 1 unit: (a) currents stacked, (b) currents overlapped.

4) Thermal Performance and Efficiency

Benefiting from the good current sharing performance, the modular cooling system can be designed for each EET unit. Each EET unit will have its own airflow (21.5 CFM). The thermal simulation results, including surface temperature and cross-section temperature, are depicted in **Fig. 3-24**. The hot spot will not exceed 60 ºC and will exist at the further side of the fan. Afterward, the region close to the LV bridge will be about ten ºC higher than other regions. Under 12 kW and 500 kHz, the thermal results of *EET-DCX II* with four EET units are shown in **Fig. 3-25**. The highest temperature from the thermal camera will not exceed 45 ºC. Finally, **Fig. 3-26** shows the measured efficiency of *EET-DCX II* with different output power.

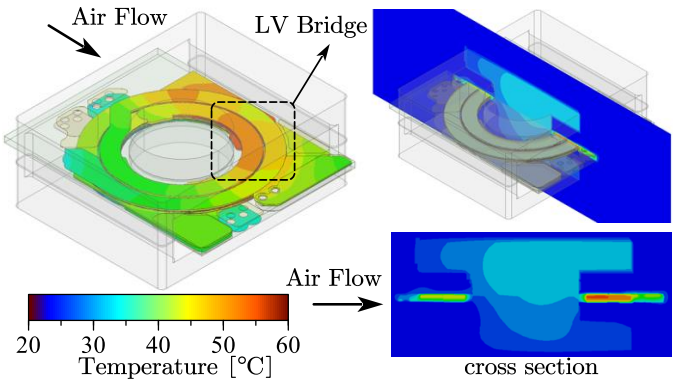


Fig. 3-24. Thermal simulation for each modular EET unit.

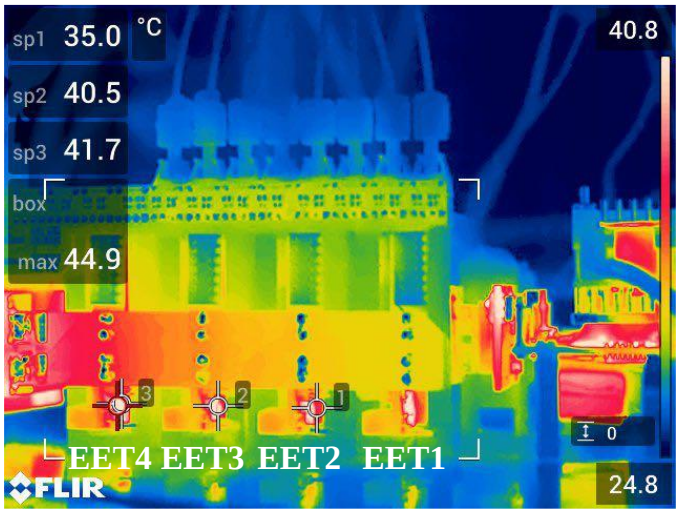


Fig. 3-25. Thermal results of *EET-DCX II* under 12 kW 500 kHz with four EET units paralleled.

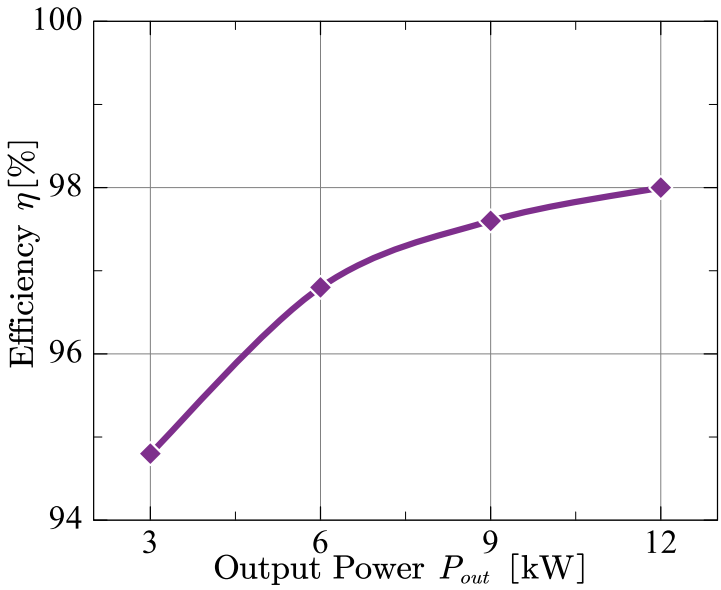


Fig. 3-26. The measured efficiency of *EET-DCX II* with different output power. The prototype can be found in Fig. 3-15.

3.3 Trapezoidal Current Modulation

In the last section, by incorporating an integrated low-voltage full bridge, the concept of an electronic-embedded transformer (EET) offers a straightforward means of achieving high-frequency, high-power fixed-gain isolated DC-DC conversion, known as a DC transformer (DCX) through parallel operation of EET units with natural current sharing. However, EET-DCX, characterized by triangular transformer current, exhibits a higher root mean square (rms) value compared to the sinusoidal current in LLC/CLLC-DCX. To address this limitation, this section proposes a trapezoidal current modulation technique for EET-DCX.

3.3.1 Operation Principle

The configuration of EET-DCX in **Fig. 3-2** comprises two HV bridges and one LV bridge integrated within a n:1 transformer. The diagram showcases various key elements: V_{in} and V_{out} denote the input and output voltages, while I_{in} and I_{out} represent the input and output currents, respectively. Additionally, v_{pri} and v_{sec} correspond to the output voltages of the two HV bridges. The floating DC voltage across C_b is denoted as V_b, and its amplitude will be further discussed and derived in subsequent sections. Furthermore, v_C indicates the LV bridge's output voltage with an amplitude equivalent to V_b. L_k represents the leakage inductance of the transformer, while i_T represents the current flowing through the transformer. The magnetizing inductance is disregarded in this context as it exclusively pertains to the HV bridges' ZVS and is unrelated to the LV bridge's ZVS. Further details regarding the ZVS implementation of the HV bridges can be found in the last section. Considering the configuration in **Fig. 3-2**, two HV bridges can be simplified as two synchronized square voltage sources with a 50% duty cycle, as depicted in **Fig. 3-27(a)**. C illustrates the detailed waveforms of voltage and current pertaining to the triangular current.

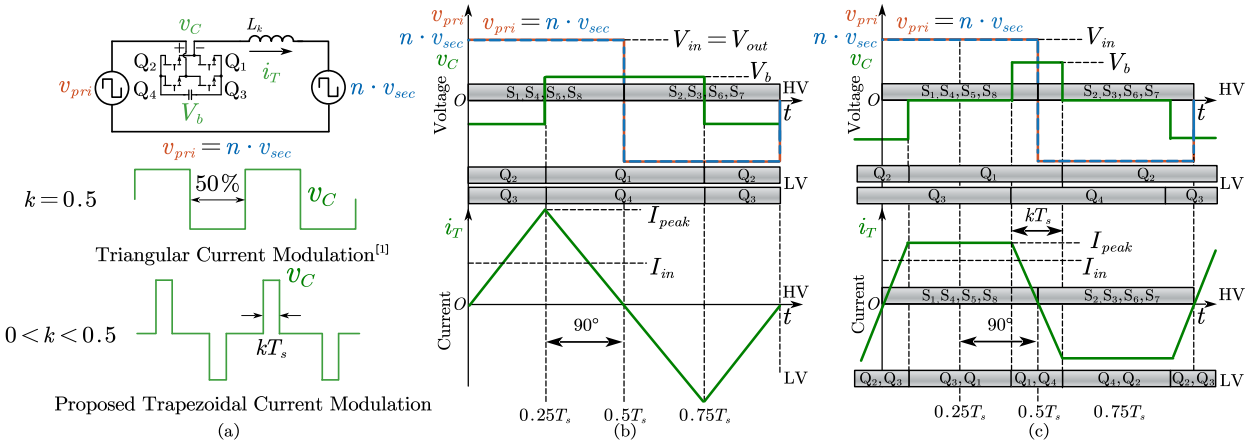


Fig. 3-27. Simplified EET-DCX circuit and related v_C waveforms. (b) previous triangular current modulation in [26], (c) proposed trapezoidal current modulation.

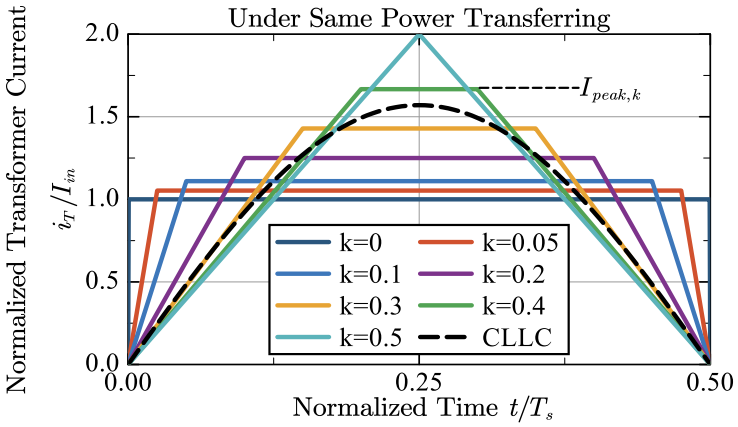


Fig. 3-28. Normalized transformer current i_T/I_{in} with different k. A certain case is shown in Fig. 3-27.

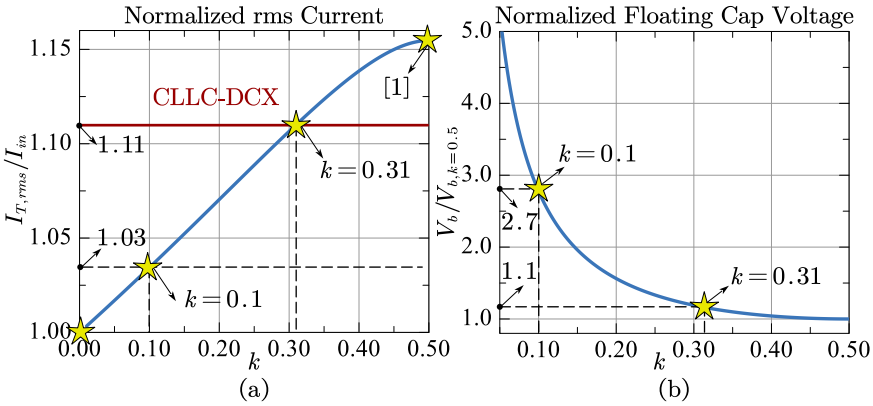


Fig. 3-29. (a) Transformer rms current $I_{T,rms}$, and (b) floating capacitor voltage V_b.

It is important to mention that this modulation technique has been extensively discussed in [26]. In the steady state, the relationship between V_{in} and V_{out}, I_{in} and I_{out}, and v_{pri} and v_{sec} can be directly determined based on the analysis.

$$V_{in} = n \cdot V_{out},\ I_{in} = I_{out}/n,\ v_{pri} = n \cdot v_{sec} \tag{3.29}$$

Based on Eq. (3.29), it can be observed that when v_{pri} equals v_{sec}, only the voltage source v_C will be utilized to drive L_k, resulting in the generation of a triangular current waveform, as shown in **Fig. 3-27(b)**. Consequently, the floating capacitor voltage V_b can be derived as shown in Eq. (3.30) . In **Fig. 3-27(a)**, the v_C waveform in traditional triangular modulation is represented by 50% duty cycle square waveforms with an amplitude of V_b, as derived in Eq. (3.30). The corresponding gating signals for the LV bridge switches Q_1-Q_4 are depicted in **Fig. 3-27(b)**. To transform the current waveform from triangular to trapezoidal, a zero-voltage stage (Q_1, Q_3, or Q_2, Q_4) needs to be introduced to v_C, creating a "current plateau," as illustrated in **Fig. 3-27(a)**. This plateau can be achieved by introducing a phase shift of kT_s between the phase legs Q_1, Q_2, Q3, and Q_4, as shown in **Fig. 3-27(c)**. Alternatively, the phase shift k can be interpreted as the duty cycle of v_C, as illustrated in **Fig. 3-27(a)**. The range of k varies from 0 to 0.5. Similar to the analysis conducted in triangular current modulation [26], the load-independent voltage gain derived from Eq. (3.29) remains valid in the trapezoidal current modulation. **Fig. 3-28** illustrates the normalized transformer current i_T/I_{in} for various duty cycles (k) under the condition of the same power transfer. When $0 < k < 0.5$, the transformer current i_T exhibits a trapezoidal waveform. At $k = 0$, the current waveform transitions to the ideal square waveform. Conversely, triangular modulation can be regarded as a special case of trapezoidal modulation when k=0.5. Additionally, for comparison purposes, the resonant current from CLLC-DCX is represented as a dashed line, assuming the same power rating.

By employing the proposed trapezoidal current modulation, the peak current (I_{peak}), rms transformer current ($I_{T,rms}$), and voltage (V_b) can be re-derived as follows:

$$I_{peak} = \frac{1}{1-k} \cdot I_{in} \tag{3.30}$$

$$I_{T,rms} = \frac{1}{1-k} \cdot \sqrt{\frac{3-4\cdot k}{3}} \cdot I_{in} \tag{3.31}$$

$$V_b = \frac{2 f_s L_k}{(1-k)k} \cdot I_{in} \tag{3.32}$$

When k=0.5, these results align with the findings in [1] regarding triangle modulation. **Fig. 3-29(a)** presents the normalized rms current $I_{T,rms}$ from equation (3.31), based on I_{in}. Comparing it with the sinusoidal current (1.11·I_{in}) observed in CLLC-DCX, the rms current can be reduced by 8% and 11% for k=0.1 and 0, respectively. Notably, for k=0.1, the rms current is significantly reduced by 13% compared to the previous triangle modulation in [26] at k=0.5. At k=0.31, EET-DCX exhibits the same rms current as CLLC-DCX.

On the other hand, **Fig. 3-29(b)** illustrates the normalized voltage V_b based on $V_{b,k=0.5}$. The only drawback of trapezoidal current modulation is that V_b increases compared to triangular current modulation when k=0.5. For example, when k=0.31, 0.1, and 0.01, V_b increases by 1.1, 2.7, and 5 times, respectively. Therefore, there is a trade-off: as k approaches 0, the trapezoidal current becomes more like a square waveform with a smaller rms current, but it results in an increase in V_b across the floating DC capacitor. However, in practical scenarios, V_b is typically very small when the high-frequency transformer electromagnetic design is optimized to minimize the leakage inductance. For instance, when k=0.1, f_s=250 kHz, L_k=200 nH, and I_{in}=10 A, the value of V_b derived from Eq. (3.32) is approximately 10 V. This indicates that the increased V_b is acceptable when it leads to a reduction in rms current.

3.3.2 Re-analysis for ZVS and Current Sharing

Fig. 3-36 illustrates a half-period current commutation process, showcasing the realization of zero-voltage switching (ZVS) for LV bridge switches Q_4 and Q_1. A similar mechanism applies to the other pair of switches, Q_2 and Q_3, during the other half of the period. Initially, during the transition from Q_2, Q_3 to Q_1, Q_3, switch Q_1 achieves ZVS as the current i_{peak} flows through the body diode D_1 before the switch turns on. Following the current plateau stage (zero stage Q_1, Q_3), switch Q_4 achieves ZVS using the same process. It is important to note that achieving ZVS on the LV bridge is independent of the load since both i_{peak} and V_b are proportionate to the input current I_{in}, as determined by Eq. (3.30) and (3.32). Even under light load conditions, where i_{peak} decreases, the voltage across the LV bridge V_b also decreases, ensuring that the i_{peak} during the dead time is sufficient to achieve LV bridge ZVS.

Fig. 3-31(a) presents the transformer-level parallel configuration with multiple EET units, while the simplified equivalent circuit is depicted in **Fig. 3-31(b)**. Each EET unit is associated with a winding resistance r_{wN}. Despite the introduction of a zero stage in v_{CN}, the fundamental component of v_{CN} still exhibits a 90-degree phase difference from v_{pri} or v_{sec}. Consequently, the impedance of the leakage inductance L_{kN} can be effectively canceled out by each LV bridge in series. In **Fig. 3-32**, a simulation is presented with parameters k=0.2, f_s=250 kHz, V_{in}=V_{out}=300 V, $L_{k1(2)}$=200 nH, and I_{in}=I_{out}=30 A. The excellent current sharing is evident due to the equality of L_{k1} and L_{k2}, as observed from V_{b1}=V_{b2}=21 V (derived from Eq. (3.32)). At approximately 0.08 ms, a doubling of L_{k2} causes a temporary drop in current i_{T2}, as illustrated in **Fig. 3-32(b)**. However, after a transient period, V_{b2} automatically adjusts to double its value, ensuring i_{T1}=i_{T2} is maintained, thereby confirming the natural current-sharing characteristic of the proposed trapezoidal modulation.

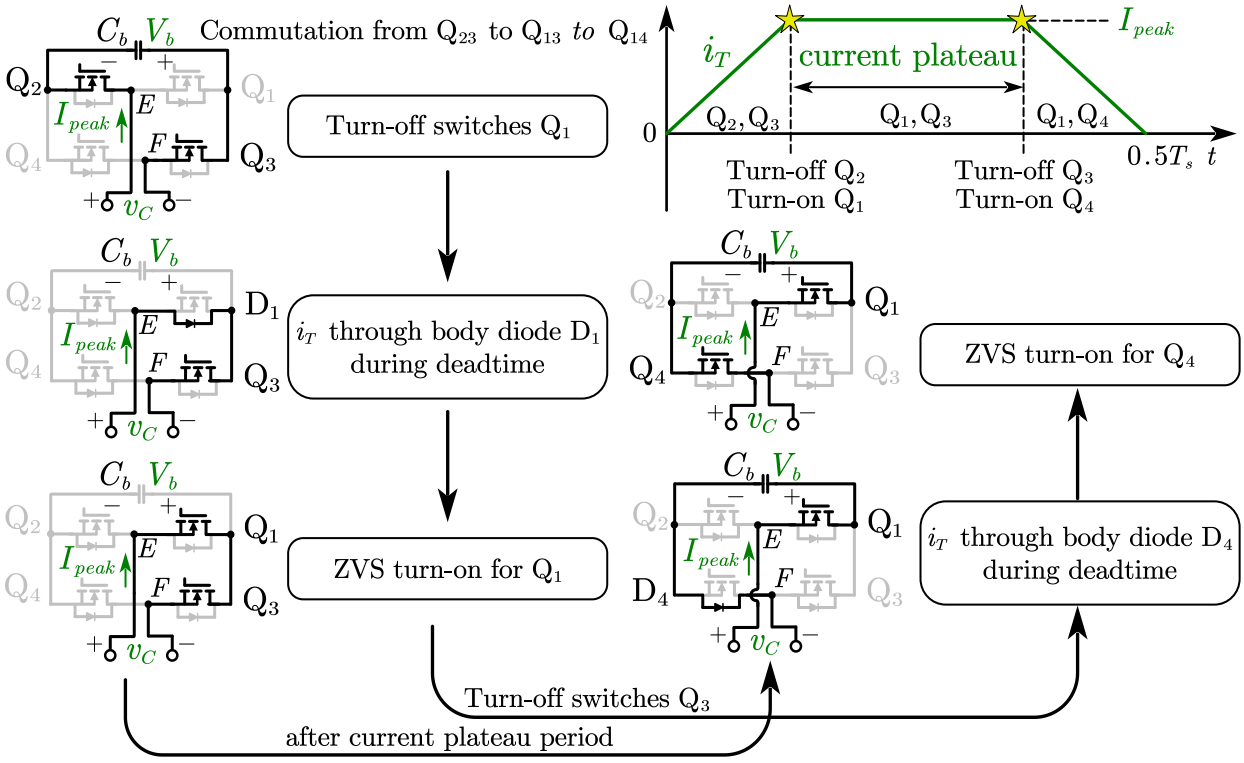


Fig. 3-30. ZVS analysis for LV bridge of EET-DCX with trapezoidal modulation. The related circuit diagram can be found in Fig. 3-27.

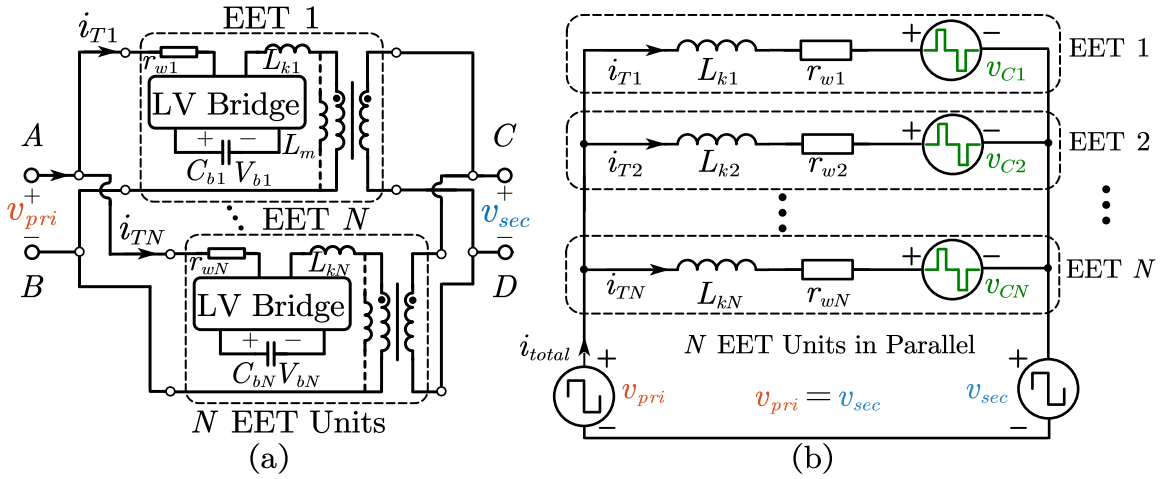


Fig. 3-31. Transformer-level parallel: (a) circuit diagram, (b) equivalent circuit. The parallel circuit diagram can be modified from the single unit diagram shown in Fig. 3-27.

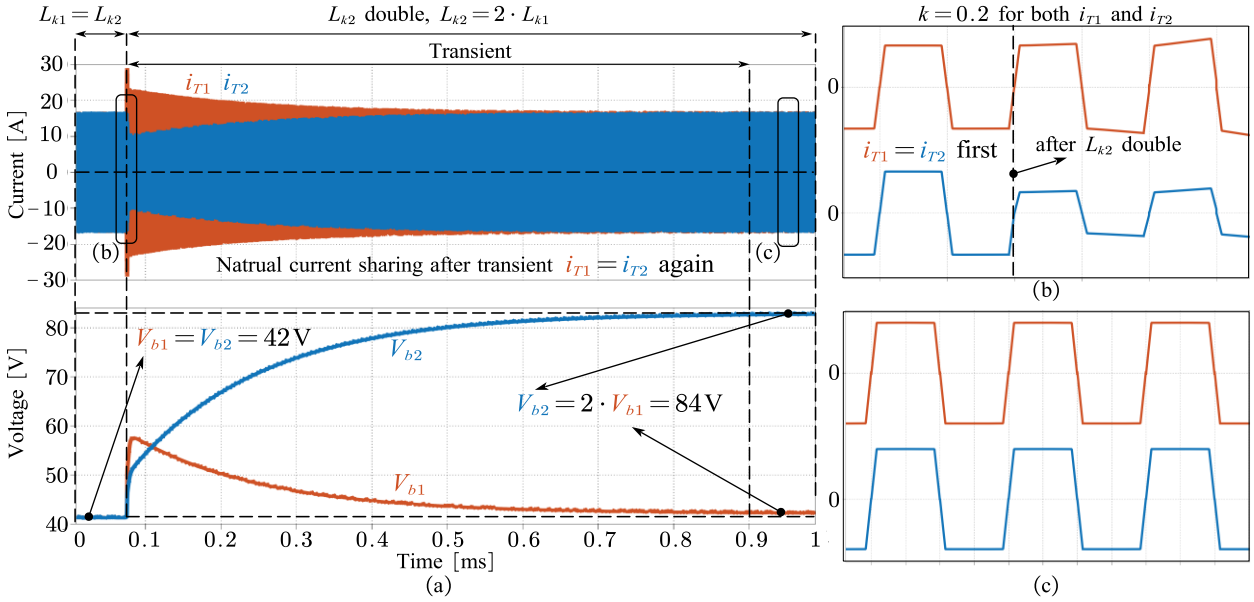


Fig. 3-32. Simulated waveforms: (a) currents and voltages in a large scale of 1 ms, (b) currents when the transient L_{k2} doubled, (c) good current sharing after transient.

3.3.3 Experimental Validation

To validate the analysis of trapezoidal modulation, a practical implementation of a 12 kW EET-DCX system was constructed, as depicted in the last section, **Fig. 3-15**. This system comprises four EET units operating in parallel. In comparison to the EET unit design described in [26], modifications were made to enable its operation as an LLC-DCX. Specifically, a resonant capacitor was introduced in series on the bottom side, and the entire LV bridge was shorted using two copper pads on the top side. Detailed parameters of the system can be found in

Table 3-4.

Fig. 3-33 presents the experimental results for each EET unit operating at a full load of 3 kW. **Fig. 3-33(a)** showcases the outcomes of the LLC-DCX configuration, where the LV bridge was shorted, and an external resonant capacitor was incorporated. In **Fig. 3-33(a)-(c)**, the results for trapezoidal modulation with k values of 0.5, 0.4, and 0.2 are displayed, respectively. As anticipated from the previous analysis, when k=0.5, the current waveform takes the shape of a triangle, while reducing k moves the waveforms closer to a square waveform, resulting in a smaller rms value as predicted by Eq. (3.31). Furthermore, as k decreases, V_b increases, as indicated by Eq. (3.32).

Fig. 3-34 presents the experimental results of current sharing when operating at a full load of 12 kW with four EET units in parallel. In **Fig. 3-34(a)** and **(b)**, it can be observed that at a switching frequency of 250 kHz with k=0.2, the current sharing is excellent, with $i_{T1\text{-}4}$ closely matching each other after overlapping. Similarly, **Fig. 3-34(c)** demonstrates the favorable current-sharing results when the switching frequency is adjusted from 250 to 200 kHz while maintaining k at 0.2. Unlike

LLC-DCX, which necessitates resonant point tuning, EET-DCX, employing trapezoidal current modulation, can achieve optimal performance at any frequency.

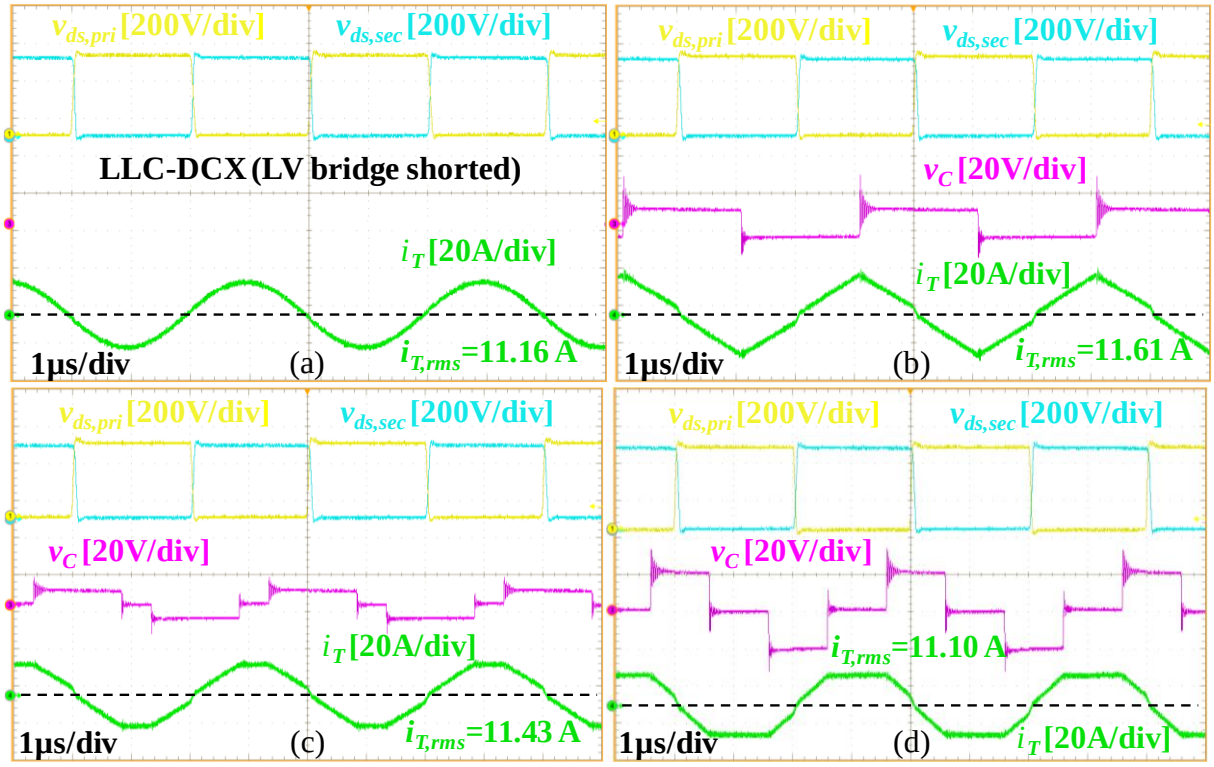


Fig. 3-33. Experimental results for each EET unit at full load 3 kW: (a) LLC-DCX configuration. LV bridge was shorted, and a resonant capacitor was added. (b) *k*=0.5, previous triangular current modulation in [26], (c) *k*=0.4, (d) *k*=0.3. The prototype can be found in Fig. 3-15.

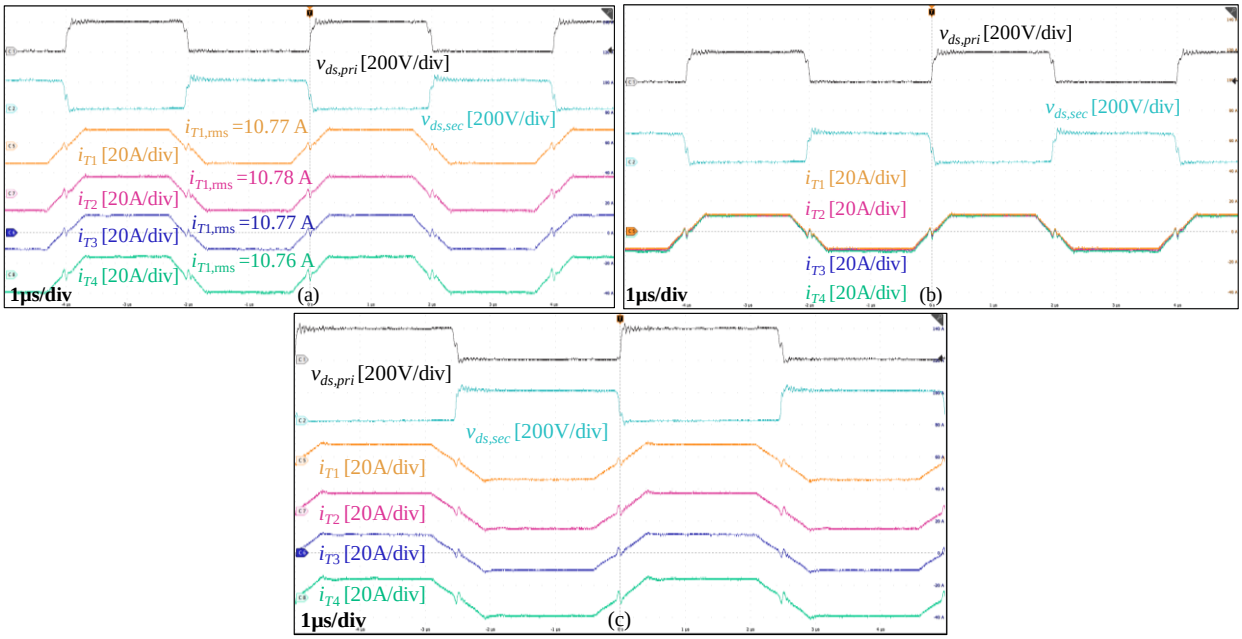


Fig. 3-34. Experimental results for current sharing at full load 12 kW with 4 EET units paralleled: (a) k=0.2, f_s=250 kHz with stacked waveforms, (b) k=0.2, f_s=250 kHz with overlapped waveforms, (c) k=0.2, f_s=200 kHz with stacked waveforms. The prototype can be found in Fig. 3-15.

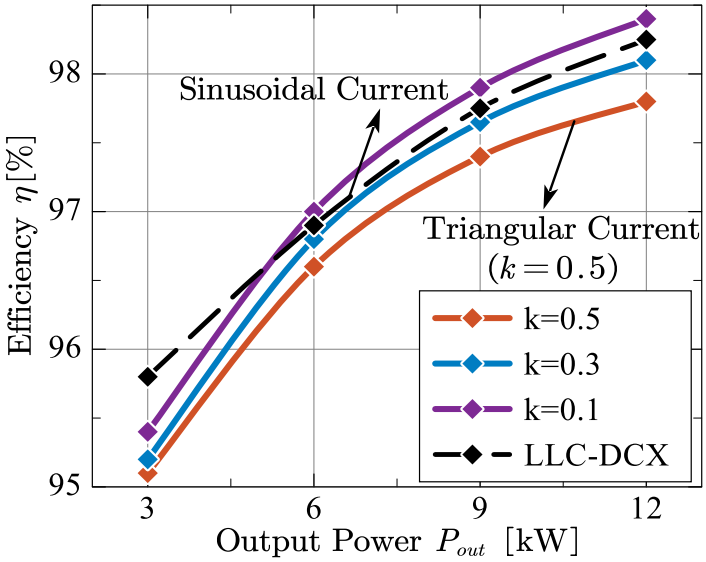


Fig. 3-35. EET-DCX Efficiency with different k. The prototype can be found in Fig. 3-15.

The small distortion on the transformer current is caused by the resonance between the HV bridge parasitic output capacitance and transformer leakage inductance. The measurement rms current $I_{T,rms}$ can be found in both **Fig. 3-33** and **Fig. 3-34(a)** with k=0.5, 0.4, 0.3, and 0.2, respectively.

Fig. 3-35 presents the efficiency results for various values of k. To provide a benchmark, the efficiency of the resonant LLC-DCX (98.25% at 12 kW) is included. When k=0.5, the triangular current waveform still exhibits a higher rms current compared to the sinusoidal current of the LLC-DCX. However, as k approaches 0, for instance, when k=0.1, the EET-DCX achieves a higher efficiency (98.4% at 12 kW) due to the reduced rms current and total conduction loss, it is important to highlight that this reduction in conduction loss not only applies to the transformer windings but also encompasses the conduction loss of the HV bridge. This aspect is particularly advantageous in high-current, high-power applications, as the additional loss on the LV bridge becomes less significant in comparison.

3.4 Resonant Commutation (RC) EET-DCX

In light of the concept of EET and corresponding trapezoidal current modulation, this section presents two significant modifications. First, it replaces the complete full bridge with a low-voltage bidirectional AC switch. Second, it introduces a resonant commutation (RC) to realize a quasi-trapezoidal transformer current with a smaller rms value. In addition to streamlining the circuit, the proposed RC EET-DCX retains all the advantages of the original EET-DCX, including simple open-loop control and natural current sharing. By incorporating only one embedded bidirectional AC switch, the impedance of the high-frequency transformer leakage inductance is fully neutralized.

3.4.1 Operation Principle of RC EET-DCX

To better understand the proposed RC EET-DCX and its associated quasi-trapezoidal current modulation, the complete circuit diagram of RC EET-DCX is depicted in **Fig. 3-36**. Its corresponding voltage and current waveforms are shown in **Fig. 3-37**. The transformer turns ratio is denoted as n, and i_T represents the current flowing through the primary. V_{in} and V_{out} refer to the input and output voltages, respectively, while v_{pri} and v_{sec} represent the HV bridge output voltages on the primary and secondary sides. In contrast with the conventional EET-DCX, the entire LV bridge is substituted with only one bidirectional AC switch $Q_{1(2)}$. C_{o1} and C_{o2} are two symmetric parallel capacitors.

$$C_{o1} = C_{o2} \tag{3.33}$$

Depending on the practical application, C_{o1} and C_{o2} can be the semiconductor's parasitic capacitors or externally added components. $v_{ds,Q1}$ and $v_{ds,Q2}$ are two drain-to-source voltages

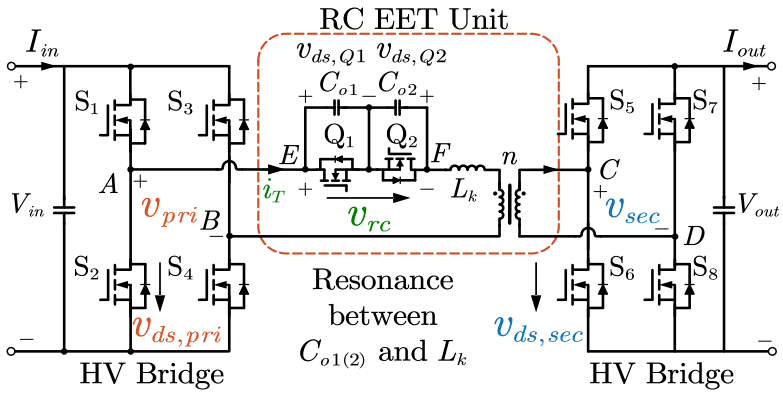


Fig. 3-36. Circuit diagram of the proposed RC EET-DCX.

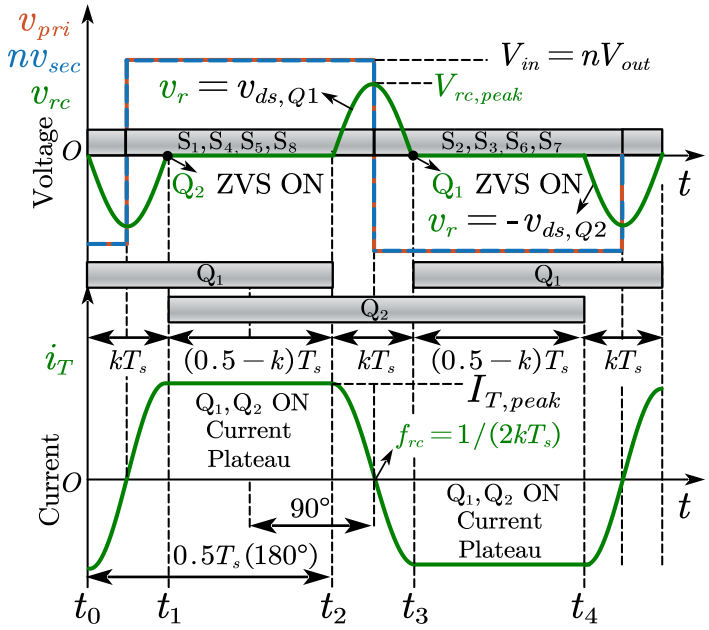


Fig. 3-37. Voltage and current waveforms of the proposed RC EET-DCX are shown in Fig. 3-36.

across Q_1 and Q_2. Voltage v_{rc} is the output resonant voltage across points E and F, and its peak value is $v_{rc,peak}$, as shown in **Fig. 3-37**.

$$v_{rc} = Q_1 \cdot v_{ds,Q1} - Q_2 \cdot v_{ds,Q2} \quad (Q_{1(2)} = 0 \text{ OFF}/1 \text{ ON}) \tag{3.34}$$

L_k stands for the leakage inductances of the transformer. Following the conclusion from the conventional EET-DCX in [1], in the steady state, the relationship between V_{in} and V_{out}, I_{in} and I_{out},

as well as v_{pri} and v_{sec}, can be initially defined in Eq. (3.35). The detailed explanation for this robust load-independent voltage gain will be discussed later.

$$\begin{cases} V_{in} = n \cdot V_{out} \\ I_{in} = I_{out}/n \\ v_{pri} = n \cdot v_{sec} \end{cases} \tag{3.35}$$

As shown in **Fig. 3-38**, both HV bridges have the same driving signals, which ensures that v_{pri} is in the phase of v_{sec}. Moreover, the gate signals for Q_1 and Q_2 both have a duty cycle of (1-k), and they exhibit a 180-degree (half cycle) phase shift, as shown in **Fig. 3-38**. Compared to the HV bridge control signals, $Q_{1(2)}$ leads with a 90-degree phase shift from S_1, S_4, S_5, S_8 (S_2, S_3, S_6, S_7). Based on this driving logic and Eq. (3.35), it can be observed that when v_{pri} equals nv_{sec}, only the voltage v_{rc} will be utilized to drive L_k, resulting in the generation of a quasi-trapezoidal current waveform as shown in **Fig. 3-38**. In a half cycle (from t_0 to t_2), during the current commutation from t_0 to t_1 (kT_s), only switch Q_1 is ON, and C_{o2} will resonate with L_k at the frequency f_{rc}.

$$f_{rc} = \frac{1}{2\pi\sqrt{L_k C_{o1(2)}}} \tag{3.36}$$

If L_k and $C_{o1(2)}$ are designed to resonate for a half cycle during $\underline{kT_s}$, an additional relationship between f_{rc} and f_s can be given as

$$f_{rc} = \frac{1}{2k} \cdot f_s \quad k \in (0, 0.5] \tag{3.37}$$

If the resonant frequency f_{rc} can be designed using Eq. (3.36) and (3.37), this half-cycle resonance between $C_{o1(2)}$ and L_k can be employed to realize the transformer current commutation during t_0-t_1

or t_2-t_3 as shown in **Fig. 3-37**. During the "Current Plateau" period from t_1 to t_2 ((0.5-k)T_s), both Q_1 and Q_2 are ON, making v_{rc} equal to 0. Due to no voltage across L_k, transformer current i_T remains flat, as shown in **Fig. 3-37**. Moreover, the ZVS turn-on for Q_2 and Q_1 will be achieved at the end of resonance (t_1 or t_3) because $v_{ds,Q2}$, and $v_{ds,Q1}$ will drop to zero. This significantly differentiates from the conventional EET-DCX, which requires a full bridge to accomplish the current commutation. The complete RC EET-DCX current commutation only requires a single bidirectional AC switch Q_{12}.

3.4.2 Robust Load-Independent Voltage Gain

To illustrate the robust independent voltage gain of RC EET-DCX in Eq. (3.35), **Fig. 3-38** shows the whole procedure with a certain load. Utilizing the superposition principle, RC EET-DCX shown in **Fig. 3-38(a)** can be disassembled into two components. The first is the HV bridge part shown in **Fig. 3-38(b)**, while the second is the LV bidirectional switch part depicted in **Fig. 3-38(c)**. The operation principle of the robust load-independent voltage gain can be explained in six steps:

***Step* 1:** Assuming V_{in} is larger than nV_{out} as shown in **Fig. 3-38(b)**, the voltage difference (V_{in}-nV_{out}) will be applied to L_k directly, causing the triangular current $i_{T,I}$ to exhibit a 90-degree phase shift from v_{pri} or v_{sec}. Obviously, due to this 90-degree phase shift, there is no real power delivered to the receiving side by $i_{T,I}$.

***Step* 2:** Since the current $i_{T,I}$ in **Fig. 3-38(b)** is in phase with the voltage v_C in **Fig. 3-38(c)**, it will always charge the capacitors C_{o1} and C_{o2} alternately. For example, from t_0 to t_1, the current $i_{T,I}$ is negative, as shown in **Fig. 3-38(b)**, and at the same time, only LV switches Q_1 is ON (Q_2 is OFF). Therefore, the electric charge Q_{Co2} will be charged to C_{o2}. As for another half period from t_2 to t_3,

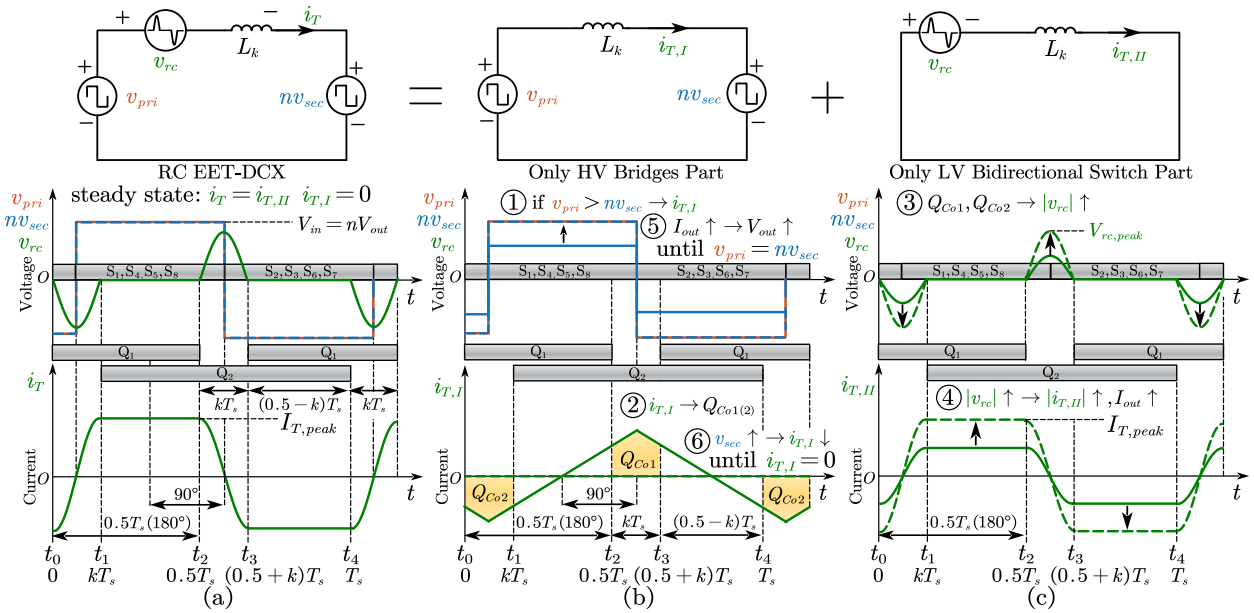


Fig. 3-38. The whole procedure of the robust load-independent voltage gain: (a) whole RC EET-DCX, (b) only HV bridge part, and (c) only LV bridge part. The original circuit diagram can be found in Fig. 3-36.

positive $i_{T,I}$ will generate Q_{Co1} to charge the capacitor C_{o1}. In conclusion, over a complete cycle, Q_{Co1} equals Q_{Co2}, maintaining the waveform v_{rc} in a state of positive and negative symmetry.

***Step* 3:** If V_{in} is larger than V_{out}, Q_{Co1}, and Q_{Co2} generated from current $i_{T,I}$ will always increase the amplitude of v_{rc} during the whole period.

$$i_{T,I} \rightarrow Q_{Co1}, Q_{Co2} \rightarrow |v_{rc}| \uparrow \tag{3.38}$$

***Step* 4:** As depicted in **Fig. 3-38(c)**, when excited solely by the voltage source v_{rc}, the current $i_{T,II}$ assumes a quasi-trapezoidal shape and can be derived as

$$i_{T,II}(t) = \begin{cases} -I_{T,peak} \cdot \cos(2\pi f_{rc} \cdot t) & t \in [0,\ kT_s] \\ I_{T,peak} & t \in [kT_s,\ 0.5T_s] \end{cases} \tag{3.39}$$

Where $I_{T,peak}$ represents the peak value of i_T, and the range of k is from 0 to 0.5. As the value of v_{rc} from Eq. (3.38) increases, the amplitude of the current $i_{T,II}$ will become larger, as shown in **Fig. 3-38(c)**. Additionally, the power $P_{T,II}$ delivered to the receiving side by $i_{T,II}$ can be given as

$$P_{T,II} = \int_0^{T_s} n \cdot v_{sec}(t) \cdot i_{T,II}(t) \tag{3.40}$$

Since v_{sec} is always in phase with $i_{T,II}$, with a larger $i_{T,II}$ shown in the dashed line, more real power $P_{T,II}$ will be delivered to the receiving side.

***Step* 5:** If the receiving power increases with a certain load, the corresponding output voltage V_{out} will increase until nV_{out} is equal to V_{in}.

$$I_{out} \uparrow \rightarrow V_{out} \uparrow, |v_{sec}| \uparrow \text{ until } n \cdot V_{out} = V_{in} \tag{3.41}$$

***Step* 6:** Meanwhile, assuming V_{in} is constant, an increasing V_{out} will lead to a smaller current $i_{T,I}$ until nV_{out} is equal to V_{in}.

In summary, the whole mechanism of RC EET-DCX in **Fig. 3-38** can be expressed as Eq. (3.42). When nV_{out} equals V_{in}, the current $i_{T,I}$ becomes zero and the peak voltage and current values, $V_{rc,peak}$ $I_{T,peak}$, respectively, remain constant, signifying that the RC EET-DCX has entered the steady state. Previous analysis from ***Steps* 1-6** is based on the premise that V_{in} is larger than nV_{out}. Conversely, if V_{in} is smaller than nV_{out}, a similar analysis from Eq. (3.37)-(3.41) leads to the conclusion that $i_{T,II}$ will discharge capacitors C_{o1}, C_{o2} during t_0-t_1 and t_2-t_3 alternately, which will result in a reduction in the output current I_{out}. With a certain load, a reduced I_{out} will decrease V_{out} until V_{in} equals nV_{out}.

$$\begin{cases} V_{in} > nV_{out} & i_{T,II} \to |v_{rc}| \uparrow \to I_{out} \uparrow \to V_{out} \uparrow \\ V_{in} = nV_{out} & i_{T,II} = 0 \to \text{const } V_{rc,peak}, I_{T,peak}, I_{out}, V_{out} \\ V_{in} < nV_{out} & i_{T,II} \to |v_{rc}| \downarrow \to I_{out} \downarrow \to V_{out} \downarrow \end{cases} \tag{3.42}$$

3.4.3 Steady State of RC EET-DCX

In the steady state, with a turns ratio n, the input voltage V_{in} should be equal to nV_{out} based on the analysis in Eq. (4.42). Therefore, like the conventional EET-DCX, the proposed RC EET-DCX also maintains a robust, load-independent voltage gain as derived from Eq. (3.35).

As for the current i_T, the component $i_{T,I}$ should equate to 0 in the steady state. If not, this current will continue to generate Q_{Co1} and Q_{Co2}, as shown in **Fig. 3-38(b)**. Consequently, the current i_T in steady state should be equal to $i_{T,II}$. Since this steady state is a stable equilibrium point, no additional control is required.

$$\begin{cases} i_{T,I} = 0 \\ i_T = i_{T,II} \end{cases} \tag{3.43}$$

Fig. 3-39 illustrates the steady-state waveforms of RC EET-DCX under varying load conditions. In the steady state, the transformer current i_T is in phase with terminal voltages v_{pri} and v_{sec}, making the transformer current dedicated to real power transfer. With different loads, the amplitude of the quasi-trapezoidal current i_T is regulated via v_{rc}, as shown in **Fig. 3-39**. Since i_T equals $i_{T,II}$ in the steady state, the time-domain expression of i_T(t) can be directly found in Eq. (3.39). On the other hand, input DC current I_{in} equals the average value of current i_T.

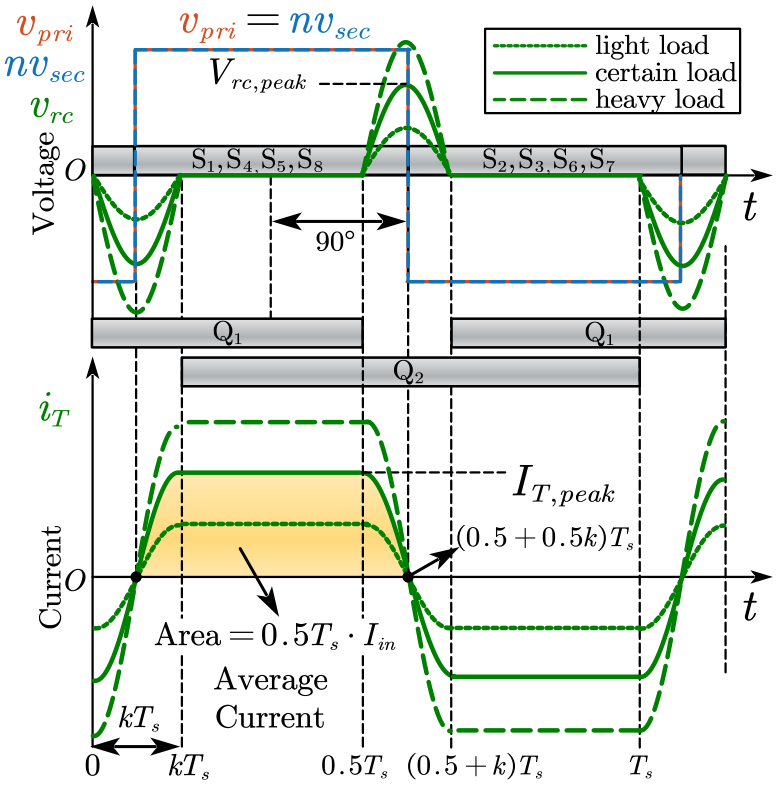


Fig. 3-39. Steady-state waveforms of RC EET-DCX under different loads. A certain load case can be found in Fig. 3-38.

$$I_{in} = \text{average current} = \frac{2}{T_s}\int_{0.5kT_s}^{(0.5+0.5k)T_s} i_T(t)\cdot dt \tag{3.44}$$

From Eq. (3.39) and (3.44), the relationship between $I_{T,peak}$, and I_{in} can be given as

$$I_{T,peak} = \frac{\pi}{4\cdot k + (1-2\cdot k)\cdot \pi}\cdot I_{in} \tag{3.45}$$

Following Eq. (3.39), (3.45), the transformer rms current $I_{T,rms}$ can also be derived as

$$\begin{aligned} I_{T,rms} &= \frac{1}{T_s}\sqrt{\int_0^{T_s} {i_T}^2(t)\,dt} \\ &= \frac{\sqrt{1-k}\cdot\pi}{(1-2\cdot k)\cdot\pi + 4\cdot k}\cdot I_{in} \end{aligned} \tag{3.46}$$

As for the resonant voltage v_{cr} in the steady state, the time-domain expression of v_{cr}(t) can be given as

$$v_{cr}(t) = \begin{cases} -V_{cr,peak} \cdot \sin(2\pi f_{rc} \cdot t) & t \in [0,\ kT_s] \\ 0 & t \in [kT_s,\ 0.5T_s] \end{cases} \tag{3.47}$$

Where the peak voltage value $V_{cr,\,the\,peak}$ can be derived as

$$\begin{aligned} V_{rc,peak} &= L_k \cdot \left.\frac{di_T(t)}{dt}\right|_{t=(0.5+0.5k)T_s} \\ &= \frac{\pi^2}{k \cdot (4 \cdot k + (1-2 \cdot k) \cdot \pi)} \cdot f_s \cdot L_k \cdot I_{in} \end{aligned} \tag{3.48}$$

From Eq. (3.48), the peak voltage $V_{rc,peak}$ applied on the LV bidirectional switch Q_1 and Q_2, is proportional to switching frequency f_s, leakage inductance L_k, and input DC current I_{in}.

$$V_{rc,peak} \propto f_s,\ L_k,\ I_{in} \tag{3.49}$$

With a pre-determined I_{in}, f_s, and k, minimizing the transformer leakage inductance L_k becomes crucial as it reduces the voltage stress on the LV bidirectional switch. By using a smaller voltage rating GaN FETs, the bidirectional switch can be easily embedded into the high-frequency transformer windings. Importantly, the voltage stress $V_{rc,peak}$ is unrelated to input or output voltage $V_{in(out)}$ according to Eq. (3.48), indicating that this proposed RC EET-DCX can be adopted in high-voltage applications. Therefore, even with large input and output voltages, an LV bidirectional switch can still be selected. To summarize, since V_{in} is equal to nV_{out} at the steady state, the resonant voltage v_{rc} will be directly applied to L_k, compensating fully for the voltage drop on L_k with the embedded LV bidirectional switch.

3.4.4 Comparison with LLC-DCX and Typical EET-DCX

Based on the time-domain expression of $i_T(t)$ from Eq. (3.39), **Fig. 3-40** illustrates the normalized transformer current i_T/I_{in} with different values of k. At the same power level, the current i_T is normalized based on the input DC current I_{in}. When $0 < k < 0.5$, the transformer current i_T exhibits a quasi-trapezoidal waveform composed of two parts: one represents the resonance part during current commutation, and the other part is the "current plateau." As k approaches 0, the current waveform changes to an ideal square waveform, while for k=0.5, the resonant current occupies the entire period, and the "current plateau" disappears, effectively transitioning the RC EET-DCX to the traditional resonant CLLC-DCX. Additionally, for comparison purposes, the triangular current from a typical EET-DCX in [26] is depicted as a dashed line, assuming the same power rating.

Following Eq. (3.46), **Fig. 3-41(a)** depicts the normalized rms current $I_{T,rms}$ based on I_{in} for different values of k. In comparison with the sinusoidal current ($1.11 \cdot I_{in}$) observed in CLLC-DCX or k=0.5 case, the rms current can be reduced by 9% and 11% for k=0.1 and 0, respectively. Notably, for k=0.1, the rms current is significantly reduced by 13% compared to the typical EET-DCX in [26].

On the other hand, **Fig. 3-41(b)** represents the normalized peak voltage $V_{rc,peak}$ based on $V_{rc,peak}$ with k=0.5 from Eq. (3.48). The proposed RC EET-DCX and corresponding quasi-trapezoidal current modulation have one drawback: $V_{rc,peak}$ increases as k decreases. Theoretically, reducing k to 0 would yield a square waveform transformer current, which is optimal. However, based on Eq. (3.48), as k approaches 0, $V_{cr,peak}$ increases dramatically. For instance, when k=0.1, $V_{rc,peak}$ increases by 4.2 times compared to the typical EET-DCX in [26].

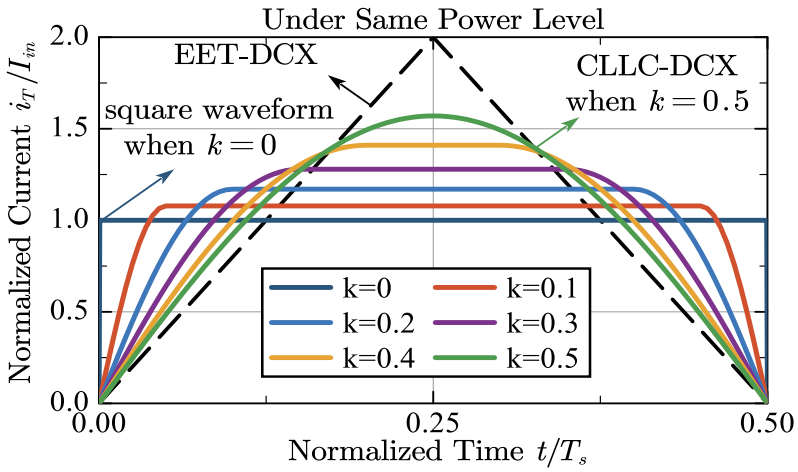


Fig. 3-40. RC EET-DCX normalized transformer current i_T/I_{in} with different k.

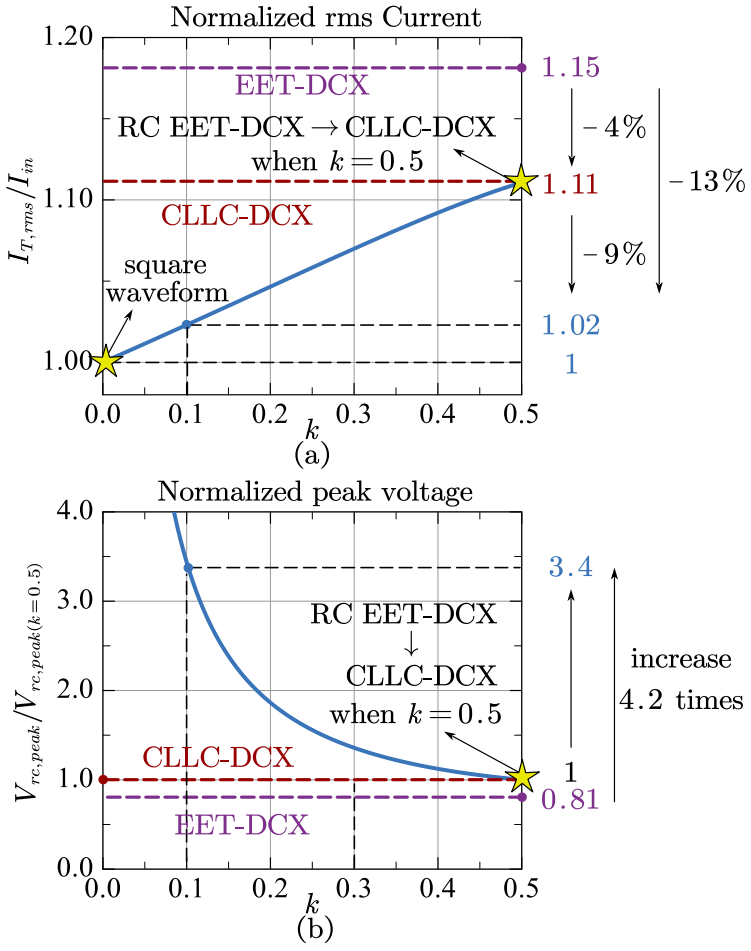


Fig. 3-41. Normalized current and voltage of the proposed RC EET-DCX: (a) normalized transformer rms current $I_{T,rms}$ based on input dc current I_{in}, (b) normalized peak voltage $V_{rc,peak}$ based on k=0.5 case. When k=0.5, the proposed RC EET-DCX will be a traditional CLLC-DCX. The corresponding time-domain current waveforms with different k can be found in Fig. 3-41.

Therefore, there is a trade-off: as k approaches 0 and the quasi-trapezoidal current becomes more like a square waveform with a smaller rms current, as shown in **Fig. 3-40**, it results in an increase in $V_{rc,peak}$ across the bidirectional switch as shown in **Fig. 3-41(b)**. Nevertheless, in practical scenarios, $V_{rc,peak}$ is typically very small.

For instance, when I_{in} is 10 A, f_s is 200 kHz, k is 0.1, and L_k is 300 nH, the voltage stress $V_{rc,peak}$ on the bidirectional switch can be derived as only 20 V from Eq. (3.48). This indicates that the increased $V_{rc,peak}$ is acceptable when it leads to a reduction in rms current.

In conclusion, the proposed RC EET-DCX, with its related quasi-trapezoidal current modulation, offers several advantages. Firstly, it reduces the total number of transistors from 4 (full bridge) to 2 (split) or 1 (monolithic). Additionally, the corresponding quasi-trapezoidal current can dramatically reduce the total conduction loss due to a smaller rms current. It should be noted that the total conduction loss comprises two HV bridge power module losses, one LV bidirectional switch loss, and the transformer winding loss.

3.4.5 Sensitivity Study on Current Sharing

1) Current Sharing Performance Overview

As mentioned above, due to higher power density, the transformer-level parallel solution is more desirable than the converter-level parallel when the DCX rating power needs to be scaled up. **Fig. 3-42** depicts three transformer-level parallel solutions with CLLC, EET in [26], and proposed RC EET, respectively. **Fig. 3-42(a)** shows three detailed circuit diagrams: CLLC with a resonant capacitor, EET with a full bridge, and RC EET with a bidirectional switch. After transforming secondary parameters to the primary side, the corresponding simplified equivalent circuits are depicted in **Fig. 3-42(b)**. $i_{T1\text{-}N}$ represents the transformer currents among each parallel unit, and $r_{w1\text{-}N}$ denotes the loop resistances on each parallel unit. Due to the robust, load-independent voltage gain from Eq. (3.35), the two HV bridges in Fig. 3-42(a) are replaced by two identical square voltage sources, v_{pri} and nv_{sec}. According to the topology solution, $v_{rc1\text{-}N}$ can be replaced by a sinewave (CLLC), a square wave (EET), or a combination of sinewave and zero-stage waveform (RC EET). Based on Kirchoff's voltage law (KVL), the terminal voltage v_{AB} can be expressed as

$$V_{AB} = jwL_{kN} \cdot i_{TN} + v_{rcN} + r_{wN} \cdot i_{TN} \quad (N = 1, 2, 3...) \tag{3.50}$$

Since the current sharing performance of CLLC-DCX and EET-DCX has been illustrated before [26], the conclusions can be summarized as follows:

1. CLLC-DCX's current sharing performance is highly sensitive to the parameters, especially the tolerance on leakage inductance L_k. When the converter deviates from the resonant point, the current sharing becomes poor. Achieving precise current sharing in CLLC-DCX requires tight control over the parameters, which can be challenging during practical implementation.

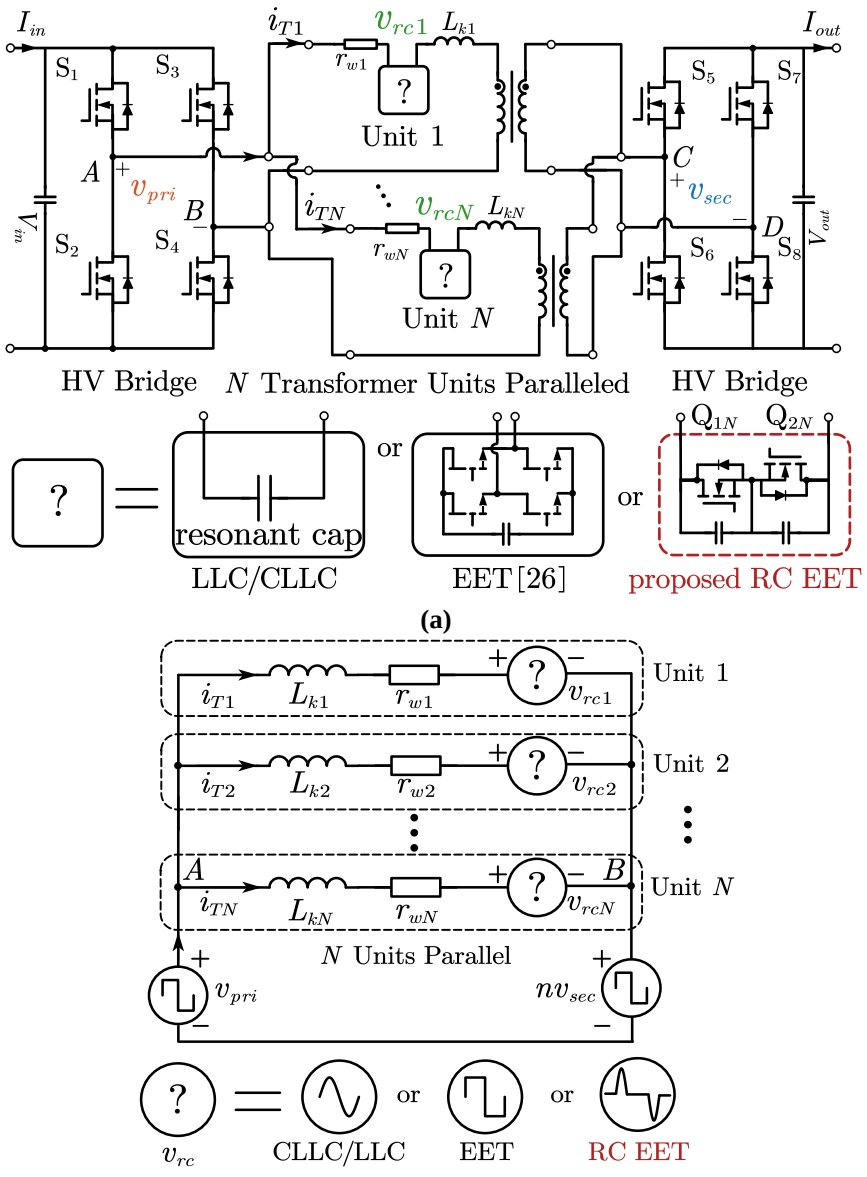


Fig. 3-42. Transformer-level parallel solution with LLC or EET or proposed RC EET unit: (a) circuit diagrams, (b) simplified equivalent circuits. The circuit diagram with multiple units was derived from the single unit diagram shown in Fig. 3-38.

2. EET-DCX proposed in [26] exhibits a very robust current sharing characteristic. This is because the square voltage source v_{rcN} always cancels out the impedance from the leakage inductance L_k. As a result, the current sharing is primarily determined by each parallel transformer's resistance r_w, which can be more easily controlled during the manufacturing or assembly processes.

In Summary, the natural current sharing of EET-DCX is a result of a constant 90-degree phase shift between v_{rc} and $v_{pri(sec)}$. On the contrary, for resonant CLLC-DCX, v_{rc} will only have a 90-degree phase shift from v_{rc} and $v_{pri(sec)}$ when it precisely operates at the resonant point. Deviations from this point can lead to significant challenges in achieving satisfactory current sharing.

2) Leakage Inductance Tolerance Impact

Regarding the proposed RC EET-DCX, the current sharing scenario differs from that of the typical EET-DCX due to the influence of the tolerance on L_k, which affects the resonant commutation frequency f_{rc} as per Eq. (3.36). To illustrate this impact, **Fig. 3-43** demonstrates two cases: one with no tolerance and another when L_k has been multiplied by a factor of m. Let's discuss the situation when m<1 first, implying that the real leakage inductance is smaller than the designed value L_k. In this case, with the tolerance factor m considered, both the resonant commutation voltage $v_{rc,m}$ and transformer current $i_{T,m}$ are plotted in **Fig. 3-43**.

As shown in **Fig. 3-43**, a smaller leakage inductance mL_k will result in an increased resonant commutation frequency from f_{rc} to $f_{rc,m}$. The relationship between $f_{rc,m}$, and the designed f_{rc} can be given as

$$f_{rc,m} = \frac{1}{m} \cdot f_{rc} \tag{3.51}$$

Where f_{rc} can be easily derived from Eq. (3.36) and (3.37), according to the driving signals for bidirectional switches Q_1 and Q_2, the resonant current commutation in **Fig. 3-43** will begin at the same time points "*A*" and "*D*," whether there is no tolerance (L_k) or with tolerance (mL_k). In the case of no tolerance, the entire current commutation will end precisely at points "*C*" and "*F*."

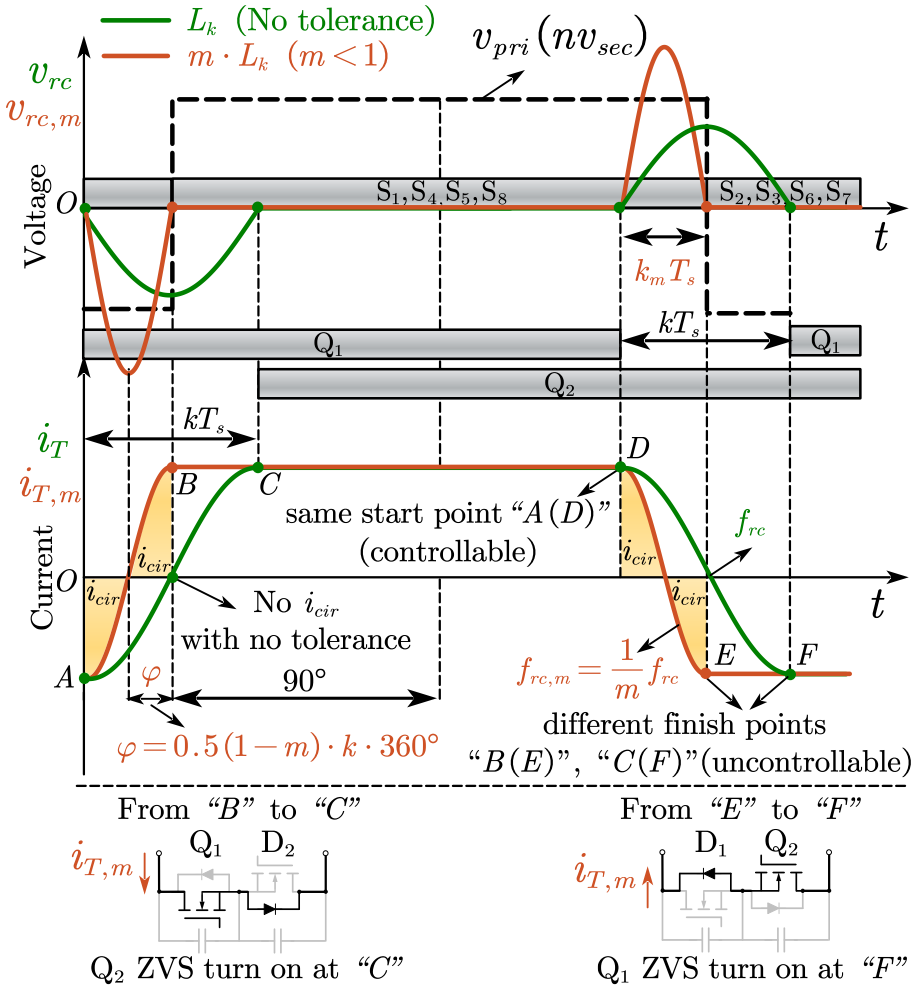


Fig. 3-43. Impact of the tolerance on leakage inductance L_k.

At these two time points, bidirectional switches Q_2 and Q_1 will turn on to achieve the ZVS, respectively. On the other hand, in the case of tolerance with mL_k leakage inductance, the current commutation will end earlier at time points "*B*" and "*E*." After the current commutation, from "*B*" to "*C*" and "*E*" to "*F*," the transformer current $i_{T,m}$ will go through one GaN FET's channel Q_1 (Q_2) and another transistor's body diode D_2 (D_1) shown in **Fig. 3-43**. Even with the tolerance, bidirectional switches Q_1 and Q_2 can still achieve ZVS turn-on. The reason for this is that before these two GaN FETs turn on at points "*C*" and "*F*", the transformer current has already passed through their body diodes. Due to the tolerance, a small phase difference between i_T and $i_{T,m}$ will occur, resulting in the existence of circulating current i_{cir}, as shown **Fig. 3-43**.

In conclusion, when the real leakage inductance is smaller than the design value, it can be considered equivalent to a new scenario with a small phase shift tolerance φ_m (defaulted to 90-dgree) and a new current commutation interval $k_m T_s$.

$$\varphi_m = 0.5 \cdot (1-m) \cdot k \cdot 360° \tag{3.52}$$

$$k_m = m \cdot k \tag{3.53}$$

Consider an example where k=0.2, and L_k has a -20 % tolerance (m=0.8). In this case, the phase shift tolerance φ can be calculated as only 7.2 degrees, and the new k_m is 0.16. Furthermore, the tolerance on phase shift itself, which usually defaults to 90-dgree, will be discussed in the next part of this section.

When the tolerance factor m is larger than 1, indicating that the real leakage inductance is larger than L_k, the bidirectional switches Q_1 and Q_2 will lose the ZVS and the current sharing performance will be disrupted. This disruption occurs because the resonant current commutation cannot be completed within the time interval of kT_s. **Fig. 3-44** illustrates the simulated waveforms of an RC EET-DCX with three parallel transformers. The simulation parameters are provided in **Table 3-5**. **Fig. 3-44(a)** shows the driving signals of HV bridges $S_{1\text{-}8}$ and LV bidirectional switches $Q_{1\text{-}2}$. In the case with no tolerance, depicted in **Fig. 3-44(b)**, all three current overlap very well, and the current sharing is perfect. **Fig. 3-44(c)** shows the case with m=0.8 (-20%) and m=0.6 (-40%) for L_{k2} and L_{k3}. Based on the previous analysis in **Fig. 3-43**, although there is a small phase difference among three transformer currents, i_{T1}, i_{T2}, and i_{T3}, the current sharing remains good because the current commutation starts at the same point for these three cases.

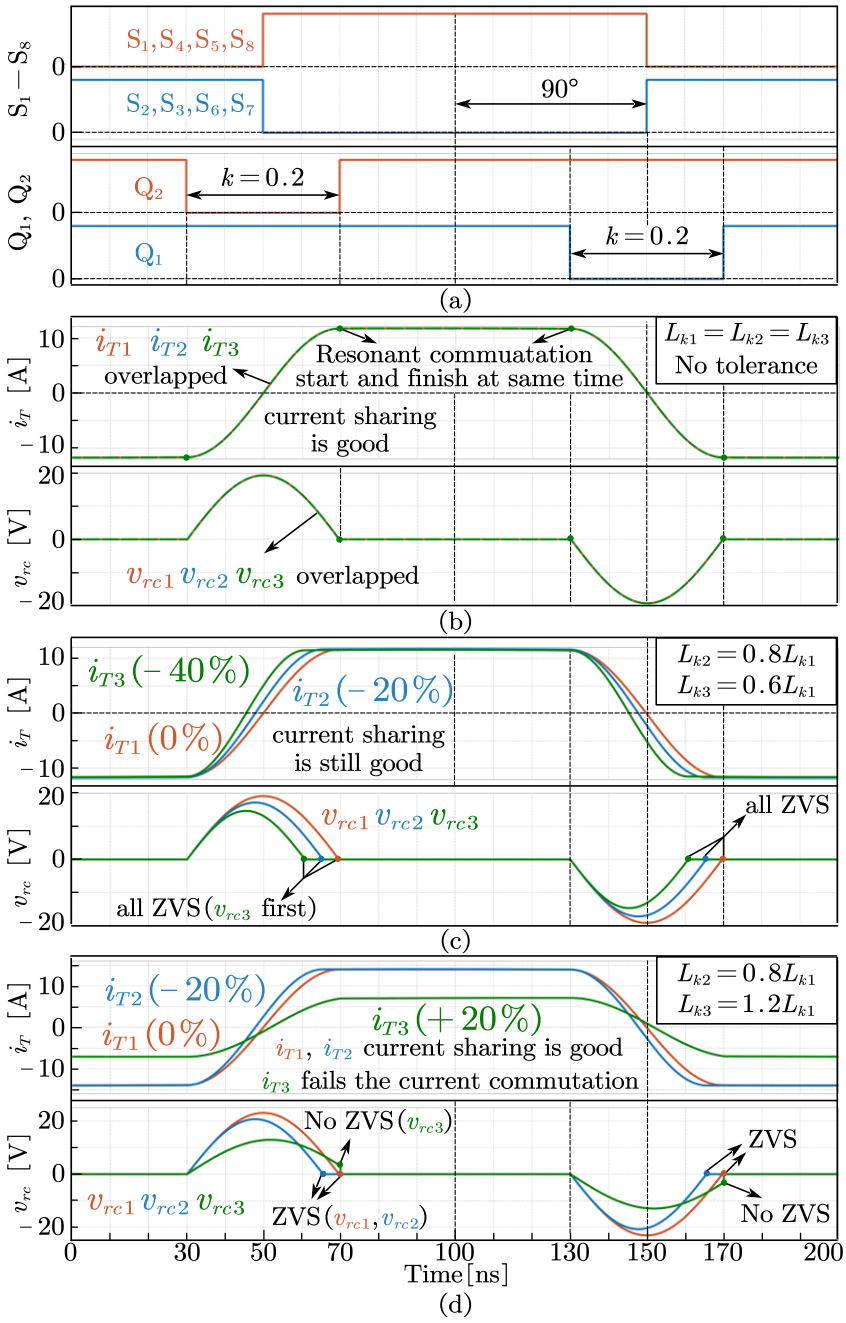


Fig. 3-44. Simulated currents and voltages of the proposed RC EET-DCX with the tolerance on leakage inductance.

Table 3-5 CURRENT SHARING SIMULATION PARAMETERS

Variable	Value	Variable	Value
Input voltage V_{in}	300 V	Output voltage V_{out}	300 V
Parallel number N	3	Loop resistance r_w	100 mΩ
Rating power P	9 kW	Switching frequency f_s	500 kHz
Commutation index k	0.2	RC frequency f_{rc}	2.5 MHz
Leakage inductance L_k	210 nH	Parallel capacitance $C_{o1(2)}$	36.2 nF

Finally, the larger inductance case when m>1 is depicted in **Fig. 3-44(d)**. As discussed earlier, when m>1, the current commutation fails, and LV bidirectional switches Q_1 and Q_2 lose ZVS because the resonant commutation period becomes longer than kT_s. To ensure the resonant current commutation can be successfully completed, some margin on L_k needs to be considered in practical design cases. More details about the RC EET-DCX hardware design will be discussed in the next section.

3) Phase Shift Tolerance Impact on Single Transformer

Since the tolerance on leakage inductance can be seen as a combination of phase shift tolerance and an adjusted k_m, the phase shift tolerance should be explained comprehensively. Firstly, with only one RC EET unit configuration (no parallel), as shown in **Fig. 3-36**, the phase shift tolerance impact is depicted in **Fig. 3-45**. Under ideal conditions, without any tolerance, the driving signals for HV bridges $S_{1\text{-}8}$ should maintain an open-loop 90-degree phase shift with the bidirectional switches $Q_{1\text{-}2}$. However, in real-world scenarios, a small tolerance denoted by φ can arise due to gate drivers' propagation delay and other factors. As a result, the new gating signals $Q_{1(2),\varphi}$ are introduced in **Fig. 3-45** to account for the phase shift tolerance. After considering this tolerance φ, the time domain expression for transformer current $i_{T,\varphi}(t)$, can be revised from Eq. (3.39).

$$i_{T,\varphi}(t)=\begin{cases} -I_{T,peak,\varphi}\cdot\cos(2\pi f_{rc}\cdot t+\varphi) & t\in[-\varphi,\ k-\varphi]\cdot T_s \\ I_{T,peak,\varphi} & t\in[k-\varphi,\ 0.5-\varphi]\cdot T_s \end{cases} \tag{3.54}$$

Where $I_{T,peak,\varphi}$ is the peak value of the transformer current $i_{T,\varphi}$ with the tolerance. Similarly, the derivation of the $I_{T,peak,\varphi}$ in **Fig. 3-45** can follow the average current calculation as below:

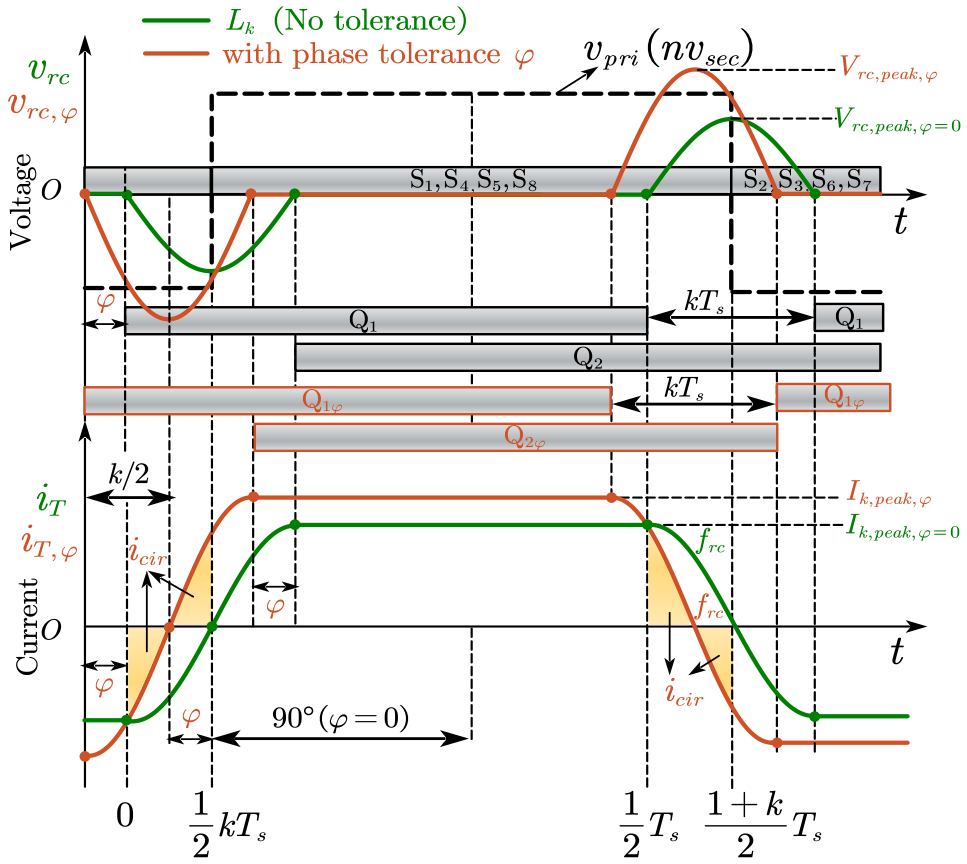


Fig. 3-45. Phase shift tolerance impact on single transformer RC EET-DCX.

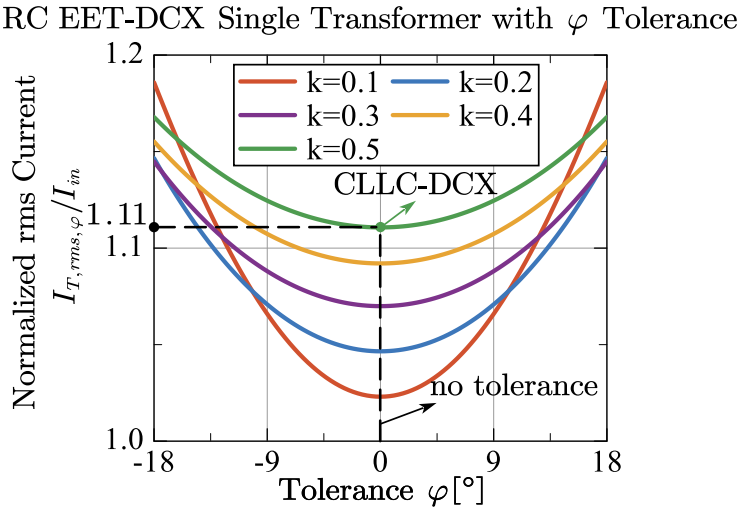


Fig. 3-46. Single transformer RC EET-DCX's normalized rms current with phase shift tolerance.

$$I_{in} = \text{average current} = \frac{2}{T_s}\int_{\frac{1}{2}kT_s}^{\frac{1+k}{2}T_s} i_{T,\varphi}(t)\cdot dt \tag{3.55}$$

From Eq. (3.54) and (3.55), the relationship between $I_{T,peak,\varphi}$, and I_{in} can be given as:

$$I_{T,peak,\varphi} = \frac{\pi}{(1-2k)\pi + 4k \cdot \cos\left(\frac{\varphi}{k} \cdot \pi\right)} \cdot I_{in} \tag{3.56}$$

Following the similar derivation without tolerance, the corresponding peak resonant voltage value $V_{rc,peak,\varphi}$ and rms current $I_{T,rms,\varphi}$ can be both revised as

$$V_{rc,peak,\varphi} = \frac{\pi^2}{k \cdot \left((1-2k)\pi + 4k \cdot \cos\left(\frac{\varphi}{k}\pi\right)\right)} \cdot f_s L_k I_{in} \tag{3.57}$$

$$I_{T,rms,\varphi} = \frac{\sqrt{1-k} \cdot \pi}{(1-2k)\pi + 4k \cdot \cos\left(\frac{\varphi}{k}\pi\right)} \cdot I_{in} \tag{3.58}$$

From Eq. (3.58), with the phase shift tolerance φ from -18 degree to +18 degree, **Fig. 3-46** depicts the normalized transformer current $I_{T,rms,\varphi}/I_{in}$ based on input dc current with different k. The black dashed line in **Fig. 3-46** shows the results with no tolerance (φ=0). When k=0.5, the RC EET-DCX transformer current will change from quasi-trapezoidal to pure sinusoidal current.

In conclusion, the tolerance on phase shift (defaulted to 90-degree) introduces a phase shift between terminal voltages $v_{pri(sec)}$ and transformer current $i_{T,\varphi}$, as shown in **Fig. 3-46**. As a result, circulating currents and reactive power are induced in the system due to this phase shift tolerance φ. When transferring the same real power, the presence of reactive power caused by the phase shift tolerance φ leads to an increase in transformer rms current compared to the scenario with no tolerance, as shown in **Fig. 3-46**.

4) Phase Shift Tolerance Impact on Transformer Parallel

When multiple transformers are paralleled to scale up the rating power, the current sharing performance can be analyzed using the phasor diagram, as shown in **Fig. 3-47**. In this diagram, the current i_{T1} branch represents no tolerance, while the current i_{T2} branch accounts for both L_k tolerance and phase shift tolerance. As discussed above, φ_m represents the equivalent phase shift tolerance caused by L_k tolerance. Due to the application of the same driving signals to both the primary and secondary side HV bridges, v_{pri} is in phase with v_{sec}. However, in the load-independent analysis conducted in Section II, v_{pri} is considered equal to nv_{sec} since the voltage drop on winding resistance was neglected. In the current sharing analysis, this voltage cannot be ignored, leading to the existence of the voltage v_{AB}, which also shares the same phase with $v_{pri(sec)}$. Consequently, Eq. (3.50) can be converted into vector form.

$$\overrightarrow{v_{AB}} = \overrightarrow{i_{T1}} \cdot r_{w1} = \overrightarrow{i_{T2}} \cdot r_{w2} + \overrightarrow{v_{rc2}} - j\omega L_k \cdot \overrightarrow{i_{T2}} \tag{3.59}$$

From Eq. (3.59), it is evident that branch i_{T1} (without tolerance) and branch i_{T2}(with tolerance) should have the same voltage drop v_{AB}, as shown in **Fig. 3-47**. Based on this geometric relationship, the current sharing relationship between i_{T1} and i_{T2} can be expressed as

$$\overrightarrow{i_{T2}} \cdot r_{w2} = \overrightarrow{i_{T1}} \cdot r_{w1} \cdot \cos(\varphi + \varphi_m) \tag{3.60}$$

To generalize Eq. (3.60) for N transformer paralleled, the current sharing can be given by

$$i_{T1} : \cdots : i_{TN} = \frac{1}{r_{w1}\cos(\varphi_1 + \varphi_{m1})} : \cdots : \frac{1}{r_{w2}\cos(\varphi_N + \varphi_{mN})} \tag{3.61}$$

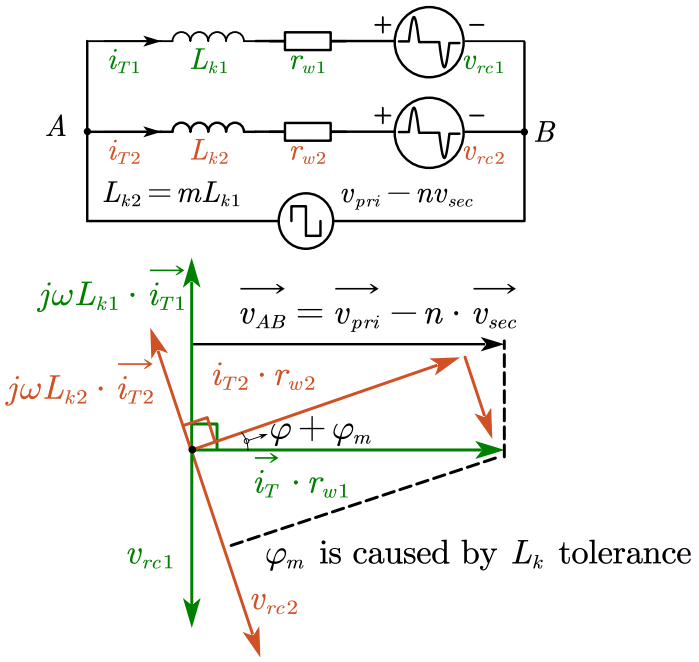


Fig. 3-47. Phasor diagram of the current sharing analysis with the phase shift tolerance.

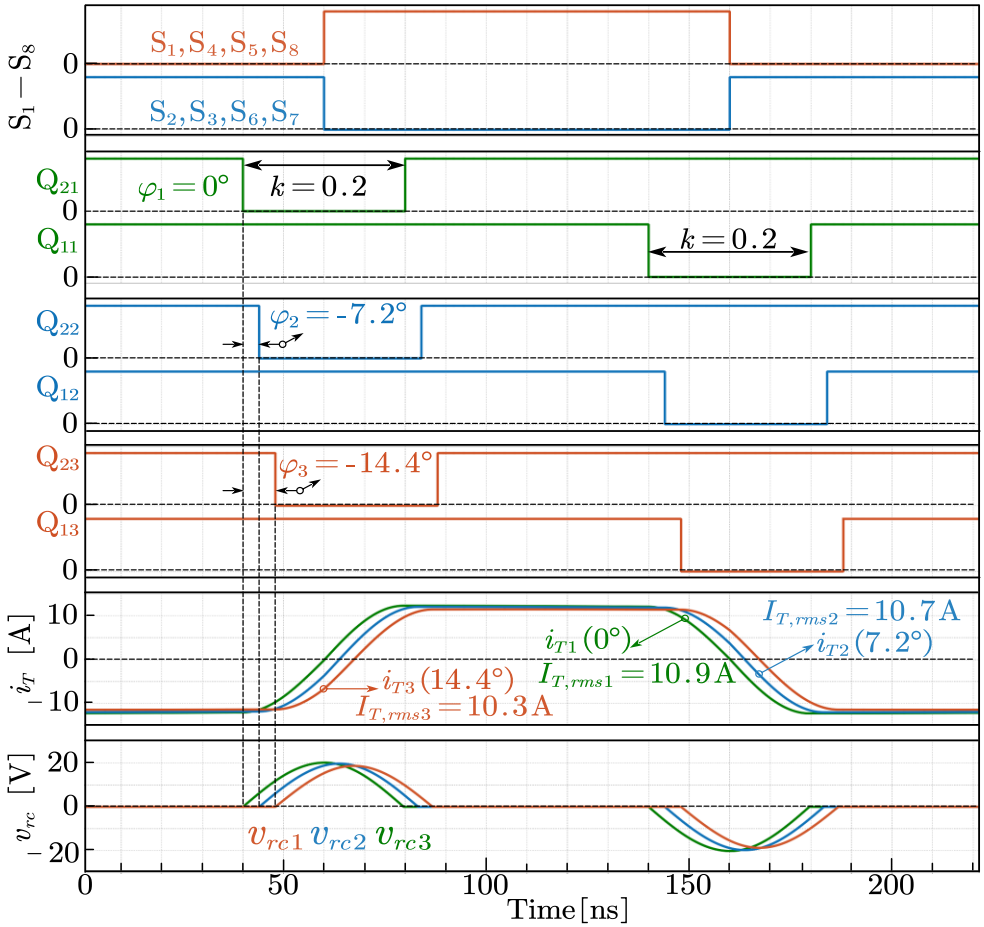


Fig. 3-48. Simulated current sharing results of the proposed RC EET-DCX with the tolerance on phase shift.

Where φ_{mN} can be found in Eq. (3.52). In the steady state, the transformer unit without the tolerance will take more current, and the current-sharing performance will be primarily determined by the total loop resistance r_w. The total loop resistance has a positive temperature coefficient and can be more easily controlled compared to inductance. Regarding the phase shift tolerance, for instance, if the phase difference is 14.4 degrees, the current difference will be only 3%. With the same parameters listed in **Table 3-6**, **Fig. 3-48** displays the simulated current sharing results considering the phase shift tolerance. Among the three paralleled branches, i_{T1}, i_{T2}, and i_{T3}, the phase shift tolerance is 0, -7.2, and -14.4 degrees, respectively. As there is no tolerance on L_k, all three currents can complete the current commutation during kT_s. A small phase difference is observed among these three currents in **Fig. 3-48**. However, the rms current for i_{T1}, i_{T2}, and i_{T3} are 10.9, 10.7, and 10.3 A, respectively, in accordance with the relationship from Eq. (3.61). In conclusion, the simulation results in **Fig. 3-48** demonstrate a good current sharing RC EET-DCX even with phase shift tolerance. It should be noted that the phase shift tolerance will have a similar impact on the current sharing performance of the typical EET-DCX.

3.4.6 Hardware and Implementation

1) Hardware Design for 12 kW RC EET-DCX

To verify the operation principle and advantages, two 12-kW DCX prototypes were built in this section, including the proposed RC EET-DCX and EET-DCX [26]. As shown in **Fig. 3-49(a)**, to achieve a fair comparison, both DCXs were based on the same platform, with two HV bridges shared between the two prototypes. To verify the current sharing performance, four RC EET/EET units are paralleled. As for the transformer part shown in **Fig. 3-49(b)**, the proposed RC EET unit has the same size and the same winding layout as the typical EET unit in [1]. All the parameters of the proposed 12 kW RC EET-DCX are listed in Table II. For the typical EET-DCX, the bidirectional switches $Q_{1(2)}$ in the RC EET unit are replaced by an LV full bridge. Both RC EET and EET units adopted the same 80 V GaN FETs *EPC 2029*. Additionally, the RC EET unit has sufficient space to accommodate measurement ports for $v_{ds,Q1}$ and $v_{ds,Q2}$, thanks to the reduced number of transistors and drivers.

It's important to highlight that both of these 12 kW DCXs shared the same Silicon Carbide (SiC) based HV bridges on the primary and secondary sides. The only distinction between the RC EET-DCX and the typical EET-DCX lies in the transformer unit part, as shown in **Fig. 3-49(b)**. As the total rating power is 12 kW with four transformer units paralleled, each unit is individually designed for 3 kW (300 V, 10 A). Based on the parameters of L_k and C_{o1}, the ideal value of k can be calculated as 0.22 using Eq. (3.36) and (3.37). However, to prevent any potential current commutation failure caused by L_k tolerance, a small margin will be incorporated. As a result, k should be slightly larger than 0.22, ensuring stable and reliable operation.

Table 3-6 PARAMETERS OF RC EET-DCX WITH FOUR EET UNITS

Variable	Value	Variable	Value
$V_{in(out)}$	300 V	$C_{o1(2)}$	22.7 nF
P	12 kW	f_s	200 kHz
L_k	620 nH	$L_{pri(sec)}$	15 μH
ER Core	ECW64A18	Core Material	DMR51
$C_{oss,pri(sec)}$	418 pF × 2	$C_{oss,LV}$	1310 pF
HV Bridge	C3M0016120k × 2	LV Q_1 and Q_2	EPC 2029

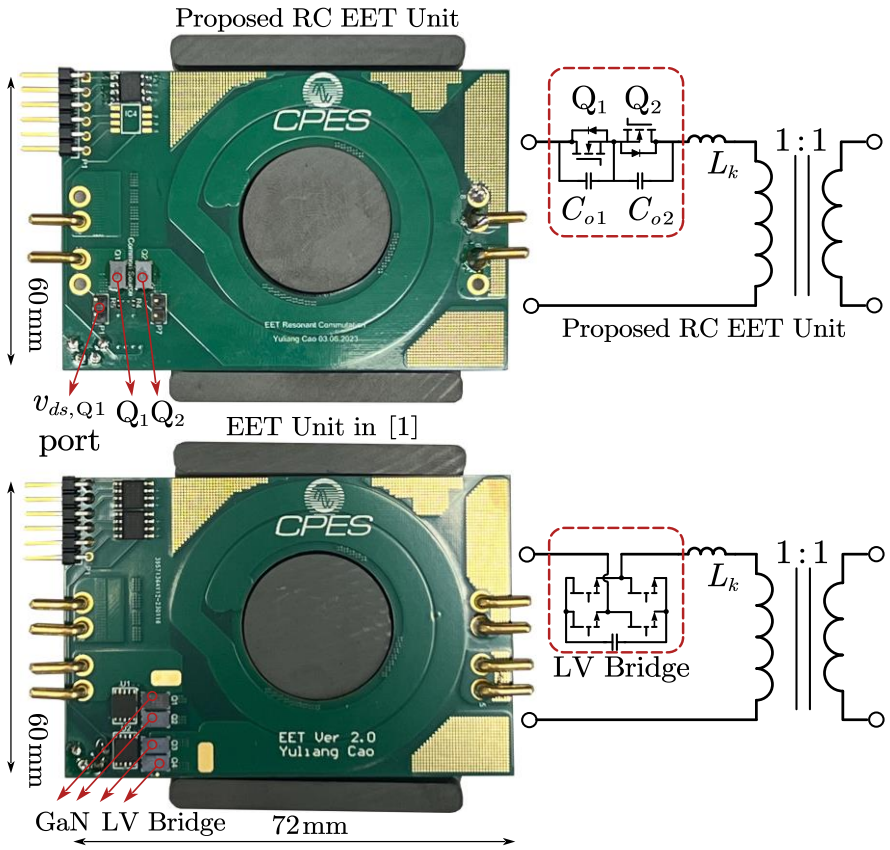


Fig. 3-49. A 12 kW DCX prototype with four configurable transformer units paralleled (a) whole converter, (b) detailed design of the proposed RC EET unit and EET unit.

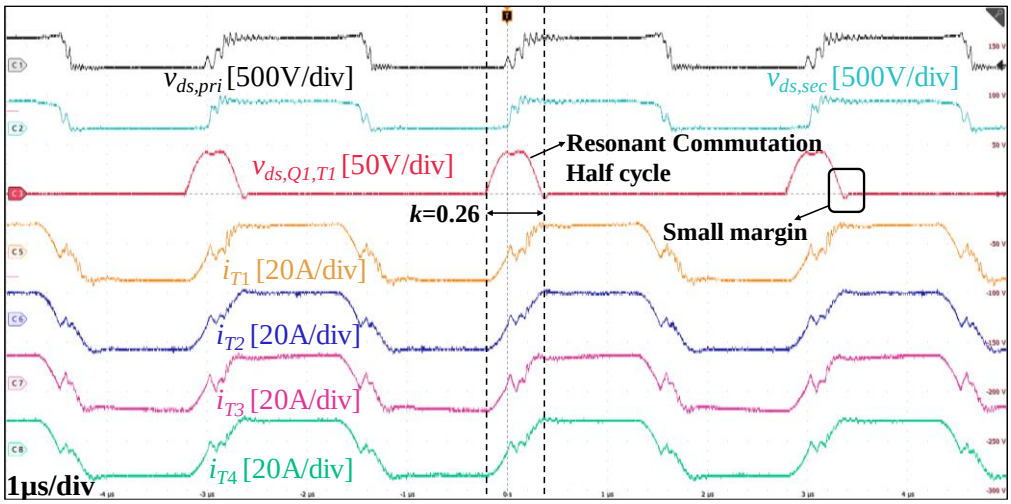
2) Experimental Results for RC EET-DCX

Fig. 3-50 presents the experimental results of the proposed RC EET-DCX under both full load (12 kW) and half load (6 kW) conditions. Considering the small margin left for k, the selected value is set to 0.26. In **Fig. 3-50(a)**, the full load results display the split currents $i_{T1\text{-}4}$, with the drain-to-source voltage $v_{ds,Q1,T1}$ of Q_1 on Transformer unit T_1 representing the half cycle of voltage v_c. The current commutation from the "negative plateau" to the "positive plateau" is achieved through a

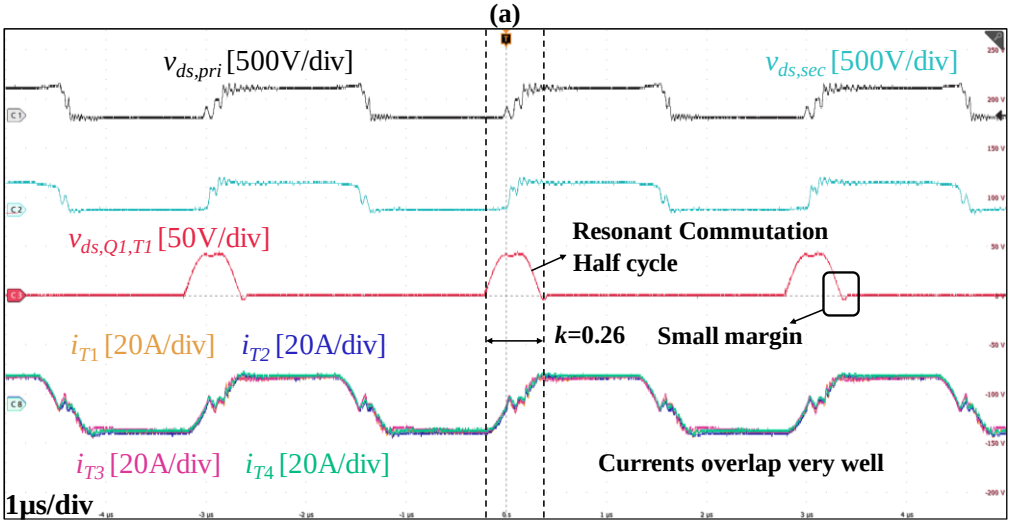
half-cycle resonance between L_k and C_{o1}. Similarly, the commutation from the "positive plateau" to the "negative plateau" is achieved through resonance between L_k and C_{o2} on the other half cycle. As the margin on k is small, the entire commutation process finishes a little earlier than the bidirectional switch turning on, resulting in a small voltage drop on $v_{ds,Q1,T1}$ after the current commutation. The transformer current subsequently goes through the body diode of the bidirectional switch before achieving ZVS. **Fig. 3-50(b)** shows all four transformer currents from **Fig. 3-50(a)** overlapped together, demonstrating excellent matching and verifying the current sharing performance of the proposed RC EET-DCX.

Furthermore, **Fig. 3-50(c)** and **(d)** display the half load (6 kW) results. As expected, with reduced load, the amplitude of resonant voltage $v_{ds,Q1,T1}$, and all transformer currents $i_{T1\text{-}4}$ are halved, consistent with Eq. (3.45) and (3.48). These equations predict that the peak voltage of $v_{ds,Q1,T1}$, and peak current of $i_{T1\text{-}4}$ should be proportional to the input dc current I_{in}, leading to a halved value when transferring half the power.

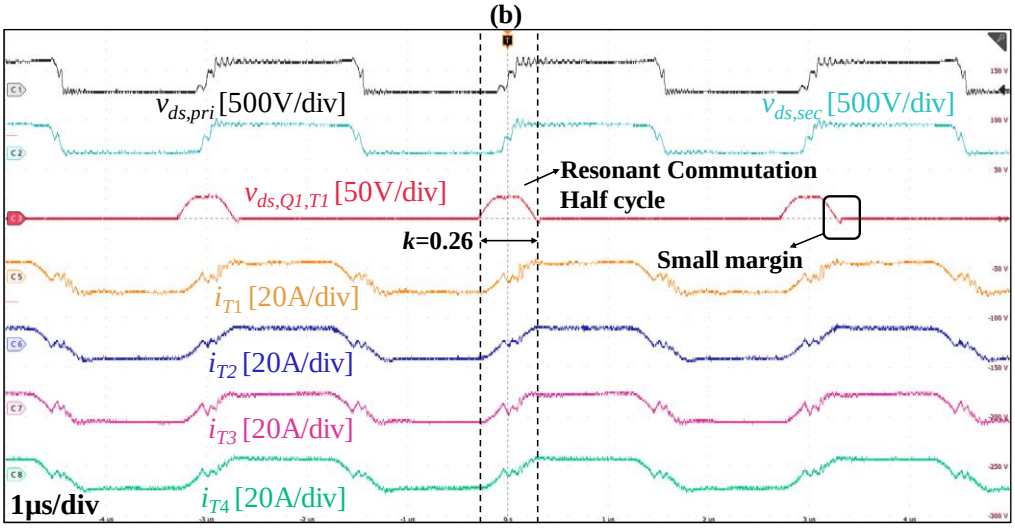
Fig. 3-51 illustrates two additional cases with different k values. In **Fig. 3-51(a)** and **(b)**, the "no margin" case has k=0.22. Under both full load and half load conditions, the resonant current commutation precisely finishes when the bidirectional LV switch turns on. As a result, no current passes through the body diodes of Q_1 or Q_2, and thus, there is no voltage drop after the current commutation.


$v_{ds,pri}$ [500V/div]
$v_{ds,sec}$ [500V/div]
$v_{ds,Q1,T1}$ [50V/div]
Resonant Commutation
Half cycle
k=0.26
Small margin
i_{T1} [20A/div]
i_{T2} [20A/div]
i_{T3} [20A/div]
i_{T4} [20A/div]
1µs/div

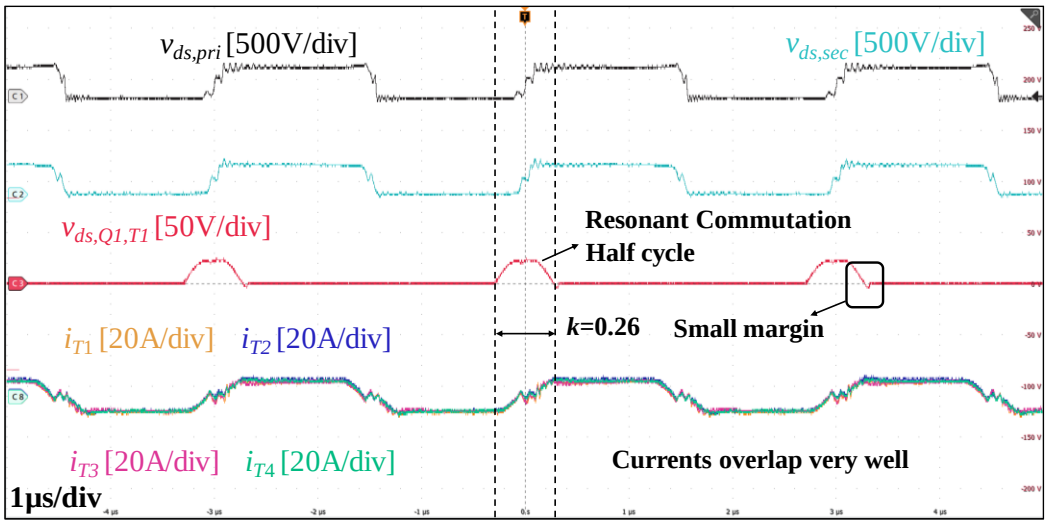
(a)


$v_{ds,pri}$ [500V/div]
$v_{ds,sec}$ [500V/div]
$v_{ds,Q1,T1}$ [50V/div]
Resonant Commutation
Half cycle
k=0.26
Small margin
i_{T1} [20A/div]
i_{T2} [20A/div]
i_{T3} [20A/div]
i_{T4} [20A/div]
Currents overlap very well
1µs/div

(b)


$v_{ds,pri}$ [500V/div]
$v_{ds,sec}$ [500V/div]
$v_{ds,Q1,T1}$ [50V/div]
Resonant Commutation
Half cycle
k=0.26
Small margin
i_{T1} [20A/div]
i_{T2} [20A/div]
i_{T3} [20A/div]
i_{T4} [20A/div]
1µs/div

(c)



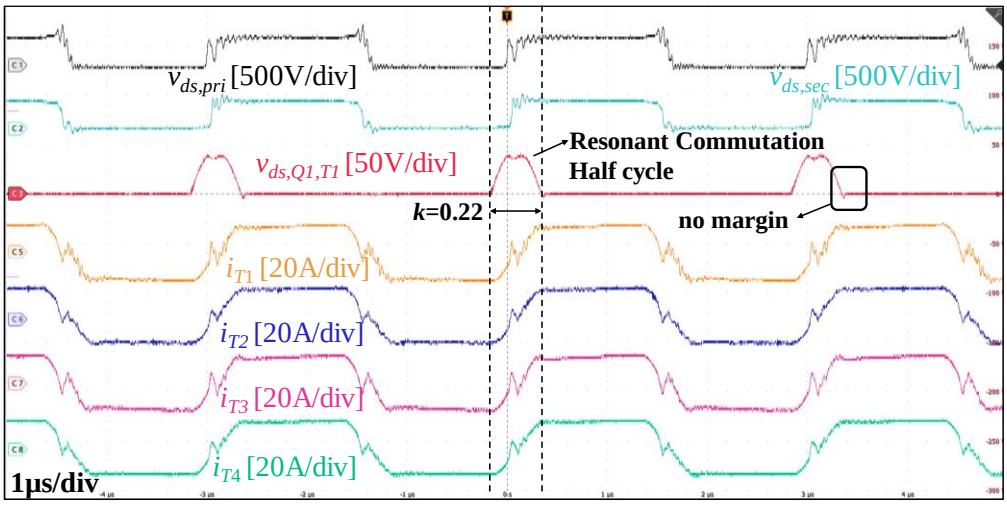
(d)

Fig. 3-50. The experimental results of RC EET-DCX with four paralleled transformers (*k*=0.26 to give a small margin for current commutation): (a) 12 kW full load with split current, (b) 12 kW full load with overlapped current, (c) 6 kW half load with split current, (d) 6 kW half load with overlapped current.

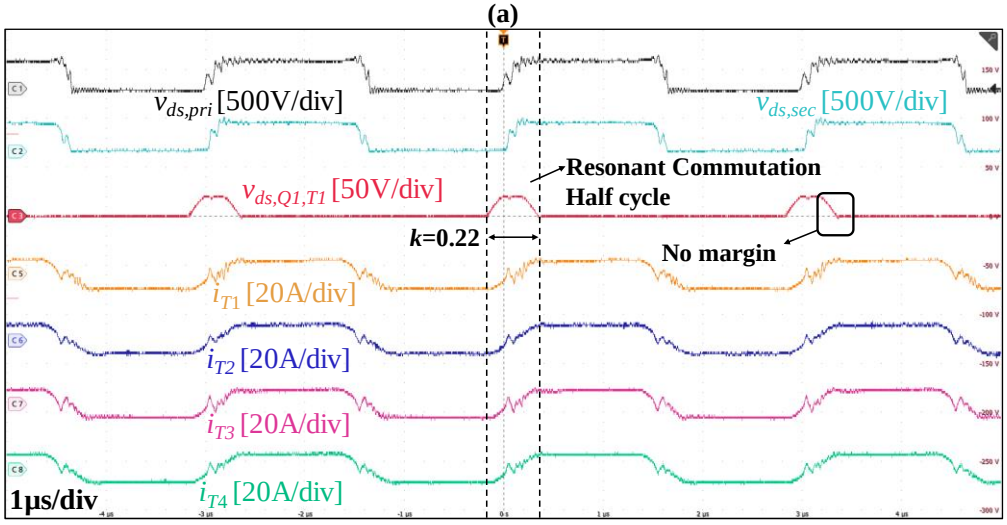
However, this scenario is more sensitive to the L_k tolerance, as a larger L_k could cause the current commutation failure, leading to a loss of ZVS in bidirectional switches Q_1 and Q_2.

In contrast, **Fig. 3-51(c)** and **(d)** depict the "large margin" case with k=0.30. Compared to the k=0.26 case in **Fig. 3-50**, a longer time for voltage drop is observed after the current commutation. This is due to the transformer current passing through the body diodes of Q_1 and Q_2 for a longer time.

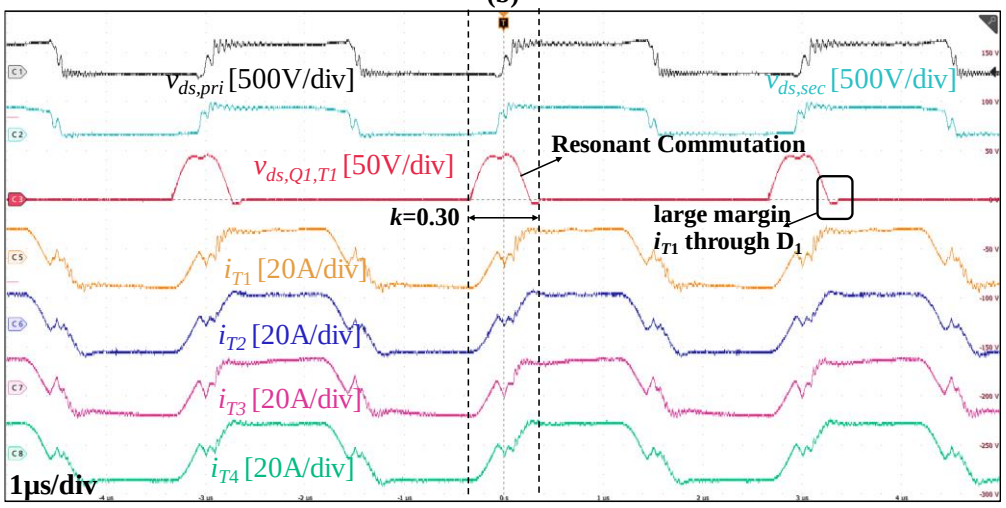
To summarize, the selection of k involves a trade-off. A "no margin" approach (smallest k) offers efficiency benefits as no current passes through the body diodes. However, it becomes more sensitive to L_k tolerance, especially with a larger L_k value. In practice, a small margin is usually given, and the final selected k is slightly larger than the calculated value, depending on the actual tolerance situation.


$v_{ds,pri}$ [500V/div]
$v_{ds,sec}$ [500V/div]
$v_{ds,Q1,T1}$ [50V/div]
Resonant Commutation
Half cycle
k=0.22
no margin
i_{T1} [20A/div]
i_{T2} [20A/div]
i_{T3} [20A/div]
i_{T4} [20A/div]
1µs/div

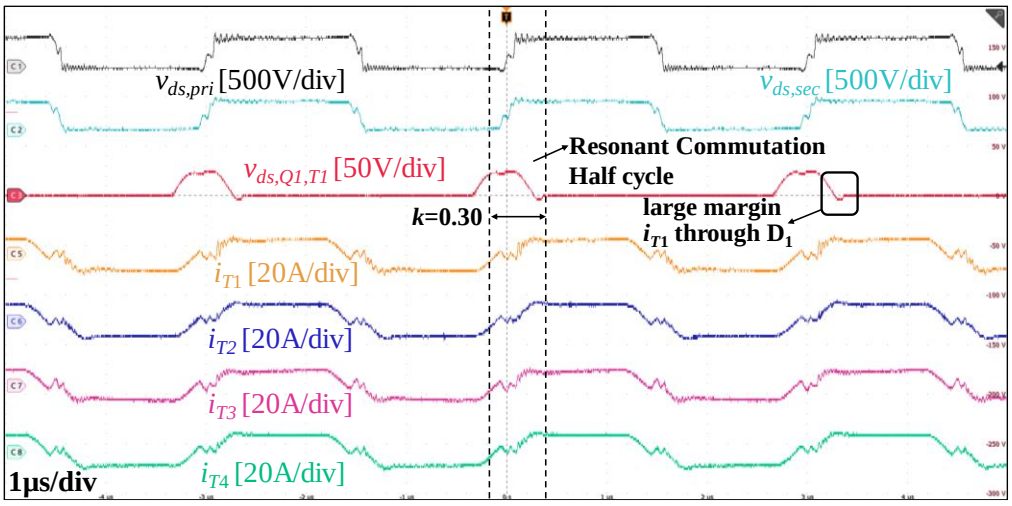
(a)


$v_{ds,pri}$ [500V/div]
$v_{ds,sec}$ [500V/div]
$v_{ds,Q1,T1}$ [50V/div]
Resonant Commutation
Half cycle
k=0.22
No margin
i_{T1} [20A/div]
i_{T2} [20A/div]
i_{T3} [20A/div]
i_{T4} [20A/div]
1µs/div

(b)


$v_{ds,pri}$ [500V/div]
$v_{ds,sec}$ [500V/div]
$v_{ds,Q1,T1}$ [50V/div]
Resonant Commutation
k=0.30
large margin
i_{T1} through D_1
i_{T1} [20A/div]
i_{T2} [20A/div]
i_{T3} [20A/div]
i_{T4} [20A/div]
1µs/div

(c)



(d)

Fig. 3-51. The experimental results of RC EET-DCX with no margin (*k*=0.22) and large margin (*k*=0.30) design (a) 12 kW full load with no margin *k*=0.22, (b) 6 kW half load with no margin *k*=0.22, (c) 12 kW full load with large margin *k*=0.30, (d) 6 kW half load with large margin *k*=0.30.

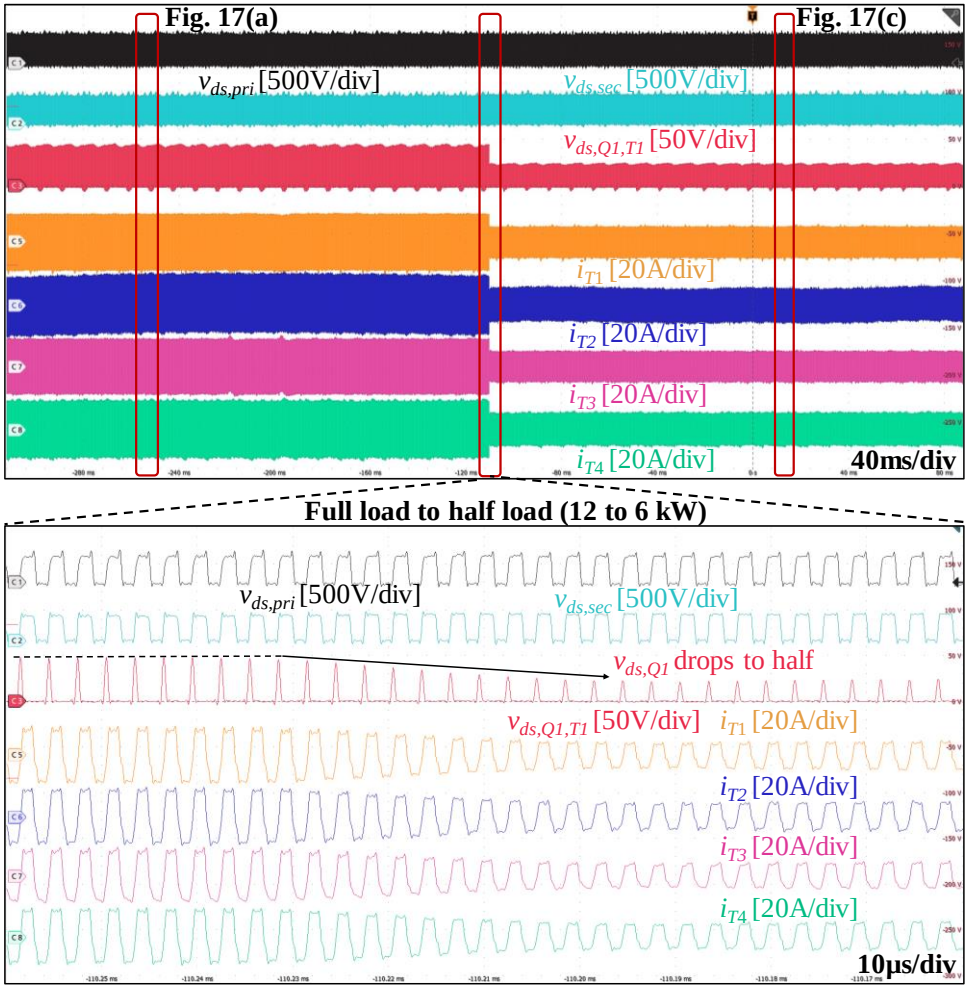


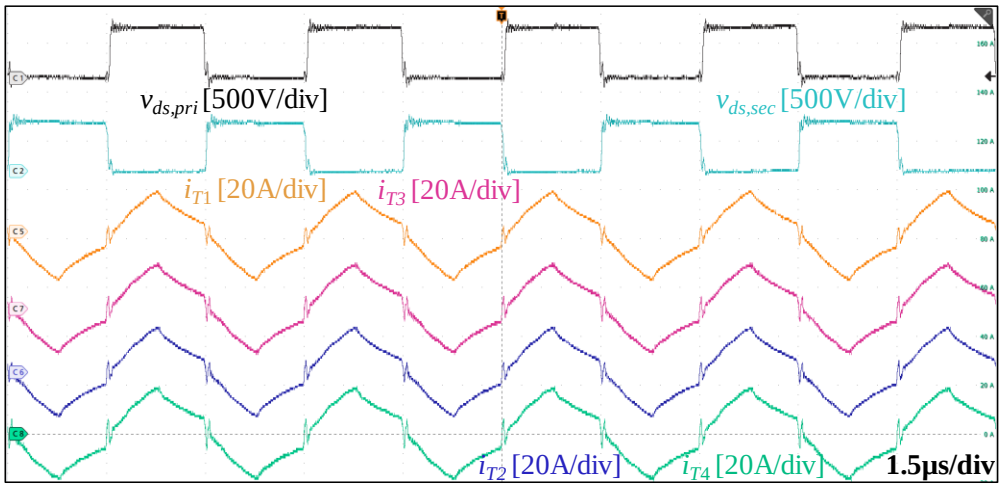
Fig. 3-52. Load changing results of the proposed 12 kW RC EET-DCX from 12 kW to 6 kW.

Fig. 3-52 shows the load-changing test results with a smaller margin (k=0.26). The detailed steady-state waveforms for full load and half load are found in **Fig. 3-50(a)** and **(c)**, respectively, while the zoomed-in load transient waveforms are provided on the bottom. When the load suddenly changes from full load to half load, the amplitudes of the resonant voltage $v_{ds,Q1,T1}$, and all four currents gradually reduce to half in about 6 cycles. The current sharing performance of the proposed RC EET-DCX remains good during the load transient period.

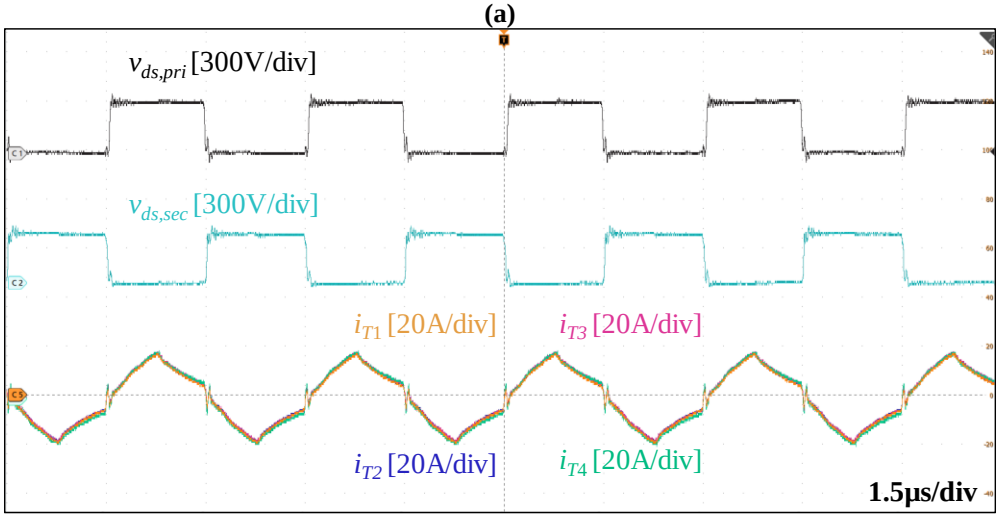
3) Experimental Results for Typical EET-DCX

To ensure a fair comparison with the proposed RC EET-DCX, a 12-kW EET-DCX prototype was also built based on the transformer unit shown in **Fig. 3-49(b)**. More details about the operation principle of the EET-DCX can be found in [26]. With an integrated LV full bridge, the current waveform for EET-DCX is a triangle, as shown in **Fig. 3-53**.

Fig. 3-53(a) depicts the 12-kW full load split current results for the EET-DCX. Upon overlapping the four EET units, as shown in **Fig. 3-53(b)**, the excellent current sharing performance can also be verified. However, in comparison to the quasi-trapezoidal current in the RC EET-DCX, the triangular current in the EET-DCX has a larger rms current, leading to higher total conduction loss. Additionally, despite achieving ZVS turn-on in both the RC EET-DCX and EET-DCX, the former also leads to smaller turn-off switching losses.



(a)



(b)

Fig. 3-53. The full load 12 kW experimental results of the typical EET-DCX with (a) split current and (b) overlapped current.

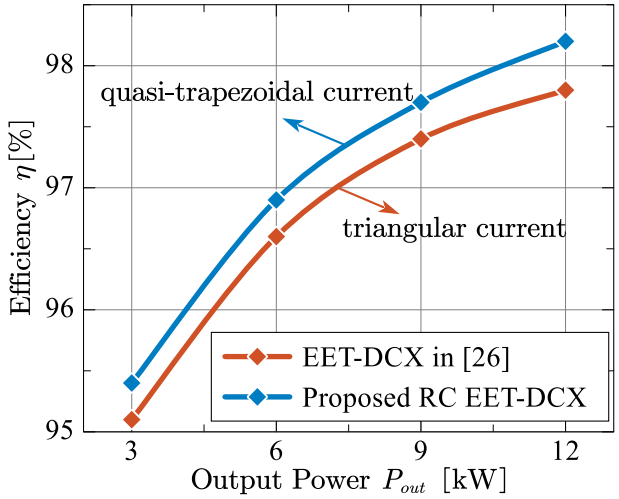


Fig. 3-54. The measured efficiency of *EET-DCX II* with different output power.

4) Efficiency Measurement

Fig. 3-54 shows the efficiency results for both the proposed RC EET-DCX and the typical EET-DCX. Based on previous analysis, the triangular current waveform in EET-DCX exhibits a higher rms current compared to the quasi-trapezoidal current in RC EET-DCX. It is crucial to emphasize that this reduction in conduction loss is not limited to just the transformer windings but also extends to encompass the conduction loss of the HV bridge. As a result, when compared to the typical EET-DCX, the proposed RC EET-DCX demonstrates higher overall efficiency (reaching 98.4% at 12 kW) across the entire load range. This efficiency advantage proves to be particularly beneficial in high-current, high-power applications, as the additional loss on the LV bridge becomes less significant in comparison.

3.5 Hybrid EET-DCX, A New Family of Soft-switching DCX

By incorporating an integrated low voltage (LV) full bridge, the concept of an electronic-embedded transformer (EET) offers a straightforward means of achieving high-frequency, high-power fixed-gain isolated DC-DC conversion, known as a DC transformer (DCX) through parallel operation of EET units with natural current sharing [26]. Besides, the trapezoidal current modulation in [56] can further reduce the root mean square (rms) current through the transformer. However, the trapezoidal current modulation will increase the voltage stress on the low-voltage full bridge, especially when the leakage inductance is large and variable, such as in the high-power wireless charging application. To break this trade-off, this paper proposes an EET-based soft-switching DCX family, as shown in **Fig. 3-55**. Based on EET-DCX, hybrid EET-DCX was first proposed by adding a series of resonant capacitors, as shown in **Fig. 3-55**. Since a large portion of the leakage inductance L_k impedance can be canceled by this resonant capacitor, the voltage stress on the LV bridge will reduce dramatically. The same trapezoidal current modulation in typical EET-DCX [56] can be directly adopted, and the transformer current in this hybrid EET-DCX will change to a quasi-trapezoidal waveform due to the resonance between the resonant capacitor and leakage inductance. With the additional design freedom of a series resonant capacitor, a more flexible parameter design can be conducted with desirable rms current and GaN FET voltage stress. Based on RC EET-DCX in the last section, an extra series resonant capacitor can also be adopted. Therefore, another hybrid resonant commutation (RC) EET-DCX was proposed in **Fig. 3-55**. Compared with typical hybrid EET-DCX in **Fig. 3-55**, the switch number and conduction loss can be reduced. At the same time, this hybrid RC EET-DCX can retain the merits of the typical hybrid EET-DCX, such as the small stress voltage, low rms current, good current sharing performance, and full load range zero voltage switching (ZVS).

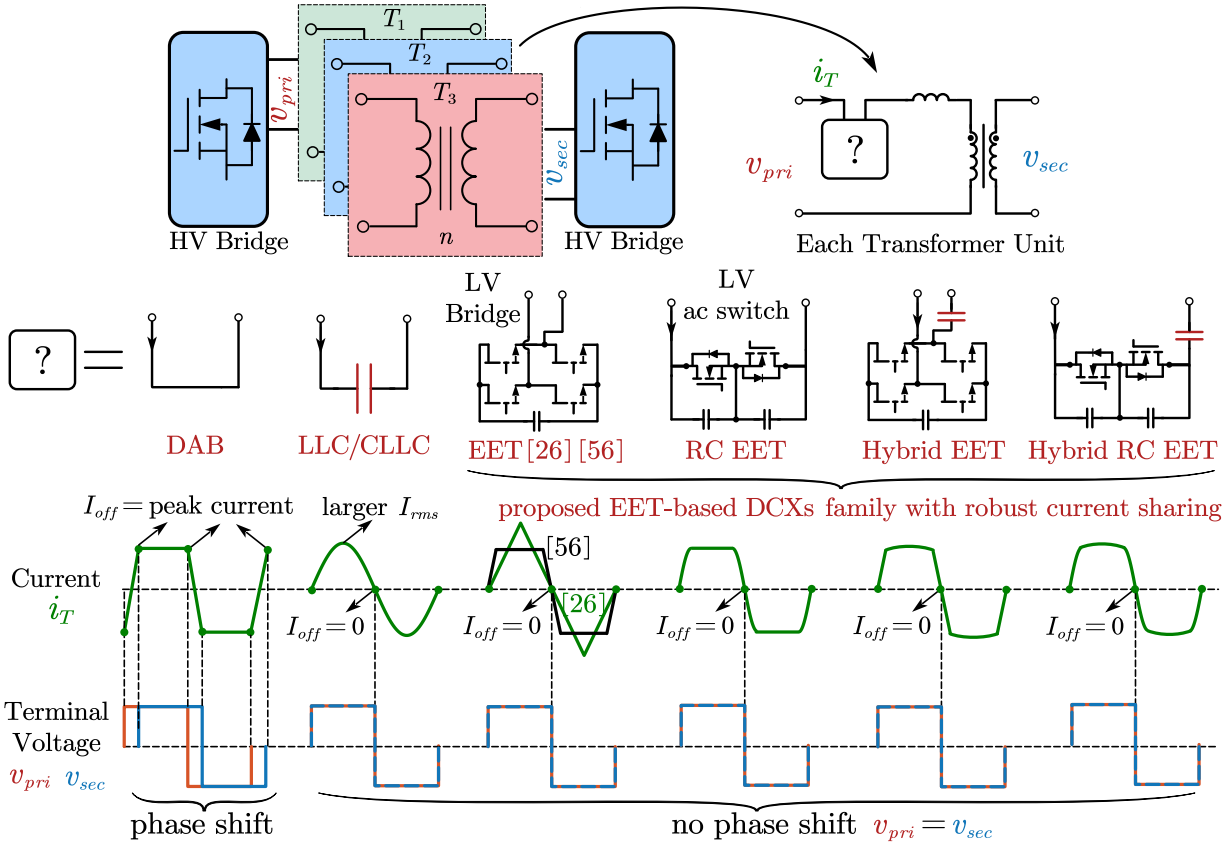


Fig. 3-55. Scalable DCX structure with different topologies, including proposed EET-DCXs family.

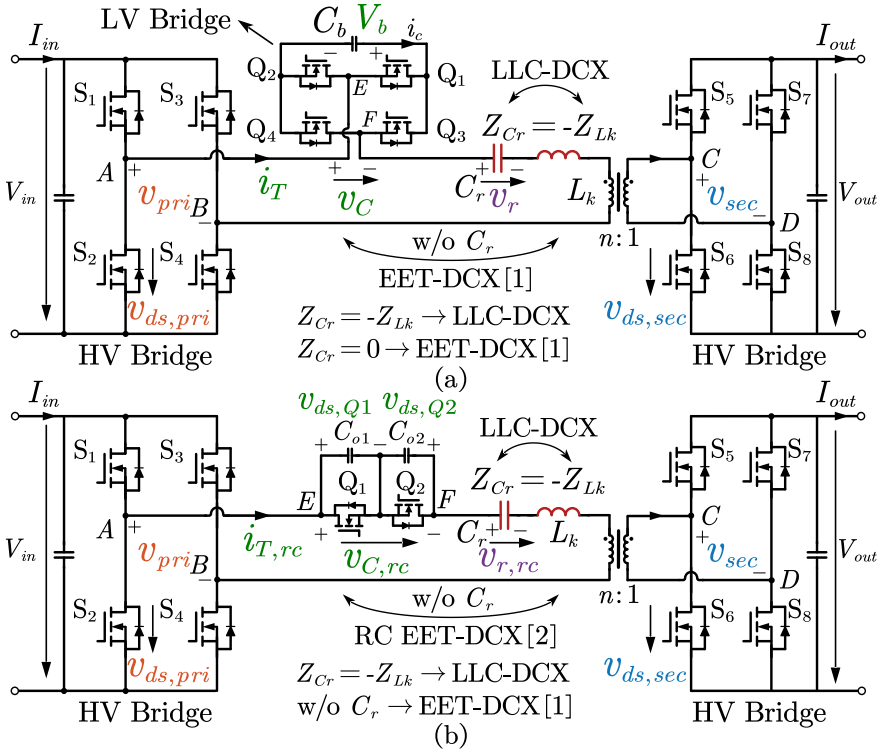


Fig. 3-56. Proposed two resonant-type hybrid topologies: (a) hybrid EET-DCX and (b) hybrid RC EET-DCX.

To sum up, a comprehensive study of these two hybrid topologies will be given in this paper, including the operation principle, time-domain model, quantitative parameter analysis, and current sharing performance. Both typical LLC/CLLC-DCX and non-resonant EET-DCX can be seen as a certain case of resonant-type EET-DCX, which means the proposed hybrid resonant-type EET-DCXs can be a "broad" bridge between LLC-DCX and EET-DCX.

3.5.1 Circuit Diagram and Definitions

Detailed circuit diagrams for hybrid EET-DCX and hybrid RC EET-DCX are depicted in **Fig. 3-56**. **Fig. 3-56(a)** illustrates the circuit diagram of the proposed hybrid EET-DCX with a single hybrid EET unit. Similar to the typical EET-DCX, the configuration comprises two HV bridges and one LV bridge integrated within a n:1 transformer. The only difference is that an extra resonant capacitor was connected in series with the LV bridge, as shown in **Fig. 3-56(a)**. After replacing the LV bridge with a bidirectional AC switch, **Fig. 3-56(b)** represented another resonant-type DCX—hybrid RC EET-DCX. For a simple explanation, these two circuit diagrams share most of the denotations, such as the input and output voltages V_{in} and V_{out}, input and output currents I_{in} and I_{out}. In addition, v_{pri} and v_{sec} correspond to the output voltages of the two HV bridges. L_k represents the leakage inductance of the transformer, while i_T represents the current flowing through the transformer. The magnetizing inductance is disregarded in this context as it exclusively pertains to the HV bridges' ZVS and is unrelated to the LV bridge's ZVS. Further details regarding the ZVS implementation of the HV bridges can be found in [26] and [56].

The only difference between these two topologies in **Fig. 3-56**is the series LV bridge or series bidirectional AC switch. In hybrid EET-DCX, the floating DC voltage across C_b is denoted as V_b, and its amplitude will be further discussed and derived in subsequent sections. Furthermore, v_C indicates the LV bridge's output voltage with an amplitude equivalent to V_b. As for another

proposed hybrid RC EET-DCX in **Fig. 3-56(b)**, the entire LV bridge displayed in **Fig. 3-56(a)** is substituted with only one bidirectional AC switch $Q_{1(2)}$. C_{o1} and C_{o2} are two symmetric parallel capacitors.

$$C_{o1} = C_{o2} \tag{3.62}$$

Depending on the practical application, C_{o1} and C_{o2} can be the transistor's inherent parasitic capacitors or externally added components. $v_{ds,Q1}$ and $v_{ds,Q2}$ are two drain-to-source voltages across Q_1 and Q_2. $v_{C,rc}$ is the output resonant voltage across points *E* and *F*, and its peak value is $V_{b,rc}$.

Considering both configurations in **Fig. 3-56**, two HV bridges can be simplified as two synchronized square voltage sources with a 50% duty cycle. It is important to mention that this modulation technique has been extensively discussed in [26]. In the steady state, the relationship between V_{in} and V_{out}, I_{in} and I_{out}, as well as v_{pri} and v_{sec} can be directly determined based on the aforementioned analysis.

$$V_{in} = n \cdot V_{out},\ I_{in} = I_{out}/n,\ v_{pri} = n \cdot v_{sec} \tag{3.63}$$

Based on Eq. (3.61), if without series resonant capacitor C_r, it can be observed that when v_{pri} equals v_{sec}, only the voltage source v_C (LV bridge) or $v_{C,rc}$ (bidirectional ac switch) will be utilized to drive L_k, resulting in the generation of a triangular or trapezoidal current waveform as shown in **Fig. 3-55**. In the next two Sections, the operation principle of hybrid EET-DCX and hybrid RC EET-DCX will be illustrated, respectively. Afterward, a comprehensive comparison between these two topologies will also be given. The magnetizing inductance of the transformer was ignored in this paper because a more detailed discussion can be found in [26].

3.5.2 Hybrid EET-DCX

1) Traditional EET-DCX with Trapezoidal Current

Fig. 3-57 represents the operation principle of hybrid EET-DCX, and **Fig. 3-58** plots the normalized transformer current i_T/I_{in}. As shown in **Fig. 3-57(a)**, the LV bridge $Q_{1\text{-}4}$ can generate a square waveform v_c with duty k. The range of k is from 0 to 0.5. The trapezoidal current modulation in [56] can be directly adopted to this hybrid EET-DCX. Following the operation principle in [56], **Fig. 3-57(b)** first shows the f_r=0 case (without C_r) with the corresponding gating signals for both the HV and LV bridge switches S_1-S_8, Q_1-Q_4. To realize a trapezoidal current, a zero-voltage stage (Q_1, Q_3 ON or Q_2, Q_4 ON) needs to be introduced to v_C, creating a "current plateau" as illustrated in **Fig. 3-57(b)**. This plateau can be achieved by introducing a phase shift of kT_s between the phase legs Q_1, Q_2, Q3, and Q_4. In [26] and [56], the voltage stress V_b and transformer rms current $I_{T,rms}$ can be derived as

$$V_b = \frac{2 \cdot f_s \cdot L_k}{(1-k) \cdot k} \cdot I_{in} \quad (0 < k \leq 0.5,\ f_r = 0) \tag{3.64}$$

$$I_{T,rms} = \frac{1}{1-k} \cdot \sqrt{\frac{3-4 \cdot k}{3}} \cdot I_{in} \quad (0 < k \leq 0.5,\ f_r = 0) \tag{3.65}$$

From Eq. (3.64), the voltage V_b is proportional to the transformer leakage inductance L_k. If L_k is difficult to control, such as in wireless power transfer or high voltage applications with insulation requirements, the voltage stress V_b across the LV bridge will be very high. On the other hand, there is an intrinsic trade-off between rms current and voltage stress V_b from Eq. (3.64) and (3.65). As shown in **Fig. 3-58(a)**, when k is closer to 0, the transformer current will be more like a square waveform with a smaller rms value. However, a smaller k will cause a higher voltage V_b across the LV bridge.

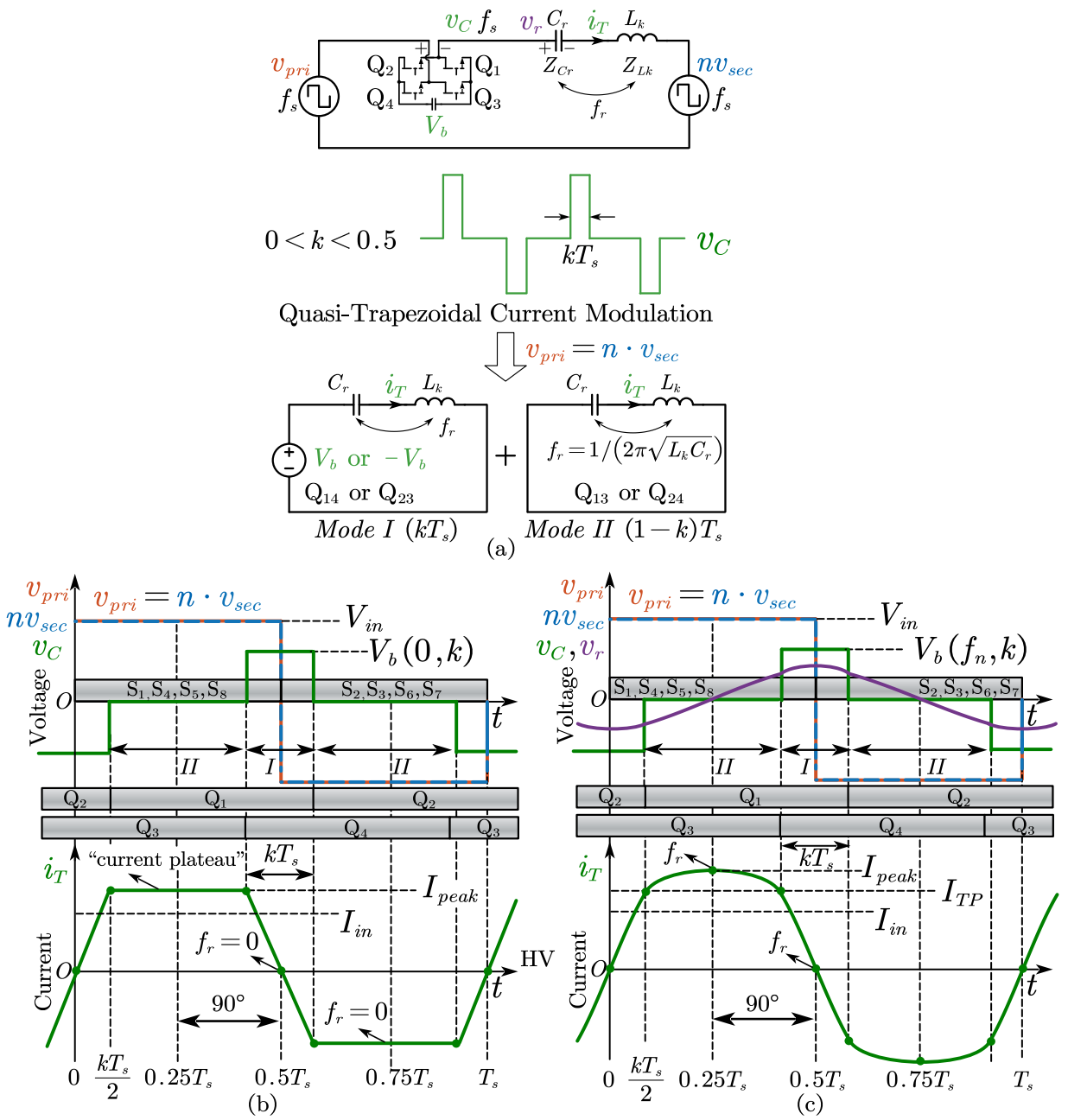


Fig. 3-57. (a) simplified hybrid EET-DCX circuit and related v_C waveforms. (b) typical EET-DCX without C_r (f_n=0) in [26] and [56], (c) Proposed resonant-type hybrid EET-DCX (f_n≠0).

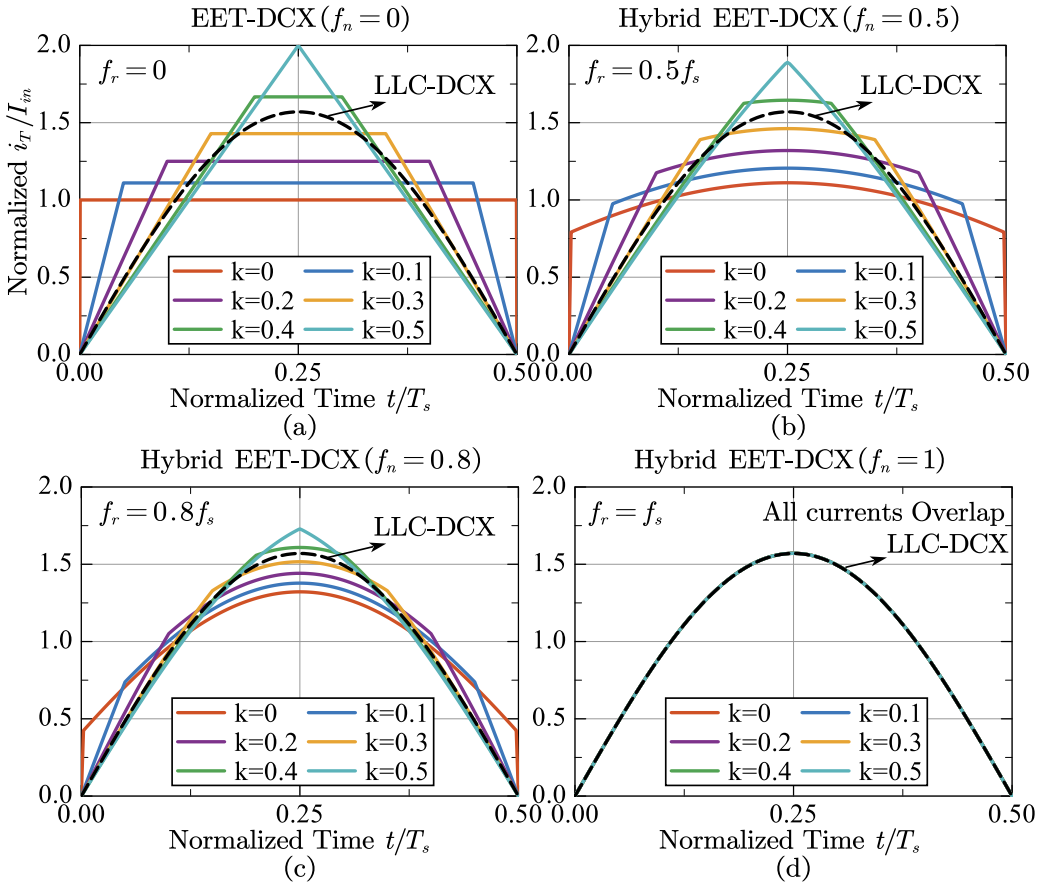


Fig. 3-58. Normalized transformer current i_T/I_{in} with different k and different f_n: (a) f_n=0, (b) f_n=0.5, (c) f_n=0.8, and (d) f_n=1.

2) Operation Principle with Resonant Capacitor C_r

To address this inherent trade-off, a resonant capacitor C_r was connected in series, as shown in **Fig. 3-57 (a)**. Due to the resonance between L_k and C_r, the resonant frequency f_r can be given as

$$f_r = 1/\left(2\pi\sqrt{L_k C_r}\right) \tag{3.66}$$

For the simple explanation, f_r can be normalized as f_n based on switching frequency f_s.

$$f_n = f_r/f_s \tag{3.67}$$

After adding C_r, two modes can be found in **Fig. 3-57(c)** during one period from 0 to $0.5T_s$. *Mode I* is from 0 to $0.5kT_s$ and $(0.5\text{-}0.5k)T_s$ to $0.5T_s$, and *Mode II* is from $0.5kT_s$ to $(0.5\text{-}0.5k)T_s$. The equivalent circuits for these two modes are plotted in **Fig. 3-57(a)**.

Mode I: voltage excitation with V_b or $-V_b$.

Mode II: Voltage excitation is 0 because of the LV bridge's short circuit.

The piecewise time-domain expression for the transformer current $i_T(t)$ can be given as

$$i_T(t)=\begin{cases} I_a\cdot\sin(2\pi f_r\cdot t) & t\in\left[0,\frac{k}{2}\right)T_s \\ I_{peak}\cdot\cos\left(2\pi f_r\cdot\left(t-\frac{1}{4}T_s\right)\right) & t\in\left[\frac{k}{2},\frac{1-k}{2}\right]T_s \\ -I_a\cdot\sin\left(2\pi f_r\cdot\left(t-\frac{1}{2}T_s\right)\right) & t\in\left(\frac{1-k}{2},\frac{1}{2}\right]T_s \end{cases} \tag{3.68}$$

Where I_{peak} is the peak transformer current in **Fig. 3-57(c)**, and I_a is an auxiliary variable. Different from the trapezoidal current without resonance in **Fig. 3-57(b)**, the quasi-trapezoidal current i_T in **Fig. 3-57(c)** has a turn point current I_{TP}. From Eq. (3.68), the relationship between I_{TP} and I_a can be given as follows.

$$I_{TP}=I_a\cdot\sin\left(2\pi f_r\cdot\frac{k}{2}T_s\right)=I_a\cdot\sin(\pi f_n\cdot k) \tag{3.69}$$

On the other hand, due to the continuity of the current i_T, I_{TP} can be expressed from Eq. (3.68) as

$$I_{TP}=I_{peak}\cdot\cos\left(2\pi f_r\cdot\frac{k-0.5}{2}T_s\right)=I_{peak}\cdot\cos(\pi f_n\cdot(k-0.5)) \tag{3.70}$$

From Eq. (3.69) and (3.70), the relationship between I_a and I_{peak} can be given as

$$I_a \cdot \sin(\pi f_n \cdot k) = I_{peak} \cdot \cos(\pi f_n \cdot (k - 0.5)) \quad k \in (0, 0.5] \tag{3.71}$$

On the other hand, input DC current Iin equals the average value of current i_T.

$$I_{in} = \text{average current} = \frac{2}{T_s}\int_0^{\frac{T_s}{2}} i_T(t) \cdot dt \tag{3.72}$$

From Eq. (3.71) and (3.72), I_{peak} and I_a can be derived as

$$I_{peak}(k, f_n) = \frac{\left(\frac{\pi}{2} f_n\right) \cdot \sin(\pi f_n \cdot k)}{\cos\left(\frac{\pi}{2} f_n \cdot (1 - 2k)\right) - \cos\left(\frac{\pi}{2} f_n\right)} \cdot I_{in} \tag{3.73}$$

$$I_a(k, f_n) = \frac{\left(\frac{\pi}{2} f_n\right) \cdot \cos(\pi f_n \cdot (k - 0.5))}{\cos\left(\frac{\pi}{2} f_n \cdot (1 - 2k)\right) - \cos\left(\frac{\pi}{2} f_n\right)} \cdot I_{in} \tag{3.74}$$

After obtaining the I_{peak} and I_a, according to Eq. (3.68), **Fig. 3-58** plotted the time-domain normalized transformer current $i_T(t)/I_{in}$ with different k and different f_n. **Fig. 3-58(a)-(d)** represents the cases when f_n=0, 0.5, 0.8 and 1, respectively. The normalized switching frequency f_n cannot exceed "1" because the branch impedance should remain inductive to guarantee the previous EET-DCX operation principle.

Fig. 3-58(a) shows the traditional trapezoidal current EET-DCX without C_r. If C_r is added to f_n=0.5, as shown in **Fig. 3-58(b)**, the "current plateau" in **Fig. 3-58(a)** will become curved based on the previous analysis. If C_r keeps increasing to f_r=0.8f_s (f_n=0.8), the current will become more curved,

as shown in **Fig. 3-58(c)**. Finally, if C_r is increased to $f_r=f_s$ (f_n=1), as shown in **Fig. 3-58(d)**, the L_k impedance has been fully canceled by C_r. In this scenario, no matter how k changes, the current i_T always coincides with the sinusoidal current LLC-DCX.

To sum up, hybrid EET-DCX is an intermediate form of traditional EET-DCX and traditional LLC-DCX, which is proposed to address the trade-off between the LV bridge voltage stress (Eq. (3.64)) and the transformer rms current (Eq. (3.65)) in traditional EET-DCX.

The voltage V_b with C_r can be derived first according to the current continuity. As shown in **Fig. 3-57(c)**, at the turn-point when t=0.5kT_s, the current change rate will jump abruptly because of the short circuit on the LV bridge. Therefore, V_b can be derived from the different di/dt on either side of the turning point.

$$V_b(k,f_n)=\frac{4\cdot\left(\frac{\pi}{2}f_n\right)^2\cdot\cos\left(\frac{\pi}{2}f_n\right)}{\cos\left(\frac{\pi}{2}f_n(1-2k)\right)-\cos\left(\frac{\pi}{2}f_n\right)}f_sL_kI_{in} \tag{3.75}$$

Subsequently, the transformer rms current I_{rms} can be derived as

$$I_{rms}(k,f_n)=\frac{1}{T_s}\sqrt{\int_0^{T_s}{i_T}^2(t)\,dt} \tag{3.76}$$

According to Eq. (3.75) and (3.76), with different k and f_n, **Fig. 3-59(a)** and **(b)** plot the normalized transformer current I_{rms}/I_{in} and normalized LV bridge voltage $V_b/V_b(0.5,0)$, respectively. The base voltage $V_b(0.5,0)$ is the voltage stress across typical EET-DCX in [26] when k=0.5, f_n=0. From Eq. (3.64), $V_b(0.5,0)$ is equal to $8f_sL_kI_{in}$. In **Fig. 3-59(a)** and **(b)**, typical EET-DCX with both triangles (k=0.5) [26] and trapezoidal current (0<k<0.5) [56] can be found when f_n=0. For a simple

explanation, five representative points "*A* (0.1, 1)", "*B* (0.1, 0.9)", "*C* (0.1, 0.8)", "*D* (0.23, 0)", "*E* (0.1, 0)", and "*F* (0.5,0)" are highlighted in both **Fig. 3-59(a)** and **(b)**. Each point corresponds to one set of (k, f_n). For example, point "*A*" represents the case when k=0.1, f_n=1.

First, "*F* (0.5, 0)" shows the traditional EET-DCX [1] with triangular current (k=0.5) and without C_r (f_n=0). To reduce the rms current, trapezoidal current modulation [2] was introduced, as shown in the case in "*E* (0.1, 0)". At point "*E*", when k=0.1, f_n=0, typical EET-DCX can realize a smaller rms current (1.03I_{in}) compared with point "F" (1.154I_{in}). However, in the meantime, point "*E*" suffers from a 2.78 times V_b across the LV bridge compared with point "*F*" as shown in **Fig. 3-59(b)**.

In order to address this trade-off, hybrid EET-DCX was introduced with an extra C_r ($0<f_n\leq1$). As shown in **Fig. 3-59(a)** and **(b)**, point "*B* (0.1, 0.9)" can be set as an example design without tolerance. Compared with typical EET-DCX, if the same rms current (1.08I_{in}) were both realized, point "*D* (0.23, 0)" represents the case without C_r. Compared with "*D*" and "*B*", hybrid EET-DCX can dramatically reduce the voltage stress V_b from 1.41 to 0.58 (2.4 times). Moreover, if the tolerance on C_r is from -20% to +20%, point "*B*" will move up to "*A* (0.1, 1)" or move down to "*C* (0.1, 0.8)", respectively. If f_n decreases with the same k, I_{rms} will decrease because the curvature becomes smaller, and the current waveform is more like a trapezoid. However, on the other hand, smaller f_n means that C_r will cancel less portion impedance of L_k. However, compared with typical EET-DCX without C_r, the voltage stress can still be reduced significantly. Considering the same L_k, V_b will increase with a smaller f_n. On the other hand, corresponding to **Fig. 3-58(d)**, when f_n=1, the current waveforms will remain pure sinusoidal, no matter how k changes.

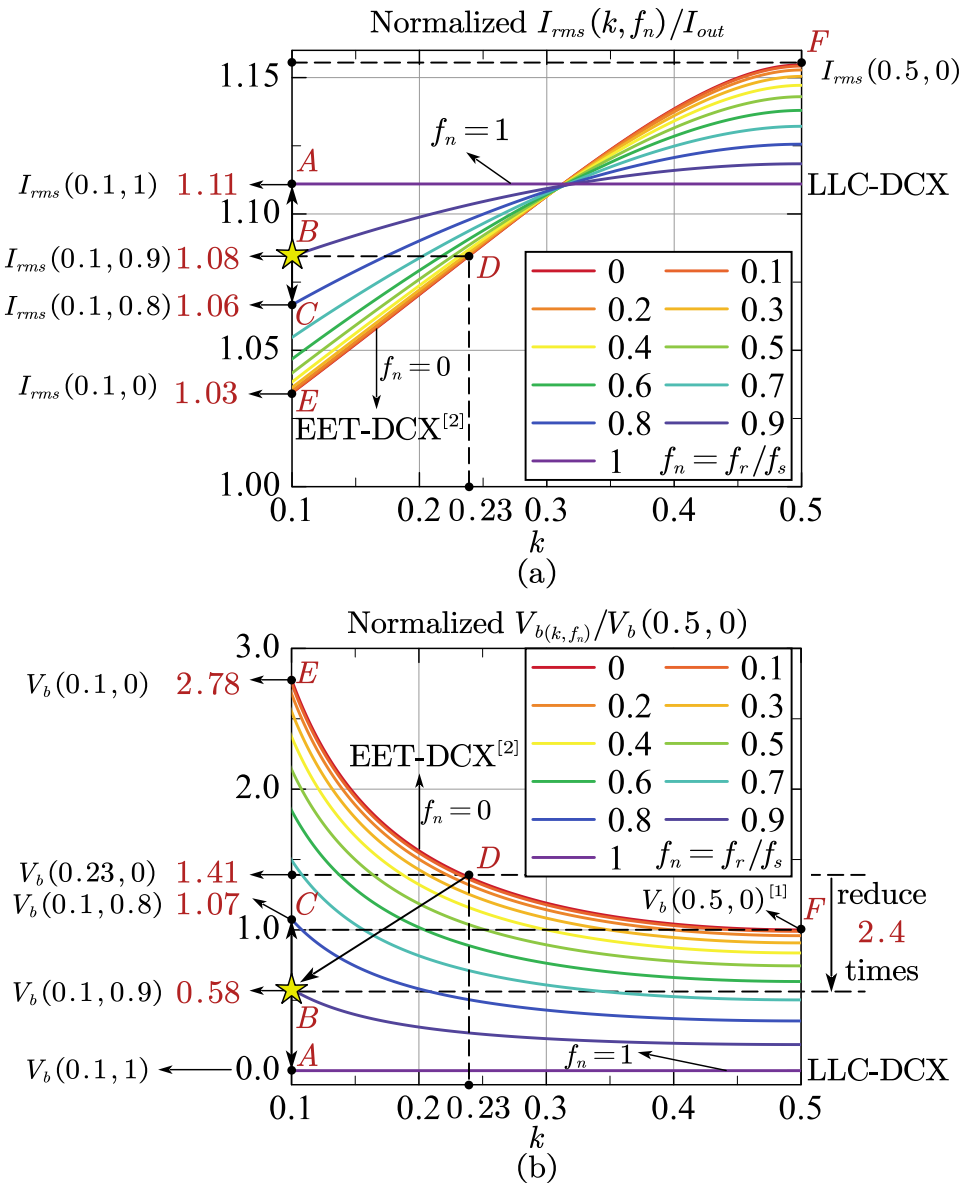


Fig. 3-59. Hybrid EET-DCX: (a) Normalized transformer rms current I_{rms}/I_{in}, and (b) normalized floating capacitor voltage $V_b/V_b(0.5,0)$.

3.5.3 Hybrid RC EET-DCX

1) RC EET-DCX without C_r

Following the circuit diagram in **Fig. 3-56(b)**, **Fig. 3-60** represents the operation principle of hybrid RC EET-DCX, and **Fig. 3-61** plots the normalized transformer current i_T/I_{in}. Firstly, as shown in **Fig. 3-60(b)** without C_r, the gate signals for Q_1 and Q_2 both have a duty cycle of (1-k), and they exhibit a 180-degree (half cycle) phase shift. Compared to the HV bridge control signals, $Q_{1(2)}$ leads with a 90-degree phase shift from S_1, S_4, S_5, S_8 (S_2, S_3, S_6, S_7). Based on a similar analysis in the last section, when v_{pri} equals nv_{sec}, only the voltage $v_{C,rc}$ will be utilized to drive L_k, resulting in the generation of a quasi-trapezoidal current waveform as shown in **Fig. 3-60(b)**. In a half cycle, during the current commutation from -0.5kT_s to +0.5kT_s, only switch Q_1 is ON, and C_{o2} will resonate with L_k at the frequency f_{rc}.

$$f_{rc} = \frac{1}{2\pi\sqrt{L_k C_{o1(2)}}} \tag{3.77}$$

If L_k and $C_{o1(2)}$ are designed to resonate for a half cycle during the current commutation period $\underline{kT_s}$, an additional relationship between f_{rc} and f_s can be given as

$$f_{rc} = \frac{1}{2k} \cdot f_s \quad k \in (0, 0.5] \tag{3.78}$$

If the resonant frequency f_{rc} can be designed using Eq. (3.77) and (3.78), this half-cycle resonance between $C_{o1(2)}$ and L_k can be employed to realize the transformer current commutation during -0.5kT_s to +0.5kT_s or (1-k)/2T_s to (1+k)/2T_s as shown in **Fig. 3-60(b)**. During the "Current Plateau" period from +0.5kT_s to (1-k)/2T_s, both Q_1 and Q_2 are ON, making $v_{C,rc}$ equal to 0.

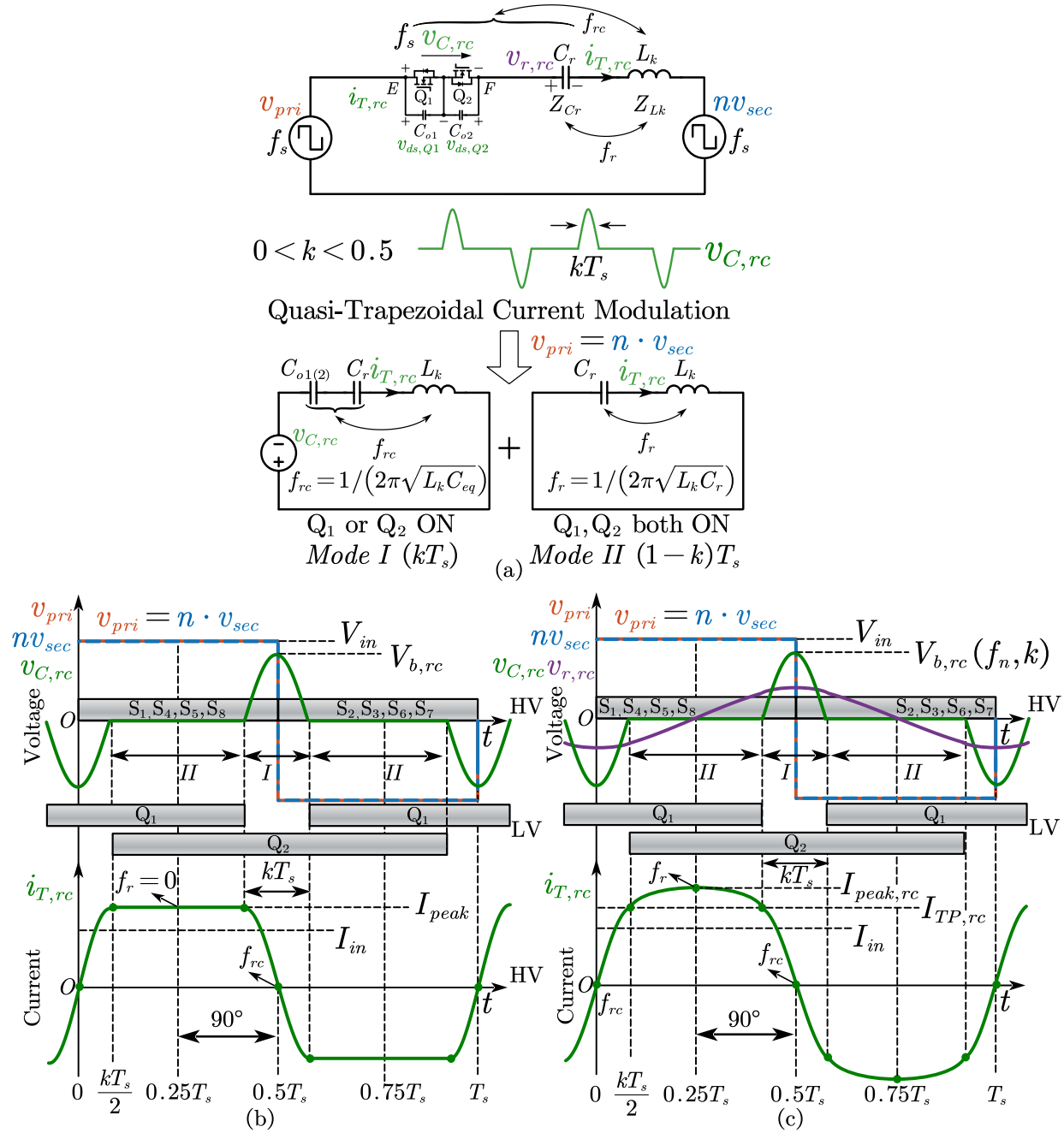


Fig. 3-60. (a) simplified hybrid RC EET-DCX circuit and related v_C waveforms, (b) typical RC EET-DCX without C_r (f_n=0), and (c) Proposed hybrid RC EET-DCX (f_n≠0).

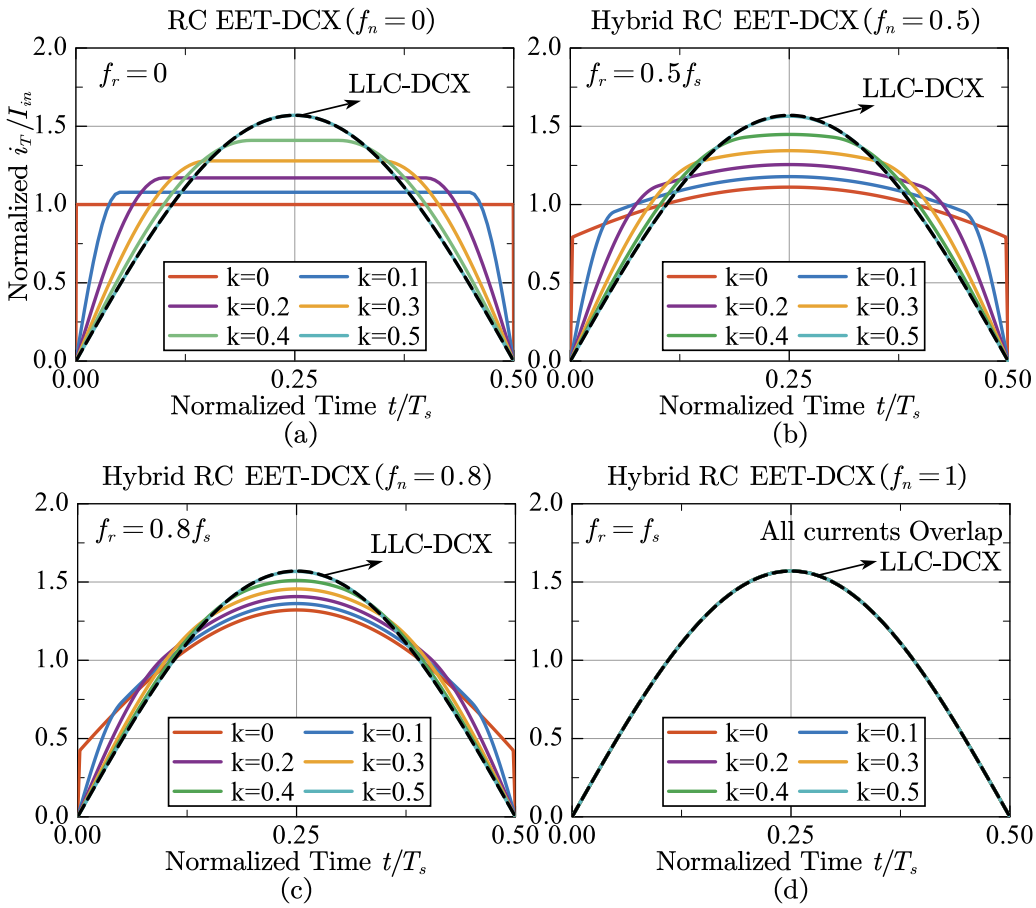


Fig. 3-61. Normalized hybrid RC EET-DCX transformer current i_T/I_{in} with different k and different f_n: (a) f_n=0, (b) f_n=0.5, (c) f_n=0.8, and (d) f_n=1.

Due to no voltage across L_k, transformer current $i_{T,rc}$ remains flat, as shown in **Fig. 3-60(b)**. Moreover, the ZVS turn-on for Q_2 and Q_1 will be achieved at the end of resonance ($+0.5kT_s$ or $(1+k)/2T_s$) because $v_{ds,Q2}$, and $v_{ds,Q1}$ will drop to zero. This significantly differentiates from the hybrid EET-DCX in the last section, which requires a full bridge to accomplish the current commutation. The complete current commutation of RC EET-DCX only requires a single bidirectional AC switch Q_{12}.

Following the similar derivation method in EET-DCX without C_r, the time-domain expression of $i_{T,rc}(t)$ in **Fig. 3-60(b)** can be given as

$$i_{T,rc}(t) = I_{peak,rc}(k,0) \cdot \begin{cases} \sin(2\pi f_{rc} \cdot t) & t \in \left[0, \frac{k}{2}\right) T_s \\ 1 & t \in \left[\frac{k}{2}, \frac{1-k}{2}\right] T_s \\ -\sin(2\pi f_{rc} \cdot (t - 0.5T_s)) & t \in \left(\frac{1-k}{2}, \frac{1}{2}\right] T_s \end{cases} \tag{3.79}$$

where $I_{peak,rc}(k,0)$ in **Fig. 3-60(b)** is the peak current when f_n=0 (without C_r) and can be derived as

$$I_{peak,rc}(k,0) = \frac{\pi}{4 \cdot k + (1 - 2 \cdot k) \cdot \pi} \cdot I_{in} \tag{3.80}$$

Following the methods in Eq. (3.75) and (3.76), without C_r, the rms current $I_{rms,rc}$ and voltage stress $V_{b,rc}$ on LV bidirectional ac switch can be given as

$$I_{rms,rc}(k,0) = \frac{1}{T_s}\sqrt{\int_0^{T_s} {i_{T,rc}}^2(t)\,dt} = \frac{\sqrt{1-k} \cdot \pi}{(1 - 2 \cdot k) \cdot \pi + 4 \cdot k} \cdot I_{in} \tag{3.81}$$

$$V_{b,rc}(k,0) = L_k \cdot \left.\frac{di_{T,rc}(t)}{dt}\right|_{t = 0.5T_s} = \frac{\pi^2}{k \cdot (4 \cdot k + (1 - 2 \cdot k) \cdot \pi)} \cdot f_s L_k I_{in} \tag{3.82}$$

From Eq. (3.82), the peak voltage $V_{peak,rc}$ across LV bidirectional switch (Q_1, Q_2) is proportional with switching frequency f_s, leakage inductance L_k, and input DC current I_{in}.

$$V_{peak,rc} \propto f_s,\ L_k,\ I_{in} \tag{3.83}$$

Similar to typical EET-DCX, with a pre-determined I_{in}, f_s, and k, minimizing L_k becomes crucial as it reduces the voltage stress on the LV bidirectional switch. In addition, the voltage stress $V_{peak,rc}$ is also unrelated to input or output voltage $V_{in(out)}$ according to Eq. (3.82), indicating that this

proposed RC EET-DCX can be adopted in high voltage applications. Therefore, even with large input and output voltages, an LV bidirectional switch can still be selected. Based on Eq. (3.79)-(3.82), **Fig. 3-61(a)** plots the normalized transformer current $i_{T,rc}/I_{in}$ for RC EET-DCX with different k.

However, the same as traditional EET-DCX, RC EET-DCX without Cr also has the trade-off between rms current and voltage stress on the LV switch. From Eq. (3.81), when k is decreasing, the rms current $I_{rms,rc}$ will also reduce because the quasi-trapezoidal current in **Fig. 3-61(a)** will be more like a square waveform. However, in the meantime, $V_{b,rc}$ will dramatically increase when k is decreased from Eq. (3.81).

2) Hybrid RC EET-DCX with C_r

To solve this intrinsic trade-off, the hybrid RC EET-DCX was proposed in **Fig. 3-56(b)** with an extra resonant capacitor C_r. **Fig. 3-60(a)** shows the operation principle and the related output voltage $v_{C,rc}$ of bidirectional AC switch (Q_1 and Q_2). Different from the hybrid EET-DCX in **Fig. 3-57(a)**, there are two different resonant frequencies as shown in **Fig. 3-60(a)**; one is f_{rc} in *Mode I* from $-0.5kT_s$ to $+0.5kT_s$, and another is f_r in *Mode II* from $+0.5kT_s$ to $(1-k)/2T_s$.

In ***Mode I***, C_r is in series with $C_{o1(2)}$, and thus, the equivalent resonant capacitor C_{eq} can be given as

$$C_{eq} = \frac{C_{o1(2)} \cdot C_r}{C_{o1(2)} + C_r} \tag{3.84}$$

Therefore, the f_{rc} in Eq. (3.77) without C_r should be revised as

$$f_{rc} = \frac{1}{2\pi\sqrt{L_k C_{eq}}} \tag{3.85}$$

Based on the same f_s as f_n in Eq. (3.67), the normalized f_{rcn} can be given as

$$f_{rcn} = f_{rc}/f_s \tag{3.86}$$

After considering the effect of C_r in **Fig. 3-60(a)** and **(c)**, the time-domain current expression $i_{T,rc}(t)$ for hybrid RC EET-DCX in Eq. (3.79) should be revised as

$$i_{T,rc}(t) = \begin{cases} I_{a,rc} \cdot \sin(2\pi f_{rc} \cdot t) & t \in \left[0, \frac{k}{2}\right) T_s \\ I_{peak,rc} \cdot \cos\left(2\pi f_r \cdot \left(t - \frac{1}{4}T_s\right)\right) & t \in \left[\frac{k}{2}, \frac{1-k}{2}\right] T_s \\ -I_{a,rc} \cdot \sin\left(2\pi f_{rc} \cdot \left(t - \frac{1}{2}T_s\right)\right) & t \in \left(\frac{1-k}{2}, \frac{1}{2}\right] T_s \end{cases} \tag{3.87}$$

Where $I_{peak,rc}$ is the peak transformer current in **Fig. 3-60(c)**, and $I_{a,rc}$ is an auxiliary variable. Different from the quasi-trapezoidal current in **Fig. 3-60(b)**, $i_{T,rc}$ in **Fig. 3-60(c)** also has a turn point current $I_{TP,rc}$. From the first section in Eq. (3.87), the relationship between $I_{TP,rc}$ and $I_{a,rc}$ can be firstly given as follows.

$$I_{TP,rc} = I_{peak,ac} \cdot \cos(\pi f_n \cdot (k - 0.5)) \tag{3.88}$$

On the other hand, due to the continuity of the current $i_{T,rc}$, $I_{TP,rc}$ can also be expressed from the second section in Eq. (3.88).

$$V_{peak,rc} \propto f_s,\ L_k,\ I_{in} \tag{3.89}$$

From Eq. (3.88) and (3.89), the relationship between I_a and I_{peak} can be given as

$$I_{a,ac} \cdot \sin(\pi f_{rcn} \cdot k) = I_{peak,ac} \cdot \cos(\pi f_n \cdot (k - 0.5)) \tag{3.90}$$

On the other hand, since $v_{C,rc}$ cannot jump at the turning point (e.g. t=0.5T_s-0.5kT_s), the current changing rate should be continued as below.

$$I_{a,rc} \cdot f_{rcn} \cdot \cos(\pi f_{rcn} \cdot k) = I_{peak,rc} \cdot f_n \cdot \sin(\pi f_n \cdot (0.5 - k)) \tag{3.91}$$

Since Eq. (3.90) and (3.91) are two transcendental equations when f_n is not equal to 0, there is no close-form solution for the $f_{rcn}(k, f_n)$ with different k and f_n. However, the numerical solution of $f_{rcn}(k, f_n)$ can be plotted in **Fig. 3-62**. When f_n=0, Eq. (3.91) has the same result as in Eq. (3.78). From **Fig. 3-62**, when f_n is larger than 0, the current $i_{T,rc}$ will resonate less than half a cycle. After obtaining f_{rcn}, input dc current I_{in} equals the average value of current $i_{T,rc}$.

$$I_{in} = \text{average current} = \frac{1}{T_s}\int_0^{T_s} i_{T,rc}(t) \cdot dt \tag{3.92}$$

From Eq. (3.71) and (3.72), $I_{peak,rc}$, and $I_{a,rc}$ can be derived as

$$I_{peak,rc}(k, f_n) = \frac{\pi \cdot f_n \cdot f_{rcn} \cdot \sin B}{4 f_n \cos A \cdot \sin^2\left(\frac{B}{2}\right) + 2 f_{rcn} \cdot \sin A \cdot \sin B} \cdot I_{in} \tag{3.93}$$

$$I_{a,rc}(k,f_n)=\frac{\pi\cdot f_n\cdot f_{rcn}\cdot\cos A}{4f_n\cos A\cdot\sin^2\left(\frac{B}{2}\right)+2f_{rcn}\cdot\sin A\cdot\sin B}\cdot I_{in} \tag{3.94}$$

Where terms "*A*" and "*B*" can be given as

$$\begin{cases} A=\pi f_n\cdot(0.5-k) \\ B=\pi f_{rcn}\cdot k \end{cases} \tag{3.95}$$

After obtaining the $I_{peak,rc}$, and $I_{a,rc}$, **Fig. 3-61** plotted the time-domain normalized transformer current $i_{T,rc}(t)/I_{in}$ with different k and different f_n. **Fig. 3-61(a)-(d)** represents the cases when f_n=0, 0.5, 0.8 and 1, respectively.

Fig. 3-61(a) shows the quasi-trapezoidal current RC EET-DCX without C_r. As shown in **Fig. 3-61(b)**, after adding C_r and when f_n=0.5, the "current plateau" in **Fig. 3-61(a)** will become curved according to the previous analysis in **Fig. 3-60(c)**. If f_n increases to 0.8, the current will become more curved, as shown in **Fig. 3-61(c)**. Finally, when f_n=1, the impedance of L_k will be fully canceled by C_r. In this scenario, no matter how k changes, the current $i_{T,rc}$ always coincides with the sinusoidal current in LLC-DCX, as shown in **Fig. 3-61(d)**.

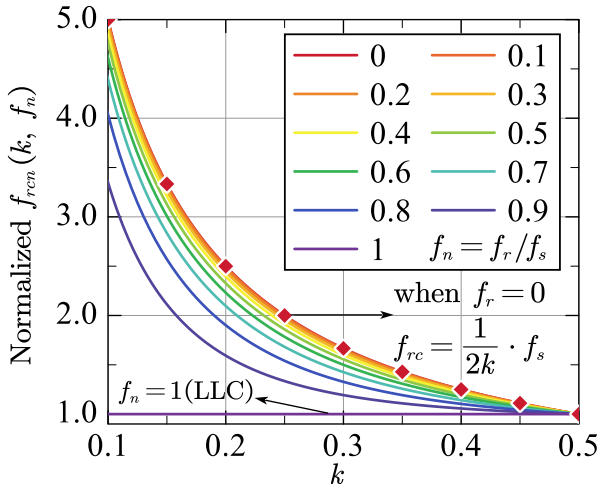


Fig. 3-62. Numerical solution of f_{rcn} with different k and f_n.

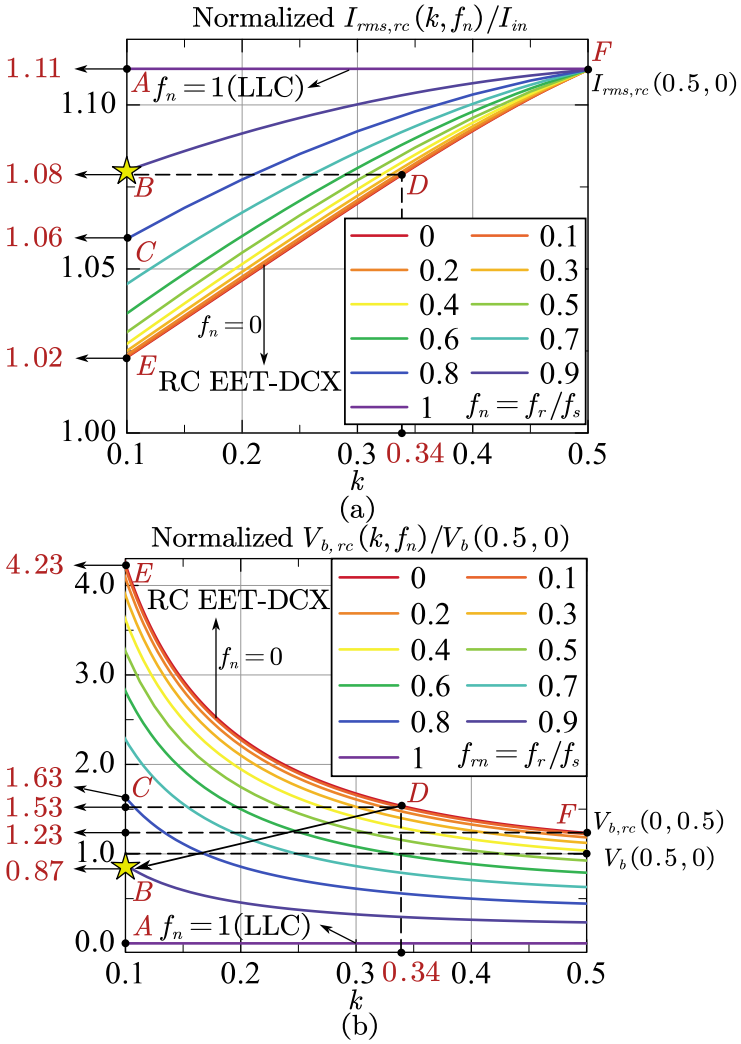


Fig. 3-63. Hybrid RC EET-DCX: (a) Normalized transformer rms current $I_{rms,rc}/I_{in}$, and (b) normalized floating capacitor voltage $V_{b,rc}/V_b(0.5,0)$.

The voltage stress $V_{b,rc}(k, f_n)$ on bidirectional ac switch (Q_1, Q_2) can be derived first. Unlike hybrid EET-DCX, the voltage across L_k in hybrid RC EET-DCX in **Fig. 3-60(c)** cannot suddenly jump at a turning point (e.g., t=0.5T_s-0.5kT_s) because voltage $v_{C,rc}$ will resonate from zero.

Therefore, as shown in **Fig. 3-60(c)**, at the turning point (t=0.5T_s-0.5kT_s), both current and current changing rates should be continuing. Therefore, V_b can be derived as

$$V_{b,rc}(k, f_n) = 2\pi f_{rcn} f_s L_k I_{a,rc} \cdot (1 - \cos B) \cdot \left(1 - \frac{{f_n}^2}{{f_{rcn}}^2}\right) \tag{3.96}$$

Where the term "B" can be found in Eq. (3.95). Subsequently, the transformer rms current $I_{rms,rc}$ can be derived as

$$I_{rms,rc}(k, f_n) = \frac{1}{T_s}\sqrt{\int_0^{T_s} {i_{T,rc}}^2(t)\,dt} \tag{3.97}$$

According to Eq. (3.97), with different k and f_n, **Fig. 3-63(a)** and **(b)** plot the normalized transformer current $I_{rms,rc}/I_{in}$ and normalized LV bridge voltage $V_{b,rc}/V_b(0.5,0)$ of the hybrid RC EET-DCX, respectively. To conduct a fair comparison, the base current and voltage are kept the same as hybrid EET-DCX in **Fig. 3-59(a)** and **(b)**. For an easier display, the "y" axis scale in **Fig. 3-63** has been slightly changed compared with **Fig. 3-59**. Similar to **Fig. 3-59**, six points from "A" to "F" are selected to explain the trade-off between rms current and voltage stress on LV bidirectional AC switch Q_1 and Q_2. Points "E" and "F" are two operation points in RC EET-DCX (f_n=0) with k=0.1 and 0.5, respectively.

If point "*B*" was selected as the reference design with f_n=0.9, with +10% or -10% tolerance on f_n, the operation point will change to "*A*" or "*C*", respectively. From "*B*" to "*A*", $I_{rms,rc}$ will increase from 1.08I_{in} to 1.11I_{in}. However, in the meantime, the voltage stress $V_{b,rc}/V_b$(0.5, 0) will be reduced from 0.87 to 0. On the other hand, from "*B*" to "*C*", rms current will decrease from 1.08I_{in} to 1.06I_{in}, and the normalized voltage stress will increase from 0.87 to 1.63.

Operation point "*D*" (f_n=0) has the same rms current as point "*B*". However, after adding series C_r (f_n=0.9), as shown in **Fig. 3-63(b)**, the normalized voltage stress can be significantly reduced from 1.53 to 0.87.

To sum up, compared with hybrid EET-DCX in *Part A*, hybrid RC EET-DCX can save the number of switches from 4 (full bridge) to 2 (split) or 1 (monolithic). However, the normalized voltage stress on hybrid RC EET in **Fig. 3-59(b)** is generally higher than hybrid EET-DCX in **Fig. 3-59(b)**. A more detailed comparison will be explained in the next part.

3) Design Procedure

In order to properly design the parameters for both proposed hybrid EET-DCX and hybrid RC EET-DCX, an overall design procedure including four steps is shown in **Fig. 3-64** and listed below.

Step 1 — According to V_{in} and V_{out} on both sides, transformer turns ratio n can be selected for these two topologies. On the other hand, the worst case (peak voltage stress V_b or $V_{b,rc}$) will occur at rating power with maximum input current I_{in}.

Step 2 — Considering the total power density, the optimal switching frequency f_s is pre-determined. After the design and fabrication of the high-frequency transformer, the value of leakage inductance L_k can be obtained. With pre-determined $f_{r,opt}$, and $L_{r,HV(TLV)}$, the resonant capacitances $C_{r,HV(TLV)}$ on both sides can be calculated from Eq. (3.62).

Step 3 — With the pre-determined boundary of V_b or $V_{b,rc}$, the optimal operation point (k_{opt}, $f_{n,opt}$) can be found in **Fig. 3-59(a)** or **Fig. 3-63(a)** with minimum rms current I_{rms}.

Step 4 — The series resonant capacitor C_r can be determined from Eq. (5) with $f_{r,opt}$. As for hybrid RC EET-DCX, after obtaining $f_{r,opt}$, the resonant commutation frequency f_{rc} can be determined from **Fig. 3-62**. Later, the related parallel capacitor $C_{o1(2)}$ can be calculated based on Eq. (3.84)-(3.85).

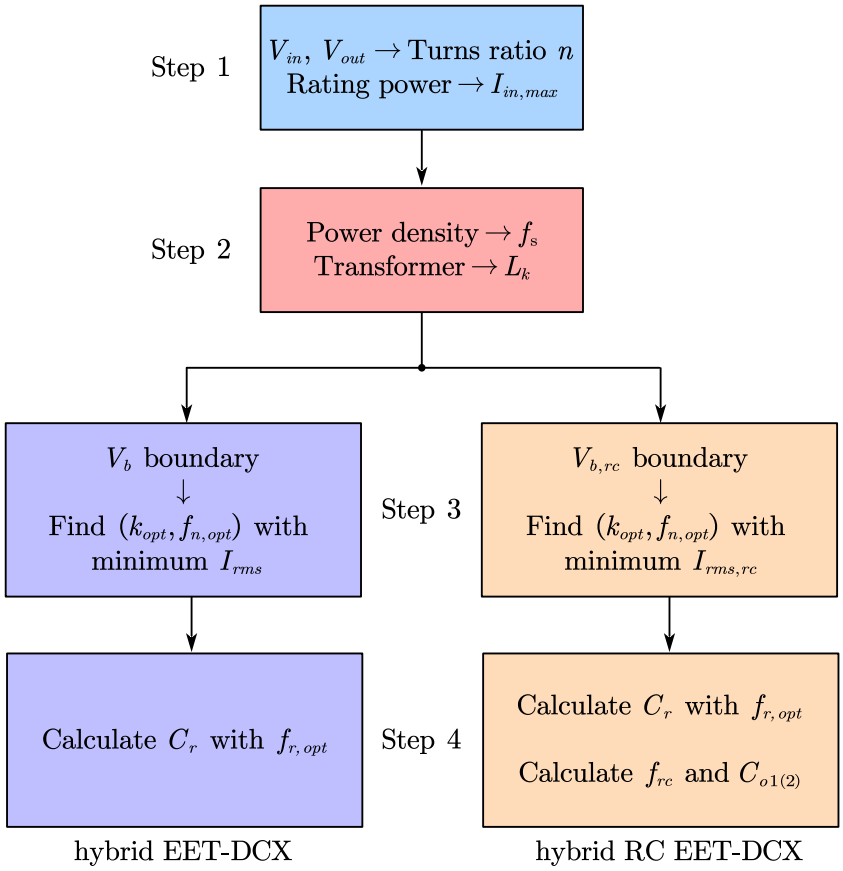


Fig. 3-64. Design procedures for hybrid EET-DCX and hybrid RC EET-DCX.

3.5.4 Analytical Comparison

1) RMS Current through Transformer

Since transformer current will lead to both conduction losses on semiconductors and transformer windings, a smaller rms current is desirable for a high-efficiency design. With different k and f_n, transformer rms currents of both hybrid EET-DCX and hybrid EET-DCX are plotted in **Fig. 3-65** from Eq. (3.76) and (3.81). The rms currents were normalized first based on input DC current I_{in}. As shown in **Fig. 3-65(a)**, with the same k and f_n, $I_{rms,rc}$ from hybrid RC EET-DCX is generally smaller than I_{rms} from hybrid EET-DCX. For the simple explanation, normalized rms currents $I_{rms,rc}/I_{in}$ and I_{rms}/I_{in} in **Fig. 3-65(a)** are projected to **Fig. 3-65(b)** and **(c)**, respectively.

To explain more about this smaller rms current from hybrid RC EET-DCX, A certain case when k=0.2, f_n=0.5 was shown in **Fig. 3-66** for both hybrid EET-DCX and hybrid RC EET-DCX. Based on previous analysis, the current changing rate di/dt at turning points (e.g., t=0.1T_s or 0.4T_s) continues in hybrid RC EET-DCX and discontinues in hybrid EET-DCX, respectively. The reason is that the voltage in hybrid EET-DCX can jump at turning points when the floating capacitor DC voltage V_b is kicked in or out. On the contrary, resonant voltage $v_{C,rc}$ must begin from zero, and thus, the di/dt in hybrid RC EET-DCX will continue, as shown in **Fig. 3-66**. With the same k and f_n, during the current commutation periods (0-0.1T_s or 0.4-0.5T_s), the current of hybrid RC-EET DCX resonates with f_{rc}=2.3f_s based on the previous analysis in **Fig. 3-62**. As for hybrid EET-DCX, the current always resonates with f_r=0.5f_s. Thus, compared to the hybrid EET-DCX (I_{rms}=1.07I_{in}), the hybrid RC-EET DCX has a more curved current waveform, which can bring the benefit of the lower rms current ($I_{rms,rc}$=1.05I_{in}). In summary, when both k and f_n are close to 0, the rms current can be minimized because the current waveform will be more like a “square” waveform, which has the smallest rms value.

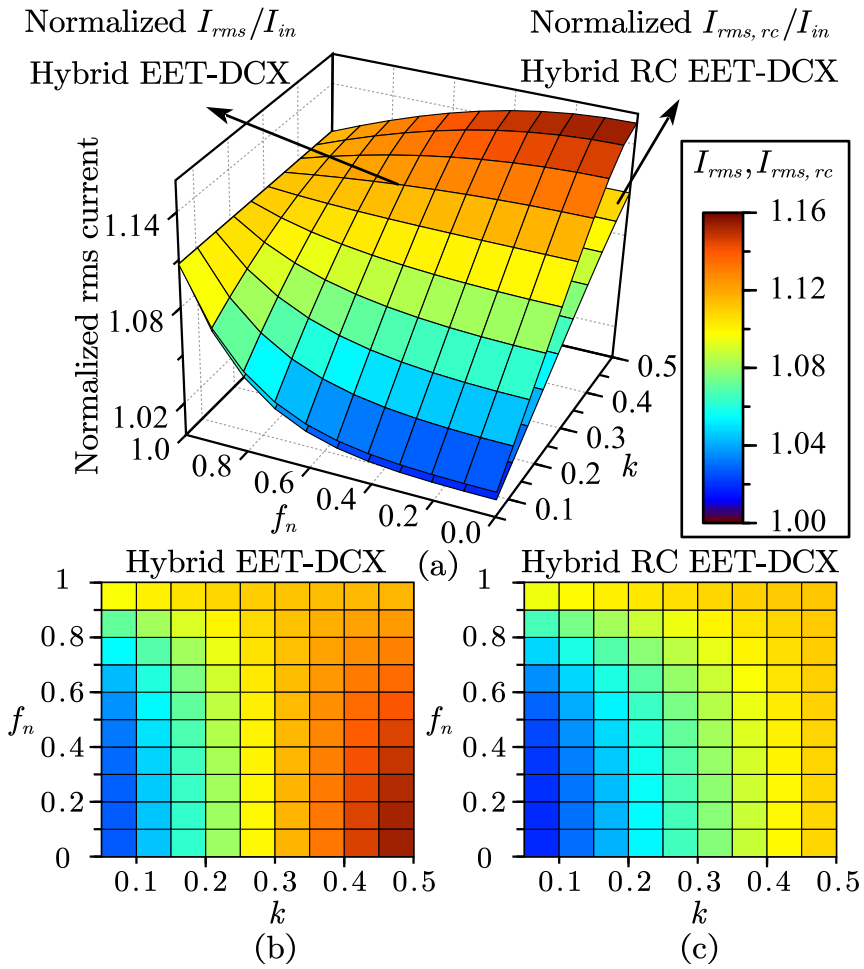


Fig. 3-65. Normalized rms current based on I_{in} with different k and f_n: (a) 3-D plot, (b) 2-D projection for hybrid EET-DCX, and (c) hybrid RC EET-DCX.

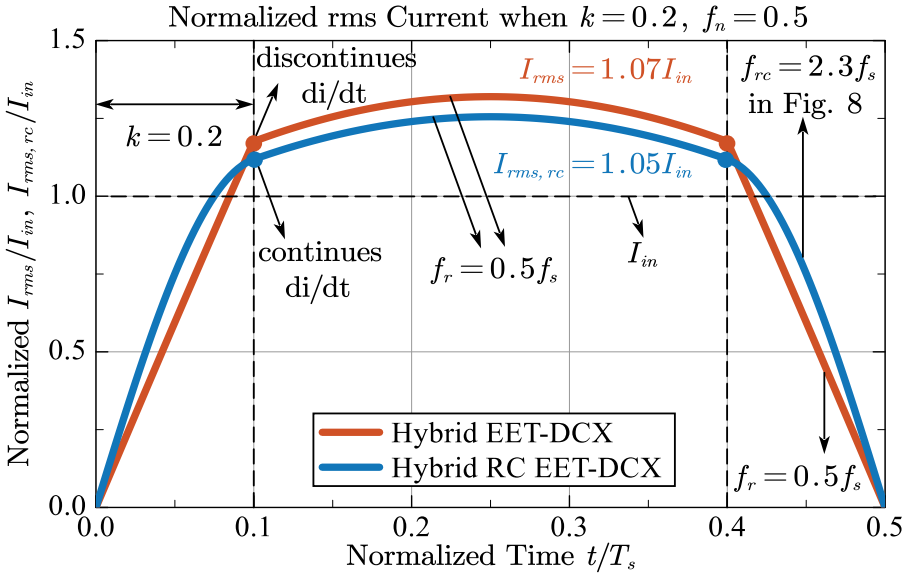


Fig. 3-66. Current waveforms for both hybrid EET-DCX and hybrid RC EET-DCX with k=0.5, f_n=0.5.

2) Voltage Stress

Fig. 3-67 represents the normalized voltage stress based on $V_b(0.5, 0)$ with different k and f_n, from Eq. (3.75) and (3.96). For comparison, the projections for both V_b and $V_{b,rc}$ are also plotted. When f_n=1 (f_r=f_s), both $V_b(k, 0)$ and $V_{b,rc}(k, 0)$ are always zero because the impedance of L_k has been fully canceled by C_r. With smaller k or smaller f_n, the voltage stress will increase, as shown in both **Fig. 3-67(a)** and **(b)**. Compared with V_b on hybrid EET-DCX, the voltage stress $V_{b,rc}$ on hybrid RC EET-DCX is generally larger. The quantitative analysis can be found in Eq. (3.75) and (3.96). However, the switch number of hybrid RC EET-DCX is 2 (split) or 1 (monolithic), and the number of hybrids EET-DCX is 4 (LV full bridge). To sum up, there is a general trade-off between voltage stress and rms current. For both resonant-type DCXs, when f_n (f_r/f_s) moves from 0 to 1, the voltage stress will decrease. However, in the meanwhile, the rms currents I_{rms} or $I_{rms,rc}$ will both increase. With the help of resonant capacitor C_r, both hybrid EET-DCX and hybrid RC EET-DCX can provide an application-oriented design.

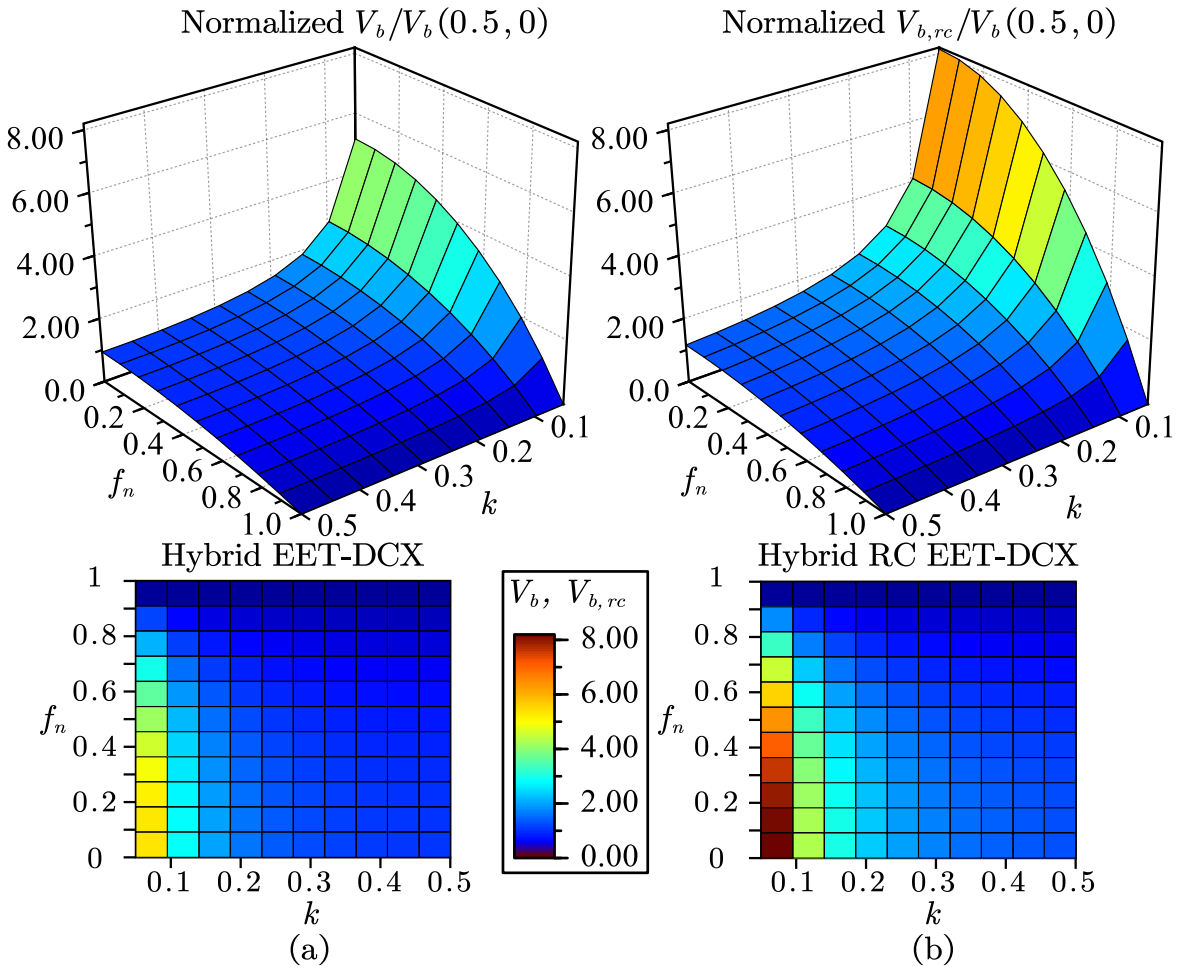


Fig. 3-67. Normalized voltage stress based V_b(0.5, 0) with different k and f_n: (a) hybrid EET-DCX, (b) hybrid RC EET-DCX.

3) Current Sharing Performance

After comparing the rms current and voltage stress, the current sharing performance between these two topologies plus typical LLC-DCX will be studied. The transformer-level parallel setup for hybrid EET-DCX, hybrid RC EET-DCX, and LLC-DCX are all shown in **Fig. 3-68**. $i_{T1(2)}$, $i_{T,rc1(2)}$, and $i_{T,LLC1(2)}$ are transformer currents through these three topologies. The two transformers are connected in parallel, and the current sharing between the two branches is determined by the impedance distribution between Z_{tank1} and Z_{tank2}. This relationship can be extended to the N branches paralleling.

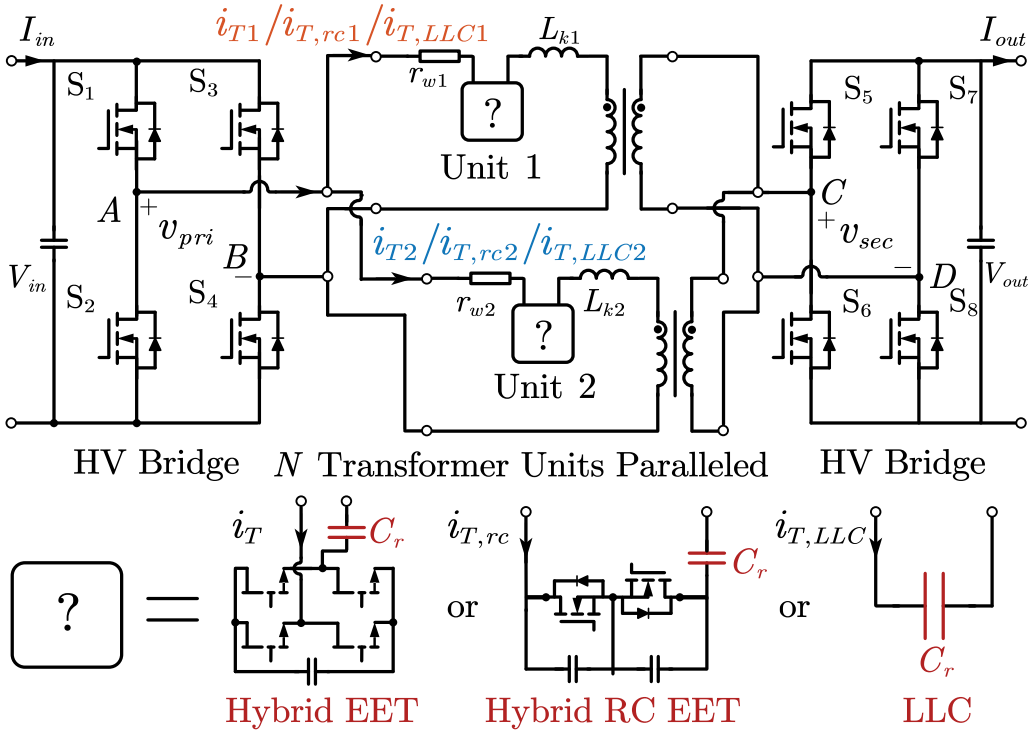


Fig. 3-68. Transformer-level parallel setup for hybrid EET-DCX, hybrid RC EET-DCX, and LLC-DCX.

Table 3-7 CURRENT SHARING SIMULATION PARAMETERS

Variable	Value	Variable	Value
Input voltage V_{in}	300 V	Output voltage V_{out}	300 V
Parallel number N	2	Loop resistance r_w	100 mΩ
Rating power P	9 kW	Switching frequency f_s	500 kHz
Commutation index k	0.2	Leakage inductance L_k	380 nH

$$i_{T1}:i_{T2}:\ \cdots\ :i_{TN}=\frac{1}{|Z_{tank1}|}:\frac{1}{|Z_{tank2}|}:\ \cdots\ :\frac{1}{|Z_{tankN}|}\quad(N=1,2\ldots) \tag{3.98}$$

Where Z_{tank} in these three topologies can be given as

$$Z_{tankN}=\underbrace{\underbrace{Z_{Lk}+Z_{Cr}}_{\text{partially cancelled}}\ +\ Z_{EET/RC\,EET}}_{\text{fully cancelled as 0}}\ +\ r_{wN}\quad(N=1,2\ldots) \tag{3.99}$$

As shown in **Fig. 3-68**, in both hybrid EET-DCX and hybrid RC EET-DCX, the impedance of L_k can be partially canceled first by C_r. Then, the residual impedance will be compensated by the EET or RC EET branch. Therefore, after utilizing EET or RC EET, the current sharing performance for these two topologies can be expressed as

$$\left.\begin{matrix}i_{T1}:i_{T2}:\ \cdots\ :i_{TN}\\ i_{T,r1}:i_{T,r2}:\ \cdots\ :i_{T,rN}\end{matrix}\right\}=\frac{1}{r_{w1}}:\frac{1}{r_{w2}}:\ \cdots\ :\frac{1}{r_{wN}}\quad(N=1,2\ldots) \tag{3.100}$$

From Eq. (3.100), the current sharing will be determined by each paralleled branch's resistance. Compared with leakage inductance, resistance can be easily controlled. In addition, copper has a positive temperature coefficient, which is beneficial for the current sharing. A more detailed discussion can be found in [26].

Fig. 3-69 shows the current sharing simulation for hybrid EET-DCX with the related current Fourier spectrum, as shown in **Fig. 3-70**. In addition, **Fig. 3-71** represents the simulation results for hybrid RC EET-DCX with the current spectrum, as shown in **Fig. 3-72**. The simulated parameters for these two topologies are listed in **Table 3-7**. As shown in both **Fig. 3-69** and Fig. 3-71, although different fn (fr/fs) will lead to a small difference from the current shape. With the same commutation period k=0.2, current i_{T1} or $i_{T,rc1}$ (f_n=0.8) has a more curved current compared

with i_{T2} or $i_{T,rc2}$ (f_n=0.5). This is because C_{r2} is smaller than C_{r1} and can compensate for the greater impedance of L_k. When f_n is closer to 1, more impedance L_k is canceled by C_r. Thus, smaller voltage stress will be applied on the LV bridge or bidirectional AC switch, as shown in **Fig. 3-69** and **Fig. 3-71**, respectively. However, from the RMS current perspective, the current sharing performances in both hybrid EET-DCX and hybrid RC EET-DCX are still very good. **Fig. 3-70** and **Fig. 3-72** plot the spectrum of currents i_{T1} (i_{T2}) and $i_{T,rc1}$ ($i_{T,rc2}$), respectively.

The current shape difference is due to the high-order harmonics such as $3f_s$. The fundamental component (f_s) with f_n=0.5 and 0.8 are very close to each other in both these two topologies, which means the good current sharing performance can be maintained even after adding C_r.

For the comparison, the LLC-DCX paralleling simulation is also given in **Fig. 3-73**. Due to the absence of EET or RC EET, the current sharing performance of LLC-DCX will rely on the resonant tank parameters. At high frequency, the impedance from L_k will dominate the whole loop impedance if there is no extra circuitry like EET or RC EET. As shown in **Fig. 3-73**, with only 5% resonant frequency point shift, nearly all current will go through loop 1 since Z_{tank1} has a much lower impedance.

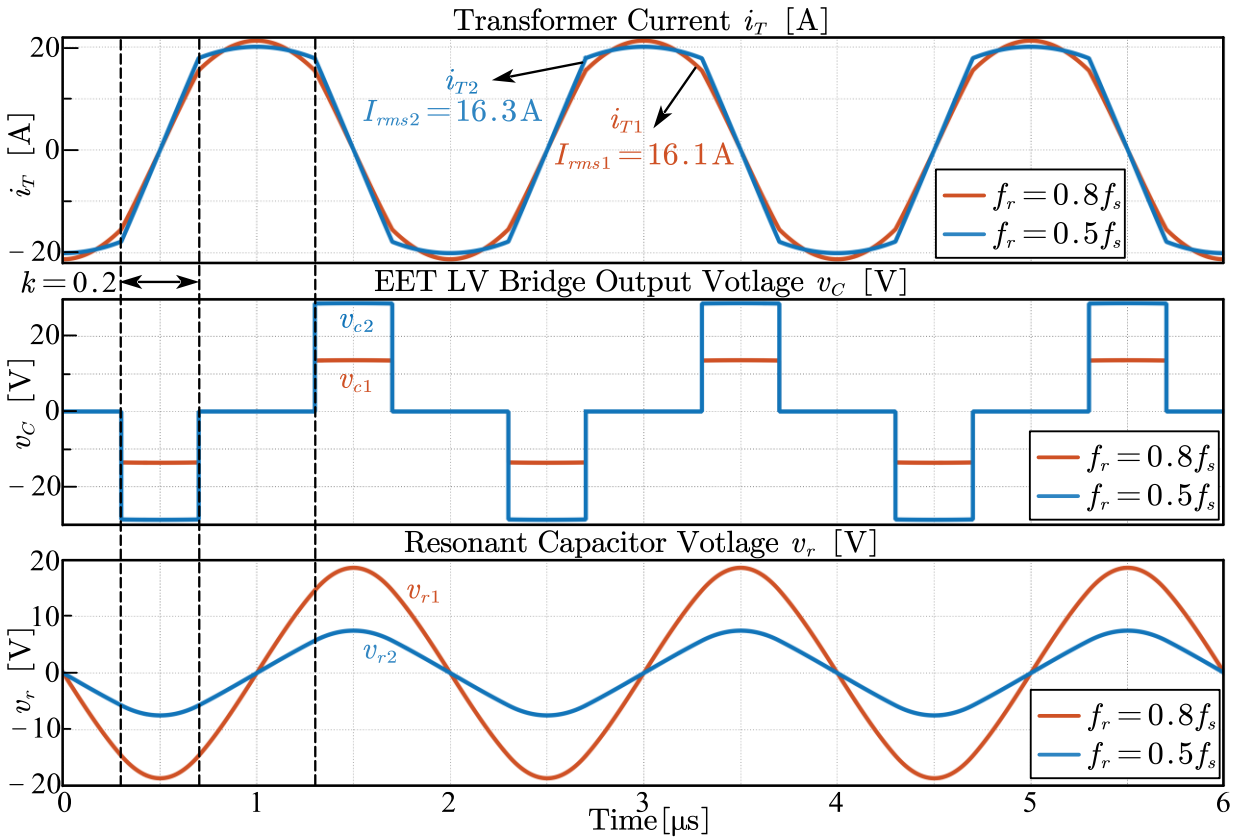


Fig. 3-69. Simulated current sharing results of hybrid EET-DCX with two transformers paralleled when *k*=0.2. The corresponding parameters are listed in Table 3-7.

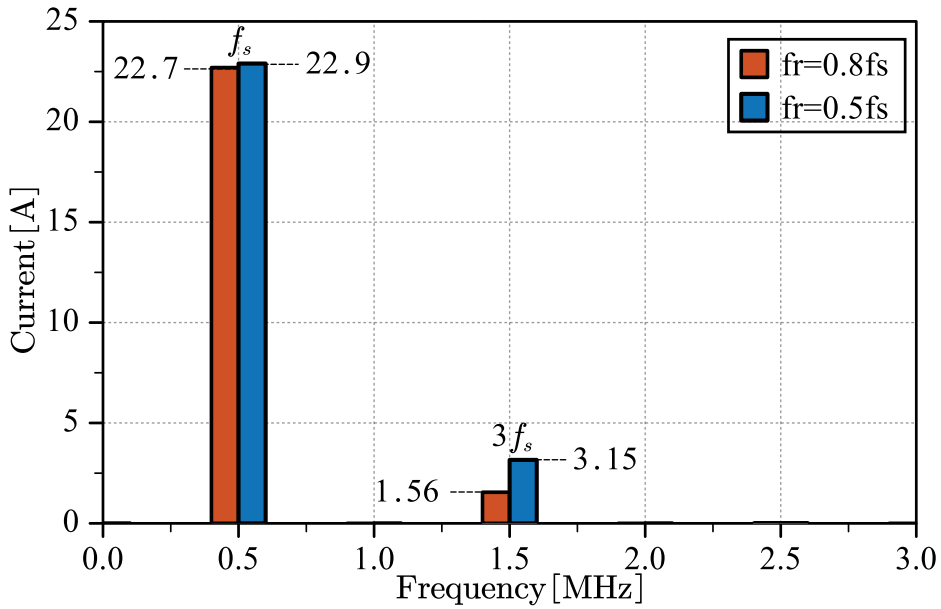


Fig. 3-70. The Fourier spectrum of hybrid EET-DCX current i_{T1} and i_{T2} based on f_s=500 kHz. The time-domain current waveforms can be found in Fig. 3-69.

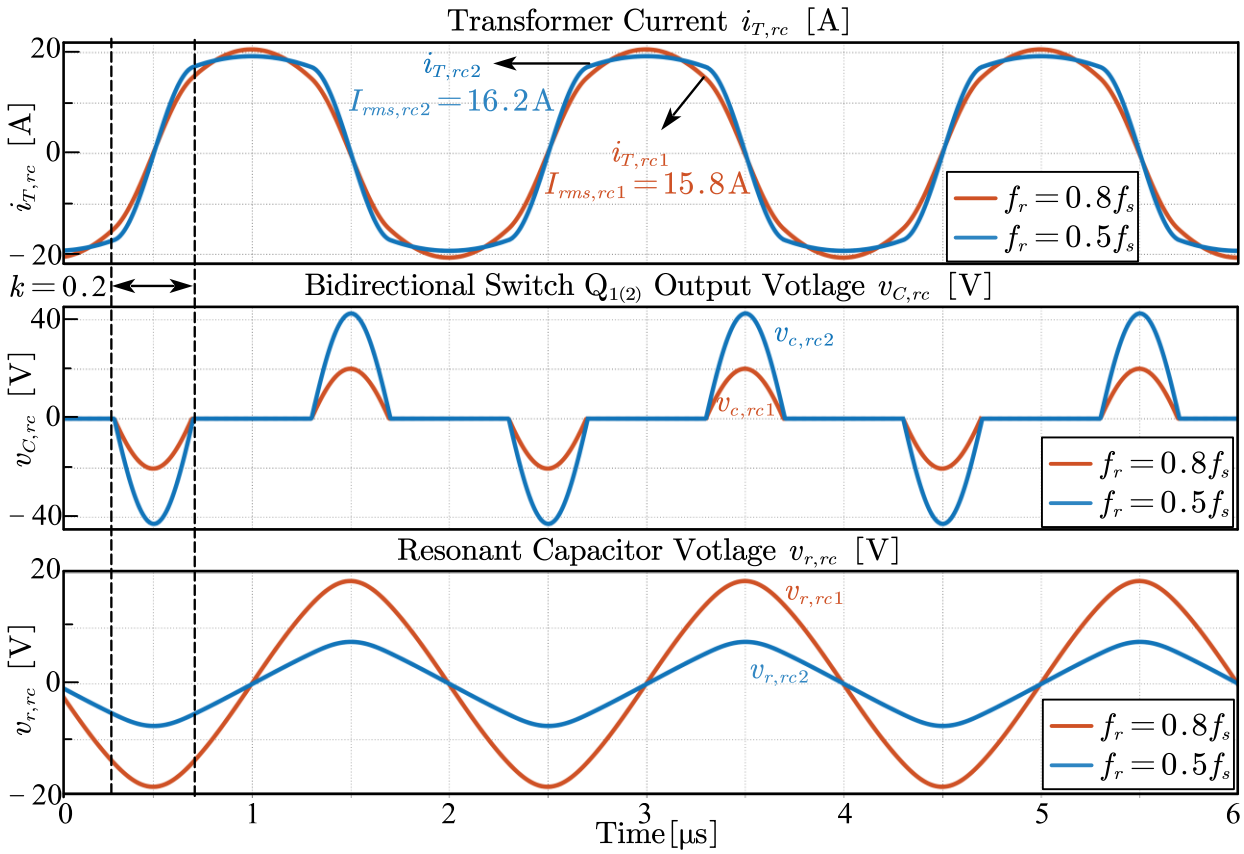


Fig. 3-71. Simulated current sharing results of hybrid RC EET-DCX with two transformers paralleled when *k*=0.2. The corresponding parameters are listed in Table 3-7.

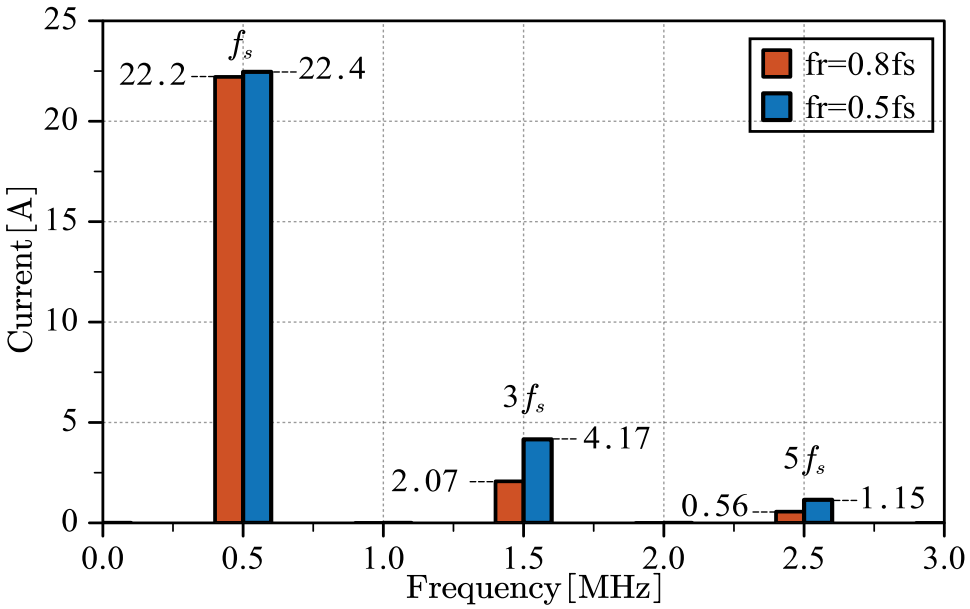


Fig. 3-72. The Fourier spectrum of hybrid RC EET-DCX current i_{T1} and i_{T2} based on f_s=500 kHz. The time-domain current waveforms can be found in Fig. 3-69.

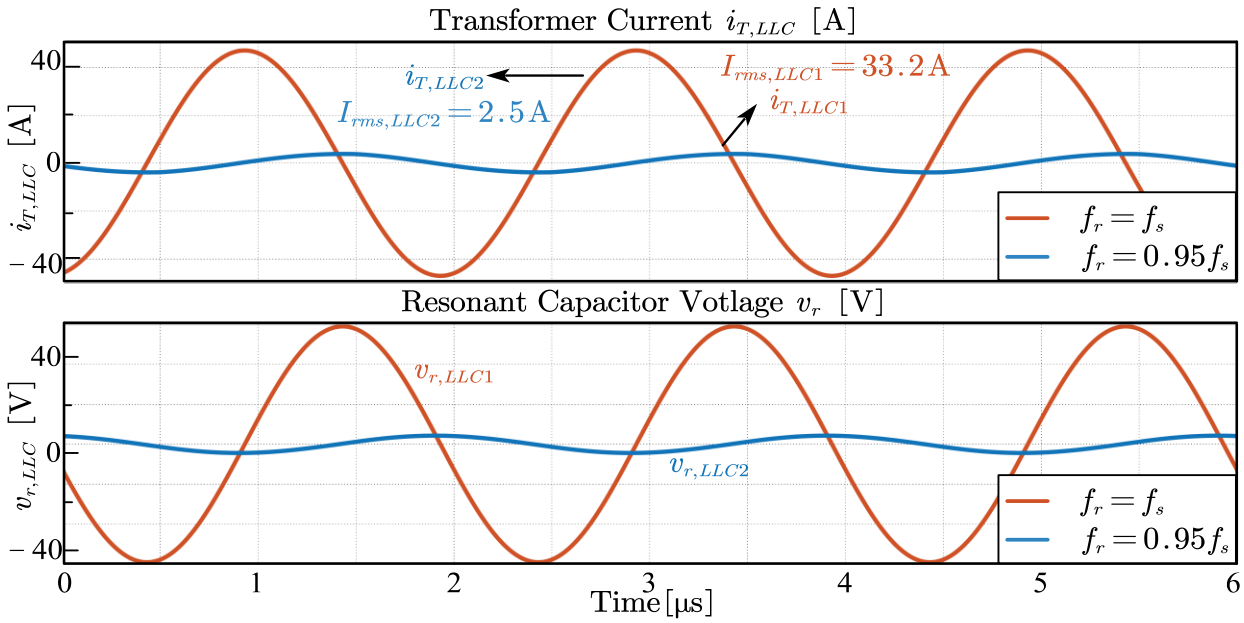


Fig. 3-73. Simulated current sharing results of LLC-DCX with two parallel transformers. The corresponding parameters are listed in Table 3-7.

3.5.5 Experimental Verification

1) 12 kW Prototypes

As shown in **Fig. 3-74**, two 12-kW prototypes of hybrid EET-DCX and RC EET-DCX were built to verify the operation principle and performance. As shown in **Fig. 3-74(a)**, both DCXs share the same platform with two HV bridges. To verify the current sharing performance, four hybrid RC EET/EET units are connected in parallel. As for the detailed transformer part shown in **Fig. 3-74(b)**, hybrid EET-DCX has one GaN-based LV full bridge, and hybrid RC EET-DCX has one bidirectional switch composed of Q_1 and Q_2. The monolithic bidirectional switch can be utilized to reduce the switch number further. The series resonant capacitor C_r was put on the backside and can be found in **Fig. 3-74(a)**. All the parameters of two 12 kW hybrid EET-DCX and hybrid RC EET-DCX were listed in **Table 3-8**. Both hybrid EET and hybrid RC EET units adopted the same 80 V GaN FETs *EPC 2029*. Since the total rating power is 12 kW with four transformer units paralleled, each unit is individually designed for 3 kW (300 V, 10 A). Moreover, for the EET unit shown in **Fig. 3-74**, two copper pads can be used to bypass the LV bridge, and the whole hybrid EET-DCX can operate as an LLC-DCX.

Table 3-8 PARAMETERS OF RC EET-DCX WITH FOUR EET UNITS

Variable	Value	Variable	Value
$V_{in(out)}$	300 V	$C_{o1(2)}$	22.7 nF
P	12 kW	f_s	250-500 kHz
L_k	286 nH	$L_{pri(sec)}$	15 μH
ER Core	ECW64A18	Core Material	DMR51
$C_{oss,pri(sec)}$	418 pF × 2	$C_{oss,LV}$	1310 pF
HV Bridge	C3M0016120k × 2	LV Q_1 and Q_2	EPC 2029

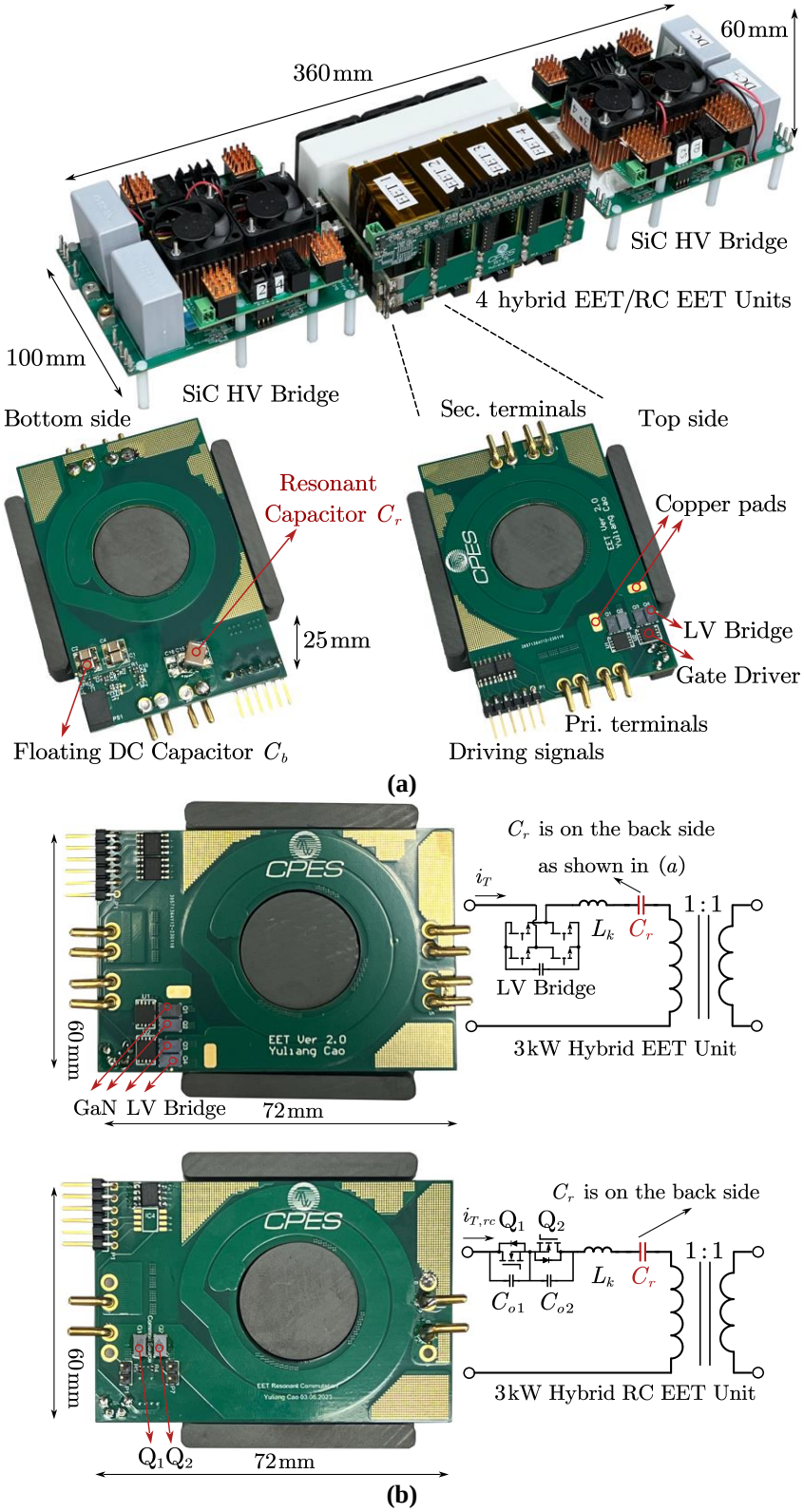


Fig. 3-74. Two 12 kW DCX prototypes with four configurable transformer units paralleled: (a) whole converter, (b) detailed design of the hybrid EET and hybrid RC EET. The corresponding parameters are listed in Table 3-8.

2) Hybrid EET-DCX

Fig. 3-75 first presents the full load (12 kW) experimental results of the hybrid EET-DCX with different k when f_n=0 (without C_r). The full load results display the split currents $i_{T1\text{-}4}$, with the drain-to-source voltages $v_{ds,pri}$, and $v_{ds,sec}$ as shown in **Fig. 3-75(a)**, when k=0.5, f_n=0, hybrid EET-DCX will operate as a typical EET-DCX with a triangle current waveform. As shown in **Fig. 3-75(b)** and **(c)**, when k was reduced to 0.3 and 0.15, the current will change to trapezoid waveforms with smaller rms current. Although smaller k can lead to smaller rms current, the voltage stress on the LV bridge will increase dramatically, as shown in **Fig. 3-59**. To verify the current sharing performance, the split currents in **Fig. 3-75** overlap together, as shown in **Fig. 3-76**, and currents $i_{T1\text{-}4}$ match very well with each other. Moreover, the dynamic changing load test was also conducted, as shown in **Fig. 3-77**. From full load to half load, the DC output current I_{out} was reduced from 40 A to 20 A. Even during load-changing transient, natural robust current sharing performance can still be retained.

After adding the resonant capacitor C_r, the hybrid EET-DCX experimental results were plotted in **Fig. 3-77** to **Fig. 3-81**. At first, the resonant f_r was tuned to 0.8f_s, as shown in **Fig. 3-77**. When f_n=0.8, the full load 12 kW results for k=0.4, 0.3, and 0.15 were represented in **Fig. 3-77(a)-(c)**, respectively. Since f_r is close to f_s (f_n=0.8), the overall transformer currents with different k are all like sinusoidal waveforms. When k=0.15, the overlapped currents full load result was also given in **Fig. 3-77(d)** to verify the current sharing performance. Moreover, the half load results when k=0.15 were plotted in **Fig. 3-78** with both split currents and overlapped currents, which means the current sharing was good for both full and half load. The dynamic load changing result from full load to half load (12 kW to 6 kW) is shown in **Fig. 3-79**.

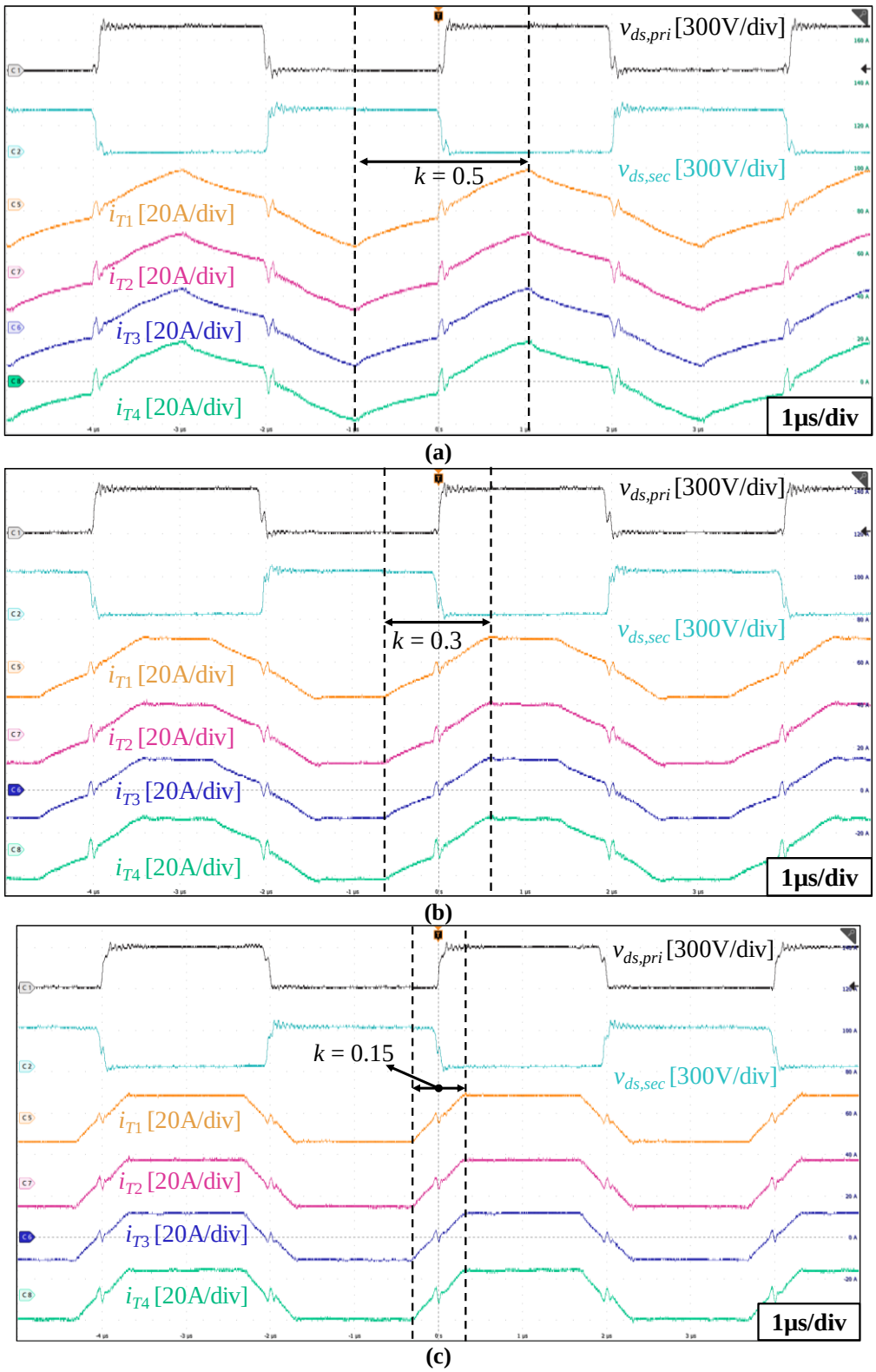
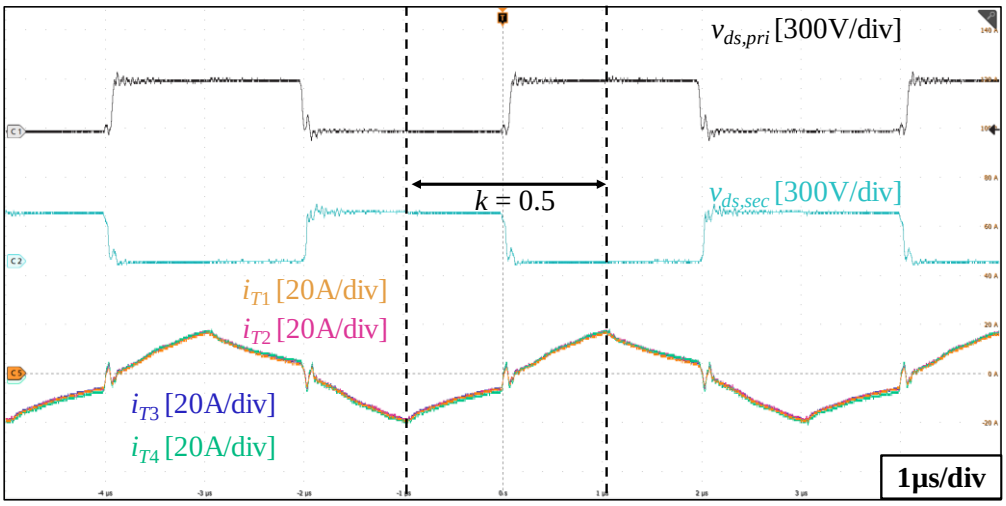
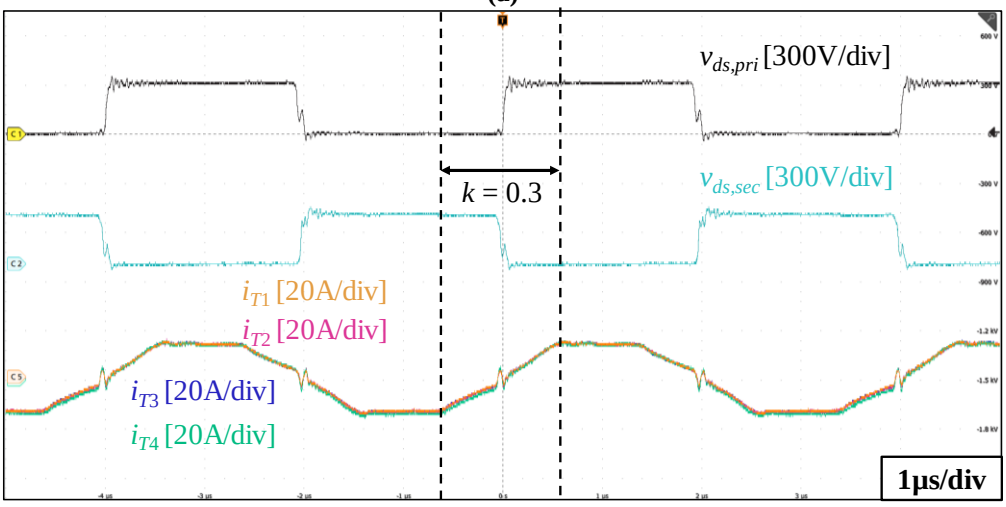


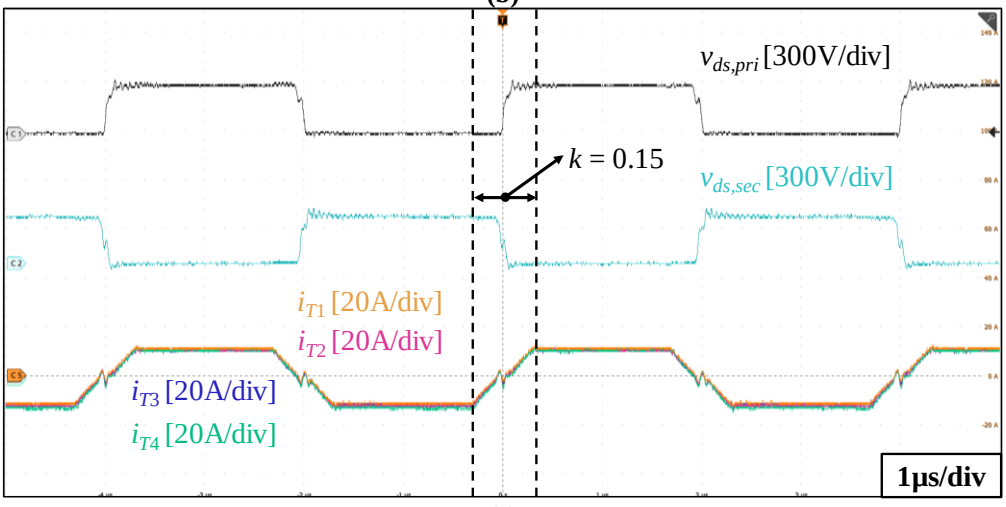
Fig. 3-75. The full load 12 kW experimental results (f_s=250 kHz) of the hybrid EET-DCX with different k when f_n=0 (without resonant capacitor C_r): (a) k=0.5, (b) k=0.3, (c) k=0.15. The corresponding parameters are listed in Table 3-8.



(a)

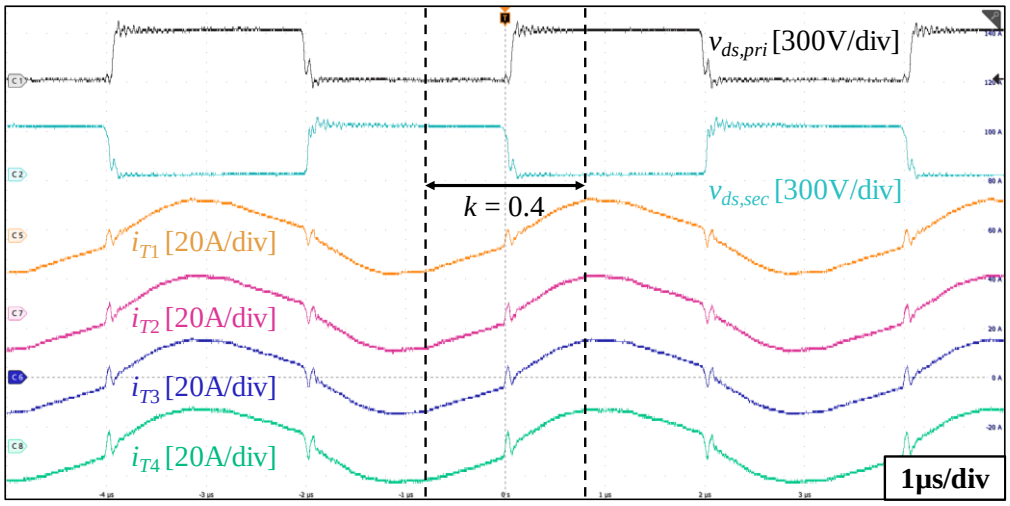


(b)

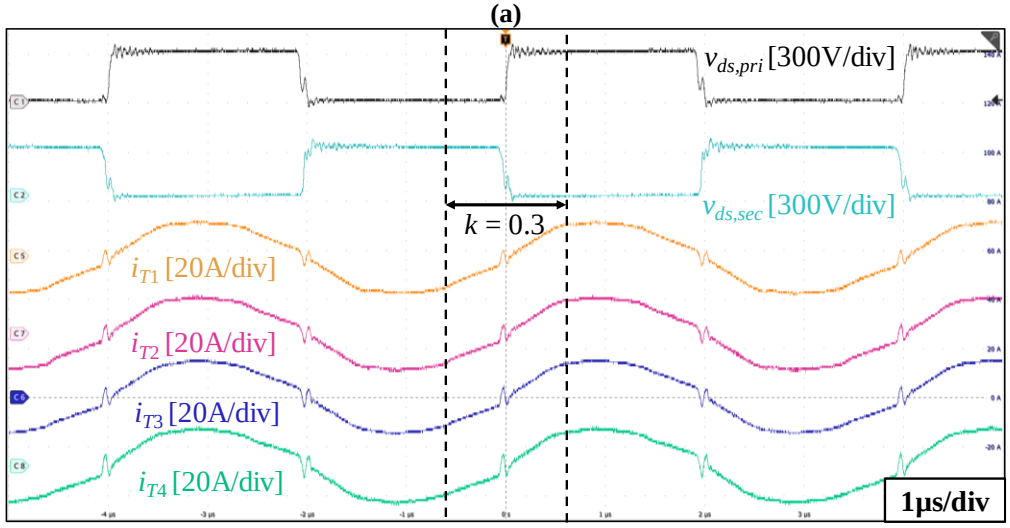


(c)

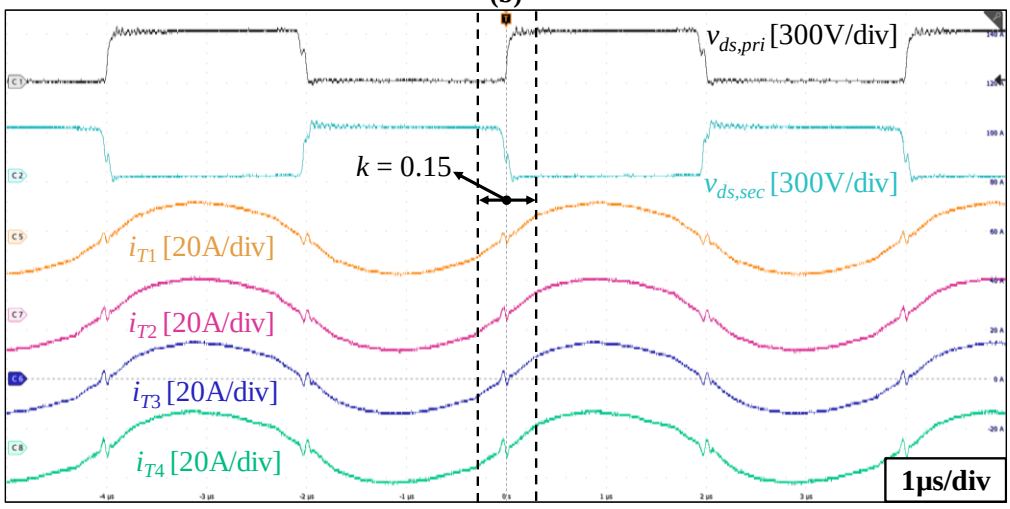
Fig. 3-76. Corresponding current sharing performance after overlapping the split currents in Fig. 21: (a) *k*=0.5, (b) *k*=0.3, (c) *k*=0.15. The corresponding parameters are listed in Table 3-8.



(a)

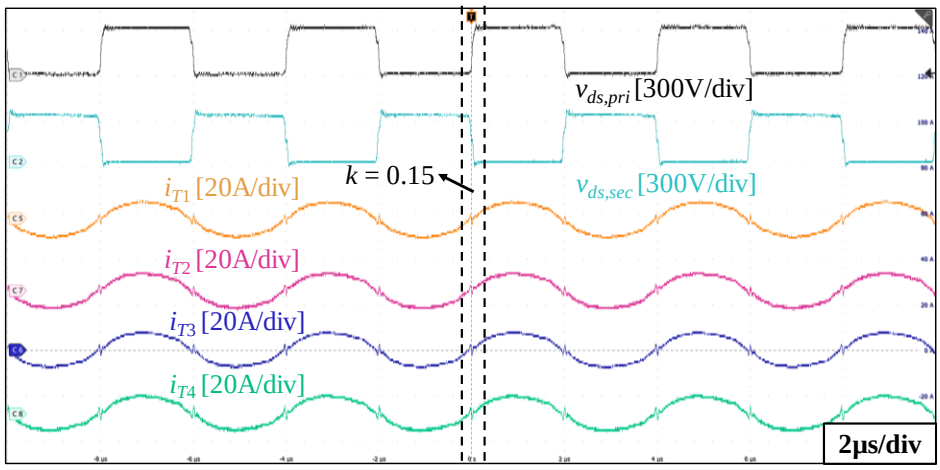


(b)

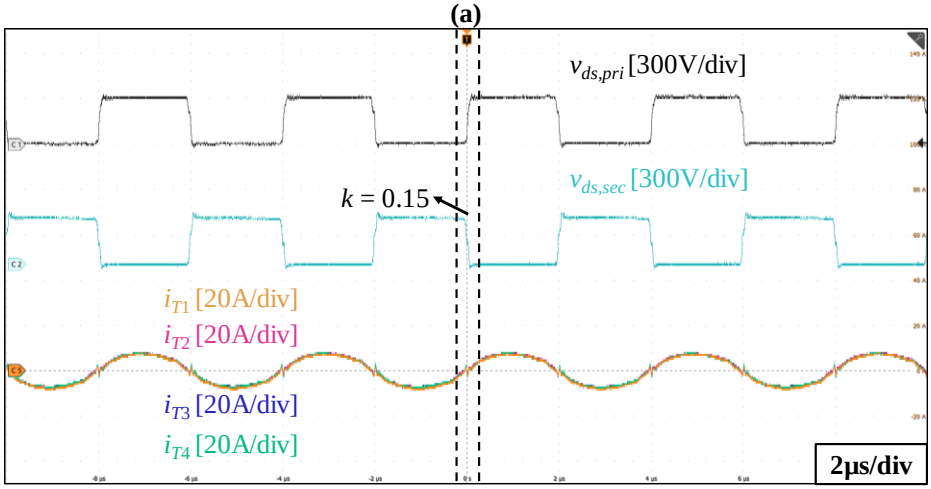


(c)

Fig. 3-77. The full load 12 kW experimental results of the hybrid EET-DCX with different k when f_n=0.8 (with resonant capacitor C_r): (a) k=0.4, (b) k=0.3, (c) k=0.15. The corresponding parameters are listed in Table 3-8.



(a)



(b)

Fig. 3-78. The half load 6 kW experimental results of the hybrid EET-DCX with *k*=0.15: (a) split currents, (b) overlapped currents. The corresponding parameters are listed in Table 3-8.

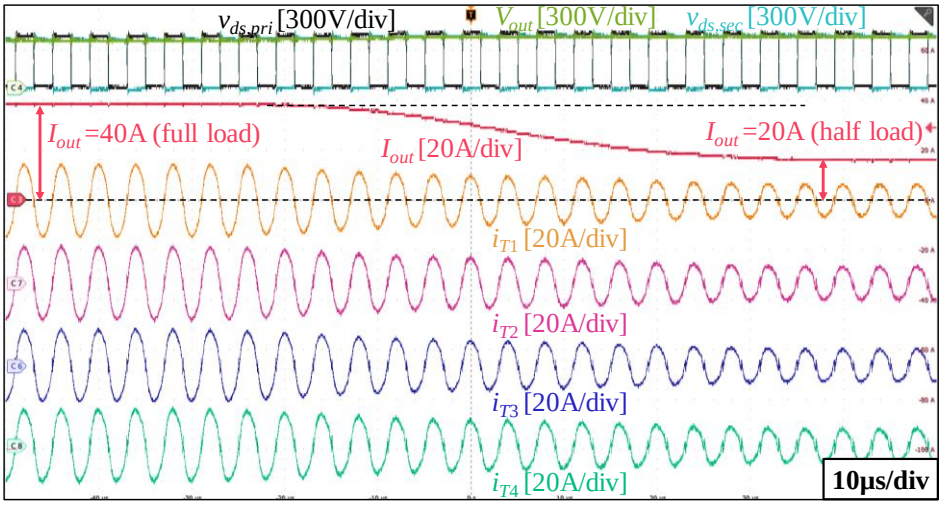


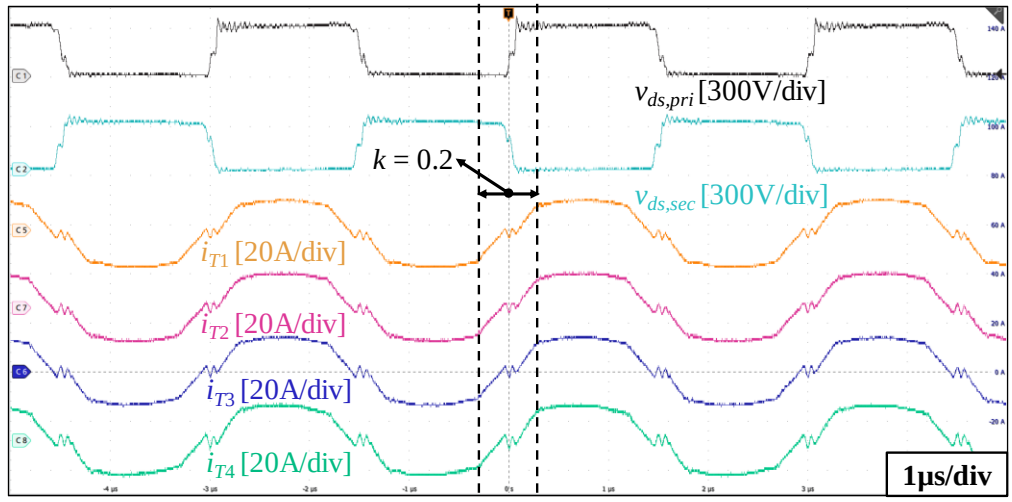
Fig. 3-79. Corresponding current sharing performance after overlapping the split currents in Fig. 21: (a) *k*=0.5, (b) *k*=0.3, (c) *k*=0.15. The corresponding parameters are listed in Table 3-8.

When the load changes from full load to half load, the DC output current I_{out} was decreased from 40 A to 20 A, and the amplitude of transformer currents $i_{T1\text{-}4}$ also reduced correspondingly. From the dynamic experimental result, the current sharing performance was also verified during the transient response.

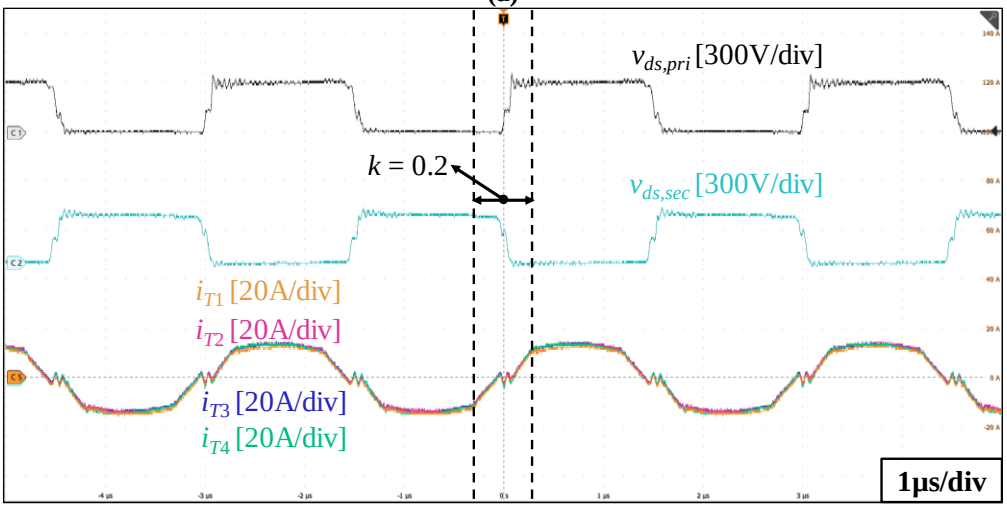
Later, the f_n was tuned to 0.6 by increasing the switching frequency f_s from 250 kHz to 333 kHz as shown in **Fig. 3-80**. When f_n=0.6 and k=0.2, the full load experimental results with split and overlapped currents were depicted in **Fig. 3-80(a)** and **(b)**, respectively. Compared with the f_n=0.8 case in **Fig. 3-77**, the currents in **Fig. 3-80** (f_n=0.6) have a less curvature, which corresponds to the ideal analysis in **Fig. 3-61**. As shown in **Fig. 3-80(b)**, the current sharing is still good when f_n changes to 0.6. In addition, the half load 6 kW testing results were also given in **Fig. 3-80(c)** and **(b)** with split and overlapped transformer currents, respectively. Either in full load or half load, the current sharing performance remains good.

Finally, the switching frequency f_s was further increased to 500 kHz, and thus, the normalized f_n (f_r/f_s) was reduced to 0.4. As shown in **Fig. 3-81**, compared to f_n=0.8 or 0.6 in **Fig. 3-77** or **Fig. 3-80**, f_n=0.4 case has a "flatter" current because f_r is further away from f_s, and C_r can only cancel a small portion of L_k impedance. **Fig. 3-81(a)-(b)** showed the full load experimental results when k=0.3 and f_n=0.4 with split and overlapped currents, respectively.

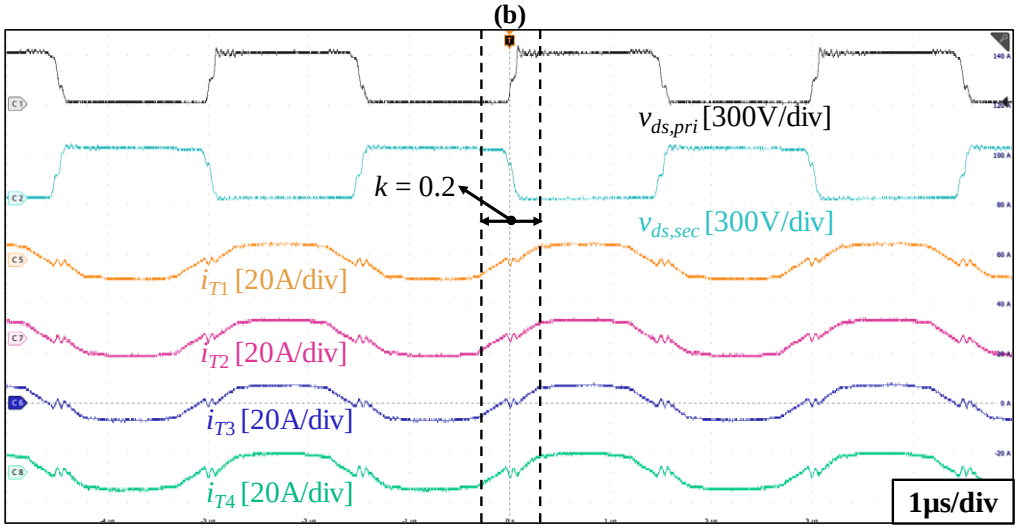
When k decreases to 0.2, the results of the split and overlapped current are shown in **Fig. 3-81(c)** and **(d)**. Similar to the previous analysis, the current sharing performance was still good when f_n=0.4 with different k. The voltage across the LV full bridge was difficult to obtain because of the high-density design, as shown in **Fig. 3-74**. However, the voltage stress reduction with C_r will be verified in the following hybrid RC EET-DCX experimental results in **Fig. 3-82**.



(a)



(b)



(c)

Fig. 3-80. Full load 12 kW and half load 6 kW testing with f_n=0.6 and k=0.2: (a) full load with split currents, (b) full load with overlapped currents, (c) half load with split currents. The corresponding parameters are listed in Table 3-8.

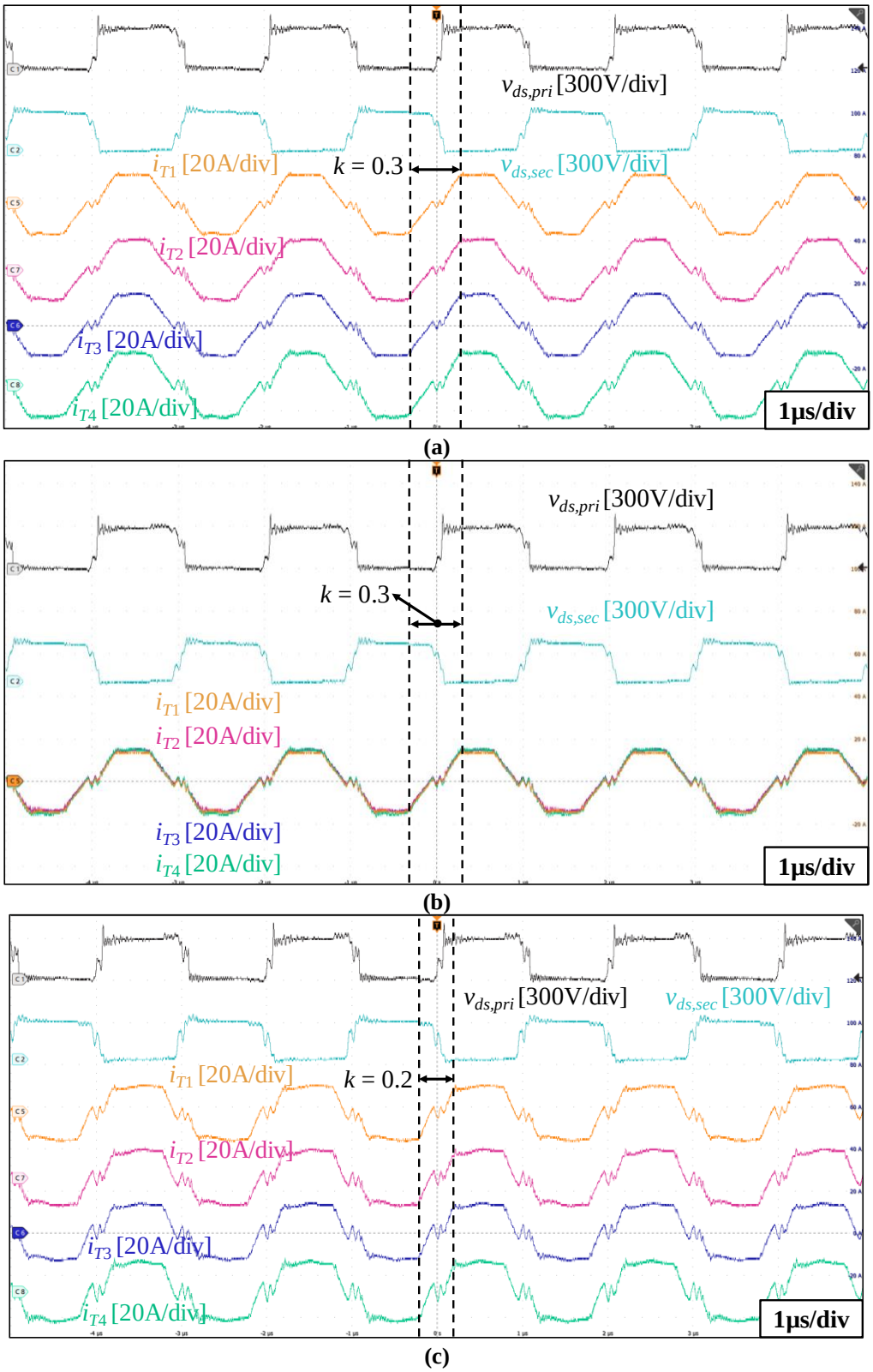


Fig. 3-81. Full load 12 kW results with f_n=0.4: (a) k=0.3 with split currents, (b) k=0.3 with overlapped currents, and (c) k=0.2 with split currents. The corresponding parameters are listed in Table 3-8.

3) Hybrid RC EET-DCX

Since hybrid RC EET-DCX only has one bidirectional AC switch $Q_{1(2)}$, as shown in **Fig. 3-74(b)**, it's feasible to measure the voltage stress across $Q_{1(2)}$. The hybrid RC EET-DCX in this part operates at 333 kHz. Due to the symmetric driving signals for Q1 and Q2, the drain to source voltage can represent $v_{C,rc}$ in the following experimental results. **Fig. 3-82(a)** and **(b)** present the full load (3 kW per unit) and half load (1.5 kW per unit) experimental results of one hybrid RC EET unit with k =0.2 when f_n=0 (without C_r). From the half-cycle resonance voltage $v_{C,rc}$, the resonant commutation was achieved. The maximum voltage stress $V_{b,rc}$ on $Q_{1(2)}$ is 28 V for full load and 16 V for half load. Theoretically, the voltage stress under half load should be half compared to full load. However, in the real case, some circuitry tolerance and measurement errors will lead to this small mismatch.

In order to verify the smaller voltage stress of hybrid RC EET-DCX, an extra C_r was added **Fig. 3-83**. The normalized resonant frequency f_n was changed from 0 to 0.6. As shown in **Fig. 3-83**, with the same k=0.2, the currents $i_{T,rc}$ became curved because of the resonance between C_r and L_k. Compared with f_n=0, the voltage stress $V_{b,rc}$ was dramatically decreased from 28 V to 17 V at full load, and 16 V to 10 V at half load.

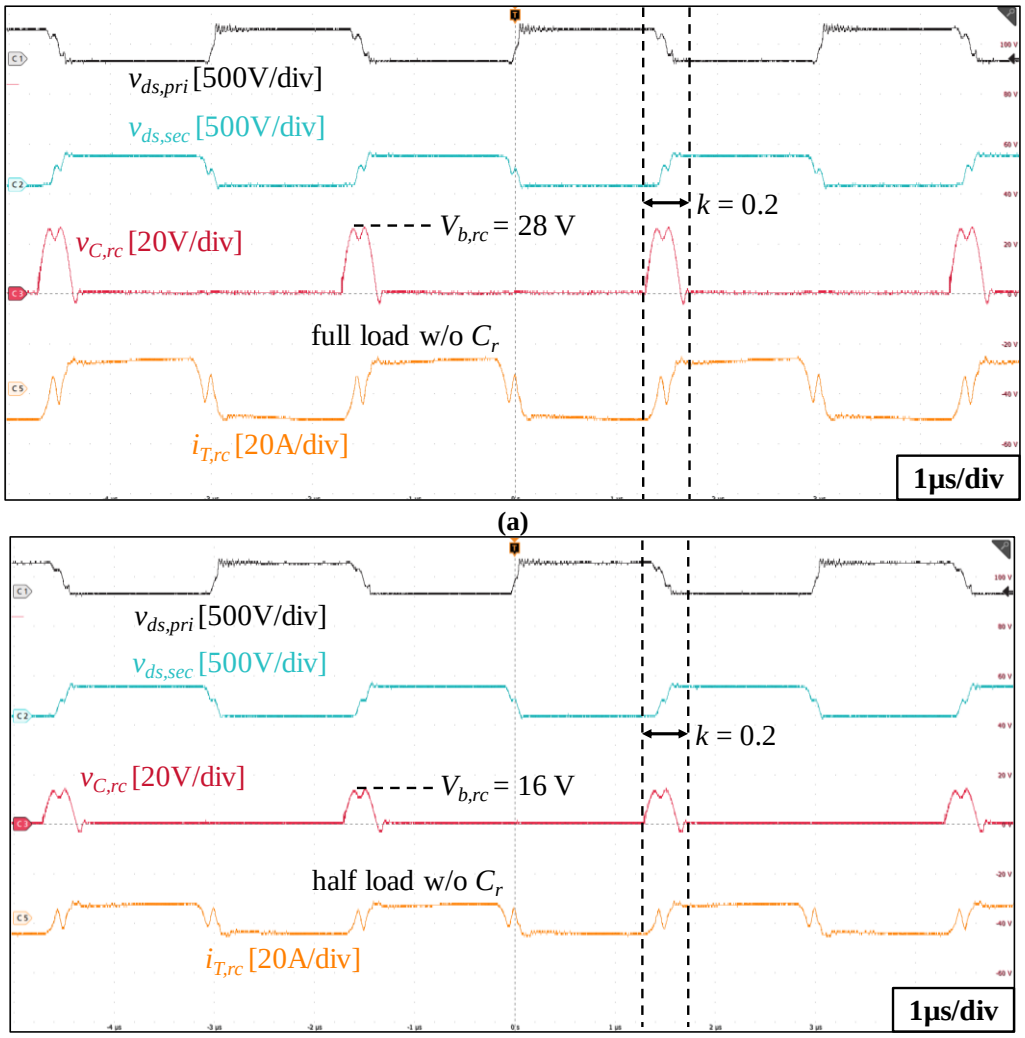


Fig. 3-82. Experimental results for hybrid RC EET-DCX without C_r (f_n=0) when k=0.2: (a) full load (3 kW per unit), (b) half load (1.5 kW per unit). The corresponding parameters are listed in Table 3-8.

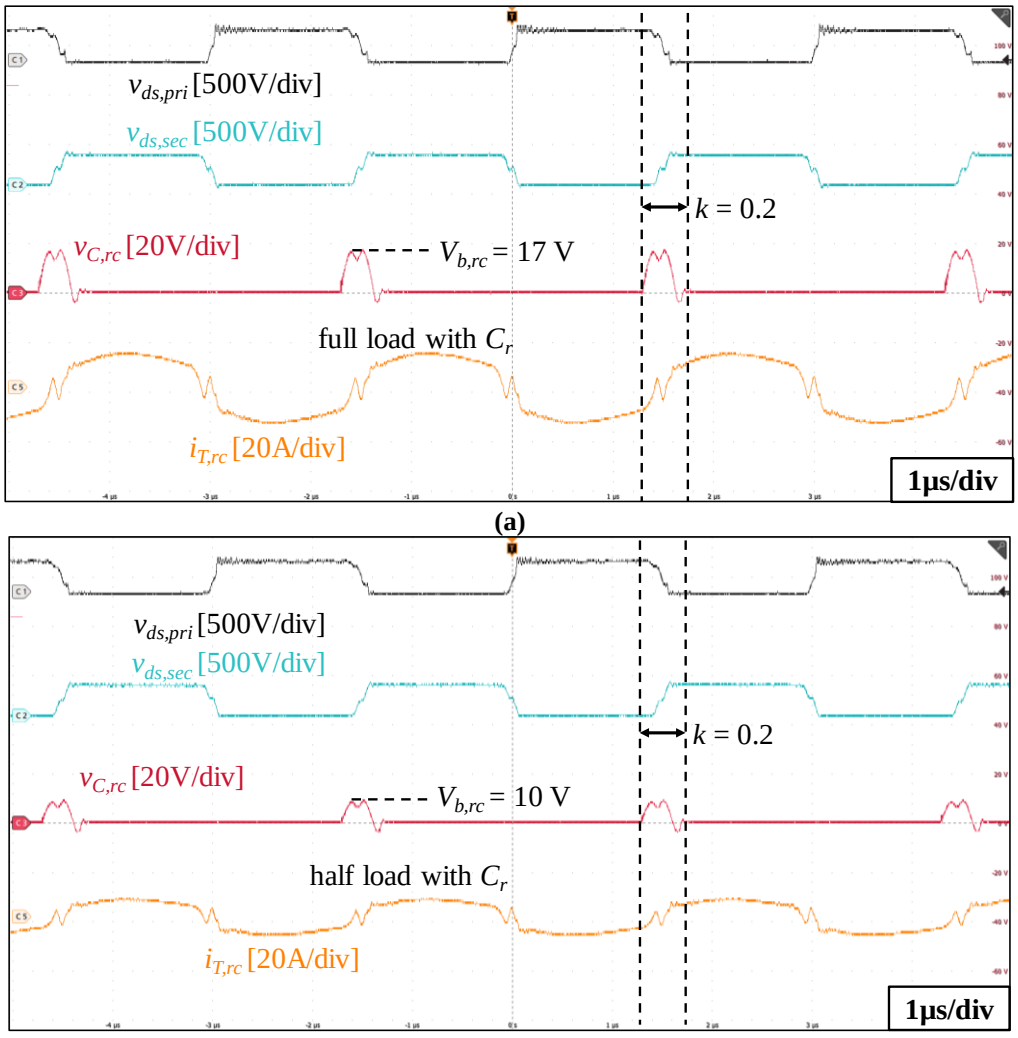


Fig. 3-83. Experimental results for hybrid RC EET-DCX with C_r (f_n=0.6) when k=0.2: (a) full load (3 kW per unit), (b) half load (1.5 kW per unit). The corresponding parameters are listed in Table 3-8.

4) Efficiency Measurement

The measured efficiency of hybrid EET-DCX and hybrid RC EET-DCX were shown in **Fig. 3-84** and **Fig. 3-85**, respectively. In **Fig. 3-84(a)** with f_n=0, the converter could get a higher efficiency with a smaller k. The reason is that a smaller k leads to a smaller rms current based on previous analysis. When f_n is closer to 1, the currents will be more like "sinusoidal" waveforms. For example, when f_n=0, as shown in **Fig. 3-84(b)**, regulating k cannot lead to a big reduction of rms current, and thus, the efficiencies with different k are very close.

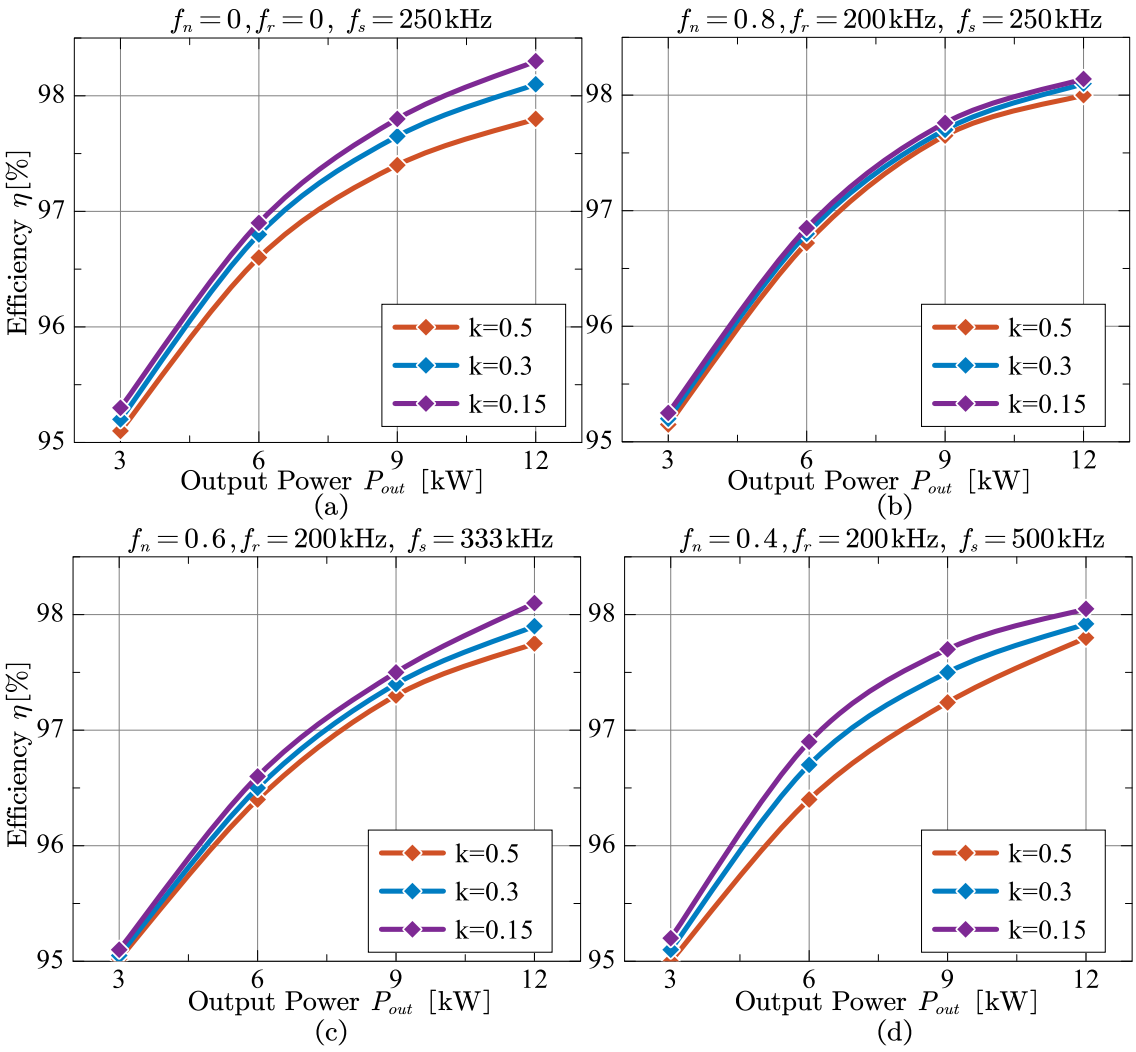


Fig. 3-84. Measured efficiency of hybrid EET-DCX with different f_n and different k: (a) f_n=0, (b) f_n=0.8, (c) f_n=0.6, and (d) f_n=0.4. The corresponding testing results are shown in Fig. 3-75 to Fig. 3-81.

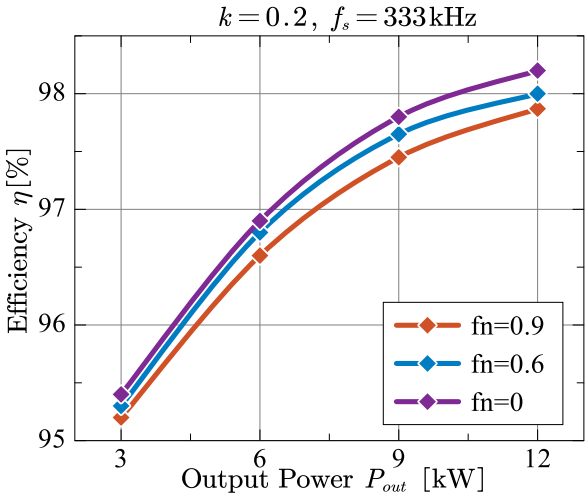


Fig. 3-85. Measured efficiency of hybrid RC EET-DCX with different f_n. The corresponding testing results are shown in Fig. 3-75.

As for f_n=0.6 and f_n=0.4 in **Fig. 3-84(c)** and **(d)**, smaller k can still cause higher efficiency because of the smaller rms current. However, if compared with the f_n=0 case in **Fig. 3-84(a)**, the efficiency with C_r is generally lower. This can be explained in two aspects: one is that the rms current with C_r is inherently smaller than without C_r case based on the previous analysis. On the other hand, since L_k has been minimized to several hundred "nH" levels, the benefit of the voltage reduction on the LV bridge cannot offset the larger rms current. However, in the situation with larger L_k, the merits of RC EET-DCX will be amplified because a large voltage stress on the LV bridge will bring higher switching loss and break down the switch.

The efficiency of hybrid RC EET-DCX is shown in **Fig. 3-85**. Compared to f_n=0.9 and 0.6 cases with the same k=0.2, the f_n=0 case has the highest efficiency. The reason is that the voltage stress reduction cannot bring enough benefit versus the larger rms current. For example, even without C_r, the voltage across the bidirectional AC switch $Q_{1(2)}$ is lower than 30 V. However, the voltage stress is proportional to the leakage inductance L_k. If L_k becomes ten times larger, the voltage applied to $Q_{1(2)}$ will get close to 300 V, which might break down the switch or lead to considerable switching loss.

To summarize, the measured efficiency for both hybrid EET-DCX and hybrid RC EET-DCX are for reference only. In the application with larger L_k, the benefit of the voltage stress reduction with C_r will be more promising.

3.6 Conclusion

In this chapter, a new concept of electronic embedded transformer (EET) was first proposed to address the transformer design trade-off between high frequency and high power. Based on the EET unit, scalable EET-DCX was found with robust current sharing and smaller rms current (compared with LLC/CLLC-DCX). Moreover, the proposed EET-DCX retains the merits of resonant LLC/CLLC-DCX, such as full load range ZVS and load-independent voltage gain.

In light of the EET concept, another resonant commutation (RC) EET-DCX was proposed to streamline the topology. The integrated full bridge in the EET unit was replaced by one bidirectional AC switch, and all merits from EET-DCX were kept in RC EET-DCX.

In order to tackle large leakage inductance or variable leakage inductance cases, hybrid EET-DCX and hybrid RC EET-DCX were both proposed by inserting an external resonant capacitor. Since a large portion of the leakage inductance impedance was compensated by this capacitor, the EET full bridge or RC EET bidirectional switch only needed to handle the remaining impedance.

To sum up, based on the EET concept, a new family of soft-switching DCXs was proposed and verified in this chapter. Compared with state-of-the-art LLC/CLLC-DCX, the obvious benefits are robust current sharing and smaller rms current.

Chapter 4

DCX with Regulation and Implementation

4.1 Introduction

Since a DC transformer (DCX) can only provide a load-independent fixed voltage gain, in many applications that require voltage regulation, a post-regulator is necessary and can be used to control the output voltage. Collaborating with DCX, this section illustrates two typical DCX applications with an EV charging system and an energy storage system.

Firstly, an 18-kW bidirectional EV charger with partial power processing was built with a 98.8% peak efficiency. In this charger, a large portion of the power is handled by DCX, and the remaining partial power will go through a 3-phase interleaved buck converter. The whole partial power converter can realize a very high efficiency because only a small portion of power is processed by the voltage regulator.

Afterward, to handle the step-up and step-down cases at the same time, a symmetric 3-level buck-boost with coupled inductors was also studied as a post regulator. With symmetric topology and quadrangle current control, the converter can achieve a common mode noise reduction and full load range ZVS with a small rms current. To further optimize the performance and simplify the control, a mid-point bridging was implemented with a better CM noise reduction and a split capacitor voltage auto-balance. A 50-kW prototype was built to verify the above analysis.

4.2 18 kW Bidirectional Charger with Partial Power Processing

The demand for high-density, high-efficiency bi-directional battery chargers is driven by the fast development of energy storage systems in renewable energy systems, microgrids, and transportation electrification. An isolated DC-DC converter that interfaces a battery with a variable voltage range is one of the critical components. An input-parallel output-series (IPOS) partial power (PP) converter is considered a promising high-efficiency, high-density solution because only a fraction of power is processed via multi-stage converters to regulate the output voltage. However, due to the tight coupling between two DC transformers (DCXs), the design of the PP converter is complicated. To solve this issue, an overall design procedure for a bi-directional soft-switching resonant-type PP converter is proposed. In the parameters design part, a decoupled design method is proposed to simplify the DCX design. With this method, two DCXs can be designed separately, and a typical optimization method can be easily applied. As for the hardware design part, to minimize the AC loop inductance and resistance, a 2-directions (2-D) flux cancelation method and an "intra-leaving" winding structure are proposed for the circuit layout and HF transformer to obtain high operation efficiency and power density. Finally, the whole design procedure is verified by an 18 kW rated, 25 kW peak prototype operating at 500 kHz. The realized PP converter features a peak efficiency of 98. 8% and a power density of 142 W/in^3.

The paper is organized as follows. **Section 4.2.1** explains the operation principle for the PP converter and proposes the overall design procedure. In order to illustrate this procedure, details of parameters and hardware design are analyzed in **Section 4.2.2** and **4.2.3**, respectively. Subsequently, in **Section 4.2.4**, experimental results are presented, showing the performance of the implemented prototype in steady-state and during dynamic voltage regulation.

4.2.1 Partial Power Converter Design Procedure

As shown in **Fig. 4-1**, the bi-directional resonant isolated IPOS PP converter consists of two CLLC-type resonant DCXs and one post-regulator. The majority power P_{MP} is transferred by the majority power (MP) DCX, and the remaining partial power P_{PP} passes through the PP DCX cascaded with a post-regulator whose output is V_r. The output of MP DCX V_{MP} is in series with the regulator output V_r. Hence, the battery voltage V_{bat} can be derived as:

$$V_{bat} = V_{MP} + V_r \tag{4.1}$$

Since the input power P_{in} is the sum of P_{MP} and P_{PP}, the partial power ratio k is defined as P_{PP} over P_{in} and can be given as

$$k = \frac{P_{PP}}{P_{in}} = \frac{P_{PP}}{P_{MP} + P_{PP}} = \frac{V_r}{V_r + V_{MP}} \tag{4.2}$$

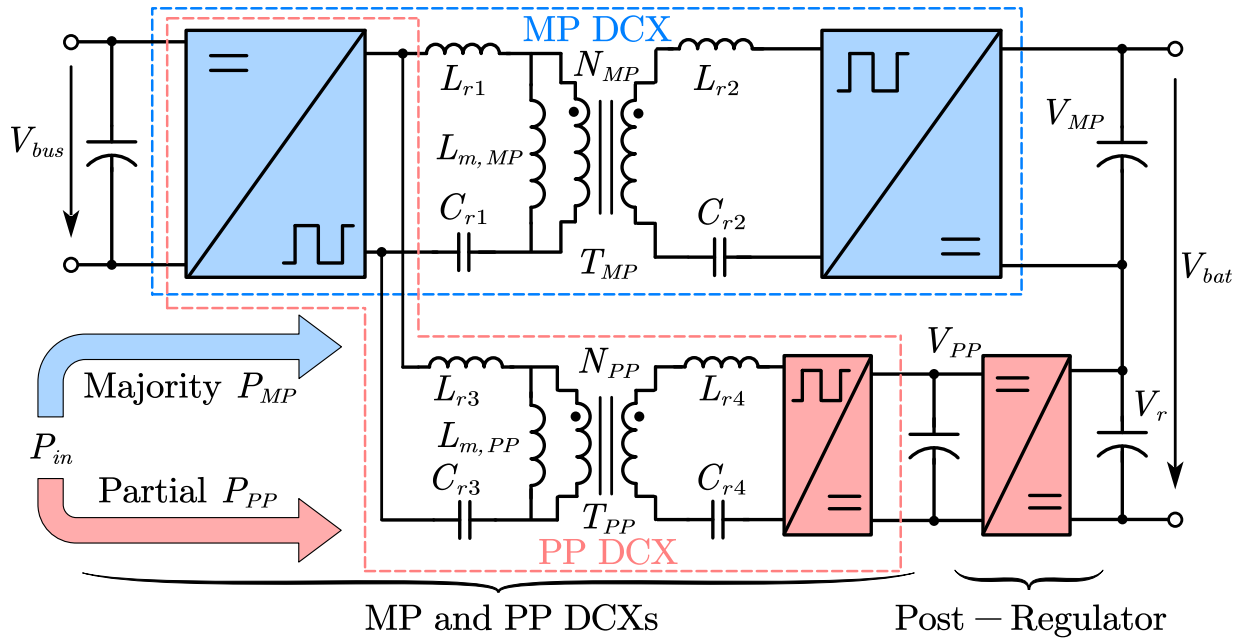


Fig. 4-1. Bi-directional Resonant Isolated IPOS PP Converter.

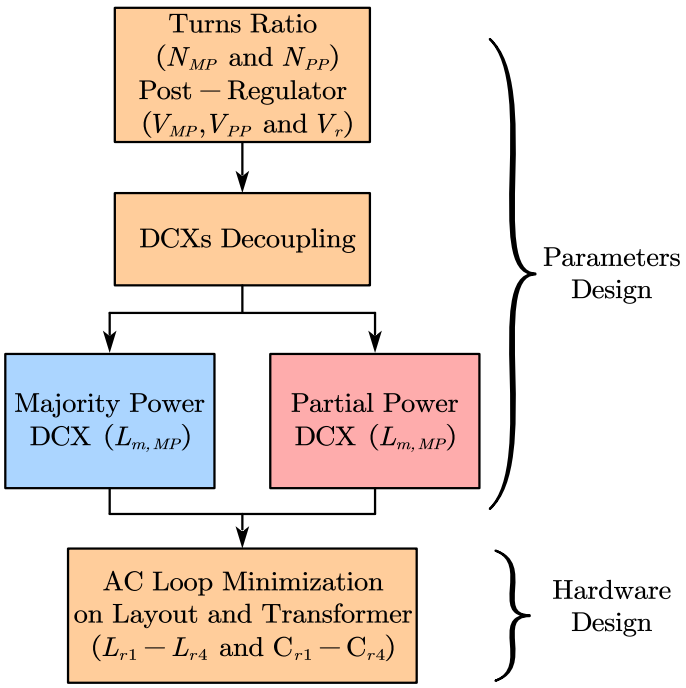


Fig. 4-2. Proposed Design Procedure for PP Converter. The circuit diagram can be found in Fig. 4-1.

Assuming $V_r << V_{MP}$, a majority of the power is transferred by the MP DCX, which can be designed at higher efficiency. Power flow and battery voltage V_{bat} are both controlled by the post-regulator. To maximize the power transfer efficiency, CLLC-type DCX operating at the resonant frequency is selected for both MP and PP DCXs. As the voltage regulation is handled by the post-regulator, the CLLC-type DCXs will operate at a fixed switching frequency near the resonant point, which provides load-independent constant gain and very high efficiency due to small circulating current plus ZVS and close to ZCS. Different from a traditional CLLC and dual active bridge (DAB) converter with a specific leakage inductance requirement for voltage-gain tuning purposes, minimum leakage inductance is desired for the selected DCX operating mode, which can simplify the transformer design process and reduce the resonant capacitor voltage rating requirement. The conventional CLLC-type DCX design procedure has been investigated a lot. However, the design of MP and PP DCXs in the PP converter is more complex because the primary side is shared by two DCXs, as shown in **Fig. 4-1**, and the post-regulator should be considered to match the battery

voltage range. In order to solve this issue, a straightforward design procedure composed of parameters and hardware design is proposed in this paper, as shown in **Fig. 4-2**.

The first step in parameter design is to determine the turns ratios and the post-regulator topology. This is because the turns ratios N_{MP} and N_{PP} of transformers T_{MP} and T_{PP} are dependent on post-regulator topology selection. According to DCX operation principle, turns ratios N_{MP} and N_{PP} can be derived as:

$$N_{MP} = \frac{V_{bus}}{V_{MP}},\ N_{PP} = \frac{V_{bus}}{V_{PP}} \tag{4.3}$$

The second step is to decouple the design of MP and PP DCXs. In this way, the MP DCX can follow the design method of a traditional DCX, while only the conduction loss of PP DCX should be considered because the switching loss of the primary side semiconductors has been totally included in the PP DCX. The parameters design will end with determining the magnetizing inductances $L_{m,MP}$, and $L_{m,PP}$ of T_{MP} and T_{PP}. After the determination of parameter design, hardware design is conducted with the goal of minimizing the AC loop inductance of the circuit and the transformer leakage inductance, which will be counted as the resonant inductors L_{r1}-L_{r4}. The corresponding resonant capacitances, C_{r1}-C_{r4}, can be derived from the resonant frequency f_r.

$$C_{rx} = \frac{1}{4\pi^2 L_{rx} {f_r}^2}\ \ (x = 1, ..4) \tag{4.4}$$

4.2.2 Parameters Design

The specifications of the battery charger are listed in **Table 4-1**. According to the different voltage levels, V_{bus}, V_{MP}, and V_{PP} sides are defined as high voltage (HV), medium voltage (MV), and low

voltage (LV) sides, respectively. Following these specifications and the design procedure shown in **Fig. 4-2**, the post-regulator topology selection and turns ratio design will be illustrated first. Later, the proposed DCXs decoupled design method and DCXs optimization will be given.

1) Post-Regulator and Turns Ratio Design

As a very basic converter, the buck converter has been widely adopted as the post-regulator in PP converters [1]. As shown in **Fig. 4-3**, besides the buck converter, three other potential candidates (multi-phase interleaved buck, full-bridge (FB), and flying capacitor (FC) converter) will be evaluated in this subsection. Considering a reasonable tradeoff between the volume of passive components and switching loss, the switching frequency of the post-regulator f_{reg} is set to 200 kHz. Continuous-conduction mode (CCM) is adopted for all candidates because it does not require a ZCD circuit and has a simple control scheme. For a fair comparison, the DC inductor and switch number in these candidates should be kept the same, so two GaN FETs are paralleled in the buck converter, and two phases are interleaved in the multi-phase buck converter. Among the four candidates, the buck, multi-phase, and FC converter can only provide positive voltage, as shown in **Fig. 4-4(a)**. So V_{MP} and V_{PP} should be set as 300 V and 150 V to match the battery voltage range, and the integer turns ratio N_{MP} and N_{PP} could be selected as 5:2 and 5:1 from Eq. (4.3). In this way, 200 V GaN FETs *EPC2015* should be used to evaluate topology performance of the buck and the multi-phase interleaved buck converter.

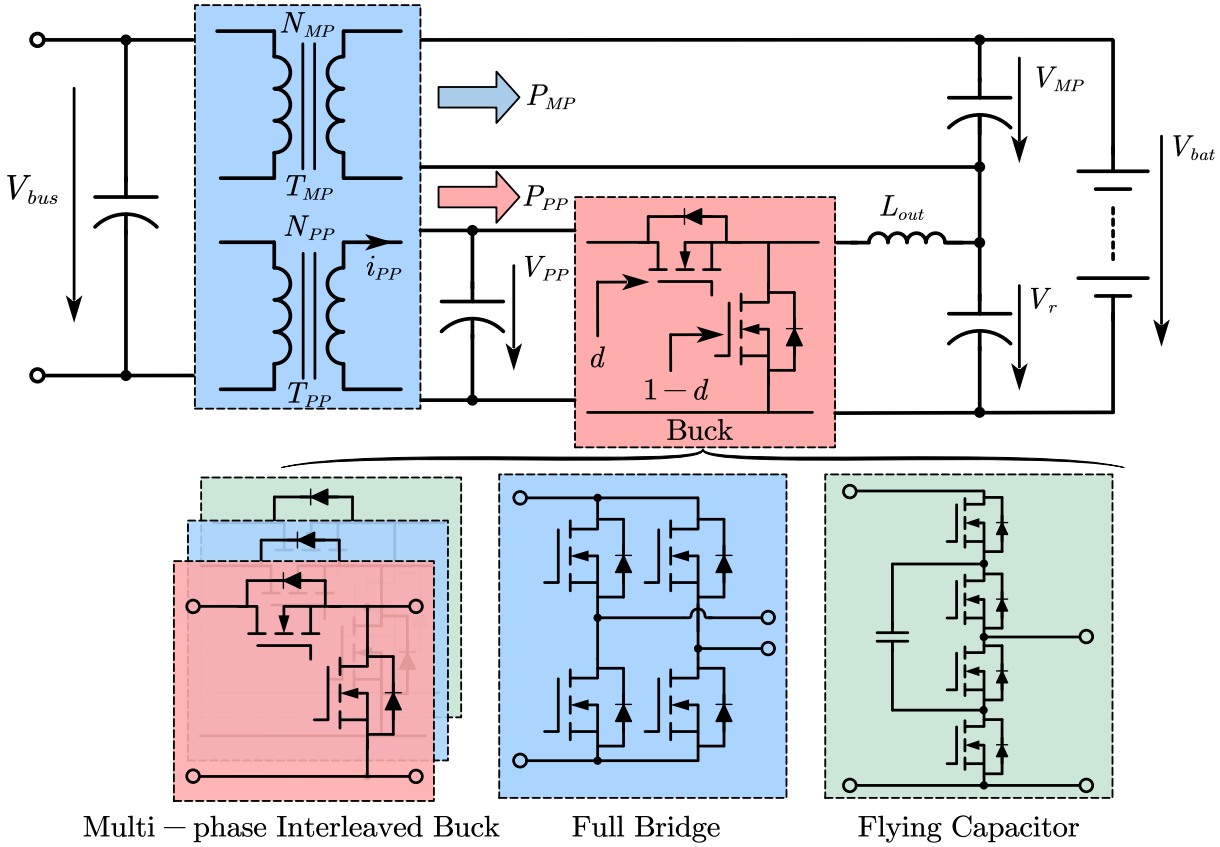


Fig. 4-3. Four potential candidates for post regulator.

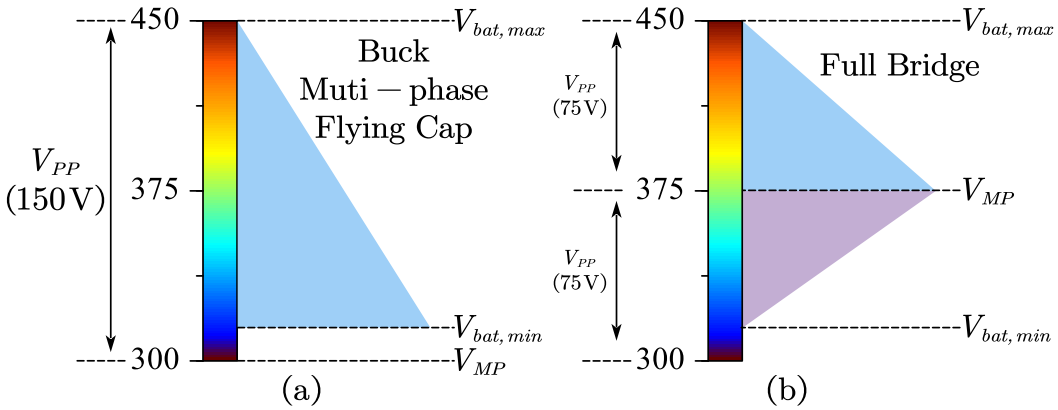


Fig. 4-4. Two turns ratio design (a) N_{MP} = 5:2, N_{PP} = 5:1 (b) N_{MP} = 2:1, N_{PP} = 10:1. The turns ratio can be found in the circuit diagram as shown in Fig. 4-3.

Table 4-1 DESIGN SPECIFICATIONS OF THE BATTERY CHARGER

Variable	Value	Description
V_{bus}	750 V	Nominal DC bus voltage
$V_{bat,nom}$	375 V	Nominal battery voltage
$V_{bat,min}$ - $V_{bat,max}$	314 - 450 V	Battery voltage range
P	18 kW	Rated power at nominal V_{bat}
f_s	500 kHz	Switching frequency for DCX
η_{peak}	98.8%	Target peak efficiency

By contrast, the FB converter works in asymmetrical mode, with one polarity selection phase-leg and another high frequency chopping phase-leg to obtain the bipolar voltage V_r, so V_{MP} and V_{PP} can be set as 375 V and 75 V to cover the whole range of battery voltage as shown in **Fig. 4-4(b)**. In this case, N_{MP} and N_{PP} can be derived as 2:1 and 10:1 from Eq. (4.3). Since V_{PP} is reduced to half, the same switch used within the FC converter is also utilized here. The parameters of the two turns ratios design are listed in **Table 4-2**.

Fig. 4-5(a) shows the semiconductor loss of the post-regulator at rated power (18 kW) with different topologies. Notice that the FB converter has the lowest loss near nominal battery voltage $V_{bat,nom}$ due to zero switching losses at zero duty cycle. With different turns ratio designs at the rated power, the partial power ratio defined in Eq. (4.2) is shown in **Fig. 4-5(b)**. It can be observed that an FB converter with a turns ratio N_{MP} = 2:1 and N_{PP} = 10:1 will process much less partial power near $V_{bat,nom}$. Furthermore, the post-regulator selection will influence the rms value of the current i_{PP}, which goes through the partial power transformer T_{PP},

$$I_{PP,rms} = \frac{\pi}{2\sqrt{2}} \cdot \frac{P \cdot V_r}{V_{bat} \cdot V_{PP}} \tag{4.5}$$

As shown in **Fig. 4-5(c)**, near $V_{bat,nom}$, $I_{PP,rms}$ with an FB converter is smaller, which means the conduction loss at PP DCX will be reduced. Since all the switching losses in DCXs are included in MP DCX, only the conduction loss of PP DCX is considered here.

$$P_{PP_DCX,\,loss} = \underbrace{2 \cdot \left(\frac{I_{PP,rms}}{N_{PP}}\right)^2 \cdot r_{ds,on}}_{\text{primary}} + \underbrace{2 \cdot {I_{PP,rms}}^2 \cdot r_{ds,on}}_{\text{secondary}} \tag{4.6}$$

Therefore, the total loss in partial power loop $P_{PP,loss}$ can be derived as,

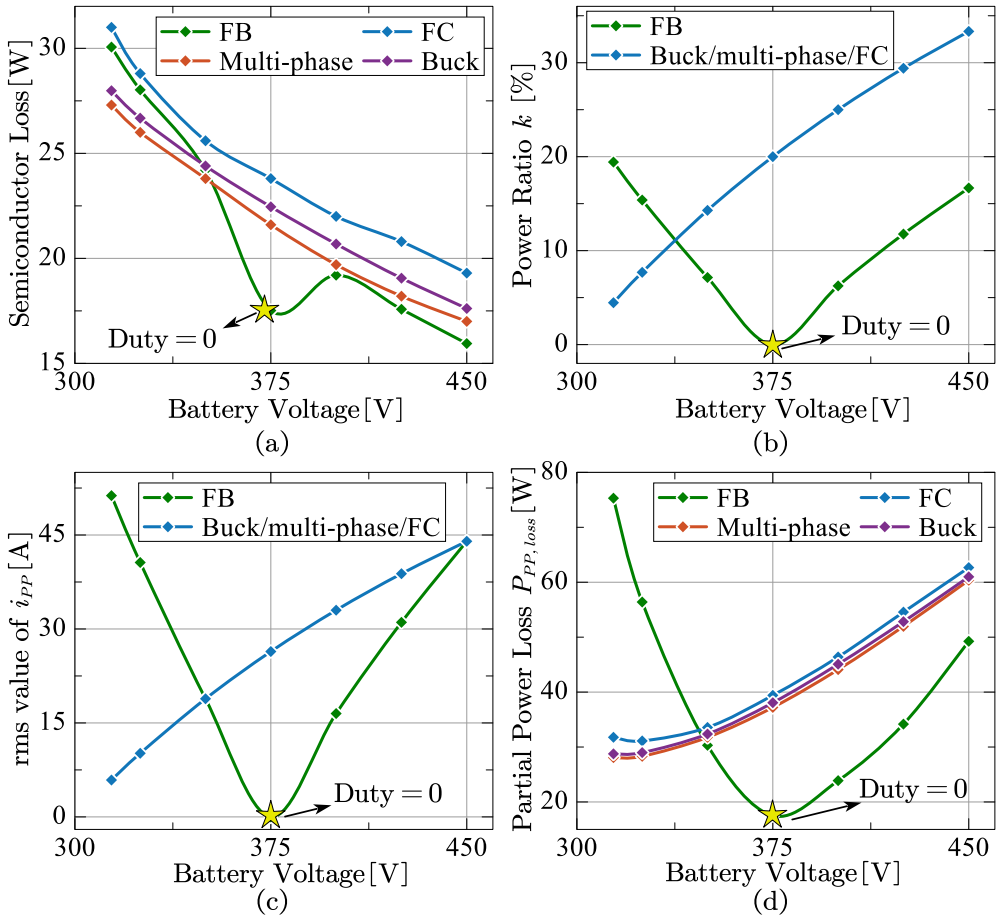


Fig. 4-5. Two turns ratio design with different topologies: (a) post-regulator loss, (b) partial power ratio, (c) rms value of i_{PP}, and (d) total partial power loop loss.

Table 4-2 PARAMETERS OF TWO TURNS RATIOS DESIGN

	V_{MP}	V_{PP}	V_r	N_{MP}	N_{PP}	GaN FETs
Buck Multi-phase	300V	150V	14-150V	5:2	5:1	EPC2215
FC FB	375V	75V	-61-75V	2:1	10:1	EPC2033

$$P_{PP,loss} = P_{PP_DCX,loss} + P_{reg,loss} \tag{4.7}$$

As shown in **Fig. 4-5(d)**, the FB converter has the lowest total partial power loss near $V_{bat,nom}$. Thus, the turns ratio N_{MP} and N_{PP} was selected to 2:1 and 10:1, and the FB converter was adopted as a post-regulator.

2) Post-Regulator Modification

After choosing the turns ratios N_{MP} and N_{PP}, the post-regulator can be modified, as shown in **Fig. 4-6**, to improve the efficiency further. The polarity selection phase-leg can employ a lower on-resistance MOSFET instead of a GaN FET because the switching loss could be ignored. In addition to switch replacement, more phase-legs can be interleaved to improve efficiency and decrease current ripple. The semiconductor loss of the post-regulator with different phase numbers is shown in **Fig. 4-7**. Considering the efficiency and power density, a bipolar 3-phase interleaved buck converter is selected as the post-regulator. Above all, the final design of the PP converter is shown in **Fig. 4-8**.

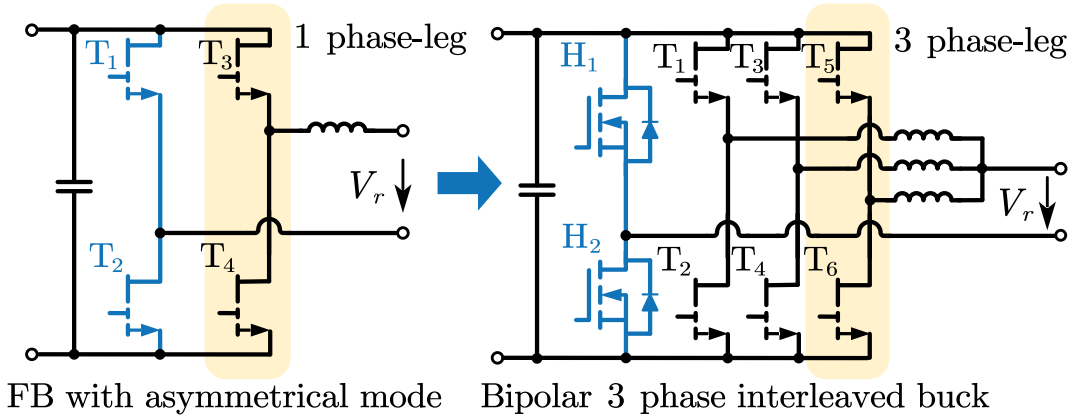


Fig. 4-6. Modification of post-regulator.

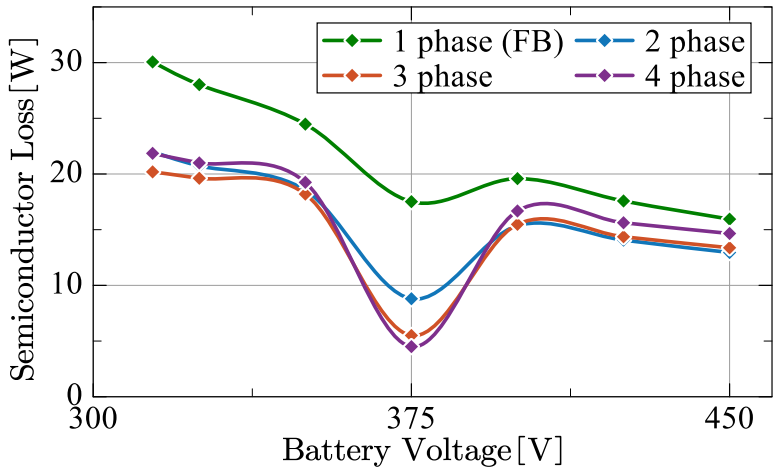


Fig. 4-7. Post-regulator loss with different phase numbers. An example of 3 phase interleaved buck converter is shown in Fig. 4-6.

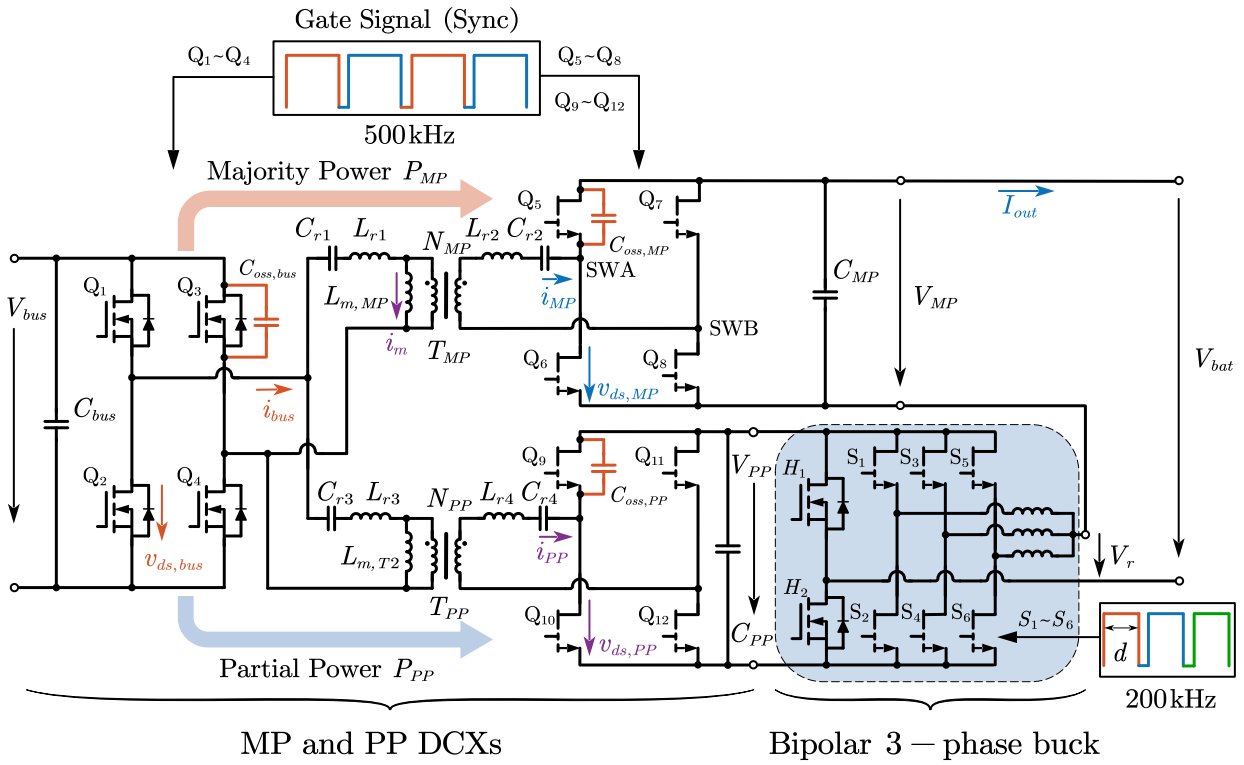


Fig. 4-8. Final design of the PP converter. The simplified circuit diagram can be found in Fig. 4-1.

3) Proposed DCXs Decoupled Design Method

As explained earlier, the MP and PP DCXs are closely coupled together (primary side sharing), which brings a design challenge to achieve ZVS for all twelve switching switches (Q_1-Q_{12}). As a result, the design of magnetizing inductances $L_{m,MP}$, and $L_{m,PP}$ cannot follow a typical optimization procedure. In order to solve this issue, a DCXs decoupled design method is proposed in **Fig. 4-9**. After ignoring the resonant inductance and capacitance (much smaller than $L_{m,MP}$ and $L_{m,PP}$), the equivalent ZVS circuit in **Fig. 4-9(a)** can be simplified as shown in **Fig. 4-9(b)**. In **Fig. 4-9(b)**, $L_{m,MP}$, and $L_{m,PP}$ are connected in parallel to provide a total magnetizing current. To satisfy the ZVS criteria during dead time t_d and achieve minimum conduction loss, the total magnetizing inductances and t_d should meet the following requirements.

$$\frac{L_{m,MP}\cdot L_{m,PP}}{L_{m,MP}+L_{m,PP}}=\frac{t_d}{8f_s\cdot\left(C_{oss,bus}+\frac{C_{oss,MP}}{N_{MP}{}^2}+\frac{C_{oss,PP}}{N_{PP}{}^2}\right)} \tag{4.8}$$

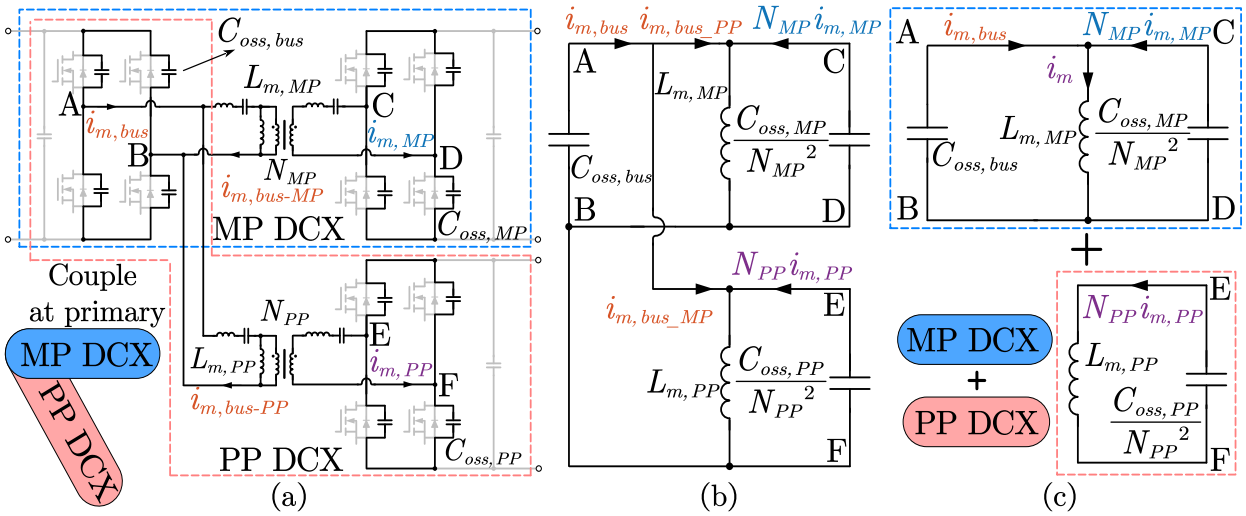


Fig. 4-9. Decoupling Procedure for DCXs (a) Equivalent ZVS circuit during dead time (b) after simplification (c) after decoupling. The whole circuit diagram is shown in Fig. 4-8.

Where $C_{oss,bus}$, $C_{oss,MP}$, and $C_{oss,PP}$ are junction capacitors for each side. The LV side is selected to have a much smaller $C_{oss,PP}$ than $C_{oss,MP}$. Due to the high turns ratio of N_{PP}, the term $C_{oss,PP}/N_{pp}^2$ in Eq. (4.8) is negligible. As shown in **Fig. 4-9(b)**, both $L_{m,PP}$ and $L_{m,MP}$ will contribute to the circulating current during the dead time. If $L_{m,PP}$ can be designed much larger than $L_{m,MP}$, Eq. (4.8) can be simplified,

$$L_{m,MP} = \frac{t_d}{8f_s \cdot \left(C_{oss,bus} + \frac{C_{oss,MP}}{N_{MP}^2}\right)} \tag{4.9}$$

The PP DCX transformer's magnetizing inductance $L_{m,PP}$, can be derived as,

$$L_{m,PP} = \frac{t_d}{8f_s \cdot \frac{C_{oss,PP}}{N_{PP}^2}} \gg L_{m,MP} \tag{4.10}$$

In this way, the design of magnetizing inductances $L_{m,MP}$, and $L_{m,PP}$ can be decoupled, as shown in **Fig. 4-9(c)**. The magnetizing current $i_{m,bus-MP}$, which is much larger than $i_{m,bus-PP}$, will provide almost all the circulating current to achieve ZVS for both MP DCX primary and secondary side

transistors. As such, MP DCX can simply follow the traditional design procedure of a resonant converter. After $L_{m,MP}$ is designed and tuned, $L_{m,PP}$ will be tuned to provide a small magnetizing current $i_{m,PP}$ to enable the ZVS on the PP secondary side LV switching transistors. As for MP DCX, the design procedure can then focus on loss minimization as the loss trade-off exists between a number of switches in parallel and the magnetizing current. Only conduction loss should be considered in PP DCX because switching loss on the primary side has been included in MP DCX.

4) MP DCX and PP DCX Optimization

The design procedure of MP DCX includes the determination of the switch number and the optimization of the corresponding $L_{m,MP}$. Considering the voltage level of MP DCX, 1.2 kV SiC MOSFET *C3M0016120,* and 650V GaN *GS66516T*, are selected due to their low R_{dson} as shown in Table III. The number of primary and secondary side switches in parallel is defined as m_1 and m_2. From Eq. (4.9), dead time t_d can be expressed as a function of m_1, m_2 and $L_{m,MP}$.

$$t_d(m_1,\ m_2,\ L_{m,MP}) = 8 f_s \cdot L_{m,MP} \cdot \left(m_1 \cdot C_{oss,bus} + \frac{m_2 \cdot C_{oss,MP}}{N_{MP}^{\ 2}} \right) \tag{4.11}$$

Because the rms current of primary side $I_{bus,rms}$, and secondary side $I_{MP,rms}$ can also be expressed as a function of m_1 and m_2 and $L_{m,MP}$, the conduction loss of MP DCX is given as:

$$P_{cond,MP}(m_1,\ m_2,\ L_{m,MP}) = 2 I_{bus,rms}^{\ 2} \cdot \frac{r_{ds,SiC}}{m_1} + 2 I_{MP,rms}^{\ 2} \cdot \frac{r_{ds,GaN}}{m_2} \tag{4.12}$$

With ZVS turn-on, MP DCX only has a turn-off loss. Based on the resonant converter operation principle, the turn-off current is equal to the peak magnetizing current $I_{m,peak}$, which can be expressed as:

$$I_{m,peak}(m_1,\ m_2,\ L_{m,MP}) = \frac{V_{bus}}{m_1 \cdot L_{m,MP}} \cdot \frac{T_s - 2t_d(m_1,\ m_2,\ L_{m,MP})}{4} \tag{4.13}$$

The switching loss of MP DCX can be derived as:

$$P_{sw,MP}(m_1,\ m_2,\ L_{m,MP}) = m_1 \cdot f_s \cdot \frac{V_{bus}}{v_{DS,ref}} \cdot E_{off}(I_{m,peak}) \tag{4.14}$$

From Eq. (4.12) and (4.14), the total loss at MP DCX can be expressed as a function of m_1, m_2, and $L_{m,MP}$.

$$P_{loss,MP}(m_1,\ m_2,\ L_{m,MP}) = P_{cond,MP} + P_{sw,MP} \tag{4.15}$$

To optimize the efficiency of MP DCX, **Fig. 4-10** shows the relationship between the total loss of MP DCX with parameters m_1, m_2, and $L_{m,MP}$. Firstly, m_1 is swept from 1 to 4 with m_2 fixed as 4 in **Fig. 4-10(a)**, and next, m_2 is swept from 2 to 5 with m_1 fixed as 2 in **Fig. 4-10(b)**. It can be seen that m_1 and m_2 could be selected as 2 and 4 to achieve the best trade-off between power density, efficiency, and paralleling difficulty. In **Fig. 4-10**, at the same time, from the selected "U shape" curve of m_1 = 2 and m_2 = 4, the value of $L_{m,MP}$ can be optimized around 20 μH. From Eq. (4.11), the corresponding dead time t_d can be optimized around 100 ns. **Fig. 4-11** depicts the simulated voltage and current waveforms (shown in **Fig. 4-8**) together with the gate signals of all switches in MP DCX, which verifies the effectiveness of the designed parameters.

As for PP DCX optimization, from Eq. (4.6), the relationship between PP DCX loss and battery voltage with different parallel numbers is plotted in **Fig. 4-12**. It is reasonable to select 2 transistors in parallel here. The final optimization results of MP DCX and PP DCX are listed in **Table 4-3**.

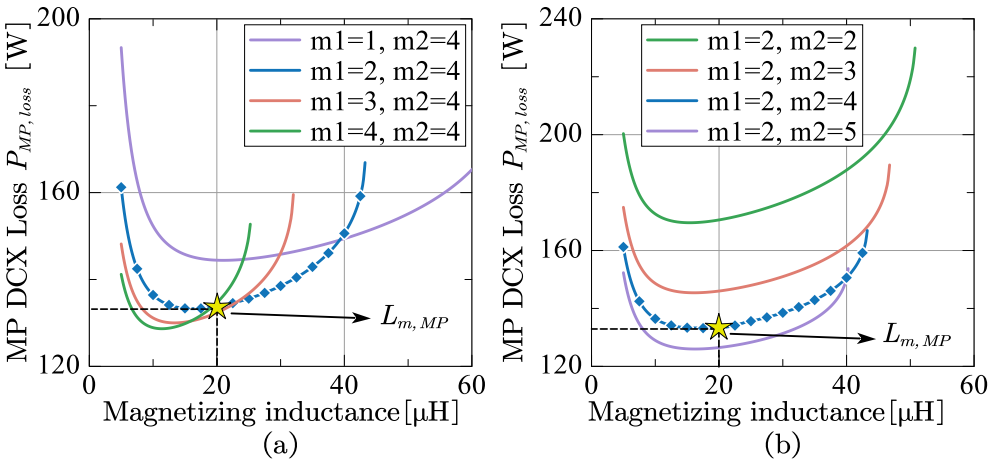


Fig. 4-10. Relationship between MP DCX Loss and magnetizing inductance with different switch parallel numbers, (a) sweep m_1, (b) sweep m_2.

Table 4-3 OPTIMIZATION RESULTS OF MP AND PP DCX

	Switch	C_{oss}	Description	Parallel No.
MP DCX	C3M0016120	418 pF	1.2 kV (17 mΩ)	2
	GS66526T	276 pF	650 V (25 mΩ)	4
PP DCX	EPC2033	900 pF	50 V (15 mΩ)	2

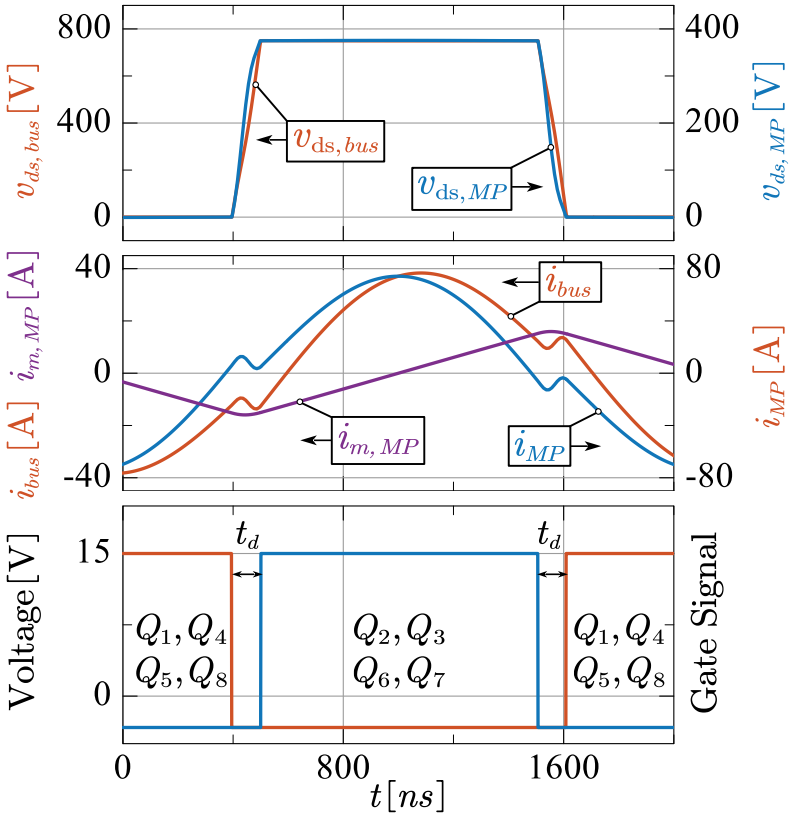


Fig. 4-11. Simulated voltage and current waveforms of the MP DCX at 18 kW together with the corresponding gate control signals ($L_{m,MP}$ =20 μH and t_d =100 ns). The related parameters are listed in Table 4-3.

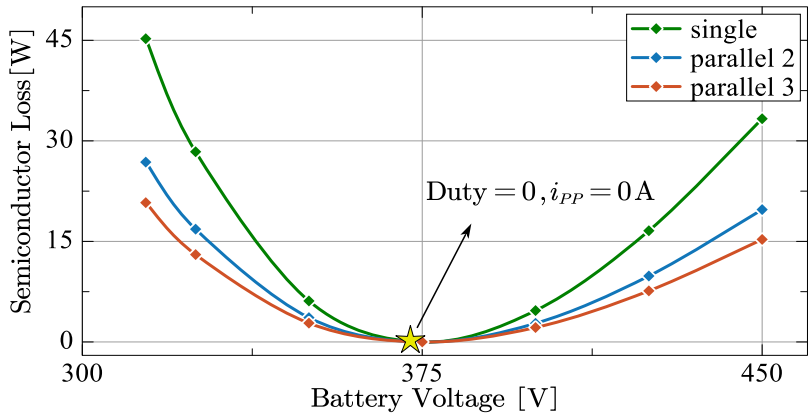


Fig. 4-12. Relationship between PP DCX loss and battery voltage with different parallel numbers.

4.2.3 AC Loop Inductance and Resistance Minimization

As discussed before, small AC loop inductance will result in less voltage stress on the resonant tank and smaller current ringing, which can improve efficiency and maintain load-independent voltage gain for DCX. The ac loop inductance consists of two parts: ac loop stray inductance from the full-bridge circuit and leakage inductance from the high frequency (HF) transformer. In addition to the AC loop inductance, the AC loop resistance, which introduces extra loss and increases thermal stress, should be minimized as well.

1) Proposed 2-D flux cancelation method for MV side

The secondary side of MP DCX is realized with 650 V, 25 mΩ GaN transistor *GS66516T* from *GaN System* because they offer a low ON-state resistance, a low inductance package, a top-side cooled configuration, and dual gate pads for optimal board layout. Following the optimization results in Table III, each switch on the secondary side consists of four parallel *GS66516T* GaN transistors. To optimize the stray loop inductance L_{stray} and ac resistance $R_{ac,stray}$ in the full-bridge circuit, a 2-D flux cancelation method, as shown in Fig. 4-13, is proposed and applied in the multi-layer printed circuit board (PCB) layout. The key point is to achieve current interleaving between adjacent layers.

Fig. 4-13 shows both the cross-section and top view of the PCB layout, where the horizontal and vertical directions are defined as "*x*" and "*y*" directions. The complete AC loop from terminal SWA to SWB is marked with dotted arrows, and four sequential segments in the AC loop are defined as follows.

The proposed method can realize flux cancellation in both the "x" and "y" directions. In the "*x*" direction at HB1, the ac current direction of segment 1 in the Top layer is opposite to that of segments 2 and 3 in the Mid 1 layer. A similar flux cancellation is also true for segments 2 (3) and 4 at HB2. In the "y" direction, the AC current direction of segment 1 Mid 3 layers is opposite to that of segment 4 (Mid 2). Compared with the existing 1-D flux cancelation layout for the same GaN transistor in [28]-[30], this proposed method achieves flux cancelation in both the "x" and "y" directions and has lower loop inductance and ac resistance under the same power level.

It should be noted that for both HB1 and HB2, there are always two layers reserved for each AC trace to handle the large 500 kHz AC current (peak value is close to 80 A). One of the two parallel layers is on the outer surface (for heat dissipation). For example, the top layer and bottom layer are assigned to SWA and SWB, respectively. Considering the skin effect at 500 kHz, the copper thickness for each layer is selected to 105 μm (3 oz). The manufactured PCB board for this layout is also shown in **Fig. 4-13**; in addition to HB1 and HB2, it also includes the DC-link capacitors and the resonant capacitors, which are both placed at the bottom side. As can be seen, the secondary circuit of MP DCX is highly compact with dimensions of only 110 × 60 mm.

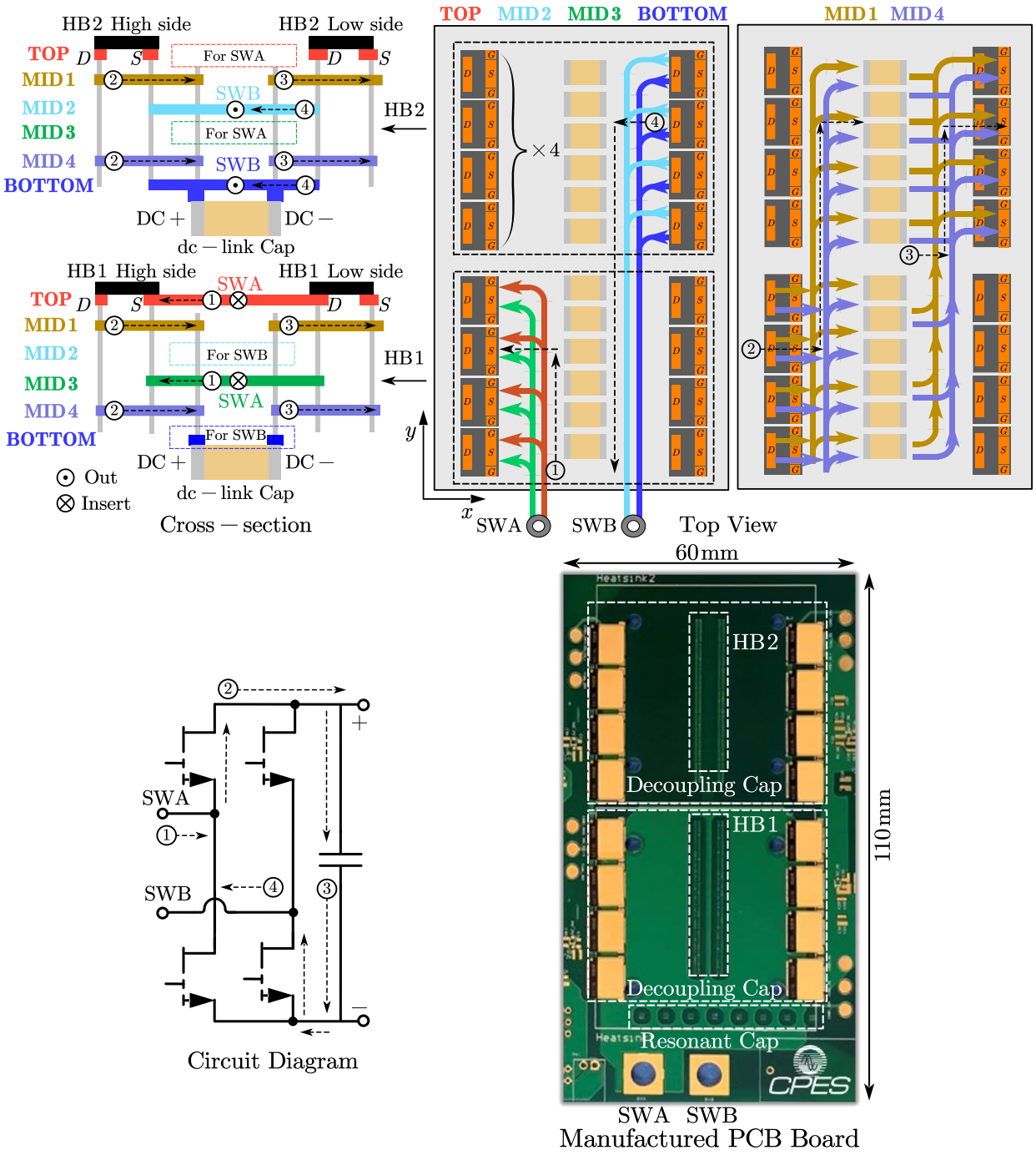


Fig. 4-13. Proposed 2-D flux cancelation method for 650 V GaN-based full-bridge layout.

2) Comparison with other layout methods

In addition to the proposed layout method in **Fig. 4-13**, there are three other possible layouts, as shown in Fig. 4-14, if two parallel layers are to conduct AC and one layer of AC trace is placed in the out layer (following the same rule). Due to the symmetrical structure, the results are equivalent regardless of whether the ac trace SWA is placed on the Top layer or Bottom layer. Thus, one layer of SWA and one layer of SWB are fixed on the Top and Bottom layers, respectively. With Q3D simulation based on the PCB layout, the loop inductance L_{stray} and ac resistance $R_{ac,stray}$ at 500 Hz with all four layouts are shown in **Table 4-4**. One flux cancelation pair is defined as two adjacent layers that have the opposite current direction.

Compared with the proposed 2-D flux cancelation method in **Fig. 4-13**, method 1 shown in **Fig. 4-14(a)** has less flux cancelation pair in the "x" direction, which causes larger loop inductance and AC resistance as listed in **Table 4-4**. Although method 2 has the same pairs as the proposed method, it still has larger Lstray and Rac, which $_{stray}$ because of an asymmetrical structure. Since only 2 pairs in the "x" direction and no pair in the "y" direction, method 3 in **Fig. 4-14(c)** has the worst performance among these four layout methods.

In addition to parasitic parameters, as shown in **Fig. 4-15**, the surface loss density on each ac trace layer is also simulated in Q3D using the 500 kHz, 80 A peak value current excitation. Compared with the other three methods, the proposed layout in **Fig. 4-13** has the best current sharing between two parallel layers, as shown in **Fig. 4-15(a)**, which is consistent with the results in **Table 4-4**.

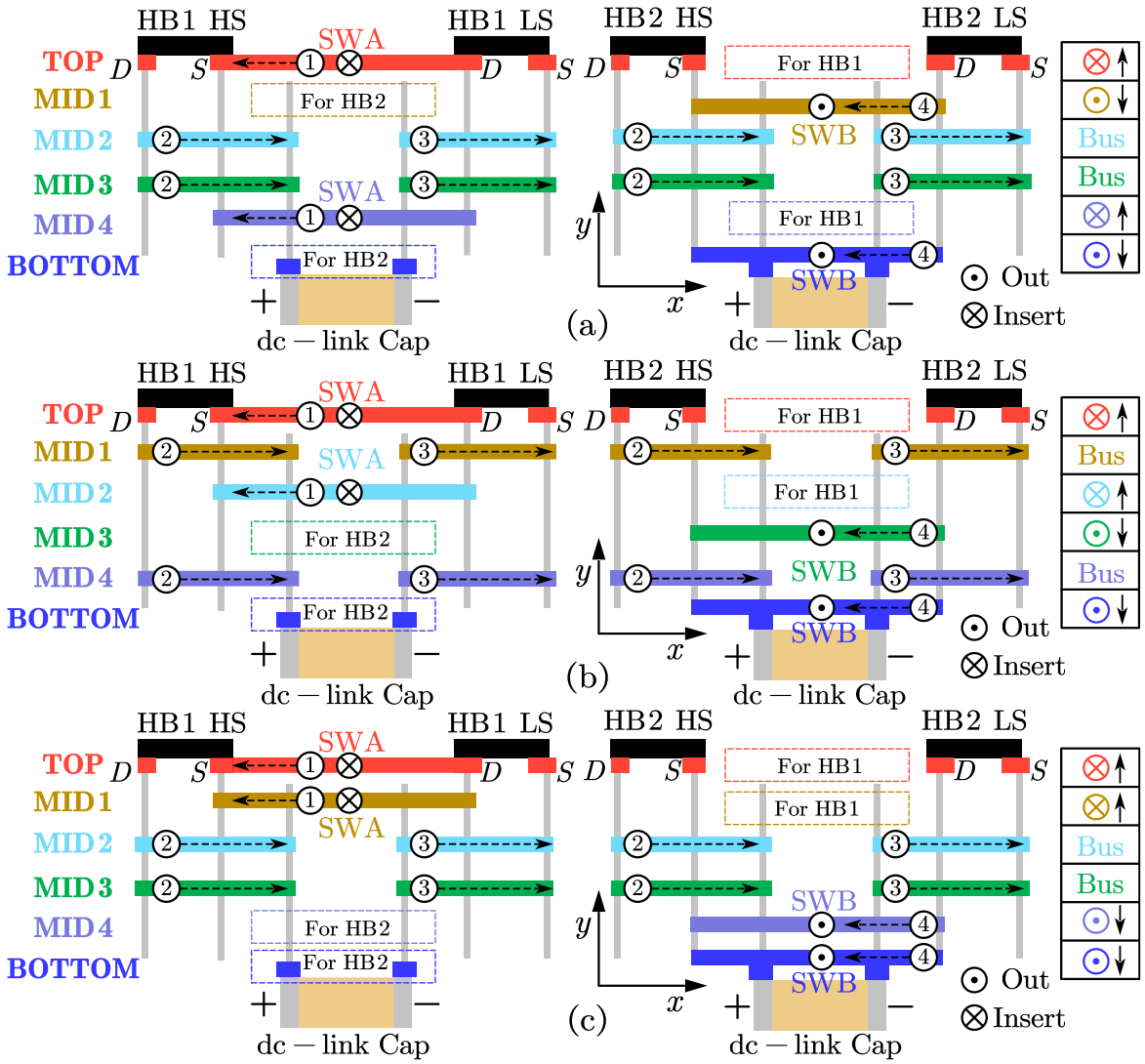


Fig. 4-14. Cross-section of other three possible layouts for 650 V GaN-based full-bridge: (a) method 1, (b) method 2, and (c) method 3. The proposed method for comparison can be found in Fig. 4-13.

Table 4-4 Q3D RESULTS OF PARASITIC PARAMETERS

Layout methods	Flux cancelation pair		L_{stray}	$R_{ac,stray}$
	"x"	"y"		
Proposed 2-D Method	4	1	4.24 nH	0.57 mΩ
1	2	2	4.56 nH	1.24 mΩ
2	4	1	5.68 nH	0.88 mΩ
3	2	0	6.25 nH	1.69 mΩ

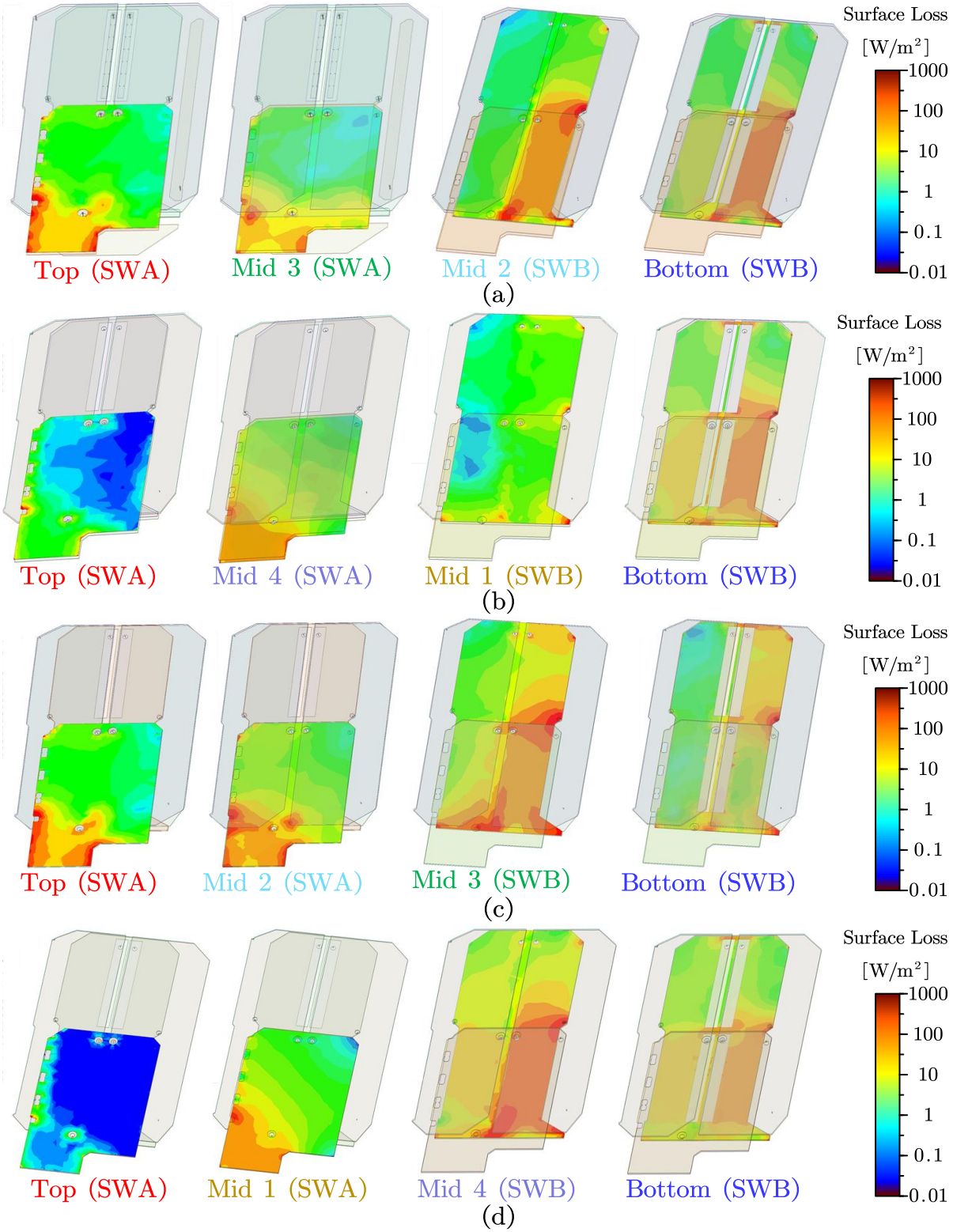


Fig. 4-15. Q3D simulation results for surface loss density: (a) proposed 2-D flux cancelation method, (b) method 1, (c) method 2, (d) method 3. The corresponding layout methods can be found in Fig. 4-13 and Fig. 4-14.

3) Transformer Loss and Leakage Inductance Optimization

The goal of this section is to design a low-profile, high-efficiency transformer with low leakage inductance L_{kp} and L_{ks}. To avoid the large cost of custom cores, the transformer design in this paper will use commercial off-the-shelf (COTS) cores. The design starts with the selection of a magnetic core material and litz wire for high-efficiency operation. Ferroxcube 3F36 was chosen due to its flat core loss from 60 ^{o}C to 100 ^{o}C, which minimizes the risk of thermal runaway. Falco Electronics 1200/44 litz wire is chosen to mitigate the impact of skin effect on wire loss. To improve the window fill factor for high power density, an identical litz wire is chosen for both the primary and secondary sides of the MP transformer. Windings are paralleled on the secondary side to handle the peak current of 56 A_{RMS}. The turns ratio N_{MP} is 2:1, as determined before. The core and winding losses are swept to determine the optimal number of turns for the T_{MP} primary sides $N_{P,MP}$. Winding and core loss are calculated using the Improved General Steinmetz Equation (IGSE) [57] and Square Field Derivative (SFD) [58]. As discussed in [59]–[62], interleaving is an effective strategy to minimize leakage inductance and reduce winding loss since it lowers total magnetomotive force (MMF). Thus, the turns sweep is conducted using maximum interleaving, as shown in **Fig. 4-16**. Loss sweep results are shown in **Fig. 4-17**. $N_{P,MP}$ of 6 and 8 give the lowest total loss of 71 W and 65 W, respectively in order to achieve a highly compact design, a planar E core is selected for a detailed leakage inductance winding configuration study.

Fig. 4-18 shows six different winding topologies considered based on the planar E core. The six winding topologies are compared in terms of leakage inductance, total loss, current sharing, and power density. For all six winding topologies, there is one primary (red) and two parallel secondary S_1 (green) and S_2 (blue). Finding individual leakage inductance for multi-winding transformers requires complex models and is computationally inefficient. As shown in [61], [62], the energy

method based on Poynting's theorem of conservation of energy for a magnetic field is used to survey winding topology leakage inductance,

$$E = \frac{1}{2} L_{kp} {I_p}^2 = \frac{\mu}{2} \iiint_V H^2 dV \tag{4.16}$$

Where E is total energy, L_{kp} is leakage inductance referred to the primary side, I_p is primary current, V is system volume, and H is magnetic field strength. The total loss and L_{kp} from finite element analysis (FEA) simulation are shown in **Fig. 4-19**. Considering the tradeoff between transformer loss and L_{kp}, winding topology 1 (PS_1PS_2) with 70 W total loss and L_{kp} = 770 nH is chosen. However, due to the high operating frequency (500 kHz), any small variation in leakage inductance between parallel windings will create a large mismatch in impedance and, in turn, poor current sharing. The current sharing for the 2 parallel secondary winding of winding topology 1 is simulated and listed in Table. V. For topology 1 (PS_1PS_2), winding S_1 takes 62 A_{peak} current while S_2 takes 18 A_{peak} current. Uneven current sharing will cause damage to the litz wire insulation since it will be operating far beyond its rated current.

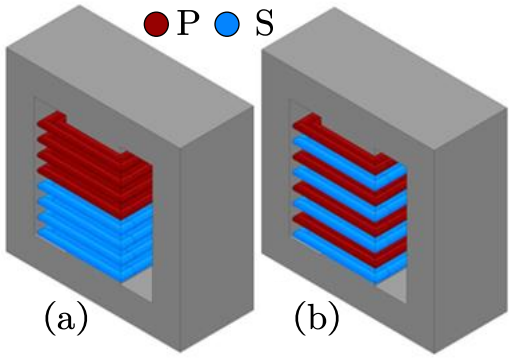


Fig. 4-16. Winding structures: (a) non-interleaved, (b) maximum interleaved.

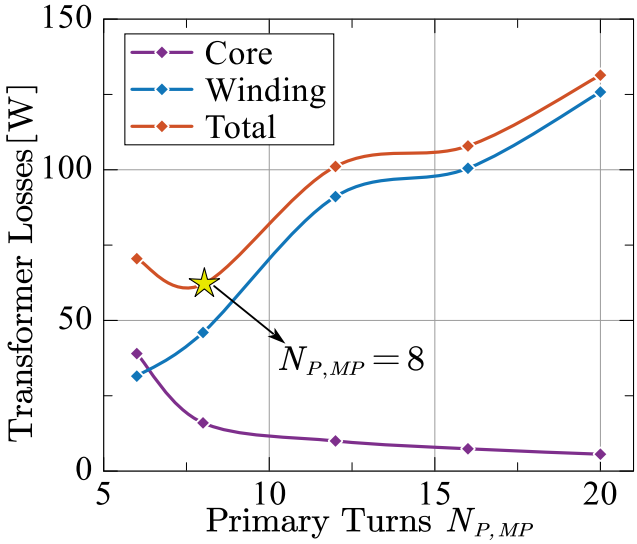


Fig. 4-17. The relationship between transformer losses and primary turns. The corresponding winding structures with different configurations can be found in Fig. 4-18.

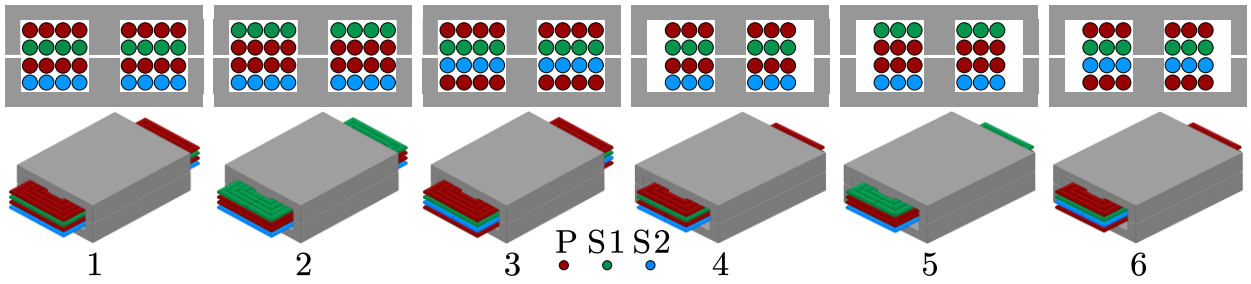


Fig. 4-18. Six potential winding topologies for planar E core. The loss breakdown with these structures is shown in Fig. 4-17.

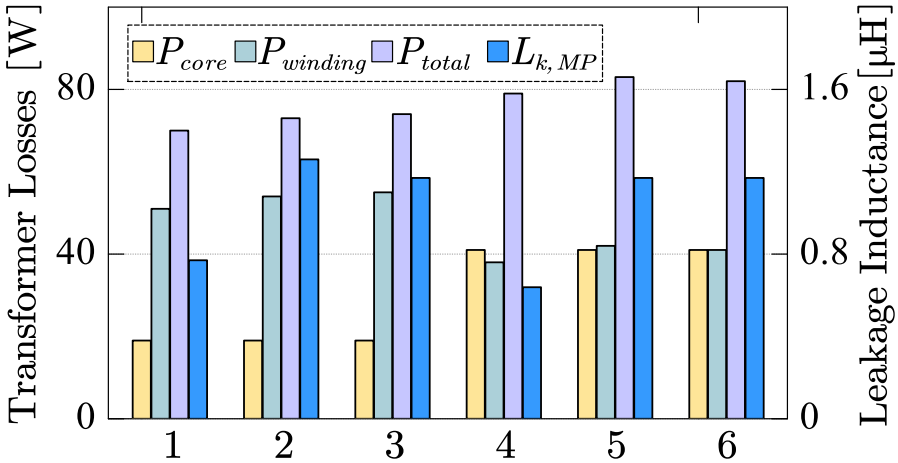


Fig. 4-19. FEA simulation results for transformer losses and leakage inductance with six potential topologies in Fig. 4-18.

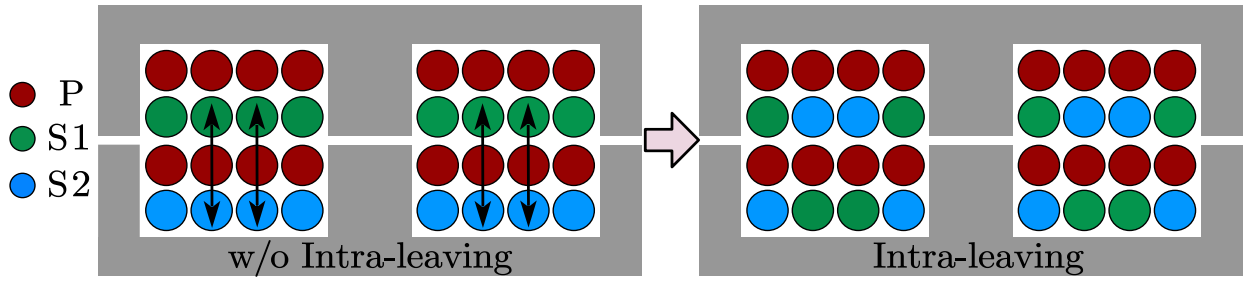


Fig. 4-20. The proposed "intra-leaving" PSPS structure is where the positions of S_1 and S_2 alternate with each turn within a layer, as opposed to interleaved, which only alternates winding positions between layers.

Table 4-5 CURRENT SHARING PERFORMANCE AND COUPLING COEFFICIENT

	w/o intra-leaving (topology 1)		w/ intra-leaving	
	S_1	S_2	S_1	S_2
Peak current	62	18	44	36
k_c	0.991	0.965	0.989	0.988

4) Proposed Intra-leaving Winding Structure

To solve uneven current sharing and achieve low L_{kp} at the same time, an "intra-leaving" winding structure is proposed in this section. Instead of paralleling 2 secondary layers as shown in topology 1, S_1 and S_2 are directly paralleled within a given layer, as shown in **Fig. 4-20**. At the end of each turn, the positions of S_1 and S_2 are interchanged to avoid winding impedance mismatch. With the "intra-leaving" structure, the coupling coefficients k_c for P to S_1 and S_2 are almost equal as listed in **Table 4-5**, implying well-matched winding impedance between parallel windings. Current sharing simulations for the "intra-leaving" structure show winding S_1 and S_2 taking 42 A_{Peak} and 38 A_{Peak}, respectively. Compared with the non "intra-leaving" topology 1, the "intra-leaving" structure has better current sharing performance. In addition, since the MMF distribution of these two structures is the same, the L_{kp} values should be similar. To balance L_{kp}, efficiency, and current sharing, planar E core with the proposed "intra-leaved" PSPS is chosen as the final design.

4.2.4 Hardware Prototype and Experimental Results

1) Prototype Implementation

As shown in **Fig. 4-21**, an 18 kW-rated 25 kW-peak PP converter with a total density of 142 W/in^3 was built first. The technical details of the implemented PP converter are listed in **Table 4-6**. Following a similar optimization procedure to T_{PP}, the primary and secondary turns number of T_{PP} are designed as 10 and 1. To lower flux density and achieve a low-profile design, two planar E cores E38/8/25 in parallel are selected. With the proposed decoupled method from Eq. (4.9) and (4.10), $L_{m,MP}$ and $L_{m,MP}$ could be optimized to 22.4 µH and 180.2 µH. The corresponding air gaps for $T_{m,MP}$ and $T_{m,MP}$ are implemented as 700 and 100 µm, respectively. Then, resonant inductances L_{r1}-L_{r4} are measured by an impedance analyzer, and the resonant capacitors C_{r1}-C_{r4} could be derived from Eq. (4.4). As for the dc-link capacitor C_{bus} at 1.2 kV SiC board, only two 12 µF 900 V film capacitors in parallel is enough to absorb the HF half-sinusoidal current. As for the DC-link capacitors C_{MP} and C_{PP} at 650 V/150 V GaN side, ceramic capacitors and film capacitors are both utilized to shorten the distance from the bridge AC terminals to the DC buses. At the post-regulator side, the value of the output filter capacitor C_r is reduced by 3-phase interleaving; thus, only ceramic capacitors are used. To improve the power density, a commercial inductor with a low profile has been selected. Since the primary side only takes half of the current compared with the secondary side in MP DCX, all 1.2 kV SiC MOSFETs could share one compact heatsink with a co-axial fan. As for the 650 V GaN side, two low-profile heatsinks with fans are adopted to cover a total of 16 switches. Finally, for the 150 V GaN module board, as shown in Fig. 4-21, a local heatsink was selected to cover one phase-leg heat dissipation.

Table 4-6 TECHNICAL DETAILS OF IMPLEMENTED PP CONVERTER

	Component		Parameter	Description
Transformer	T_{MP}	core	E43/10/28 × 2	Ferroxcube 3F36 with 700 μm air gap
		Pri. turns	8	1200/44 HF-litz wire
		Sec. turns	4	1200/44 HF-litz wire (2 parallel)
		$L_{m,MP}$	22.4 μH	Magnetizing Inductance
	T_{PP}	core	E38/8/25 × 2	Ferroxcube 3F36 with 100 μm air gap
		Pri. turns	10	1200/44 HF-litz wire
		Sec. turns	1	1200/44 HF-litz wire (2 parallel)
		$L_{m,PP}$	180.2 μH	Magnetizing Inductance
Resonant Tank		L_{r1}	730 nH	Leakage Inductance at T_{MP} Primary
		C_{r1}	10 nF × 12	1 kV C0G 2220 MLCC
		L_{r2}	181 nH	Leakage Inductance at T_{MP} Secondary
		C_{r2}	33 nF × 13	1 kV C0G 2220 MLCC
		L_{r3}	3.5 μH	Leakage Inductance at T_{PP} Primary
		C_{r3}	4.7 nF × 5	1.2 kV C0G 2220 MLCC
		L_{r4}	37.8 nH	Leakage Inductance at T_{PP} Secondary
		C_{r4}	0.1 μF × 22	630V C0G 2220 MLCC
DC Capacitors & DC Inductance		C_{bus}	12 μF × 2	900 V Film Capacitor
	C_{MP}	$C_{MP,film}$	5 μF	500 V Film Capacitor
		$C_{MP,mlcc}$	1 μF × 18	630 V X7R 2220 MLCC
	C_{PP}	$C_{PP,film}$	33 μF	160 V Film Capacitor
		$C_{PP,mlcc}$	0.47 μF × 30	250 V X7R 1210 MLCC
		C_r	0.47 μF × 16	250 V X7R 1210 MLCC
		L_{buck}	10 μH × 3	22 A Fixed Inductor
Cooling System	R_{th}	HV side	1.6 K/W	30×30×100 mm^3
		MV side	0.38 K/W × 2	48.5×48.5×23 mm^3
		LV side	1.03 K/W × 5	25× 25×27.9 mm^3
	Fan	HV side	12 V DC	30×30×10 mm^3 (5.5 CFM)
		MV side	12 V DC × 2	40× 40×10 mm^3(10 CFM)
		LV side	5 V DC × 5	20×20 ×10 mm^3 (1.5 CFM)

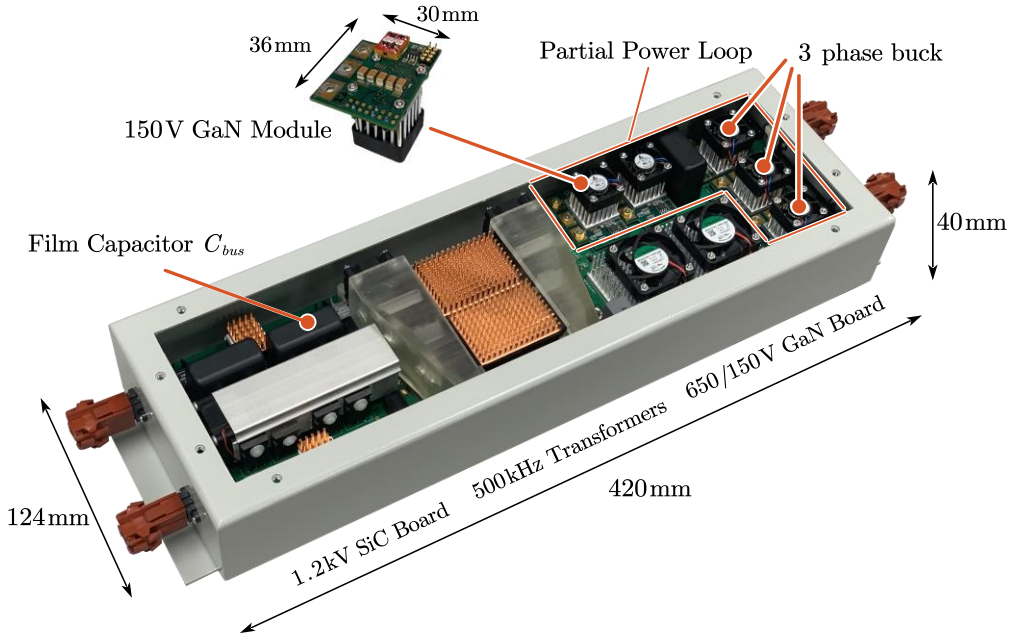


Fig. 4-21. 18 kW PP converter prototype operated in 500 kHz. The circuit parameters are listed in Table 4-6.

2) Experimental Results for MP DCX

With the proposed layout method and winding structure, the performance of MP DCX was estimated first when the duty cycle *d* for the post-regulator is 0. In this case, the PP converter operates like a pure DCX. The current sharing results between S_1 and S_2 at 18 kW are shown in **Fig. 4-22**. Without the proposed "intra-leaving" structure, the peak values of $i_{MP,S1}$ and $i_{MP,S2}$ are 56 A and 24 A, as shown in **Fig. 4-22(a)**. However, after utilizing the proposed structure, the current sharing performance became much better, as shown in **Fig. 4-22(b)**. At this time, $i_{MP,S1}$, and $i_{MP,S2}$ are much closer; one is 42 A, and the other is 38 A. Thus, the effectiveness of the "intra-leaving" structure can be verified.

Fig. 4-23 shows the steady state waveform for MP DCX at 18 kW. Before gate signal $v_{gs,Q2}$ is turned on, the drain to source voltages $v_{dc,bus}$ and $v_{ds,MP}$ on both sides have been reduced to zero, which means the ZVS has been achieved on both sides. Furthermore, during ZVS transitions, the current ringing on i_{bus} and i_{MP} are both very small, which can indicate the AC loop inductance optimization is effective. Thus, the proposed layout method and winding structure could reduce the stary and leakage inductance, respectively.

Because the secondary side of MP DCX has the largest heat dissipation (transferring majority power), the full load thermal result for the 650 V GaN board is shown in **Fig. 4-24**. With good thermal design, the switch's surface temperature and the heatsink temperature are only 42 ^{o}C and 40 ^{o}C. In addition, since the whole board temperature is very low with the proposed layout method, the effectiveness of AC resistance reduction could be verified.

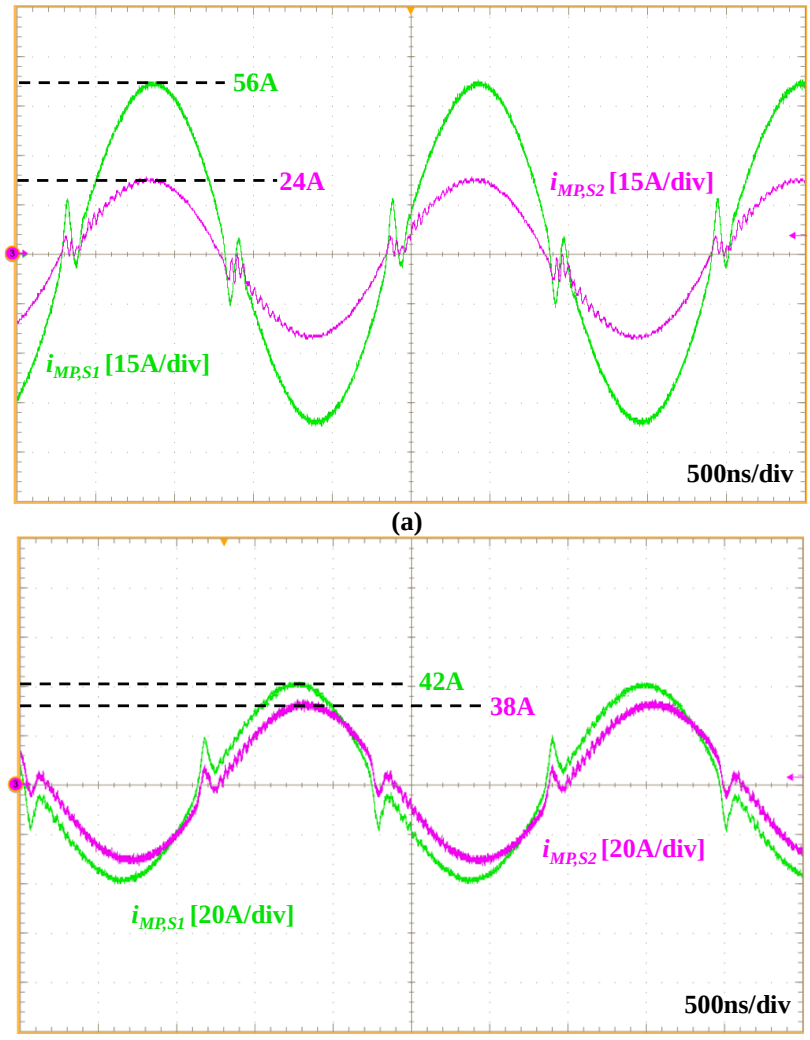


Fig. 4-22. Current sharing results between S_1 and S_2 windings at 18 kW: (a) without Intra-leaving and (b) with intra-leaving. The circuit parameters are listed in Table 4-6.

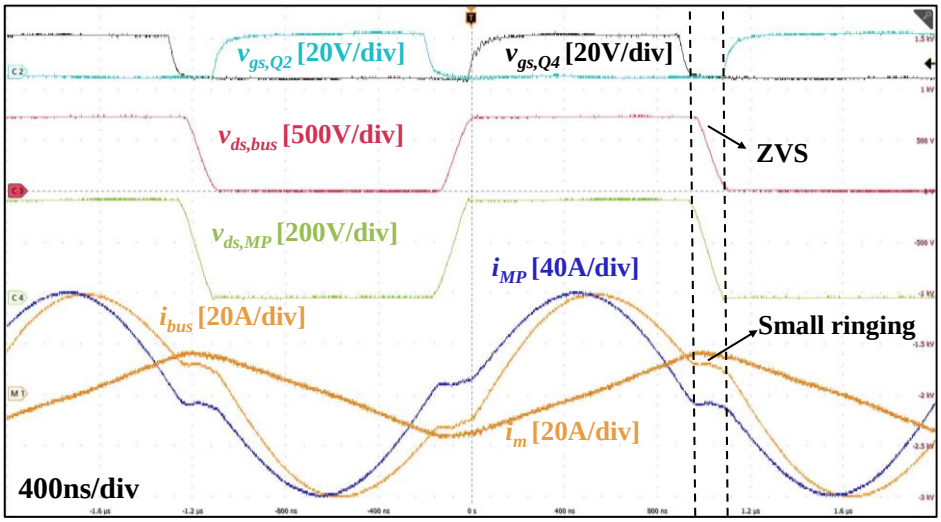


Fig. 4-23. Steady-state waveforms of the PP converter at 18 kW when d = 0.

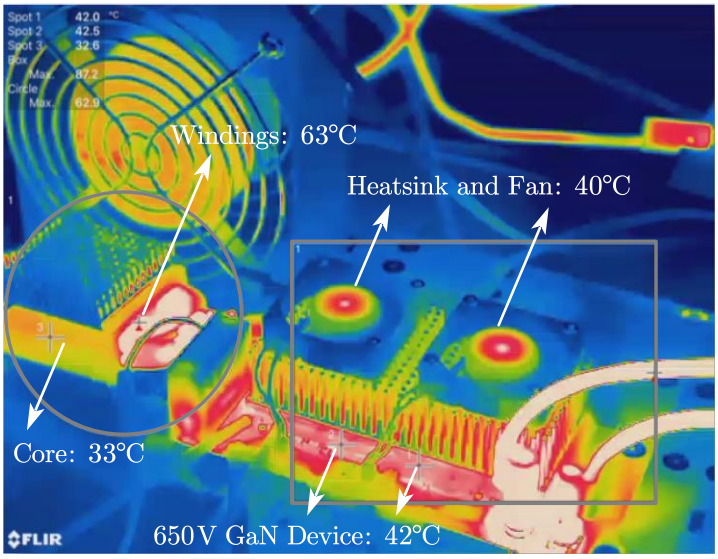
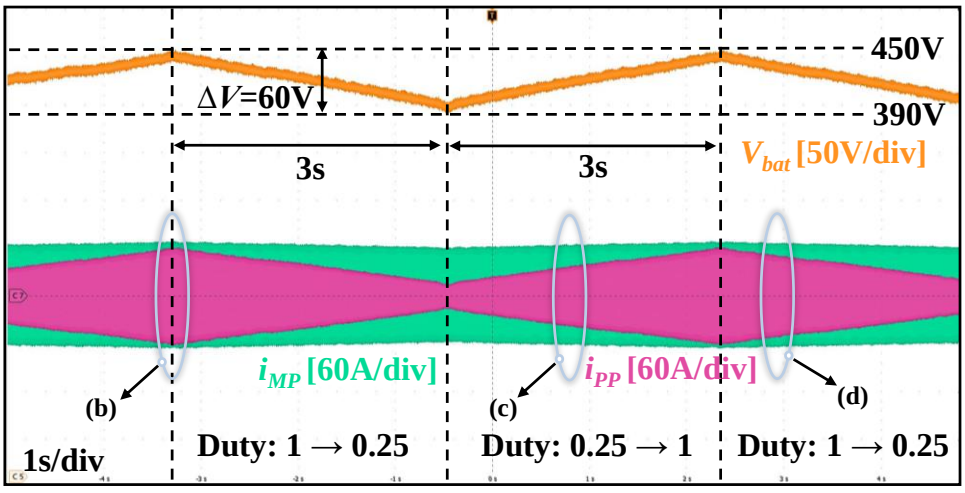
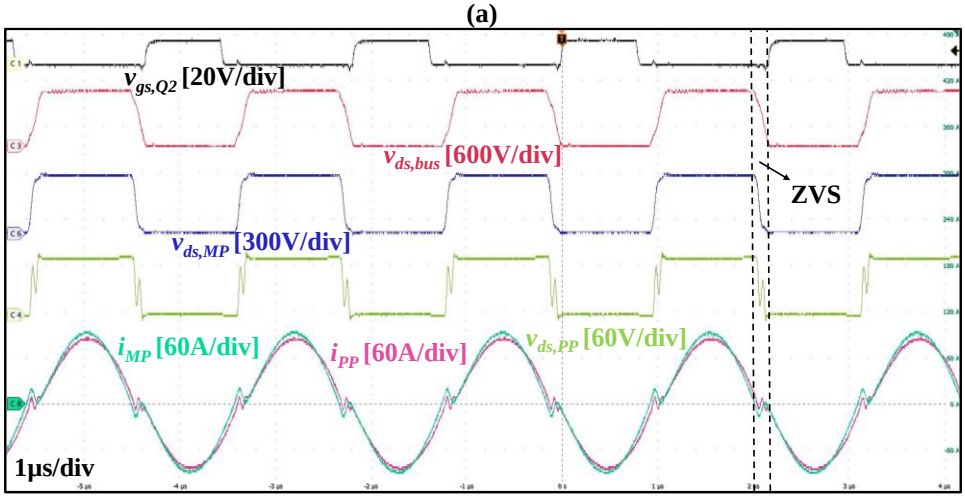


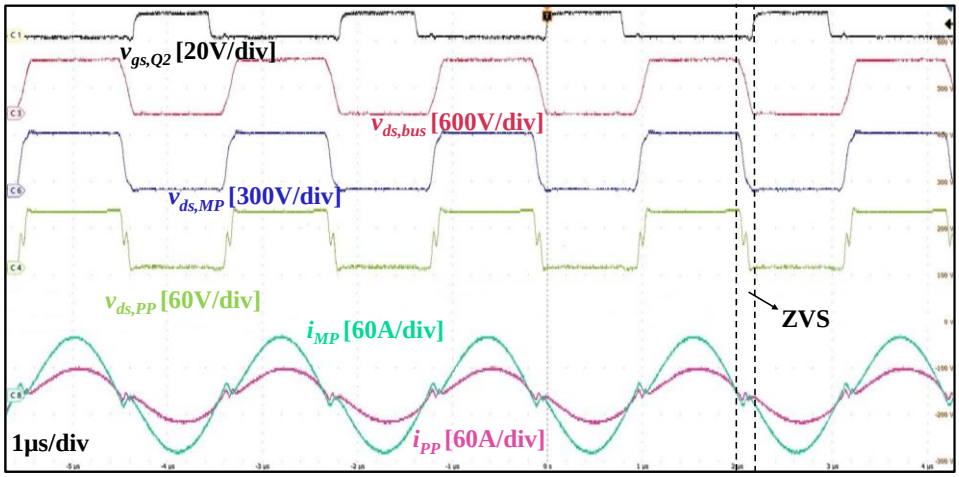
Fig. 4-24. Thermal results for MP DCX secondary side at 18kW.



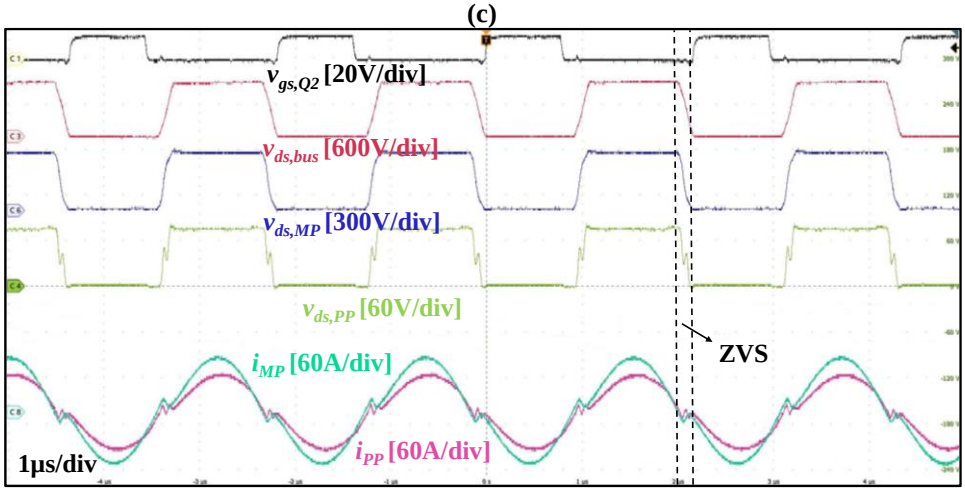
(a)



(b)



(c)



(d)

Fig. 4-25. Forward operation from V_{bus} to V_{bat}: (a) dynamic voltage regulation (b) output 450 V at 25 kW when d = 1 (c) output 413 V at 21 kW when d = 0.5 (d) output 431 V at 23 kW when d = 0.75. The circuit parameters are listed in Table 4-6.

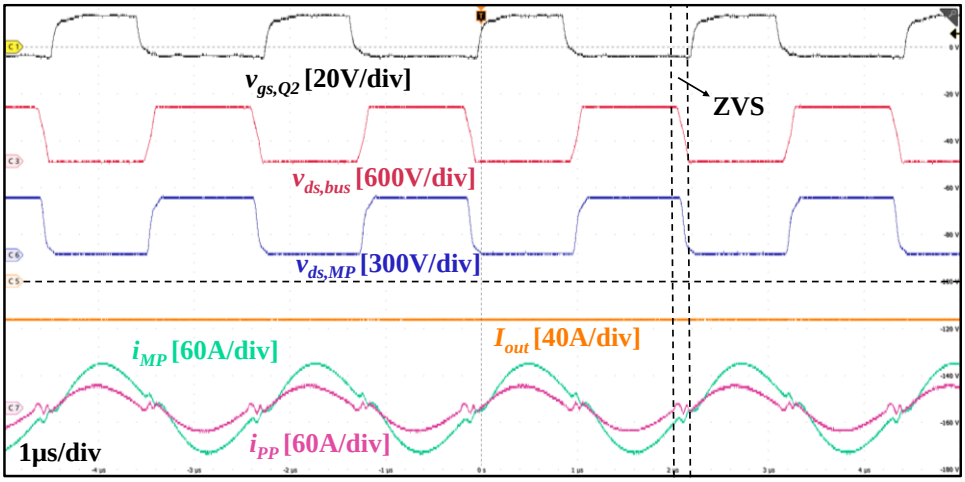


Fig. 4-26. Reverse operation from V_{bat} to V_{bus} when d = 0.5 at 16 kW.

3) Experimental Results for PP Converter

When the post-regulator begins to process power, the PP converter can regulate the output voltage. As the duty cycle d changes back and forth between 0.25 and 1, the result of dynamic voltage regulation with forward operation at full power is shown in **Fig. 4-25(a)**. When d changes from 1 to 0.25, the output battery voltage V_{bat} changes from 450 V to 390 V, which is consistent with Eq. (4.1).

Thus, the functionality of the PP converter can be verified. On the other hand, when V_{bat} decreases, i_{PP} through T_{PP} also decreases, and i_{MP} through T_{MP} remains nearly constant. It means that the partial power P_{PP} processed by PP DCX and post-regulator is reduced, and the majority power P_{MP} transferred by MP DCX is almost constant. Furthermore, three cases with different d in **Fig. 4-25(a)** are zoomed in, as shown in **Fig. 4-25(b)-(d)**. In these cases, d is equal to 1, 0.5, and 0.75, respectively. As can be seen, during the ZVS transition, before gate signal $v_{gs,Q2}$ are turned on, the drain to source voltages $v_{dc,bus}$, $v_{ds,MP}$ and $v_{ds,PP}$ on all three sides have been reduced to zero, which means the ZVS has been achieved on all three sides. Thus, the proposed decoupling method for MP and PP DCXs, which can simplify the design of the PP converter, was verified.

As shown in **Fig. 4-26**, the reverse operation from V_{bat} to V_{bus} has been verified when d=0.5 at 16 kW. It should be noted that the reverse operation power is smaller than the forward operation because the current limit of the power supply is 40 A. To highlight the reverse operation, the negative output current I_{out} was measured. Compared with forward operation, the phases of currents i_{MP} and i_{PP} are reversed in reverse operation, which means the power flow direction has been changed.

4) Efficiency and Loss Breakdown

The conversion efficiency of the PP converter was determined with the Keysight PA 2203A power analyzer, as shown in **Fig. 4-27**. It should be noted that, to achieve 18 kW output power with 375 V output, a 7.8 Ω resistance bank is used as the battery load in this paper. Therefore, the higher output voltage case has the larger output power. For example, when the PP converter outputs 450 V with a 7.8 Ω resistance load, the maximum power is close to 25 kW. With 375 V output at 18 kW, the PP converter has the best efficiency at 98.8%. In this case, *d* is 0, and all power is transferred by MP DCX. When the output voltage increases from 375 V, the efficiency of the PP converter will get worse because more power is processed by the PP DCX and post-regulator. Finally, the loss breakdown of the PP converter with different battery voltage at 18 kW is plotted in **Fig. 4-28**. The total converter loss is composed of three parts: the major power loss PMP,loss from Eq. (4.15), the partial power loss PPP,loss from Eq. (4.7), and the transformer loss Ptran from FEA simulation results (winding loss) and IGSE calculation (core loss).

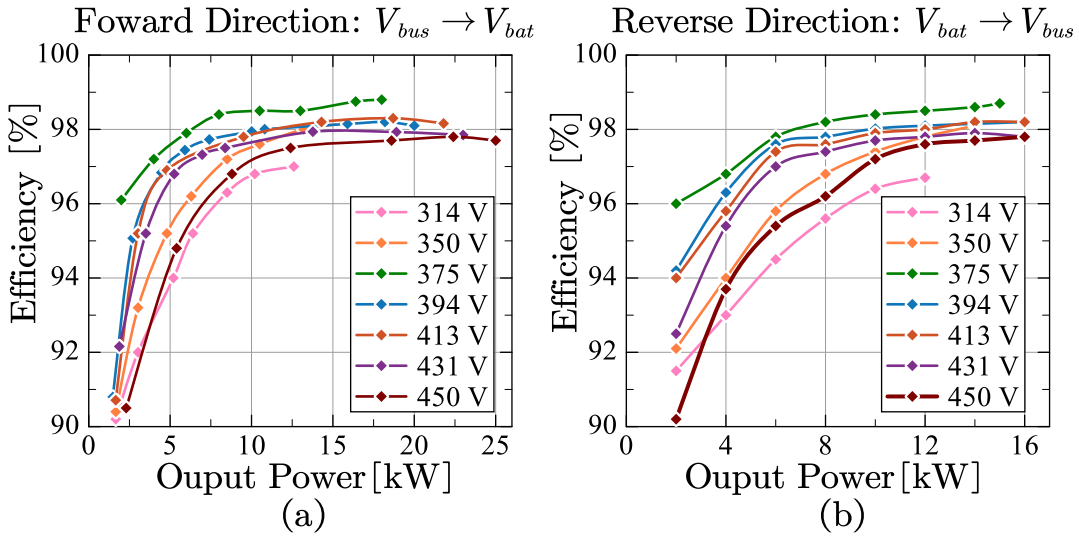


Fig. 4-27. Efficiency of the PP converter with respect to output power determined with Keysight PA 2203A power analyzer.

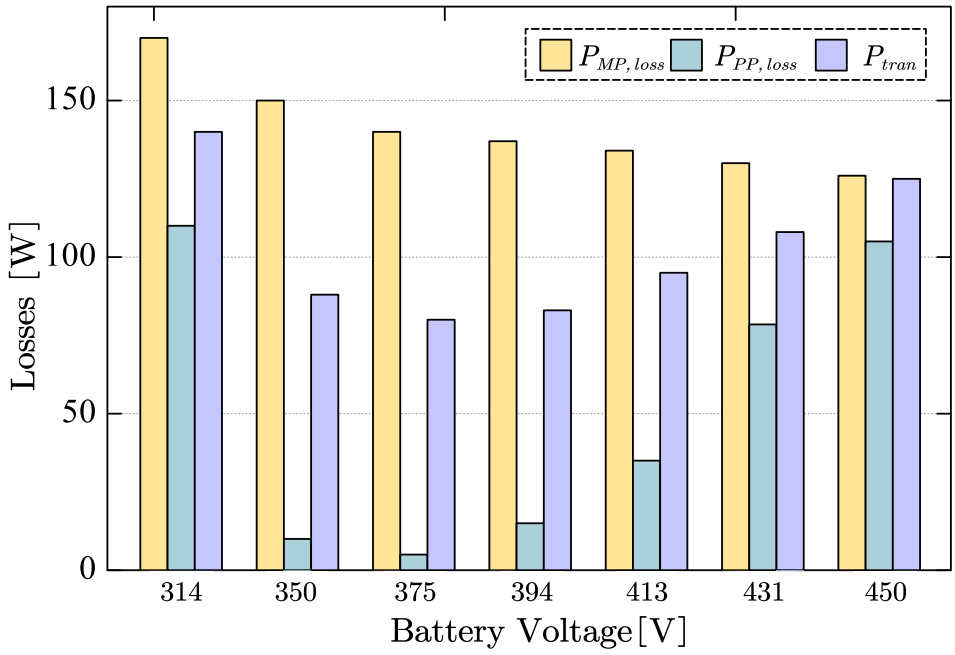


Fig. 4-28. Loss breakdown with different battery voltage at 18 kW. The calculation is based on the circuit parameters listed in Table 4-6.

4.3 Three-level Buck-boost Converter with Common-Mode Noise Suppression

The demand for a bi-directional DC-DC converter with a flexible output is driven by the fast development of renewable energy systems, transportation electrification, and microgrids. In order to accommodate different DC buses, two-stage AC-DC-DC architecture has been widely used, and the DC output regulation was handled by a rear-end DC-DC converter. If galvanic isolation is not required, the four-switch buck-boost (FSBB) converter with quadrangle control is a good candidate because of the bidirectional non-inverting output, step-up/down capability, and zero voltage switching (ZVS). However, to achieve the minimum rms current and soft switching, the calculation of quadrangle control is complicated and often requires resource-consuming loop-up tables or additional high-frequency current detection circuits. Moreover, due to the unbalanced circuit topology, the common-mode (CM) noise is another concern. In this chapter, a symmetric three-level (3-L) buck-boost converter was first proposed to suppress the CM noise. To increase the power density and efficiency, planar coupled inductors were designed for this 3-L buck-boost converter with a 30% winding loss reduction. To realize a simple close-loop output control, a real-time simplified minimum rms current calculation for quadrangle modulation was found without look-up tables or ZCD circuits. Based on this simplified output control, a decoupled mid-point balance control for both input and output sides was also proposed. Finally, the simplified close-loop control, the decoupled active balance control, and the CM mode noise reduction were all verified by a 30 kHz 50 kW 3-L buck-boost converter. Compared with the typical FSBB converter, the proposed 3-L buck-boost converter has up to 25 dB CM noise reduction from 150 kHz to 30 MHz. This article is accompanied by two videos demonstrating the effect of decoupled active balance control.

4.3.1 Proposed 3-L Buck-Boost Converter

1) Quadrangle Modulation for Four-switch Buck-Boost (FSBB) Converter

The circuit diagram of traditional FSBB is depicted in **Fig. 4-29(a)**. V_{in} and V_{out} are the input and output voltages, respectively. The gating signals and corresponding inductor current i_L are shown in **Fig. 4-29(b)**. D_1 and D_2 are the duty cycle for half bridge $S_{1,2}$ and $S_{3,4}$, and the phase shift between D_1 and D_2 is φ. D_1, D_2, and φ are three basic control variables for the FSBB converter, and they can control the shape of i_L. Due to the soft-switching and minimum rms current, quadrangle modulation has been widely used in FSBB converters [6], [7], [63]. I_1 and I_2 in **Fig. 4-29(b)** are two peak currents of i_L. This modulation has a total of three merits, as explained below:

Merit 1 is the simple output regulation: due to the volt-second balance, the voltage gain of a typical FSBB converter can be easily controlled by D_1 and D_2.

$$\frac{V_{out}}{V_{in}} = \frac{D_1}{D_2} \tag{4.17}$$

Merit 2 is the soft switching with minimum negative current. To realize the ZVS during the deadtime t_d, a small negative current I_{ZVS} is required to charge and discharge the parasitic output capacitance C_{oss}, as shown in **Fig. 4-29(a)**. The amplitude of this negative current can be given as

$$|I_{ZVS}| \geqslant \frac{2C_{oss}V_{out,\max}}{t_d} \tag{4.18}$$

Merit 3 is the minimum rms value of the inductor current i_L. To obtain this, the inductor current i_L is controlled as a quadrangular waveform, as shown in **Fig. 4-29(b)**; the inductance L in **Fig. 4-29(a)** should meet the requirement below.

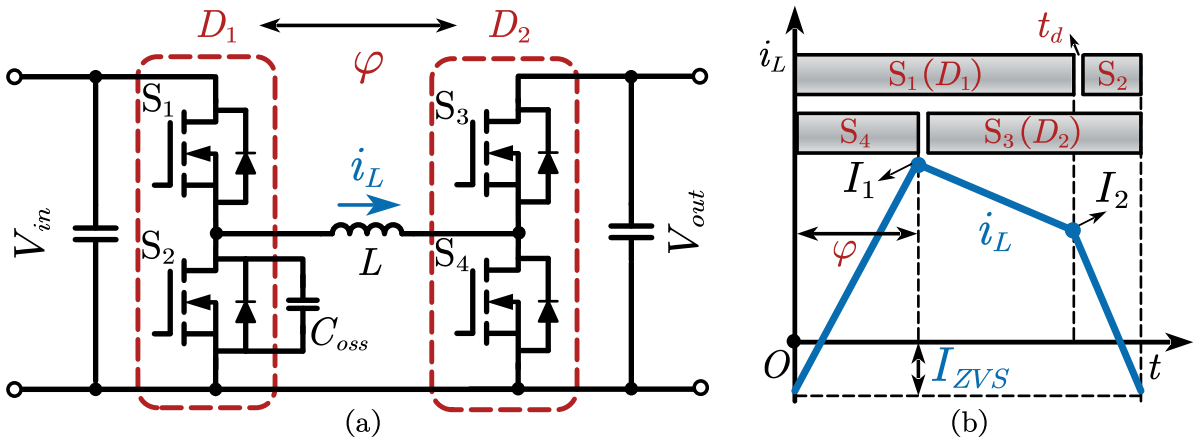


Fig. 4-29. (a) The circuit diagram of a typical four-switch buck-boost (FSBB) converter, (b) the corresponding inductor current i_L with a quadrangle control.

$$L = \frac{{V_{in}}^2 {V_{out}}^2}{2P_{max,ZVS} f_s ({V_{in}}^2 + V_{in} V_{out} + {V_{out}}^2)} \tag{4.19}$$

Where $P_{max,ZVS}$ is the maximum power that the FSBB converter could achieve ZVS with minimum rms current.

2) Proposed 3-L Buck-Boost Converter with Coupled Inductors

Based on the typical FSBB converter with a quadrangle modulation, a 3-L buck-boost converter was proposed in **Fig. 4-30(a)** to reduce the CM noise. S_{14}, S_{23}, S_{58}, and S_{67} are four switch pairs, and each pair has identical gate signals. For example, switches S_1 and S_4 have the same driving signal. N_1 and N_2 are two midpoints on the input and output sides, respectively.

Moreover, to increase the power density and decrease the winding loss, two separate inductors, L_T in **Fig. 4-30(a)**, can be integrated as 1:1 coupled inductors, as shown in **Fig. 4-30(b)**. The L_s and M are the self-inductance and mutual inductance. **Fig. 4-30(c)** depicts the simplified equivalent circuit with coupled inductors. v_{AN1}, v_{BN1}, v_{CN2}, and v_{DN2} are four voltage sources which are used to replace four half bridges. Due to the symmetrical modulation, without the consideration of circuit tolerance, the amplitude of v_{AN1} and v_{CN2} are exactly equal to v_{BN1}, v_{DN2}, respectively.

$$\begin{cases} v_{AN_1} = -v_{BN_1} \\ v_{CN_2} = -v_{DN_2} \end{cases} \tag{4.20}$$

The influence of circuit tolerance will be discussed in *Section IV*. L_{DM} and L_{CM} are DM and CM inductance and can be given as

$$\begin{cases} L_{DM} = 2L_s + 2M \\ L_{CM} = (L_s{}^2 - M^2)/(2L_s + 2M) \end{cases} \quad M \approx L_s \longrightarrow \begin{cases} L_{DM} \approx 4L_s \\ L_{CM} \approx 0 \end{cases} \tag{4.21}$$

When the coupling coefficient is close to 1, L_{DM} and L_{CM} can be approximated as $4L_s$ and 0. Compared with the two separate inductor designs shown in **Fig. 4-30(a)**, the coupled inductors design can decrease the turns number from N to $\sqrt{2}/2N$ with the same value L_{DM}. Therefore, the winding loss can be reduced by 30% with a sacrifice of CM inductance.

This cost is acceptable because this proposed symmetric 3-L buck-boost converter can reduce the CM voltage emission as explained below:

The equivalent circuit in **Fig. 4-30(c)** can be decomposed into two DM and CM equivalent circuits, as shown in **Fig. 4-30(d)**. From Eq. (4.20), two CM voltage sources, $v_{N1(2),CM}$, and the total CM voltage v_{CM} can be derived as

$$\begin{cases} v_{N_1,CM} = 0.5\,(v_{AN_1} + v_{BN_1}) = 0 \\ v_{N_2,CM} = 0.5\,(v_{CN_2} + v_{DN_2}) = 0 \end{cases} \tag{4.22}$$

$$v_{CM} = v_{N_1,CM} - v_{N_2,CM} = 0 \tag{4.23}$$

From Eq. (4.23), this proposed topology has zero CM voltage emission theoretically, which means the coupled inductors are suitable in this case. As for the DM equivalent circuit depicted in **Fig. 4-30(d)**, four DM voltages $v_{A(BCD),DM}$, and the total DM voltage v_{DM} can be given as

$$\begin{cases} v_{A(B),DM} = v_{A(B)N_1} - v_{N_1,CM} \\ v_{C(D),DM} = v_{C(D)N_2} - v_{N_2,CM} \end{cases} \tag{4.24}$$

$$v_{DM} = (v_{A,DM} - v_{B,DM}) - (v_{C,DM} - v_{D,DM}) \tag{4.25}$$

From Eq. (4.23), the CM current i_{CM} is theoretically equal to 0, and the inductor should be equal to the DM current.

$$\begin{cases} i_{CM} = 0 \\ i_{DM} = i_L \end{cases} \tag{4.26}$$

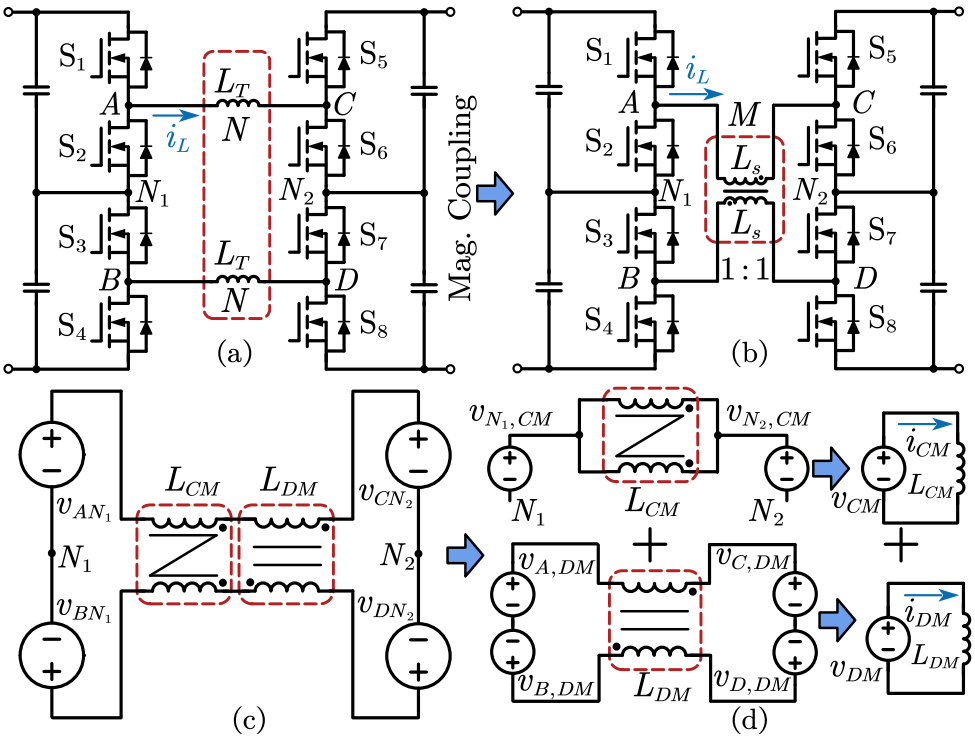


Fig. 4-30. Proposed 3-L buck-boost converter: (a) with separate inductor, (b) with coupled inductors, (c) simplified equivalent circuit, (d) DM and CM equivalent circuits. The proposed 3-L circuit diagram can be derived from the original FSBB shown in Fig. 4-29.

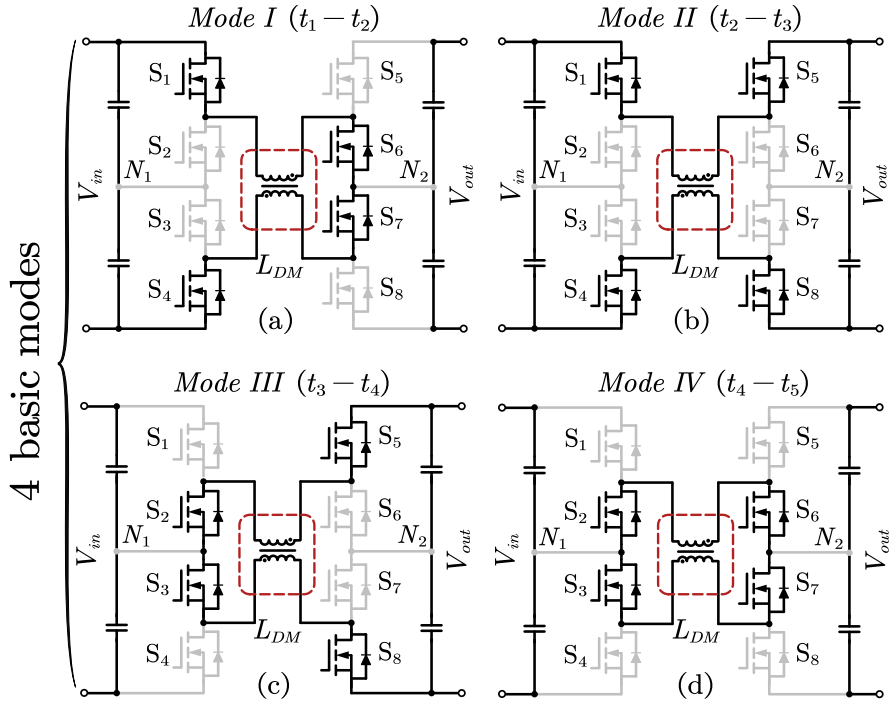


Fig. 4-31. The equivalent circuit diagrams of four basic modes: (a) *Mode I* (t_1-t_2), (b) *Mode II* (t_2-t_3), (c) *Mode III* (t_3-t_4), (d) *Mode IV* (t_4-t_5). The original circuit diagram is shown in Fig. 4-30.

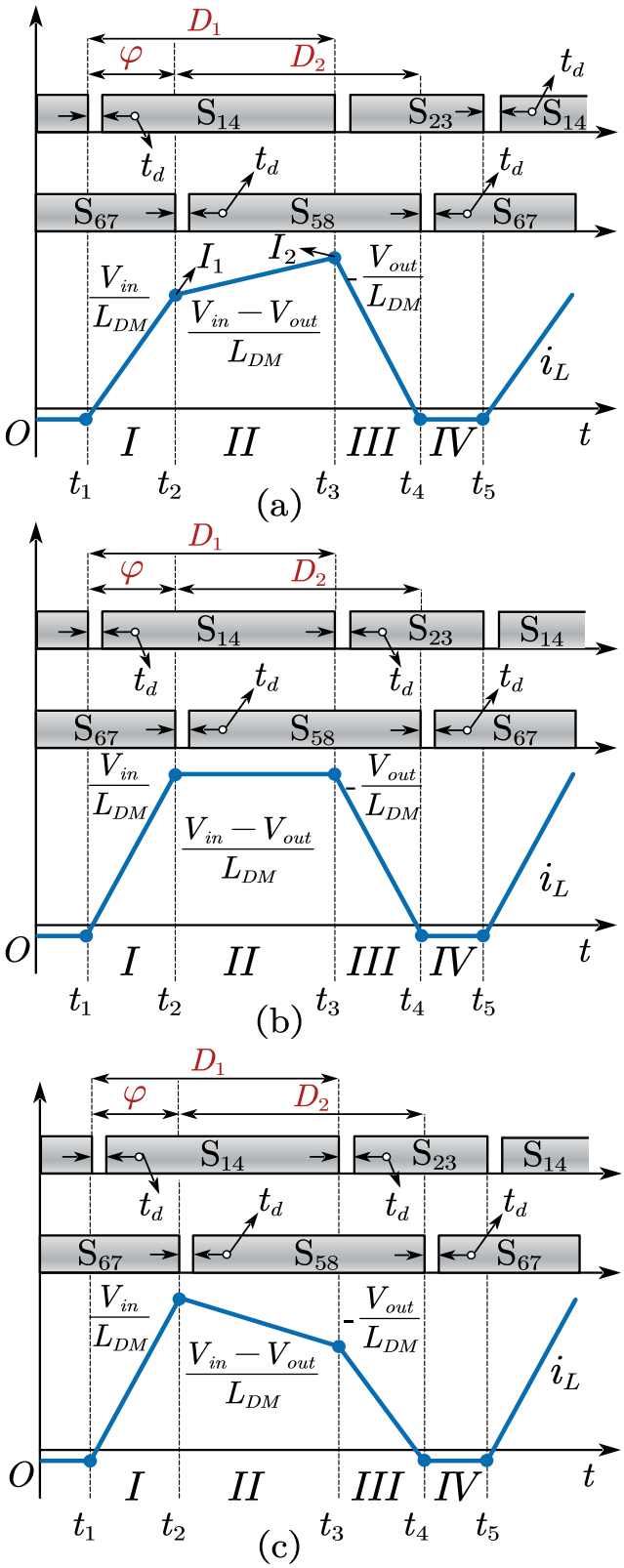


Fig. 4-32. The corresponding waveforms of the 3-L buck-boost converter: (a) step-down case when $V_{in}>V_{out}$, (b) unit-gain case when $V_{in}=V_{out}$, (c) step-up case when $V_{in}<V_{out}$. The circuit diagram is shown in Fig. 4-30.

3) Operation Principle

With the symmetrical modulation, the operation principle of the 3-L buck-boost converter is very similar to the typical FSBB. For example, the voltage gain, the negative ZVS current I_{ZVS}, and the inductance requirement can follow Eq. (4.17) -(4.19).

Fig. 4-31 shows the equivalent circuit diagrams of four basic operation modes of a 3-L buck-boost converter. The corresponding current waveforms and driving signals are depicted in **Fig. 4-32** with three different cases. In order to realize ZVS at all switches, deadtime t_d is adopted. Each operation mode is illustrated as follows.

Mode I — As depicted in **Fig. 4-31(a)**, four switches, S_1, S_4, S_6, and S7, are turned on from t_1 to t_2. Since only the input voltage V_{in} is applied on the coupled inductor L_{DM}, the inductor current i_L will increase linearly with the slope m_I, as shown in **Fig. 4-31**.

$$m_I = V_{in}/L_{DM} \tag{4.27}$$

Mode II — In **Fig. 4-31(b)** and **Fig. 4-32**, switches S_1, S_4, S_5 and S_8 are in the ON state from t_2 to t_3. The difference voltage between V_{in} and V_{out} is applied on the coupled inductors L_{DM}, and the current slop m_{II} can be given as

$$m_{II} = (V_{in} - V_{out})/L_{DM} \tag{4.28}$$

Mode III — In the **Fig. 4-31(c)** and **Fig. 4-32**, S_2, S_3, S_5 and S_8 are conducting during t_3 to t_4. Since only the output voltage V_{out} is applied to L_{DM}, the current slope m_{III} can be derived as

$$m_{III} = -V_{out}/L_{DM} \tag{4.29}$$

Mode IV — In **Fig. 4-31(d)** and **Fig. 4-32**, four switches S_2, S_3, S_6 and S_7 are turned on during t_4 to t_5. The voltage across Since this free-wheeling mode will increase the rms value of i_L, *Mode IV* is not expected and should be avoided at heavy load. With the combinations of these four operation modes, the inductor current shape can be controlled as a quadrangle. Three difference cases, step-down, unit-gain, and step-up cases, are depicted in **Fig. 4-32(a)-(c)**, respectively. The definition of D_1, D_2, and φ in **Fig. 4-32** is the same as traditional FSBB in **Fig. 4-29**. The inductor current slope m_{IV} can be given as

$$m_{IV} = 0 \tag{4.30}$$

Since this free-wheeling mode will increase the rms value of i_L, *Mode IV* is not expected and should be avoided under heavy loads. With the combinations of these four operation modes, the inductor current shape can be controlled as a quadrangle. Three different cases, step-down, unit-gain, and step-up cases, are depicted in **Fig. 4-32(a)-(c)**, respectively. The definition of D_1, D_2, and φ in **Fig. 4-32** is the same as traditional FSBB in **Fig. 4-29**.

4) DM Inductor Design and Marginal Power

The specifications of the proposed 3-L buck-boost converter are listed in **Table 4-7**. The input voltage V_{in} is constant at 900 V, and the output voltage V_{out} is from 500 V to 1 kV. The rating power P is 50 kW, and the switching frequency f_s is 30 kHz.

Due to the similar operation principle as the FSBB converter explained in *Part A*, the DM inductance L_{DM} in **Fig. 4-30(b)** should be determined by requirement Eq. (4.19). With a fixed V_{in}=900 V, **Fig. 4-33(a)** depicts the maximum ZVS power $P_{max,ZVS}$ with L_{DM} and V_{out}. To achieve the ZVS, $P_{max,\ and\ ZVS}$ should be larger than the rated power P, which means the required operating region should be lower than 50 kW. To simplify the explanation, **Fig. 4-33(b)** projects $P_{max,ZVS}$ in **Fig. 4-33(a)** to a two-dimensional (2-D) plane with different V_{out}. Only when L_{DM} is smaller than 50 μH, $P_{max,ZVS}$ with the full V_{out} range exceed the rating power of 50 kW. If L_{DM} is larger than 50 μH, $P_{max,ZVS}$ at V_{out}=500 V will be smaller than 50 kW, which means the full load range ZVS will lose. On the other hand, a smaller L_{DM} will cause a larger current ripple from Eq. (4.27)-(4.29), which means the rms current on the inductor will also increase. **Fig. 4-33(c)** projects $P_{max,ZVS}$ to another 2-D plane with different L_{DM}. With a similar analysis, in order to achieve whole range ZVS and minimum rms current, the optimized value of L_{DM} can be re-confirmed as 50 μH.

Table 4-7 SPECIFICATIONS OF THE PROPOSED 3-L BUCK-BOOST CONVERTER

Variable	Value	Variable	Value
Input voltage V_{in}	900 V	Rating Power P	50 kW
Output voltage V_{out}	500 V to 1 kV	Switching frequency f_s	30 kHz

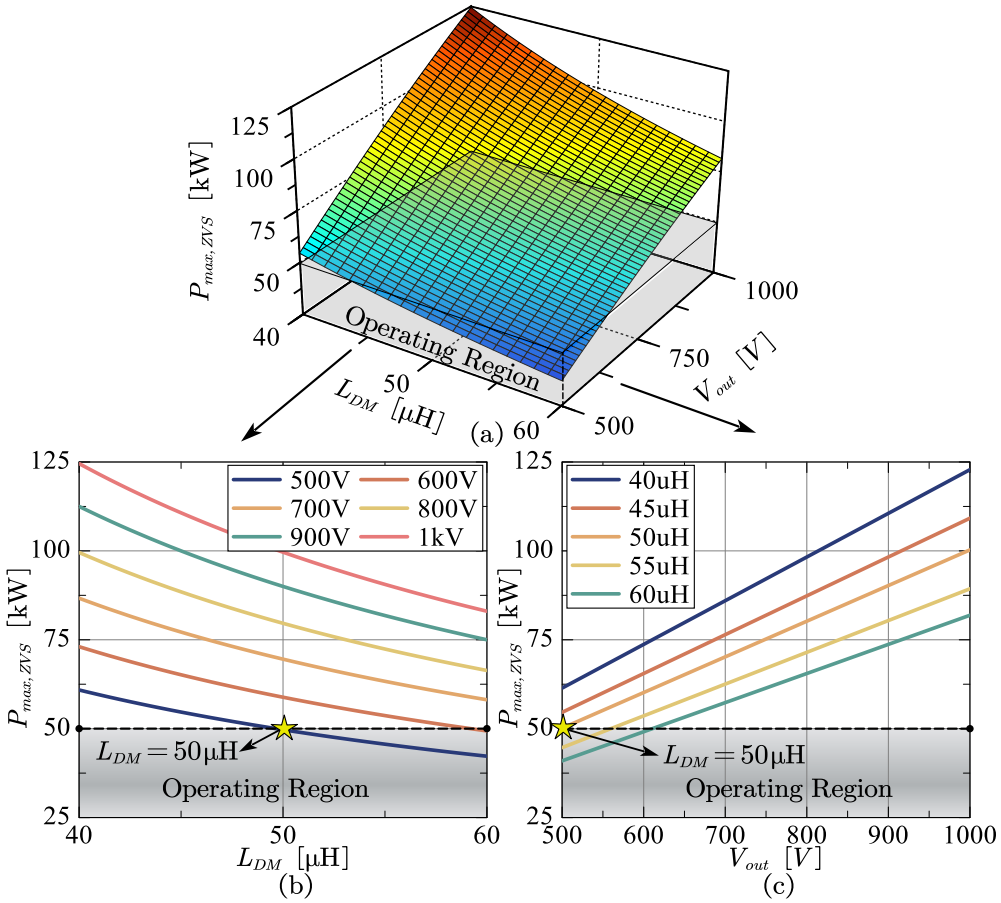


Fig. 4-33. The relationship between (a) $P_{max,ZVS}$ with different L_{DM} and V_{out}, (b) $P_{max,ZVS}$ and L_{DM}, and (c) $P_{max,ZVS}$ and V_{out}.

With a determined L_{DM}, **Fig. 4-34** shows the inductance current i_L waveforms with different load conditions. Under a heavy load, to obtain a minimum rms current, i_L can be controlled as a quadrangle without *Mode IV*. However, if the load becomes lighter, the current shape will change to a triangle because of the smaller output current. Marginal power is defined as the power boundary when i_L transforms into a triangle without *Mode IV*. As for the step-down operation, as shown in **Fig. 4-34(a)**, the marginal power case only consists of *Mode II* and *III*. As for the unit gain case, marginal power is equal to zero because i_L always remains an isosceles trapezoid, as shown in **Fig. 4-34(b)**. As for the step-up operation, the marginal power case is composed of only *Mode I* and *II*, as shown in **Fig. 4-34(c)**.

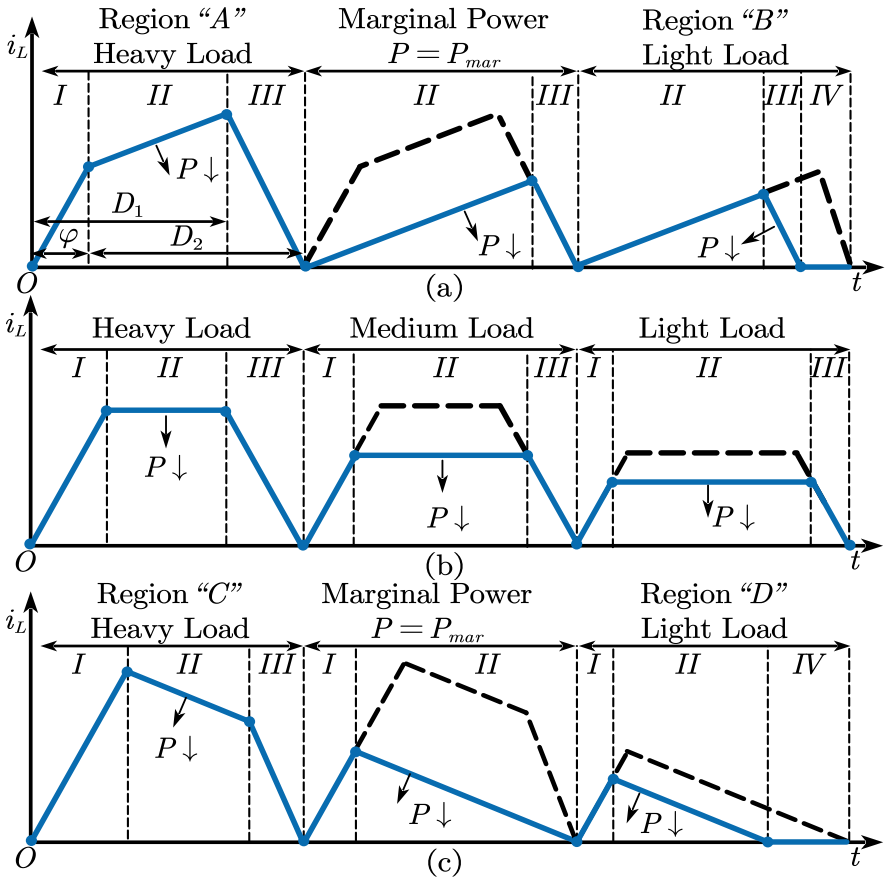


Fig. 4-34. Inductance current waveforms with different load conditions: (a) step-down, (b) unit-gain, (c) step-up.

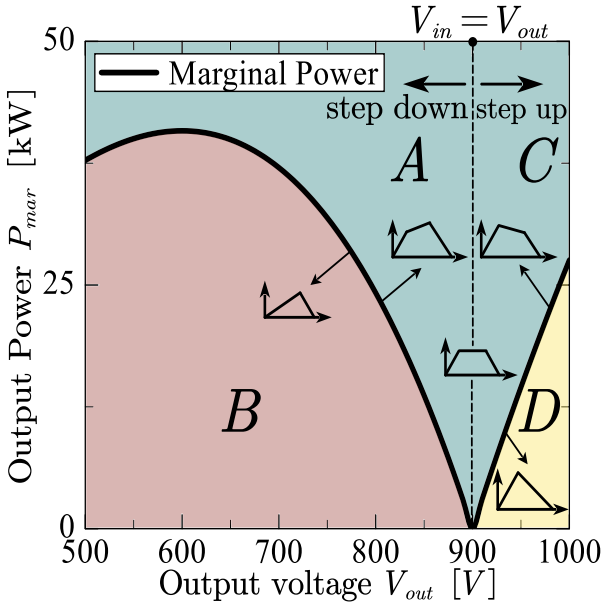


Fig. 4-35. The relationship between marginal power P_{mar} and output voltage V_{out}. The corresponding current waveforms, including marginal power case, can be found in Fig. 4-34.

When the operation power is smaller than P_{mar}, to obtain a smaller output current, *Mode IV* will occur to fill up the blank time. With a determined V_{out}, V_{in}, f_s, and L_{DM}, the marginal power P_{mar} can be given as

$$P_{mar} = \begin{cases} {V_{out}}^2 (V_{in} - V_{out}) / (2 f_s L_{DM} V_{in}) & V_{in} > V_{out} \\ {V_{in}}^2 (V_{out} - V_{in}) / (2 f_s L_{DM} V_{out}) & V_{in} \leq V_{out} \end{cases} \tag{4.31}$$

According to the specifications listed in **Table 4-7**, **Fig. 4-35** depicts the relationship between the marginal power P_{mar} and the output voltage V_{out}. *Region* "*A*" and "*B*" show the step-up case with heavy load and light load, respectively. Regions "C" and "D" depict the step-down case with heavy and light loads. As shown in **Fig. 4-35**, the unit gain case is presented by a dashed line (V_{in}=V_{out}) and its marginal power is equal to zero, which means the shape of i_L keeps as an isosceles trapezoid at the full load range.

4.3.2 Simplified Close-loop Control

1) Simplified Minimum RMS Current Calculation

As shown in **Fig. 4-29**, three basic control variables, D_1, D_2, and φ, can be used to control the current shape and achieve the three merits: output regulation, soft-switching, and minimum rms current. **Fig. 4-36(a)** shows a typical minimum rms current calculation block, which has been widely used to determine D_1, D_2, and φ with four input variables: input and output voltage reference $V_{in,ref}$, $V_{out,ref}$, output dc current I_{out}, and negative current I_{ZVS}. In order to avoid the complex real-time calculation, a look-up table and extra I_{ZVS} current detection methods have been adopted. However, an external flash is required to store huge look-up table data. An extra high-frequency current detection circuit is costly and difficult to implement in high-power applications.

In order to achieve a real-time calculation without an extra current detection circuit, a simplified minimum rms current calculation block was proposed, as depicted in **Fig. 4-36(b)**. The input variable I_{ZVS} has been replaced by a ZVS factor "*k*". This new variable was adopted to simplify the calculation and describe the amplitude of I_{ZVS}. **Fig. 4-37** shows the inductance current i_L with different ZVS factors "*k*." For example, when the factor *k* is equal to 0, as shown in **Fig. 4-37(a)**, the ZVS current I_{ZVS} is also equal to 0. When *k* is not equal to 0, the negative ZVS current I_{ZVS} will occur, as shown in **Fig. 4-37(b)**; the relationship between I_{ZVS} and *k* will be explained in *Part B* in this section. **Fig. 4-38** shows the flowchart of the simplified minimum rms current calculation. The first step is to determine the load condition. If the output power is larger than the marginal power P_{mar} from Eq. (4.31), the current can be controlled as a quadrangle without *Mode IV*, and three basic control variables D_1, D_2, and φ can be derived as

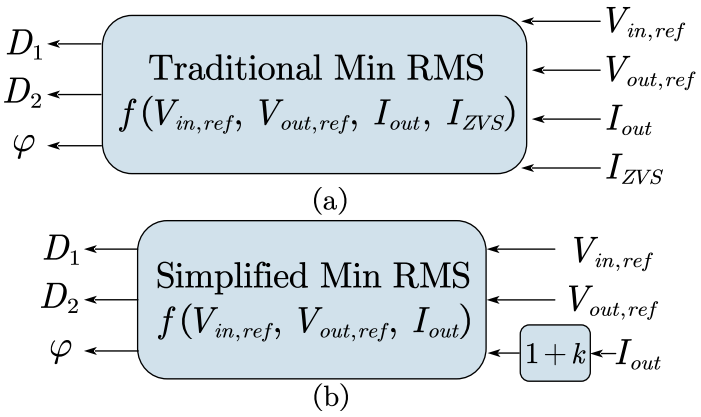


Fig. 4-36. The minimum rms current calculation blocks for quadrangle control FSBB converter: (a) the traditional calculation, (b)the simplified calculation.

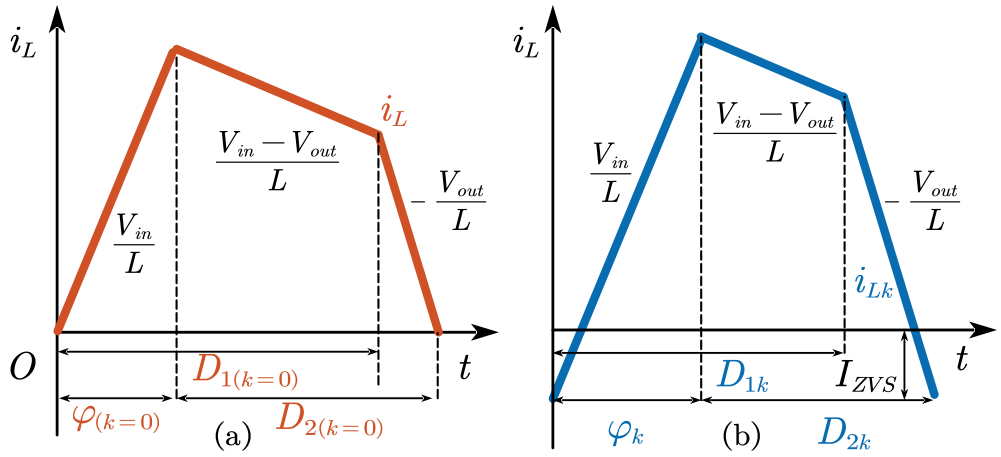


Fig. 4-37. The relationship between marginal power P_{mar} and output voltage V_{out}. The original current waveforms can be found in Fig. 4-29(b) with k=0.

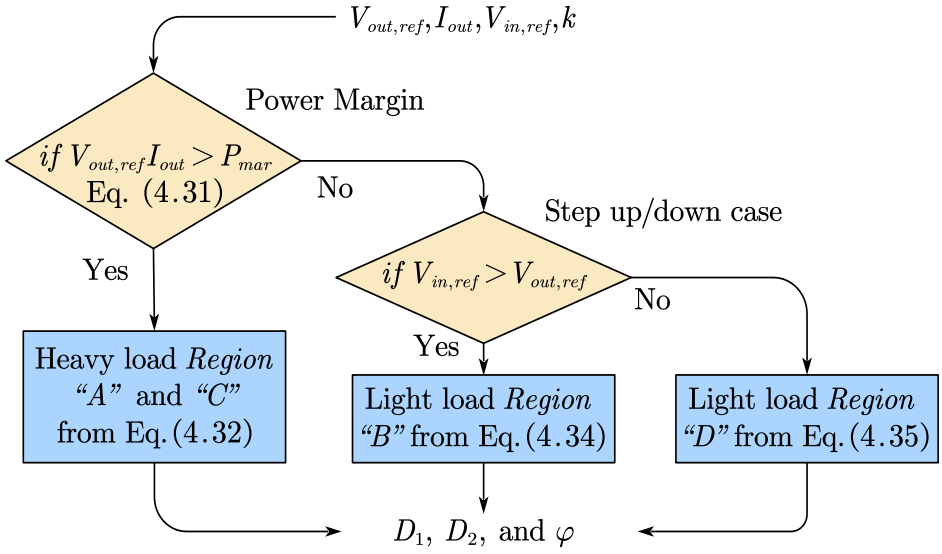


Fig. 4-38. The flowchart of the simplified minimum rms current calculation.

$$
\begin{aligned}
&D_1 = V_{out}/V_{in}\,D_2 \\
&D_2 = 1-\varphi \\
&\varphi = \frac{1-\sqrt{{V_{in}}^3 {V_{out}}^{-3} - 2(1+k)\,I_{out} L_{DM} f_s \cdot X}}{Y}
\end{aligned}
\tag{4.32}
$$

Where terms "X" and "Y" can be given as

$$
\begin{aligned}
&X = V_{in}{V_{out}}^{-2} + {V_{in}}^2 {V_{out}}^{-3} + {V_{in}}^3 {V_{out}}^{-4} \\
&Y = {V_{in}}^2 {V_{out}}^{-2} + V_{in}{V_{out}}^{-1} + 1
\end{aligned}
\tag{4.33}
$$

Therefore, under the heavy load, *Region* "*A*" and "*C*" in **Fig. 4-35** share a unified Eq. (3.32). When output power is smaller than marginal power P_{mar}, the second step is to determine the step-up or step-down case. If V_{in} is larger than V_{out}, the derivation for D_1, D_2, and φ under *Region* "*B*" can be given as follows.

$$
\begin{aligned}
&D_1 = \frac{\sqrt{2L_{DM}(1+k)\,I_{out}V_{out}}}{V_{in}\sqrt{(1-\mathrm{V}_{out}/\mathrm{V}_{in})\,f_s}} \\
&D_2 = \frac{V_{in}}{V_{out}}D_1 \\
&\varphi = 0
\end{aligned}
\tag{4.34}
$$

As for the step-up case, the derivation for D_1, D_2, and φ under *Region* "*D*" can be given as

$$
\begin{aligned}
&D_1 = \frac{\sqrt{2L_{DM}(1+k)\,I_{out}V_{out}}}{V_{in}\sqrt{(1-\mathrm{V}_{in}/\mathrm{V}_{out})\,f_s}} \\
&D_2 = \frac{V_{in}}{V_{out}}D_1 \\
&\varphi = D_1 - D_2
\end{aligned}
\tag{4.35}
$$

It should be noted that the marginal power P_{mar} for unit gain case (V_{in}=V_{out}) is zero, which means only Eq. (3.32) will be adopted for calculation, and the inductance current i_L will keep as a quadrangle even though under light load condition.

2) Linearization and Normalization for I_{ZVS} and k

The relationship between I_{ZVS} and ZVS factor "k" will be discussed in this section. **Fig. 4-39** depicts the simulation results of inductance current i_L with different k. Under a certain load, adopting different k will obtain different amplitude of I_{ZVS}. **Fig. 4-39(a)** and **(b)** show the step-up case (900 V to 1 kV) under 50 kW and unit gain case (900 V to 900 V) under 40.5 kW, respectively. The DC output current I_{out} in these two cases is equal to 50 A and 45 A. As shown in **Fig. 4-39**, with a larger ZVS factor "k", a larger negative I_{ZVS} will be obtained. **Fig. 4-40(a)** depicts the amplitude of I_{ZVS} with k under different load conditions and different output voltages (input voltage keeps constant at 900 V). It can be easily found that I_{ZVS} and k are approximately linear relationships. Since different power levels and different output voltages will get different output current I_{out}, as shown in **Fig. 4-40(b)**, the amplitude of I_{ZVS} in **Fig. 4-40(a)** is normalized based on I_{out}. After the normalization and linearization, the relationship between I_{ZVS} and k can be approximated as below, especially when k is close to 0.

$$|I_{ZVS}|/I_{out} = 1.1k \tag{4.36}$$

With a required I_{ZVS} value from Eq. (4.18), the corresponding k can be obtained from Eq. (4.36). In practice, the value k will be slightly larger than the calculated value to guarantee the ZVS.

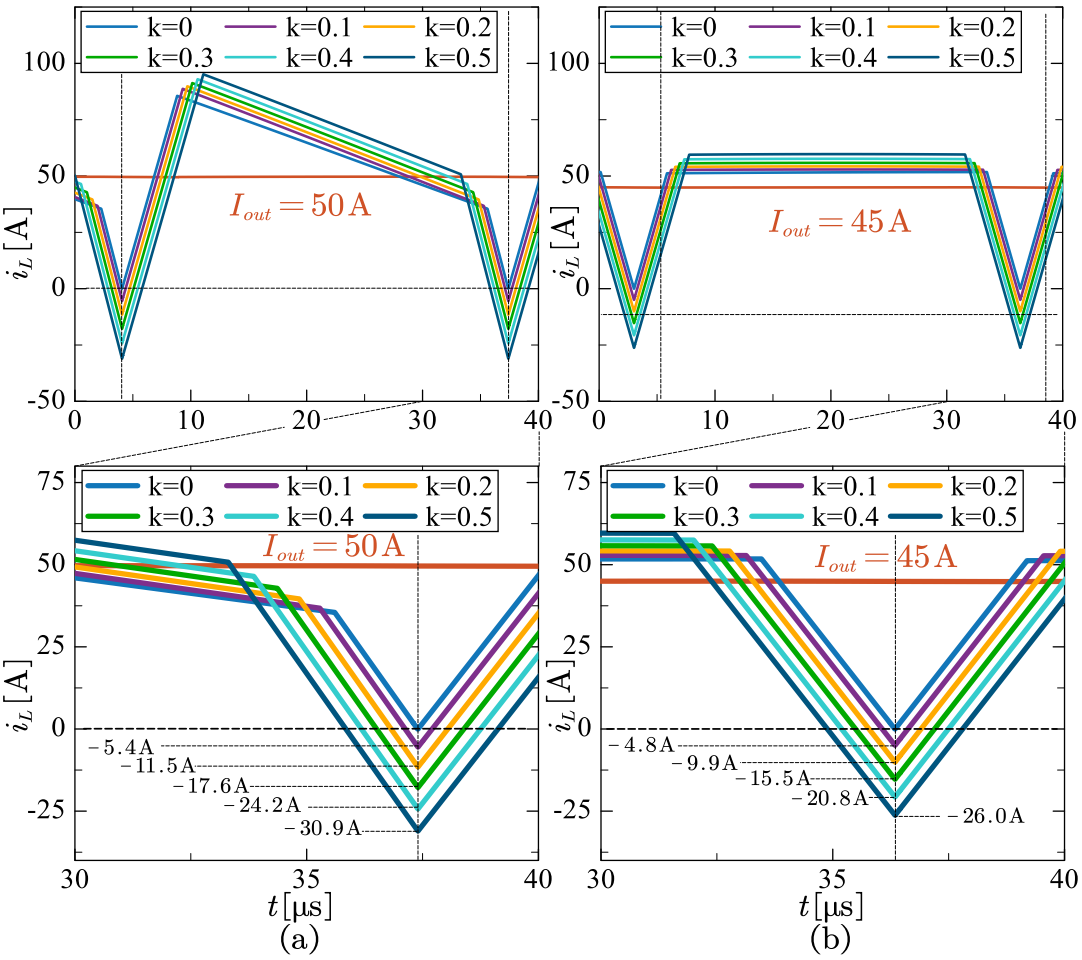


Fig. 4-39. The inductor current i_L with different ZVS factor k: (a) V_{in}=900V, V_{out}=1 kV, P=50 kW, and (b) V_{in}=900 V, V_{out}= V, P=40.5 kW.

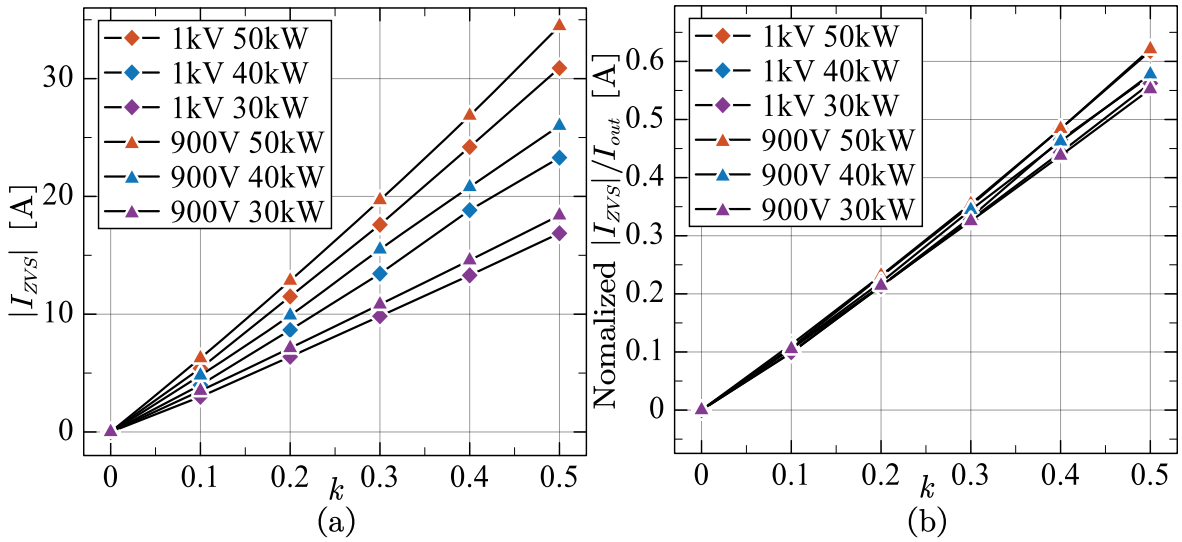


Fig. 4-40. The relationship between I_{ZVS} and k under different load conditions and output voltages: (a) before normalization, (b) after normalization. The time-domain current waveforms are shown in Fig. 4-39.

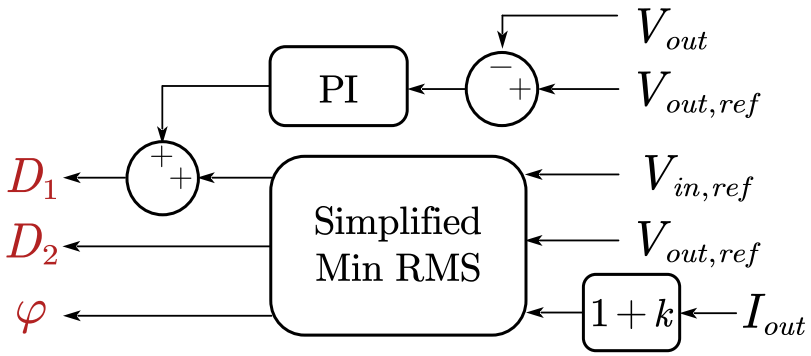


Fig. 4-41. Close-loop control diagram with simplified minimum rms current calculation block. The simplified minimum RMS calculation block can be found in Fig. 4-36(b).

3) Close-loop Control with Simplified Calculation Block

With a simplified minimum rms current calculation block, as shown in **Fig. 4-36(b)**, the close-loop control diagram for this 3-L buck-boost converter was plotted in **Fig. 4-41**. Based on $V_{in,ref}$, $V_{out,ref}$, I_{out} and k, the open-loop values of three basic control variables D_1, D_2, and φ can be obtained. However, if there is a tolerance on the value of L_{DM} and measured I_{out}, the actual output voltage V_{out} might have a slight difference from the reference value $V_{out,ref}$. In order to compensate for these tolerances and regulate the output voltage accurately, an extra "PI" controller was adopted to slightly change D_1. From (4.17), the output voltage V_{out} is proportional to D_1. For instance, if the measured V_{out} is larger than the reference value $V_{out,ref}$, the output of the "PI" controller is negative. This closed-loop control will decrease D_1 to guarantee the actual output voltage V_{out} is exactly equal to the reference value $V_{out,ref}$.

4.3.3 Decoupled Active Balance Control

1) Proposed ΔD_1 and ΔD_2 for Voltage Balance

As mentioned before, in order to reduce CM voltage, this proposed 3-L buck-boost converter should theoretically have a symmetric driving gate signal. **Fig. 4-42** shows the detailed circuit diagram of this proposed 3-L buck-boost converter. On the input side, both top and bottom duties D_{1T} and D_{1B} should be equal to D_1. As for the output side, both D_{2T} and D_{2B} should be equal to D_2.

$$\begin{cases} D_{1T} = D_{1B} = D_1 \\ D_{2T} = D_{2B} = D_2 \end{cases} \tag{4.37}$$

The duties D_1 and D_2 could be obtained by the close-loop control, as shown in **Fig. 4-42**. As shown in **Fig. 4-43**, at the input side, V_{iT} and V_{iB} are the voltages across the split top and bottom capacitors. V_{oT} and V_{oB} are the voltages across the output side split capacitors. The relation between total input (output) voltages and split V_{iT} and V_{iB} (V_{oT} and V_{oB}) can be easily derived as

$$\begin{cases} V_{in} = V_{iT} + V_{iB} \\ V_{out} = V_{oT} + V_{oB} \end{cases} \tag{4.38}$$

Due to the tolerance between top and bottom half bridges, such as the gate driver propagation delay, the split capacitor voltage imbalance might happen on both the input and output sides ($V_{iT} \neq V_{iB}$ and $V_{oT} \neq V_{oB}$). However, the four basic operation modes *Mode I-IV* in **Fig. 4-31** have no capability to regulate the balance on either the input or output side because both sides split capacitor currents i_{Cin} and i_{Cout} in **Fig. 4-42** are always 0. Therefore, the ideal symmetric 3-L buck-boost converter with only four basic modes might suffer from the imbalance issue on both the input and output sides.

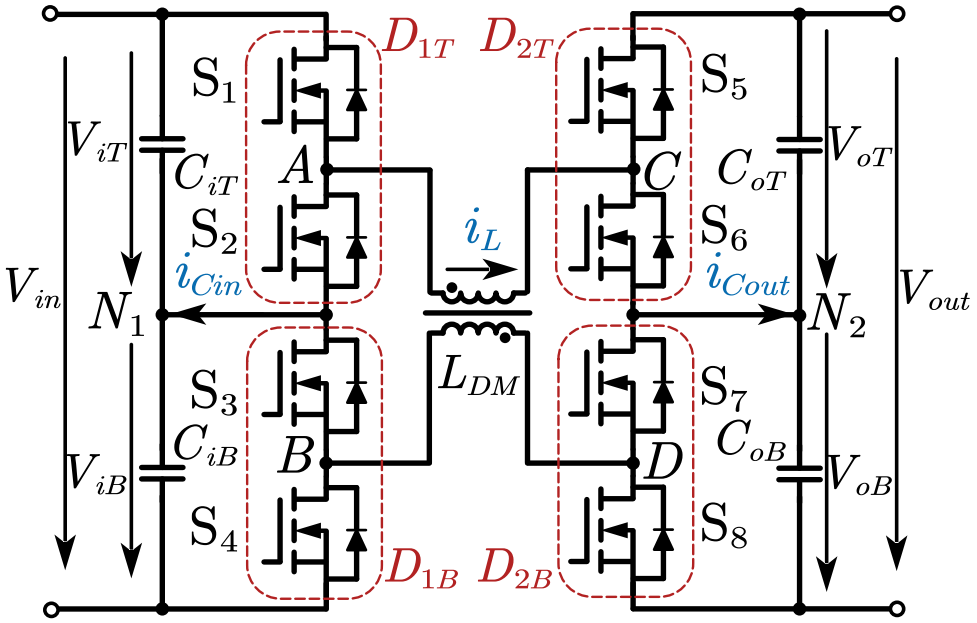


Fig. 4-42. Circuit diagram of the 3-L buck-boost converter with decoupled balance control.

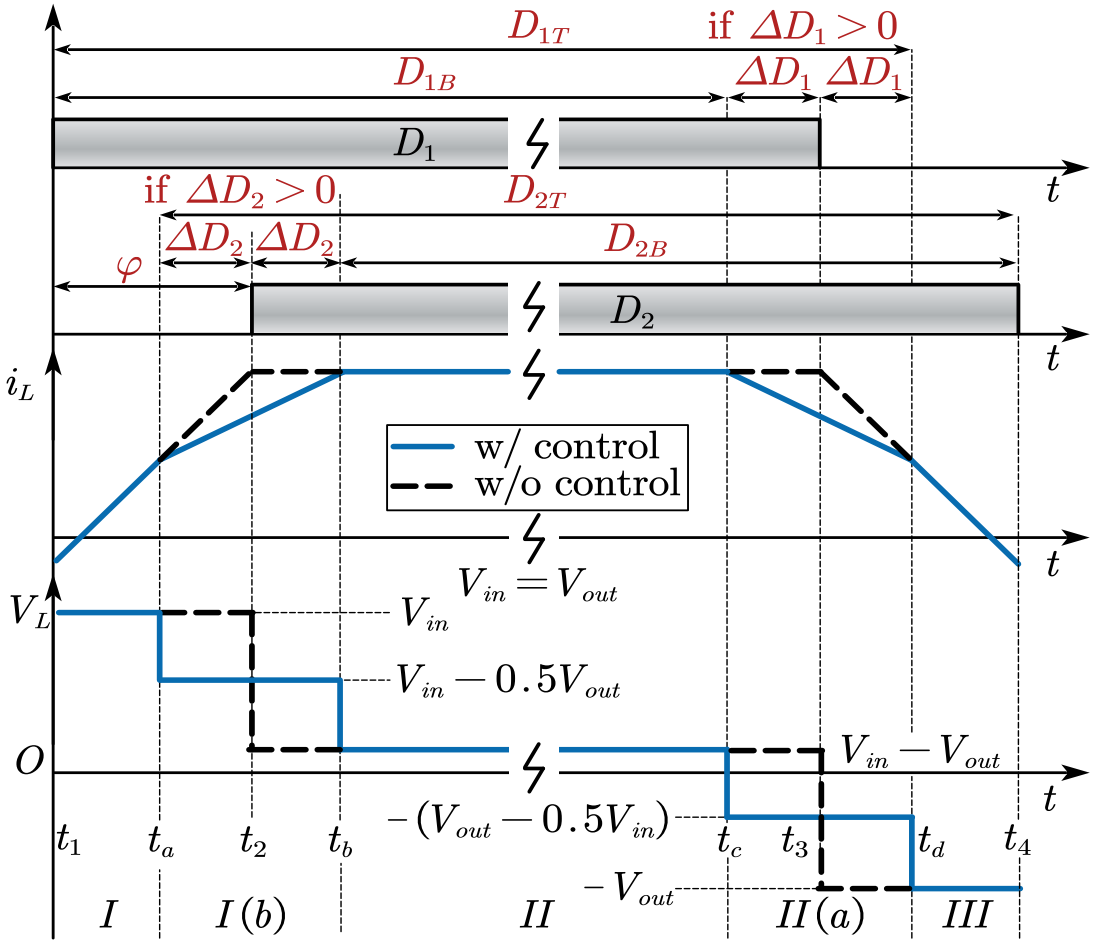


Fig. 4-43. The corresponding waveforms of the gate signals, inductor current i_L, and inductor voltage V_L. The circuit diagram can be found in Fig. 4-42.

In order to decouple the balance control of the input and output sides, two small duty differences ΔD_1 and ΔD_2 have been introduced, as shown in **Fig. 4-43**. With these two control variables, the top side duties $D_{1(2)T}$ will not equal to the bottom side $D_{1(2)B}$ anymore, and the new relationship can be given as

$$\begin{cases} D_{1(2)T} = D_{1(2)} + \Delta D_{1(2)} \\ D_{1(2)B} = D_{1(2)} - \Delta D_{1(2)} \end{cases} \tag{4.39}$$

From Eq. (4.39), the total voltage gain V_{out}/V_{in} can still be maintained as D_1/D_2, as shown in Eq. (4.40), which means that the mid-point balancing control will not influence the output regulation.

$$\frac{V_{out}}{V_{in}} = \frac{D_{1T} + D_{1B}}{D_{2T} + D_{2B}} = \frac{D_1}{D_2} \tag{4.40}$$

2) Four Intermediate Operation Modes

After introducing ΔD_1 and ΔD_2, **Fig. 4-43** shows the gating signals $D_{1(2)}$, $D_{1(2)T}$, $D_{1(2)B}$, and inductor current i_L and voltage V_L. The inductor voltage V_L applied to the coupled inductor can be given as

$$V_L = V_{AC} + V_{DB} \tag{4.41}$$

As shown in **Fig. 4-43**, compared with no balancing control, the current i_L will have two small differences during t_a-t_b and t_c-t_d. These two small differences in i_L are caused by different voltages of V_L across the coupled inductors. According to the polarity of ΔD_1 and ΔD_2, four possible new intermediate modes, *Mode I*(*a*), *Mode I*(*b*), *Mode II*(*a*), and *Mode II*(*b*), will be introduced as shown in **Fig. 4-44**. Each intermediate mode has the capability to control either the input or output side balancing. The detailed balancing effects of these four modes are listed in **Table 4-8**. Since *Mode I*(*a*) and *Mode I*(*b*) can only impact the output side split capacitor current i_{Cout}, ΔD_1 is dedicated to controlling the output side balance. As for the output side, ΔD_2 can be adopted to control the input side split capacitor current i_{Cin}.

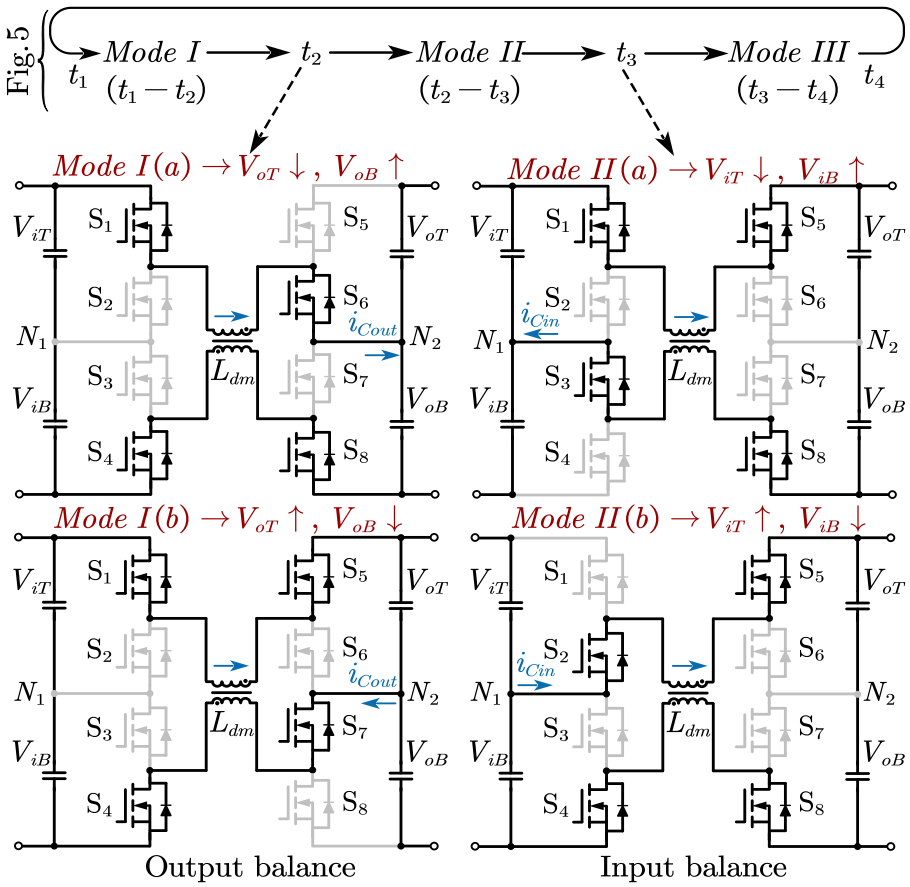


Fig. 4-44. Decoupled active balance control: (a) input side, (b) output side. The circuit diagram after introducing balance control is shown in Fig. 4-42.

Table 4-8 BALANCING EFFECT OF FOUR INTERMEDIATE OPERATION MODES

Mode	Side	i_{Cin} and i_{Cout}	Balancing Effect	$\Delta D_{1(2)}$ polarity
Mode I(*a*)	output	i_{Cin}=0, i_{Cout}>0	$V_{oT}\downarrow$ $V_{oB}\uparrow$	negative ΔD_2
Mode I(*b*)		i_{Cin}=0, i_{Cout}<0	$V_{oT}\uparrow$ $V_{oB}\downarrow$	positive ΔD_2
Mode II(*a*)	input	i_{Cin}>0, i_{Cout}=0	$V_{iT}\downarrow$ $V_{iB}\uparrow$	positive ΔD_1
Mode II(*b*)		i_{Cin}<0, i_{Cout}=0	$V_{iT}\uparrow$ $V_{iB}\downarrow$	negative ΔD_1

For example, if ΔD_1 and ΔD_2 are both positive, as shown in **Fig. 4-43**, *Mode I*(*b*) and *Mode II*(*a*) will be introduced during t_a-t_b and t_c-t_d. Based on the balancing effect in Table II, *Mode I*(*b*) will increase the V_{oT} and decrease the V_{oB}, and *Mode II*(*a*) will decrease the V_{iT} and increase the V_{iB}. Therefore, the input and output side balance control can be decoupled by ΔD_1 and ΔD_2.

3) Close-loop Control and Simulation

Since the input and output split capacitor voltages can be separately controlled by ΔD_1 and ΔD_2, the decoupled active balance was proposed in **Fig. 4-45**. By measuring the split capacitor voltages V_{iT}, V_{iB}, V_{oT}, and V_{oT}, the input and output voltage differences (V_{iT} -V_{iB}) and (V_{oB} -V_{OT}) can be feedbacked. According to the balance mechanism listed in **Table 4-8**, two "PI" controllers can be adopted to regulate the input and output balance, respectively. The outputs of these two "PI" controllers are the ΔD_1 and ΔD_2. Based on the total output voltage closed-loop control, as shown in **Fig. 4-41**, three basic control variables, D_1, D_2 and φ, can be obtained in advance, with these three basic variables and $\Delta D_{1(2)}$, from Eq. (4.39), the duties $D_{1T(B)}$ for the input side, and $D_{2T(B)}$ for output side can be determined, respectively. As shown in **Fig. 4-42** and **Fig. 4-45**, $D_{1T(B)}$ is the driving signal for switches $S_{1(4)}$, and $D_{2T(B)}$ are the driving signals for $S_{5(8)}$.

In order to verify the proposed active decoupled balance control shown in **Fig. 4-45**, a unit gain case from 900 V to 900 V under 45 kW has been simulated, as shown in **Fig. 4-46**. To create some imbalance because of the circuit tolerance, the initial value of the input and output split capacitor voltages V_{iT}, V_{iB} V_{OT} V_{oB} were set to 500 V, 400 V, 400 V, and 500 V. Before 3 ms, only output voltage close loop control shown in **Fig. 4-41** was adopted. As explained previously, this closed-loop control has no capability to control either input or output balance because of the zero split capacitor currents i_{Cin} and i_{Cout}.

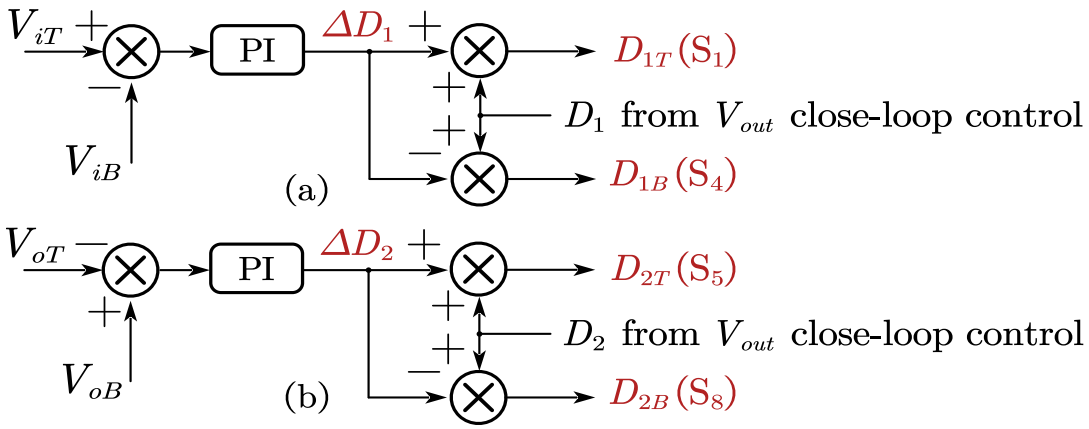


Fig. 4-45. Decoupled active balance control: (a) input side, (b) output side. The closed-loop control diagram can be found in Fig. 4-41.

At 3 ms, the proposed decoupled active balance control shown in **Fig. 4-45** was added on both the input and output sides. After 3 ms, with this decoupled control, the input and output split capacitor voltages V_{iT}, V_{iB} V_{OT} V_{oB} begin to converge towards the equilibrium value 450 V. After zooming in the inductor current i_L at 3 ms, intermediate modes *Mode I*(a) and *Mode II*(b) can be seen because V_{iT} is larger than V_{iB} at the input side, and V_{oT} is smaller than V_{oB} at the output side.

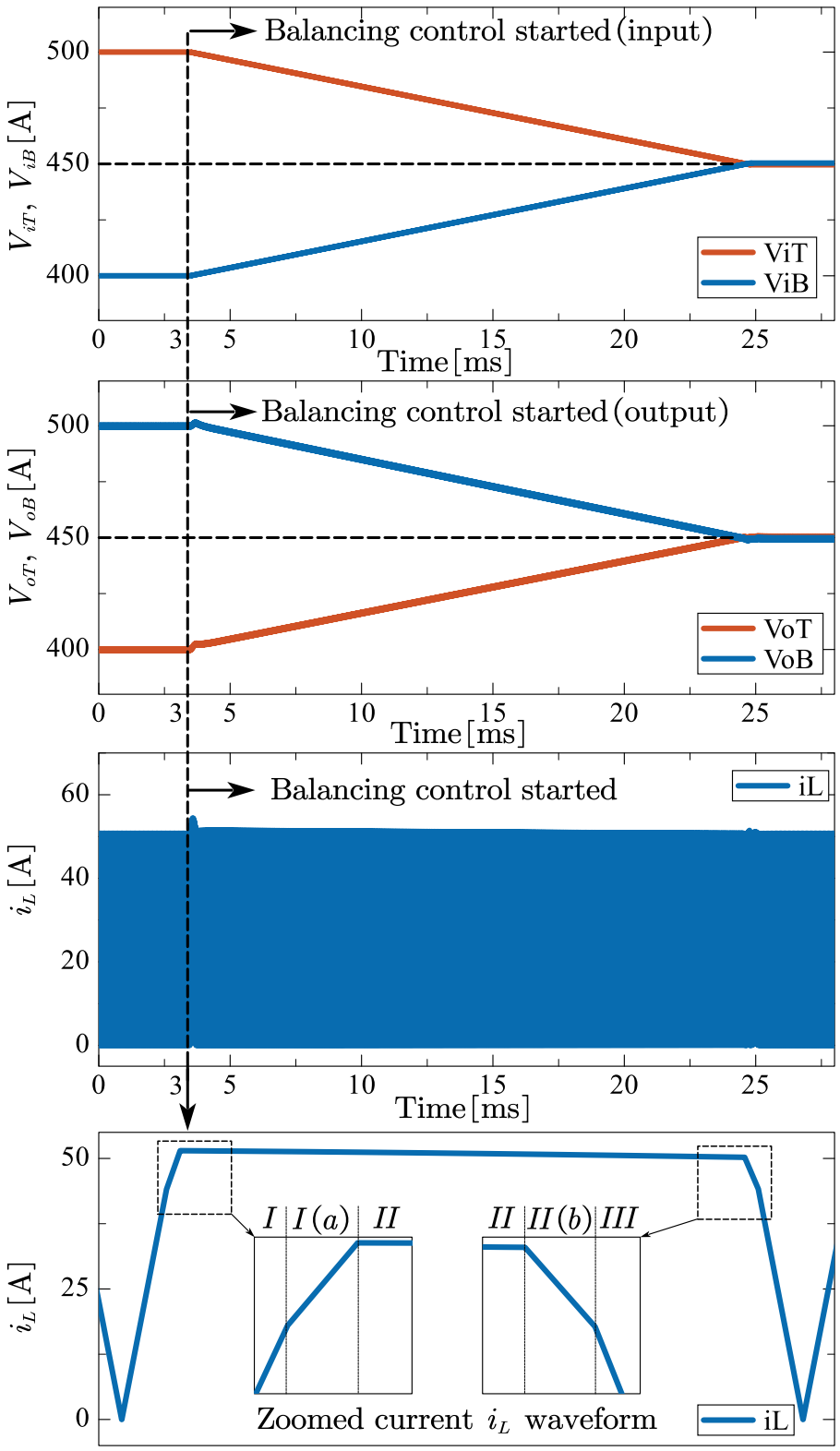


Fig. 4-46. Simulation results for the decoupled active balance control under 45 kW unit gain case (900 V to 900 V). The parameters in the simulation are listed in Table 4-8.

4.3.4 A 50 kW 3-L Buck-Boost Converter Prototype

1) Prototype Implementation and Hardware Setup

As shown in **Fig. 4-47**, a 50 kW 3-L buck-boost converter was built first. The specifications have been listed in **Table 4-7**, and more technical details of this proposed 3-L buck-boost converter are listed in **Table 4-9**. In order to improve the power density and handle large DC bias flux, planar magnetics was adopted with an amorphous AMCC core from *Hitachi*. The heavy copper printed circuit board (PCB) technique has been used for inductor windings to handle large currents. The turns numbers are 7:7, and the thickness of the trace is 15 oz. A two-board design was adopted to reduce the fringing effect loss. Following the design procedure of L_{DM} in **Fig. 4-33**, the airgap is designed as 1.8 mm, and coupled inductors with 50.4 μH L_{DM} has been obtained. Due to the low-profile design, as shown in **Fig. 4-47(b)**, the power density of this planar inductor is 3.5 kW/in^3. As for the split dc-link capacitors C_{iT}, C_{iB}, C_{oT}, and C_{oB} shown in **Fig. 4-42**, ten 20 μF film capacitors are connected in parallel. Due to the small turn-on resistance $R_{ds,on}$ (4 mΩ at 25 ºC), four 1.2 kV SiC half-bridge modules *GE12047CCA3* from *GE* have been adopted.

To verify the CM noise reduction, **Fig. 4-48(a)** and **(b)** show the testing setups for the proposed 3-L buck-boost converter and typical FSBB converter, respectively. For both setups, a 50 Arms Line Impedance Stabilization Network (LISN) was connected at the input side, and a current transducer (CT) was used to measure the CM current. The current $i_{CT,mes}$ is the output of the CT. Since the selected CT has a 30 dB external attenuation, the measured CM current i_{CM} can be expressed as

$$i_{CM} = 10^{1.5} \cdot i_{CT,mes}/2 \tag{4.42}$$

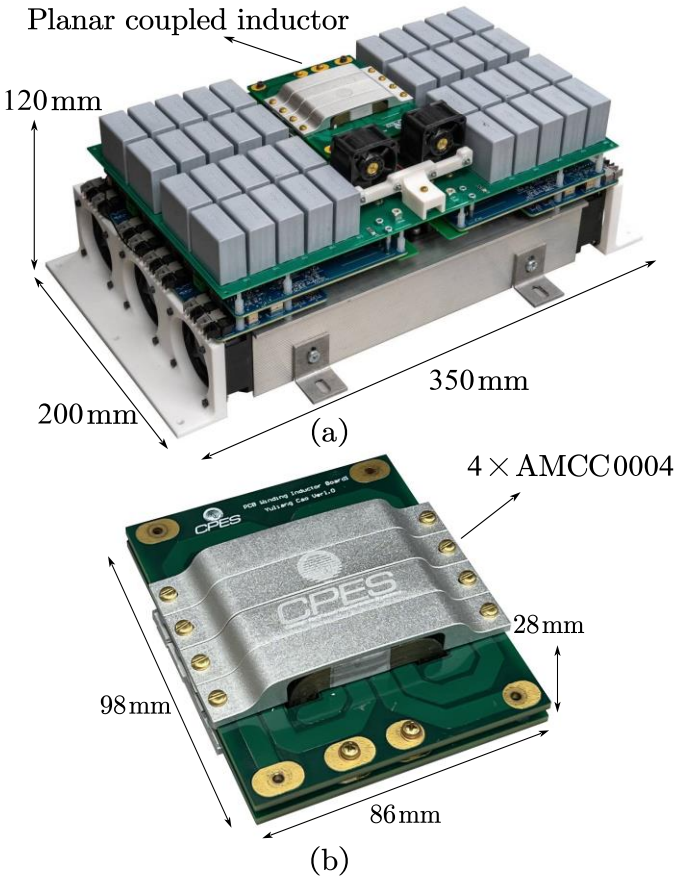


Fig. 4-47. 50 kW 3-L buck-boost converter prototype with planar coupled inductors: (a) whole power stage, (b) heavy copper coupled inductors. The circuit parameters are listed in Table 4-9.

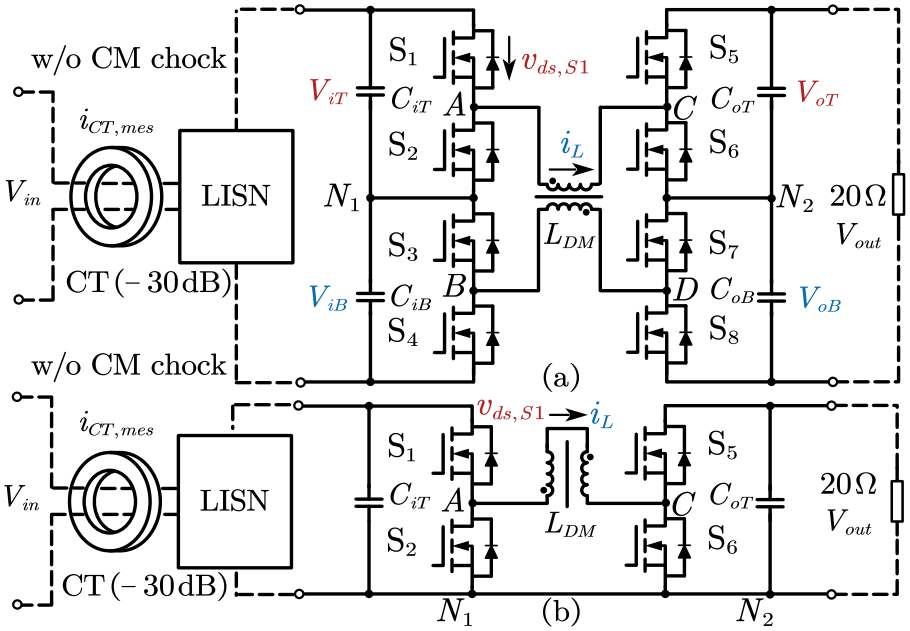


Fig. 4-48. Diagrams of the experimental setups: (a) proposed 3-L buck-boost converter, (b) typical FSBB converter. The prototype can be found in Fig. 4-47.

Table 4-9 TECHNICAL DETAILS OF 3-L BUCK-BOOST CONVERTER

	Component		Parameter	Description
Coupled Inductors	core		AMCC-0004 × 4	Hitachi amorphous core
	Pri. turns		7 (two layers parallel)	Heavy copper PCB (15 oz)
	Sec. turns		7 (two layers parallel)	Heavy copper PCB (15 oz)
	L_{DM}		50.4 µH	Differential mode inductance
	Air gap		1.8 mm	Ceramic pad for the air gap
Capacitors & SiC MOSFETs	C_{iT}		20 µF × 10	Split DC bus film capacitor
	C_{iB}		20 µF × 10	Split DC bus film capacitor
	C_{oT}		20 µF × 10	Split DC bus film capacitor
	C_{oT}		20 µF × 10	Split DC bus film capacitor
	SiC Module		1.2 kV half bridge × 4	*GE12047CCA3* 4 mΩ at 25 ºC
Cooling System	Fan	Planar Inductor	24 V_{DC} (5 W) × 2	25× 25×20 mm^3 (10.5 CFM)
		Module heatsink	24 V_{DC} (3 W) × 6	60×60 ×25 mm^3 (5.5 CFM)

The experimental results in the next part will only show the CM current i_{CM} after converting. A 900 V DC source was connected at the input side, and the output side adopted a 20 Ω resistance load. As shown in **Fig. 4-48(b)**, the top half of the 3-L buck-boost converter in Fig. 4-48(a) was adopted as a typical FSBB converter, and two mid-points, N1 and N2, were connected. To obtain the same inductor current i_L in the typical FSBB converter (same value of L_{DM}), the coupled inductors were connected, as shown in **Fig. 4-48(b)**. It should be noted that no CM choke was used in these two setups. The following experimental results for both the 3-L buck-boost converter and typical FSBB will keep the same setup, as shown in **Fig. 4-48**. Since this 3-L buck-boost converter was adopted on the rear end, more details about the whole grid-interface converter, including gate driver design and communication design, can be found in [64]–[66].

2) Experimental Results for CM Noise Suppression

Fig. 4-49 shows the experimental results for the 3-L buck-boost converter with decoupled active balance control. The input voltage V_{in} is kept as 900 V. With four different output voltages V_{out}, the step-up case (V_{out}=1 kV), unit gain case (V_{out}=900 V), and step-down cases (V_{out}=800V, V_{out}=500 V) are depicted in **Fig. 4-49(a)-(d)**, respectively. As shown in **Fig. 4-48(a)**, since the load is a constant 20 **Ω** resistance, the output powers for these four cases are 50 kW, 40.5 kW, 32 kW, and 12.5 kW. The corresponding output current is 50 A, 45 A, 40 A, and 25 A. As shown in **Fig. 4-49**, it can be easily seen that both the input and output side voltages V_{iT}, V_{iB}, V_{oT}, and V_{oT} have been balanced well, which could verify the proposed decoupled active balance control.

As for the soft switching, with 300 ns deadtime and 3.2 nF time-related output capacitance from 0 to 500 V, the required negative ZVS current I_{ZVS} can be calculated as -21.3 A from Eq. (4.18). According to the approximate relationship between I_{out} and I_{ZVS} from (20), the ZVS factor k was set as 1.4 with a small margin. As shown in **Fig. 4-49**, under different output currents, 50 A (V_{out}=1 kV), 45 A (V_{out}=900 V), 40 A (V_{out} =800 V), and 25 A (V_{out}=500 V), the measured I_{ZVS} are -22.7 A, -19.4 A, -16.5 A, and -12.2 A. With these measured I_{ZVS}, the approximately linear relationship in (20) between I_{out} and I_{ZVS} can also be verified.

The experimental results without the decoupled active control were plotted in **Fig. 4-50**. Except for the balance control, **Fig. 4-50** keeps the same testing conditions as **Fig. 4-49**. As mentioned before, due to the circuit tolerances, distinguished voltage differences (up to 92 V) existed at both the input and output sides without a balance control.

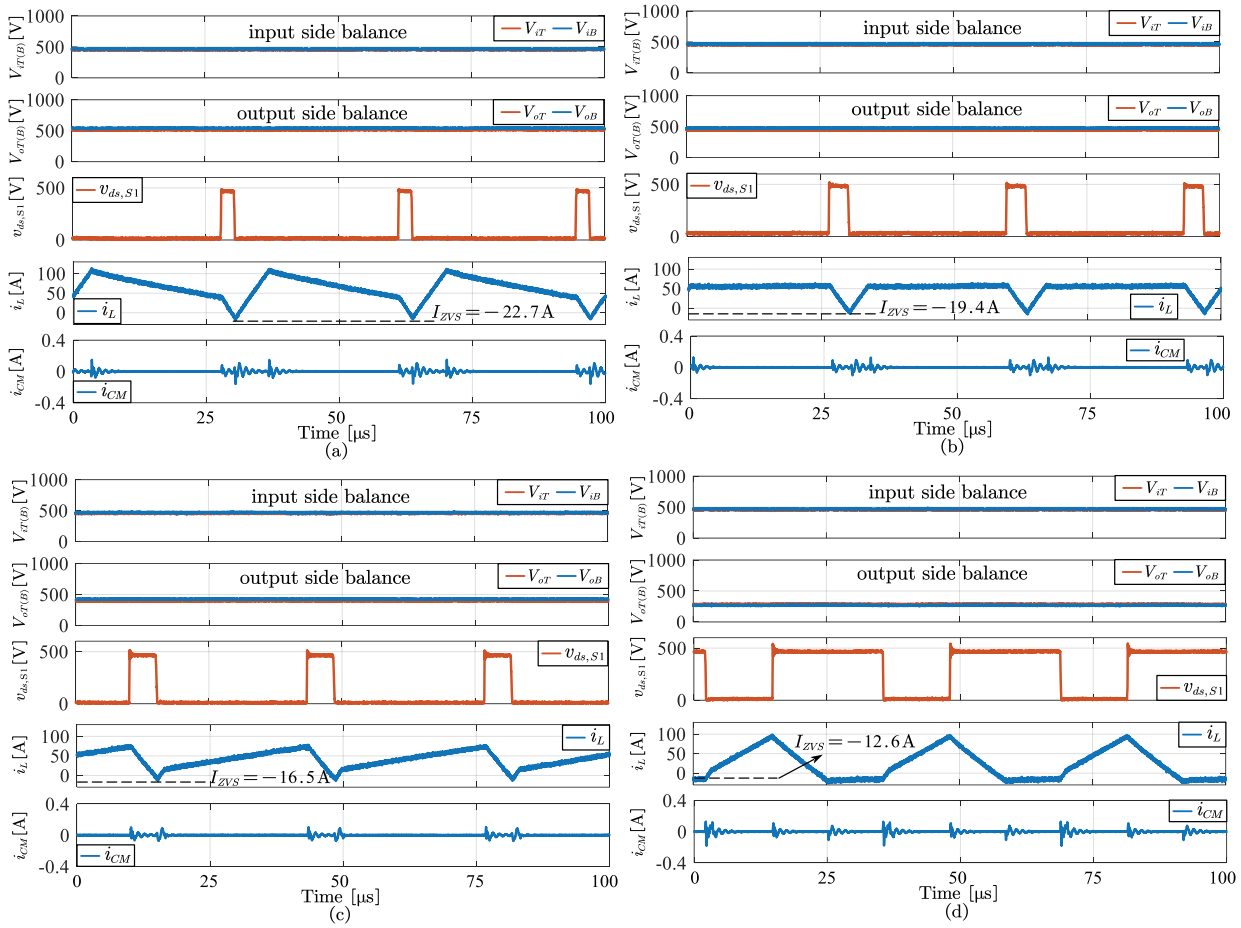


Fig. 4-49. Experimental results of the 3-L buck-boost converter with decoupled balance control: (a) V_{out}=1 kV, (b) V_{out}=900 V, (c) V_{out}=800 V, (d) V_{out}=500 V. The circuit parameters are listed in Table 4-9.

Following the setup shown in **Fig. 4-48(b)**, **Fig. 4-51** shows the experimental results for a typical FSBB converter. Since the rating voltage of the SiC module is 1.2 kV, for a safety operation, only 900 V, 800 V, and 500 V output cases have been conducted in a typical FSBB converter. The testing results of these three cases have been plotted in **Fig. 4-51(a)-(c)**, respectively. Compared with the results of the 3-L buck-boost converter shown in **Fig. 4-50** and **Fig. 4-51**, the inductance current iL should be the same because the inductance value LDM has been kept the same.

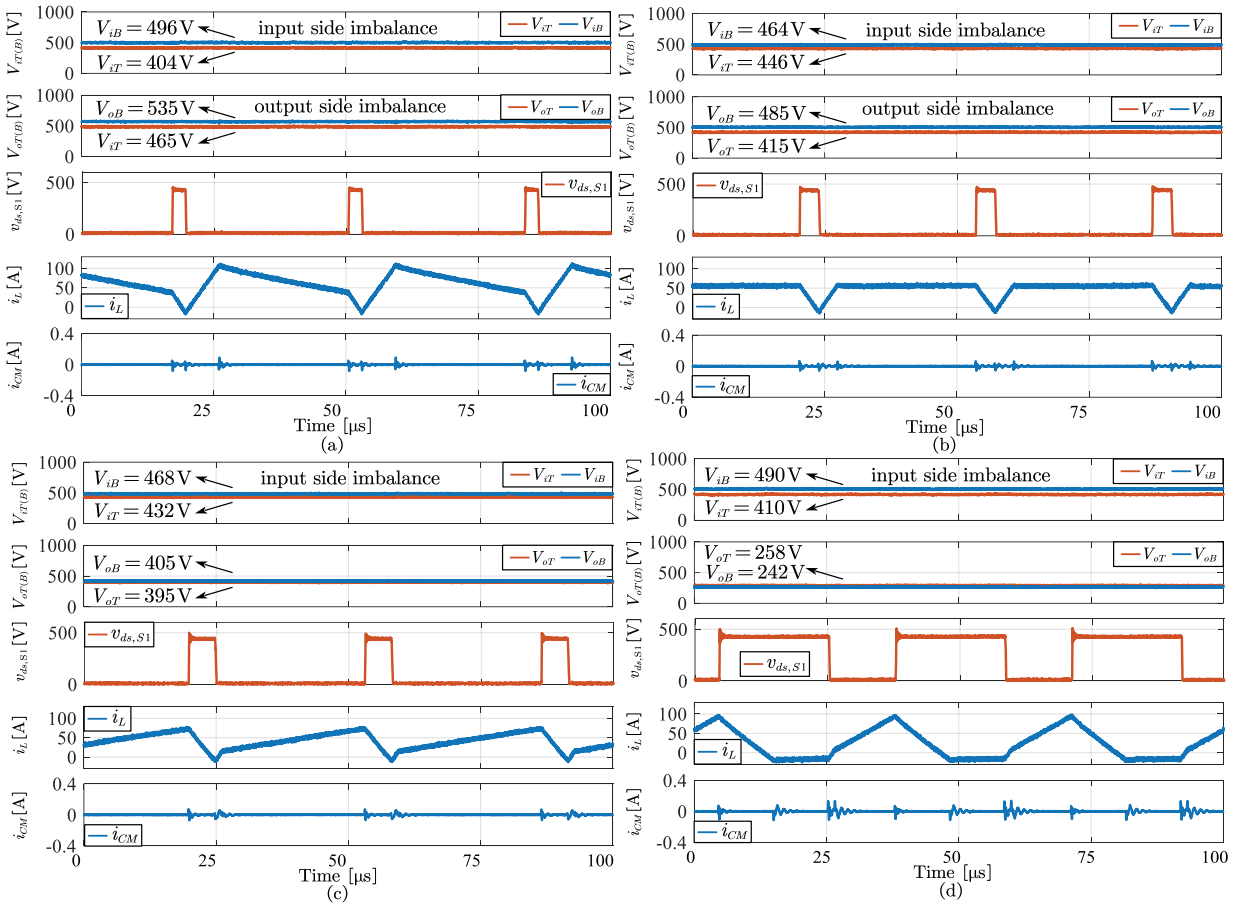


Fig. 4-50. Testing results of the 3-L buck-boost converter without decoupled balance control: (a) V_{out}=1 kV, (b) V_{out}=900 V, (c) V_{out}=800 V, (d) V_{out}=500 V. The circuit parameters are listed in Table 4-9.

Fig. 4-52 plots all the measured CM current results from **Fig. 4-49** to **Fig. 4-51** in the frequency domain (150 kHz to 30 MHz). The results of 900 V, 800 V, and 500 V output voltages are represented in **Fig. 4-52(a)-(c)**, respectively. The results of the 3-L buck-boost converter with balance control, without balance control, and typical FSBB converter are depicted together with the standard requirement DO-160.

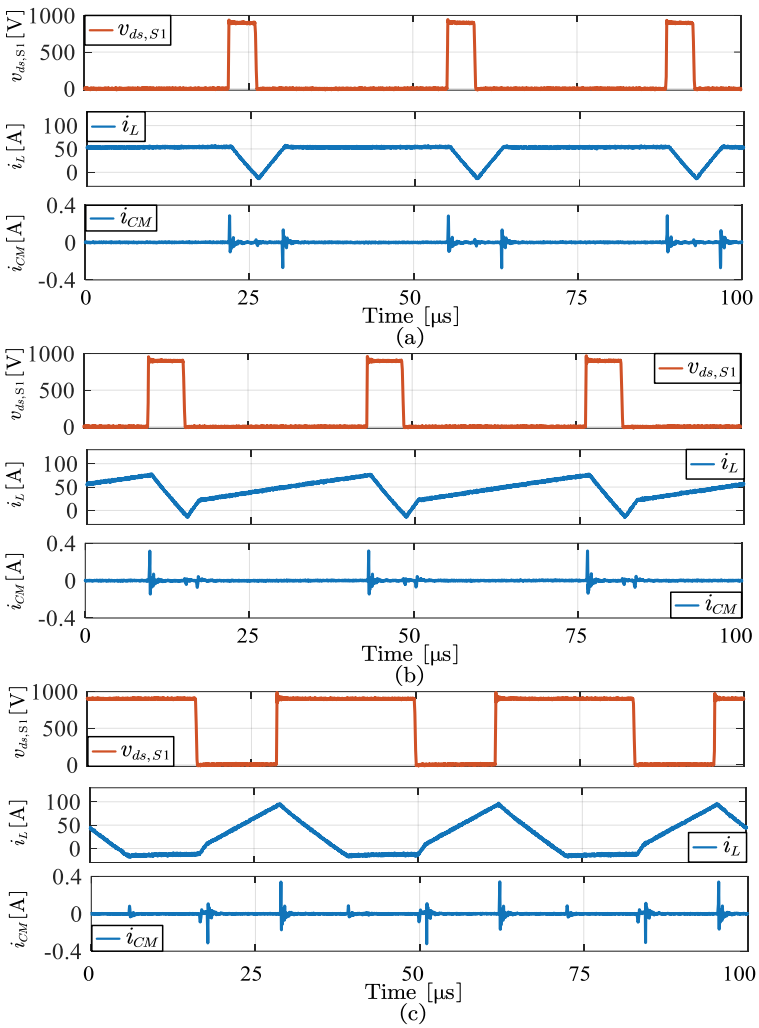


Fig. 4-51. Testing results of the typical FSBB converter: (a) V_{out}=900 V, (b) V_{out}=800 V, (c) V_{out}=500 V. The circuit parameters are listed in Table 4-9.

From 150 kHz to 500 kHz, the amplitude of CM current i_{CM} is close in all three cases. From 500 kHz to 1 MHz, compared with typical FSBB, CM current i_{CM} of 3-L buck-boost with or without balance control both have up to 15 dB attenuation. After 1 MHz, the merits of the 3-L buck boost are more obvious. From 3 MHz to 30 MHz, the 3-L buck-boost with or without balance control both have about 15 dB (up to 25 dB) attenuation.

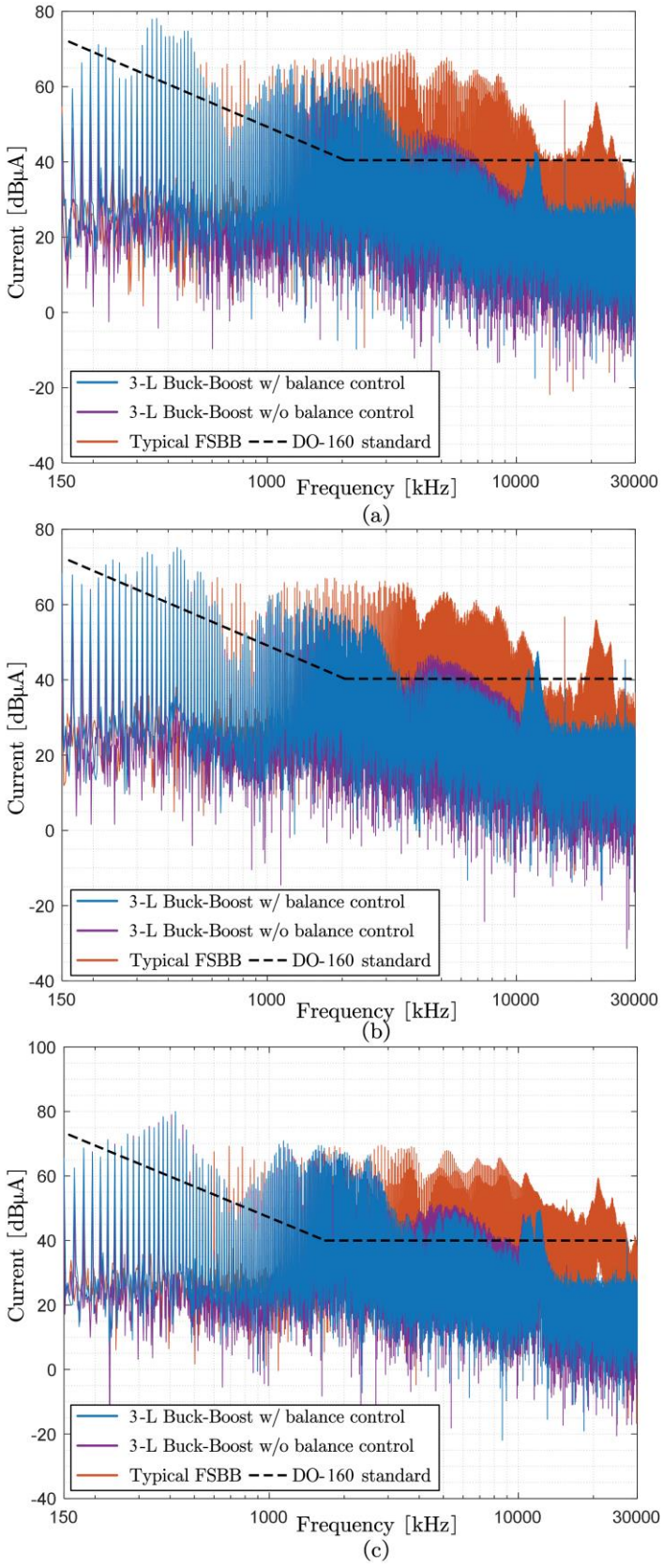


Fig. 4-52. Measured CM current results under different cases: (a) V_{out}=900 V, (b) V_{out}=800 V, (c) V_{out}=500 V.

The dynamic experimental results for the soft start-up and close-loop output voltage regulation have been shown in **Fig. 4-53(a)** and **(b)**, respectively. The load is still a 20 Ω resistance. During the close-loop soft start-up, the input voltage V_{in} was first pre-charged to 900 V. To increase the output voltage V_{out} from 0 V to 1 kV, a ramp reference voltage $V_{out,ref}$ is adopted in the close-loop control.

After finishing the start-up procedure, to verify the close-loop output regulation capability, a triangular output voltage reference $V_{out,ref}$ from 500 V to 1 kV and back again, was given, as shown in **Fig. 4-53(b)**. With the simplified close-loop control, the output can be well-regulated because V_{out} can follow the reference $V_{out,ref}$.

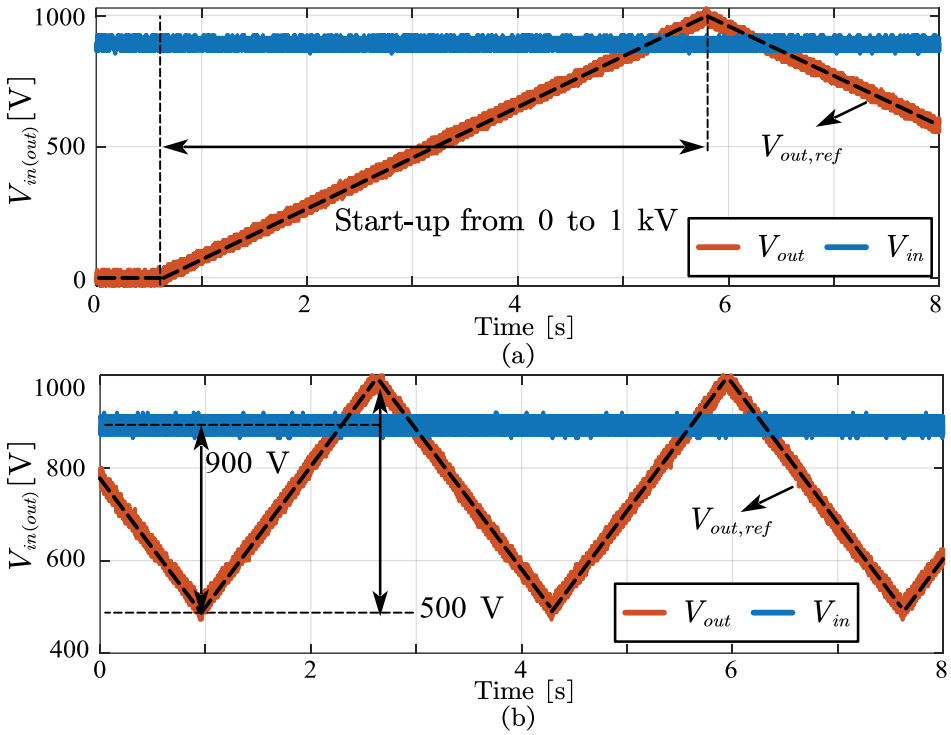


Fig. 4-53. Dynamic close-loop experimental results: (a) soft start-up, (b) output voltage regulation. The circuit parameters are listed in Table 4-9.

3) Switching Transition Results and I_{ZVS} with different "*k*"

Following the setup shown in **Fig. 4-48(a)**, **Fig. 4-54** and **Fig. 4-55** plot the zoomed waveforms for the proposed 3-L buck-boost converter without or with the balance control. The deadtime t_d has been changed from 300 ns to 600 ns in these two cases. In **Fig. 4-54** and **Fig. 4-55**, from top to bottom, eight channels scope was used to record the waveforms of $v_{ds,S2}$, $v_{ds,S3}$, ($v_{ds,S2}$- $v_{ds,S3}$), $v_{ds,S6}$, $v_{ds,S7}$, ($v_{ds,S6}$ - $v_{ds,S7}$), $i_{CT,mes}$, v_{N1N2}, i_L. The steady state values of $v_{ds,S2}$, $v_{ds,S3}$, and vds,S6, vds, and S7 can indicate the split DC cap voltages on both input and output sides V_{iT}, V_{iB}, V_{oT}, and V_{oB}. ($v_{ds,S2}$- $v_{ds,S3}$) and ($v_{ds,S6}$ - $v_{ds,S7}$) are two CM noise sources in this topology.

As shown in **Fig. 4-54(b)** and **(c)**, the falling edges of $v_{ds,S2}$, $v_{ds,S3}$ and the rising edges of $v_{ds,S6}$, $v_{ds,S7}$ hardly have any delay. However, due to no balance control, the steady state will have a difference. After adding the balance control as shown in **Fig. 4-55(b)** and **(c)**, $v_{ds,S6}$, and $v_{ds,S7}$ can match very well in both switch transition and steady state.

To verify the approximate linear relationship between "ZVS factor" *k* and negative ZVS current I_{ZVS}, the experimental results with different *k* under V_{out}=900 V, *P*=45 kW, t_d=600 ns are plotted in **Fig. 4-57**. When *k*=0.2, 0.3, 0.4, 0.5, the negative current I_{ZVS} are equal to -10 A, -15.6 A, -20.8 A, and -26 A, respectively. Therefore, the approximate linear relationship between I_{ZVS} and "*k*" in (4.36) can be verified.

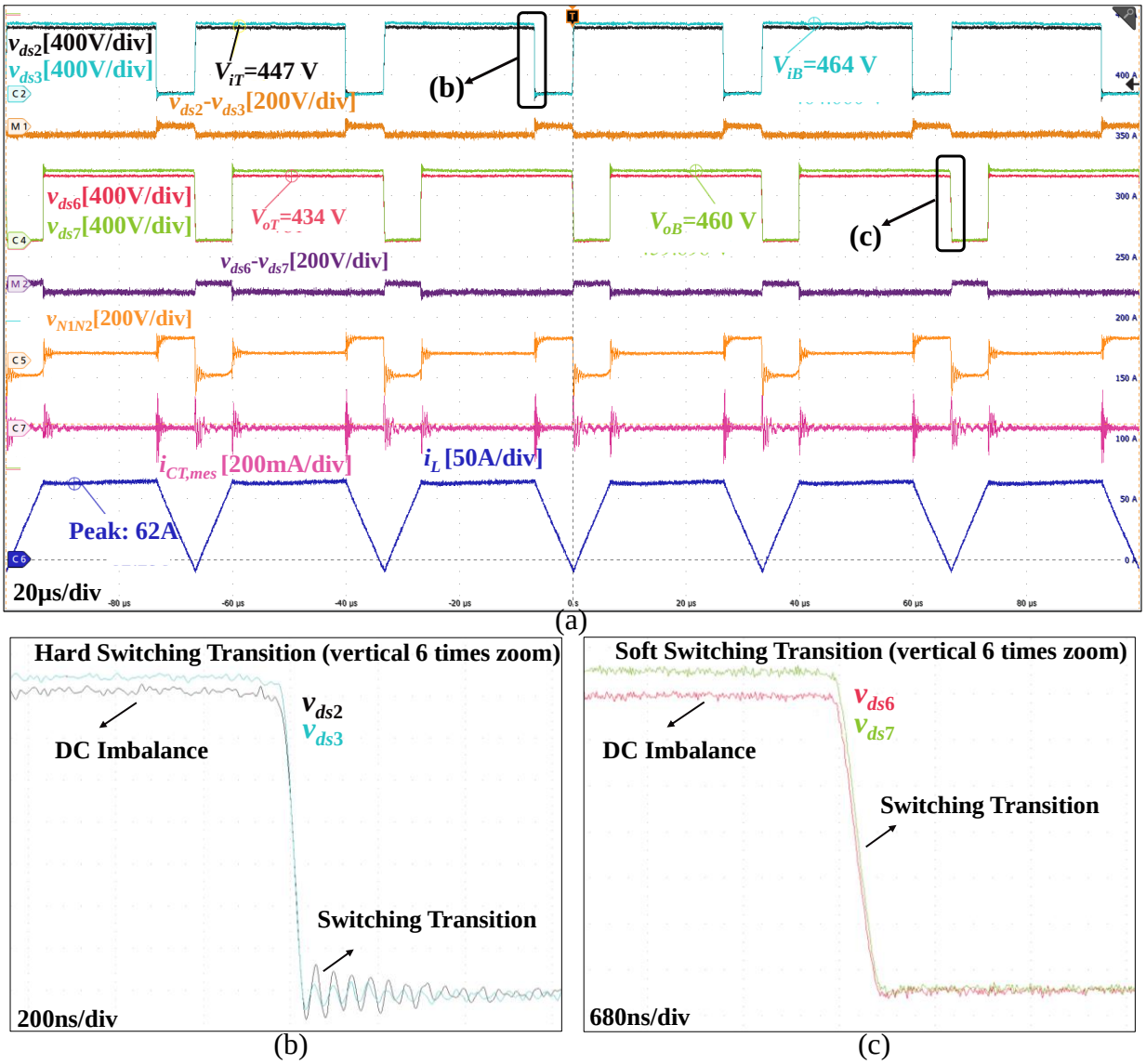


Fig. 4-54. Experimental results (V_{out}=900 V, P=45.5 kW t_d=600 ns) without decoupled active balance control: (a) large scale voltage and current waveforms, (b) zoomed $v_{ds,2}$ and $v_{ds,3}$ during hard switching transition. (c) zoomed $v_{ds,6}$ and $v_{ds,7}$ during soft-switching transition. The circuit parameters are listed in Table 4-9.

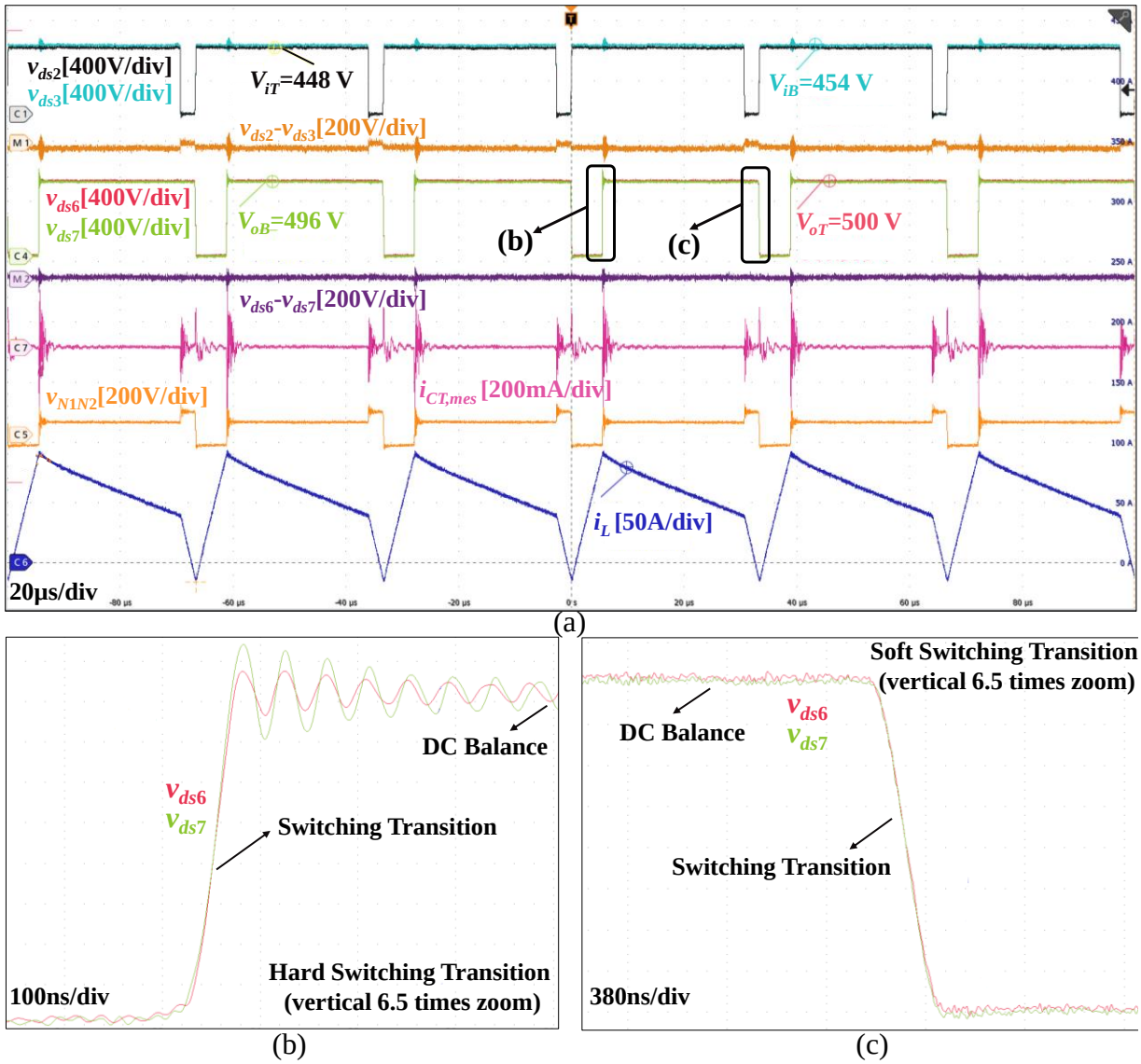


Fig. 4-55. Experimental results (V_{out}=1 kV, P=50 kW t_d=600 ns) with decoupled active balance control: (a) large scale voltage and current waveforms, (b) zoomed $v_{ds,6}$ and $v_{ds,7}$ during hard switching transition. (c) zoomed $v_{ds,6}$ and $v_{ds,7}$ during soft-switching transition. The circuit parameters are listed in Table 4-9.

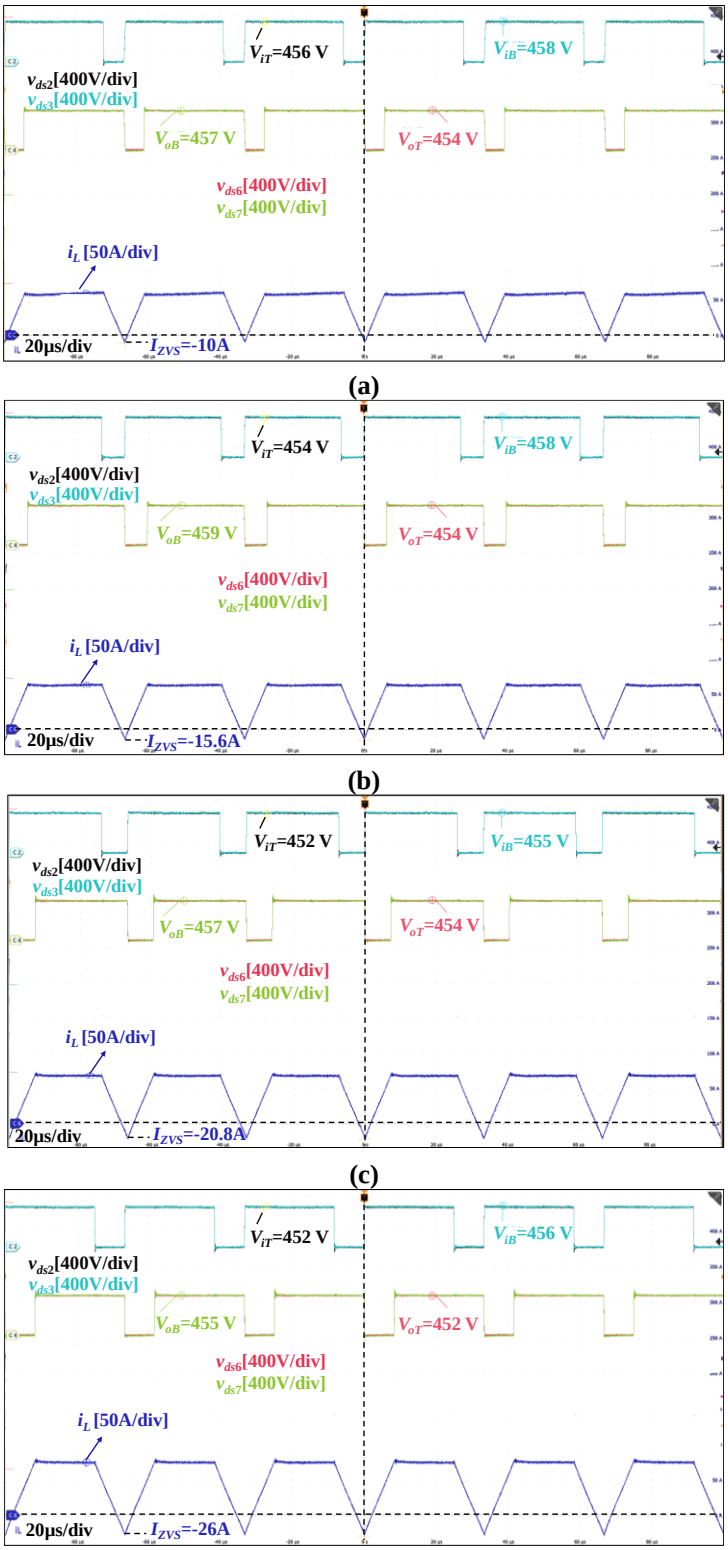


Fig. 4-56. Experimental results with different "ZVS factor" *k* under V_{out}=900 V, *P*=45 kW, t_d=600 ns: (a) *k*=0.2, (b) *k*=0.3, (c) *k*=0.4 (d) *k*=0.5. The circuit parameters are listed in Table 4-9.

4) Thermal Performance and Efficiency

Fig. 4-57 shows the thermal result of coupled inductors. Benefits from 15 oz heavy copper PCB technique, the hot spot temperature is 47.1 ºC under 50 kW, 1 kV output voltage. More details about this heavy copper coupled inductor design and core loss measurement can be found in [28]. With the consideration of auxiliary losses such as gate driving losses, controller losses, and cooling fans losses, the conversion efficiency of the proposed 3-L buck-boost converter and 2-L FSBB are both shown in **Fig. 4-58**. The peak efficiency of the 3-L buck-boost converter is 98.9% and occurs at full load unit gain case (V_{out}=900 V). Compared with the 3-L buck-boost, 2-L FSBB with the same setup has a slightly higher efficiency because only the top half circuit was used, as shown in **Fig. 4-58(b)**. Theoretically, 2-L FSBB and 3-L buck-boost should have similar efficiency because half voltage rating SiC MOSFETs can be selected on 3-L buck-boost topology. More discussion on the difference between 3-L buck-boost and 2-L FSBB will be explained in the next part.

In addition, the loss breakdown of the proposed 3-L buck-boost converter at 50 kW is plotted in **Fig. 4-59**. Among step-up, step-down, and unit-gain cases, the unit-gain case has the lowest peak current because of a flat trapezoidal current waveform.



Fig. 4-57. Thermal testing results for the planar coupled inductor under 50 kW step-up case (900 V to 1 kV).

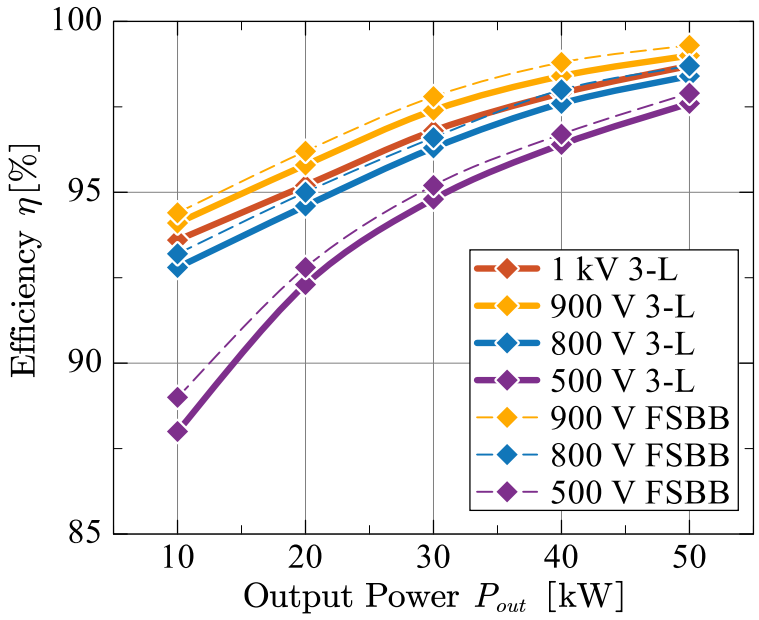


Fig. 4-58. The efficiency of the 3-L buck-boost converter and 2-L FSBB with different output voltage. The 2-L FSBB cannot run at 1 kV because the SiC MOSFETs rating is only 1.2 kV.

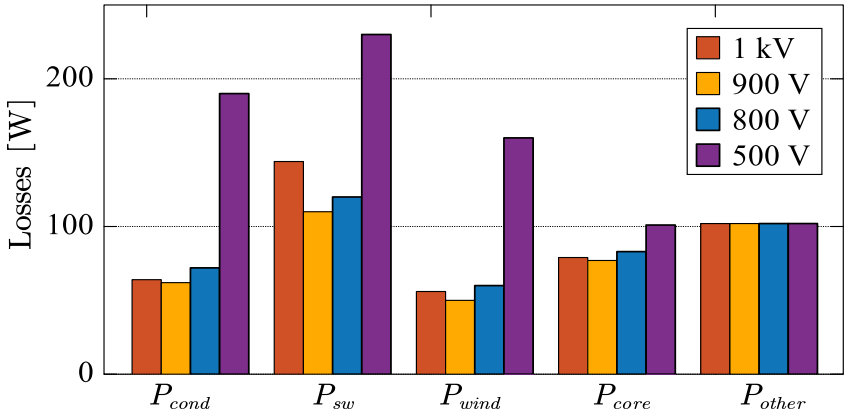


Fig. 4-59. Loss breakdown of the 3-L buck-boost converter at 50 kw with different output voltages. The calculation was based on the parameters in Table 4-9.

Table 4-10 COMPARISON OF PROPOSED 3-L BUCK-BOOST CONVERTER AND 2-L FSBB

Variable	3-L buck-boost	2-L FSBB
Switch voltage stress (P.U.)	0.5	1
Switch current stress (P.U.)	1	1
Switch number	8	4
Capacitor voltage stress (P.U.)	0.5	1
Capacitor Value (P.U.)	2	1
Inductor voltage stress (P.U.)	1	1
Inductor voltage stress (P.U.)	1	1
Gate driver number	8	4
Mid-points balance control	Yes	No
CM noise	Small	Large

5) Comparison of the 3-L buck-boost converter and 2-L FSBB

The comparison between the proposed 3-L buck-boost converter and the traditional 2-L FSBB converter is listed in **Table 4-10**. It should be noted that except for the switch number and gate driver number, other variables have been normalized based on 2-L FSBB. For example, if the conventional 2-L FSBB has 1 per unit (P.U.) voltage stress on each switch, the proposed 3-L buck-boost converter only has 0.5 P.U. Based on Table IV, the loss comparison can be explained as:

1. Switching loss: considering the switch number, switch voltage, and current stress, the total switching loss of these two topologies should be very similar with the same inductor current waveform i_L.

2. Conduction loss: with the assumption that a double voltage rating semiconductor will have double $R_{ds(on)}$, the total conduction loss will be similar.

3. Inductor loss: due to the same voltage and current stress on the inductor, the conduction loss and core loss of the inductor should be very similar between these two topologies. In addition to the loss comparison, with up to 25 dB CM noise, the CM filter for the proposed 3-L buck-boost converter will be smaller than traditional FSBB.

It should be noted that this paper focuses on CM noise reduction. Thus, the 2-L FSBB in this paper is only for the purpose of CM noise comparison. With a 1.2 kV SiC module, the output voltage of 2-L FSBB can be pushed up to 900 V. However, the required maximum V_{out} is 1 kV, which means 2-L FSBB cannot meet this requirement. If 2-L FSBB was selected, 1.7 kV SiC modules should be adopted to meet 1 kV V_{out}. However, the availability of 1.7 kV SiC modules is a concern when more than 1.2 kV commercial SiC modules exist from multiple vendors in the market. Therefore, there is a tradeoff between semiconductor availability and converter complexity.

4.4 Capacitor Voltage Auto-Balance with Mid-points Interconnection

As explained in the last section, a four-switch buck-boost (FSBB) converter with quadrangle control is a good candidate for non-isolated dc-dc power conversion applications due to its feature of soft-switching, bidirectional power flow and capability of voltage step-up and step-down. However, the 2-level FSBB exhibits a high degree of CM emissions. To down-size the required EMI filter, a 3-level buck-boost converter is proposed in this letter based on the symmetry principle [9]. As shown in **Fig. 4-60(a)**, the proposed circuit resembles a mirrored FSBB converter with a conventional FSBB converter on the top and its mirror on the bottom. With synchronized switching actions on each mirrored switching pair, S_1, and S4, as an example, the circuit can ideally present zero CM emission. However, due to real-world errors such as gating delay, switching transient mismatch, and unbalanced DC-link voltages, CM emissions persist.

As shown in the dashed line in **Fig. 4-60(a)**, the proposed topology has the option to bridge the input and output midpoints. This letter intends to address two interesting impacts after bridging the two midpoints. First, a part of CM noise is trapped inside the converter, and smaller CM emissions can be measured from the outside, potentially leading to a much smaller EMI filter. Second, in addition to the bridged midpoints, a coupled buck-boost inductor is used, as shown in **Fig. 4-60(a)**. The coupled inductor operates as a "transformer" and clamps the split DC-link voltages on both input and output sides, meaning the converter features automatic capacitor voltage balancing.

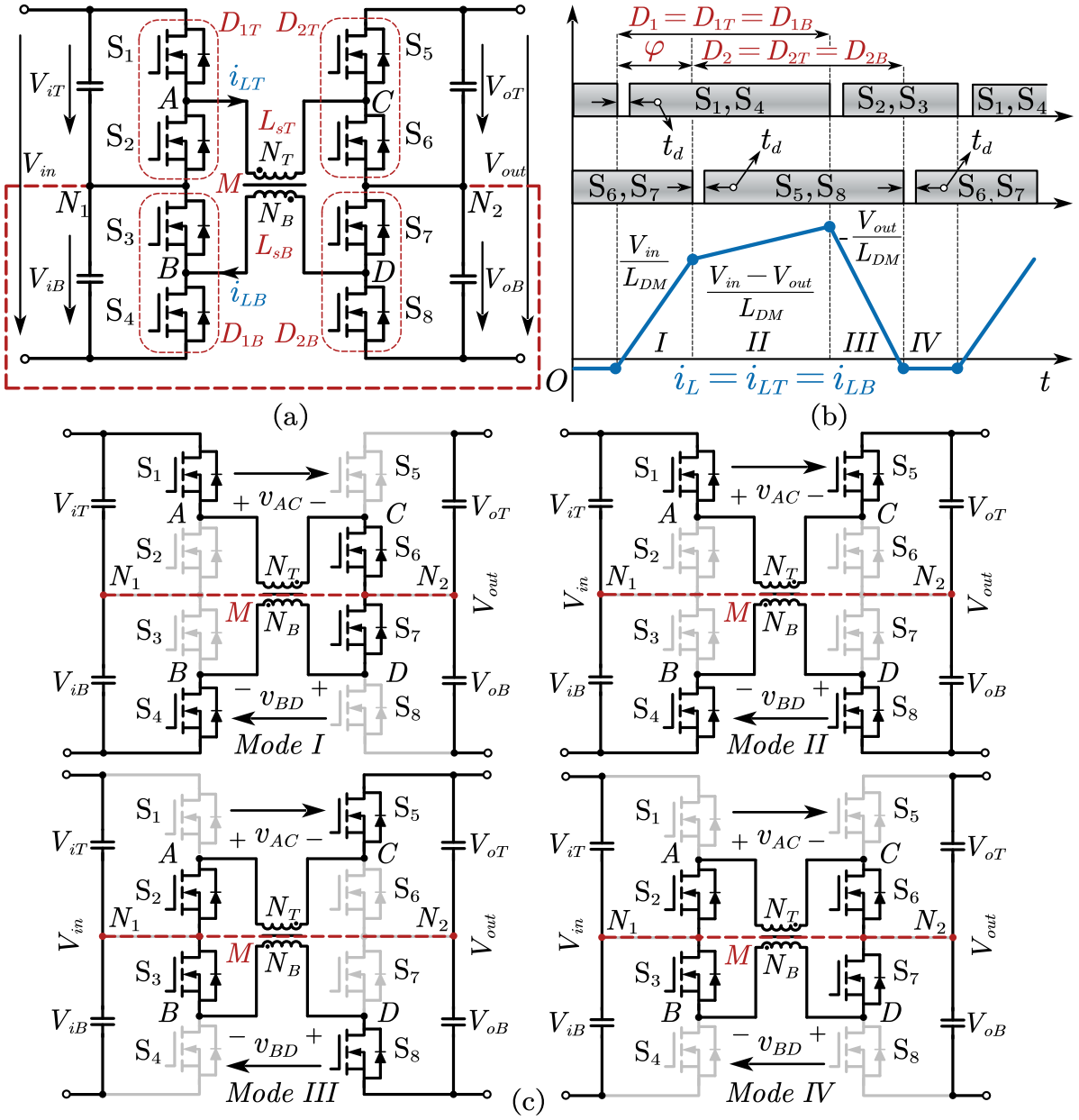


Fig. 4-60. Proposed 3-L buck-boost converter and its operating principle (a) circuit diagram, (b) driving signals and i_L waveforms with quadrangle modulation, (c) four operating modes.

4.4.1 Circuit Operation Principle

The circuit diagram of the 3-L buck-boost converter is shown in **Fig. 4-60(a)**. It consists of an FSBB converter on the top and its mirror on the bottom, with a coupled buck-boost inductor between them. The quadrangle current modulation [67] is adopted for both FSBB converters.

According to the symmetry principle, the modulation for the two converters needs to be "synchronized" to reduce the CM emission where a mirrored pair of switches share the same gating commands, S_1 equal to S_4 as an example. Accordingly, four circuit modes *I-IV* are depicted in **Fig. 4-60(c)**. Typical gating signals and inductor current i_L are shown in **Fig. 4-60(b),** where duty ratio D_1, D_2, and phase-shift φ are denoted as the key control variables in the quadrangle modulation to help achieve zero-voltage switching (ZVS) and minimized inductor current RMS value [11]. According to the volt-second balance of the buck-boost inductor, the relationship between D_1 and D_2 is given as Eq. (4.43), where V_{in} and V_{out} are the input and output voltages. In **Fig. 4-60(a)**, N_1 and N_2 are the two midpoints on the input and output side. Ideally, the two midpoints share the same voltage potential.

$$V_{out}/V_{in} = D_1/D_2 \tag{4.43}$$

4.4.2 Midpoints Bridging Impact on CM Emissions

The CM cancellation discussed above will, however, be compromised in real applications due to any reason that can cause asynchronous operation of the top and bottom FSBB converters, like gating delay, switching transient mismatch, or unbalanced DC-link voltages. Circuit modeling is done in this section, showing that by bridging the two mid-points, the CM emission caused by non-ideal factors can be largely trapped inside the converter.

Fig. 4-61 derives the decoupled CM and differential mode (DM) equivalent circuits for the proposed 3-L buck-boost converter. Four half bridges (S_1, S_2), (S_3, S_4), (S_5, S_6), and (S_7, S_8) in **Fig. 4-60(a)** are replaced by four voltage sources v_{AN1}, v_{BN1}, v_{CN2}, v_{DN2} which can be decoupled into CM components $v_{N1,CM}$ and $v_{N2,CM}$, and DM components $v_{i,DM}$ (i=*A*,*B*,*C* or *D*).

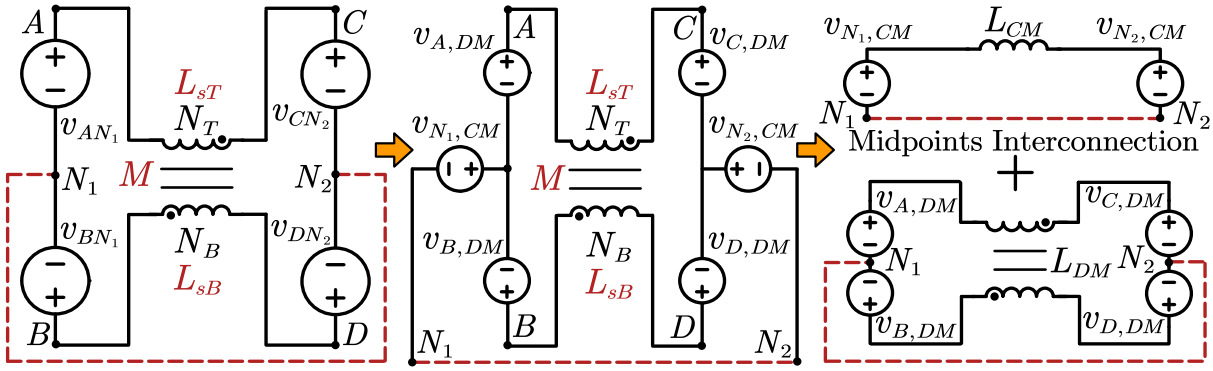


Fig. 4-61. CM and DM equivalent circuits. The original circuit diagram can be found in Fig. 4-60.

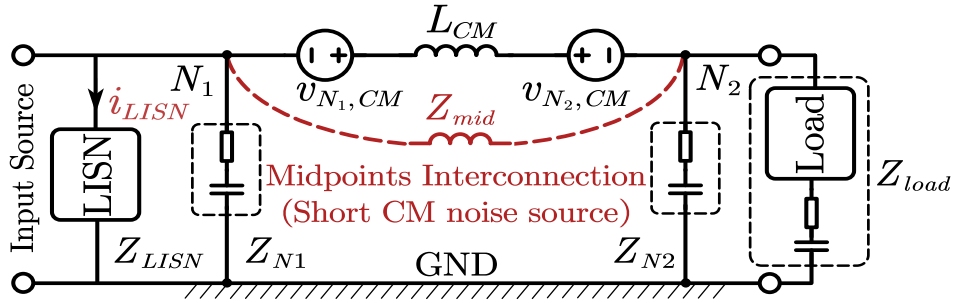


Fig. 4-62. CM lump model with parasitics, LISN, and load. The simplified circuit without the consideration of parasitic parameters is shown in Fig. 4-61.

$$\begin{cases} v_{AN_1} = \mathrm{S}_1 \cdot V_{iT},\ v_{BN1} = -\mathrm{S}_4 \cdot V_{iB}\ \ (\mathrm{S}_1 = \mathrm{S}_4 = 0 \text{ or } 1) \\ v_{CN_2} = \mathrm{S}_5 \cdot V_{oT},\ v_{DN1} = -\mathrm{S}_8 \cdot V_{oB}\ \ (\mathrm{S}_5 = \mathrm{S}_8 = 0 \text{ or } 1) \end{cases} \tag{4.44}$$

$$\begin{cases} v_{N_1,CM} = 0.5\,(v_{AN_1} + v_{BN_1}) = 0 \\ v_{N_2,CM} = 0.5\,(v_{CN_2} + v_{DN_2}) = 0 \end{cases} \tag{4.45}$$

$$\begin{cases} v_{A,DM} = v_{AN_1} - v_{N_1,CM},\ v_{B,DM} = v_{BN_1} - v_{N_1,CM} \\ v_{C,DM} = v_{CN_2} - v_{N_2,CM},\ v_{D,DM} = v_{DN_2} - v_{N_2,CM} \end{cases} \tag{4.46}$$

Fig. 4-62 illustrates a simplified lump model showing the CM noise propagation path with parasitic, line impedance stabilization network (LISN), and load included. Due to the discussed non-ideal factors, the total CM noise source, $V_{N2,CM}$ - $V_{N1,CM}$, cannot be fully canceled, and CM noise persists

on the LISN side. Take **Fig. 4-62** as an example; without mid-point interconnection, the current through LISN i_{LISN} can be derived as

$$i_{LISN} = \frac{V_{N2,CM} - V_{N1,CM}}{L_{CM} + Z_{eq}} \cdot \frac{Z_{N1}}{Z_{LISN} + Z_{N1}} \tag{4.47}$$

Where equivalent impedance Z_{eq} can be expressed as

$$Z_{eq} = \frac{Z_{LISN} \cdot Z_{N1}}{Z_{LISN} + Z_{N1}} + \frac{Z_{load} \cdot Z_{N2}}{Z_{load} + Z_{N2}} \tag{4.48}$$

Where Z_{LISN} is the impedance from LISN to ground, Z_{N1} and Z_{N2} are both parasitic impedances from points N_1 or N_2 to ground, and Z_{load} is the impedance from load to ground.

However, the proposed circuit remains the option to electrically bridge the two mid-points, N_1 and N_2, as shown in the dashed line in **Fig. 4-60** and **Fig. 4-61**. As a result, a low-impedance path Z_{mid} can be created in parallel with the LISN path, as shown in **Fig. 4-62**. It traps the noise inside the converter and effectively directs the emission away from the LISN branch, where the level of electromagnetic emission is standardized. As shown in **Fig. 4-62**, after bridging two mid-points, N_1 and N_2, with a low impedance path Z_{mid}, the current i_{LISN} through LISN should be revised as

$$i_{LISN} = \frac{V_{N2,CM} - V_{N1,CM}}{L_{CM} + \frac{Z_{eq} \cdot Z_{mid}}{Z_{eq} + Z_{mid}}} \cdot \frac{Z_{mid}}{Z_{eq} + Z_{mid}} \cdot \frac{Z_{N1}}{Z_{LISN} + Z_{N1}} \tag{4.49}$$

From Eq. (4.49), if Z_{mid} is very small, the CM current through LISN i_{LISN} will be trapped by this mid-point interconnection.

4.4.3 Midpoints Bridging Impact on Voltage Balance

This part discusses how the switching asymmetry compromises the noise cancellation feature. In addition, it meanwhile unbalances the top and bottom DC-link voltages. A typical technique to address the balance issue is to introduce controlled DC-link capacitor charging and discharging currents by using small duty ratio modifications [6]. Yet this approach inevitably leads to severe switching mismatch with a timescale of hundreds of nanoseconds. It significantly deteriorates the CM emission where the frequency of interest is in the range from hundreds of kilohertz to tens of megahertz [6]. As discussed above, bridging the two midpoints is beneficial for CM noise mitigation. This section aims to demonstrate its further benefit in achieving automatic voltage balancing for split DC-link capacitors.

After bridging mid-points N_1 and N_2, the detailed equivalent circuit is depicted in **Fig. 4-63(a)** with leakage inductances L_{kT}, L_{kB} included. k_T and k_B are defined as the coupling coefficients of the top and bottom side windings. Based on coupled inductor definition, terminal voltages v_{AC} and v_{DB} are given in Eq. (4.50).

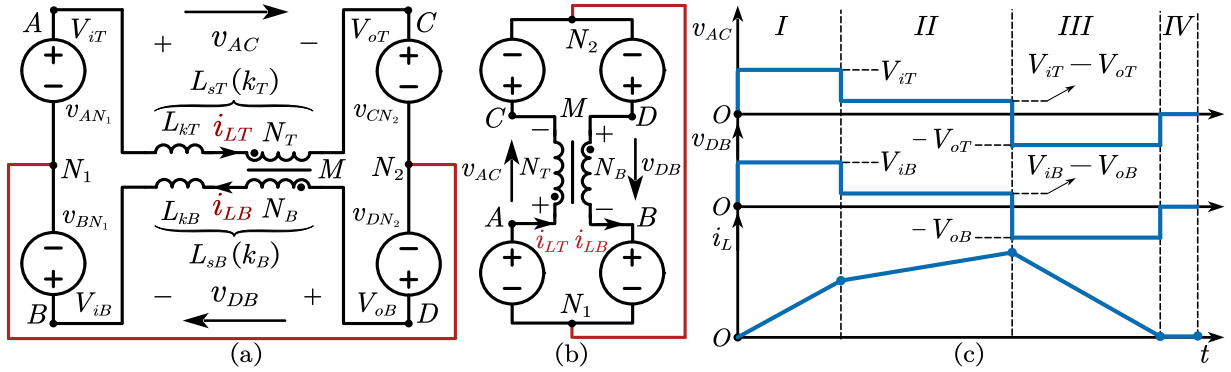


Fig. 4-63. Automatic dc-link voltage balance with input-output mid-points connected: (a) equivalent circuit with the consideration of leakage inductance, (b) equivalent circuit with perfect coupling, (c) terminal voltages v_{AC}, v_{BD} and buck-boost inductor current waveforms.

$$\begin{cases} L_{sT} \cdot di_{LT}/dt + M \cdot di_{LB}/dt = v_{AC} \\ L_{sB} \cdot di_{LB}/dt + M \cdot di_{LT}/dt = v_{DB} \end{cases} \tag{4.50}$$

Where L_{sT}, and L_{sB} are the self-inductances and M is the mutual inductance. If the coupled inductor has a perfect coupling for the top and bottom windings ($k_T = k_B = 1$), leakage inductance L_{kT} and L_{kB} can be ignored, and a simplified circuit is shown in **Fig. 4-63(b)**. With a perfect coupling, L_{sT}, L_{sB}, and M can be given as

$$L_{sT} = {N_T}^2 \cdot L,\ L_{sB} = {N_B}^2 \cdot L,\ M = N_T \cdot N_B \cdot L \tag{4.51}$$

From Eq. (4.50) and Eq. (4.51), the relationship between v_{AC} and v_{DB} can be given as

$$v_{AC}/v_{DB} = N_T/N_B \quad (\text{if } k_T = k_B = 1) \tag{4.52}$$

According to Eq. (4.51), interestingly the coupled inductor operates as a 'transformer' which clamps the ratio between the two terminal voltages v_{AC} and v_{DB} based on winding turn-ratio N_T: N_B. In one switching period, the converter migrates from *Mode I* to *IV* sequentially. *Mode I* to *IV* are defined in **Fig. 4-60(c)**. Meanwhile, the value of $v_{AC(DC)}$ is sequentially equal to $V_{iT(B)}$, $V_{iT(B)}$-$V_{oT(B)}$, $V_{oT(B)}$, 0, as shown in **Fig. 4-63(c)**. v_{AC} and v_{DB} satisfy the relationship in Eq. (4.51) in each mode as given in. As a result, under the assumption of perfect coupling, the input and output split dc-link capacitor voltages are clamped according to the winding turn ratio as given by Eq. (4.52), meaning that the mid-point voltages can be controlled by adjusting the turn ratio of the transformer-like coupled inductor. For instance, DC-link capacitor voltages can be automatically balanced ($V_{iT} = V_{iB}$, $V_{oT} = V_{oB}$) by using a unity turn ratio ($N_T = N_B$) without closed-loop voltage balancing control. Moreover, when the turns ratio is not 1, the ratio $V_{i(o)T}/V_{i(o)B}$ can be controlled asymmetrically by adjusting N_T/N_B as in Eq. (4.52).

$$V_{iT}/V_{iB} = V_{oT}/V_{oB} = N_T/N_B \quad (\text{if } k_T = k_B = 1) \tag{4.53}$$

In weak coupling cases where L_{kT} and L_{kB} are not negligible, As shown in **Fig. 4-63(a)**, the relationship in Eq. (4.53) can be generalized as in Eq. (4.54). To achieve the dc-link voltage auto-balance, two design criteria should be met for the coupled inductor design as listed below:

1. Unity turns ratio ($N_T = N_B$).

2. Strong coupling of input and output winding (coupling coefficients k_T and k_B are close to 1).

$$\frac{V_{iT}}{V_{iB}} = \frac{V_{oT}}{V_{oB}} = \frac{N_T}{N_B} \cdot \frac{2M + \frac{N_T}{N_B} \cdot L_{kT}}{2M + \frac{N_B}{N_T} \cdot L_{kB}} \quad \left(\text{assume } \frac{di_{LT}}{di_{LB}} = \frac{N_T}{N_B}\right) \tag{4.54}$$

4.4.4 Experimental Validation

As shown in **Fig. 4-64(a)**, a SiC-based 50 kW 3-L buck-boost converter was built to verify the midpoints bridging impacts on CM emission and capacitor voltage balancing. The specifications of the converter are listed in **Table 4-11**. The input voltage V_{in} is 900 V while the output voltage ranges from 500 V to 1 kV. The measurement setup for the 3-L buck-boost converter is shown in **Fig. 4-64(b)**. Meanwhile, the designed prototype is configured as a conventional 2-L FSBB, as shown in **Fig. 4-64(c)**, to compare the CM emissions. In **Fig. 4-64(b)** and **(c)**, current transformers (CT) are used to measure the CM current.

Based on the previous discussion, non-ideal factors will cause unbalanced DC-link voltage if the two midpoints are not bridged. As shown in **Fig. 4-65(a)**, without active balance control, neither input nor output side voltages are balanced with 1 kV output voltage and 50 kW output power. With an active balance control, as shown in **Fig. 4-65(b)**, both sides have balanced dc-link voltage. Also, the quadrangle modulation ensures a minimum rms current and ZVS on all switches.

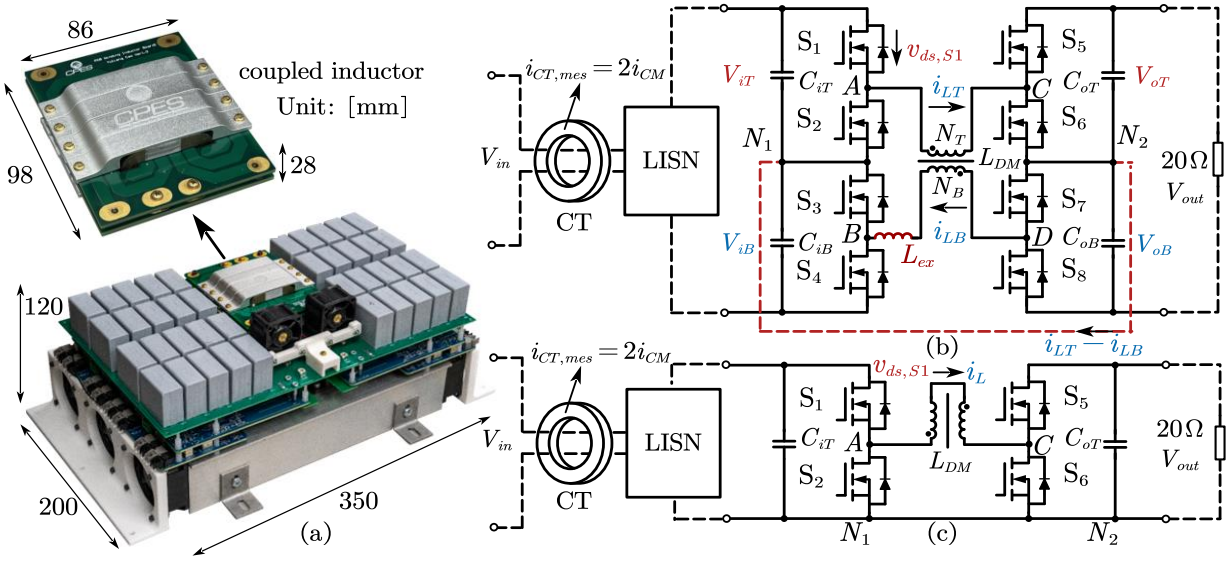


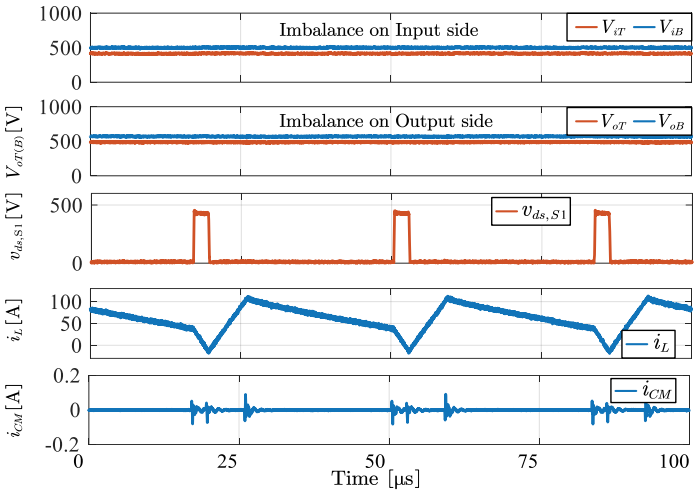
Fig. 4-64. SiC-based converter prototype and its measurement setups: (a) 50 kW prototype, (b) test setup for proposed 3-L buck-boost converter, (c) test setup for conventional 2-L FSBB.

Table 4-11 SPECIFICATIONS OF THE PROPOSED 3-L BUCK-BOOST CONVERTER

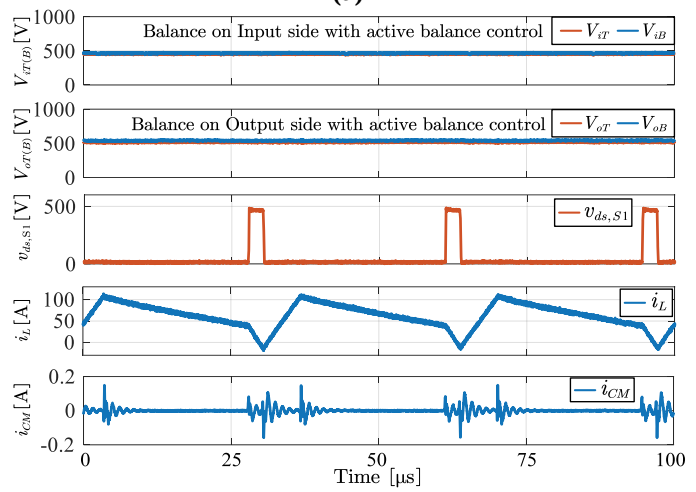
Parameter	Value	Parameter	Value
Input voltage V_{in}	900 V	Rating power P	50 kW
Output voltage V_{out}	500 V to 1 kV	Switching frequency f_s	30 kHz
Mutual inductance M	12.5 μH	Leakage inductor L_{kT}, L_{kB}	120/108 nH
Turns ratio N_T:N_B	7:7 or 7:8 or 8:7	External leakage inductor L_{ex}	0/2.5/ 3.6/5.8μH

In comparison, with bridged midpoints and unity-coupled inductor turn-ratio, the DC-link voltage can be automatically balanced. Test results in **Fig. 4-65(c)** validate the analysis. With a turns ratio of N_T: N_B=7:7 and negligible leakage inductance, DC-link voltages are automatically balanced without any active balance control under the same operating condition of 1 kV output voltage and 50 kW power.

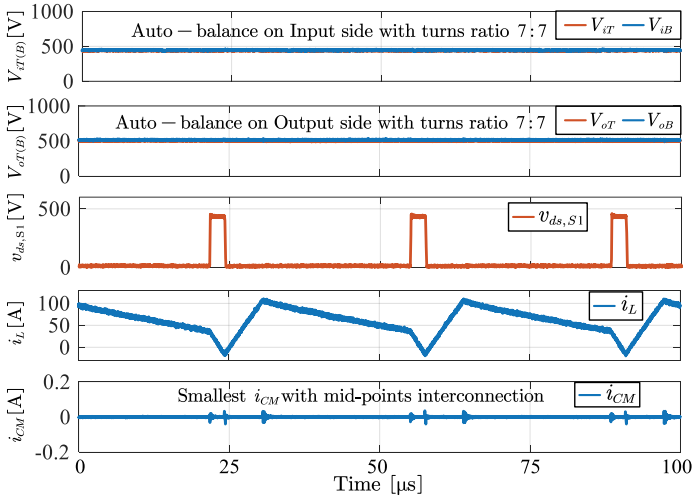
In addition, to verify the impacts from the coupled inductor turn-ratio, **Fig. 4-66(a)** and **(b)** demonstrate the results with turn-ratio of N_T: N_B=7:8 and 8:7. It can be found in both cases, input and output voltage ratios V_{iT}/V_{iB} and V_{oT}/V_{oB} will follow the turn-ratio of the coupled inductor as in Eq. (4.53).



(a)



(b)



(c)

Fig. 4-65. Experimental results under V_{out}= 1 kV P=50 kW (a) without midpoint connection and without balance control, (b) without midpoint connection and with balance control, (c) with midpoint connection and natural voltage balance. The circuit parameters are listed in Table 4-11.

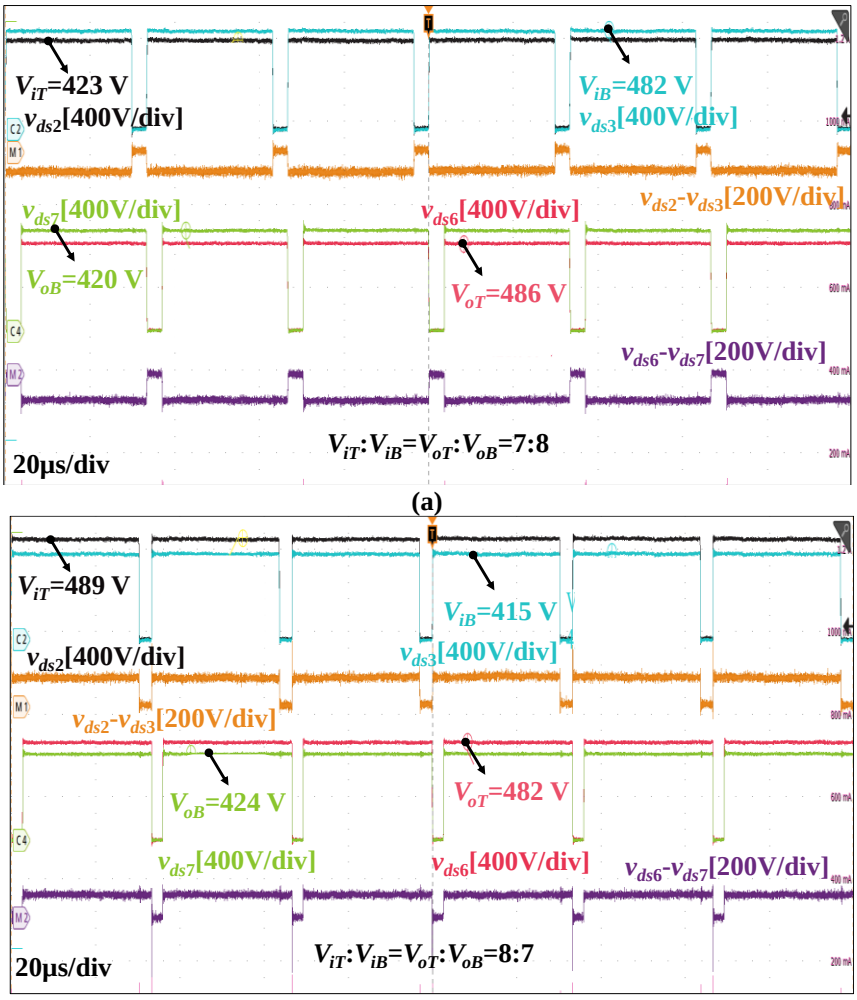


Fig. 4-66. Experimental results with bridged midpoints under V_{out}=900 V P=45 kW: (a) N_T: N_B=7:8, (b) N_T: N_B=8:7. The circuit parameters are listed in Table 4-11.

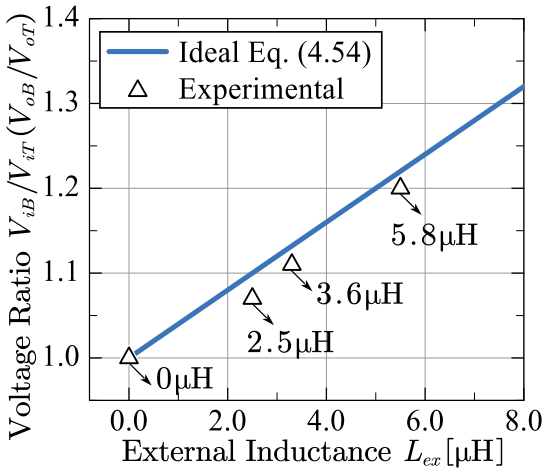


Fig. 4-67. Leakage inductance impact on midpoint voltage balance. The circuit parameters are listed in Table 4-11.

In order to verify the leakage inductance impact, an external inductor L_{ex} was added in series with the bottom windings, as shown in **Fig. 4-64(b)**. With the unity turns ratio of N_T: N_B=7:7, to validate Eq. (4.54) under different leakage inductance, tests are performed with different leakage inductance of 0 μH, 2.5 μH, 3.6 μH or 5.8 μH. **Fig. 4-67** shows both the theoretical and experimental input-output voltage ratio $V_{i(o)T}/V_{i(o)B}$ with different L_{ex} (0/2.5/3.6/5.8μH). The experimental results agree with the theoretical results calculated according to Eq. (4.54), effectively validating the impact of the leakage inductance.

Fig. 4-68 plots the measured CM current results under 900 V output in the frequency range from 150 kHz to 30 MHz. The results of the conventional 2-L FSBB (**Fig. 4-64(c)**) and proposed 3-L buck-boost converter (**Fig. 4-64(b)**) with and without midpoints interconnection are all depicted together. Due to the circuit asymmetry, conventional 2-L FSBB has the highest CM noise. Compared with no midpoint interconnection, the CM noise can be reduced by up to 30 dB after connecting N_1 and N_2, which can verify that this interconnection can bring benefits for CM noise suppression. Moreover, this 3-L buck-boost converter with the midpoint's interconnection can largely meet the standard DO-160 without any CM filter. Furthermore, the benefits brought by the bridged mid-points and coupled inductor structure are also applicable to 3-L buck or boost converters, as shown in **Fig. 4-69**, where the mitigated CM emission and automatic DC-link voltage balance are expected.

4.5 Conclusion

In this chapter, two DCX applications are implemented: one is an 18 kW 98.8% peak efficiency battery charger with partial power processing, and the other is a 50 kW symmetric 3-L buck-boost converter with coupled inductor and common-mode (CM) noise suppression. With partial power

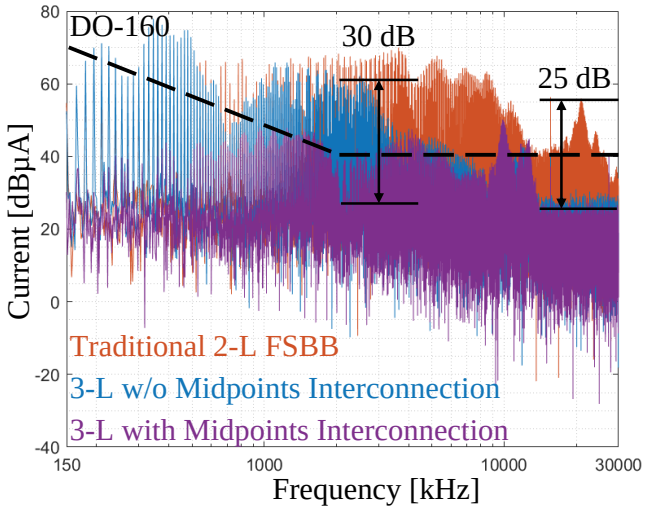


Fig. 4-68. CM noise measurement results under V_{out}=900 V 45.5 kW. The circuit parameters are listed in Table 4-11.

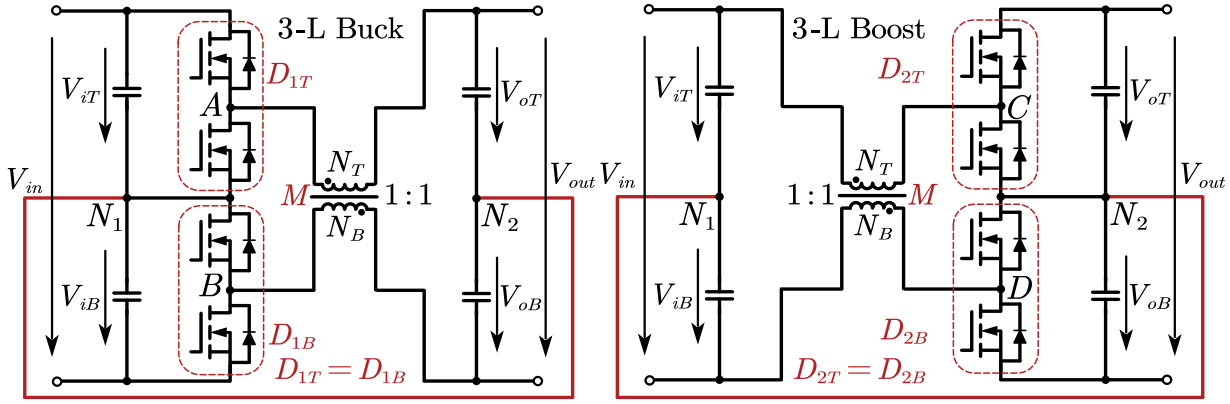


Fig. 4-69. Extended midpoint interconnection topologies: symmetric 3-L buck or boost converter with coupled inductor.

processing, main power will be handled by DCX with very high efficiency. To regulate the output voltage, the remaining small portion of power will be processed by a post-regulator. Besides partial power converters, DCX is also widely used in typical two-stage DC-DC converters. In order to accommodate different DC buses, the output regulation is handled by a rear-end DC-DC converter. For CM noise suppression, a symmetric 3-L buck–boost converter is proposed. By bridging the input and output midpoints, the noise is trapped inside the power. Also, a combination of bridged midpoints and coupled buck-boost inductors grants the converter a desirable DC-link capacitor voltage auto-balance feature.

Chapter 5

Conclusions and Future Work

In this chapter, the contributions of this research and future work are discussed.

5.1 Contributions

This work mainly focuses on soft-switching DC transformer (DCX) topology, control, and application. The main contributions of this work are:

1. A switching transition analysis and optimization for resonant CLLC-DCX is proposed, which can realize no deadtime loss, small current ringing, and load-independent voltage gain. With the same set of specifications, the efficiency can be improved by 0.4% after optimization.

2. To overcome the limitations of high-power and high-frequency transformer designs in traditional LLC/CLLC-DCX, the concept of the electronic-embedded transformer (EET) is proposed as a solution. Building upon this concept, the EET-DCX is proposed to address the transformer-level paralleling issue encountered in traditional LLC-DCX systems.

3. A novel trapezoidal current modulation technique for EET-DCX is also proposed, which offers significant advantages, such as a considerable reduction in rms current while preserving key features like natural current sharing, load-independent voltage gain, and full-load range ZVS. When compared to state-of-the-art LLC/CLLC-DCX topologies, the proposed approach can achieve up to a 23% reduction in total conduction loss.

4. A simplified topology resonant commutation (RC) EET-DCX is proposed. Compared to typical EET-DCX, the full bridge was replaced by only one bidirectional switch, and thus, the semiconductor number was reduced by half.

5. Two hybrid EET-based DCXs are proposed to reduce the voltage stress on integrated full bridge or bidirectional AC switch. Including EET-DCX and RC EET-DCX, these four DCX topologies consist of a new family of soft-switching DCXs.

6. Two practical DCX applications are implemented with good performance. One is an 18 kW 500 kHz 98.8% peak efficiency battery charger; the other is a 50-kW symmetric 3-L buck-boost converter with a coupled inductor and CM noise suppression.

5.2 Future Work

1. For CLLC-DCX switching transition optimization, the parasitic output capacitance is assumed to be constant and equal to its time-related value. However, when ZVS occurs, the voltage across the switch is variable. Thus, more studies on this topic can be done in the future.

2. For EET-DCX, the magnetizing inductance is replaced by two external inductors for the modular design. The impact of air gap and magnetizing inductance can be explored more.

3. So far, the control signals and auxiliary power for EET are provided externally. The self-sustained EET can be implemented in the future.

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