

A Study of a Versatile Low Power CMOS Pulse Generator for Ultra Wideband Radios

Kevin M. Marsden

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Dr. Dong S. Ha, Chairman

Dr. J. R. Armstrong

Dr. Sanjay Raman

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Kevin Marsden

Dr. Dong S. Ha, Chairman

Bradley Department of Electrical and Computer Engineering

(ABSTRACT)

Ultra-Wideband (UWB) technologies are at the forefront of wireless communications, offering the possibility to provide extremely high data rate wireless solutions. In addition to high data rate applications, UWB technologies also offer an extremely low cost alternative for many low data rate systems. In this thesis, we describe the design of a CMOS pulse generator for impulse based UWB systems. The structure of our pulse generator is based on the topology of a single tap CMOS power amplifier. By increasing the number of taps on a CMOS power amplifier, it is possible to generate sub-nanosecond pulses with a desired shape. A power saving scheme that significantly reduces the power consumed at low data rates is also described. The versatility of our design lies in the ability to support dynamically varying output power levels and center frequencies. Our pulse generator design is extended to a rectified cosine generator, necessary for a multiband approach. The performance of our pulse generators is estimated through simulation with a target technology of TSMC 0.18 μm CMOS at a supply voltage of 1.8 V. The simulation results indicate that our pulse generator produces high fidelity Gaussian monocycle pulses with a pulse width of approximately 160 ps and a peak output power of more than 10 mW. We believe that our design of a CMOS pulse generator for UWB systems is a feasible option for many applications in which power and cost are most important.

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Chapter 1

Introduction

As the wireless revolution continues to gain momentum we witness an increasing drive to replace wired connections with wireless technology. Existing wireless local area network (WLAN) technologies can only support data rates of up to 54 Mbps, excluding high data rate applications such as HDTV. Ultra-Wideband (UWB) technology has been around for over a century and has recently been given a rebirth. UWB technology pushes the limits of high data rate communications, enabling wireless devices to be realized that were never thought possible.

Gerald Ross, a researcher with the Sperry Rand Corporation, first introduced UWB technology in the late 1960's. The first U.S. patent for UWB communications was granted in 1973 to Ross and the Sperry Rand Corporation [1]. The technology was first used in a ground penetrating radar system in 1974, and became a success at Geophysical Survey Systems, Inc. (GSSI). In the US, the Department of Defense began to use the technology to image through walls and into the ground [2]. In 1998, the FCC realized the potential of UWB technology and began to investigate the possibility of allowing commercial use and the necessary regulations. Research and development of UWB systems has exploded since the FCC's allocation of a spectrum for UWB communication on February 14, 2002. Compared to other traditional narrowband communication systems, UWB has several advantages such as high data rate, low radiated power, excellent immunity to multipaths, and simple hardware. Many of these potential advantages are directly related to the large bandwidth of a UWB device [3], [4].

Since the bandwidth of UWB is so large, it poses many challenges for a CMOS implementation of a UWB system. The challenge stems from the fact that UWB uses extremely narrow pulses to transmit data. The pulse width at the output of an impulse UWB system is generally on the order of one to a few hundred picoseconds. To generate such a narrow pulse, existing UWB radios rely on silicon germanium (SiGe) technology due to its high frequency capabilities over CMOS technology.

In this thesis, we investigate the feasibility of a versatile CMOS pulse generator that is capable of generating very narrow pulses for an impulse-based UWB system. The pulse generator should be also adaptable, as we want to extend the impulse-based design to construct a rectified cosine generator, necessary to support a multiband method considered by an alliance of companies. The major goal of this research is to develop a pulse generator that is versatile, adjusting to various modulation schemes dynamically, and efficient in terms of power, area and complexity.

The thesis is organized as follows. In Chapter 2, we describe the necessary background information and terms required to understand the development of both generators. Then, in Chapter 3, we discuss the design of the impulse-based pulse generator and describe a power saving scheme that significantly reduces the power consumption. The extendibility of this type of pulse generation is shown in Chapter 4 as we describe how the design is modified into a rectified cosine generator for a multi-band transmitter. Simulation results of both designs are discussed in Chapter 5. Lastly, in Chapter 6, we discuss conclusions drawn from our generator designs.

Chapter 2

Preliminaries

In this chapter, we describe an overview of UWB that including terms, types of UWB pulse, and pulse generators. The concepts discussed are necessary to understand the design of our pulse generator.

2.1 Overview of UWB

2.1.1 Definition of UWB and FCC Regulations

It was not until February 14, 2002 when UWB technology gained great momentum as the FCC allocated a 7.5 GHz band for indoor wireless communications. The FCC has defined a UWB device as having a -10 dB bandwidth between 3.1 and 10.6 GHz, while meeting the indoor spectrum mask that is shown in Figure 2.1 and occupying a bandwidth of at least 500 MHz or more than 20% of the center frequency [5], [6].

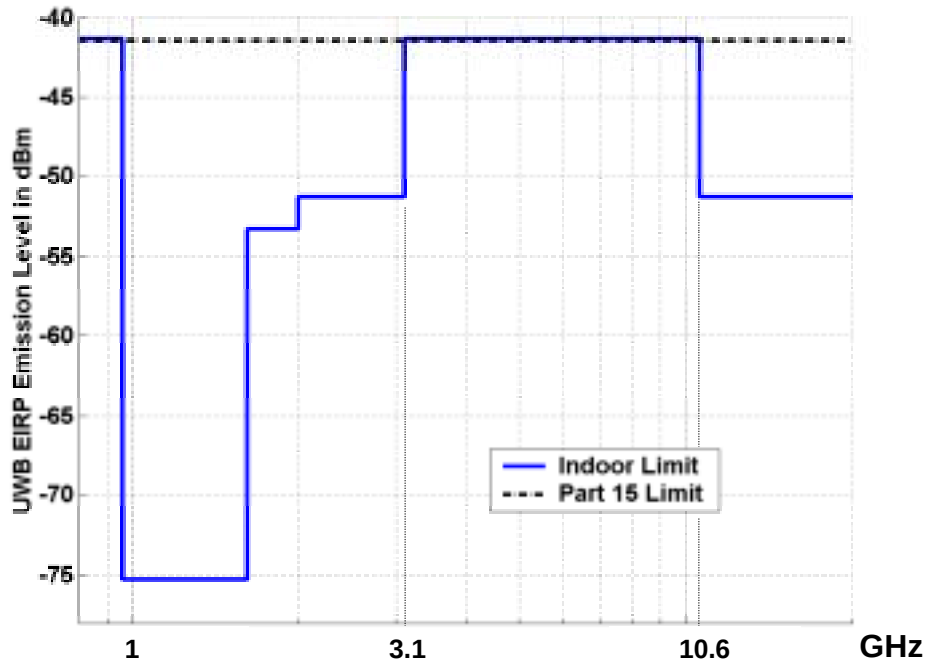


Figure 2.1: UWB indoor spectrum mask

The spectrum mask shown in Figure 2.1 requires that the energy emitted from a UWB device not exceed -41.25 dBm/MHz. The mask shown in Figure 2.2 is for the UWB outdoor spectrum [6].

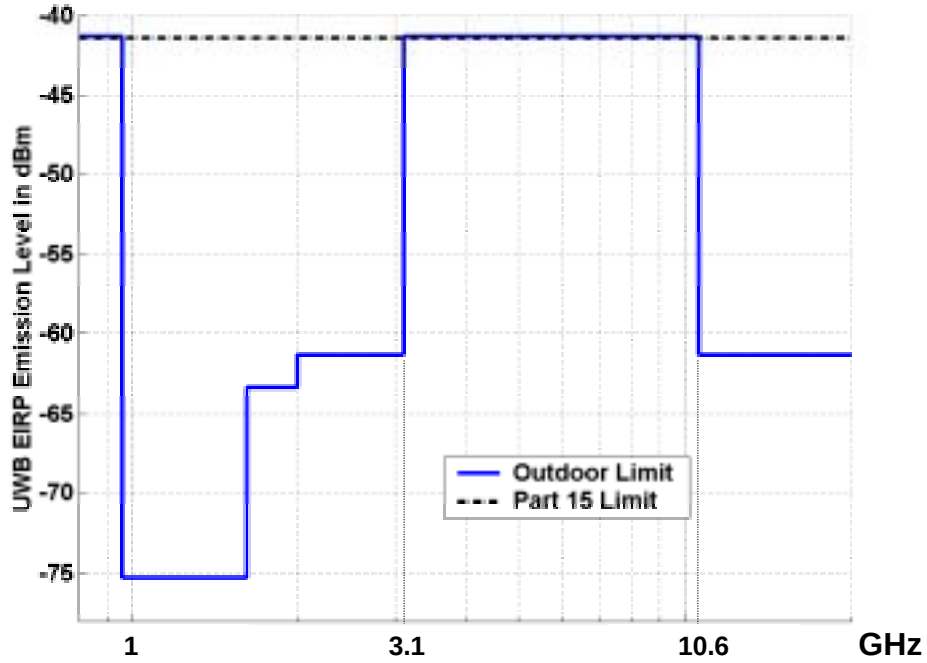


Figure 2.2: UWB outdoor spectrum mask

The differences between the indoor and outdoor masks are the strict attenuation requirements at 3.1 and 10.6 GHz. These strict requirements for outdoor UWB transmissions helps protect GPS receivers, which are centered at 1.6 GHz [6].

2.1.2 Advantages of UWB over narrowband systems

UWB radios have many advantages over narrowband systems. UWB is based on the transmission of extremely narrow pulses with a small amount of power. The energy of these pulses is spread over a wide frequency range, and therefore causes little interference to other devices. As a result of using very narrow pulses, UWB devices are also resistant to multi-path interference. UWB signals appear as noise to most other

wireless devices, so it is possible that UWB devices can exist in the same spectrum as other devices, such as 802.11a. Conventional narrowband devices consume more power as compared to UWB devices and can only achieve data rates of up to 54 Mbs as with 802.11g devices. Because the channel capacity is so large, it is expected that the data rate of UWB devices can exceed 1 Gbps as technology scales with Moore's Law [7]. Another advantage of UWB devices is their inherent low cost due to the fact that UWB devices do not require the amplifiers and oscillators that narrowband devices require [5], [8].

2.1.3 Applications of UWB systems

The potential of UWB systems is extremely vast, resulting from inherently high data rates and low power. Before the FCC allowed commercial use of UWB radios, the main use of UWB technology was for military applications. A major commercial application is home networking including high data rate televisions such as High Data Rate Television (HDTV). In addition to HDTV, most people that own TVs, also own VCRs and DVD players. These components can also be connected wirelessly using UWB home networks.

UWB high data rate wireless personal area networks (WPAN) are the focus of many companies and the IEEE 802.15.3a standardization committee. WPANs allow consumers to eliminate virtually all wires from their computers to such peripherals as the printers, monitors, PDAs, and others, which require data rates that are not yet available in a reliable wireless form. These peripheral devices can communicate with each other through a network. Using UWB systems as part of a home network has great potential and a wide variety of uses [10].

Another application of UWB technology is in the RFID (Radio Frequency Identification) market, which has a wide array of applications. One major use of RFID is as a tracking device. RFID tracking devices can be attached to items in an office, lab, hospital, etc, for locating or tracking inventory [11]. Another application is its use in employee badges, which can be used to open doors in offices, or to open garage doors to parking areas. Because of the low power required and relatively low data rate, these devices can be made to have a long lifetime on a single battery at a relatively low cost.

One interesting application is for grocery store items that require cooking in the microwave or conventional oven. These packages can contain small RFID chips that are read by ovens and automatically cook the food for the appropriate amount of time [12].

2.1.4 Impulse based vs. Multi-band based Standard

Currently, the IEEE standardization committee is in the process on finalizing a standard for 802.15.3a, focused on WPANs. After many meetings and proposals, there were only two proposals that remained. One proposal supported by an Intel lead alliance is a multi-band approach using Orthogonal Frequency Division Multiplexing (OFDM) [13], while the other approach proposed by an XtremeSpectrum and supported by Motorola and others, is an impulse based approach [14].

The proposed multi-band approach breaks the 7.5 GHz of available spectrum into 15 subbands. Such a method provides great spectral efficiency, utilizing the entire available bandwidth. By using many different subbands, the system can easily co-exist worldwide, by simply turning off some sub-bands that might interfere with other devices. Another advantage of a multi-band approach is its ability to efficiently capture multipath energy without fading [5], [13].

The proposed impulse based approach has changed slightly since the standardization process has started. Originally, the proposed method involved using just one band 3.1 to 10.6 GHz, as UWB was first thought of. However, XtremeSpectrum has modified their proposed method to include two sub bands, one on each side of the 5GHz frequency reserved for 802.11a. The proposed method uses a form of CDMA technology in order to allow for multiply users and also for better coexistence [14].

While both methods have their advantages and disadvantages, the multiband approach has gained much of the support for a standard; however, the support has not been great enough to finalize a single standard. Unless the mulitband approach can gain more support, it is likely that the standardization committee will standardize both approaches. Supporters of the multiband approach argue that the dual-band approach suffers from problems such as the near/far problem and the need for a more complex receiver than the proposed multiband approach [5]. Supporters of the dual-band approach argue that their approach costs less, consumes less power, and has a faster time

to market, especially since XtremeSpectrum has already developed chips using this technology for high data rate wireless video applications using Silicon Germanium (SiGe). Although, a multiband approach can reuse many known techniques of narrowband systems, it requires a more costly transmitter due to the additional hardware needed to support the 15 possible sub-bands. For uses in an RFID application it would not be feasible to use a multiband approach. Although it is likely an impulse-based system will not be a standard for 802.15.3a, an impulse-based solution can always be used in applications such as RFID or military applications, like ground-penetrating radar.

2.2 Gaussian Pulses

Since the main focus of this thesis is the on the development of a pulse generator for an impulse based system, we describe the basic types of pulses that are generated to transmit data in this fashion. Three types of pulses are Gaussian pulses, Gaussian Monocycle pulses, and Gaussian doublets.

2.2.1 The Gaussian Pulse

A Gaussian pulse has the Gaussian shape as shown in Figure 2.3 and is expressed as:

$$V(t, f_c, A) = Ae^{-2(\pi f_c)^2} \quad (2.1)$$

where A is the amplitude of the monocycle pulse, and f_c is the center frequency [15]. Note that the frequency spectrum of the Gaussian pulse does not meet the FCC regulations, as the bandwidth is too large.

2.2.2 The Gaussian Mono-cycle Pulse

Taking the derivative of the equation 2.1 we can obtain the equation for a Gaussian monocycle pulse.

$$V(t, f_c, A) = 2\sqrt{e} A \pi t f_c e^{-2(\pi t f_c)^2} \quad (2.2)$$

The center frequency of the monocycle pulse is usually defined as $(\pi\tau_0)^{-1}$ Hz, where τ_0 is defined as the time between the maximum and minimum points of the monocycle pulse [16]. Figure 2.4 shows the Gaussian monocycle pulse and its frequency spectrum. Again, note that the frequency spectrum does not meet the FCC regulations due to the bandwidth being too large.

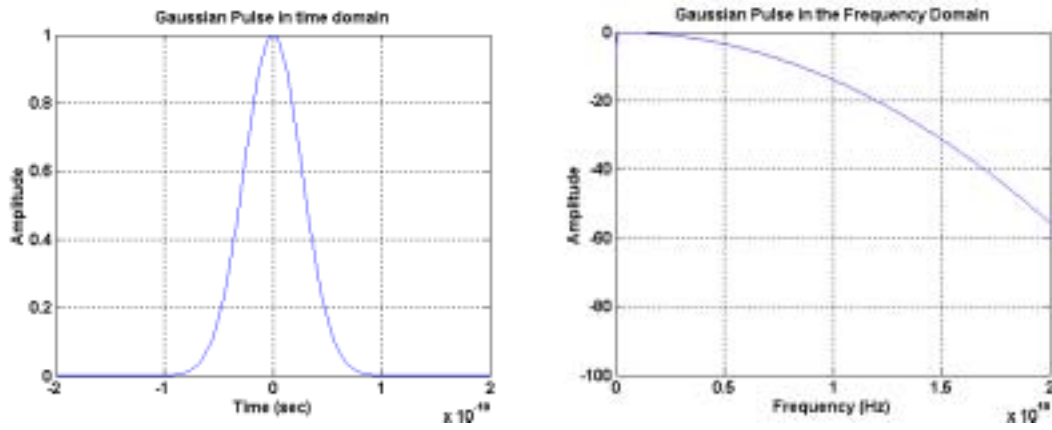


Figure 2.3: Gaussian Pulse and Frequency Spectrum

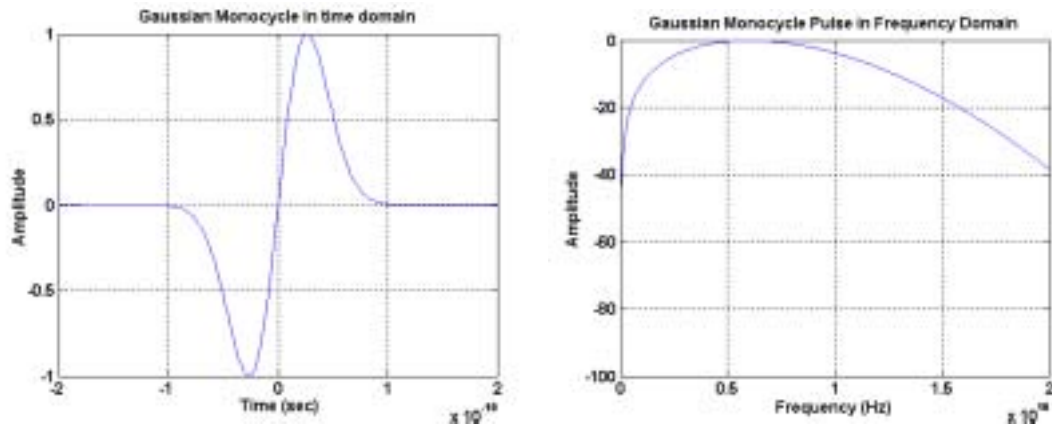


Figure 2.4: Gaussian Monocycle Pulse and Frequency Spectrum

2.3 Basic Modulation Schemes

We will discuss some modulation schemes that are considered for an impulse-based approach [18].

2.3.1 Binary Phase Shift Keying (BPSK)

The most common approach used in impulse based UWB systems is BPSK. This method of modulations involves transmitting a single bit of data with each pulse; a positive pulse representing a '1', and a negative pulse representing a '0' [19]. This is the one of the simpler approaches, requiring that only two pulses be generated, and requiring less processing at the receiver.

2.3.2 Differential Phase Shift Keying (DPSK)

An alternative to BPSK is DPSK, requiring slightly more digital processing at the receiver end. The current pulse is based on the previous pulse. If a '1' is to be transmitted, the pulse will equal the previous pulse. And if a '0' is to be transmitted, the pulse will be 180 degrees out of phase with the previous pulse. At the beginning of the bit stream it is assumed that the previous pulse was a positive pulse. Figure 2.5 shows an example DPSK modulation scheme.

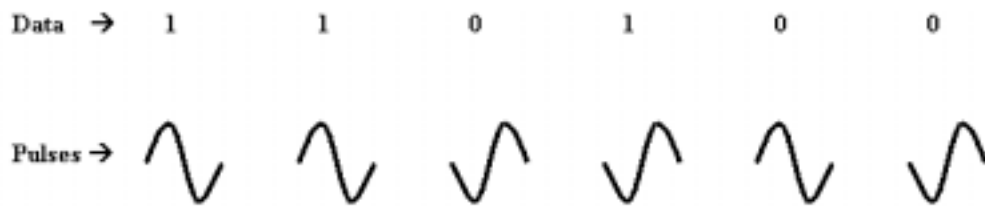


Figure 2.5: DPSK Modulation Example

2.3.3 Pulse Position Modulation (PPM)

Another alternative method of modulating data that has already been proposed by Staccato Inc. is PPM. This technique involves transmitting the same pulse in one of two positions in the time domain in order to represent a '0' or a '1' [22]. This method may require a more complex receiver in order to determine the position of the received pulse.

2.3.4 Ternary Modulation

Similar to PPM is a technique known as Ternary modulation. In this scheme, two bits of data are transmitted with a single pulse. For each transmission, a 0 and either +1 or -1 are transmitted. A zero is represented by no pulse, while +1 and -1 are represented by positive and negative pulses, respectively. Shown below in Figure 2.6 is just one possible way of relating the binary data to the ternary representation and then to a waveform [23].

Bit Values	Ternary Values	Pulsed Waveform
0 0	0 1	
0 1	0 -1	
1 0	1 0	
1 1	-1 0	

Figure 2.6: Example of a Ternary Modulation Method

It is possible that all of the modulation schemes mentioned in this section could be combined into one in order to transmit three bits with a single pulse. The pulse shape, position and phase of the pulse could be used simultaneously. Although this scheme would save power and increase data rates, its performance has not been studied rigorously. It increases complexity both at the transmitter and receiver.

2.4 MOS Current Mode Logic (MCML) Basics

An essential part of our pulse generator relies on the ability to generate extremely short delays. Contemporary CMOS technology cannot meet the specific delay requirements of a pulse generator for a UWB system. In this section, we briefly introduce MOS Current Mode Logic (MCML), which is inherently much faster than traditional CMOS logic due to the use of a lower swing voltage. Although, MCML circuits are typically used for low power consumption, we adopt MCML circuits mainly for high speed.

2.4.1 Basic Structure

A basic MCML circuit consists of pull up resistors, a pull down network controlling the flow of current, and a current source. Figure 2.7 shows the most basic MCML circuit, an inverter/buffer [24], [25].

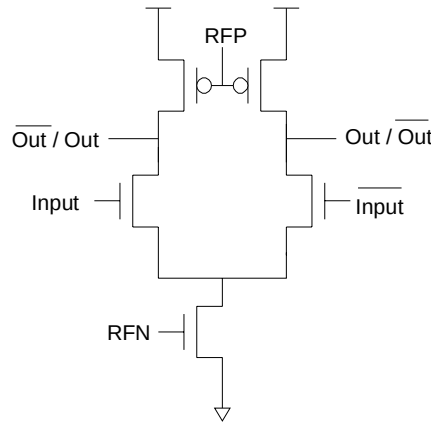


Figure 2.7: Basic MCML Inverter/Buffer Circuit

It consists of two P transistors that act as pull up resistors, an N transistor differential pair acting as the pull down network, and a single N transistor as a current source. There are other methods of designing a current source and pull up resistors; however, we use single transistors in our design for reduced area and complexity.

The pull down network requires two complimentary inputs, and the circuit produces complimentary outputs. As the inputs change, the current swings from one side

to the other, raising or lowering voltage levels on the two outputs accordingly. Determined solely by the current set by the RFN transistor and the resistance of the RFP transistor, the voltage swing of the output is generally much smaller than VDD. The voltage swing is calculated as $\Delta V = I \times R$. In most designs where MCML circuits are implemented, the voltage swing is usually on the order of a few hundred millivolts [25].

2.4.2 MCML Delay and Power Dissipation

Assume that each output has a load capacitance C and voltage swing ΔV . Noting that $I = C \frac{dv}{dt}$ the total delay of N identical inverters can be generalized as:

$$\text{Delay} = \frac{N \times C \times \Delta V}{I} = N \times C \times R \quad (2.3)$$

Hence, the delay can be adjusted through ΔV and the bias current I . We adjust these two parameters to obtain the necessary delay in our design. Due to a constant current source, the static power consumption of an MCML circuit can be calculated as follows:

$$\text{Power} = N \times I \times V_{dd} \quad (2.4)$$

Since MCML circuits have a much smaller voltage swing than CMOS circuits, it has been shown in [25] that there is a break point when MCML circuits consume less power than CMOS circuits. If CMOS circuits switch often, the power consumed from short circuit power consumption begins to dominate, and this is where the MCML circuit's small voltage swing enables MCML to dissipate less power than CMOS.

2.4.3 Loading Effects

Our design requires conversion from MCML to regular CMOS circuits. When driving MCML with CMOS logic, one design consideration is the generation of differential inputs. We describe the impact of the timing difference between the availability of these inputs on the MCML circuit operation in the next chapter. Another

issue is the loading effect on an MCML circuit. When we previously discussed the equation for the delay, we assumed that all load capacitances were the same for N gates. However, if an MCML circuit must drive two gates, resulting in twice as much capacitance, the delay increases. One method of combating this is to decrease the voltage swing. Another method, one that is adopted in our design, is to increase the current, which yields increased power consumption.

2.5 Impulse and Multi-band Pulse Generators

We have based the designs in this thesis on two methods for transmitting data using UWB technology. As discussed previously, there are two approaches that are actively being pursued, an impulse based approach and a multiband based approach. Here, we will give a generic example for the TX structure for both approaches. In doing so, we will be able to show just how a pulse generator can be used in both approaches and how it fits into the transmitter.

2.5.1 Basic Impulse Based TX Structure

The basic transmitter structure of an impulse-based system is much simpler than that of a multiband system. Figure 2.8 shows a basic impulse based TX structure.

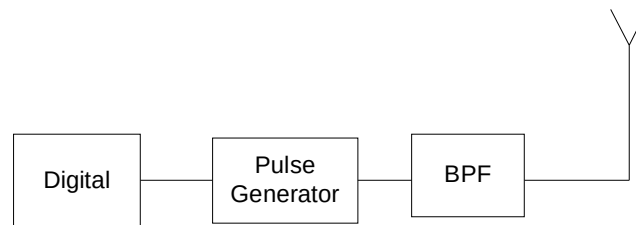


Figure 2.8: Basic Impulse Based TX

The BPF is used to ensure that the generated pulse from the pulse generator meets the FCC's spectrum restrictions. The difference in most impulse-based designs is in the creation of such a short pulse using a pulse generator.

2.5.2 Previous Work on Subnanosecond Pulse Generation

Existing methods for generating subnanosecond pulses generally require large circuits, which result in increased cost. These existing pulse generators are often not evaluated in terms of power consumption and the feasibility of integrating them into a wireless device. Some pulse generators were developed using spark gaps [29], which are not an option for consumer electronics due to their size. Another method of generating subnanosecond monocycle pulses involves the use of a schottky diode, a step recovery diode (SRD), and a coplanar waveguide [30]. The pulse generator developed in [30] using a SRD is shown in Figure 2.9.

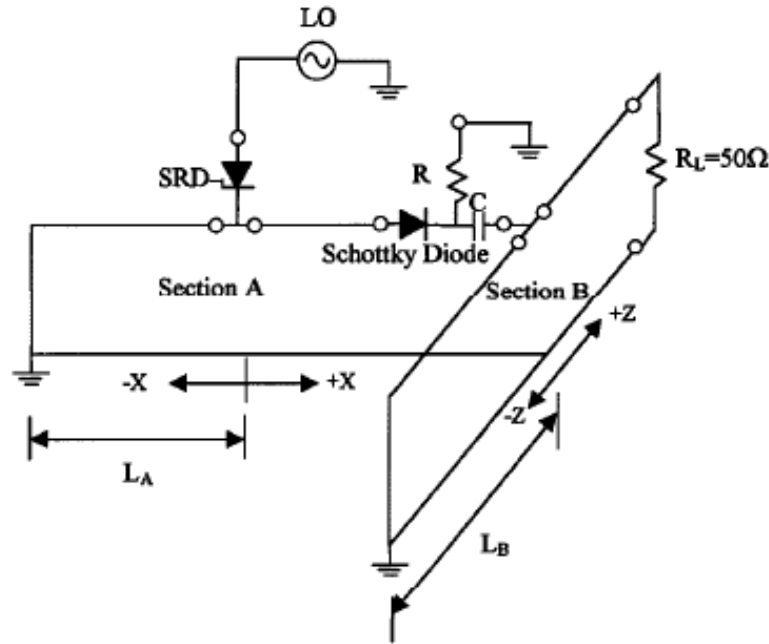


Figure 2.9: Pulse Generator Developed in [30]

In order to examine how a pulse is generated, the pulse generator is broken up into two sections, A and B. First, the LO provides a 10 MHz square wave to the SRD, which generates a step-like pulse. Once a step-like pulse arrives at transmission line A, it is divided into two other step pulses that propagate in the $+x$ and $-x$ direction. The step function traveling to the short circuit is reflected back along the transmission line and combines with the other step pulse to form a Gaussian pulse. This Gaussian-like pulse then travels to the Schottky diode, turns the diode on and charges the capacitor C. This

pulse is then high-pass filtered by the capacitance, C , and resistance, R , which allows only the positive and negative edges of the pulse to continue to section B and into the $+z$ and $-z$ directions. Just as in section A, the pulse propagating in the $-z$ direction is reflected back at the short circuit and travels to the load. This negative pulse arrives at the load and combines with the positive pulse to form a monocycle pulse.

The pulse generated in the design above was improved by incorporating an impulse-shaping network using a MESFET [31]. A depiction of this improved circuit is shown in Figure 2.10.

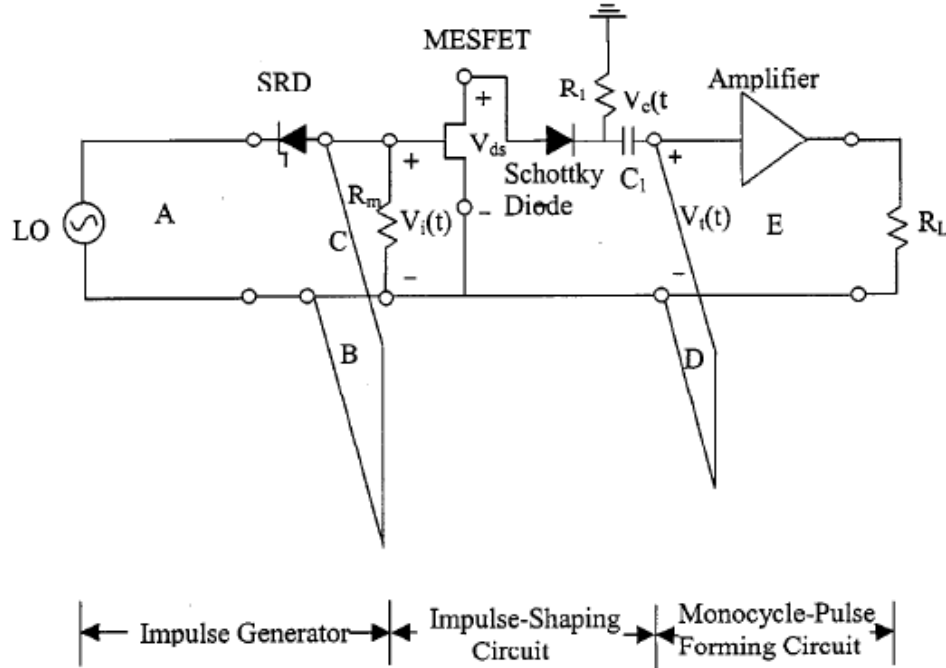


Figure 2.10: Pulse Generator Developed in [31]

Similar to the previous method, the LO produces a square wave and the SRD produces a step function, which is then divided into two equal step functions. The step function propagates into transmission lines B and C. Then the step function traveling in line B is reflected back from the short circuit and combines with the other step function in line C to form a negative impulse at $V_i(t)$. The MESFET inverts the negative pulse and amplifies it. Also, the MESFET transfers the voltage source to a current source in order to create a less-distorted impulse. The resultant positive impulse turns on the Schottky diode, travels through the high-pass filter, and forms a monocycle pulse. This improved

approach achieves less distortion, easy wideband matching, and an improved pulse repetition rate as a result of incorporating a MESFET into the design. One disadvantage of time domain methods of pulse generation is that a great deal of energy in the pulse lies around DC, which cannot be radiated by the antenna.

An alternate method of pulse generation, which is very accurate, is to generate an impulse in the frequency domain rather than the time domain [32], [33]. The approach proposed in [33] is a Fourier method of waveform generation. The desired waveform in the time domain is expanded using Fourier series, then the sinusoidal components obtained from the Fourier series expansion are generated and transmitted. The Fourier series expansion contains an infinite amount of terms; however, in reality the transmitter only transmits a finite number of these terms, depending on the desired performance. Figure 2.11 shows the basic block diagram of the proposed frequency domain pulse generator where a separate oscillator generates each harmonic, which is amplitude and phase controlled.

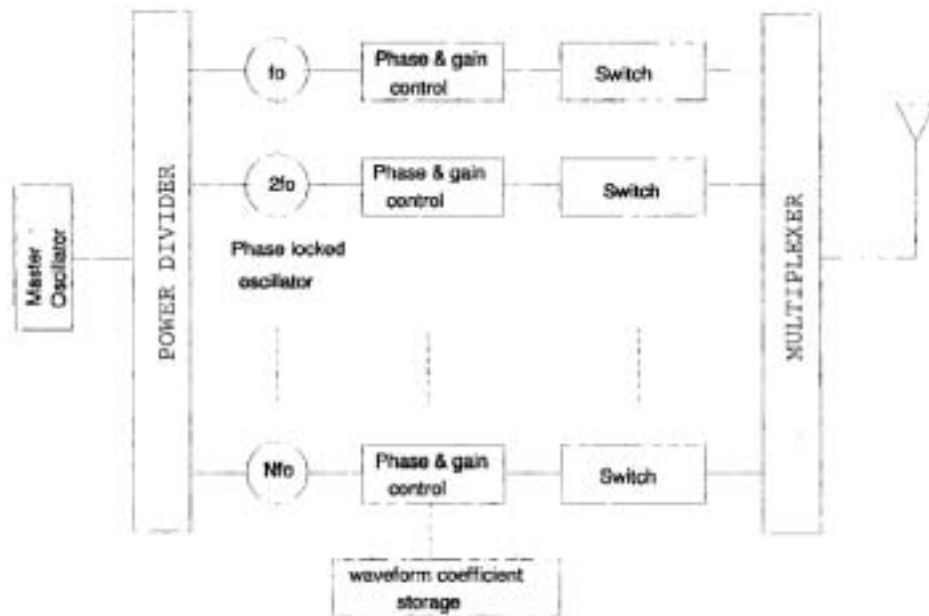


Figure 2.11: Block Diagram of Frequency Domain Transmitter [33]

Although the approach depicted in Figure 2.11 can produce extremely accurate results in theory, it requires a very complex transmitter design. Since the approach requires that the pulse be broken into multiple harmonics, the receiver will have to receive all of the generated harmonics, requiring a complex receiver. Due to the complex nature of the design it is not suitable for most wireless UWB applications.

The methods described above all have one common problem, large area requirements and hence, high cost. Another alternative approach, which is the basis for our design is to use a single stage CMOS amplifier [36]. The basic CMOS amplifier is shown below in Figure 2.12.

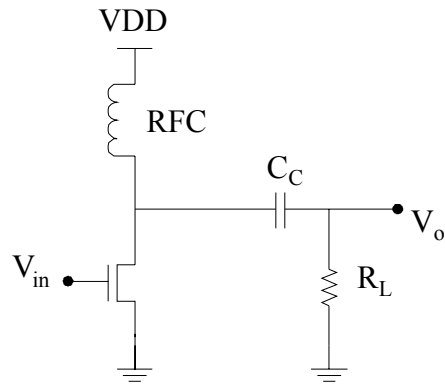


Figure 2.12: Basic single stage CMOS amplifier

The amplifier generates pulses at the output by switching the input of the single transistor. By toggling the input of the transistor, the direction of the current is controlled, and a pulse is generated through the charging and discharging of the capacitor. This approach can be implemented onto a single chip, at a low cost compared to existing pulse generation methods. The pulse repetition frequency and shape can be controlled by control logic applied to V_{in} .

2.5.3 Basic Multi-band Based TX Structure

Here, we briefly discuss a rectified cosine generator often used for a multiband transmitter, and show the use of a rectified cosine generator. A rectified cosine generator generates a continuous cosine pulse with a DC offset that is half the peak-to-peak amplitude. It is represented as follows [37].

$$f(t) = \frac{A}{2} \left[1 + \cos \frac{2\pi}{T} \left(t - \frac{T}{2} \right) \right], \quad 0 \leq t \leq T \quad (2.5)$$

A rectified cosine pulse is shown in Figure 2.13. Ideally, a rectified cosine pulse reaches half of its peak amplitude at the halfway point in time between the center and the end of the pulse.

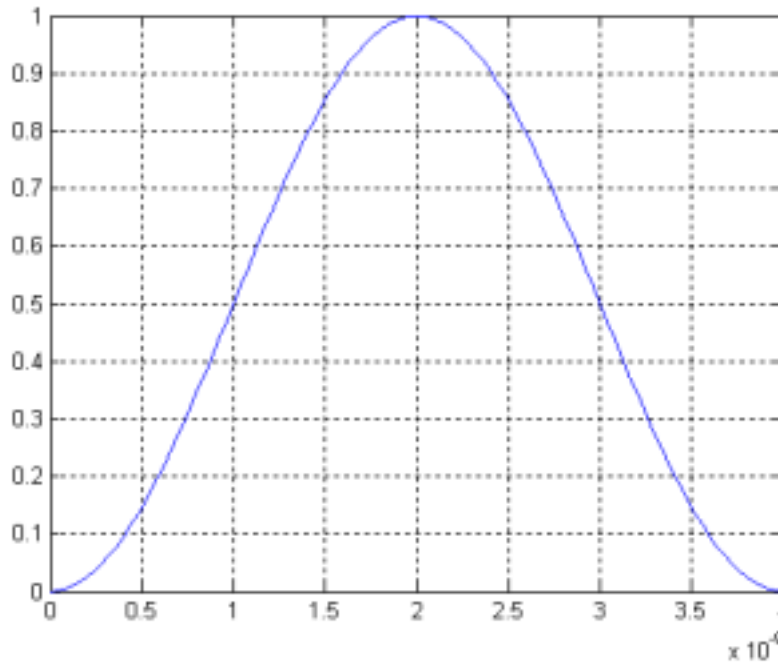


Figure 2.13: Rectified Cosine Pulse

In order to understand the use of a rectified cosine generator in a multiband system, we describe one simple approach of which most approaches are based. A

multiband approach divides the 7.5GHz of available spectrum into several subbands, where each subband has a -10dB bandwidth of more than 500 MHz. Figure 2.14 shows one possible approach for a multiband system, where N represents the number of subbands. The structure consists of N local oscillators for each of the sub-bands. The generated rectified cosine is mixed with each LO independently in order to meet the FCC's 500 MHz minimum bandwidth regulation. In this example, a MUX is used to select the subbands to be used.

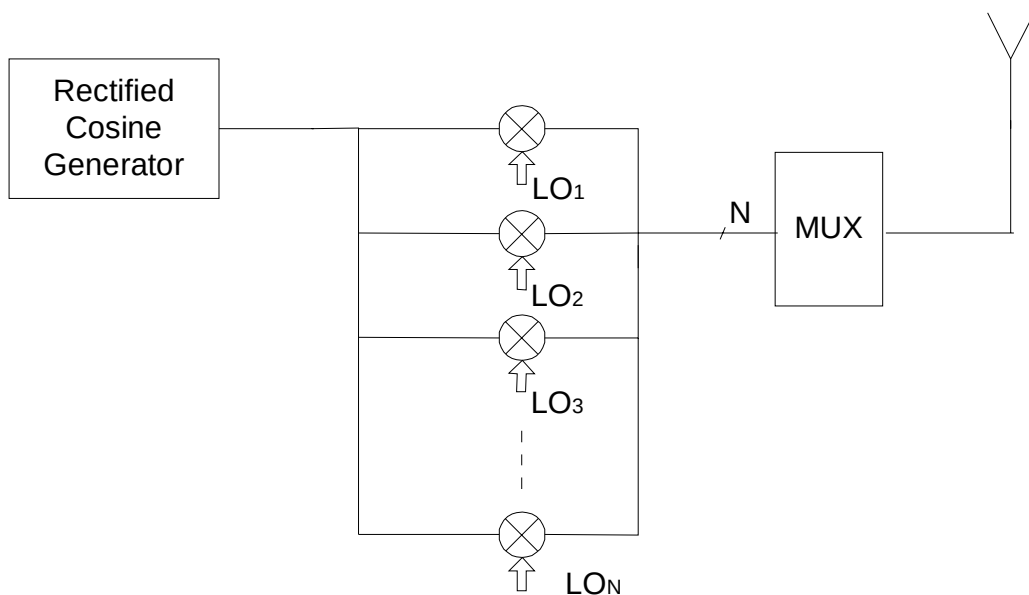


Figure 2.14: Basic Multi-band TX

There are many possible approaches and variations of a TX structure for a multiband system, but all approaches require a rectified cosine generator or filter to provide the envelope necessary to meet the FCC minimum bandwidth requirements.

Chapter 3

Design of a Pulse Generator for Impulse UWB Radios

In this chapter, we describe the development of our pulse generator for impulse based UWB radios, which can be extended to many applications of UWB radios. The design involves a CMOS-based approach, which has not been realized before, but as technology progresses will become an even more viable option.

3.1 System Target Specifications

Although the main goal of our design is to show that a CMOS-based pulse generator is possible for UWB radios, we also based our design around possible applications such as a low data rate RFID system. In order to achieve a versatile design we have developed a pulse generator that can adapt to meet the specifications of an impulse-based system. Although our design is for an impulse-based system, the next chapter shows the versatility of such a pulse generator approach when we extend the design to a multiband system. In order to meet the FCC's UWB requirements, we have developed the target specifications given in Table 3.1.

Table 3.1: Pulse Generator Target Specifications

Specification	Target value
Center frequency	6 GHz
Bandwidth	6 GHz
Transmit power	-42dBm

Most of the specifications shown above are related to the spectral emission limits. As we have described in the previous chapter, it is difficult for Gaussian pulses and monocycle pulses to meet the emissions requirements without an additional filter. So the

emissions regulations are not as critical in our design as the pulse shape and pulse duration, which determine the fidelity of the received signal. The emissions requirements will be met through minimal filtering following the pulse generator.

3.2 Overview of Pulse Generator Structure

Our pulse generator is based on a single stage CMOS power amplifier, where the switching of a single transistor is used to generate impulses. We have extended this power amplifier approach from one transistor to four transistors, thereby, as will explain, allowing the generation of more than one pulse shape.

3.2.1 Basic Structure

The basic structure of our design involves a power amplifier with four control taps, A through D, as shown in Figure 3.1. The desired pulse is broken up into specific transitions in time. The pulse generator generates the desired pulse through a combination of specific input transitions on the control taps.

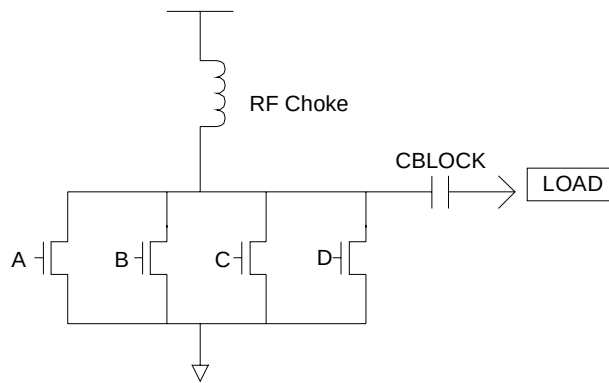


Figure 3.1: Basic Pulse Generator Structure

The circuit involves an off-chip RF Choke, which provides a constant current source over a large range of frequencies. A blocking capacitance is used, as in most circuits, to eliminate the amount of DC at the output of the amplifier.

3.2.2 Pulse Generation

In Figure 3.1, suppose that control taps A, B, C, and D are set to Vdd, GND, GND, and Vdd, respectively. The power amplifier is in an idle state with no current flowing to the load. Note that the current flows through the RF choke and the two conducting transistors. We illustrate the generation of a positive Gaussian monocycle pulse as an example. From the idle state, suppose that the control tap B switches to GND, turning transistor B off. The current flowing through transistor B starts to flow through the capacitor to the load, generating the first positive slope of a pulse. After a certain delay, the control taps A and D are turned on. Then the current starts to flow in the opposite direction, generating the negative slope of the pulse. Lastly, the control tap C is turned off, and the direction of the current changes again, generating a positive slope of the pulse. Figure 3.2 shows a waveform illustrating the switching sequence of the four control taps and the resulting Gaussian monocycle pulse.

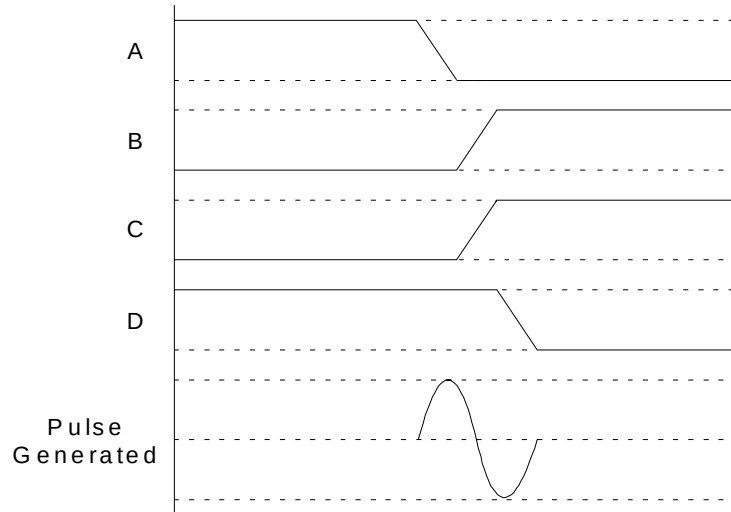


Figure 3.2: Monocycle Pulse Generation Example

In addition to generating a positive monocycle pulse as described above, this four-tap power amplifier can also generate both positive and negative Gaussian pulses and monocycle pulses through different input switching sequences. An example of the generation of a Gaussian pulse is shown in Figure 3.3.

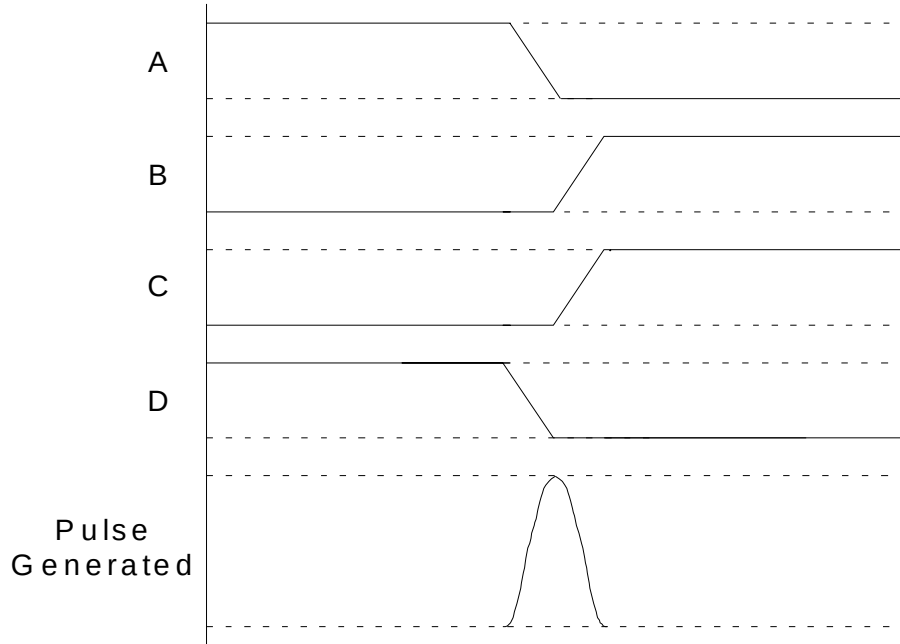


Figure 3.3: Gaussian Pulse Generation Example

The generation of the pulses shown above is possible using a CMOS power amplifier with only four taps; however, this approach can be extended to generate additional pulses such as a Gaussian doublet, or further derivatives of the Gaussian pulse, by adding additional control taps. The number of pulses that are possible using this approach is limited only by the complexity of the control circuitry, which is directly related to the number of control taps. For this reason, we have chosen to design a pulse generator capable of producing only two types of pulses.

Figure 3.4 presents a partial transition diagram and the shape of the generated pulses from an initial state. The “Positive” or “Negative” of a state denotes the starting slope of the pulse generated, and the four binary values are the final values of the four control inputs, A, B, C, and D, respectively. The order and timing of the control inputs determine the shape of pulses generated, as shown in Figure 3.4. The label associated with a transition indicates the order of the inputs that is necessary to change from the initial state 0110 to the final state 1001, and commas indicate the delays between two input changes. For example, if the control input A changes to 1 first, followed by the simultaneous change of B and C, and then by a change of D, this is labeled as “A,BC,D”.

This example results in the generation of a negative pulse, as shown in Figure 3.4. The diagram suggests that the introduction of more control taps combined with variations of the timing and the order of control inputs enables us to generate various shapes of pulses such as Gaussian doublets.

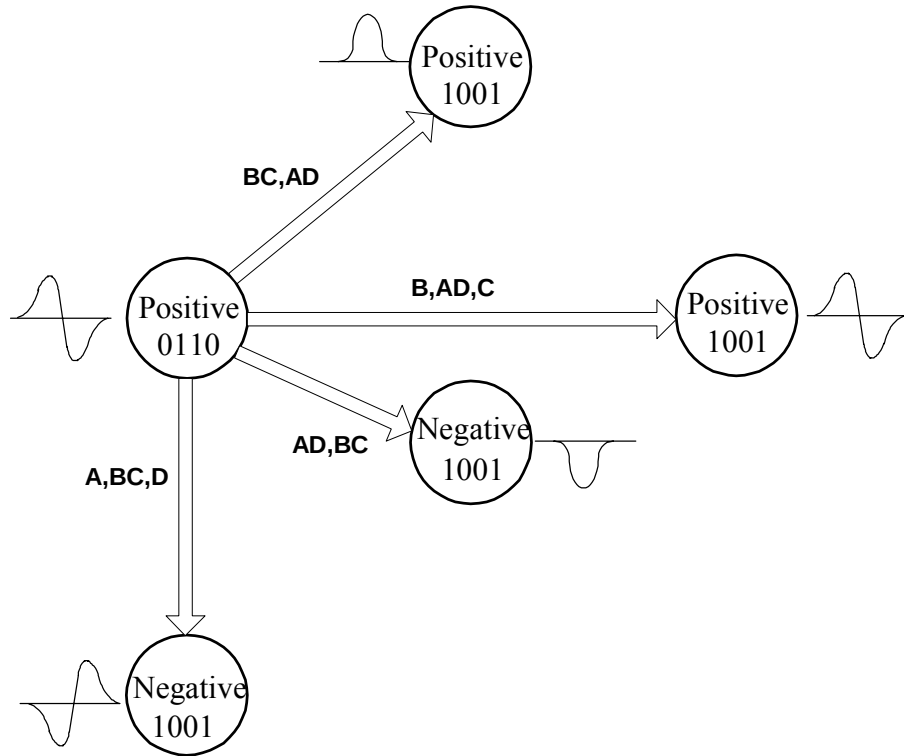


Figure 3.4: Control Tap State Transition Diagram

Initial simulations were conducted to determine the fidelity of the pulses generated using the 4-tap CMOS power amplifier approach. Inputs with 50 ps rise and fall times were applied to the 4 taps in order to generate the four possible pulses. The results are shown below in Figure 3.5, (a) though (d).

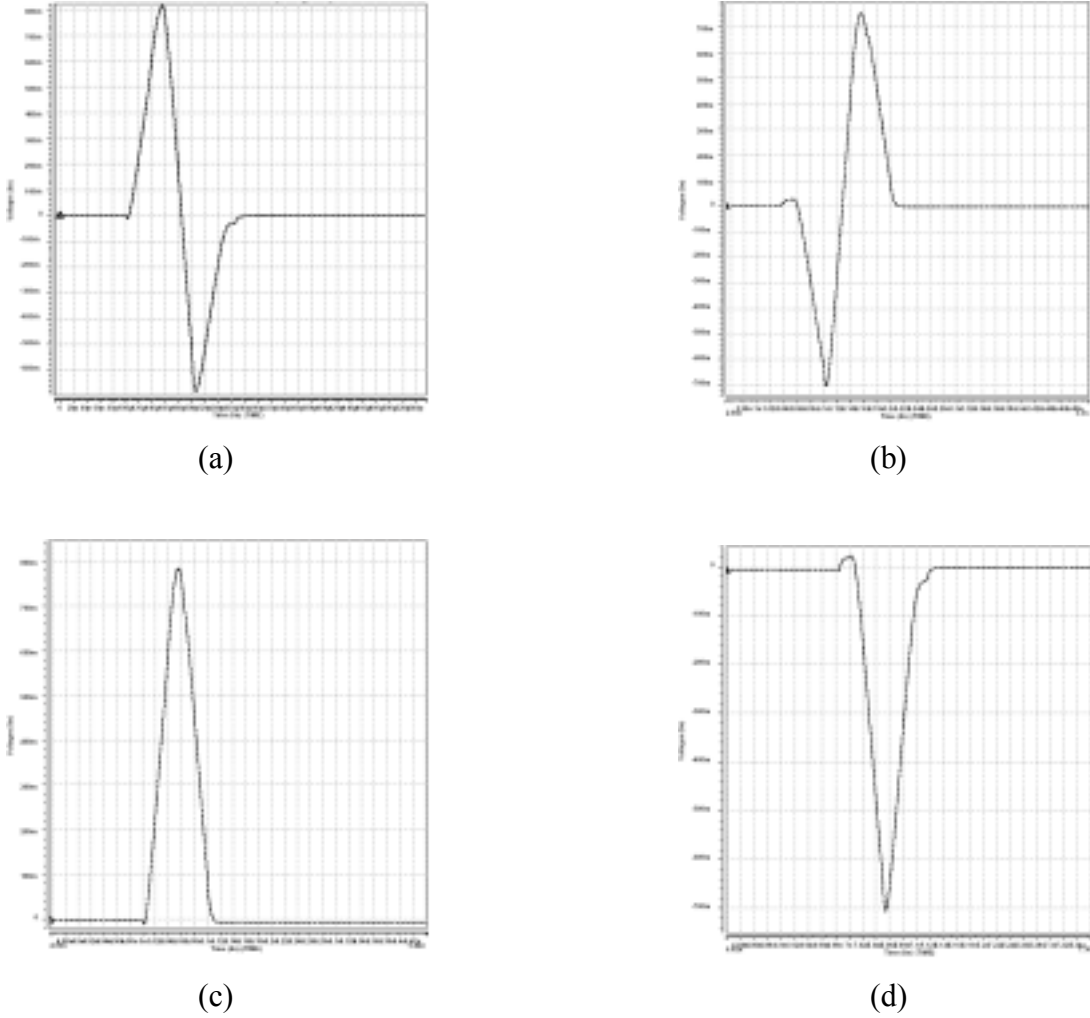


Figure 3.5: Initial simulations of the pulse generation

3.3 Pulse Generator Design

We designed our pulse generator with the target technology of the TSMC 0.18 μm CMOS processing at a supply voltage of 1.8 V. The number of taps, i.e., transistors, in Figure 3.1 determines the fidelity of the pulse shape generated, and the size of the transistors mainly determines the amplitude of the pulse. In order to minimize power consumption, control logic complexity, and area, we chose a four-tap power amplifier capable of generating pulses with constant amplitude.

3.3.1 Pulse Generator Organization

In order to support the timing requirements and many possible modulation schemes, a control logic block consisting of a state machine, delay elements, a set of D Flip-Flops and a pass transistor control section was developed. Figure 3.6 shows the entire block diagram of our pulse generator including a bandpass filter. The bandpass filter is added at the output of the pulse generator to remove any DC offset and to eliminate the out-of-band undesired spectrum. The delay generator block is used to generate a delayed clock signal. The delayed clock signals are used to control the timing of the input to the four control taps of the power amplifier. The delay for each stage of the delay generator necessary to generate pulses with a pulse width of 150 ps was obtained through simulation and is set to 50 ps for our design.

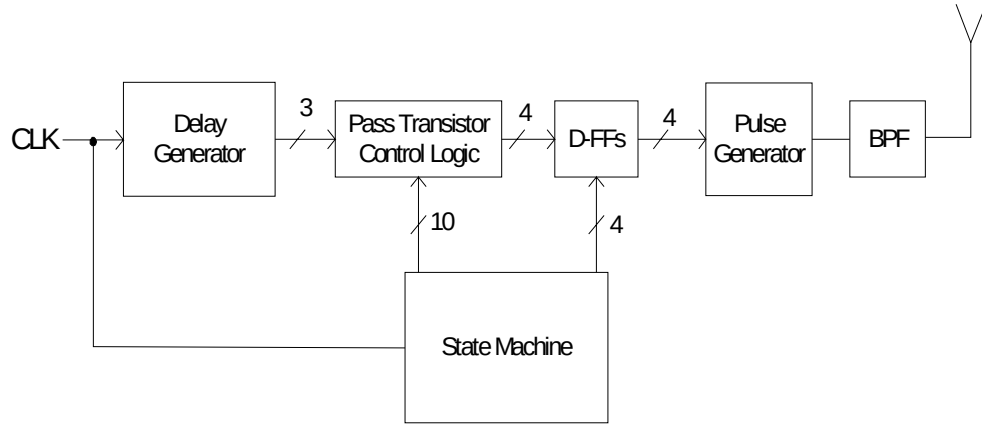


Figure 3.6: A Block Diagram of Proposed Pulse Generator

Figure 3.7 shows a more detailed view of the control logic. The delay generator produces the necessary 50 ps delayed clock signals. These delayed clock signals are connected as the clock inputs to the D flip-flops through buffers and pass transistor logic, which is controlled by outputs from a state machine. In addition to controlling the switching of the pass transistors, the state machine controls the D inputs to the flip-flops. The “state machine” can be implemented on chip, or for re-programmability, it can be implemented off chip as a small processor or re-programmable device. The outputs of the flip-flops are connected through buffers to the four large transistors of the power amplifier.

As it can be seen, pass transistors are used to control the path of the delayed clock signal to either of the four flip-flops. In order to maintain the same load and the same delay for the delayed clock signals, an extra pass transistor is used with the switches before the first two D flip-flops. So signal X or Y in the first two flip-flops incurs the same delay as X, Y, or Z in the last two flip-flops.

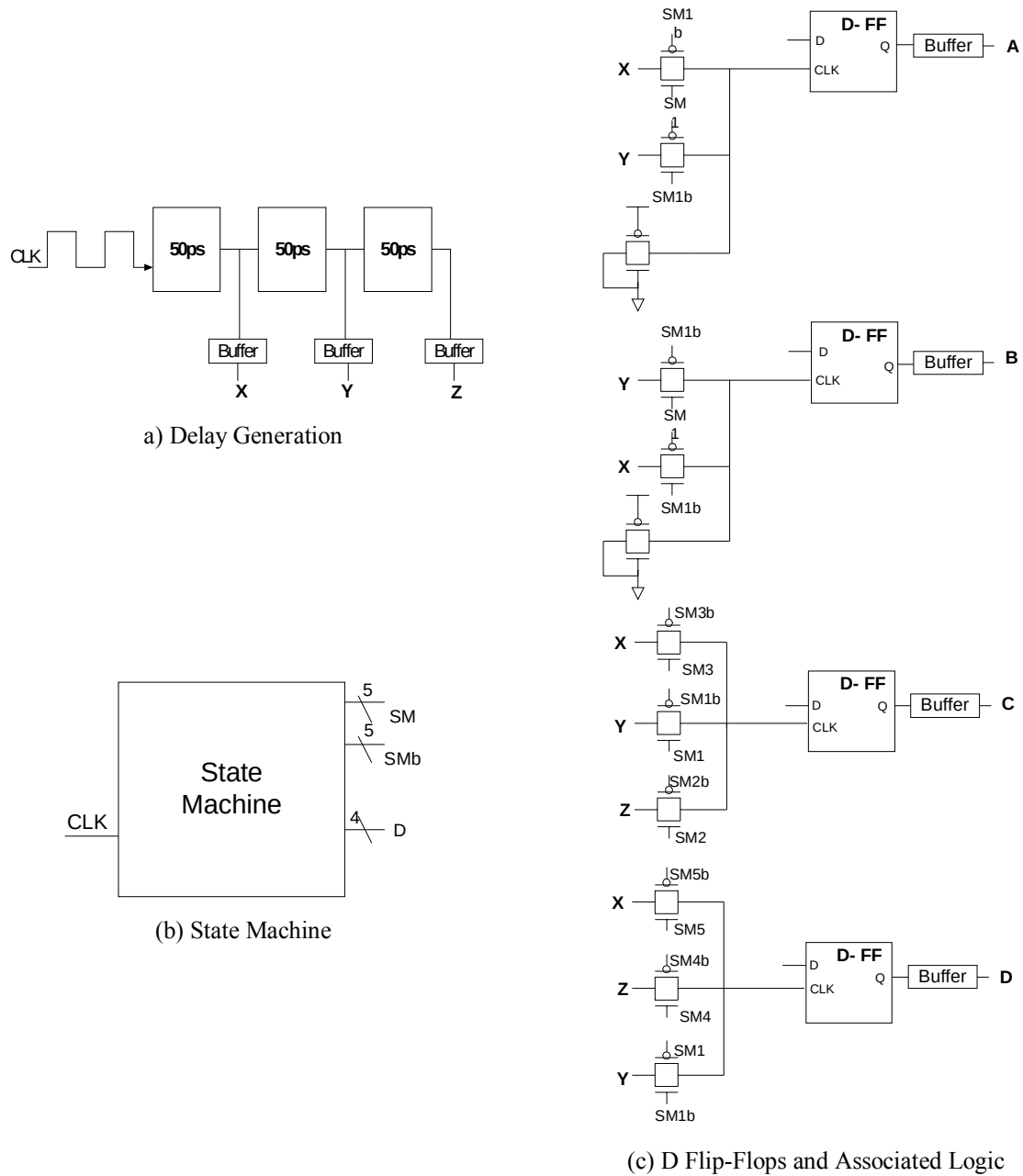


Figure 3.7: Control Logic Block Diagram

The outputs from the state machine shown in Figure 3.7 SM1 through SM5 and SM1b through SM5b drive the transmission gates in such a way that they determine the ordering of the delayed clock inputs to the D flip-flops. Shown in Table 3.2 is the truth table that determines the values of these control signals.

Table 3.2: Transmission Gate Control Truth Table

INPUTS								OUTPUTS (flip-flop inputs)			
<u>X</u>	<u>Y</u>	<u>Z</u>	<u>SM1</u>	<u>SM2</u>	<u>SM3</u>	<u>SM4</u>	<u>SM5</u>	<u>A</u>	<u>B</u>	<u>C</u>	<u>D</u>
X	Y	Z	0	1	0	0	0	Y	X	Z	Y
X	Y	Z	1	0	0	1	0	X	Y	Y	Z
X	Y	Z	1	0	0	0	1	X	Y	Y	X
X	Y	Z	0	0	1	0	0	Y	X	X	Y

3.3.2 Developing MCML Delay Elements

One of the most important elements for our pulse generator is the generation of precise delays, necessary for accurate pulse generation. The speed of a CMOS circuit is limited by the technology and is not able to produce the necessary delays for our control circuit. Thus, we implement the delay elements using MOS current mode logic (MCML), which can achieve faster speeds than CMOS by using a smaller voltage swing. Although MCML circuits are fast, there are concerns using these circuits in our design. Our concerns include the ability of MCML circuits to drive large loads, to produce complimentary inputs to the MCML circuit that meet necessary timing requirements, and to precisely set the delay to 50 ps.

The first step in designing the 50 ps delay is to observe the effect of transistor sizing on the delay of an MCML circuit. After simulating MCML buffer chains of various depths we found that an easy way to accurately generate the necessary 50 ps delay was to use two MCML inverters and one MCML buffer. A schematic view of a single delay element is shown below in Figure 3.8.

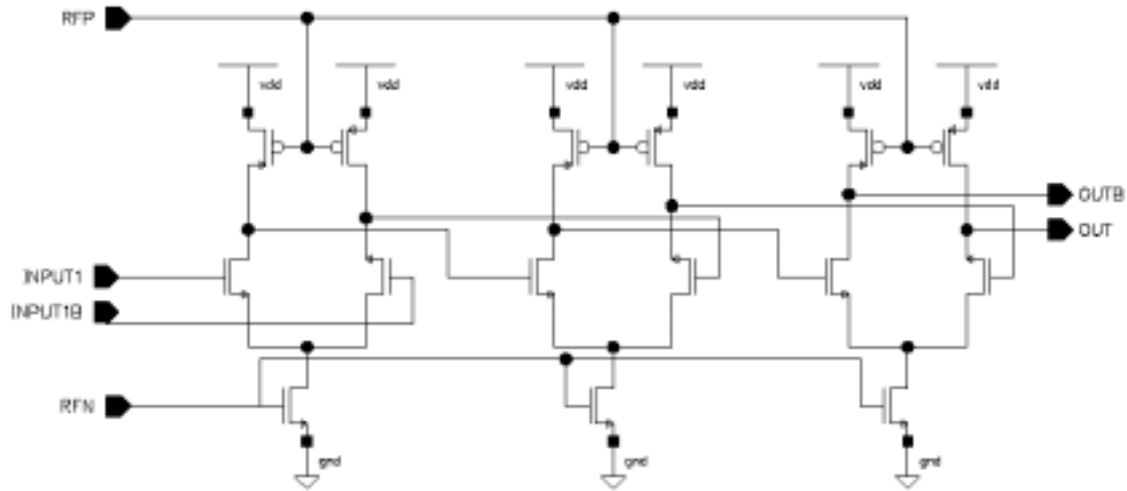


Figure 3.8: Single Delay Element Designed

The delay element was simulated to determine the transistor sizing that provided the most accurate and robust 50 ps delay. After running many spice simulations and adjusting the transistors, we achieved a rise delay of 45.172 ps and a fall delay of 44.947ps. The circuit in Figure 3.8 achieves the delay, in which the transistor sizes are $W=2.08 \mu\text{m}$ and $W=0.37 \mu\text{m}$ for the RFN and RFP transistors, respectively. Shown in Figure 3.9 below is the waveform that resulted from the simulation of the circuit described above.

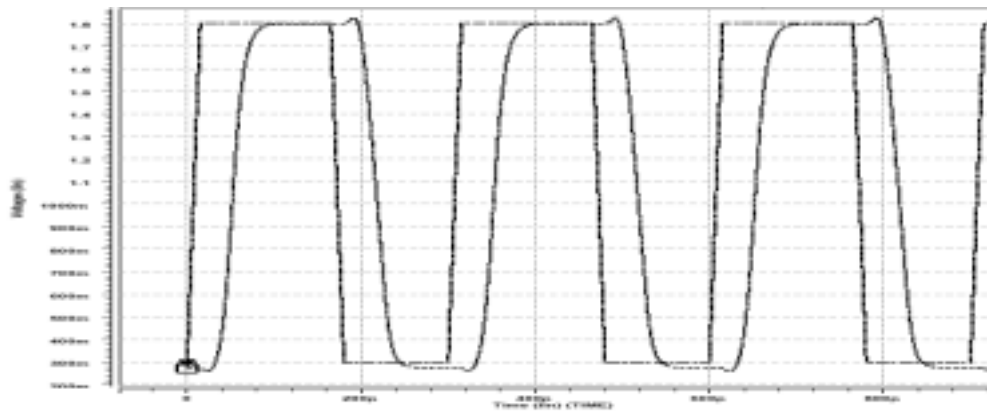


Figure 3.9: Input and Output of Delay element ~ 45ps delay

The next step in designing the 50 ps delay elements is to observe the affect of loading. These circuits should be able to drive a CMOS gate and another MCML inverter. Two MCML delay elements are cascaded together and the delay at the output of the first element is observed. The results of spice simulations show that there is only a slight increase in the delay time, from 45.172 ps and 44.947ps to **49.795 ps** and **49.547 ps** for the rise and fall delays, respectively.

The last concern that we addressed is the effect of the timing difference between the complementary inputs needed for an MCML circuit. To test this, we simulated the delay elements with various timing differences between the two inputs. The same transistor sizes are used as in the scheme described above which produced delays of about 45 ps. The results of these simulations indicate the delay between complimentary inputs does not have a significant impact on the delay of the MCML circuit. With these results, a simple CMOS inverter can be used to provide the complimentary inputs to this circuit.

After completing the initial simulations, we can construct the entire delay element to accurately produce the necessary 50, 100, and 150 ps delays. Consisting of three cascaded 50 ps delay elements, the circuit is tested and we find that the impact of loading has a slightly larger affect than predicted. This is easily corrected by sizing the transistors and observing the resulting delays at the three outputs. The transistors are sized so that the first delay element is approximately three times that of the last, and the second is approximately twice that of the last. The completion of the delay chain is an important part of the entire pulse generator, and after realizing the circuit; we design the rest of the control circuitry.

3.3.3 D Flip-Flops

The control logic for the pulse generator uses D flip-flops to control the four input taps of the power amplifier. The MCML delay circuits provide the necessary delay between the clock inputs of the four D flip-flops; however, it is important that this delay is maintained through each flip-flop, whether the output is logic 0 or logic 1. Additionally, it is highly important that the rise and fall times of the outputs are relatively the same, as this has a large effect on the generated pulse shape.

Since for the initial design our main concern is simply the ability to generate a well-shaped pulse, we use a very simple D flip-flop. The topology of flip-flop we use is shown in Figure 3.10.

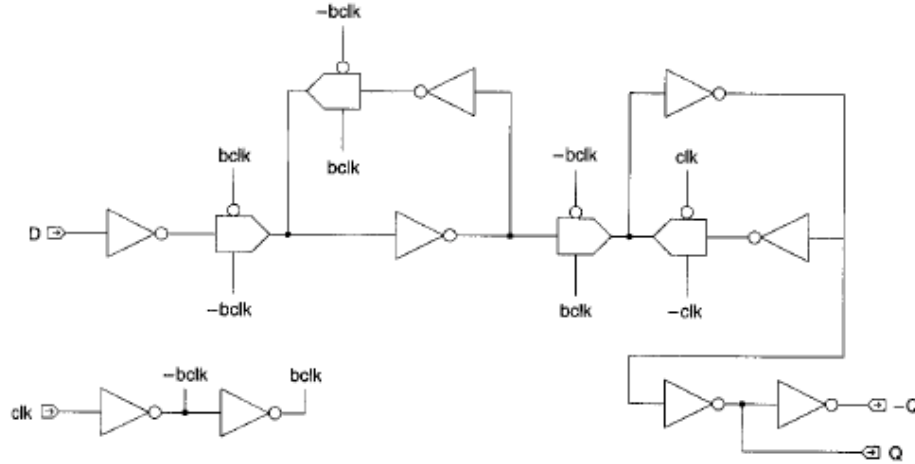


Figure 3.10: D flip-flop topology [40]

The D flip-flop uses pass transistors and inverters, and is not necessarily designed for speed. Rather, this design is chosen for the controllability of the rise and fall times through transistors sizing. The flip-flop was constructed, simulated and the transistors were sized until the delay through the flip-flops for 1's and 0's matched. The clock to Q delay for rising and falling Q outputs match at 191 ps, while the rise and fall times are approximately 32.9 ps and 26.8 ps, respectively. It is important to note that the delays through the flip-flops match rather than the rise and fall times of the output, as those can be manipulated after the flip-flop. A schematic view of the D flip-flop used in our design is shown below in Figure 3.11.

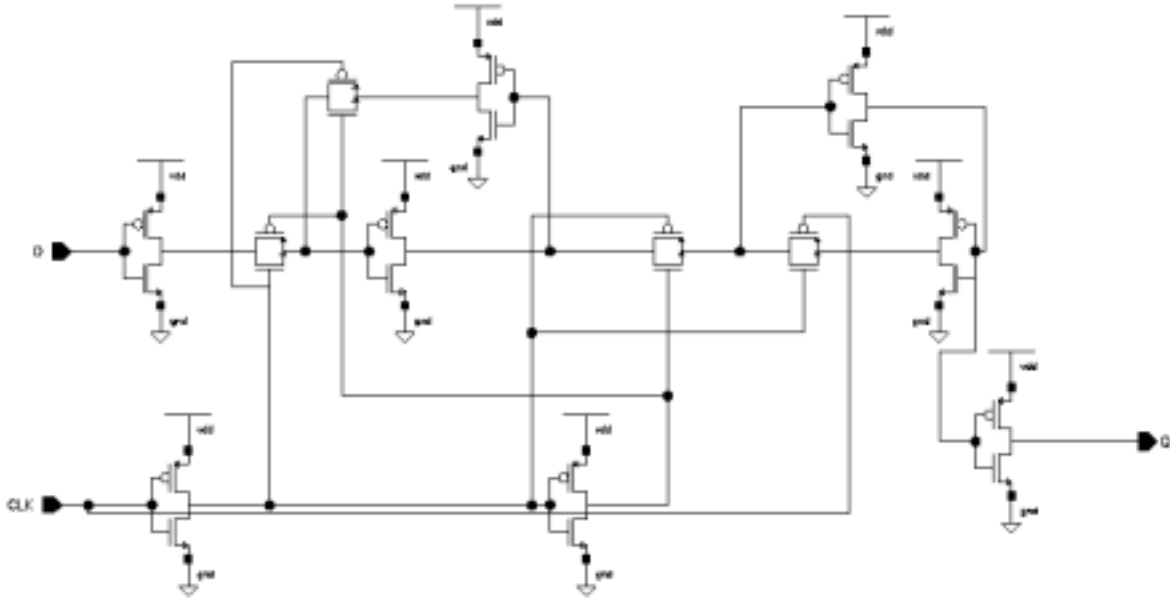


Figure 3.11: Schematic view of D flip-flop

In order for the output of the D flip-flop to be able to drive the large load of the four taps of the power amplifier, the entire FF would need to be extremely large to achieve equal rise and fall times. Thus, inverter chain buffers are used between the flip-flops and the power amplifier.

3.3.4 Buffering Components

Inverter buffer chains are used to maintain speed, and relatively low rise and fall times between unequal loads. It is not reasonable to have a 270 nm wide transistor drive a transistor that is 40 μm wide, as is the case at the output of the D flip-flop. For this reason, an inverter buffer chain is used between these components. For speed, the optimal ratio between the device widths of the buffers is known to be “e” (2.718) [42]. To reduce the number of large transistors, we use a ratio of three to four between inverters, requiring a chain of six inverters. The inverter buffer chain is shown below in Figure 3.12.

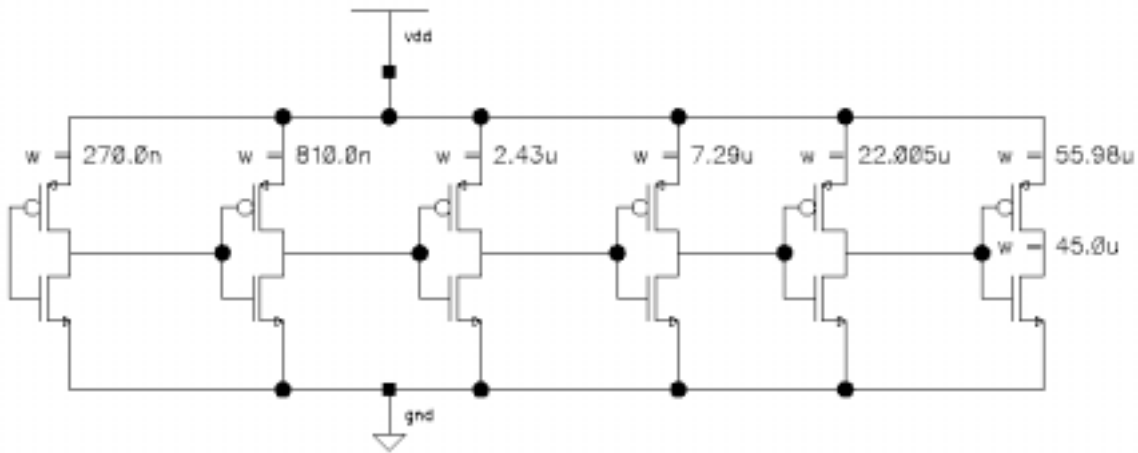


Figure 3.12: Inverter buffer Chain

Just as the D flip-flops are not able to drive the large load of the power amplifier, the MCML delay elements are not designed to drive the pass transistor switches of the control logic. It is possible to design the delay elements to drive the pass transistors, but it requires much larger transistors in the MCML circuits and since minimizing cost is an objective, we choose to use buffers instead. A similar inverter buffer chain to that shown in Figure 3.12 is used between the MCML delay elements and the pass transistors of the control logic. These are also sized such that that ratio of widths between the inverters is three to four.

3.3.5 Inductor for Constant Current

The ability to generate short powerful pulses stems from the quick swing of current at the output of the power amplifier. To supply a constant current we use an RF choke, which can be implemented as an inductor. Many off-chip inductors can be modeled as an inductance in series with a resistance as shown below in Figure 3.13.



Figure 3.13: Model of Inductor

An inductor is often evaluated in terms of a Quality Factor (Q). The quality factor is measured as the reactive power divided by the real power. The Q simplifies to

$$Q = \frac{\omega L}{R_s} \quad (3.1)$$

where ω is the operating frequency of the inductor, approximately 6 GHz in our case. Simulations were run where the inductor was modeled as shown above and the resistance was increased to determine the lowest Q that could be used while still achieving reasonable performance. We found that the desired Q of an inductor to meet our specifications is approximately 40.5. This result came from the inductance modeled with $L = 10.75$ nH, and $R_s = 10$ Ω . It is important to note, that in these initial simulations to find the inductor Q we considered R_s as independent of frequency, where as, in reality at these high frequency, R_s becomes a function of frequency and will have to be considered when the design nears fabrication [41].

3.3.6 Pulse Generator Timing

Now that we illustrated the structure and design of each component of the pulse generator, we show the timing requirements between the components in the circuit. To illustrate the timing of the circuit we refer back to Figure 3.7, where the pulse generator is broken in to three different sections. The only timing requirement that exists is the

requirement that the outputs of the state machine, the D inputs and the pass transistor controls arrive before the delayed clock signals output from the MCML delay elements. This direct dependence therefore limits the maximum clock speed at which the circuit can operate. Through simulations we found that the maximum clock frequency for our original design was approximately 750 MHz.

From simulations, we found that there is an ample amount of time between the arrival of the signals from the state machine and the delayed clock signals, which trigger the flip-flops. The logic is designed so that the state machine updates its outputs on the rising edge of the clock, while the flip-flops trigger on the falling edge of the clock after the respective delays.

3.3.7 BPF to limit spectral emissions

As discussed previously, Gaussian monocycle pulses alone cannot meet the FCC spectrum mask. Thus, it is necessary to provide some type of filtering at the output of the pulse generator. Like other UWB pulse generators, we suggest a bandpass filter at the output of our pulse generator. However, the design of such a component is out of the scope of this research. Thus, after the fabrication of our pulse generator, we will use an off the shelf band pass filter for preliminary testing.

3.4 Power Saving Scheme

In addition to generating an accurate Gaussian monocycle pulse, a major objective in our design is to minimize the power consumption of the entire circuit. To reduce the power, we first need to determine where the largest amount of power is being consumed. As expected, most power is consumed in the power amplifier section of the pulse generator. In the power amplifier, the average power dissipated is based on the current through two 40 μm wide NMOS transistors. Through initial simulations it was found that the power dissipated, as a result of this short circuit current, was over 80 mW. In addition, the bias current in the MCML delay circuits also contributes a large amount of static power dissipation.

3.4.1 Power Saving Scheme Illustration

To reduce the overall power consumption, we use a power saving scheme that can significantly reduce the overall power consumption for low data applications such as RFIDs. The basic scheme involves turning the pulse generator on, generating a desired pulse (in 3 clock cycles), and turning the generator off. This sequence can easily be implemented through the state machine by setting all the inputs of the D flip-flops to 0 volts, thereby turning off the 4 transistors in the power amplifier on the next clock pulse. The MCML delay circuit can also be turned off by changing the bias voltage applied to the RFN transistor to 0 volts.

As an example, Figure 3.14 illustrates the timing of our pulse generator for a data rate of 500 bps with a clock frequency of 250 MHz, which is sufficient for most RFID applications. The pulse generator turns on for 12 ns to send one significant bit accompanied by two spurious bits and consumes 57.15 mW during the time. Then, it is turned off for about 2 ms, (precisely speaking, 1,999,988 ns) consuming only 8.44 uW during this period. As a result of implementing this power saving scheme, the average power consumption is reduced to 8.783 uW.

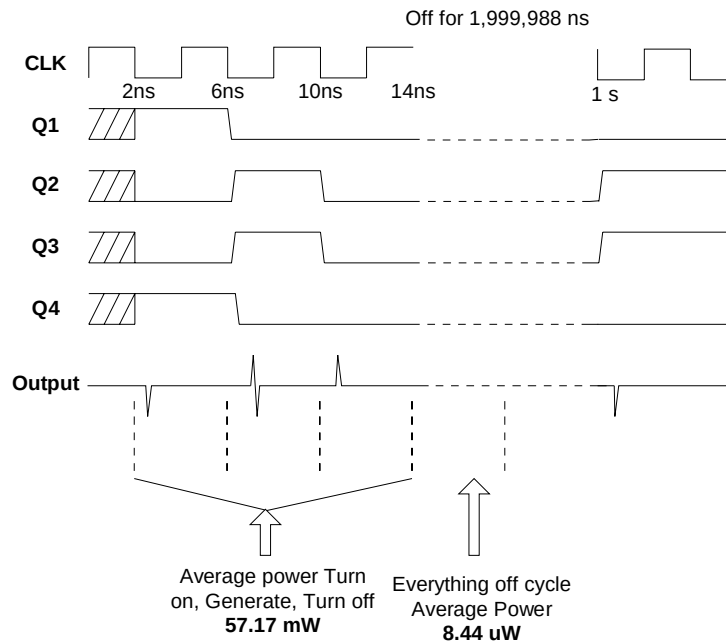


Figure 3.14: Timing Diagram of Power Saving Scheme

3.4.2 Side Effects and Limitations

One side affect of this type of power saving scheme is the introduction of spurious pulses. As shown in Figure 3.14, the pulse generator generates small spurious pulses when turned on and off. Our simulation indicates that the spectrum of these pulses is out-of-band and is filtered out by the band pass filter that follows the pulse generator. A limitation of this power saving scheme is that power is only significantly reduced at very low data rates. Table 3.3 is shown below to illustrate the relationship between data rate and power consumption for this type of power saving scheme. The entire power saving scheme described above can easily be implemented as part of the state machine in the control logic.

Table 3.3: Power Savings vs. Data Rate (Clock = 250Mhz)

Data Rate	Power Consumption without Scheme (mW)	Power Consumed with Scheme (mW)	Power Saved using Scheme (mW)
<i>100 bps</i>	84.00	0.00851	83.99
<i>1 Kbps</i>	84.00	0.00913	83.99
<i>10 kbps</i>	84.00	0.01530	83.98
<i>100 kbps</i>	84.00	0.07703	83.92
<i>1 Mbps</i>	84.00	0.69438	83.31
<i>10 Mbps</i>	84.00	6.86783	77.13
<i>100 Mbps</i>	84.00	68.60231	15.40

3.5 Future Work

The pulse generator designed shows the possibility of a CMOS realization for UWB systems. However, there are areas of this design, which can be improved. The areas of future work include minimizing power consumption at high data rates, reducing the effect of the near/far problem, reducing the number of off chip components, such as the inductor and BPF, and providing flexibility in terms of adjusting to a dual band/co-existence friendly approach.

3.5.1 Dynamically varying power

Although the power saving scheme described previously significantly reduces the power for low data rate applications, the power saving capabilities of this approach is limited at high data rates. We have investigated an approach for reducing the power consumption at higher data rates, which also provides a small amount of resolve for the near/far problem associated with impulse-based radios. Our design uses a discrete power level for transmitting data, with no relation to the distance from the receiver.

By adjusting the amplitude of the pulse dynamically we can vary the emitted power and therefore, reduce the power consumption when in close proximity to the receiver. The approach involves the addition of extra taps to the power amplifier section of the pulse generator, potentially yielding many discrete pulse amplitude settings. As an example, Figure 3.15 shows a configuration with 3 additional sets of control taps with widths decreasing by 50% from set to set, for a total of 16 control taps, yielding 4 different possible pulse amplitudes when the 4 sets are used independently of each other; however, depending on the desired complexity of the control logic, one can use 4 or more transistors from different sets to generate many additional pulse amplitudes.

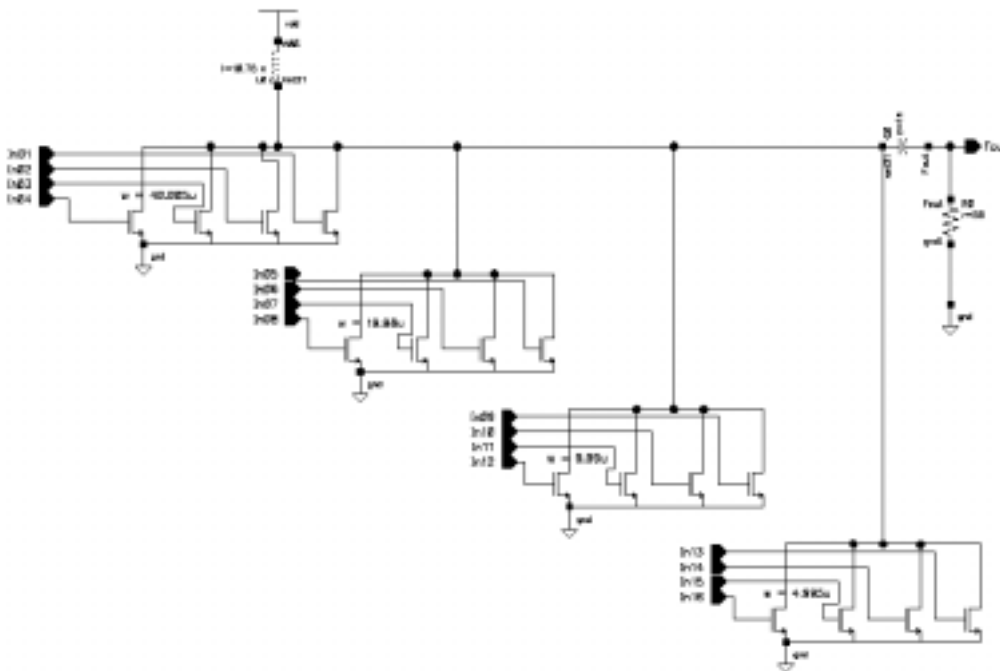


Figure 3.15: Example circuit for reducing power and varying amplitude

Power is saved when the transmitter is closer to the receiver. At any time, even though there are 16 control taps, there are only 2 control taps that are ever on in the idle state, while the other 12 control taps are grounded. Control logic is necessary to switch between each set of 4 transistors depending on the distance between the transmitter and receiver. This approach limits the pulses to certain predetermined amplitudes, but this solution is less complex than other approaches to solve the near-far problem. The pulses generated from initial simulations of this approach are shown in Figure 3.16.

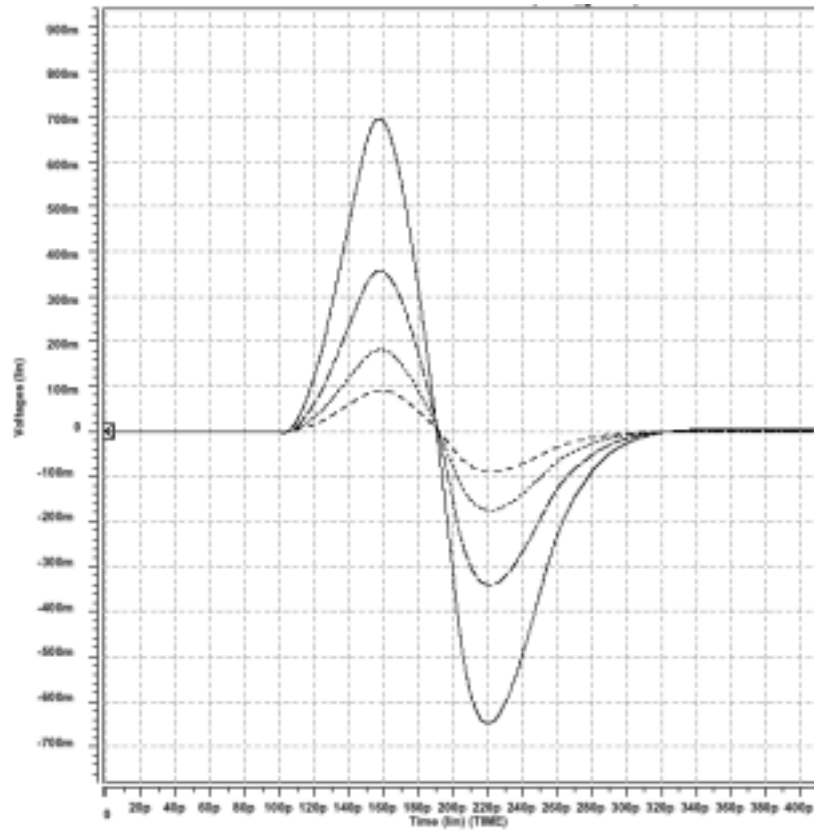


Figure 3.16: Generated Pulses with varying amplitude

The pulse amplitude is reduced by 50% each time when going through the four transistor sets, which would be expected since the width of the four transistors in each set is also reduced by 50%. Additionally, when the set of transistors with a width of $40\text{ }\mu\text{m}$ is used, the amplitude is about 700 mW with an average power dissipation of 79.9 mW. The other values of amplitude and power are summarized in Table 3.4.

Table 3.4: Summary of Scheme to Dynamically Varying Power

4T set	Power Consumed Generating Pulse (mW)	Peak Voltage of Generated Pulse (mV)
40 μm	79.9	700
20 μm	39.9	350
10 μm	20.0	180
5 μm	10.1	90

Just as with previous power saving schemes, this causes the pulse generator to generate spurious pulses when switching between the desired set of transistors, which is filtered out by the band pass filter.

3.5.2 Dynamically Varying Center Frequency

One concern with UWB systems is their co-existence with other devices in nearby or overlapping bands. One such band is at 5 GHz, reserved for 802.11a. Since the impulse based pulse generator we have designed spreads the pulse energy over a very large frequency range, there is the possibility of additional noise contributed to other systems like 802.11a. Therefore, in order to support co-existence and a multi-band impulse based approach we have considered how we can support such a scheme with our pulse generator.

We tested two methods of varying the center frequency of the generated pulse. In our design, the only way to vary the center frequency is to increase or decrease the delay between input transitions on the four input taps of the power amplifier. This delay is controlled only by the MCML delay elements. The delay of an MCML gate is expressed as

$$\text{Delay} = \frac{C \times \Delta V}{I} \quad (3.1)$$

where C is the load capacitance and ΔV is the MCML circuit's voltage swing [24]. The current I is controlled by the size of the RFN transistor and/or by the voltage applied to

the gate of the RFN transistor. Thus, we can either increase or decrease the current, thereby changing the center frequency by varying the voltage applied to the RFN transistor. Introducing additional RFN transistors, we are able to simplify the design by only requiring that VDD or GND be supplied rather than a varying voltage level. Through simulations we found that this achieved the best performance while varying the center frequency, and requires less complexity.

As an example, a pulse generator for a dual-band approach using a MCML inverter/buffer circuit is shown in Figure 3.17.

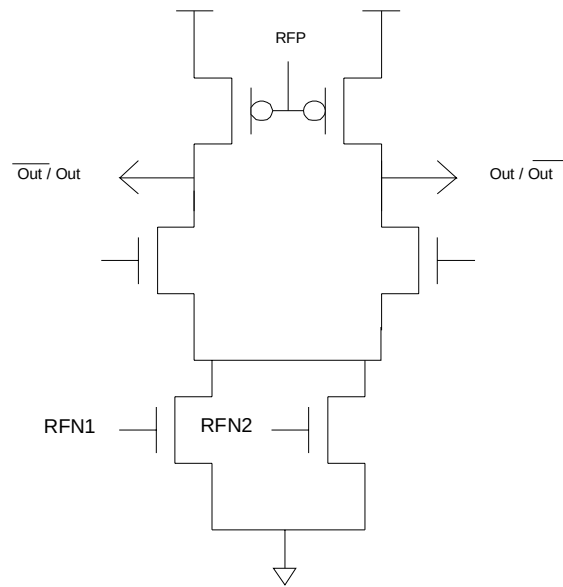


Figure 3.17: Example of MCML Circuit with 2 Transistors as Current Source

In this example, supporting a dual-band approach, the RFN1 transistor is sized, so that when RFN1 is turned on and the RFN2 transistor is turned off, the delay is set for a lower frequency band, below 5 GHz. Alternatively, if we desire to generate pulses in an upper frequency band, we can turn on both the RFN1 and RFN2 transistors to achieve less delay through the MCML delay element. RFN2 should be sized appropriately through simulation to achieve this additional center frequency.

Chapter 4

Design of a Rectified Cosine Generator

In this chapter, we extend the design of the previous chapter to show the versatility of our method for producing various shaped pulses. We have shown how a four-tap CMOS power amplifier can be used to generate very narrow pulses. By adding additional taps to the power amplifier, we can, in theory, produce any pulse shape; however, limitations exist due to the limited accuracy of simulation tools and also, process variation. We show the possible design of a rectified cosine generator, of which will become a more feasible option as CMOS technology advances in the next few years.

4.1 Target Multi-band System

The most basic multi-band structure is presented in Figure 2.10, involving a rectified cosine generator whose output is multiplied with each local oscillator in various mixers, followed by a multiplexor to select the current band. The proposed multi-band OFDM system, discussed in Chapter 2, could have as many as 15 subbands each with a bandwidth of 500 MHz, as proposed by Intel [12]. We base the specifications of our design on this proposed standard, requiring a continuous rectified cosine signal with a period of approximately 3.3 ns. A continuous rectified cosine signal is the same as the superposition of multiple Gaussian pulses. Thus, we first design a Gaussian pulse generator, and then control the generator to generate such pulses continuously.

4.2 Modifying the Impulse Based Pulse Generator

The pulse generator designed in the previous chapter was constructed using a 4-tap CMOS power amplifier. The pulse was generated by separating the pulse into 3 stages, based on the polarity of the slope and the magnitude of the slope. We were able to generate a 150 ps wide monocycle pulse with only 4 taps by using rise and fall times of the tap inputs. In order to generate a rectified cosine pulse with a pulse width of 3.3 ns

and using only 4 taps, we should control the rise and fall times of the inputs, so that they were are the desired pulse width, 1.15 ns. Precisely, setting the rise and fall times to 1.15 ns, considerably large amount of time by today's standards, is very difficult. In an initial attempt to generate this pulse, we use the exact same pulse generator and attempt to increase the input rise and fall times of the control tap inputs. Through simulations we find that it is impossible to generate a rectified signal with good fidelity using this strategy. Thus, we begin simulations to determine the best way of generating a rectified cosine pulse.

4.2.1 Adding Additional Taps

In order to determine the optimal number of taps for producing a cosine signal with the highest fidelity, we attempt to generate Gaussian pulses with different amounts of taps. We strip away the control logic from the previous design and simulate the inputs to the control taps. Shown in Figures 4.1 through 4.3 are the simulation results of generating a pulse with 2, 6, and 10 taps, the taps are sized to have symmetry, meaning there are at least two transistors which have the same width, one for both the negative and positive slopes of the pulse.

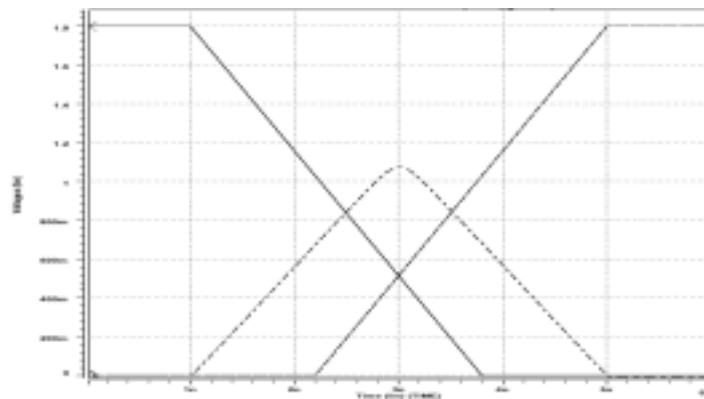


Figure 4.1: Pulse Generated using 2 taps

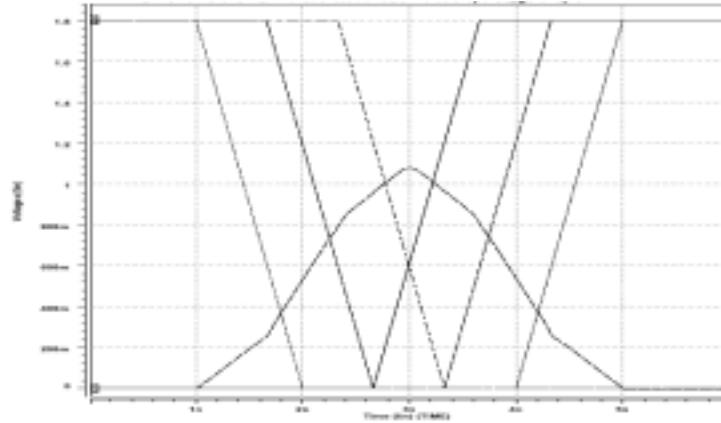


Figure 4.2: Pulse Generated using 6 taps

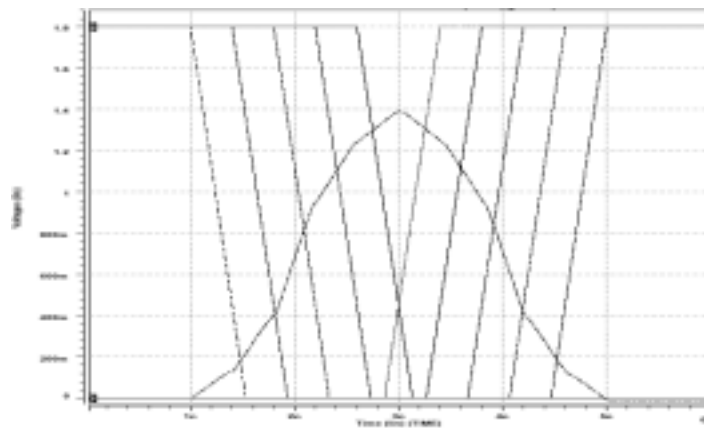


Figure 4.3: Pulse Generated using 10 taps

In order to generate a pulse that is 3.3 ns wide, the control tap inputs must have rise and fall times that are much larger than a typical value. With only 6 taps as shown above the rise and fall times must be about 0.55 ns, which is hard to precisely control using real inputs. If the rise and fall times were shorter, then the transitions in the pulse would happen too quickly, resulting in a very distorted pulse shape. We define a typical rise and fall time of an inverter given the current technology to be roughly 100 ps. The pulse shown below in Figure 4.3 shows the pulse that is generated by increasing the

number of taps to 10. Increasing the number of taps increases the circuit complexity, but yields a better shaped pulse and reduces the required rise and fall times of the tap inputs to about 0.33 ns, the smaller the rise and fall times the better in this case, as it is easier to control.

Since the rise and fall times of the inputs to the power amplifier determine the fidelity of the pulse generated, we determined the number of taps required to use typical rise and fall times. As stated previously, a more realistic rise and fall time for our technology, 0.18 μm , is about 100 ps, as found from simulating a ring oscillator. If the number of taps is based on an input transition time of 100 ps, we will need 33 different transition stages, for a pulse width of 3.3 ns.

4.2.2 Calculating Transistor sizes from slopes

In an attempt to generate a more accurate monocycle pulse than in previous attempts using our pulse generator, we develop a 30-tap pulse generator. The size of a transistor in this type of amplifier is directly related to the magnitude of the change in current at the output. Thus, the size is directly related to the magnitude of the slope of the output. We size the 30 transistors by estimating the slope at 33 different locations along the pulse, evenly spaced in time. Shown below in Table 4.1 is a table that summarizes the slopes and shows the transistor sizes that we will use. The transistor sizes are normalized to the smallest slope, which corresponds to the smallest available width, 270 nm. The larger the transistor, the greater the slope will be at the output for a given transition on the input of the transistor. If larger amplitude at the output is desired, the size of the transistors can easily be scaled, thus we base this design on the smallest transistors.

Transistion	Time (ns)	Slope at Time	Slope relative to smallest slope	Transistor Size Needed (nm)
0	0.00	0.0000000	0.0000	0.00000
1	0.10	0.1950903	1.0000	270.00000
2	0.20	0.3826834	1.9616	529.62405
3	0.30	0.5555702	2.8478	768.89495
4	0.40	0.7071068	3.6245	978.61764
5	0.50	0.8314696	4.2620	1150.73261
6	0.60	0.9238795	4.7357	1278.62557
7	0.70	0.9807853	5.0273	1357.38166
8	0.80	1.0000000	5.1258	1383.97434
9	0.90	0.9807853	5.0273	1357.38166
10	1.00	0.9238795	4.7357	1278.62557
11	1.10	0.8314696	4.2620	1150.73261
12	1.20	0.7071068	3.6245	978.61764
13	1.30	0.5555702	2.8478	768.89495
14	1.40	0.3826834	1.9616	529.62405
15	1.50	0.1950903	1.0000	270.00000
16	1.60	0.0000000	0.0000	0.00000
17	1.70	0.1950903	1.0000	270.00000
18	1.80	0.3826834	1.9616	529.62405
19	1.90	0.5555702	2.8478	768.89495
20	2.00	0.7071068	3.6245	978.61764
21	2.10	0.8314696	4.2620	1150.73261
22	2.20	0.9238795	4.7357	1278.62557
23	2.30	0.9807853	5.0273	1357.38166
24	2.40	1.0000000	5.1258	1383.97434
25	2.50	0.9807853	5.0273	1357.38166
26	2.60	0.9238795	4.7357	1278.62557
27	2.70	0.8314696	4.2620	1150.73261
28	2.80	0.7071068	3.6245	978.61764
29	2.90	0.5555702	2.8478	768.89495
30	3.00	0.3826834	1.9616	529.62405
31	3.10	0.1950903	1.0000	270.00000
32	3.20	0.0000000	0.0000	0.00000
			Total Transistor Size	28103.4546

Table 4.1: Computing the Transistor Sizes for a 30 tap amplifier

We simulate the 30-tap circuit described here using simulated inputs with a transition time of 100ns and find that a more accurate Gaussian pulse is generated, as would be expected. Shown in Figure 4.4 is the output of the pulse generator in this initial simulation.

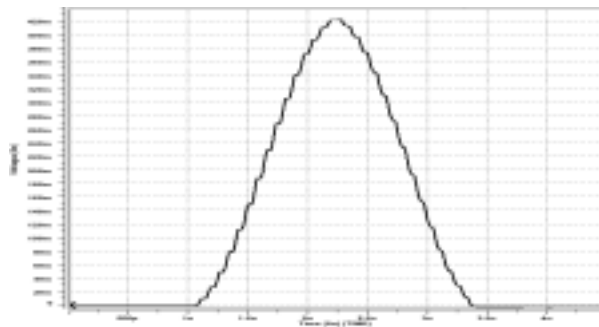


Figure 4.4: Pulse Generated from 30-tap amplifier

4.3 Rectified Cosine Generator Control Logic

Naturally, a 30-tap generator would seem to have complex control logic; however since we are only generating a single type of pulse with a fixed amplitude and fixed period the controlling circuitry can be simplified.

4.3.1 Control Logic Requirements

In our previous design, we used a delay element, transmission gates and D-flip flops to control the precise delayed switching between taps, but the specifications are much more relaxed. We need only a delay of 100 ps between each input transition, and there are only two possible ways in which the input needs to be ordered to generate continuous pulses. The 30 transistors can be divided into two sections, one set of 15 taps has logic '0' applied to the input, while the other set has logic '1' applied to the inputs in the idle state. The control taps with logic '1' applied to their inputs have logic '0' applied to their inputs one after another with a delay of 100 ns between each transition, generating the first half of the pulse with a positive slope. Then the same is done for the second set of taps, with logic '0' applied to their inputs, generating the second half of the pulse with a negative slope. In order to generate the next pulse immediately following the first, the inputs to the second set will now have to transition first, followed by the first set.

4.3.2 Control Logic Circuit

Control logic was developed to perform the switching described above. The control circuit consists of a 62-inverter chain and four transmission gates. To meet the 100ps delay requirement between each control tap input transition, the size of the inverters in the inverter chain were size to 1.89 μm and 990 nm for P-FETS and N-FETS, respectively. The entire control logic is designed such that the entire circuit only requires three inputs. The inverter chain provides the necessary delayed clock signal to the 30 control taps of the power amplifier, while the transmission gates provide the ability to generate continuous pulses. Without the transmissions gates, continuous positive and

negative pulses would be generated. The transmissions gates are used to control where the clock enters the 62-inverter chain and the path of the delayed clock signal through the chain.

At first, the clock signal enters through the first inverter and travels through all inverters after each delay, generating the desired positive pulse. After the first pulse is generated, the transmission gates are set so that the clock signal enters through the 31st inverter and travels through the end of the chain, and then back to the beginning of the inverter chain to the 30th inverter. This process continues, alternating the path of the clock, generating continuous positive pulses.

4.4 Power Reduction

Although the power requirements for applications of a multi-band approach, mainly targeting home networks, are more relaxed than in our previous design, targeting RFID applications, power is always a concern. Even if battery life is not a driving force in a design, other factors such as packaging and cooling can add a considerable amount of cost to a design if too much power is consumed.

In this type of circuit, in which all components are used to continuously generate the same pulse over and over again; there are few areas of the design that can be exploited to reduce the power. As in the previous design, the main source of power dissipation is from the power amplifier portion of the circuit, in which there is a large amount of constant current flowing from the source to the ground. Thus, an effective way to achieve significant power savings is to turn this portion of the circuit off when it is not being used; however, this portion of the circuit is always being used. Just as in the previous design, this section of the generator can be turned off. Therefore, power savings can be determined by whether the generator needs to continuously generate pulses, or if it can be turned off for some duration between transmissions.

4.5 Band pass Filtering

As one can see from the pulse generated in Figure 4.4, the pulse shape is not perfect; it appears more as the output from an ADC or a sample hold circuit. The shape of this pulse is important to the overall performance of the systems, as it is used as an envelope for the transmitted signal. It is believe that this type of rectified generator requires a bandpass filter at the output. Future simulations are necessary to determine the specifications of the filter and are left to future research.

Chapter 5

Simulation Results

In this chapter, we show simulation results of our designs described in the previous two chapters. We examine the fidelity of the pulses generated from each design in terms of the pulse shape and the respective frequency spectrum. Additionally, characteristics such as the static and dynamic power dissipation, and area are examined. Lastly, we review the FCC regulations in terms of the pulses generated from our pulse generators.

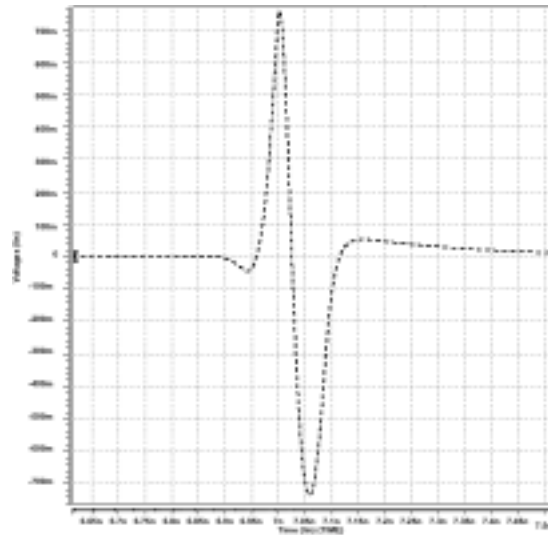
5.1 Simulation Environment

All of our designs were constructed in Cadence at the transistor-level targeting TSMC 0.18 μm CMOS technology. The netlists extracted using a Cadence tool were used to perform simulations in Hspice. Upon extraction from Cadence, modifications to the designs were made on the Hspice netlists. In addition, all waveform simulations were graphically displayed using AvanWaves.

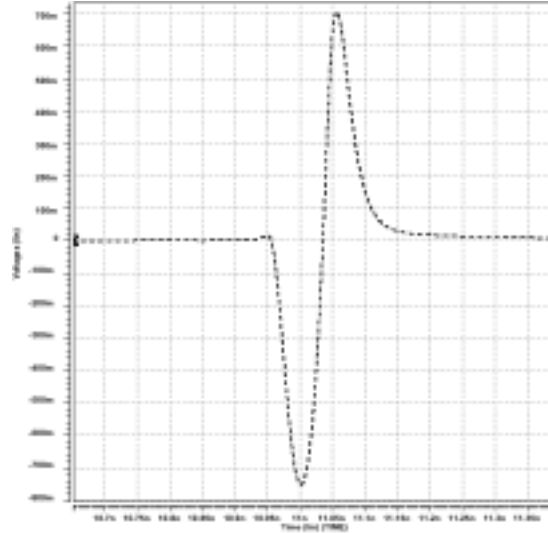
5.2 UWB Pulse Generator Simulation Results

5.2.1 Simulated Gaussian Pulses

The pulse generator described in Chapter 3 generates Gaussian monocycle pulses and can support a variety of modulation schemes. The fidelity of the generated pulses has a significant impact on the overall performance of the entire system. The generated Gaussian monocycle pulses are shown in Figures 5.1.



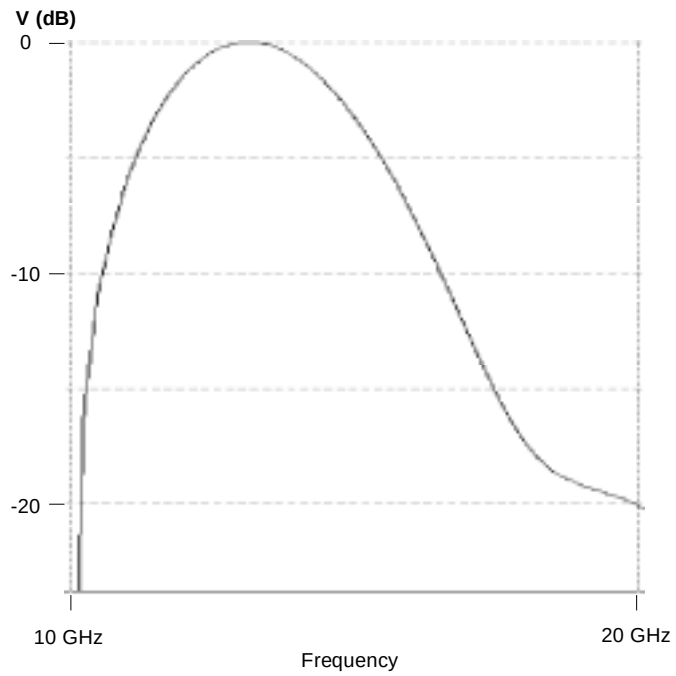
(a) Positive Gaussian Monocycle



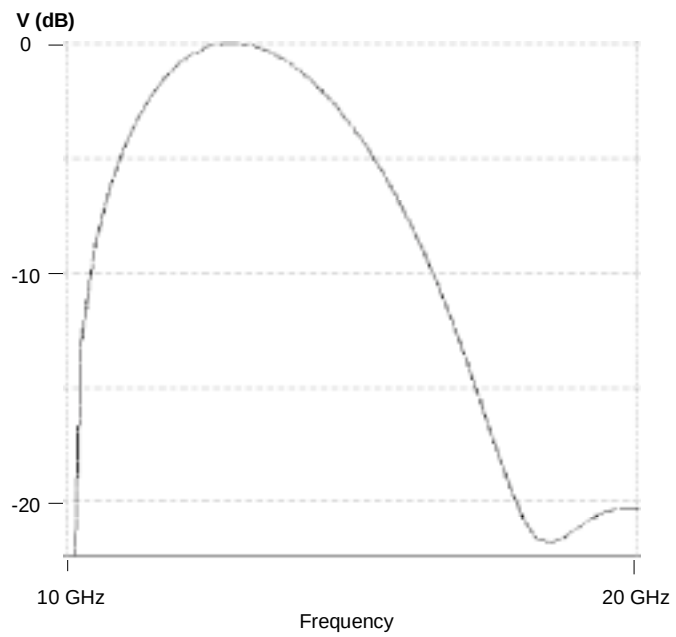
(b) Negative Gaussian Monocycle

Figure 5.1: Generated Gaussian Monocycle Pulses

The pulses shown above have a peak-to-peak voltage of approximately 1.45 volts, resulting in a peak power of 10.5 mW delivered to a 50 Ω load. In order to determine the center frequency of the generated pulses, we examined the frequency spectrum of each monocycle pulse. The frequency spectrums of the pulses shown above are shown in Figure 5.2. The frequency spectrums plots are shown for each pulse from DC to 20 GHZ.



(a) Frequency Spectrum of Positive Gaussian Monocycle Pulse



(b) Frequency Spectrum of Negative Gaussian Monocycle Pulse

Figure 5.2: Frequency Spectrum of Generated Pulses

5.2.2 FCC Rules Revisited scheme

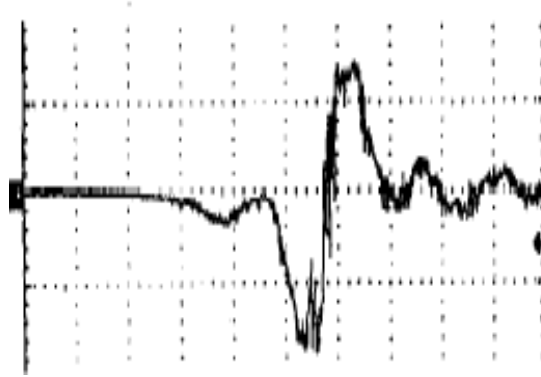
As described in Chapter 2, the FCC has defined a UWB pulse as having a -10 dB bandwidth between 3.1 and 10.6 GHz, while occupying a bandwidth of at least 500 MHz and meeting the spectrum mask. From the results of the frequency analysis shown in Figure 5.2, the center frequencies of each pulse were found to be 6.5 GHz and 6.0 GHz for positive and negative pulses, respectively. Thus, the center frequency meets that FCC requirement; however, the simulations verified, as expected, that the bandwidth of the pulses does not meet FCC regulations as summarized in Table 5.1. The table shows that the regulations are not met, since the required attenuation is not met at 3.1 and 10.6 GHz. So, our pulse generator requires a small amount of filtering with minimal distortion of the wideband pulse.

Table 5.1: Frequency Spectrum Summary

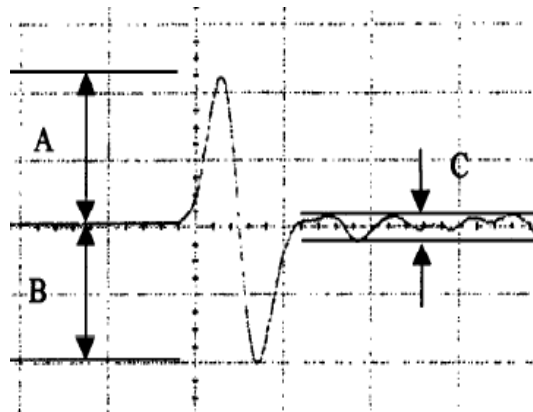
	FCC Regulations	Positive Pulse	Negative Pulse
<i>Low -10dB Cutoff Freq.</i>	3.1 GHz	1.14 GHz	0.857 GHz
<i>High -10dB Cutoff Freq.</i>	10.6 GHz	13.1 GHz	12.9 GHz
<i>Bandwidth</i>	> 500 MHz < 10.5 GHz	11.96 GHz	12.043 GHz

5.2.3 Comparing Alternative Pulse Generation

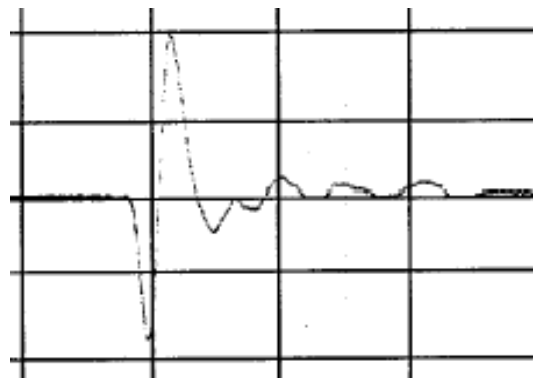
Here we show the output of a few alternative pulse generators in order to compare the difference between our approach and others. Figure 5.3 depicts the output of the pulse generators discussed in Chapter 2.



(a) Pulse Generation [29]



(b) Pulse Generated [30]



(c) Pulse Generated [31]

Figure 5.3: Results of Alternative Pulse Generators

In most papers, the performance of the pulse generator is only characterized by the shape of the pulse at the output, not in terms of power, area, or frequency spectrum. Thus, we can only compare the different designs based on the appearance of the generated pulse shape and the technology used. When comparing the shape of the pulses in Figures 5.1 and 5.3 one can notice that the output of our pulse generator is comparable to other designs in terms of pulse shape. It can be seen that our design produces a pulse in which the + and – peak voltages match most accurately. Additionally, our design has minimal ringing at the output of the pulse generator, while other methods have a considerable amount of ringing.

5.2.4 Area Estimation

The area required for our design was estimated by summing the widths and lengths of the 240 transistors in the design. Since the RF choke will be implemented as a high-Q off-chip inductor, we only focus on the transistor area. The relative size of each section of the pulse generator is illustrated in the Figure 5.4. The sum of all the widths and lengths of each device was found to be 887.35 μm and 43.02 μm , respectively. Without considering interconnections, the total area of the design is approximately 0.038169 mm^2 . So our design has requires a small amount of area and cost.

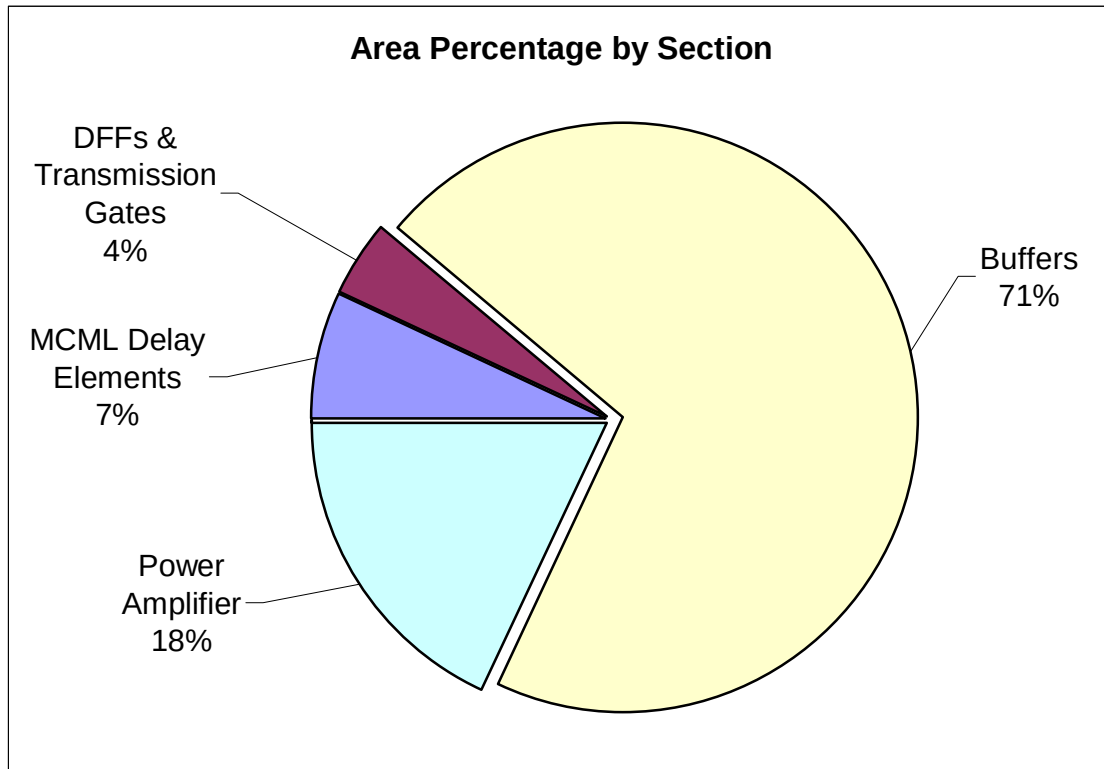


Figure 5.4: Pulse Generator Area Breakdown

5.2.5 Power Estimation

The power dissipation of our pulse generator was estimated through HSpice simulations for both static and dynamic power dissipation. The static power was estimated in terms of two idle states. The first static state we considered is when the pulse generator is completely off, with no direct paths from VDD to GND. The second static state is when the MCML delay element and power amplifier circuit are on; both circuits have an open path from VDD to GND. We estimated dynamic power as the average of three pulse-generating states. In our power saving scheme the pulse generator must first be turned on, generating a spurious pulse, this is the first state of dynamic power dissipation. The second portion of dynamic power is consumed when a real pulse is generated, and the last portion of dynamic power is consumed when the generator is turned off, generating another spurious pulse. Figure 5.5 illustrates all static and

dynamic power dissipation. One should note the drastic difference in power consumed between the states when a pulse is generated and when the pulse generator is turned completely off. If the pulse generator is always turned on, over 84 mW of power is consumed continuously.

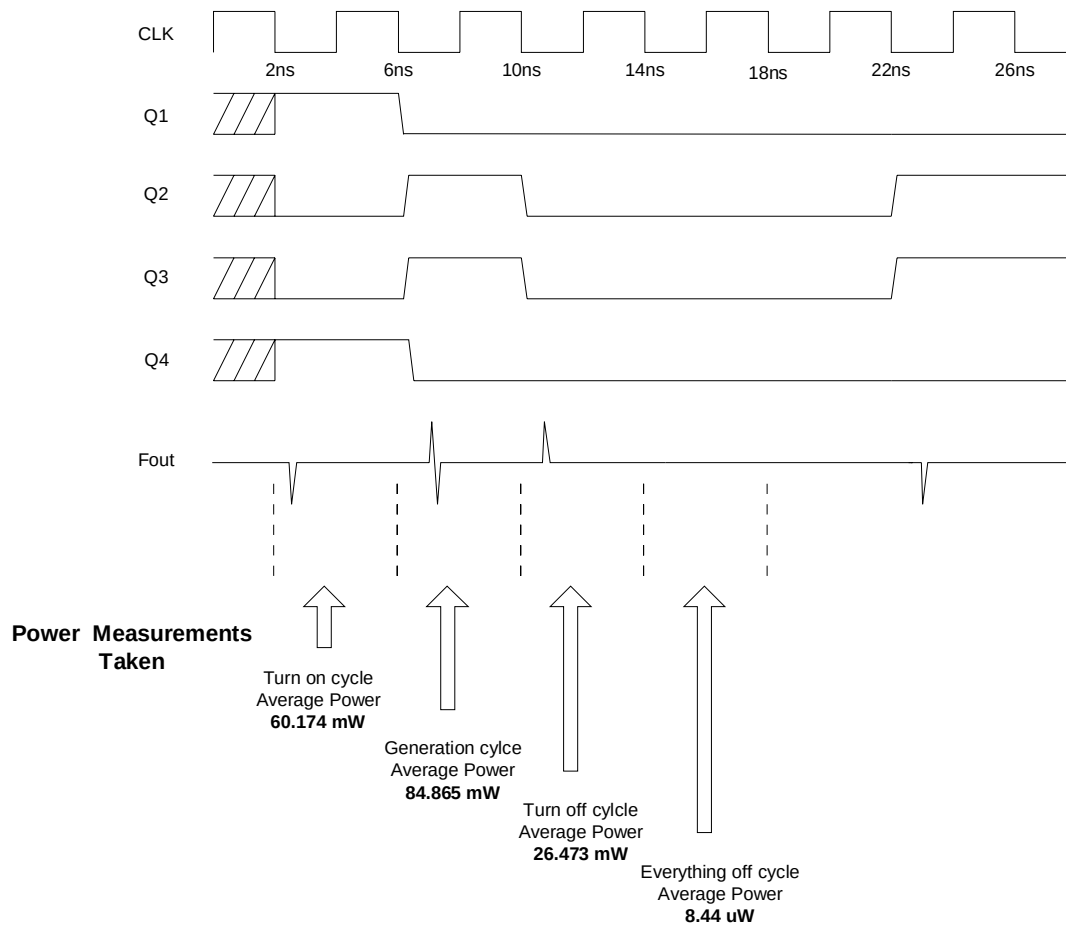


Figure 5.5: Summary of Power Dissipation

As discussed in Chapter 3, our power saving scheme is effective for low data rates. However, as the data rate increases, the amount of time that the pulse generator is on also increases, and thus consumes more power. Figure 5.6 illustrates the relationship between power dissipation and the data rate using our power saving scheme.

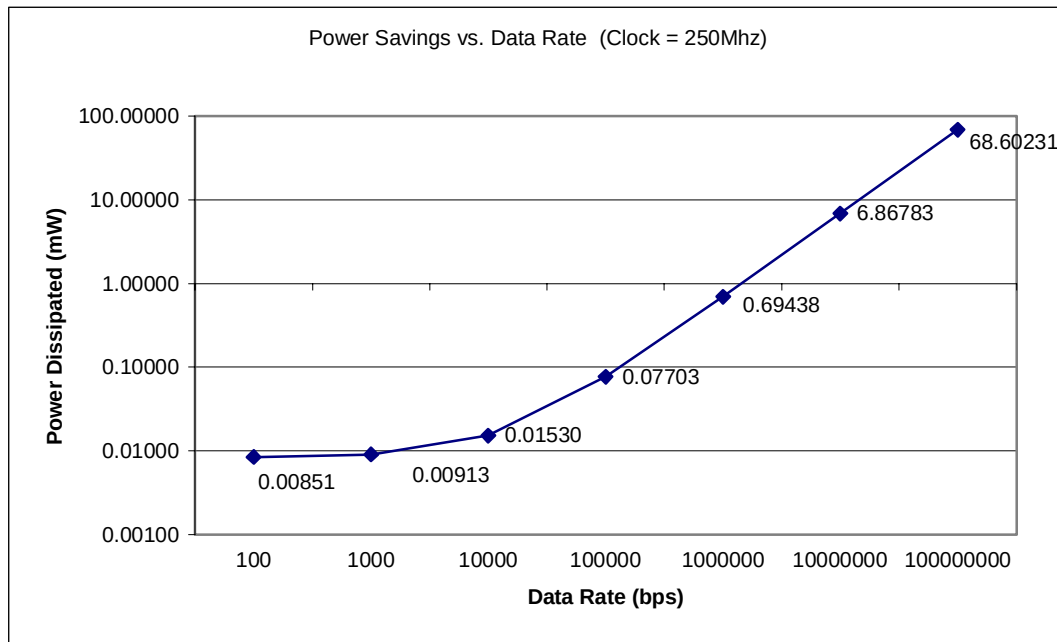


Figure 5.6: Power Dissipation vs. Data Rate (Log Scale)

From Figure 5.4, we have shown that the amount of power dissipated increases substantially at higher data rates. In addition to the data rate, the effectiveness of our power saving scheme also depends on the clock frequency. In most digital circuits, as the clock frequency increases, more power is dissipated; however the opposite is true in our design. The higher the clock frequency, the faster the pulse generator can generate a pulse and turns off again, and therefore consume less power. When a clock with a low frequency is used, the pulse generator is on consuming a large amount of power, while it is waiting for the next clock. Figure 5.7 illustrates the relationship between power and the clock frequency.

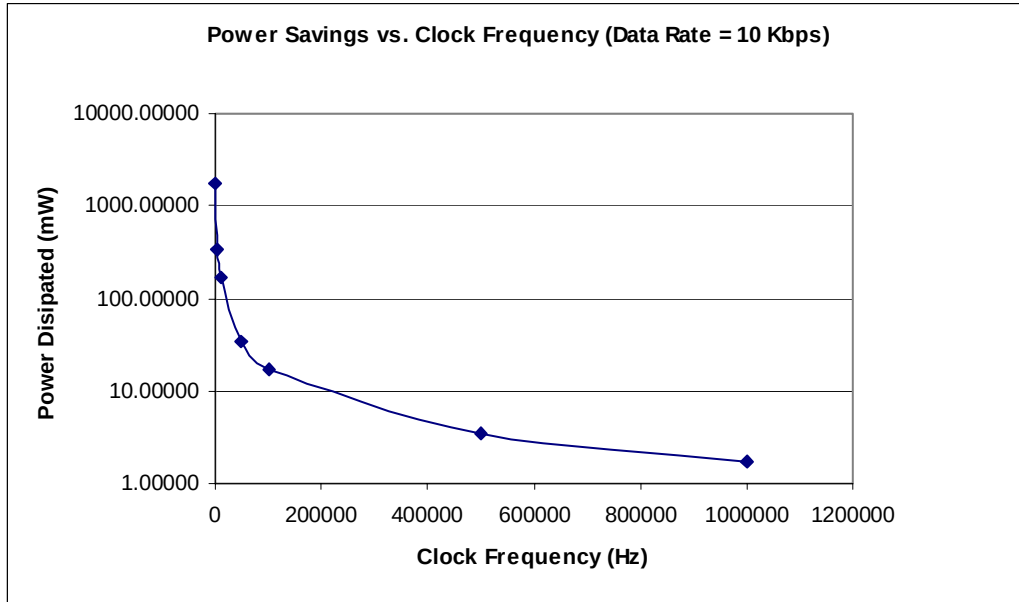
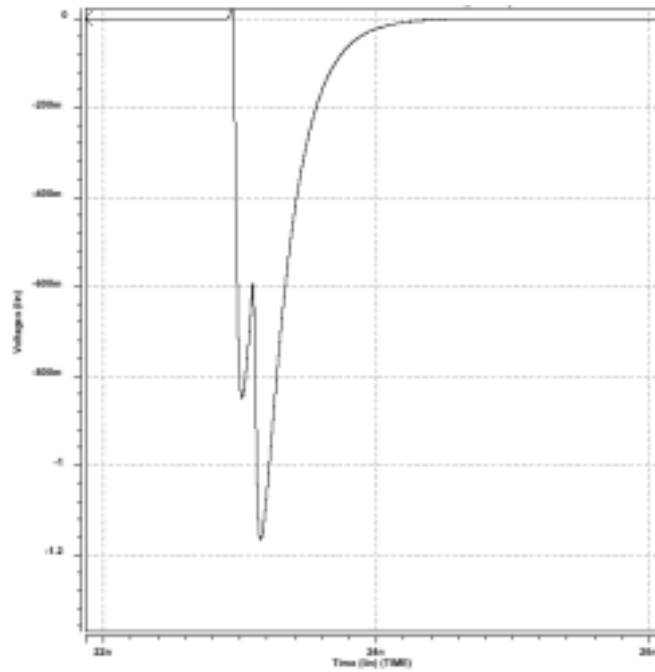


Figure 5.7: Power Dissipation vs. Clock Frequency

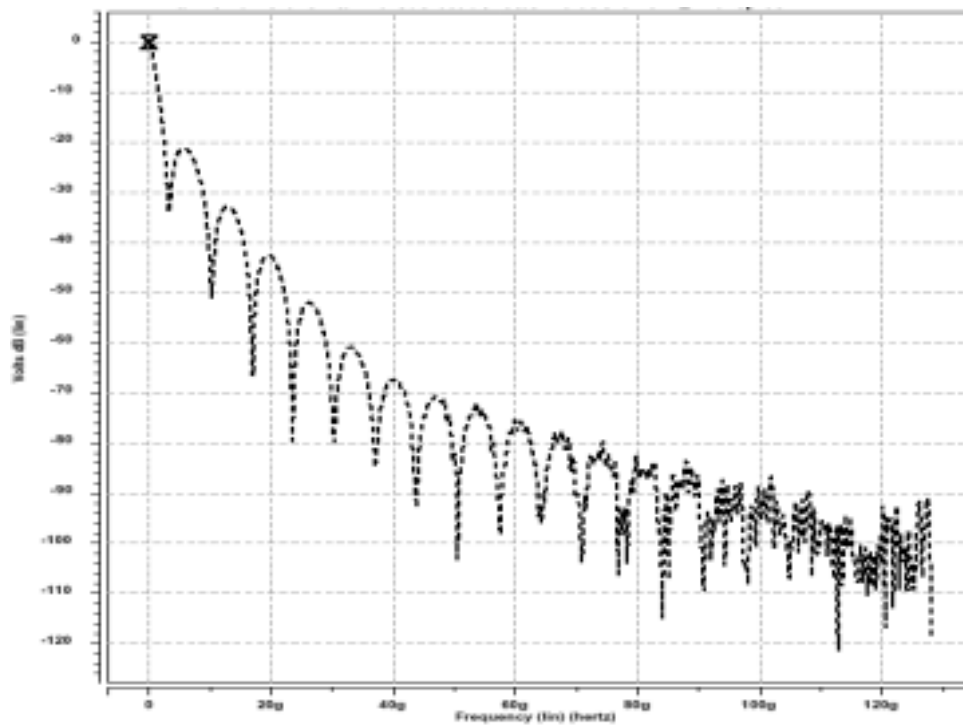
We can see from the figure above that the power is largely dependent on the clock frequency. Ideally, it is better to operate the pulse generator at its maximum clock frequency to reduce power. Through simulations we determined the maximum clock frequency to be around 750 MHz. The minimum pulse repetition interval (PRI) is approximately 1.33 ns for the maximum clock frequency. As technology scales down, the minimum PRI for this type of design will decrease.

5.2.6 Frequency Spectrum of Spurious Pulse

In Chapter 3, we stated that the spurious pulses generated when the pulse generator is turned on and off would be removed by a bandpass filter following the pulse generator. This claim is verified by performing frequency spectrum simulations during the generation of these spurious pulses. The generated spurious pulses are shown in Figures 5.5 and 5.6 along with their respective frequency spectrums.

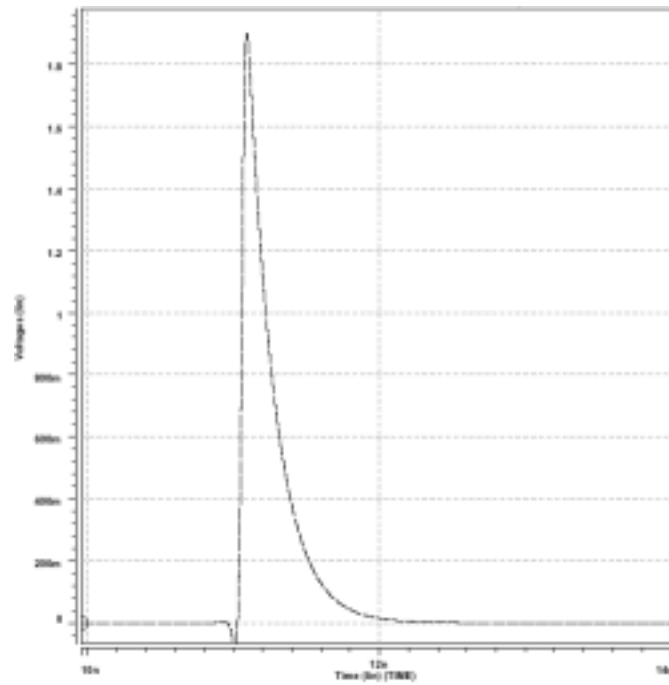


(a) Spurious Pulse Generated

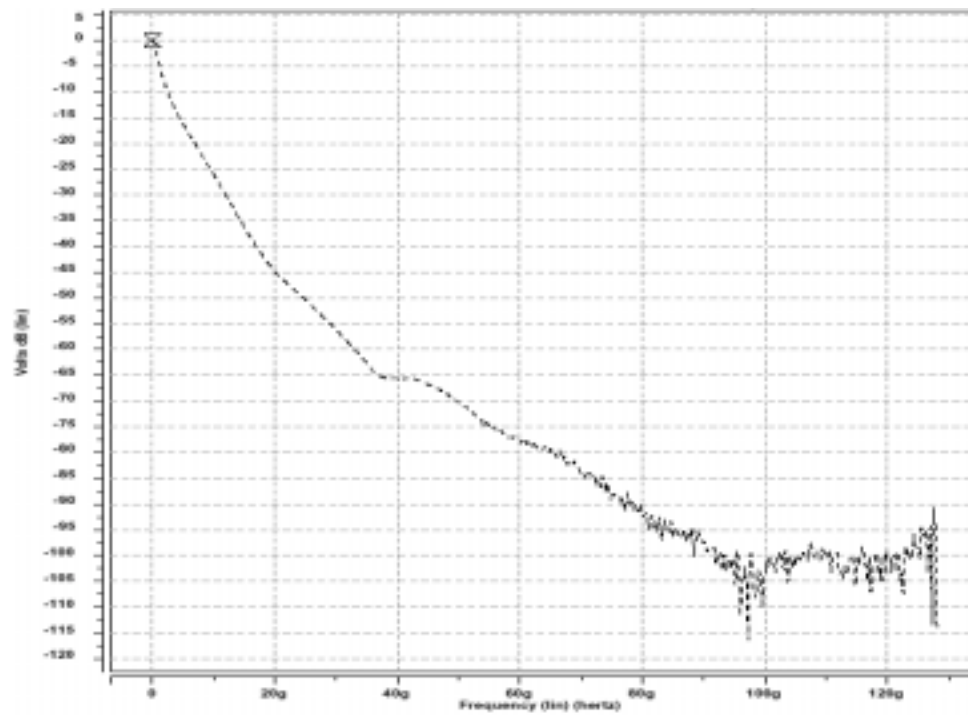


(b) Frequency Spectrum

Figure 5.8: “Turn on” Spurious Pulse and Frequency Spectrum



(a) Spurious Pulse Generated



(b) Frequency Spectrum

Figure 5.9: “Turn off” Spurious Pulse and Frequency Spectrum

From the spectrum analysis shown in Figures 5.8 and 5.9, we can see that the majority of the energy in the spurious pulses is concentrated around the DC frequency. This verifies that all spuriously generated pulses can be filtered out in a bandpass filter that follows the pulse generator.

5.3 Simulation Results of the Multi-band Rectified Cosine Generator

5.3.1 Simulated Rectified Cosine

The design of a rectified cosine generator, capable of generating continuous Gaussian pulses, was discussed in Chapter 4. Figure 5.10 shows the waveform generated from this design. There were two simulated inputs to the circuit, a 300 MHz clock, and 2 control inputs to provide the switching necessary to generate continuous pulses.

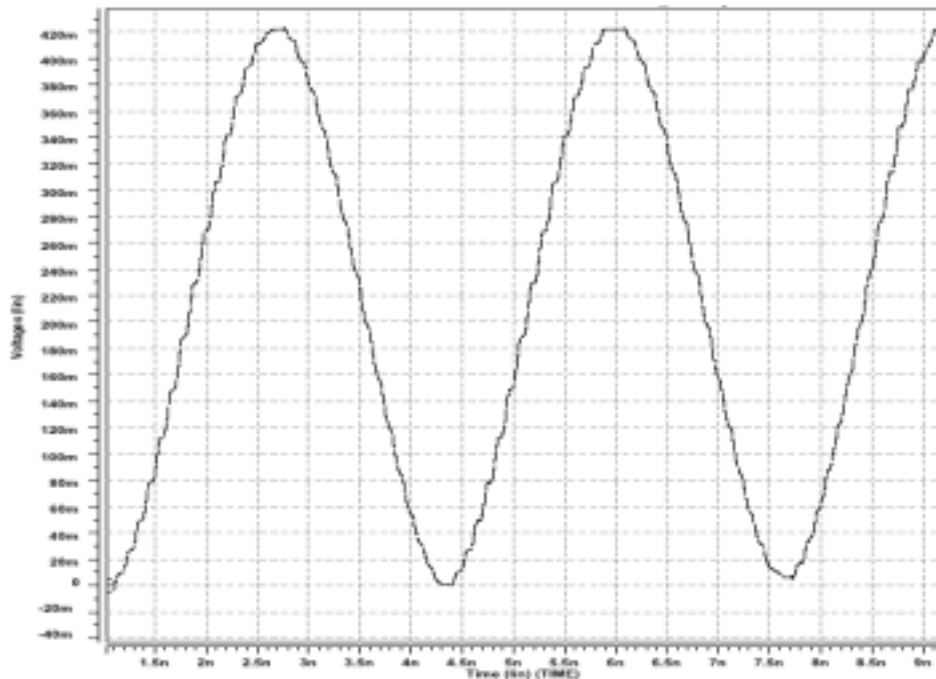


Figure 5.10: Generated Rectified Cosine Waveform

In order to illustrate the accuracy of the generated rectified cosine waveform, Figure 5.11 shows a generated waveform along with an ideal rectified cosine waveform. The two waveforms on top of each other show that the difference between the two waveforms is small.

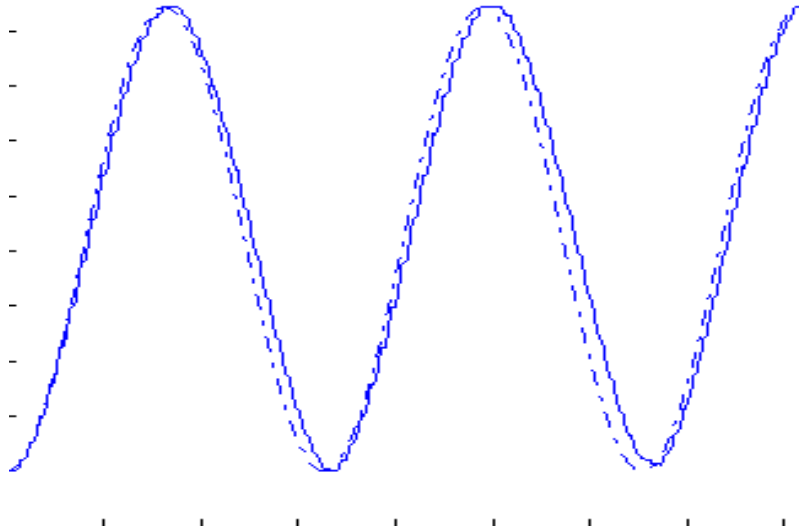


Figure 5.11: Ideal vs. Generated Rectified Waveform

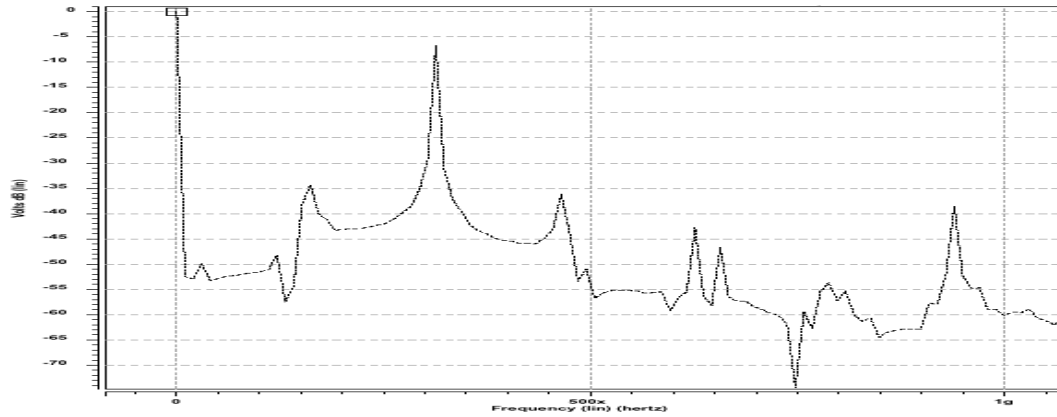
--- Ideal, — Generated

As mentioned in Chapter 4, the design was scaled to use the smallest device sizes for this initial design; however, the amplitude of the waveform can easily be increased by scaling all of the transistors in the design appropriately. The waveform generated using the smallest device sizes has a peak-to-peak voltage of approximately 0.43 V. When comparing the two waveforms shown in Figure 5.11 the RMS error of the generated signal was found to be 0.0230 V.

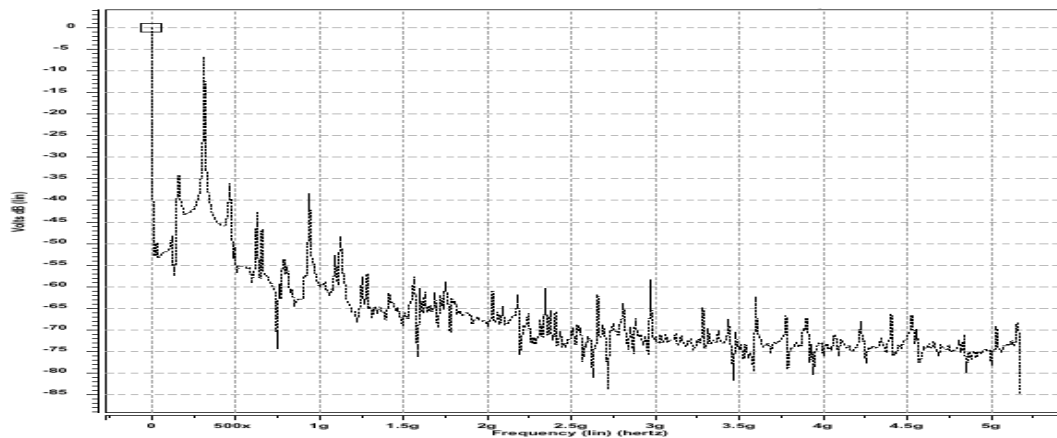
5.3.2 FCC Rules Revisited

The FCC requires that a UWB signal have a minimum bandwidth of 500 MHz. Figure 5.12 depicts a plot of the frequency spectrum of the generated cosine signal. From the frequency spectrum analysis, the center frequency of the generated cosine signal was

found to be 312 MHz. So this signal will provide an envelope necessary to meet the FCCs minimum bandwidth requirements.



(a) Zoomed FFT Plot from 0 to 1 GHz



(b) FFT Plot from 0 to 5 GHz

Figure 5.12: Frequency Spectrum of Rectified Cosine Signal

5.3.3 Power Estimation

The power dissipation of our rectified cosine generated was characterized in terms of the average power dissipation over the time interval in which a single rectified cosine pulse was generated. Since the circuit runs continuously, there is no need to calculate static and dynamic power dissipation separately. The average power dissipation

estimated through simulations in HSpice was found to be 9.29 mW. If we separate the control logic from the power amplifier portion of the generator, we find that the control circuitry consumes 3.28 mW on average, while the 30-tap power amplifier consumes 6.01 mW on average.

5.3.4 Area Estimation

The area required for our design was estimated, as done in the previous design, by summing the widths and lengths of the 160 transistors in this design. The relative area required for each section of the rectified cosine generator is illustrated in the Figure 5.13. The sum of all the widths and lengths of each device was found to be 215.370 μm and 43.74 μm , respectively. This gives an area of approximately 0.00942 mm^2 . As seen in the previous design, this pulse generation approach requires a small amount of area, and thus, low cost.

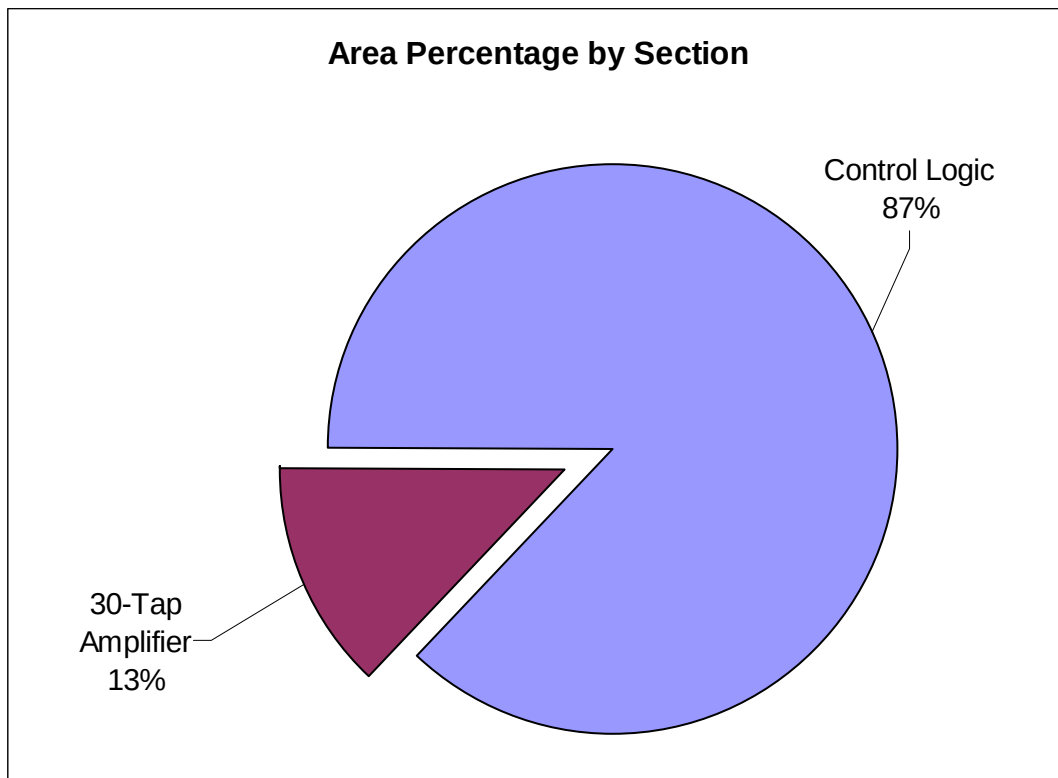


Figure 5.13: Rectified Cosine Generator Area Breakdown

Chapter 6

Conclusion

Ultra-Wideband technologies are at the forefront of wireless communications, with the possibility to provide higher data rate wireless solutions than have ever been realized before. In addition to high data rate applications, UWB technologies have the potential to provide low cost and low data rate solutions for many applications. Whether it is a low or high data rate application, the possibilities of wireless devices using UWB technology are unlimited.

In this thesis we have presented the design of a Gaussian pulse generator and a rectified cosine generator, targeting both low and high data rate applications. The design for both circuits was based on a single tap CMOS power amplifier, which we extended to several taps in order to shape the generated pulse. The objective of our UWB pulse generator design was to examine the ability to create a versatile CMOS based solution, while yielding a circuit which had low complexity, low power consumption, and low cost. The objective of our rectified cosine generator design was to create a CMOS based, low cost cosine generator, and to show how a multi-tap CMOS amplifier can be used to generate various pulse shapes.

Our pulse generator is capable of producing Gaussian monocycle pulses with a center frequency of approximately 6 GHz. We showed that the pulses generated have good fidelity when compared to other pulse generators. Additionally, we developed a power saving scheme, which can significantly reduce the power by turning the pulse generator off while it is not active. We examined the versatility of our design by describing methods to support dynamically varying center frequencies, which supports co-existence. Additionally, we discussed how we could achieve dynamically varying output power levels, which further reduces the power consumptions and alleviates the near/far problem associated with impulse-based systems. The simple CMOS circuit used to create the pulse generator is inherently low in cost, and supports a single chip transmitter solution.

We extended the 4-tap pulse generator design to construct a 30-tap rectified cosine generator. The rectified cosine generator was first designed to generate a single rectified cosine pulse. Then, a control circuit was introduced to generate continuous pulses, accurately producing a raised cosine waveform. Like the pulse generator, the rectified cosine generator provides a low cost and low complexity CMOS solution.

In summary, we presented a new approach to generating and shaping pulses for UWB applications. Our pulse generator is suitable for many RFID applications, as well as military applications such as ground penetrating radars and see-through-wall radar. Many RFID applications require extremely low power and low cost chips, making CMOS technology an ideal candidate. This thesis has shown a possible CMOS solution that is capable of meeting the wide bandwidth requirements of UWB systems by exploiting the slope transitions in a pulse. We believe that our design is a feasible solution for a UWB pulse generator, offering low area, low cost, and low power.

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Vita

Kevin Matthew Marsden was born in Fairfax, Virginia on October 22, 1980. He graduated *magna cum laude* from Virginia Tech in Blacksburg, Virginia in December 2002 with a Bachelor of Science degree in Computer Engineering. Before graduation he obtained a year of co-op experience at Lockheed Martin Federal Systems in Manassas, Virginia. As an undergraduate he was in the B.S./M.S. program at Virginia Tech where he completed half of his graduate course work before graduating with his undergraduate degree. As a graduate student, we worked under Dr. Dong S. Ha at the Virginia Tech for VLSI Telecommunications (VTVT) Laboratory and studied low-power VLSI design and digital UWB pulse generators.