

The Modeling and Control of a Cascaded-Multilevel Converter-Based STATCOM

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(ABSTRACT)

This dissertation is dedicated to a comprehensive study of static synchronous compensator (STATCOM) systems utilizing cascaded-multilevel converters (CMCs). Among flexible AC transmission system (FACTS) controllers, the STATCOM has shown feasibility in terms of cost-effectiveness in a wide range of problem-solving abilities from transmission to distribution levels. Referring to the literature reviews, the CMC with separated DC capacitors is clearly the most feasible topology for use as a power converter in the STATCOM applications. The controls for the CMC-based STATCOM were, however, very complicated. The intricate control design was begun without well-defined system transfer functions. The control compensators were, therefore, randomly selected. The stability of the system was achieved by trial and error processes, which were time-consuming and ineffective. To be able to operate in a high-voltage application, a large number of DC capacitors are utilized in a CMC-based STATCOM. All DC capacitor voltages must be balanced in order to avoid over-voltages on any particular link. Not only do these uneven DC voltages introduce voltage stress on the semiconductor switches, but they also lower the quality of the synthesized output waveforms of the converter. Previous researches into DC capacitor voltage-balancing techniques were very straightforward, in that individual voltage compensators were added into the main control loop. However, the compensator design for these individual loops is very problematic because of the complexity of the voltage-loop transfer functions. Basically, the trial and error technique again provides the simplest way to achieve acceptable compensators. Moreover, the greater number of voltage levels, the more complex the control design, and the main controller must perform all of the feedback control procedures. As a result, this approach potentially reduces the reliability of the controller.

The goal of this dissertation is to achieve high-performance, reliable, flexible, cost-effective power stages and controllers for the CMC-based STATCOM. Major contributions are addressed

as follows: 1) optimized design for the CMC-based STATCOM power stages and passive components, 2) accurate models of the CMC for reactive power compensations in both ABC and DQ0 coordinates, 3) an effective decoupling power control technique, 4) DC-link balancing strategies; and 5) improvements in the CMC topology.

To enhance the modularity and output voltage of the CMC, the high-switching-frequency, high-power H-bridge building block (HBBB) and the optimized design for its power stage and snubber circuits are first proposed. The high-switching-frequency feature is achieved by utilizing the Virginia Tech-patented emitter turn-off (ETO) thyristor. Three high-power HBBB prototypes were implemented, and their performance was experimentally verified.

To simplify the control system design, well-defined models of the CMC in both ABC and DQ0 coordinates are proposed. The proposed models are for the CMC with any number of voltage levels. The key system transfer functions are achieved and used in the control design processes. To achieve independent power control capability, the control technique, called the decoupling power control, is proposed. By applying this control technique, real and reactive power components can be controlled separately.

In order to balance the DC capacitor voltages, a new, effective pulse width modulation (PWM) technique, which is suitable for any number of H-bridge converters, is proposed. The proposed cascaded PWM algorithm can be practically realized into the field programmable gate arrays (FPGA), and its complexity is not affected by the number of voltage levels. In addition, the complexity of the main controller, which is essentially based on the digital signal processor (DSP), is no longer a function of the number of the output voltage levels. The basic structure of the cascaded PWM is modular, which, in general, enhances the modularity of the CMC power stages.

With the combination of the decoupling power control and the cascaded PWM, a CMC with any number of voltage levels can be simply modeled as a three-level cascaded converter, which is the simplest topology to deal with. This significantly simplifies and optimizes the control design process. To verify the accuracy of the proposed models and the performance of the control system for the CMC-based STATCOM, a low-power, seven-level cascaded-based

STATCOM hardware prototype is implemented. The key control procedures are performed by a main controller, which consists of a DSP and an FPGA. The simulation and experimental results indicate the superior performance of the proposed control system, as well as the precision of the proposed models.

To

My Mother and Father

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Chapter 1 INTRODUCTION AND LITERATURE REVIEWS

1.1 Overview

In recent years, major transformations have been introduced into the structure of electrical power utilities to improve efficiency in the operation of the power system networks by deregulating the industries and opening it to their private competitors. This global trend and similar structural changes have occurred elsewhere in other industries, i.e., in airline transportation and telecommunications industries. The net effect of such adjustments will mean that the generation, transmission and distribution systems must now adapt to a new set of rules dictated by open markets. In particular for the transmission sector of power utilities, this adaptation may require the construction or modification of inter-connections between regions and countries. Furthermore, the adaptation to new generation patterns will also necessitate changes and will require increased flexibility and availability of the transmission system. Adding to these problems is the growing environmental concern and the constraints upon the rights-of-way for new installations and facilities. Yet additional demands are continually being made upon utilities to supply increased loads, to improve reliability, and to deliver energy at the lowest possible cost and with improved power quality. The power industry has responded to these challenges with the power-electronics-based technology of flexible AC transmission systems (FACTS). This term covers a whole family of power electronic controllers, some of which may have achieved maturity within the industry, while some others are as yet in the design stage.

FACTS has been defined by the IEEE as follows [G1]:

"A power electronic based system and other static equipment that provide control of one or more AC transmission system parameters to enhance controllability and increase power transfer capability."

In general, FACTS controllers can be divided into three categories:

1. Series controllers,
 2. Shunt controllers and
-

3. Combined series-shunt controllers.

Among FACTS controllers, the shunt controllers have shown feasibility in term of cost-effectiveness in a wide range of problem-solving from transmission to distribution levels. For decades, it has been recognized that the transmittable power through transmission lines could be increased, and the voltage profile along the transmission line could be controlled by an appropriate amount of compensated reactive current or power. Moreover, the shunt controller can improve transient stability and can damp power oscillation during a post-fault event. Using a high-speed power converter, the shunt controller can further alleviate or even cancel the flicker problem caused by electrical arc furnaces.

1.2 Shunt-Connected Controllers and STATCOM

In principle, all shunt-type controllers inject additional current into the system at the point of common coupling (PCC). An impedance of the shunt controller, which is connected to the line voltage, causes a variable current flow, and hence represents an injection of current into the line. As long as the injected current is in phase quadrature with the line voltage, the shunt controller only supplies or consumes variable reactive power.

The ultimate objective of applying reactive shunt compensation in a transmission system is to increase the transmittable power capability from the generator to the load, which is required to improve the steady-state transmission characteristic as well as the stability of the system.

The shunt controller basically consists of three groups.

1. Static var compensator (SVC)
 - 1.1. Thyristor-controlled reactor (TCR) and thyristor-switched reactor (TSR)
 - 1.2. Thyristor-switched capacitor (TSC)
2. Static synchronous compensator (STATCOM)
3. Static synchronous generator (SSG) or STATCOM with energy-storage system (ESS)

The SVC absorbs or generates controllable reactive power by synchronously connecting inductor or capacitor banks in and out of the power network. As a result, the SVC is too slow to respond to fast transient problems. In addition, the compensated reactive power is dependent on

system parameters. The compensated capacity of the TSC, for example, is indirectly proportional to the square of the line voltage.

Employing turn-off-capability semiconductor devices, switching power converters have been able to operate at higher switching frequencies and to provide a faster response. This makes the voltage-source converter (VSC) an important part in the FACTS controllers [G2]. The STATCOM is the first power-converter-based shunt-connected controller. The concept of STATCOM was disclosed by Gyugyi in 1976 [G3]. Instead of directly deriving reactive power from the energy-storage components, the STATCOM basically circulates power with the connected network. The reactive components used in the STATCOM, therefore, can be much smaller than those in the SVC.

In 1995, the first $\pm 100\text{MVA}$ STATCOM was installed at the Sullivan substation of Tennessee Valley Authority (TVA) in northeastern Tennessee. This unit is mainly used to regulate 161kV bus during the daily load cycle to reduce the operation of the tap changer of a 1.2GVA-161kV/500kV transformer. Its 48-pulse power converter consists of eight two-level VSCs with complex-interface magnetic circuits. Because this is a two-level VSC, a series connection of five of gate-turn-off (GTO) thyristors is used as a main switch. The control scheme used in this STATCOM is a 60Hz staircase. Due to the slow switching speed of the GTOs, the firing angles of the output waveform are fixed; therefore, the amplitude of each output waveform is controlled by exchanging real power of the DC-link capacitor with the power grid. Since it began operating, several weak points of the TVA-STATCOM system have been pointed out.

Among recently developed power converter topologies, multilevel converters have become an important technology, and have been utilized in high-power applications, particularly FACTS controllers. Several multilevel converter topologies have been developed to demonstrate their superiority in such applications [A1], [A2]. With converter modules in series, and with balanced voltage-sharing among them, lower-voltage switches can possibly be used in high-voltage systems. Thus, the low-voltage-oriented insulated gate bipolar transistor (IGBT) devices can be stacked for medium-voltage systems. For higher-voltage applications, however, efforts have been made to use GTO-based devices for multilevel converters [H1], [B4].

In reactive power compensation, cascaded-multilevel VSCs with separated DC capacitors are somewhat the most feasible topology for many reasons [A1], [A2], [B4], [B5], [B7], [B8], [B11], [B15], [B26]. The cascaded-multilevel converter (CMC) is constructed with a number of identical H-bridge converters. This modular feature makes the cascaded converter very attractive. The cascaded converter topology not only simplifies hardware manufacturability, but also makes the entire system flexible in terms of power capability. In addition, for the same power capability, the cascaded converter requires fewer total components. Auxiliary components, such as the clamped diodes and capacitors, are not required in the CMC topology.

The CMC-based STATCOM, however, challenges researchers to improve its dynamic responses and to balance its excessive number of DC capacitor voltages. To date, several papers have discussed the configurations and control strategies for the reactive power compensation systems that utilize CMCs [B4], [B5], [B7], [B8], [B11], [B15], [B26]. Based on these previous works, an accurate model and an effective control technique associated with the simple DC capacitor balancing strategy are elements important to achieving a high-performance, stable, cost-effective CMC-based STATCOM.

1.3 Cascaded-Multilevel Converters

The basic concept of the CMC has existed for more than two decades; however, it was not fully realized until two researchers, Lai and Peng, patented it and presented its various advantages in 1997. Since then, the CMC has been utilized in a wide range of applications. Research and development of the CMCs is conducted from small-power applications such as electric vehicles to very-high-power applications such as STATCOM and FACTS controllers. In the industrial community, Robicon Corporation commercialized their medium-voltage drives utilizing the CMC or the series-cell multilevel topology in 1999. In 1998, GEC ALSTHOM T&D (now ALSTOM T&D) proposed to use the CMC topology as a main power converter in their STATCOMs that are associated with the TSR and TCR.

With its modularity and flexibility, the CMC shows superiority in high-power applications, especially shunt and series connected FACTS controllers. The CMC synthesizes its output near sinusoidal voltage waveforms by combining many isolated voltage levels. With a sufficiently

high number of voltage levels, a premium-quality output waveform with fast system response can be achieved by switching the main power semiconductor devices only at the line frequency. This naturally minimizes the entire system losses and the output filter requirement. In addition, by adding more H-bridge converters, the amount of Var can simply increased without redesign the power stage, and build-in redundancy against individual H-bridge converter failure can be realized. Moreover, a three-phase CMC topology is essentially composed of three identical phase legs of the series-chain of H-bridge converters, which can possibly generate different output voltage waveforms and offers the potential for AC system phase-balancing. This feature is impossible in other VSC topologies utilizing a common DC link.

By nature of this topology, however, the CMC is impossible to apply in intertie or back-to-back applications, such as universal power flow controllers (UPFC). Fortunately, with energy-storage systems, the CMC can now successfully overcome this limitation. This combination also enhances recent low-voltage energy-storage system technology for high-voltage applications.

A great combination of the STATCOM concept and the CMC topology is a promising controller in the modern FACTS technology.

1.4 Literature Review of the STATCOM Utilizing-Cascaded Multilevel Converters

To date, CMC-based STATCOM has only just begun to be explored. This technology is relatively new. A complete control system for STATCOM applications basically consists of two main parts: external and internal controls. Generally, the external control depends on the power system network to which the STATCOM is connected. Meanwhile, the internal control mainly depends on the VSC topologies. An ideal internal control should instantaneously respond to a given command, which is generated by the corresponding external controller. Different VSC-based STATCOMs can be operated with the same external control as long as they are connected to the same problematic power network. In the past two decades, several hundred publications have discussed STATCOM external controls, and several effective control strategies are now mature and have been applied in the field [H1]-[H20]. On the other hand, the research on the

internal control for the CMC-based STATCOM is relatively new. Three major challenges, which have yet fully investigated, have made this research area very attractive.

First, a well-defined model is a key to improvements in the effectiveness and stability of a feedback control and for system parameter optimizations. Numerous parameters that need control mean that CMC-based STATCOM modeling is not trivial. None of the previous works has shown a valid model [B1]-[B28]. The feedback-control parameters were thus randomly selected. This dissertation, thus, proposes a simplified model of the CMC-based STATCOM in both ABC and DQ0 coordinates, which can be effectively applied in any number of voltage levels.

Because the STATCOM deals with power control, two power components, real and reactive, must be controlled separately. Moreover, to maximize the stability of the system operation, a spontaneous response is very desirable. The second challenge is thus how to achieve a control that has power-decoupling capability. With the help of the proposed CMC-based STATCOM model, decoupling power control technique is proposed. By applying the proposed control strategy, the AC state variables are transformed into DC form in which the classical control theories can be used to evaluate the system stability and to optimize the design process. As a result, the performance of the feedback control can be maximized, and the control stability can be confirmed.

To be able to operate in a high-voltage application, an excessive number of DC capacitors are utilized in a CMC-based STATCOM. Voltages across these DC links must be balanced to avoid over-voltage on any particular link. Not only do these unbalanced DC voltages introduce voltage stress on the semiconductor switches, but they also lower the quality of the synthesized output waveforms of the converter. Consequently, how to maintain and balance these many DC links with a straightforward and cost-effective technique thus becomes the third challenge for this topology. The previous work on the DC capacitor voltage-balancing techniques, [B5], [B10], [B11], [B15], [B23], [B26], are basically the same approach, which adds $3N$ individual voltage loops into the main control loop, where N is the number of H-bridge converters per phase. The design of the compensators of the individual loop is very difficult because of the complexity of the voltage-loop transfer functions. Basically, trial and error technique, which is very time-

consuming, provides the simplest way to achieve a good compensator. Moreover, the greater number of voltage levels, the more complex the control design. The main controller, which is the DSP-based, must perform all of those feedback controls. As a result, this approach potentially reduces the reliability of the controller. A new DC-capacitor voltage balancing technique—the cascaded PWM is, therefore, proposed to effectively overcome the complexity of the compensator designs. The cascaded PWM has the following features: it is suitable for any number of H-bridge converters, it offers hardware-based realization, modularity, and its complexity is not affected by the number of voltage levels. Since the proposed technique can be realized by hardware circuitry, the calculation time in the DSP is just slightly increased when more voltage levels are employed. The basic structure of the proposed technique is modular; therefore, it is suitable for any number of H-bridge converters. With these features, the complexity of the DSP programming for the control loop is not affected by increasing the number of voltage levels.

1.5 Motivation and the Dissertation Outline

To improve the performance and effectiveness of the control for the CMC-based STATCOM system, the following five contributions are proposed in this dissertation:

1. optimized design for the CMC-based STATCOM power stage and its passive components,
2. modeling of the CMC for reactive power compensation,
3. decoupling power control method,
4. DC-link balancing technique, and
5. improvement in the CMCs.

Based on the flow of the contributions, this dissertation is divided into seven chapters.

Chapter 2 presents the operation principals of the STATCOM and the distributed-STATCOM (DSTATCOM). The literature written about multilevel VSCs for reactive and real power compensation is discussed. All published VSC topologies are categorized based on their structures and are compared based on their feasibilities for reactive power compensation functions.

Chapter 3 presents the optimized design for the CMC-based STATCOM system, which includes the CMC power stage and the embedded passive components. An H-bridge building block (HBBB), which is a basic identical unit in the CMC topology, is proposed. The power stage of the HBBB is optimally designed based on the Virginia Tech-invented high-power semiconductor devices, the emitter turn-off (ETO) thyristor. By applying the HBBB concept, a STATCOM system becomes more flexible, reliable, and cost-effective. In addition, to maximize the overall system performance, the passive-component design optimization strategy is also investigated.

Chapter 4 begins with the operating principles of the CMC-based STATCOM. The key control laws are addressed. A modeling development methodology for the CMC-based STATCOM is proposed. Due to the excessive number of controlled variables in the CMCs, an effective simplification, based on practical assumptions and proposed variable definitions, is proposed. Average and small-signal models in ABC and DQ0 coordinates are proposed. Major transfer functions of the system are determined for use in feedback-control designs.

In Chapter 5, the decoupling power control technique is proposed for the CMC-based STATCOM system. Simulation and experimental results demonstrate the superiority of the control method in a wide operation range. Moreover, another major contribution is proposed, i.e., a new effective DC-capacitor voltage-balancing technique—cascaded pulse width modulator, which is used to assure well-regulated voltages across all the DC capacitors of the CMC. The performance of the proposed technique is verified experimentally.

Chapter 6 proposes two novel improvements in the cascaded-multilevel VSC topology. A new cascaded-multilevel VSC with minimum number of isolated DC links is demonstrated. To improve the switching loss and to increase the range of operation, a new optimum multilevel modulation technique is proposed.

Chapter 7 draws conclusion for this dissertation and proposes future work.

Chapter 2 MULTILEVEL VOLTAGE-SOURCE CONVERTERS FOR STATCOM APPLICATIONS

This chapter presents the operating principals of the STATCOM. The STATCOM is basically one of the parallel FACTS controllers. The same kind of STATCOM is the so-called distribution static compensator (DSTATCOM), which is applied in distribution networks. The key component of the STATCOM is a power VSC, which is based on high-power electronics technologies. All kinds of VSCs are compared in order to show their advantages and disadvantages in STATCOM applications. Based on its superior characteristics, the most promising topology for the STATCOM application is the CMC with separated DC capacitors (SDCCs).

2.1 Operating Principals of the STATCOM

The STATCOM is the solid-state-based power converter version of the SVC. The concept of the STATCOM was proposed by Gyugyi in 1976. Operating as a shunt-connected SVC, its capacitive or inductive output currents can be controlled independently from its connected AC bus voltage. Because of the fast-switching characteristic of power converters, the STATCOM provides much faster response as compared to the SVC. In addition, in the event of a rapid change in system voltage, the capacitor voltage does not change instantaneously; therefore, the STATCOM effectively reacts for the desired responses. For example, if the system voltage drops for any reason, there is a tendency for the STATCOM to inject capacitive power to support the dipped voltages.

Theoretically, the power converter employed in the STATCOM can be either a VSC or a current-source converter (CSC). In practice, however, the VSC is preferred because of the bi-directional voltage-blocking capability required by the power semiconductor devices used in CSCs. To achieve this kind switch characteristic, an additional diode must be connected in series with a conventional semiconductor switch, or else the physical structure of the semiconductor must be modified. Both of these alternatives increase the conduction losses and total system cost. In general, a CSC derives its terminal power from a current source, i.e., a reactor. In comparison,

a charged reactor is much lossier than a charged capacitor. Moreover, the VSC requires a current-source filter at its AC terminals, which is naturally provided by the coupling transformer leakage inductance, while additional capacitor banks are needed at the AC terminals of the CSC. In conclusion, the VSCs can operate with higher efficiency than the CSCs do in high-power applications. A suitable VSC is selected based on the following considerations: the voltage rating of the power network, the current harmonic requirement, the control system complexity, etc.

Basically, the STATCOM system is comprised of three main parts: a VSC, a set of coupling reactors or a step-up transformer, and a controller. In a very-high-voltage system, the leakage inductances of the step-up power transformers can function as coupling reactors. The main purpose of the coupling inductors is to filter out the current harmonic components that are generated mainly by the pulsating output voltage of the power converters. The STATCOM is connected to the power networks at a PCC, where the voltage-quality problem is a concern. All required voltages and currents are measured and are fed into the controller to be compared with the commands. The controller then performs feedback control and outputs a set of switching signals to drive the main semiconductor switches of the power converter accordingly. The single-line diagram of the STATCOM system is illustrated in Figure 2-1. In general, the VSC is represented by an ideal voltage source associated with internal loss connected to the AC power via coupling reactors.

In principal, the exchange of real power and reactive power between the STATCOM and the power system can be controlled by adjusting the amplitude and phase of the converter output voltage. In the case of an ideal lossless power converter, the output voltage of the converter is controlled to be in phase with that of the power system. In this case, there is no real power circulated in the STATCOM; therefore, a real power source is not needed. To operate the STATCOM in capacitive mode or var generation, $+Q$, the magnitude of the converter output voltage is controlled to be greater than the voltage at the PCC. In contrast, the magnitude of the output voltage of the converter is controlled to be less than that of the power system at the PCC on order to absorb reactive power or to operate the STATCOM in inductive mode, $-Q$. However, in practice, the converter is associated with internal losses caused by non-ideal power semiconductor devices and passive components. As a result, without any proper controls, the

capacitor voltage will be discharged to compensate these losses, and will continuously decrease in magnitude. To regulate the capacitor voltage, a small phase shift δ is introduced between the converter voltage and the power system voltage. A small lag of the converter voltage with respect to the voltage at the PCC causes real power to flow from the power system to the STATCOM, while the real power is transferred from the STATCOM to the power system by controlling the converter voltage so that it leads the voltage at the PCC. Figure 2-2 illustrates phasor diagrams of the voltage at the PCC, converter output current and voltage in all four quadrants of the PQ plane.

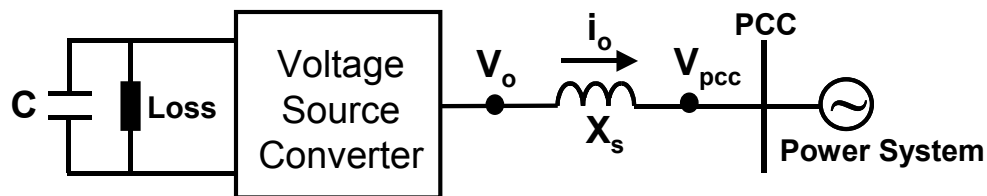


Figure 2-1. Single-line diagram of the voltage-source converter-based STATCOM.

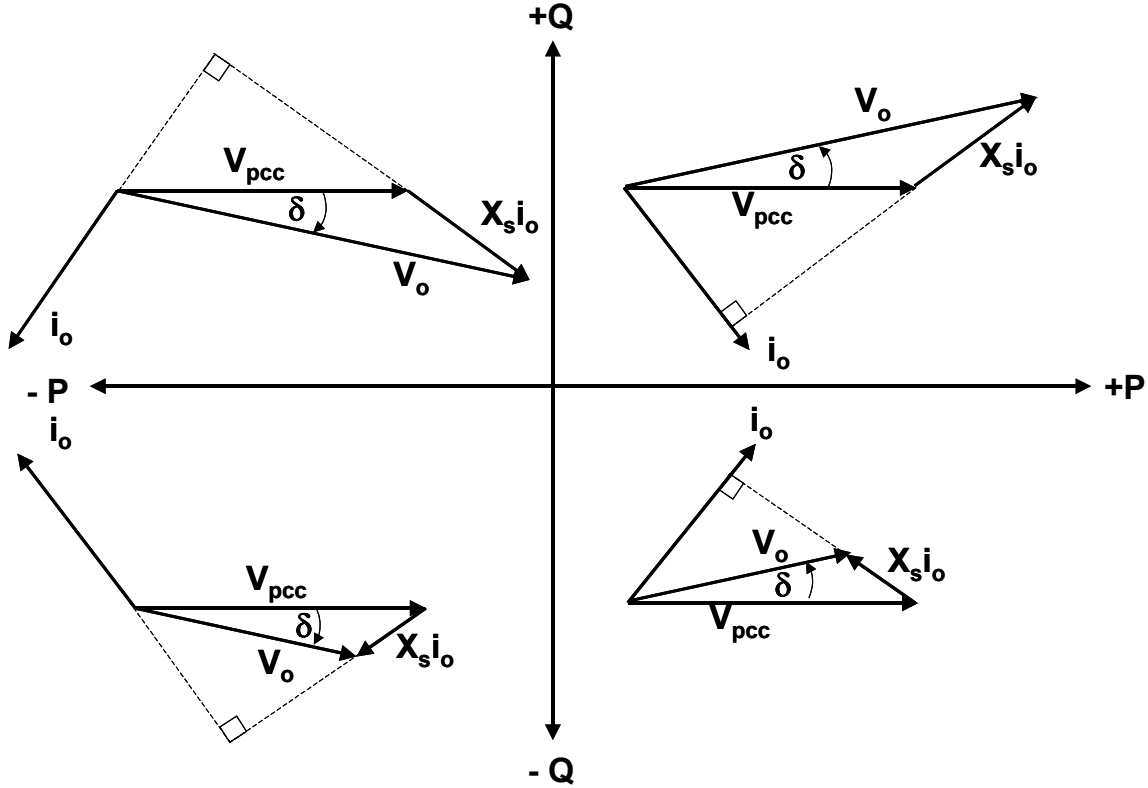


Figure 2-2. Phasor diagram for power exchanges in STATCOM applications.

2.2 Voltage-Source Converters for STATCOM Applications

Based on the number of their synthesized output voltage levels, VSCs can generally be categorized into two major groups: conventional two-level converters and more-than-two-level converters or multilevel converters. With recent power semiconductor technologies, a traditional two-level VSC is not viable for high-voltage applications such as FACTS controllers. In the U.S., the voltage level for distribution to the transmission system ranges from 4.1 kV to 765 kV. To be able to be used in such high-voltage applications, a main switch of the two-level converter is formed by many semiconductor devices connected in series. By doing so, many constraints need to be addressed. Due to the different scattering times of semiconductor devices, the following issues must be well considered in order to avoid voltage-sharing problems among the switches. The electrical and thermal characteristics of the semiconductor devices in the same

switch need to be matched. Additional care is needed for the turning-off process of the switch, as well as for its gate currents. As a result of these restrictions, the switching frequency of the series switch is inefficiently decreased. This causes a slow system response and bulky output-filter circuits. Although the blocking voltage of the switch in the two-level converter is increased, a step-up transformer is still needed for coupling to the transmission networks.

An attractive alternative to the two-level converter is a multilevel VSC. Without semiconductor devices connected in series, the multilevel converters show feasible capability of clamping the voltages across individual devices below their limitations. This allows the recent semiconductor devices to be utilized in higher-voltage applications without incurring voltage-sharing problems. Another significant advantage of the multilevel configuration is the harmonic reduction in the output waveform with very low switching frequency, line frequency for example. Besides the high-voltage capability, multilevel converters also provide other advantages over the two-level converters. To be compared to the two-level converters, a cascaded three-level converter, which will be detailed in the multilevel converter section of this chapter, is used as an example of the multilevel converter in the four following aspects: output voltage quality, DC capacitance requirement, losses and power capacity. The schematics of the two-level converter and the cascaded three-level converter are shown in Figure 2-3(a) and (b), respectively.

I. Comparison between Two-Level and Three-level Voltage-Source Converters

A. Harmonics in Output Waveform

Figure 2-4(a) and (b) show the output line-to-line waveforms of a two-level VSC and a three-level cascaded converter, respectively. The number of line-to-line voltage levels for the two-level VSC is three, while the number of levels in the output waveform of the three-level cascaded converter is five. Both converters operate at the same line-to-line voltage of $\sqrt{2} \cdot 2000$ V, a switching frequency of 1 kHz, and a modulation index of 0.8. The sinusoidal pulse-width modulation (SPWM) is applied in both systems. The frequency spectra of Figure 2-4(a) and (b) are shown in Figure 2-4(c) and (d), respectively. The results show that the total harmonic

distortion (THD^*) of the three-level converter output voltage is 45%, whereas it is 94% for that of the two-level VSC. As a result, the three-level converter can operate at a lower switching frequency to achieve the same THD. Meanwhile, at the same THD, the output filter circuit for the three-level converter can be much smaller. In order to minimize harmonics, the two-level converter adopts a zigzag transformer to achieve a pseudo-multilevel waveform. However, this increases the size and cost, but decreases the liability. This will be discussed more in the section on hybrid multilevel converters.

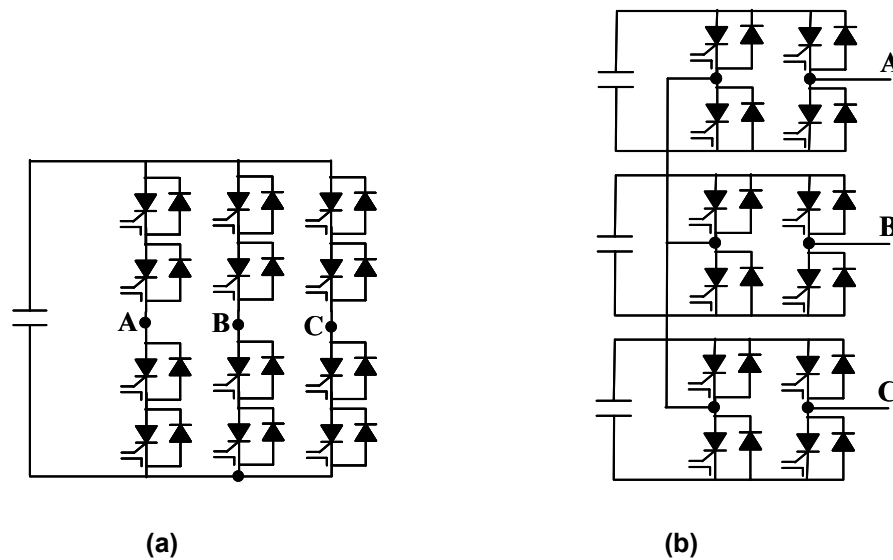


Figure 2-3. (a) Conventional two-level converter and (b) the three-level cascaded converter.

B. Capacitance Requirement

To compare the capacitance requirement, the capacitances required in the two-level VSC and the three-level converter for the same reactive power rating are determined. Table 2-1 shows an example of the specifications for the STATCOM system.

* THD denotes the pre-filter voltage harmonics, which will be reduced significantly after being filtered.

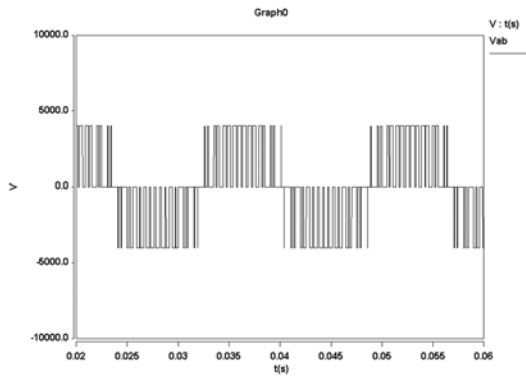
In the cascaded converter, the capacitance requirement is given as follows:

$$C_{dc_cascade} = \frac{I_{Lrms}}{\sqrt{2} \cdot \pi \cdot f \cdot \Delta V_{dc}} .$$

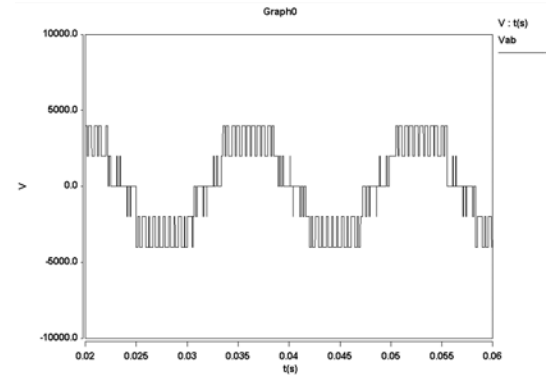
Equation 2-1

Then, substituting the numbers from Table 2-1 into Equation 2-1 yields

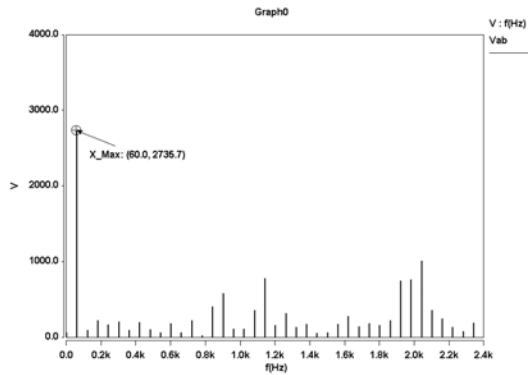
$$C_{dc_cascade} = 9.4 \text{ mF} .$$



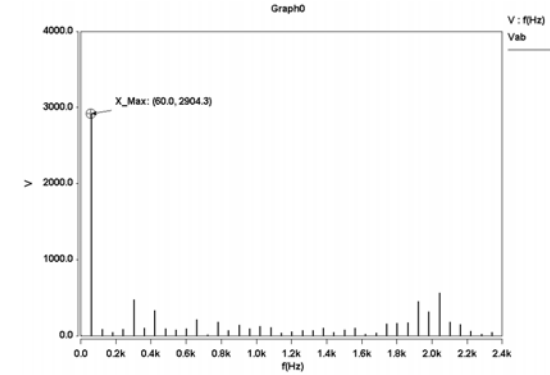
(a)



(b)



(c)



(d)

Figure 2-4. Simulation results for (a) the two-level VSC line-to-line voltage, (b) the three-level cascaded converter line-to-line voltage, (c) the frequency spectrum of (a), and (d) the frequency spectrum of (b).

TABLE 2-1. ASSUMED SPECIFICATIONS OF THE STATCOM.

Maximum VAR	2 MVar
Line Frequency, f	60 Hz
Switching Frequency, f_s	1 kHz, SPWM
Line-to-Line Voltage, V	3464 V _{pk}
Line Current, I_{Lrms}	500 A _{rms}
Capacitor Ripple Voltage, ΔV_{dc}	10% of Vdc

Therefore, the capacitor required in the three-level converter is 9.4 mF/3000 V, and three of these capacitors are needed. For the two-level converter, the capacitance requirement is given as follows:

$$C_{dc_2level} = \frac{I_{Lrms}}{\sqrt{6} \cdot \pi \cdot f \cdot \Delta V_{dc}}.$$

Equation 2-2

Thus, the capacitor required in the two-level converter is 6 mF/6000 V. The calculated total capacitances for both cases are shown in Table 2-2. The total capacitance requirement for the three-level converter is about 4.5 times that for the two-level converter. However, the capacitor required in the two-level converter has double the voltage rating of those in the cascaded converter.

To make a fair comparison, the same DC voltage rating of the capacitors is considered for the two. Table 2-3 shows the total capacitance requirement in both cases: that of the cascaded converter is slightly higher than that for the two-level VSCs.

TABLE 2-2. CALCULATED RESULTS OF THE CAPACITANCE REQUIREMENT IN BOTH TOPOLOGIES.

	Capacitor	Quantity	Total
Two-Level VSC	6 mF, 6000 V	1x	6 mF
Cascaded Converter	9.4 mF, 3000 V	3x	28.2 mF

TABLE 2-3. TOTAL CAPACITANCE REQUIREMENT UNDER THE SAME DC VOLTAGE IN BOTH TOPOLOGIES.

	Capacitor	Quantity	Total
Two-Level VSC	12 mF, 3000 V	2x	24.0 mF
Cascaded Converter	9.4 mF, 3000 V	3x	28.2 mF

C. Main Device Losses

In this section, semiconductor device losses, i.e., conduction loss and switching loss, are compared between both topologies. Both converters operate at the same specifications, as shown in Table 2-1, except with different switching frequencies. For the sake of simplicity, the switching frequency is reduced to 300 Hz. In this comparison, ETOs are used as the main switches. The ETO loss data is based on a 2kA/4500V GTO 5SGA20H4502 from ABB (according to the corresponding datasheets).

1. Conduction Loss

$$P_{con}(I) = 1.8 \cdot I + 1.25 \cdot 10^{-3} \cdot I^2$$

Equation 2-3

2. Switching Loss

- Turn-on Loss: $E_{on} < 0.25 J$ at $V = 2000$, $di/dt = 630 A/\mu s$

- Turn-off Loss: $E_{off}(I, V_d) = (2.917 \cdot 10^{-3} \cdot I + 0.0416) \frac{V_d}{1900}$,

Equation 2-4

where I is the RMS current drawn by the ETO, and

V_d is the voltage across the ETO.

Because they draw the same level of current, the conduction losses in both topologies are approximately identical. For the switching losses in applications where di/dt snubbers are used, the turn-on loss can be ignored because it is much smaller than the turn-off loss. Therefore, only the turn-off loss, which is a function of currents and voltages of the switches, will be considered.

Figure 2-5 shows switching patterns of one phase leg of the two-level converter and the three-level cascaded converter. The switching frequencies for each switching device are shown in Figure 2-5. Under the same line-to-line voltage, the switch voltage of the two-level converter is $\sqrt{3}/2$ times that of the three-level converter. Theoretically, the turn-off loss can be derived as follows:

$$P_{off} = E_{off} \cdot f_s.$$

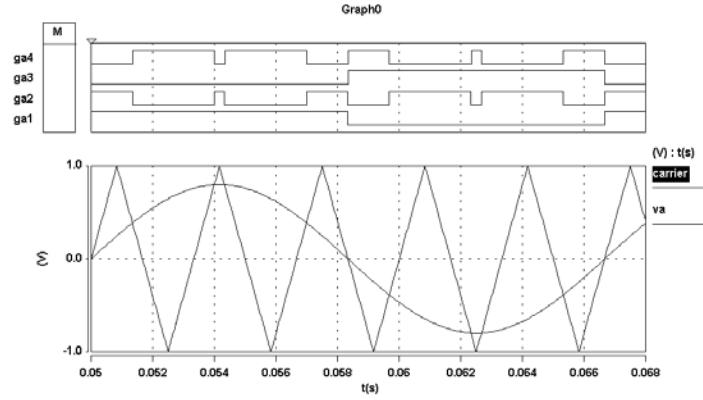
Equation 2-5

Using Equation 2-5 and Table 2-4,

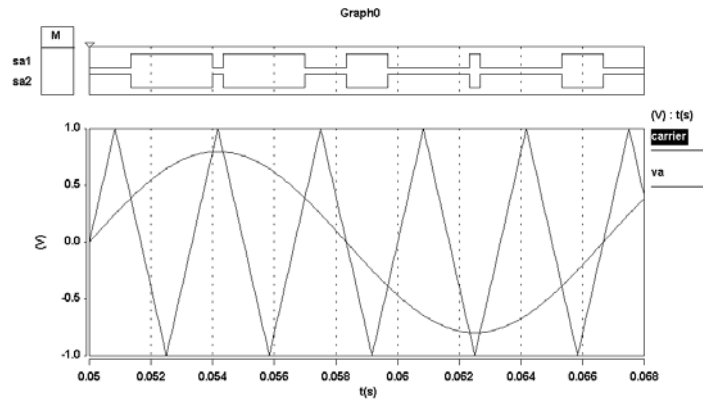
$$\frac{P_{off_cascade}}{P_{off_two-level}} = \frac{k \cdot V_d \cdot (2/5 + 2)f_s}{k \cdot (V_d) \cdot (4)f_s},$$

Equation 2-6

where $k = 2.917 \cdot 10^{-3} \cdot I + 0.0416$.



(a)



(b)

Figure 2-5. Switching pattern of one phase leg of (a) the three-level cascaded converter, and (b) the two-level converter.

TABLE 2-4. SWITCHING FREQUENCY, VOLTAGE AND RMS CURRENT FOR EACH SWITCHING DEVICE.

Three-Level Cascaded Converter			Two-level converter		
Figure 2-5(a)	ga1, ga3	ga2, ga4	Figure 2-5(b)	sa1 (x2)	sa2 (x2)
Switching Frequency	$f_s/5$	f_s	Switching Frequency	f_s	f_s
Switch Voltage	V_d		Switch Voltage	V_d	
RMS Current	I		RMS Current	I	

Thus, the ratio of the cascaded converter turn-off loss to that of the two-level converter is

$$\frac{P_{off_cascade}}{P_{off_two-level}} = 0.6.$$

Equation 2-7

Thus, at the same switching frequency, the switching loss in the cascaded converter is about 60% of that in the two-level converter.

D. High Power-Rating Capability

To increase the power rating, three-level converters can simply be modified to be higher-level converters. The power stress of switches is independent from the number of voltage levels. In contrast, there is a need to redesign all component ratings in the two-level converter. Moreover, the voltage or current stress of the switching devices increases; therefore, more devices must be connected in series or parallel to form one switch. As a result, dynamic voltage-sharing and turn-off-synchronizing are concerns, since they reduce the reliability of the system. In other words, under the same device capability, the three-level inverter can operate up to full device capability without any major penalties, whereas this is impossible in the two-level system.

For the STATCOM application, three-level converters are more feasible than two-level converters, since they can operate at lower switching frequencies to achieve the given THD requirement. The switching loss can thus be reduced. At the same line-to-line voltage, compared with the two-level VSC, although the required DC capacitance is higher, the voltage rating of the capacitors is lower in the cascaded converter.

2.3 Multilevel Voltage-Source Converters

For the past two decades, multilevel VSC technology has been a rapidly developing area in power electronics. It promises power-conversion equipment for applications that operate in the medium-voltage (4.6-13.8 kV) grid without requiring step-up transformers. With the step-up transformer, the multilevel converter may also be operated at higher voltage levels, such as transmission levels. Multilevel VSC technology has recently been utilized in various types of

industrial applications, such as AC power supplies, reactive power compensations, adjustable-speed drive systems, etc.

Fundamentally, the output voltage waveform of a multilevel converter is synthesized from different levels of voltages obtained from capacitor voltage sources. Figure 2-6 shows an equivalent circuit of a half bridge of a multilevel VSC. A bi-directional, single-pole, multi-throw switch is a key element of the multilevel topology. By controlling the way in which the switch is connected to a portion of the capacitors, a number of output voltage levels can be synthesized. To generate a negative output voltage, the reference of the output can be connected to different segments of the capacitor string. Two or more half bridge of the converter shown in Figure 2-6 can be utilized to form a multiphase, multilevel converter.

A voltage level of three is considered to be the smallest number in multilevel converter topologies. Due to the bi-directional switches, the multilevel VSC can work in both rectifier and inverter modes. This is why it is referred to as a converter instead of as an inverter throughout this dissertation. As the number of levels reaches infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage-imbalance problems, voltage clamping requirements, circuit layout and packaging constraints, complexity of the controller, and, of course, capital and maintenance costs.

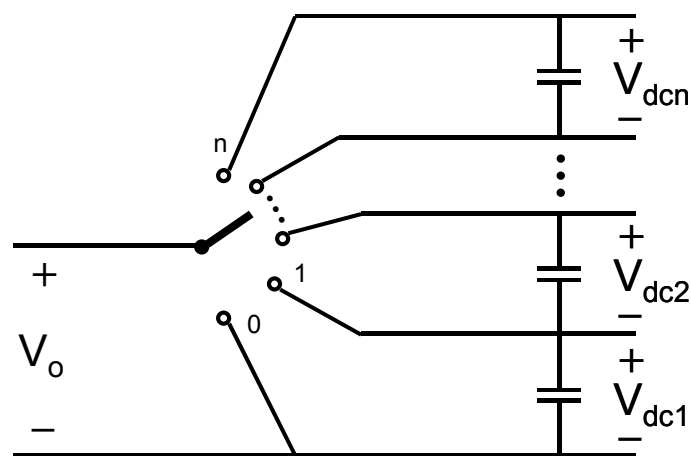


Figure 2-6. Equivalent circuit of multilevel voltage-source converters.

In the past two decades, several state-of-the-art multilevel VSCs have been introduced by both universities and industries. Some of these have become quite popular, but some have not. Different topologies showed their advantages in particular applications. In this literature review, multilevel VSCs are categorized into two groups: topology-level multilevel converters and hybrid multilevel converters.

In the first category, there are four major capacitor-voltage synthesis-based multilevel converters, listed as follows:

- A) diode-clamped multilevel converter [C1]-[C4];
- B) flying-capacitor multilevel converter [D1]-[D4];
- C) P2 multilevel converter [E1]; and
- D) cascaded converters with separated DC sources [B1]-[B27].

Multilevel converters in the second category are fundamentally a combination of two topologies in the first category, or one of the first category with additional magnetic circuits. The second category can be divided into two basic topologies, as follows:

- A) multi-pulse based on two-level and three-level converters [H1], and
- B) mixed-level hybrid cell converters [F8], [F9].

I. Topology-Level Multilevel Converters

A. Diode-Clamped Multilevel Converter

The diode-clamped multilevel converter (DCMC) uses capacitors in series to divide up the DC bus voltage into a set of voltage levels. To produce an m -level phase voltage, a diode-clamped converter needs $m-1$ capacitors on the DC bus. A three-phase, five-level diode-clamped converter is shown in Figure 2-7. The DC bus consists of four capacitors: C_1 , C_2 , C_3 and C_4 . For a DC bus voltage V_{dc} , the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level, $V_{dc}/4$, through clamping diodes. DCMC output-voltage synthesis is relatively straightforward.

To explain how the staircase voltage is synthesized, point O is considered as the output-phase voltage reference point. Using the five-level converter shown in Figure 2-7, there are five switch combinations that generate five-level voltages across A and O. Table 2-5 shows the phase voltage levels and their corresponding switch states.

From Table 2-5, state 1 represents that the switch is on, and state 0 represents that the switch is off. In each phase leg, a set of four adjacent switches is on at any given time. There are four complementary switch pairs in each phase, i.e., S_{a1} - $S_{a'1}$, S_{a2} - $S_{a'2}$, ..., and S_{a4} - $S_{a'4}$.

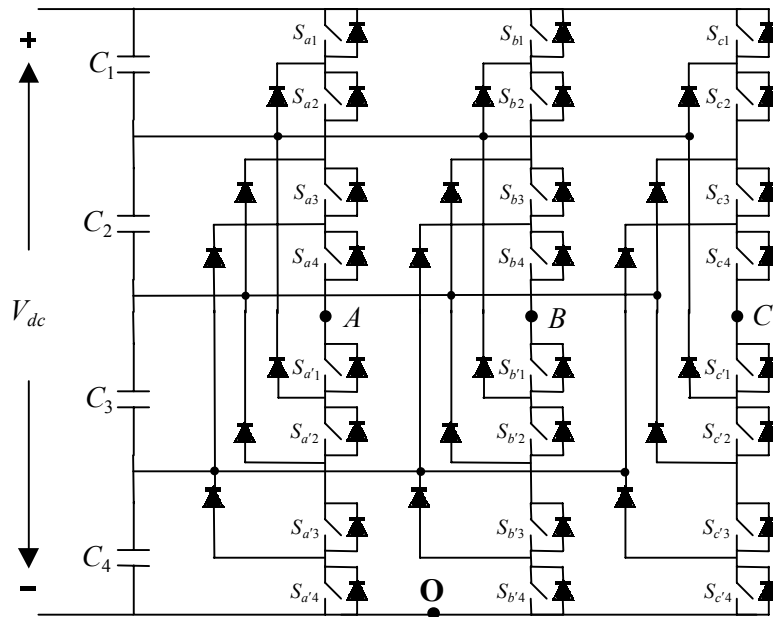


Figure 2-7. A three-phase, five-level diode-clamped converter.

TABLE 2-5. DIODE-CLAMPED FIVE-LEVEL CONVERTER VOLTAGE LEVELS AND THEIR SWITCH STATES.

Output V_{AO}	Switch State							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	0	1	1	1	1	0	0	0
$V_3=V_{dc}/2$	0	0	1	1	1	1	0	0
$V_2=V_{dc}/4$	0	0	0	1	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

B. Flying-Capacitor Multilevel Converter

A flying-capacitor multilevel converter (FCMC), as shown in Figure 2-8, uses a ladder structure of DC capacitors for which the voltage on each capacitor differs from that on the next capacitor. To generate an m -level staircase output voltage, $m-1$ capacitors in the DC bus are needed. Each phase leg has an identical structure. The size of the voltage increment between two capacitors determines the size of the voltage levels in the output waveform.

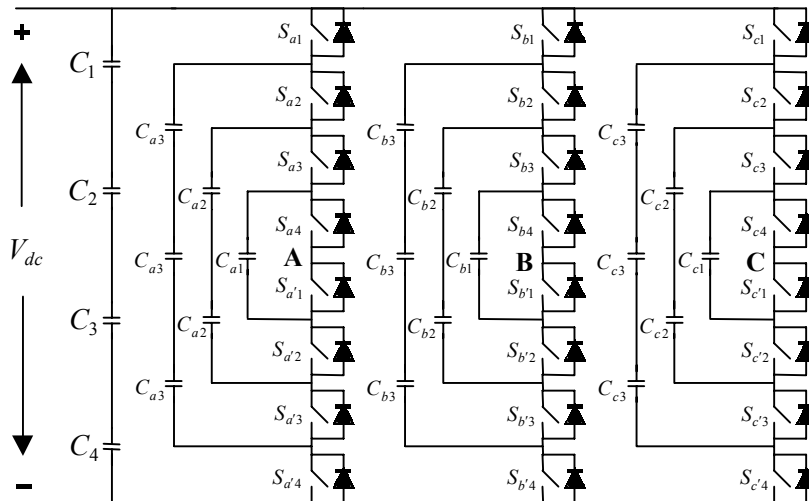


Figure 2-8. A three-phase, five-level flying-capacitor converter.

It is obvious that the three inner-loop balancing capacitors for phase leg A (C_{a1} , C_{a2} and C_{a3}) are independent from those for phase leg B. All phase legs share the same DC-link capacitors, C_1 - C_4 . Table 2-6 shows a possible switch combination of the voltage levels and their corresponding switch states.

TABLE 2-6. A POSSIBLE SWITCH COMBINATION OF THE VOLTAGE LEVELS AND THEIR CORRESPONDING SWITCH STATES.

Output V_{AO}	Switch State							
	S_{a1}	S_{a2}	S_{am-1}	S_{am}	$S_{a'1}$	$S_{a'2}$	$S_{a'm-1}$	$S_{a'm}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_3=V_{dc}/2$	1	1	0	0	1	1	0	0
$V_2=V_{dc}/4$	1	0	0	0	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

In fact, there is more than one combination that can produce output voltages V_2 , V_3 and V_4 , which makes the FCMC more flexible than the DCMC. Table 2-6, however, shows only one possible combination.

C. P2 Multilevel Converters

Referring to previous work [A1], since this converter consists of a number of basic two-level cells, this generalized multilevel converter topology is called the P2 multilevel converter (P2MC). Regardless of the load characteristic, this converter can balance each voltage level independently. Figure 2-9 shows a phase leg of the MC. Switches S_{p1} - S_{p4} , S_{n1} - S_{n4} and their anti-parallel diodes are the main devices that synthesize the desired voltage waveforms. The rest of the switches and diodes are used for clamping and balancing the capacitor voltages. Table 2-7 shows one possible switching state to produce a five-level output voltage.

TABLE 2-7. SWITCHING STATE TO PRODUCE OUTPUT VOLTAGE OF THE P2MC.

Output V_{ON}	Switch State							
	S_{p1}	S_{p2}	S_{p3}	S_{p4}	$S_{a'1}$	$S_{a'2}$	$S_{a'm-1}$	$S_{a'm}$
$4V_{dc}$	1	1	1	1	0	0	0	0
$3V_{dc}$	1	1	1	0	0	0	0	1
$2V_{dc}$	1	1	0	0	0	0	1	1
V_{dc}	1	0	0	0	0	1	1	0
0	0	0	0	0	1	1	1	1

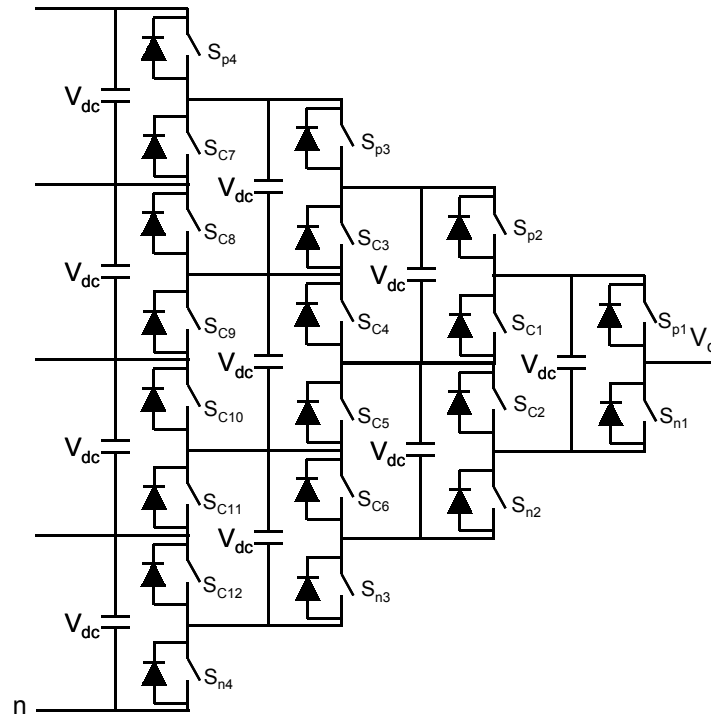


Figure 2-9. Phase leg of the five-level P2 converter.

D. Cascaded-Multilevel Converters with Separated DC Sources

The last topology discussed here is a multilevel converter, which uses cascaded converters with separate DC sources (SDCSs). Since shorter name is preferred for this converter, it will be referred to as a CMC. The general function of this multilevel converter is the same as that of the three previous converters. The CMC synthesizes a desired voltage from several independent sources of DC voltages, which may be obtained from batteries, fuel cells or solar cells. This configuration has recently become very popular in high-power AC supplies and adjustable-speed drive applications. This new converter can avoid extra clamping diodes or voltage-balancing capacitors. A single-phase, m -level configuration of the CMC is shown in Figure 2-10.

Each SDCS is associated with a single-phase H-bridge converter. The AC terminal voltages of different-level converters are connected in series. Through different combinations of the four switches, S_1 - S_4 , each converter level can generate three different voltage outputs, $+V_{dc}$, $-V_{dc}$ and zero. The AC outputs of different full-bridge converters in the same phase are connected in series such that the synthesized voltage waveform is the sum of the individual converter outputs. Note that the number of output-phase voltage levels is defined in a different way from those of the two previous converters. In this topology, the number of output-phase voltage levels is defined by $m = 2N+1$, where N is the number of DC sources.

A seven-level cascaded converter, for example, consists of three DC sources and three full-bridge converters. Minimum harmonic distortion can be obtained by controlling the conducting angles at different converter levels.

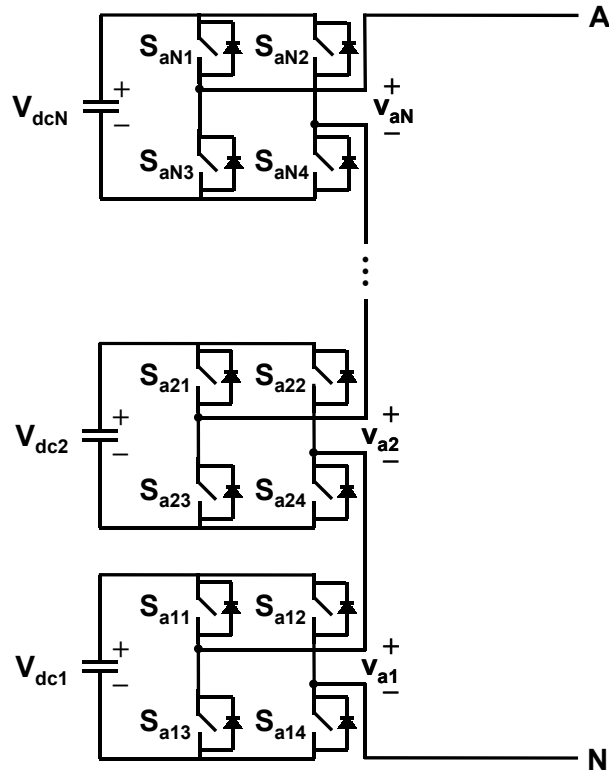


Figure 2-10. Single-phase structure of the cascaded-multilevel converter.

For a three-phase system, the output voltage of the three cascaded converters can be connected in either wye or delta configurations. For example, a wye-configured m-level converter using a CMC with separated capacitors is illustrated in Figure 2-11.

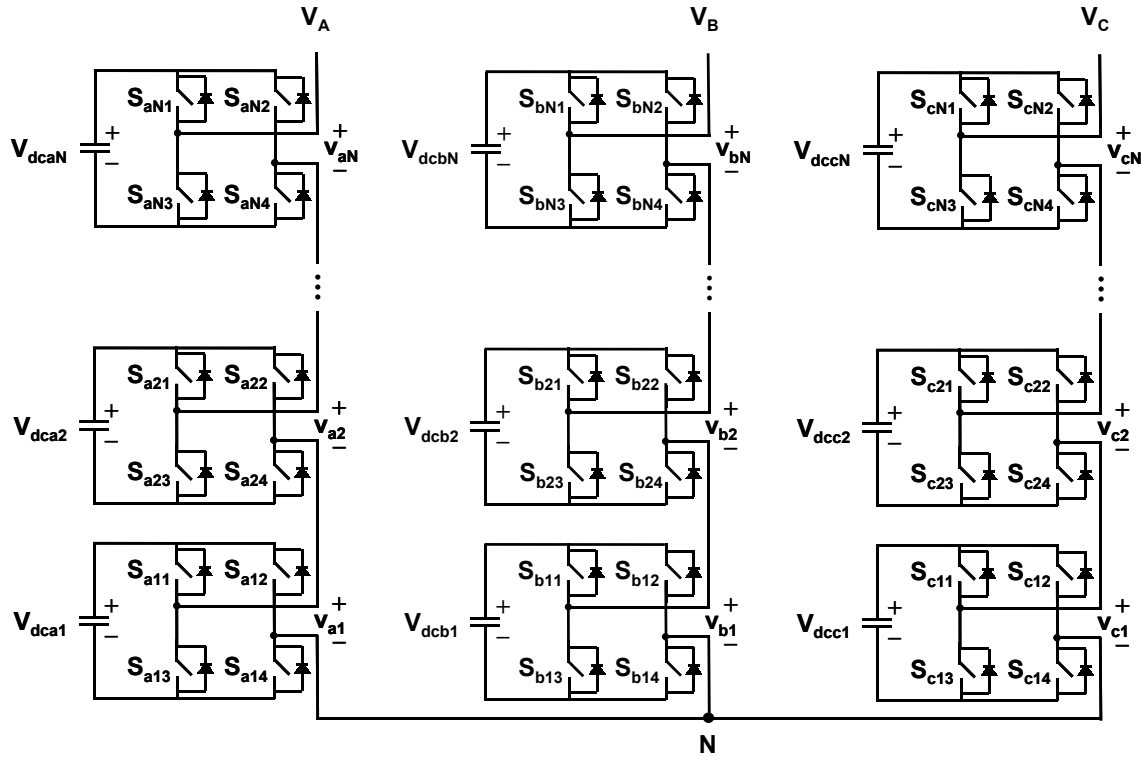


Figure 2-11. A general three-phase wye-configuration CMC.

II. Hybrid Multilevel Converters

A. Multi-Pulse Converters

This special kind of hybrid multilevel converter has been extensively presented for quite some time. Basically, it synthesizes the output voltage by magnetically series-connecting output voltages of a number of two-level, three-phase converters. A sophisticated transformer circuit is used to create a multilevel wave shape, as well as to increase the voltage rating. Figure 2-12 illustrates a 24-pulse converter. Four two-level converters share the same DC link. Although the complicated magnetic circuits are used in the multi-pulse converters, the main switches are still formed by a great number of series-connected semiconductor devices such that it can withstand very high voltage levels. As a result, to avoid asynchronous switching problems for the series-connected semiconductor devices, this converter must operate at very low switching frequency, which varies from line frequency up to a few hundred Hertz.

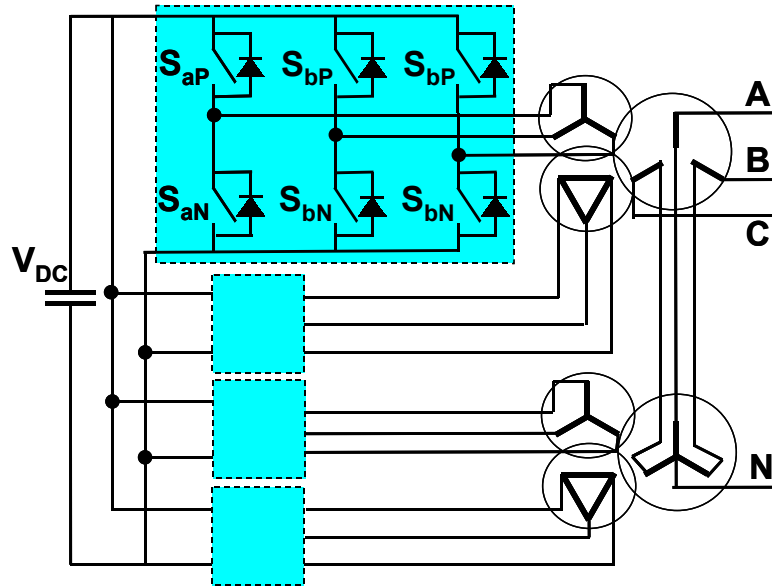


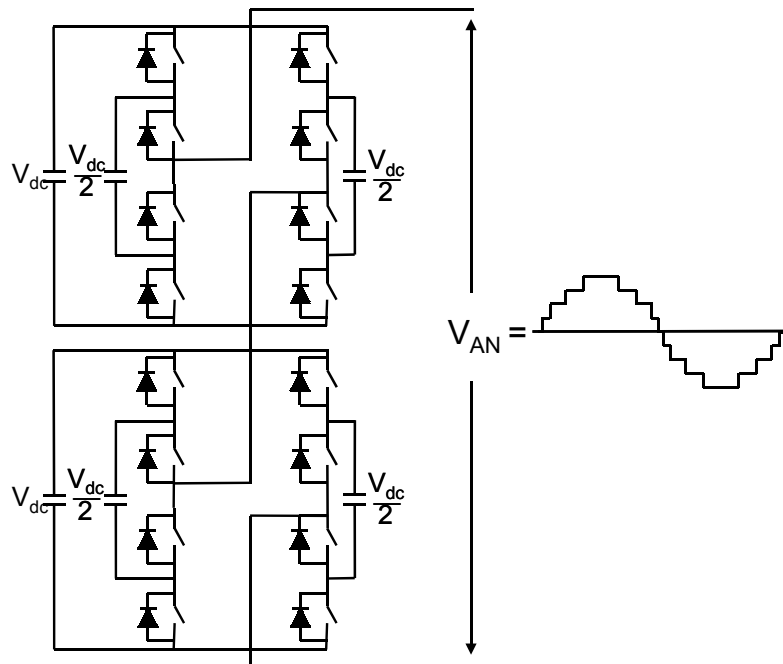
Figure 2-12. A 24-pulse converter.

B. Mixed-Level Cascaded Converters

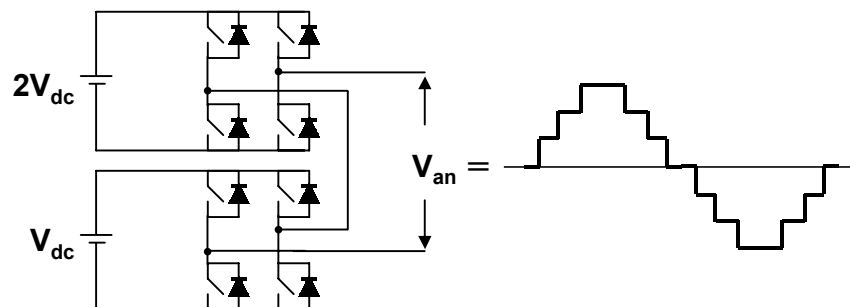
Due to the attractive modularity feature of this topology, the CMC can be modified by replacing its conventional two-level converters with multilevel converters in the first category [F8]. This emerging multilevel converter is called a mixed-level cascaded converter. A nine-level hybrid multilevel VSC is shown in Figure 2-13(a). This hybrid converter employs a two-phase, three-level flying-capacitor converter to form a five-level H-bridge converter. Thus, to synthesize a nine-level voltage waveform, only two DC buses are enough, whereas four DC buses are used in the conventional CMC.

Another interesting type of this converter topology is the so-called asymmetric CMC [F9]. Instead of using an identical DC link for every H-bridge converters, different DC links can be used to synthesize a greater number of output voltage levels. To determine the voltage levels among different DC links, a binary system can be effectively used, i.e., $1V_{dc}$, $2V_{dc}$, $4V_{dc}$, ..., $2^{(N-1)}V_{dc}$, where N is the number of H-bridge converters in one phase leg. The maximum number of the synthesized voltage levels can be up to $\sum_{i=1}^n 2^i + 1$. To further improve the output-voltage

quality, the switching frequency of the lower-voltage H-bridge converter, which utilizes low-voltage semiconductor devices such as IGBTs, can be higher than that of the higher-voltage one, which employs high-voltage, low-speed semiconductor devices. The effective switching frequency thus increases.



(a)



(b)

Figure 2-13. Hybrid multilevel converters and their output waveforms: (a) mixed-level hybrid multilevel converters and (b) asymmetric cascaded-multilevel converters.

III. Comparison among Multilevel Converters for STATCOM Applications

In the case of the multi-pulse converter, as shown in Figure 2-12, its complicated magnetic circuit makes the system less attractive after the multilevel converters emerge as an alternative. Because of the low-quality output voltage of two-level converters, the magnetic circuit or zigzag transformer is utilized in the multi-pulse topology in order to suppress low-order harmonic components. This transformer is the most expensive equipment in the system. It occupies 40% of the total real estate and, more importantly, produces about 50% of the total loss of the system. Moreover, besides the complex zigzag transformer, a set of low-pass filter circuits is still needed in the 24-pulse converter. To avoid this additional filter circuit, a greater number of voltage pulses is required. By combining two 24-pulse converter circuits together, a 48-pulse converter can be achieved. With a sufficiently high number of voltage levels, the 48-pulse converter can synthesize clean sinusoidal output voltage using a relatively small filter circuit. However, the total cost is increased. As an alternative to the multi-pulse converters, the multilevel converters can appropriately replace the existing system that uses traditional multi-pulse converters, as shown in Figure 2-12, without the need for those harmonic-reduction transformers.

Without series semiconductor devices or specially designed magnetic circuits, multilevel converters have rapidly become increasingly attractive in high-voltage applications such as the STATCOM. Because of their multi-step output-voltage waveforms, the THD of the multilevel converter voltages is relatively low. A harmonic-free sinusoidal voltage waveform can be achieved when the number of voltage levels approaches infinity. Moreover, the effective switching frequency of the multilevel converters is also a function of its number of voltage levels. The higher the number of voltage levels, the higher the effective switching frequency. In other words, to achieve the same voltage THD, a higher-level converter can operate at a lower switching frequency than can lower-level converters. As a result, high-quality output voltage and high efficiency can be simultaneously realized in the multilevel converter topologies. Besides its premium-quality output voltages, a multilevel converter with a sufficiently high voltage level can directly connect to a medium-voltage power network, 13.8 kV for example, without requiring step-up transformers. In a STATCOM system, only small linear reactors are needed to serve as a current filter and a reactive power coupler.

Obviously, the superiority of a multilevel converter is proportional to its number of its voltage levels. However, the number of voltage levels is limited by control complexity, complication of the system structure, and cost-ineffectiveness.

Four mature multilevel VSCs have been researched and developed: DCMC, FCMC, P2MC and CMC. These converter topologies are compared in terms of the feasibility of their utilization in STATCOM applications.

The number of components needed in each system is firstly compared. According to the MIL-HDBK-217F standard, the reliability of a system is indirectly proportional to the number of its components. Table 2-8 compares the main power component requirements per phase leg among these four multilevel VSCs, where m is the number of voltage levels. In Table 2-8, the number of main switches and main diodes needed by each converter to achieve the same number of voltage levels is the same except for the P2MC. The P2 five-level converter, for example, requires 20 main switches and 20 anti-parallel diodes, while the other multilevel converters need only eight switches and eight diodes.

Clamping diodes are not required in the FCMC, P2MC and CMC, while balancing capacitors are not needed in the DCMC and CMC. Figure 2-14 shows the total required components in the multilevel converters as a function of the number of voltage levels. Although the same number of main switches and diodes is needed in the CMC, FCMC and CMC, the total numbers of components needed in these three topologies are totally different at higher voltage levels. In the entire voltage range, the P2MC unquestionably requires too many components as compared to the others; therefore, it does not qualify for use with high numbers of voltage levels. As shown in Figure 2-14, to synthesize the same number of voltage levels, the CMC requires the least number of total main components. Even though the CMC needs more capacitors as compared to those needed in the DCMC, this is not considered to be a disadvantage in STATCOM applications. In contrast, the CMC topologically also supports energy storage system integration. An ultra capacitor bank or a fuel cell module, for example, can be individually integrated with each H-bridge converter to enable real power compensation capability in a STATCOM system.

TABLE 2-8. COMPARISON OF POWER COMPONENT REQUIREMENTS PER PHASE LEG AMONG THREE MULTILEVEL CONVERTERS.

Converter Configuration	DCMC	FCMC	P2MC	CMC
Main Switching Devices	$2(m-1)$	$2(m-1)$	$m(m-1)$	$2(m-1)$
Main Diodes	$2(m-1)$	$2(m-1)$	$m(m-1)$	$2(m-1)$
Clamping Diodes	$(m-1)(m-2)$	0	0	0
DC Bus Capacitors	$m-1$	$m-1$	$m-1$	$(m-1)/2$
Balancing Capacitors	0	$(m-1)(m-2)/2$	$(m-1)(m-2)/2$	0
Total	$m^2 + 2m - 3$	$(m^2 + 8m - 8)/2$	$(5/2)m(m-1)$	$(9/2)(m-1)$

Another dominant advantage of the CMC is circuit layout flexibility. Modularized circuit layout and packaging is possible in CMC topology, because each level has the same structure, and there are no extra clamping diodes or voltage-balancing capacitors, which are required in the DCMC and the FCMC. The number of output voltage levels can then be easily adjusted by changing the number of full-bridge converters.

For the more-than-three-level configuration used in the STATCOM application, the DCMC voltage-imbalance problem cannot be overcome by utilizing control techniques only [13]. Either oversized capacitors or complex balance circuits are absolutely required. This makes the DCMC unsuccessful in high-voltage var-compensation applications.

In the FCMC topology, an unacceptable amount of capacitance is required for high voltage levels. In the flying-capacitor seven-level converter, for example, 15 clamping capacitors plus six DC-link capacitors are required per phase to achieve the same voltage rating yielded by utilizing three capacitors in the CMC topology. This is unacceptable. Not only do these many capacitors make the system less cost-effective, but they also induce a severe voltage-imbalance problem in the transient period and at the steady state.

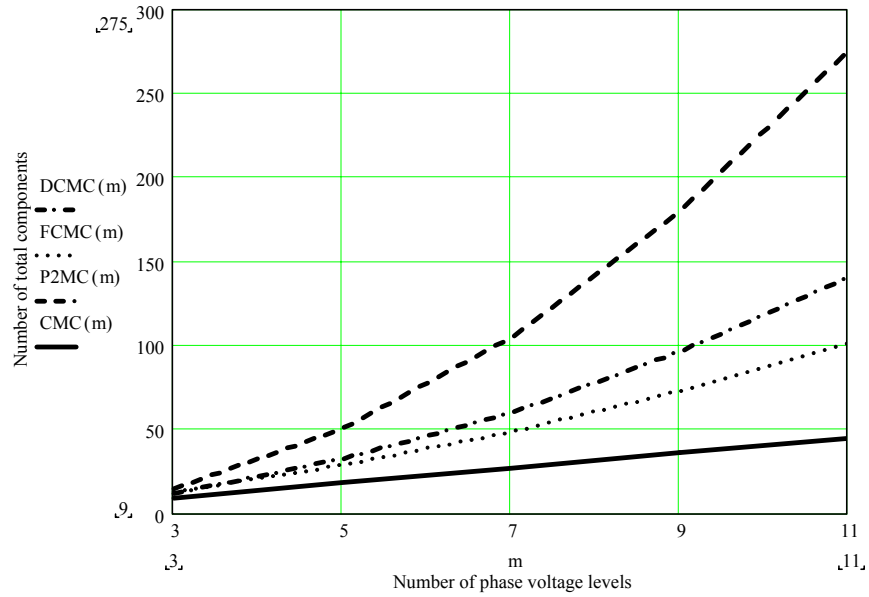


Figure 2-14. Number of components required in the multilevel converters as a function of the number of voltage levels.

2.4 Conclusion

In conclusion, among the mature multilevel converter topologies, the cascaded-multilevel VSC is the most promising alternative for the STATCOM application. It requires the least number of components to achieve the same number of output voltage levels. With its modularized structure, the CMC can flexibly expand the output power capability and is favorable to manufacturing. Moreover, redundancy can be easily applied in the CMC to enhance reliability for the entire system.

Control complexity of the CMC is, however, directly proportional to the number of H-bridge converters. In the STATCOM application, the AC voltage of each H-bridge converter is derived from its DC capacitor voltage, which needs to be individually regulated. As the number of voltage levels increases, the voltage-imbalance problem becomes more of a concern. To achieve

as stable a system as possible, a well-defined model and an effective DC-link-balancing method are necessary.

Chapter 3 DESIGN APPROACH FOR CMC POWER STAGES AND PASSIVE COMPONENTS IN STATCOM SYSTEMS

In general, a STATCOM system can be divided into three key parts: the converter power stage, the passive components and the control system. As presented in Chapter 2, several multilevel converter topologies have been developed to demonstrate their superiority in high-voltage applications. In summary, the most promising topology among them is the CMC. Serving as a basic unit in the CMC, the H-bridge converter makes the CMC-based STATCOM much more modular and flexible in terms of power capability. A well-designed H-bridge converter therefore plays an important role in maximizing the performance and improving the cost-effectiveness of such a system. This chapter presents a 1.5MVA H-bridge building block (HBBB) that uses ETOs to demonstrate its superior performance and concept of modularity. The modular HBBB is intended to be used in high-power CMCs for reactive power compensation applications, particularly the STATCOM. Because of their identical layouts, the HBBBs are simply manufactured for both the building block itself and for the entire system. Whenever the power capability requirement of the system needs to be changed, HBBBs are simply added into or taken away from the system without redesigning the HBBB component ratings. The hardware configuration as well as component selection and design of the HBBB are presented. A new air-core snubber inductor design, which lowers losses and is lighter-weight than the conventional iron-core inductor, is proposed. An ETO-based 1.5MVA HBBB prototype has been implemented and tested in both buck converter and inverter modes. Experimental results indicate that the proposed ETO-based HBBB with the snubber components operates effectively at high frequencies and high power levels.

Besides the key components, such as the HBBBs, the passive components used in the CMC-based STATCOM also dictate the performance of the entire system. The reactive component requirement criteria for reactive power compensations have been investigated. Two key passive components that are included in this study are the coupling inductors and the DC capacitors. The results of this research lead to optimized design processes. With the proposed HBBB and

optimized passive components, a cost-effective, high-performance CMC-based STATCOM system is, therefore, achieved.

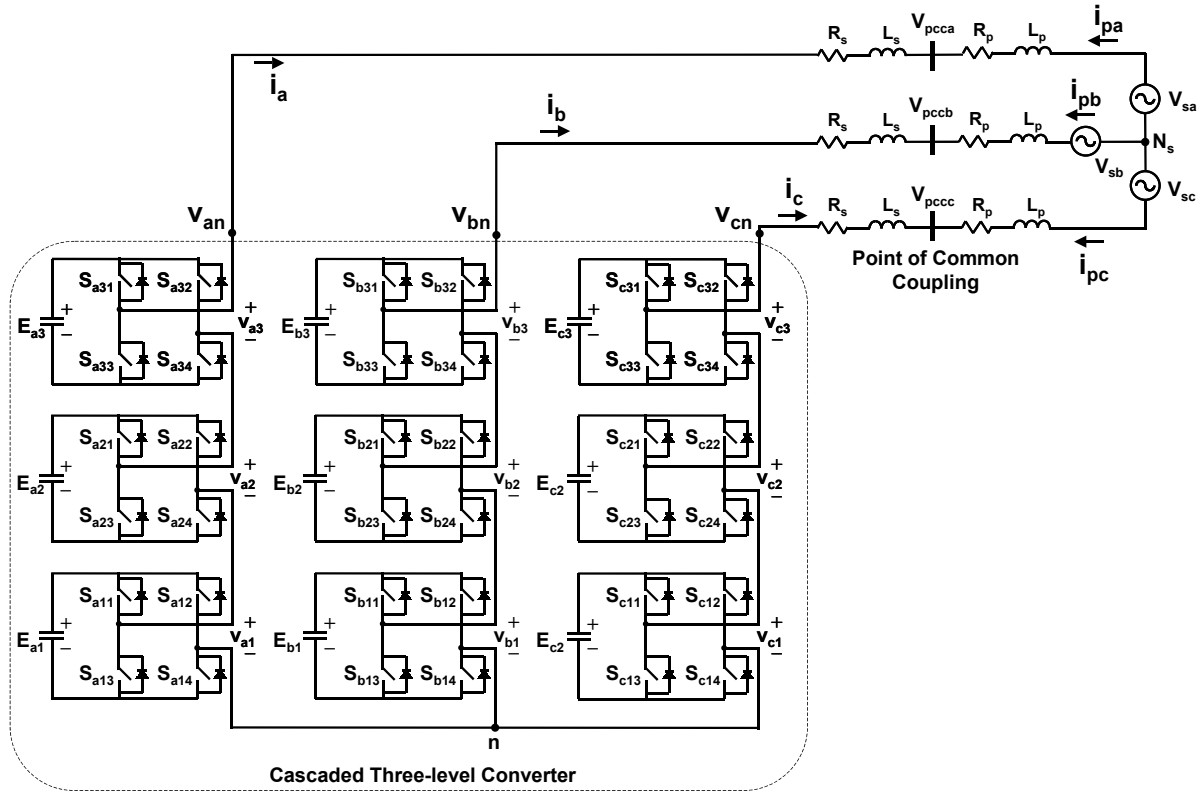


Figure 3-1. A Y-connection, seven-level cascaded converter connected to the power system via coupling inductors.

3.1 H-Bridge Building Block: A Basic Unit of the CMC

I. Introduction

Multilevel converters have recently become an important technology in high-power applications, especially for FACTS devices. With converter modules in series, and with balanced voltage-sharing among them, lower-voltage switches can possibly be used in high-

voltage systems. Thus, the low-voltage-oriented IGBT devices can be stacked for medium-voltage systems. For higher-voltage applications, however, efforts have seldom been made to use GTO-based devices for multilevel converters.

As a basic unit in the CMC topology, a 1.5MVA HBBB, using the newly developed ETO thyristor, is proposed and implemented to demonstrate the modularity concept of the HBBB for high-frequency, high-power applications. The proposed HBBB can be used to form a CMC for reactive power compensations such as in a shunt compensator and in a series compensator. By electrically connecting these identical building blocks, the CMC topology can be straightforwardly implemented. Thanks to their identical layouts, the HBBBs are easily manufactured not only for the module itself but also for the entire system. The challenges for such a high-power building block, however, are their component design and selection and the hardware configurations of electrical connections and snubber components. In the proposed design, low-inductance, high-voltage film capacitors and air-core inductors were selected and designed for long-term reliability considerations. The DC bus capacitor current capability was calculated based on the negative-sequence current requirement. The air-core inductor was designed to avoid saturation under fault conditions. In addition, an ETO-based DC circuit breaker serves as a local over-current protection. The design procedure will be provided, and the experimental results of the HBBB prototype tested in buck converter mode and inverter mode, will be presented.

It is clear from Figure 3-1 that an HBBB, which consists of an H-bridge converter and a DC power source, is a common part in a reactive power compensation application that uses a cascaded-multilevel VSC. The specifications for the power stage of the proposed ETO-based H-bridge converter are given in Table 3-1. At the full load, the H-bridge converter is capable of operating at a bus voltage of 2.1 kV and an output RMS current of 1.25 kA. The power capability is approximately 1.5 MVA, and is determined by the thermal and electrical capabilities of four 4kA/4.5kV ETOs.

TABLE 3-1. THE SPECIFICATIONS FOR THE PROPOSED ETO-BASED HBBB.

Main Device	4kA/4.5kV ETO
Rated Bus Voltage	2.1 kV
Rated Output RMS Current	1.25 kA
Switching Frequency	Up to 2 kHz
Power Capability	1.5 MVA

II. Emitter Turn-off Thyristor

The ETO is a new type of MOS-controlled thyristor that is suitable for use in high-power converters due to its improved switching performance and simple control [K1]-[K3]. Compared to the conventional GTO, the ETO is turned off under hard-driven conditions; therefore, it has a much shorter storage time. Due to its configuration, the ETO is a voltage-controlled power device with a large reverse-biased safe operation area (RBSOA). The ETO also has a built-in over-current protection function. This works without any additional current sensors. These combined advantages make the ETO-based power system simpler in terms of the required dv/dt snubber and the system's over-current protection, both of which result in significant savings in overall costs. Compared to the gate power requirement of the GTO, the ETO gate driver requires much lower power. Furthermore, the integrated ETO gate driver provides minimum on-time and off-time control, flexible controller interface, and on-board power supply and current protection. The equivalent circuits of the ETO and its electrical symbol are shown in Figure 3-2(a) and (b), respectively. An ETO is realized by integrating a GTO with an emitter switch Q_E and a gate switch Q_G . During the normal forced turn-off transient, Q_E is turned off and Q_G is turned on. The GTO cathode current is totally bypassed via switch Q_G before the anode voltage begins to rise. In this way, the thyristor latch-up is broken, and the ETO is turned off under the hard-driven condition. During the turn-on transient, Q_E is turned on and Q_G is turned off. A high-current pulse is injected into the GTO's gate to reduce the turn-on delay time and to improve the turn-on di/dt rating. Figure 3-2(c) shows a photograph of a 4kA, 4.5kV ETO with an integrated gate driver, which is used as a main switch in the proposed HBBB. This ETO can block forward voltage of 4.5 kV and can interrupt a maximum anode current of 4 kA.

III. Snubber Arrangement Operation

Although the ETO has the snubberless turn-off capability, a small dv/dt snubber circuit is required to reduce the switching loss and to increase the long-term switch reliability. In addition, because of the poor performance of the high-power diode, its reverse recovery increases the stress on the ETO. As a result, the di/dt limitation is needed to reduce such switch stress. The snubber topology employed for each phase leg in the HBBB was proposed by McMurray [K4] and is shown in Figure 3-3. The McMurray snubber has several advantages over others. Firstly, the McMurray snubber arrangement reduces the size of the snubber and minimizes the number of snubber components. It is applicable and optimal for the converter phase legs, where the switching devices are subject to high levels of turn-on and turn-off stresses. In addition, the McMurray snubber circuit is now very mature and has been applied in many power electronics circuits. In Figure 3-3, S_1 to S_4 are the main switches, and D_1 to D_4 are the main anti-parallel diodes or freewheeling diodes. The snubber circuit comprises shunt capacitors C_{SX} , auxiliary diodes D_{SX} , series inductances L_{SX} , and a discharge resistor R_{SX} , where X is 1 to 4.

To explain how the snubber circuit works, a phase leg of the circuit shown in Figure 3-3 is used as an example, and is sequentially depicted in Figure 3-4. The thick lines shown in Figure 3-4 indicate that those components actively conduct current during that period of time. In this example, the sequence for the commutation of the load current from the bottom anti-parallel diode to the main top switch is illustrated in Figure 3-4(a) through (e). The corresponding current and voltage waveforms of the top switch are shown in Figure 3-5(a). Figure 3-4(f) through (h) then shows the return commutation of the load current from the main top switch to the bottom anti-parallel diode, and the corresponding top-switching current and voltage waveforms are illustrated in Figure 3-5(b). In Figure 3-4(b) through (d), the intermediate sequence depicts the operation of the snubber arrangement to relieve the turn-on stress of the main switch. On the other hand, Figure 3-4(f) through (h) shows the operation of the snubber component used to relieve the turn-off stress of the main switch. The next step after that, as shown in Figure 3-4(h), will repeat the one shown in Figure 3-4(a). This completes one cycle of operation in the switching mode of a reversible DC converter.

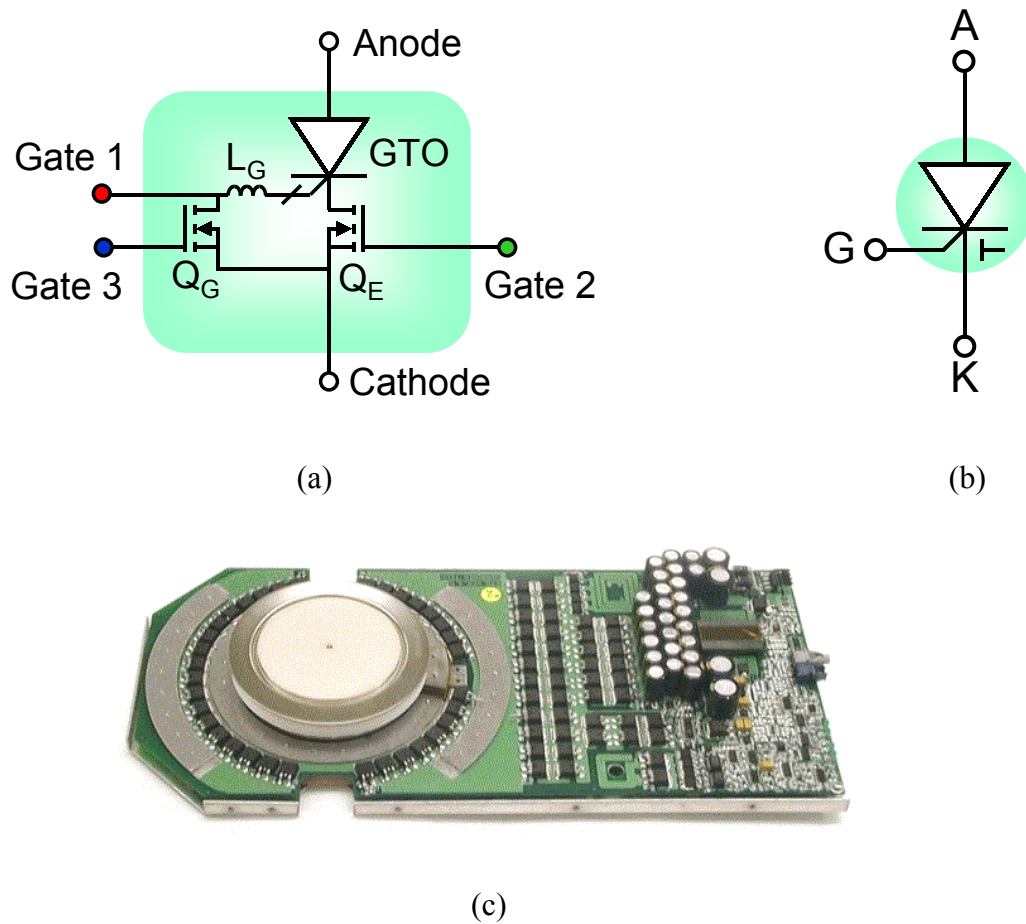


Figure 3-2. (a) Equivalent circuit of the ETO, (b) the ETO symbol and (c) a photograph of the newly developed 4kA/4.5kV ETO4045A.

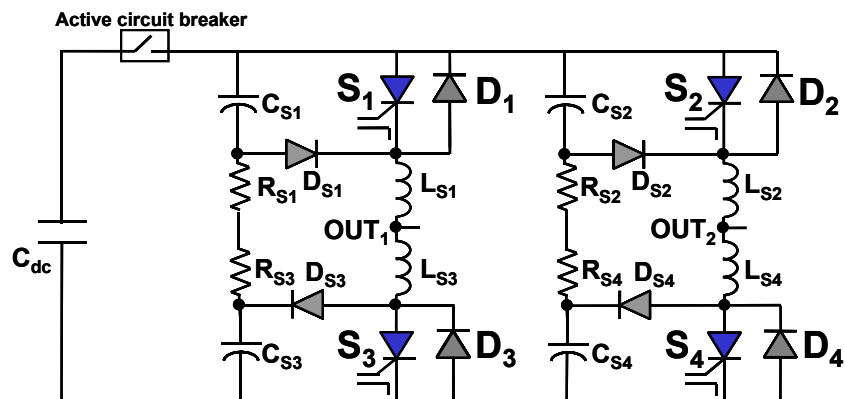


Figure 3-3. Schematic of the proposed ETO-based H-bridge building block.

In the HBBB prototype, the snubber components consist of four shunt capacitors C_S , four auxiliary diodes D_S , two series inductances L_S , and four discharge resistors R_S , where N is 1 to 4. For a shunt capacitor C_S , a 0.5mF/4.5kV film capacitor from ICAP is used. Diode 10H4502 from ABB is employed for auxiliary diodes D_S . A 0.25W press resistor is used as discharge resistor R_S .

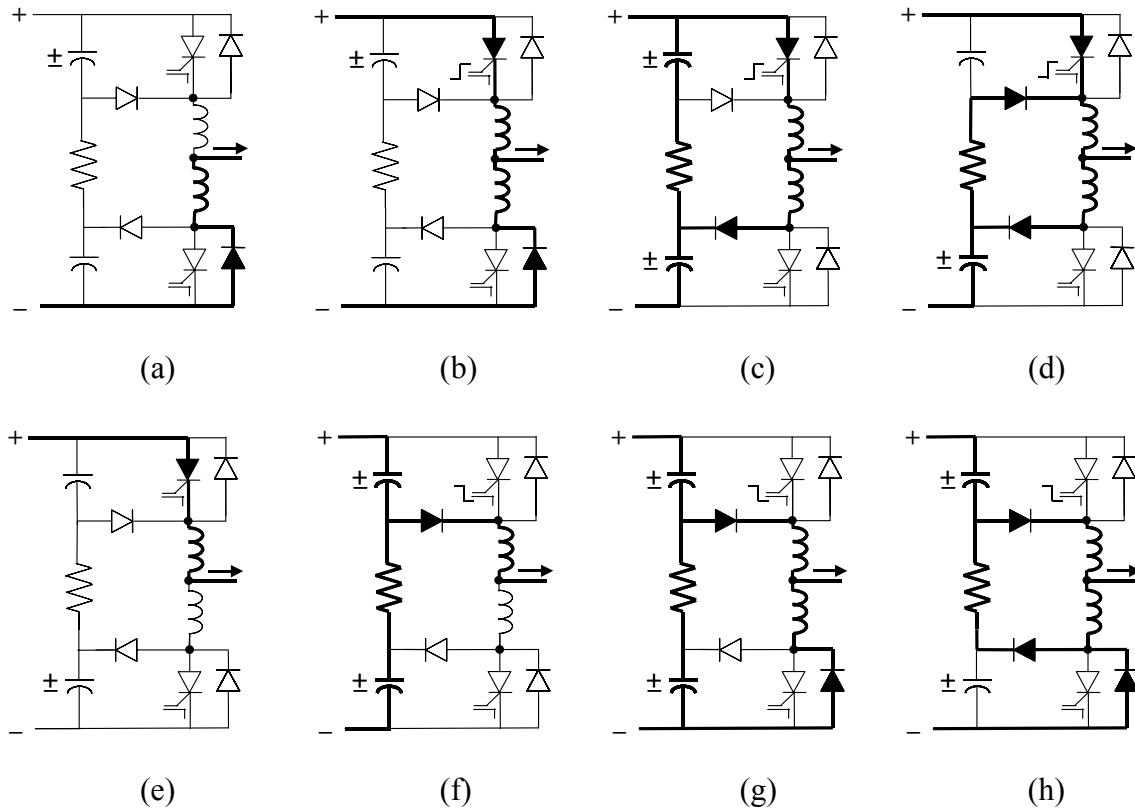


Figure 3-4. Snubber operation for one switching cycle: (a) t_0-t_1 , (b) t_1-t_2 , (c) t_2-t_3 , (d) t_3-t_4 , (e) t_4-t_5 , (f) t_5-t_6 , (g) t_6-t_7 , and (h) t_7-t_8 .

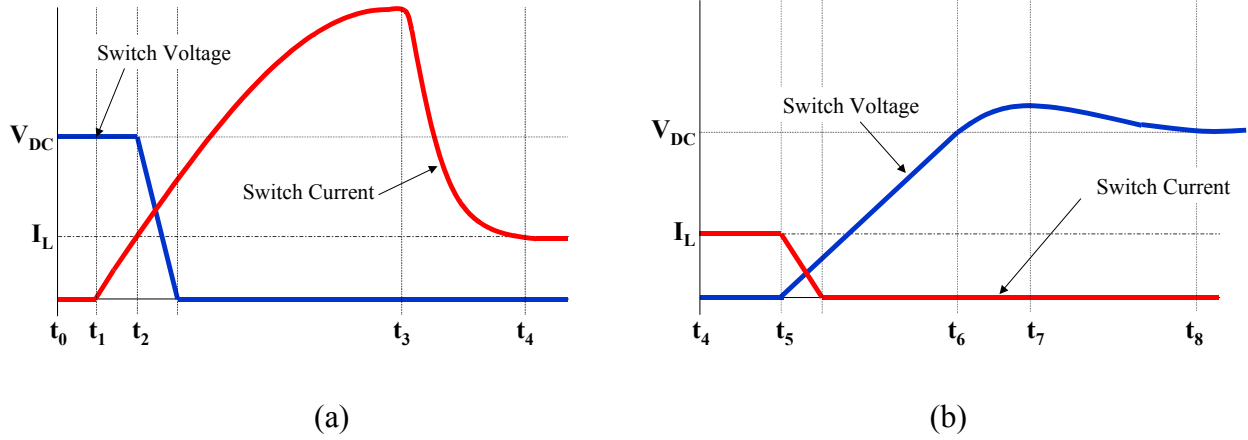
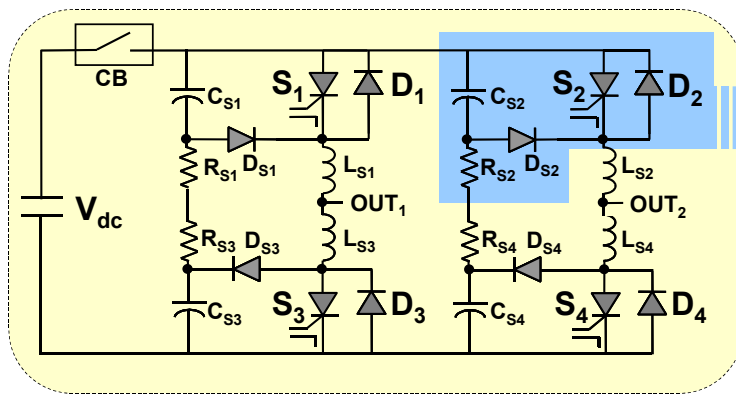


Figure 3-5. Top-switch voltage and current waveforms during the (a) turn-on and (b) turn-off process corresponding to the snubber operation.

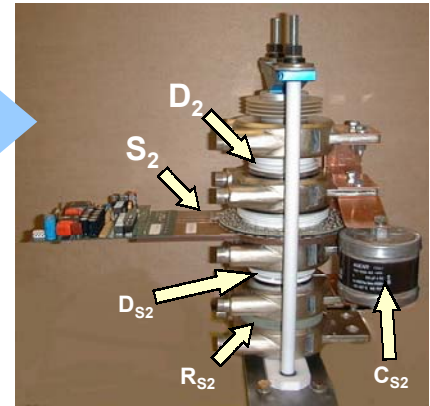
IV. Layout Considerations

To optimize the HBBB structure, several issues need to be considered. The building-block concept is applied to the layout of the HBBB so that it can be simply manufactured. To achieve high power density, the layout is designed to be as compact as possible. To minimize the voltage overshoot in the output waveform that results in the main-switch voltage stress, the stray inductance in the layout must be kept as small as possible. Hence, the H-bridge converter must be as close as possible to the DC capacitor bank. Similarly, the capacitor snubber loop must be as small as possible.

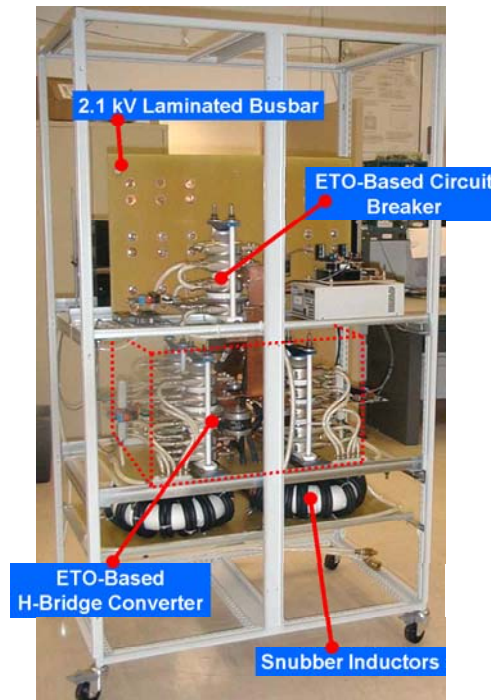
To simplify and modularize the structure of the building block, the H-bridge circuit shown in Figure 3-6(a) is divided into four identical quarter H-bridges. The structure of a quarter H-bridge shown in Figure 3-6(b), for example, consists of a main switch S_2 , an anti-parallel diode D_2 , a snubber capacitor D_{S2} , and a discharge resistor R_{S2} . To form an H-bridge converter, four-quarter H-bridge stacks are electrically connected by copper connectors. A DC capacitor bank and the snubber inductors are then connected to the H-bridge converter to complete an HBBB, as shown in Figure 3-6(c). For reactive power compensation, the DC sources in the HBBB mainly supply or absorb only the reactive power between the power system and the converter; therefore, there is no need for DC power supplies other than the DC capacitors.



(a)



(b)



(c)

Figure 3-6. Structure of the H-bridge building block: (a) schematic, (b) quarter H-bridge structure and (c) HBBB prototype.

After a quarter H-bridge stack is completely implemented, an insulation test is conducted. Figure 3-7 illustrates two critical insulation breakdown spots in the quarter H-bridge stack. The most critical point is spot A, where the ETO is most adjacent to the threaded rod of the clamp.

Teflon that is 0.0625 inches thick is used as an insulator between the ETO and the clamp. The breakdown voltage is measured using SERIES HIPOT & MEGOHMETER. At spot A, the breakdown voltage is 4.5 kV. Spot B, where the bottom heat sink is the closest to the chassis metal bar, breaks down at over 6 kV. Again, Teflon is used as an insulation material. Its thickness is 0.5 inches.

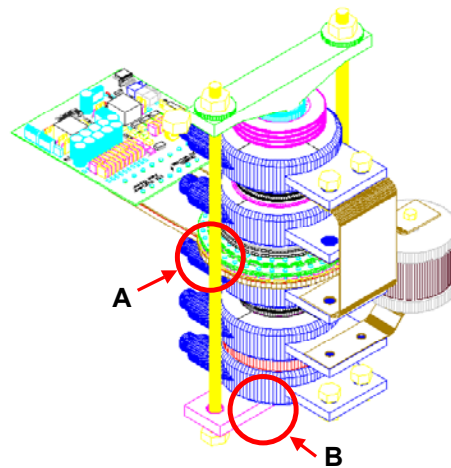


Figure 3-7. Two critical insulation breakdown spots in the quarter-HBBB structure.

V. Snubber Inductor Design

During the turn-on process, the di/dt of the main switch current is mainly limited by the snubber inductor network. The top and bottom ETOs of the same phase leg share the same di/dt snubber. The schematic of the snubber inductors is shown in Figure 3-8(a). To increase the total inductance of the snubber inductors, two series inductors, L_{S1} and L_{S2} , each having a self-inductance of L_S , are magnetically coupled with a mutual coefficient of k . Thus, the total series inductance is $2L_S(1+k)$. To avoid saturation and core losses, it is desirable to use the air core. Compared to the conventional iron-core inductor, the air-core inductor is expected to allow lower losses and to be lighter-weight [L1]. The previous configuration [L1] tends to radiate the field and interfere with the electronic circuit. The preferred configuration involves adopting the toroid to contain the field inside the circle, as shown in Figure 3-8(b). To achieve a better coupling

coefficient, both windings are interleaved along the complete toroid, with the end of the L_{S1} winding tied to the beginning of the L_{S2} winding. From electromagnetic theory [L2], the self-inductance and the mutual inductance of the toroid-type inductor, whose two-dimensional structure is shown in Figure 3-8(c), can be given as Equation 3-1 and Equation 3-2, respectively:

$$L_{S1} = \frac{\mu_o \cdot N_1^2 \cdot S \cdot m}{2 \cdot \pi \cdot b}, L_{S2} = \frac{\mu_o \cdot N_2^2 \cdot S \cdot m}{2 \cdot \pi \cdot b}, \text{ and}$$

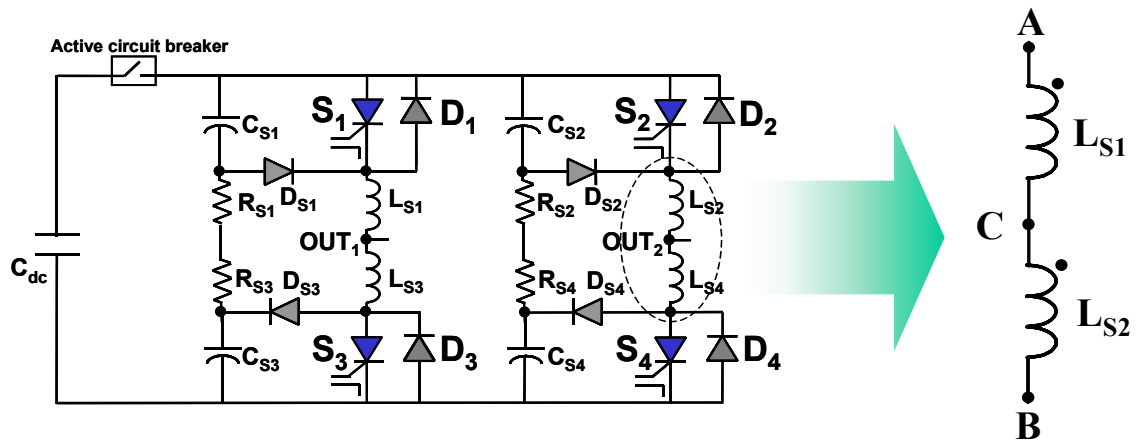
Equation 3-1

$$L_{SM} = \frac{\mu_o \cdot N_1 \cdot N_2 \cdot S \cdot m}{2 \cdot \pi \cdot b},$$

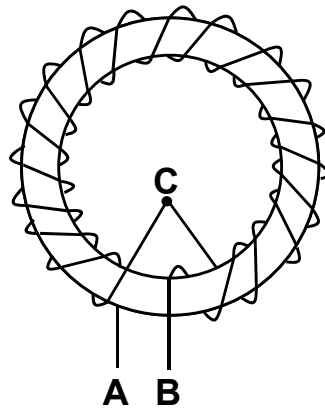
Equation 3-2

where μ_o is the permeability of air, which is $0.4\pi \mu\text{Hm}^{-1}$, N_1 and N_2 are the number of turns for windings 1 and 2, respectively, S is the cross-section of the toroid, b is the mean radius, and m is the non-ideal factor, which varies from 0 to 1.

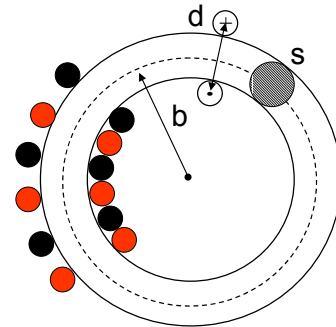
The snubber is designed to limit the di/dt of the ETO anode current at 100 A/ μs . For the designed bus voltage of 2 kV, the required total inductance is 20 mH. To withstand 1kA load current, the 2/O-AWG wire with an external diameter of 2 cm is used for both L_{S1} and L_{S2} windings. From Equation 3-1, Equation 3-2 and Figure 3-6(c), given 15 turns for both windings and 0.5 for the non-ideal factor, the calculated parameters d and b are thus 5 inches and 5.7 inches, respectively. An inductor prototype, as shown in Figure 3-9, is then fabricated based on the preceding calculation. Based on the five measurements given in Table 3-2, the average values of the inductances are $L_{S1} = 6.62$ mH, $L_{S2} = 6.16$ mH, and $L_{A-B} = 19.64$ mH, all of which are consistent with the calculated values. The coupling coefficient k is 54%. From several prototype measurements, the k value can be improved by making both windings as close to each other as possible and by reducing the size of the wire. Compared to the previous configuration [L1], the proposed toroidal configuration not only avoids field radiation, but also improves the coupling coefficient. The proposed coupling inductor is thus suitable for high-power converter applications.



(a)



(b)



(c)

Figure 3-8. The proposed air-core coupling snubber inductor: (a) schematic, (b) structure and (c) cross-section.



Figure 3-9. The air-core snubber inductor prototype.

TABLE 3-2. THE MEASURED INDUCTANCE OF THE SNUBBER INDUCTOR PROTOTYPE.

	#1	#2	#3	#4	#5	Average
L_{S1}	6.87	6.75	6.43	6.75	6.32	6.62
L_{S2}	5.98	6.05	6.20	6.04	6.53	6.16
L_{A-B}	19.4	18.95	19.26	18.94	21.66	19.64

VI. The DC Capacitance Requirement

Figure 3-10 illustrates the voltage, current, and voltage ripple of the DC capacitor of an H-bridge converter in reactive power compensation. At high-switching-frequency operation with a proper output filter, the load current and output voltage of the converter may be assumed to be sinusoidal with a small amplitude of surplus harmonics. Consequently, only the fundamental components of both voltage and current are considered. Generally, the relationship of the capacitance, total charge and ripple voltage can be given as follows:

$$C_{dc} = \frac{Q}{\Delta V_{dc}}.$$

Equation 3-3

As shown in Figure 3-10, the maximum ΔV_{dc} occurs in the period of $\pi/4$. The total Q , the area under the current waveform up to $t = \pi/4$, can then be expressed as follows:

$$Q = \int_{\frac{a \cos(\frac{M\pi}{4})}{2\pi f}}^{\pi/4} \sqrt{2} \cdot I_{RMS} \cdot \cos(2 \cdot \pi \cdot f \cdot t) dt,$$

Equation 3-4

where I_{RMS} is the converter RMS current, f is the fundamental frequency, and M is the modulation index.

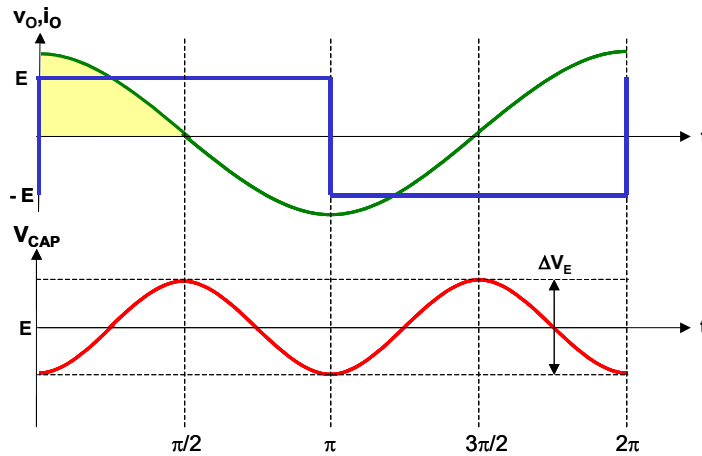


Figure 3-10. Fundamental components of the output voltage, current, and voltage-ripple waveform for the DC capacitor of the H-bridge converter.

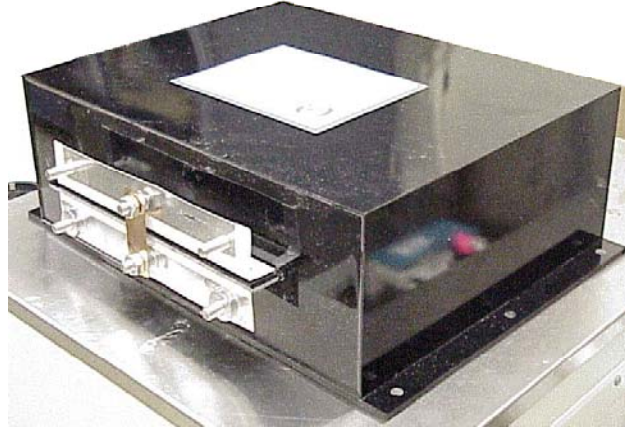


Figure 3-11. The customized film capacitor for the DC bus.

Substituting Equation 3-4 into Equation 3-3, the minimum DC capacitance requirement thus becomes

$$C_{dc_cascade} = \frac{I_{RMS}}{\sqrt{2} \cdot \pi \cdot f \cdot \Delta V_{dc}} \left[1 - \sin\left(\arccos\left(\frac{M\pi}{4}\right)\right) \right].$$

Equation 3-5

For a given ΔV_{dc} and operating RMS current, the DC capacitance requirement for the system can be determined using Equation 3-5. An HBBB that can compensate the 60Hz-1250A reactive current with 10% allowable ripple voltage at 2.1kV bus, for example, requires a minimum DC capacitance of 8.5 mF and operates at the maximum modulation index of 1. To provide a sufficient voltage margin, the voltage rating of the designed DC capacitor is selected to be 2.5 kV. In the proposed HBBB, the customized polypropylene film capacitors in a thermo-plastic housing are employed, and are connected in series to form a DC bus. Figure 3-11 shows the designed film capacitor unit, the rating of which is 850 mF, 2.5 kV, and 740 A_{RMS}. The detailed specifications are shown in Table 3-3.

TABLE 3-3. CAPACITOR SPECIFICATIONS.

Nominal Capacitance	850.0 μF
Tolerance	+/- 10%
DC Voltage Rating	2.5 kV
E.S.R	< 0.001 Ω
Inductance	20 nH
Maximum Peak Current	55.0 kA
DV/DT	70 V/ μs

VII. Active Circuit Breaker

Without the over-current protection, if a shoot-through fault occurs in the phase leg of switches S_1 and S_3 , as shown in Figure 3-6(a), the energy on the DC bus capacitor will be dumped through these two switches. The switches as well as the DC capacitors will probably be destroyed, because the fault current increases very rapidly to an extremely high level, at a rise rate dictated only by the bus voltage and di/dt snubber inductance. With the DC circuit breaker, once the fault current reaches the threshold level, the over-current protection is triggered and the fault current is cut off after a delay time.

Due to its fast switching speed, snubberless turn-off capability, and built-in current sensing, the ETO is also a superior high-power semiconductor device suitable for use in DC circuit breakers. Like a high-speed fuse in a high-power system, the ETO-based DC circuit breaker is installed between the energy-storage component and the positive busbar of the HBBB.

A. Built-In Current Sensing

When the ETO is gated “on,” the gate switch Q_G is “off” and the emitter switch Q_E is “on,” Q_E appears as a small resistor and Q_G behaves like a diode, since both Q_E and Q_G are formed by paralleling many low-voltage, high-current power MOSFETs in order to improve the current capability, as shown in Figure 3-12. Thus, the voltage drop across Q_E can be used as an indicator of device current, since the voltage across Q_E increases somewhat linearly with the device current, as experimentally shown in Figure 3-13. At higher temperatures, the voltage on Q_E will increase because the MOSFET has a positive temperature coefficient during the on state.

Although the voltage on Q_E results in an increased conduction loss for the ETO, the additional conduction loss is usually kept below 10% of the total conduction loss by paralleling many power MOSFETs.

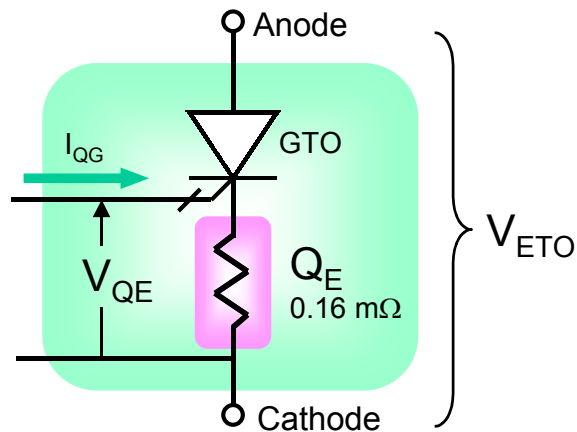


Figure 3-12. Equivalent circuit of the ETO4045TA during the on state.

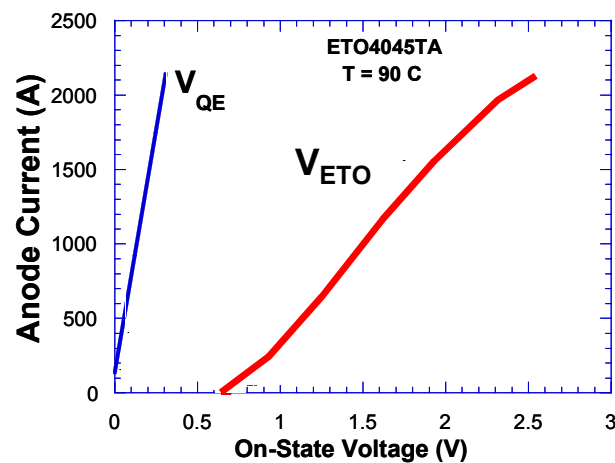


Figure 3-13. On-state characteristics of the ETO at $T = 90^{\circ}\text{C}$.

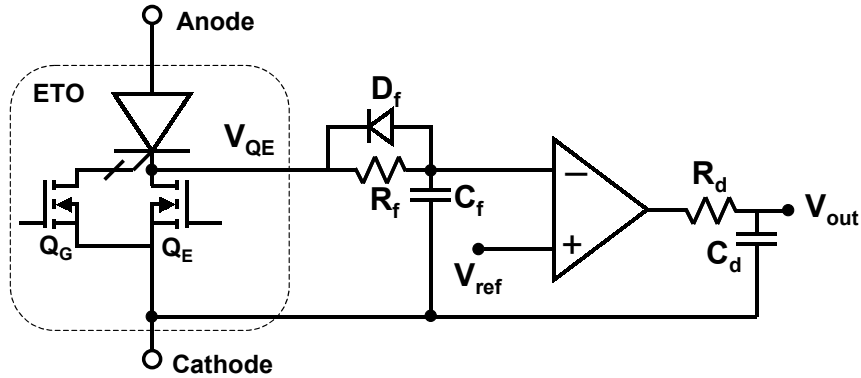


Figure 3-14. ETO gate-drive circuit for over-current protection.

B. ETO Gate-Drive Circuit for Over-Current Protection

The ETO's gate-drive circuit for over-current protection is shown in Figure 3-14. The voltage across Q_E (V_{QE}) is first filtered by R_f and C_f , and is then sent to the analog comparator to be compared with the reference voltage V_{ref} , which represents the setting current. Once V_{QE} is larger than V_{ref} , indicating that the device current is higher than the setting current, the comparator will change its output from high to low logic levels. After a delay of about $3 \mu s$, as dictated by R_d and C_d to prevent the false trigger, the device is turned off in order to cut off the fault current.

Figure 3-15 shows the schematic of the DC circuit breaker prototype based on the 4kA/4.5kV ETO. To improve the reliability and to reduce the turn-off loss, an RC snubber is employed to limit dv/dt . The snubber resistor R_C is 1.0 W, and the snubber capacitor C_C is 1.0 μF . A 2kA/4.5kV freewheeling diode parallels with the ETO to provide the reverse conduction path. With double-sided water-cooling, the designed circuit breaker prototype can handle the average current of 1.5 kA. As shown in the test results given in Figure 3-16, the circuit breaker is set to interrupt the 2kA main current (anode current) and the 2.1kV bus voltage (anode voltage). After the fault current reaches this setting, the circuit breaker takes about $7.5 \mu s$ to complete the

process. In this way, the maximum fault current is controlled within a safe level, and system destruction is prevented.

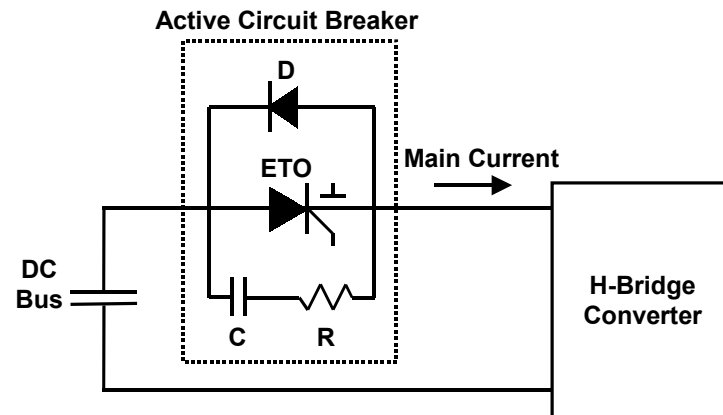


Figure 3-15. The ETO-based circuit breaker installed to protect the H-bridge converter.

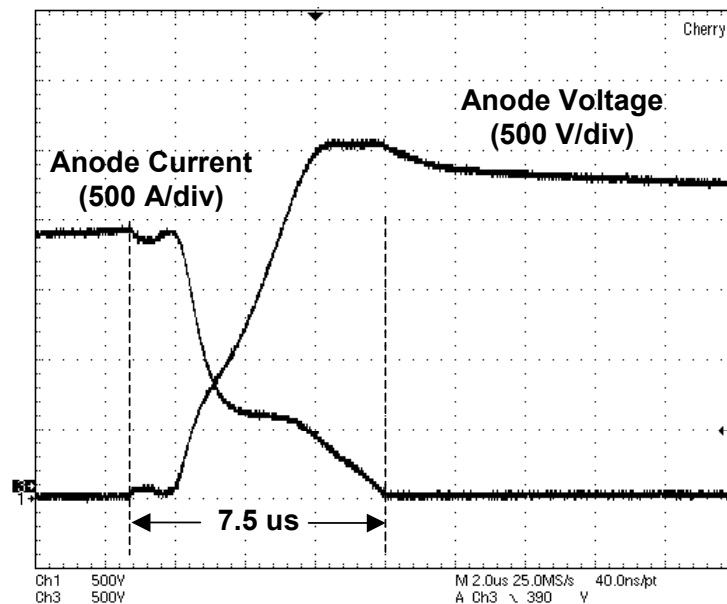


Figure 3-16. The test results of the circuit breaker at a bus voltage of 2.1 kV and anode current of 2 kA.

VIII. Simulation and Experimental Results

A. DC-DC Mode

- **Simulation Results**

To ensure that the components and connections work properly, a half-bridge converter with all necessary snubber components is firstly simulated. Figure 3-17 shows the simulation circuit in which the top and bottom switches alternately conduct the load current. The operating frequency for the top switch is 1 kHz and has a 60% duty cycle. At this stage, the DC bus is 1 kV; therefore, the output voltage is 600 V, and the load current is approximately 150 A. The operating power is thus 90 kW.

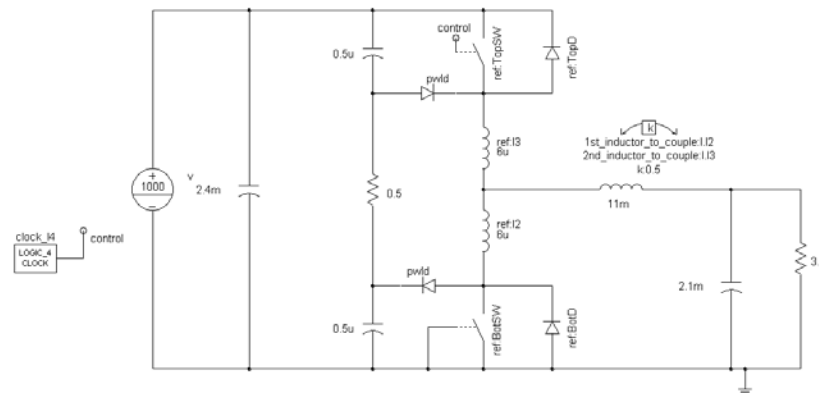
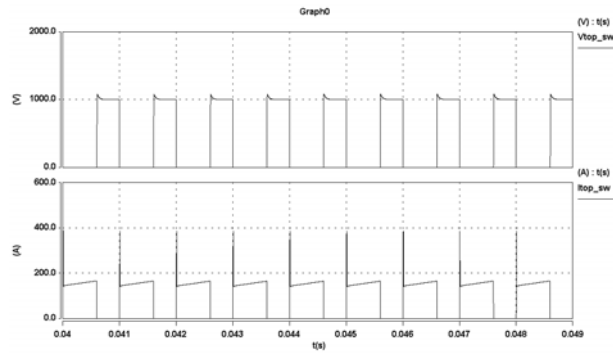
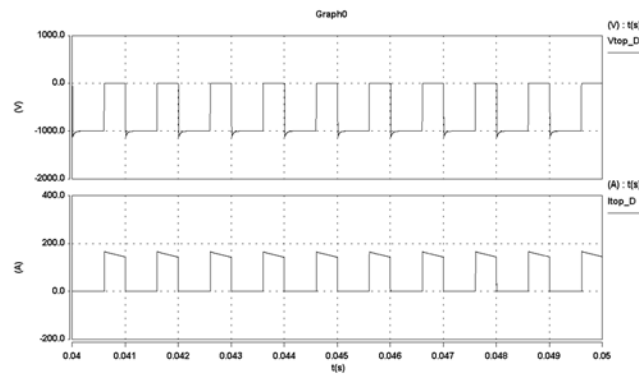


Figure 3-17. The simulation circuit of a half bridge operated as a buck converter.

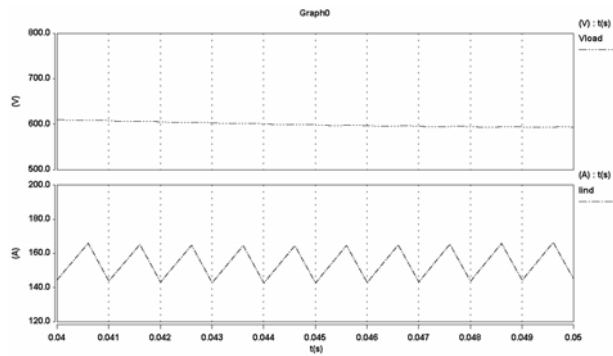
Figure 3-18(a) and (b) show the waveform of the top-switch voltage and current and the bottom-diode voltage and current, respectively. From Figure 3-18(c), the output voltage is 600 V, and the average inductor current is 150 V. In Figure 3-19(a), the dv/dt when the top switch turns off at 150 A is approximately 125 V/ μ s. The di/dt when the top switch turns on at 1 kV, as shown in Figure 3-19(b), is 55 A/ μ s.



(a)

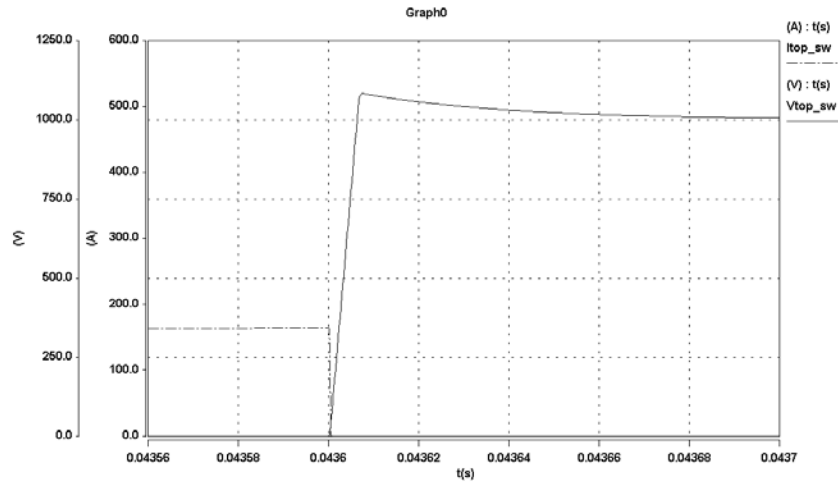


(b)

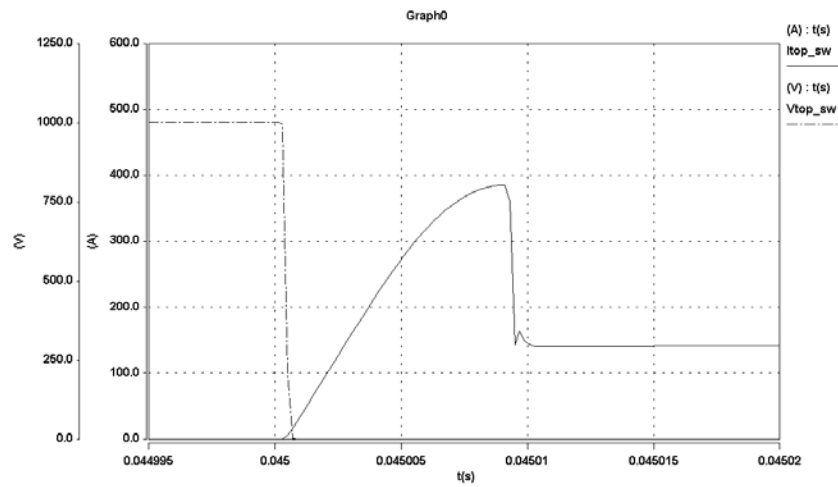


(c)

Figure 3-18. Simulation results for buck mode: (a) the top-switch voltage and current, (b) the bottom-diode voltage and current, and (c) the output voltage and inductor current.



(a)



(b)

Figure 3-19. The top-switch waveforms: (a) at turn-off and (b) at turn-on.

• *Experimental Results*

The circuit shown in Figure 3-17 has been set up. The maximum testing power at this stage is 100 kW, which is the full capability of the DC voltage supply. The switching frequency is 1 kHz with a 60% duty cycle. The DC link is 1 kV, and the resistive load is 3.8 Ω . Figure 3-20 shows the waveform of the top-switch voltage and current and the inductor current. The current and voltage waveforms of the bottom diode are shown in Figure 3-21.

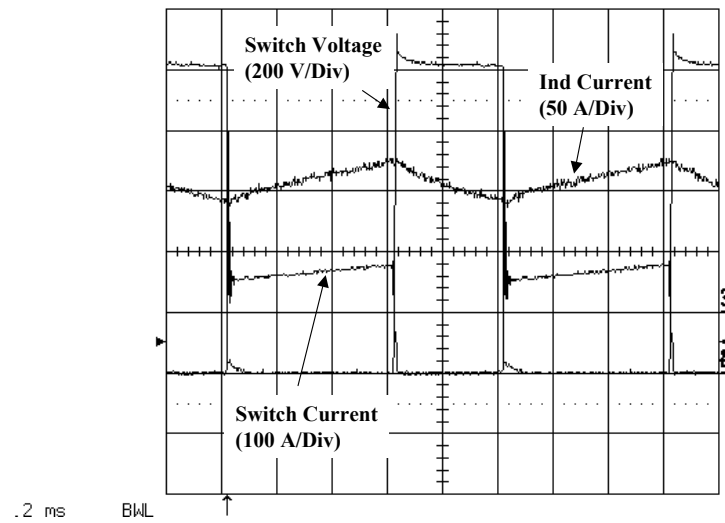


Figure 3-20. The top-switch voltage and current and the inductor current at 1kHz, with a 60% duty cycle.

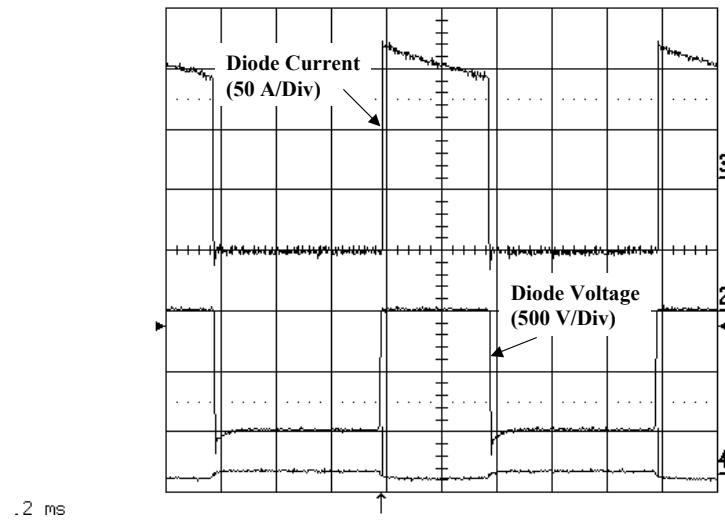
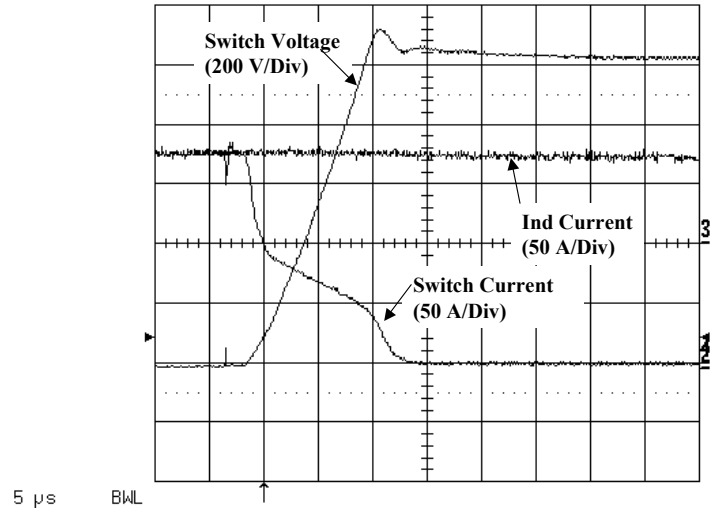
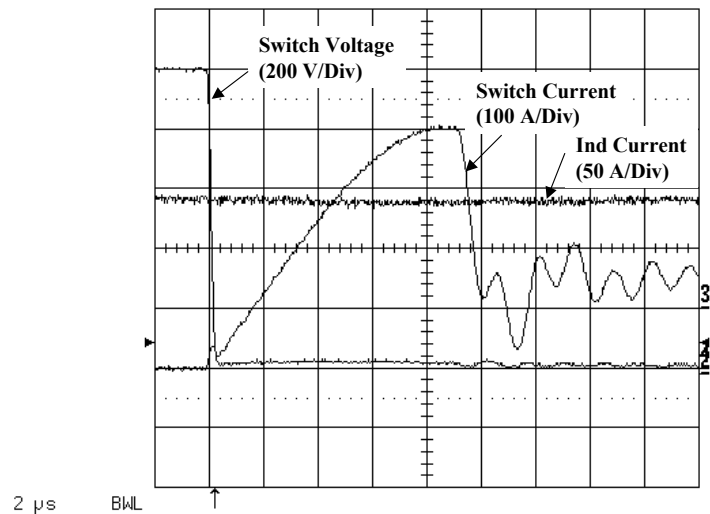


Figure 3-21. The bottom-diode voltage and current at 1kHz, with a 60% duty cycle.



(a)



(b)

Figure 3-22. The top-switch voltage and current during (a) turn-off and (b) turn-on periods.

The waveforms of the top-switch voltage and current during turn-on and turn-off are shown in Figure 3-22(a) and (b), respectively. In Figure 3-22(a), the dv/dt is approximately $100 \text{ V}/\mu\text{s}$, as compared to $125 \text{ V}/\mu\text{s}$ from the simulation results. This difference exists because an ideal switch is used in the simulation; therefore, most of switch current simultaneously goes to the snubber

capacitor. On the other hand, in the real circuit, because of the real switch, part of the switch current goes into the snubber capacitor; thus, a slow dv/dt is obtained.

From Figure 3-22(b), the di/dt is approximately $50 \text{ A}/\mu\text{s}$, which agrees with the simulation results. However, these results differ when the ringing occurs after the switch current decreases to the inductor current level, as shown in Figure 3-23(a), because at t_0 , snubber diode starts to conduct the current, which is mainly the inductor current. Because of the existence of the stray inductances L_{p1} , L_{p2} and L_{p3} , as shown in Figure 3-23(c), there exist two high-frequency current paths, i.e., paths 1 and 2. As shown in Figure 3-23(a), due to the smaller stray inductances, the frequency of the AC current in path 1 is approximately three times higher than that in path 2. This two-frequency ringing thus occurs in the top-switch current during turn-on.

During the test, the temperature of the water-cooling system is set at 10°C . The temperature of the top switch reaches 27°C , and the temperature of the discharge resistor is 36°C . The temperatures of the rest of the components are about the same as that of the setting.

In the proposed HBBB, four $4\text{kA}/4.5\text{kV}$ ETOs are used as the main switches. Diodes 10H4502 from ABB are used for the anti-parallel and snubber diodes. To provide safe levels of dv/dt and di/dt for the ETO, two $0.5\text{mF}/4.5\text{kV}$ snubber film capacitors and two snubber inductor prototypes of 20 mH with a 1kA current rating are selected. The selected discharge resistance is 0.5Ω .

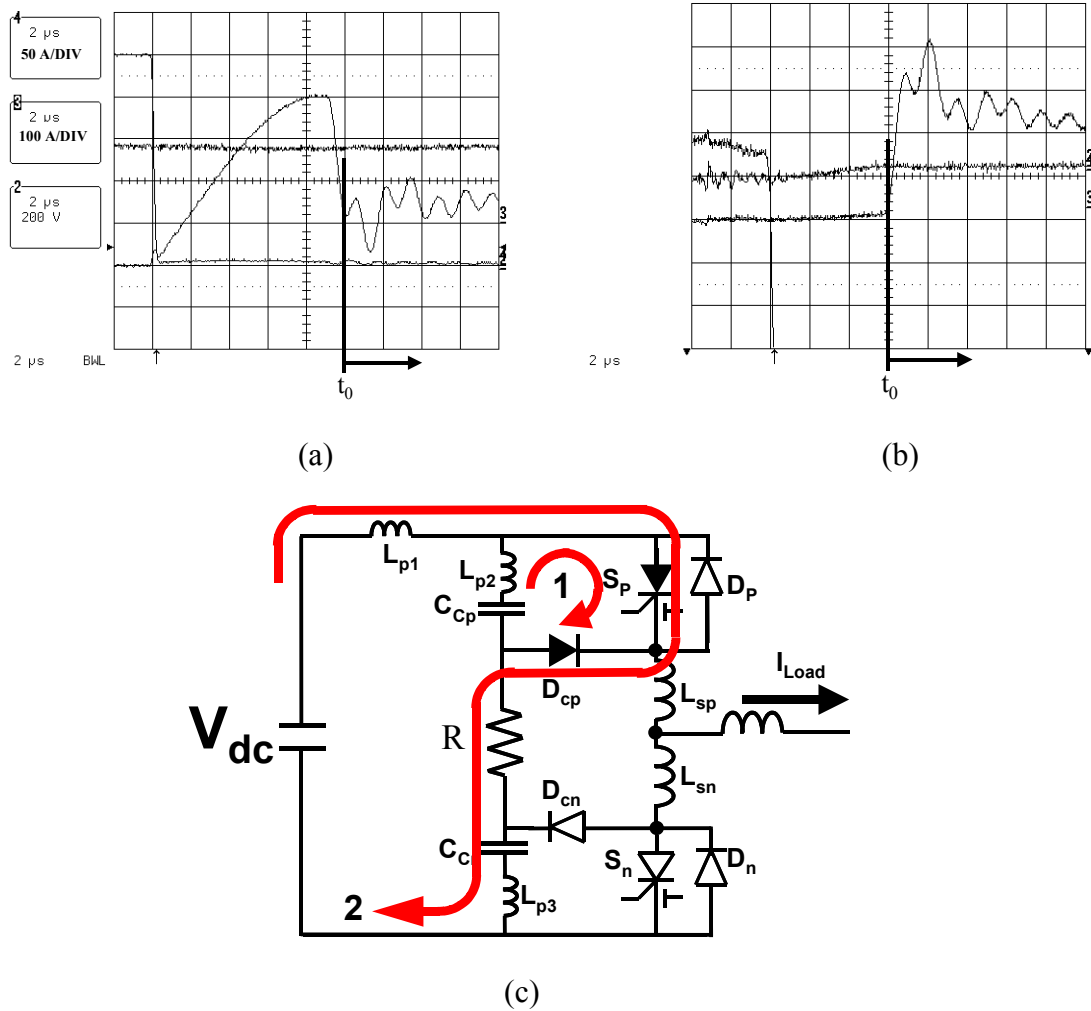


Figure 3-23. The ringing in the top-switch current during turn-on: (a) switch- S_p current, (b) snubber diode D_{cp} current, and (c) AC current paths after t_0 .

B. Inverter Mode

To verify the operation of the selected snubber components, the HBBB prototype has been tested in the inverter mode. The test setup is shown in Figure 3-24. An AMDC300 DSP provides a 1kHz SPWM switching signal to the main switches.

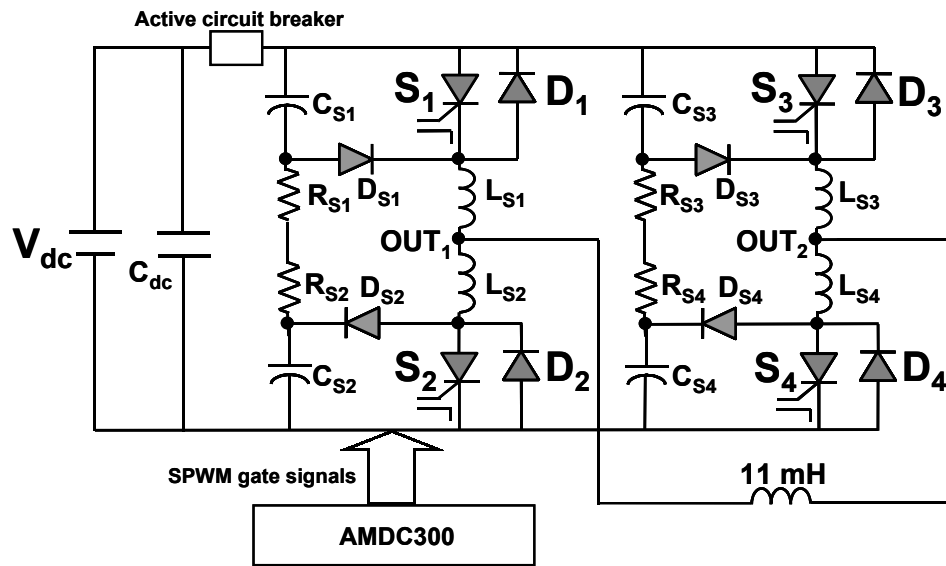
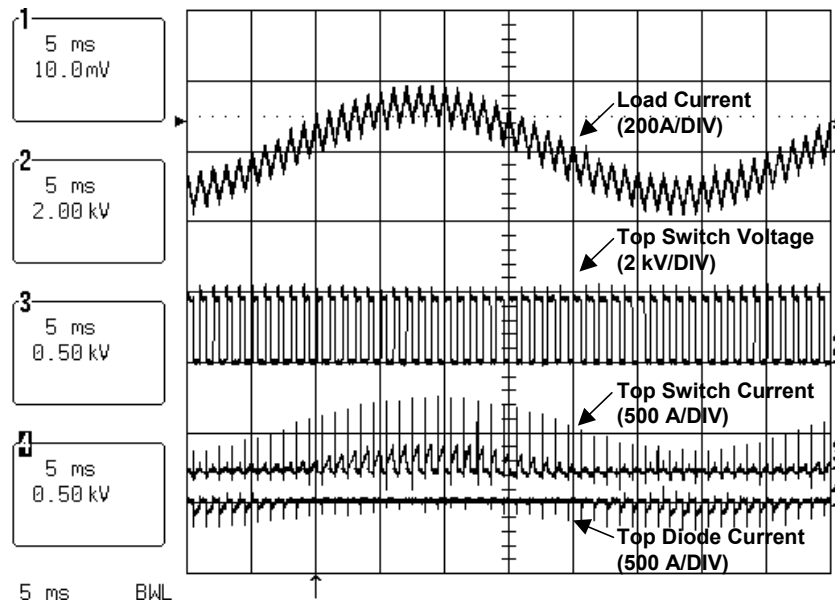
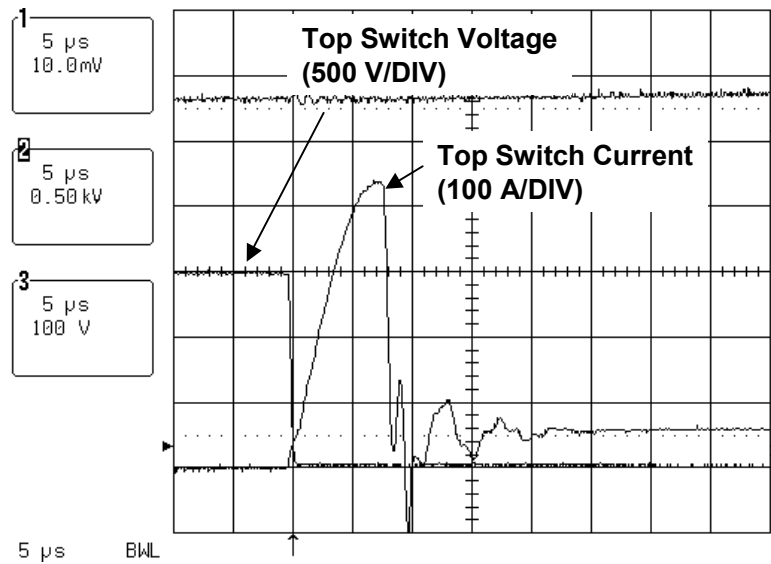


Figure 3-24. The system under test.



(a)



(b)

Figure 3-25. Experimental results: (a) load current, top-switch voltage and current and top-diode current and (b) the di/dt limitation of the top-switch current during the turn-on period at 1.5kV bus voltage.

A 5kV/10A DC power supply is used as the power source. The HBBB is connected to an inductive load of 11 mH. The load bank is the air-core inductor, whose current rating is 500 A_{RMS}. Figure 3-25(a) shows the experimental results of the inductor load current, the top-switch voltage, the top-switch current, and the top-diode current. Due to the limitations of the power supply, the maximum tested DC voltage is about 1.8 kV. The peak load current reaches 200 A. The results demonstrate the high-frequency, high-voltage performance of the ETO. Figure 3-25(b) shows the limitation imposed on the di/dt of the top-switch current by the proposed air-core snubber inductors at 1.5kV bus. Based on the test results, the maximum di/dt limitation at 2kV bus is thus 107 A/μs, which is consistent with the designed value of 100 A/μs.

In conclusion, the proposed HBBB design and the hardware prototype are feasible for use in high-voltage applications. With the relatively high-switching capability of the ETO, the HBBB provides fast dynamic responses and improves the output waveform quality.

3.2 Reactive Component Requirement Criteria for the CMC-Based STATCOM

Besides the high performance of the HBBBs, the passive components used in the STATCOM system also determine the overall system performance and reliability. One of the goals proposed in this dissertation is to determine what criteria play important roles in sizing the reactive components in the CMC-based STATCOM system. In high-voltage applications, a reliable, stable, inexpensive, and high-performance system is mandatory. This study is based on the cascaded-multilevel VSCs. Two major passive components are considered: DC-link capacitors and coupling inductors. Each component is studied based on the different factors in the system, i.e., the DC-link capacitor as a function of

- voltage ripple,
- modulation index,
- switching frequency,
- harmonic distortion in converter output voltages and currents, and
- transient voltage overshoot,

and the coupling inductor as a function of

- converter output current THD,
- range of converter operation, and
- system dynamic response .

I. DC Bus Capacitor Requirement Criteria

The DC capacitor, as shown in Figure 3-26, is an important part of the converter for the reactive power applications, because it is used as a circulating energy buffer. Working together with the solid-stage power converter, the DC capacitor is much smaller in size compared to the AC capacitor bank used to achieve the same Var rating in the conventional SVC.

In an H-bridge converter, the minimum capacitance requirement can be expressed as follows:

$$C_{dc_cascade} = \frac{I_{RMS}}{\sqrt{2} \cdot \pi \cdot f \cdot \%V_r \cdot 10^{-2} \cdot E} \left[1 - \sin(\arccos(\frac{M\pi}{4})) \right],$$

Equation 3-6

where I_{RMS} is the rated load current, $\%V_r$ is the peak-to-peak ripple voltage percentage, E is the nominal DC bus voltage, f is the fundamental frequency, and M is the modulation index.



Figure 3-26. DC capacitor utilized in an H-bridge converter.

A. DC Capacitances vs. Voltage Ripples

In reactive power applications, the output voltage and current of the power converters are approximately 90 degrees out of phase; therefore, real energy is not exchanged in the capacitor. As a result, the size of the capacitor determines the amplitude of the voltage ripple across its DC link, as shown in Figure 3-10.

From Equation 3-6, the voltage-ripple magnitude is obviously indirectly proportional to the DC capacitance. At the same DC voltage, the capacitance decreases as the voltage ripple increases. Figure 3-27 illustrates the voltage ripples across three DC capacitors at the same DC voltage of 2.1 kV and at an output RMS current of 1 kA. The larger the capacitor, the smaller the ripple. The relationship between voltage ripple and capacitance for three different DC-link voltages is presented in Figure 3-28. This graph shows that at the same voltage-ripple percentage, a smaller DC capacitance is needed in the higher DC-link voltage.

Consequently, for the same output current and DC-link voltage, a larger capacitor provides a smaller ripple.

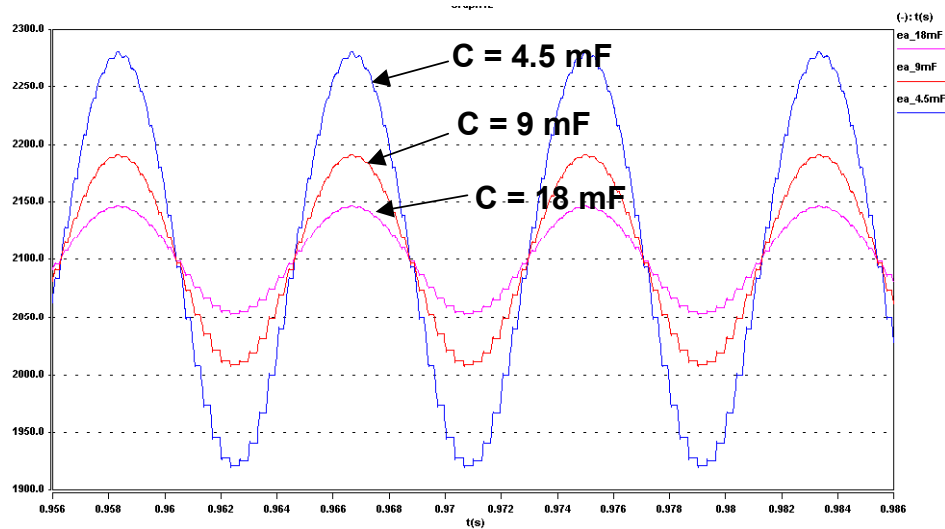


Figure 3-27. Voltage ripples across different capacitances at a DC bus of 2.1 kV.

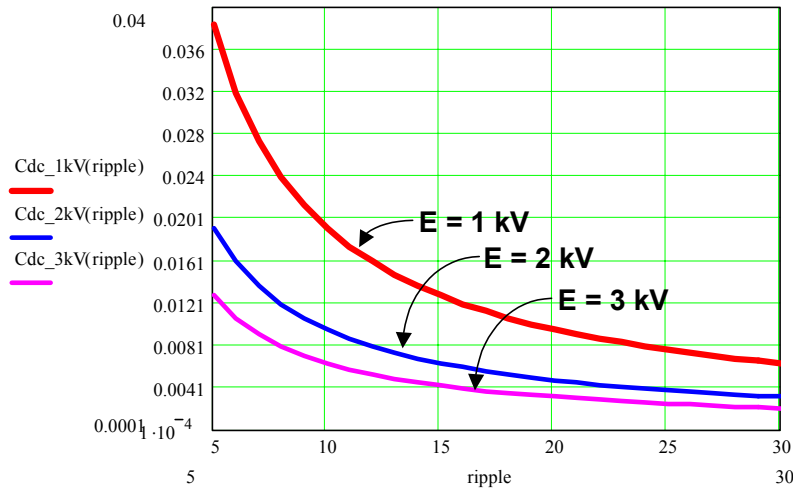


Figure 3-28. Relationship between voltage ripple and capacitance for a switching frequency of 1.5kHz for three different DC-link voltages.

B. DC Capacitances vs. Modulation Indices

Modulation index is one of the factors that dictate the size of the DC capacitor in reactive power compensation. To meet the requirement for the entire operation, the maximum modulation index is used in the capacitance calculation. From Figure 3-29, if the converter operates at the maximum M of 1, the minimum DC capacitance of 8.51 mF is required to suppress the voltage ripple to below 10%. However, if the converter is designed to operate at a lower modulation index (0.9 in this case), the required capacitance becomes 6.53 mF in order to meet the same percentage of voltage ripple. Generally, to maximize the operation range of the STATCOM, the converter is designed to operate at the highest modulation index. In some cases, moreover, it is necessary to go above a modulation index of 1; a larger capacitor may even be needed.

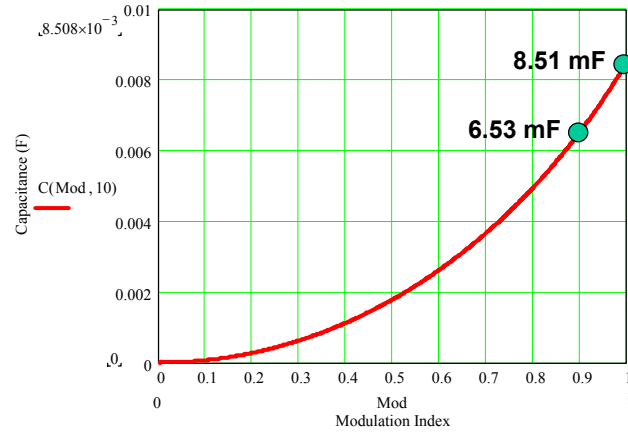


Figure 3-29. The minimum DC capacitance requirement as a function of the modulation index (%Vr = 10, E = 2100 V, I_{RMS} = 1250 A).

C. DC Capacitances vs. Switching Frequencies

According to Equation 3-6, the DC capacitance requirement does not depend on the converter switching frequency. To verify this conclusion, the DC links are simulated with three different switching frequencies, i.e., 1.5 kHz, 3 kHz, and 5 kHz. The DC capacitance, the DC-link voltage, and the output current are kept constant in all three cases. Figure 3-30 demonstrates the simulation results. The simulation results solidly indicate that the peak-to-peak voltage ripples across the DC link are not different for the three different switching frequencies.

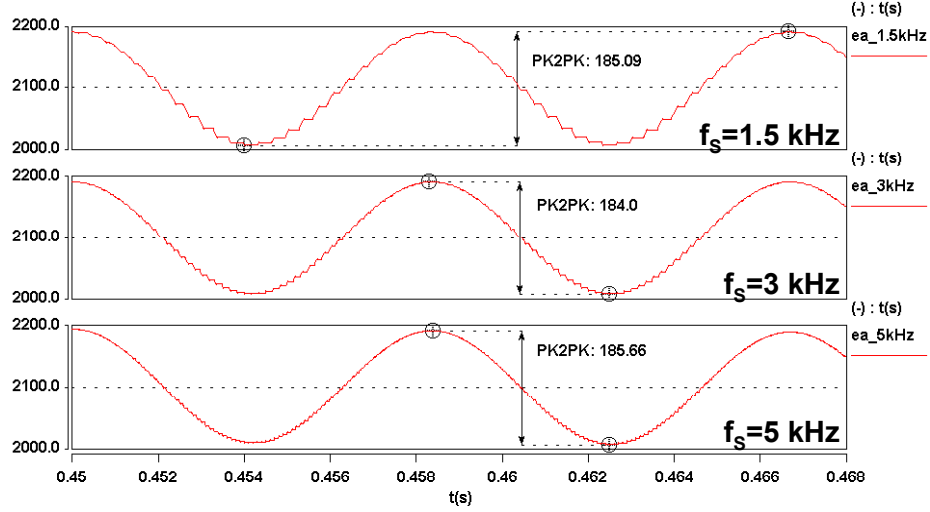


Figure 3-30. DC bus voltage for different switching frequencies
($C = 9 \text{ mF}$, $E = 2.1 \text{ kV}$, $i_{Orms} = 1 \text{ kA}$).

D. DC Capacitances vs. Converter Output Current Harmonic Distortion

It is interesting that the DC capacitor influences the quality of the converter output current. This study, however, shows that it is insignificant. Figure 3-31(a) shows the distortion in the output voltage synthesized by the DC link associated with the ripple. This study focuses on the situation in which the converter operates as a Var generator (in capacitive mode). The surplus voltage caused by the DC-link ripple is defined as V_{ro} . By applying the Fourier series, the spectrum of V_{ro} is determined and is plotted in Figure 3-31(b). The spectrum of V_{ro} indicates a significant amount of third harmonics. Interestingly, it also consists of the fundamental component. This means that the DC voltage can be further utilized. Other voltage harmonic components, however, increase with higher DC voltage ripples, as shown in Figure 3-32(a). The voltage THD is, therefore, increased with a higher DC voltage ripple. Fortunately, in a three-phase, three-wire system, the third harmonic does not exist. The converter output current harmonic is in turn insignificantly affected by the DC voltage ripple, which is verified by simulation results shown in Figure 3-32(b). In other words, converter output-current quality does not depend on the size of the DC capacitor.

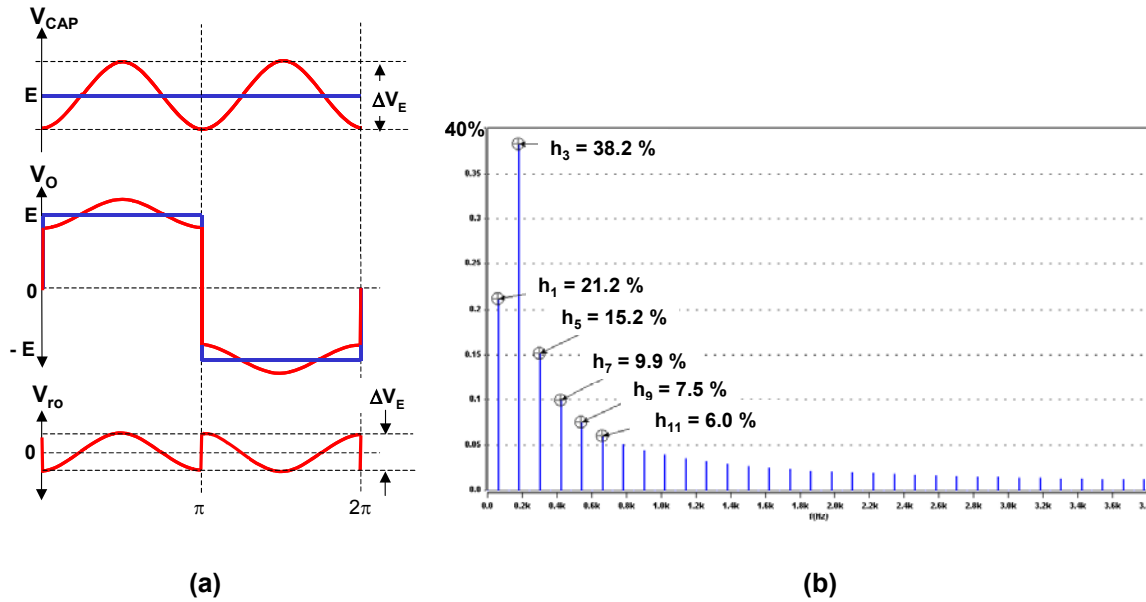


Figure 3-31. (a) Harmonic components in converter output voltage, V_{ro} , introduced by the voltage ripple across the DC capacitor, and (b) the spectrum of V_{ro} .

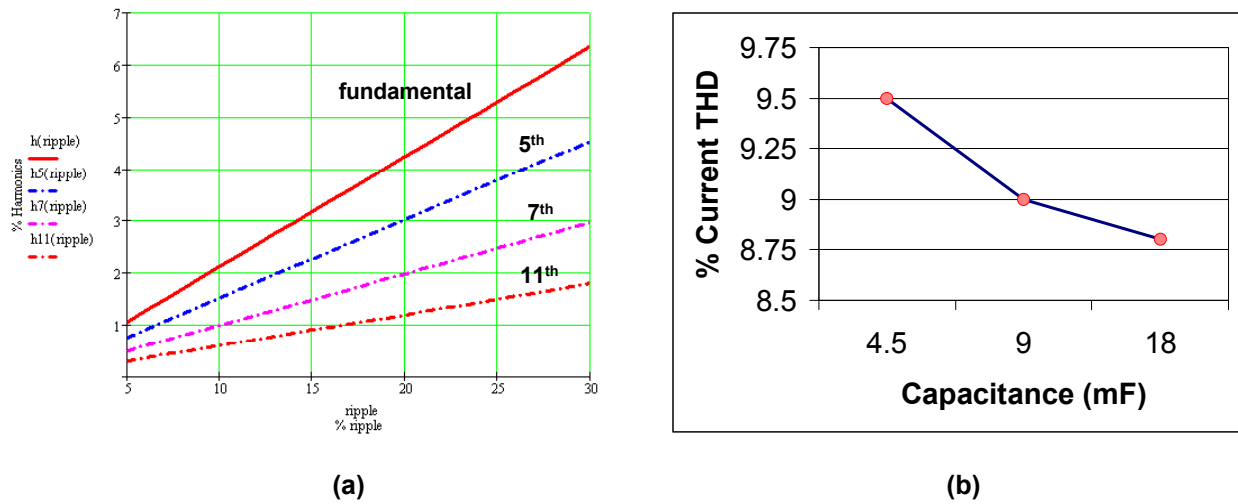
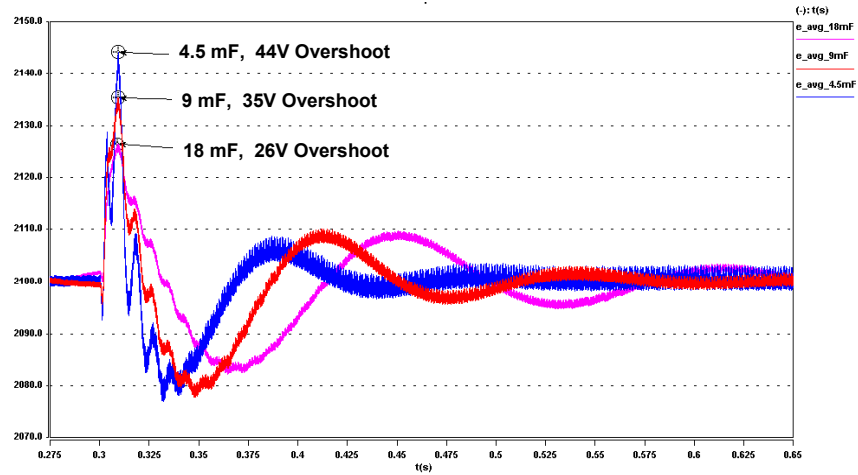


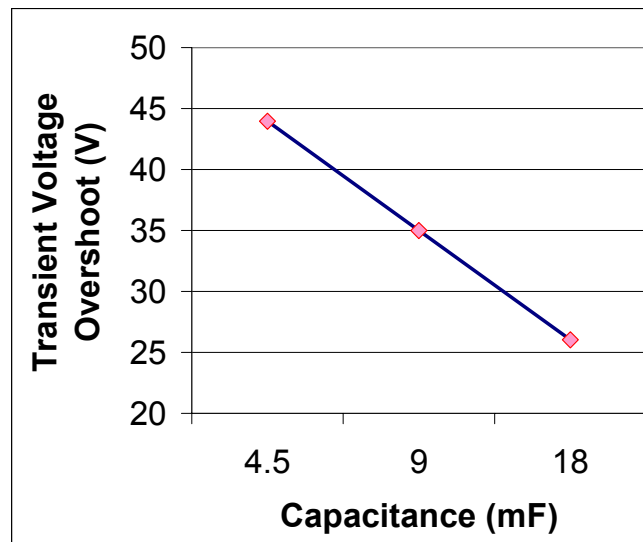
Figure 3-32. (a) Percentage of voltage harmonic components as a function of DC voltage ripples, and (b) percentage of current THD as a function of DC capacitance.

E. DC Capacitances vs. DC-Link Transient Voltage Overshoot

The last parameter of concern in this study is the transient overshoot of the DC-link voltage. A STATCOM system is simulated to demonstrate the effect of DC capacitance on the voltage overshoot. In fact, the time constant of voltage across a DC capacitor is determined by multiplying its capacitance with its equivalent series resistance (ESR). Due to the relatively small ESR in power capacitors, a larger capacitance provides a longer time constant, and consequently allows less overshoot. Figure 3-33 illustrates the overshoot of the regulated DC-link voltage under three different DC capacitances, i.e., 4.5, 9, and 18 mF. To make a fair comparison, the current-feedback parameter is kept unchanged in all three cases. The overshoot is caused by a step command to change the output current of the STATCOM from standby to full capacitive mode. From the simulation results shown in Figure 3-33(a), the voltage overshoot is indirectly proportional to the size of the DC capacitance, as shown in Figure 3-33(b).



(a)



(b)

Figure 3-33. (a) Average-DC-link overshoot waveforms as functions of three different DC capacitances and (b) overshoot of the regulated DC-link voltages as functions of DC capacitances.

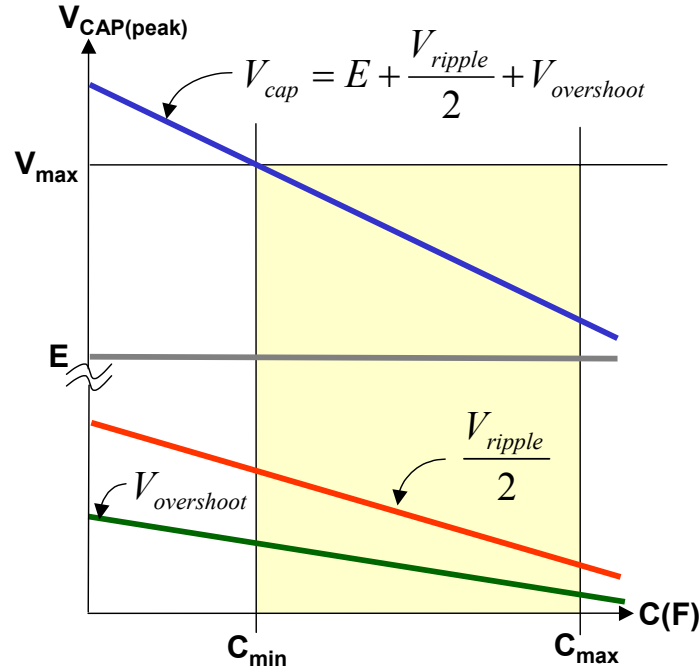


Figure 3-34. DC capacitance criteria.

F. Summary of DC Capacitance Requirement Criteria

For a given output current and operating voltage, the size of the DC capacitor utilized in an H-bridge converter for the CMC used in reactive power compensation should be selected based on the following considerations. One factor limiting the minimum capacitance is over-voltage, which is a function of the voltage ripple and transient voltage overshoot. The voltage ripple is directly proportional to the maximum modulation index of the HBBB. In contrast, the cost is the only factor that limits the maximum size of the capacitor. In addition, the capacitor size does not depend on switching frequency. The output-current THD does not significantly improve with larger DC capacitors. Figure 3-34 shows the boundary of the DC-link requirement.

II. Coupling Inductor Requirement Criteria

The coupling inductor is the second key component in STATCOM applications. At the transmission level, the leakage inductance of the power transformer can serve as the coupling inductor, as long as its size is suitable. A single-line diagram shown in Figure 3-35 illustrates the

connection of the coupling inductor to the PCC. The coupling inductor basically serves as a current low-pass filter for either a power electronic converter or a reactive power coupler. The size of the coupling inductor, however, plays an important role the performance of the STATCOM system.

Based on coupling-inductance variations, the following three key affected parameters are studied: converter output-current harmonics, range of converter operation, and system transient response. The study is based on the CMC-based STATCOM.

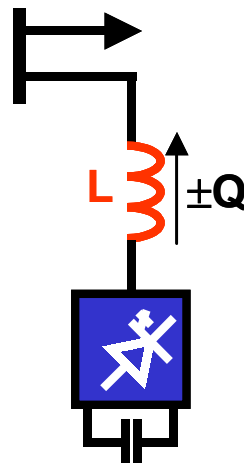


Figure 3-35. Coupling or leakage inductance used in STATCOM applications.

A. Coupling Inductance vs. Converter Output Current Harmonics

As one of its two main functions, the coupling inductor in STATCOM applications is used to filter out the harmonic components that are primarily caused by the low-switching-frequency pulsating voltage that is synthesized by the high-power converter. Obviously, a larger inductor can attenuate more harmonic components. Simulation results shown in Figure 3-36 indicate that for 15kHz SPWM, current harmonic THDs are 5.8% and 11.1% with coupling inductances of 0.35 mH and 0.7 mH, respectively. Thus, a larger coupling inductance improves the quality of the output currents of the converter.

B. Coupling Inductance vs. Converter Operation Range

To be able to operate the power converter in reactive power compensation applications, the coupling inductor must also act as a reactive power interface or coupler. As explained in Chapter 2, the amount of reactive current exchanged between the PCC and the STATCOM is controlled by the voltage drop across the coupling inductor. In other words, the output voltage of the converter is controlled to provide a suitable voltage drop across the coupling inductor. According to modulation techniques, the duty cycle determines the operating window range for its converter. In general, the duty cycle is limited to 1 by the switching behavior of power converters. The operating range of the converter, therefore, limits the size of the coupling inductor. Figure 3-37 demonstrates how the coupling inductor affects the operating window of the converter. The same converter with the same control parameters is operated with two different coupling inductors, i.e., one at 0.35 mH and one at 0.7 mH. The results show the transition of the modulation-index responses to the command from standby to full capacitive mode. In DQ control, the duty cycle is limited at 1.225. With an inductance of 0.7 mH, the duty cycle is always saturated in capacitive mode, whereas the converter with an inductance of 0.35 mH can operate within the entire range.

In conclusion, a higher inductance introduces a higher reactive power loss; therefore, a wider operation window is needed for the converter.

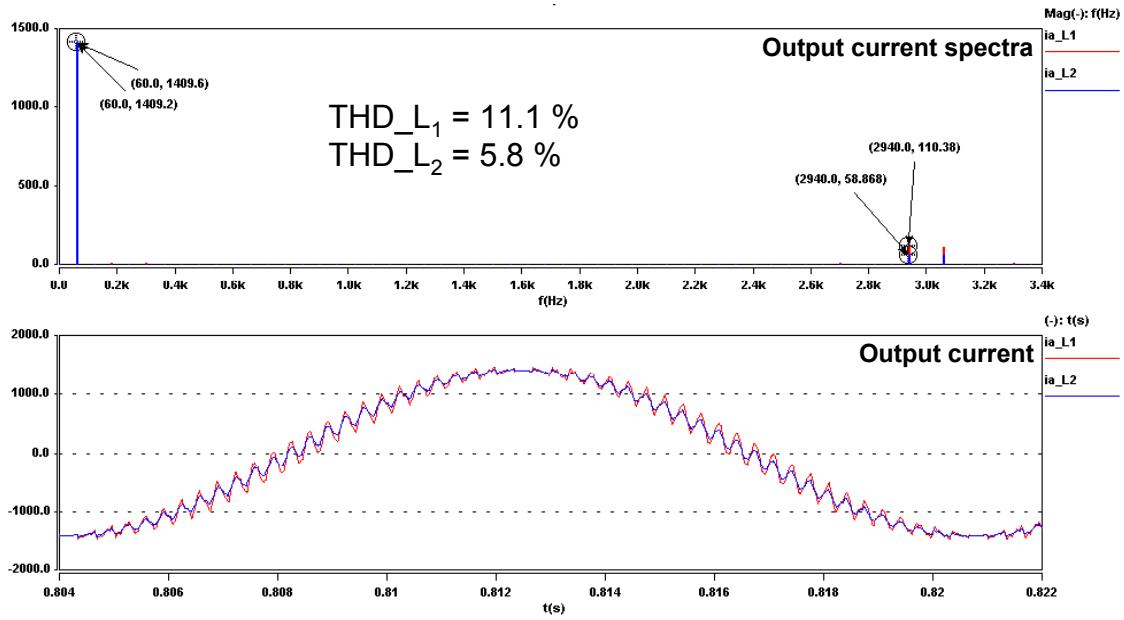


Figure 3-36. Output current THD of the converter as a function of coupling inductances ($L_1 = 0.35$ mH, $L_2 = 0.7$ mH, switching frequency = 1.5 kHz).

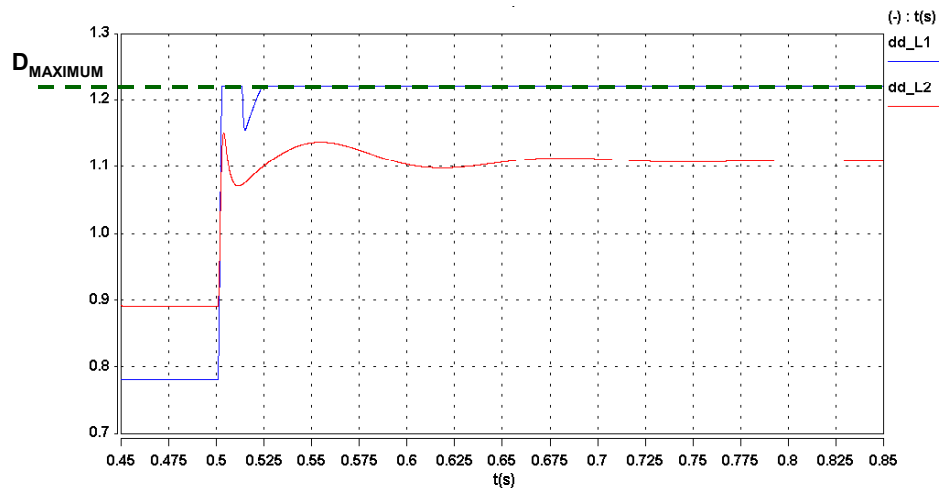


Figure 3-37. Operating window of the converter as a function of coupling inductances ($L_1 = 0.7$ mH, $L_2 = 0.35$ mH, switching frequency = 1.5 kHz).

C. Coupling Inductance vs. System Dynamic Response

In a STATCOM, the size of the coupling inductor determines the system dynamic response. The larger the coupling inductance, the slower the system response. Figure 3-38 illustrates Bode plots of two different open-loop control-to-output current transfer functions, i.e., G_{idd_L1} and G_{idd_L2} . In this study, L_2 is twice as large as L_1 . Obviously, the L_2 case yields a slower transfer function. This physically means that the L_2 system responds to the disturbances more slowly than the L_1 system does. However, applied proportional-integrated compensators can identically compensate the closed-loop gains of these two different open-loop gains, as shown in Figure 3-39. Figure 3-40 shows the step-command dynamic responses of the compensated reactive currents. The simulation results show similar responses for the L_1 and L_2 cases.

Consequently, system response is not dictated by a variation in the coupling inductances.

Figure 3-38. Comparison of the inductance effect on the control-to-output-current transfer function ($L_1 = 0.35$ mH, $L_2 = 0.7$ mH).

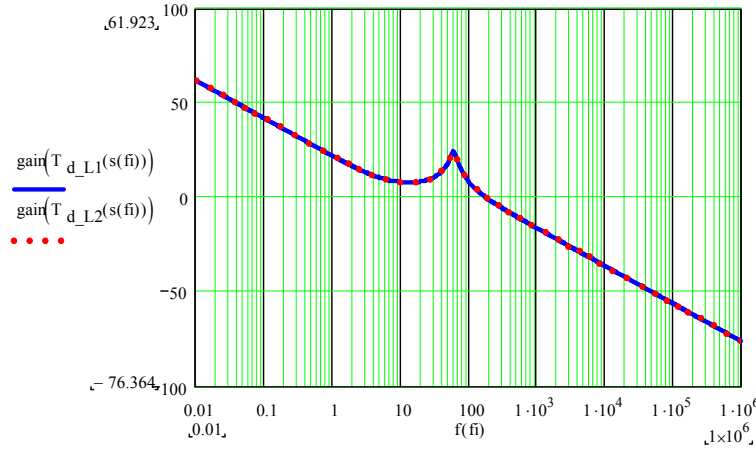


Figure 3-39. Current loop gains can be compensated to achieve the same dynamic response.

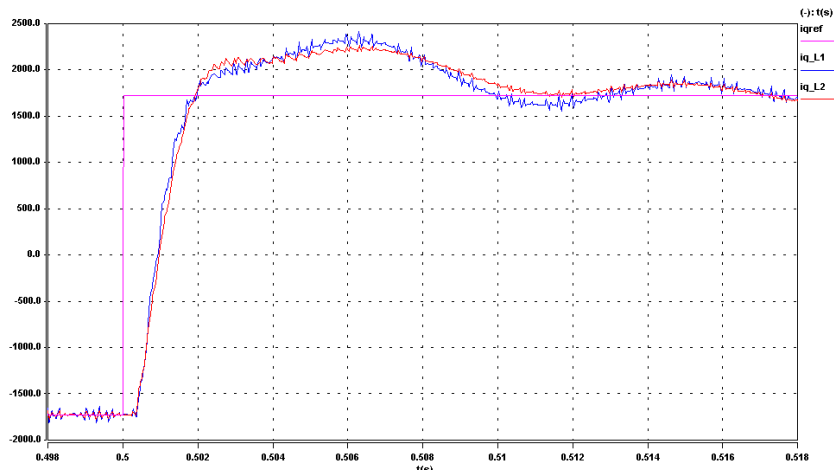


Figure 3-40. Transient responses of output currents as functions of coupling inductances.

D. Summary of Coupling Inductor Requirement Criteria

In conclusion, for a given output current and operating voltage, the size of the coupling inductor is minimally limited by output-current harmonic distortions. The maximum inductance is limited by the operation range of the converter (reactive power loss) and, of course, by the cost. However, the coupling inductance does not influence the system dynamic response. Figure 3-41 illustrates the coupling inductance requirement criteria.

3.3 Conclusion

The configuration and structure of the high-voltage ETO-based HBBB have been presented. Because of their identical layout, the HBBBs are simple to manufacture. Their modularity makes the entire system flexible in terms of power capability. By connecting these modules in series, the CMC topology that is suitable for reactive power compensations can be readily implemented. The McMurray snubber applied in the HBBB showed excellent operation. The snubber component selection and implementation have been discussed. The experimental results of the HBBB operating in inverter mode have been obtained, and the key results have been presented. The high-frequency, high-power operation of the HBBB is clearly demonstrated.

Besides the key components, such as the HBBBs, the passive components used in the CMC-based STATCOM also dictate the performance of the entire system. The reactive component requirement criteria for reactive power compensations have been investigated. Two key passive components that are included in this study are the coupling inductors and the DC capacitors.

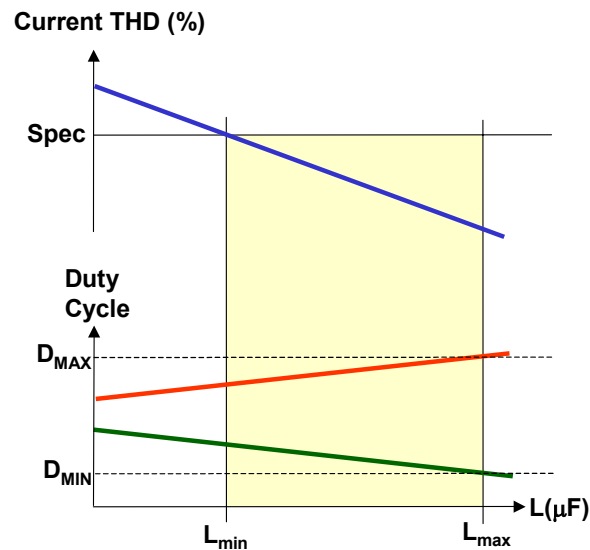


Figure 3-41. Coupling inductance requirement criteria.

Chapter 4 MODELING OF CASCADED-MULTILEVEL CONVERTER-BASED STATCOM

An accurate and well-defined model plays the most important role in designing a system with superior feedback control. However, as discussed in Chapter 1, no previous work has yet shown a good model for the cascaded-multilevel VSC. The major controlled parameters in those previous works have been determined by either trial and error or by random tuning.

The proposed model, which can be utilized in all applications, is generally suitable for cascaded converters with any number of levels. This chapter proposes an accurate and simple modeling technique for the CMC-based STATCOM in both stationary (ABC coordinates) and synchronous (DQ0 coordinates) frames. Due to the excessive number of controlled variables in the cascaded-multilevel VSCs, an effective simplification, based on practical assumptions and proposed variable definitions, is proposed. Combining the proposed DC-link-balancing technique presented in Chapter 5 with the proposed modeling technique, cascaded-multilevel VSCs with any number of voltage levels can be modeled as three-level cascaded VSCs. This technique is one of the major contributions in this dissertation.

The methodology of the model development for the CMCs is presented in this chapter. The proposed model is then utilized in STATCOM applications. Finally, all necessary transfer functions are determined and used in the feedback-control design process. A simplified model for the three-phase system in DQ0 will be used in the feedback-control design proposed in Chapter 5.

4.1 Operating Principle of the Cascaded-Multilevel Converter-Based STATCOM

A schematic of a CMC-based STATCOM is shown in Figure 4-1. Basically, the STATCOM system is composed of three main parts: a multilevel-cascaded VSC with separated DC capacitors, the coupling inductors, and a controller. A coupling inductor in each phase serves as both a converter output-current filter and a reactive power coupler. The main purpose of the

coupling inductors is to filter out current harmonic components that are mainly caused by the modulation techniques used in the converters. In a very-high-voltage system, above 13.8 kV, the leakage inductances of coupling step-up power transformers can function as coupling reactors.

A multilevel-cascaded converter consists of a number of identical H-bridge converters, whose output terminals are connected in series. The output voltage is thus the summation of those H-bridge converters, i.e.,

$$V_{kn} = V_{k1} + V_{k2} + \dots + V_{kN},$$

Equation 4-1

where k is the phase notation, i.e., a, b or c, and
 N is the number of H-bridge converters per phase.

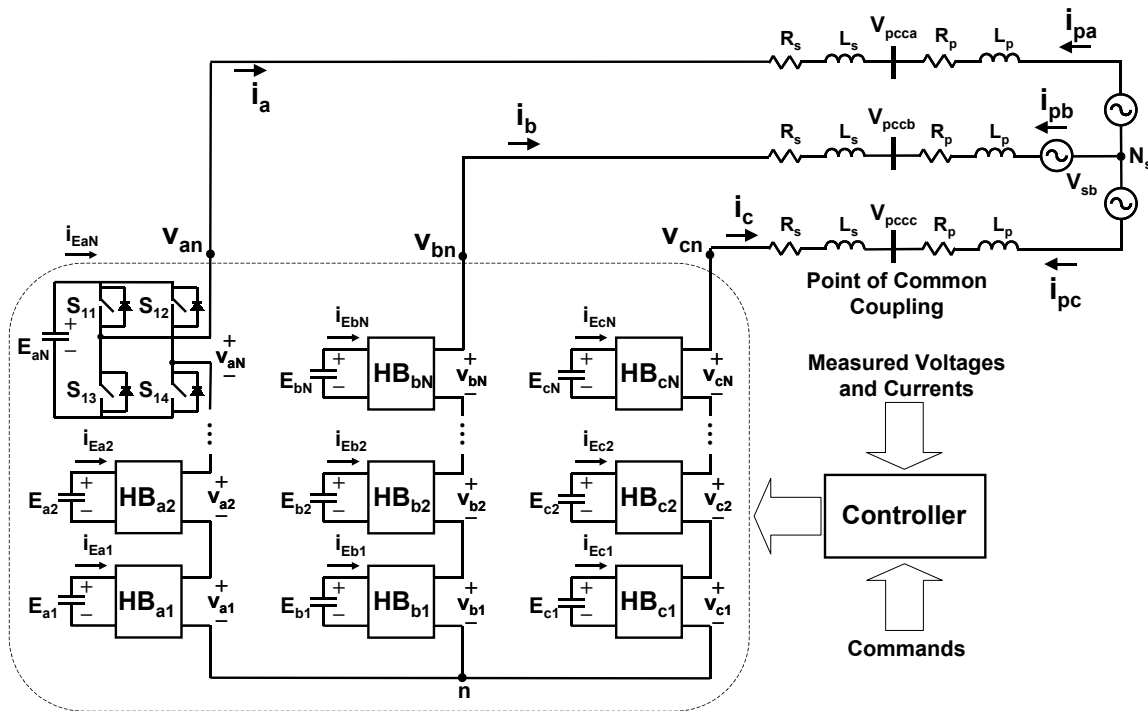


Figure 4-1. Schematic of a cascaded-multilevel converter-based STATCOM system.

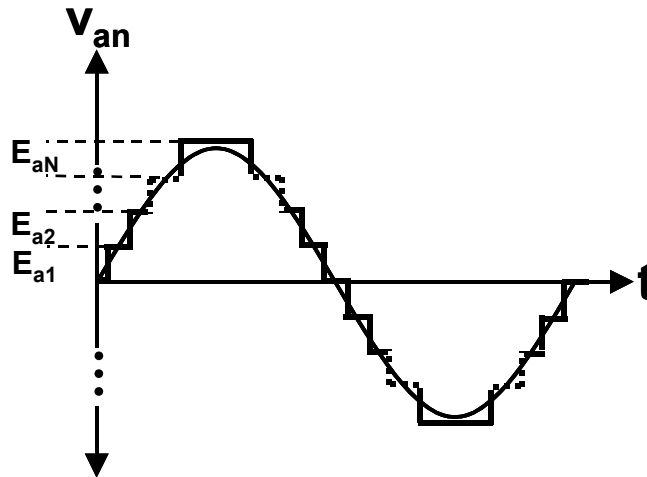


Figure 4-2. Phase-voltage waveform of the cascaded-multilevel converter.

Since three output voltage levels can be synthesized by an H-bridge converter, the total number of output-phase voltage levels, as shown in Figure 4-2, equals $2N+1$. The maximum number of line-to-line voltage levels is $4N+1$. By increasing the number of H-bridge converters, the output-voltage THD is significantly improved. The output-voltage waveform approaches sinusoidal when the number of H-bridge converters reaches infinity. Moreover, the power capacity of the system is increased, and the dynamic response is improved. The number of H-bridge converters is, however, limited by numerous practical concerns. The most important one is the complexity of the control system. A greater number of voltage levels introduces the DC-link-imbalance problems, and of course increases the system cost.

The STATCOM is connected to the problematic bus of a power network at a PCC. To make the entire system work effectively and properly, the controller needs to be robust. All necessary voltages and currents are measured and then fed into the controller to be compared with the commands. The controller then performs feedback control, and outputs a set of switching signals to drive the main valves of the power converter accordingly. The feedback controller regulates the output currents and DC-link voltages. The single-line diagram of the STATCOM system is illustrated in Figure 4-3. In general, the CMC is represented by an ideal VSC, which is associated with internal loss, that is connected to the AC power via coupling impedances.

Generally, the internal losses are accumulated from semiconductor switching and conduction losses, stray resistance losses in interconnects and passive components, snubber circuit losses, etc.

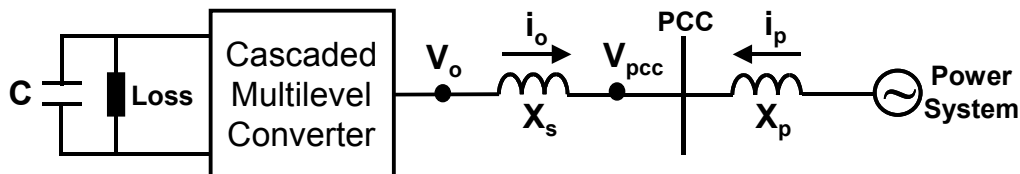


Figure 4-3. Single-line diagram of the cascaded-multilevel converter-based STATCOM.

The exchange of real power and reactive power between the cascaded converter and the power system can be controlled by adjusting the amplitude and displacement angle of the converter output voltages with respect to the voltage at the PCC. In the case of a lossless converter, the output voltage of the converter is controlled to be in phase with that of the power system. In the capacitive mode, the STATCOM generates a given amount of reactive power to the connected network, while, in the inductive mode, the STATCOM absorbs a given amount of reactive power from the connected network. To operate the STATCOM in capacitive mode, $+Q$, the magnitude of the converter output voltage is controlled to be greater than that of the power system. On the other hand, the output-voltage magnitude of the converter is controlled to be less than that of the power system in order to operate the STATCOM in inductive mode, $-Q$. However, in practice, a converter is associated with internal losses. As a result, without any control, the capacitor voltage will decrease and will eventually collapse. To regulate the capacitor voltage, a small phase shift δ is introduced between the converter voltage and the power system voltage. Figure 4-4 illustrates phasor diagrams of the voltage at the PCC, the converter output current, and the voltage in all four quadrants of the PQ plane. This PQ plane reveals two important control laws of the cascaded-multilevel VSC for STATCOM applications:

1. The amount of transferred reactive power (Var, Q) can be controlled by adjusting the magnitude of the converter output voltage; and
2. The amount of transferred real power (Watt, P) can be controlled by adjusting the phase displacement of the converter output voltage with respect to the voltage at the PCC.

To further explain the operation of the STATCOM, the power exchange of the STATCOM in the PQ plane can be mapped into the direct-quadrature (DQ) plane, as shown in Figure 4-5. The phasor of the STATCOM output current, I_O , and the phasor of the voltage at the PCC, V_{PCC} , is presented in the DQ plane. For reactive power compensation, I_O is normally located inside the white slices of the circle whose radius is the rated current of the STATCOM. The top white slice represents the STATCOM operating in capacitive mode or $+Q$, while the bottom slice is where the STATCOM operates in inductive mode or $-Q$. The light-gray area on the left-hand side of the Q-axis represents the STATCOM startups. In this operation area, the STATCOM operates in boost rectifier mode.

In the case of a STATCOM with an energy-storage system, the gray slice is an additional operating area, where the STATCOM can inject the amount of real current into the power grid.

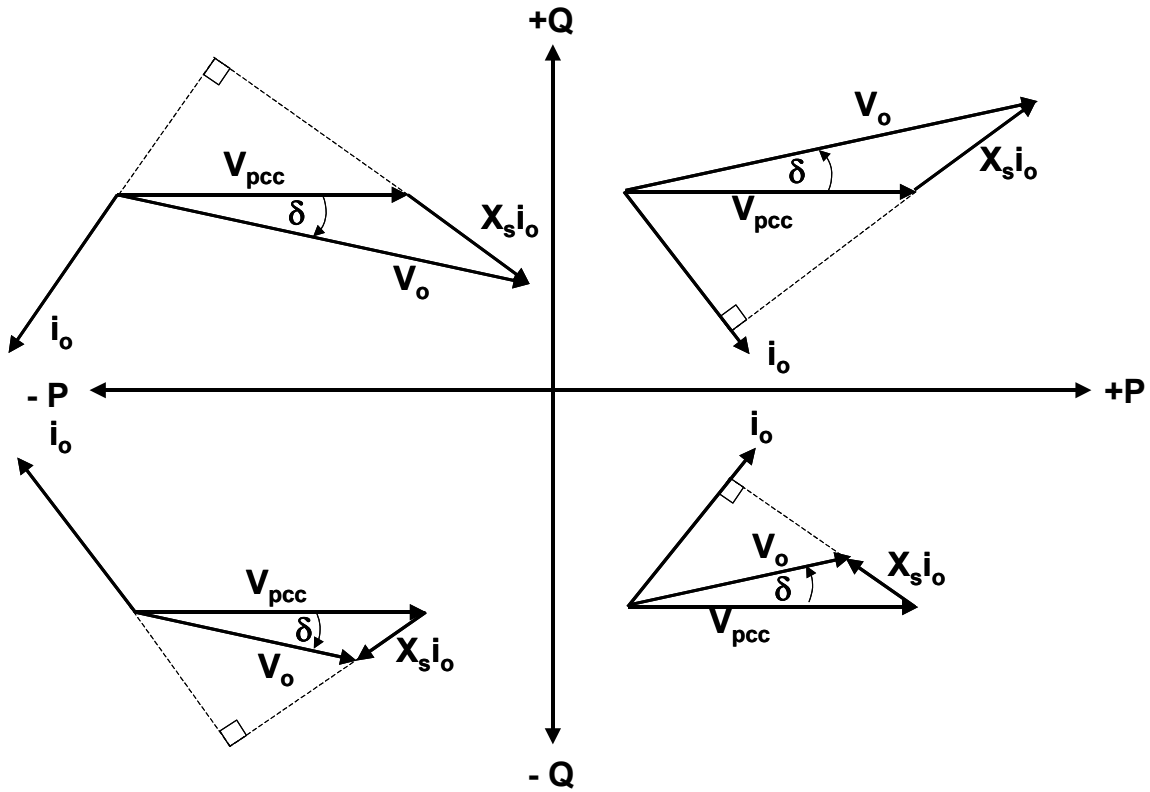


Figure 4-4. Phasor diagram for power exchanges in STATCOM applications.

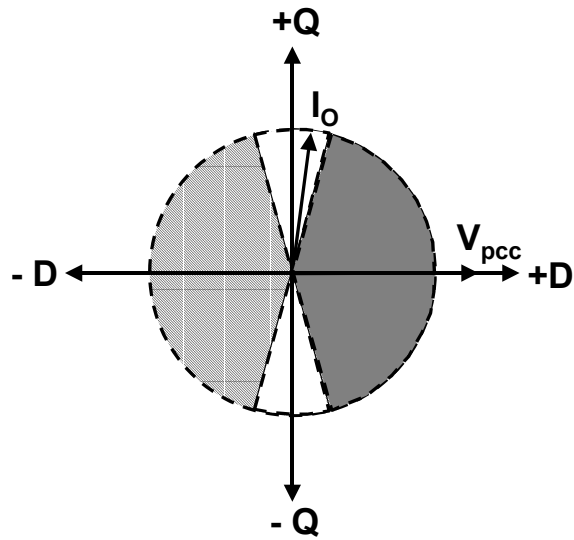


Figure 4-5. Phasor diagram of the STATCOM output current and its voltage at the PCC.

4.2 Model and Feedback-Control Development

This section proposes a development procedure for the model and feedback control of a CMC-based STATCOM. Figure 4-6 illustrates the block diagram, showing the relationship between the modeling and feedback-control design. Although this methodology focuses on STATCOM applications, it can be employed elsewhere. The process begins with model development. The results of this step are key transfer functions of the control parameters to state variables such as STATCOM currents and DC capacitor voltages. As will be proposed in Chapter 5, the feedback control is designed and evaluated based on the derived transfer functions. Because of the proposed modeling method, the stability of the feedback loops can be systematically evaluated. The loop gains are then modified to achieve as much stability as possible, while the dynamic response is not sacrificed. The proposed control technique is validated by both computer simulation and experiments.

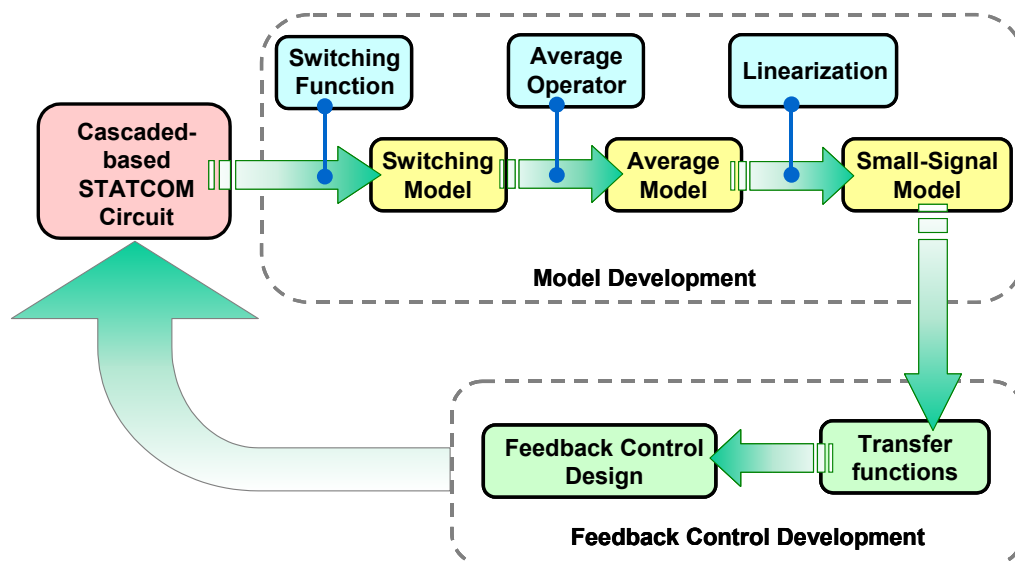


Figure 4-6. Control development for the cascaded-multilevel converter-based STATCOM.

4.3 Model Development

Figure 4-7 shows the model development flowchart. The process is begun by defining the switching functions of the converter power stage. By applying the defined switching functions, the CMC can be represented by a switching model. The next step is to average the switching model. In this step, all switching behaviors are neglected; only fundamental components are considered. An important parameter that emerges from the average model is the duty cycles, which are the main controlled parameters of the power stage. A generalized average model is derived in ABC coordinates; this model can be used for any kind of power-conversion systems. To derive an average model for the CMC-based STATCOM, the derived average model is integrated with a linear model of three-phase AC sources and coupling reactors.

Due to the proposed decoupling power-control technique, variables in the ABC coordinates must be transferred into DQ0 coordinates. The last step is linearization, by which the small-signal model is derived. Transfer functions of the system are then realized from the derived small-signal model. In the synchronous frame, all AC parameters become DC parameters. In other words, both the inverter and rectifier modes of a converter behave the same as the DC-to-DC converter mode. Classical linear control can therefore be applied. As a result, the stability of the feedback loop can be simply evaluated, and the control parameters can be optimized to achieve the best performance. In addition, reactive and real power components can be controlled independently.

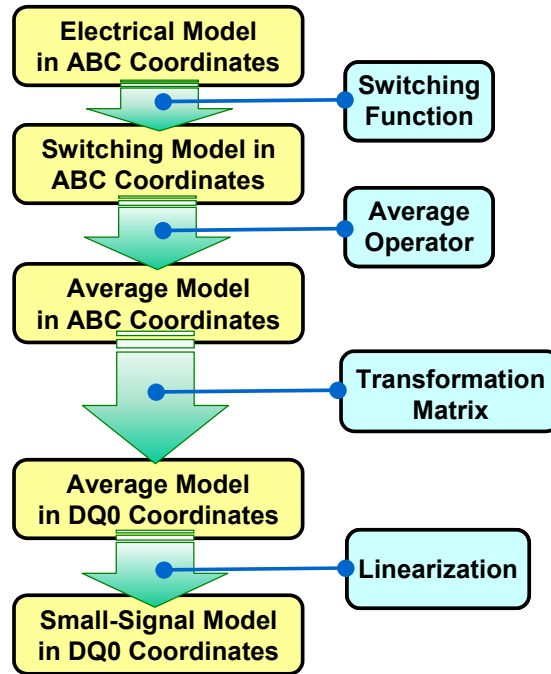


Figure 4-7. Model development.

I. Switching Model

The CMC basically consists of many identical H-bridge converters connected in series. The basic structure of an H-bridge converter is shown in Figure 4-8(a). Three possible synthesized output-voltage levels of the H-bridge converter and their corresponding switch combinations are illustrated in Figure 4-8(b). With the voltage constraint of the circuit, the top and bottom switches in the same phase leg must not be turned on simultaneously, or a short circuit will be introduced across the DC link. In other words, the top and bottom switches are switched complementarily. The top switch can therefore be used to represent the switching status of its phase leg. As a result, the output state of the phase leg is determined solely by the status of its top switch. The equivalent circuit of the H-bridge converter can thus be depicted as shown in Figure 4-8(c). To show the relationship between the output current and voltage on the DC side and those on the AC side, four possible combinations of both top switches are given in Table

4-1. The 0 represents that the switch is connected to a negative polarity of the DC voltage source, and the 1 represents that the switch is connected to a positive polarity.

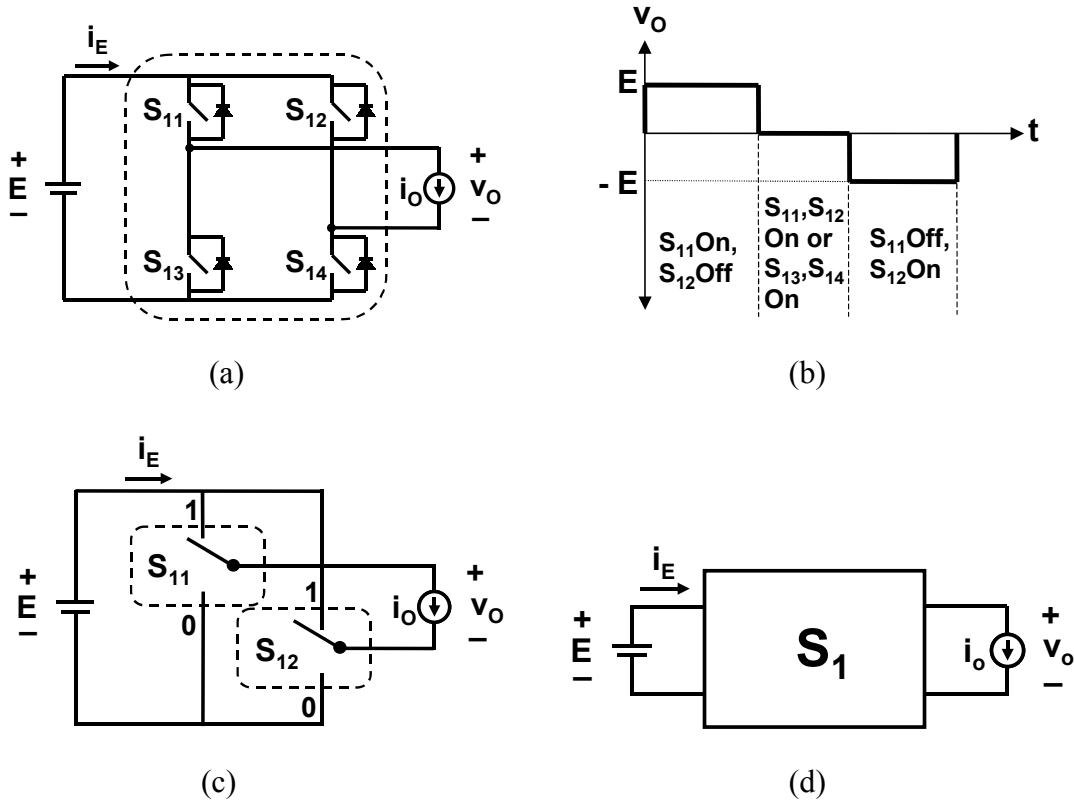


Figure 4-8. Development of the switching model of an H-bridge converter: (a) basic structure of an H-bridge converter, (b) output voltage of the H-bridge converter, (c) equivalent circuit of the H-bridge converter, and (d) the switching model of the H-bridge converter.

TABLE 4-1. INTEGRATED SWITCH COMBINATIONS.

S_{11}	S_{12}	v_o	i_E
0	0	0	0
1	0	E	i_o
0	1	-E	$-i_o$
1	1	0	0

From Table 4-1, the relationship between the DC voltage and the output voltage, as well as the relationship between the capacitor current and the output current, can be expressed as:

$$v_o = (S_{11} - S_{12})E, \text{ and}$$

Equation 4-2

$$i_E = (S_{11} - S_{12})i_o.$$

Equation 4-3

S_I is defined as a difference of two top-switch statuses, i.e.,

$$S_I = S_{11} - S_{12}.$$

Equation 4-4

By substituting S_I , Equation 4-2 and Equation 4-3 become

$$v_o = S_I \cdot E, \text{ and}$$

Equation 4-5

$$i_E = S_I \cdot i_o.$$

Equation 4-6

Finally, the switching model of the H-bridge converter can be represented as shown in Figure 4-8(d). Each H-bridge converter in the cascaded-multilevel VSC, as shown in Figure 4-1, can then be replaced with its switching model, as shown in Figure 4-9.

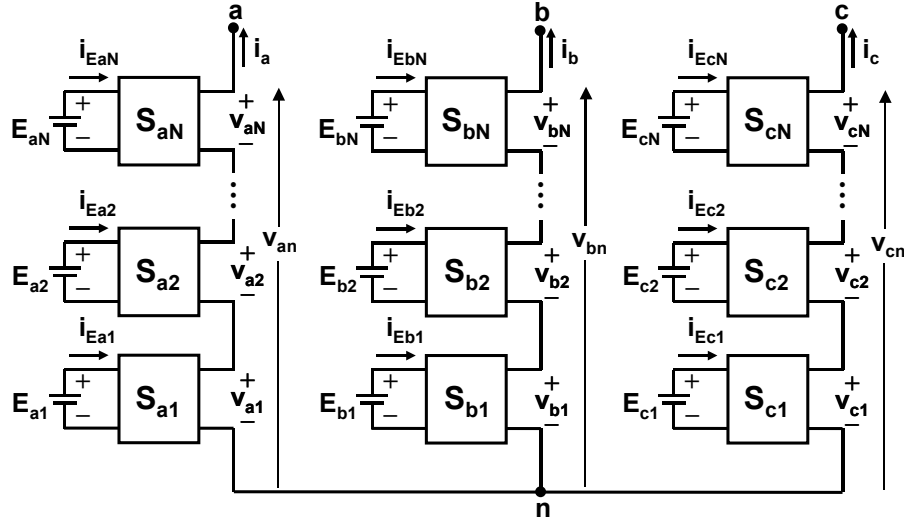


Figure 4-9. Switching model of the cascaded-multilevel converter.

II. Average Model in Stationary Frame (ABC Coordinates)

To develop an average model of the H-bridge converter, the switching function is averaged over one switching cycle. Thus, the switching behavior and harmonic components of all parameters are not taken into account.

Basically, the average operator can be expressed as

$$d = \bar{S}(t) = \frac{1}{T} \int_{t-T}^t S(\tau) d\tau,$$

Equation 4-7

where $S(\tau)$ is switching function, and

d and $\bar{S}(t)$ are average value of the switching function, which is defined as the duty cycle.

Figure 4-10 demonstrates this definition of a duty cycle. The switching function between time 0 and T is used as an example, and is expressed in Equation 4-8. The switching function

equals 1 for the d_1T second, and 0 for the $(1-d_1)T$ second, where T is a switching period. After applying the average operator in Equation 4-7 to Equation 4-8, the duty cycle for switching function $S(t)$ is d_1 . Likewise, average switching function $S(t)$ from time T to $2T$ is $-d_2$.

With the presented switching model development, the duty cycle of an H-bridge converter can possibly be varied from -1 to 1 , as shown in the following:

$$\bar{S}(t) = \begin{cases} 1, & 0 < t < d_1T \\ 0, & d_1T < t < T \end{cases}$$

Equation 4-8

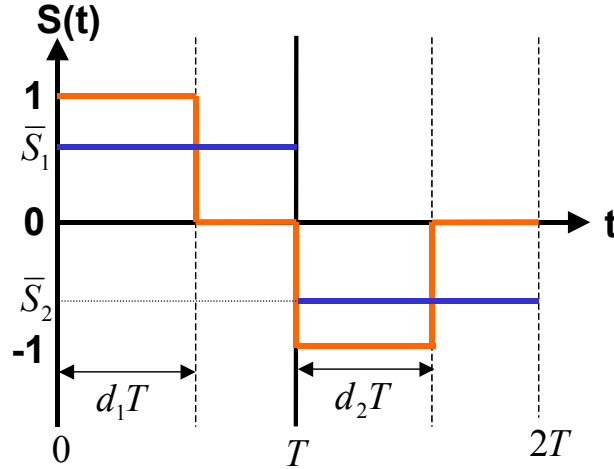


Figure 4-10. Averaged switching function over a switching cycle.

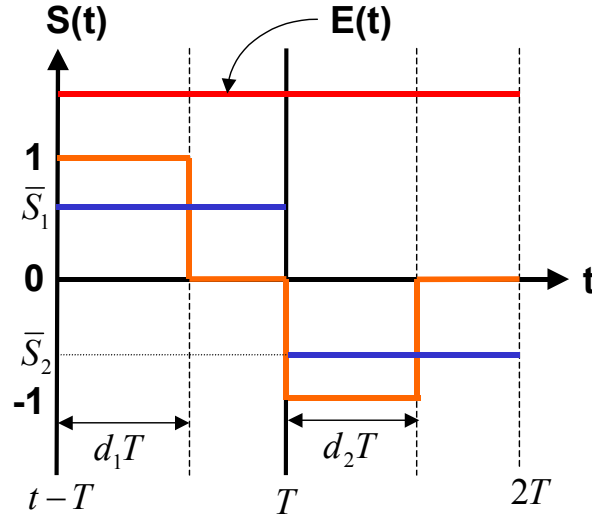


Figure 4-11. Average of the quadratic term.

To derive the average model of the H-bridge converter, the average operator is applied to the voltage and current in Equation 4-5 and Equation 4-6, respectively. The right-hand side of both equations is, however, made up of quadratic terms, representing the multiplication of two time-dependent terms. To simplify these quadratic terms, the DC voltages and the output currents of the converter are reasonably assumed to be constant in one switching cycle. These assumptions are practical, because firstly, the DC-link capacitors are relatively large in STATCOM applications; hence, their voltage is insignificantly changed over a switching period. Secondly, the effective switching frequency of converters, typically in the 500 Hz to 3 kHz range, is relatively high as compared to their fundamental frequencies, which are either 50 Hz or 60 Hz. To be clearly explained, the voltage in Equation 4-5 is used as an example, and is depicted in Figure 4-11. Based on the first assumption, Equation 4-5 can thus be averaged as follows:

$$\bar{v} = \frac{1}{T} \int_{t-T}^t S(\tau) d\tau \cdot E = d \cdot E .$$

Equation 4-9

Likewise, based on the second assumption, the current in Equation 4-6 can be averaged as follows:

$$\bar{i}_E = d \cdot i_O .$$

Equation 4-10

For a $2N+1$ -level cascaded converter, where N is the number of H-bridge converters per phase, average output-phase voltages can be expressed as a summation of average output voltages of N H-bridge converters, as shown in Equation 4-11, whereas its average DC capacitor output current can be expressed as shown in Equation 4-12:

$$V_{phase} = \sum_{j=1}^N d_j \cdot E_j , \text{ and}$$

Equation 4-11

$$\bar{i}_{Ej} = d_j \cdot i_{oj} ,$$

Equation 4-12

where $j = 1 \dots N$, and N is the number of H-bridge converters per phase.

Derived from Equation 4-11, Equation 4-12 and the switching model shown in Figure 4-9, a general average model in ABC coordinates for the CMC-based STATCOM shown in Figure 4-1 can be realized, as shown in Figure 4-12. In this average model, R_L represents the internal losses of the H-bridge converters. The ESR of high-power DC capacitors is neglected in this average model, because in practice, it is relatively small as compared to the impedance.

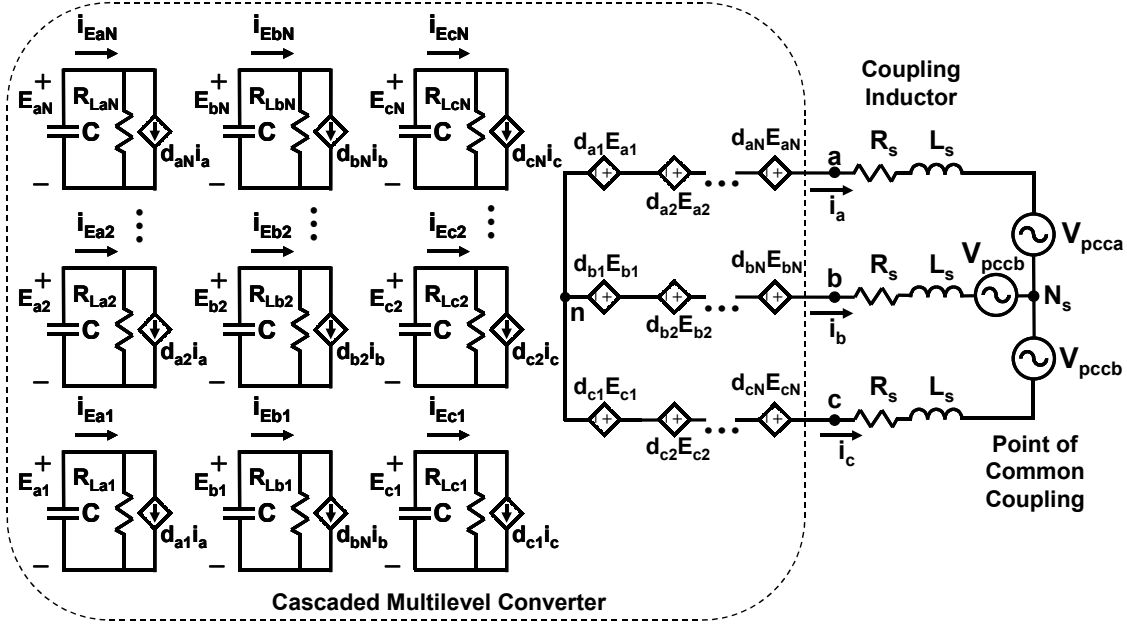


Figure 4-12. Average model of the cascaded-multilevel converter-based STATCOM in the ABC frame.

As shown in Figure 4-12, this average model is still too complicated to be used in the STATCOM-control design process. Therefore, to simplify the model, the following three assumptions are made based on the definition of average operator:

- 1) Based on a meaningful AC output control, all DC voltage sources are assumed to be equally regulated, i.e.,

$$E_j = E_{aj} = E_{bj} = E_{cj} , \text{ for } j = 1 \dots N , \text{ and}$$

$$E = E_1 = E_2 = \dots = E_N .$$

- 2) Internal losses in high-power converters are insignificant; therefore, the losses for each H-bridge converter in the same level are assumed to be identical, as follows:

$$R_{Lj} = R_{Laj} = R_{Lbj} = R_{Lcj} , \text{ for } j = 1 \dots N .$$

- 3) Due to equal synthesized output voltages, all duty cycles in the same phase are assumed to be identical, i.e.,

$$d_k = d_{k1} = d_{k2} = \dots = d_{kN}, \text{ for } k = a, b, c.$$

Based on these three assumptions, the average model in ABC coordinates (shown in Figure 4-12) can be simplified as shown in Figure 4-13.

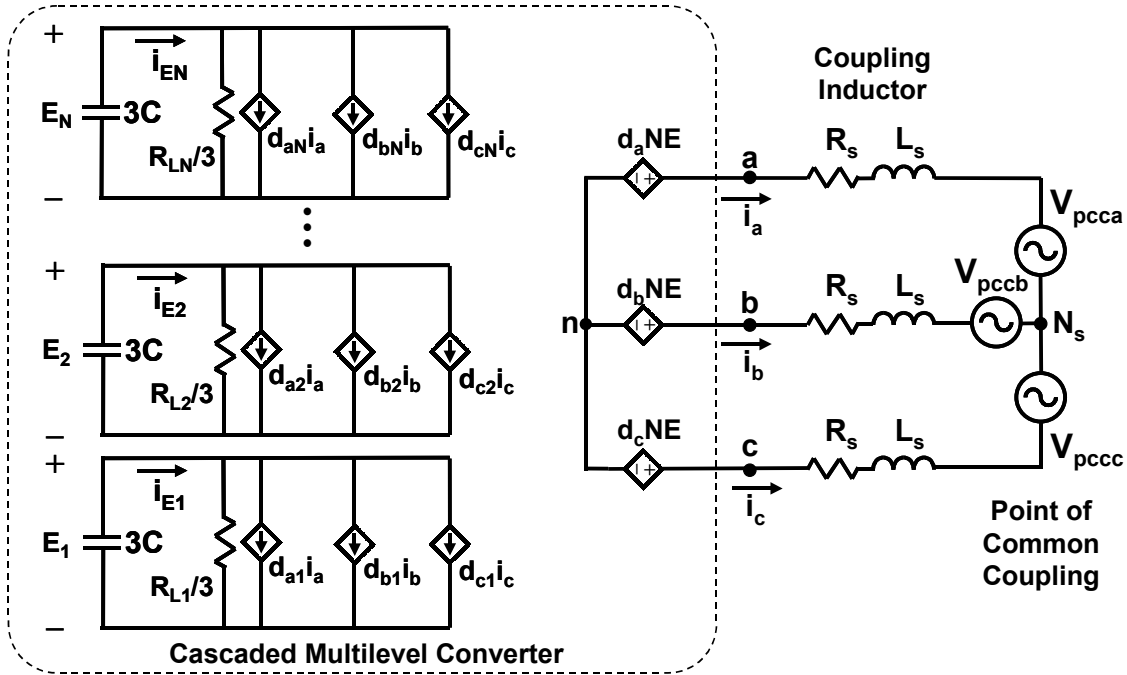


Figure 4-13. A simplified average model for the cascaded-multilevel converter-based STATCOM in the ABC frame.

III. Development of the Average Model in DQ0 Coordinates

According to the proposed decoupling control scheme, the control variables in DQ0 coordinates are utilized. From the average model in the ABC frame, as shown in Figure 4-13, two characteristic equations can be derived, as follows.

The three-phase output-current differential equation matrix for the CMCs is

$$\frac{d\vec{i}_{abc}}{dt} = \frac{E \cdot N \cdot \vec{d}_{abc}}{L_s} - \frac{\vec{v}_{pccabc}}{L_s} - \frac{R_s}{L_s} \cdot \vec{i}_{abc},$$

Equation 4-13

and the differential equation matrix of the common DC-link voltage is

$$\frac{dE}{dt} = -\frac{E}{R_{lj}C} - \frac{1}{3C} \vec{d}_{abcj}^T \cdot \vec{i}_{abc}, \quad j = 1 \dots N,$$

Equation 4-14

where $\vec{i}_{abc} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}$, $\vec{d}_{abcj} = \begin{bmatrix} d_{aj} \\ d_{bj} \\ d_{cj} \end{bmatrix}$, $\vec{v}_{pccabc} = \begin{bmatrix} v_{pcca} \\ v_{pccb} \\ v_{pccc} \end{bmatrix}$, and

N is the number of H-bridge converters per phase.

To transform the variables in ABC to DQ0 coordinates, Equation 4-13 and Equation 4-14 are multiplied on both sides by Park's transformation matrix.

Thus, the average output-current differential equation matrix in DQ0 coordinates for the CMCs applied in STATCOM is expressed as follows:

$$\frac{d}{dt} \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{N \cdot E}{L_s} \begin{bmatrix} d_d \\ d_q \\ d_0 \end{bmatrix} - \frac{1}{L_s} \begin{bmatrix} v_{pccd} \\ v_{pccq} \\ v_{pcc0} \end{bmatrix} - \begin{bmatrix} \frac{R_s}{L_s} & -\omega & 0 \\ \omega & \frac{R_s}{L_s} & 0 \\ 0 & 0 & \frac{R_s}{L_s} \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix},$$

Equation 4-15

and the differential equation matrix in DQ0 coordinates of the common DC-link voltage is

$$\frac{dE}{dt} = -\frac{3E}{R_{Lj}C} - \frac{1}{3C} \begin{bmatrix} d_{dj} & d_{qj} & d_{0j} \end{bmatrix} \cdot \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix}.$$

Equation 4-16

In this dissertation, the preferred Park's transformation matrix is

$$\bar{T}_{dq0/abc} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix},$$

Equation 4-17

where $\theta = \int_0^t \omega(\tau) d\tau + \theta(0)$, and $\omega(\tau)$ is the angular velocity.

Thus, a simplified average model for the CMC-based STATCOM in DQ0 coordinates can be obtained, as shown in Figure 4-14.

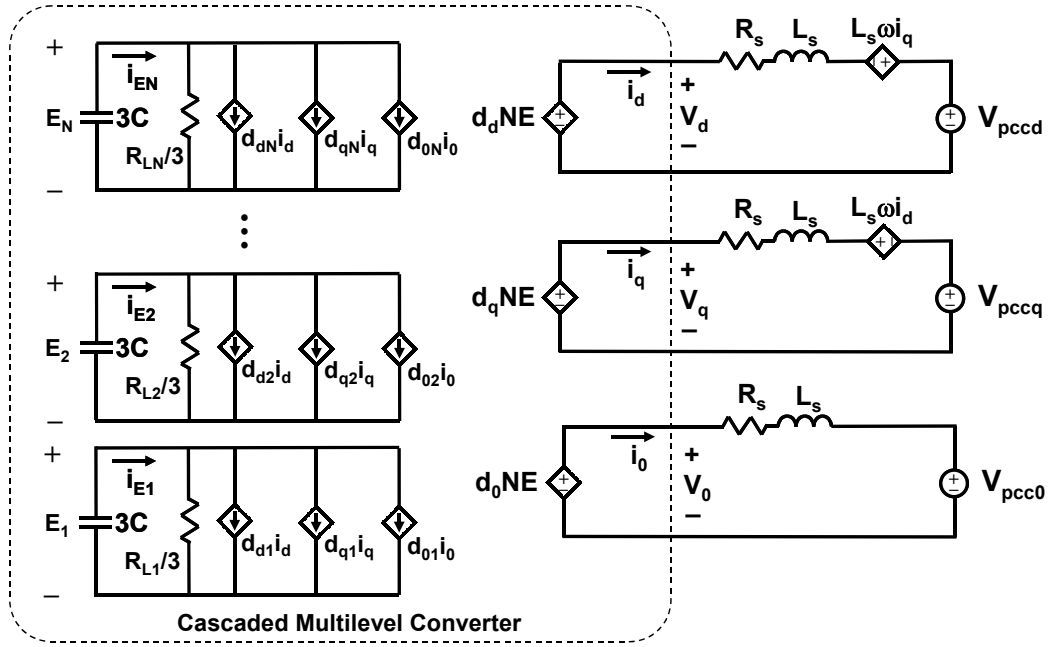


Figure 4-14. Simplified average model for the cascaded-multilevel converter-based STATCOM in DQ0 coordinates.

IV. Small-Signal Model in DQ0 Coordinates

A small-signal model can be developed by linearizing all variables in Equation 4-15 and Equation 4-16 around their quiescent operating points, which yields:

$$\frac{d}{dt} \begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \\ \tilde{i}_0 \end{bmatrix} = \frac{E}{L_s} \begin{bmatrix} \tilde{d}_d \\ \tilde{d}_q \\ \tilde{d}_0 \end{bmatrix} + \frac{\tilde{E}}{L_s} \begin{bmatrix} D_d \\ D_q \\ D_0 \end{bmatrix} - \frac{1}{L_s} \begin{bmatrix} \tilde{v}_{pccd} \\ \tilde{v}_{pccq} \\ \tilde{v}_{pcc0} \end{bmatrix} - \begin{bmatrix} \frac{R_s}{L_s} & -\omega & 0 \\ \omega & \frac{R_s}{L_s} & 0 \\ 0 & 0 & \frac{R_s}{L_s} \end{bmatrix} \cdot \begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \\ \tilde{i}_0 \end{bmatrix}, \text{ and}$$

Equation 4-18

$$\frac{d\tilde{E}_j}{dt} = -\frac{3\tilde{E}_j}{R_{Lj}C} - \frac{1}{3C} \begin{bmatrix} I_d & I_q & I_0 \end{bmatrix} \cdot \begin{bmatrix} \tilde{d}_{dj} \\ \tilde{d}_{qj} \\ \tilde{d}_{0j} \end{bmatrix} - \frac{1}{3C} \begin{bmatrix} D_{dj} & D_{qj} & D_{0j} \end{bmatrix} \cdot \begin{bmatrix} \tilde{i}_d \\ \tilde{i}_q \\ \tilde{i}_0 \end{bmatrix}, \quad j = 1 \dots N,$$

Equation 4-19

where $\tilde{i}$ is the small-signal AC variation of i , whose quiescent operating point is I ;

$\tilde{d}$ is the small-signal AC variation of d , whose quiescent operation point is D ; and

N is the number of H-bridge converters per phase.

Using Equation 4-18 and Equation 4-19, the small-signal model of the STATCOM system is depicted in Figure 4-15.

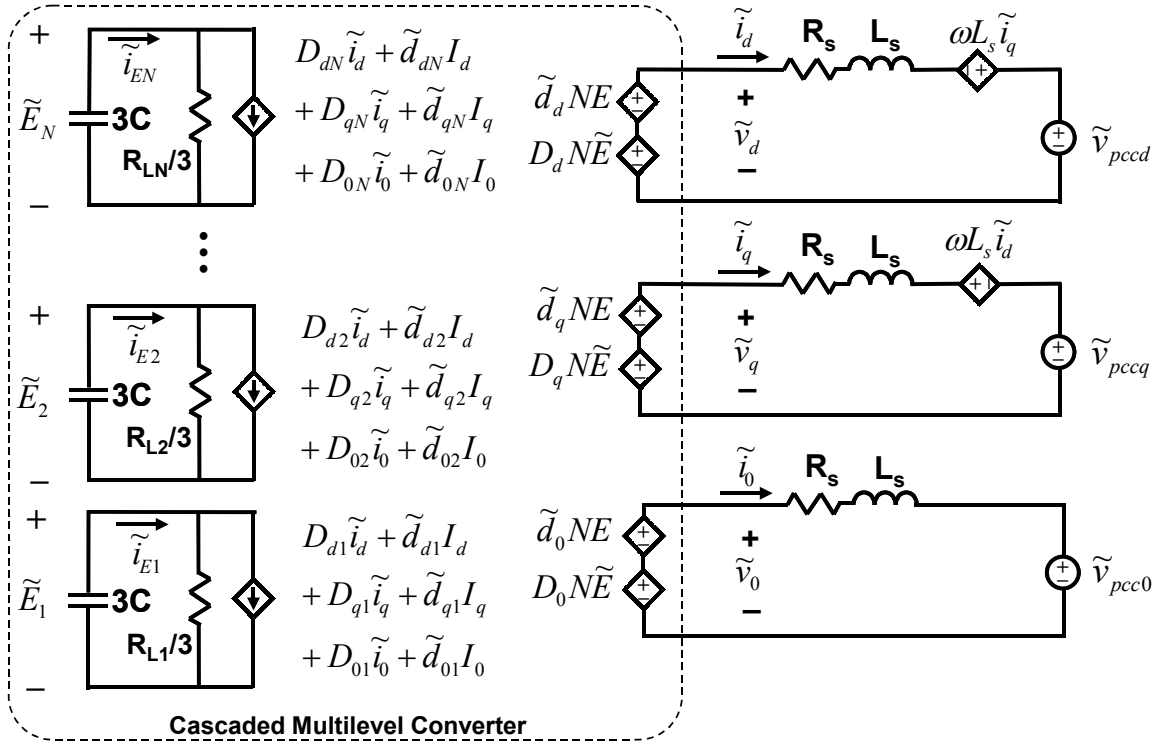


Figure 4-15. Small-signal model for the cascaded-multilevel converter-based STATCOM in DQ0 coordinates.

Based on the derived small-signal model, the following key open-loop transfer functions of the STATCOM system are listed as follows.

1. Control-to-Output-Current Transfer Function:

$$G_{idd} = \frac{\tilde{i}_d}{\tilde{d}_d}, \text{ and } G_{iqq} = \frac{\tilde{i}_q}{\tilde{d}_q}.$$

Equation 4-20

2. Control-to-Cross-Coupling-Output-Current Transfer Function:

$$G_{iqd} = \frac{\tilde{i}_q}{\tilde{d}_d}, \text{ and } G_{idq} = \frac{\tilde{i}_d}{\tilde{d}_q}.$$

Equation 4-21

3. Output-Current-to-DC-Bus-Voltage Transfer Function:

$$G_{Eid} = \frac{\tilde{E}_j}{\tilde{i}_d}, \quad j = 1 \dots N,$$

Equation 4-22

where N is the number of H-bridge converters per phase.

Figure 4-16 illustrates the block diagram of the open-loop transfer functions of the CMC-based STATCOM. Based on these transfer functions, the proposed control technique is designed, as presented in Chapter 5.

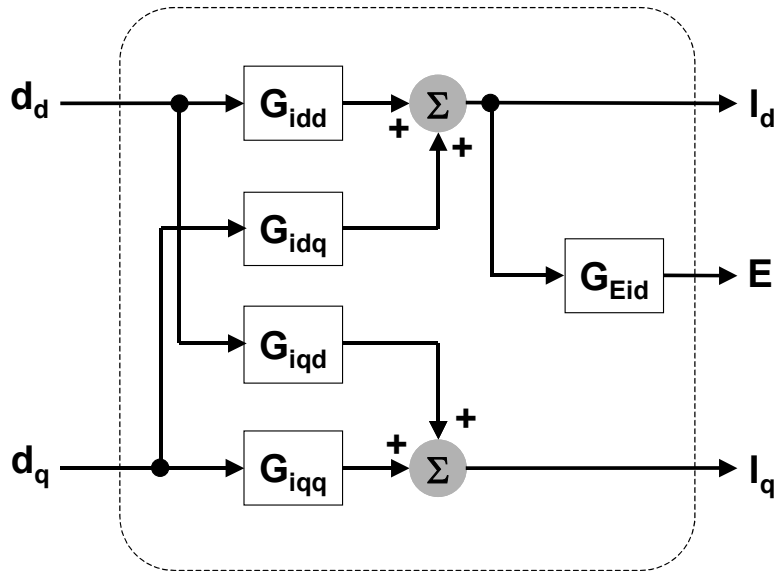


Figure 4-16. Open-loop transfer functions.

V. Transfer Function Derivation

A. Control-to-Output-Current Transfer Function, G_{idd}

From Figure 4-15, by setting other perturbations to zero, the KVL of the D channel is expressed as:

$$\tilde{d}_d NE + \omega L_s \tilde{i}_q = (R_s + SL_s) \tilde{i}_d.$$

Equation 4-23

By applying the KVL to the Q channel, its output current is derived, as follows:

$$\tilde{i}_q = \frac{-\omega L_s}{(R_s + SL_s)} \tilde{i}_d.$$

Equation 4-24

Substituting Equation 4-24 into Equation 4-23 yields

$$G_{idd} = \frac{\tilde{i}_d}{\tilde{d}_d} = \frac{NE(R_s + L_s S)}{L_s^2 S^2 + 2L_s R_s S + (R_s^2 + \omega^2 L_s^2)}.$$

Equation 4-25

Equation 4-25 can also be expressed as a standard second-order transfer function, as follows:

$$G_{idd} = \frac{\tilde{i}_d}{\tilde{d}_d} = \frac{K_{idd} \left(\frac{S}{\omega_z} + 1 \right)}{\left(\frac{S}{\omega_p} \right)^2 + \frac{S}{Q\omega_p} + 1},$$

Equation 4-26

where

$$K_{idd} = \frac{NER_s}{R_s^2 + (\omega L_s)^2}, \quad Q = \frac{\sqrt{R_s^2 + (\omega L_s)^2}}{2R_s},$$

$$\omega_p = \frac{\sqrt{R_s^2 + (\omega L_s)^2}}{L_s}, \quad \text{and } \omega_z = \frac{R_s}{L_s}.$$

From the small-signal model shown in Figure 4-15,

$$G_{iqq} = \frac{\tilde{i}_q}{\tilde{d}_q} = \frac{NE(R_s + L_s S)}{L_s^2 S^2 + 2L_s R_s S + (R_s^2 + \omega^2 L_s^2)}, \text{ or}$$

Equation 4-27

$$G_{iqq} = \frac{\tilde{i}_q}{\tilde{d}_q} = \frac{K_{iqq} \left(\frac{S}{\omega_z} + 1 \right)}{\left(\frac{S}{\omega_p} \right)^2 + \frac{S}{Q\omega_p} + 1},$$

Equation 4-28

where

$$K_{iqq} = \frac{NER_s}{R_s^2 + (\omega L_s)^2}, \quad Q = \frac{\sqrt{R_s^2 + (\omega L_s)^2}}{2R_s},$$

$$\omega_p = \frac{\sqrt{R_s^2 + (\omega L_s)^2}}{L_s}, \quad \text{and } \omega_z = \frac{R_s}{L_s}.$$

B. Control-to-Cross-Coupling-Output-Current Transfer Function, G_{iqd}

From Equation 4-24, the output current in the D channel is

$$\tilde{i}_d = \frac{-(R_s + SL_s)}{\omega L_s} \tilde{i}_q.$$

Equation 4-29

Substituting the D-channel output current into Equation 4-23, yields:

$$G_{iqd} = \frac{\tilde{i}_q}{\tilde{d}_d} = \frac{-NE\omega L_s}{L_s^2 S^2 + 2L_s R_s S + (R_s^2 + \omega^2 L_s^2)}, \text{ or}$$

Equation 4-30

$$G_{iqd} = \frac{\tilde{i}_q}{\tilde{d}_d} = \frac{K_{iqd}}{\left(\frac{S}{\omega_p}\right)^2 + \frac{S}{Q\omega_p} + 1},$$

Equation 4-31

where

$$K_{iqd} = \frac{-\omega L N E}{R_s^2 + (\omega L_s)^2}, \quad Q = \frac{\sqrt{R_s^2 + (\omega L_s)^2}}{2R_s},$$

$$\omega_p = \frac{\sqrt{R_s^2 + (\omega L_s)^2}}{L_s}, \quad \text{and } \omega_z = \frac{R_s}{L_s}.$$

Likewise, the transfer function G_{idq} is

$$G_{idq} = \frac{\tilde{i}_d}{\tilde{d}_q} = \frac{-NE\omega L_s}{L_s^2 S^2 + 2L_s R_s S + (R_s^2 + \omega^2 L_s^2)}, \text{ or}$$

Equation 4-32

$$G_{idq} = \frac{\tilde{i}_d}{\tilde{d}_q} = \frac{K_{idq}}{\left(\frac{S}{\omega_p}\right)^2 + \frac{S}{Q\omega_p} + 1},$$

Equation 4-33

where

$$K_{idq} = \frac{-\omega L N E}{R_s^2 + (\omega L_s)^2}, \quad Q = \frac{\sqrt{R_s^2 + (\omega L_s)^2}}{2R_s},$$

$$\omega_p = \frac{\sqrt{R_s^2 + (\omega L_s)^2}}{L_s}, \quad \text{and } \omega_z = \frac{R_s}{L_s}.$$

C. Output-Current-to-DC-Bus-Voltage Transfer Function, G_{Eid}

Using the DC capacitor circuit shown in Figure 4-15, with perturbations of the D-channel and Q-channel currents, yields:

$$\tilde{E}_j = -\frac{(D_{dj}\tilde{i}_d + D_{qj}\tilde{i}_q)}{3CS}, \quad j = 1 \dots N,$$

Equation 4-34

where N is the number of H-bridge converter per phase.

Substituting the Q-channel current as a function of the D-channel current, as shown in Equation 4-24, into Equation 4-34, yields:

$$G_{Eidj} = \frac{\tilde{E}_j}{\tilde{i}_d} = - \left[\frac{D_{dj}L_sS + (D_{qj}\omega L_s + D_{dj}R_s)}{3CL_sS^2 + 3CR_sS + D_{dj}D_{qj}N} \right], \text{ or}$$

Equation 4-35

$$G_{Eidj} = \frac{\tilde{E}_j}{\tilde{i}_d} = \frac{K_{Eid} \left(\frac{S}{\omega_z} + 1 \right)}{\left(\frac{S}{\omega_p} \right)^2 + \frac{S}{Q\omega_p} + 1},$$

Equation 4-36

where

$$K_{Eidj} = \frac{D_{qj}\omega L_s + D_{dj}R_s}{D_{dj}D_{qj}N}, \quad Q = \sqrt{\frac{D_{dj}D_{qj}NL_s}{3CR_s^2}},$$

$$\omega_p = \sqrt{\frac{D_{dj}D_{qj}N}{3CL_s}}, \quad \text{and } \omega_z = \frac{D_{qj}\omega}{D_{dj}} + \frac{R_s}{L_s}.$$

4.4 Summary

This chapter presented the operating principles of the CMC-based STATCOM system. Modeling development for the CMC in both ABC and DQ0 coordinates were presented, and these could generally be applied in any applications. Based on practical assumptions, the simplified model of the STATCOM utilizing the CMC was proposed. The key transfer functions, which will be used in the control design process, were derived.

Chapter 6 IMPROVEMENT IN CASCADED-MULTILEVEL VOLTAGE-SOURCE CONVERTERS

When the cascaded-multilevel VSC is selected as the main power-conversion topology, two interesting and challenging issues are worthy of investigation. One is how to minimize its number of isolated DC sources without degrading any characteristics. Reduction in the number of isolated DC sources, of course, means greater cost-effectiveness. The second issue is how to improve the quality of its synthesized output waveforms. The improvement should be effective both in the quality of the output-voltage waveforms and in a reduction in the total system losses that are generated by the switching events of the main semiconductor devices.

To improve the quality of the synthesized output waveform of multilevel converters, an optimum harmonic-reduction technique is proposed. Not only does the proposed scheme show superior quality in terms of generated waveforms, but it also can expand its capability through the entire range of modulation indices, as well as any number of levels.

To minimize the number of isolated DC sources in the CMC, a new CMC topology is presented. It requires only 50% of the isolated DC sources utilized in a conventional five-level cascaded converter.

Section 6.1 proposes a novel modulation technique to be applied to multilevel VSCs that are suitable for high-voltage, high-power applications such as power supplies and FACTS devices. The proposed technique can generate output-stepped waveforms with a wide range of modulation indices and minimized THD for the voltage. The main power devices switch only once per cycle, as is suitable for high-power applications. In addition to meeting the minimum turn-on and turn-off time requirements for high-power semiconductor switches, the proposed technique excludes from the synthesized waveform any pulses that are either too narrow or too wide. Moreover, by using a systematic method, only the polarities and the number of levels need to be determined for different modulation levels. To verify the theory and the simulation results, a cascaded converter-based hardware prototype, including a low-cost microcontroller as well as modularized IGBT-based power stages and gate-driver circuits, is implemented. Experimental

results indicate that the proposed technique is effective for the reduction of harmonics in multilevel converters, and both the theoretical and simulation results are well validated.

In Section 6.2 , a new CMC is presented. By using systematic analysis, a novel multilevel converter with a minimum number of separated DC sources has been developed. This multilevel converter requires only 50% of the number of DC sources required in conventional five-level cascaded converters. In addition, the three-phase output voltages of this converter can be easily balanced because they are synthesized by using the same DC sources. The harmonic-reduction method is proposed to eliminate both the fifth and seventh harmonics. To demonstrate its performance, the proposed cascaded converter is applied in a motor-drive system; however, it can be employed in high-voltage power supplies and FACTS controllers. Simulation results show that the proposed converter can drive an induction motor with satisfactory speed responses. Moreover, the proposed method is easily realized.

6.1 Optimum Harmonic Reduction with a Wide Range of Modulation Indices for Multilevel Converters

Given the requirements for quality and efficiency in high-power systems, as well as the limitations of switching speed, a low switching frequency and minimized THD are desirable. By applying appropriate modulation schemes, these two goals can be achieved simultaneously. The challenge of the modulation techniques, therefore, plays a very important role in multilevel converter circuits.

Previous harmonic optimization techniques [A3], [J3] initiated the concept of achieving harmonic reduction using selected harmonic elimination. These techniques require more than one switching per cycle to obtain a wide modulation index range. In this research, the proposed modulation technique involves generalizing the optimum harmonic-reduction technique that switches the main power devices once per cycle, and at the same time, achieving a wide range of modulation indices. The output voltage presents a stepped-type wave shape, similar to that which can be achieved by using the traditional methods. This modulation technique is fairly simple to implement in multilevel converters. The basic concept is to swap the polarities of some levels so that a low modulation index can be obtained. The computation effort is seamless for the entire

range of modulation indices. Consider, for example, a seven-level cascaded converter. The traditional selected harmonic elimination can only reach the modulation index of 0.5. The proposed method, however, indicates that a modulation index of 0.1 can be easily achieved.

I. Optimized Harmonic Stepped-Waveform Technique

A. Conventional Stepped Waveforms

Figure 6-1 shows a generalized quarter-wave symmetric stepped-voltage waveform synthesized by a $2m+1$ -level converter, where m is the number of switching angles. By applying the Fourier series, the amplitude of any odd n^{th} harmonic of the stepped waveform can be expressed as Equation 6-1, whereas the amplitudes of all even harmonics are zero:

$$h_n = \frac{4}{n\pi} \sum_{k=1}^m [V_k \cos(n\alpha_k)],$$

Equation 6-1

where h_n is the n^{th} harmonic, n is the odd-harmonic order, m is the number of switching angles, α_k is the k^{th} switching angle, and V_k is the k^{th} DC bus voltage.

According to Figure 6-1, α_1 to α_m must satisfy the following condition:

$$\alpha_1 < \alpha_2 < \dots < \alpha_m < \frac{\pi}{2}.$$

Equation 6-2

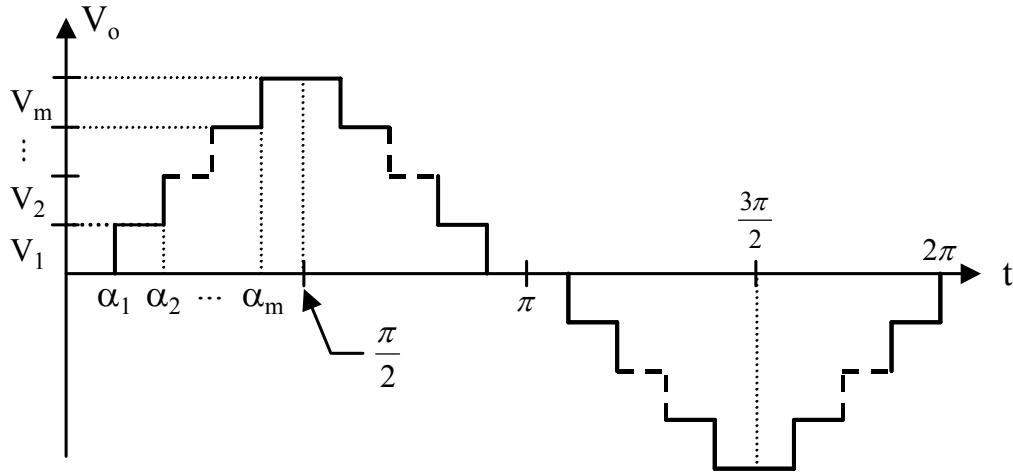


Figure 6-1. Generalized $2m+1$ -level quarter-wave stepped-voltage waveform.

Consider Equation 6-1. To minimize harmonic distortion and to achieve adjustable amplitude for the fundamental component, up to $m-1$ harmonic components can be removed from the voltage waveform. In general, to minimize the size of the output filter circuit, the most significant low-frequency harmonic components will be chosen for elimination. Then, high-frequency harmonic components can be readily removed by the filter circuits. According to Equation 6-1, to keep a constant number of eliminated harmonics, all switching angles must be less than $\pi/2$. However, if the switching angles do not satisfy the condition, this scheme no longer works. As a result, this modulation scheme basically provides a narrow range of modulation indices, which is its main disadvantage. For example, in a seven-level, equally stepped waveform, to continue eliminating two surplus harmonic components, its modulation index is only available from 0.5 to 1.05. At any modulation index lower than 0.5, if this scheme is still applied, the number of harmonic components that might be eliminated will reduce from two to one. As a result, a low-order harmonic component appears in the output waveform. In turn, the voltage THD increases. In the following section, a new technique is presented to overcome the limitations of the conventional scheme.

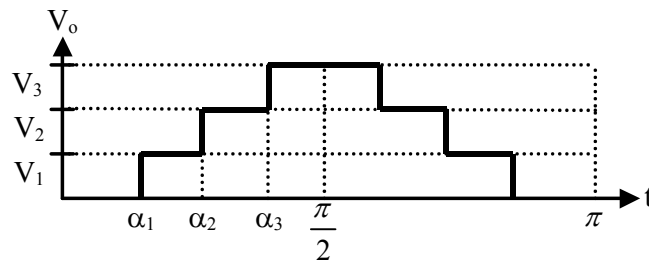
B. New Stepped Waveforms

As discussed earlier, the traditional stepped waveform provides a narrow modulation index range. This research, therefore, proposes a new modulation technique, which is an extension of the conventional stepped-waveform technique. The proposed technique can generate output-voltage waveforms with a wide range of modulation indices. With a set of appropriate switching angles, this proposed modulation scheme also minimizes the THD of the synthesized waveforms for certain modulation indices. In addition to meeting the minimum turn-on and turn-off time requirements for high-power semiconductor devices, the proposed technique also avoids undesirable pulses from the synthesized waveform.

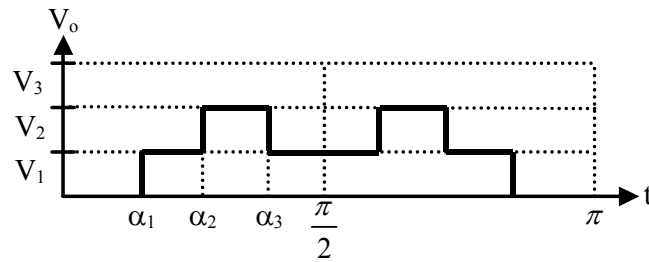
To minimize the THD of the line voltage, the lowest significant $m-1$ non-triplen harmonic components need to be eliminated from the synthesized phase voltage, where m is the number of switching angles in the phase-voltage waveform. Take a three-phase, seven-level stepped waveform as an example. In this case, $m = 3$. To minimize the line-to-line voltage harmonic distortion and to achieve adjustable amplitude for the fundamental component, from Equation 6-1, up to two surplus harmonics are selected for removal. Thus, the fifth and seventh harmonics, which are the two lowest non-triplen harmonics, are chosen for elimination from the phase voltages.

The new stepped-waveform concept, which provides a wide range of modulation indices and keeps the same number of eliminated harmonic components, is proposed here. Figure 6-2 illustrates the positive half-cycle of seven-level stepped waveforms with different modulation index levels. In this case, the range of modulation indices can be divided into three levels; i.e., high, middle and low. An output waveform with a high modulation index level is shown in Figure 6-2(a). Whenever α_3 is greater than $\pi/2$, this waveform no longer exists. Therefore, the output waveform shown in Figure 6-2(b), which gives a middle range of modulation indices, will be applied instead. The basic idea is to swap the polarity of the top level of the waveform from positive to negative, while the polarities of the other levels are not changed. When the switching angles α_1 to α_3 in Figure 6-2(b) are not convergent at a low modulation index, the output waveform shown in Figure 6-2(c) will replace it. At a low modulation index level, the positive polarity of the middle level of the output waveform is made negative, and the polarity of the top

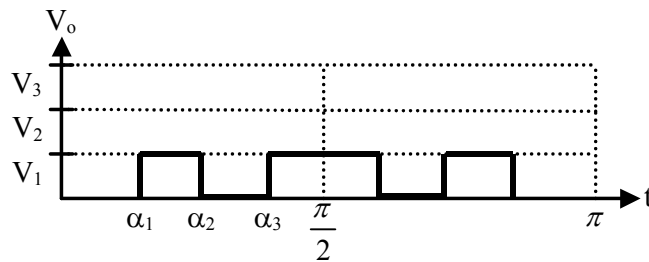
level is made positive. Generally, a stepped waveform, which consists of m switching angles, can be divided into m modulation index levels. By using this technique, wide modulation indices, low switching frequencies and minimized THD in the output waveforms can be achieved.



(a)



(b)



(c)

Figure 6-2. A positive half-cycle of a seven-level stepped waveform with different modulation indices: (a) high modulation index, (b) middle modulation index, and (c) low modulation index.

II. Optimum Harmonic Reduction with a Wide Range of Modulation Indices in the $2m+1$ -Level Waveform

A. Selective Harmonic Elimination

By using the Fourier series, the amplitude of the odd harmonics of the waveforms shown in Figure 6-2(a) through (c) are expressed as follows:

$$h_n = \frac{4}{n\pi} [V_1 \cos(n\alpha_1) + V_2 \cos(n\alpha_2) + V_3 \cos(n\alpha_3)],$$

Equation 6-3

$$h_n = \frac{4}{n\pi} [V_1 \cos(n\alpha_1) + V_2 \cos(n\alpha_2) - V_3 \cos(n\alpha_3)], \text{ and}$$

Equation 6-4

$$h_n = \frac{4}{n\pi} [V_1 \cos(n\alpha_1) - V_2 \cos(n\alpha_2) + V_3 \cos(n\alpha_3)].$$

Equation 6-5

According to Equation 6-3 through Equation 6-5, α_1 through α_3 must satisfy the following condition:

$$\alpha_1 < \alpha_2 < \alpha_3 < \frac{\pi}{2}.$$

Because of their symmetric characteristic, no even-harmonic components exist in these three waveforms. By inspecting Equation 6-3 through Equation 6-5 and Figure 6-2, at an edge corresponding to a switching angle, the rising edge provides positive polarity for the corresponding cosine term, whereas the falling edge gives the cosine term a negative polarity.

Following this observation, the generalized amplitudes of the odd-harmonic components in a $2m+1$ -level output waveform for all modulation indices is given as

$$h_n = \frac{4}{n\pi} [V_1 \cos(n\alpha_1) \pm V_2 \cos(n\alpha_2) \pm \dots \pm V_m \cos(n\alpha_m)].$$

Equation 6-6

Switching angles α_1 through α_m must satisfy the following condition:

$$\alpha_1 < \alpha_2 < \dots < \alpha_m < \frac{\pi}{2}.$$

In Equation 6-6, the positive sign expresses the rising edge, and the negative sign expresses the falling edge. Based on the design for the power stage of the CMC, the voltages of DC links are equally regulated, i.e.,

$$V_1 = V_2 = \dots = V_m = V_{dc}.$$

Equation 6-7

Therefore, Equation 6-6 becomes

$$h_n = \frac{4V_{dc}}{n\pi} [\cos(n\alpha_1) \pm \cos(n\alpha_2) \pm \dots \pm \cos(n\alpha_m)].$$

Equation 6-8

By using systematic analysis, only the polarities and the number of levels are required to determine the switching angles for different modulation index levels in any multilevel topologies to which multilevel synchronous modulation is applied.

B. Minimum Turn-On and Turn-Off Time Considerations

To properly operate high-power semiconductor devices, minimum turn-on time, $t_{on(min)}$, and minimum turn-off time, $t_{off(min)}$, need to be taken into account. The GTO is used as an example. The minimum turn-on time is the minimum time required by the GTO to establish uniform anode-current conduction. To be able to turn off its rated anode current under the specified conditions, a minimum turn-on time is also necessary for the GTO. Normally, the GTO is connected to a snubber circuit for turn-off protection. During the on-state, the snubber capacitor

must be discharged so that it is ready for dv/dt protection at turn-off. Therefore, another minimum on-time is required for the snubber to recover. Hence, the control logic for the GTO is generated according to these two minimum turn-on times, i.e., minimum on-time for the GTO and minimum on-time for the snubber. On the other hand, the minimum turn-off time is the minimum time that the GTO requires before it may be triggered again by a positive gate current. If the device is re-triggered during this time, there is a certain risk of localized turn-on, and destruction may result.

Two well-known multilevel converter topologies are investigated in terms of how the minimum on-time and off-time affect their synthesized output waveforms. Figure 6-3(a) and (b), for example, illustrate a five-level diode-clamped converter and a five-level cascaded converter, respectively. DC voltage sources are assumed to be well balanced in both topologies. Now, consider a five-level phase voltage, V_{an} , as shown in Figure 6-4(a), for a high modulation index. Figure 6-4(b) shows the gate signals of top switches S_{a1} through S_{a4} . The other four gate signals of the bottom switch, S'_{a1} through S'_{a4} , are complementary to the signals of the top switches, S_{a1} through S_{a4} . Therefore, they are not shown here. From Figure 6-4(b), gate signal S_{a1} follows the top-level waveform shown in Figure 6-4(a), while gate signal S_{a4} follows the bottom-level waveform. Hence, pulse p must satisfy both the minimum turn-on time of switch S_{a1} and the minimum turn-off time of switch S_{a4} . However, the power semiconductor devices can be controlled to avoid undesirable pulses by coordinating the gate signals of the other two phases. Because of its complexity, this method is not used in conjunction with the proposed technique. In the CMC, a possible set of four gate signals, S_{a1} through S_{a4} , of the top-level H-bridge converter is shown in Figure 6-4(c). It is obvious that the minimum turn-on and turn-off times are not required in this topology. Figure 6-5 shows the five-level phase voltage, V_{an} , for a low modulation index. Clearly, the same scenario exists here.

By observation, the greatest switching angle, α_m , must take into account the minimum turn-on and turn-off times. Hence, α_m in Figure 6-1 must satisfy the following condition:

$$\alpha_m < \frac{\pi}{2} - (\max(t_{on(\min)}, t_{off(\min)}) \cdot \pi \cdot f_L).$$

Equation 6-9

To explain the approach numerically, the 5SGF40L4502-4.5kV/4.0kA GTO from ABB is used as an example. According to the datasheet, the required minimum turn-on time is 100 μ S. The minimum turn-off time of this GTO is also 100 μ S. In this example, the turn-on time for the snubber circuit is assumed to be less than 100 μ S. Based on a 60Hz system, from Equation 6-9, α_m must be less than 88.92° to meet the minimum turn-on and turn-off times of the given GTO. As a result, whenever α_m is greater than 88.92°, a switching pattern for different modulation index levels will be applied.

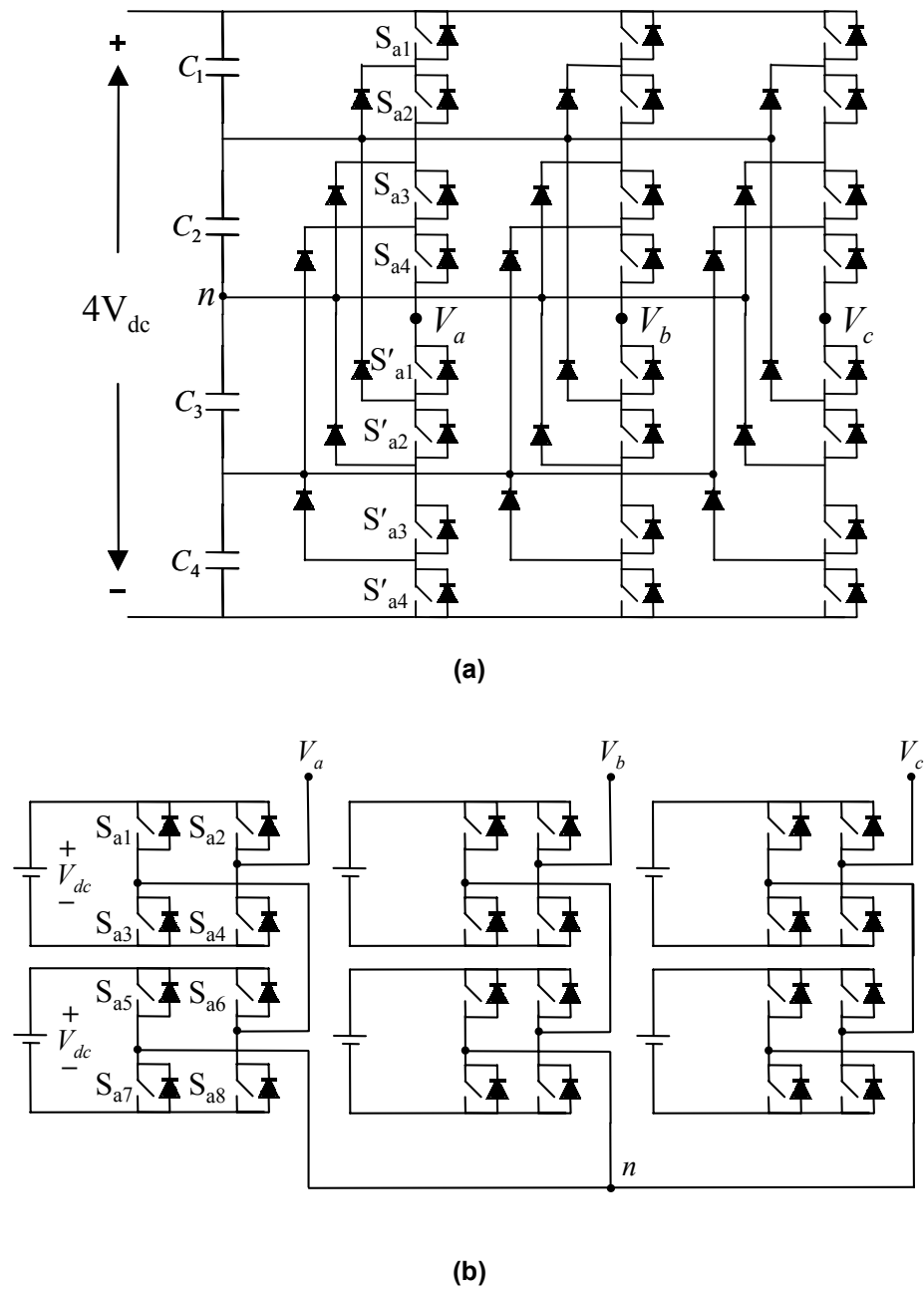


Figure 6-3. (a) A five-level diode-clamped converter and (b) a five-level cascaded converter.

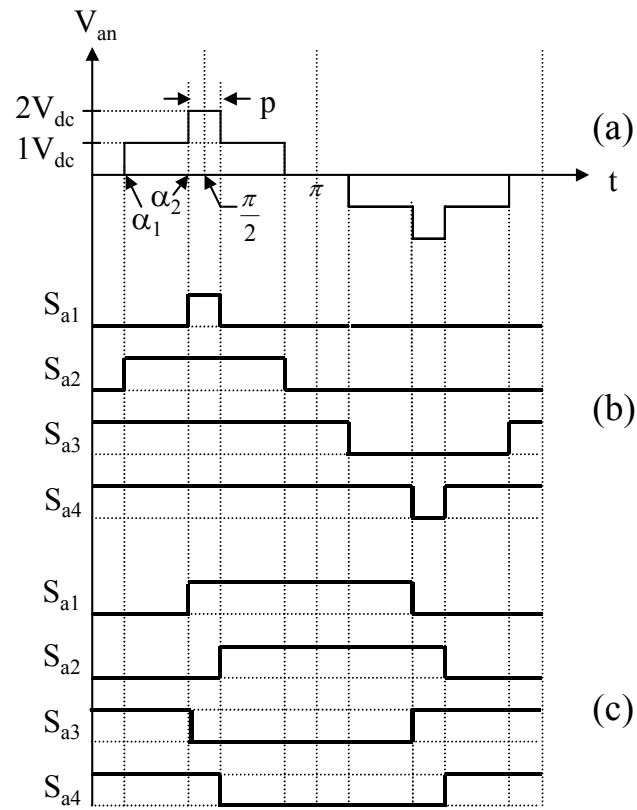


Figure 6-4. (a) A five-level phase-voltage waveform for a high modulation index, (b) gate signals of the top four switches of the diode-clamped converter shown in Figure 6-3(a), and (c) gate signals of the four switches of the top H-bridge converter of the cascaded converter shown in Figure 6-3(b).

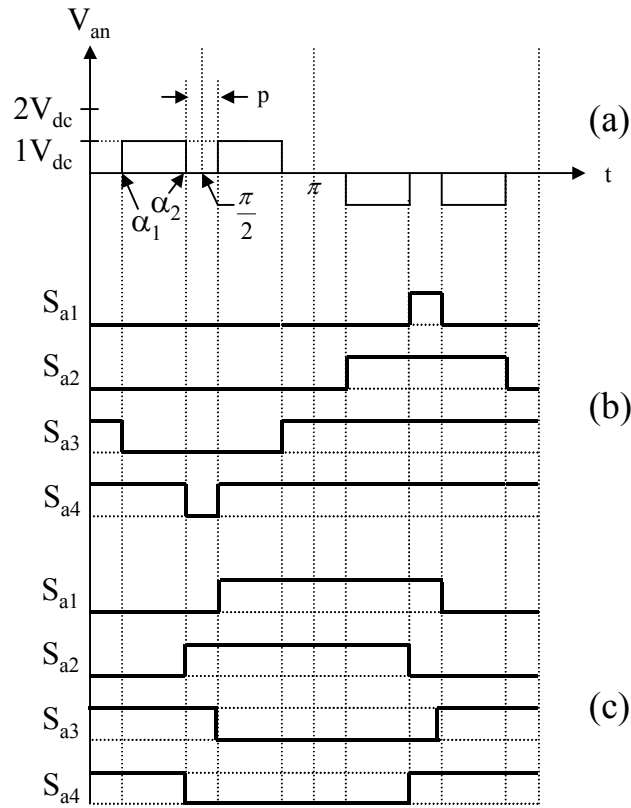


Figure 6-5. (a) A five-level phase-voltage waveform for a low modulation index, (b) gate signals of the top four switches of the diode-clamped converter shown in Figure 6-3(a), and (c) gate signals of the four switches of the top H-bridge converter of the cascaded converter shown in Figure 6-3(b).

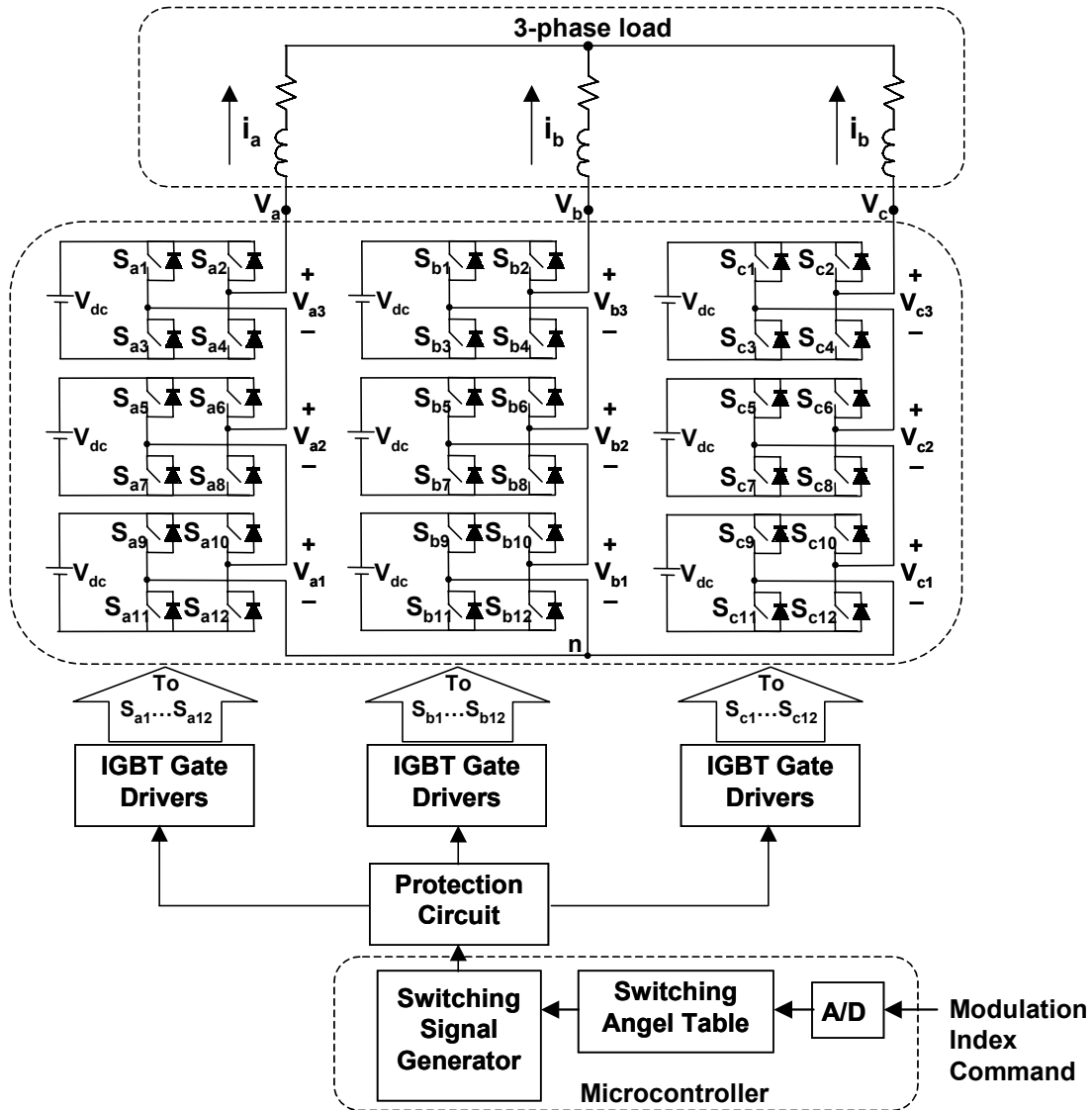


Figure 6-6. A seven-level cascaded converter system.

III. Simulation Results and Experimental Results

In this chapter, a seven-level cascaded converter, which is shown in Figure 6-6, is one of the topologies chosen for study. The modulation index for the cascaded-multilevel waveform, M , is defined as follows:

$$M = \frac{h_1}{mV_{dc}}.$$

Equation 6-10

A seven-level waveform for a medium modulation index level is used as an example. To minimize the line-voltage THD, the fifth and seventh harmonics need to be eliminated from the phase voltage. Thus, from Equation 6-8 and Equation 6-10, a set of nonlinear equations for $M = 0.4$ are given as follows:

$$[\cos(\alpha_1) + \cos(\alpha_2) - \cos(\alpha_3)] = \frac{3(0.4)\pi}{4},$$

Equation 6-11

$$[\cos(5\alpha_1) + \cos(5\alpha_2) - \cos(5\alpha_3)] = 0, \text{ and}$$

Equation 6-12

$$[\cos(7\alpha_1) + \cos(7\alpha_2) - \cos(7\alpha_3)] = 0.$$

Equation 6-13

By using the Newton-Raphson method, the switching angles for a given modulation index can be easily obtained from Equation 6-11 through Equation 6-13 [J3], [J6]. Likewise, the switching angles for other modulation indices can be solved, and some of these are listed in Table 1.

To indicate the quality of the output waveform, the line-voltage THD is defined as follows:

$$THD(\%) = \frac{\sqrt{\sum_{n=2}^{200} [h_n]^2}}{h_1} \cdot 100.$$

Equation 6-14

Figure 6-7 shows the relationship between all modulation indices and the calculated level of line-voltage THD. It shows that the line-voltage THD is inversely proportional to the modulation index. It is possible to reduce the voltage THD at a lower modulation index; however, the proposed technique needs to either be extended to include more than one switching per cycle or to be applied in conjunction with a small low-pass filter circuit.

TABLE 6-1. CALCULATED SWITCHING ANGLES FOR DIFFERENT MODULATION INDEX LEVELS.

Modulation Index Level	Modulation Index, M	a1	a2	a3
High	1.05	12.57°	23.81°	54.33°
	1.00	11.68°	31.18°	58.58°
	0.85	22.77°	49.38°	64.57°
	0.70	38.34°	53.93°	73.96°
	0.60	39.43°	58.58°	83.10°
Medium	0.50	19.32°	66.11°	80.18°
	0.40	44.17°	74.33°	87.40°
	0.36	45.85°	79.87°	88.62°
Low	0.30	29.23°	39.24°	52.51°
	0.20	50.92°	63.36°	73.19°
	0.10	55.85°	63.43°	83.02°
	0.05	57.98°	61.86°	86.60°

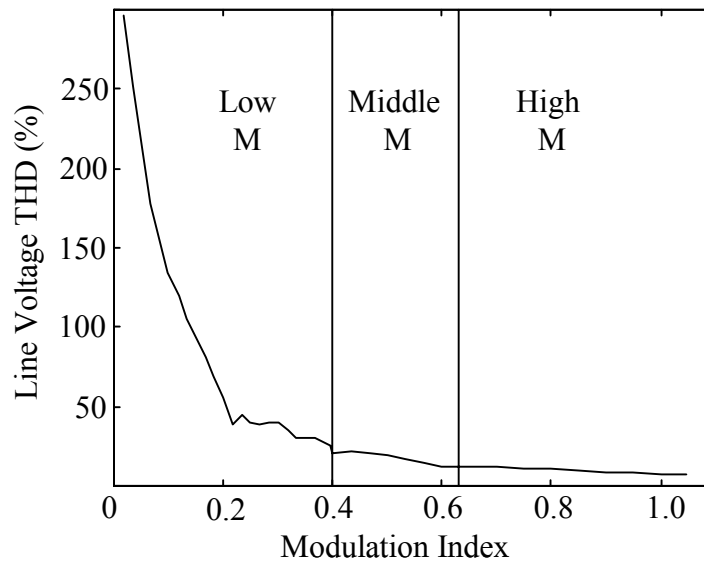
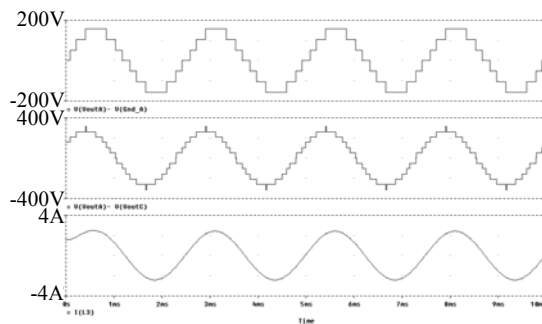


Figure 6-7. Modulation index vs. line-voltage THD.

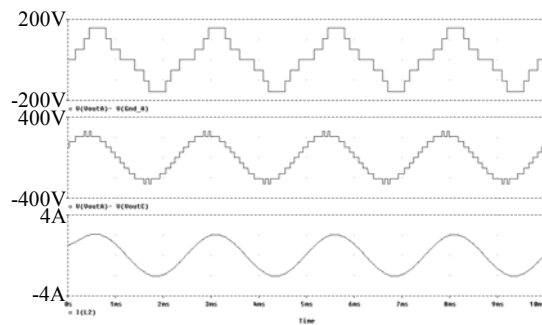
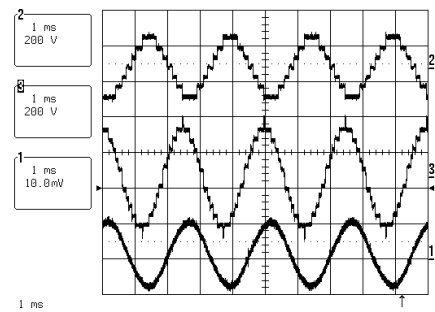
To verify the simulation results, a seven-level VSC, using cascaded converters with separated DC sources, as shown in Figure 6-6, is used as a hardware prototype. Four HGT30M60B-model IGBTs are used as the main switches, which are connected in full-bridge converter configuration. Each power stage is supplied by a variable DC source. In the control circuit, an eight-bit microcontroller is employed to generate the necessary gate-drive signals. A set of switching angles for the entire range of modulation indices is calculated off-line, and is stored in the program memory of the microcontroller. An analog-to-digital converter is used to convert the analog modulation index command to the digital domain for the controller. Figure 6-8 shows simulation and experimental results of phase voltage, line voltage and load current with modulation indices of 1.0, 0.85, 0.4 and 0.1. The experimental line-voltage spectra in dB are also presented in Figure 6-9. As expected, the results show that the fifth and seventh harmonics of the line voltage are of very small magnitudes. Because of the 120° phase shifts among phase voltages, all triplen harmonics in the line voltages are also very small. The experimental results closely match those obtained through calculation and simulation.

Due to limited computational capability and control resolution, the experimental output quality is not as good as expected, especially at low modulation indices. It should be noted that

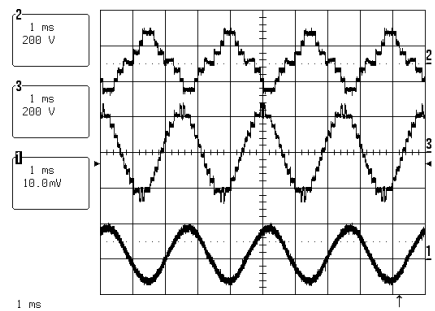
the number of levels is actually reduced when the modulation is less than 0.5. This result agrees with the initial analysis in which the convergence failed at $M = 0.5$. At $M = 0.4$, the seven-level waveform becomes five levels, and at $M = 0.1$, it becomes three levels.



$$M = 1.0, \alpha_1 = 11.68^\circ, \alpha_2 = 31.18^\circ, \alpha_3 = 58.58^\circ$$



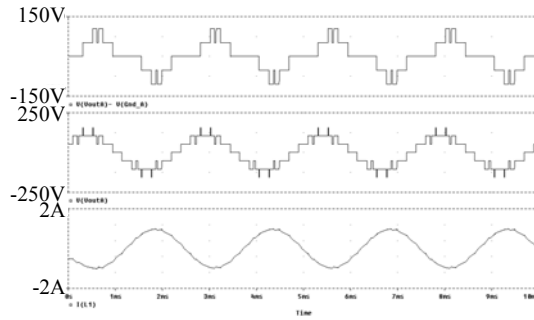
$$M = 0.85, \alpha_1 = 22.77^\circ, \alpha_2 = 49.38^\circ, \alpha_3 = 64.57^\circ$$



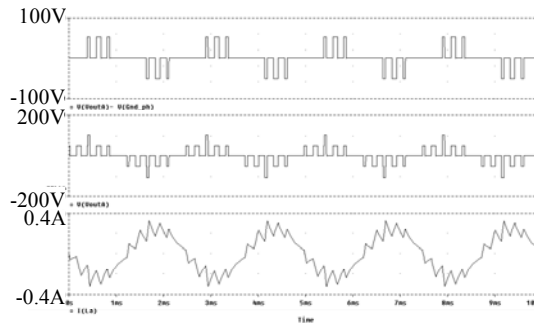
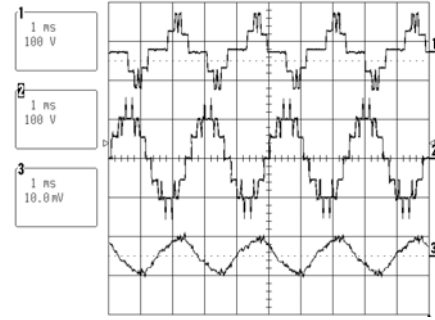
(a)

(b)

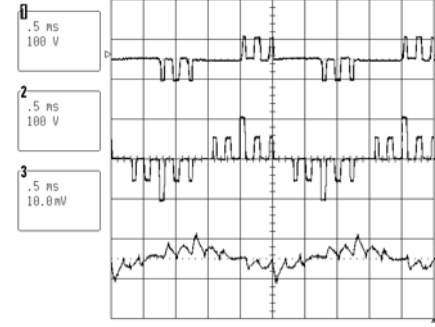
Figure 6-8. The waveforms of phase voltage, line voltage and load current: (a) simulation results and (b) experimental results.



$$M = 0.4, \alpha_1 = 44.17^\circ, \alpha_2 = 74.33^\circ, \alpha_3 = 87.40^\circ$$



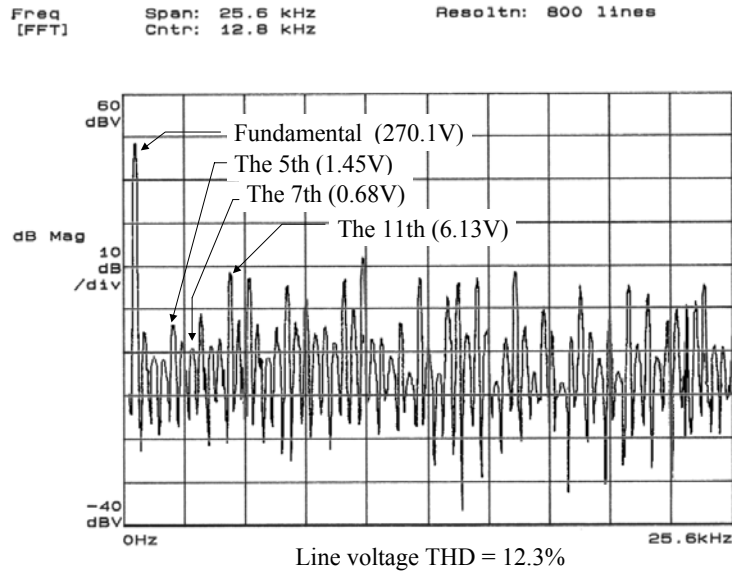
$$M = 0.1, \alpha_1 = 55.85^\circ, \alpha_2 = 63.43^\circ, \alpha_3 = 83.02^\circ$$



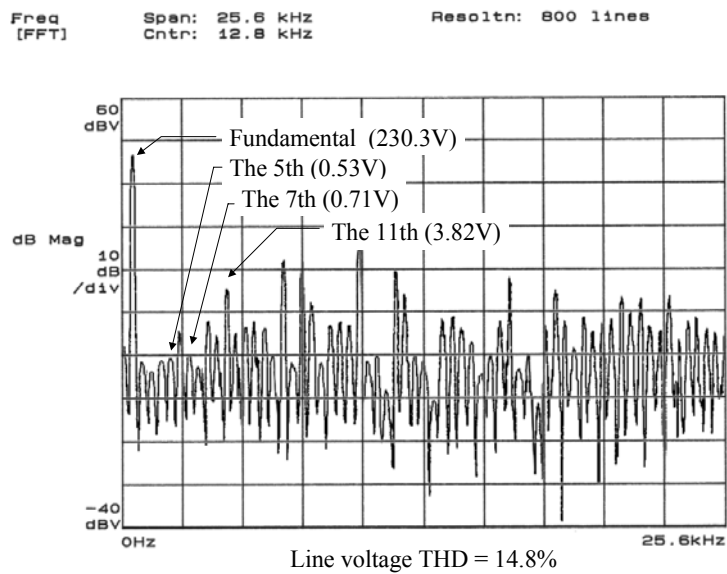
(a)

(b)

Figure 6-8. (cont.) The waveforms of phase voltage, line voltage and load current: (a) simulation results and (b) experimental results.

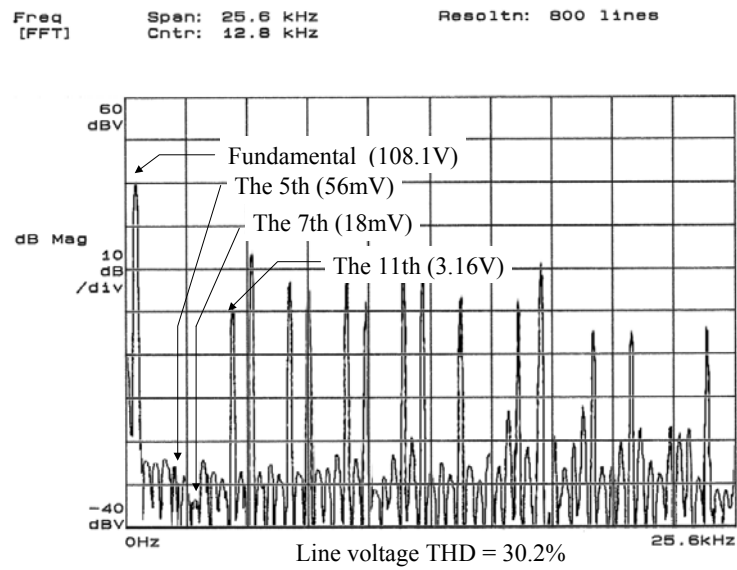


(a)

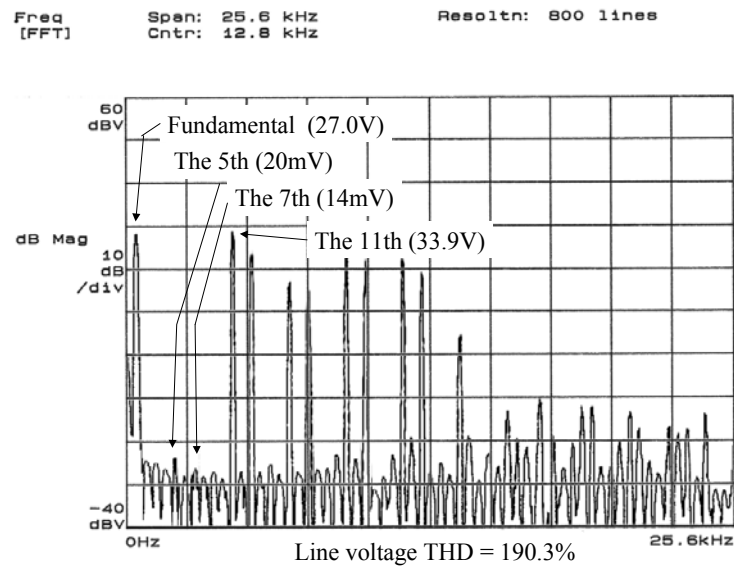


(b)

Figure 6-9. Measured line-voltage spectra: (a) $M = 1.0$, and (b) $M = 0.85$.



(c)



(d)

Figure 6-9. (Cont.) Measured line-voltage spectra: (c) $M = 0.4$, and (d) $M = 0.1$.

6.2 A Novel Cascaded-Multilevel Converter with Minimum Number of Separated DC Sources

Compared to its counterparts, the CMC with separated DC sources has been shown to have many advantages, particularly in terms of its modularized circuit layout and packaging. This confers feasibility to the CMC for manufacturing and flexibility in the sense of power expansion. The separated-DC-source converter, however, requires many isolated DC voltage sources. The total number of DC sources utilized in the cascaded converter topology is equal to the product of voltage levels and the number of phases of the converter. A seven-level, three-phase cascaded converter for reactive power compensation applications, for example, requires nine separated DC capacitors, while only five capacitors are required in the neutral-point-clamped topology. In addition, for motor-drive applications, each DC source must be controlled with respect to motor speed in order to achieve constant V/f control. A constant flux control scheme can then be realized, but this makes the control method much more complex.

As a result, an improved cascaded converter is proposed to minimize the number of separated DC sources, as well as to maintain good system performances and output quality. By using the proposed method, the required DC sources are only dependent on the number of voltage levels, and are independent of the number of phases in the converter. By sharing the same DC voltage sources, the synthesized voltage can be simply balanced. To reduce its THD, the output waveforms are synthesized by a PWM technique--the so-called selected harmonic-elimination PWM (SHE-PWM). To verify the proposed technique, an induction motor-drive system is used as an example. According to the simulation results obtained for the proposed drive system, its speed response and the quality of its output waveforms are comparable to those of a conventional CMC with the same PWM technique, which is SHE-PWM in this study.

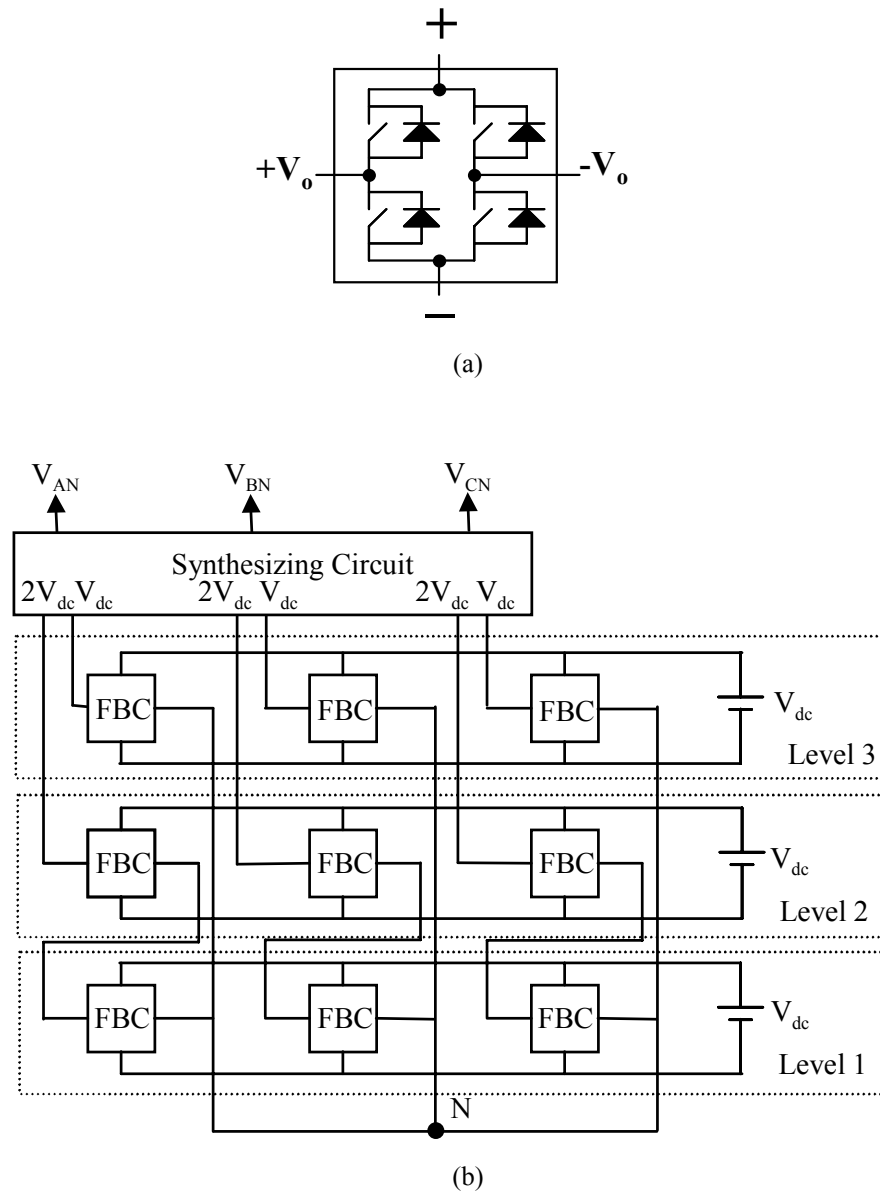


Figure 6-10. Proposed cascaded-multilevel converter with minimum number of isolated DC sources: (a) a full-bridge cell (FBC), (b) circuit diagram and (c) output waveform.

I. Principles of The Proposed Cascaded-Multilevel Converters

The basic circuit of the proposed converter is shown in Figure 6-10. Figure 6-10(a) shows the schematic of an H-bridge converter, which is a basic component in the converter and is defined as a full-bridge cell (FBC). Based on the switch combinations of each FBC, three output-voltage

levels at $+V_0$ with respect to $-V_0$ and vice versa can be synthesized, i.e., $+V_{dc}$, 0 and $-V_{dc}$. The proposed three-phase multilevel converter shown in Figure 6-10(b) consists of nine FBCs, three DC sources, and a synthesizing circuit. The FBCs in levels 1 and 2 are cascaded to generate a three-phase output voltage of $\pm 2V_{dc}$, while the FBCs in level 3, which is independent from levels 1 and 2, are used to generate $\pm V_{dc}$ three-phase output voltages. To clearly explain how the proposed converter works, the FBCs in level 1 are used as an example. If one of the FBCs switches, the others, which share the same DC voltage, must keep floating or use the same switching patterns. Otherwise, a short-circuit of the DC sources or shoot-through will be introduced. By applying this principle, a possible synthesized phase-voltage waveform of the proposed converter is thus illustrated in Figure 6-11. To generate three-phase waveforms, one cycle of the voltage waveform is equally divided into six parts. Each part, therefore, has a width of 60° . In general, the zero-sequence voltage of the system should be maintained at zero at all times. The waveform shown in Figure 6-11 indicates that the summation of the three voltages in each part is zero.

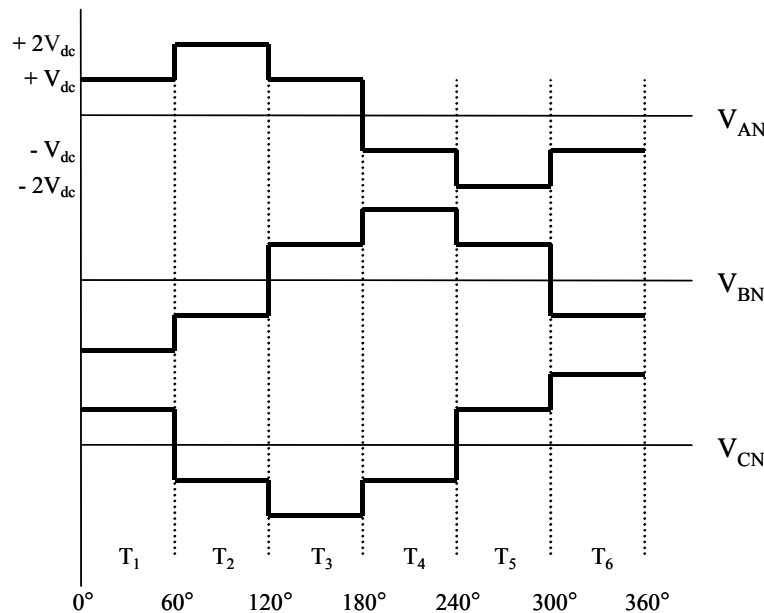


Figure 6-11. Output waveform of the proposed cascaded-multilevel converter with minimum number of isolated DC sources.

A synthesizing circuit is designed to select the output voltage of the converter from either $\pm 2V_{dc}$ or $\pm V_{dc}$. Figure 6-12(a) shows the basic structure of the synthesizing circuit. By properly selecting two of the six switches, the output voltage can be synthesized. For example, if switches S_3 and S_4 are turned on, the voltage $+2V_{dc}$ is connected to the motor, while the voltage of the motor becomes $+V_{dc}$ when switches S_3 and S_5 are turned on. Given the possible switch combinations, the output voltage can be either $\pm 2V_{dc}$ or $\pm V_{dc}$. This study proposes two practical methods for realizing the required synthesizing circuit. The circuit of method 1 is shown in Figure 6-12(b). By using diodes and IGBTs, the function of the synthesizing circuit can be realized. Figure 6-12(c) shows the circuit for method 2, which employs bi-directional AC switches (BSs). Each BS can be realized by using one of the following: a TRIAC, two parallel GTOs, or two parallel SCRs. The snubber circuits are then required to absorb the spikes when the switches turn on or off. Compared with method 1, method 2 is simpler and needs fewer devices; therefore, the topology in Figure 6-12(c) will be used as the simulated synthesizing circuit throughout this study.

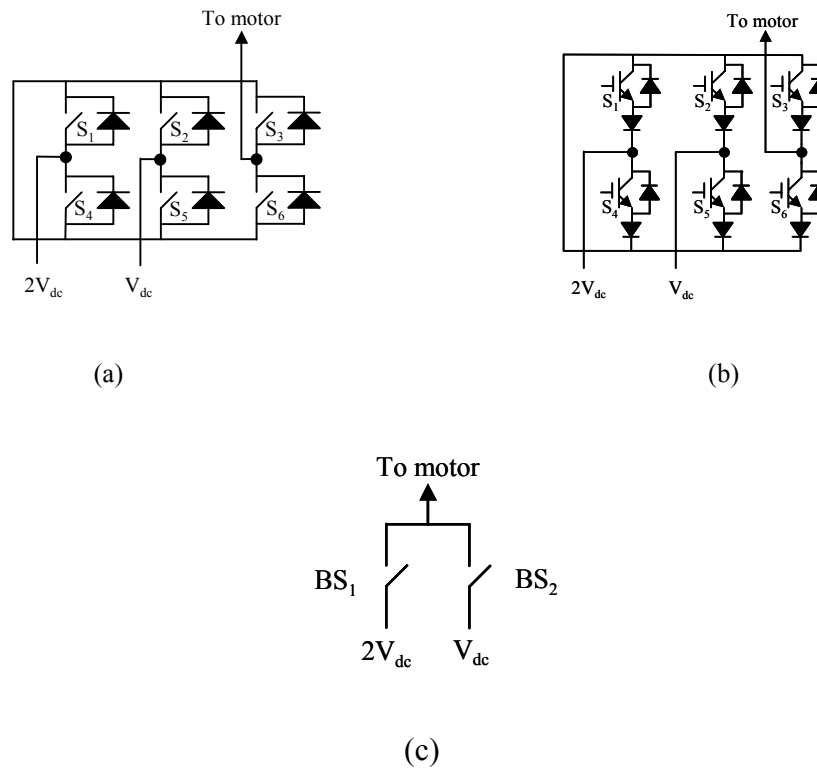


Figure 6-12. Synthesizing circuit: (a) basic circuit, (b) method 1 and (c) method 2.

II. Harmonic Component Elimination

Due to the line-frequency PWM technique shown in Figure 6-11, the THD for this kind of waveform is considered unacceptable. A simple selective harmonic-elimination method is, therefore, presented to improve the waveform quality. The idea is to get rid of low-order harmonic components in the waveforms. The output voltage shown in Figure 6-11 is associated with significant non-triplen odd harmonics such as the fifth, seventh, eleventh, and so on. Generally, the lowest surplus harmonics, whose magnitudes are relatively higher than those of higher orders, are selected for elimination. To remove the lower two harmonics, for example, the phase voltage must add four notches per cycle, as illustrated in Figure 6-13. By applying the Fourier series, the Fourier coefficients of the waveform can be determined, and are given as follows:

$$\begin{aligned} a_n &= \frac{4}{\pi} \int_0^{\frac{\pi}{2}} v(\theta) \sin(n\theta) d\theta, \text{ and} \\ &= \frac{4V_{dc}}{n\pi} [1 - \cos(n\alpha_1) + \cos(n\frac{\pi}{3}) + \cos(n\alpha_2) - 2\cos(n\frac{\pi}{2})]; \end{aligned}$$

Equation 6-15

$$b_n = \frac{4}{\pi} \int_0^{\frac{\pi}{2}} v(\theta) \cos(n\theta) d\theta = 0.$$

Equation 6-16

From Equation 6-15, by replacing n with an even integer, the coefficient a_n becomes zero. The even-harmonic components thus do not exist in the waveform. In other words, only odd harmonics distort the waveform. For an odd n , the coefficient a_n is a function of the switch angles α_1 and α_2 . Because of their Y-connection characteristic, the triplen harmonics are automatically cancelled out, and do not appear in the line-to-line voltages. The most significant low-order harmonics thus turn out to be the fifth and seventh harmonics, which can be eliminated from the synthesized waveform by applying the appropriate switching angles α_1 and α_2 . From Equation 6-15, the amplitude of the fifth and seventh harmonics can be written as follows:

$$a_5 = \frac{4V_{dc}}{5\pi} [1.5 - \cos(5\alpha_1) + \cos(5\alpha_2)], \text{ and}$$

Equation 6-17

$$a_7 = \frac{4V_{dc}}{7\pi} [1.5 - \cos(7\alpha_1) + \cos(7\alpha_2)].$$

Equation 6-18

By setting to zero the a_5 and the a_7 in Equation 6-17 and Equation 6-18, respectively, and using the numerical method, α_1 and α_2 are calculated to be 8.286° and 27.722° , respectively. With these two switching angles, the fifth and seventh harmonics of the waveform shown in Figure 6-13 are removed. To verify the calculated switching angles, the proposed PWM technique is simulated in Pspice software. The simulation results of the corresponding waveform are shown in Figure 6-14. The phase and line-to-line voltages are illustrated in Figure 6-5(a). To show the harmonic components associated with the output-voltage waveform, the spectrum of the line-to-line voltage is calculated and plotted in Figure 6-14(b). Obviously, the significant low-order harmonic in the line-to-line voltage is the eleventh, which results from the elimination of the fifth and seventh harmonics.

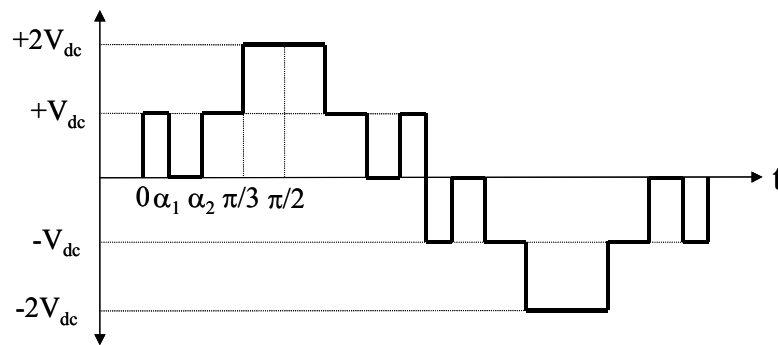
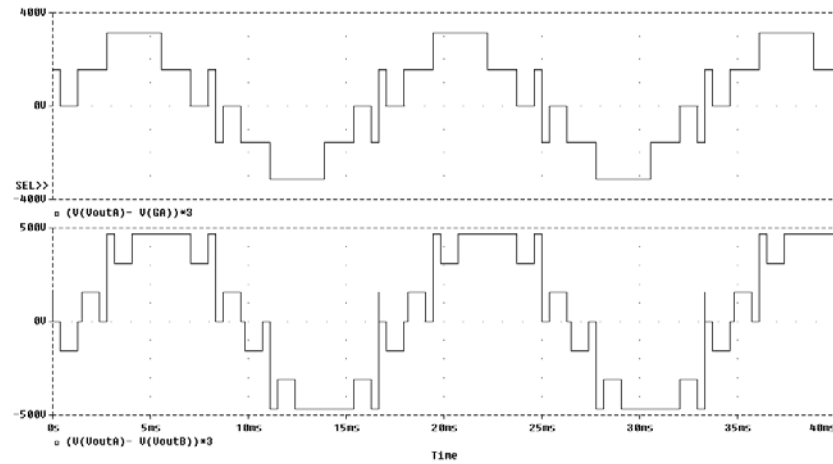


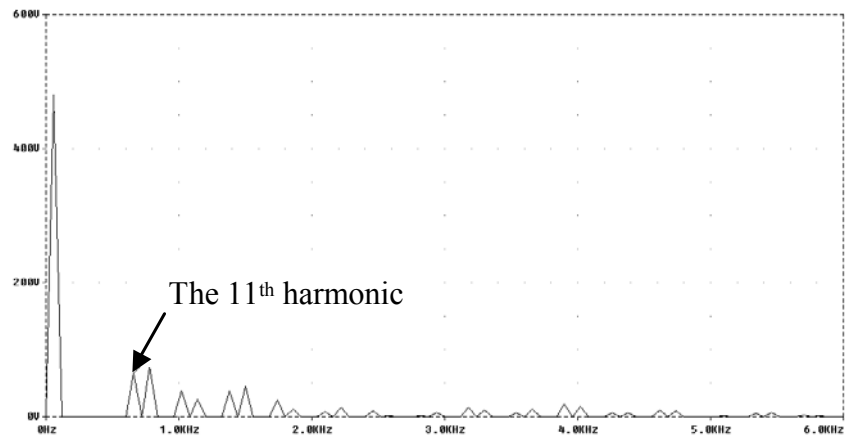
Figure 6-13. Output-phase voltage of the proposed converter.

III. Example Induction Motor-Drive System

To show the performance of the proposed cascaded converter, an adjustable-speed induction motor drive is studied. Figure 6-15 shows the block diagram of the proposed drive system. The system is designed for a three-phase, high-power, constant-flux induction motor-drive system. The DSP is used as the main controller. The DSP reads the speed command from a user and then computes the required output voltage and frequency of the converter. Next, the DSP computes each DC voltage level and sends the gating signals to the AC/DC converter to obtain the required DC voltages, and to the converter to generate the required AC output waveforms. The transformers are used to isolate the DC sources. By selecting the Y- Δ configurations and the phase-shifted angles among the three transformers, the input-current harmonic distortion of the three-phase AC source can be effectively reduced. Phase-controlled rectifiers are used as AC/DC converters. Six SCRs are, therefore, required for each converter. By adjusting the firing angles of the SCRs, three adjustable DC voltages can be obtained. The proposed converter synthesizes a three-phase multilevel waveform from the calculated switching angles. The converter thus generates the variable-amplitude, variable-frequency voltage waveforms to drive the induction motor. A constant flux control scheme is, therefore, achieved.



(a)



(b)

Figure 6-14. Simulation results of: (a) phase voltage and line-to-line voltage and (b) the line-to-line voltage spectrum of the converter.

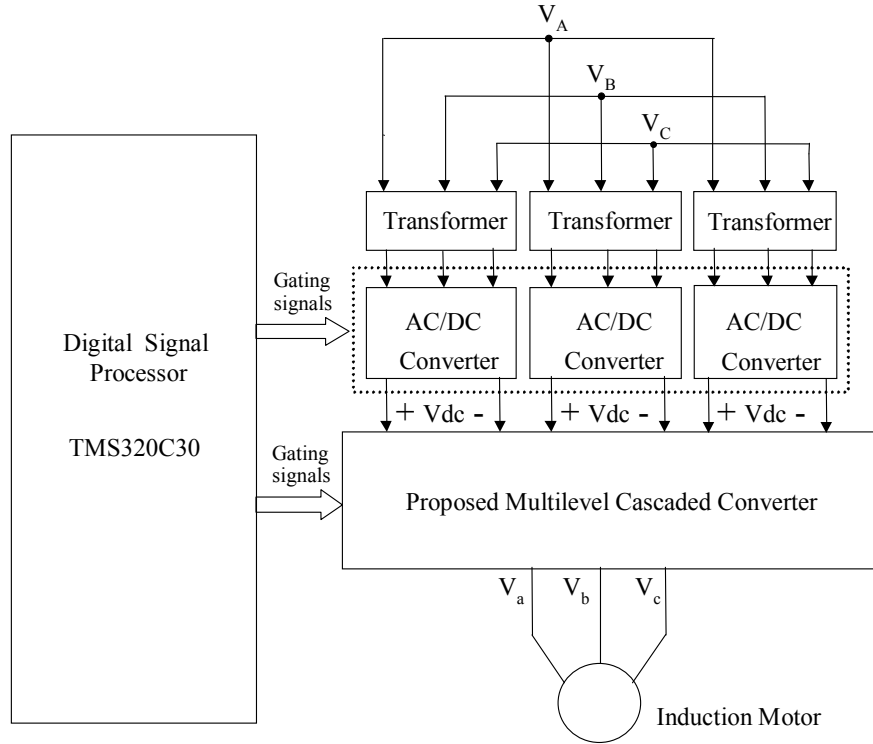
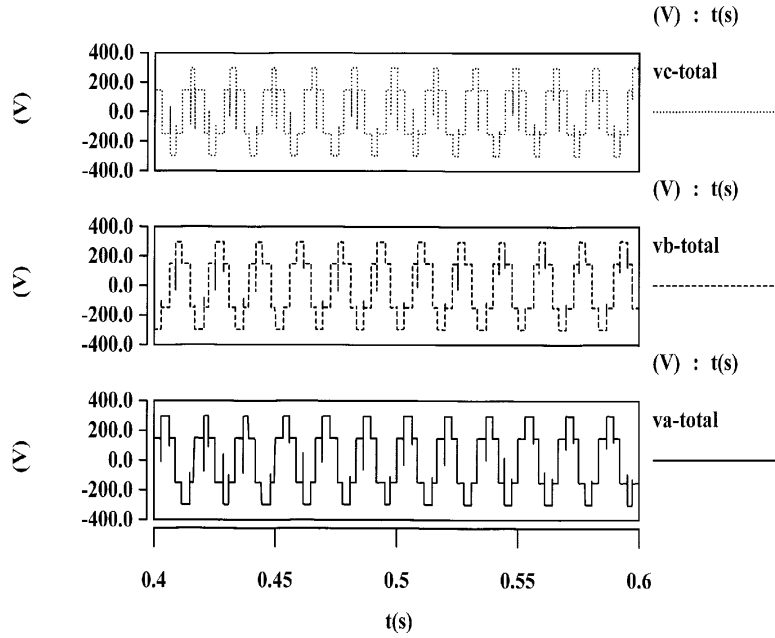


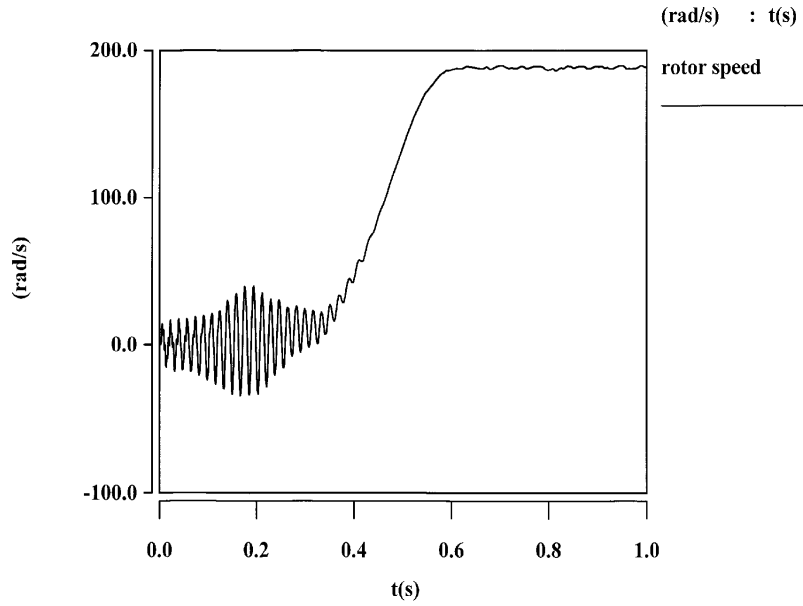
Figure 6-15. Proposed adjustable-speed induction motor-drive system.

IV. Simulation Results

To verify the theoretical analysis, a complete system is simulated using the SABER program, and the simulation results are presented in Figure 6-16 through Figure 6-18. Figure 6-16(a) shows the simulation results of the three-phase output voltages of the proposed converter without additional notches. The open-looped speed response of the motor driven by the proposed converter is shown in Figure 6-16(b). In steady state, a small-speed ripple is introduced due to the harmonics of the output voltage, specifically the fifth and seventh harmonics.



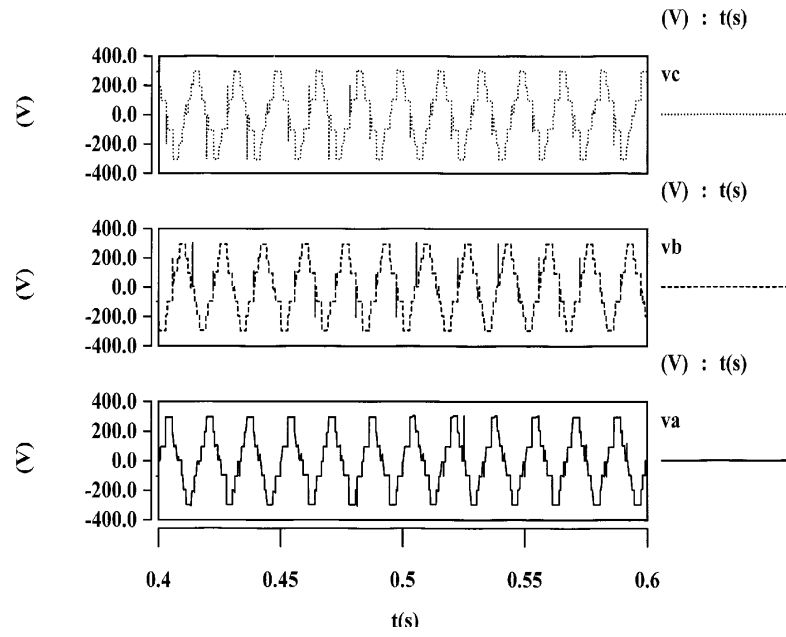
(a)



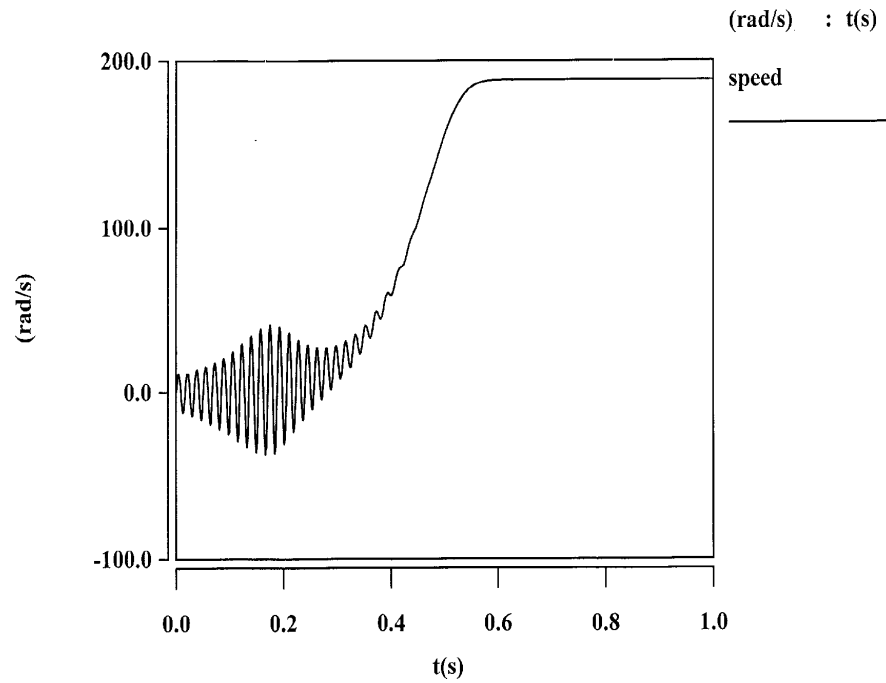
(b)

Figure 6-16. Simulation results of the proposed drive system without notched PWM: (a) three-phase voltage waveforms and (b) motor speed response.

Figure 6-17(a) shows the three-phase voltages of a conventional seven-level cascaded converter with optimized harmonic reduction. The peak-to-peak voltage of the conventional converter is kept at the same value as that of the proposed converter. Figure 6-17(b) shows the speed response of the motor driven by the conventional converter. By observing Figure 6-16 and Figure 6-17, we see that the conventional method with optimized harmonic reduction has better performance in the steady-state condition. During the transient, however, they are not different. As has been discussed, the speed ripple produced by the proposed converter can be improved by using the proposed harmonic-elimination method. After properly adding four notches per cycle into its voltage waveform, the proposed converter shows a better performance, as shown in Figure 6-18. The speed ripple is nearly eliminated in the steady state. In addition, Figure 6-18(b) has a speed response similar to that of Figure 6-18(b), which uses the conventional converter with the optimized harmonic-elimination method.

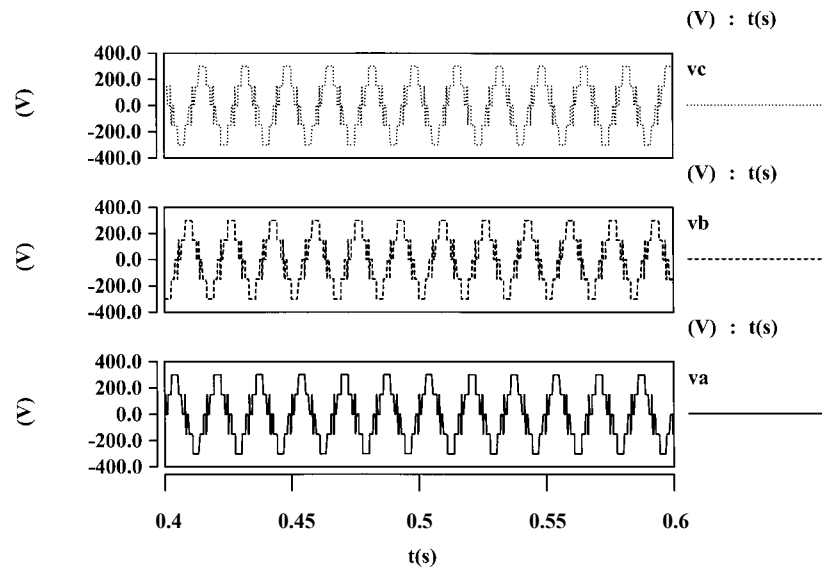


(a)

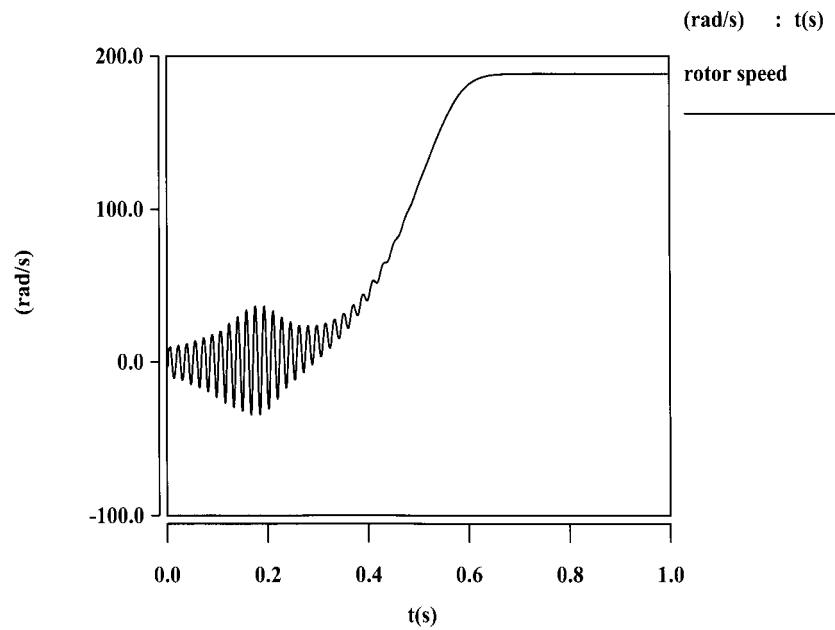


(b)

Figure 6-17. Simulation results for a conventional seven-level cascaded-based induction motor drive: (a) phase voltage and (b) motor speed response.



(a)



(b)

Figure 6-18. Simulation results of the proposed drive with notched PWM: (a) phase voltage and (b) motor speed.

6.3 Conclusions

This chapter has presented a new modulation technique to be applied to multilevel VSCs and a new cascaded converter with a minimum number of separated DC sources. These two technologies are suitable for high-voltage, high-power applications.

The proposed modulation technique can generate output stepped waveforms with wide modulation indices, and at the same time minimizes voltage THD. For all modulation index levels, the switching devices of the main power stage switch only once per cycle, which is suitable for use with high-power semiconductor devices. The simulation and experimental results validate the theoretical analysis. A three-phase, seven-level cascaded converter prototype is used as an example. The principle developed in this chapter can be easily applied to other multilevel converter topologies and with any number of levels. For THD concerns, the proposed technique can be further extended to have more than one switching per line cycle in order to lower the THD at low modulation indices.

To synthesize three-phase, five-level voltage waveforms, only three DC sources are required in the proposed converter, whereas six DC sources are required in a conventional five-level cascaded converter. The simulation results show that the proposed method has a satisfactory performance. The proposed drive system with notches has a speed response similar to that of the conventional drive system with optimized harmonic elimination. With simplicity and expandability as well as low switching frequency, the proposed technique using a cascaded converter with a minimum number of DC sources can be effectively applied in high-power drive systems.

Chapter 7 CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

Among FACTS controllers, the shunt controllers have shown feasibility in terms of cost-effectiveness in a wide range of problem-solving abilities from transmission to distribution levels. For decades, it has been recognized that the transmittable power flowing through transmission lines could be increased without additional transmission infrastructures, and the voltage profile along the transmission line could be controlled by an appropriate amount of compensated reactive power. In addition, the shunt controller can improve transient stability and can damp power oscillation during a post-fault event. Using a high-speed power converter, the shunt controller can further alleviate or even eliminate the flicker problem caused by electrical arc furnaces.

Employing turn-off-capable semiconductor devices, switching power converters have been able to operate at higher switching frequencies and to provide a faster response. This makes the VSC an important part in the FACTS controllers. The STATCOM is the first power-converter-based shunt-connected controller. Instead of directly deriving reactive power from the energy-storage components, the STATCOM basically circulates power with the connected network. Therefore, the reactive components used in the STATCOM, can be much smaller than those in the SVC.

For transmission and distribution voltage levels, the multilevel VSC offers various advantages over its counterparts. As discussed in Chapter 2, among the mature multilevel converter topologies, the CMC is the most promising alternative for the STATCOM application. To achieve the same number of output voltage levels, the CMC requires the least total number of components. With its modular structure, the CMC can flexibly expand the output power capability that corresponds to the requirements of the connected power system networks. Additionally, its modularity is favorable to manufacturing. Moreover, redundancy can be easily applied in the CMC to enhance reliability for the entire system. A complete control system for STATCOM applications basically consists of two main parts: external and internal controls.

Generally, the external control depends on the characteristics of the power system network to which the STATCOM is connected. In contrast, the internal control primarily depends on the VSC topologies. This dissertation mainly focused on the internal control for the STATCOM utilizing the CMC. Three major challenges, which were not yet fully discovered in the past, have made this research area very attractive.

First, a well-defined model is a key to improvements in the effectiveness and stability of feedback control and for system parameter optimizations. Numerous parameters that need control mean that CMC-based STATCOM modeling is not trivial. None of the previous works has shown a valid model. The feedback-control parameters were thus randomly selected. Because the STATCOM deals with power control, two power components--real and reactive--must be controlled separately. Moreover, to maximize the stability of the system operation, a spontaneous response is very desirable. The second challenge is thus how to achieve a control technique that has the power-decoupling capability in order to maximize the system performance and to confirm the control stability. To be able to operate in a high-voltage application, an excessive number of DC capacitors are utilized in a CMC-based STATCOM. Voltages across these DC links must be balanced to avoid over-voltage on any particular link. Not only do these unbalanced DC voltages introduce voltage stress on the semiconductor switches, but they also lower the quality of the synthesized output waveforms of the converter. Consequently, how to maintain and balance these many DC links with a straightforward and cost-effective technique becomes the third challenge for this topology.

To further improve the performance and effectiveness of the CMC-based STATCOM system, the following five contributions have been proposed: optimized design for the CMC-based STATCOM power stage and its passive components, modeling of the CMC for reactive power compensation, a decoupling power control method, a DC-link balancing technique, and improvement in the CMCs.

The concept of the high-power electronic building block, which becomes a basic unit of the CMC topology, was presented in Chapter 3. The configuration and structure of the high-voltage ETO-based HBBB have been proposed. Because of their identical layouts, the HBBBs are simple to manufacture and very cost-effective. Their modularity feature makes the entire system

design and planning processes flexible in terms of power capability. By connecting these modules in series, the CMC topology that is used as the power converter in the STATCOM application can be readily implemented. To maximize the output power and to reduce the electrical and thermal stresses on the ETOs of the HBBBs, the snubber components have been optimally selected and implemented. The key performances of the HBBB were experimentally confirmed. The high-frequency, high-power operation of the HBBB is clearly demonstrated. Besides the key components, such as the HBBB power stage and its snubber circuit, the passive components used in the CMC-based STATCOM also dictate the performance of the entire system. The reactive component requirement criteria for the reactive power compensations have been investigated. Two main passive components that are included in this study are the DC capacitors and the coupling inductors. For a given output current and operating voltage, the size of the DC capacitor utilized in an HBBB for the CMC used in reactive power compensation should be selected based on the following considerations. One factor limiting the minimum capacitance is over-voltage, which is a function of the voltage ripple and the transient voltage overshoot. In the H-bridge VSC, the voltage ripple is directly proportional to the maximum modulation index of the HBBB. In contrast, the cost is the only factor that limits the maximum size of the capacitor. In addition, the capacitor size does not depend on the switching frequencies; a higher switching frequency does not help to reduce the size of the DC capacitor. In addition, the output-current THD does not significantly improve with larger DC capacitors. For a given output current and operating voltage, the size of the coupling inductor is minimally limited by the output-current harmonic distortions, and the maximum inductance is limited by the operation range of the converter (reactive power loss) and, of course, by the cost. This means that, besides the cost, if the coupling inductor is too big, the converter will not have sufficient windows of operation to supply the reactive power, particularly in the capacitive mode. Moreover, the coupling inductance does not influence the dynamic response of the systems, because the transfer functions of the current loop gain can be shaped by an appropriate compensator.

The proposed model, which can be utilized in all applications, is generally suitable for the CMC topology with any number of voltage levels. An accurate and simple modeling technique for the CMC-based STATCOM in both stationary (ABC coordinates) and synchronous (DQ0

coordinates) frames has been proposed. Due to the excessive number of controlled variables in the cascaded-multilevel VSCs, an effective simplification, based on the practical assumptions and the proposed variable definitions, was proposed. All key system transfer functions, which will be used in the control design process, have been derived. Based on the derived transfer functions, basic electrical characteristics of the CMC-based STATCOM have been investigated, and the relationship among system parameters has been revealed. In addition, the DQ0 model of the CMC-based STATCOM enhances the feasibility of the proposed decoupling power control technique in which real and reactive power channels can be controlled separately.

Based on the proposed STATCOM model, the feedback-control technique, called the decoupling power control, was first presented for the three-level cascaded-based STATCOM, and its performance and stability were verified by both computer simulations and experiments. This control technique allows reactive and real power to be independently controlled. The experimental results were very consistent with the simulation results. Moreover, the results demonstrated the accuracy of the model and the superior performance of the control technique. A new multilevel-voltage modulation technique, named the cascaded PWM, was proposed to overcome the imbalance problem among the DC-capacitor voltages in the CMC-based STATCOM. The cascaded PWM can be directly realized by the FPGA, which minimizes the complexity of the main control loop and significantly improves the reliability of the entire control system. The seven-level cascaded-based STATCOM system was selected as an example in order to validate the proposed control system. The performance of the feedback control, which is derived from that used in the three-level cascaded-based STATCOM, is verified by both simulations and experiments. The results showed the superior performance and stability of the designed controller, which combines the decoupling power control and the cascaded PWM.

By utilizing the cascaded PWM, all DC-capacitor voltages can be balanced in all operation conditions. Based on the philosophy behind the proposed technique, CMCs with any number of voltage levels can be modeled as three-level cascaded converters. This dramatically simplifies the entire control design process. This technique is one of the major contributions in this dissertation.

Finally, a new modulation technique to be applied to multilevel VSCs and a new cascaded converter with a minimum number of separated DC sources were proposed. These two technologies are suitable for high-voltage, high-power applications. The proposed modulation technique can generate output stepped waveforms with wide modulation indices, and at the same time minimizes voltage THD. For all modulation index levels, the switching devices of the main power stage switch only once per cycle, which is suitable for use with high-power semiconductor devices. The simulation and experimental results validate the theoretical analysis. A three-phase, seven-level cascaded converter prototype is used as an example. The developed principle can be easily applied to other multilevel converter topologies and with any number of levels. For THD concerns, the proposed technique can be further extended to have more than one switching per line cycle in order to lower the THD at low modulation indices.

7.2 Future Work

Although this dissertation has covered most of the interesting issues and challenges of the CMC-based STATCOM, additional work has been left for future research. The first part is the coordination between the proposed internal and external controls. From the standpoint of external control design, the internal control, which is the combination of the decoupling power control technique and the cascaded PWM, can be modeled as a black box in which high-quality output voltage-current waveforms and relatively fast dynamic responses are embedded. With an effective external control design, a high-performance, stable, reliable CMC-based STATCOM system can be completely achieved.

The second part is the fault-protection study for the CMC-based STATCOM. Due to the excessive number of semiconductor devices and passive components, how to design a fault-protection scheme to enhance the ride-through capability in various fault scenarios remains as an important challenge.

Finally, the last part is the redundancy of the CMC-based STATCOM system. Due to the identical HBBBs used in the CMC, the N+1 rule may be applied, where N is the number of HBBBs per phase. The seven-level cascaded converter, for example, can have four HBBBs

instead of three. In case of a semiconductor failure in one HBBB in the same phase leg, the rest of the HBBBs can still generate a normal output voltage.

APPENDIX A: PARK'S TRANSFORMATION MATRIX DERIVATION

The purpose of the Park's transformation is to transfer a parameter in ABC coordinates to a new coordinated called DQ0, where D stands by direct, Q stands by quadrature, and 0 stands by zero. The advantage of this transformation technique is that, under a balance three-phase system, a three-phase AC parameter in ABC coordinates can be represented by a two-phase DC parameter in DQ0. Consequently, the classical control technique, which is valid only in DC space, can be simply applied in the AC environment.

A coordinate in the ABC coordinates can be represented by a vector, whose direction points from the origin to its coordinate. The output current of the STATCOM, for example, can be represented as a following 3x1 matrix:

$$\vec{i}_{abc}(t) = \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix},$$

Equation A - 1

where $i_a(t)$, $i_b(t)$ and $i_c(t)$ are phase A, phase B and phase C output currents of a STATCOM, respectively.

Figure A - 1 shows the location of vector $\vec{i}_{abc}$ in the ABC coordinates.

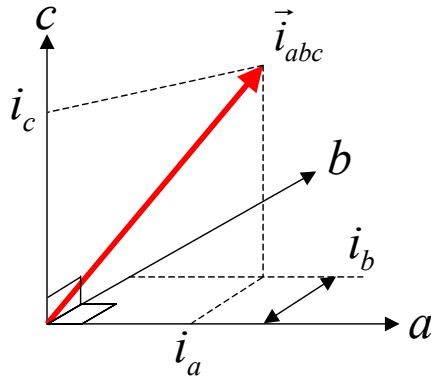


Figure A - 1. Vector $\vec{i}_{abc}$ represents an instantaneous output current of a STATCOM.

The first step of the Park's transformation derivation begins with defining an intermediate coordinates called $\alpha\beta\gamma$. The $\alpha\beta\gamma$ coordinates locate in the ABC coordinates, as shown in Figure A - 2. The direction of the γ axis is in line with the vector (1,1,1) in the ABC coordinates.

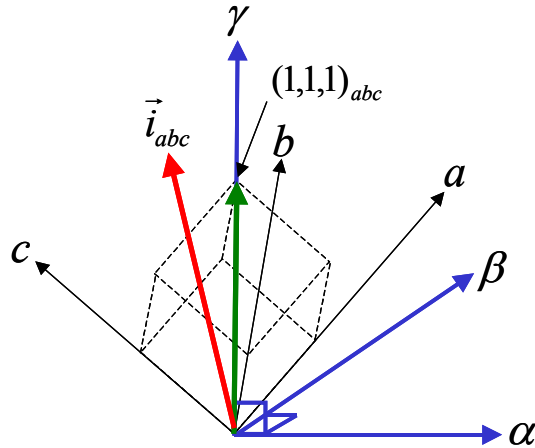


Figure A - 2. The $\alpha\beta\gamma$ coordinates locate in the ABC coordinates.

A vector in the ABC coordinates can be represented in the $\alpha\beta\gamma$ coordinates by applying the following equations:

$$\vec{i}_{\alpha\beta\gamma}(t) = \vec{T}_{\alpha\beta\gamma/abc} \cdot \vec{i}_{abc}(t),$$

Equation A - 2

where

$$\vec{T}_{\alpha\beta\gamma/abc} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

After the transformation, the component in γ is always zero in the case of balanced-three-phase system. In other word, current vector $\vec{i}_{\alpha\beta\gamma}(t)$ is on the $\alpha\beta$ plane and rotates around the γ axis. As a result, a balanced-three-phase AC vector in the ABC coordinates can be represented by a two-phase AC vector in the $\alpha\beta\gamma$ coordinates. If the $\alpha\beta$ plane synchronously rotates along with vector $\vec{i}_{\alpha\beta\gamma}(t)$, $i_\alpha(t)$ and $i_\beta(t)$ then becomes constant. With this principle, the DQ0 coordinates is created. Figure A - 3 illustrates vector $\vec{i}_{abc}$ in the DQ0 and $\alpha\beta\gamma$ coordinates. The D and Q axis rotates with the angular velocity of ω or $2\pi f$, f is the line frequency. Based on this approach, the Park's transformation matrix, $\vec{T}_{dq0/abc}$, is then derived and used as an operator to directly transform a vector from the ABC coordinates to the DQ0 coordinates. The transformation is shown in Equation A - 3, and the Park's transformation matrix is shown in Equation A - 4.

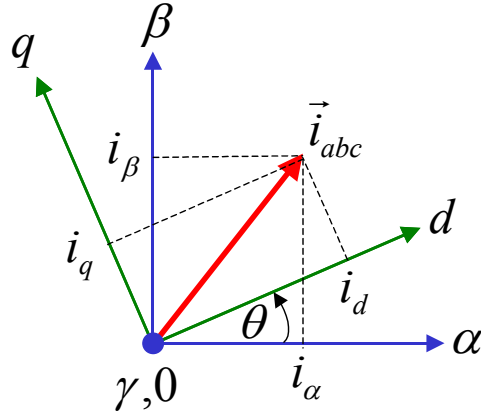


Figure A - 3. The rotating DQ0 coordinates with respect to the $\alpha\beta\gamma$ coordinates.

$$\vec{i}_{dq0} = \vec{T}_{dq0/abc} \cdot \vec{i}_{abc}.$$

Equation A - 3

$$\vec{T}_{dq0/abc} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix},$$

Equation A - 4

where $\theta = \int_0^t \omega(\tau) d\tau + \theta(0).$

The inverse Park's transformation matrix, as shown in Equation A - 5, is used to convert a vector in the DQ0 coordinates back to the ABC coordinates.

$$\vec{i}_{abc} = \vec{T}_{dq0/abc}^{-1} \cdot \vec{i}_{dq0}.$$

Equation A - 5

APPENDIX B: IGBT-CMC-BASED STATCOM TESTBED

The low-power IGBT-CMC-based STATCOM testbed are used to verify the designed closed-loop control algorithm, to evaluate the basic functions of the controller circuit, to investigate effects of other factors that were not taken into account during the system modeling and design stages, and to study on system fault protections in both controller circuit and power stages. Additionally, the testbed is designed to be flexible; therefore, it can be configured for other types of FACTS controllers, active power filters, and adjust speed motor drives utilizing the cascaded-multilevel VSCs.

Basically, the testbed, as shown in Figure B - 1, consists of three main parts: the electrical networks, the CMC, and the DSP-based controller. The electrical network, which is composed of the electrical sources, the autotransformers and the passive or non-linear loads, emulates scaled-down electrical characteristics of the power system networks in which the CMC is connected.

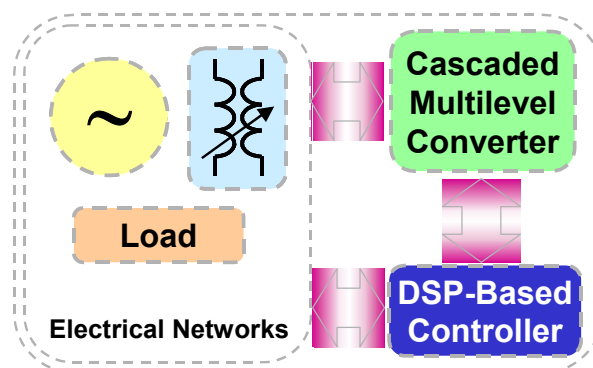


Figure B - 1. Three basic components in the CMC testbed.

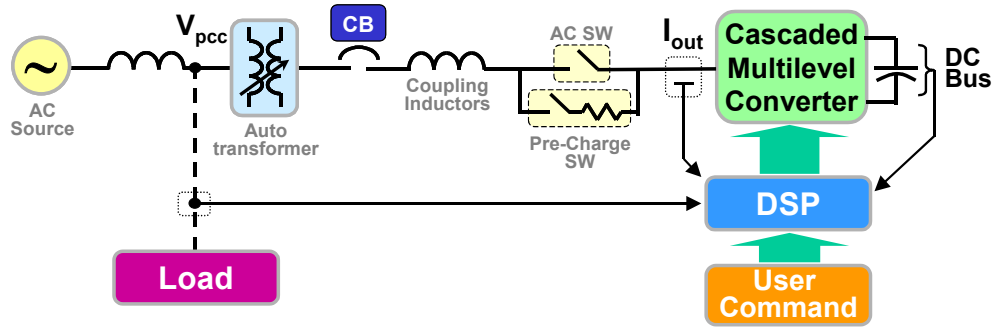


Figure B - 2. The testbed is configured as a STATCOM system.

As used in this dissertation, the testbed is configured as a STATCOM system, as shown in Figure B - 2. A 208V, three-phase voltage source is stepped down to a given voltage by the autotransformer. The IGBT-based CMC is connected to the secondary side of the autotransformer through the manual circuit breaker (CB) and the remote AC switch. The pre-charge switch is used to provide limited current paths to the DC capacitors at the beginning of the operation. The coupling inductor of 0.5 to 2 mH per phase is used as a converter output current filter, as well as a reactive power coupler.

The CMC used in the testbed consists of several IGBT-based H-bridge converters. Figure B - 3(a) shows a block diagram of the seven-level converter, which is composed of nine H-bridge converters, whose structure are replicated those of the ETO-based HBBBs. The schematic of an IGBT-based H-bridge converter is shown in Figure B - 3(b). The specification of the H-bridge converter is listed in Table B - 1.

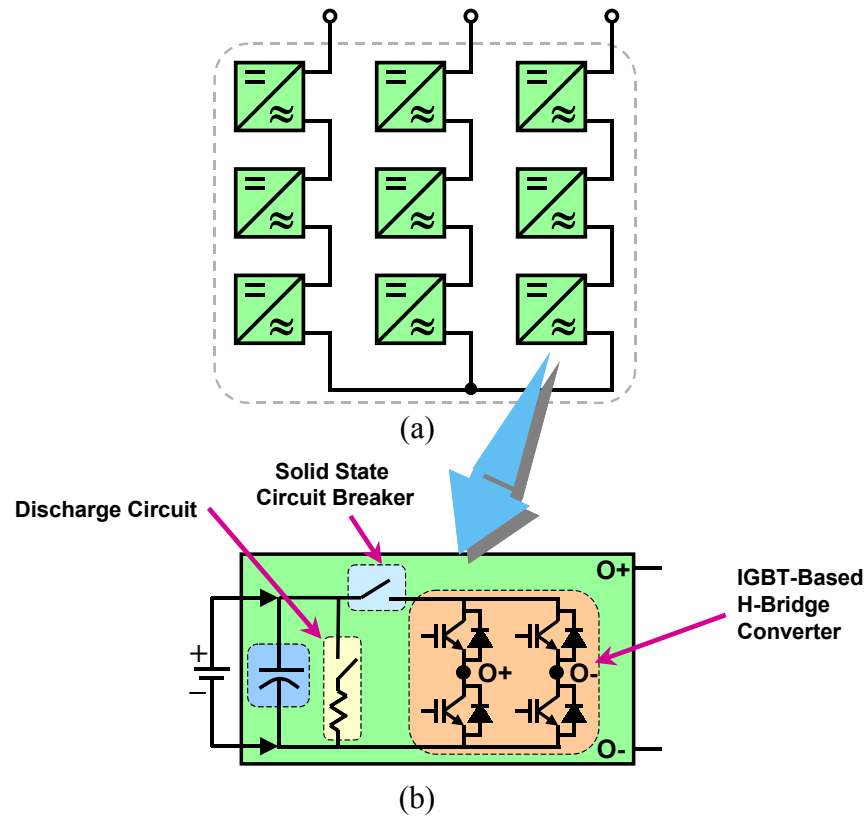


Figure B - 3. The IGBT-based CMC: (a) block diagram of the seven-level cascaded converter and (b) the schematic of the H-bridge converter.

TABLE B - 1. SPECIFICATIONS OF AN IGBT-BASED H-BRIDGE CONVERTER.

Main Switches, Circuit Breaker and Discharge Switch	HGTG30N60 IGBT with Internal Freewheeling Diodes
Maximum Output RMS Voltage (V)	300 V
Maximum RMS Output Current (A)	30 A
Operation Switching Frequency (Hz)	1-5 kHz
Gate Driver Interface	Optical
Cooling System	Convection Heat Sink

The main controller that is used in this testbed consists of a 64-bit DSP and a 50k-gate FPGA. The DSP is a floating-point and runs at 133 MHz. The main feedback control routines are

programmed in the Texas Instrument DSP format. The calculation frequencies for the main feedback control routine and the PLL are 10 kHz and 30 kHz, respectively. The FPGA, which is in the daughter board, is used to generate PWM signals and provides inputs and outputs for the DSP. Three PWM generators are programmed in the FPGA and are outputted to the FPGA via the digital channels. The measurements are acquired by ADCs and are fed into the DSP via the analog inputs of the FPGA. The specifications for both the DSP and FPGA are given in Table B - 2. The hardware prototype of the IGBT-CMC-based testbed and its components are shown in Figure B - 4.

TABLE B - 2. DSP AND FPGA SPECIFICATIONS.

DSP Evaluation Board	
DSP	133MHz, floating point TMS320C0701
Interface	PCI
Flash Memory	512 kB
FPGA Daughter Board	
FPGA	Xilinx XCV50
I/O	
Analog	16
Digital	24
Analog-to-Digital Converters	4



Figure B - 4. Pictures of the IGBT-CMC-based STATCOM hardware prototype and its components.

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