6. DC AND AC DISTRIBUTED POWER SYSTEM COMPARISON

6.1 Introduction

The last chapter established circuit topologies, bus waveform shapes, and printed-circuit board bus structures that realize a HF AC DPS suitable for computer system power architectures. Although the relative effects of varying different design parameters (e.g., the effects of the bus voltage transition times on the measured electric field) were addressed, a meaningful baseline from which to draw comparisons about the overall system performance is needed. Since the concept of an AC distributed power system was developed in order to address perceived shortcomings of a comparable DC DPS, a comparison between the two systems is in order.

Therefore, this chapter contains comparisons between the AC DPS developed in the last chapter and a DC DPS designed to identical input/output specifications. The following items are compared:

1) Efficiency.
2) Electric and magnetic radiated field characteristics.
3) Complexity, as reflected by each systems piece-parts cost.

6.1.1 Comparison methodology

Since the AC DPS designed in the last chapter is used for this comparison, the DC DPS must be designed to the same specifications in order for the comparison results to be meaningful. These specifications are given in Section 5.2.2. The test bed discussed

in Chapter 6 (Fig. 5.9), is used for both systems. Two post-regulators, each with a maximum output power of 50 W, are used in each experimental setup. Both the AC and DC DPSs use the same PFC boost converter in their front-end designs. Of course, the second-stage converter in each design is different. The power distribution bus structure is kept constant throughout the comparison's experimental portion. A 2 layer w/shield, 4 conductor structure is used. Efficiency is measured between the AC line input and the post-regulator outputs. The experimental electric field measurements use the setup discussed in Section 5.3.3 and Fig. 5.40. The setup for measurements of the magnetic field will be discussed later in the chapter.

6.2 Description of the DC Distributed Power System

Figure 6.1 shows a simplified schematic of the DC DPS used in the comparison. An active-clamp forward converter [46] regulates the 48 Vdc bus voltage off of the 380 Vdc input from the PFC boost converter. This topology is a well suited compromise between complexity and efficiency when considering applications where a maximum output power of 300 W - 400 W is required. The major components selected for the power stage design are indicated in the figure. The active-clamp forward converter's switching frequency was selected to be 150 kHz.

The converters that comprise the post-regulators in the DC system are simple resonant-reset DC/DC converters with switching frequencies of 300 kHz - identical to the AC DPS's bus frequency. The reason for using the resonant reset scheme is simplicity in the design that approaches that of the post-regulator design used in the AC DPS - no additional reset windings or circuitry is required. As a matter of fact, identical transformer designs are used in all four post-regulators, two for the AC system and two for the DC system. Since the resonant reset converters used in the DC system operate with a duty cycle of around 50 %, the center-tap in the transformer design is simply not brought out, giving the DC system's transformers half the turns ratio of the transformers

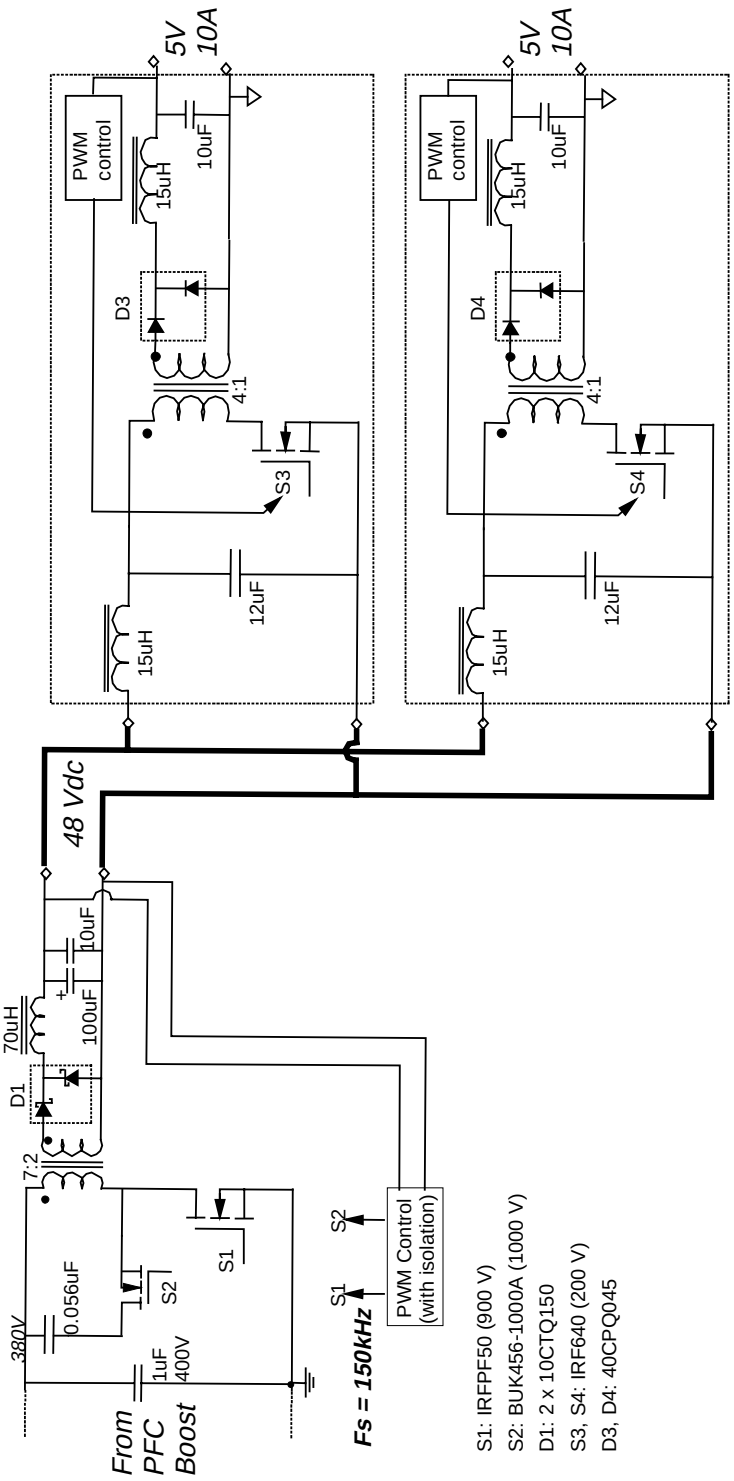


Fig. 6.1 Simplified DC DPS schematic.

used in the AC DPS post-regulators. The disadvantage of the simplicity of the resonant reset scheme is the voltage stress introduced on S3, S4, D3, and D4. For example, even with a fixed 48 Vdc input, S3 and S4 have to have a 200 V breakdown rating.

A single-section LC input filter is incorporated into each post-regulator, as shown in Fig. 6.1. The input inductor is necessary to prevent sinusoidal currents from circulating on the bus due to the FE's output voltage ripple appearing across the input capacitor of each post-regulator. Even with relatively small amplitudes of bus voltage ripple (110 mVpp with Po = 75 W for this system), depending upon the values of post-regulator input capacitance, suprisingly large bus ripple currents can result in the absence of an input inductor. Figure 6.2 shows experimental drain-to-source voltage waveforms for S1 in the FE active-clamp forward converter and for S3 in one of the two post-regulators. The switching frequencies of the front-end converter and post-regulators were not synchronized.

6.3 Comparison Results

This section presents the comparison results and provides some commentary regarding these results.

6.3.1 Efficiency

Figure 6.3 displays the overall system efficiencies with an input voltage of 110 Vac. For the AC DPS the bus voltage rise/fall times are about 215 ns, however, it was difficult to measure any efficiency differences when utilizing different transition times. This data includes losses due to control circuit bias power. As can be seen from the plot, the AC system has better efficiency than the DC system above about 12 % of full load (~ 50 W). At about 25 % of full load the AC DPS is about 6 % more efficient. The efficiency of the AC system drops off at very light loads due to increased magamp losses in the post-regulators. At lightest load the magamps block the greatest amount of volt-seconds. Due to the limitation on the number of post-regulators constructed for the

Fig. 6.2 Typical DC DPS experimental waveforms.

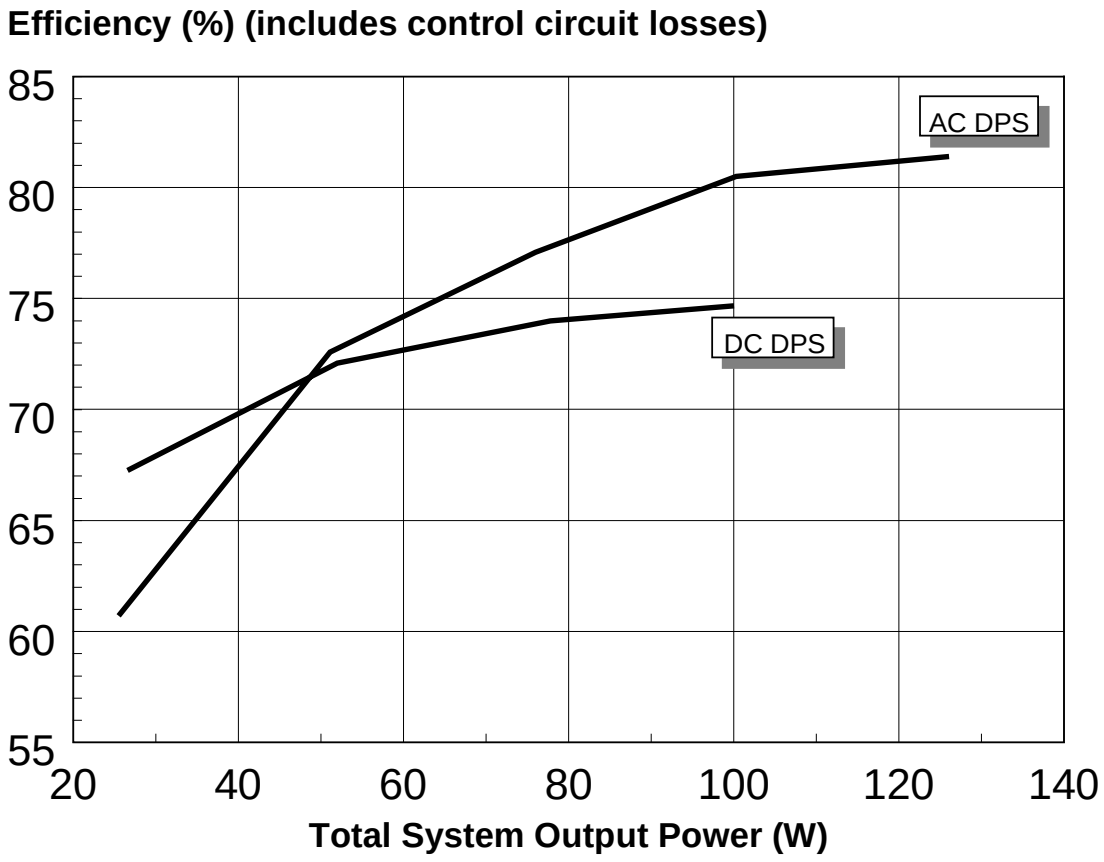


Fig. 6.3 Experimental efficiencies.

breadboarded systems, direct efficiency measurements stop at around 100 W. However, the data can be extrapolated to higher power levels by measuring the efficiency of the individual "modules" in the system and combining the results. For example, the DC system front-end's efficiency can be measured to 350 W. Also, the individual efficiencies of the DC systems' post-regulators can be measured up to their maximum output power of 50 W. The efficiency of a 350 W system could then be determined with seven post-regulators, all operating at maximum load. At 50 W power level increments, between 100 W and 350 W, the requisite number of post-regulators (all operating at their maximum load of 50 W) are used to determine the overall system efficiency. This efficiency data is presented in Fig. 6.4.

Except for the PFC boost converter, determining the individual module efficiencies for the AC system presents a special challenge. No power meters, true RMS voltage meters, or true RMS current meters are available with sufficient bandwidth to directly measure the efficiency of either the HB inverter or the post-regulators. To obtain the AC DPS extrapolated data shown in Fig. 6.4, the inverter efficiency was determined through "thermal calibration." This crude method essentially matches the heating of a resistive load by the inverter to the same heating of the same resistive load as supplied by a DC power source. The output power of the DC source is adjusted to achieve the same resistor case temperature that was obtained when using the inverter. The efficiency of the inverter can then be calculated based on the assumption the heating effects on the resistive load are identical for both the AC and DC sources. A small "thermal chamber" was constructed for the resistive loads, which were mounted on a large heatsink. The efficiency of a post-regulator was estimated by measuring the individual efficiencies of the PFC boost converter and HB inverter at 100 W, and calculating the post-regulator efficiency from the overall system efficiency data given in Fig. 6.3.

6.3.2 Induced logic noise

Figure 6.5 somewhat summarizes the results of attempts to measure the induced logic noise for the DC DPS. The "noise" levels were much higher than expected, especially in

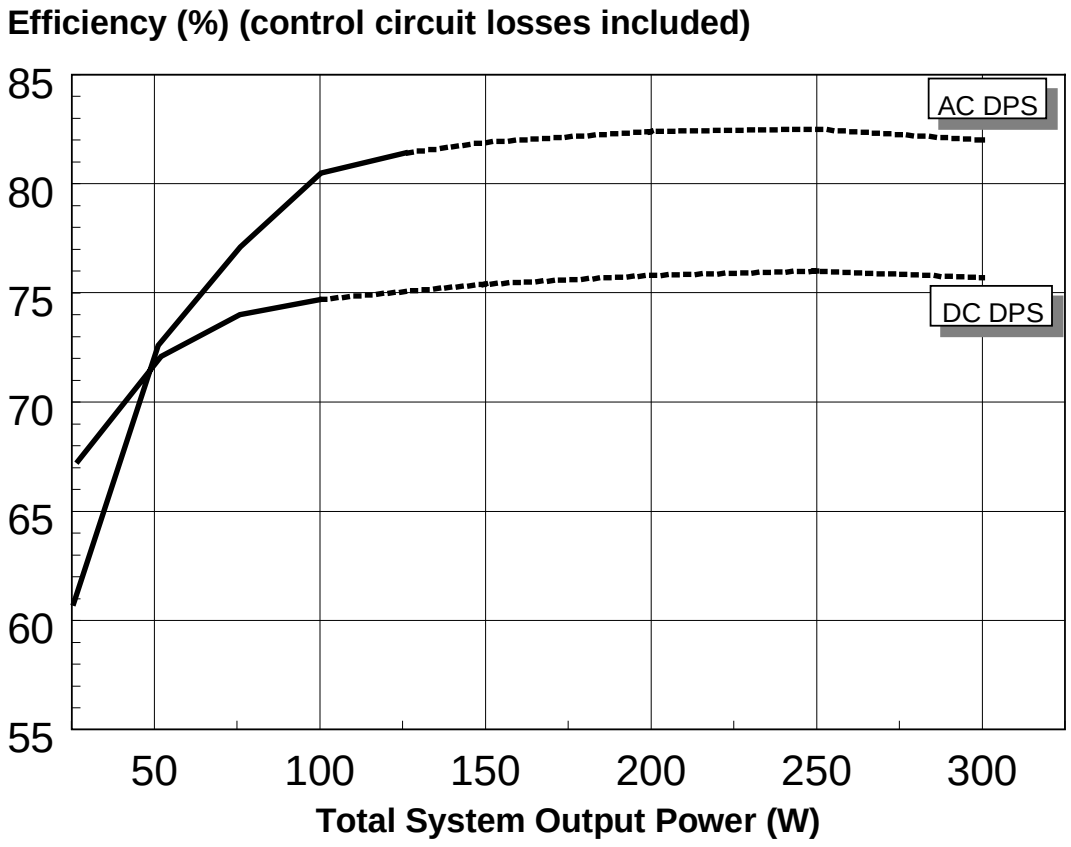
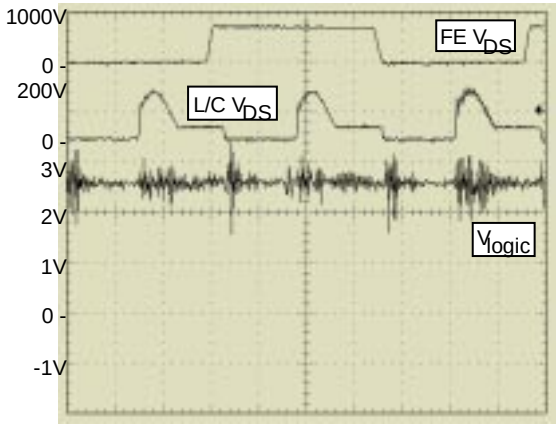
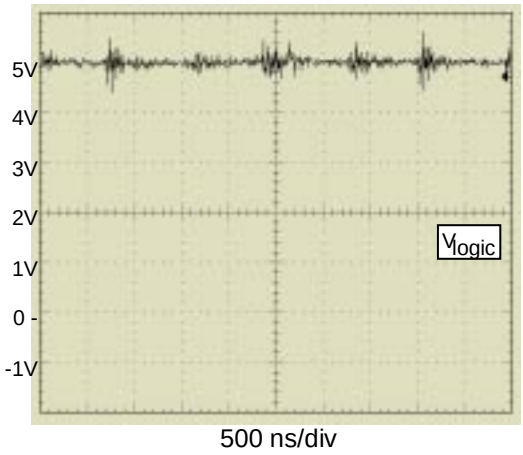


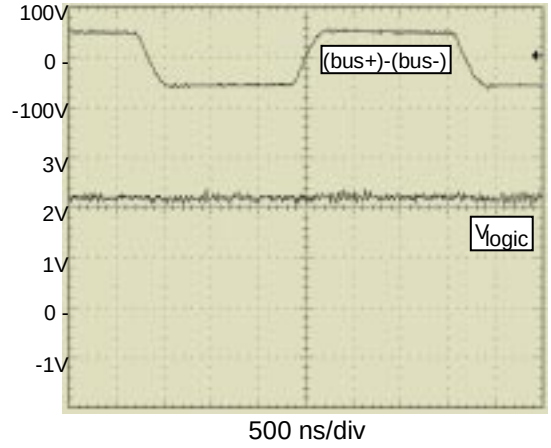
Fig. 6.4 Extrapolated experimental efficiencies.



(a) DC DPS, Vcc = 2.6 Vdc



(b) DC DPS, Vcc = 5 Vdc.



(c) AC DPS, Vcc = 2.2 V.

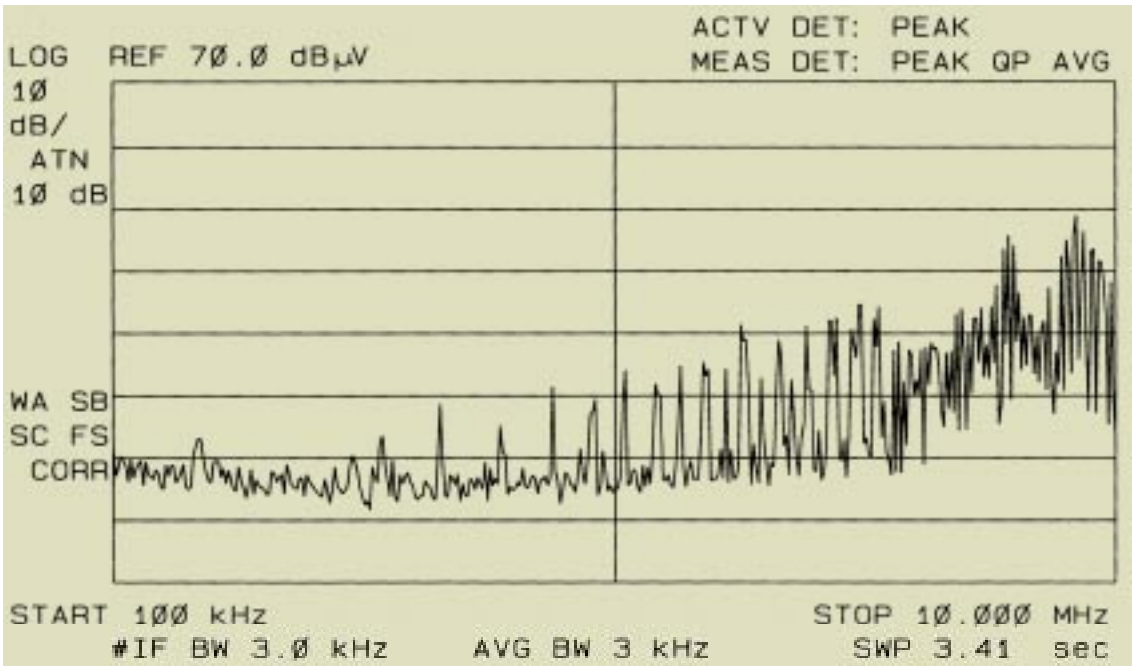
Fig. 6.5 Induced logic noise.

comparison with the AC DPS. As is apparent from the waveforms in Fig. 6.5(a), the logic noise "bursts" correspond to the drain voltage transitions of the inverter switches in the post-regulators. Increasing the logic supply voltage to 5 Vdc, as shown in Fig. 6.5(b), improved performance a small amount, indicating scope probe pickup as the primary contributing factor to the measured noise levels.

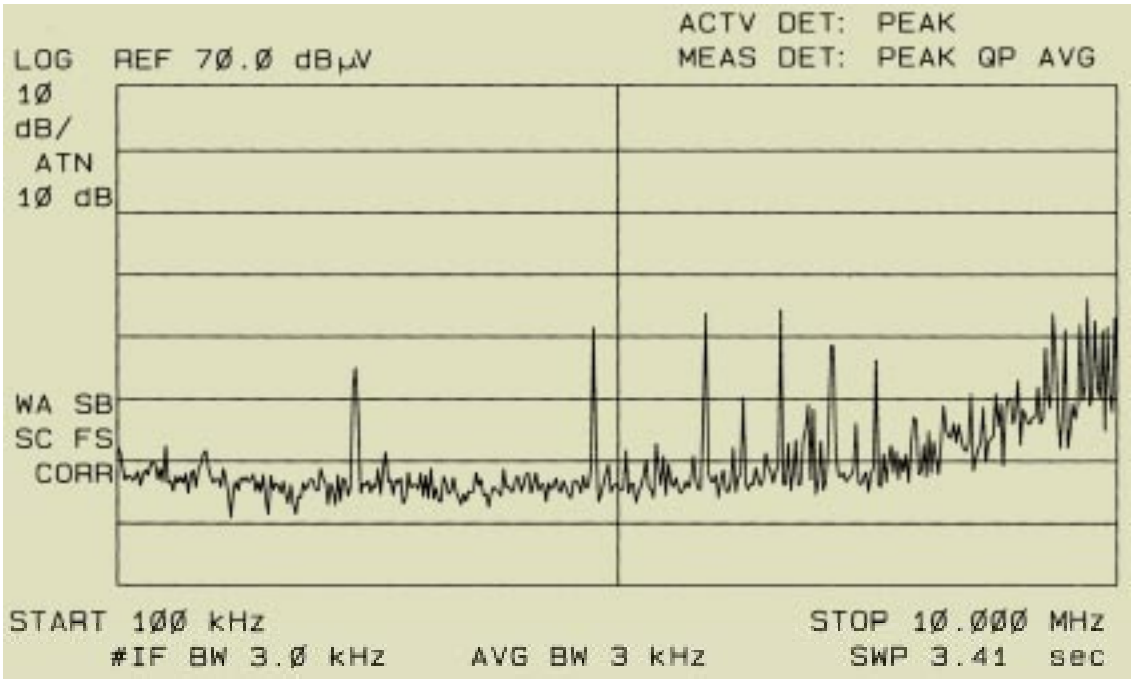
6.3.3 Electric and magnetic radiated fields

6.3.3.1 Electric field

The electric field measurements for both systems were carried out using the setup described in Section 5.3.3 and shown in Fig. 5.40. The results are shown in Figs. 6.6 (100 kHz to 10 MHz) and 6.7 (10 MHz to 50 MHz). All plots were taken at an operating point of Vin = 110 Vac and Po = 75 W. Starting first with Fig. 6.6, at frequencies below about 3 MHz the AC and DC systems are comparable, with the third and fifth AC DPS harmonics being about 10 dB above any DC DPS harmonics at similar frequencies. However, above 3 MHz the intensity of the electric field generated by the DC DPS far exceeds the AC system. In particular, around 25 MHz (see Fig. 6.7), the DC system's E field intensity is about 30 dB above the AC DPS's. Coincidentally, this is in the frequency range displayed by the high-frequency ringing present on the post regulator's drain waveform during transformer reset (see Fig. 6.2). As was experimentally demonstrated in Section 5.3.3, the bus structures being utilized here contribute very little to the electric field intensities that are being measured with the setup shown in Fig. 5.40. The data displayed in Figs. 6.6 and 6.7 confirm this (the bus voltages and currents are, for all practical purposes, "DC" when compared with the AC system's bus waveforms). The E field characteristics are predominately determined by the "quality" of the converter waveforms. Future investigations into the differences between the E field characteristics of AC and DC systems should focus on pinpointing the specific sources that give rise to these differences.

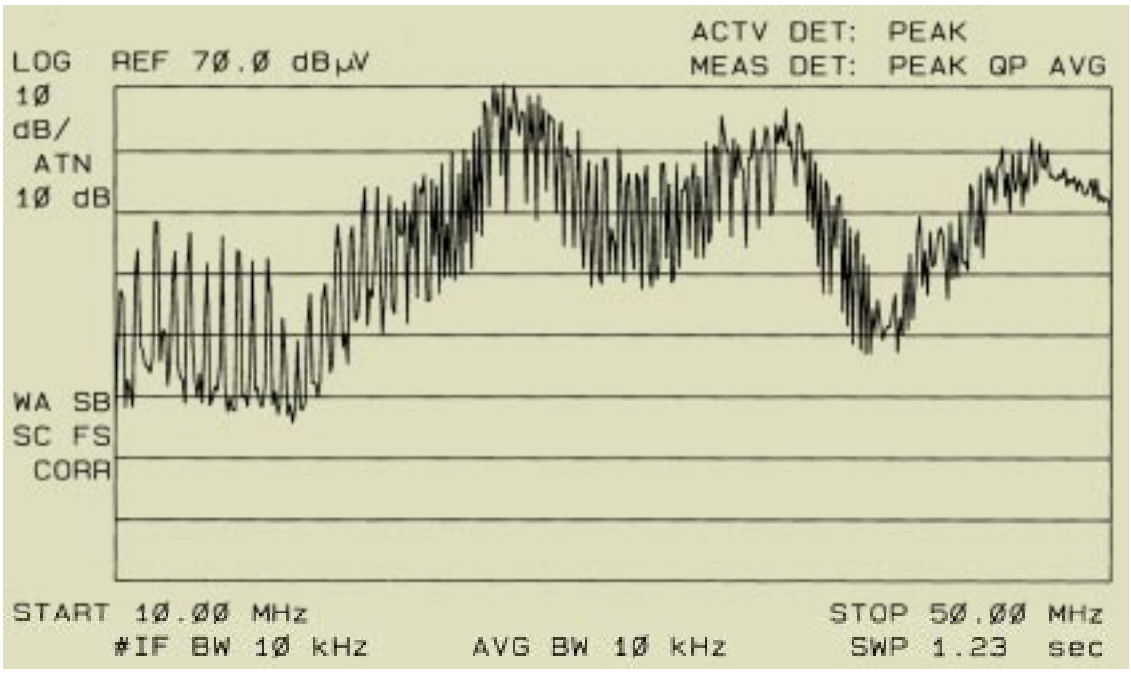


(a) DC DPS.

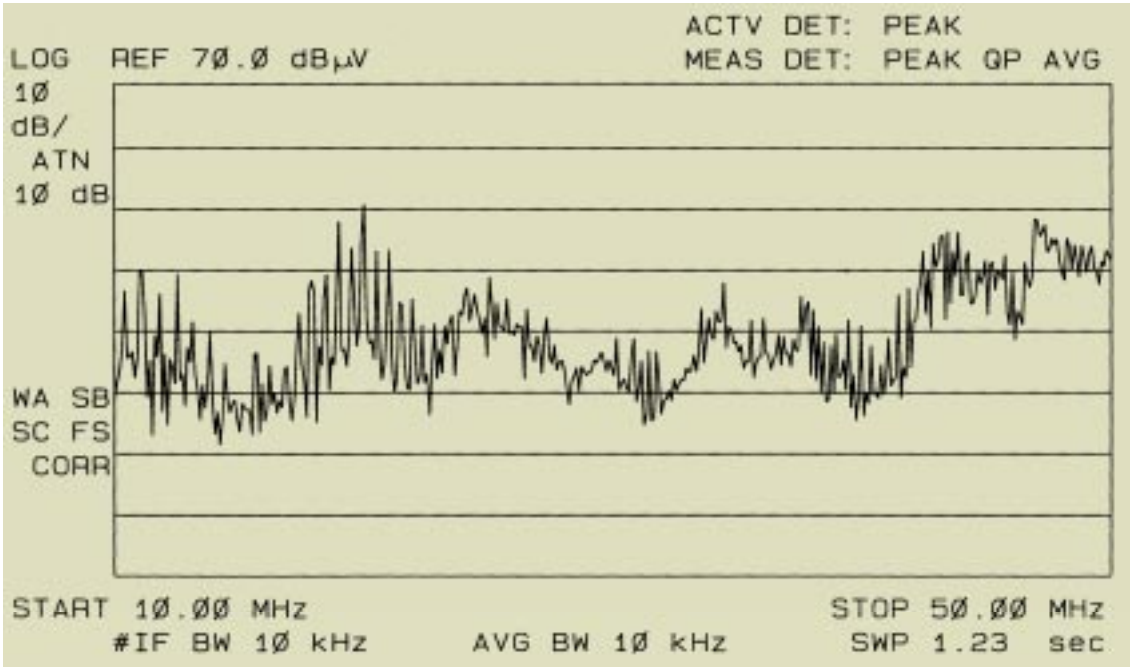


(b) AC DPS with $t_r/t_f \approx 190$ ns.

Fig. 6.6 E field radiated noise, 100 kHz - 10 MHz.



(a) DC DPS.



(b) AC DPS with $t_r/t_f \approx 190$ ns.

Fig. 6.7 E field radiated noise, 10 MHz - 50 MHz.

6.3.3.2 Magnetic field

The characteristics of the magnetic field in the immediate vicinity of the bus can be determined through the use of the experimental setup shown in Fig. 6.8. The HP11941A Close-Field Probe is designed to measure B field intensity over the frequency range shown in the figure [67]. The purposes of this experiment, the probe is placed directly on the top of the bus, approximately at the center-edge, as shown. Due to the thickness of the vector board used to mechanically insure the PCB structure, the probe tip resides about 60 mils above the actual bus conductor. During experimentation, it was noted that although the intensity of the magnetic field spectra changed as a function of probed placement around the bus, the *relative* difference between the AC and DC system data was fairly constant as long as the probe placement was within an inch or so of the bus.

The magnetic field data is presented in Fig. 6.9 for 100 kHz to 10 MHz, and in Fig. 6.10 for 10 MHz to 50 MHz. Beginning with Fig. 6.9(b) (since it is the only one of the four plots that has a ghost of a chance for explanation) shows the B field harmonics decreasing at a rate of about 20 dB/decade, as indicated on the plot. Referring to Fig. 5.36, the time domain waveform comprising the bus current is approximately trapezoidal with a duty cycle of 50 % and a rise/fall time of about 10 % of the waveform's period. It should be noted that this rise/fall time is the 0 % to 100 % time, not the 10 % to 90 % rise/fall times that have been associated with the bus voltage waveform. For such a current waveform, the harmonic amplitudes are given by:

$$I_n = I \frac{\sin(\frac{n\pi}{2})}{\frac{n\pi}{2}} \frac{\sin\left(\frac{n\pi}{10}\right)}{\frac{n\pi}{10}}, \tag{6.1}$$

where I is the peak-to-peak amplitude of the bus current and n is the harmonic number. The key feature to be derived from Eq. (6.1) is that the slope of the envelope of the bus

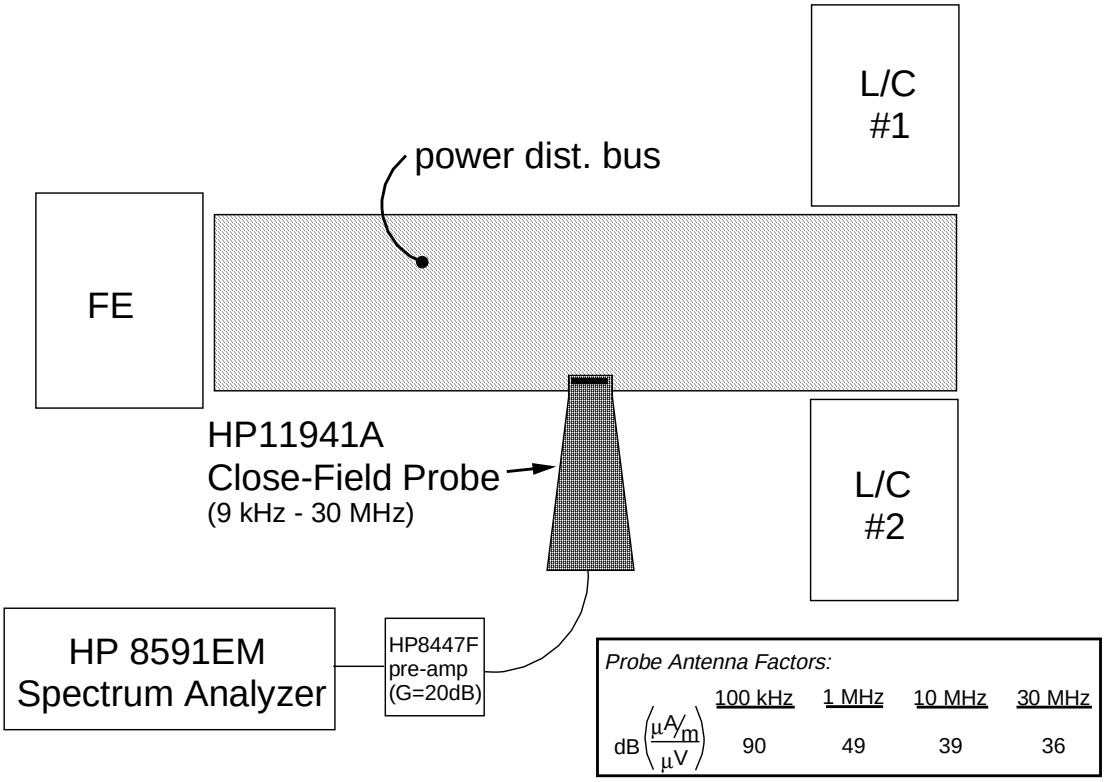


Fig. 6.8 Experimental B-field measurement setup.

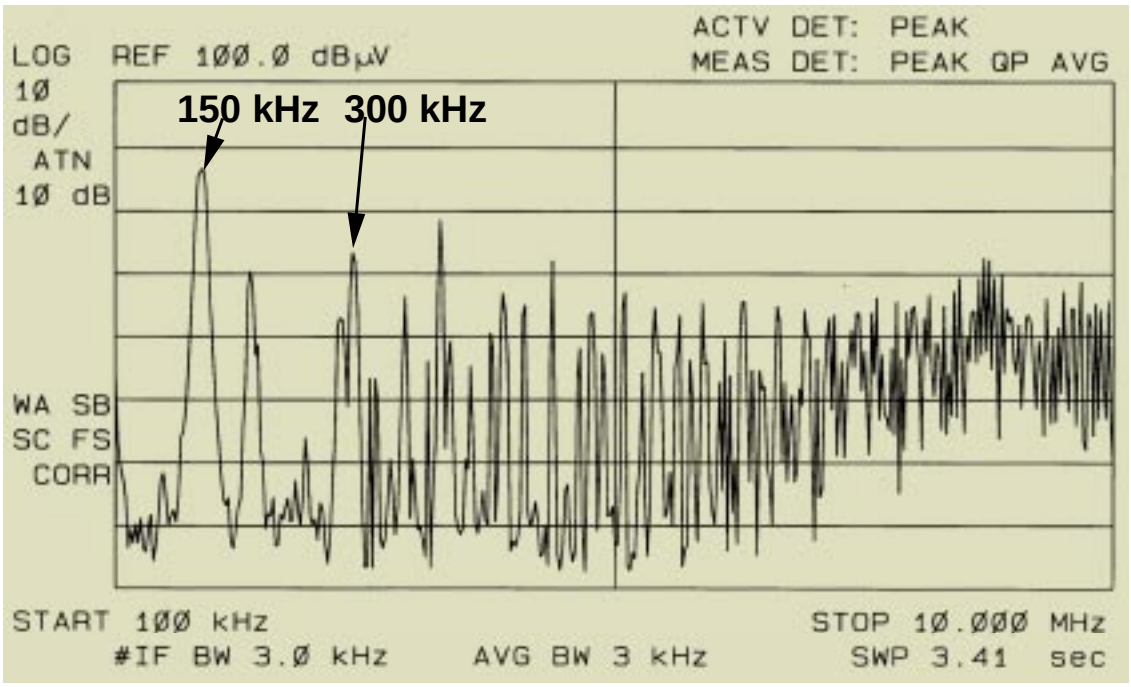
current harmonics is 20 dB/decade up to a frequency of $1/(\pi t_r)$, or about 1 MHz in this case. Above $1/(\pi t_r)$ Hz the envelope's slope is 40 dB/decade. The experimental result clearly shows the 20 dB/decade behavior, but this slope appears to continue well past 1 MHz. This could be partially due to the fact that the actual bus current has an "on" slope associated with the action of the post-regulator output inductors. This effect on the bus current harmonics is not taken into account by Eq. (6.1).

For the DC system, the magnetic field harmonics appear to follow a 20 dB/decade slope to just past 1 MHz, although way they would display this behavior is unclear. The time domain bus voltage and current waveforms for the DC system are shown in Fig. 6.11. The peak-to-peak bus current amplitude is about 250 mA and is somewhat sinusoidal in shape. While the low-frequency harmonics are less than the AC systems' (as would be expected), at higher frequencies the DC systems' magnetic field harmonics are on the order of 25 to 30 dB greater than the AC DPS's. Why this would be is not known, but probably has some association with the exaggerated electric field intensities displayed by the DC system at high frequencies. Much more experimental and theoretical work needs to be done to adequately account for the data presented in Figs. 6.9 and 6.10.

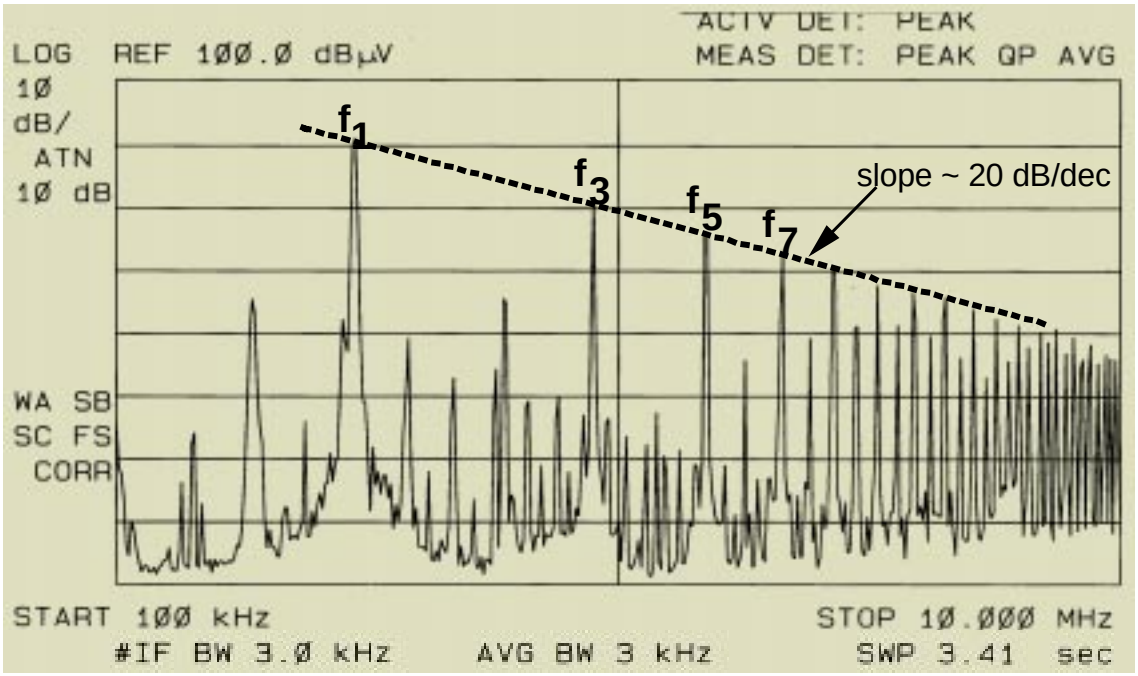
6.3.4 Piece parts cost

A similar cost analysis as was performed in the topology trade-off study for the AC DPS in Section 5.2 was also completed for the DC DPS. Table 6.1 summarizes the piece-parts costs for the DC and AC system front-ends (PFC boost converter is not included since it is common to both designs). Table 6.2 does likewise for the post-regulators. The data in the tables indicates that the front-end piece-parts cost for the AC DPS is about 20 % less than for the DC DPS. For the post regulators, the AC DPS parts costs are about 15 % (on a per module basis) less than for the DC DPS.

It needs to be emphasized that the cost comparison is valid only for the power train of the system under consideration here (300 W to 400 W total system power with roughly a

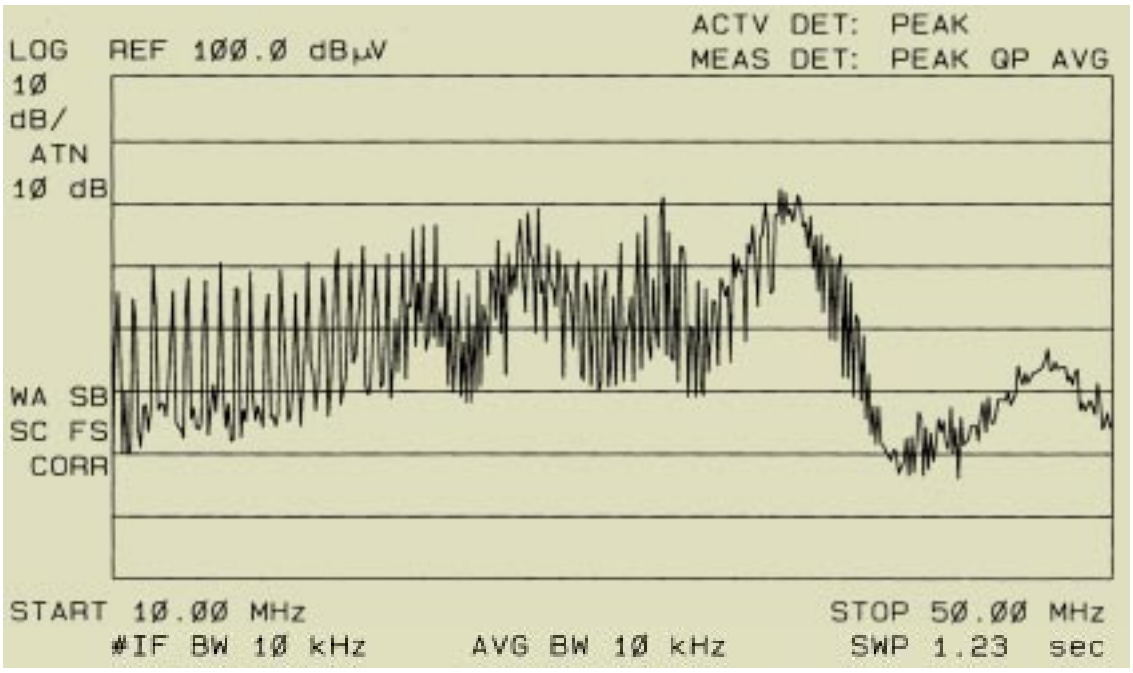


(a) DC DPS.

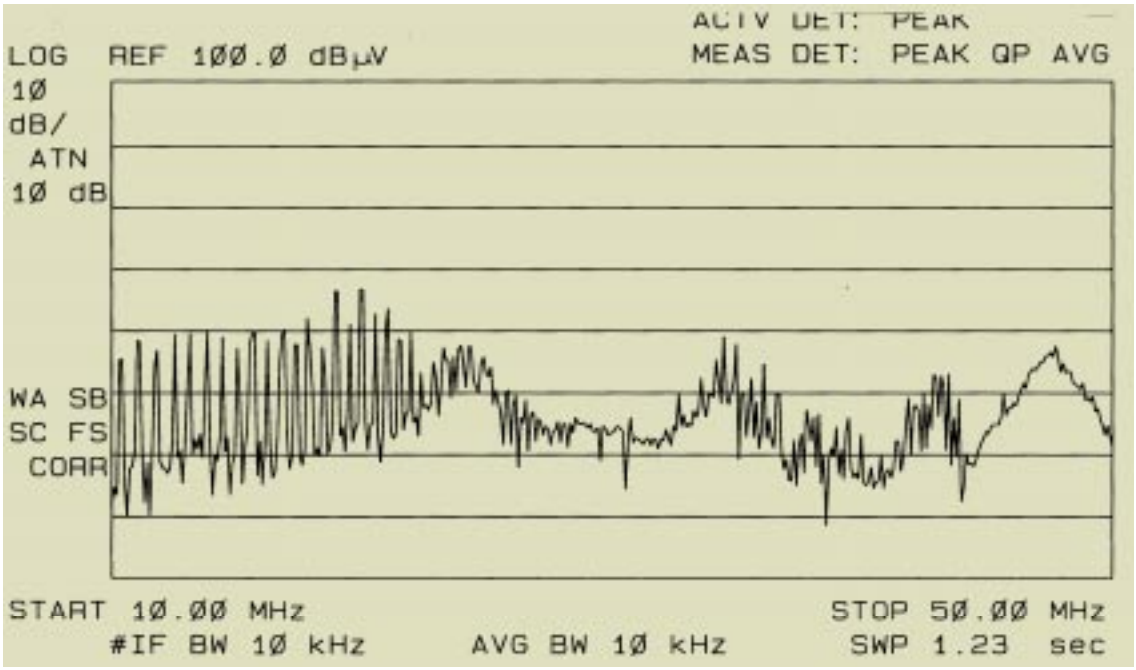


(b) AC DPS with $t_r/t_f \approx 190$ ns.

Fig. 6.9 B-field radiated noise, 100 kHz - 10 MHz.



(a) DC DPS.



(b) AC DPS with $t_r/t_f \approx 190$ ns.

Fig. 6.10 B-field radiated noise, 10 MHz - 50 MHz.

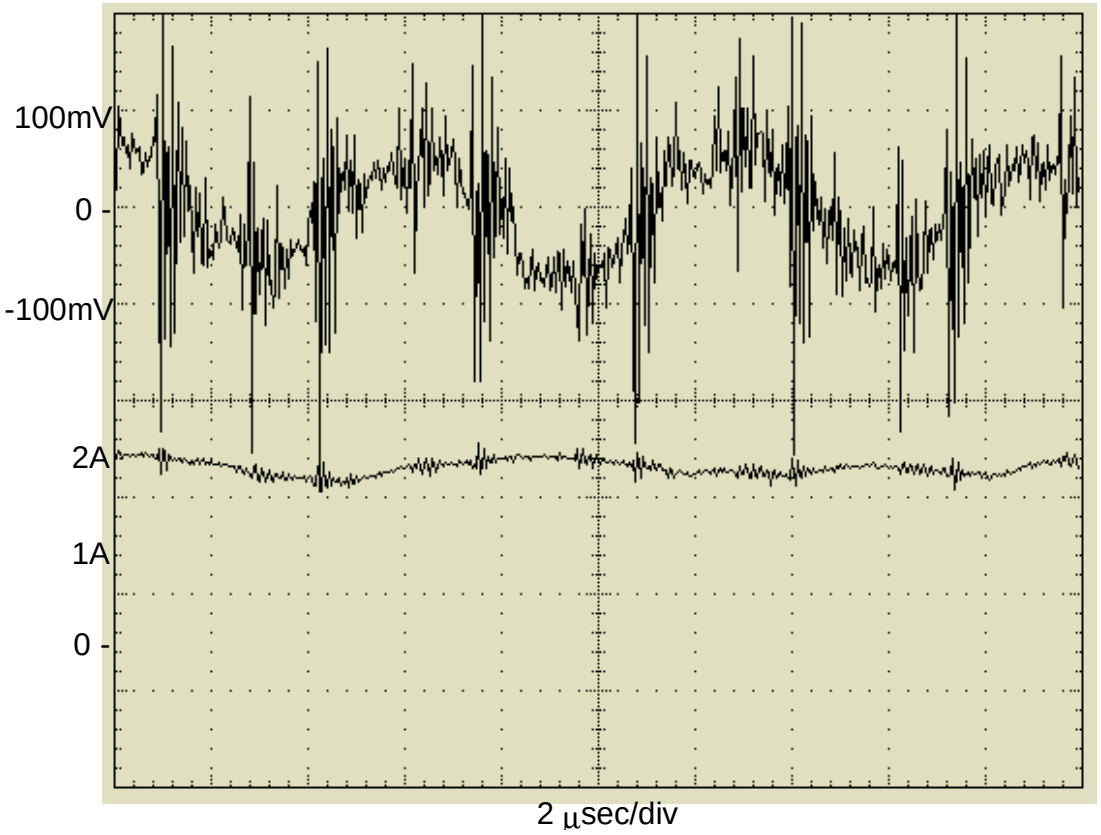


Fig. 6.11 DC DPS bus voltage and current. The bus voltage is AC coupled.

Table 6.1 DC and AC DPS FE piece parts cost summary.

	DC DPS	*Cost**	*AC DPS*	*Cost**
Transistors	**IRFPF50**	\$8.09	**2 x IRFP460**	\$5.78 ea
	IRFBF30	\$1.93		
Diodes	**2 x 10CTQ150**	\$1.72 ea		
Capacitors	**0.056 μF, 400V**	\$0.46		
	100 μF, 63V	\$0.34		
	2 x 1 μF HF, 100 V	\$0.49 ea		
	2 x 0.47 μF HF, 400V	\$1.22 ea	**2 x 1 μF HF, 250V**	\$1.77 ea
Magnetics	**Iso transformer**	\$2.00	**Iso transformer**	\$2.00
	Gate drive xfmr	\$0.25	**Gate drive xfmr**	\$0.25
	Output L	\$1.50		
Bus Reg Circuit	**PWM controller IC (UC3843 type)**	\$0.50		
	TL431	\$0.25		
	4N26 Optoisolator	\$0.34		
Driver Circuit	**2 x TC4426 MOSFET driver**	\$1.35 ea	**2 x TC4426 MOSFET driver**	\$1.35 ea
			LM555	\$0.24
			74AC74 Flip Flop	\$0.51
Total Cost		**\$25.22**		**\$20.80**

*Based on quantity 100 piece price from Digi-Key Corporation's July-September, 1998 catalog (except for magnetic components).

Table 6.2 DC and AC DPS post-regulator piece-parts cost summary.

	DC DPS	*Cost**	*AC DPS*	*Cost**
Transistors	**IRF640**	$1.16		
Diodes	**30CPQ060**	$3.07	**32CTQ030**	$1.55
Capacitors	**2 x 1 μF HF, 100 V**	$0.49 ea		
	68 μF OS-CON, 6.3V	$0.79 ea	**68 μF OS-CON, 6.3V**	$0.79
Magnetics	**Input L**	$0.50		
	Transformer	$1.25	**Transformer**	$1.50
	Output L	$0.65	**Output L**	$0.50
			2 x magamp	$1.38 ea
Output Reg Circuit		$2.50 (total)		$2.50 (total)
	4N26 Optoisolator	$0.34		
Total Cost		**$11.24**		**$9.60**

*Based on quantity 100 piece price from Digi-Key Corporation's July-September, 1998 catalog (except for magnetic components). OS-CON capacitor prices based on quantity 1000 pieces.

20 % to 100 % load range). Costs for such functions as post-regulator fault protection, current control, etc. are not included and could skew the comparison. For example, the presence of the relatively expensive magamps in the AC DPS post-regulator designs offsets the cost of the additional "inverter" switch required by the DC DPS post-regulators. However, this inverter switch can also serve the purpose of disconnecting the post-regulator from the bus in the event a fault is detected. For the AC DPS post-regulators implementation investigated here, the magamps could fulfill this purpose, but only with a considerable increase in size and cost over the parts used in the testbed. As another example, expanding the post-regulator load range will also increase the size and cost of and power loss in the magamps. No such detriment would occur with the DC DPS's post-regulator inverter switch. It is interesting to note that the DC DPS is considerably less expensive than the sinewave AC DPS examined in Chapter 5.

6.4 Summary

This chapter has experimentally demonstrated several fundamental advantages of the AC DPS developed in Chapter 5 over a DC DPS designed to the identical specifications. These include:

1) A power train efficiency improvement of more than 5 % over the DC system between total system load ranges of 20 % to 100 %. This includes control circuit losses.

2) Electric field intensities which are actually *lower* for the AC DPS when compared with the DC system. DC DPS performance can be made comparable to the AC DPS by choosing FE and, in particular, post-regulator topologies that utilize switch waveforms with lower peak voltage stresses and lower harmonic content. However, the complexity, and hence the cost of the DC DPS will increase.

3) A front-end piece-parts cost reduction of about 20 % over the DC DPS front-end, and an approximate 15 % per post-regulator cost reduction.

The experimental comparison of the magnetic field intensity needs further analysis before firm conclusions can be drawn.