# Evaluation and Design of a SiC-Based Bidirectional Isolated DC/DC Converter

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## Abstract

Galvanic isolation between the grid and energy storage unit is typically required for bidirectional power distribution systems. Due to the recent advancement in wide-bandgap semiconductor devices, it has become feasible to achieve the galvanic isolation using bidirectional isolated DC/DC converters instead of line-frequency transformers.

A survey of the latest generation SiC MOSFET is performed. The devices were compared against each other based on their key parameters. It was determined that under the given specifications, the most suitable devices are X3M0016120K 1.2 kV 16 mΩ and C3M0010090K 900 V 10 mΩ SiC MOSFETs from Wolfspeed.

Two of the most commonly utilized bidirectional isolated DC/DC converter topologies, dual active bridge and CLLC resonant converter are introduced. The operating principle of these converter topologies are explained. A comparative analysis between the two converter topologies, focusing on total device loss, has been performed. It was found that the CLLC converter has lower total device loss compared to the dual active bridge converter under the given specifications. Loss analysis for the isolation transformer in the CLLC resonant converter was also performed at different switching frequencies. It was determined that the total converter loss was lowest at a switching frequency of 250 kHz

A prototype for the CLLC resonant converter switching at 250 kHz was then designed and built. Bidirectional power delivery for the converter was verified for power

levels up to 25 kW. The converter waveforms and efficiency data were captured at different power levels. Under forward mode operation, a peak efficiency of 98.3% at 15 kW was recorded, along with a full load efficiency value of 98.1% at 25 kW. Under reverse mode operation, a peak efficiency of 98.8% was measured at 17.8 kW. The full load efficiency at 25 kW under reverse mode operation is 98.5%.

# Evaluation and Design of a SiC-Based Bidirectional Isolated DC/DC Converter

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## General Audience Abstract

Electrical isolation between the grid and energy storage unit is typically required for bidirectional power distribution systems. Traditionally, this isolation is achieved via line-frequency transformers, which tend to be bulky and heavy. This imposes a limit on the overall system power density, which is a crucial performance metric for bidirectional power distribution systems.

Alternatively, the required electrical isolation can be implemented through bidirectional power converters. As a result, the overall system power density can be drastically improved. However, the losses incurred by the semiconductor devices in such converters could significantly reduce the overall system efficiency, which is another important performance metric.

Due to the recent advancement in semiconductor devices, it has become feasible to design the required bidirectional power converters with high efficiency and high power density. A survey of the latest generation semiconductor devices is performed. A 25 kW converter prototype was designed and built using the selected semiconductor devices. Experimental testing was conducted for the converter prototype and efficiency values exceeding 98% were captured across the entire load range. The converter prototype has a power density of 78 W/in$^3$.

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# Chapter 1 Introduction

## 1.1 Background

Galvanic isolation between the grid and the energy storage unit is typically required in bidirectional power distribution systems due to safety reasons. Traditionally this is achieved using line-frequency transformers as shown in Figure 1.1 [1]. While line-frequency transformers are relatively efficient, they tend to be bulky and heavy. This has a large impact on the system power density. The technical specifications for a 30 kVA rated line-frequency transformer from Eaton is outlined in Table 1.1.

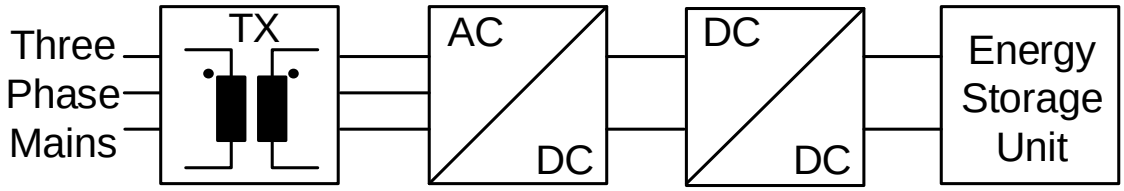



Figure 1.1. Bidirectional power distribution system with line-frequency transformer.

Table 1.1. Technical specifications for V48M47T3016CU transformer from Eaton.

| **Specifications** | **V48M47T3016CU** |
|---|---|
| Power Rating | 30 kVA |
| Volume | 19388 $in^3$ |
| Length | 36.88 in |
| Width | 21.13 in |
| Height | 24.88 in |
| Weight | 415 lb |
| Efficiency | > 98.23% |

Alternatively, galvanic isolation can be achieved with bidirectional isolated DC/DC converters operating as a DC transformer (DCX) shown in Figure 1.2 [2]. The typical structure of such converter topologies is shown in Figure 1.3. An isolation transformer operating at the switching frequency of the converter provides the galvanic isolation. There is a full-bridge network on each side of the isolation transformer to allow power delivery in both direction. Usually, there are also reactive elements connected to the isolation transformer that are driven by the output of the full-bridge network. The switching frequency of such converters tends to be in the range of at least tens of kilohertz. The size of the transformer for a given power level is inversely proportional to the operating frequency. The higher operating frequency in the isolated DC/DC converter enables a reduction in transformer volume by orders of magnitude. Consequently, the weight of the transformer is also reduced.

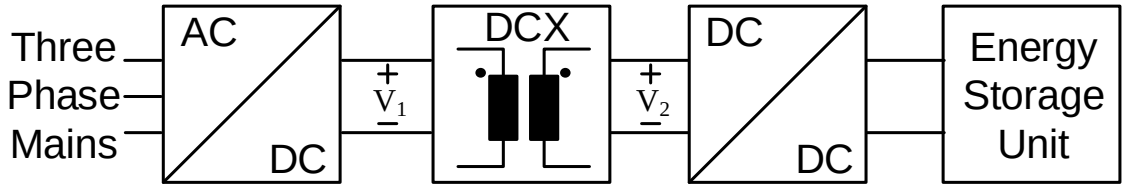



Figure 1.2. Bidirectional power distribution system with DC transformer (DCX).

The total device loss forms a large portion of the loss in a bidirectional isolated DC/DC converter. The loss in a device can be broken down into driving loss, conduction loss and switching loss. At higher power levels, the driving loss is usually negligible compared to the conduction loss and switching loss. For a given power level, the conduction loss is determined by the on-state resistance of the device in the converter. The higher the on-state resistance, the greater the conduction loss will be in the converter.

The switching loss is determined by the switching speed of the device. Faster switching transitions leads to lower switching energy dissipated in the device. The switching loss in a device is a product of the switching energy and switching frequency. Therefore, if a specified converter efficiency needs to be met, the switching speed imposes a limit on the maximum allowable witching frequency. This poses an obstacle on further reduction in the isolation transformer volume.

Based on the above discussions, it can be concluded that the semiconductor device has a large impact on the overall performance of the bidirectional isolated DC/DC converter. Devices with low on-state resistance and faster switching speed are required to improve both the efficiency and power density of the converter.

Recent advancements in semiconductor devices have dramatically increased the switching speed of the devices along with reduction in the on-state resistance. This enables the power density and the efficiency of the bidirectional isolated DC/DC converter to be pushed even further.

A survey on the performance metrics of state of the art bidirectional isolated DC/DC converters has been performed. The data for peak efficiency vs. rated power is shown in Figure 1.4. The figure shows higher efficiency in bidirectional isolated DC/DC converters across different rated power levels has been reported in recent years. .

The curve for power density vs. rated power level for state of the art bidirectional isolated DC/DC converters is shown in Figure 1.5. Additionally, the power density values for these converters are plotted against their peak efficiency values as shown in Figure 1.6. The general trend suggests that the advancement in semiconductor devices has enabled an increase in both the power density and the peak efficiencies of power converters.

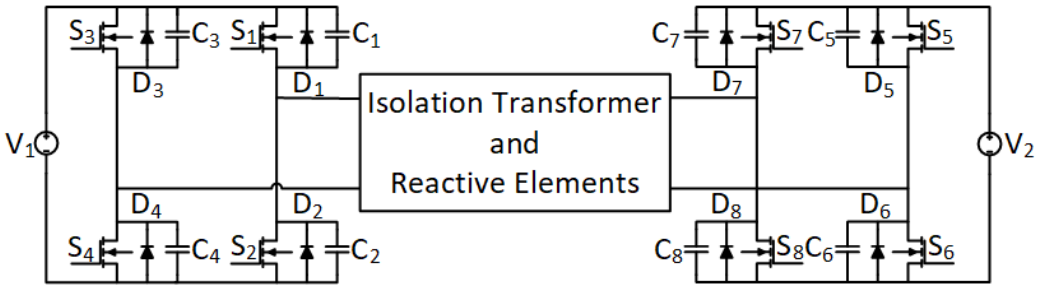



Figure 1.3. General circuit structure of bidirectional isolated DC/DC converter.

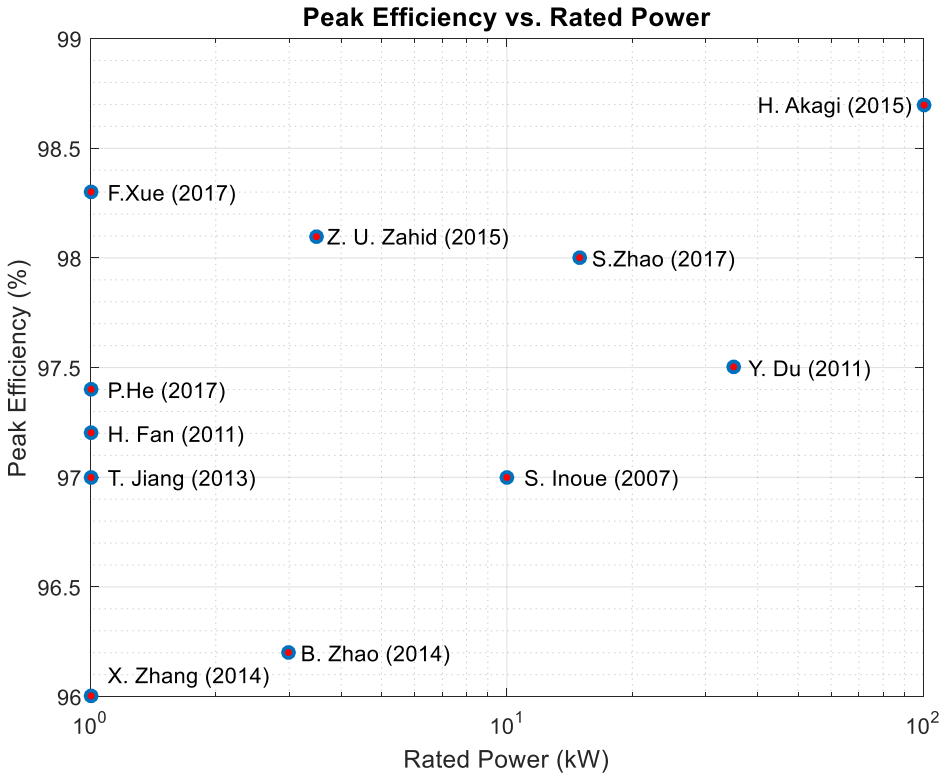



Figure 1.4. Peak efficiency vs. rated power for state of the art bidirectional isolated DC/DC converter reported by S. Zhao (2017) [3], B. Zhao (2014) [4], Z. U. Zahid (2015) [5], P. He (2017) [6], F. Xue (2017) [7], H. Akagi (2015) [8], S. Inoue (2007) [9], H. Fan (2011) [10], X. Zhang (2014) [11], T. Jiang (2013) [12], Y. Du (2011) [13].

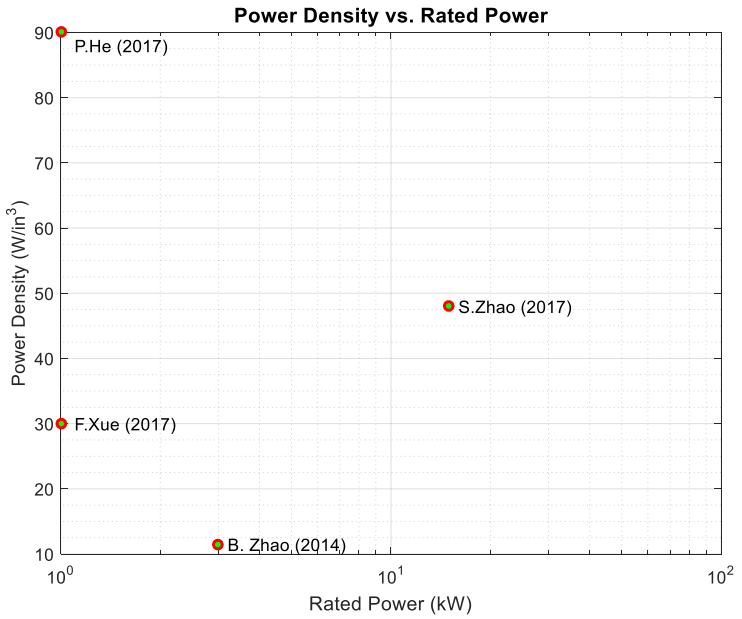



Figure 1.5. Power density vs. rated power for state of the art bidirectional isolated DC/DC converter reported by S. Zhao (2017) [3], B. Zhao (2014) [4], P. He (2017) [6], F. Xue (2017) [7].

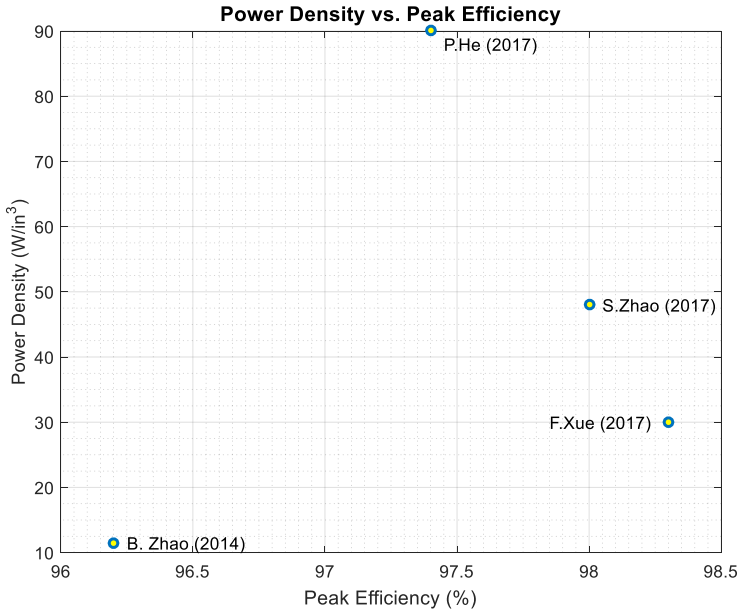



Figure 1.6. Power density vs. peak efficiency for state of the art bidirectional isolated DC/DC converter reported by S. Zhao (2017) [3], B. Zhao (2014) [4], P. He (2017) [6], F. Xue (2017) [7].

The objective of the research outlined in this thesis is to evaluate and design a bidirectional isolated DC/DC converter to achieve galvanic isolation in a bidirectional power distribution system. This converter shall be designed for high efficiency and high power density using latest generation semiconductor devices. The target specifications for the converter are outlined in Table 1.2.

Table 1.2. Converter specifications.

| **Converter Specifications** | **Value** |
|---|---|
| Bidirectional Power Output | 25 kW |
| Primary Side Voltage, $V_1$ | 800 V |
| Secondary Side Voltage, $V_2$ | 530 V |
| Peak Efficiency | > 98.5% |
| Power Density | > 70 W/in$^3$ |

## 1.2 Thesis Outline

This thesis shall focus on the design and evaluation for a SiC-based bidirectional isolated DC/DC converter based on the given specifications. This converter shall serve as a DC transformer in a bidirectional power distribution system, providing the required galvanic isolation that is traditionally fulfilled by a line-frequency transformer.

In Chapter 1, the motivation for achieving galvanic isolation using bidirectional isolated DC/DC converters in a bidirectional power distribution system is discussed. The improved feasibility of this application due to the recent advancement in wide-bandgap semiconductor technology is explained. A survey on the performance metrics of state-of-the-art bidirectional isolated DC/DC converters is performed. The target specifications for the converter prototype to be designed and built is also presented.

In Chapter 2, an overview of different semiconductor device technology is provided. The selection of the latest generation SiC power MOSFETS under the given converter specifications is performed. Two of the most common bidirectional isolated DC/DC converter topologies, dual active bridge and CLLC resonant converter are introduced. The operation and salient characteristic of the two topologies are then discussed. For the given converter specification, a comparative analysis between the two topologies is performed to determine the topology with the lowest total device loss. Loss analysis on the isolation transformer in the converter is also performed to determine the optimal switching frequency.

Chapter 3 focuses on the design of the 25 kW CLLC resonant converter prototype. Design challenges associated with high frequency switching of SiC MOSFETs are considered. Gate driver circuitry design is performed to address the design challenges such as asymmetry in propagation delay, crosstalk and common mode transient immunity. The impact of the power stage layout on converter performance is also discussed. In addition, the layout of the actual power stage, in particular the steps taken to minimize gate-loop inductance and commutation path inductance are presented.

Testing and evaluation of the 25 kW converter prototype is outlined in Chapter 4. The verification of the power stage layout and gate driver design via double pulse testing is presented. The captured waveforms for double pulse testing on the devices with different external gate resistance are presented. The assembled 25 kW converter prototype was tested up to 25 kW with power delivery in both directions. The converter operating waveforms along with the efficiency data are captured at different power levels.

Chapter 5 provides an overall summary of the thesis along with potential areas of interest that can be continued as an extension of the research outlined in this thesis.

# Chapter 2 Device Selection and Topology Evaluation

## 2.1 Wide-Bandgap Device Selection

The key material properties for silicon (Si), silicon carbide (SiC) and gallium nitride (GaN) are outlined in Table 2.1 [14] [15]. Due to their larger bandgap energy compared to silicon, silicon carbide and gallium nitride are referred to as wide-bandgap semiconductor materials. This bandgap energy is typically defined as the energy required for electrons to jump from one layer to another. Theoretically, a higher bandgap energy indicate a lower leakage current and higher operating temperatures.

Wide-bandgap semiconductor devices also have larger critical fields compared to silicon. This larger critical field enables a thinner drift region for a given breakdown voltage. As a result, a lower on-state resistance values can be achieved for wide-bandgap devices. The larger electron mobility for the wide-bandgap materials further reduces the required die-area for a given on-state resistance. Given that the junction capacitance of a semiconductor device is related to the die area, wide-bandgap devices would have lower capacitance. The lower junction capacitance combined with a higher saturated electron velocity lead faster switching transitions compared to silicon devices with similar power ratings, hence the resulting switching energy is lower [16] [17] [18] [19]. Finally, the higher thermal conductivity for wide-bandgap semiconductor devices reduces the burden on the thermal management components within the system. Consequently, the power density of the converter can be further improved.

Table 2.1. Material properties for Si, SiC and GaN materials.

| Material Property | Si | SiC | GaN |
|---|---|---|---|
| Bandgap (eV) | 1.12 | 3.2 | 3.4 |
| Critical Field (MV/cm) | 0.3 | 3.5 | 3.3 |
| Electron Mobility ($cm^2$/V-s) | 1500 | 650 | 2000 |
| Saturated Electron Velocity ($10^7$ cm/s) | 1.0 | 2.0 | 2.5 |
| Thermal Conductivity (W/cm-K) | 1.5 | 4.9 | 1.3 |

Based on the general structure of the converter, the full bus voltage shall appear across the device when it is turned off. This corresponds to 800 V for the primary side device and 533 V for the secondary side device as outlined in the converter specifications. General design guidelines suggest that the rated voltage of the device needs to be at least 1.5 times the full bus voltage. Therefore, the primary side and secondary side devices need to be rated for at least 1.2 kV and 800 V respectively. However, a recent survey shows that commercially available GaN devices have voltage ratings up to 650 V only [15]. Therefore, silicon carbide devices shall be selected for the specified converter.

A survey of the latest generation SiC MOSFETs has been performed and outlined in Table 2.2 along with the key performance metrics. The 1.2 kV 16 mΩ (X3M0016120K) and 900 V 10 mΩ (C3M0010090K) devices from Wolfspeed are selected for the primary side and the secondary side respectively. These two devices have the lowest $R_{ds,on}$ among devices with similar voltage ratings. In addition, the Kelvin connection in the TO-274-4 package yields lower switching energy resulting in lower expected switching loss compared to similar devices with TO-247-3 packaging [20].

Table 2.2. Summary of latest generation SiC MOSFET devices.

| | **X3M0016120K** | **C2M0025120D** | **GE12025RF-3** | **C3M0010090K** |
|---|---|---|---|---|
| Manufacturer | Wolfspeed | Wolfspeed | GE | Wolfspeed |
| $V_{dss}$ (V) | 1200 | 1200 | 1200 | 900 |
| Package | TO-247-4 | TO-247-3 | DE-150 | TO-247-4 |
| $R_{ds,on}$@25°C (mΩ) | 16 | 25 | 25 | 10 |
| $T_j$ (°C) | -50 to +175 | -55 to +150 | -55 to +175 | -55 to +150 |
| $I_D$ @ 25°C (A) | 107 | 90 | 61 | 160 |
| $V_{gs}$ (V) | -8/+19 | -10/+25 | -15/+23 | -8/+19 |
| $V_{gs,th}$ (V) | 2.5 | 2.6 | 3.2 | 2.4 |
| $C_{oss}$ (pF) | 233 @$V_{DS}$ = 1000 V | 220 @$V_{DS}$ = 1000 V | 199 @$V_{ds}$ = 500 V | 350 @$V_{DS}$ = 600 V |
| $Q_g$ (nC) | 227 (-4/+15 V) @$V_{DS}$ = 800 V | 161 (-5/+20 V) @$V_{DS}$ = 800 V | 170 (0/20V) @$V_{DS}$ = 600 V | 222 (-4/+15 V) @$V_{DS}$ = 600 V |

## 2.2 Operation of Bidirectional Isolated DC/DC Converter Topologies

Dual active bridge (DAB) is one of the most commonly used topology for bidirectional isolated DC/DC power conversion [6] [13] [21] [22]. It was first proposed by R.W. De Doncker in [23]. The circuit diagram for the dual active bridge converter is shown in Figure 2.1. The equivalent circuits during one complete switching cycle are shown in Figure 2.2 and Figure 2.3. The converter waveforms under steady state operation are shown in Figure 2.4.

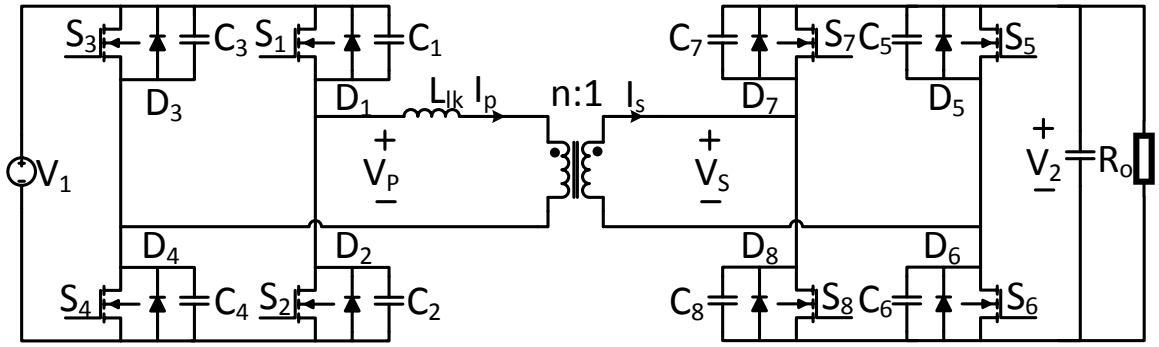



Figure 2.1. Dual active bridge converter.

The operation of the dual active bridge converter during one complete switching cycle is discussed below [24].

Mode 1 [$t_1$-$t_2$]: At $t_1$, the MOSFETs $S_1$ and $S_4$ are turned on. The MOSFETs $S_5$ and $S_8$ are already conducting. The primary side bridge output $V_p$ is positive. The secondary side bridge output $V_s$ is negative. Therefore, a positive voltage is applied across the leakage inductor $L_{lk}$ and the current flowing through it increases linearly. In the case where the voltage $V_1$ is equal to or greater than the value of $V_2$ reflected to the primary side, the initial current flowing through inductor $L_{lk}$ at $t_1$ will always be negative.

Mode 2 [$t_2$-$t_3$]: At $t_2$, the MOSFETs $S_5$ and $S_8$ turn off. The MOSFETs $S_1$ and $S_4$ are still conducting. The energy stored in inductor $L_{lk}$ at $t_2$ charges the output capacitances $C_5$ and $C_8$ and discharges $C_6$ and $C_7$. The voltage across the secondary side bridge output Vs transitions from $-V_2$ to $+V_2$. If the energy stored in the leakage inductor is sufficient to complete the charge and discharge process of these capacitances, then ZVS is achieved by MOSFETs $S_6$ and $S_7$ when they are turned on at $t_3$. No power transfer from primary side to secondary side occurred during this interval.

Mode 3 [$t_3$-$t_4$]: At $t_3$, the MOSFETs $S_6$ and $S_7$ are turned on. The MOSFETs $S_1$ and $S_4$ are already conducting. The voltage across the primary side bridge output is positive.

The voltage across the secondary side bridge output is also positive. Assuming the voltage $V_1$ is equal to or greater than the value of $V_2$ reflected to the primary side, the current flowing through inductor $L_{lk}$ ramps up linearly.

Mode 4 [$t_4$-$t_5$]: At $t_4$, the MOSFETs $S_1$ and $S_4$ turn off at the peak inductor current value. The MOSFETs $S_7$ and $S_8$ are still conducting. The energy stored in the inductor $L_{lk}$ at $t_2$ charges the MOSFET output capacitances $C_1$ and $C_4$ and discharges $C_2$ and $C_3$. The voltage across primary side bridge output $V_p$ transitions from the $+V_1$ to $-V_1$. If the energy stored in the leakage inductor is sufficient to complete the charge and discharge process of these capacitances, then ZVS is achieved by MOSFETs $S_2$ and $S_3$ when they are turned on at $t_5$. No power transfer from primary side to secondary side occurred during this interval.

Mode 5 [$t_5$-$t_6$]: At $t_5$, the MOSFETs $S_2$ and $S_3$ are turned on. The MOSFETs $S_7$ and $S_8$ are already conducting. The voltage across the primary side bridge output is negative. The voltage across the secondary side bridge output is positive. The resulting voltage applied across inductor $L_{lk}$ is negative. The current flowing through the leakage inductor $L_{lk}$ ramps down linearly.

Mode 6 [$t_6$-$t_7$]: At $t_6$, the MOSFETs $S_6$ and $S_7$ turn off. The MOSFETs $S_2$ and $S_3$ are still conducting. The energy stored in inductor $L_{lk}$ at $t_6$ charges the output capacitances $C_6$ and $C_7$ and discharges $C_5$ and $C_8$. The voltage across secondary side bridge output Vs transitions from $+V_2$ to $-V_2$. If the energy stored in the leakage inductor is sufficient to complete the charge and discharge process of these capacitances, then ZVS is achieved by MOSFETs $S_5$ and $S_8$ when they are turned on at $t_7$. No power transfer from primary side to secondary side occurs during this interval.

Mode 7 [$t_7$-$t_8$]: At $t_7$, the MOSFETs $S_5$ and $S_8$ are turned on. The MOSFETs $S_2$ and $S_3$ are already conducting. The voltage across the primary side bridge output is negative. The voltage across the secondary side bridge output is also negative. Assuming the voltage $V_1$ is equal to or greater than the value of $V_2$ reflected to the primary side, the current flowing through inductor $L_{lk}$ ramps down linearly.

Mode 8 [$t_8$-$t_9$]: At $t_8$, the MOSFETs $S_2$ and $S_3$ turn off at the most negative leakage inductor current value. The MOSFETs $S_5$ and $S_8$ are still conducting. The energy stored in the inductor $L_{lk}$ at $t_8$ charges the output capacitance $C_2$ and $C_3$ and discharges $C_1$ and $C_4$. The voltage across primary side bridge output $V_p$ transitions from the $-V_1$ to $+V_1$. If the energy stored in the leakage inductor is sufficient to complete the charge and discharge process of these capacitances, then ZVS is achieved by MOSFETs $S_1$ and $S_4$ when they are turned on at $t_5$. No power transfer from primary side to secondary occurs side occurs during this interval.

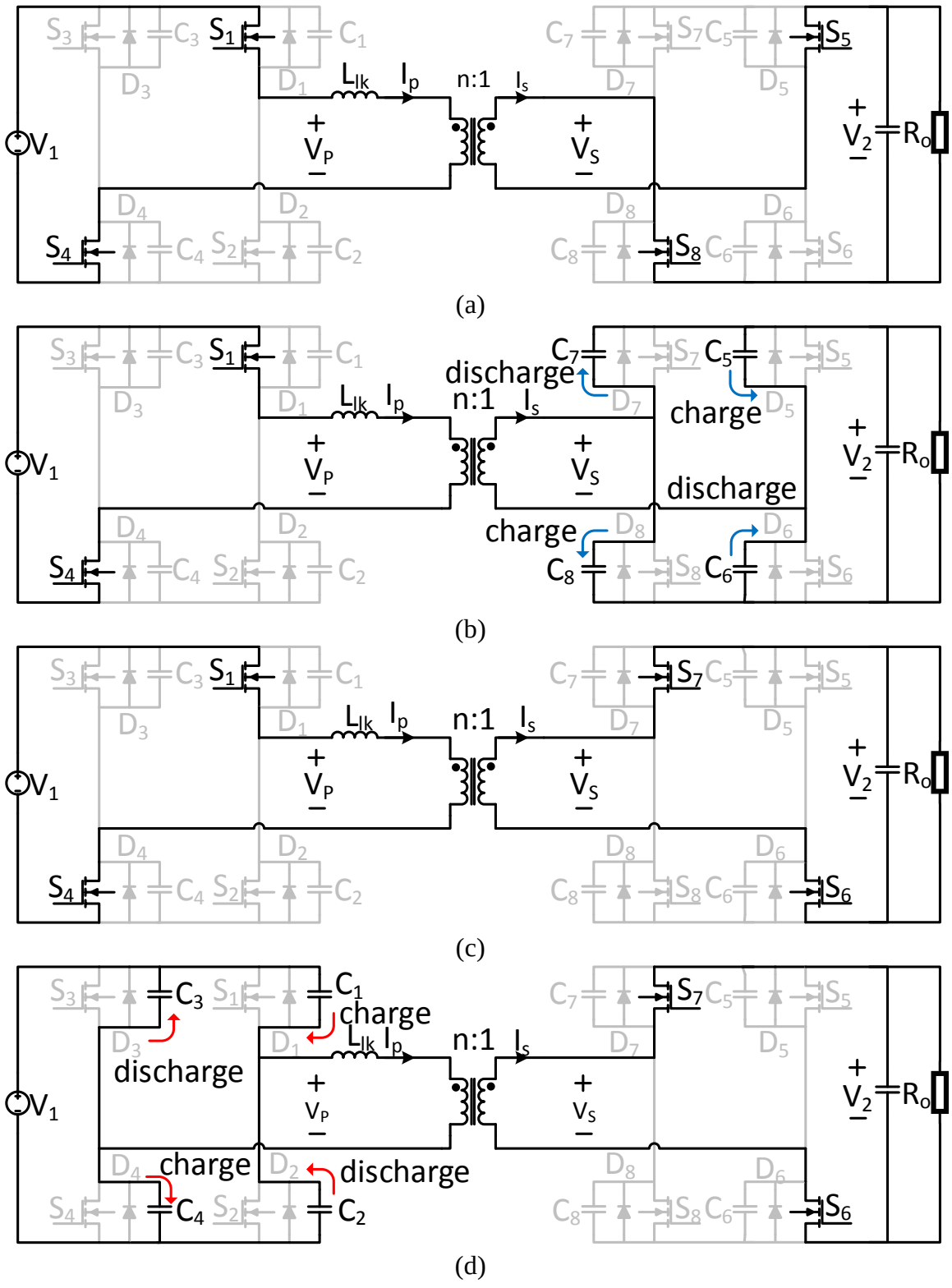



Figure 2.2. Equivalent circuit during dual active bridge converter operation for (a) Mode 1, (b) Mode 2, (c) Mode 3, and (d) Mode 4.

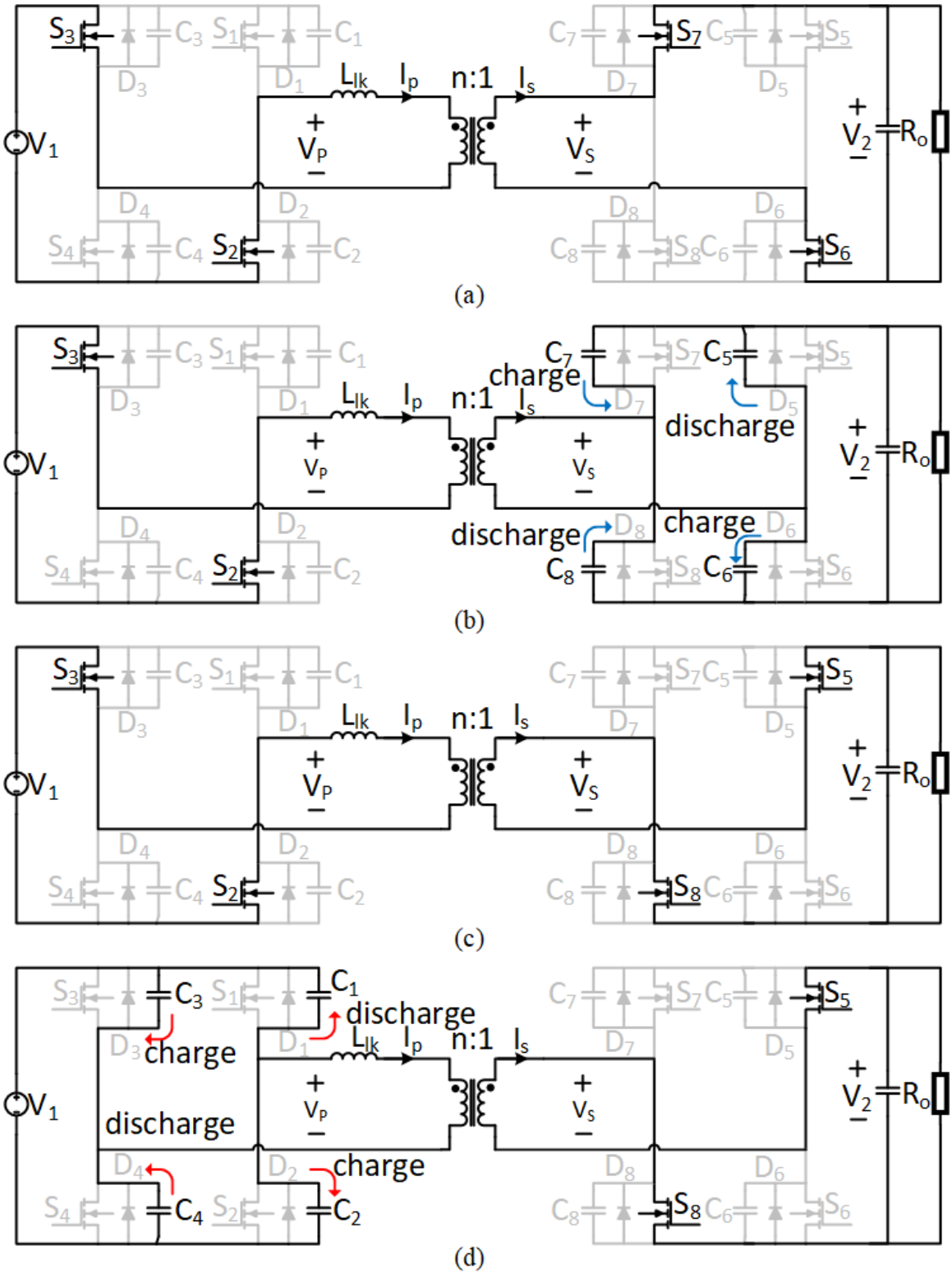



Figure 2.3. Equivalent circuit during dual active bridge converter operation for (a) Mode 5, (b) Mode 6, (c) Mode 7, and (d) Mode 8.

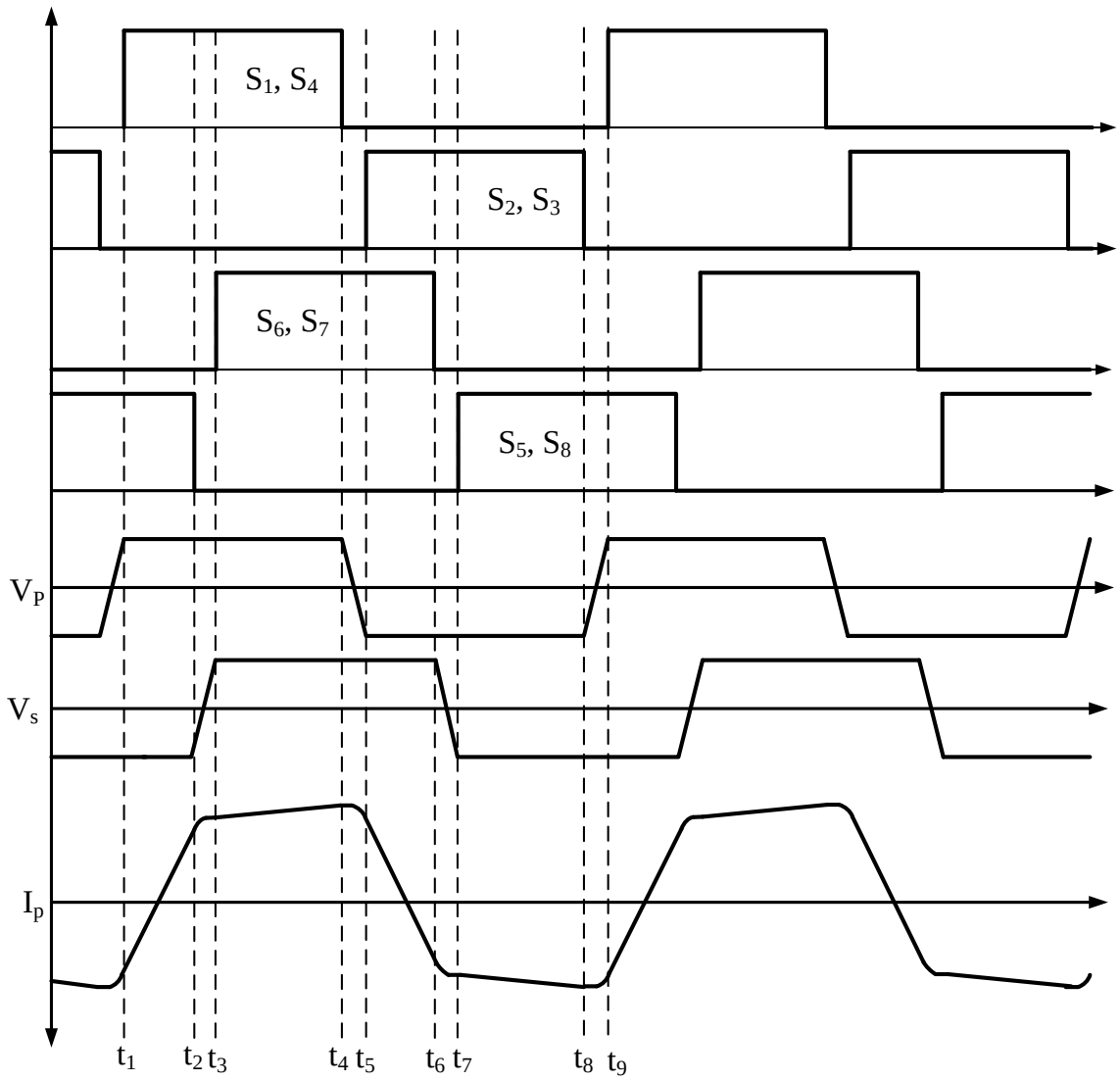



Figure 2.4. Converter operating waveforms for dual active bridge.

The CLLC resonant converter is another common topology used to achieve bidirectional DC/DC power conversion with galvanic isolation [25].The circuit diagram for the CLLC resonant converter is shown in Figure 2.5. The different equivalent under one complete switching cycles is shown in Figure 2.6. The converter waveforms under steady state operation is shown in Figure 2.7.

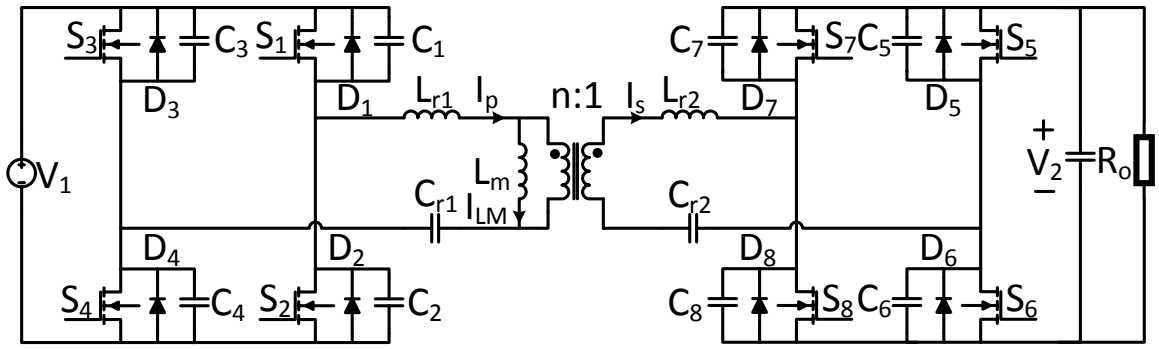



Figure 2.5. CLLC resonant converter.

The operation of the CLLC resonant converter (CLLC) during one complete switching cycle is discussed below.

Mode 1 [$t_1$-$t_2$]: At $t_1$, the MOSFETs $S_1$, $S_4$, $S_6$ and $S_7$ turn on. Power is transferred from the primary side to the secondary side. The bus voltage $V_1$ is applied across the magnetizing inductance $L_m$, hence the magnetizing inductor current $I_{LM}$ increases linearly. Inductors $L_{r1}$ and $L_{r2}$ resonate with capacitors $C_{r1}$ and $C_{r2}$. Therefore, the current flowing out of the secondary winding $I_s$ goes through half of a resonant cycle. The primary winding current $I_p$ also resonates until it reaches the peak magnetizing inductor current at $t_2$.

Mode 2 [$t_2$-$t_3$]: At $t_2$, the MOSFETs $S_1$, $S_4$, $S_6$ and $S_7$ turn off. The circuit enters the deadtime region. The energy stored in the magnetizing inductance ensures the current flowing through it is continuous. This current charges the equivalent MOSFET output capacitances $C_1$, $C_4$, $C_6$ and $C_7$ and discharges $C_2$, $C_3$, $C_5$ and $C_8$. If the charge and discharge of the these capacitances are complete before $t_3$, ZVS is achieved by MOSFETs $S_2$, $S_3$, $S_5$ and $S_8$ when they turn on. No power transfer between the primary side and secondary occurs during this time interval.

Mode 3 [$t_3$-$t_4$]: At $t_3$, the MOSFETs $S_2$, $S_3$, $S_5$ and $S_8$ turn on. The power is transferred from the primary side to the secondary side. The negative values of bus voltage

$V_1$ is applied across the magnetizing inductance $L_m$. As a result, the current $I_{LM}$ flowing through it decreases linearly. Inductors $L_{r1}$ and $L_{r2}$ resonate with capacitors $C_{r1}$ and $C_{r2}$.The current flowing out of the secondary winding $I_s$ goes through half of a resonant cycle in an opposite direction compared to Mode 1. The primary winding current $I_p$ also resonates until it reaches the minimum magnetizing inductor current at the instant $t_4$.

Mode 4 [$t_4$-$t_5$]: At $t_4$, the MOSFETs $S_2$, $S_3$, $S_5$ and $S_8$ turn off. The circuit again enters the deadtime region. The energy stored in the magnetizing inductance ensures the current flowing through it is continuous. This current charges the equivalent MOSFET output capacitances $C_2$, $C_3$, $C_5$ and $C_8$ and discharges $C_1$, $C_4$, $C_6$ and $C_7$. If the charge and discharge of these capacitances are complete before $t_5$, ZVS is achieved by MOSFETs $S_1$, $S_4$, $S_6$ and $S_7$ when they turn on. No power transfer between the primary side and secondary occurred during this time interval.

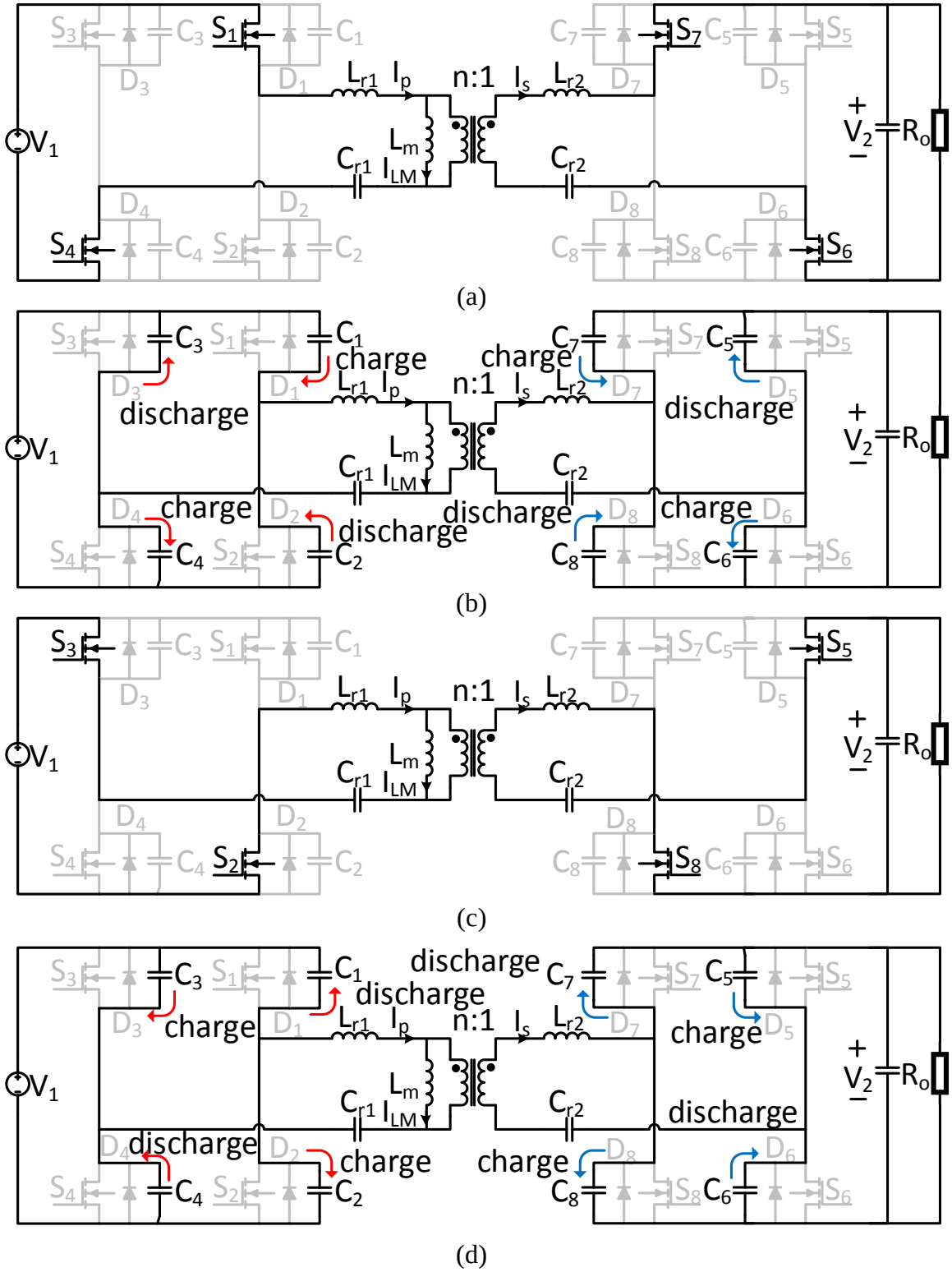



Figure 2.6. Equivalent circuit during CLLC converter operation for (a) Mode 1, (b) Mode 2, (c) Mode 3, and (d) Mode 4.

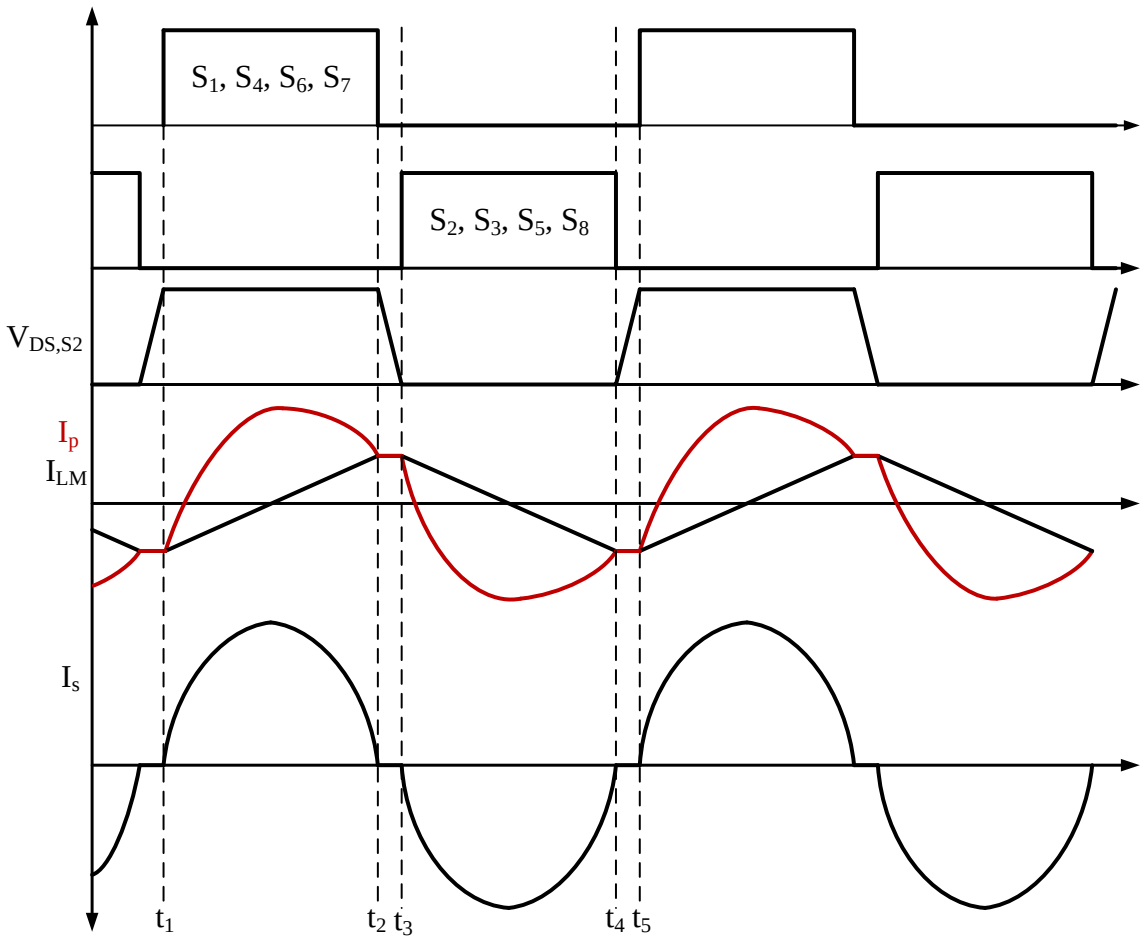



Figure 2.7. Converter operating waveforms for CLLC resonant converter.

## 2.3 Comparative Analysis of Bidirectional Isolated DC/DC Converter Topologies

In order to determine the most suitable topology for the given application, the optimal design at different switching frequencies need to be performed and the resulting total device loss shall be compared. Due to the symmetrical nature of both converter topologies, it would be reasonable to assume that an analysis based on power delivery from primary to secondary side would yield a trend that would also hold true for power delivery in the reverse direction.

Given that both DAB and CLLC converters achieve high efficiency through zero voltage switching, the optimal converter designs must satisfy this criterion. Therefore, as a first step in the design process, the charge-equivalent output capacitance of the device at the specified DC operating voltage need to be determined [26].

The small-signal junction capacitances at different DC operating voltage values for C3M0010090K and X3M0016120K are shown in Figure 2.8 and Figure 2.9 respectively. The total charge $Q_{oss}$ stored across the device is determined by integrating the area underneath $C_{oss}$ with respect to $V_{ds}$ up until the specified DC voltage. The formula is given by (1).

$$Q_{oss} = \int_0^{V_{DC}} C_{oss}(v_{ds}) dv_{ds} \quad (1)$$

Once the stored charge is determined, the charge-equivalent output capacitance is determined using the formula given by (2).

$$C_{oss,Q} = Q_{oss}/V_{DC} \quad (2)$$

The resulting charge-equivalent capacitance for C3M0010090K and X3M0016120K are 430 pF and 860 pF respectively.

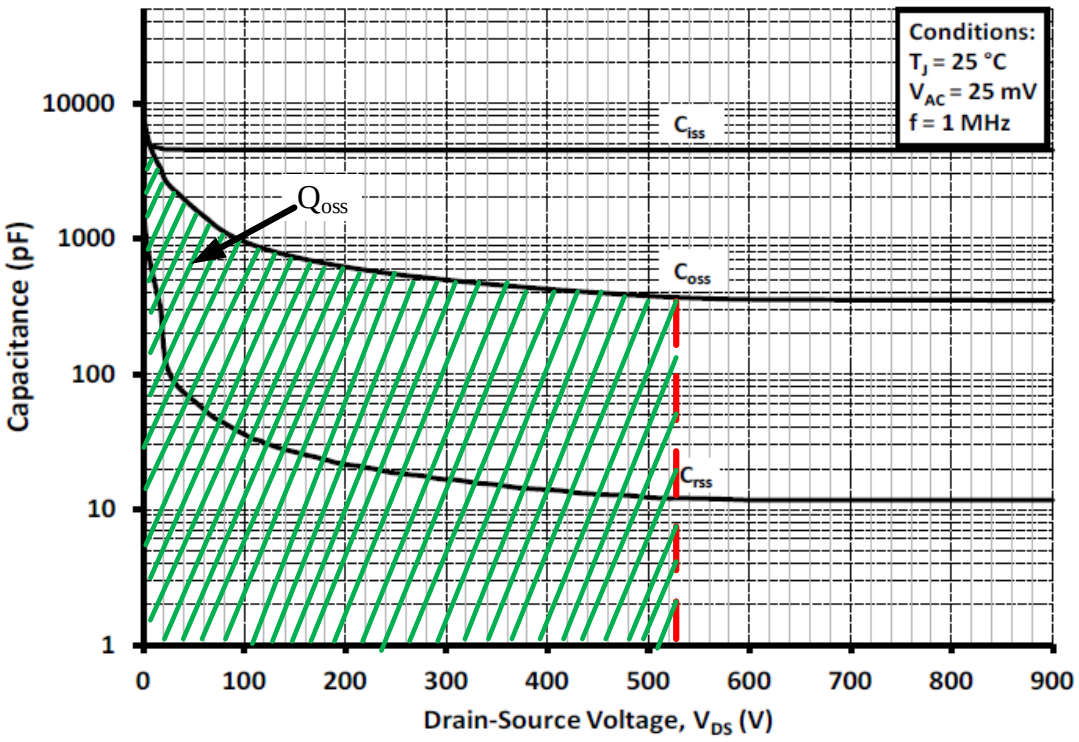



Figure 2.8. Output capacitance curve for C3M0010090K.

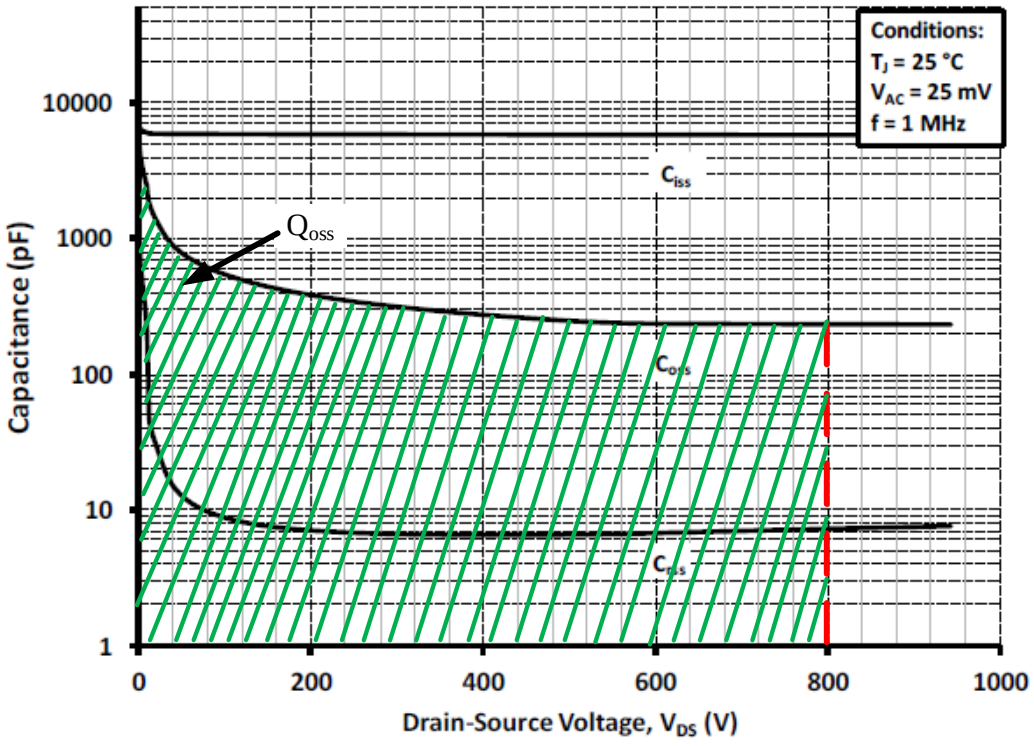



Figure 2.9. Output capacitance curve for X3M0016120K.

For the DAB converter, once the charge-equivalent output capacitance values are determined, the minimum required leakage inductance $L_{lk}$ is determined according to method outlined in [26].

The resulting converter parameters for DAB converter under different design cases are outlined in Table 2.3.

Table 2.3. Converter parameters for DAB converter under different design cases.

| DAB Parameter | **Case 1** | **Case 2** | **Case 3** | **Case 4** |
|---|---|---|---|---|
| Switching Frequency, $f_s$ (kHz) | 50 | 100 | 250 | 500 |
| Output Power (kW) | 25 | 25 | 25 | 25 |
| Transformer Turns Ratio, n | 1.5 | 1.5 | 1.5 | 1.5 |
| Leakage Inductance, $L_{lk}$ (µH) | 1 | 1 | 1 | 1 |
| Primary Magnetizing Inductance, $L_m$ (µH) | Inf. | Inf. | Inf. | Inf. |

The design process for the CLLC resonant converter similar to the one described in [27] begins with the determination of the optimal deadtime $t_d$. The formulae for primary winding rms current $I_{p,rms}$ and secondary winding rms current $I_{s,rms}$ are given by (3) and (4). As an example, the graphs of rms current in the primary winding and secondary winding at deadtime for a switching frequency of 250 kHz are shown in Figure 2.10 and Figure 2.11 respectively. It can be observed from the plot that the minimum rms current for both windings do not occur at the same deadtime. Hence the optimal deadtime to minimize the total conduction loss in the devices depends on the on-state resistance of the device in the converter.

$$I_{p,rms}(t_d) = \frac{I_o}{4\sqrt{2}n}\sqrt{\frac{64n^4 C_{oss} R_o^2}{t_d^2} + 4\pi^2 + \frac{16\pi^2(T_o t_d + t_d^2)}{T_o^2}} \qquad (3)$$

$$I_{s,rms}(t_d)$$

$$= \frac{\sqrt{6}I_o}{24\pi}\sqrt{\frac{64n^4(5\pi^2-48)C_{oss}^2R_o^2T_o}{t_d^2(T_o+2T_d)}+\frac{12\pi^4T_o}{T_o+2t_d}+\frac{48\pi^2(T_ot_d+t_d^2)}{T_o(T_o+2t_d)}} \quad (4)$$

The formula for total conduction loss in the devices is given by (5). The resulting plot for a switching frequency of 250 kHz is shown in Figure 2.12. It is shown that an optimal deadtime of 100 ns leads to the lowest total conduction loss in the devices. Although it is worth noting that the difference in total conduction loss in the devices changes by no more than 25 W for a deadtime ranging between 30 ns to 350 ns.

$$P_{cond} = 2I_{p,rms}^2R_{dson,p} + 2I_{s,rms}^2R_{dson,s} \quad (5)$$

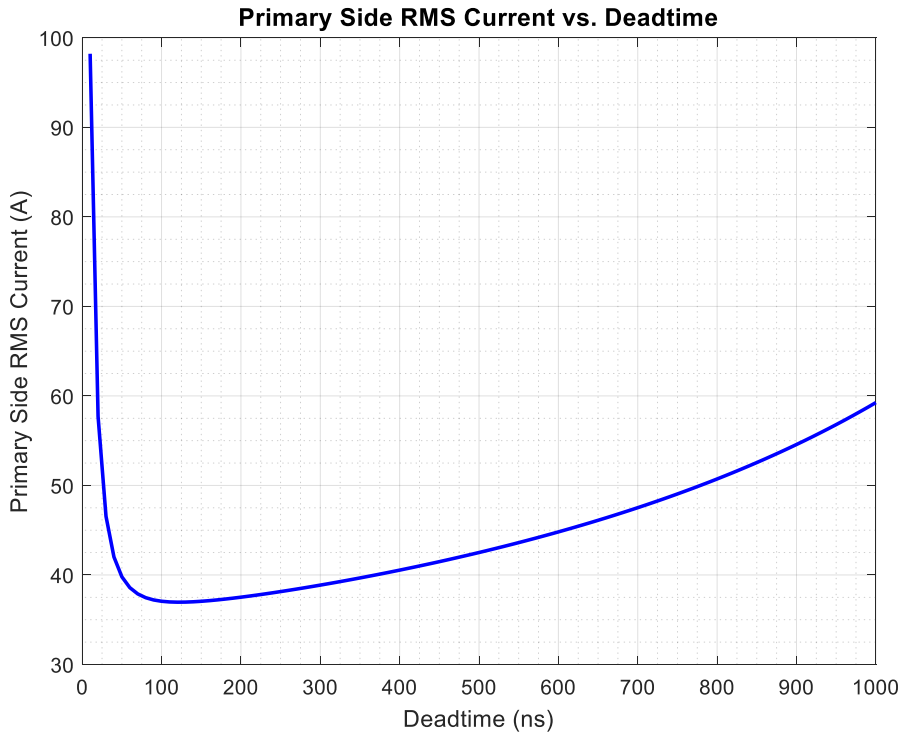



Figure 2.10. CLLC converter primary side RMS current vs. deadtime for $f_s$ = 250 kHz.

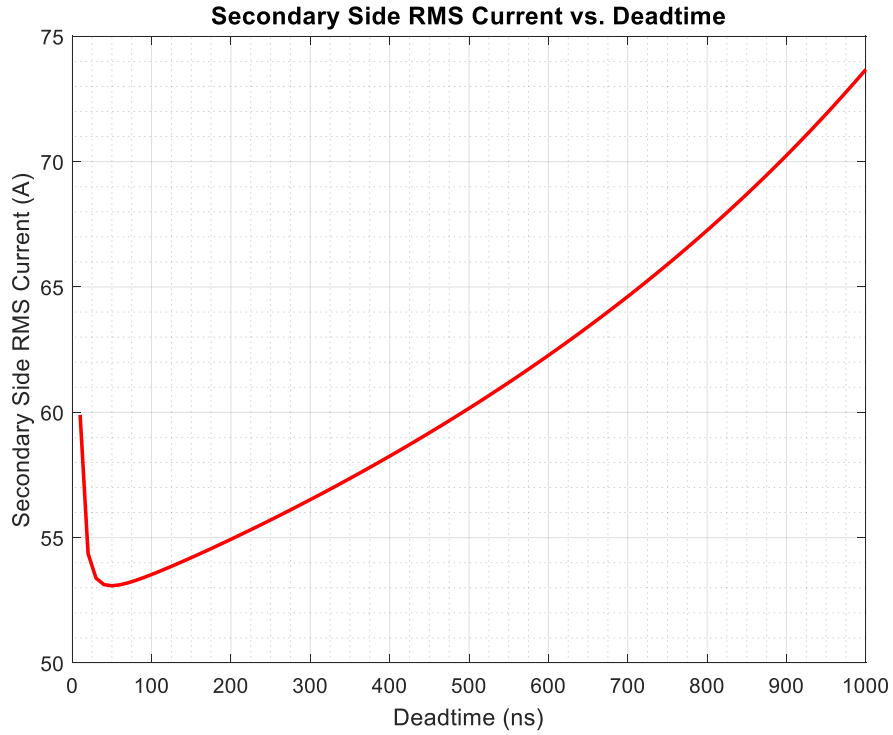



Figure 2.11. CLLC converter secondary side RMS current vs, deadtime for $f_s$ = 250 kHz.

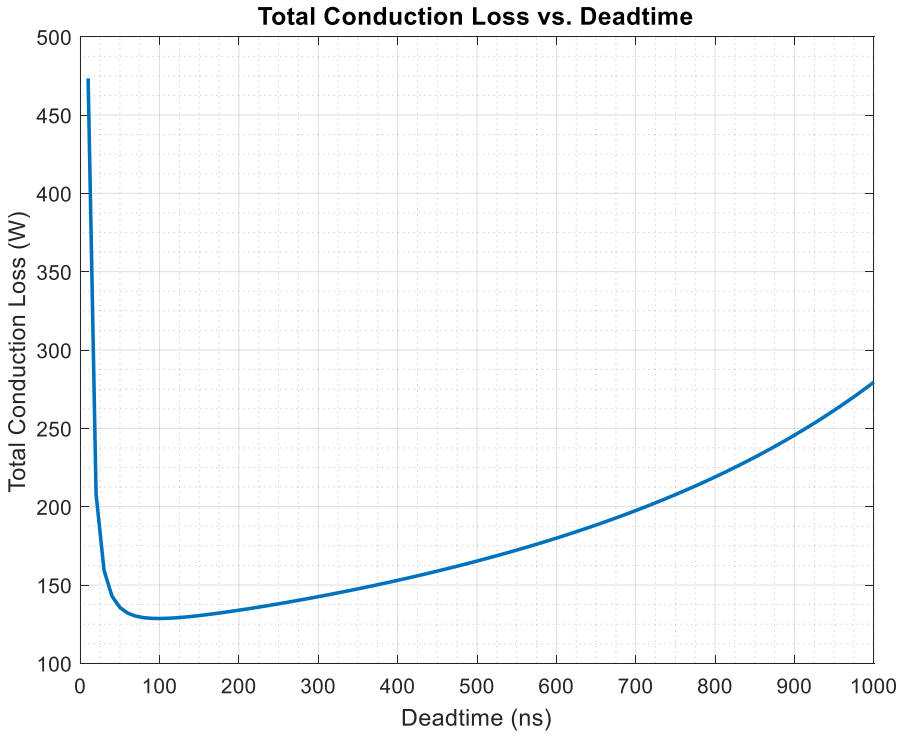



Figure 2.12. CLLC converter total conduction loss vs. deadtime for $f_s$ = 250 kHz.

Once the optimal deadtime known, the maximum allowable magnetizing inductance can be determined. This ensures that ZVS is achieved for all the devices in the converter across the entire load range. The formula is given by (6).

$$L_{M,max} \leq \frac{(T_s - 2t_d)t_d}{8(C_{oss,p} + \frac{C_{oss,s}}{n^2})} \tag{6}$$

Finally, the reactive elements in the CLLC resonant tank were calculated using the formulae shown below.

$$L'_{r2} = n^2 L_{r2} \tag{7}$$

$$C'_{r2} = \frac{C_{r2}}{n^2} \tag{8}$$

$$C_{eq} = \frac{C_{r1}C'_{r2}}{C_{r1} + C'_{r2}} \tag{9}$$

$$L_{eq} = L_{r1} + L'_{r2} \tag{10}$$

$$T_s = \frac{1}{f_s} \tag{11}$$

$$T_o = T_s - 2t_d \tag{12}$$

$$C_{eq} = \frac{1}{(2\pi f_o)^2 L_{eq}} \tag{13}$$

$$L_{r1} = L'_{r2} \tag{14}$$

$$C_{r1} = C'_{r2} \tag{15}$$

$$L_{eq} = 2L_{r1} \tag{16}$$

$$C_{eq} = \frac{C_{r1}}{2} \tag{17}$$

The resulting converter component values for CLLC resonant converter under different switching frequencies are outlined in Table 2.4.

Table 2.4. Converter parameters for CLLC converter under different design cases.

| CLLC Parameter | **Case 1** | **Case 2** | **Case 3** | **Case 4** |
|---|---|---|---|---|
| Switching Frequency (kHz) | 50 | 100 | 250 | 500 |
| Output Power (kW) | 25 | 25 | 25 | 25 |
| Transformer Turns Ratio, n | 1.5 | 1.5 | 1.5 | 1.5 |
| Primary Leakage Inductance, $L_{r1}$ (µH) | 6 | 2.2 | 0.5 | 0.20 |
| Secondary Leakage Inductance, $L_{r2}$ (µH) | 2.67 | 0.98 | 0.22 | 0.09 |
| Primary Resonant Capacitance, $C_{r1}$ (µF) | 1.62 | 1.08 | 0.73 | 0.43 |
| Secondary Resonant Capacitance, $L_{r2}$ (µF) | 3.65 | 2.44 | 1.65 | 0.98 |
| Primary Magnetizing Inductance, $L_m$ (µH) | 600 | 220 | 50 | 20 |

The simulated current for both DAB and CLLC resonant converters with a switching frequency of 50 kHz are shown in Figure 2.13. It can be observed that the primary and secondary rms current are higher for the CLLC resonant converter compared to the DAB converter. At any given power level, the average current flowing through the windings of the isolation transformer should be almost identical for both the dual active bridge and CLLC resonant converter. The shape of the transformer winding current is quasi-square for the dual active bridge and quasi-sinusoidal for the CLLC resonant converter. Quasi-sinusoidal waves have larger rms current compared to quasi-square waveforms. Therefore, it is within expectation that CLLC resonant converter has higher rms winding current values compared to DAB.

It can also be observed that the turn-off current in both the primary and secondary devices are higher for the DAB converter compared to the CLLC resonant converter. For the DAB converter, the devices turn off at the peak leakage inductor current values.

Whereas for the CLLC converter, the primary side turn-off current is determined purely by the peak magnetizing inductor current and the secondary device turn-off current is zero due to zero-current-switching (ZCS).

The total device loss for both the DAB and CLLC resonant converter for a switching frequency of 50 kHz are shown in Figure 2.14. The conduction loss in the device is higher for the CLLC resonant converter due to the larger rms current flowing through its windings. However, the switching loss in the device is much higher in the DAB converter due to the larger device turn-off current. The difference between the switching loss values for DAB and CLLC resonant converter is large enough such that larger total device loss is reported for the DAB even at 50 kHz switching frequency.

The simulated current for both the DAB and CLLC resonant converter under Case 2 are shown in Figure 2.15. The rms current in both the primary and secondary windings along with the device turn-off current remain relatively unchanged compared to Case 1. From the device loss data shown in Figure 2.16. It can be observed that due to the higher switching frequency, the switching loss in both converter increases. Also, the difference in total device loss between the DAB and CLLC resonant converter becomes much greater.

The simulated current and total device loss for both the DAB and CLLC resonant converter under Case 3 are shown in Figure 2.17 and Figure 2.18 respectively. The total device loss for both DAB converter and CLLC resonant converter are even higher compared to previously discussed cases due to the increased switching loss at higher switching frequencies. Similar trend can be found in the simulated current and total device loss for DAB and CLLC resonant converter under Case 4, which are shown in Figure 2.19 and Figure 2.20 respectively.

Based on simulated data across the range of switching frequencies, it can be determined that the total device loss for the CLLC resonant converter is higher than the DAB under the given specifications. Hence, the CLLC resonant converter is selected to achieve the galvanic isolation typically required in the bidirectional power distribution system.

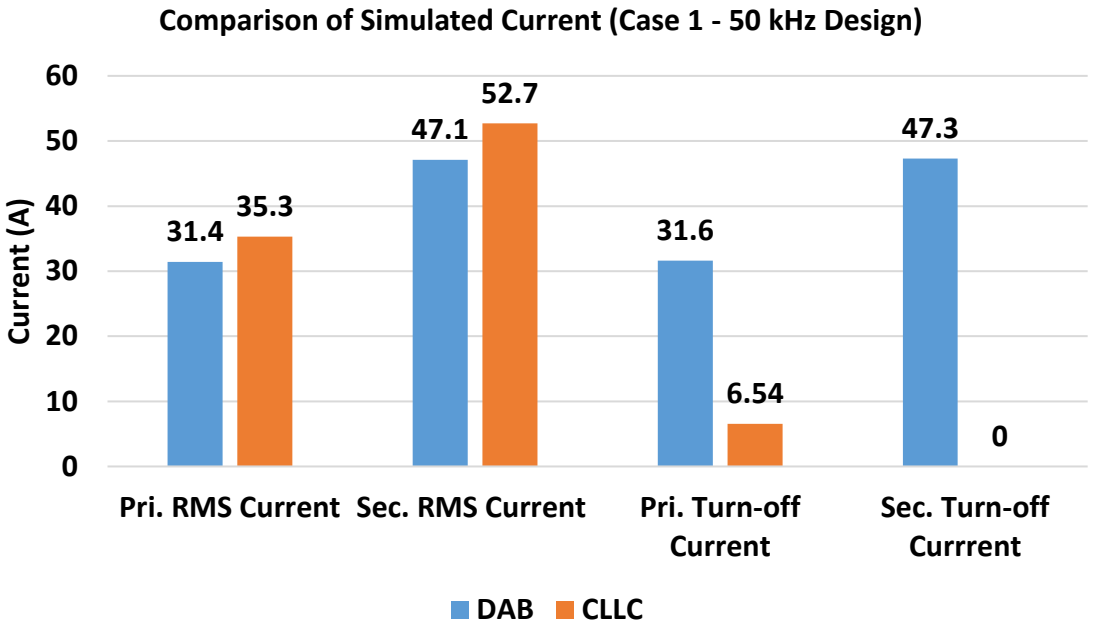



Figure 2.13. Comparison of simulated current for DAB vs. CLLC under Case 1.

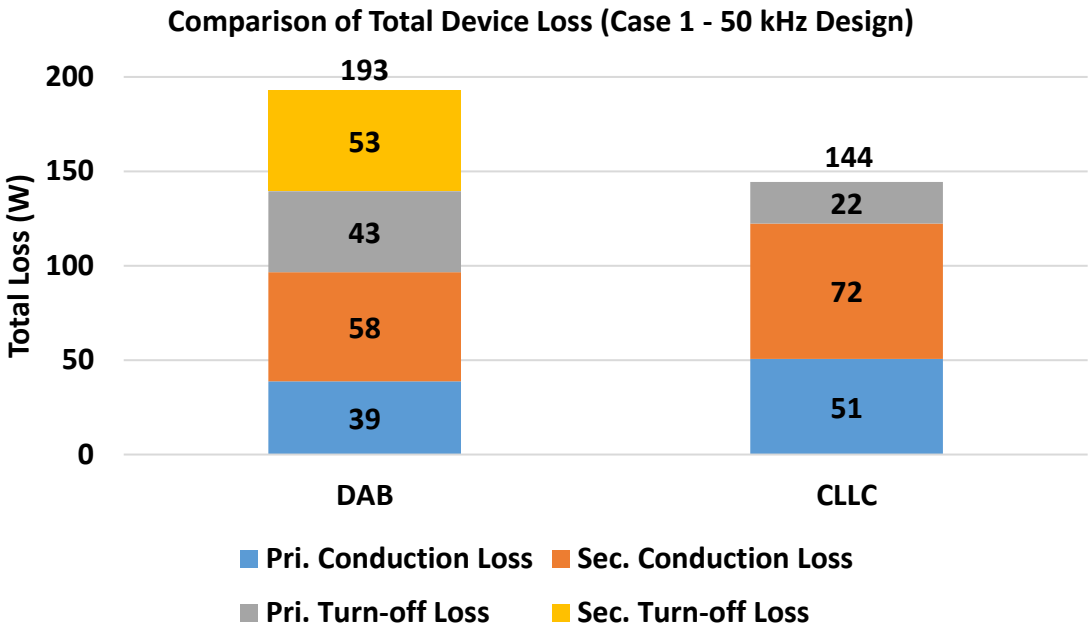



Figure 2.14. Comparison of total device loss for DAB vs. CLLC under Case 1.

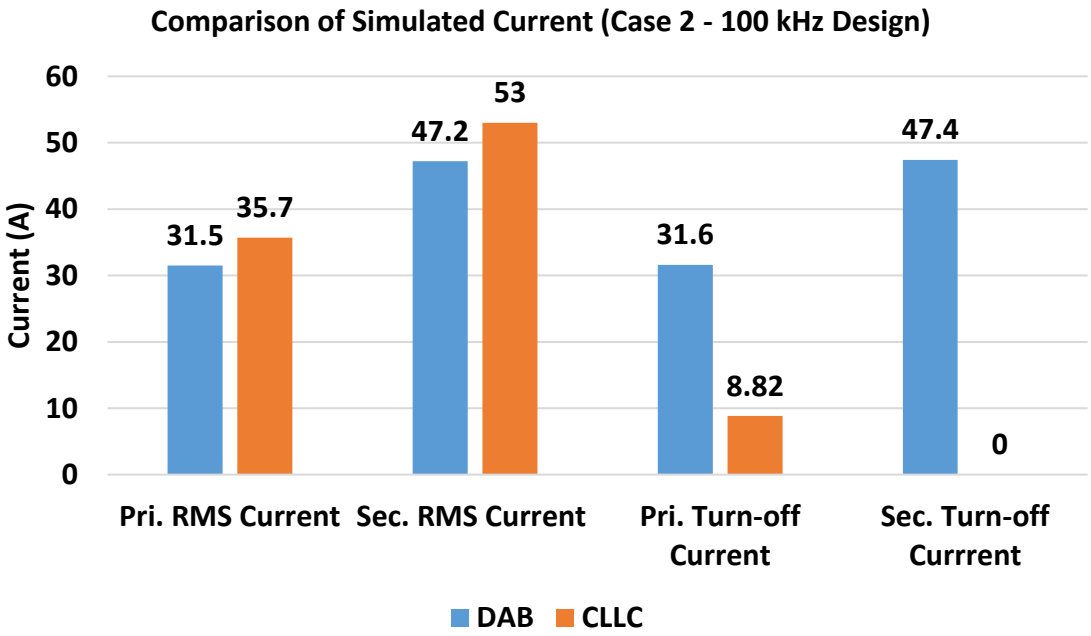



Figure 2.15. Comparison of simulated current for DAB vs. CLLC under Case 2.

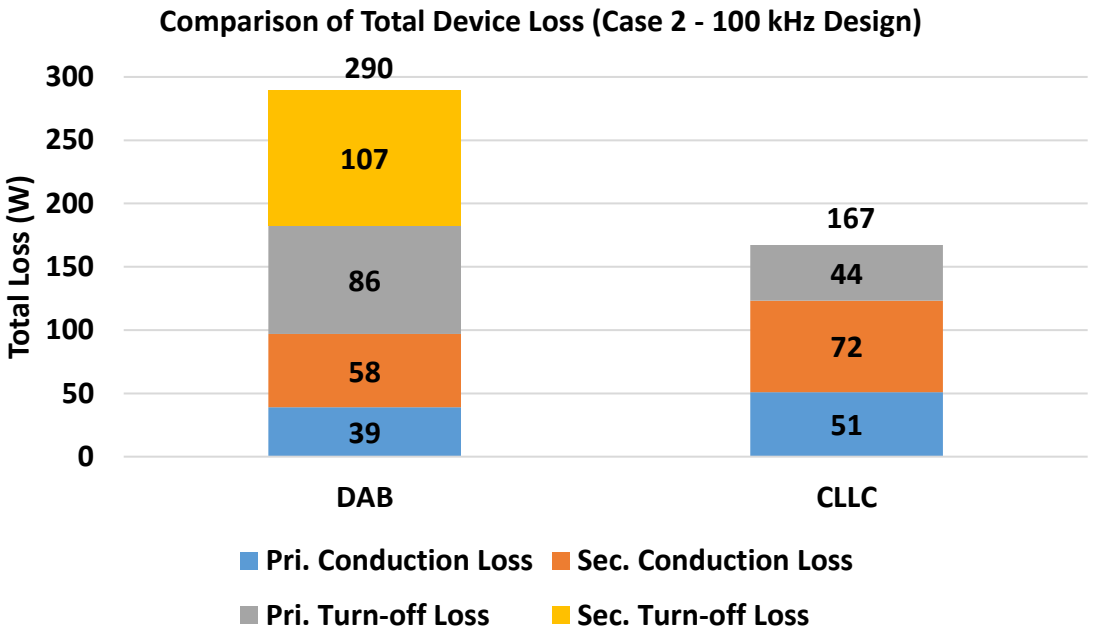



Figure 2.16. Comparison of total device loss for DAB vs. CLLC under Case 2.

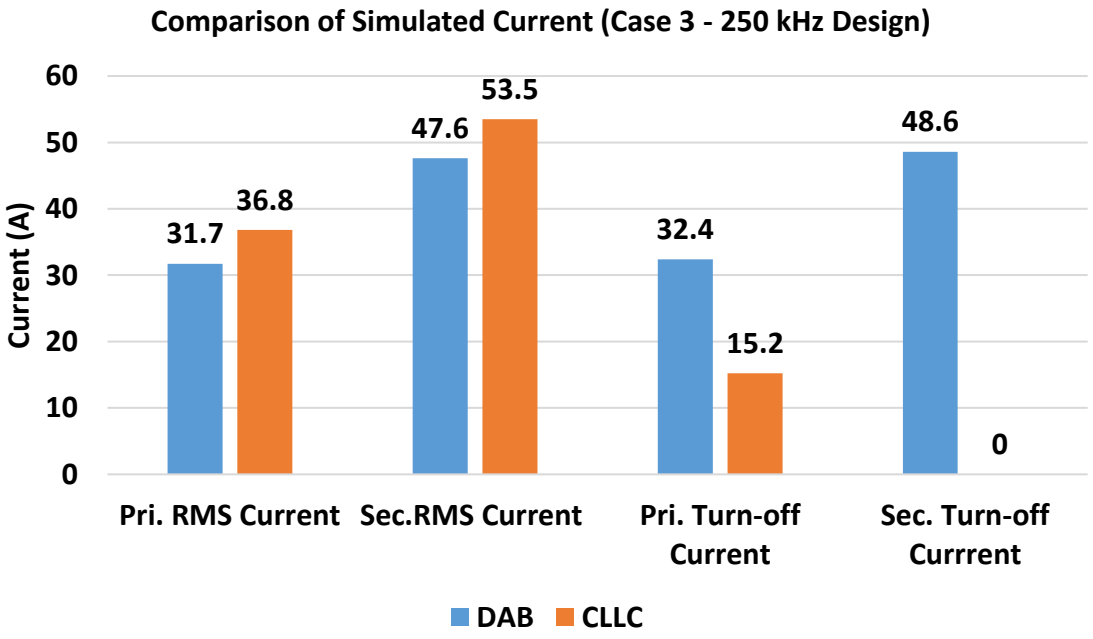



Figure 2.17. Comparison of simulated current for DAB vs. CLLC under Case 3.

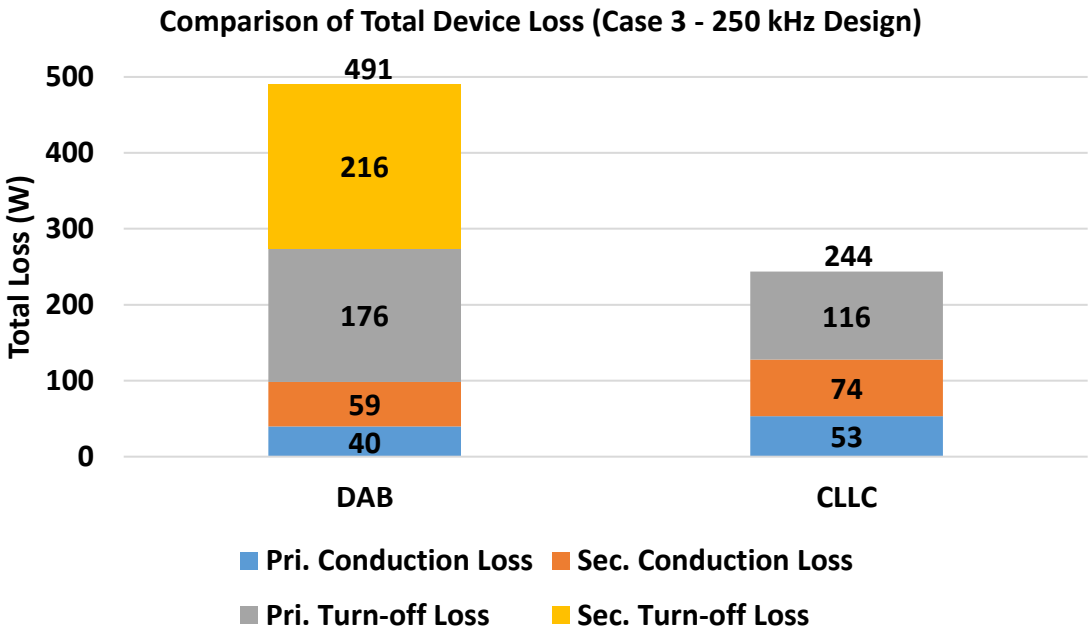



Figure 2.18. Comparison of total device loss for DAB vs. CLLC under Case 3.

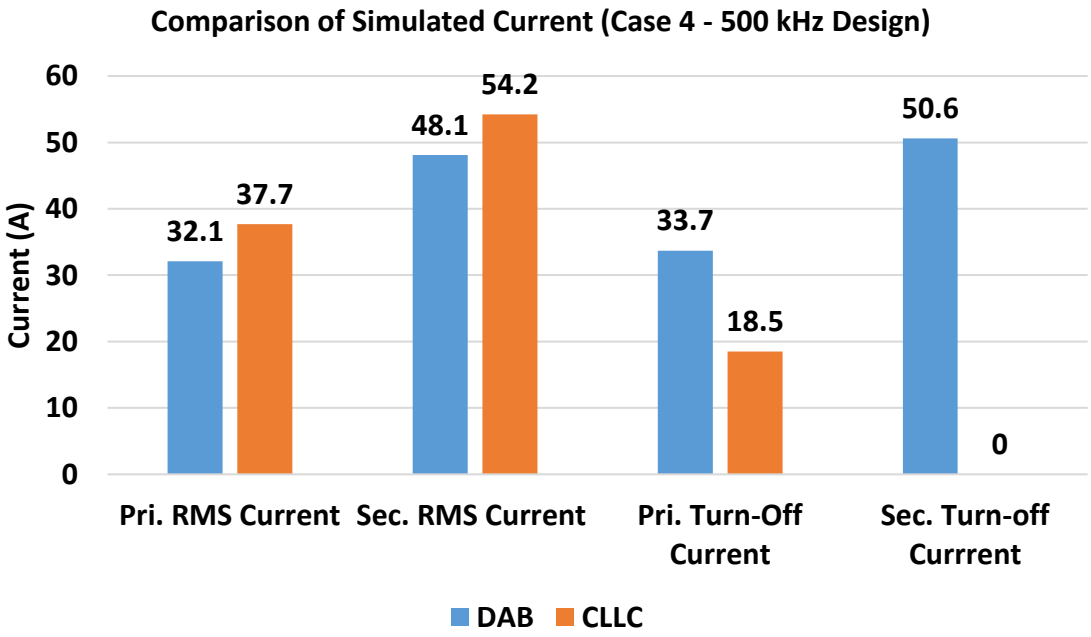



Figure 2.19. Comparison of simulated current for DAB vs. CLLC under Case 4.

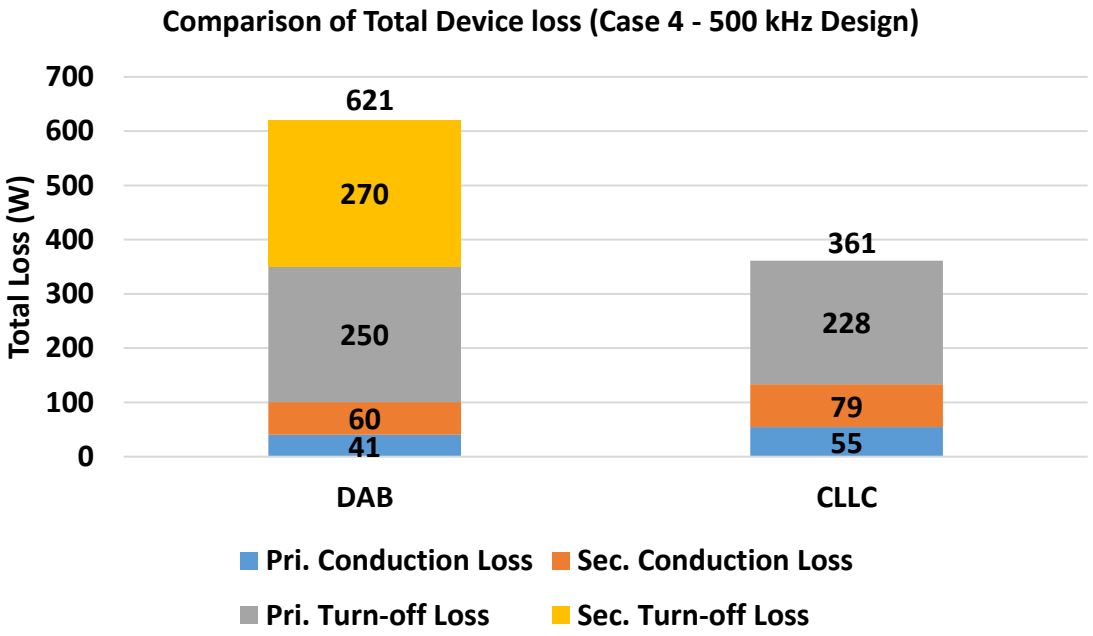



Figure 2.20. Comparison of total device loss for DAB vs. CLLC under Case 4.

The 2D drawing for the isolation transformer in the CLLC converter is shown in Figure 2.21. The core material for this isolation transformer is 3F36 from Ferroxcube. The transformer loss at different switching frequencies is outline in Table 2.5. The core loss data is obtained via the Steinmetz's equation model provided in the material datasheet. The winding loss data is based on simulation model built by the transformer manufacturer. Given that the saturation magnetic flux density, $B_{sat}$ for the 3F36 core material is exceeded at 50 kHz, no winding loss and core loss data is determined at this frequency.

Table 2.5. Transformer loss breakdown.

| Transformer Parameter | **Case 1** | **Case 2** | **Case 3** | **Case 4** |
|---|---|---|---|---|
| Switching Frequency (kHz) | 50 | 100 | 250 | 500 |
| Core Material | 3F36 | 3F36 | 3F36 | 3F36 |
| Saturation Magnetic Flux Density, $B_{sat}$ (T) | 0.42 | 0.42 | 0.42 | 0.42 |
| Effective Cross-Sectional Area, $A_e$ ($mm^2$) | 540 | 540 | 540 | 540 |
| Effective Core Volume, $V_e$ ($mm^3$) | 79800 | 79800 | 79800 | 79800 |
| Magnetic Flux Density, $\Delta B$ (T) | 0.618 | 0.309 | 0.123 | 0.062 |
| Core Loss Density ($W/mm^3$) | 0.00229 | 0.00229 | 0.00043 | 0.00016 |
| Core Loss (W) | N/A | 182 | 34 | 13 |
| Winding Loss (W) | N/A | 50 | 64 | 93 |
| Total Transformer Loss (W) | N/A | 232 | 98 | 106 |

The total converter loss at 100 kHz. 250 kHz and 500 kHz are shown in Figure 2.22. The transformer core loss decreases with switching frequency and the winding loss increases with switching frequency. The resulting total converter loss is lowest at the switching frequency of 250 kHz. This shall be the operating frequency for the 25 kW CLLC resonant converter prototype discussed in subsequent chapters.

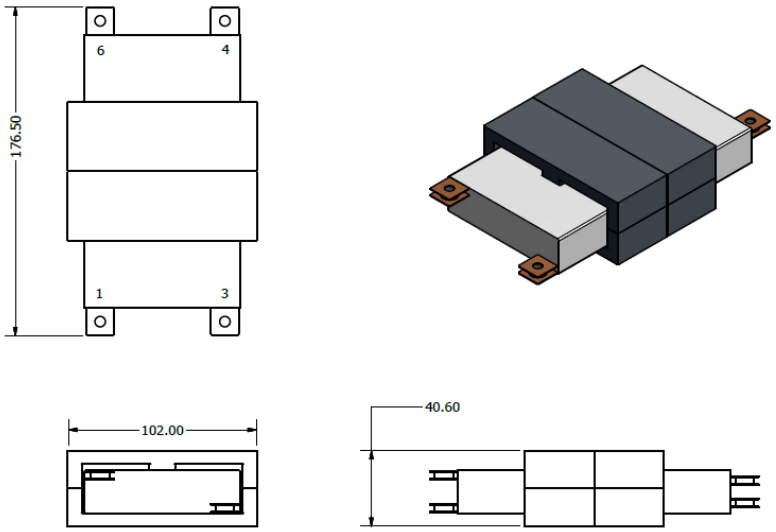



Figure 2.21. Mechanical drawing of isolation transformer for CLLC resonant converter.

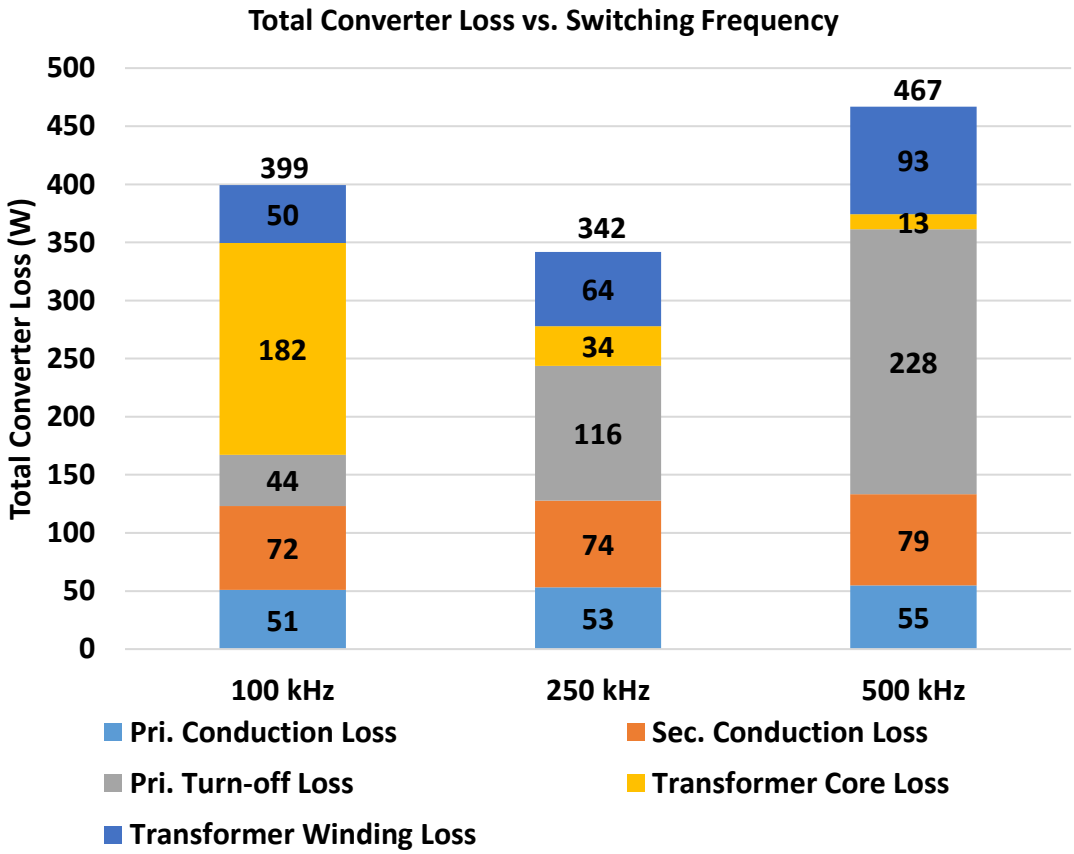



Figure 2.22. Total CLLC converter loss vs. switching frequency.

# Chapter 3 CLLC Resonant Converter Design

## 3.1 Gate Driver Circuit Design

The design of a high-performance and reliable gate driver is crucial in obtaining proper operation of the overall converter. There are several factors in designing gate-driver for SiC MOSFETs that must be considered during the design process to achieve the desired performance for the converter.

At high switching frequencies, a mismatch in the propagation delay between rising edge and falling edge of the gate-driver output signal will result in a large deviation in the effective dutycycle.

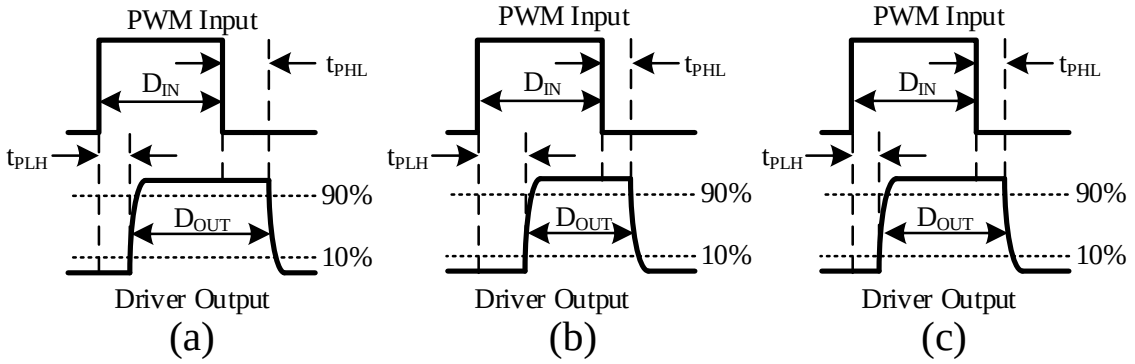



Figure 3.1. Effect of mismatch in propagation delay on gate-driver output for Case 1 (a) $t_{PLH} < t_{PHL}$, Case 2 (b) $t_{PLH} > t_{PHL}$ and Case 3 (c) $t_{PLH} = t_{PHL}$.

A rising edge in the gate-driver output with smaller propagation delay than the one in the falling edge is present in Case 1. This results in a larger effective dutycycle in the driver output signal compared to the command signal. If the effective dutycycle exceeds 50%, there would be a duration of time within each switching period where both devices in a phase leg would conduct. A large shoot-through current would then flow into the

phase-leg. As a result, additional losses would occur which could potentially destroy the devices.

In Case 2 the propagation delay in the rising edge is larger than the one in the falling edge, hence the effective dutycyle in the driver output signal is smaller than the command signal. A smaller effective dutycycle means that for the same switching period, the time allowed for energy transfer between the primary and secondary sides of the converter is reduced. As a result, at a given output power level, the rms current flowing through the devices will be greater, which leads to higher conduction loss.

Case 3 represents the ideal case where the propagation delay in the rising edge is equal to the propagation delay in the falling edge. Under this case, there is no deviation in the effective output dutycycle compared to the dutycycle of the command signal.

Additionally, due to the fast switching action involved at 250 kHz, it is also crucial to select a gate driver with a high common-mode transient immunity (CMTI). Static CMTI is typically defined as the largest dv/dt between the voltage rails on each side of the gate-driver IC, with inputs held either high or low such that the output of the gate driver IC would still remain at the expected logic level.

The list of commercially available gate-driver ICs is outlined in Table 3.1 and Table 3.2. The gate-driver IC from Analog Devices (ADuM4136) was selected for its performance in terms of CMTI, rise and fall times, peak gate current capability and pulse-width distortion

Table 3.1. List of commercial gate-driver ICs.

| | **1ED020I12-B2** | **ISO5851** | **ADuM4136** |
|---|---|---|---|
| Manufacturer | Infineon | Texas Instruments | Analog Devices |
| Package | PG-DSO-16-15 | SOIC-16 | SOIC-16 |
| Max. Output Positive Supply, $V_{CC2}$ (V) | 20 | 35 | 35 |
| Mini. Output Negative Supply, $V_{EE2}$ (V) | -12 | -17.5 | -15 |
| Peak Current Capability (A) | 2 (source)<br>2 (sink) | 2.5 (source)<br>5 (sink) | 4 (source)<br>4 (sink) |
| Turn-on Propagation Delay, $t_{PLH}$ (ns) | 195 | 110 | 68 |
| Turn-off Propagation Delay, $t_{PHL}$ (ns) | 190 | 110 | 68 |
| Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$ (ns) | 20 | 20 | 15 |
| Output Rise Time (10%-90%), $t_r$ (ns) | 60<br>@$C_{LOAD}$ = 1 nF | 35<br>@$C_{LOAD}$ = 1 nF | 22.9<br>@ $C_L$ = 2 nF |
| Output Fall Time (90%-10%), $t_f$ (ns) | 90<br>@$C_{LOAD}$ = 1 nF | 37<br>@$C_{LOAD}$ = 1 nF | 22.9<br>@ $C_L$ = 2 nF |
| Soft Turn-Off Scheme | TLTO | N/A | LRTO |
| Transient Voltage Rating, $V_{IOTM}$ (V) | 6000 | 8000 | 8000 |
| Common Mode Transient Immunity (kV/μs) | 50 | 100 | 100 |

Isolated power supplies are required for the gate-driver ICs. One important criteria in selecting the appropriate power supply is the required output power. The isolated power supply needs to provide enough power for both charging and discharging the MOSFET gate capacitances. but also the isolated side of the gate driver IC. The formula to determine the required power rating is given by . The required power from the isolated power supply is outlined in Table 3.3.

$$P_{DRV} = Q_g \Delta V_{gs} f_s + P_{Driver} \quad (18)$$

Another important specification for the isolated power supply is the output voltage rail. The recommended values for turn-on and turn-off gate voltage of the device need to be met.

Table 3.2. List of commercial gate-driver ICs (continued).

| | ISO5452 | STGAP1AS | BM6104FV-C |
|---|---|---|---|
| Manufacturer | Texas Instruments | ST Microelectronics | Rohm |
| Package | SOIC-16 | SO-24W | SSOP-B20W |
| Max. Output Positive Supply, $V_{CC2}$ (V) | +35 | +40 | +30 |
| Min. Output Side Negative Supply, $V_{EE2}$ (V) | -17.5 | -15 | -15 |
| Peak Current Capability (A) | 2.5 (source)<br>5 (sink) | 5 (source)<br>5 (sink) | 5 (source)<br>5 (sink) |
| Turn-on Propagation Delay, $t_{PLH}$ (ns) | 110 | 130 | 115 |
| Turn-off Propagation Delay, $t_{PHL}$ (ns) | 110 | 130 | 115 |
| Pulse Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$ (ns) | 20 | 10 | 20 |
| Output Rise Time (10%-90%), $t_r$ (ns) | 35<br>@$C_{LOAD}$ = 2 nF | 25<br>@$C_{LOAD}$ = 2 nF | 50<br>@$C_{LOAD}$ = 10 nF |
| Output Fall Time (90%-10%), $t_f$ (ns) | 37<br>@$C_{LOAD}$ = 2 nF | 25<br>@ $C_{LOAD}$ = 1 nF | 50<br>@$C_{LOAD}$ = 10 nF |
| Soft Turn-Off Scheme | LRTO | TLTO | TLTO |
| Transient Voltage Rating (V) | 8000 | 4000 V | 2500 V |
| Common Mode Transient Immunity (kV/μs) | 100 | 50 | 100 kV/us |

Table 3.3. Requirements for Gate Driver Power Supply

| Parameter | X3M0016120K | C3M0010090K |
|---|---|---|
| Positive Gate Drive Voltage (V) | +15 | +15 |
| Negative Gate Drive Voltage (V) | -4 | -4 |
| Gate Charge (nC) | 227 | 222 |
| Required Drive Power per Device @ 250 kHz (W) | 1.08 | 1.05 |
| Gate-Driver IC Power Requirement @250 kHz (W) | 0.2 | 0.2 |
| Power Required from Gate-Driver Power Supply (W) | 1.28 | 1.25 |

Finally, due to the large dv/dt induced by the switching action of the device, leakage current may travel through the isolation barrier of the isolated power and disrupt the driving logic signal [28]. Therefore, it is important to select the isolated power supply with a small isolation capacitance.

A list of commercial isolated power supplies is shown in Table 3.4. The dual output isolated power supply R24P21503D from Recom was selected as it has the desired output voltage levels. No further processing circuitry is required to split the output voltage into the required levels. Also, it has a reasonably low isolation capacitance of 10 pF,

Table 3.4. List of Commercial Isolated Power Supplies.

| | MGJ2D241505SC | R24P21503D | THB 3-2415 |
|---|---|---|---|
| Manufacturer | Murata | Recom | Traco Power |
| Package | 7-SIP | 7-SIP | DIP-24 |
| Min. Input Voltage (V) | 21.6 | 21.6 | 18 |
| Max. Input Voltage (V) | 26.4 | 26.4 | 36 |
| Nom. Input Voltage (V) | 24 | 24 | 24 |
| Output Power (W) | 2 | 2 | 3 |
| Number of Output | 2 | 2 | 1 |
| Ch. 1 Output Voltage (V) | 15 | 15 | 24 |
| Ch. 2 Output Voltage (V) | -5 | -3 | N/A |
| Ch. 1 Output Current (mA) | 80 | 93 | 125 |
| Ch. 2 Output Current (mA) | 40 | 185 | N/A |
| Efficiency (%) | 80.5 (typ.) | 82 (typ.) | 84 (typ.) |
| Operating Temp. (°C) | -40 to 100 | -40 to 95 | -40 to 85 |
| Isolation Voltage (kV) | 5.2 | 5.2 | 4.8 |
| Isolation Capacitance (pF) | 2.7 (typ.) | 10 (max.) | 13 (max.) |

The potential short-circuit conditions for the device are also considered during the gate-driver design process. There are two potential cases under which a short-circuit condition can occur [29]. One of which is commonly referred to as "fault under load" (FUL), where the load is shorted out while the device is still conducting. The other case involves the device turning on to form a short-circuit and is commonly referred to as "hard switched fault". Under both short-circuit conditions, the device is subjected both large voltage across its drain and source terminals while a large current is flowing along it. The resulting thermal dissipation could destroy the device. Therefore, it is important that the gate-driver circuitry is designed to detect device short-circuit conditions in a timely manner and perform the necessary shutdown sequence.

For fault under load, the MOSFET is initially turned-on and conducting load current. The load is then shorted out and the current flowing through the device increases rapidly, pulling the MOSFET into the saturation region. The voltage across the drain and source terminals would rise. This dv/dt induces a current flowing along the Miller capacitance that increases the voltage across the gate and source terminals. This voltage has a dominant effect on the current flowing through the device in the saturation region. Hence the short-circuit current increases with the gate to source voltage. The rise of the voltage across the drain and source terminals would eventually taper out, and the gate voltage would then decrease from its peak value. Consequently, the short-circuit current would reach a value determined by the characteristics of the device.

Under hard switched fault, the full DC-bus voltage appears across the MOSFET device before it is turned on. When the MOSFET is turned on, its drain current increases at a rate influenced by the junction capacitances and the slew rate of the gate-driver output.

A drop below the DC-bus voltage would then appear across the drain and source terminals, due to the stray resistive and inductive elements in the commutation path. The short-circuit current is removed when the MOSFET is turned off.

Under hard-switched fault conditions, the dv/dt appearing across the drain and source terminals of the device tend to be relatively small. So there is almost no additional increase in the voltage across the gate and source terminals due to the Miller effect. Therefore, the peak magnitude of short-circuit current under hard switched fault condition tend to be smaller than the one under fault under load condition.

Under both short-circuit conditions, the MOSFET device is no longer operating in the linear region but enters the saturation mode instead. Therefore, the desaturation detection techniques used to determine the occurrence of short-circuit conditions of IGBTs can also be used for MOSFETs.

The high-level implementation of desaturation detection circuitry in most commercial gate-driver ICs is shown in Figure 3.2. The diode $D_{DESAT}$ blocks the DC bus voltage when the device is in its off state. It is essential that this diode has a low junction capacitance and small reverse recovery time.

During turn-on transients of the freewheeling diode that is in parallel with the MOSFET device, a negative voltage can appear across the DESAT pin and ground reference of the gate-driver IC. A relatively large current could flow out of the DESAT pin and damage the gate-driver IC. The resistor $R_{DESAT}$ is then selected to limit the current draw under this condition.

The Zener diode $D_Z$ provides an additional voltage drop $V_{DZ}$ in series with $D_{DESAT}$ such that the effective threshold for the voltage $V_{DS}$ under short-circuit conditions can be adjusted. The resulting voltage across the DESAT pin is given by (19).

$$V_{DESAT} = V_{DS} + V_{DZ} + V_D + V_R \tag{19}$$

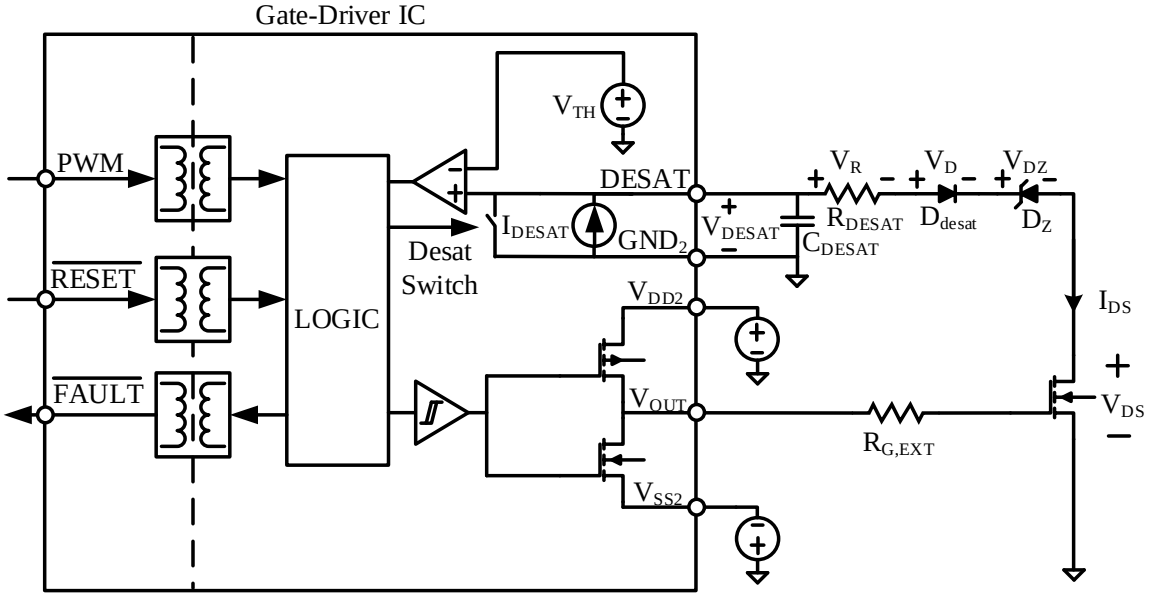



Figure 3.2. High-level diagram for desat detection circuitry.

A signal timing diagram during a short-circuit event with the selected gate driver IC (ADuM4136) is shown in Figure 3.3. Initially, when the PWM input to the gate-drive IC is low, the output is also low. The desat switch is conducting hence a negligible voltage appears at the DESAT pin. Both FAULT and RESET signals are pulled high.

When the input to the gate driver changes from the initial low state to a high state, the output also changes from low to high. After a delay $T_{DS,\,DELAY}$ of 300ns, the desat switch turns on. The current from the constant current source $I_{DESAT}$ flows into the MOSFET device.

When a short-circuit event occurs, the MOSFET device enters the saturation region and the voltage across its drain and source terminals $V_{DS}$ start to rise. When the sum of $V_{DS}$

and the voltage drop across the Zener diode exceeds the voltage at the DESAT pin, the diode $D_{DESAT}$ would be reverse biased and $I_{DESAT}$ will flow into $C_{DESAT}$ instead. The time $T_{BLANK}$ for which it takes to charge $C_{DESAT}$ is given by (20).

$$T_{BLANK} = \frac{C_{DESAT} V_{TH}}{I_{DESAT}} \tag{20}$$

After this blanking time $T_{BLANK}$ has passed, the capacitor $C_{DESAT}$ is charged to the threshold voltage $V_{TH.}$ The output of the gate-driver IC then goes to low regardless of the input with a propagation delay $T_{DESAT,\ PHL}$ that is less than 300 ns. The minimum time between the occurrence of a short-circuit event and the gate-driver IC changing its output to low is given by (21).

$$T_{shutdown} = T_{DS_{DELAY}} + T_{BLANK} + T_{DESAT,PHL} \tag{21}$$

There is a minimum delay $T_{REPORT}$ of 2 µs from the time $V_{DESAT}$ exceeds $V_{TH}$ and the time when FAULT pin is pulled low by the gate-driver IC. Therefore, the minimum time between the occurrence of a short-circuit event and the notification being sent to the system controller is given by (22).

$$T_{ctrl,delay} = T_{DS_{DELAY}} + T_{BLANK} + T_{REPORT} \tag{22}$$

To resume normal operation after the FAULT signal has been pulled low. The RESET pin needs to be pulled low for a minimum duration $T_{RESET}$ to clear the FAULT flag. After the FAULT flag is cleared and RESET signal goes back to high, the gate driver IC assumes normal operation where the driver output follows the PWM input.

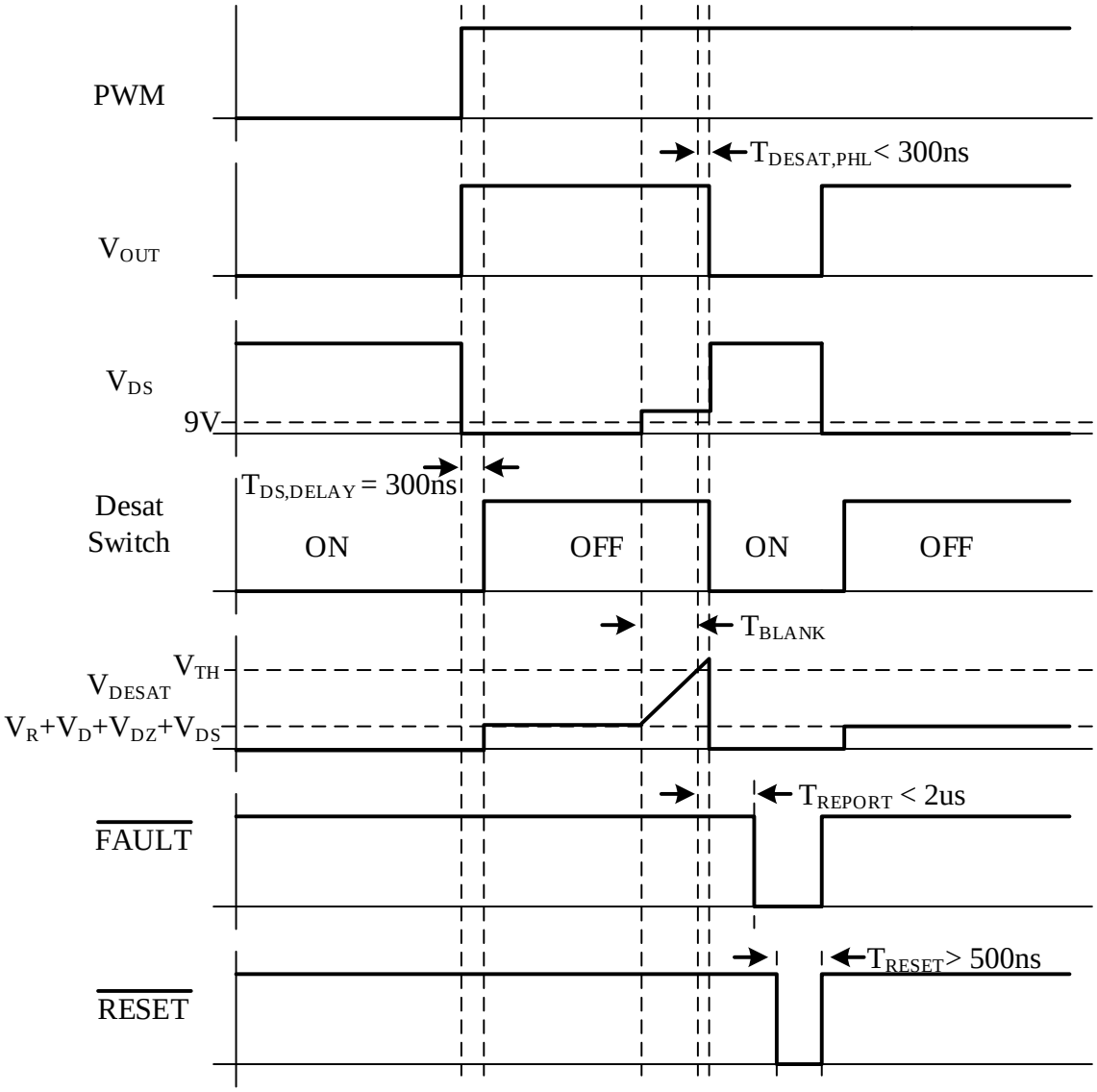



Figure 3.3. General timing diagram for desat detection circuitry.

The effect of crosstalk introduced by the fast dv/dt transition of the devices also need to be considered [30]. The switching sequence for a single-phase leg with load current flowing out of the phase-leg is illustrated in Figure 3.4.

Initially, the lower device is off and upper device is carrying the load current, the full bus voltage is applied across the lower device. When the upper device is being turned off, there is a dv/dt appearing across the drain and source terminals of both devices. The voltage across the upper device rises and while the voltage across lower device falls. The

negative dv/dt across the lower device induces current flow along its Miller capacitance. This current is in a direction such that the voltage across the gate and source terminals become more negative. The voltage appearing across the gate to source terminal of the lower device is given by (23). The voltage drops $V_{RGL,EXT}$, $V_{RGL,INT}$, $V_{LGS,L}$ are positive and $V_{LG,L}$ is negative. If the rated minimum voltage across the gate and source terminal of the device is exceeded, the device may get overstressed and fail.

$$V_{GS,L} = V_{DR,L} - V_{RGL,EXT} - V_{RGL,INT} - V_{LGS,L} + V_{LG,L} \qquad (23)$$

The output capacitance of upper device then gets fully charged and the output capacitance of bottom device gets fully discharged. The freewheeling diode in the lower device carries the load current. The load current would flow through the lower MOSFET when it is turned on.

When the lower MOSFET is turned off, assuming the load current is still flowing out of the phase-leg, the freewheeling diode of the lower device would carry the load current. As no dv/dt occurred during this transition, the upper device experiences no crosstalk related phenomenon.

During the turn-on transition of the upper device, the voltage across its drain and source terminals falls and there is a dv/dt appearing across both devices. The dv/dt across the lower device is positive. This induces a current flowing along its Miller capacitance such that the voltage across the gate and source terminals becomes more positive. The voltage across gate to source terminal of the lower device during this instance is also given by (23). However, it is worth noting that the polarity of the some of the voltage drops in the gate-loop is reversed. The voltage drops $V_{RGL,EXT}$, $V_{RGL,INT}$, $V_{LGS,L}$ are negative and $V_{LG,L}$ is positive. If this voltage were higher than the turn-on threshold of the lower device,

then a shoot-through would occur, resulting in a large amount of current to flow through both the upper and lower devices. This current may result in heat dissipation large enough to destroy the devices.

The explanation above describes the occurrence of crosstalk related phenomenon for both the upper and lower devices in a single phase-leg. There are two potential causes of failure relating to crosstalk. Both are occurring in a device while the its dedicated driver output is providing a logic “LOW” signal. A negative dv/dt across the device induces a current flowing through the Miller capacitance such that the voltage across the gate and source terminals becomes more negative. This could place a large stress on the device. A positive dv/dt across the device induces a current flowing through its Miller capacitance that makes the voltage across the gate and source terminal of the device become more positive. If this voltage exceeds the turn-on threshold of the device, then both devices in the phase-leg would conduct. The resulting shoot-through current flowing along the devices may result in excessive thermal dissipation and destroy the device.

It is worth noting that during steady state operation of the CLLC converter, ZVS is achieved. This means that both the top and bottom device would turn-on after the voltage across it has reached zero. As a result, the devices should not experience shoot-through caused by crosstalk. Whether the device will be damaged due to its gate to source voltage reaching below the negative limit shall be verified via double pulse testing.

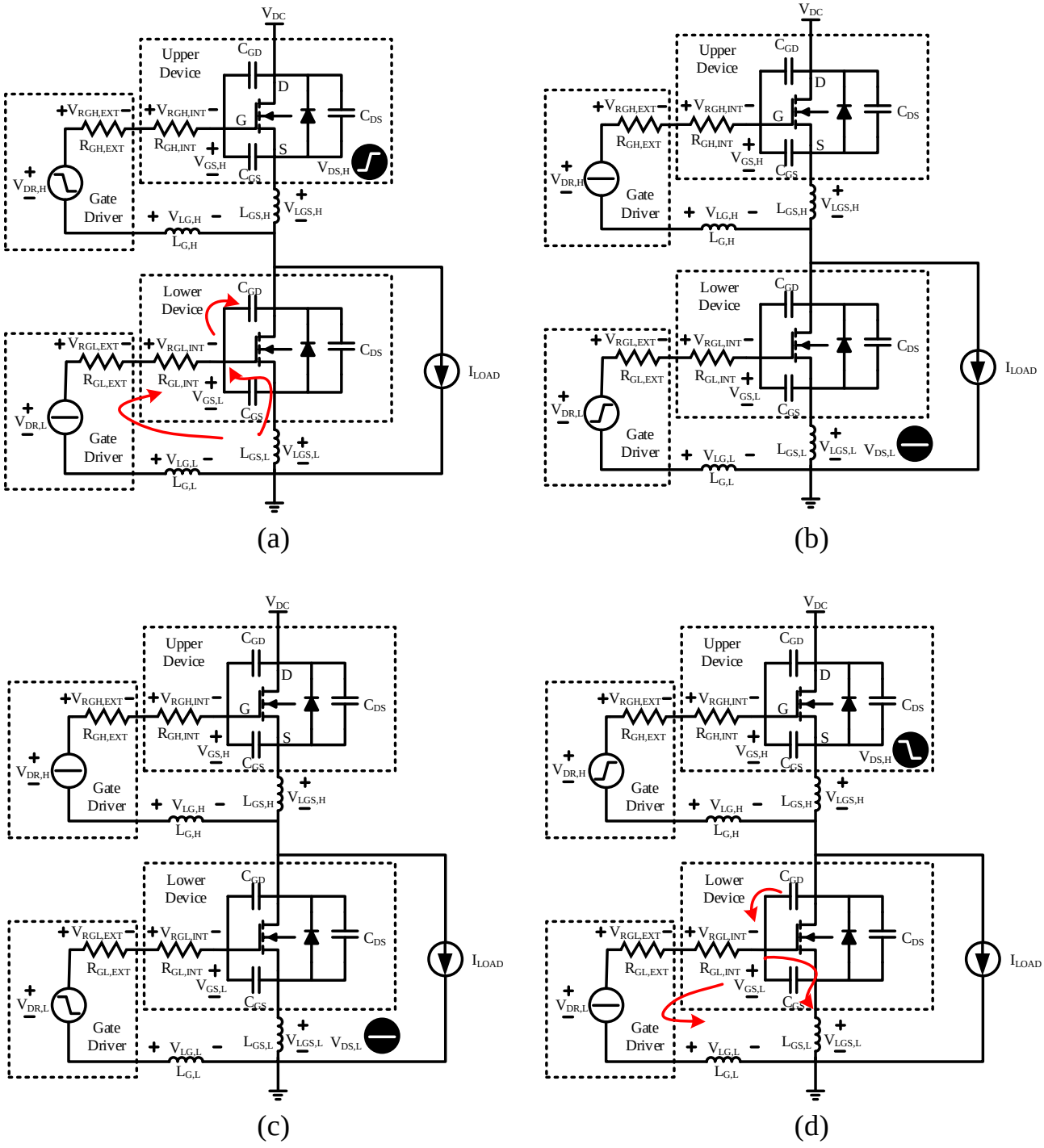



Figure 3.4. Circuit diagram illustrating crosstalk phenomenon with load current flowing out of phase-leg for (a) upper device turn-off (b) lower device turn-on (c) lower device turn-off and (d) upper device turn-on.

It is also worthwhile to calculate the peak gate current in the gate loop to determine whether a current booster circuit is required. Ideally, the addition of current booster circuit should be avoided based on several reasons. First, the introduction of current booster circuit increases the board space and component count. In addition, an extra stage between the switching signal generator (typically the system controller) and the switching device would induce additional delays. Finally, current booster circuits do not interface well with the internal soft-shutdown mechanism of most commercially available gate-driver ICs. Current booster circuits that are based on MOSFET totem-pole circuits cannot be used to interface with large resistance turn-off (LRTO) or (two level turn-off (TLTO) soft-shutdown mechanisms. BJT-based current boosters do not interface well with LRTO based soft-shutdown mechanisms [28]

The formulae used to calculate the peak current in the gate-loop during turn-on and turn-off transitions are given by (24) and (25) respectively. The resulting peak gate current with 3 Ω external gate resistance is outlined in Table 3.5. It can be shown the peak current is smaller than the rated 4 A. hence no external booster circuit is required.

The gate driver for the overall converter follows a modular architecture where each device would get its dedicated modular gate-driver board. Therefore, there are 8 gate-driver boards per converter assembly. Electrical connection between the gate-driver boards and the devices in the power stage boards are made when they are plugged. The 3D rendering of the modular -gate-driver board is shown in Figure 3.5.

$$I_{G,peak\,(on)} \approx 0.74 \frac{\Delta V_{gs}}{R_{G,int} + R_{G,ext} + R_{DR,on}} \tag{24}$$

$$I_{G,peak\,(off)} \approx 0.74 \frac{\Delta V_{gs}}{R_{G,int} + R_{G,ext} + R_{DR,off}} \tag{25}$$

Table 3.5. Calculation of required gate-driver peak current capability.

| Parameter | X3M0016120K | C3M0010090K |
|---|---|---|
| Internal Gate Resistance, $R_{g,int}$ (Ω) | 3.0 | 1.6 |
| External Gate Resistance, $R_{g,ext}$ (Ω) | 1.5 | 3.0 |
| Turn-on Gate Driver Resistance, $R_{DR,on}$ (Ω) | 0.318 | 0.318 |
| Turn-off Gate Driver Resistance, $R_{DR,off}$ (Ω) | 0.417 | 0.417 |
| Peak Turn-on Gate Current, (A) | 3.74 | 3.66 |
| Peak Turn-off Gate Current, (A) | 3.66 | 3.59 |

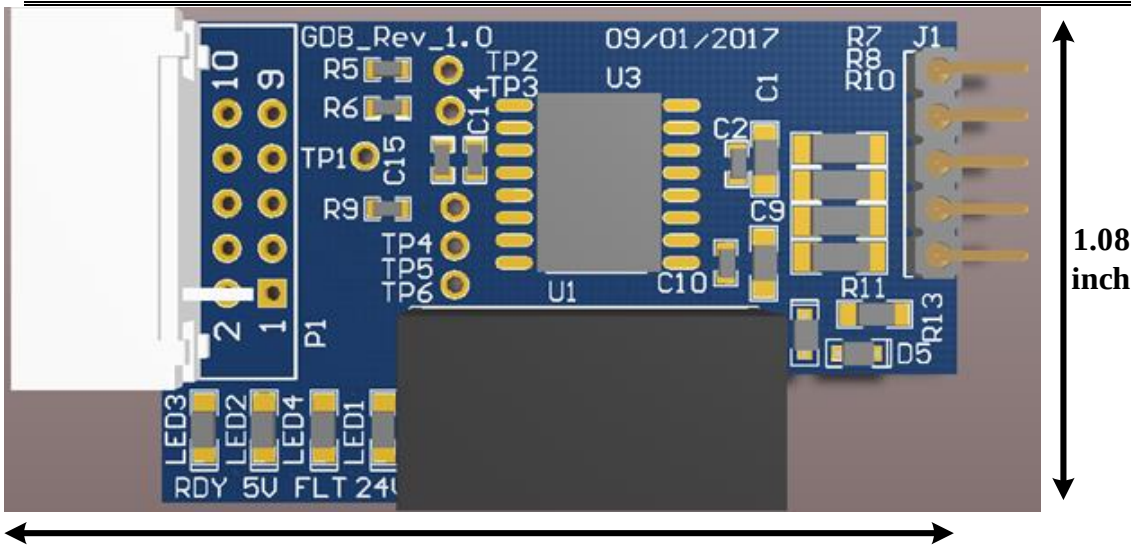



Figure 3.5. 3D rendering of modular gate-driver board.

## 3.2 Power Stage Layout

The actual layout of the power stage has a significant impact on converter operation. A single-phase leg with the associated stray inductance elements is shown in Figure 3.6. The inductance $L_{s1}$ represents the sum of the stray inductance in the DC link capacitor $C_{DC}$ connections and drain terminal of the device. The inductance $L_{s2}$ represents

the stray inductance associated with the connection between the source pin of the upper device and the phase-leg output. The inductance $L_{s3}$ represents the stray inductance associated with the connection between drain terminal of the lower device and the phase-leg output. These stray inductance elements associated with a phase-leg all contribute to an induced voltage overshoot during device turn-off. If the overshoot is large enough, it could potentially destroy the device. The magnitude of this overshoot is related to the product of the stray inductance in the commutation path and the rate of change of current during device turn-off. Given that the turn-off transition occurs very fast for SiC MOSFET switching at high frequencies, it is crucial to minimize the stray inductance in the commutation path during the layout of the power stage PCB.

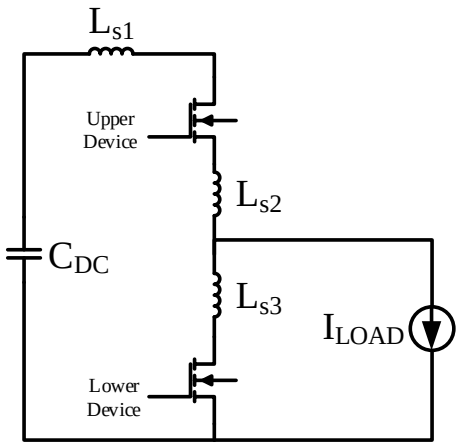


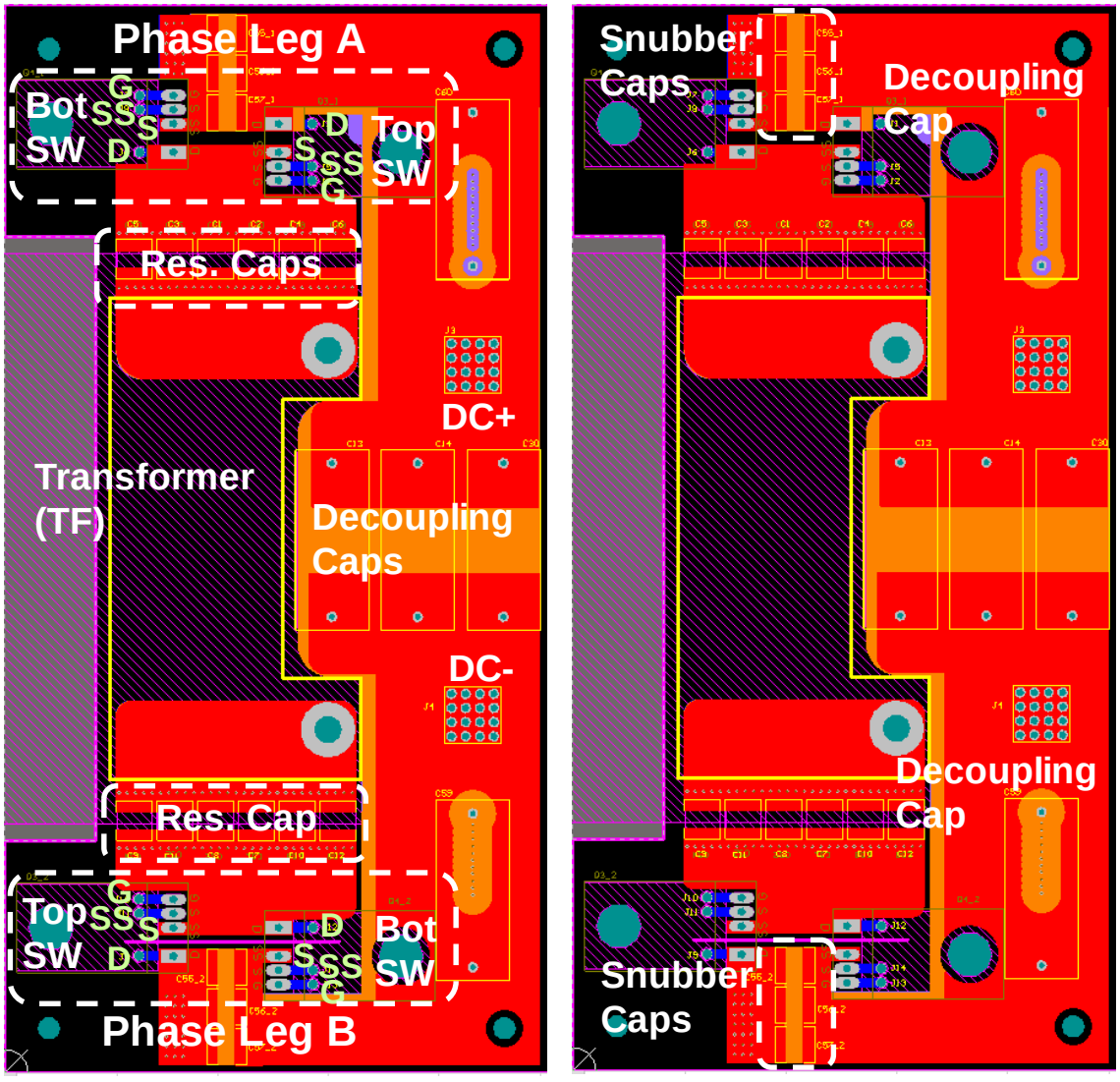

Figure 3.6. Single phase-leg with stray inductance in the commutation path.

The PCB layout of the power stage with all the copper layers visible is shown in Figure 3.7. It can be observed that for each phase-leg, the source terminal of the top device is placed very close to the drain terminal of the bottom device. This was done to minimize the stray inductance $L_{s2}$ and $L_{s3}$.

As shown in Figure 3.8, large copper planes are utilized for DC+ and DC- connections over multiple layers. These copper planes are overlapped against each other to

emulate a laminated bus structure. This arrangement minimizes the loop area in the commutation path, which in turns minimizes the stray inductance $L_{s1}$.

The 3D rendering of the converter assembly is shown in Figure 3.11. The width and length of the completed assembly are 8.02 inch and 7.51 inch respectively. The 3D rendering of the converter assembly with the modular gate-driver boards plugged in is shown in Figure 3.10.




(a) (b)

Figure 3.7. Power stage layout with all-layers shown

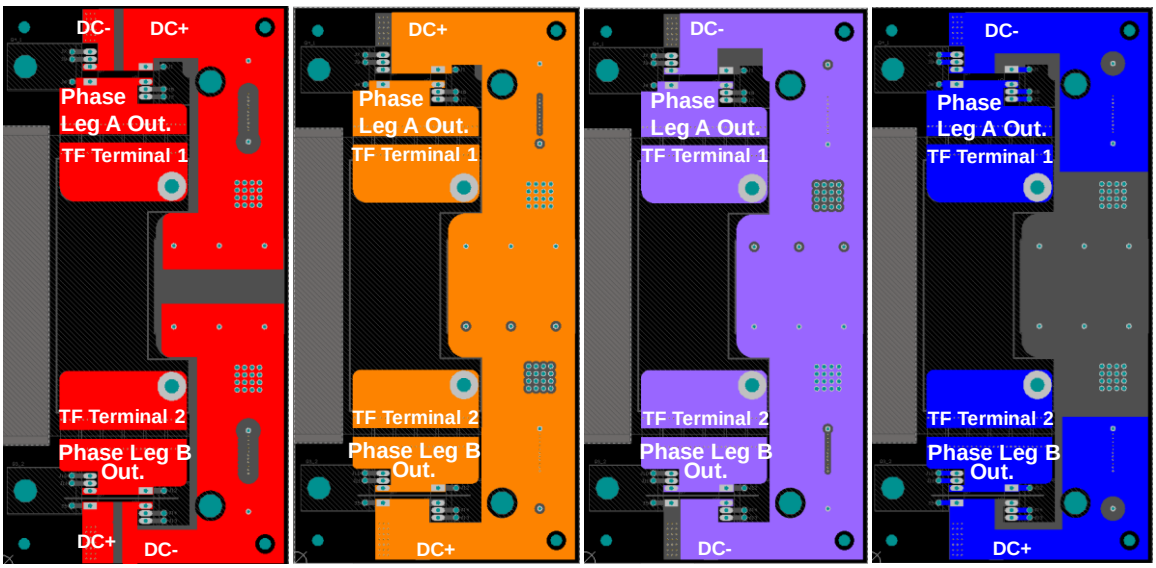



Figure 3.8. Power stage layout for (a) top-layer (b) inner-layer 2 (c) inner-layer 1 and (d) bottom-layer.

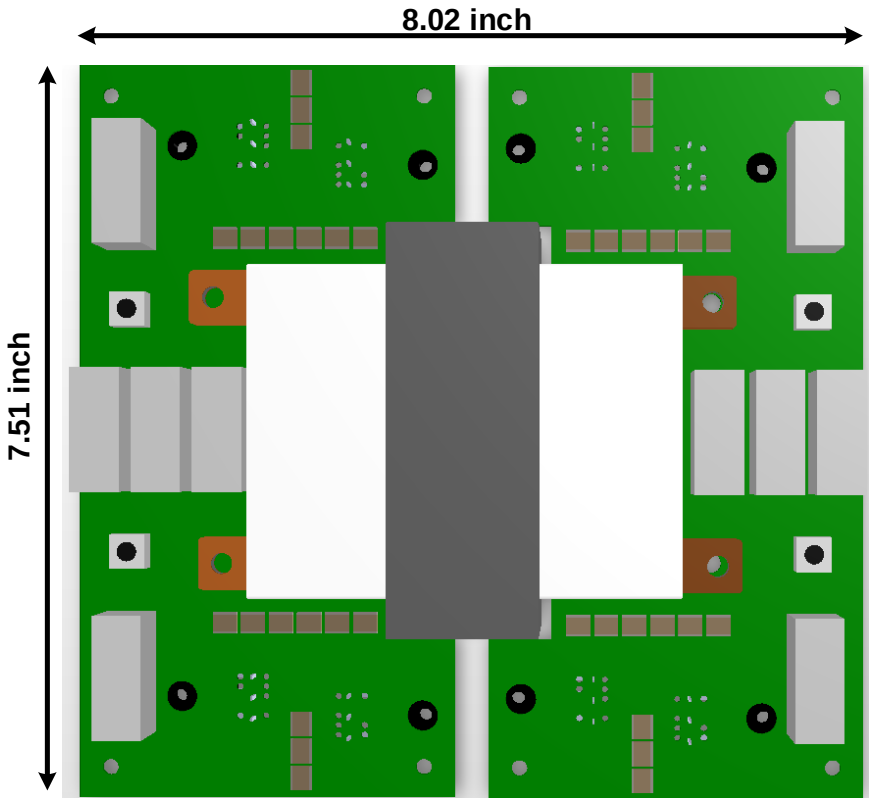



Figure 3.9. 3D rendering of converter assembly without gate-driver board.

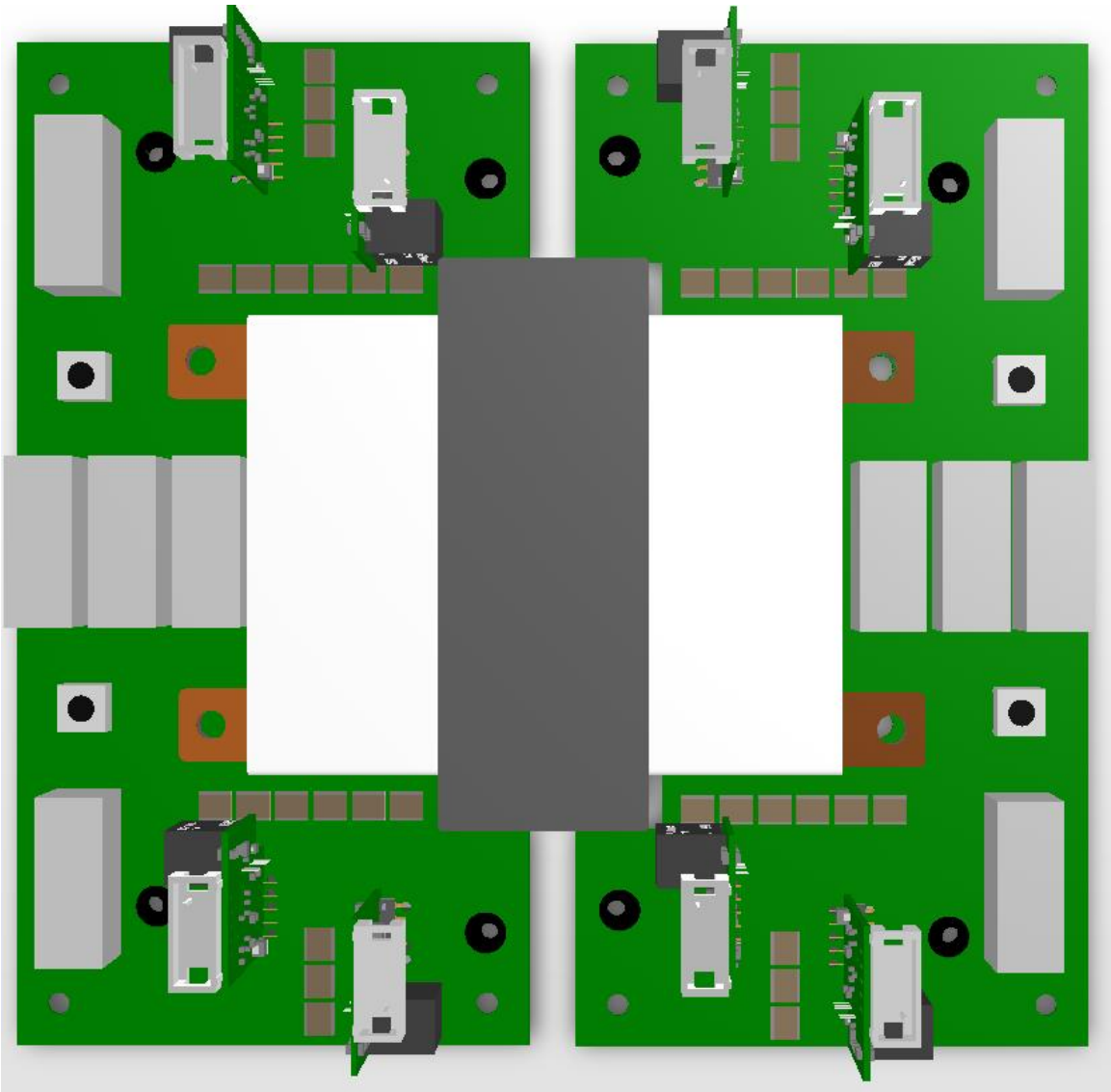


Figure 3.10. 3D rendering of converter assembly with modular gate-driver boards.

# Chapter 4 Experimental Testing for CLLC Resonant Converter

## 4.1 Double Pulse Testing

Before fully assembling the CLLC resonant converter, it is prudent to perform double pulse testing using the power stage and modular gate-driver boards. Double pulse testing serves multiple purposes. It verifies the proper operation of each power stage board and modular gate-driver board under the full DC bus voltage. Additionally, an assessment on whether there is excessive stray inductance in the commutation path can be made. This allows the design and assembly of the power stage and gate driver boards to be verified independent of the CLLC resonant tank. Consequently, the hardware testing process is carried out in a methodical manner. Any design or assembly error can then be identified at a much earlier stage in the hardware development process.

The high-level diagram for double pulse testing is shown in Figure 4.1. The PWM signals used to control the devices are fed into the adaptor board via a waveform generator. The driving signal for the top device will be kept at a constant logic “LOW” such that the top device will remain off throughout the duration of the test. This way only the freewheeling diode of the top device can conduct the current along the load inductor while the bottom device is off.

The 24 V DC from the Agilent power supply is also fed into the adaptor board. An onboard DC/DC converter generates a 5 V DC rail that is used to power the logic circuitry on the modular gate driver boards. This along with the 24 V DC rail and the PWM signals

are distributed among the modular gate driver boards for each device via ribbon cable connections.

A single phase-leg on the power stage board is populated with the device to be tested. Both phase-legs on the power stage board are laid out in a symmetrical nature. Therefore, it should be sufficient to test only one of the phase-legs for verification of gate-driver operation and device switching behavior. The DC bus voltage is provided by a high voltage DC power supply, which can supply the maximum bus voltage designated for converter operation.

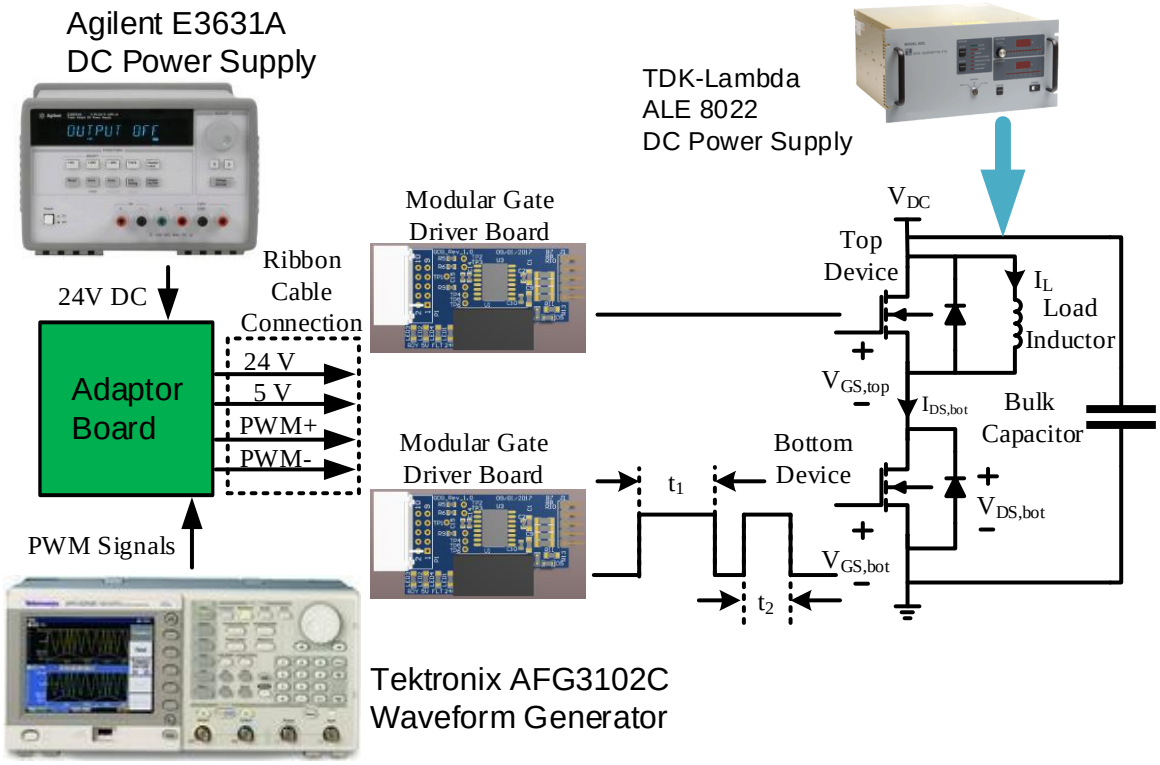



Figure 4.1. High-level diagram for double pulse test.

The physical test setup for the double pulse test is shown in Figure 4.2. Test points were added to the circuit board as shown in Figure 4.3 to minimize the stray inductance in the measurement loop for the passive probes. The instrumentation of the Rogowski coil for measuring the load inductor current is shown in Figure 4.4.

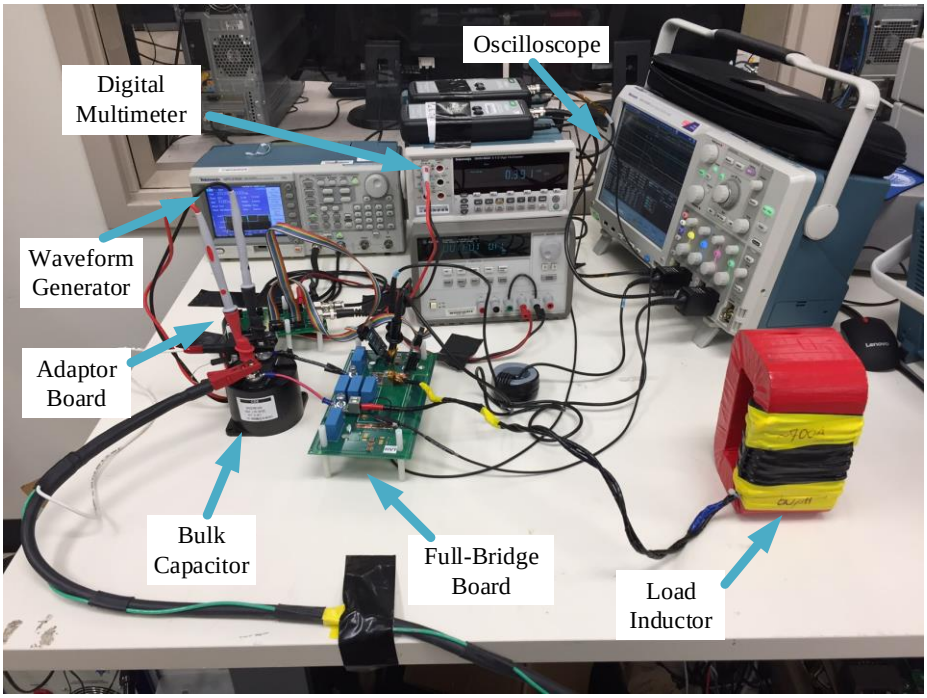



Figure 4.2. Physical setup for double-pulse test.

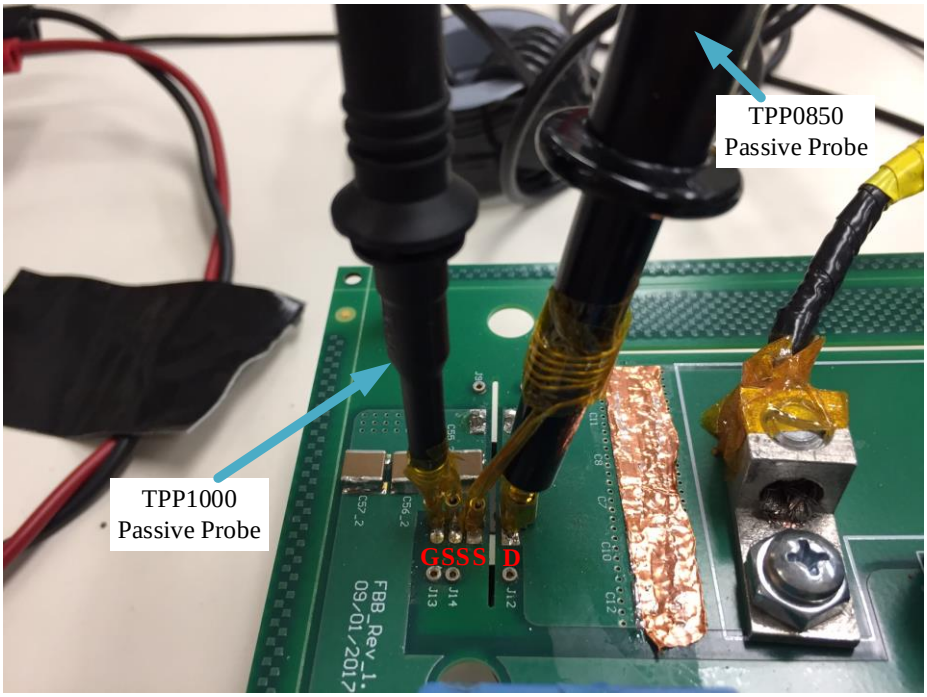



Figure 4.3. Physical setup for double pulse test highlighting the passive voltage probes.

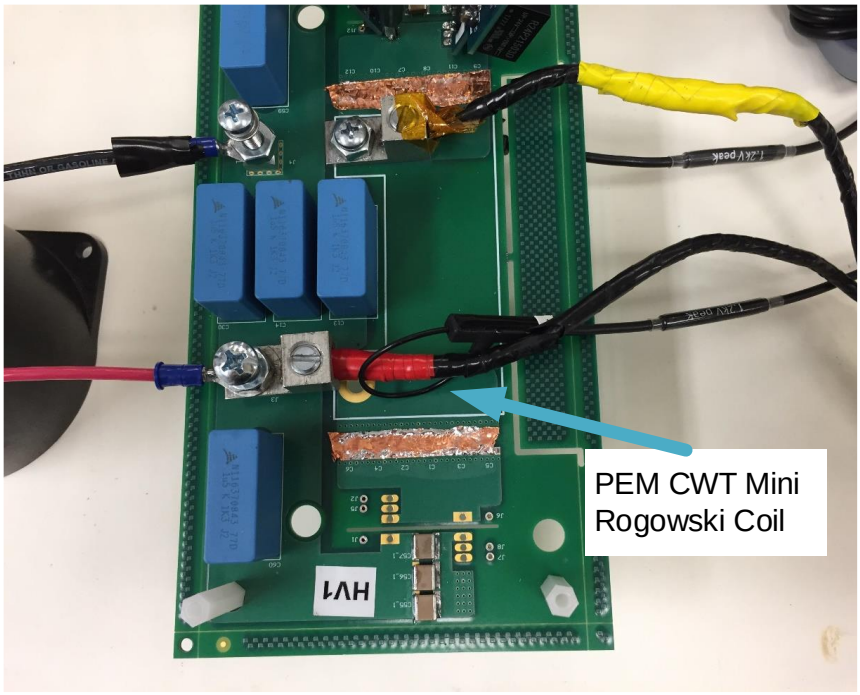



Figure 4.4. Physical setup for double pulse test highlighting the Rogowski coil.

The instrumentation summary for the double pulse test is outlined in Table 2.2 and considerations outlined in [31] were made. A probe bandwidth higher than the bandwidth of the signal would be sufficient to fully capture the magnitude information. However, an accurate capture of the phase information requires a probe bandwidth that is at least ten times the bandwidth of the signal. The signal bandwidth is estimated using the formula given by (26).

$$BW = \frac{0.37}{t_r} \tag{26}$$

The probe instrumentation setup for the double pulse test is outlined in Table 4.1. All the probes had bandwidth exceeding ten times the signal bandwidth, except for the Rogowski coil, which was used to measure the current flowing along the bottom device.

For the current flowing along the bottom device, the probe bandwidth is barely higher than the signal bandwidth. This meant while accurate magnitude information was

captured, it is unlikely that accurate phase information was captured. As a result, the switching energy data derived from post-processing the results of the DPT would be a qualitative measure instead of quantitative. A current shunt would be more suitable in accurately capturing the magnitude and phase of the device drain current [31]. However, the lack of available space on the power-stage board prevents it from being integrated into the testing setup. Nevertheless, double pulse testing is still a crucial stage in the overall hardware testing process due to the reasons previously mentioned in this chapter.

Selecting the right oscilloscope is also crucial in terms of capturing both the magnitude and phase information of the measured signals accurately. Similar to the requirement for the probes, the bandwidth of the oscilloscope must be at least ten times the bandwidth of the signal being measured. The required sampling rate of the oscilloscope depends on the interpolation method used. If a linear interpolation method is used, then the sampling rate of the oscilloscope needs to be at least ten times the bandwidth of the measured signal. The measured signal with the highest bandwidth in the DPT setup is the voltage across the drain and source terminals of the bottom device, which has an estimated bandwidth of 20.6 MHz. Therefore, the required minimum bandwidth and sampling rate of the oscilloscope are 206 MHz and 206 MS/s respectively. The oscilloscope in the DPT setup is MSO5104B from Tektronix, which has a bandwidth and sampling rate of 1 GHz and 10 GS/s respectively.

The test parameters including pulse duration, maximum DC bus voltage, and load inductor values are outlined in Table 4.2. The pulse durations are selected such that turn-off current exceeding the expected values are tested at the specified maximum DC bus voltage.

Table 4.1. Probe instrumentation for double pulse test.

| | Peak Measured Value | Rise Time, $t_r$ | Signal Bandwidth, BW | Probe | Equipment Bandwidth |
|---|---|---|---|---|---|
| $V_{GS,BOT}$ | < 20 V | 22.9 ns | 15.3 MHz | TPP1000 Passive Probe | 1 GHz |
| $V_{DS,BOT}$ | < 1.2 kV | 17 ns | 20.6 MHz | TPP0850 Passive Probe | 800 MHz |
| $I_{D,BOT}$ | < 30 A | 20 ns | 17.5 MHz | PEM CWT Mini Rogowski Coil | 20 MHz |
| $I_L$ | < 30 A | 19 us | 250 kHz | PEM CWT Mini Rogowski Coil | 20 MHz |

Table 4.2. Parameters for double pulse test.

| Device | X3M0016120K | C3M0010090K |
|---|---|---|
| Maximum DC Bus Voltage under Test (V) | 800 | 600 |
| Simulated Peak Turn-off Current (A) | 15.4 | 23.1 |
| Peak Turn-off Current under Test (A) | 30 | 30 |
| Duration for First Pulse, $t_1$ (μs) | 1.9 | 1.9 |
| Pulse Duration for Second Pulse, $t_2$ (μs) | 1 | 1.9 |
| Load Inductor Value (μH) | 60 | 60 |

The experimental waveforms for the double pulse test performed on C3M0010090K under different DC bus voltage and external gate resistance are shown in Figure 4.5 thru Figure 4.16.

The experimental waveforms for the double pulse test performed on X3M0016120K under different DC bus voltage and external gate resistance are shown in Figure 4.17 thru Figure 4.28.

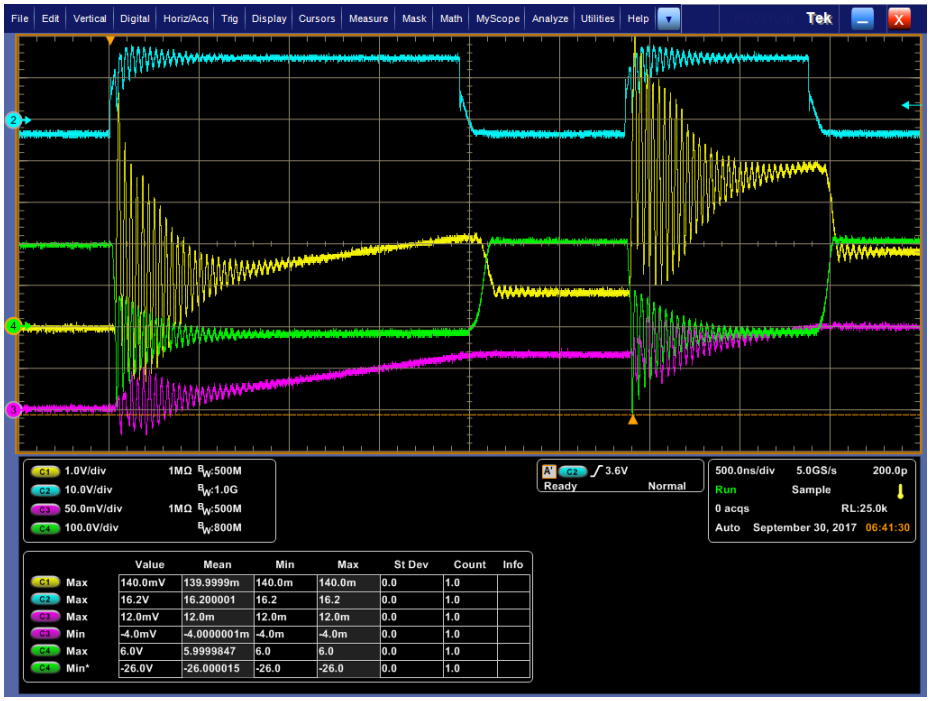



Figure 4.5. DPT waveforms for C3M0010090K with 1.5Ω external gate resistance and 200 V DC bus for (1) $I_{D,\,BOT}$ (5 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (5 A/div), and (4) $V_{DS,\,BOT}$.

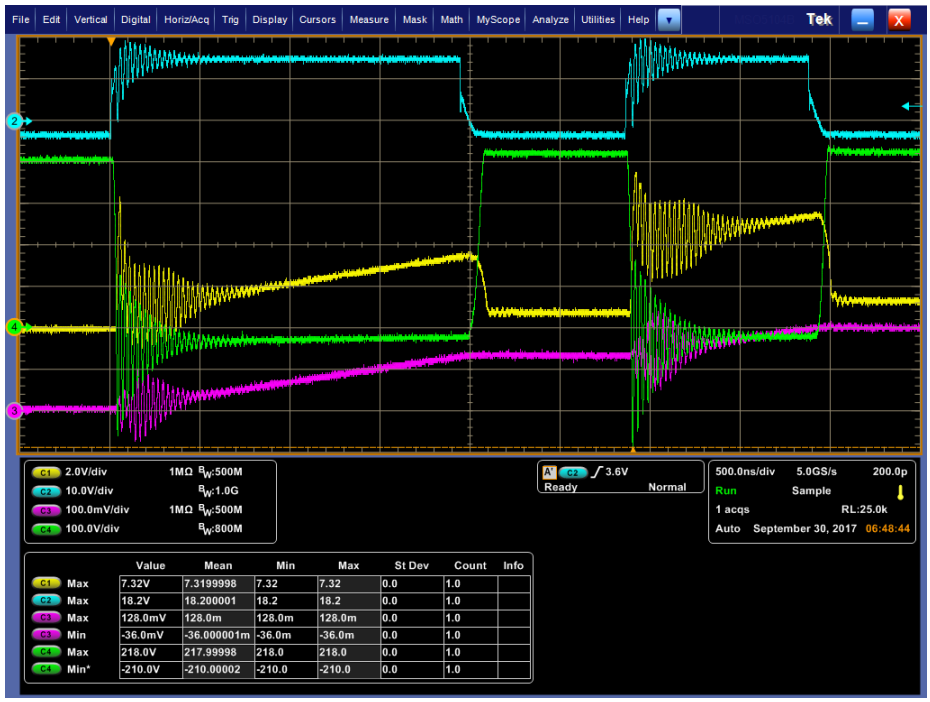



Figure 4.6. DPT waveforms for C3M0010090K with 1.5Ω external gate resistance and 400 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

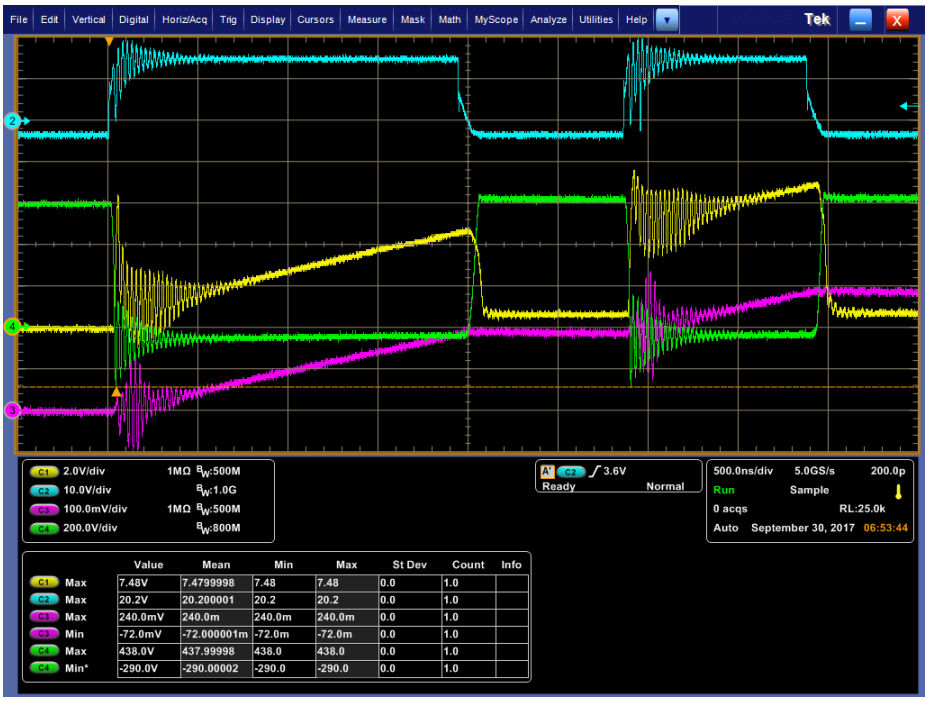



Figure 4.7. DPT waveforms for C3M0010090K with 1.5Ω external gate resistance and 600 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

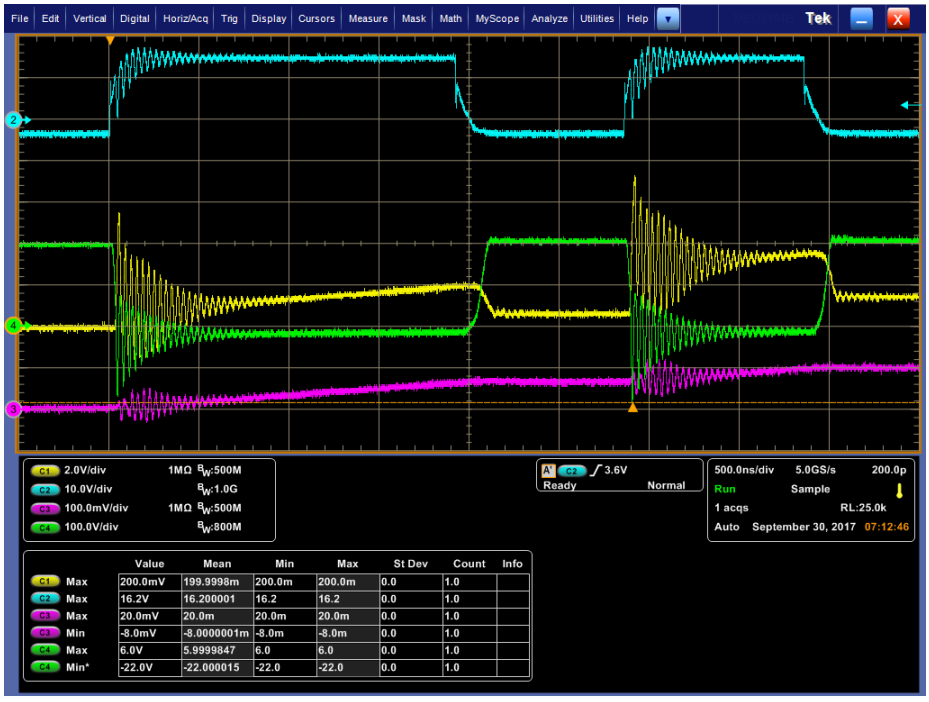



Figure 4.8. DPT waveforms for C3M0010090K with 3Ω external gate resistance and 200 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

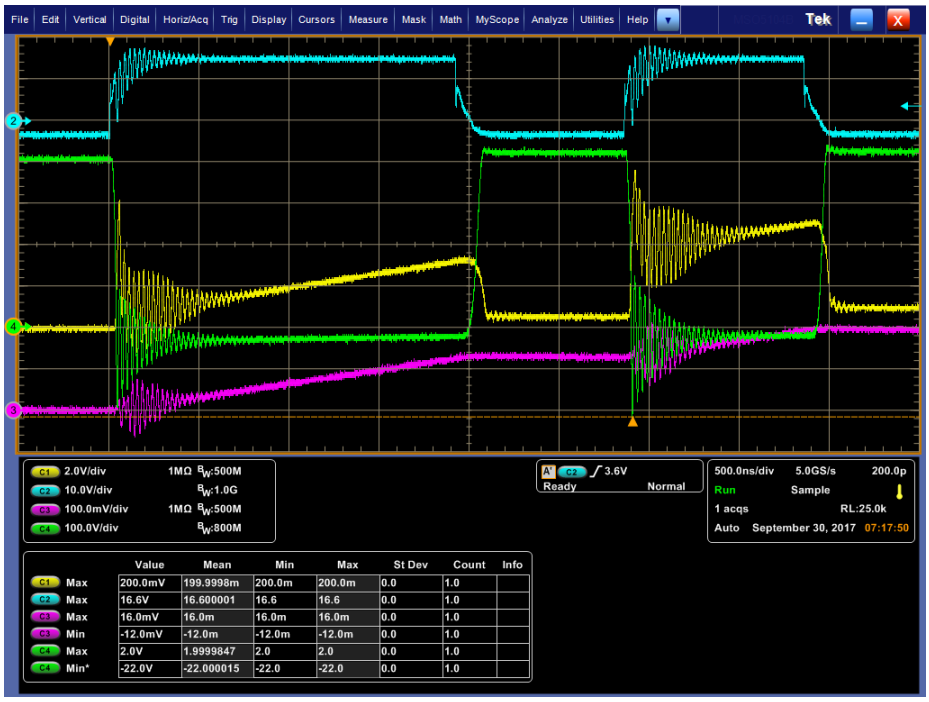



Figure 4.9. DPT waveforms for C3M0010090K with 3Ω external gate resistance and 400 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

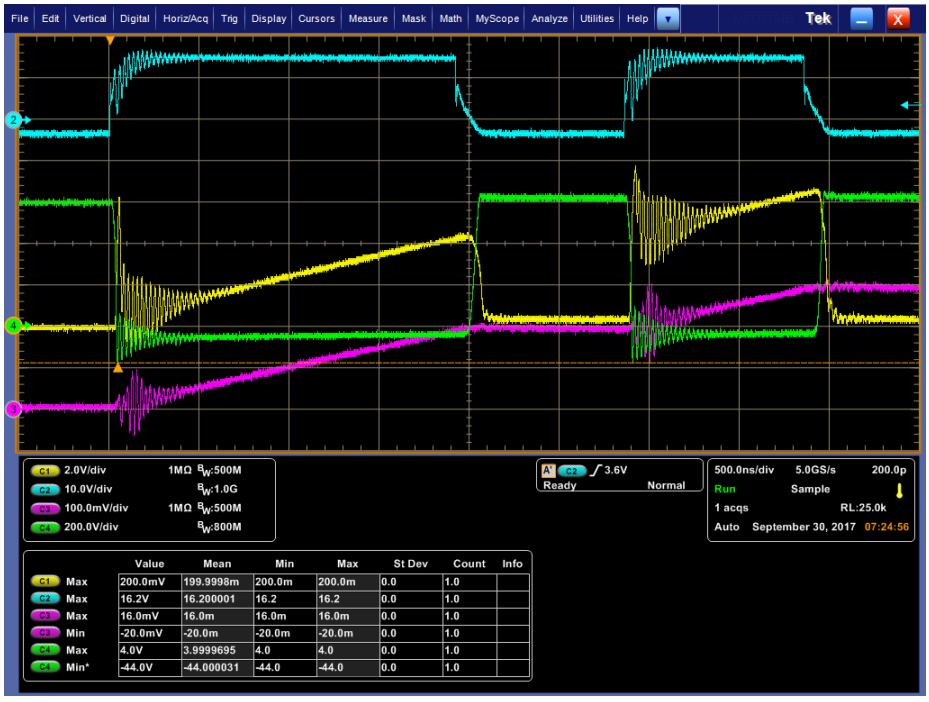



Figure 4.10. DPT waveforms for C3M0010090K with 3Ω external gate resistance and 600 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

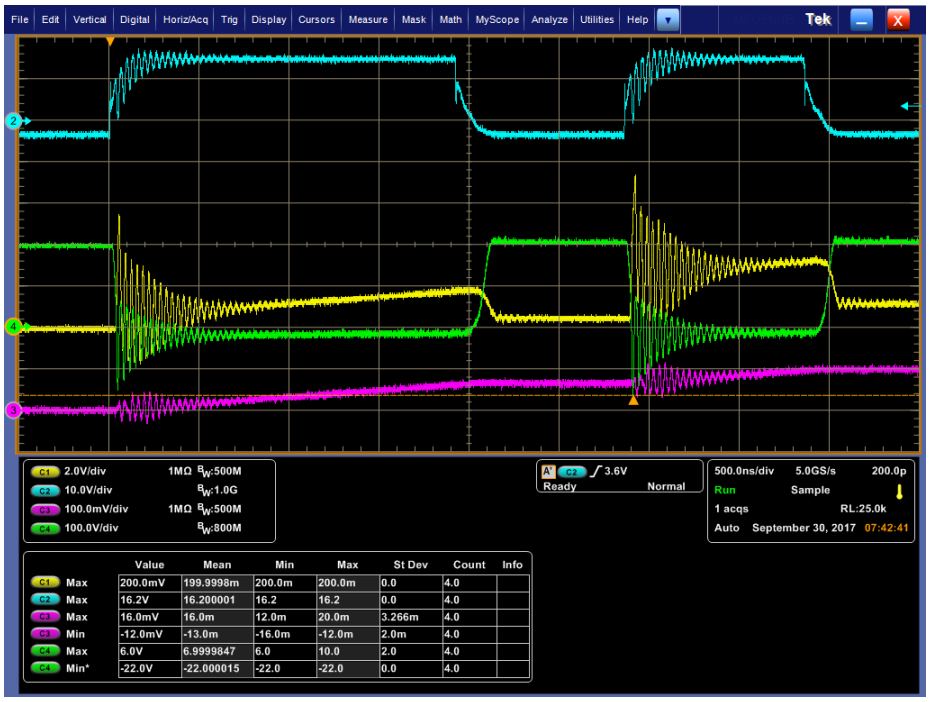



Figure 4.11. DPT waveforms for C3M0010090K with 4Ω external gate resistance and 200 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

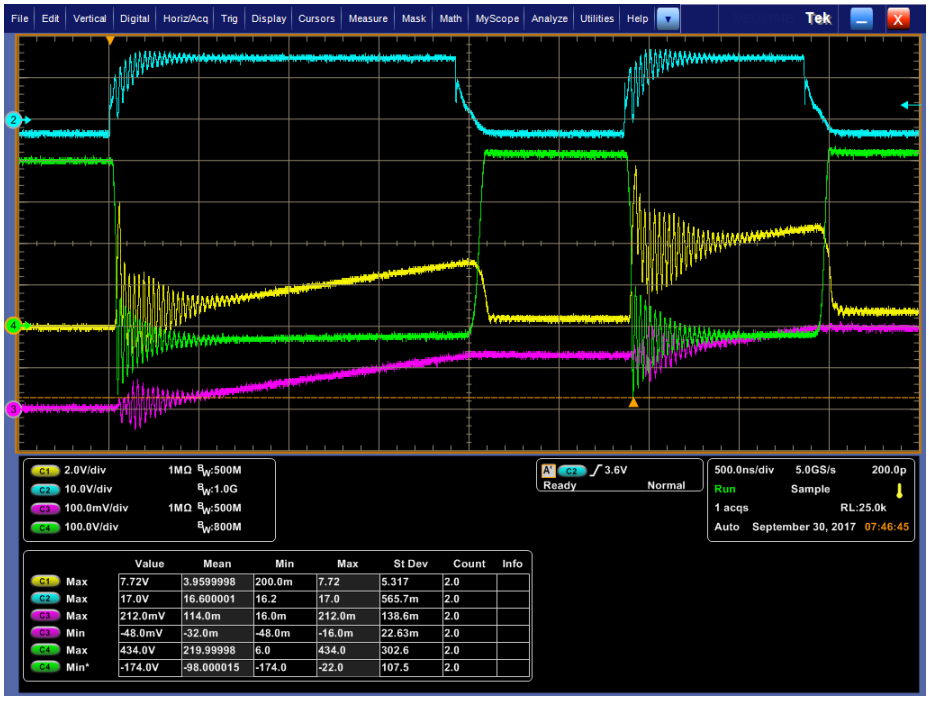



Figure 4.12. DPT waveforms for C3M0010090K with 4Ω external gate resistance and 400 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

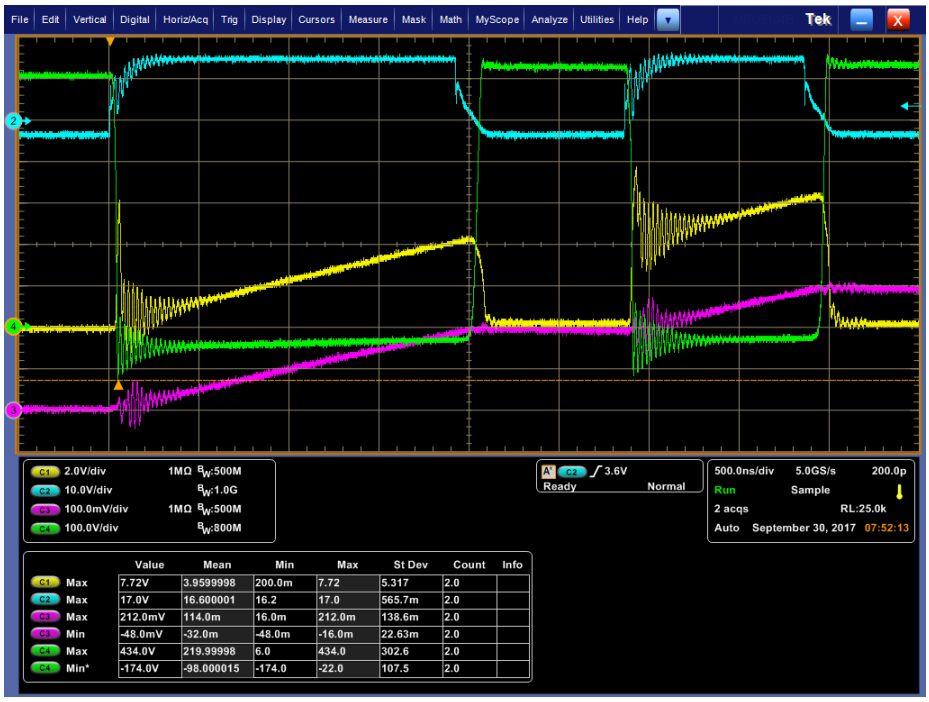



Figure 4.13. DPT waveforms for C3M0010090K with 4Ω external gate resistance and 600 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

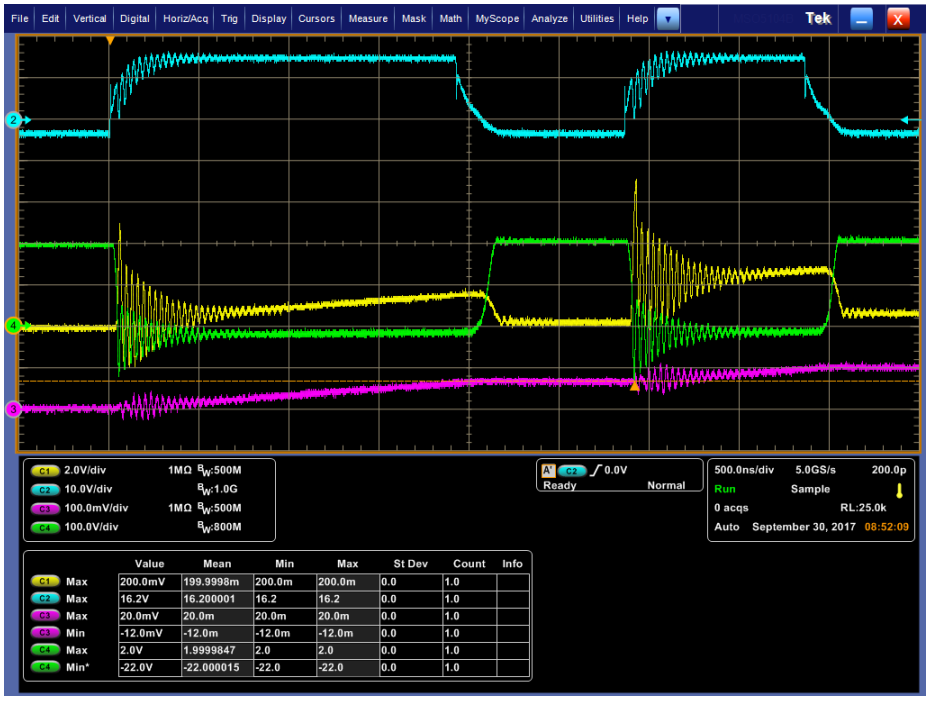



Figure 4.14. DPT waveforms for C3M0010090K with 6Ω external gate resistance and 200 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

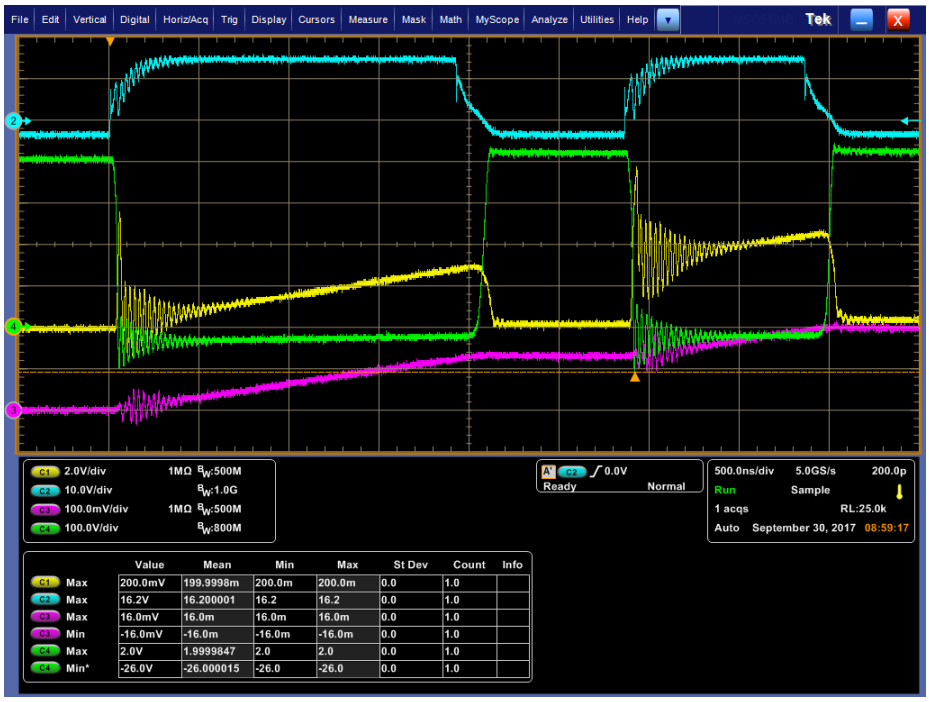



Figure 4.15. DPT waveforms for C3M0010090K with 6Ω external gate resistance and 400 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

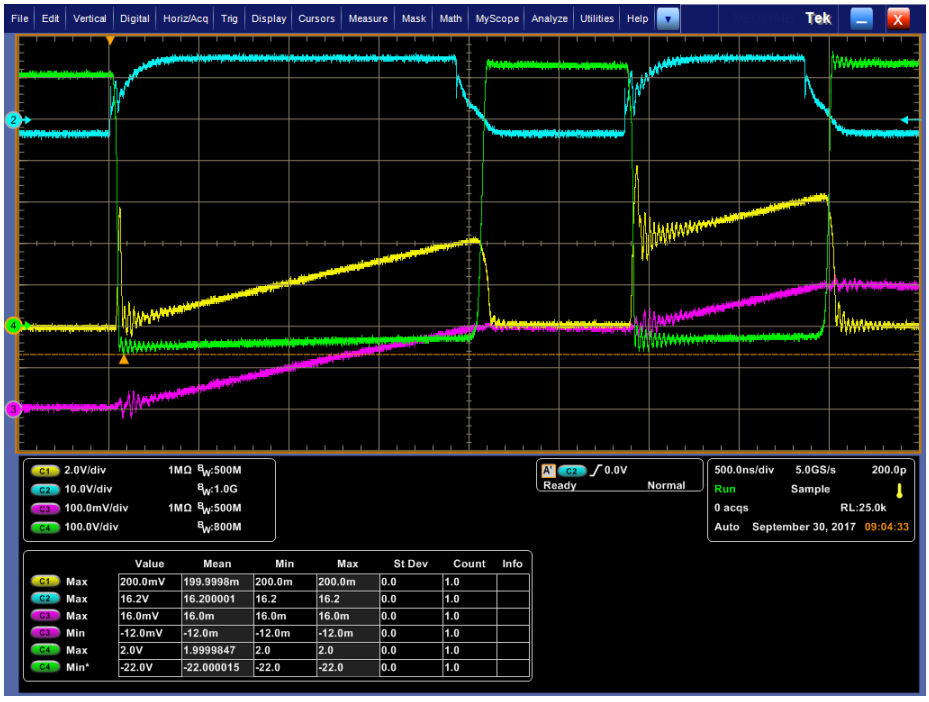



Figure 4.16. DPT waveforms for C3M0010090K with 6Ω external gate resistance and 600 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

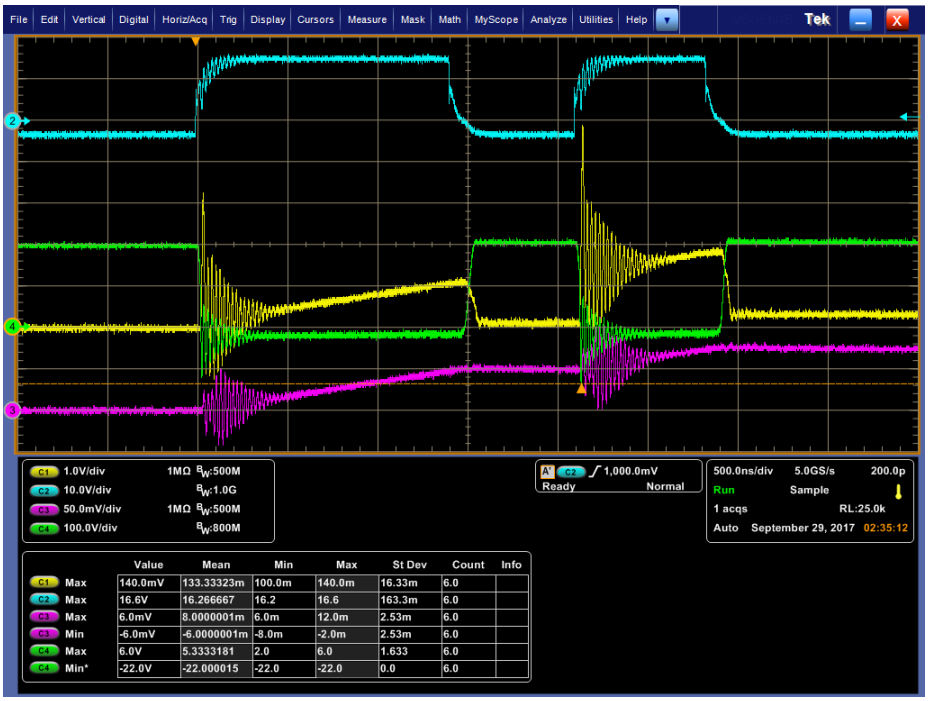



Figure 4.17. DPT waveforms for X3M0016120K with 3Ω external gate resistance and 200 V DC bus for (1) $I_{D,\,BOT}$ (5 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (5 A/div), and (4) $V_{DS,\,BOT}$.

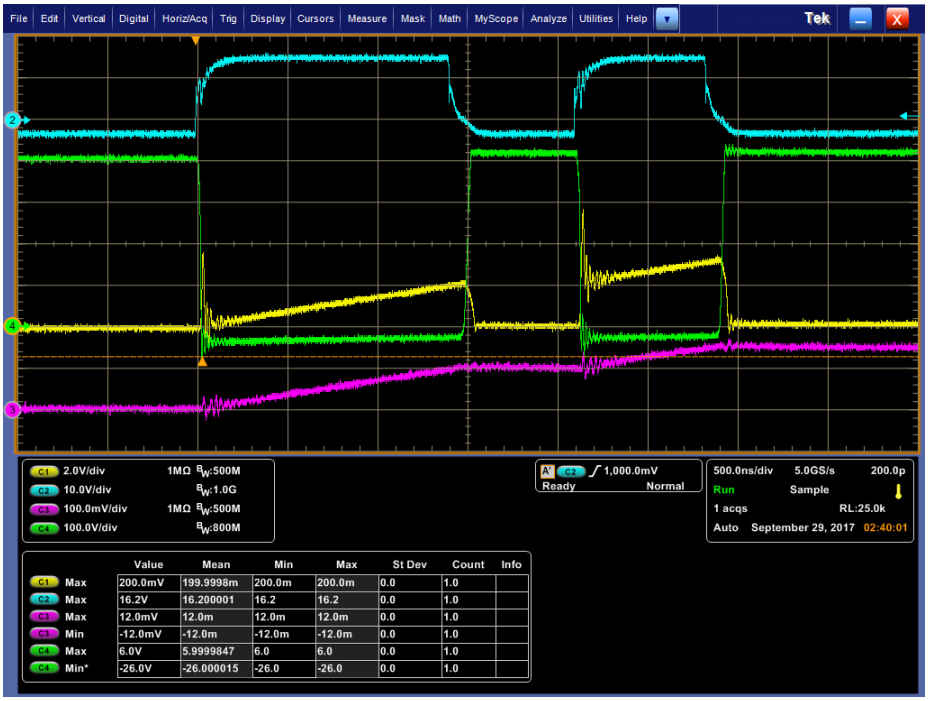



Figure 4.18. DPT waveforms for X3M0016120K with 3Ω external gate resistance and 400 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

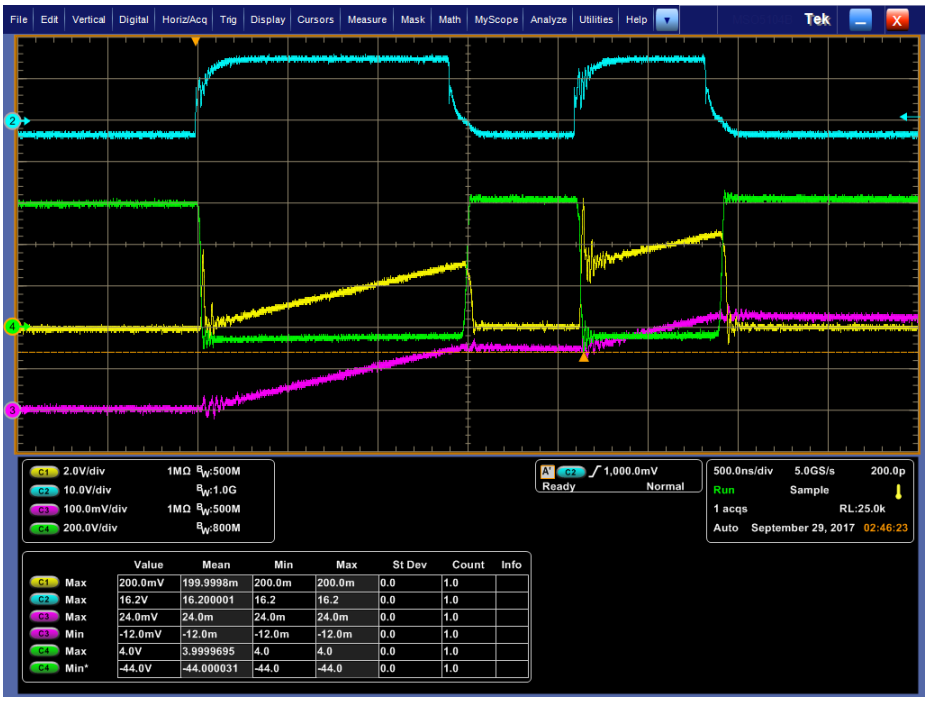



Figure 4.19. DPT waveforms for X3M0016120K with 3Ω external gate resistance and 600 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

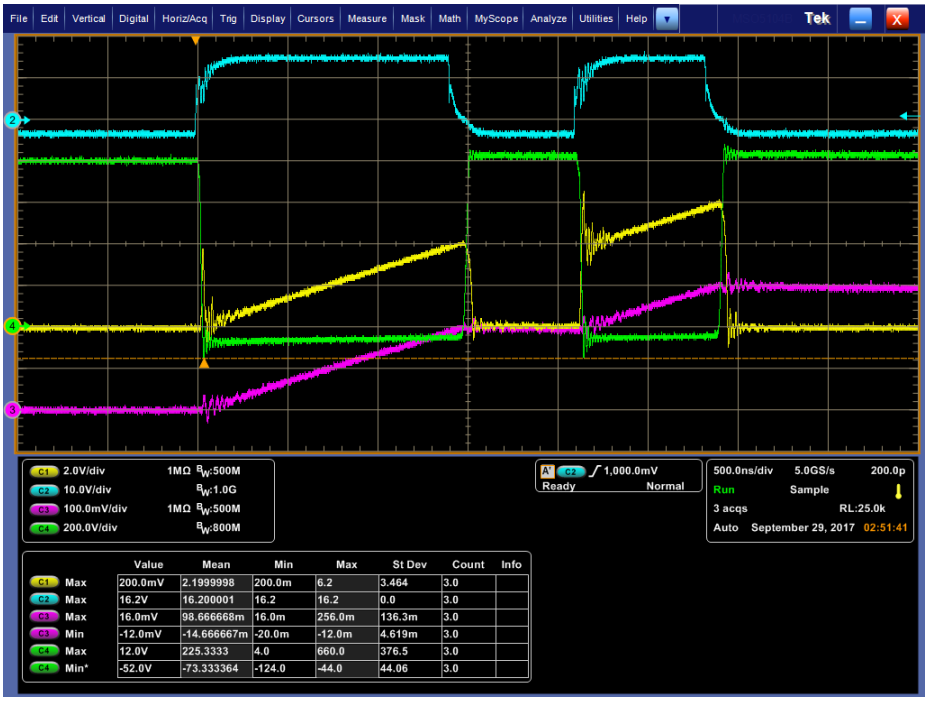



Figure 4.20. DPT waveforms for X3M0016120K with 3Ω external gate resistance and 800 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

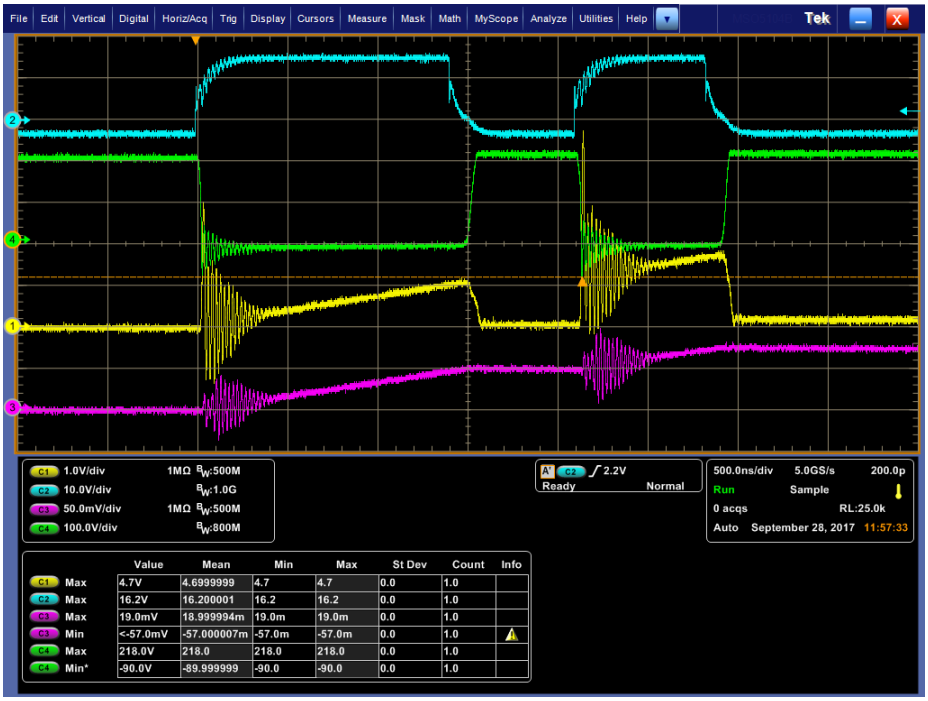



Figure 4.21. DPT waveforms for X3M0016120K with 4Ω external gate resistance and 200 V DC bus for (1) $I_{D,\,BOT}$ (5 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (5 A/div), and (4) $V_{DS,\,BOT}$.

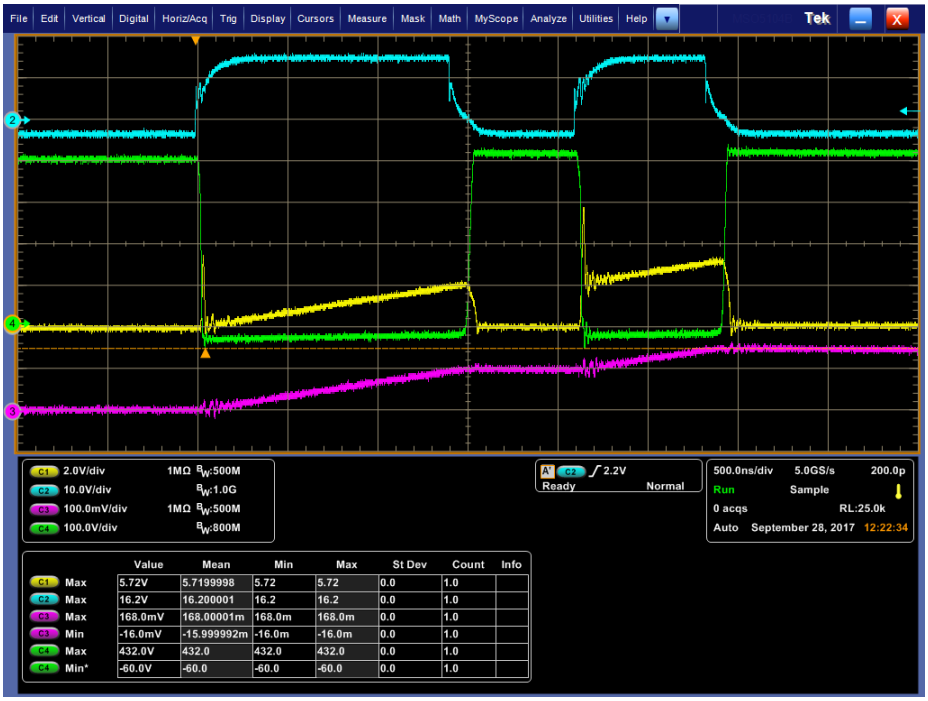



Figure 4.22. DPT waveforms for X3M0016120K with 4Ω external gate resistance and 400 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.


Figure 4.23. DPT waveforms for X3M0016120K with 4Ω external gate resistance and 600 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

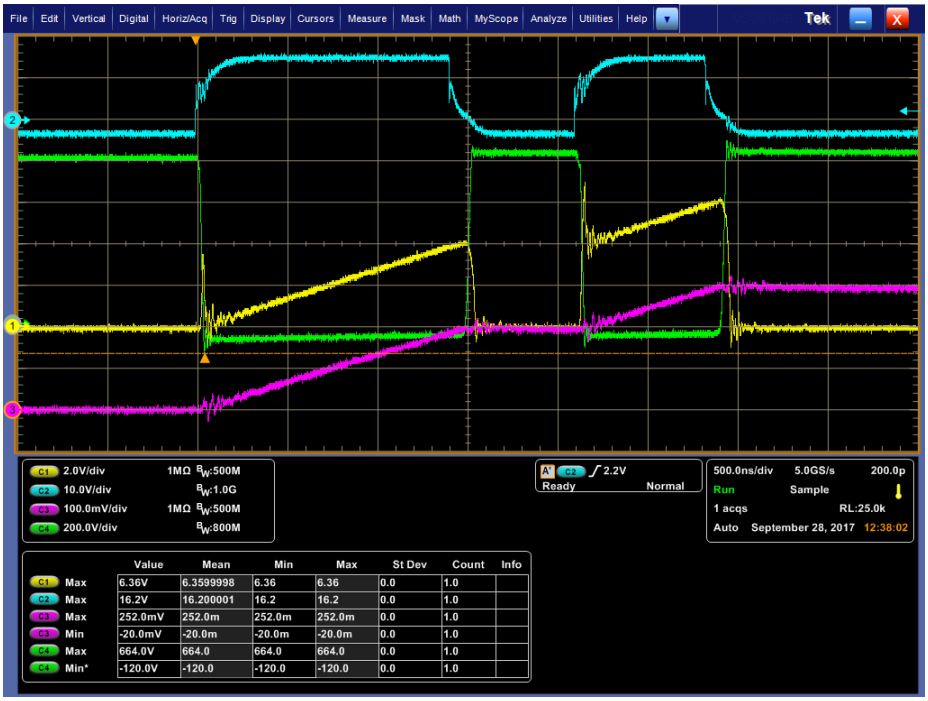



Figure 4.24. DPT waveforms for X3M0016120K with 4Ω external gate resistance and 800 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

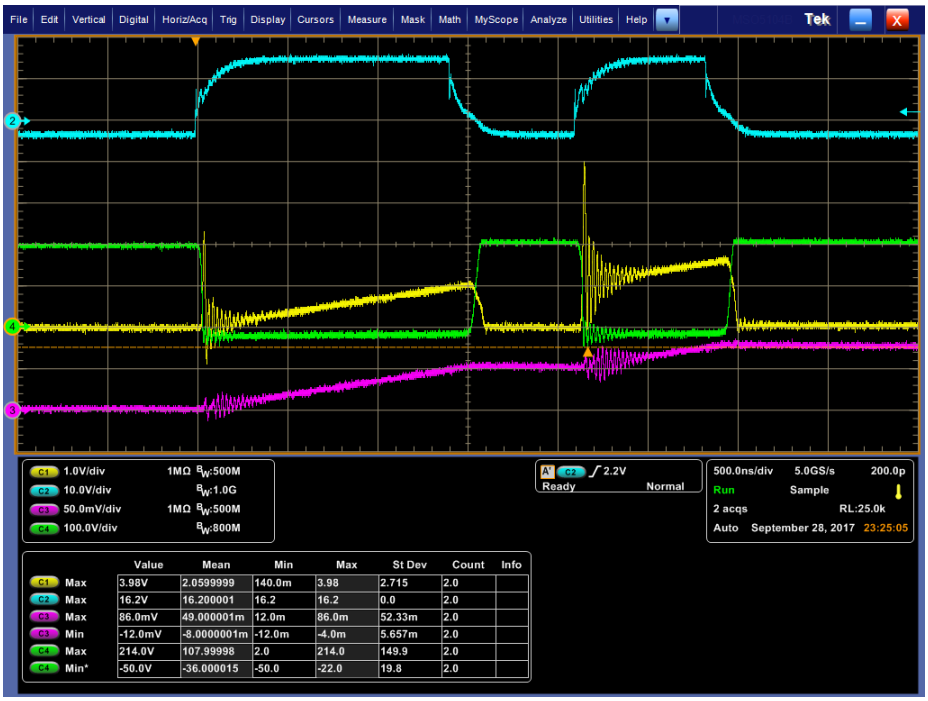



Figure 4.25. DPT waveforms for X3M0016120K with 6Ω external gate resistance and 200 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

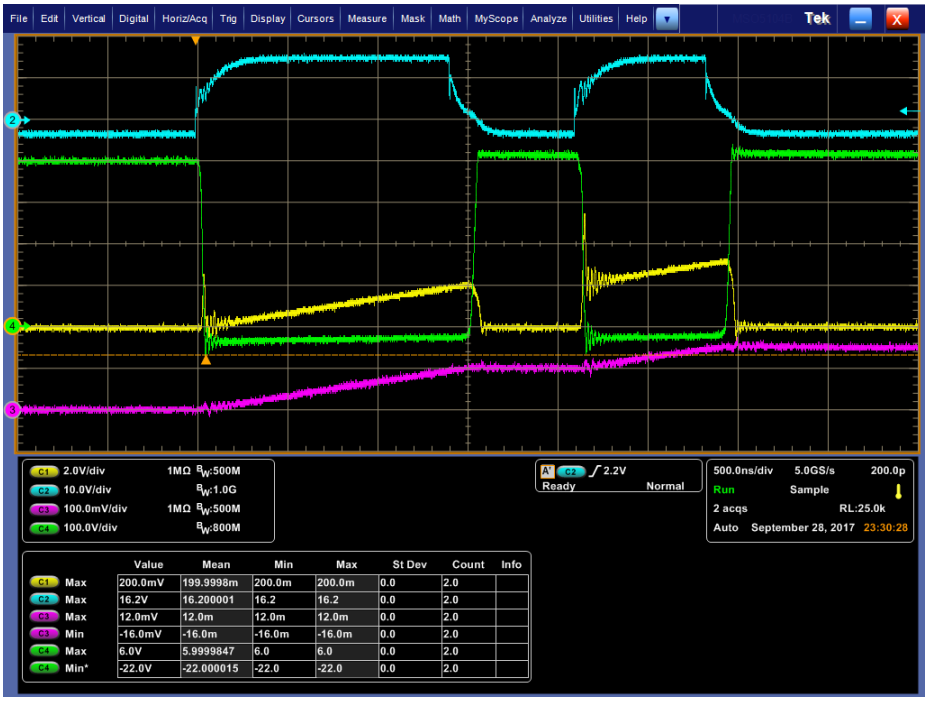



Figure 4.26. DPT waveforms for X3M0016120K with 6Ω external gate resistance and 400 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

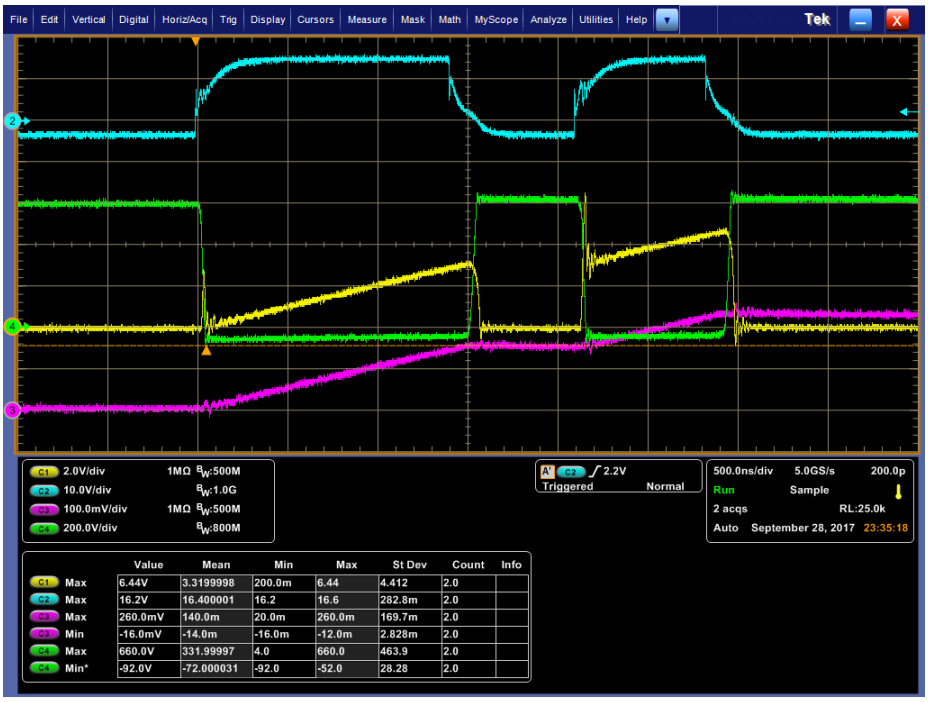



Figure 4.27. DPT waveforms for X3M0016120K with 6Ω external gate resistance and 600 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

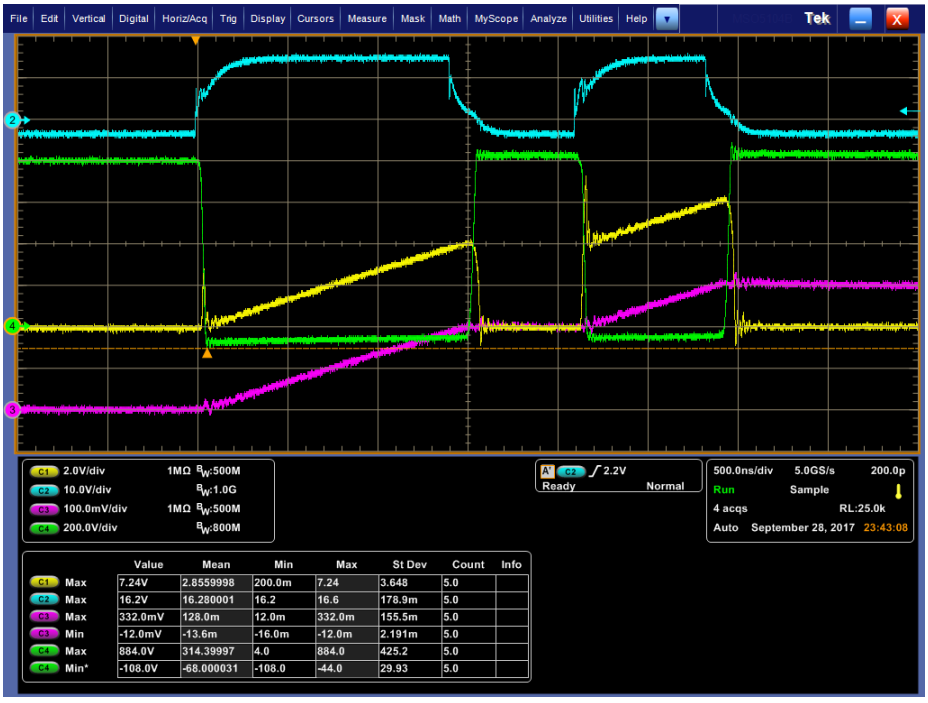



Figure 4.28. DPT waveforms for X3M0016120K with 6Ω external gate resistance at 800 V DC bus for (1) $I_{D,\,BOT}$ (10 A/div), (2) $V_{GS,\,BOT}$, (3) $I_L$ (10 A/div), and (4) $V_{DS,\,BOT}$.

## 4.2 250 kHz CLLC Resonant Converter Test

The physical unit for the isolation transformer used in the CLLC converter assembly is shown in Figure 4.29. The circuit diagram for the actual converter setup under forward mode operation and reverse mode operation are shown in Figure 4.30 and Figure 4.31 respectively. The component values for the converter setup are outlined in Table 4.3.

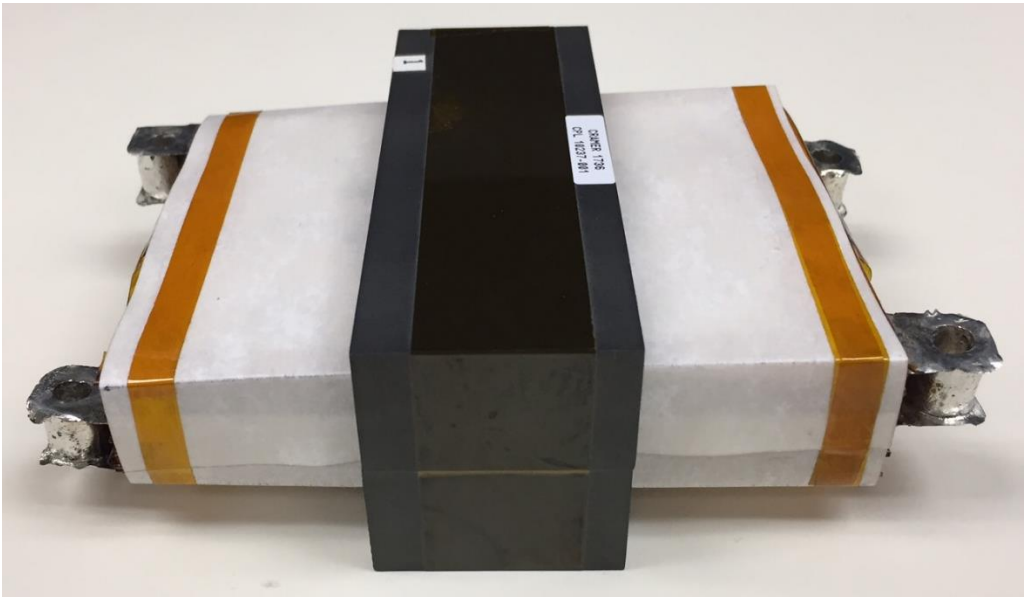


Figure 4.29. Isolation transformer used in CLLC converter assembly.

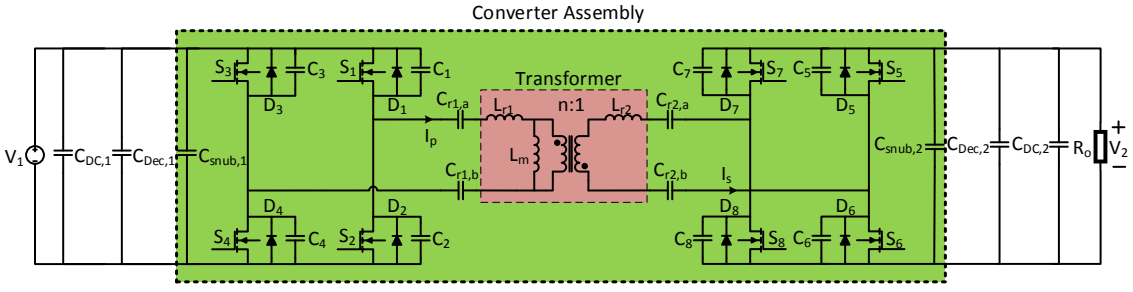



Figure 4.30. Circuit diagram for actual converter testing setup (forward mode).

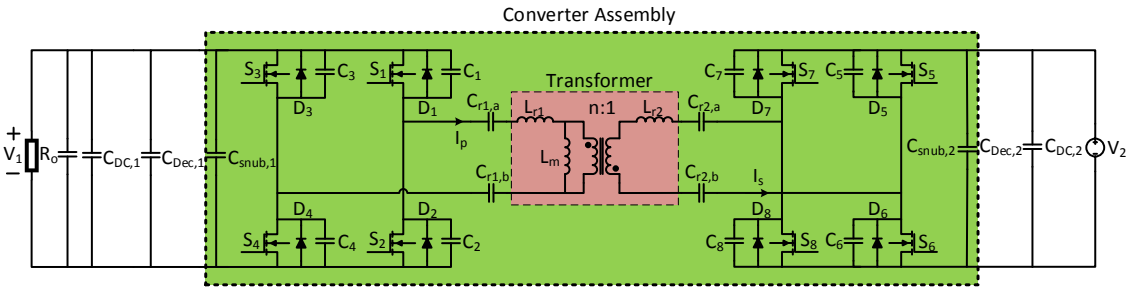



Figure 4.31. Circuit diagram for actual converter testing setup (reverse mode).

Table 4.3. Summary of component values for actual CLLC converter setup.

| Parameter | Value |
|---|---|
| Primary Side Device $S_1$, $S_2$, $S_3$, $S_4$ | X3M0016120K |
| Secondary Side Device $S_5$, $S_6$, $S_7$, $S_8$ | C3M0010090K |
| Magnetizing Inductance (referred to Primary side), $L_m$ | 50.4 µH |
| Primary to Secondary Transformer Turns Ratio, n | 1.5 |
| Primary Side Leakage Inductance, $L_{r1}$ | 139 nH |
| Primary Side Leakage Inductance, $L_{r2}$ | 102 nH |
| Primary Side Resonant Capacitor, $C_{r1,a}$ | 4.29 µF |
| Primary Side Resonant Capacitor, $C_{r1,b}$ | 4.29 µF |
| Secondary Side Resonant Capacitor, $C_{r2,a}$ | 5.61 µF |
| Secondary Side Resonant Capacitor, $C_{r2,b}$ | 5.61 µF |
| Primary Side Snubber Capacitor, $C_{snub,1}$ | 0.3 µF |
| Primary Side Decoupling Capacitor, $C_{Dec,1}$ | 7.5 µF |
| Primary Side DC-Link Capacitor, $C_{DC,1}$ | 100 µF |
| Secondary Side Snubber Capacitor, $C_{snub,2}$ | 0.3 µF |
| Secondary Side Decoupling Capacitor, $C_{Dec,2}$ | 7.5 µF |
| Secondary Side DC-Link Capacitor, $C_{DC,2}$ | 300 µF |

The experimental setup for CLLC converter testing is shown in Figure 4.32. A waveform generator generates the required switching signals, which are running at 250 kHz with 250 ns deadtime. These PWM signals are sent to the adaptor board and distributed among the eight modular gate-driver boards in the converter assembly along with the auxiliary 24 V and 5 V rails required to power the gate-driver circuitry.

The equivalent volume of the converter assembly used to calculate the power density is 8.02 inch x 9.50 inch x 4.10 inch. The dimensions of the DC fans were included in the calculation of this equivalent volume. However, the dimensions of the DC-link capacitors on both the primary and secondary side were not included. This can be justified by the fact that in a bidirectional power distribution system, the DC-link capacitor typically resides within the assembly for the nonisolated AC/DC and DC/DC converters. Hence these capacitors are not counted as part of the DC transformer. The resulting power density is 78 $W/in^3$.

The zoomed in converter waveforms under 5 kW during $S_2$ turn-off transition and $S_2$ turn-on transition are shown in Figure 4.33 and Figure 4.34 respectively. It can be observed that the drain to source voltage across $S_2$, $V_{ds,\,S2}$, rises to the DC bus voltage of 800 V before $S_4$ is turned on and falls to zero before $S_2$ is turned on. Therefore, ZVS is achieved. It is also worth noting that even though the optimal deadtime for 250 kHz switching was determined to be 100 ns. The oscillation in the transformer winding current increased the actual required deadtime time to 250 ns. However, this should increase the total conduction loss in the devices by no more than 10 W as predicted by the curve in Figure 2.12.

The converter waveforms at different power levels under forward mode operation are shown in Figure 4.35 thru Figure 4.39. The converter waveforms at different power levels under reverse mode operation are shown in Figure 4.40 thru Figure 4.44.

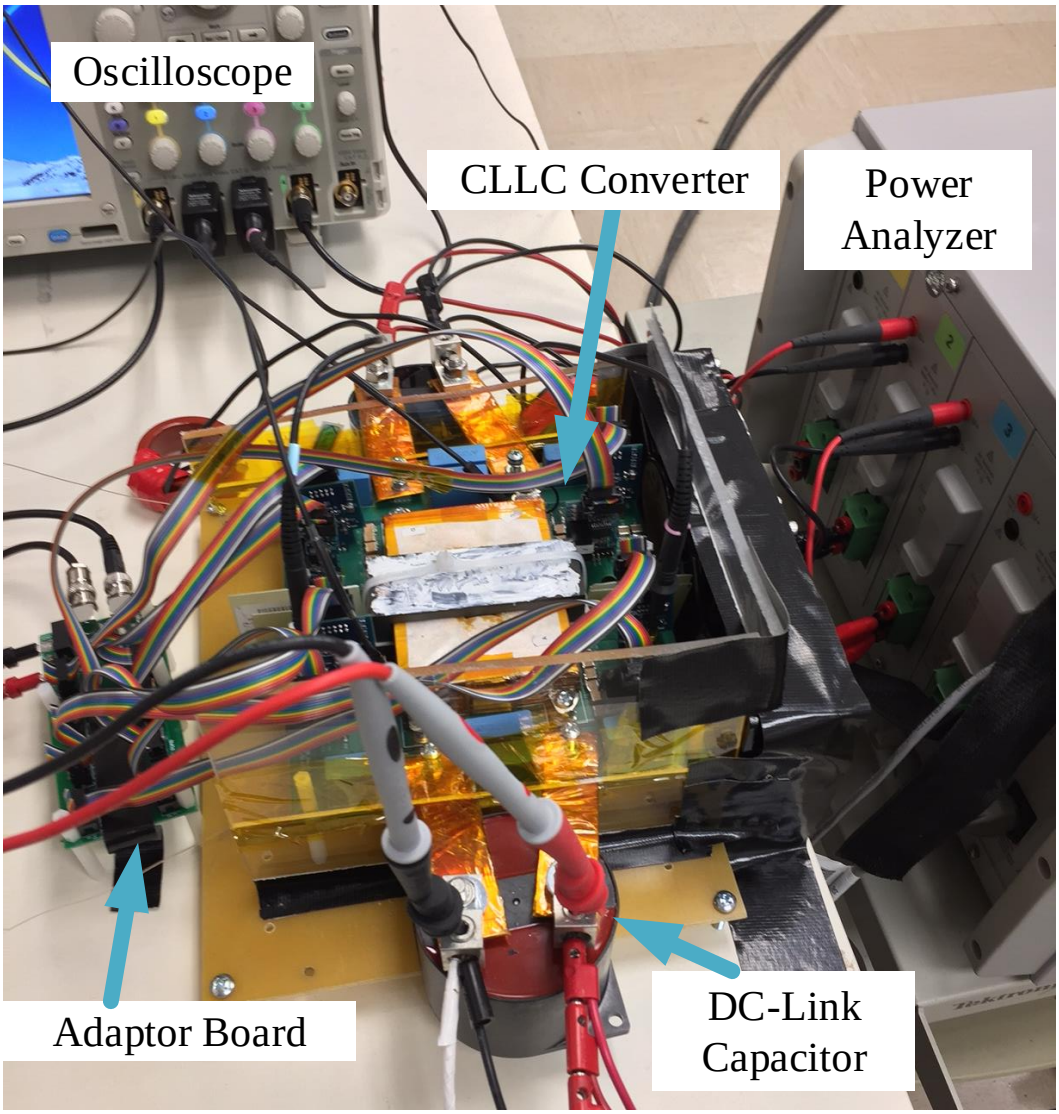



Figure 4.32. Testing setup for 25 kW CLLC converter.


Figure 4.33. Zoomed in CLLC converter waveform under 5 kW load (forward mode) for (1) $I_p$ (10 A/div), (2) $V_{GS,\,S4}$, (3) $V_{GS,\,S2}$, and (4) $V_{ds,\,S2}$.


Figure 4.34. Zoomed in CLLC converter waveform under 5 kW load (forward mode) for (1) $I_p$ (10 A/div), (2) Gate to source voltage $V_{GS,\,S4}$ (3) $V_{GS,\,S2}$ and (4) $V_{ds,\,S2}$.

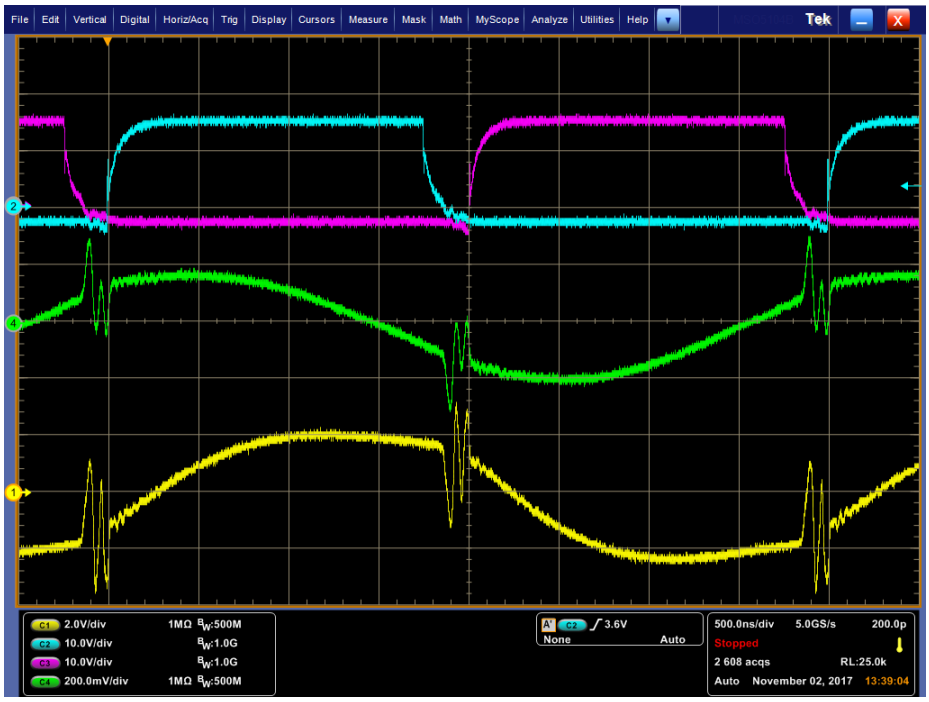



Figure 4.35. CLLC converter waveform under 5 kW load (forward mode) for (1) $I_p$ (10 A/div), (2) $V_{GS,\,S4}$, (3) $V_{GS,\,S2}$, and (4) $I_s$ (20 A/div).

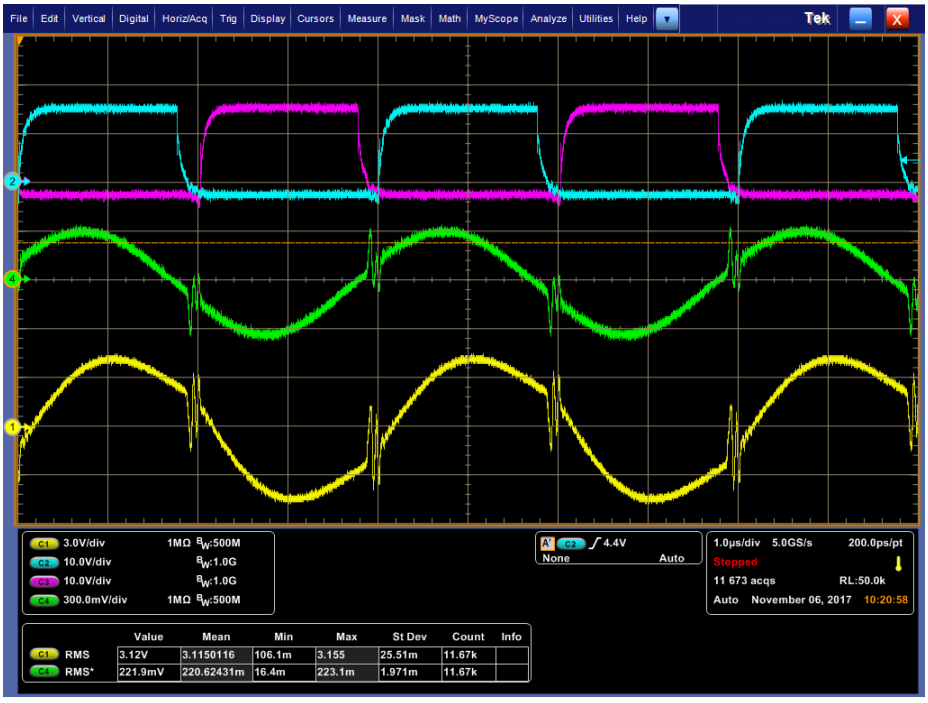



Figure 4.36. CLLC converter waveform under 10 kW load (forward mode) for (1) $I_p$ (15 A /div), (2) $V_{GS,\,S4}$, (3) $V_{GS,\,S2}$, and (4) $I_s$ (30 A /div).

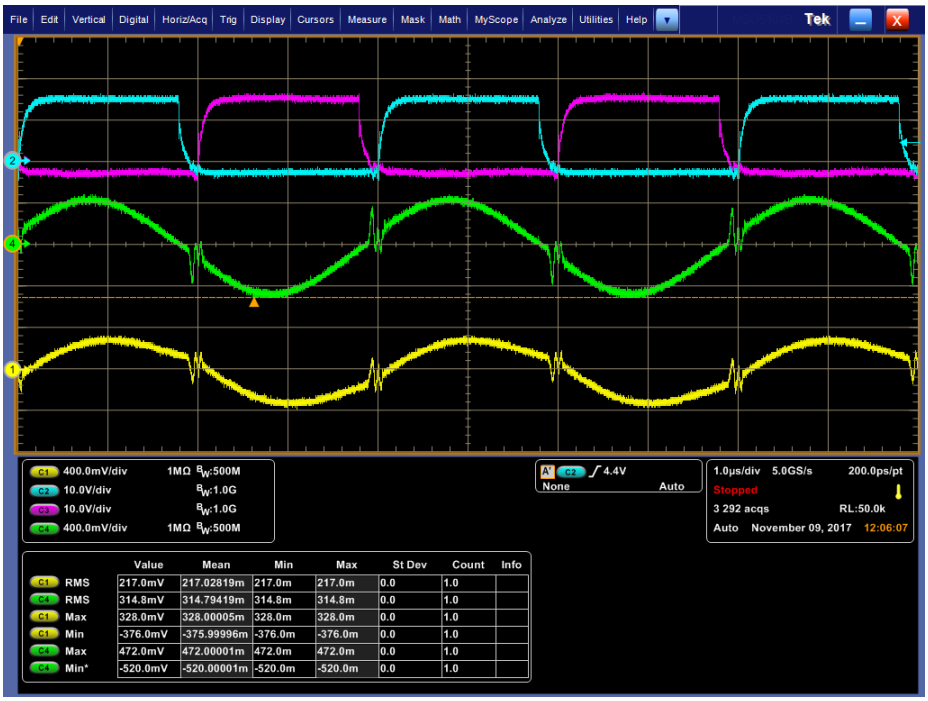



Figure 4.37. CLLC converter waveform under 15 kW load (forward mode) for (1) $I_p$ (40 A/div), (2) $V_{GS,\,S4}$ (3) $V_{GS,\,S2}$ and (4) $I_s$ (40 A/div).

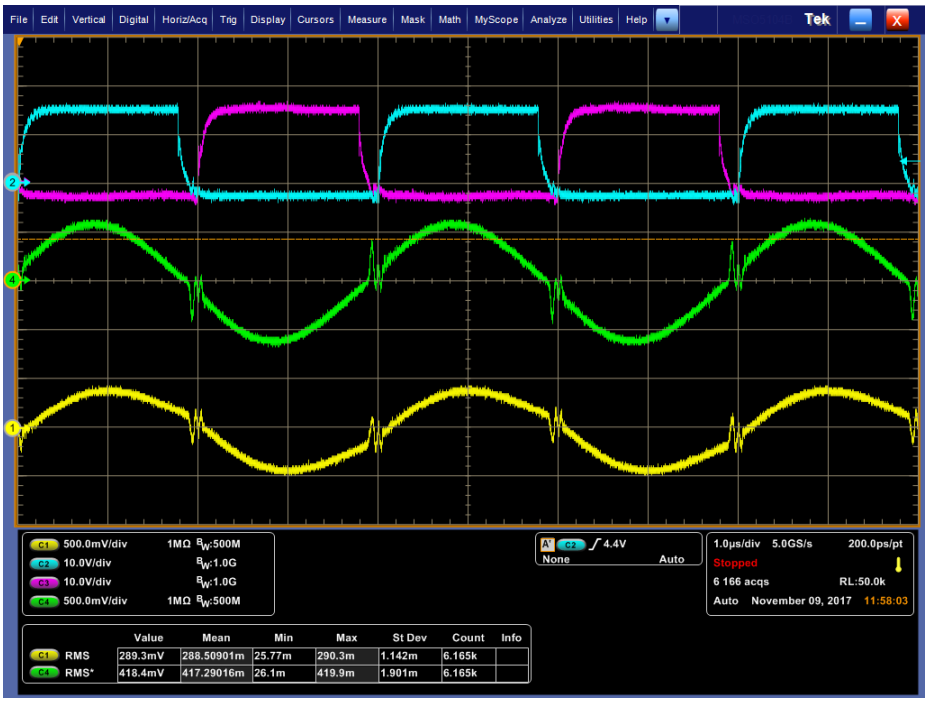



Figure 4.38. CLLC converter waveform under 20 kW load (forward mode) for (1) $I_p$ (50 A/div), (2) $V_{GS,\,S4}$ (3) $V_{GS,\,S2}$ and (4) $I_s$ (50 A/div).

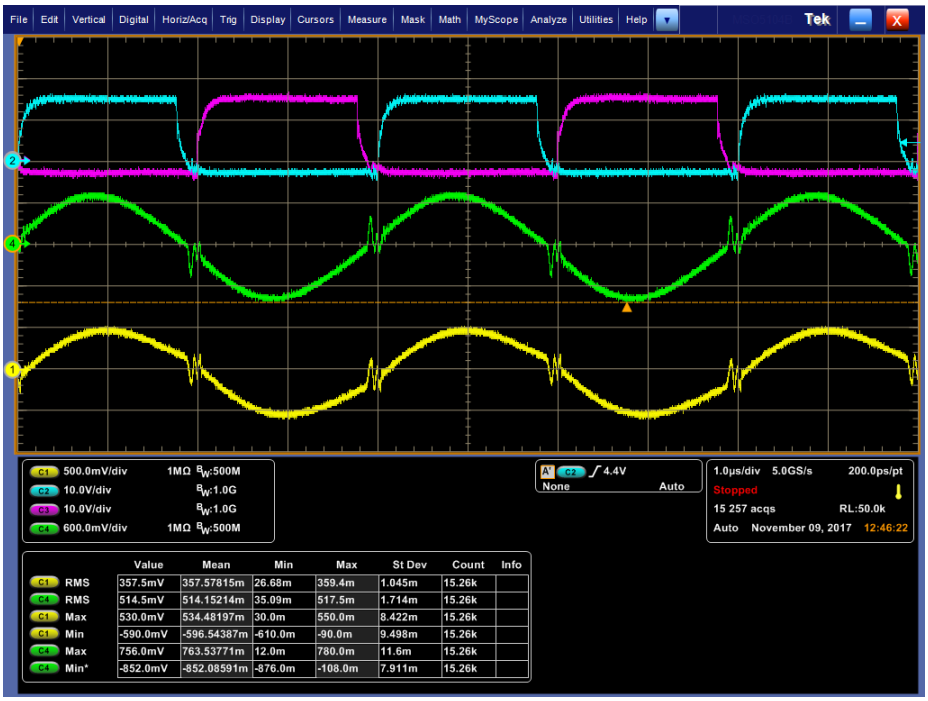



Figure 4.39. CLLC converter waveform under 25 kW load (forward mode) for (1) $I_p$ (50 A/div), (2) Gate to source voltage $V_{GS,\,S4}$ (3) $V_{GS,\,S2}$ and (4) $I_s$ (60 A/div).

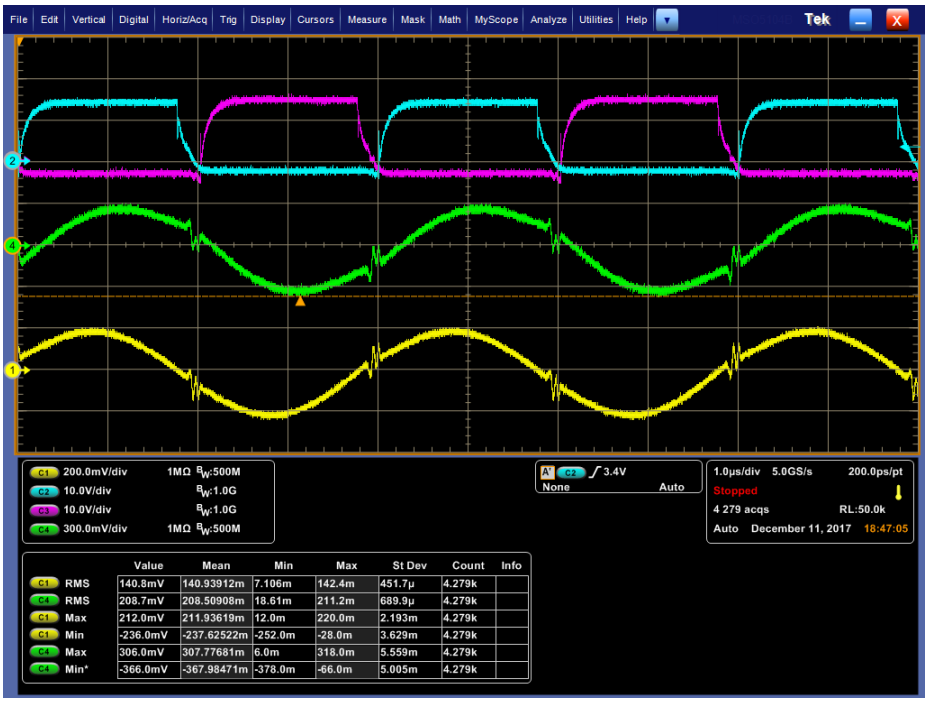



Figure 4.40. CLLC converter waveform under 9 kW load (reverse mode) for (1) $I_p$ (20 A/div), (2) $V_{GS,\,S6}$, (3) $V_{GS,\,S8}$, and (4) $I_s$ (30 A/div).

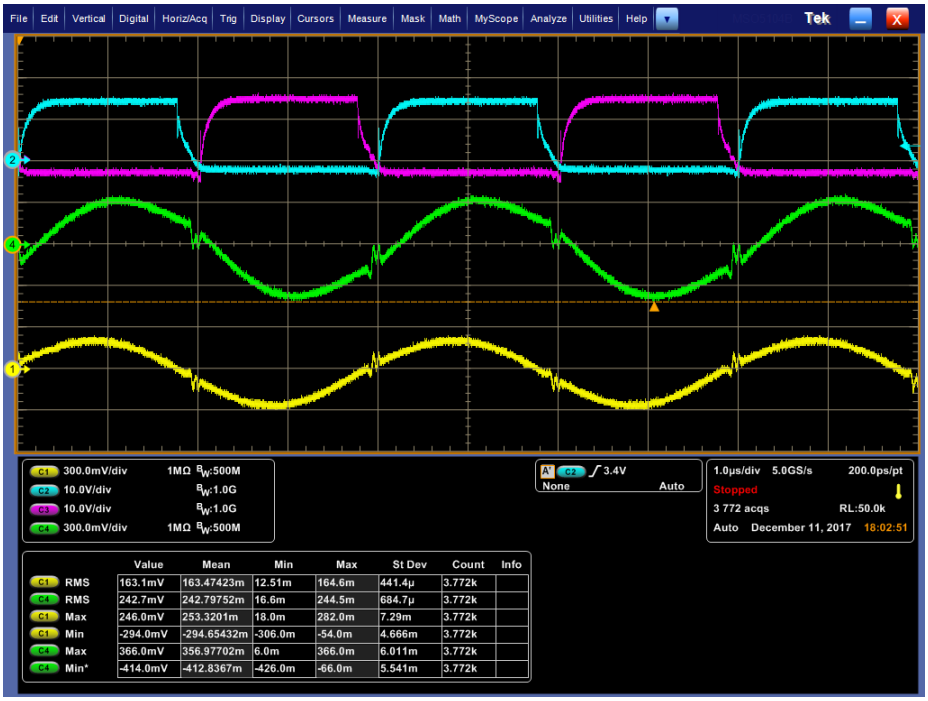



Figure 4.41. CLLC converter waveform under 11 kW load (reverse mode) for (1) $I_p$ (30 A/div), (2) $V_{GS,\,S6}$, (3) $V_{GS,\,S8}$, and (4) $I_s$ (30 A/div).

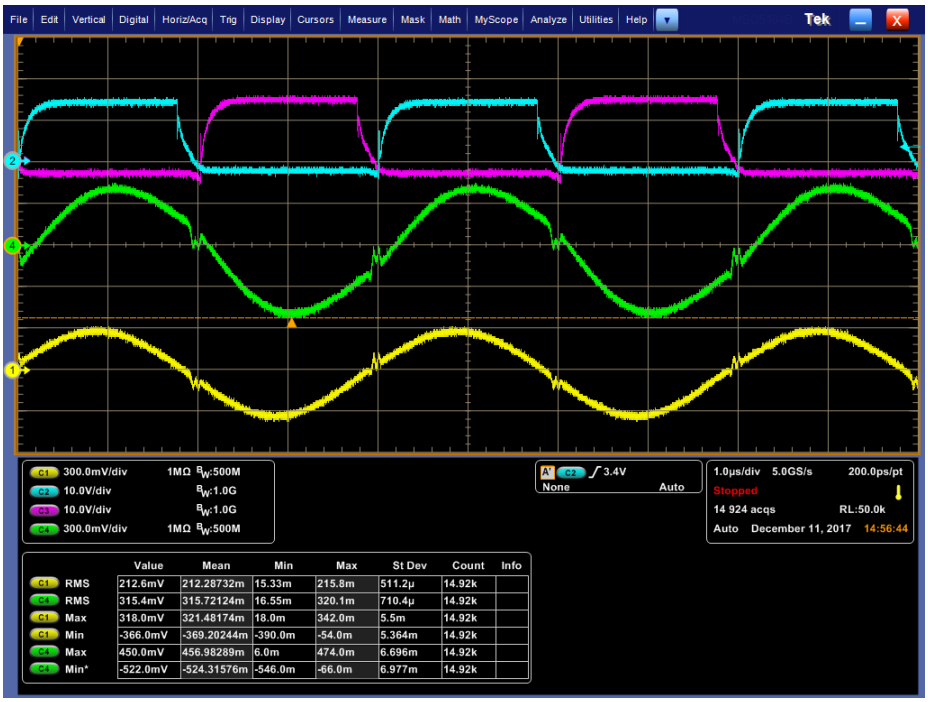



Figure 4.42. CLLC converter waveform under 14 kW load (reverse mode) for (1) $I_p$ (30 A/div), (2) $V_{GS,\,S6}$ (3) $V_{GS,\,S8}$ and (4) $I_s$ (30 A/div).

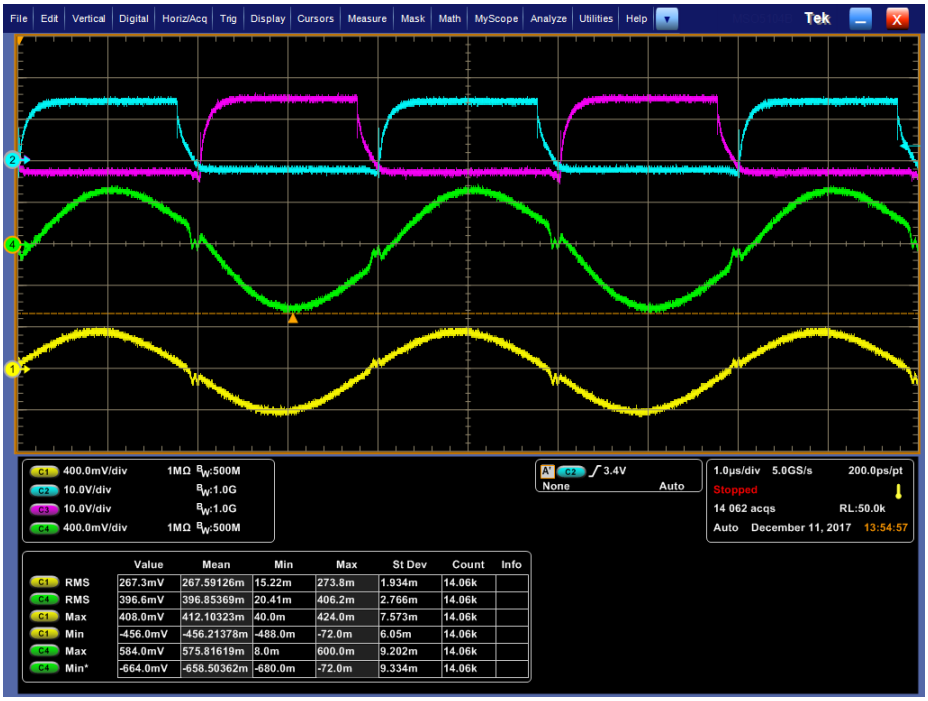



Figure 4.43. CLLC converter waveform under 18 kW load (reverse mode) for (1) $I_p$ (40 A/div), (2) $V_{GS,\,S6}$ (3) $V_{GS,\,S8}$ and (4) $I_s$ (40 A/div).

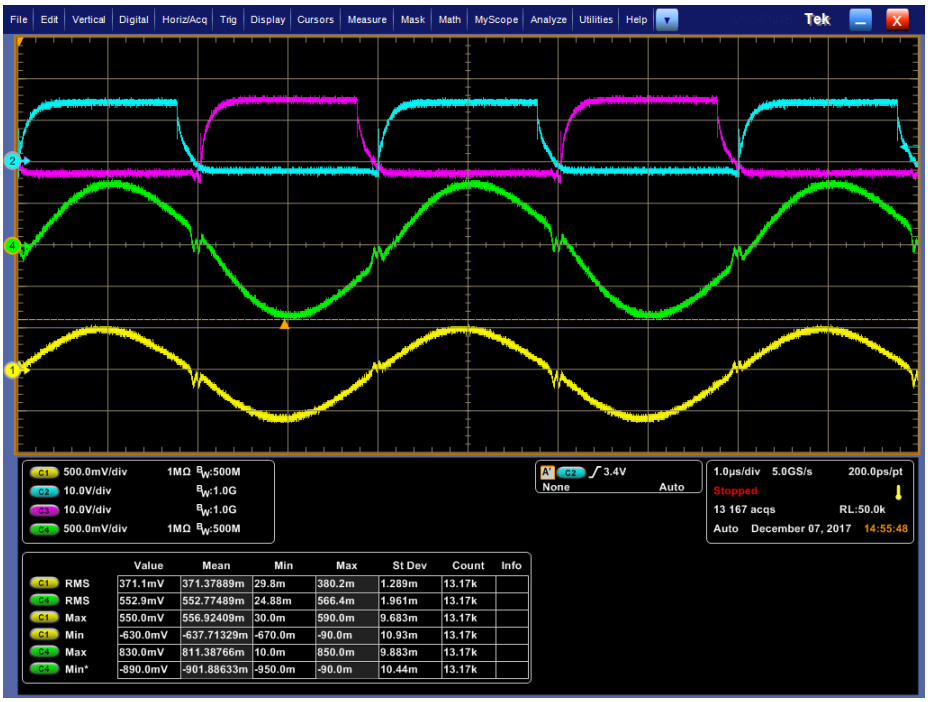



Figure 4.44. CLLC converter waveform under 25 kW load (reverse mode) for (1) $I_p$ (50 A/div), (2) $V_{GS,S6}$, (3) $V_{GS,\,S8}$ and (4) $I_s$ (50 A/div).

The converter efficiency at different output power is shown in Figure 4.45. A peak efficiency of 98.3% at 15 kW is measured under forward mode operation, with a recorded full load efficiency of 98.1% at 25 kW. Under reverse mode operation, a peak efficiency of 98.8% is measured at 17.8 kW. The full load efficiency at 25 kW under reverse mode operation is 98.5%. The power analyzer setup used to measure the converter efficiency was verified. Therefore, the difference in the efficiency values between forward and revere modes are most likely contributed by the difference in device characteristics between X3M0016120K and C3M0010090K.

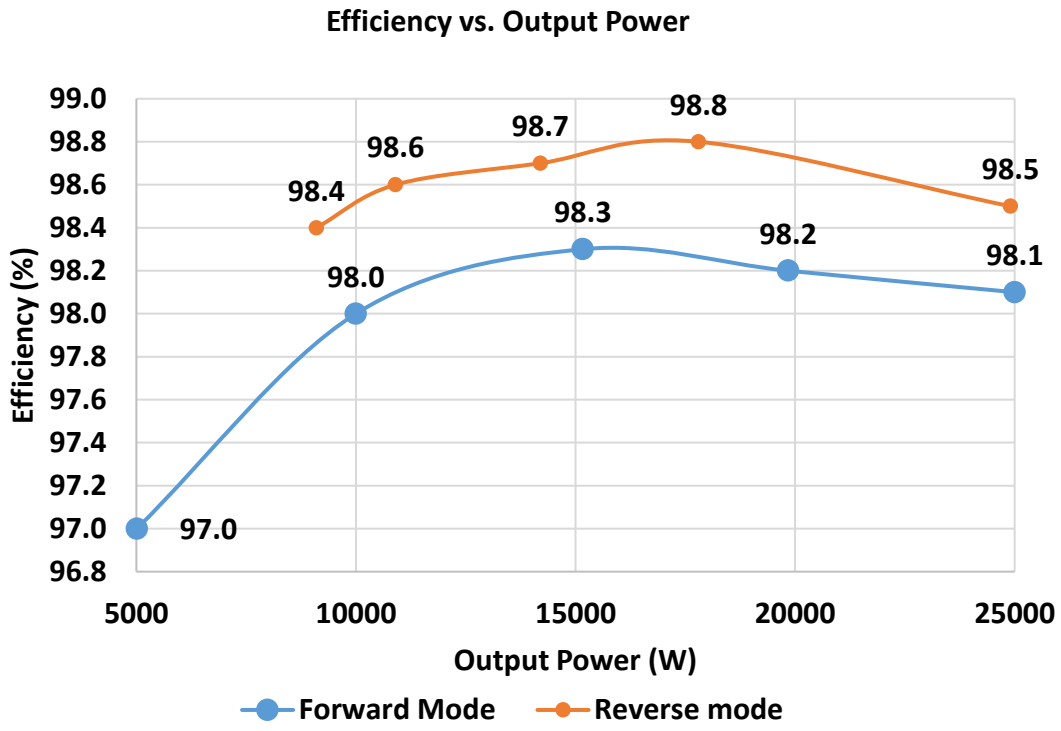



Figure 4.45. Converter Efficiency measurement at different output power level.

# Chapter 5 Conclusions and Future Work

Galvanic isolation is typically required in bidirectional power distribution systems. Traditionally, this isolation is achieved via a line-frequency transformer, which tends to be bulky and heavy. However, due to recent advancements in wide-bandgap semiconductor devices, bidirectional isolated DC/DC converters can be designed to possess high efficiency and high power density. Consequently, the feasibility to achieve the required galvanic isolation with these converters in a bidirectional power distribution system has been drastically improved.

A survey of the latest generation SiC MOSFETs was performed. The key parameters of the devices under consideration were compared against each other. It was found that the most suitable devices under the given specifications were X3M0016120K 1.2 kV 16 mΩ and C3M0010090K 900 V 10 mΩ SiC MOSFETs from Wolfspeed.

Two of the most commonly utilized bidirectional isolated DC/DC converter topologies, dual active bridge and CLLC resonant converter were then introduced. The operating principle of these converter topologies were discussed. A comparative analysis between the two converter topologies focusing on total device loss was also performed. It was found that under the given specifications, the CLLC resonant converter has lower total device loss compared to the dual active bridge converter across a range of switching frequencies. It was also determined that the total loss in the CLLC resonant converter is the lowest at 250 kHz when the loss in the isolation transformer were also considered.

A prototype for the CLLC converter has been designed and assembled to operate at a rated power of 25 kW. The intended switching frequency for the converter prototype

is 250 kHz with 250 ns deadtime. Given the relatively high switching frequency, these factors were considered during the design stage of the gate driver circuitry.

- Symmetry in the propagation delay of the gate-driver output
- The rise and fall times of the gate-driver output
- Common mode transient immunity
- Isolation capacitance of the isolated power supply in the gate driver circuitry
- Short-circuit protection detection and soft shut-down mechanisms in the gate-driver circuitry
- Peak current in the gate loop

In terms of the layout for the gate driver board and the power stage, the design was performed such that the stray inductance in the gate loop and the commutation path was minimized.

Double pulse testing was performed for both X3M0016120K 1.2 kV and C3M0010090K 900 V MOSFETs under different external gate resistance and DC bus voltage values. Both devices were tested up to 30 A turn-off current, which is higher than during the expected peak turn-off current during converter operation under full load. From the results of the double pulse tests, it can be found that the gate-driver circuitry is functional at the rated bus voltage and the stray inductance in the commutation path is small enough such that the voltage overshoot during device turn-off is not large enough to damage the device.

The converter waveforms at different output power levels were captured and ZVS operation for the devices were verified. A peak efficiency of 98.3% at 15 kW is measured under forward mode operation, with a recorded full load efficiency of 98.1% at 25 kW.

Under reverse mode operation, a peak efficiency of 98.8% is measured at 17.8 kW. The full load efficiency at 25 kW under reverse mode operation is 98.5%. The resulting converter power density is 78 W/in$^3$.

In order to further extend the research in this area, the following topics may be considered:

1) Optimization of transformer design

The loss in the isolation transformer constitute a significant portion of the total loss in the CLLC resonant converter. To further increase the converter efficiency, the design of the isolation transformer needs to be investigated further. The selection of appropriate magnetic core material would help in minimizing the core loss. An investigation on the optimal winding arrangements would provide insight on how to achieve further reduction in the winding loss. Additionally, it needs to be determined whether integrating the required inductance for the CLLC resonant tank into the isolation transformer would lead to optimal converter efficiency and power density.

2) CLLC resonant converter start-up behavior

The CLLC resonant converter is rarely a stand-alone system. A typical application for this converter is to provide galvanic isolation in a bidirectional power distribution system. The CLLC resonant tank in the converter would impose a very low input impedance during the system start-up sequence. Therefore, the devices could be subjected to large current stress that leads to converter failure. A study on different system-level control schemes could help to minimize or eliminate this potential failure mode.

3) Packaging for the silicon carbide devices

Currently, a lot of the available discrete SiC power MOSFETs are in a TO-247 package. The impact on the converter performance from the stray inductance and capacitance become much more pronounced at higher switching frequencies and power levels. Therefore it would be of great benefit to explore device packaging techniques that would minimize these stray components. Additionally, an alternative device package that has lower junction to case thermal resistance would reduce the thermal requirement in the overall system. This could further improve the overall system efficiency, power density and cost.

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