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Dynamic R_{ON} Free 1.2 kV Vertical GaN JFET

Xin Yang, *Student Member, IEEE,* Ruizhe Zhang, *Graduate Student Member, IEEE,* Bixuan Wang, *Student Member, IEEE,* Qihao Song, *Graduate Student Member, IEEE,* Andy Walker, *Member, IEEE,* Subhash Pidaparthi, *Member, IEEE,* Cliff Drowley, *Senior Member, IEEE,* and Yuhao Zhang, *Senior Member, IEEE*

***Abstract*—Dynamic on-resistance (R_{ON}) or threshold voltage (V_{TH}) instability caused by charge trapping is one of the most crucial reliability concerns of some GaN high-electron mobility transistors (HEMTs). It has been unclear if this issue can be resolved using an alternative GaN device architecture. This work answers this question by characterizing, for the first time, the dynamic R_{ON} and V_{TH} stability of an industrial vertical GaN transistor-NexGen's 1200V/70mΩ fin-channel JFET, fabricated on 100 mm bulk GaN substrates. A circuit setup is deployed for the in-situ measurement of the dynamic R_{ON} under steady-state switching. The longer-term stability of R_{ON} and V_{TH} is tested under the prolonged stress of negative gate bias and high drain bias. The vertical GaN JFET shows nearly no R_{ON} or V_{TH} shift in these tests, which could be attributed to the low defect density of the GaN-on-GaN homoepitaxial growth, the absence of electric field crowding near the surface, and the minimal charge trapping in the native junction gate. These results present a critical milestone for vertical GaN devices towards power electronics applications.[1]**

***Index Terms*— power electronics, gallium nitride, JFET, on-resistance, threshold voltage, stability, reliability**

I. Introduction

Gallium nitride (GaN) high-electron mobility transistor (HEMT) has been recently commercialized up to 900 V and deployed in numerous applications [1]–[3]. A well-known reliability issue of some GaN HEMT is dynamic on-resistance (R_{ON}), where the R_{ON} after device turn-on is much higher than its DC value [4], [5]. This issue can induce a higher conduction loss of the device [5] and a degraded device lifetime [6] in applications. A decade of study has revealed its physical origins to be the threshold voltage (V_{TH}) instability and the electron trapping in the GaN buffer or passivation interface [4], [7]. However, it is still under debate if such an issue is inherent to GaN devices in general or can be eliminated by deploying alternative device structures.

Recently, vertical GaN devices have gained great traction for medium-voltage applications [8]–[10]. Industrial transistors with various structures have been reported [11]–[14]. Among them, the normally-off vertical GaN fin-channel junction-gate field-effect transistor (JFET) has shown several advantages including low specific R_{ON} and high-temperature stability [14], [15], as well as the high avalanche and short-circuit robustness [15]–[18]. However, its dynamic stability and reliability remain to be comprehensively evaluated.

To date, dynamic R_{ON} testing has only been reported on one vertical GaN diode [19] and is still lacking in vertical GaN transistors. Compared to diodes, transistors additionally include a gate stack and a gated channel, both of which have been shown to significantly impact device R_{ON}. As an evidence, the gate-bias induced instability reported in an early vertical GaN MOSFET [20] suggest the transistor reliability could be more complicated than diode.

During hard switching in power converters, power transistors simultaneously experience high current and high voltage. Such a stress is not experienced by power diodes (also true for GaN p-n diode, as it has minimal reverse recovery current [21]). More importantly, such hard-switched stress can cause dynamic R_{ON} in GaN HEMTs. The stress can produce a large number of hot electrons in the gated channel and their trapping deteriorates the dynamic R_{ON} [22], [23]. This suggests that a diode's dynamic R_{ON} results cannot be convincingly extended to transistors.

On the other hand, accurate characterization of dynamic R_{ON} is vital. The pulse I-V method or the single-event double-pulse test (DPT) method have produced inconsistent results, because a) the device operation in the former method is usually not an inductive switching, and b) the latter method does not specify the device blocking time before switching and ignores the accumulated trapping effect [5], [24]. To evaluate dynamic R_{ON} for practical power applications, it is now a consensus that the in-situ circuit measurements are required under the steady-state switching conditions [24], [25].

In addition to dynamic R_{ON}, the V_{TH} stability is critical for power electronics applications. The V_{TH} instability could not only impact the dynamic R_{ON} but result in false device turn-on through interactions with the gate loop parasitics [26]. In SiC, over a decade of study has revealed a superior reliability and stability of the JFET gate as compared to the MOSFET gate [27]. However, whether this superiority also holds for vertical GaN JFETs remain an open question, as the fabrication process of SiC and GaN JFETs are very different. While the SiC JFET gate is made by the p-type ion implantation, the GaN JFET gate is fabricated by p-GaN regrowth [15].

This work presents the first dynamic R_{ON} characterization of a vertical GaN transistor under steady-state switching. In addition, the longer-term R_{ON} and V_{TH} stability are tested under the prolonged stress of gate-source bias (V_{GS}) and drain-source bias (V_{DS}). In addition to the vertical GaN JFET, similarly-rated

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X. Yang, R. Zhang, B. Wang, Q. Song, and Y. Zhang are with the Center of Power Electronics Systems, Virginia Polytechnic Institute and State University, Blacksburg, VA 24060 USA (e-mail: yhzhang@vt.edu).

A. Walker, S. Pidaparthi, and C. Drowley are with NexGen Power Systems Inc., Santa Clara, CA 95051 USA. (email: SubhashP@nexgenpowersystems.com)

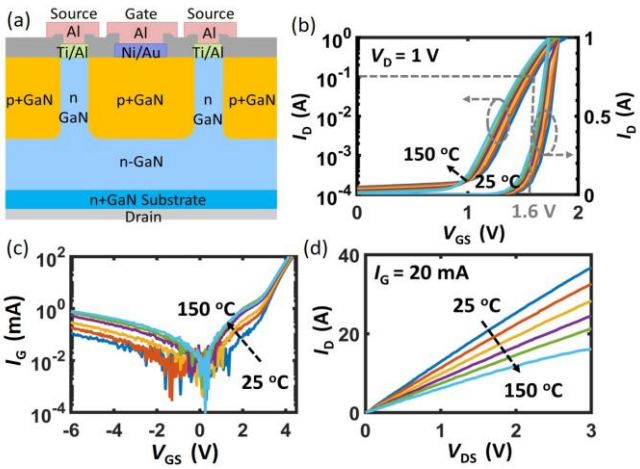

Fig. 1. (a) Schematic of the vertical GaN JFET. (b) Transfer characteristics, (c) gate current characteristics and (d) output characteristics of 1.2 kV vertical GaN JFET at 25-150 ºC with a 25 ºC incremental step.

commercial GaN HEMTs and SiC MOSFETs are tested under the same setups. The vertical GaN JFET shows no dynamic R_{ON} or V_{TH} shift in these tests. This result fills a significant gap in the stability and reliability of GaN power devices.

II. Device Under Test

The devices under test (DUTs) include the 650V/200mΩ and 1200V/70mΩ rated GaN JFETs fabricated by NexGen Power Systems, as well as commercial 650 and 1200 V SiC MOSFETs (IMZA65R083M1H, C3M0075120D), and 650-V GaN HEMT (GS-065-011-1-L). From the different types of commercially available GaN HEMTs, we selected a GaN HEMT with the Schottky-type p-GaN gate (i.e., GaN SP-HEMT), which is a mainstream structure widely deployed by many device vendors and foundries [5].

Fig. 1(a) shows the cross-sectional schematic of NexGen's vertical GaN JFET fabricated on 100-mm bulk n^+-GaN substrates. The sub-micrometer wide, 1 µm high n-GaN fin channels are surrounded by p-GaN gate. The net donor concentrations in the n-GaN fin and drift region are ~10^{17} cm^{-3} and ~10^{16} cm^{-3}, respectively, and the magnesium concentration in p-GaN is ~10^{19} cm^{-3}. The drift region thickness of 650-V and 1200-V JFETs are ~8 and ~10.5 µm with an avalanche breakdown voltage of ~800 V [17] and ~1500 V [15], respectively. The JFETs are assembled in DFN packages.

Fig. 1(b)-(d) shows the transfer, gate-source junction, and output characteristics of the 1200-V vertical GaN JFET from 25 ºC to 150 ºC. The V_{TH} is extracted to be 1.6 V at 0.1 A drain current (I_D) at 25 ºC, and decreases to 1.45 V at 150 ºC (Fig. 1(b)). The I_G-V_{GS} characteristics exhibit p-n junction behavior with gate current (I_G) < 0.4 mA at V_{GS} = -6 V, ramping up at V_{GS} > 3 V, and reaching ~0.1 A at V_{GS} = 4 V (Fig. 1(c)). At I_G of 20 mA (similar to the circuit operation condition), R_{ON} is extracted to be ~70 mΩ at 25 ºC and ~150 mΩ at 150 ºC (Fig. 1(d)). The static R_{ON} at a specific temperature can be modeled using the 25 ºC value and a temperature coefficient of 0.64 mΩ/ºC.

III. Dynamic On-Resistance Test

Dynamic R_{ON} is measured using a continuous, hard-switching DPT with an active measurement circuit. The test circuit schematic for tests under 400 V is shown in Fig. 2(a). To minimize the reverse recovery loss, a GaN HEMT (GS66508T) in reverse conduction is used as the commutation device. For 800 V tests, a 1200 V SiC Schottky diode (C4D10120) is used as the commutation device. A standard MOSFET driver is used for GaN HEMTs and SiC MOSFETs with an on/off-state driving V_{GS} of 6/-4 V and 16/0 V, respectively.

An *RC*-interface gate driver is used for vertical GaN JFET, (Fig. 2(b)). This gate driver can increase the switching speed while maintaining a low I_G at the steady on-state, thereby reducing the driver loss. Here C_G represents the DUT's gate capacitance. R^G_{ON} and R^G_{OFF} are used to limit the peak gate current during the switching transitions. R_{SS} is used to set the steady state on-current. C_{SS} is used to provide a negative V_{GS} during the turn-off the transient. V_{G+} is the on-state driver voltage. The component optimization for this *RC*-interface

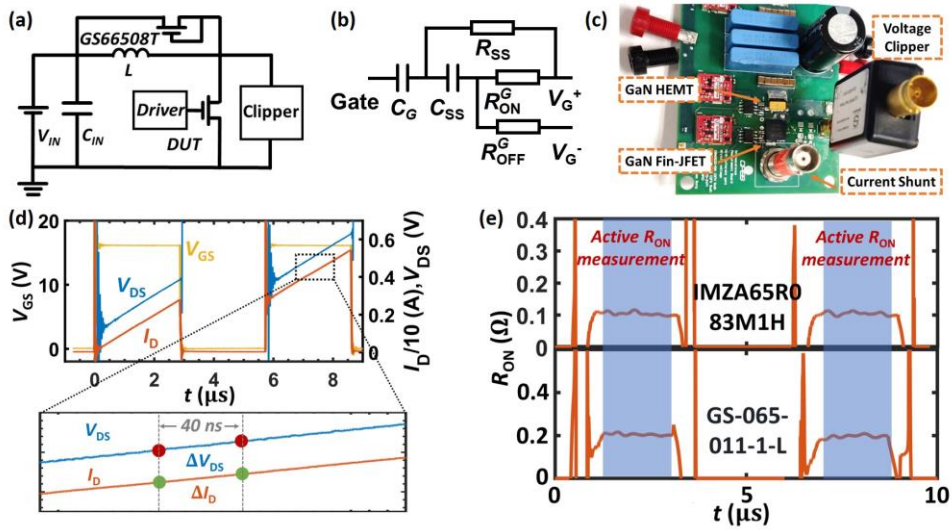

Fig. 2. (a) Circuit schematic of the in-situ dynamic R_{ON} test setup under 400 V. For 800 V test, a SiC diode is used as the commutation device. (b) Schematic of the *RC*-interface driver for vertical GaN JFET. (c) Photo of the prototyped 400V test setup. (d) A cycle of DPT waveform of a SiC MOSFET and the illustration of the R_{ON} extraction based on ΔV_{DS} and ΔI_D. (e) Extracted R_{ON} of 650 V SiC MOSEFT (top) and GaN SP-HEMT (bottom) in a DPT cycle at 400 V V_{IN}.

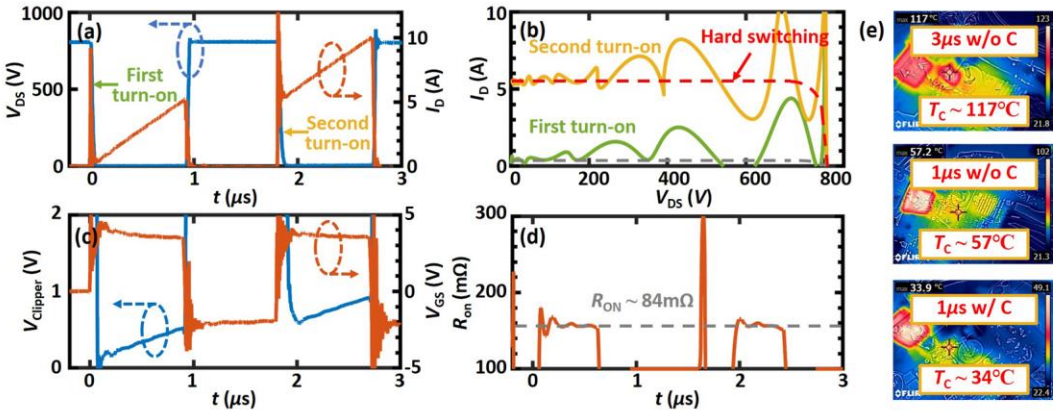

Fig. 3. (a) A cycle of the 800V/10A DPT waveform of the 1200-V vertical GaN JFET. (b) I_D-V_{DS} switching locus of the device turn-on in the first and second pulse. (c) The waveform of the clipper voltage and device V_{GS} in a cycle of the DPT. (d) Extracted dynamic R_{ON} in this DPT cycle; the T_C is 57 ºC in the steady-state operation. (d) Thermal camera images at the steady-state 800V/10A DPT under three conditions: 1) each pulse width is 3 μs and without cooling, 2) each pulse width is 1 μs and without cooling, and 3) each pulse width is 1 μs and with fan cooling.

driver for vertical GaN JFETs is detailed in [28]. Based on the optimization, we select V_{G+} = 12 V, R_{ON} = 4.7 Ω, R_{OFF} = 0 Ω, R_{SS} = 820 Ω, and C_{SS} = 10nF. This set of optimized driver parameters produces a driving I_G of 10~20 mA at 25 ºC to 150 ºC when the device is in the on-state.

The active measurement unit comprises of a voltage clipper (CLP1500V15A1) connected to the DUT for measuring the on-state voltage drop (V_{DS}). This clipper isolates the voltage test point from the high-voltage signal when the DUT is turned-off and connects it to the DUT drain when the DUT is turned-on. Such a technique has been widely adopted for dynamic R_{ON} measurement of GaN HEMTs [6], [29], [30]. During the test, the input voltage (V_{IN}) is fixed by a power supply, while the DUT's V_{GS}, V_{DS} and I_D signals are measured by probes and coaxial current shunt. A photo of the prototyped circuit board is shown in Fig. 2(c).

In each test, the circuit is run for over 10 minutes to ensure the DUT's steady state is achieved with no variations in the DUT's case temperature (T_C) and waveforms. Fig. 2(d) shows the waveforms in one cycle of the continuous DPT for an exemplar DUT (SiC MOSFET). The DUT is switched on twice, each with an on-duration (t_{ON}) of 3 μs. The inductor values are tuned under different V_{IN} to keep the peak I_D around 5 A for the GaN SP-HEMT, SiC MOSFETs, and 650-V GaN JFET. The peak I_D is tested up to 10 A for the 1200-V GaN JFET for measuring the dynamic R_{ON} under a wider current range. The frequency is 1 kHz to ensure the inductor current reduces to zero before the next cycle starts. To intentionally test the dynamic R_{ON} of GaN JFETs at higher T_C, the external cooling is not applied to 650-V GaN JFET, while the fan cooling is applied to the tests of GaN SP-HEMT and SiC MOSFET.

It is reported that the direct R_{ON} calculation using the I_D and the V_{DS} measured by the voltage clipper may be impacted by the common-mode noise and the *RC* discharging delay [6], [25]. Here we extract R_{ON} from the incremental ΔV_{DS} and ΔI_D similar to [6] to cancel the impacts of clipper noise and delay, as illustrated in Fig. 2(d). To also minimize the possible oscilloscope noise, the R_{ON} at moment t_0 is calculated by averaging 500 measurements of R_{ON} spanning a 200 ns period based on the following equation:

$$R_{on}(t_0) = \sum_{t_i=t_0,t_0+0.4ns,\ldots}^{t_0+200ns} \frac{V_{DS}(t_i+40ns)-V_{DS}(t_i)}{I_D(t_i+40ns)-I_D(t_i)} /500 \quad (1)$$

The measurement system and data analysis method are first applied to SiC MOSFETs and GaN HEMTs for calibration and verification. Fig. 2(e) shows the extracted dynamic R_{ON} of the 650-V SiC MOSFET and 650-V GaN SP-HEMT in a DPT cycle at V_{IN} =400 V. The dynamic R_{ON} of the SiC MOSFET is similar to its static value at V_{GS} = 16 V, while the dynamic R_{ON} (~0.2 Ω) of GaN HEMT is larger than its static value (0.15 Ω). This is consistent with prior reports that SiC MOSFET has minimal dynamic R_{ON} variation and GaN SP-HEMT has a dynamic R_{ON} increase of 30~60% under similar conditions [24], [25].

To evaluate the dynamic R_{ON} of 1200-V vertical GaN JFETs under a wider T_C range, we vary the t_{ON} in the DPT test and also apply the external fan cooling. Fig. 3(a) shows the 800V/10A DPT waveform with a t_{ON} of 1 μs. Fig. 3(b) shows the extracted I_D-V_{DS} switching locus of the device turn-on process in the first and second pulses. The turn-on in the second pulse shows a clear inductive hard switching. Fig. 3(c) shows the recorded waveforms of the clipper voltage and device V_{GS}, and Fig. 3(d) shows the extracted dynamic R_{ON}. The GaN JFET shows similar dynamic R_{ON} in the first and second pulses, with the value nearly equal to the static R_{ON} at the same T_C. Fig. 3(e) shows the thermal camera images recorded under the steady-state 800V/10A DPT tests. The T_C drops from 117 ºC at a t_{ON} of 3 μs without external cooling to 57 ºC at a t_{ON} of 1 μs and 34 ºC with the external cooling further applied.

Fig. 4(a)-(d) shows the dynamic R_{ON} as a function of V_{IN} for 650-V SiC MOSFET, 650-V vertical GaN JFET, 650-V GaN SP-HEMT and 1200-V vertical GaN JFET. Based on the T_C measured by thermal camera, the dynamic R_{ON} is normalized to its static R_{ON} at the same T_C measured by curve tracer. Note here we put a 2X I_D on the 1200-V GaN JFET and no cooling on the 650-V GaN JFET to measured their dynamic R_{ON} under high T_C. Fig. 4(e) shows the dynamic R_{ON} of 1200-V vertical GaN JFET as a function of the peak I_D with V_{IN} = 800 V. Fig. 4(f) shows the dynamic R_{ON} of 1200-V vertical GaN JFET as a function of T_C under the same 800V/10A DPT test, with the T_C modulated by t_{ON} and the external cooling.

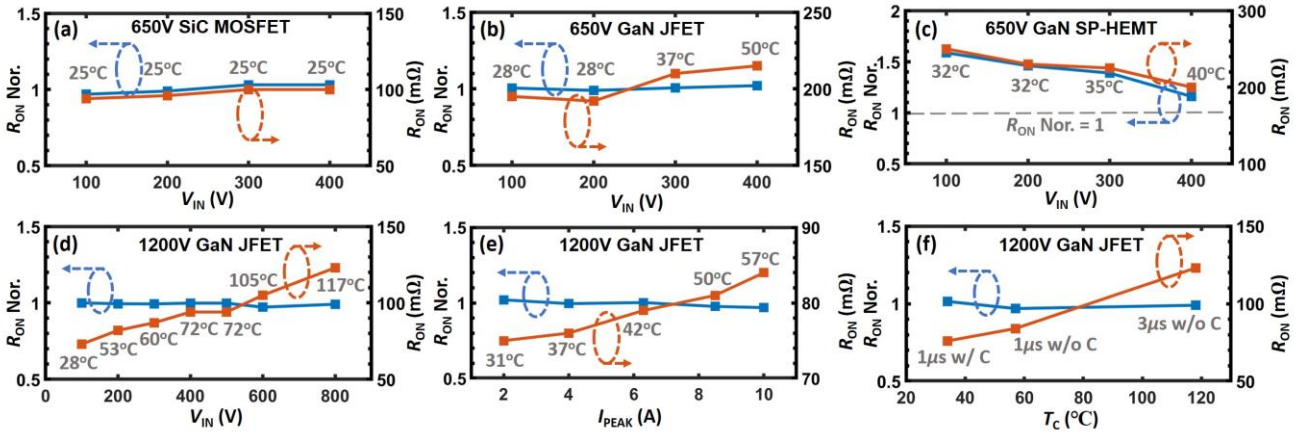

Fig. 4. Extracted dynamic R_{ON} and the normalized dynamic R_{ON} as a function of V_{IN} for (a) 650-V SiC MOSFET, (b) 650-V GaN JFET, (c) 650-V GaN SP-HEMT, and (c) 1200-V GaN JFET. The case temperatures are marked. Each pulse width is 3 μs. Fan cooling is applied to SiC MOSFET and GaN SP-HEMT, while no external cooling is applied to GaN JFET. Extracted dynamic R_{ON} and the normalized dynamic R_{ON} of the 1200-V GaN JFET (e) as a function of peak I_{DS} at V_{IN} = 800 V and each pulse width of 1 μs and (f) as a function of T_C under the same 800V/10A steady-state DPT with and without cooling.

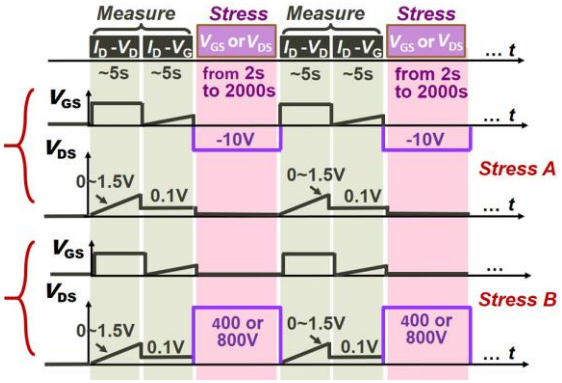

Fig. 5. Illustration of the bias conditions for the two static stress tests. The V_{GS} of I_D-V_{DS} sweep is 6 V, 4 V, and 22 V for GaN HEMT, GaN JFET, and SiC MOSFET, and V_{GS} range in the I_D-V_{GS} sweep is 0~3 V, 0~3 V, and 0~6 V, respectively.

As shown in Fig. 4(b) and Fig. 4(d)-(f), the dynamic R_{ON} of vertical GaN JFETs under various V_{IN}, I_D and T_C conditions are found to be only induced by the elevated T_C with the normalized value being constant unity. In contrast, as shown in Fig. 4(c), the dynamic R_{ON} of GaN SP-HEMT is 20~60% higher than its static value, and the dependence on V_{IN} is similar to prior report [5], [25]. The results show 650-V and 1200-V GaN JFETs are both dynamic R_{ON} free.

IV. Static Stress Test

Static-stress testing is employed to investigate the impact of the longer-term off-state V_{GS} and V_{DS} stresses on the stability of R_{ON} and V_{TH}, which is relevant to applications where the device is primarily in the off-state. The test is performed on a Keysight B1505 Power Device Analyzer, and the test scheme is shown in Fig. 5. The static stresses are applied intermittently with the stress time exponentially increased from 2 s to 2000 s. The output and transfer characteristics are swept between two stresses to extract R_{ON} and V_{TH}. Such a sweep of two characteristics takes about 10 s, so the measured parametric shifts reflect those that cannot recover within a few seconds (i.e., the longer-term dynamic parametric shift as compared to the dynamic R_{ON} extracted in Section III). In this work, two types of stress are applied: a) V_{GS} = -10 V and V_{DS} = 0 V, and b) V_{DS} = 400/800 V for 650/1200 V rated devices and V_{GS} = 0 V.

Fig. 6 shows the extracted R_{ON} and V_{TH} evolution under the V_{GS} and V_{DS} stress test for 650-V GaN SP-HEMT, 1200-V vertical GaN JFET, and 1200-V SiC MOSFET, all measured at both 25 °C and 150 °C. The GaN JFET shows a 0.05% max V_{TH} shift and 1.38% max R_{ON} shift. The SiC MOSFET shows only small V_{TH} shift <5% under V_{GS} stress, which can be possibly explained by oxide trapping [31]. In contrast, the V_{TH} and R_{ON} of GaN SP-HEMT show up to 20% and 10% shifts under the negative V_{GS} stress, respectively, which can be explained by the electron trapping in the p-GaN/AlGaN/GaN gate stack [32]. Under the high V_{DS} stress, bidirectional V_{TH} and R_{ON} shifts are observed in GaN SP-HEMT at 25 °C and 150 °C, which can be explained by the concurrence and competition of a) the hole deficiency in the p-GaN gate [33] and b) the impact ionization in the GaN channel and the followed hole removal through the p-GaN gate [34]–[36].

V. Discussion on Physical Mechanism

The results presented in prior sections show the superior dynamic R_{ON} and V_{TH} stability performance of the vertical GaN JFET when compared to the lateral GaN SP-HEMT. Before discussing the relevant physical mechanisms, we would like to clarify that the performance of the GaN SP-HEMT tested in this work may not be representative of all types of GaN HEMTs. In the next paragraph, we provide a brief overview of the recent reports on dynamic R_{ON} and V_{TH} stability performance of various types of commercial GaN HEMTs. However, it should be noted that, the focus of this work is not comparing different GaN HEMTs; the brief overview is only to provide relevant context for readers in the broader field.

Other than the SP-HEMT architecture, hybrid-drain gate-injection-transistor (HD-GIT) and cascode GaN HEMT [5] architectures are also used for commercial 600/650V-rated GaN HEMTs. For GaN SP-HEMTs, consistent with our results, a 30-70% dynamic R_{ON} increase at various V_{IN} is also reported in other steady-state circuit measurements [24], [25], [37]. For

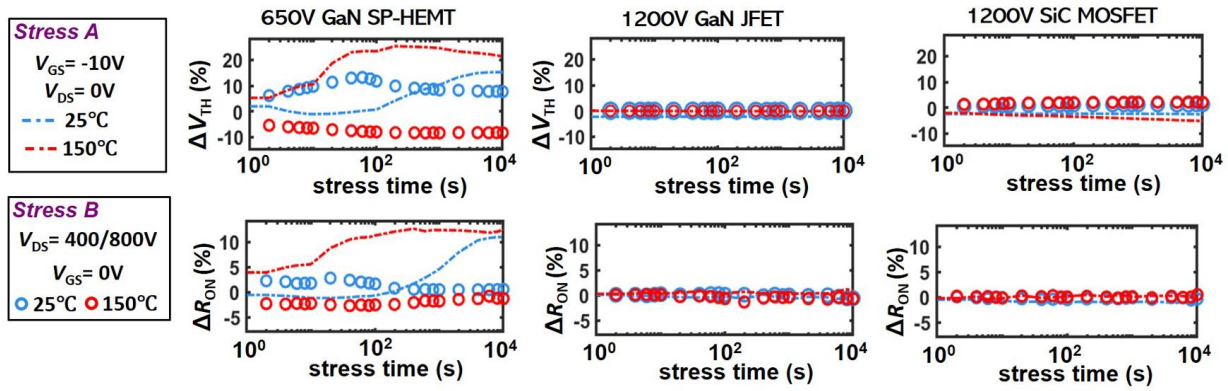

Fig. 6. Percentage of V_{TH} and R_{ON} shift (ΔV_{TH} and ΔR_{ON}) with respect to the static values as a function of the stress time for 650-V GaN SP-HEMT, 1200-V GaN JFET, and 1200-V SiC MOSFET, at 25 and 150 ºC. The dashed lines and circular symbols refer to the shifts under the V_{GS} stress and V_{DS} stress, respectively.

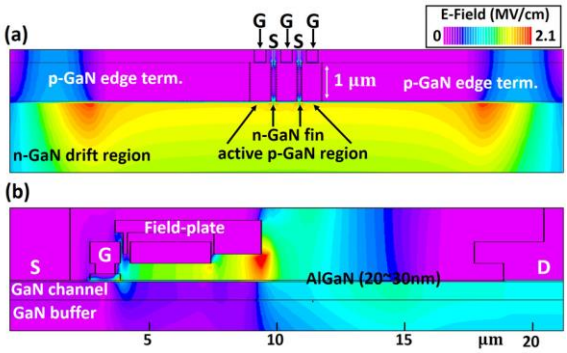

Fig. 7. Simulated electric field contour in (a) 1200 V-rated vertical GaN JFET biased at 800 V and (b) 650 V-rated lateral GaN SP-HEMT biased at 400 V. The structure of GaN HEMT is based on the cross-sectional microscopic image reported in [46], and this GaN HEMT has a breakdown voltage over 1000 V.

GaN HD-GITs, some works reported a smaller dynamic R_{ON} increase under certain circuit operation conditions [37], [38]. For example, a minimal dynamic R_{ON} increase is reported in [38] under soft switching. For cascode GaN HEMTs, a 15-30% dynamic R_{ON} increase is reported in [39] using a single-pulse DPT, while there seems to still lack a report of the steady-state circuit measurement. On the other hand, it is widely reported that the GIT exhibits a superior V_{TH} stability over SP-HEMT under various DC and dynamic stresses [35], [40]–[42] due to the more efficient carrier supply or extraction in the Ohmic-type gate [33], [35].

Despite the variation of GaN HEMTs and their reliability performance, a generic comparison of the electrostatics inside a lateral GaN HEMT and a vertical GaN JFET is helpful to understand the physics behind the absence of dynamic R_{ON} and V_{TH} shift in the vertical JFET. For this, we simulate the electric field contour inside a vertical GaN JFET and a lateral GaN SP-HEMT in Silvaco Atlas based on the physical models similar to [43]–[45]. The structure of GaN SP-HEMT is based on the microscopic images of a commercial device reported in [46].

Fig. 7 shows the simulated electric field (E-field) contour in the two devices at high V_{DS}. In the GaN SP-HEMT, the peak E-field is near the device surface in the active region. The carrier channel is 20~30 nm away from the device surface, easily inducing trapping at the device surface or in the heterostructure [6], [47]. In the GaN JFET, the peak E-field is at the edge termination (implantation-based, similar to [21], [48]); the high E-field in the active region is embedded at the p-n junction, which is far from (~1 µm) the device surface. In addition, due to the lower defect density in GaN epi layers grown on GaN substrate compared to those grown on Si [49], both surface and buffer trapping are largely suppressed. Finally, the native p-n junction gate in JFET has no band discontinuities, enabling the more efficient carrier supply or extraction as compared to the p-GaN/AlGaN/GaN hetero-gate in the HEMTs (particularly with the Schottky contact to p-GaN in SP-HEMT [41]).

VI. Summary

This work presents the first experimental characterization of dynamic R_{ON} and V_{TH} stability in vertical GaN transistors. The dynamic R_{ON} is measured in-situ in a steady-state switching circuit, and the R_{ON} and V_{TH} stability are measured under the prolonged V_{GS} and V_{DS} stresses. Both 650 and 1200 V vertical GaN JFETs show negligible parametric shifts in these tests, revealing significantly superior stability as compared to some GaN HEMTs. These results show the great potential of vertical GaN devices for power electronics applications.

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