Diode Predistortion Linearization for Power Amplifier RFICs in Digital Radios

by

Christopher B. Haskins

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Sanjay Raman, Chair
Charles W. Bostian
Dennis G. Sweeney

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(ABSTRACT)

The recent trend in modern information technology has been towards the increased use of portable and handheld devices such as cellular telephones, personal digital assistants (PDAs), and wireless networks. This trend presents the need for compact and power efficient radio systems. Typically, the most power inefficient device in a radio system is the power amplifier (PA). PA inefficiency requires increased battery reserves to supply the necessary DC bias current, resulting in larger devices. Alternatively, the length of time between battery charges is reduced for a given battery size, reducing mobility.

In addition, communications channels are becoming increasingly crowded, which presents the need for improved bandwidth efficiency. In order to make more efficient use of the frequency spectrum allocated for a particular system, there is a push towards complex higher order digital modulation schemes in modern radio systems, resulting in stricter linearity requirements on the system. Since power efficient amplifiers are typically nonlinear, this poses a major problem in realizing a bandwidth *and* power efficient radio system. However, by employing various linearization techniques, the linearity of a high efficiency PA may be improved.

The work presented in this thesis focuses on diode predistortion linearization, particularly for PA RFICs in digital radios. Background discussion on common linearization techniques available to the PA designer is presented. In addition, a discussion of traditional and modern methods of nonlinearity characterization is presented, illustrating the nonlinear PA effects on a modulated signal. This includes the use of two-tone analysis and the more modern envelope analysis. The

operation of diode predistortion linearizers is discussed in detail, along with diode optimization procedures for PA linearization with minimum impact on return loss and gain. This diode optimization is effective in improving the ability to integrate the predistorter into a single, linearized PA RFIC chip. MESFET and HBT based diode linearizers are studied for use with corresponding MESFET and HBT based PAs in the 2.68 GHz and 1.95 GHz frequency bands, respectively. Results show an improvement in adjacent channel power ratio (ACPR) due to the linearizer in both MESFET and HBT cases. A fully integrated 1.95 GHz linearizer and PA RFIC in HBT technology is also presented. Design considerations, simulations, and layouts for this design are presented. Finally, several recommendations are made for continued research in this area.

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1 Introduction

Amplifier linearity plays a major role in the design of modern communication systems. To accurately decode most modern digitally modulated signals, linear amplification and frequency conversion are necessary throughout the transmit and receive portions of the system. Any amplitude and/or phase distortions on the signal may reduce the ability to decode these signals properly. Due to the limited amount of available frequency spectrum, communications channels are quickly becoming crowded. Claude Shannon's theoretical channel capacity limits are coming within reach and in some cases exceeded (Shannon's limit assumes additive white Gaussian noise (AWGN) channel). Today's communications engineers must find new and innovative ways to reach these limits and possibly push them even further. This push towards increased bandwidth usage presents a need for increased bandwidth efficiency in order to increase system capacities. The current solution is found in more bandwidth efficient modulation schemes, which in turn requires highly linear amplification throughout radio architectures.

Higher order modulation schemes such as QPSK, OQPSK, and $\pi/4$ DQPSK are generally favored for their efficient use of bandwidth; however, they exhibit a non-constant envelope when filtered or pulse shaped. This non-constant envelope is susceptible to nonlinearities in the radio. Constant envelope modulation schemes such as FSK or GMSK may be used, but they have wider main lobes than PSK techniques, and thus are still not as spectrally efficient. Other types of modulation such as QAM exhibit greatly improved bandwidth efficiency at the expense of further susceptibility to nonlinearities due to their large non-constant envelope [1][2].

Several problems arise when the designer requires a linear amplifier in a radio system. The first major problem is that linear amplifiers are generally very inefficient in their use of power. This in turn causes excess current drain on the radio's power supply. In modern mobile and remotely located radios, the power supply is usually a battery, which has a limited lifetime. This mandates the efficient use of current to prolong operating time

and/or reduce battery size. Power added efficiency (PAE) is a common term used to characterize this power amplifier (PA) efficiency and is defined as the following:

$$PAE = \frac{P_1 - P_{IN}}{P_{DC}}, \tag{1.1}$$

where P_1 is the fundamental RF output power, P_{IN} is the RF drive power, and P_{DC} is the DC power. PAE will be used throughout this paper whenever power efficiency is referred to.

The second major problem with the use of linear amplifiers is the cost factor. Typically, a high efficiency, saturating amplifier is simply backed-off from the compression point to an input power point that exhibits the required linearity. This back-off method is quite acceptable and is used widely in industry; however, the cost associated with doing this is high since the designer is using a more expensive, higher power amplifier to do the job. The higher power amplifier must be operated at a lower power output, which could result in the requirement of additional amplifier stages, driving up the overall system cost. Also, even lower PAE results through this back-off technique, leading to a higher current consumption in the desired product. For example, a +30 dBm saturated output power amplifier could be backed-off by 6 dB to achieve the required linearity. The cost difference of purchasing a +30 dBm amplifier versus purchasing a +24 dBm amplifier can be quite high, especially when it is a microwave or mm-wave amplifier.

An alternative to the above back-off method to achieve the required amplifier linearity is through device biasing. *Class A* biased amplifiers exhibit the best linearity but have poor PAE and exhibit a reduced power output. These amplifiers are biased exactly in the middle of their linear region of operation. As long as the RF signal never drives the amplifier out of this linear region, perfect linearity is ideally achieved. Due to the PAE problem and limited power output, these amplifiers are avoided if possible. Amplifiers biased for higher PAE include *Class AB*, *Class B*, and *Class C*. These amplifiers obtain higher efficiency by biasing the device at a low quiescent current (near cutoff) and

allowing the RF input signal to swing the device into conduction. This causes the amplifier to draw less current since it only "turns on" and draws large amounts of current when driven into conduction. These amplifiers are sometimes referred to as *reduced conduction angle amplifiers*. Since these reduced conduction angle amplifiers are operated in a nonlinear region, any envelope information contained in the RF signal will be lost or severely distorted. The phase or frequency information is obtained through harmonic filtering of the nonlinear output, thus is not affected by the nonlinear operation. From this the reader can see that the nonlinear operation of these high efficiency amplifiers is detrimental to a signal containing any envelope information. If some form of linearization technique could be applied to a lower power, more efficient, saturated (nonlinear) amplifier to approach the linearity of a Class A amplifier, significant cost savings could occur while maintaining a decent PAE.

The intended application of focus in this thesis is for *RF integrated circuit* (RFIC) PAs. The increased need for smaller, lightweight, and power efficient circuits in portable devices has led to the need for these RFICs. Since PAs typically consume a large portion of the power in a system, they are an obvious target for power efficiency improvement. In addition, the ability to integrate a given linearization technique is key in reducing overall device size and weight; thus this is an important factor to consider when choosing a linearization technique.

The remainder of Chapter 1 presents an overview of common linearization techniques. The advantages and disadvantages of each technique are discussed. Predistortion linearizers are discussed in detail. Chapter 2 of this thesis discusses the typical nonlinear characteristics that may affect a digitally modulated signal. A traditional two-tone analysis is presented. Common terms such as intermodulation distortion (IMD), peak envelope power (PEP), peak-to-average ratio (PTAR), AM-AM, AM-PM, and adjacent channel power ratio (ACPR) are defined and discussed. The importance of envelope analysis and a brief example concludes Chapter 2. The next two chapters present the details of a diode predistorter optimization. A MESFET based predistorter for a 2.68 GHz MESFET PA is analyzed and optimized in Chapter 3. A HBT based predistorter for a 1.95 GHz HBT PA

Table 1.1 Summary of Common Linearization Techniques

Feedback	Feedforward	Predistortion
Cartesian Loop Polar loop	Basic feedforward	Linear amplification using nonlinear components (LINC)/ combined analog-locked loop universal modulator (CALLUM)
RF feedback	Envelope elimination and restoration (EER)	RF/IF predistortion
Adaptive baseband predistortion		Adaptive baseband predistortion

is analyzed and optimized in Chapter 4. Results are also presented in both of these chapters. Chapter 5 builds on the results of the previous chapters to design and simulate a fully integrated linearized HBT PA RFIC chip. The thesis is concluded in Chapter 6. Recommended areas of future work are suggested. This future work includes the additional fabrication and testing of the fully integrated RFIC chip designed in Chapter 5.

1.1 An Overview of Common Linearization Techniques

A wide range of linearization techniques is available to the modern power amplifier/ communication system designer. These techniques can be roughly classified into three groups: (1) feedback, (2) feedforward, and (3) predistortion. Each of these three groups contains several techniques, which are shown in Table 1.1. Notice that adaptive baseband predistortion falls into both feedback and predistortion groupings [3][4]. These techniques will be briefly described in the following sections.

1.1.1 Cartesian Loop

Cartesian Loop is a form of feedback that involves linearization of the complete transmitter (Figure 1.1). Baseband I and Q signals are upconverted to the carrier frequency and then amplified to the desired power level. This signal is then sampled and downconverted back into quadrature components. The resulting I and Q signals are fed

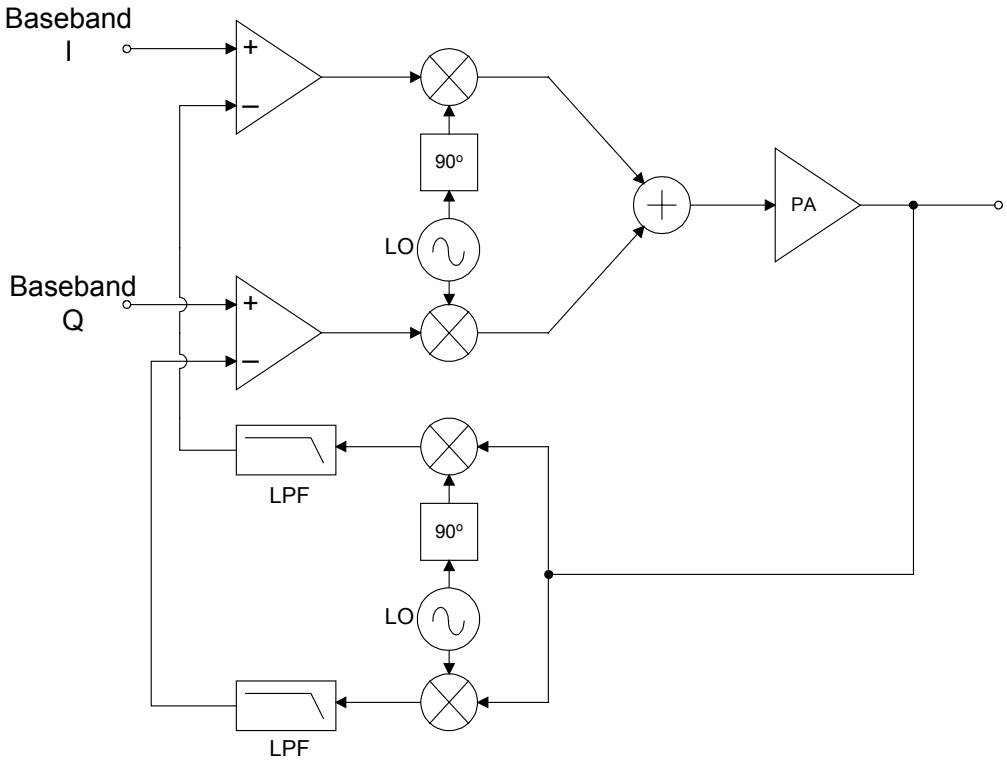


Figure 1.1 Cartesian loop feedback transmitter [3]

back to the transmitter input, where they are compared to the original baseband inputs with error amplifiers.

With this technique, any nonlinearity in the transmitter is effectively cancelled out. The entire process of upconversion and any intermediate stages of amplification are included in the linearization process. One of the main drawbacks of this technique is a limited bandwidth due to delay around the loop. Thus, a compromise must be made between the bandwidth of the feedback loop and linearity improvement. Due to the addition of the feedback demodulators and error amplifiers, the PAE of this system is generally not improved unless the additional components can be implemented in an IC with low power dissipation and a high efficiency power amplifier (e.g. Class C) is used [3].

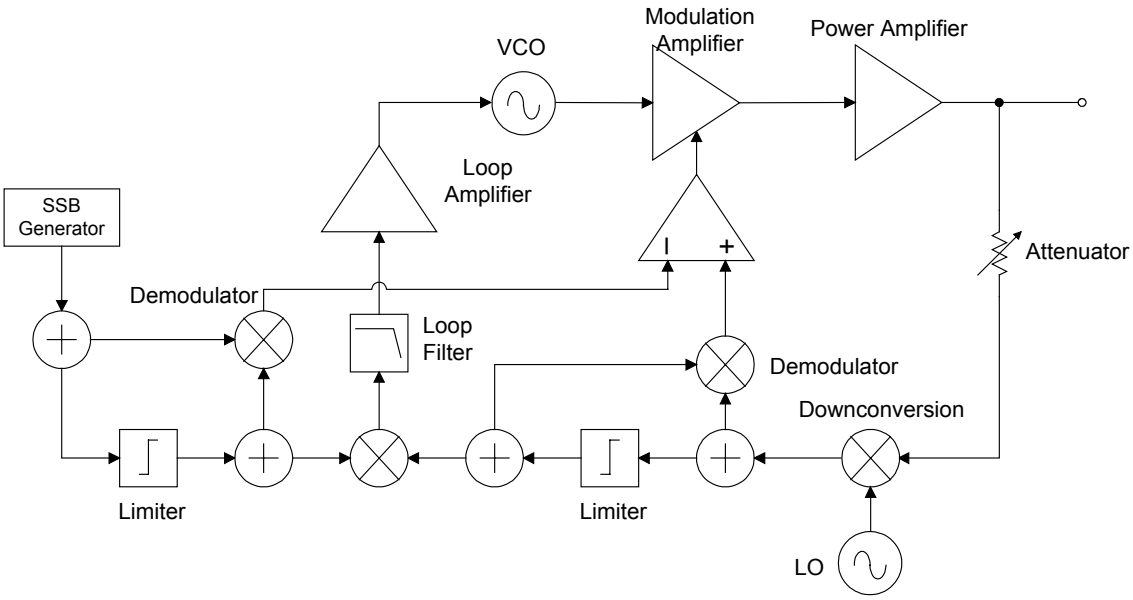


Figure 1.2 Polar loop feedback transmitter [3]

1.1.2 Polar Loop

Another form of feedback that may be used for linearization is *polar loop* [3]. This technique is similar to the Cartesian loop except that amplitude and phase are fed back rather than I and Q (Figure 1.2). A resulting problem with this method is that the required feedback bandwidths for the amplitude and phase components are different from each other for most modulation formats. This limits the available loop gain to either the amplitude or phase path since one path will require a feedback bandwidth that reduces the available loop gain, while the other path may need a larger loop gain. This effectively limits the overall linearity improvement. Essentially, the operation of the phase-feedback path relies on a phase-locked loop; the loop can experience locking problems at low amplitude levels and also have problems tracking abrupt changes in phase, such as those occurring at the envelope minima in a two-tone test. This linearization method is generally not used in practice.

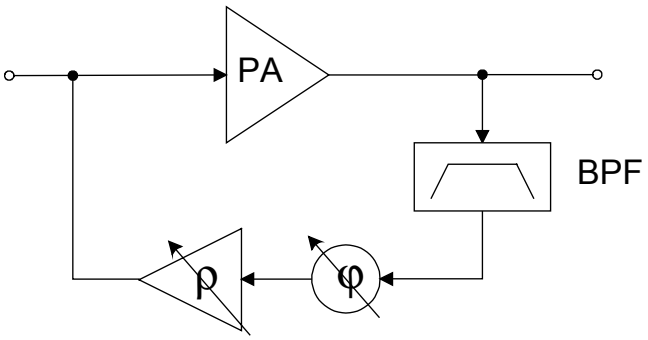


Figure 1.3 RF feedback amplifier with gain and phase adjustment for second harmonic feedback technique [6]

1.1.3 RF Feedback

The above methods all make use of feedback to achieve linearization, but through feedback and modification of the *baseband* inputs to the transmitter. RF amplifier feedback (Figure 1.3) may also be used in the design of the PA to achieve some measure of linearization. One technique makes use of narrowband, negative feedback to the amplifier input. In order to preserve stability and achieve good IMD improvement, the delay in the feedback path must be carefully taken into consideration. Also, a bandlimiting filter must exist in the feedback path for stability [6]. Stability problems limit this technique to narrowband radio systems.

Another form of feedback that has received increased attention in recent years is *second harmonic feedback*. This technique feeds the second harmonic signal produced at the PA output back to the PA input to reduce third order IMD. The nonlinearity of the amplifier causes interaction between the source signals and their fed-back second harmonics. By proper selection of the phase and amplitude of the fed-back second harmonics, it is possible to have the third order IMD produced by the second harmonics be out of phase and equal in amplitude from the original third order IMD. Thus, ideally, the third order IMD may be totally eliminated [7].

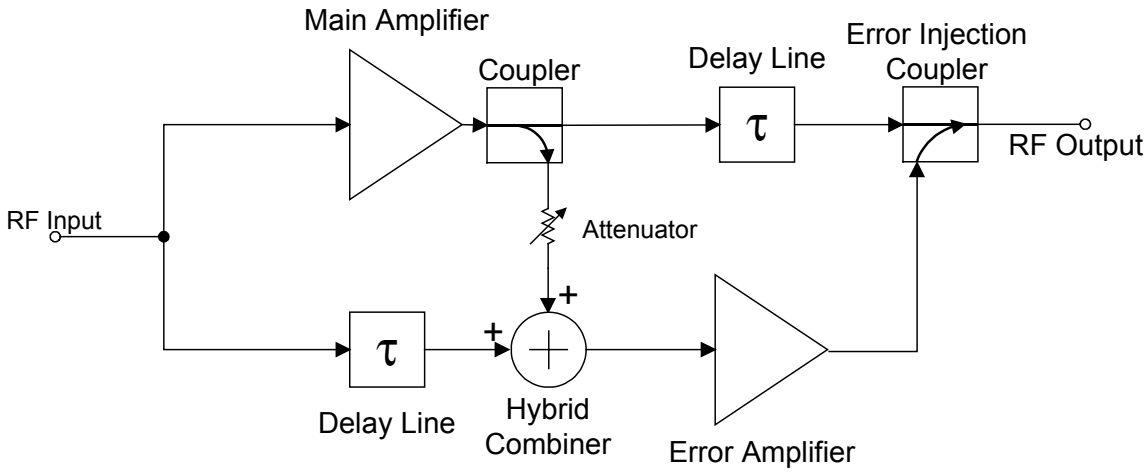


Figure 1.4 Feedforward transmitter [9]

However, this second harmonic feedback technique does have limitations. As stated above, the phase and amplitude in the feedback path must be accurately selected for ideal reduction/elimination of the third order IMD product. Similarly, the second harmonic has also been utilized in the feed-forward technique [8] to reduce spectral regrowth. Spectral regrowth will be discussed in Chapter 2. In [8] the authors state that a phase error of +/- 10° gave an increase of 6 dB in spectral regrowth, while a gain error of +/- 2 dB gave an increase of 8 dB in spectral regrowth, indicating the importance of proper gain and phase matching.

1.1.4 Feedforward

The *feedforward* technique (Figure 1.4) is the subject of considerable active research, and as a result a large number of articles are available in the literature [4][9][10]. Its popularity is due largely to the ability to linearize wideband, multicarrier signals. This technique is conceptually simple, but can become rather costly to implement in hardware. In its simplest form, there are two paths: a signal cancellation path and main RF path. A hybrid splitter divides the power between the two paths. Half of the RF input power is fed through a 180° delay line. The other half of the RF input power is fed to the main PA. IMD is generated in this PA and the output is sampled and fed through a hybrid combiner

where it is combined with the signal in the delay path. Thus, an amplified, distorted signal is combined with the original input signal, which has been delayed by 180°. With an adjustable attenuator in line with the sampled (coupled), distorted signal to adjust for amplitude matching between the two signals, the main signal is exactly cancelled out while the distortion products feed through the combiner. These distortion products are then amplified by a highly linear class A error amplifier. The signal in the upper path at the output of the main amplifier and coupler is the desired RF signal including distortion created by that amplifier. The signal in the lower path at the output of the error amplifier is ideally an amplified form of only the distortion created by the main amplifier. The delay line in the upper path is adjusted to compensate for the delay in the error amplifier in the lower path. This is because both signals must reach the output coupler 180° out of phase. In addition, the distortion signal in the lower path must be of sufficient amplitude to compensate for the coupling factor in the output error injection coupler. If the two signals are 180° out of phase and the distortion product amplitudes are the same, perfect distortion cancellation may occur and result in a distortion-free RF signal at the output of the system [9].

The most critical component in a feedforward system is the error amplifier. It must not contribute any IMD products itself and it must have high gain and minimal propagation delay. The propagation delay affects the required delay line length in the upper path and thus the insertion loss at the main amplifier output. Excessive delay results in poorer efficiency and reduced IMD improvements, due to the need to drive the main amplifier harder to overcome these losses. In addition, the delay and gain in this system must be accurately controlled for ideal IMD reduction; thus some form of control must be implemented to adjust gain and delay. A digital signal processor (DSP) may be used to perform this gain and delay adjustment, or degraded performance may be accepted based on a calculated maximum phase and gain error in the system. While this technique is costly to implement, it has proven to be quite effective on wideband, multicarrier signals such as CDMA and WCDMA. This is an important advantage to the feedforward linearization technique, justifying the cost and hardware overhead in already expensive

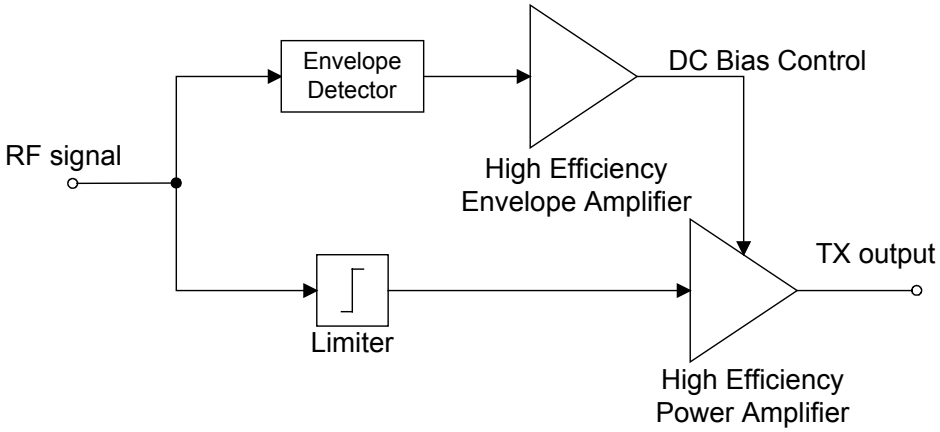


Figure 1.5 EER transmitter [5]

base station and satellite systems. However, this technique is generally not practical in low cost, lightweight, mobile terminals.

1.1.5 Envelope Elimination and Restoration (EER)

A variation of the feedforward technique is *envelope elimination and restoration (EER)* (Figure 1.5), which is also known as the Kahn technique. Here the modulated RF input signal is sampled through a coupler or power divider to recover the envelope information. In parallel, the RF signal is limited; this eliminates the envelope and allows the constant amplitude, phase modulated carrier to be amplified efficiently by a suitable nonlinear PA. To restore the envelope information, the final RF PA stage is amplitude modulated via the DC bias of the PA [5]. The envelope information (voltage) swings on top of the PA DC bias. This technique may be accomplished with analog or DSP techniques and may involve the entire transmitter or just the PA.

Very good results can be attained due to the fact that high efficiency switching (Class C, D, E, or F) power amplifiers and audio amplifiers may now be used to amplify the constant envelope signal (which is less susceptible to nonlinearities). Ideally, 100% efficiency may be attained, although this is not the case in the real world. However, this technique is limited to modest levels of envelope variation. Large envelope variations may drive the PA transistor bias into cutoff resulting in significant distortion [3].

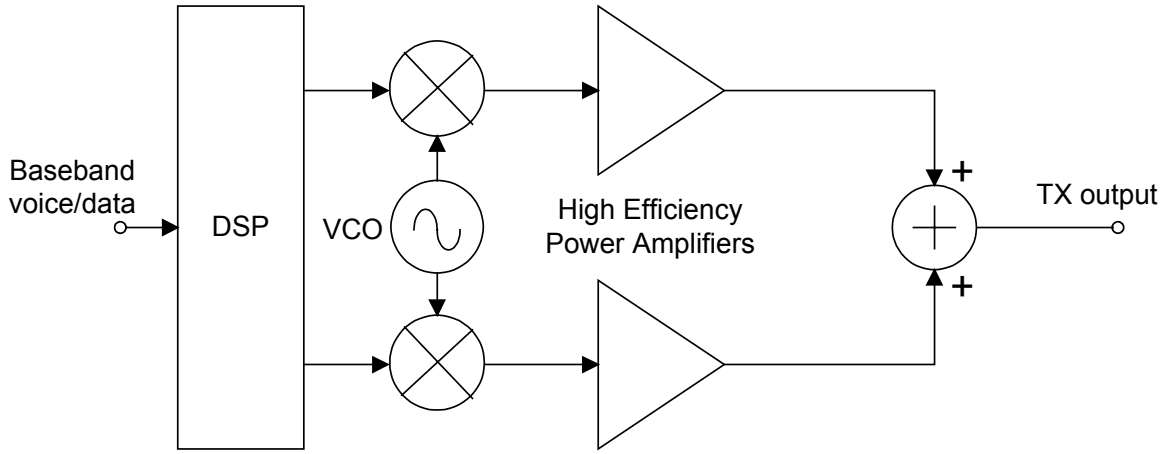


Figure 1.6 LINC transmitter [3][11]

1.1.6 Linear Amplification Using Nonlinear Components (LINC)/Combined Analog-Locked Loop Universal Modulator (CALLUM)

The *LINC* technique [3][11] (Figure 1.6) uses a DSP to generate two constant envelope phase-modulated baseband signals, which, after upconversion and nonlinear power amplification, will produce the required linear output signal upon final summation. Any unwanted nonlinear elements remaining in the signal before summation will be opposite in phase in each path and will cancel upon summation. This method also makes use of high efficiency switching amplifiers to achieve efficiencies theoretically approaching 100%.

The main drawback of this technique is that gain and phase balance must be tightly controlled in the two RF paths in order to obtain ideal cancellation at the output. The *CALLUM* technique [12] is a feedback technique that attempts to solve the gain and phase imbalance problem in the LINC method. Cartesian feedback is used in CALLUM, where the output signal is downconverted into quadrature signals. These feedback signals are compared with the input baseband signals and used to generate an error signal. The main problem with the CALLUM technique is stability. Due to stability issues, CALLUM must be limited to narrowband applications. It should be noted that the unwanted parts of the signals pass through the PA before they are summed and cancelled out in both of these

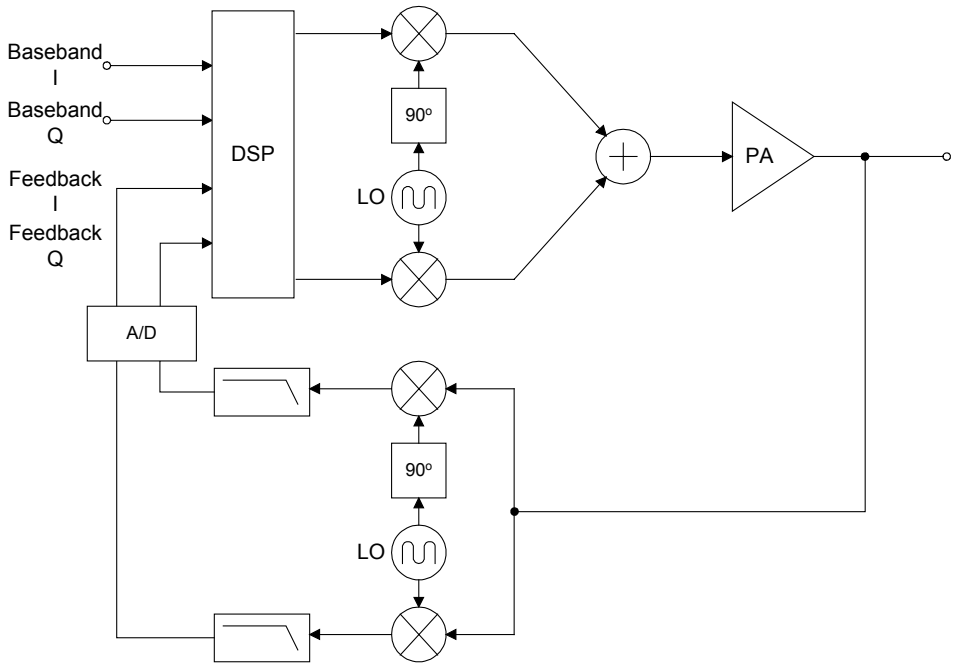


Figure 1.7 Adaptive baseband predistortion transmitter [30]

techniques; these extra signals are actually amplified in two separate amplifiers. Thus, a high percentage of the system efficiency may be lost here.

1.1.7 Adaptive Baseband Predistortion

Adaptive baseband predistortion is essentially a Cartesian loop feedback scheme, but with the addition of a DSP to predistort the baseband signals. Predistortion is a technique in which the known amplitude and phase nonlinearities of a system are applied to a signal in a manner opposite to that of the original distortion. The result upon cascade of the predistortion generator and the nonlinear system is distortion cancellation. In this particular technique, the feedback path is digitally sampled with an A/D converter and fed into the DSP, which uses this data to predistort the I and Q baseband signals that will be fed into the transmitter (Figure 1.7). The DSP calculates and stores a set of predistortion coefficients and updates these with the information from the feedback path. This technique achieves good linearization but does not significantly improve PAE. DSPs consume a large amount of power to perform the necessary calculations. Also, A/D converters are required in the

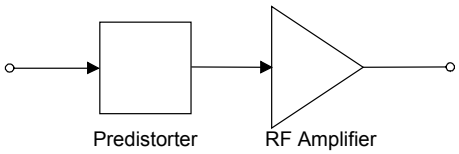


Figure 1.8 Predistortion amplifier

feedback path, which further increase the power consumption. Finally, these DSP and A/D components increase the cost of the implementation.

1.1.8 RF/IF Predistortion

Of the linearization techniques presented in Section 1.1, *RF predistortion* (Figure 1.8) is the simplest and has the ability to linearize over the entire RF bandwidth. Therefore, it has strong potential for use in wideband, multicarrier systems. Also, its simplicity lends itself to straightforward integration into amplifier ICs with little impact on size and complexity. Some form of control or adjustment may be required for high degrees of linearity, although this is not always the case [4]. RF/IF predistortion is similar to adaptive baseband predistortion except that the predistortion is done immediately before (or after in a postdistorter) the RF amplifier. However, there is no feedback in this technique, thus it is an open-loop system. This means that the distortion to be cancelled must be known in advance. This method may be applied at IF also. The advantage of IF predistortion is that the same design may be used for a range of different carrier frequencies by simply varying the LO. The predistorter generates a distortion signal/characteristic that is opposite to that of the RF amplifier. When the distortion generator and the amplifier are cascaded together, the distortion is cancelled out. This process will be discussed in detail in Section 1.2.

Typically, third order IMD has been of most concern. Therefore, a cubic predistorter is typically used to help reduce third order IMD products generated in a power amplifier. Very good results have been achieved using this form of predistorter. Another class of predistorters compensate for the AM-AM and AM-PM of the PA. The difficulty in these predistortion methods is in designing a circuit that will accurately produce a characteristic

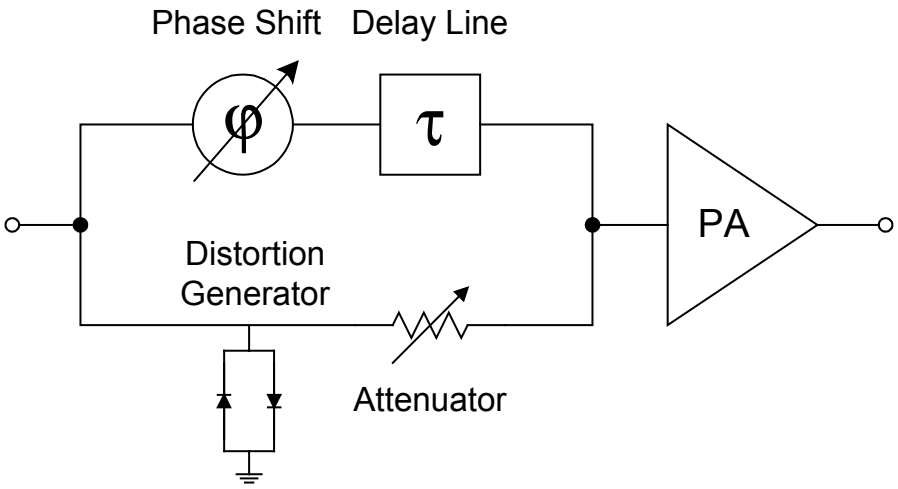


Figure 1.9 Cubic predistortion amplifier

opposite to the original distortion. However, due to the relative simplicity of RF/IF predistortion compared to other linearization techniques, this may be an ideal candidate for PA's used in mobile and hand-held radios where small size, low-cost, and low power is a large factor in the design. Therefore, this thesis will focus on analog predistortion methods and their implementation. The nature of some possible predistortion circuits will be discussed in detail in the following section.

1.2 Predistortion Linearizers

As mentioned in the previous section, there are two main classes of predistortion circuits found in the literature. The first generally involves the use of a pair of anti-parallel diodes to generate odd-order distortion. This method is called cubic predistortion. The second method involves AM-AM and AM-PM compensation. This is generally a nonlinear phase shift network and will be referred to as series diode predistortion.

1.2.1 Cubic Predistortion

A block diagram of a typical *cubic predistortion* linearizer is shown in Figure 1.9 [13][14]. There are two paths in the circuit. The RF power is split between these two paths and then recombined before the PA. The lower path consists of the distortion generator and an

attenuator. The distortion generator is typically a pair of anti-parallel diodes or a single diode biased at the desired operating point. The advantage of using anti-parallel diodes is that theoretically only odd order distortion is generated, while the even order distortion circulates inside the diode loop [18]. A single diode, when driven with RF, will generate even and odd order distortion. The diode may be forward biased closer to its turn on point so that lower power RF signals will still have sufficient distortion generated. Larger RF signals may be sufficiently rectified by the diode to generate enough distortion without this forward bias. The biasing of anti-parallel diodes must be done carefully with regards to RF choking and maintaining diode balance; however, the DC bias provides an extra degree of freedom in adjusting the linearizer. The signal in the upper path is phase shifted so that the original RF signal and the distortion generated in the lower path are 180° out of phase. The fixed delay line equalizes the group delays between the two paths. The attenuator allows the distortion level to be adjusted to match that of the distortion generated in the PA. When the two signals are recombined prior to the PA, the result is a signal containing the original RF signal plus distortion phase-shifted by 180°. When this signal is passed through the PA, the predistortion cancels with the normal distortion generated in the PA. For this technique to work well, the distortion level generated must be well matched and properly adjusted in phase with respect to the PA distortion. This creates the need for accurate control of the phase shifter, attenuator, and distortion generator bias to achieve maximum linearization. This technique is relatively simple compared to some of the others discussed previously and works well, but introduces quite a bit of loss into the system. A loss of about 5.5 dB is reported in [14].

1.2.2 Series Diode Predistortion

The final linearization technique to be discussed here is the *series diode predistorter* shown in Figure 1.10. Compared to the techniques presented above, it is the simplest and least expensive to implement and offers a relatively modest improvement in linearity. This technique is a good candidate for mobile applications such as small handheld radios or cell phones due to the minimal circuitry and additional controls needed.

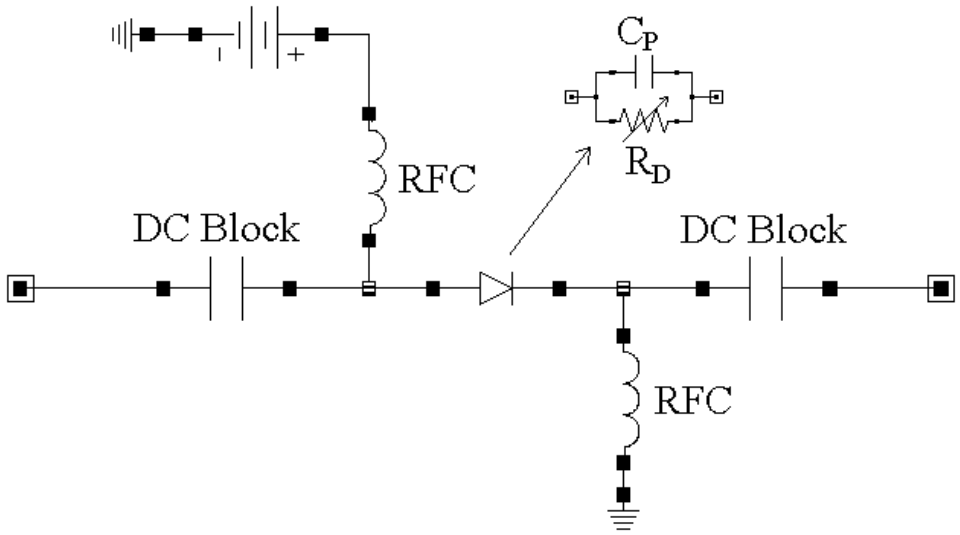


Figure 1.10 Series diode predistorter

A version of this circuit was presented in [15] to compensate directly for an amplifier's AM-AM and AM-PM distortion. Typically, amplifiers driven into their nonlinear regions exhibit *gain compression* (AM-AM) and *phase advance* (AM-PM). In the circuit in Figure 1.10, the diode functions as a nonlinear resistor (R_D) with a parasitic capacitance (C_P) in parallel. Since the diode is operated under a forward bias, the nonlinear C/V is neglected. The resistance and capacitance is used to form a nonlinear RC phase shift network. Additional R and C may be added externally if needed. The diode is forward biased to set R_D and C_P at an initial small-signal operating point. As the diode is driven past small signal with RF power, the diode rectifies the RF power and the operating point changes with increasing input power. Effectively, R_D decreases with increasing input power since its operating point is moved up the I/V curve. R_D changes nonlinearly due to the diode's I/V characteristic, resulting in a nonlinear phase shift with increasing input power. The S_{21} for the RC network is given by:

$$S_{21} = \frac{2Z_o Y}{1+2Z_o Y}, \qquad Y = j\omega C_P + \frac{1}{R_D} \tag{1.2}$$

To examine the effect of a nonlinear resistance on this RC phase shift network, a simulation was performed using Matlab [16]. C_P was set to a fixed value of 3pF in this example. R_D is varied and the results of Equation 1.2 in a 50Ω system are plotted versus R_D on a log scale in Figures 1.11 and 1.12. Inspection of these results shows a resulting gain *expansion* and *decrease* in phase shift for a decreasing R_D (increasing P_{in}). Notice in Figure 1.11 that R_D must be chosen properly in order to get gain expansion rather than gain compression (roughly ≤ 80Ω for this example). This gain expansion characteristic is opposite to that of the inherent amplifier, thus this circuit should be able to compensate for the nonlinear amplifier characteristics. A more detailed treatment on this particular circuit may be found in [15].

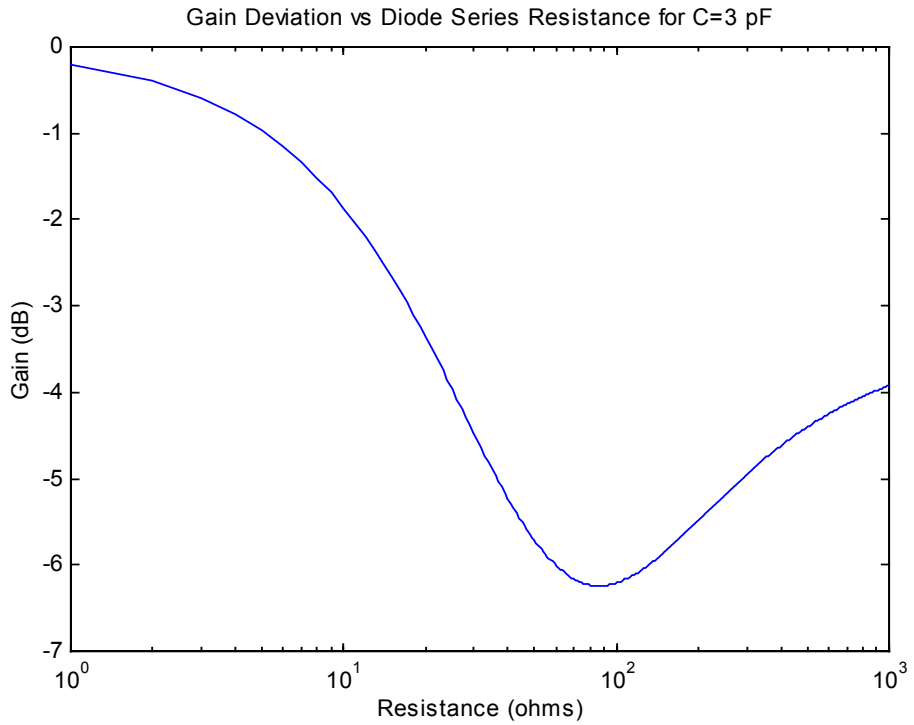


Figure 1.11 Results of Equation 1.2 in log magnitude format

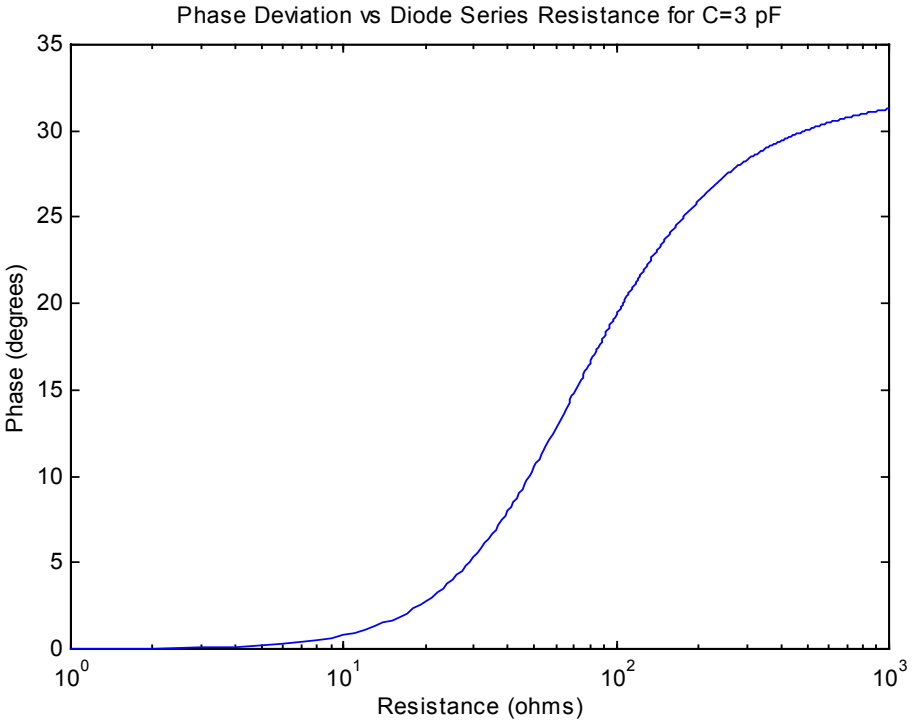


Figure 1.12 Results of Equation 1.2 in phase format

2 Digital Modulation Considerations

The type of modulation used in a radio system puts different demands on the linearity requirements of the system. Several forms of filtered QPSK are becoming popular, characterized by a non-constant envelope exhibiting a peak envelope power (PEP) higher than the signal's average power as shown in Figure 2.1. The peak to average ratio (PTAR) is a ratio of this PEP to the average signal power, and is a term commonly used when describing different digital modulation schemes [1]. The PTAR must be considered when linearity in a system is required. PTAR and PEP will be illustrated further in Section 2.3. The following discussions demonstrate the importance of PTAR characterization and the usefulness of AM-AM and AM-PM curves. The relationship of these terms to amplifier linearity and IMD products, as well as the importance of ACPR characterization will be discussed.

2.1 Weakly Nonlinear Effects and Intermodulation Distortion

Traditionally, IMD products have primarily been used for characterizing an amplifier's nonlinearity. Two-tone analysis makes use of an amplifier's weakly nonlinear characteristics and a power series expansion to characterize nonlinearity. An amplifier is in a weakly nonlinear region when it is operated at power levels far below where it starts to exhibit gain compression (saturation). In this weakly nonlinear region, IMD at levels lower than about –30 dBc become significant [1]. Two-tone analysis is most useful in receiver and low noise amplifier (LNA) design where IMD products at very low levels can interfere with weak desired signals. In power amplifier characterization, two-tone analysis is still important and is commonly used as a figure of merit for amplifier nonlinearity; however, better methods are evolving for nonlinearity analysis in the *strongly* nonlinear region. The strongly nonlinear region is generally considered where an amplifier is operating at or beyond the gain compression point and corresponds to the cutoff and clipping behavior of the transistor(s) [1]. The importance of the strongly nonlinear region, and methods of its characterization will be discussed shortly; however, first a brief

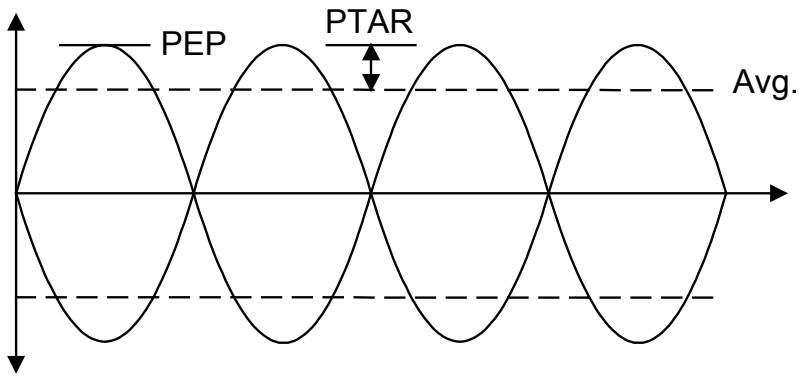


Figure 2.1 Definition of the terms PEP and PTAR

example of two-tone IMD analysis will be presented [1].

In the weakly nonlinear region, an amplifier's transfer characteristic is typically described by a power series:

$$v_0(t) = \alpha_1 v_i(t) + \alpha_2 v_i^2(t) + \alpha_3 v_i^3(t) + \alpha_4 v_i^4(t) + \alpha_5 v_i^5(t) + \ldots, \tag{2.1}$$

where v_i is the RF input signal and v_0 is the RF output signal of the amplifier. For two-tone analysis, the input signal consists of two equal amplitude RF signals closely spaced in frequency and in or near the desired band of operation of the amplifier:

$$v_i(t) = A\cos\omega_1 t + A\cos\omega_2 t \tag{2.2}$$

When Equations 2.1 and 2.2 are combined, the resulting output may be expressed as:

$$v_0(t) = \alpha_1 A(\cos\omega_1 t + \cos\omega_2 t) + \alpha_2 A^2(\cos\omega_1 t + \cos\omega_2 t)^2 + \alpha_3 A^3(\cos\omega_1 t + \cos\omega_2 t)^3 + \ldots \tag{2.3}$$

If $v_0(t)$ in Equation 2.3 is expanded and the result is manipulated through the use of common trigonometric identities, it will be seen that the output signal will contain frequency components at DC, ω_1, ω_2, $2\omega_1$, $2\omega_2$, $3\omega_1$, $3\omega_2$, $\omega_1 \pm \omega_2$, $2\omega_1 \pm \omega_2$, $\omega_1 \pm 2\omega_2$, and so on. Of particular importance are the IMD products that fall within the desired passband. A significant problem arises if two strong interferers experience third or fifth

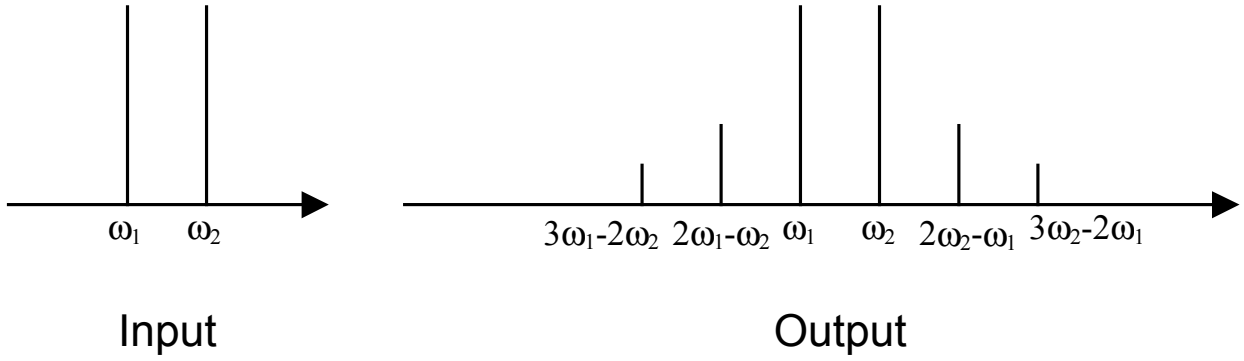


Figure 2.2 Two tone IMD spectrum

order nonlinearity and one of the resulting IMD products falls within the passband with the desired signal. These are usually odd order IMD products, since even order IMD products are typically far enough out of band to be of less concern. The third order IMD products that potentially fall within the passband of the desired signal are $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$. Fifth and higher order IMD products must be considered when operating in the compression and saturation region, but are typically ignored in the weakly nonlinear region. Figure 2.2 shows that the IMD products appear as sidebands to the two input tones at the same frequency spacing of the two tones. The third and fifth order IMD products are shown in the figure. Other products of Equation 2.3 generally do not fall in the passband of the amplifier and are not shown here. These odd-order IMD products can corrupt a weak desired signal.

One can see in this figure how, as the order *n* of an IMD product [$(n+1)\omega_1-n\omega_2$ and $(n+1)\omega_2-n\omega_1$] increases, the amplitude of the product decreases. The amplitudes can be derived from a detailed expansion of Equation 2.3 and are the basis for a commonly used figure of merit in weakly nonlinear amplifiers called the *intercept point*. The intercept point (IP) is the point at which an amplifier's IMD product is equal in amplitude to the main signal component. This imaginary point is extrapolated from a plot of IMD products amplitudes and the main signal amplitude versus input power. Typically, the third order intercept point (IP_3) is of most interest and is commonly listed on an amplifier's data sheet as the figure of merit for linearity. Since second order (and other even order) IMD products, which results in an IP_2, fall outside of the desired passband, these are not of

concern unless a direct conversion architecture is being implemented. Higher order odd IMD products, such as fifth order (which would result in an IP_5), may have significance in a particular system, but are typically of less concern due to much lower amplitudes compared to third order IMD products. For these reasons, IP_3 is typically the dominant characteristic and thus is useful for characterizing the nonlinearity of an amplifier in the weakly nonlinear region. A problem sometimes arises due to the use of this imaginary point outside of the weakly nonlinear region. A small variation in the third order IMD product amplitudes results in a larger variation of the extrapolated IP_3 point, which is negligible when backed-off enough. This variation in IP_3 is a source of error in the use of two-tone linearity characterization in the compression region of an amplifier. In the weakly nonlinear region where most receive amplifiers operate, this error is not as significant since the amplifiers are not intended to be operated at high enough power levels to go into compression and operate near the IP_3 unless a strong received signal is present. However, power amplifiers (PA) typically need to be operated at or near the compression point for reasons that will be discussed in the next section. Therefore, the IP_3 is not of as much use for PA design [1], and has resulted in the development of other more meaningful methods of characterizing PA nonlinearities.

2.2 Strongly Nonlinear Effects and Adjacent Channel Power

As mentioned above, nonlinearity characterization using two-tone analysis is very useful for characterizing amplifiers in the weakly nonlinear region. In the strongly nonlinear region, higher order IMD products become much more significant as an amplifier is driven further into the compression region. This effect is due to the limiting behavior of the transistor(s). As an amplifier is operated in the strongly nonlinear region and pushed further into compression, the amplifying transistor(s) will start to exhibit current pinchoff (in the case of a FET) as the gate-to-source voltage completely closes the channel [1]. Therefore, the higher order IMD products are more important. In this region, fifth and even seventh order IMD products can be significant. The presence of multiple strong IMD products in this region requires a different method of characterizing nonlinearity for PA design.

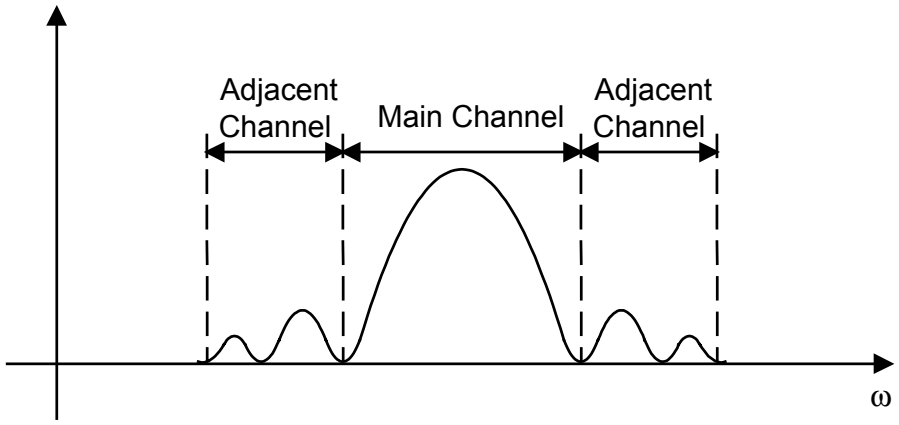


Figure 2.3 Adjacent channel power

Adjacent channel power (or spectral regrowth) ratio (ACPR) is defined as the measured power in an adjacent communications channel of a specified bandwidth relative to the power in the main channel of specified bandwidth (Figure 2.3). ACPR has become one of the dominant specifications for modern PAs due to the increasing use of multicarrier systems, digital modulation, as well as more densely packed communications channels. ACPR can roughly be related to the simple two-tone analysis in the previous section as follows. The previous two-tone analysis assumed two separate carriers at fixed frequencies. In a modern digital system this would not be the case. The two interfering carriers would typically be modulated carriers from another interfering radio system or within a multicarrier transmitter. A simple analog example could be two frequency modulated (FM) signals in adjacent channels of a multicarrier transmitter. These FM signals would exhibit modulation sidebands around the carrier. Due to these sidebands, the IMD products would also exhibit sidebands. The IMD modulation sidebands extend to three times the original modulation bandwidth in the case of the third-order IMD products and five times in the case of fifth order as illustrated in Figure 2.4 [1]. As the modulation bandwidth increases, so do the sidebands, creating more interference in the adjacent channel due to IMD. As the number of channels in a multicarrier system increases, the amount of IMD increases and a simple two-tone analysis quickly becomes inaccurate. The number of tones required to analyze a large multicarrier system becomes unwieldy and additional effects like cross-modulation come into play as well; this is one reason for the use of ACPR as a figure of merit for linearity. ACPR is basically a measure of power in

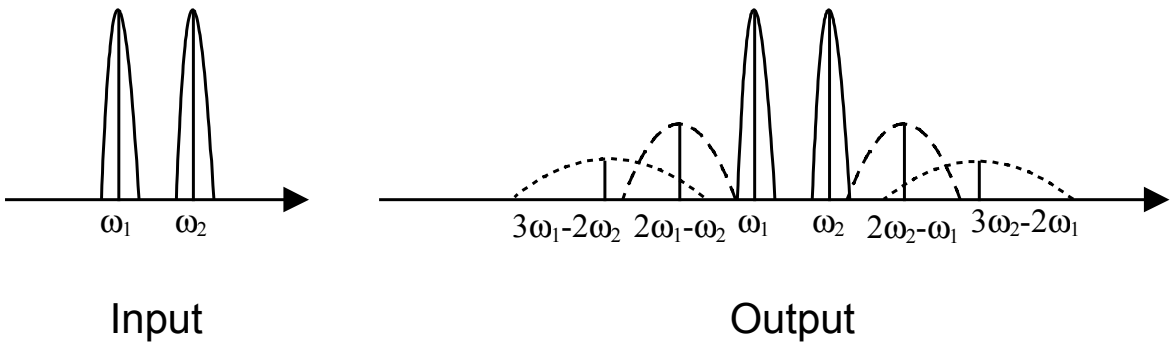


Figure 2.4 IMD spectrum for frequency modulated carriers in multicarrier transmitter

the sidelobes due to all of the IMD products relative to the desired channel. Since it is important in modern communication systems to utilize bandwidth efficiently, the lower the ACPR, the tighter channels may be packed together in a given amount of bandwidth with minimal interference to one another. There are ongoing efforts to relate the standard IP_3 to ACPR (e.g. [23]).

In addition to multicarrier systems, digitally modulated systems show a need for this ACPR figure of merit. In basic digital modulation, a baseband stream of bits is used to modulate the RF carrier. Ideally, this data stream is a series of ones and zeros in the form of flat top pulses. The absolute bandwidth on an ideal flat top pulse is infinity. At a certain point the sidelobe levels become insignificant, thus the bandwidth can be truncated to something less than infinity, but the bandwidth of a flat top pulse is still significantly large relative to modern communications channels. Ideally, this data bandwidth translates to the RF bandwidth centered on an RF or microwave carrier frequency. Since efficient use of RF bandwidth is increasingly important in modern communication systems, this infinite or very large bandwidth is unacceptable. Various pulse shaping filters, such as a Nyquist filter, may be used to limit this bandwidth, but this baseband filtering must be used with caution to avoid intersymbol interference (ISI)[19].

In addition to ISI problems, pulse shaping will have an effect on the amplitude of the RF signal envelope. A constant envelope modulation such as QPSK may be pulse shaped

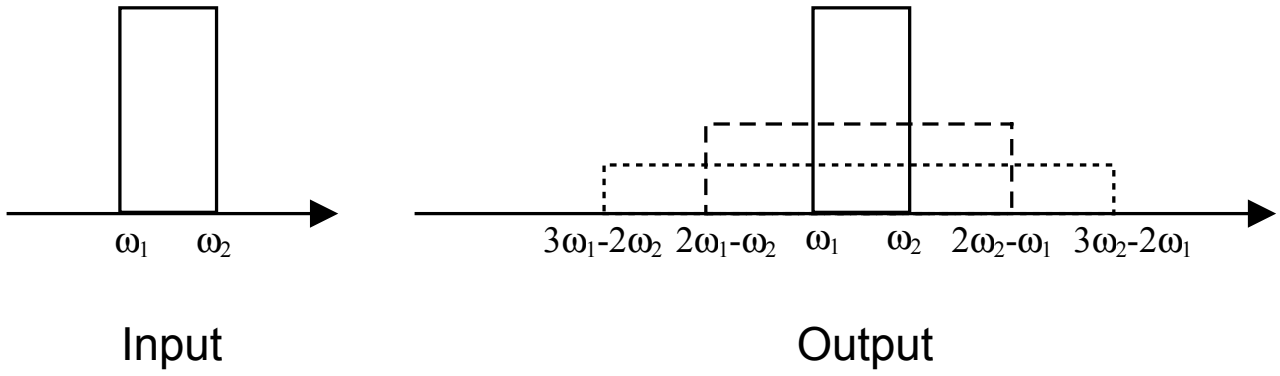


Figure 2.5 IMD spectrum for typical digitally modulated signal

(filtered); however, if the resulting non-constant envelope after pulse shaping is distorted through amplifier nonlinearities, the zero crossings where phase information is contained may be distorted, resulting in a loss of information. This loss of information is typically specified as bit error rate (BER). In addition, in-channel phase and amplitude distortion is possible on the signal constellation. This is visualized as a spreading and rotation of constellation points and has been studied in detail in [21]. Constant envelope modulation schemes where the information is contained in frequency rather than phase, such as FSK or GMSK, are relatively immune to this effect, thus they may theoretically be amplified with a highly nonlinear amplifier; however these modulation schemes suffer from a lower bandwidth efficiency compared to other schemes and they are usually not coherently detected.

From this discussion, the need for a nonlinearity figure of merit such as ACPR for multicarrier and digital radio systems is evident. In addition, the amplitude statistics of a two-tone signal used for IMD analysis are very different than those of complex digitally modulated signals [22], presenting another motivation for ACPR measurements. Figure 2.5 shows a simple IMD spectrum for digital signals; this is similar to the FM multicarrier example in terms of IMD product content and the modulation sidebands. Note that baseband digital signals typically contain information close to DC and are not band-limited, leading to the wide power spectral density in the desired signal. Also, since multi-tone CDMA spreading codes are commonly used to spread the RF signal, complex

digitally modulated signals are noise-like and completely fill their assigned bandwidth; as a result, IMD products occur in a spread fashion as well, resulting in spread sidelobes. This results in steps in the ACPR. Each higher order of IMD results in another lower step in the ACPR.

2.3 Envelope Analysis

In the previous section it was seen that a simple two-tone IMD analysis becomes inaccurate and unwieldy for complex digitally modulated signals as well as multicarrier signals. Alternative methods are required for the PA designer to predict ACPR based on simulations. The answer may lie in a method called envelope analysis. Envelope analysis treats these modulated signals in the time domain rather than the frequency domain. As shown in the beginning of this chapter, a modulated signal's time domain envelope exhibits a PEP higher than the signal's average power (Figure 2.1). This gives rise to the PTAR. This idea can be further visualized in a MATLAB simulation based on the analysis presented in [1]. A variable envelope signal is generated using a multi-carrier signal of the form:

$$v_s(t) = v[\cos(\omega_m t) + m_2 \cos(2\omega_m t) + m_3 \cos(3\omega_m t) + ...]\cos(\omega t), \tag{2.4}$$

where m_2, m_3, and m_n are the second, third, and nth harmonic amplitude coefficients, ω_m is the modulating frequency, and ω is the carrier frequency. The number of harmonics included in the modulating signal limits the maximum PTAR. For a signal with no harmonics, the maximum PTAR is 3 dB. If the second harmonic is included, then the maximum PTAR is 6 dB, and so on. Varying the coefficients m changes the harmonic content in the signal and thus the PTAR. Varying m_2 changes the amount of second harmonic present in the signal. The second harmonic mixing with another tone causes third order IMD products. Since the addition of the second harmonic to the signal introduces extra power, the signal level is adjusted so that all cases have the same calculated average power level of +30 dBm for a 1Ω resistive load. The signal described above has a peak voltage amplitude of $v(1+m_2)$, which corresponds to a peak rms power (into 1Ω) of:

$$P_{pk} = \frac{v^2}{2}(1+m_2)^2 \tag{2.5}$$

Truncating Equation 2.4 to second order, the average power of each individual frequency component is then summed to get the total signal average rms power of:

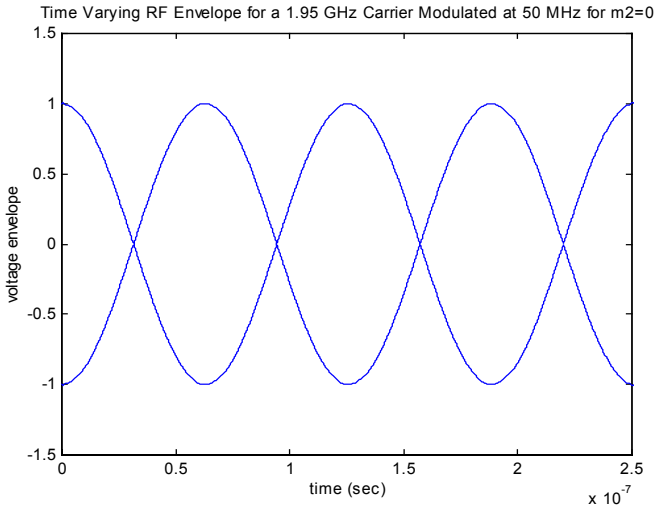
$$P_m = \frac{1}{2}\left[\left(\frac{v}{2}\right)^2 + \left(\frac{v}{2}\right)^2 + \left(\frac{vm_2}{2}\right)^2 + \left(\frac{vm_2}{2}\right)^2\right] = \left(\frac{v^2}{4}\right)\left(1+m_2{}^2\right) \tag{2.6}$$

From (2.5) and (2.6), an expression for the PTAR can be formed:

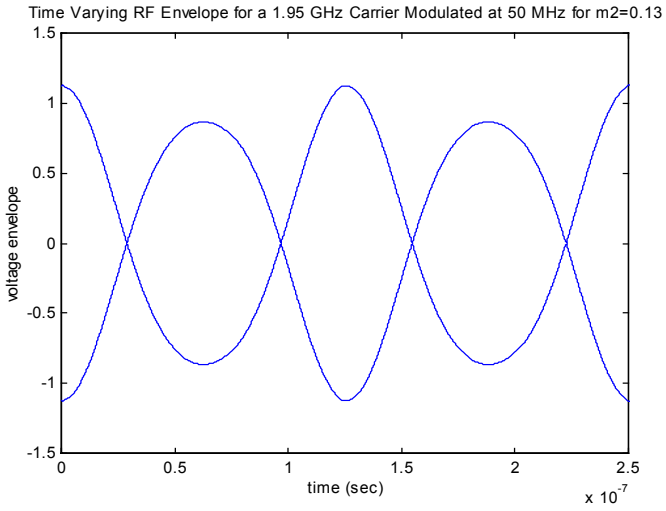
$$PTAR = \frac{P_{pk}}{P_m} = \frac{\frac{v^2}{2}(1+m_2)^2}{\left(\frac{v^2}{4}\right)(1+m_2{}^2)} = 2\frac{(1+m_2)^2}{1+m_2{}^2} \tag{2.7}$$

These formulas are used to calculate the average rms power and PTAR as a function of m_2. v is varied for each case to adjust for the same average rms power of +30 dBm into a 1Ω load. The results are presented in Figure 2.6. Calculations were performed for m_2 values of 0, 0.13, 0.25, and 1.0, corresponding to PTARs of 3.0, 4.0, 4.7, and 6.0 dB respectively. The significance of the 4.7 dB PTAR for m_2 = 0.25 is that only a single peak exists above the mean power per cycle. The rest of the peaks are at the mean level. It should be noted that the envelope peaks become higher with an increasing amount of second harmonic added to the signal.

When an amplifier is operated at or near compression, it becomes important to consider the PTAR. If a modulated signal drives an amplifier at an average operating point near or at compression, the peaks in the envelope will drive the amplifier further into compression, resulting in greater distortion than at the average operating point. An amplifier's power dependent S-parameters may be used in conjunction with the signal envelope to understand the effect of compression and large-scale nonlinearity on the signal. A simulated or measured S_{21} versus input power is all that is needed for a basic analysis. The gain compression (log magnitude of S_{21}) and phase advance curves (phase of S_{21}) are plotted vs.



(a)



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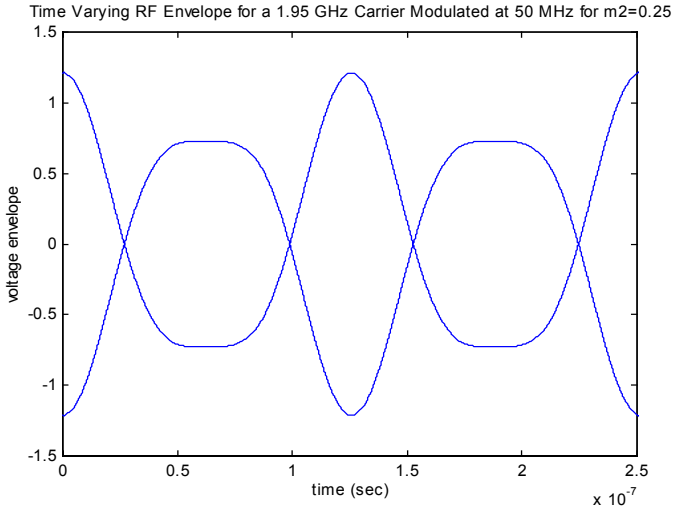

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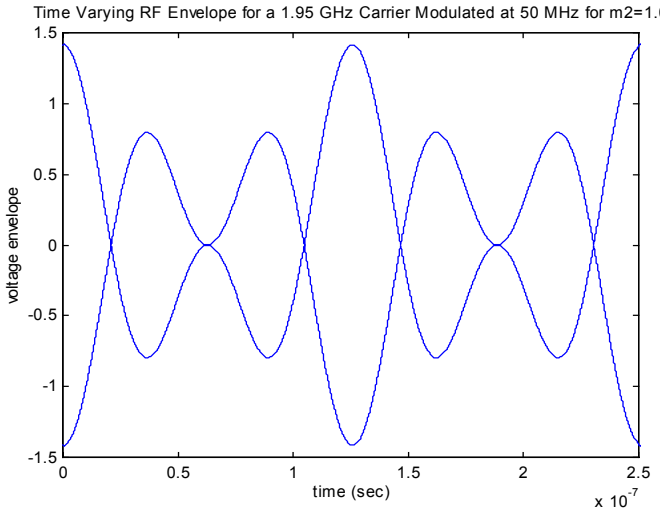


(d)

Figure 2.6 RF voltage envelopes for varying peak-to-average ratios but equal mean power levels: PTAR = 3.0 dB (a), 4.0 dB (b), 4.7 dB (c), and 6.0 dB (d)

increasing input power. These curves are commonly referred to as AM-AM and AM-PM curves respectively and are usually normalized to the small signal gain and phase. The AM-AM curves are commonly studied by PA designers and are used to estimate the required amount of *backoff* needed in the signal drive level to meet linearity requirements. However, the AM-PM curves are equally important when it comes to operating a PA near the compression region. A nonlinear change in phase will also occur on the envelope, distorting the signal in phase rather than amplitude. Many modern modulation schemes encode the desired digital information in the phase, thus phase distortion must also be reduced for optimum BER. The importance of these AM-AM and AM-PM curves, and their usefulness in studying amplifier nonlinearities in or near the compression region, has been reported by several groups [20][21].

Representative PA curves are shown in Figure 2.7. PA gain, phase, AM-AM, and AM-PM curves are shown versus increasing input power. The AM-AM and AM-PM curves are simply the gain and phase curves normalized to the small-signal gain and phase. For low input powers, the AM-AM and AM-PM are ideally zero.

The envelopes shown Figure 2.6 may be affected by these AM-AM and AM-PM curves depending on their respective envelope powers. If the PEP of the modulated signal is around –20dBm or less prior to the PA characterized by these curves, then there will be very little or no AM-AM or AM-PM effect on the signal as it passes through the PA. As the PEP is increased, the AM-AM and AM-PM due to the PA transfer characteristic increases and nonlinearly distorts the envelope. From these plots, it can be seen that in order to maintain a completely linear signal the PEP must be kept below where the AM-AM and AM-PM starts to become significant. To visualize these effects, a MATLAB simulation is performed which imposes these AM-AM and AM-PM curves (Figure 2.7) on the original signal envelope. An envelope with a PTAR=6.0 dB is used as an example. The original signal envelope is shown in Figure 2.6 (d). The input signal power is adjusted so that the *average* signal power is slightly into gain compression; thus the envelope will push further into compression and exhibit a nonlinear distortion.

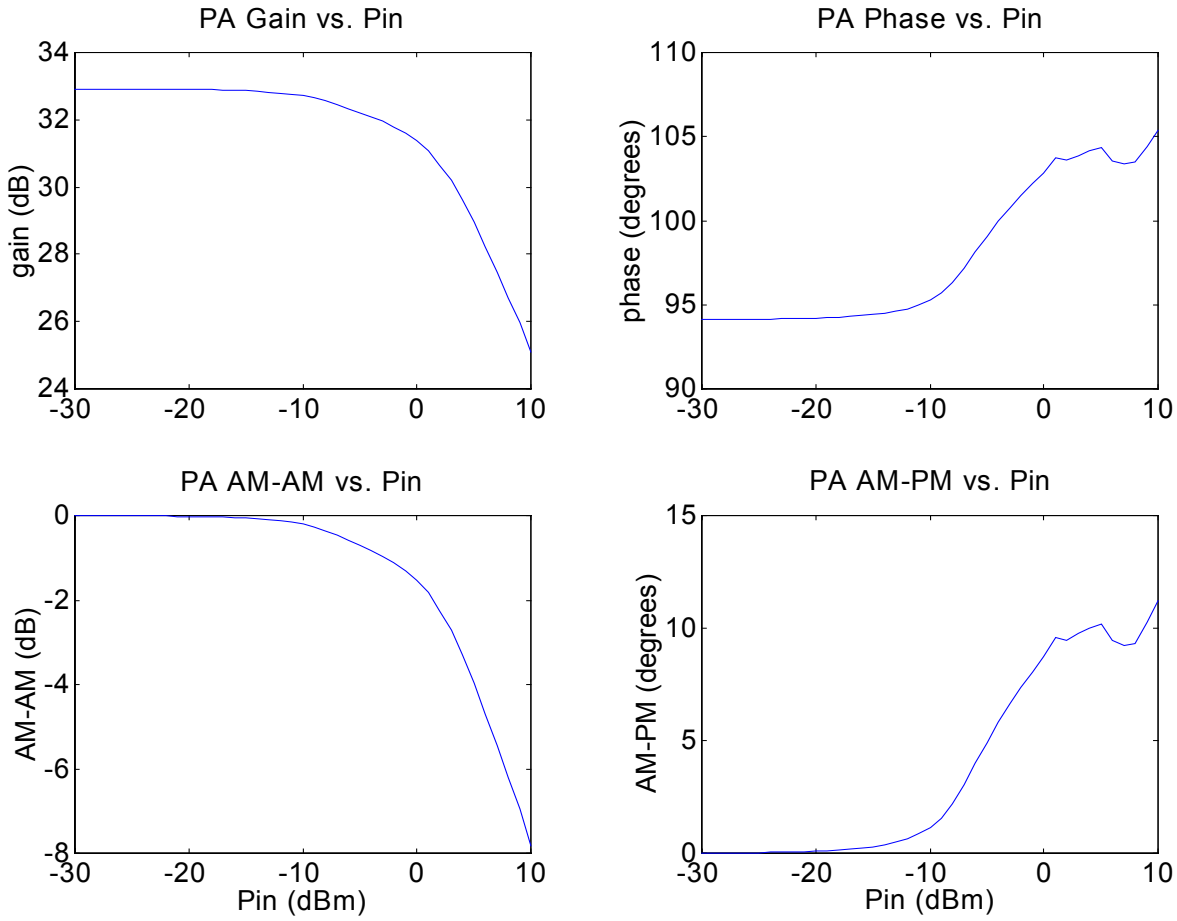


Figure 2.7 Representative PA linearity curves

Figure 2.8 shows the effect of the nonlinear PA on the signal envelope in terms of amplitude only (top), phase only (middle), and both amplitude and phase (bottom). It is clear in these figures that the nonlinear PA AM-AM and AM-PM do have a significant effect on the signal envelope. This nonlinear distortion may also be visualized using constellation diagrams [21]; the AM-AM and AM-PM effects will result in a signal compressed inwards due to amplitude distortion and rotated and spread due to phase distortion, respectively.

The nonlinear PA effects on a signal's envelope have now been demonstrated. However, one may wonder why it is undesirable to simply back-off the PA from compression to reduce the amount of nonlinearity on the envelope. The reason is the negative impact on

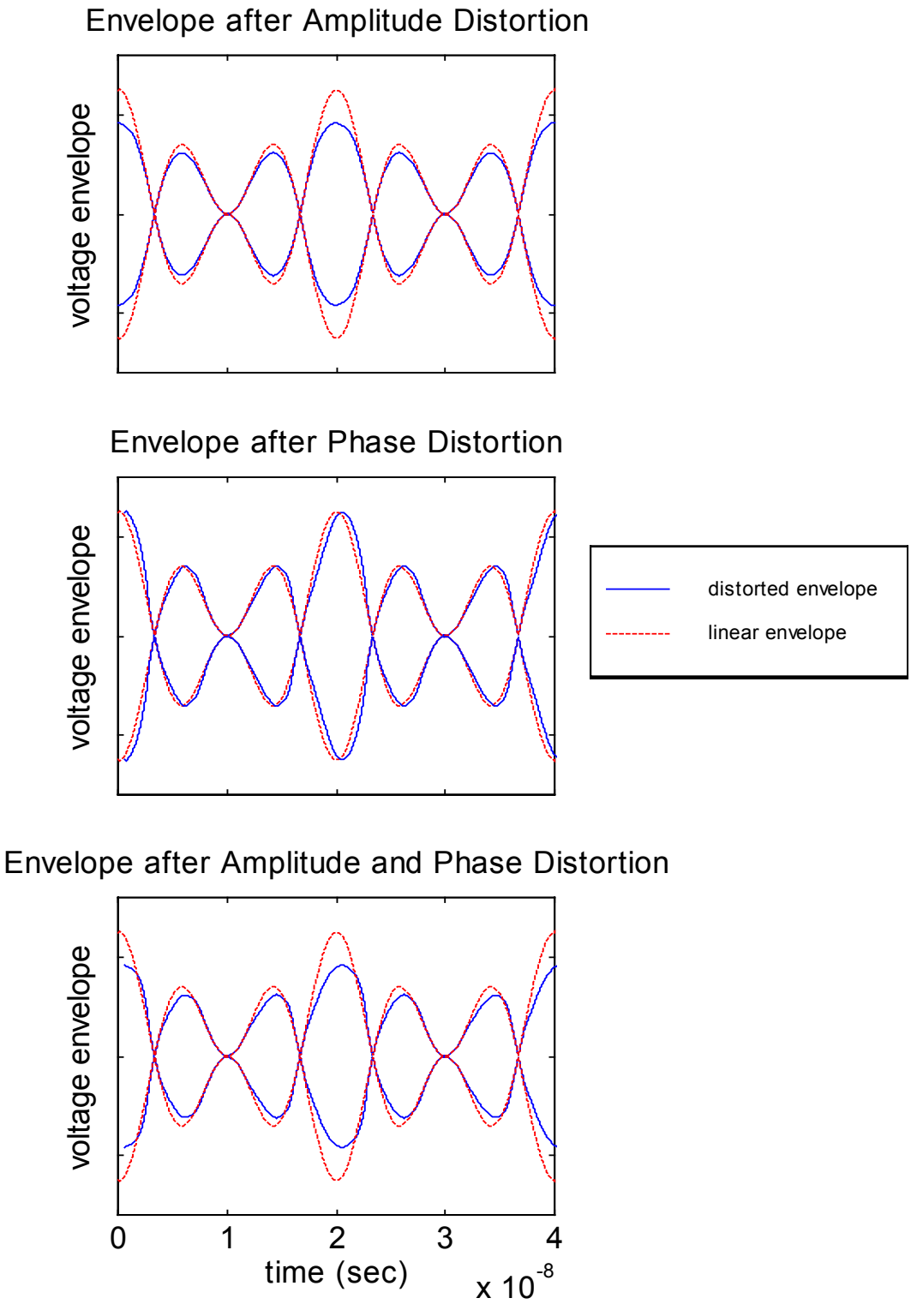


Figure 2.8 Effect of nonlinear PA on signal envelope

power efficiency. An amplifier's highest PAE occurs in the compression region, where the amplifier performance is most nonlinear. PAE decreases as an amplifier is backed-off from compression. PAE is very important in modern communications where mobile handsets must be lightweight and small. The more efficient an amplifier is, the smaller it can be as well as gaining the benefit of prolonged device operating times with respect to battery powered applications. With these comments in mind, the importance of reducing (and ideally eliminating) these PA nonlinearities in their most efficient region of operation (compression) can be seen.

2.4 Conclusions

An overview of PA design parameters for digitally modulated and multicarrier systems has been presented. The usefulness of a traditional two-tone analysis in weakly nonlinear regions of operation was shown. ACPR was defined and discussed as an important specification of PA nonlinear characteristics, which must be considered in modern digitally modulated systems.

Next, the basics of envelope analysis were presented with a Matlab simulation. Through this simulation, the importance of using envelope analysis in the strongly nonlinear region of operation was shown. Terms such as PEP, PTAR, AM-AM, and AM-PM were defined. These terms are important in characterizing PA nonlinearities in a digitally modulated system.

The following chapters use the background theory presented in Chapters 1 and 2 to study the series diode predistorter in detail. Specific case studies and results will be presented. An investigation into MESFET and HBT based diode predistorters will be discussed.

3 FET Diode Optimization for Series Diode Predistorter

As mentioned in Chapter 1, the series diode predistorter is the focus of this study. The optimization of the diode's size and bias versus input power is studied in this chapter. This optimization is performed to obtain the required R and C for the equivalent nonlinear phase shift network to match the AM-AM/AM-PM of a nonlinear GaAs MESFET PA. Resulting improvements in ACPR for digital modulation schemes with varying PTARs are presented as well.

3.1 Background

A nonlinear GaAs MESFET PA is the target for linearization in this chapter; thus the diode used should be fabricated in the same process as the PA in order to demonstrate the ability to easily integrate a predistorter into a single linearized PA RFIC or MMIC. The ITT GaAsTEK 5A GaAs MESFET process [24] was used for the PA in this initial study. The intent was to linearize a 1.9 GHz *personal communication system* (PCS) band PA marketed for use in mobile handsets where efficiency, weight, and size requirements are critical. In addition, for PCS band IS-95 [25] operation, stringent ACPR specifications must be met. Thus an improvement in ACPR using this predistorter could be very advantageous.

Drain-source connected MESFETs fabricated in GaAsTEK's 3F process were used for the diodes in this study. The 3F process is similar enough to the PA 5A process for these purposes. Figure 3.1 illustrates the topology of this FET. A drain-gate connected MESFET could also be used as the diode, but half of the device size would effectively be lost compared to the drain-source configuration; in the interest of minimal die size for integration, the drain-source configuration is preferred. The diode is formed by the gate-channel Schottky barrier. The gate serves as the anode and the drain-source serves as the cathode. The gate length, approximately the distance from source to drain in the FET, is about 0.4-0.8μm for these processes. The gate periphery is approximately 2xNxW, where N is the number of gate fingers and W is the gate width. This gate periphery is the total

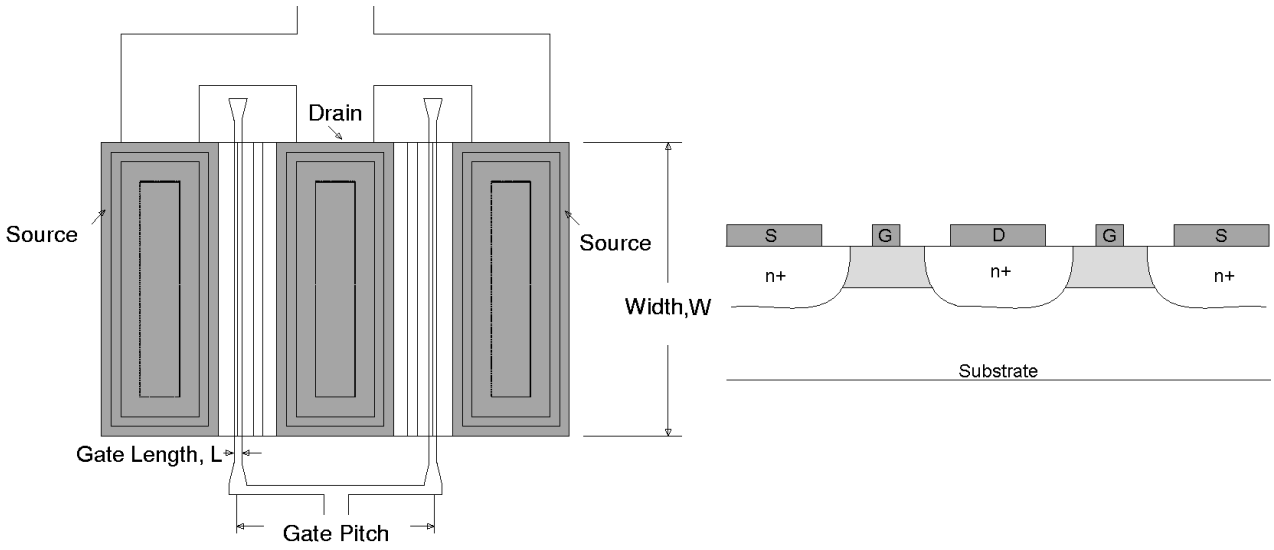


Figure 3.1 Topology of MESFET diode: (left) top view, (right) side view

perimeter of all of the gate fingers and is the key size identifier for this study. Total gate periphery is adjusted to size the diode for the PA predistortion application. Gate peripheries of 50µm to 2400µm were studied.

3.2 Diode Characterization and Measurement Setup

A printed circuit board (PCB) was designed to facilitate testing of series diodes. A representative PCB is shown in Figure 3.2. A diode is epoxied inline with each one of three through lines. Wire bonds are used to connect the anode (gate) to the RF input side of the through line and the cathode (drain-source) to the RF output side. Input and output end-launch SMA connectors allow testing in a coaxial system. Three different diodes are accommodated on each board, allowing three diodes to be tested individually on one PCB. Multiple boards were assembled containing a variety of diode sizes for characterization. Biasing was achieved through 3.5mm (DC-26.5GHz) bias tees and an external DC programmable power supply. This configuration allows calibration of the vector network analyzer (VNA) up to the SMA connectors on the test PCB. The biasing components (bias tees) are accounted for in the full two-port calibration, providing more accurate characterization of the diodes. A block diagram of the basic test setup is shown in Figure 3.3.

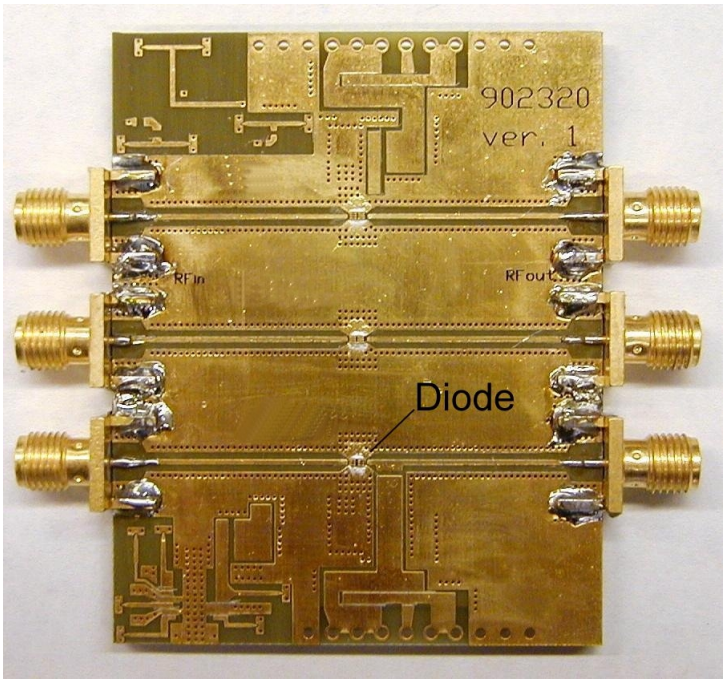


Figure 3.2 PCB for characterization of series diodes

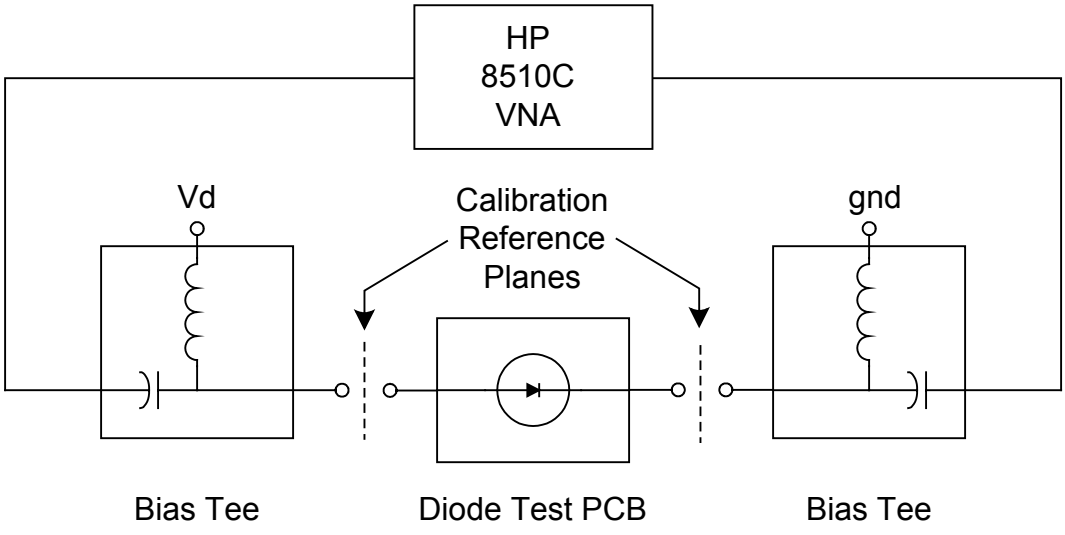


Figure 3.3 Block diagram of basic test setup for diode characterization

The VNA was operated in power sweep mode and full two-port S-parameter measurements were performed. A program was written in HP Vee [26] to automate these measurements, calibrate the system, and display initial AM-AM and AM-PM data based on the S_{21} measurements. In addition to the two-port calibration using an short, open, load, through (SOLT) technique, a power calibration was performed. Due to losses in the VNA, the S-parameter test set, and cable/connector losses, the actual power from the port 1 reference plane into the diode test PCB does not match the displayed value on the VNA. Obviously, this actual power level is not important when measuring S-parameters (power wave ratios). However, knowledge of the exact power driving the diode or PA is important in characterizing the compression region and nonlinearities in these devices. To account for the losses and calibrate the VNA power source to known power values, a sequence in the HP Vee program was added to perform a power calibration. The sequence simply sets the VNA power to a set value, measures the actual power output using a CW power sensor, and then derives a loss factor from this measurement. This loss factor is then used to properly set the VNA power to obtain a desired power level at the port 1 reference plane. A second measurement was made with the power sensor to test for +/- 0.1 dB accuracy. This calibration method worked well for this application; however one must be careful not to overdrive the VNA source itself into compression. The VNA must be operated below approximately its own 0.1 dB compression point to achieve the required linearity. Otherwise, the nonlinearities of the VNA source come into play and may obscure the DUT measurements. Another issue is the limited linear dynamic range of the VNA power source, since it is necessary to achieve power sweep levels to drive the PA or DUT sufficiently into compression. Fortunately, the PAs studied in this chapter have a reasonable amount of gain and require fairly low input levels.

The calibration and S-parameter measurements were verified by measuring a through line (Figure 3.4). One can see that the magnitude/phase of S_{21} is flat and centered around 0 dB/0 degrees and that the *return loss* (RL) is high. The only undesirable effect seen here is the noise present at lower power levels where the system noise has an effect on the calibration. This noise is acceptable as long as it is within the tolerance of the given application. In this case, the noise on S_{21} varies less than +/- 0.1dB and +/- 1 degree,

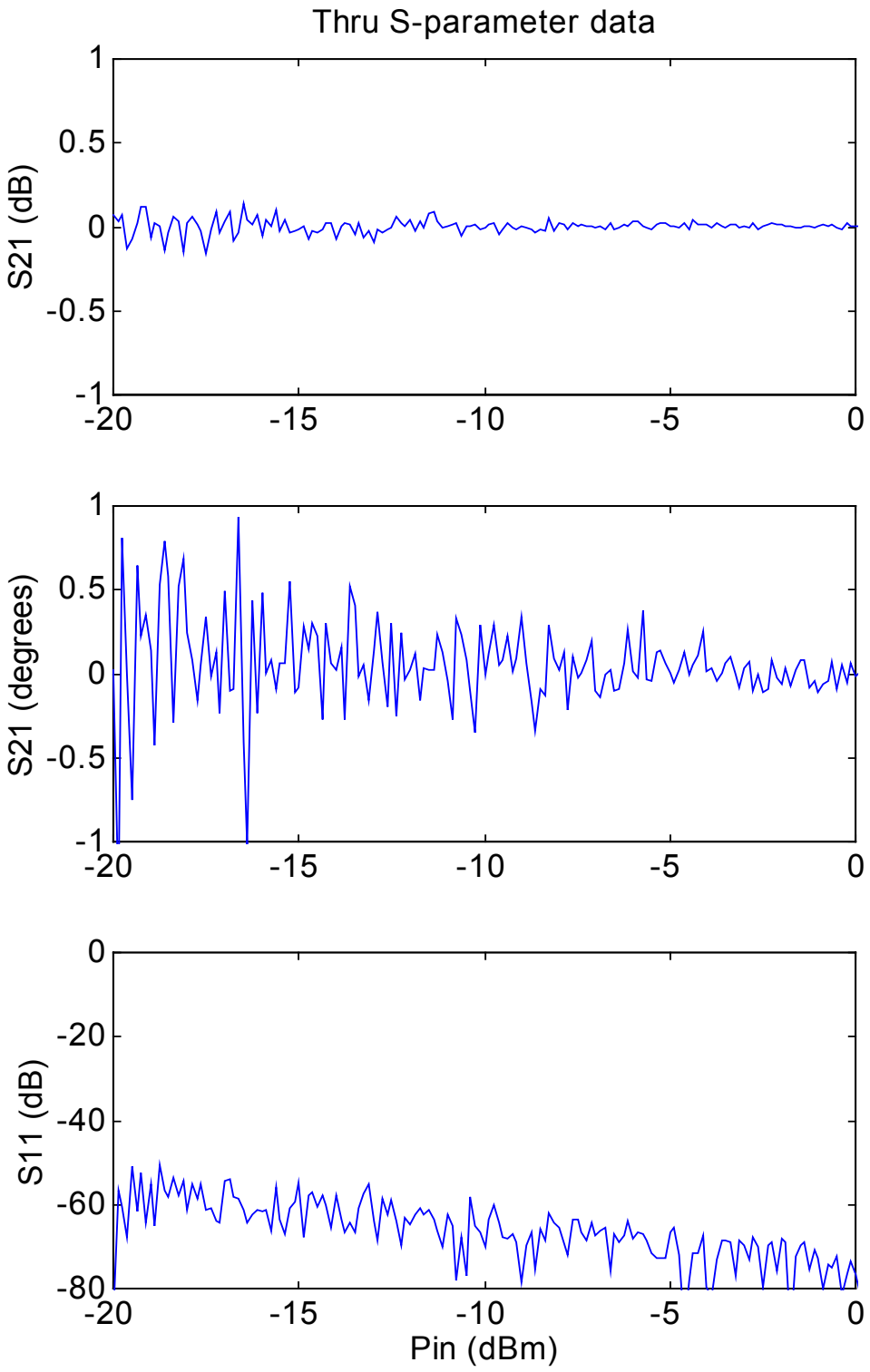


Figure 3.4 S-parameter data for through line for verification of calibration

which is acceptable when measuring S_{21} magnitudes of several dB and phases of tens of degrees of S_{21}. Note that this noise is due to low power levels reaching the detector in the VNA receiver. If attenuation is added into the system to reduce either port 1 or port 2 power levels for safety or drive level adjustment, more noise may exist in the calibration due to further limitations of the dynamic range of the VNA receiver detectors.

3.3 Diode Characterization Results

Diodes with 50μm to 2400μm gate peripheries were initially studied at 1.9 GHz. The parameters of interest are input RL (S_{11} in dB), *insertion* loss (IL) (S_{21} in dB), AM-AM, and AM-PM. AM-AM is derived from the log of S_{21} *normalized to the small-signal value*, and AM-PM is derived from the angle of S_{21} *normalized to the small-signal value*. To optimize the diode for this application, minimum IL, maximum RL, and moderate AM-AM and AM-PM are desired. The diodes must be forward biased near the turn-on voltage to set the initial small-signal operating point. When the diode is biased at this point, the RF power will be rectified, modifying the diode operating point and varying the R and C values in the equivalent RC network. For a GaAs MESFET based diode, the turn-on voltage is approximately 0.6V.

It was found that the larger diodes require much more RF drive level to get a reasonable change in operating point due to RF rectification. Initial power sweeps of –20 to 0 dBm were performed on 1200 and 2400μm sizes for biases in the range of 0 to 0.9V. No noticeable operating point shift could be seen, indicating that these diodes were too large for this power range. Further investigations showed that the 1200μm diode started to exhibit some operating point shift when the power drive was increased to ~ +10 dBm. For higher power applications, such as a PA with a higher required input drive level before becoming nonlinear, larger diode sizes may be necessary. However for the target PA in this chapter, the power range of interest was ~ -20 to 0 dBm or so.

Subsequently, smaller diodes of 50, 100, 200, and 300μm gate periphery were measured. A shift in operating point due to RF rectification was apparent in this power range. For

example, Figure 3.5 shows the measured S-parameter data versus input power and forward bias for a 50μm diode. One can see that as the bias is increased, less RF drive is needed to shift the operating point with the input power. In addition, the diode R in the equivalent RC network is being changed with the bias and input power. A nonlinear change in gain and phase with increasing input power can be seen. This is the AM-AM and AM-PM characteristic trend that is desired. Approximately 0.6V bias in this set of plots gives moderate AM-AM and AM-PM, while minimizing IL and maximizing RL. Although the IL and RL are relatively poor, the curves show that the nonlinear RC network concept works. The results of the 100, 200, and 300μm diodes are similar, but with higher RL and lower IL. At ~0.6V forward bias, it was found that a medium sized diode (~500μm) exhibited the smallest IL and the best RL at small signal for this process. The good RL obviates the need for external matching. In addition, this optimization of RL removes the need for isolators (as used in [15]), improving the ability to integrate the linearizer into an RFIC or MMIC. An inspection of the circuit's AM-AM curve (S_{21} in dB) shows a decrease in IL with an increasing input power, or "gain expansion". This circuit must therefore be driven harder to overcome the IL - this represents a drawback of this particular linearization scheme. In addition to the above considerations, the required AM-AM and AM-PM compensation for the PA to be linearized must be established.

Figure 3.6 shows the measured S-parameters for the 300μm diode for a much smaller range of bias voltages. The better IL and RL of this diode can be seen here. Also note that 10mV steps in the bias have a significant effect on the operation of the circuit; this is because the diode is biased in the knee of the diode I/V curve. Process variations may have an effect on where this knee occurs; thus, an accurate and variable voltage source is necessary to control this bias. The implication of this bias accuracy requirement for on-chip applications is that a separate diode bias control pin may be necessary, increasing the required package size. In addition, this bias may need to be thermally stabilized to compensate for variations in the diode I/V characteristic with temperature, increasing power supply complexity. The bias steps here correspond to changes in the amount of

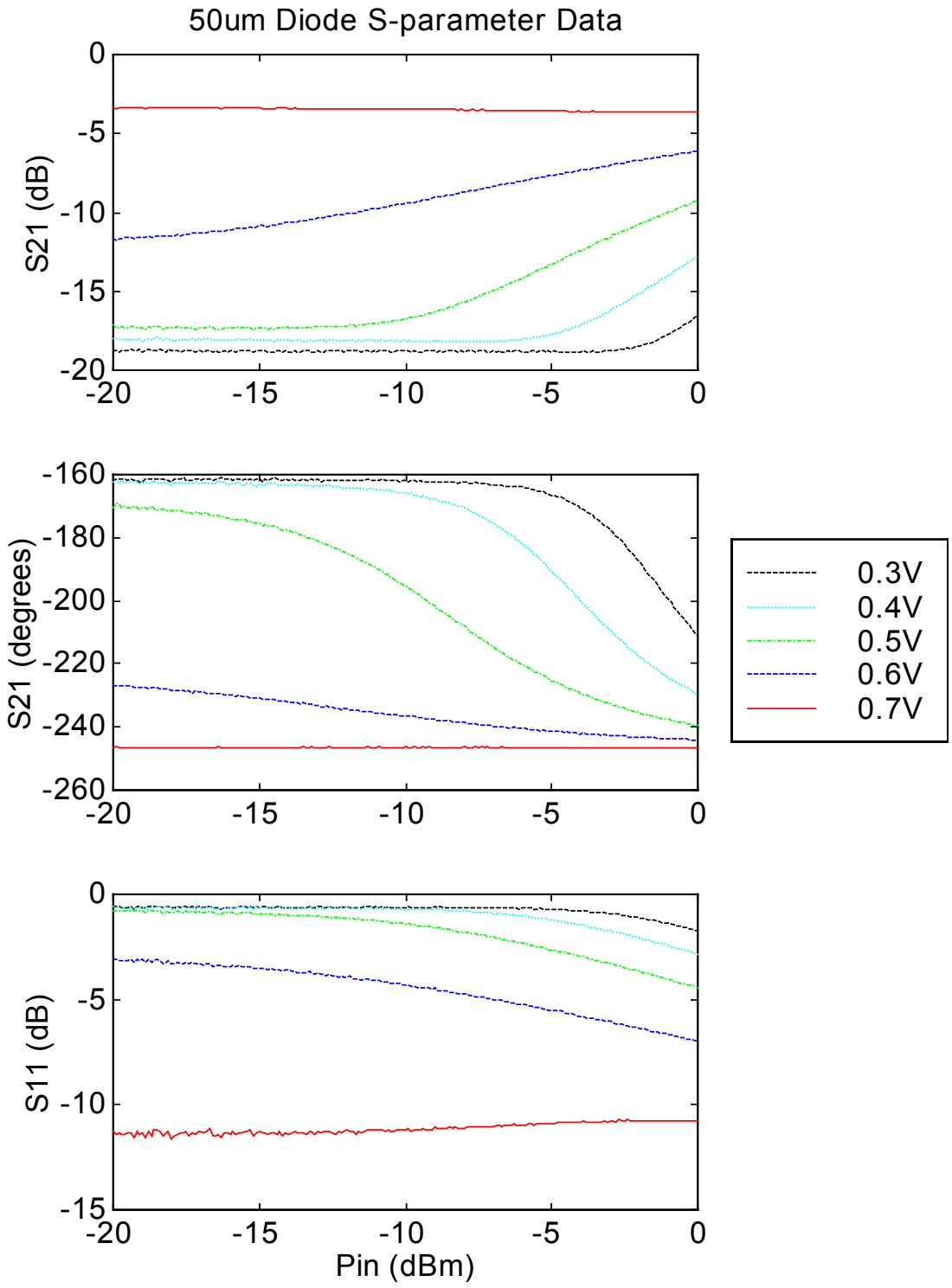


Figure 3.5 50µm diode S-parameter data versus input power and bias at 1.9 GHz

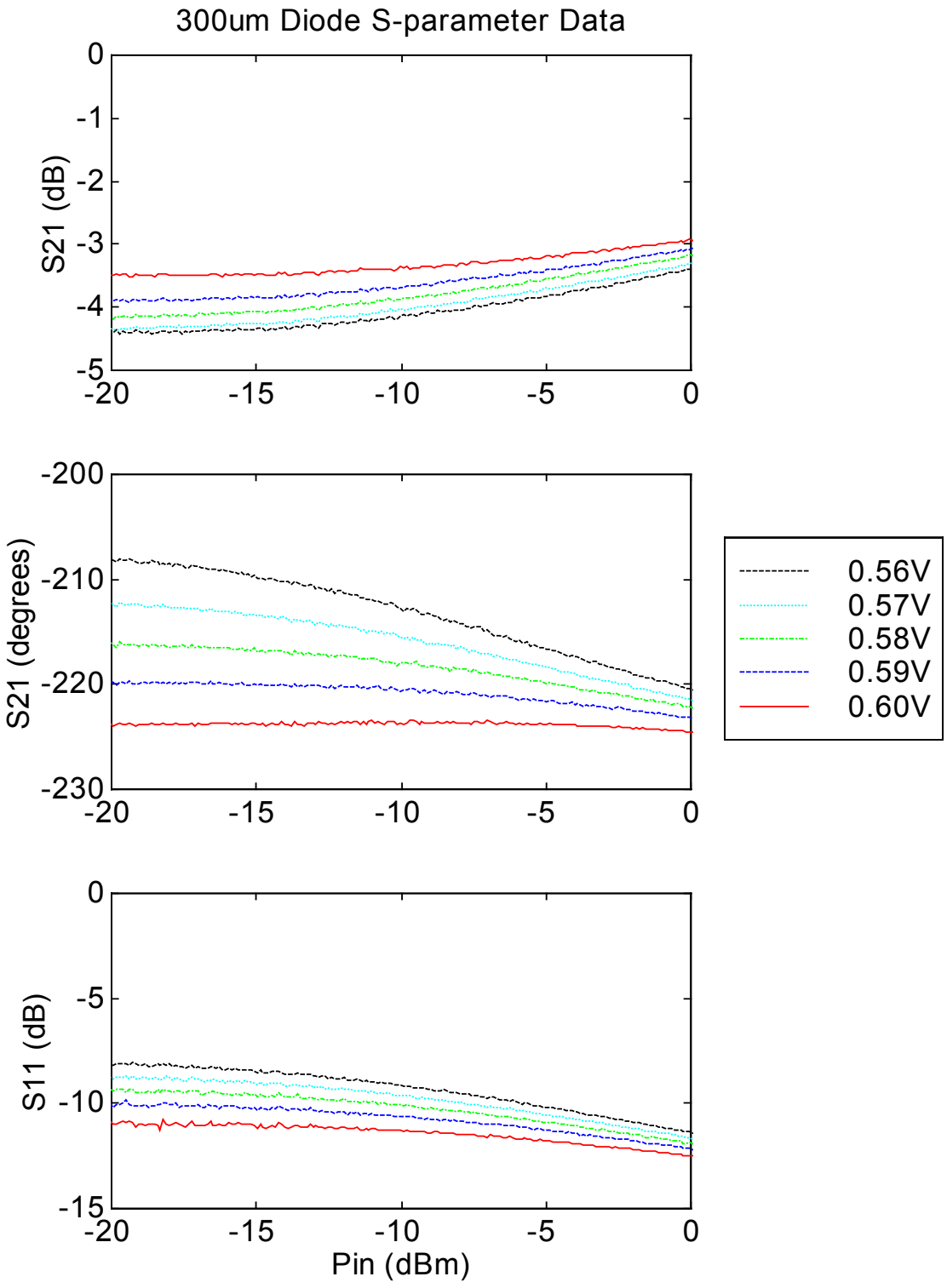


Figure 3.6 300µm diode S-parameter data versus input power and bias at 1.9 GHz

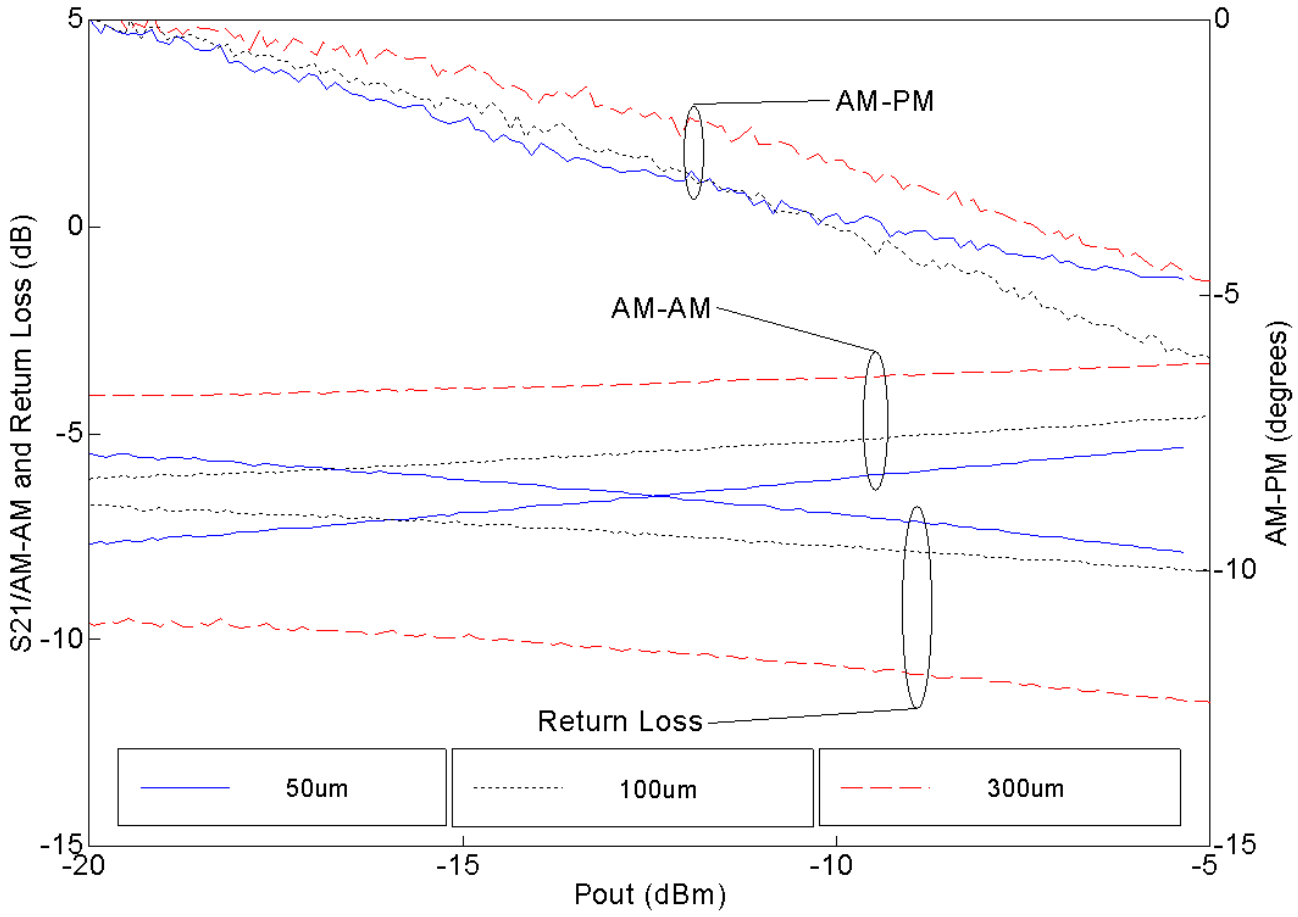


Figure 3.7 Measured AM-AM, AM-PM, and RL for a 50, 100, and 300µm diode biased for roughly 5 degrees of AM-PM at 1.9 GHz

AM-AM and AM-PM and may be used as an adjustment for matching the AM-AM and AM-PM of a nonlinear PA. The 500µm diode exhibits even better RL and IL, but at the expense of AM-AM and AM-PM. The parasitic capacitance of the diode, which is used as part of the equivalent RC network, increases as the diode size increases. At a certain point, the R and C of the diode will not be sufficient to achieve the required AM-AM and AM-PM over a given input power range.

Figure 3.7 shows a plot of the AM-AM, AM-PM, and RL for 50, 100, and 300µm diodes. The bias for each diode was adjusted to obtain roughly 5 degrees of AM-PM. Adjustment of the bias provides an extra degree of freedom in controlling the diode AM-AM, AM-PM, RL, and IL once the diode size has been fixed. The data in the figure is plotted versus

output power since this is the power arriving at the PA input, allowing the diode IL to be neglected for the time being. It can be seen that for roughly the same AM-PM characteristics, the larger diode has less IL, higher RL, and less AM-AM. The 300μm diode input impedance is approaching 50Ω, meaning that this diode will have a relatively minimal impact on the input match of the PA if used as a predistortion linearizer. In addition, for a lower IL, less additional input power is needed to properly drive the PA. This is important since excessive IL may negate the ACPR improvements with the linearizer due to increased linearity requirements on the driver stage. A small amount of AM-AM correction (a few tenths of a dB) is possible; however, since the effectiveness of phase correction is stressed in [20], AM-PM compensation was made the focus of this study.

As has been shown above, for a hybrid linearizer circuit, performance can be tuned by swapping in other diode sizes. However, for a fully integrated linearizer, the ability to accurately simulate the nonlinear diode characteristics is important for reducing the number of die fabrication runs. Large signal S-parameter simulations were performed in HP EEsof Libra [27]. The model used for the MESFET diode is based on the ITT GTC Scalable Voltage Variable model of a MESFET unit cell (discussed in section 3.1) with a total gate periphery of 1000μm. The MESFET diode is simulated by tying the drain and source together in the circuit schematic. To verify the validity of these models, a 500μm gate periphery diode biased at 0.57V was simulated in HP EEsof Libra. Ideal biasing chokes and capacitors were used in the circuit schematic, which was arranged as shown in Figure 1.10. However, the simulated S-parameters for this diode did not correlate well with measured data. Measurements show that the turn on voltage for these diodes is about 0.6V; however, the simulated diode showed a turn on voltage of about 1.5V. Obviously, this approach does not accurately model the source-drain connected diode; a more accurate Schottky diode model must be developed to support future integrated linearized PA design.

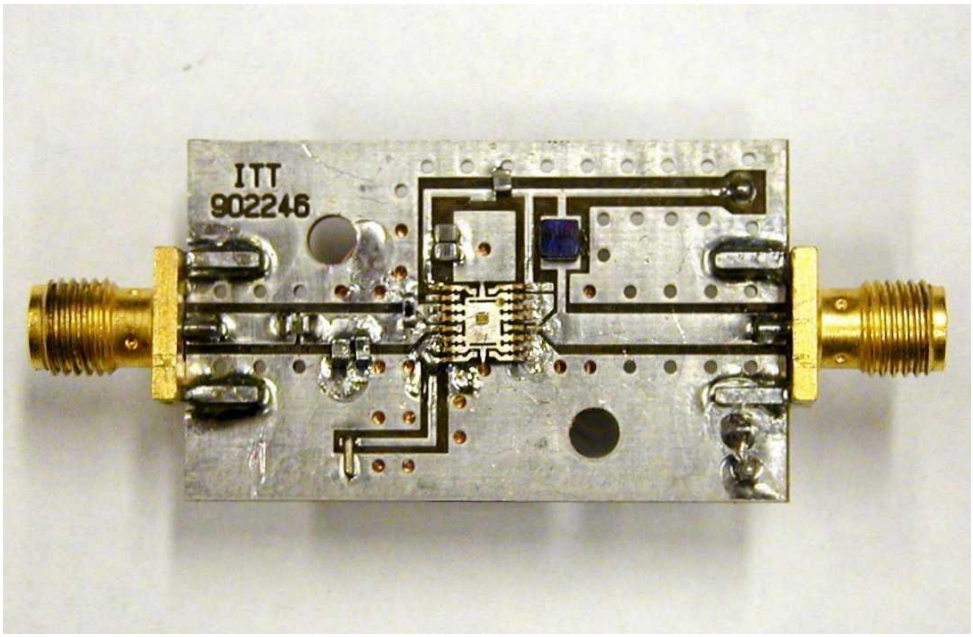


Figure 3.8 2.68 GHz MESFET PA and test PCB

3.4 PA Characterization

A 1.9 GHz PCS band PA was the initial target amplifier; however, due to availability problems, a 2.68 GHz GaAsTEK MESFET PA was used instead. This PA was fabricated in the same process as the 1.9 GHz PA and is similar in topology and nonlinearity characteristics. Applications for this PA include Bluetooth and wireless LAN. The PA is mounted in a lead frame package and matched to 50Ω at the input and output on a test PCB as shown in Figure 3.8.

The PA operates from a +5V supply at <100mA with a grounded gate bias. The small-signal gain is about 22dB and the saturated output power is approximately +22dBm. Due to this high saturated output power, the PA output must be attenuated prior to the VNA test port. The test setup for characterizing the PA is shown in Figure 3.9. The 20dB pad on

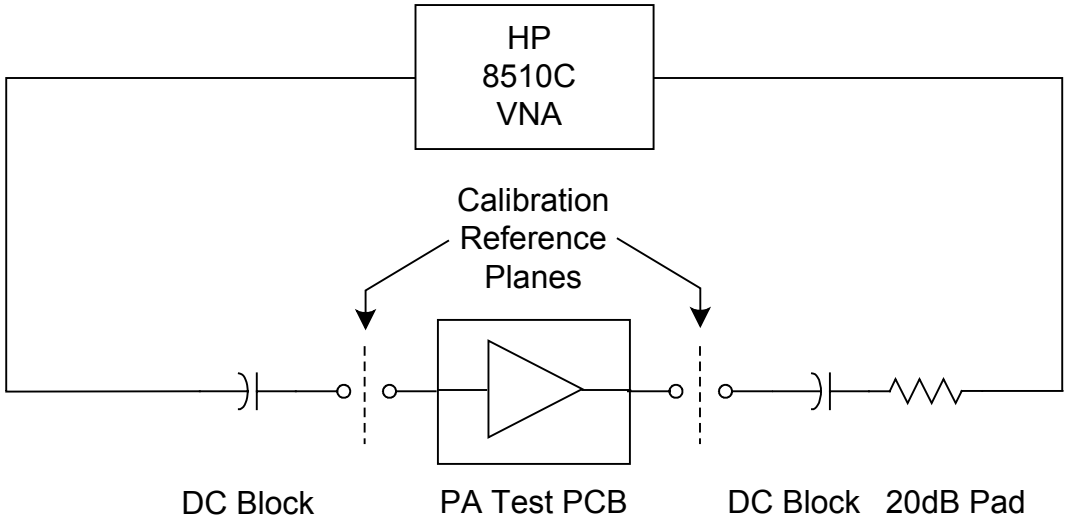


Figure 3.9 Block diagram of test setup used to characterize PA

the VNA port 2 input is used to reduce the PA output power to a safe level prior to the VNA test port. In addition, DC blocking capacitors are used to ensure that no DC bias from the PA reaches the VNA test ports. These DC blocks and the 20dB pad are included in the VNA two-port calibration. The effect of this attenuator in the calibration is the addition of noise as previously discussed in Section 3.2. The same measurement procedure used for diode characterization is used for the PA. Measurements were performed at 2.68 GHz and a PA input power sweep of –20 to 0 dBm.

Results of the PA characterization are shown in Figure 3.10; in this input power range, the PA exhibits ~2.6 dB of AM-AM and ~18 degrees of AM-PM. This data is used in conjunction with the diode data to choose a diode size and bias that results in the best match to the PA AM-AM and AM-PM.

3.5 Diode Choice to Match PA

The diode measurements at 1.9 GHz were representative enough to use as a guide for choosing the proper size diode for the 2.68 GHz PA. The 300 and 500μm diodes were then re-characterized at 2.68 GHz. The 2.68 GHz data varies slightly from the 1.9 GHz due to the effect of the parasitic diode capacitance and its corresponding impedance.

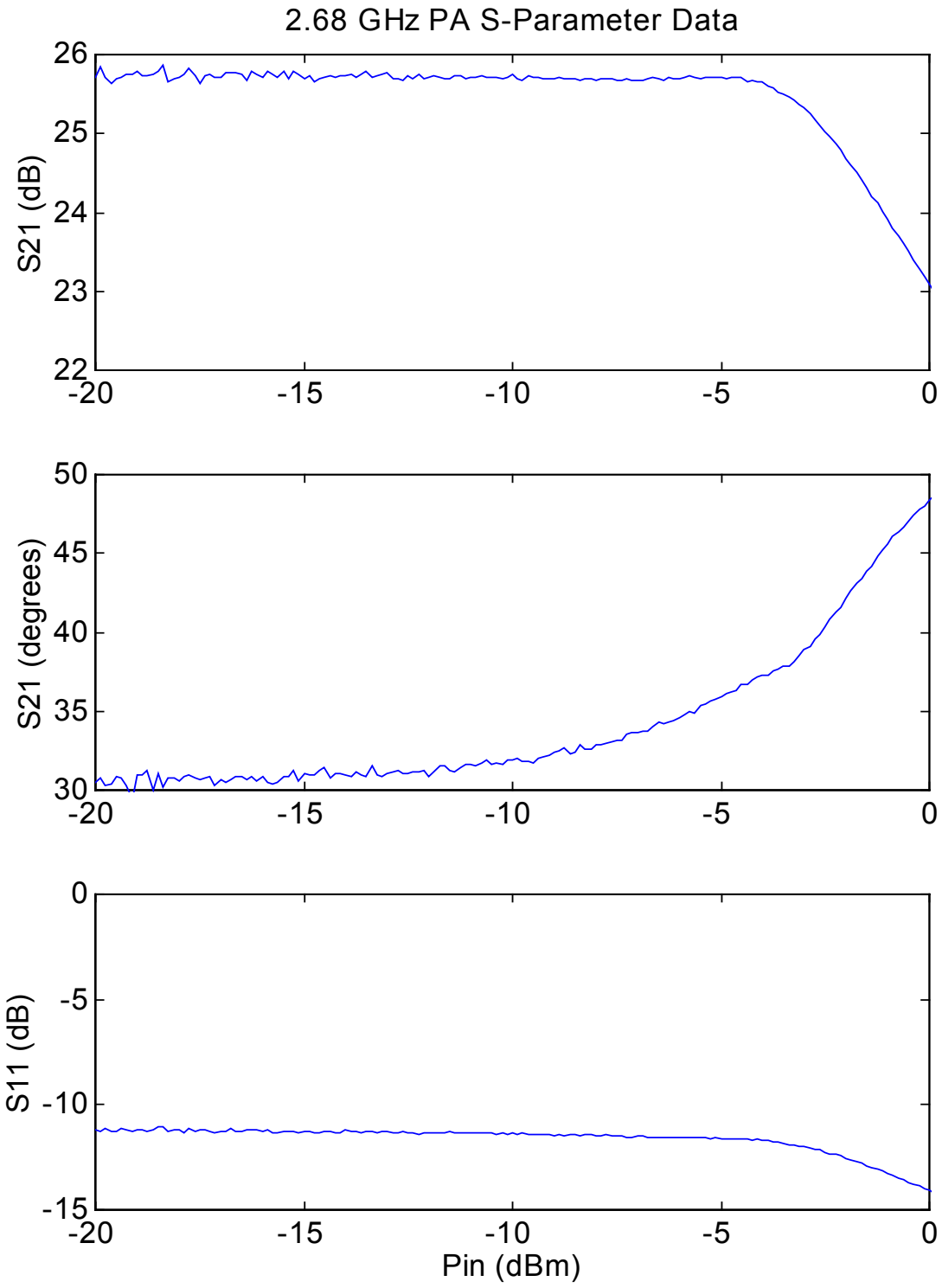


Figure 3.10 2.68 GHz MESFET PA S-parameters versus input power

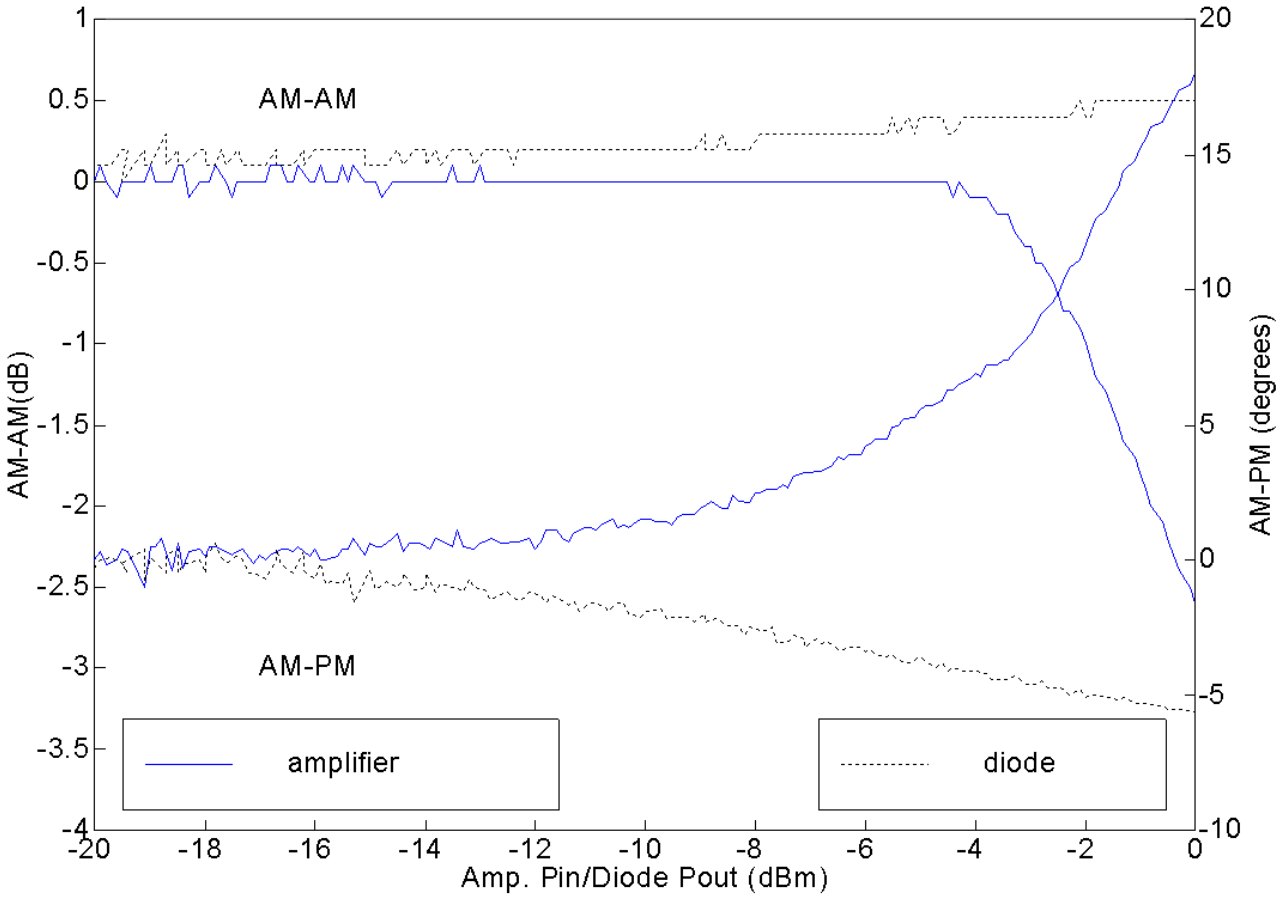


Figure 3.11 PA and 500µm diode (biased at 0.57V) AM-AM and AM-PM at 2.68 GHz

However, in terms of rough sizing, the two frequencies are close enough. An inspection of these new diode results and the PA characteristics shows that a 500µm diode biased at 0.57V provides the necessary compensation with an input small signal RL of ~15dB and IL of ~2.2dB. Figure 3.11 shows the PA and the 500µm diode (biased at 0.57V) AM-AM and AM-PM curves on the same plot. The AM-AM curves show the potential for slight improvement. The AM-PM curves show a noticeable possibility of improvement on the order of ~ 6 degrees.

The next step is to place the 500µm diode PCB in series with the PA PCB to observe linearization performance. The HP Vee measurement program is used with the test setup shown in Figure 3.12. The only additional component here is the bias tee between the diode and PA necessary for completing the diode bias circuit. This will introduce an extra

IL on the order of ~0.2 dB at this frequency; however, this is not a significant problem since the diode IL is considerably larger.

Figure 3.13 shows the results for the diode and PA cascaded together to form a linearized circuit using this test setup. A clear reduction in AM-PM, as well as a slight reduction in AM-AM, can be seen in this figure. This diode linearizer is operating as expected in terms of flattening AM-AM and AM-PM curves.

3.6 ACPR Results

For the linearized MESFET PA discussed above, a set of ACPR measurements was performed. ACPR was measured for some common types of complex digital modulation with different PTARs and an average PA output power of +15 dBm. The test setup for this measurement is shown in Figure 3.14. A Rhode & Schwartz SMIQ signal generator was used to generate the signal at the maximum average power needed for all measurements. A variable attenuator was placed at the output of the signal generator to keep the signal generator's inherent ACPR constant as the drive level was varied. Since the signal generator is itself nonlinear to some degree, it generates its own ACPR; this will vary as its power is stepped higher and into compression. A linear adjustment of power is achieved using this variable pad to minimize variations in ACPR versus power due to the signal generator. A 20 dB directional coupler is used to monitor the power drive level to the linearized PA or standalone PA as the attenuator is adjusted. In the linearized PA case, the input power must be increased to overcome the linearizer IL.

The results are summarized in Table 3.1. ΔUACPR/ΔLACPR is the upper/lower channel ACPR *improvement* due to the linearizer. The baseband filtering used is the IS-95 specified filter for a CDMA mobile station. ACPR was measured in a 30 kHz channel, 1.25 MHz away from f_c for a 1.25 MHz chip rate [25]. An example PA output spectrum for OQPSK modulation is included in Figure 3.15.

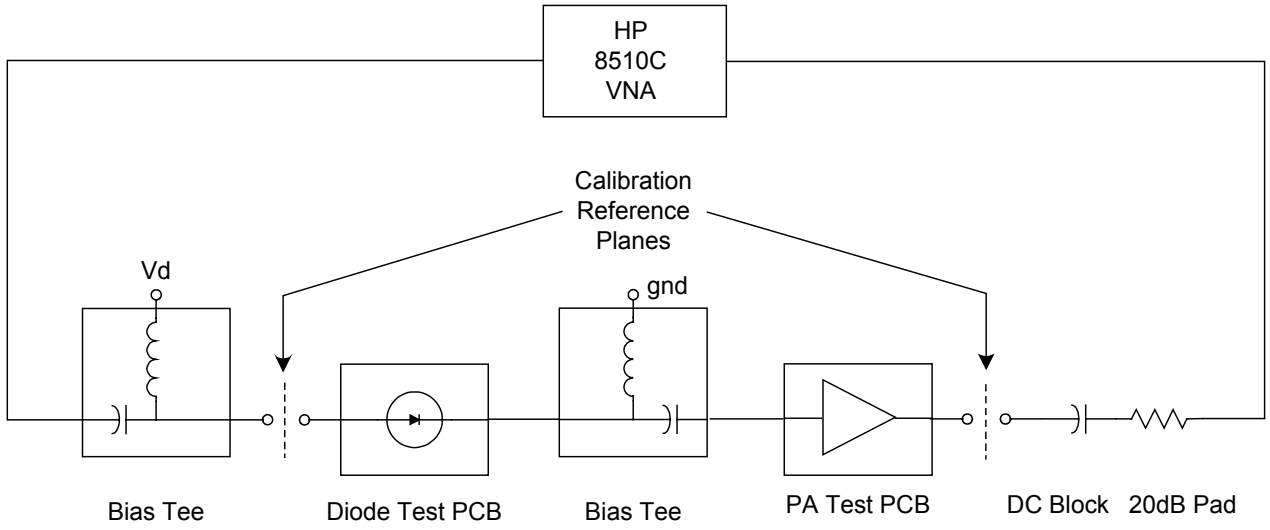


Figure 3.12 Block diagram of test setup used to characterize PA and diode predistorter together

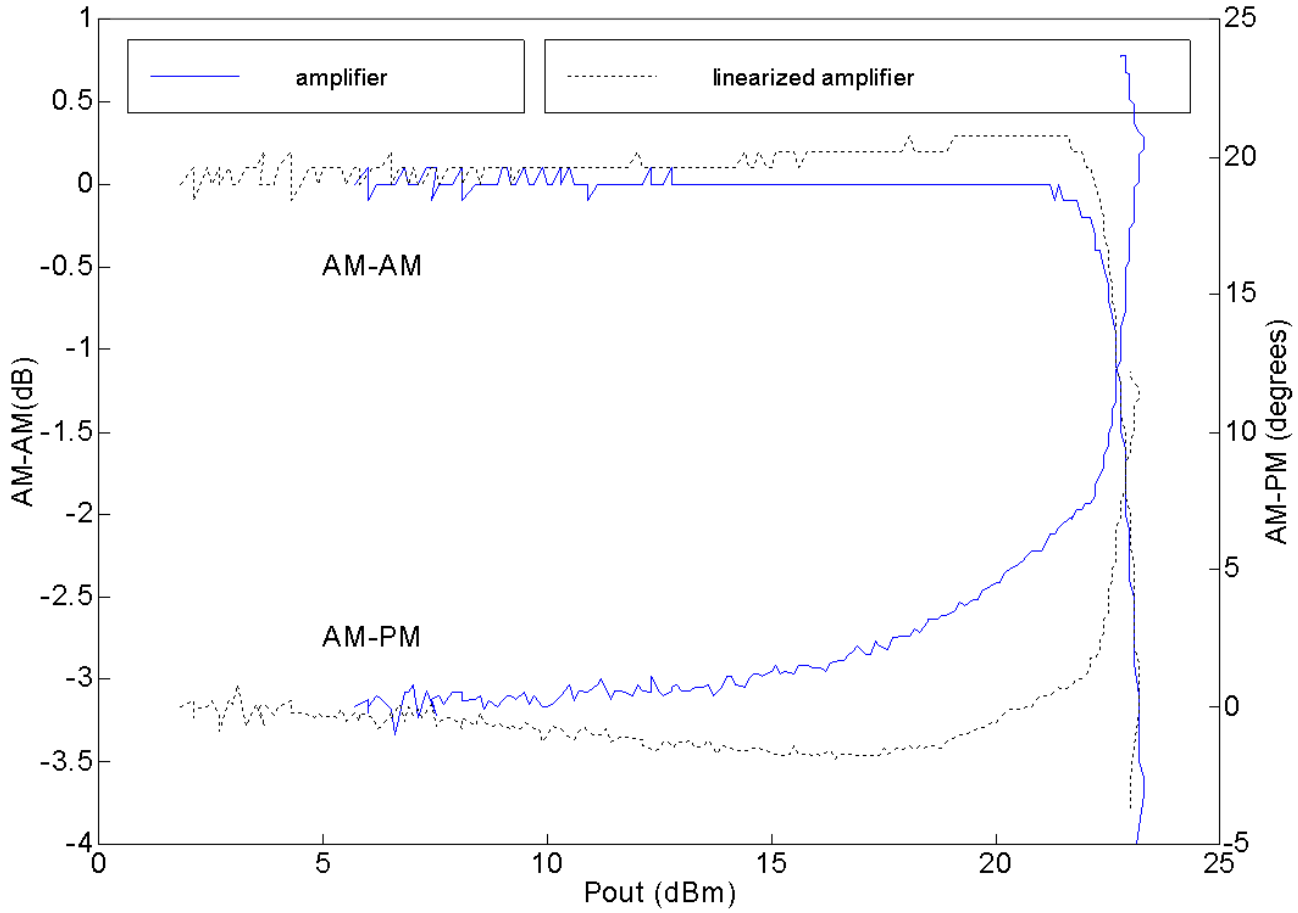


Figure 3.13 AM-AM and AM-PM results of linearized and standalone PA at 1.95 GHz

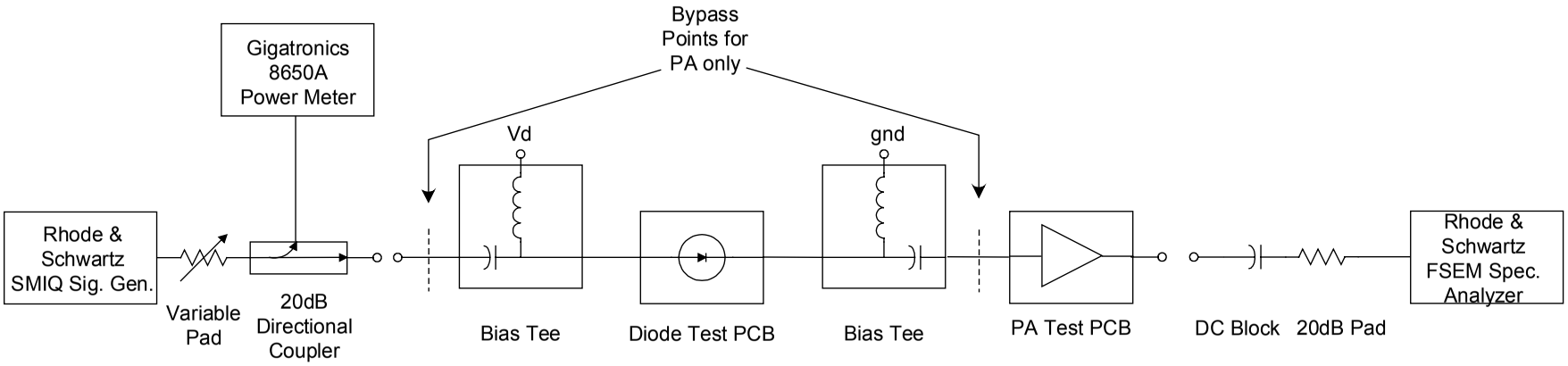


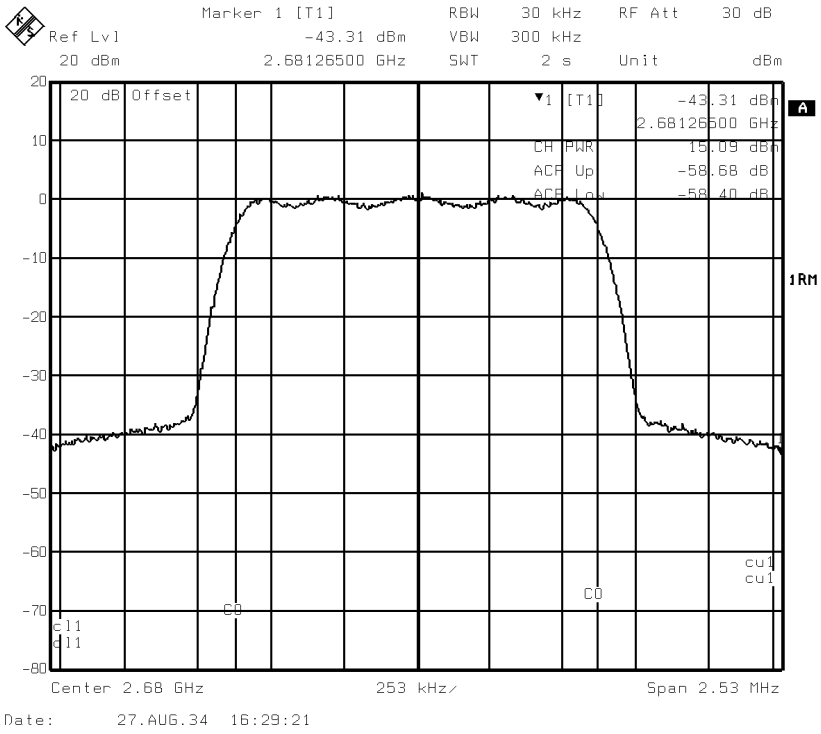
Figure 3.14 Block diagram of test setup used to characterize ACPR of linearized and standalone PA

Table 3.1 ACPR improvement due to linearizer for various modulation and PTAR

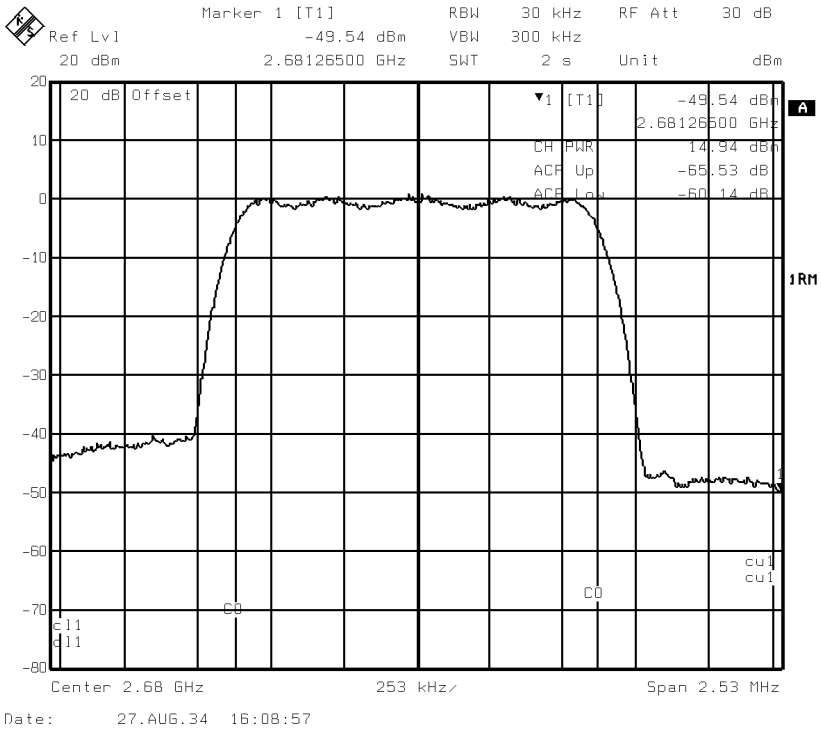
Modulation	PTAR (dB)	ΔUACPR (dB)	ΔLACPR (dB)
QPSK	6.84	5.8	2.2
OQPSK	5.49	6.7	1.7
Pi/4 DQPSK	6.14	5.7	1.6
16 QAM	9.37	4.9	1.8
256 QAM	11.05	4.9	2.1

These results show that the linearizer is most effective for signals with a lower PTAR. A high PTAR pushes the signal much further into the compression region, thus having a much more detrimental effect due to the nonlinearity. To effectively linearize a signal under high PTAR conditions, the linearizer would have to be able to generate the peaks that the PA cannot (see Figure 2.8 in Chapter 2). Some form of post-distortion would be required. These results show that flattening AM-PM results in an improved ACPR. For higher output power where the PA is operating further into compression, there is less or no envelope correction from the linearizer, thus there will be less or no improvement in ACPR as power increases. At small signal or high back-off, the only effect of the linearizer is to introduce IL, thus there will be no improvement in ACPR at high back off conditions. This means that the linearizer works best at points of slight back off from or near compression.

There is a discrepancy between upper and lower ΔACPR results. One brief investigation of this asymmetry was performed. Since this linearizer is used as a nonlinear RC phase shift network to cancel out AM-AM and AM-PM, the harmonic distortion generated by the diode is not being used to cancel out IMD products as in other predistortion methods [13][14]. If these diode distortion products are significant, then they may actually be degrading the results by constructively adding with the distortion products in the PA. To investigate this, an RLC Electronics 4 GHz low pass filter was placed after the diode output bias tee (Figure 3.14) to filter out the diode harmonics. No second or third harmonics could be seen above the noise floor in the output signal from this filter on a



(a)



(b)

Figure 3.15 Spectrum plots for filtered OQPSK modulation at output of (a) standalone PA (b) linearized PA

spectrum analyzer. The ACPR was then measured with the filter as detailed above. No difference in the ACPR results could be seen, indicating that diode harmonic distortion was not causing the asymmetry.

In [1], the asymmetry due to AM-PM is discussed in the context that different physical device mechanisms are responsible for AM-AM and AM-PM. The *phase difference* between the mechanisms causing AM-AM and AM-PM may be introducing the asymmetry problem. The fact that AM-PM IMD products may constructively or deconstructively add with the AM-AM IMD products due to this phase difference may account for the asymmetry. Further investigation is necessary to explore reduction or elimination of the asymmetry.

3.7 Conclusions

In conclusion, the 2.68 GHz MESFET PA linearization was successful using the series diode predistorter; AM-AM and AM-PM compensation was achieved using minimal additional circuitry. An improvement in ACPR was measured for modulation schemes with a range of PTARs. OQPSK had the smallest PTAR, experiencing a 6.7dB improvement in one sideband, while 256QAM had the highest PTAR, experiencing a 4.9dB improvement in one sideband. This shows that a reduction in AM-PM using the optimized series FET diode linearizer presented here does lead to an improvement in ACPR. However, the linearizer may alternatively be optimized for either AM-AM or AM-PM, or both.

The linearized PA exhibits an improved ACPR over the standalone PA with the same output power. However, the requirement of more drive level to overcome the 2.2dB small-signal IL of this linearizer circuit must be weighed carefully with efficiency requirements. In addition, the ability to accurately control the diode bias in steps of approximately 10mV in this application is important. Thermal and process related variations in the diode bias should also be compensated for to accurately control AM-AM and AM-PM reduction. Finally, the ACPR improvement shows an asymmetry between the upper and lower

channels. It is suggested that the phase difference between the IMD products due to AM-AM and AM-PM mechanisms is the likely cause. The presence of diode harmonic distortion on the signal as a cause of the asymmetry has been ruled out.

Chapter 4 will extend the above study to an HBT based process and PA. This will demonstrate the flexibility of this linearization technique in addition to providing another linearized PA case study.

4 HBT Diode Optimization for Series Diode Predistorter

The advantages of using the series diode predistorter have been demonstrated using a GaAs MESFET diode and PA. Due to the advantages of improved power densities over MESFETs as well as using a single, positive supply in modern handheld radios, *heterojunction bipolar transistor* (HBT) technology is emerging as the potential technology of choice for PAs. Therefore, it is logical to investigate the linearization techniques previously used with MESFET amplifiers for use with HBT amplifiers. The purpose of this chapter is to extend the series diode predistortion technique to an HBT process and compare the results to the MESFET demonstration from Chapter 3.

4.1 Background

A nonlinear HBT PA is the target for linearization in this chapter, thus the diode used should also be HBT based. The intent was to use both a PA and diode from GaAsTEK's HBT foundry source, but due to availability issues an RFMD PA was used for proof of concept. GaAsTEK HBT PAs are still in the development stage and are not mature enough for experiments in this chapter, however, HBT diodes of varying sizes were fabricated through the foundry for proof of concept. An RFMD RF2128P HBT PA was used in this initial study. The intent was to linearize a 1.95 GHz PA similar to that used in the preceding MESFET study.

To realize the diode, a collector-base connected HBT is fabricated. The base-emitter junction forms the diode. The base serves as the anode and the emitter serves as the cathode. The device size is based on an $80\mu m^2$ unit cell (Figure 4.1). This unit cell consists of a double-emitter structure with each emitter having dimensions of 2μm x 20μm. This results in a 2 x $40\mu m^2$ = $80\mu m^2$ total emitter area. This emitter area is adjusted to optimize the diode size for predistortion applications. Emitter areas from $20\mu m^2$ to $360\mu m^2$ were studied at 1.95 GHz.

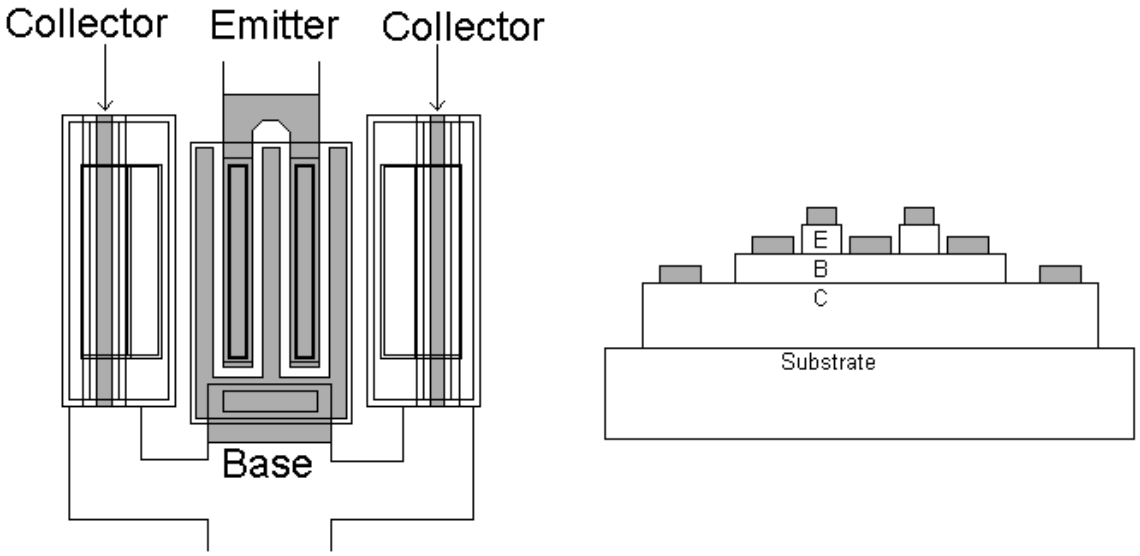


Figure 4.1 Topology of HBT diode: (left) top view, (right) side view

4.2 Diode Characterization

The same measurement setup as was used in the MESFET study in Chapter 3 was used here. Refer to Section 3.2 for a detailed discussion of this setup. Diode measurements at 1.95 GHz were performed in the same fashion as described in Section 3.3. For these HBT diodes, the turn on voltage is approximately 1.25V. Again, as expected, it was found that the larger diodes required much more RF drive level to obtain a change in operating point due to RF rectification. An input power sweep of –20 to 0 dBm was performed for biases in the range of ~ 1.2 to ~ 1.4V. At ~1.25V forward bias, it was found that a ~240μm^2 sized diode exhibited the smallest IL as well as the best RL at small signal for this process. The good RL levels obviate the need for external matching. The benefits of this size and bias optimization, as well as the drawbacks of this linearization scheme, were discussed in Chapter 3.

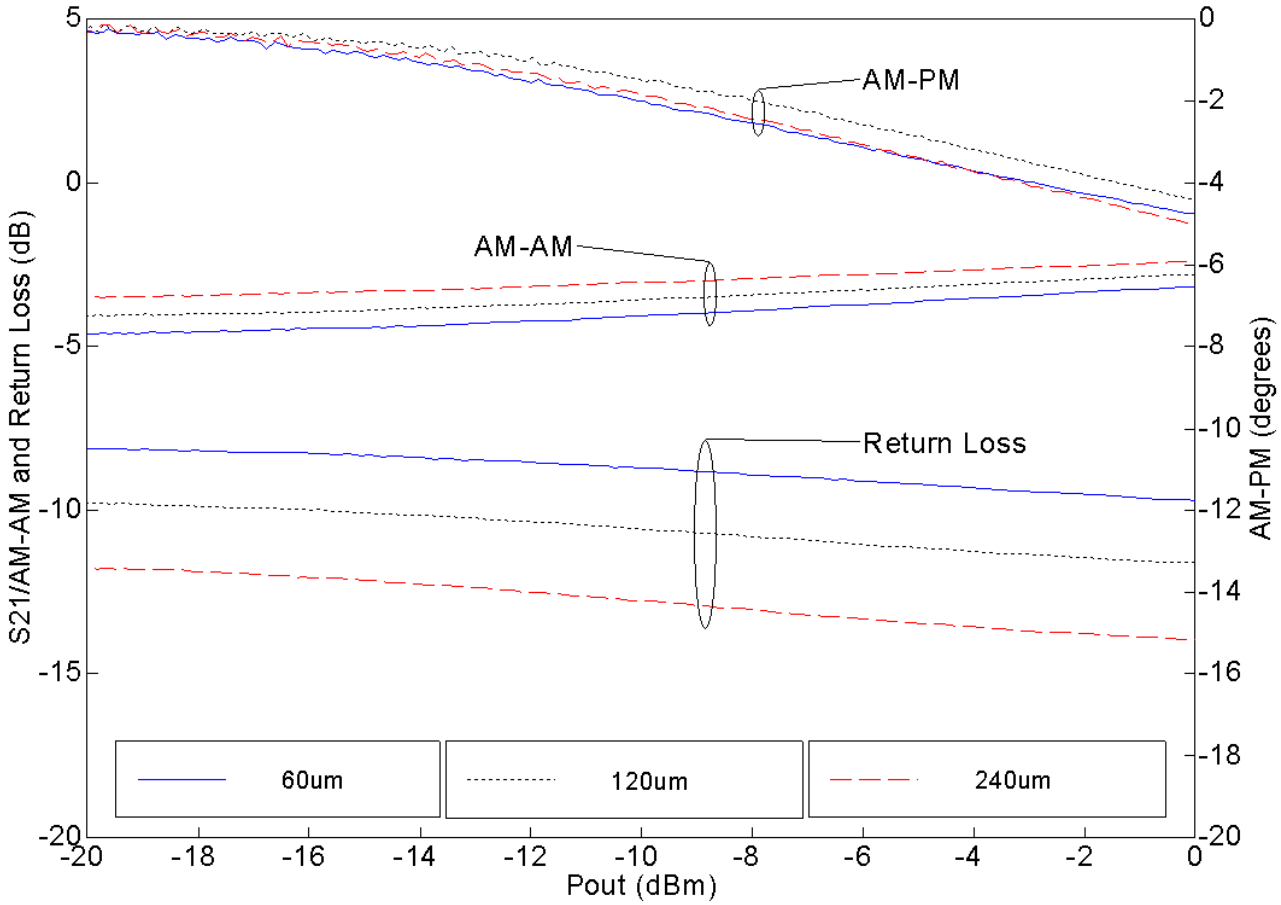


Figure 4.2 Measured AM-AM, AM-PM, and RL for a 60, 120, and 240μm^2 diode biased for roughly 5 degrees of AM-PM at 1.95 GHz

Figure 4.2 shows a plot of the AM-AM, AM-PM, and RL versus diode output power for 60, 120, and 240μm^2 diodes. The bias for each diode was again adjusted to get about 5 degrees of AM-PM. The results are similar to the MESFET diodes presented in Chapter 3. It can be seen that for about the same AM-PM, the larger diode (240μm^2) has less IL, higher RL, and about the same AM-AM. The 240μm^2 diode would be the best choice for a 50Ω system requiring moderate AM-AM and AM-PM correction.

In addition, large signal S-parameter simulations were performed in HP EEsof Libra. The models used for the HBT diode are based on a Gummel Poon model for the HBT unit cell discussed in Section 4.1. The HBT diode was simulated by tying the collector and base together in the circuit schematic. To verify the validity of these models, a 240μm^2 diode biased at 1.25V was simulated in HP EEsof Libra. Ideal biasing chokes and capacitors

were used in the simulated circuit, which is implemented as shown in Figure 1.10. The results are displayed in Figure 4.3. The measured and simulated S-parameters at 1.95 GHz for the 240μm^2 diode biased at 1.25V are in good agreement. The only major difference is a roughly 1dB higher IL for the measured diode. This difference results from the bond wires, non-ideal 50Ω transmission lines, and physical SMA end launch connectors in the measured circuit. The AM-AM and AM-PM characteristics for the measured and simulated diodes are in very good agreement. This suggests that the Gummel Poon HBT model used for this diode is accurate enough to simulate these diodes. This is important since a later stage of this project involves the integration of the linearized PA into a single RFIC chip.

Given the accuracy of this HBT device model, certain model/device parameters may be tuned to engineer the RC phase shift network at the device level. So far this study has used the diode forward bias and emitter area as a method of tuning the diode input impedance and optimizing this impedance for a 50Ω system. In addition, this tuning has been used to optimize the AM-AM and AM-PM correction for a given PA. Clearly, any additional methods of tuning the circuit would be advantageous to the designer, adding additional degrees of freedom. Since the base-emitter junction of the HBT forms the diode for this application, the base-emitter zero-bias depletion capacitance (CJE) forms the capacitance in the equivalent RC network. Varying the emitter area corresponds to a change in CJE. If CJE can be controlled otherwise in the device process, then an additional degree of freedom exists in tuning the series diode predistorter.

4.3 PA Characterization

The procedures and setups discussed in section 3.4 for the MESFET PA measurements were also used for the HBT study. In this case, the target PA was an RFMD RF2128P medium power linear HBT amplifier (Figure 4.4) designed for use in the 1900 to 2500 MHz range for PCS, 2.5 GHz ISM, and WLAN applications. The PA may be operated from a single +5V supply at ~100mA maximum current. The small-signal gain is typically ~25dB with approximately +20dBm saturated output power. Again, the amplifier output

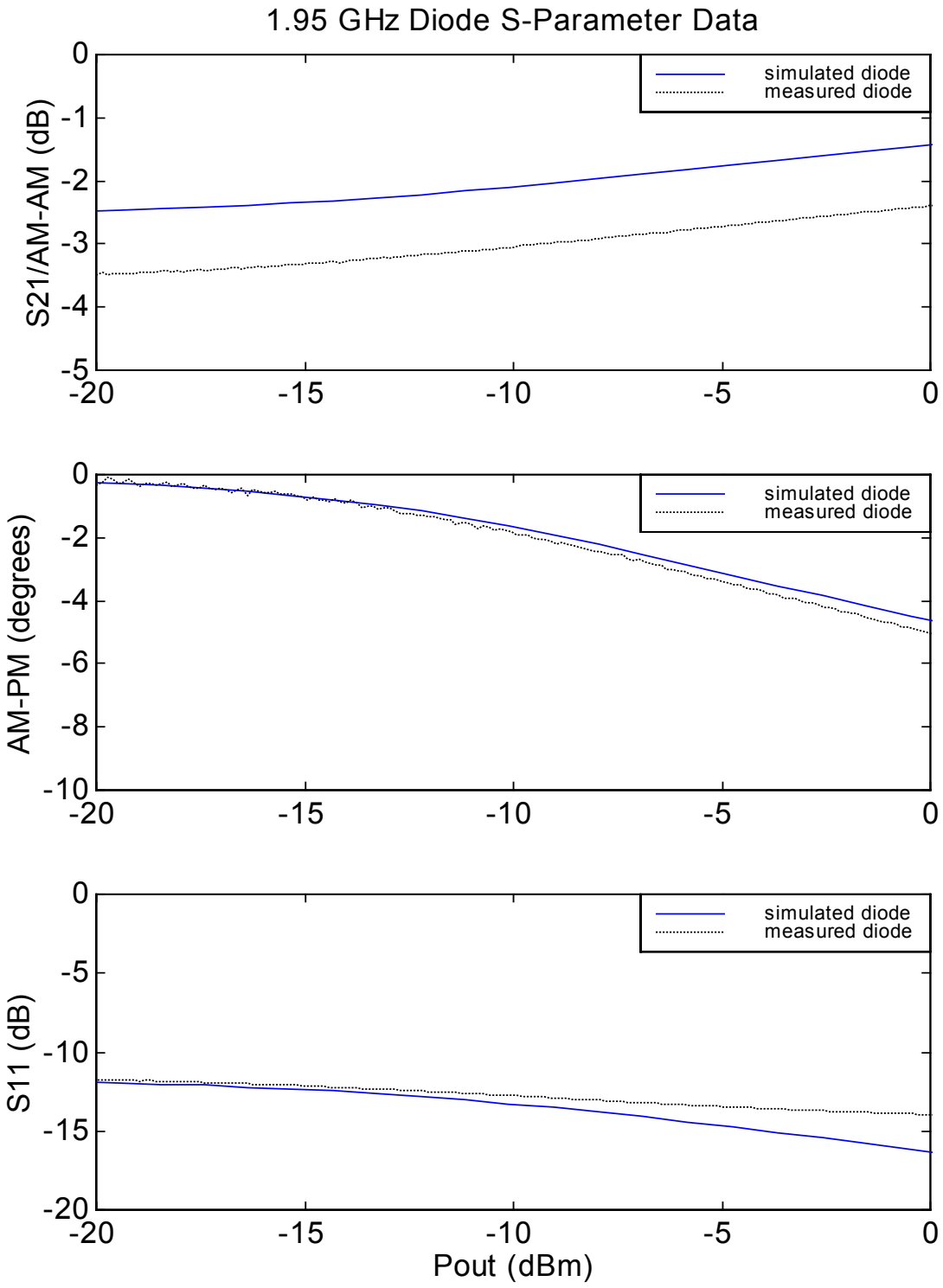


Figure 4.3 Simulated and measured S-parameters at 1.95 GHz versus output power for a 240μm^2 diode biased at 1.25V

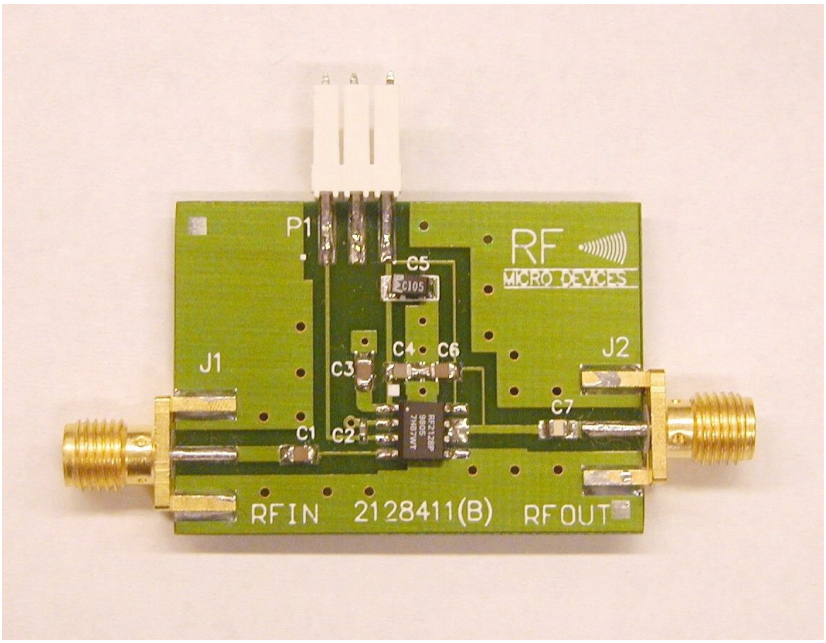


Figure 4.4 1.95 GHz HBT PA and test PCB

must be attenuated prior to the VNA test port. Data was gathered at 1.95 GHz and a PA input power of –25 to -5 dBm using the aforementioned test setup.

Measured PA S-parameter results are shown in Figure 4.5. The PA's AM-AM and AM-PM characteristic can be clearly seen. Over the measured input power range, the PA exhibits ~2.1 dB of AM-AM and ~3 degrees of AM-PM. Compared to the MESFET PA, this HBT PA has much less AM-PM distortion; this could be due to either the PA design, the HBT process used, or a combination of both.

The HBT PA has a similar amount of AM-AM compared to the MESFET PA; however, the AM-AM curve is much "softer" - the MESFET AM-AM curve is very flat until close to saturation, while the HBT curve compresses more gradually over this power range. The measurements therefore indicate that it should be easier to correct for the AM-AM in this PA compared to the MESFET PA due to the compression "softness". On the other hand, since only 3 degrees of AM-PM are exhibited, there is not much room for phase correction. Based on the measured PA and diode characteristics, a diode size and bias were chosen to result in as close of a match as possible to the PA AM-AM and AM-PM distortion.

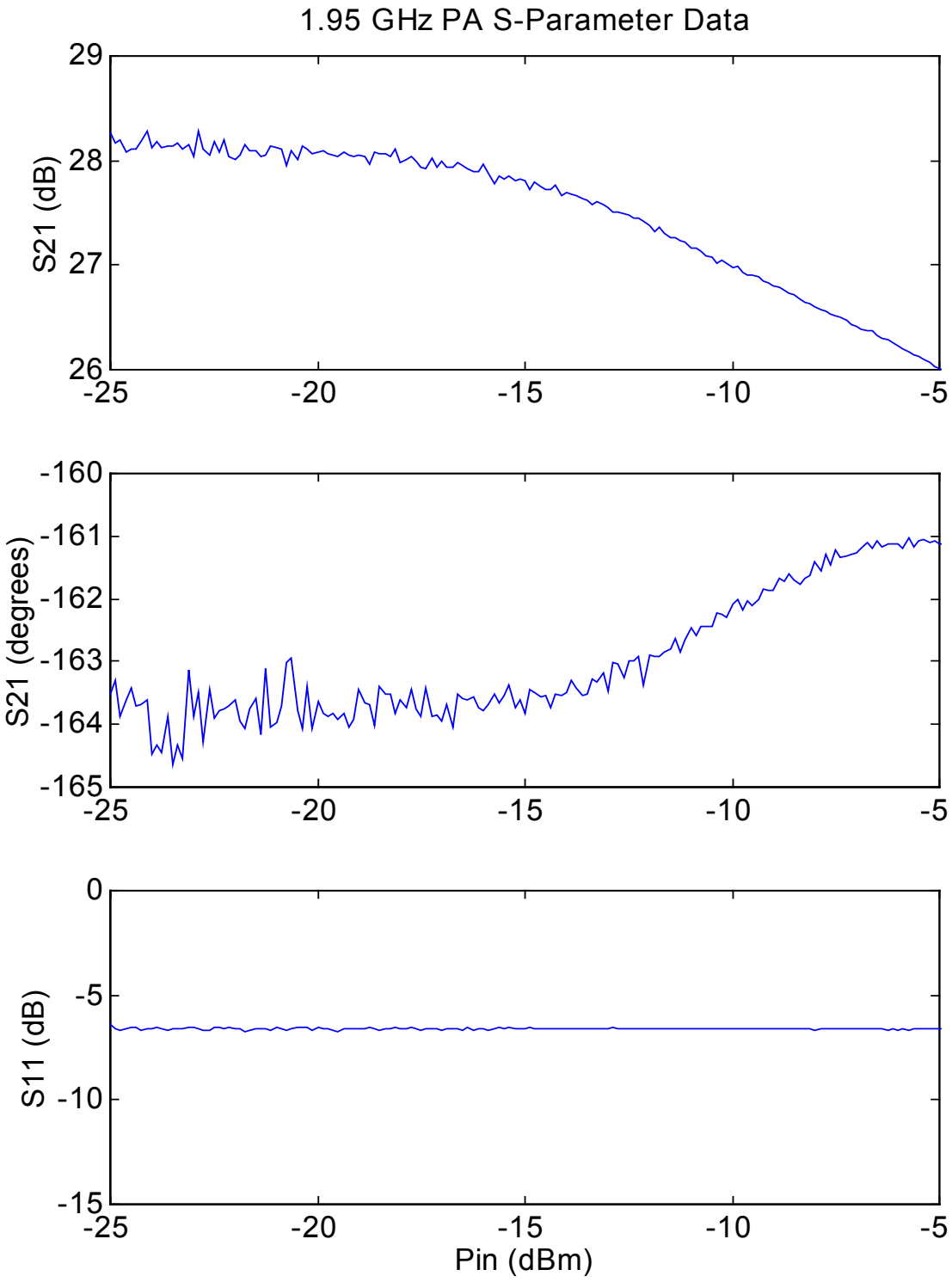


Figure 4.5 1.95 GHz HBT PA S-parameters versus input power

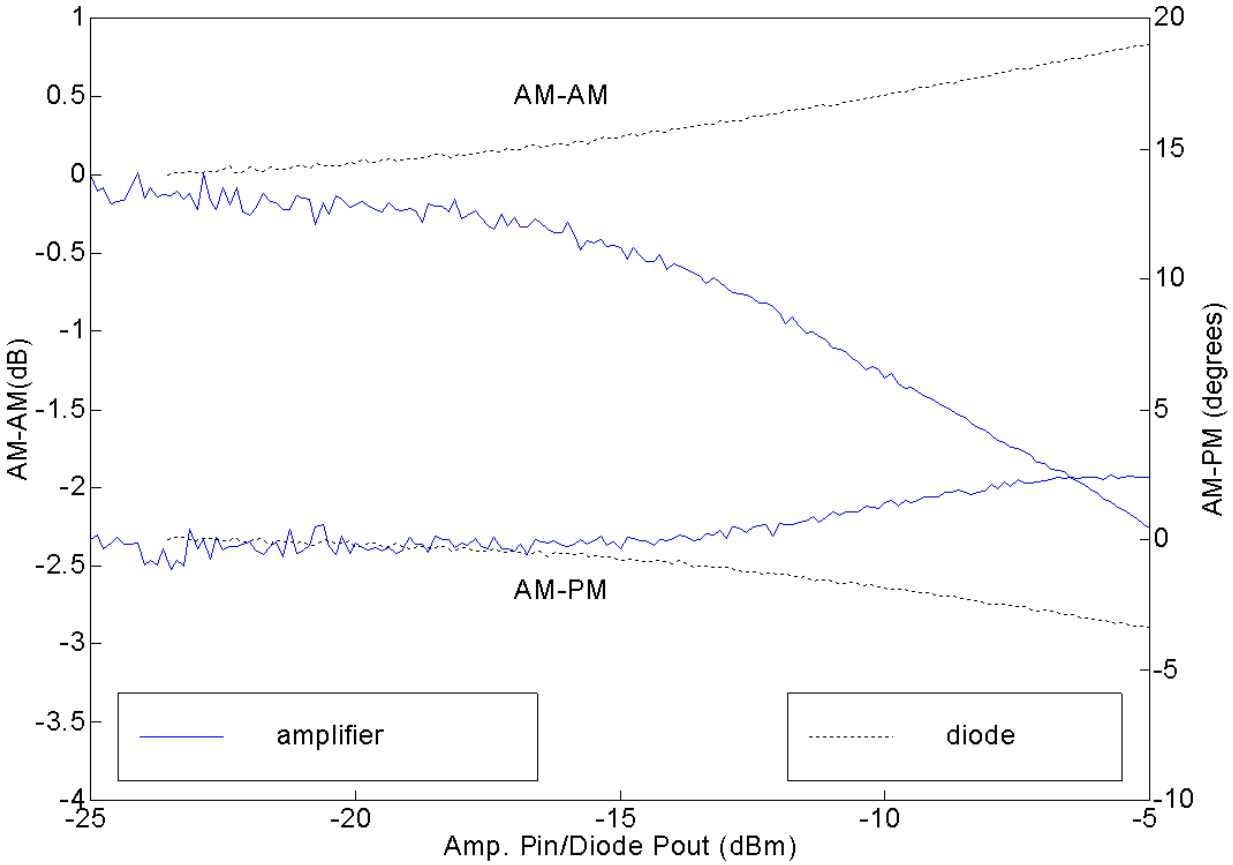


Figure 4.6 PA and 240µm diode (biased at 1.25V) AM-AM and AM-PM at 1.95 GHz

4.4 Diode Choice to Match PA

Based on the measured HBT diode data, a 240µm^2 diode biased at 1.25V should provide the necessary compensation for the target PA with an input small-signal RL of ~12dB and IL of ~3.5dB. Figure 4.6 shows the PA and 240µm^2 diode (biased at 1.25V) AM-AM and AM-PM curves. The curves show the possibility for ~0.8dB AM-AM reduction and ~2.5 degrees of AM-PM reduction. In addition, the potential for improved AM-AM reduction compared to the MESFET case should be noted - since the AM-AM curve is "softer", it easier to correct for. The diode and PA test PCBs were then cascaded together to form the linearized PA. The same measurement setup and procedures as discussed in Section 3.5 were used.

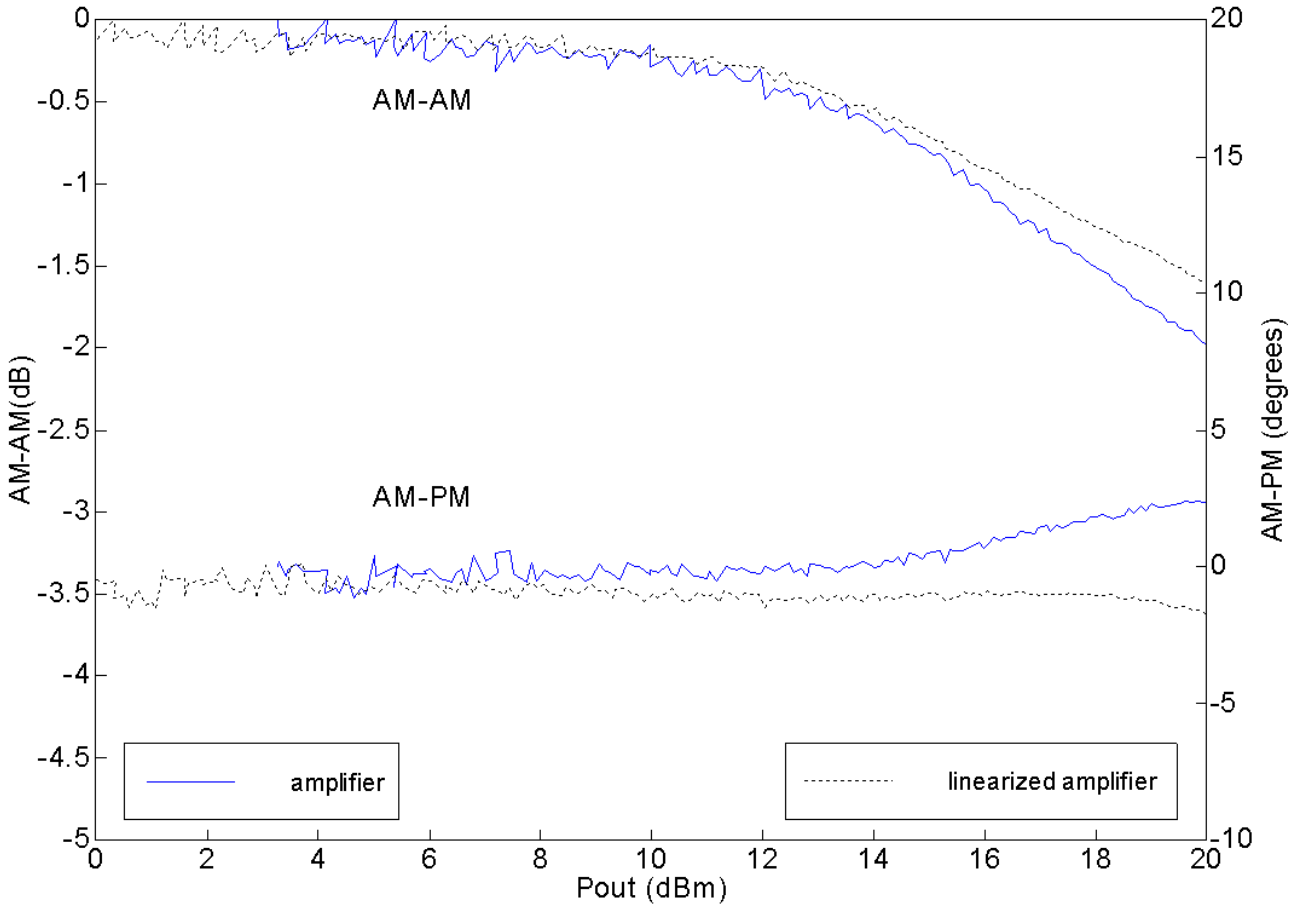


Figure 4.7 AM-AM and AM-PM results of linearized and standalone PA at 1.95 GHz

Figure 4.7 shows the results of the cascaded HBT diode and PA. A clear reduction in AM-AM and AM-PM can be seen in this figure; this diode linearizer operates as expected. Roughly 2.5 degrees of AM-PM compensation and 0.4 dB of AM-AM compensation were obtained in this power range with the linearizer.

4.5 ACPR Results

For the linearized HBT PA discussed above, ACPR measurements were performed as described in Section 3.6. ACPR was measured for some common types of complex digital modulation with different PTARs for an average PA output power of +15 dBm. The results are summarized in Table 4.1 and example plots from the spectrum analyzer for

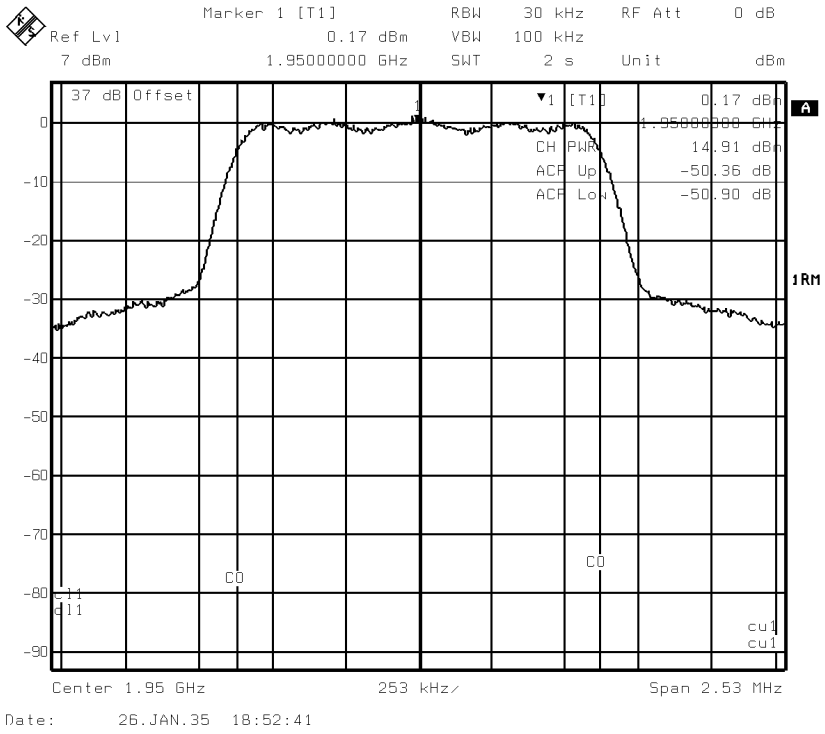
Table 4.1 ACPR improvement due to linearizer for various modulation and PTAR

Modulation	PTAR (dB)	ΔUACPR (dB)	ΔLACPR (dB)
QPSK	6.84	0.2	2.9
OQPSK	5.49	0.1	3.1
Pi/4 DQPSK	6.14	0.0	2.9
16 QAM	9.37	0.0	3.0
256 QAM	11.05	0.0	3.0

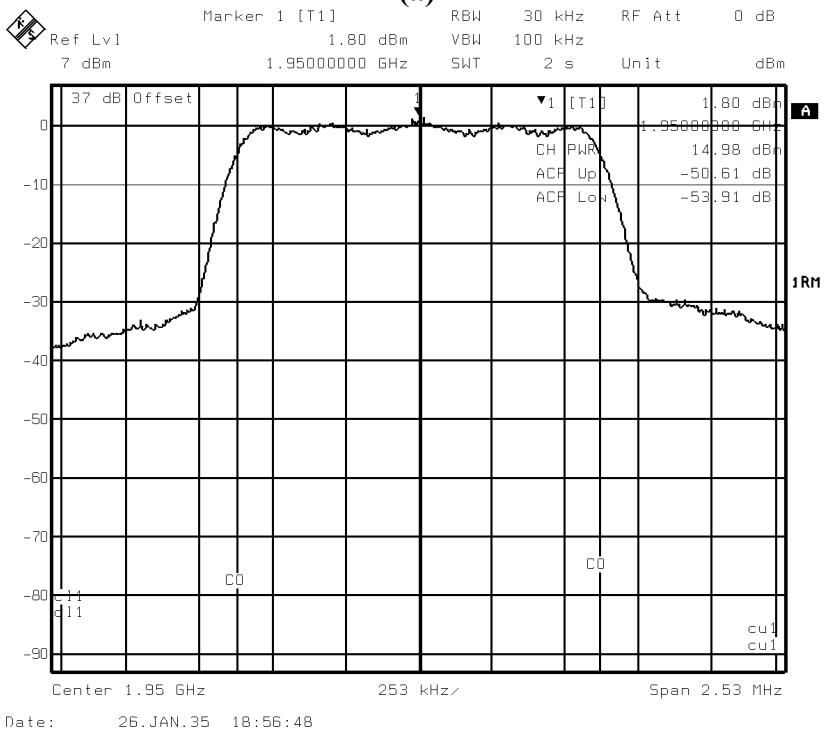
OQPSK are included in Figure 4.8. ΔUACPR/ΔLACPR is the upper/lower channel ACPR *improvement* due to the linearizer.

The baseband filtering used was the IS-95 specified filter for a CDMA mobile station. ACPR was measured in a 30 kHz channel, 1.25 MHz away from f_c for a 1.25 MHz chip rate. These results are similar to the MESFET linearizer results in Chapter 3; however, the HBT linearizer exhibits less improvement since the HBT PA is more linear than the MESFET PA to begin with. The standalone HBT PA exhibits ~1 degree of AM-PM at it's 1dB compression point, while the standalone MESFET PA exhibits ~5 degrees at it's own 1dB compression point. In addition, an asymmetry in the ACPR improvement still exists; however the sidelobe that shows improvement in the HBT case is opposite to that in the MESFET case. This is most likely due a difference in the phase term discussed earlier, which exists due to the separate device mechanisms that generate AM-AM and AM-PM. These results show that this HBT linearizer operates as expected, and is similar in operation to the MESFET linearizer.

The ACPR improvement versus *power* was also measured. Since the ACPR is created through distortion of a signal's envelope as it drives into the PA compression region, the drive level or power output of the PA should affect the amount of improvement due to the linearizer. To test this idea, an OQPSK signal was used to drive the HBT PA. Its power level was varied to achieve +4 to +20 dBm output from the PA. A plot of the ACPR improvement due to the linearizer versus output power is shown in Figure 4.9. From this



(a)



(b)

Figure 4.8 Spectrum plots for filtered OQPSK modulation at output of (a) standalone PA (b) linearized PA

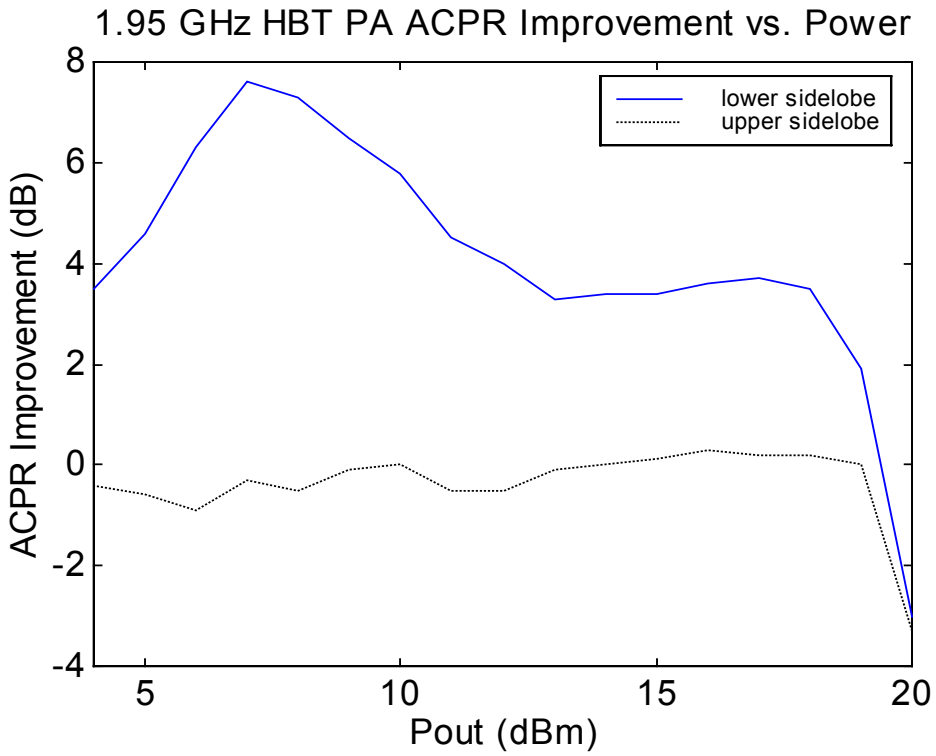


Figure 4.9 ACPR improvement due to linearizer versus PA output power with OQPSK

plot, one can see that there is an optimum power level at about +7 dBm output for optimum linearization. This power level is dependent on the PTAR of the signal as well as the AM-AM and AM-PM characteristics of the PA. For this case, a +7 dBm average power output results in roughly a 12.5 dBm PEP. Figure 4.7 in Section 4.4 shows very little AM-AM or AM-PM distortion at this output level. This power level appears to be just before gain compression, which is the ideal operating point for this type of linearizer.

As the signal is backed-off further or driven harder from this ideal operating point, the improvement due to the linearizer degrades. At low power levels, the linearizer has no effect other than the additional IL that it presents. At higher power levels, the linearizer improvement degrades and ultimately results in worse ACPR than the standalone PA.

4.6 Conclusions

In conclusion, a 1.95 GHz HBT PA was successfully linearized using a series diode predistorter; AM-AM and AM-PM compensation was achieved using minimal additional

circuitry. An improvement in ACPR was measured for modulation schemes with varying PTARs. Results similar to the MESFET linearizer study in Chapter 3 were achieved. Similar asymmetries exist in both cases in the power spectrum. The HBT case exhibited much more AM-AM improvement due to the linearizer compared to that of the MESFET case. This was possible due to the "softer" AM-AM curve of the HBT PA. This however, did not correct for the asymmetry problem as previously discussed. Overall, the HBT PA ACPR improvement was less than that of the MESFET PA for the initial chosen output power level of +15 dBm. This could be partly due the fact that the HBT PA exhibited improved phase linearity over the MESFET PA at each of their respective 1dB compression points. In addition, an ACPR measurement over a swept power range for the HBT PA showed that an optimum output power level exists for optimum linearization; this optimum power level was just before the PA started to exhibit compression. Thus, since the HBT and MESFET PA compression characteristics are different, they may exhibit different optimum output power levels for optimum linearization.

The next chapter will extend the above results to the design of a fully integrated HBT-based diode predistorter and PA RFIC chip.

5 An Integrated HBT Diode Predistorter

In the previous chapters the series diode predistorter concept has been demonstrated in both MESFET and HBT processes. The next step is to implement a fully integrated linearized PA RFIC or MMIC chip consisting of a single die with both the diode predistorter and PA circuits. The ability to accurately simulate the diode and the PA is necessary for proper design of the PA RFIC chip. This limits the design presented here to the HBT process of Chapter 4 since it was shown in Section 3.3 that the available MESFET models for the process were insufficient for use in large signal diode simulations. Section 4.2 showed that the HBT Gummel Poon model would be sufficient for this simulation.

An HBT PA designed at ITT GaAsTEK is used as the starting point for the linearized PA design. This PA is intended for operation around 1.95 GHz using various multilevel digital modulation formats as previously discussed. Specifically, CDMA and WCDMA applications are of particular interest; basic QPSK with a 1.25 MHz chip rate will be used as an initial basis for testing.

5.1 Design Procedure

In order to start the design process the AM-AM and AM-PM characteristics must be known. The aforementioned ITT GaAsTEK HBT PA design was simulated at 1.95 GHz in HP EEsof Libra using a swept input power (-30 to +10 dBm) as was previously performed experimentally. The results are shown in Figure 5.1. These results show the expected AM-AM and AM-PM characteristics that must be compensated for based on the results in Chapters 3 and 4. The soft gain compression characteristic potentially allows for improved AM-AM correction. The nearly 12 degrees of AM-PM shows a need for a large phase correction.

The previous linearizer studies in this thesis examined optimizing the diode predistorter for a 50Ω system. However, the on-chip input impedance of the PA is not 50Ω; these PAs are

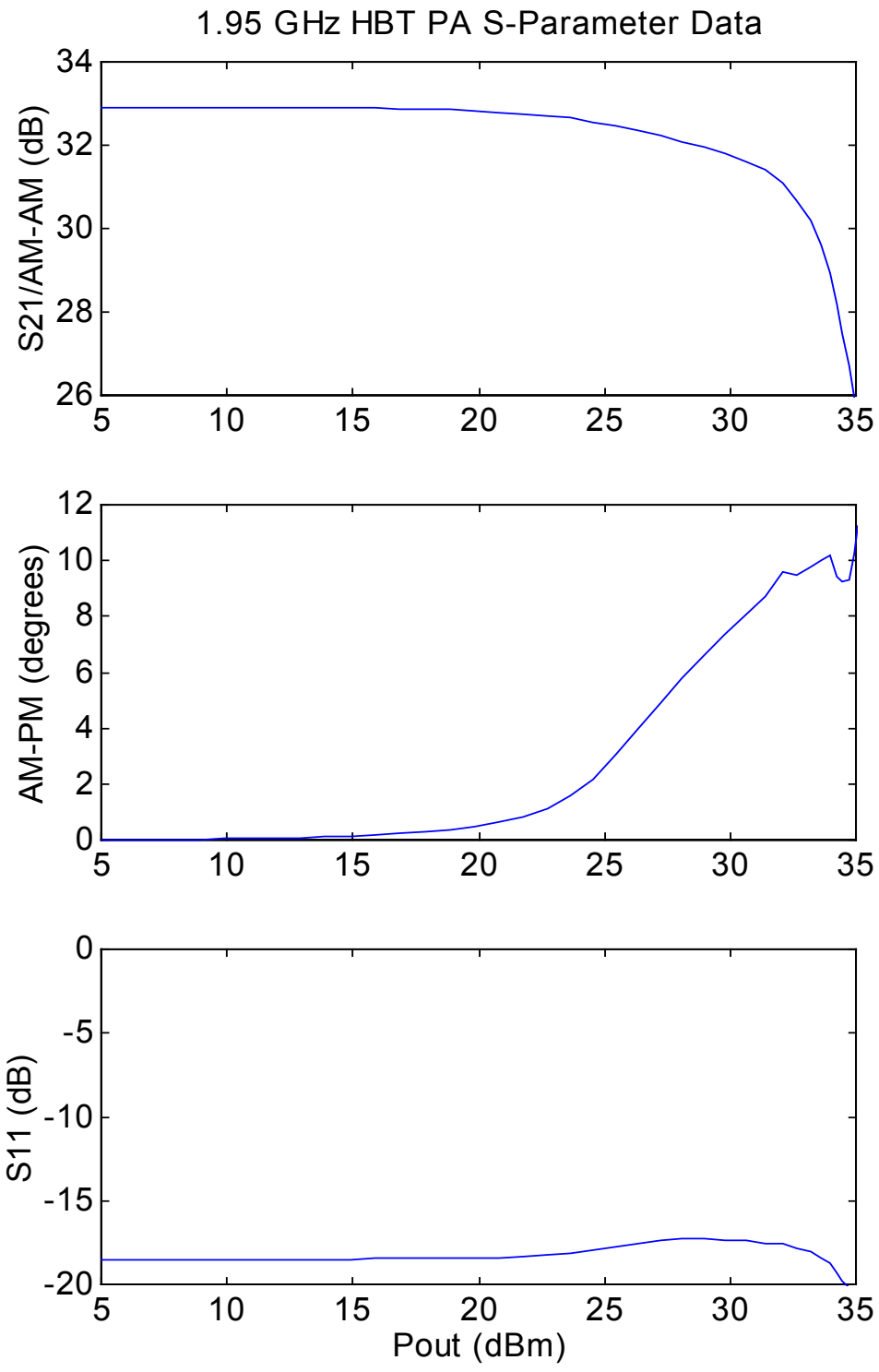


Figure 5.1 1.95 GHz HBT PA simulated S-parameter data versus output power

externally impedance matched. If on-chip PA matching were used, as could be done at microwave frequencies, the diode predistorter could be easily placed at the input of the matching network where a near-50Ω impedance would exist. However, in this case, to reduce the number of off-chip transitions for biasing and matching, the diode predistorter should be placed *following* the off-chip matching network, at the on-chip input of the PA. This requires a somewhat different design procedure, which will be discussed in the remainder of this section.

The next step is to simulate the PA without the input matching components in order to examine the actual input impedance. These simulation results are shown in Figure 5.2. From these results, a very similar AM-PM characteristic to the matched PA can be seen. On the other hand, the amount of AM-AM present differs since the significant loss at the input due to mismatch reduces the saturating effect of the PA. An input RL of ~2 dB is seen, as well as a ~3.5 dB reduction in gain. An inspection of the input impedance on a Smith chart (Figure 5.3) shows ~6.1-j16.1Ω, which remains nearly constant over this input power range of –30 to +10 dBm.

This low input impedance means that the 50Ω optimized diode cannot be used for the on-chip PA predistorter. A diode optimized for 6Ω is required. However, the 50Ω optimized diode was used as a starting point for the on-chip predistorter design. Biasing the diode at a higher forward voltage reduces its resistance, bringing it closer to the required 6Ω. If sufficient AM-AM and AM-PM can be obtained with this size diode at the higher bias, then the diode can be placed directly at the PA input and the overall circuit can be matched for optimum RL using off-chip matching components as before. The results in Chapter 4 showed that a 240μm^2 diode biased at 1.25V presents an input impedance of approximately 50Ω (at 1.95 GHz) while offering a moderate amount of AM-AM and AM-PM compensation; this size diode and bias was used as a starting point and placed in the schematic directly at the unmatched PA input (Figure 5.4). The necessary off-chip biasing chokes and DC blocking capacitors for the diode predistorter were also added into the schematic. The PA and diode (biased at 1.25V) with no input matching was simulated and the large-signal S-parameters were obtained. The input was then roughly matched to 50Ω

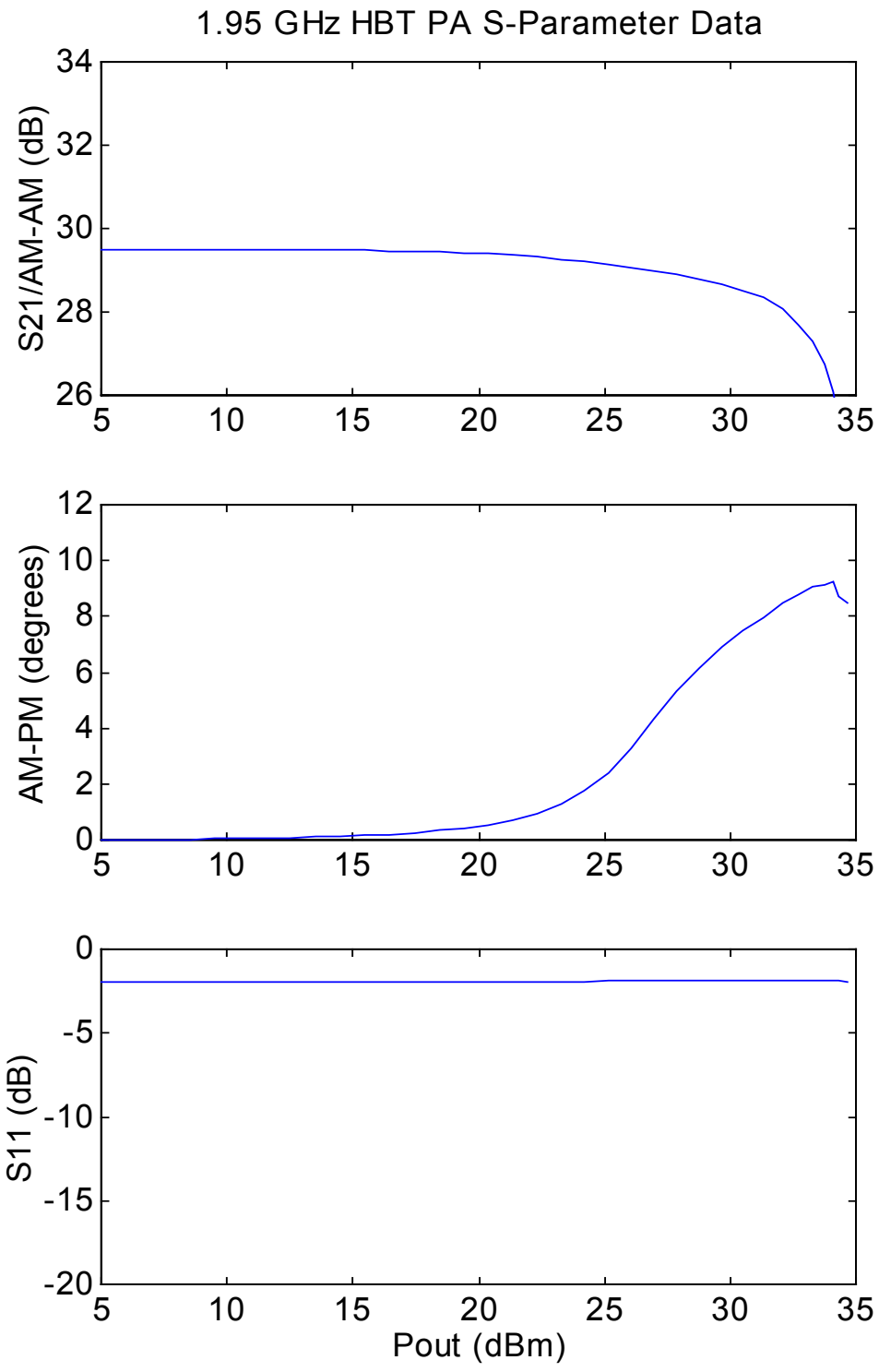


Figure 5.2 Input impedance unmatched - 1.95 GHz HBT PA simulated S-parameter data versus output power

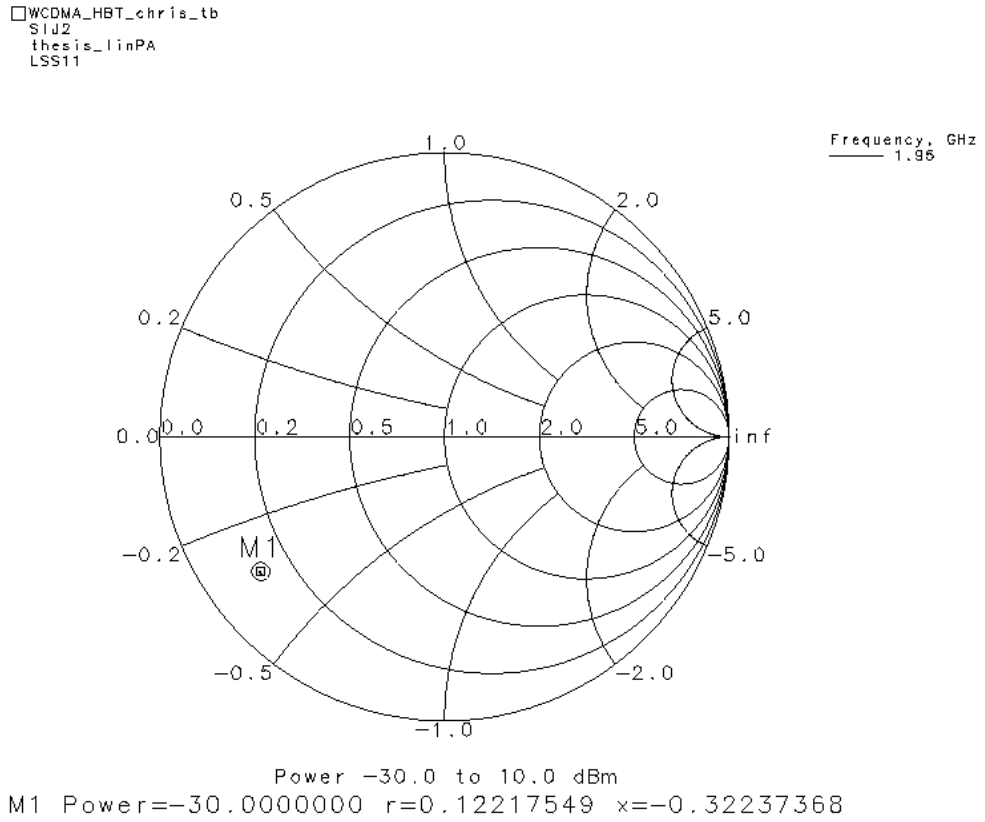


Figure 5.3 Input impedance unmatched - 1.95 GHz PA simulated input impedance Smith chart

using an L-C impedance matching network. The resulting circuit was simulated again and the large-signal S-parameters obtained. From the resulting plots (Figures 5.5 and 5.6), one can see that there is a large amount of IL as well as a large amount of AM-AM resulting from the incorporation of the diode biased at 1.25V. In addition, the AM-PM of the diode overcompensates the AM-PM of the PA. At higher input drive levels, the RL is good (better than 10 dB), indicating a reasonably good match. The cause of the problem of excessive amounts of AM-AM and AM-PM correction is due to the fact that the diode biased at 1.25V is optimum for a 50Ω system at 1.95 GHz (Chapter 4), while the PA input where the diode was placed is approximately 6Ω. This can be seen in the large variation in S_{11} on the Smith Chart versus input power (Figure 5.6). Since the diode resistance is much higher than 6Ω, any variation in it versus input power will have a stronger effect on the circuit compared to if the diode was optimized for 6Ω. The variation in the input impedance versus input drive level needs to be reduced.

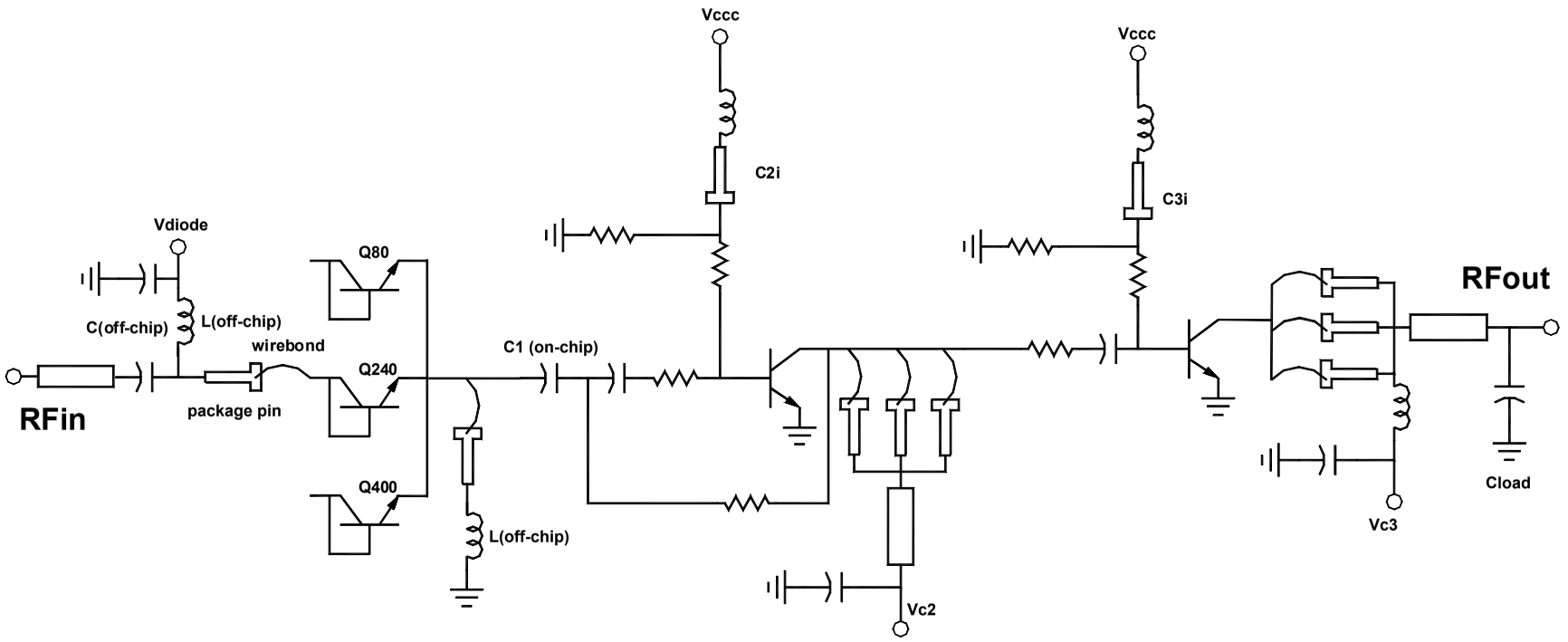


Figure 5.4 Schematic for diode linearized 1.95 GHz HBT PA (Standalone PA design property of GaAsTEK)

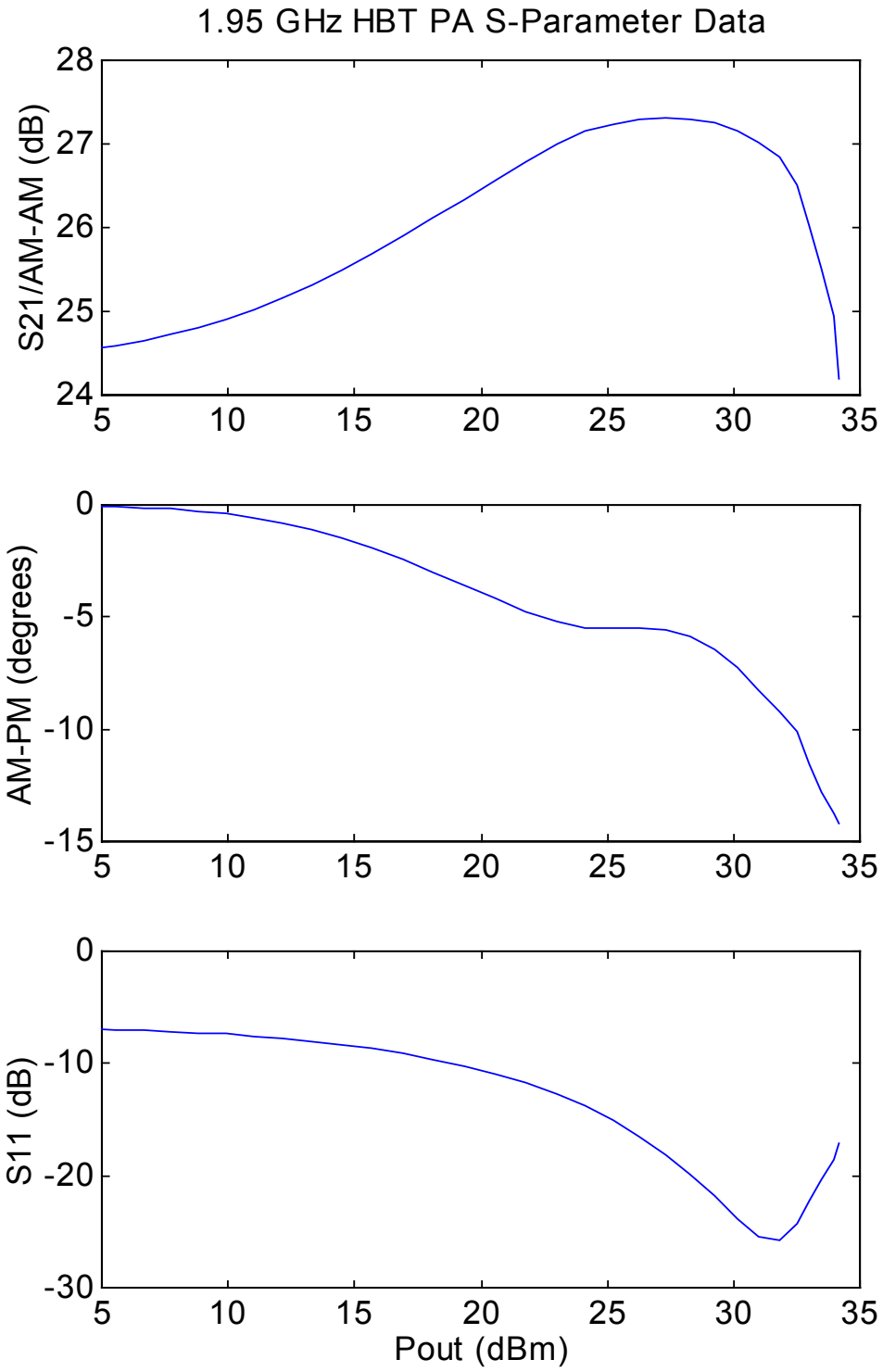


Figure 5.5 Input impedance matched - 1.95 GHz HBT PA cascaded with 240μm^2 diode predistorter (biased at 1.25V) simulated S-parameter data versus output power

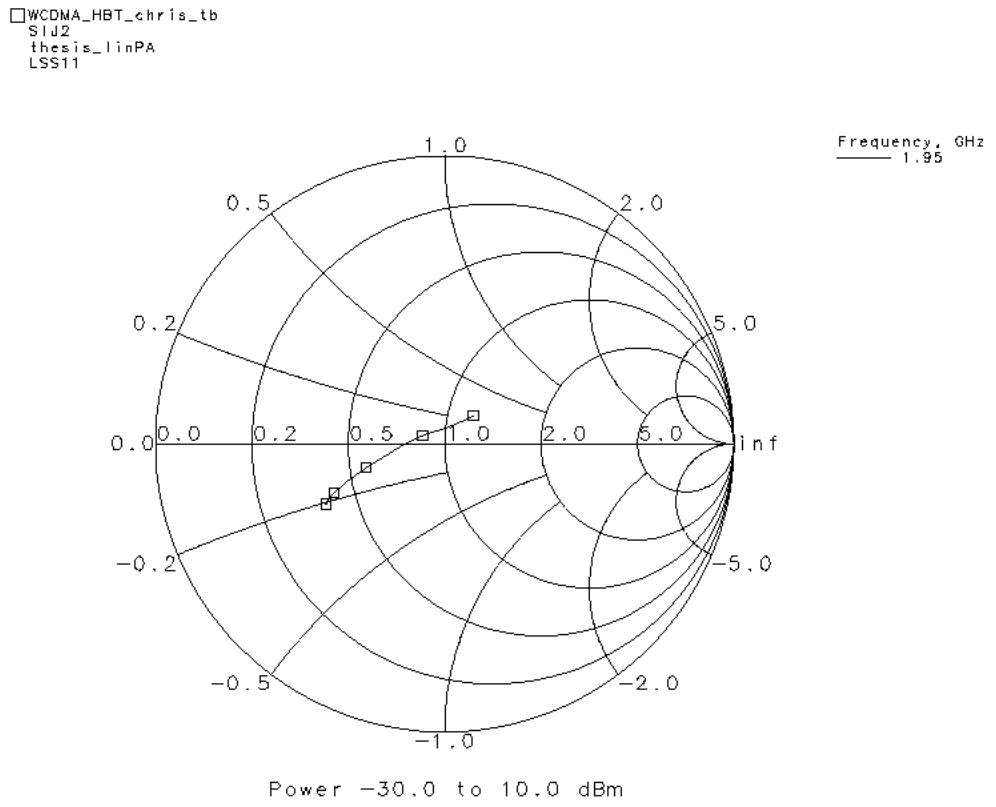


Figure 5.6 Input impedance matched - 1.95 GHz HBT PA cascaded with 240μm^2 diode predistorter (biased at 1.25V) simulated input impedance Smith chart

As discussed above, biasing the diode at a voltage slightly higher than 1.25V will lower it's resistance and improve its match to the PA input impedance. In the equivalent RC network of this series diode predistorter, the R and C values together result in a certain AM-AM and AM-PM characteristic. More or less AM-AM and AM-PM will result if either R or C is tuned. Thus, biasing this diode higher to lower its R closer to 6Ω should result in a reduced AM-AM and AM-PM characteristic compared to that shown in Figure 5.5, where the diode predistorter overcompensates. AM-AM, AM-PM, and RL simulations were conducted while slowly increasing the diode bias. For a diode bias of 1.29V, an optimum solution was achieved. The results are shown in Figures 5.7 and 5.8.

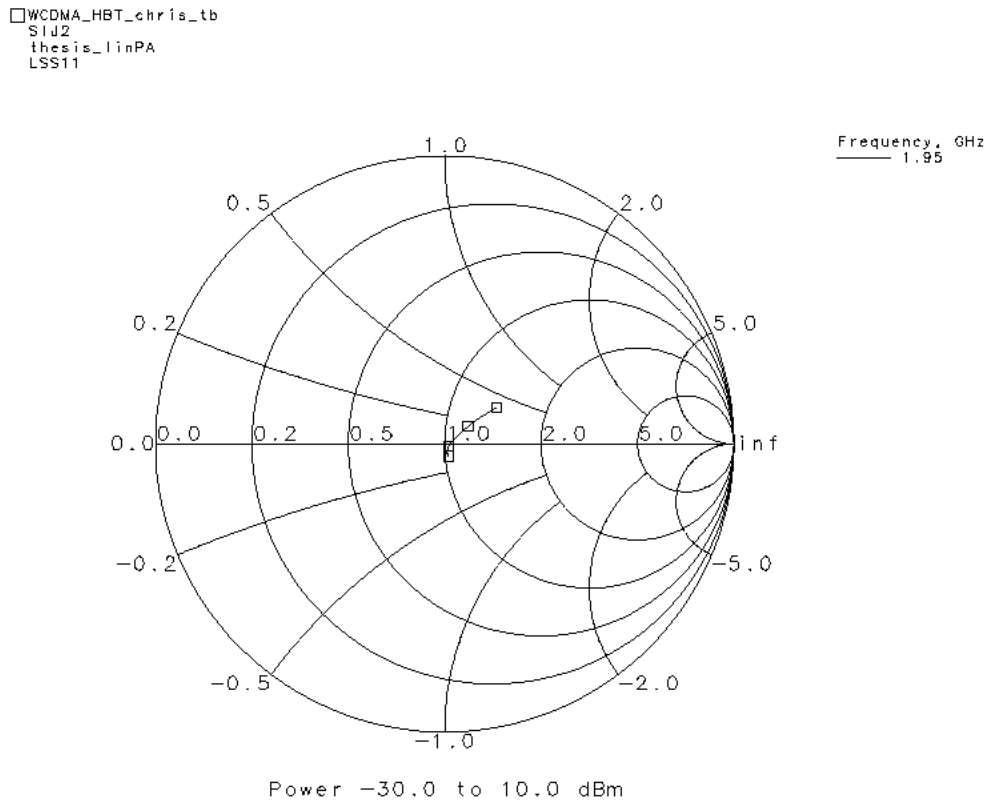


Figure 5.7 Input impedance matched - 1.95 GHz HBT PA cascaded with 240μm^2 diode predistorter (biased at 1.29V) simulated input impedance Smith chart

Increasing the diode bias to reduce its resistance is clearly the answer. S_{11} on the Smith chart (Figure 5.7) shows much less variation versus input power. Figure 5.8 shows a clear AM-AM and AM-PM improvement as well as an improved input match. Figure 5.9 shows these results along with the original PA characteristics for comparison. A ~2 dB improvement in the 1 dB compression point and a ~5 degree reduction in AM-PM is the result of this diode predistorter. The next section will investigate potential ACPR improvements with this configuration.

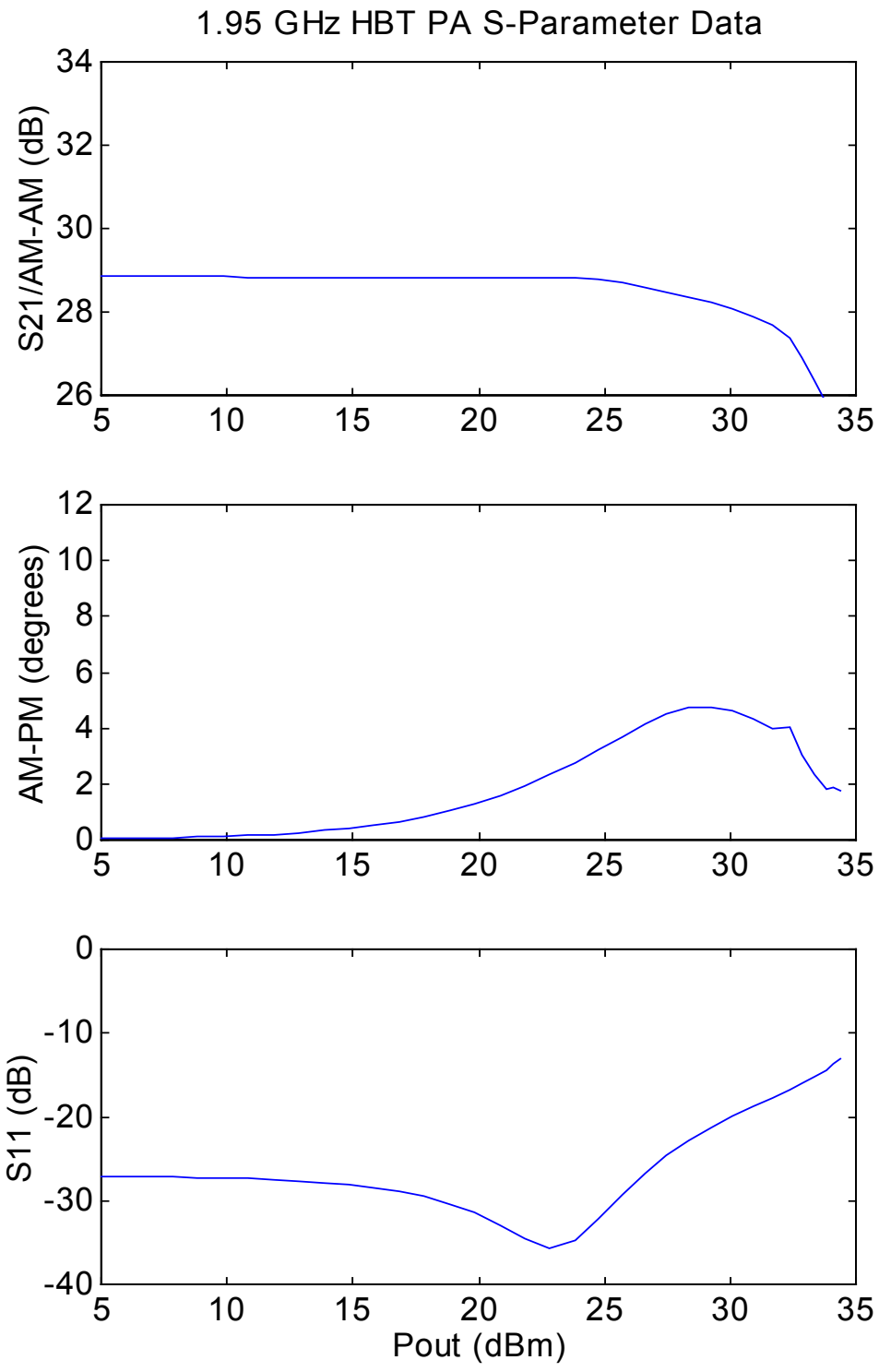


Figure 5.8 Input impedance matched - 1.95 GHz HBT PA cascaded with 240μm^2 diode predistorter (biased at 1.29V) simulated S-parameter data versus output power

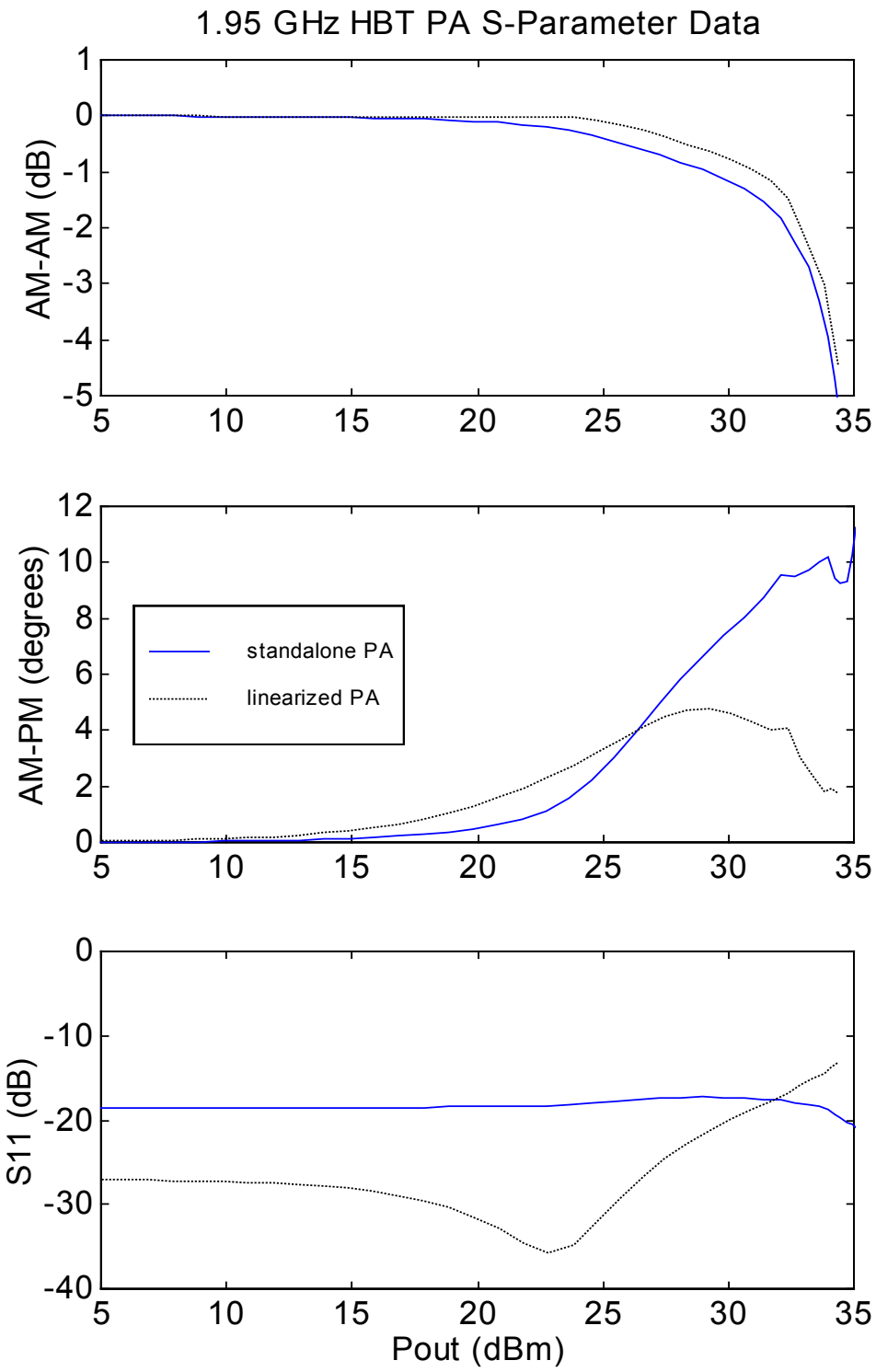


Figure 5.9 Simulated AM-AM and AM-PM results of linearized and standalone PA for a diode bias of 1.29V

5.2 ACPR Simulation and Results

In order to simulate the ACPR of this PA, additional processing was required. The large-signal S-parameters from the simulations in Section 5.1 were exported to data files from HP EEsof Libra. These files contain all of the necessary information to perform a rough envelope analysis for the standalone and linearized PAs. Next, an IS-95 test bench in HP EEsof Omnisys was created for this application. This test bench generates a 1.95 GHz CDMA signal with QPSK modulation and a 1.25 MHz chip rate from a random data stream. The resulting signal drives the DUT, which is represented by the two-port large-signal S-parameter file previously generated in Libra. The output power spectrum is generated and displayed in a format similar to a spectrum analyzer. The signal drive level to the PA input is adjusted in both cases to achieve +23 dBm output power. This is necessary due to the additional IL introduced by the diode. This power level was chosen since it would set the average signal power just prior to where the PA starts to exhibit compression. The envelope will then further drive the PA into compression. As discussed in the previous chapters, this drive level is where the series diode predistorter is most effective.

The resulting power spectra for the standalone and linearized PAs are shown in Figure 5.10. A clear improvement in ACPR can be seen in the linearized PA case. It is interesting to note that the improvement is lost beyond a certain frequency offset from the main 1.25 MHz channel. Therefore, one must consider the specified method of measuring ACPR for a particular communications system when weighing the advantages of this type of predistorter. This resulting power spectrum data is exported to a spreadsheet for ACPR analysis[1]. In the spreadsheet, the logarithmic power values are converted into linear power. Numerical integration (Simpson's Rule) is used to determine the total power in a specified bandwidth. The power in the main 1.25 MHz channel and the power in the upper and lower 30 kHz channels 1.25 MHz away from the main channel edge are calculated in accordance with the IS-95 ACPR specification. The results of these calculations show a

[1] HP EEsof Omnisys does not currently have a feature for measuring power in a specified bandwidth.

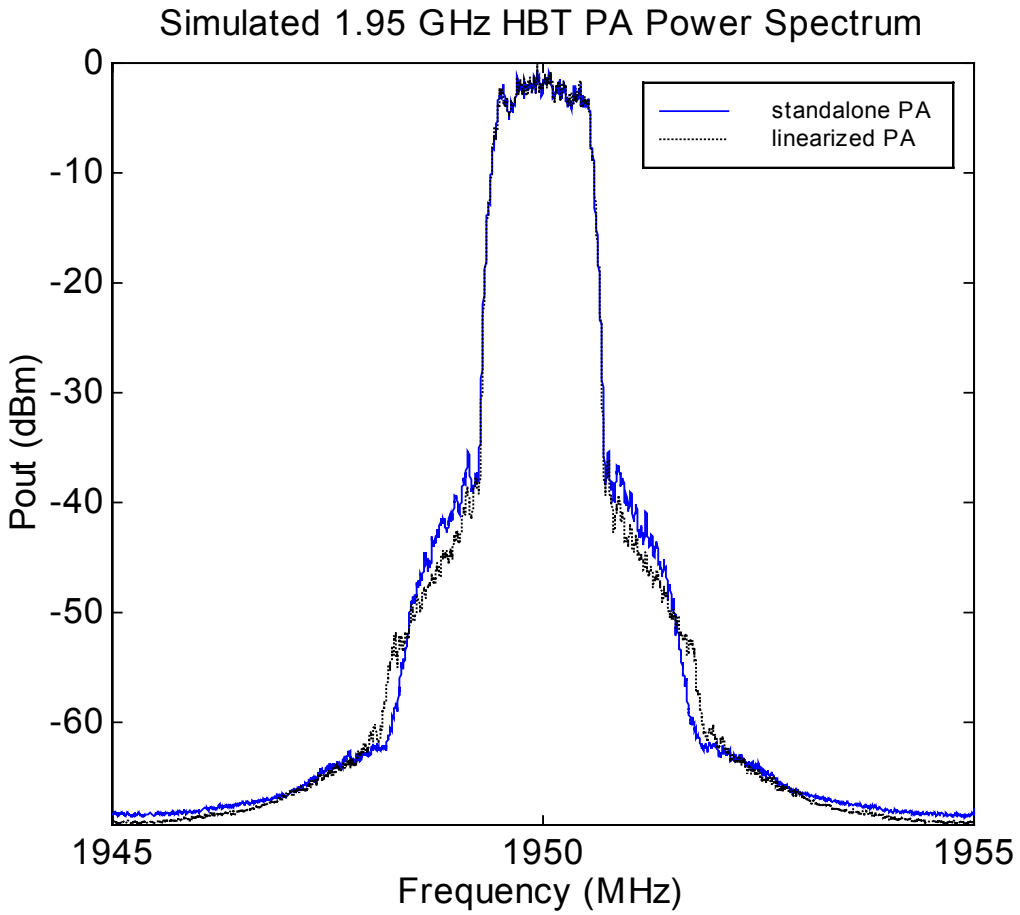


Figure 5.10 Linearized (diode biased at 1.29V) and standalone 1.95 GHz HBT PA peak power spectrum simulated in HP EEsof

lower channel ACPR improvement of 2.9 dB and an upper channel ACPR improvement of 3.0 dB. Note that no asymmetry exists in this simulated spectrum. The lack of asymmetry suggests that the simple envelope analysis presented here does not account for an important factor in the nonlinear analysis. One cause of this discrepancy could be that the envelope analysis used here utilizes only one tone to gather the AM-AM and AM-PM data, while the CDMA signal used to simulate ACPR consists of many tones. In addition, Chapter 3 discussed the possibility that different device mechanisms cause AM-AM and AM-PM and that these two nonlinearities may actually have a phase difference between the distortions that generate them; the envelope analysis discussed here does not account for this phase difference. In the event that this is the cause of asymmetry, a more accurate

characterization of the DUT would be required. This characterization would have to account for the phase difference between the individual nonlinearities; the information in a two-port S-Parameter file does not contain this potential phase difference. Thus, a new nonlinear model would have to be created to incorporate this additional phase factor. No ACPR simulation techniques have been found in the literature to date that account for this phase difference.

5.3 RFIC Die Layout

Based on the integrated linearized HBT PA design, a die layout for fabrication of the PA was completed. The existing design rule checked (DRC) HBT PA die layout was used as a basis and the diode linearizer added to the layout (Figure 5.11). 80μm^2 and 400μm^2 diodes were included in addition to the 240μm^2 diode for tuning flexibility. The individual diodes, or combinations of diodes, may be wirebonded into the circuit. Off-chip RF chokes and matching components are necessary and would be included on a evaluation PCB.

The fabricated die would be epoxied into a plastic package and wirebonded to the necessary pins. Figure 5.12 shows the wirebonding diagram for this configuration. Here the 240μm^2 diode is shown wirebonded in, and the other diode sizes are left unconnected. Notice the three diodes in the upper left hand corner of the die. The outputs of these diodes connect directly to the input DC blocking capacitor at the PA input. A bond pad at this connection is provided for the diode choke to ground, which is required to properly bias the diode predistorter. A test PCB was also designed to accommodate the RFIC, off-chip RF chokes, matching components, and biasing. This PCB will facilitate future testing of the linearized HBT PA RFIC.

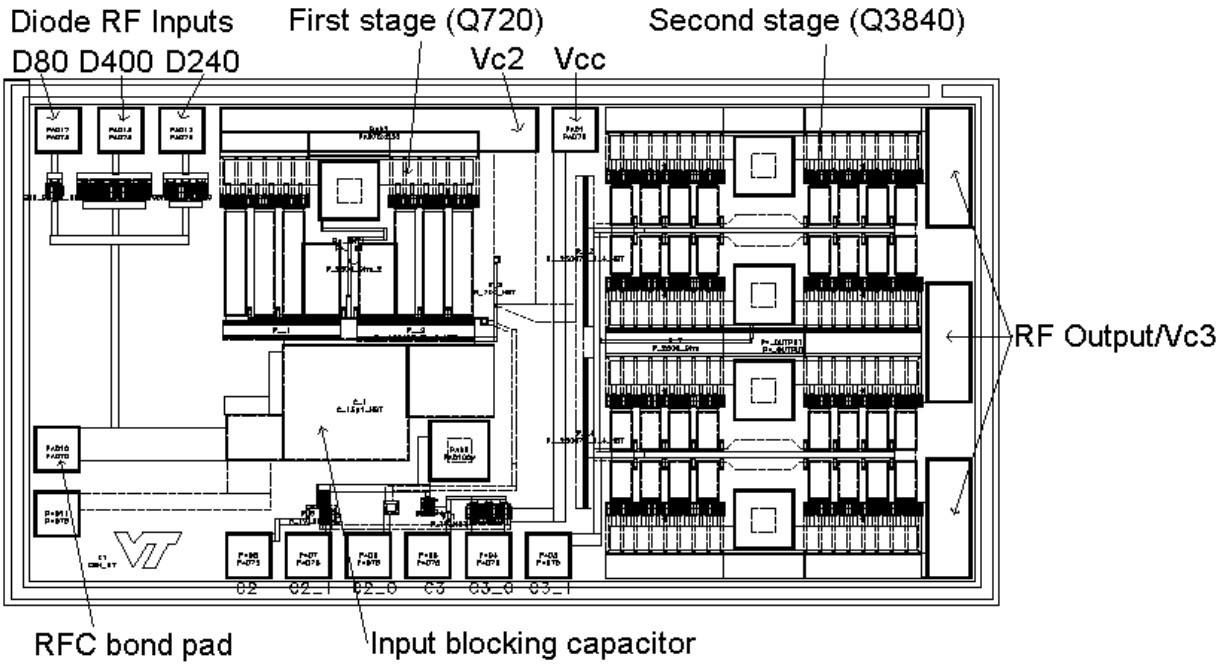


Figure 5.11 Diode linearized PA RFIC die layout (Standalone PA design property of GaAsTEK).

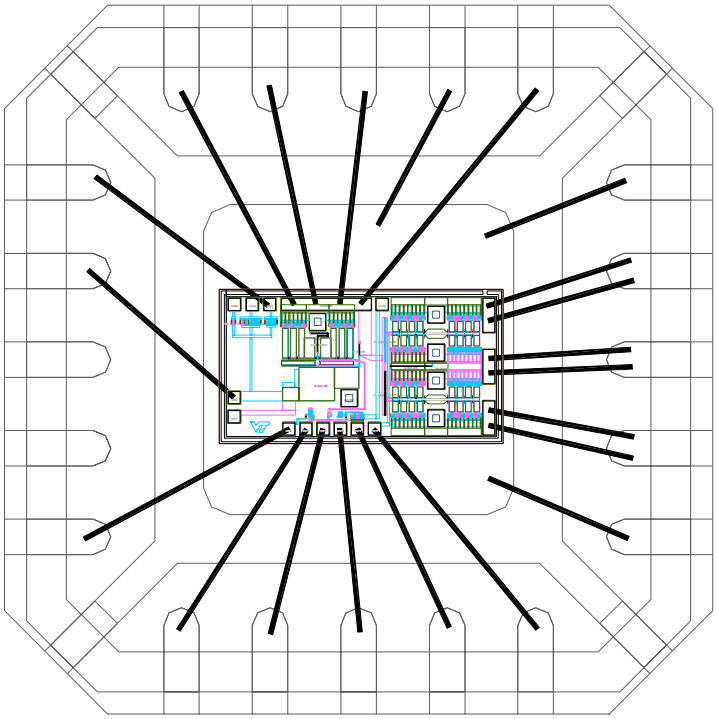


Figure 5.12 Diode linearized PA RFIC die wire bonding diagram.

5.4 Conclusions

In conclusion, a procedure for the design of a fully integrated linearized 1.95 GHz HBT PA RFIC chip has been presented. The results from Chapters 3 and 4 were used as a basis for the design. The design was fully simulated in HP EEsof. It was shown that the 50Ω optimized diode presented in Chapter 4 was insufficient for a PA with off-chip matching components due to the need to reduce off-chip transitions for biasing and matching. As a result, the diode input impedance had to be tuned via its forward bias to closer match the on-chip input impedance of the PA. Using this technique, sufficient AM-AM and AM-PM compensation was obtained. A ~2dB improvement in the 1 dB compression point and a ~5 degree reduction in AM-PM resulted.

The resulting simulated large-signal S-parameter curves were used in HP EEsof Omnisys to simulate their effect on a 1.25 MHz chip rate CDMA signal. The resulting power spectrum for the linearized PA showed a 2.9 dB lower channel and 3.0 dB upper channel ACPR improvement over the standalone PA for a +23 dBm PA output power; this shows the potential of the fully integrated diode predistorter and PA. An interesting result of the technique used here to simulate ACPR is that no asymmetry was observed in the power spectrum. The most likely cause of this is the fact that the phase difference between the device mechanisms that create AM-AM and AM-PM are not accounted for. It is suggested that this phase difference be investigated fully and possibly incorporated into the envelope simulation.

In addition to the simulated results, a die layout was completed for the linearized PA RFIC chip. Supporting wirebonding diagrams for packaging the RFIC were completed as well. At the time of writing this thesis, this is the most up to date data and design work for the fully integrated diode linearized HBT PA. Die fabrication is expected in the near future and actual chip testing would be the next step. It is expected that results similar to the simulations presented in this chapter would be obtained.

6 Conclusions / Future Work

The objective of this thesis was to address the increasing linearity requirements of modern communications systems. The recent trend has been towards the use of portable and handheld devices. These devices must be lightweight and compact; battery capacity and size is a major limitation on the overall size and compactness of a portable or handheld system. As a result, power efficiency is a major factor in reducing overall portable system size.

The RF PA is typically the greatest power sink in a radio system; high efficiency PAs are inherently nonlinear. In contrast, linearity requirements on communications systems are rapidly increasing. In order to increase bandwidth efficiency to accommodate crowding communications channels and increasingly high-bandwidth applications, high-order complex digital modulation schemes are becoming mainstream; to accurately demodulate and decode these modulation schemes with minimum BER, increasingly linear and distortionless designs must be utilized. This poses a tradeoff between bandwidth efficiency and power efficiency. Various linearization techniques may be used to improve the linearity of a high efficiency PA.

6.1 Conclusions

With compact, lightweight, and power efficient devices in mind, analog RF predistortion was chosen as an ideal linearization technique candidate. The series diode predistorter is capable of moderate predistortion with minimal additional circuitry, power consumption, and layout size.

Issues of nonlinearity in communication systems focusing on PAs were discussed. Traditional nonlinearity characterization methods such as two-tone IMD analysis were presented. Envelope analysis was presented as a more modern and useful nonlinearity analysis for digitally modulated PA design.

The primary contribution of this thesis was the design and optimization of series diode predistorters for specific PA designs. A study of a MESFET based diode's S-parameters versus forward bias, size, and RF drive level was performed. Using this data, the diode size and bias were chosen for optimized use in this predistortion application with a particular PA. Maximum return loss, minimum insertion loss, and the correct AM-AM and AM-PM are desired. The AM-AM and AM-PM characteristics of a 2.68 GHz MESFET PA were measured and used in conjunction with 2.68 GHz diode S-parameter data to choose an optimum diode size and bias for optimum reduction in AM-AM and AM-PM of the PA. The results of this "linearized" PA showed an ACPR improvement of up to 6.7 dB due to the reduction in the PA AM-AM and AM-PM. However, an asymmetry in the ACPR improvement was evident - the lower sideband showed a reduced improvement in ACPR compared to the upper sideband. It was suggested that the phase difference between the IMD products due to separate AM-AM and AM-PM device mechanisms is the likely cause. A drawback of this predistorter is the requirement of more drive level to overcome the IL; this must be weighed carefully with efficiency requirements. In addition, the importance of accurately controlling the diode bias in 10mV steps and over temperature is stressed.

The optimization of the diode predistorter was also conducted in HBT technology. Similar results were achieved, with similar ACPR asymmetry. The AM-AM of the HBT PA was easier to correct for due to it's "soft" compression characteristic. However, the target PA's phase linearity was much better than the MESFET PA, allowing for less AM-PM correction. A brief study of ACPR improvement versus PA drive level was performed. It was found that there is an ideal drive level for optimum ACPR improvement. This can be related to the AM-AM and AM-PM curves of the PA as well as the PTAR of the modulated signal. The significance of envelope analysis was evident in this study.

Finally, a fully integrated diode predistorted HBT PA was designed and simulated. The previous cases used a separate predistorter cascaded with the standalone PA as a proof of concept; however, this entailed optimizing the diode for a 50Ω match. This study was aimed at fully integrating the predistorter and PA onto a single RFIC chip, requiring the

predistorter to be optimized for the unmatched PA input impedance. The necessary design, simulations, and IC layout were performed. It was found that biasing the diode at a higher voltage was effective in reducing the diode predistorter impedance to a value closer to that of the on-chip PA input impedance while still maintaining the necessary AM-AM and AM-PM compensation. A ~2 dB improvement in the 1 dB compression point and a ~5 degree reduction in the AM-PM was the result of this simulated on-chip diode predistorter. In addition, simulated ACPR improvements of ~3 dB were found in both the upper and lower adjacent channels. No asymmetry exists, thus the limitations of this method of simulation must be addressed. It was suggested that since different device mechanisms may generate AM-AM and AM-PM, a phase difference might exist between these two distortion mechanisms. The characterization of nonlinearities using an S-parameter file lacks this AM-AM and AM-PM phase difference; this was suggested as the possible cause of the lack of asymmetry in the ACPR simulation.

6.2 Future Work

Future work related to this thesis should first and foremost be the completion of the fully integrated diode predistorted HBT PA effort. Due to delays in having the RFIC fabricated, only simulated results were presented. Further work obviously involves having the RFIC chip fabricated and tested. The testing procedures involved should be similar to those described in this thesis. It is expected that this fully integrated linearized PA will exhibit an improved ACPR performance over a similar standalone PA.

In addition, the optimization of the diode at the device level should be investigated. It was found that the upper frequency of operation of this diode predistorter design is determined by the diode device parasitic capacitance. This capacitance limits the maximum usable frequency (MUF) of the predistorter. To extend the MUF, this parasitic capacitance must be reduced at the device level, which may be accomplished by reducing the anode area or etching semiconductor material from under the anode finger [28].

Finally, the ACPR improvements shown in this thesis were narrowband in nature. The measurements were in accordance with the relevant current wireless systems specifications

such as IS-95. Future specifications currently under development are shifting to a more broadband nature. Wideband CDMA (WCDMA) [29] specifies a 1.25 MHz adjacent channel bandwidth rather than the 30 kHz adjacent channel bandwidth used in this thesis. While this linearizer is expected to be relatively broadband, the AM-AM and AM-PM curves used in the optimization process were generated from a single tone. Thus, the analysis used in this thesis uses a narrowband distortion assumption relative to the carrier frequency. As communications signals become more broadband, this assumption becomes less accurate. Further studies on the broadband capabilities of envelope analysis as well as this diode predistortion linearizer are recommended.

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Vita

Christopher Burke Haskins was born on February 13, 1975 in Baltimore, Maryland. His family later moved to the rural town of Baldwin, just outside of Baltimore, where Chris spent most of his childhood years. After graduating from Loyola High School in 1993, Christopher studied in Virginia Tech's Electrical Engineering program. He received his Bachelor of Science in Electrical Engineering in May of 1997.

Upon completion of his undergraduate studies, Christopher filled the position of Development Engineer with Adaptive Broadband Corporation's SCADA Products Group (formerly California Microwave – Microwave Data Systems) in Rochester, New York. He participated in the design and development of RF and microwave data telemetry point-to-multipoint terrestrial radio systems. In August 1998, Christopher left this job in the pursuit of a graduate degree in Electrical Engineering at Virginia Tech.

The requirements for his Master of Science degree in Electrical Engineering will be met in April of 2000. Upon graduation, Christopher will join the Johns Hopkins University Applied Physics Lab in the Space Science and Engineering Group as an Associate Member of Professional Staff.