VIRGINIA TECH

WSN-1

MICS

Switched Capacitor Power Amplifiers: Powering the Next Generation of Wireless Communication, from RF to mm-Wave

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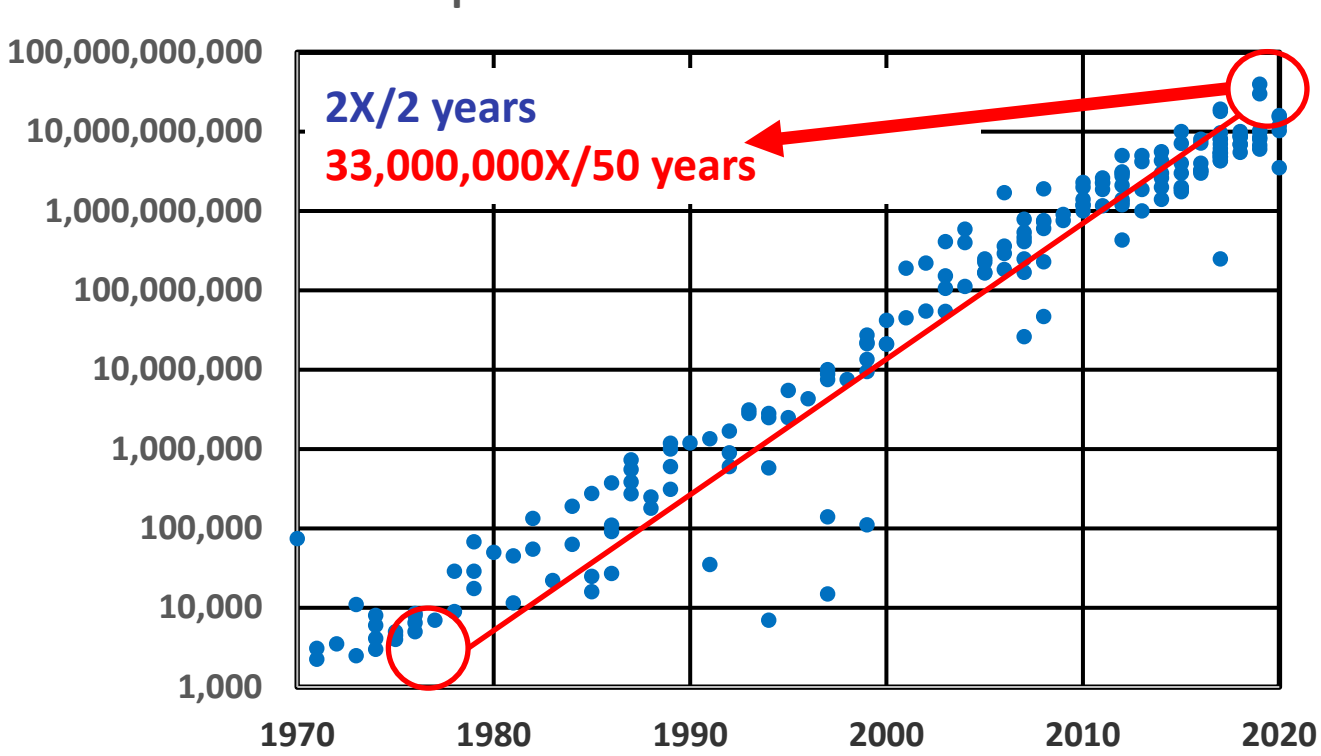
Outline

- **Background and Motivation**
- Switched-Capacitor Power Amplifier (SCPA) Introduction
- Recent Demonstrations of SCPAs
- mmWave SCPAs
  - Frequency multiplying class-D
  - Frequency multiplying SCPA
- Conclusions

CMOS: Economics Over Performance

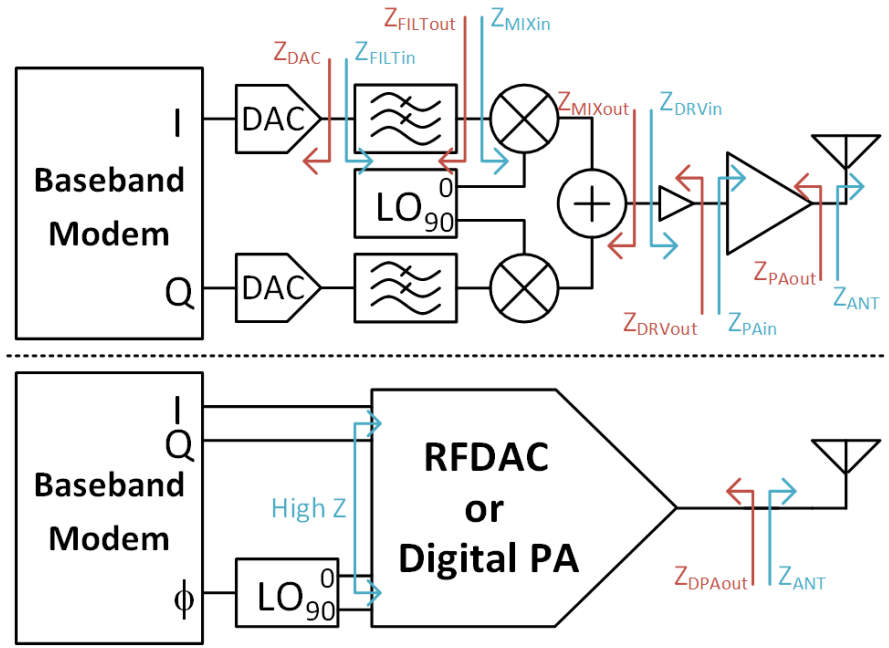
Data source: https://en.wikipedia.org/wiki/Transistor_count



- Scaling CMOS
  - Faster, lower loss switch
  - Reduced intrinsic gain
- Architectural Changes in Analog/RF/Mixed-Signal Circuits
  - More Digital Circuits
  - Fewer Analog Blocks (e.g., Amplifiers)

Goal: Use transistors as switches, or find architectures that do well with reduced precision

Interfaces: Analog vs. Digital PA

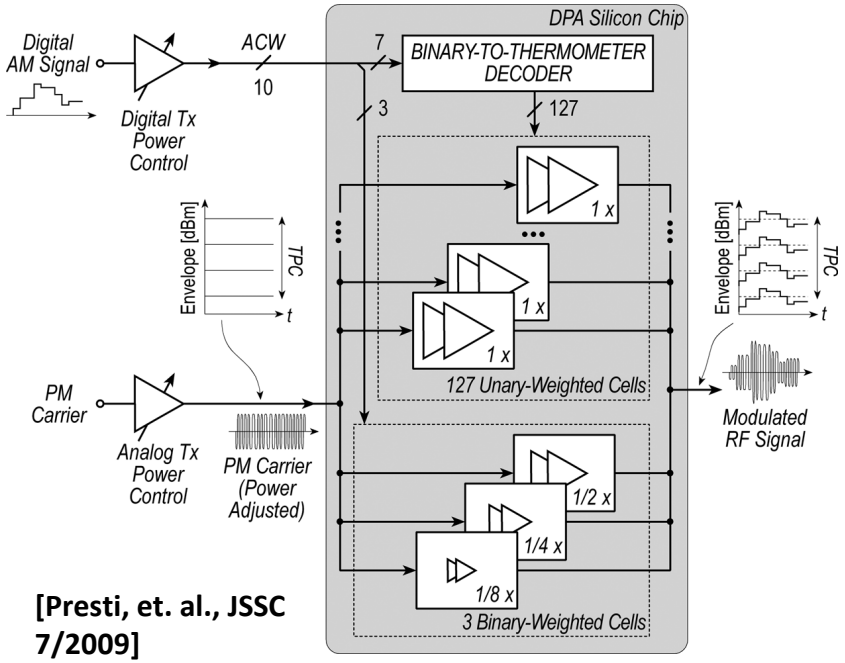


Analog Interfaces at DAC, Filter, Mixer, Driver, PA, Antenna

Switching Interfaces everywhere but DPA-to-Antenna

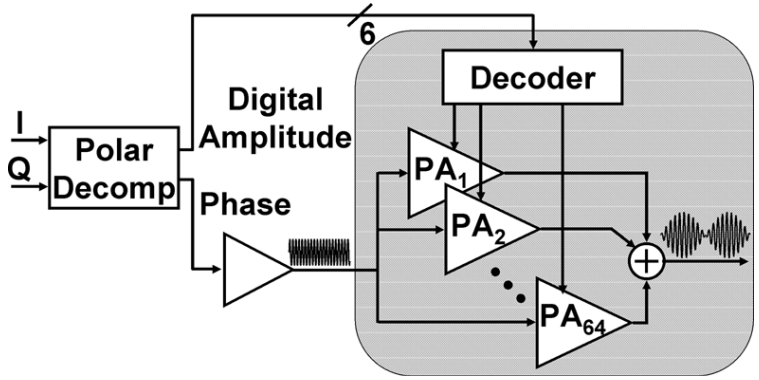
- Conventional TX: impedance, linearity, noise, gain specs at every interface; driven by analog performance
- Digital PA: high-impedance gate interfaces; driven by digital switching performance

What is a Digital PA?



[Presti, et. al., JSSC 7/2009]

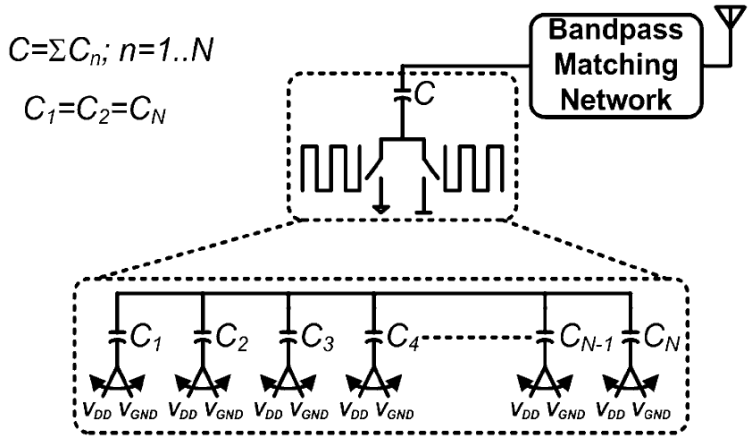
IDPA = Current DPA



[Kavousian, et. al., JSSC 10/2008]

VDPA = Voltage DPA

SCPA = Switched-capacitor PA



[Yoo, et. al., JSSC 12/2011]

- Sometimes called “RF-DAC”, “DPA=Digital PA”
  - A DAC (Converts complex digital-signal to RF-signal)
  - A Mixer (Translates signal from baseband to RF)
  - An Output Stage (PA Predriver or PA)

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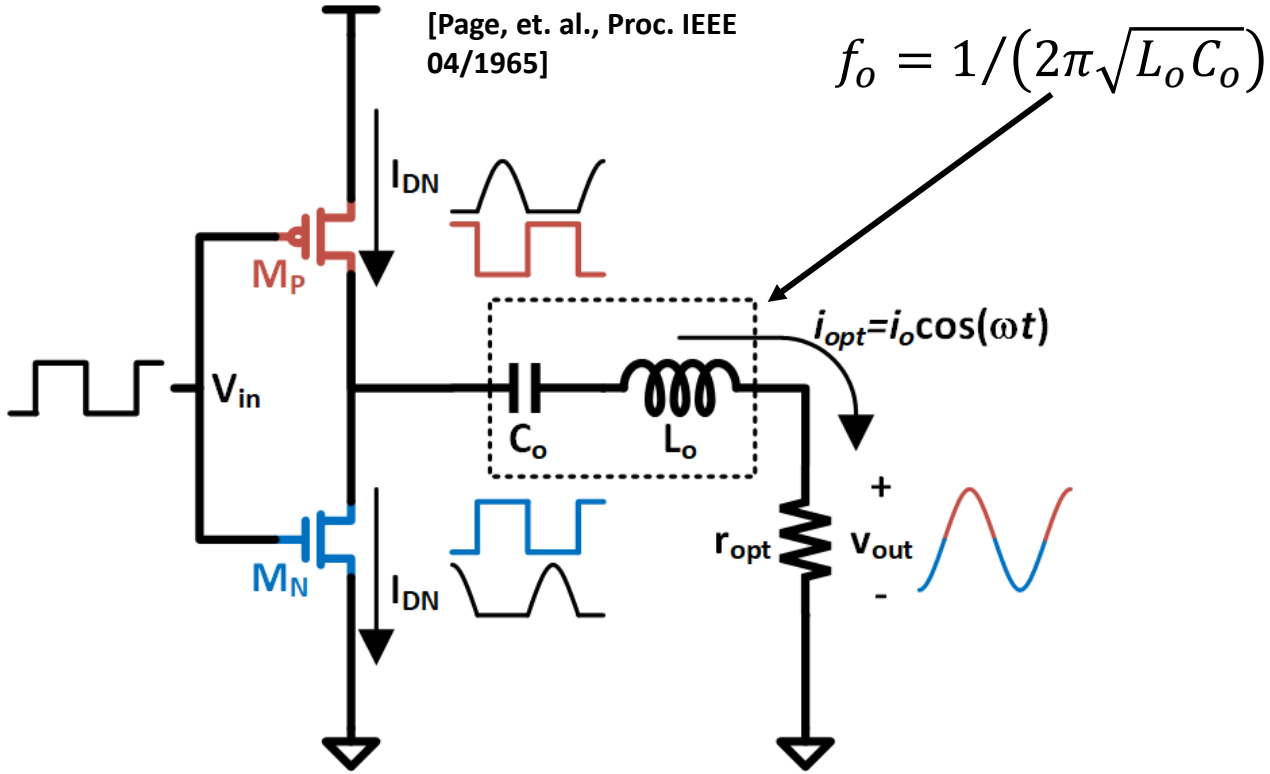
Class-D PA – Ideal CMOS Operation



- Output Power:

$$P_{out} = \frac{2}{\pi^2}\frac{V_{DD}^2}{r_{opt}}$$

- Drain Efficiency:

$$\eta = 100\%$$

- R_{opt}:

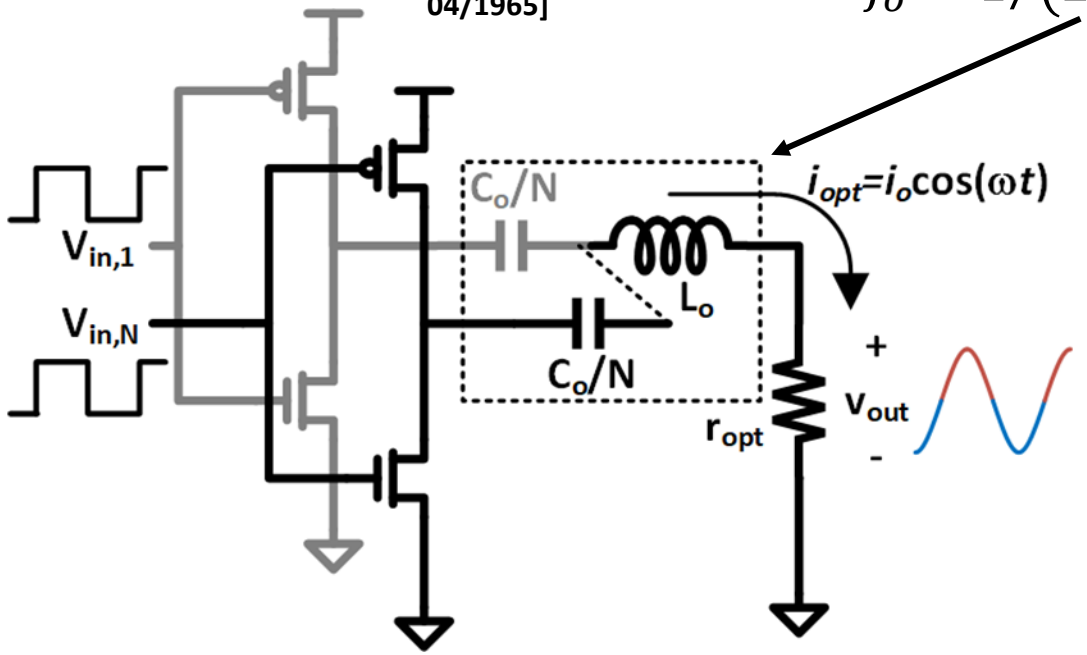
$$r_{opt} = \frac{2}{\pi^2}\frac{V_{DD}^2}{P_{out}}$$

- CMOS Inverter + Series Resonant Filter
- Input is driven with CE pulse train
- Reduces Drain Voltage/Current Overlap → η=100%

“Sliced” Class-D PA

[Page, et. al., Proc. IEEE 04/1965]

$$f_o = 1/\left(2\pi\sqrt{L_o C_o}\right)$$



- Output Power:

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- Drain Efficiency:

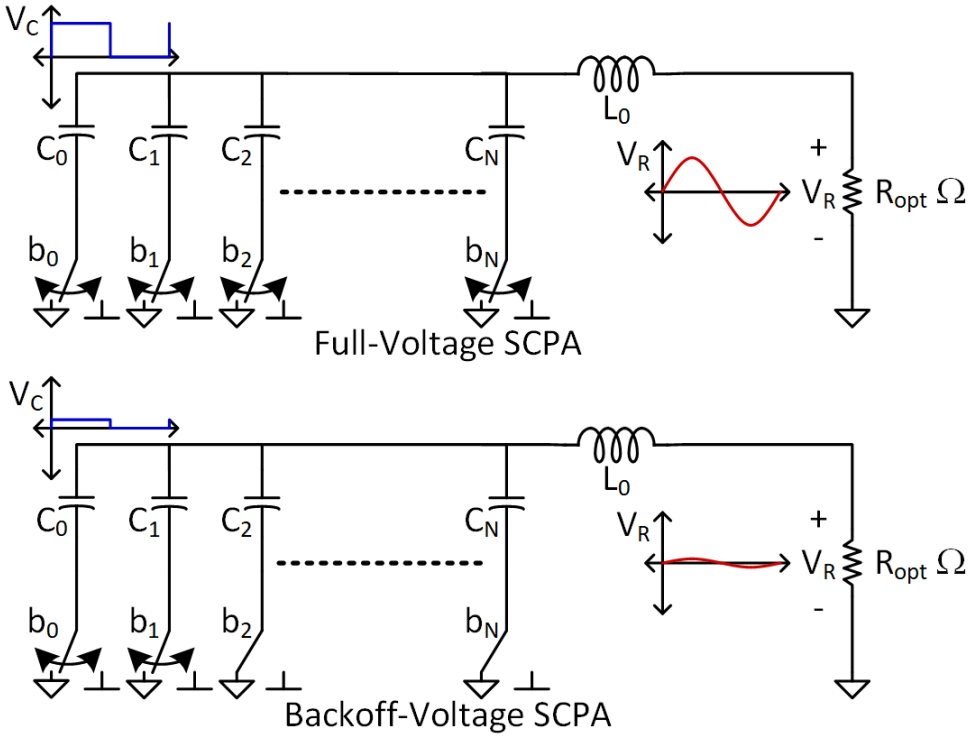
$$\eta = 100\%$$

- R_{opt}:

$$r_{opt} = \frac{2}{\pi^2}\frac{V_{DD}^2}{P_{out}}$$

- In CMOS switches and capacitors can be sub-divided
  - Slices can be unary ($\div N$) or binary ($\div 2^N$) weighted
- When all slices are switched, circuit is equivalent to class-D PA
- Resonance constant if RC product from switch-capacitor constant

Switched-Capacitor PA (SCPA)



Unit Capacitance:

$$C_N = C_U = \frac{C}{N}$$

[Yoo, et. al., JSSC 12/2011]

Switch at V_{DD}:

$$Q_1 = nC_UV_{DD}$$

Switch at V_{GND}:

$$Q_2 = NC_UV_C$$

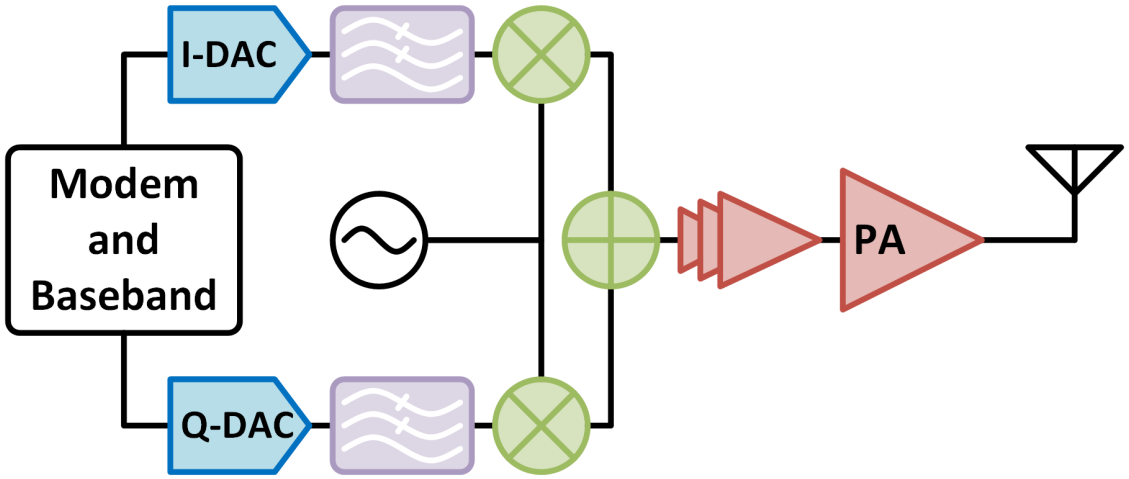
Charge Conservation:

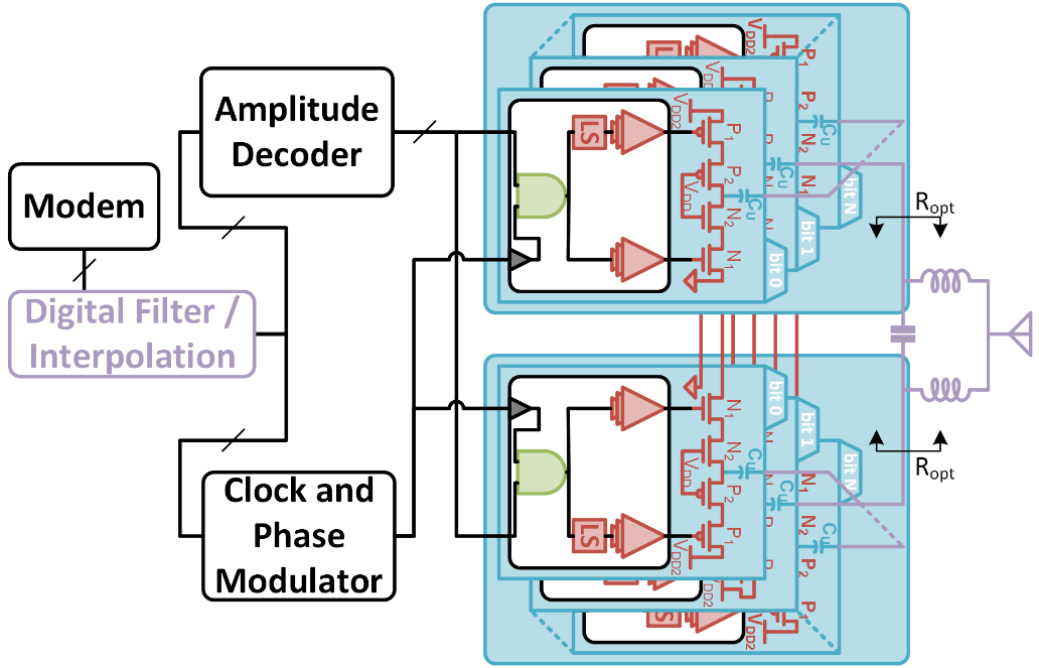
$$Q_1 = Q_2$$

$$V_C = \frac{n}{N}V_{DD}$$

- Voltage at capacitor top-plate changes due to charge-redistribution
- Very linear → precision capacitors and switches in CMOS
- Can model switch as variable-voltage switch!

Conventional TX vs. DPA

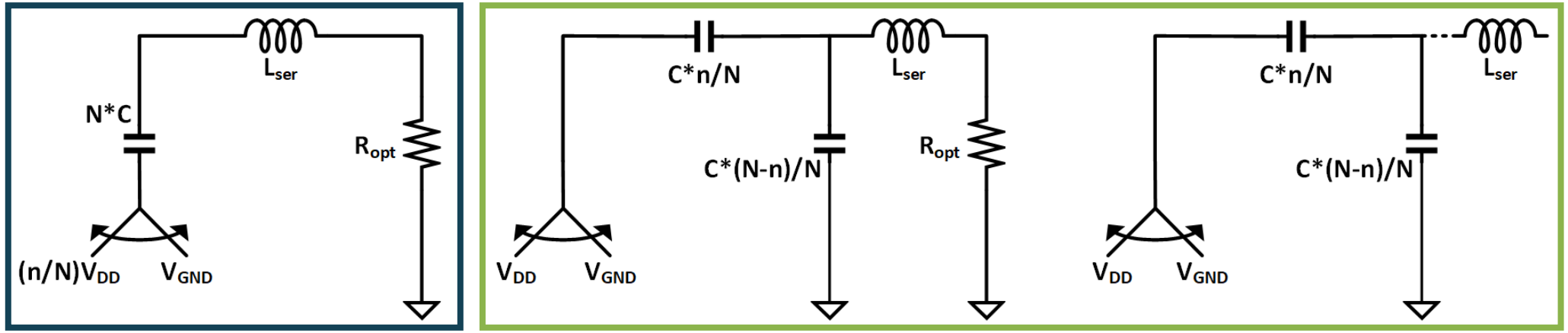




- DAC + Filter + Mixer + Amplifier + RF Filter
- All blocks Mixed-Signal/Analog/RF
- Filter is at Analog Baseband

- Digital Filter + Mixer + Amplifier + DAC + RF Filter
- All SCPA blocks realized by switching
- Filter at RF and Digital Baseband

SCPA: Output Power

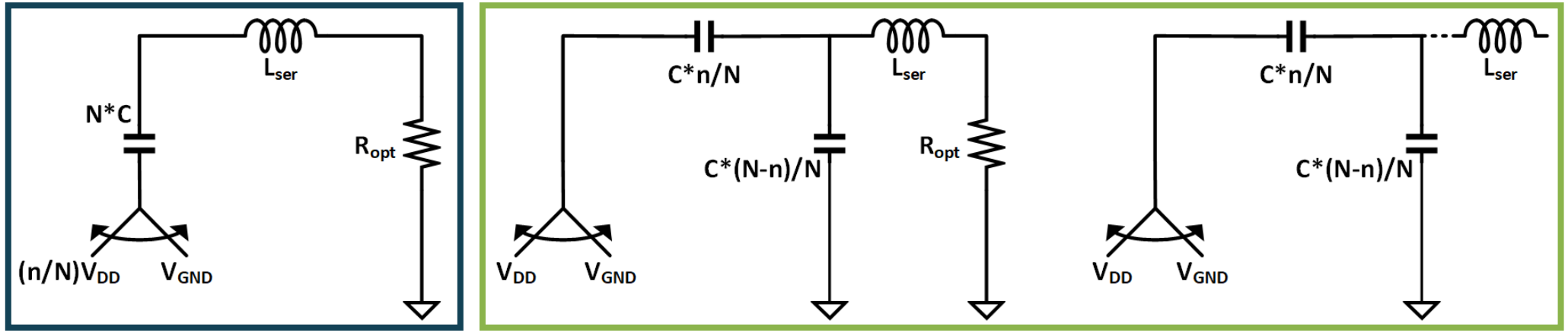


[Walling, et. al., RFIC-VJ 12/2018]

- Thevenin Eq.: variable voltage switch in series with RLC
- RLC tuned to switch closure frequency, f_{RF}
  - Selects fundamental Fourier component of pulsed V:

$$V_{out} = \frac{1}{2}\frac{4}{\pi}\left(\frac{n}{N}\right)V_{DD} \qquad P_{out} = \frac{2}{\pi^2}\left(\frac{n}{N}\right)^2\frac{V_{DD}^2}{R_{opt}}$$

SCPA: Power Dissipation



[Walling, et. al., RFIC-VJ 12/2018]

- Input power: $\propto C_{in}\, V_{DD}^2 f_{RF}$
- L_{ser} is RF current source → Open if switch closure is fast
- Input capacitance: $C_{in} = C\,\frac{N-n}{N^2}$

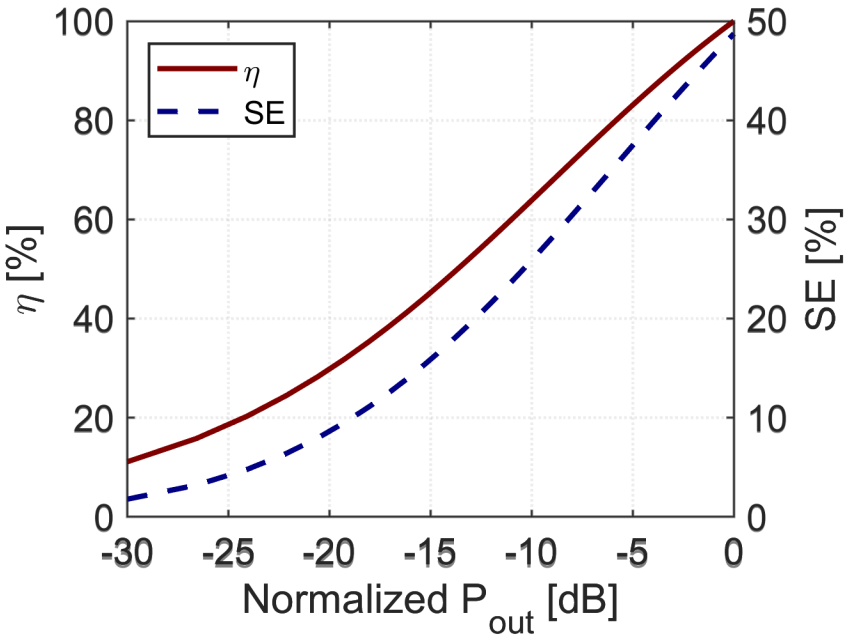
$$V_{out} = \frac{1}{2}\frac{4}{\pi}\left(\frac{n}{N}\right)V_{DD} \qquad P_{out} = \frac{2}{\pi^2}\left(\frac{n}{N}\right)^2 \frac{V_{DD}^2}{R_{opt}}$$

$$P_{in} = C\left(\frac{n-N}{N^2}\right)V_{DD}^2\, f_{RF}$$

SCPA: System Efficiency (SE)

- SCPA Total Power Consumption:
  - Lossy inductor: α
  - SW parasitic R: β
  - SW parasitic C: $P_{SWC} = (n/N) C_{SW} V_{DD}^2 f_{rf}$
  - Switch driver: $P_{DR} = (n/N) C_{DR} V_{DD}^2 f_{rf}$
  - Clock distribution: $P_{CLK} = C_{CLK} V_{DD}^2 f_{rf}$
  - Logic Decoders: $P_{Logic} = C_{Logic} V_{DD}^2 f_{rf}$

Benefit from scaling



$$\eta = \frac{P_{out}}{P_{out} + P_{in}} = \frac{4n^2}{4n^2 + \frac{\pi n(N-n)}{Q_{NW}}}$$

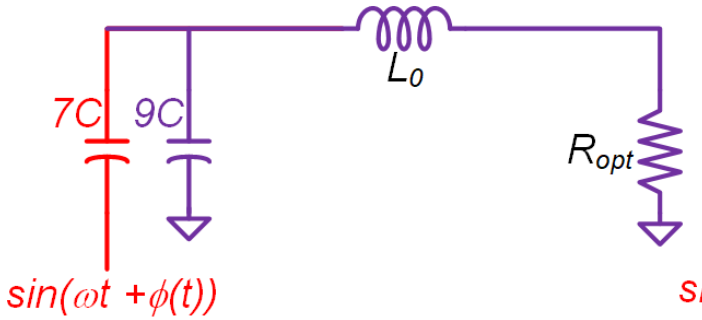
$$Q_{NW} = \frac{1}{2\pi f_{RF} C r_{opt}} = \sqrt{\frac{50\Omega}{r_{opt}} - 1}$$

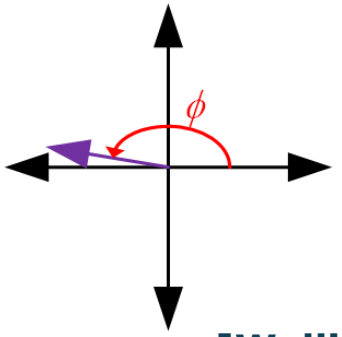
$$SE = \frac{\alpha \cdot \beta \cdot P_{out}}{P_{out} + P_{in} + P_{SWC} + P_{DRV} + P_{CLK} + P_{Logic}}$$

$$\alpha = \frac{1}{1 + \frac{Q_{nw}}{Q_L}} \quad \beta = \left(\frac{R_{opt}}{R_{sw} + R_{opt}}\right)^2$$

Multi-phase (M)-SCPA

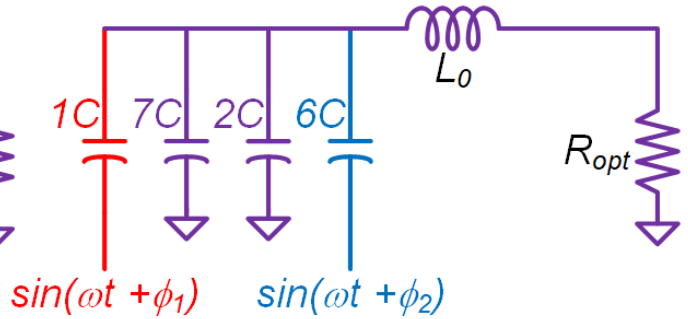
Polar (M=∞)

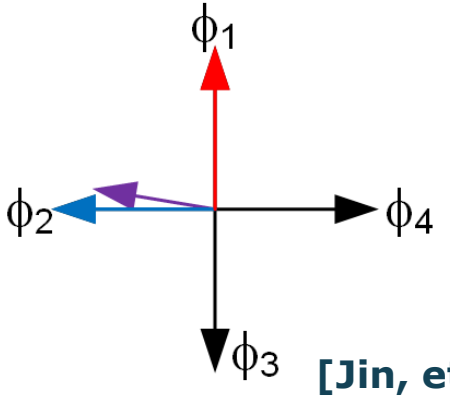




[Walling, et. al., RFIC-VJ 2019

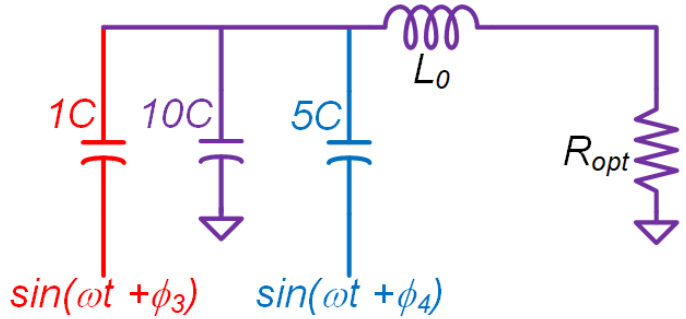
Quadrature (M=4)

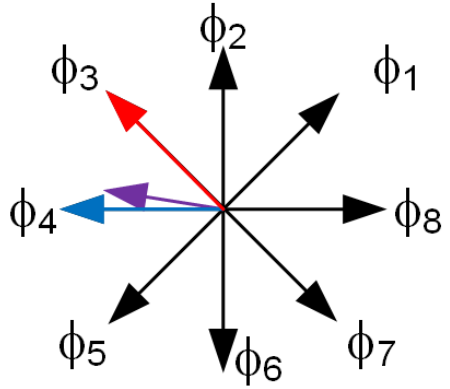




[Jin, et. al., JSSC, 05/2017 and Yoo, et. al., RFIC 2018]

Multiphase (M>4)





[Yuan, et. al., JSSC, 05/2017]

- Polar → Multi-phase: Rather than phase shift clock, switch capacitors on different phases with arbitrary weights

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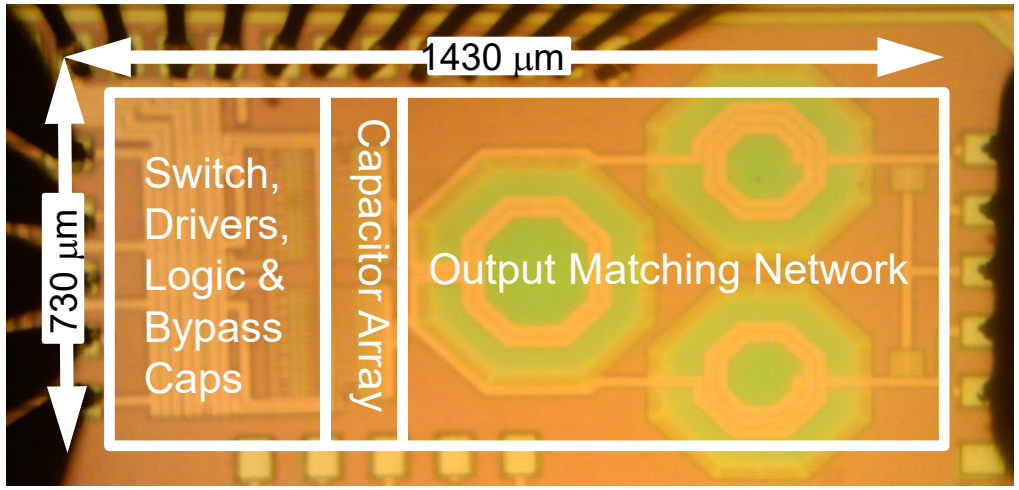
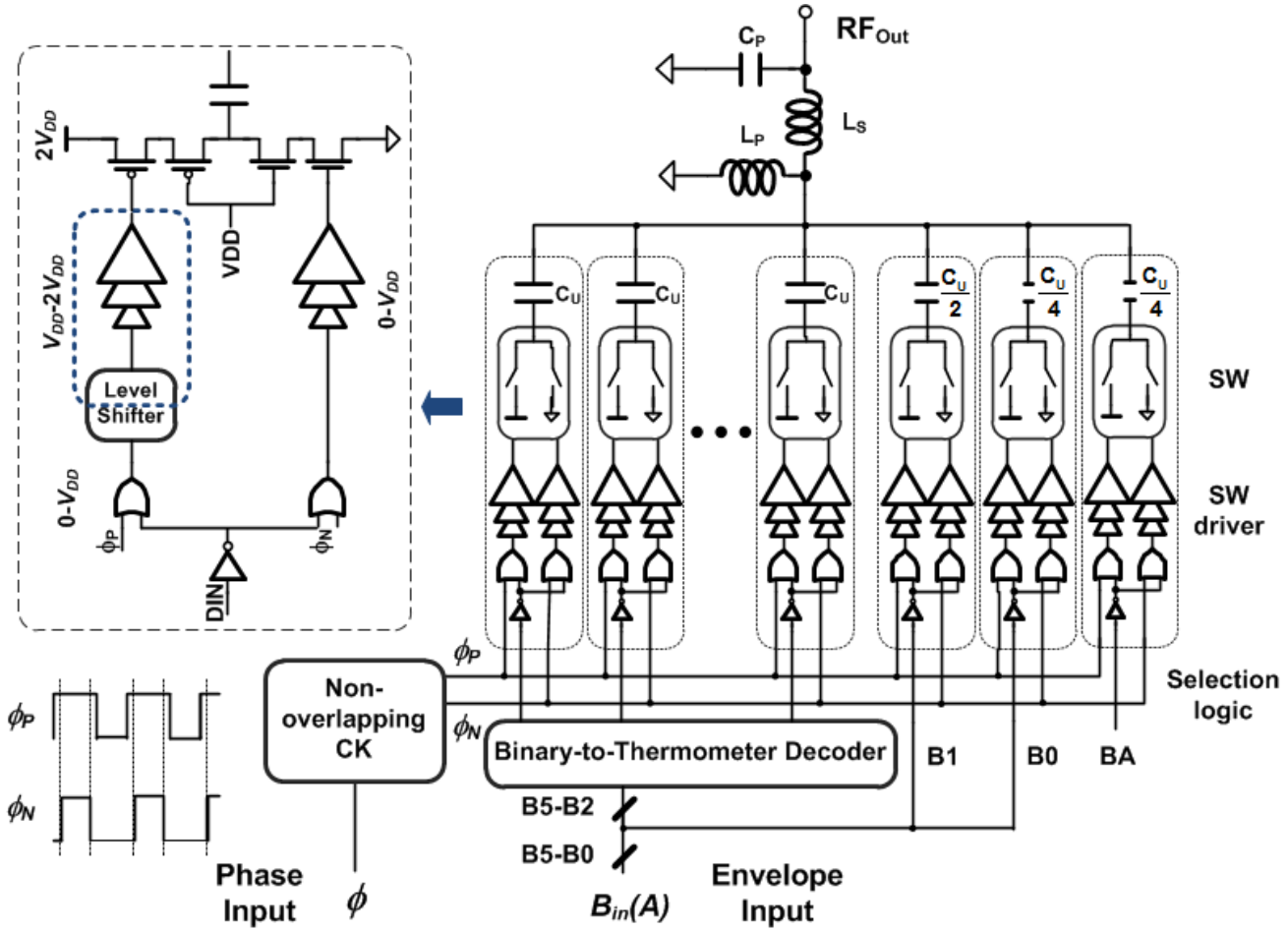
Example: Polar SCPA - I

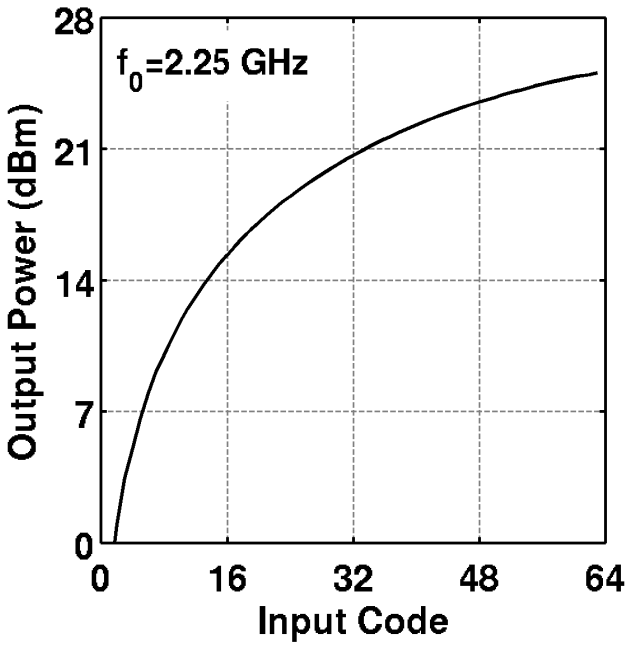


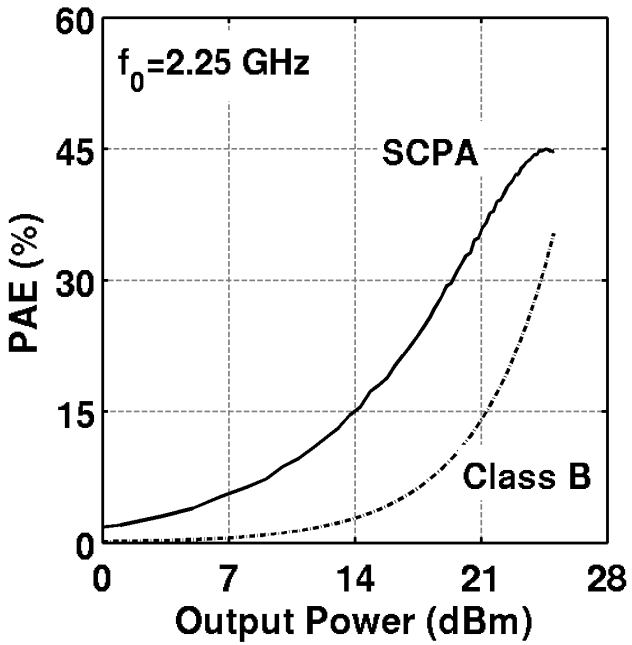
- First voltage-mode DPA!
- 90nm 6b segmented (4bU + 2bB) array
- Cap array in MiM layer
- Cascoded switch → higher η

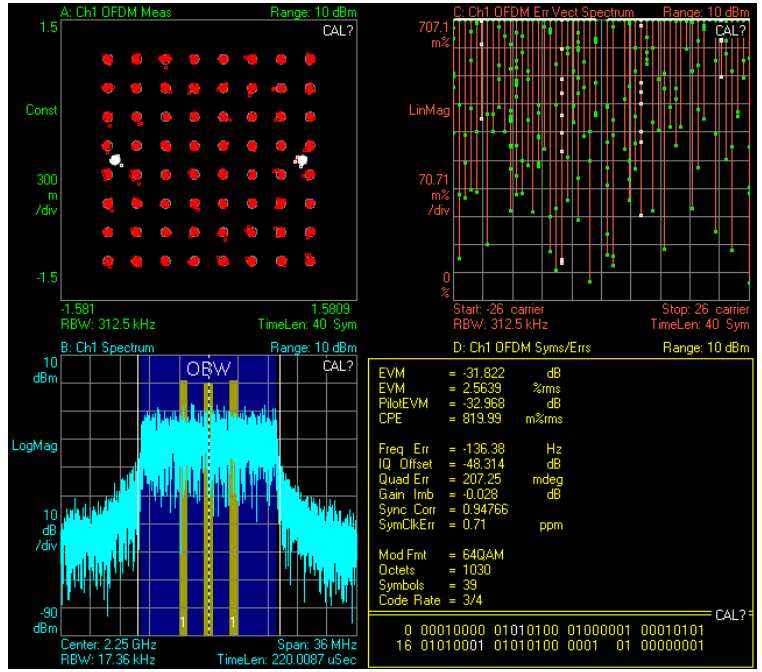


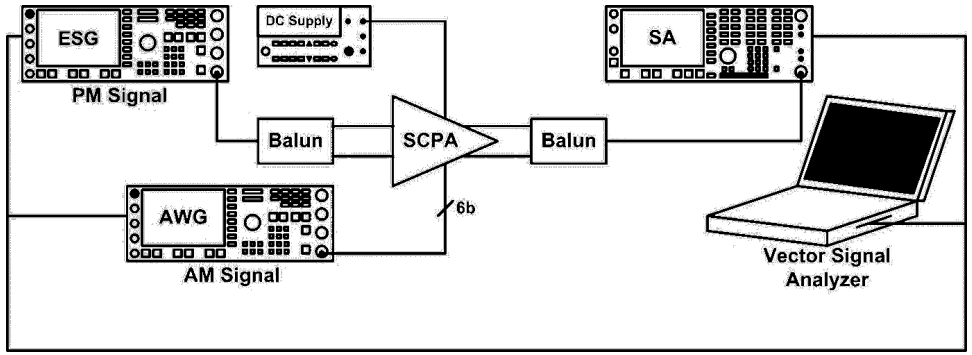
[Yoo, et. al., JSSC 12/2011]

Example: Polar SCPA - II



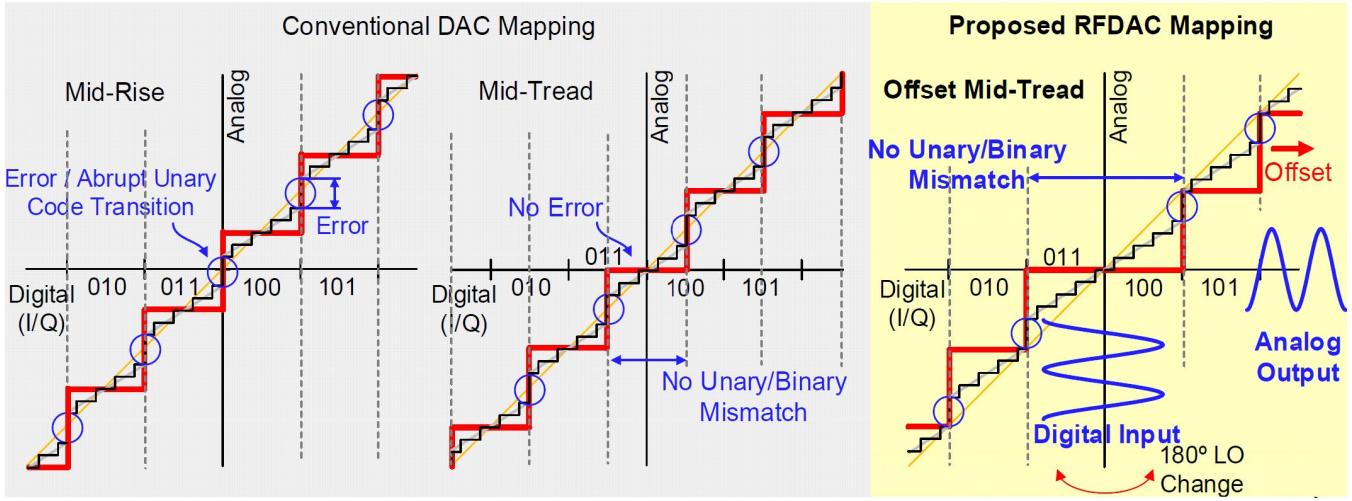






- EVM = 2.6%-rms @ P_{out} = 17.7 dBm (SE = 27%)
- Phase Modulation input from ESG
- Amplitude Modulation → digital pattern generator

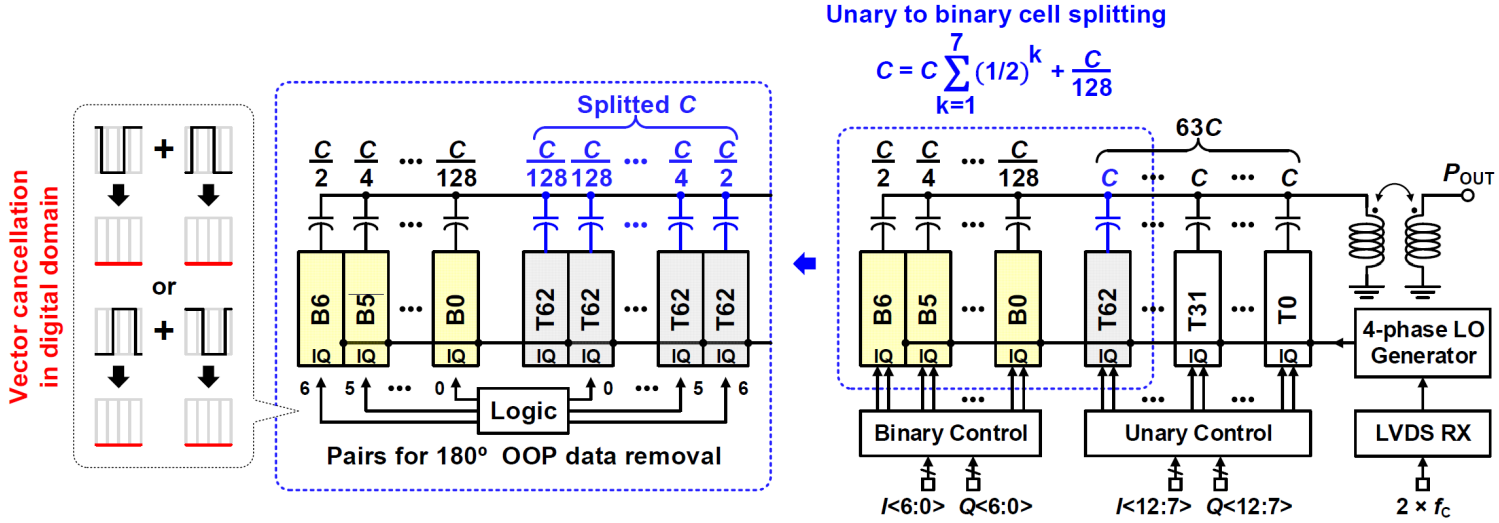
Example: Cartesian SCPA - I



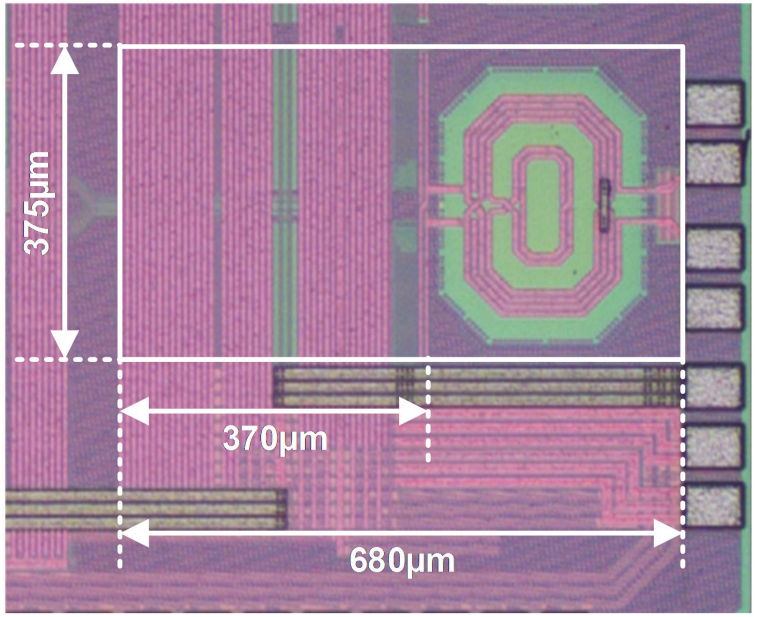
- Segmented DACs have large errors during unary → binary transitions
- Error is similar when using traditional DAC code mapping

[Yoo, et. al., ISSCC 2020]

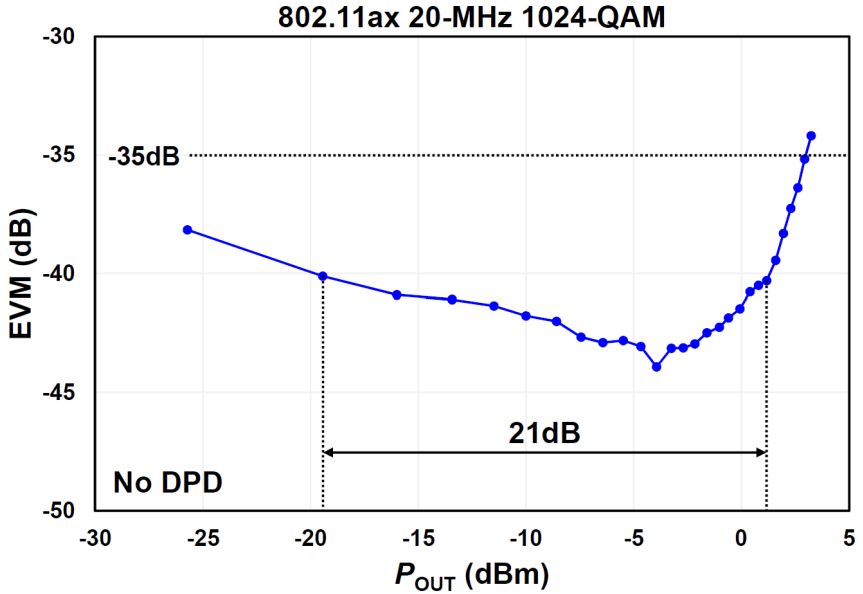
- Can modify the mapping by driving cells anti-phase so that their charge cancels!



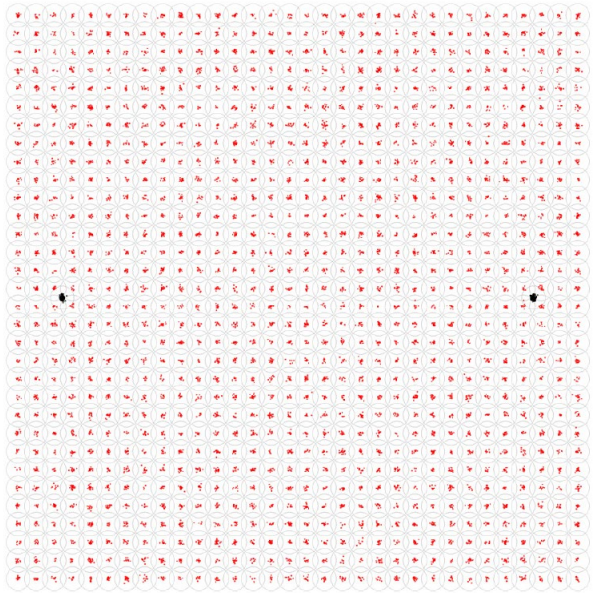
Example: Cartesian SCPA - II



[Yoo, et. al., ISSCC 2020]



802.11ax 40-MHz 1024-QAM



EVM = -42.2dB (@P_{OUT} = -3.0dBm)

- 65nm TX achieves < -40 dB EVM over 21 dB of power backoff
- Full digital transmitter occupies < 0.26mm^2

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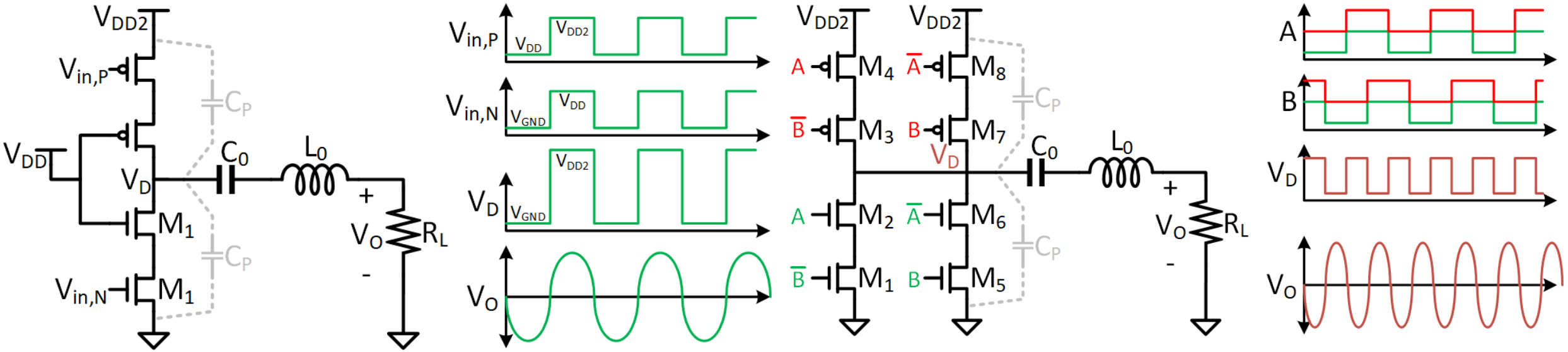
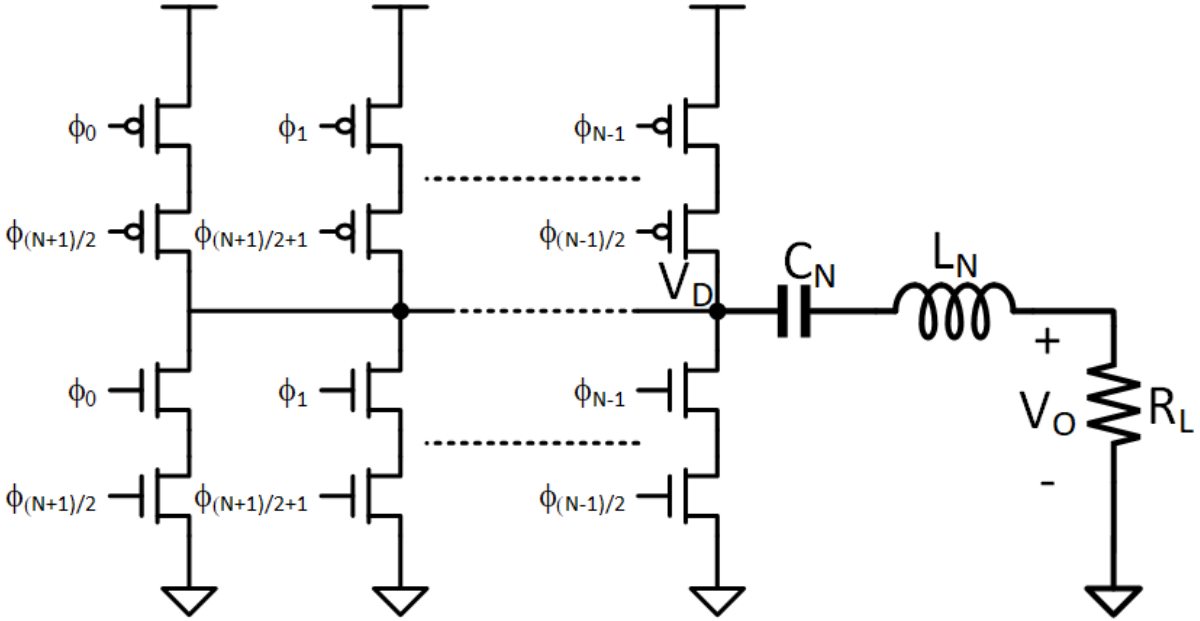
Multiplying SCPA: Leverage Edge-Combining

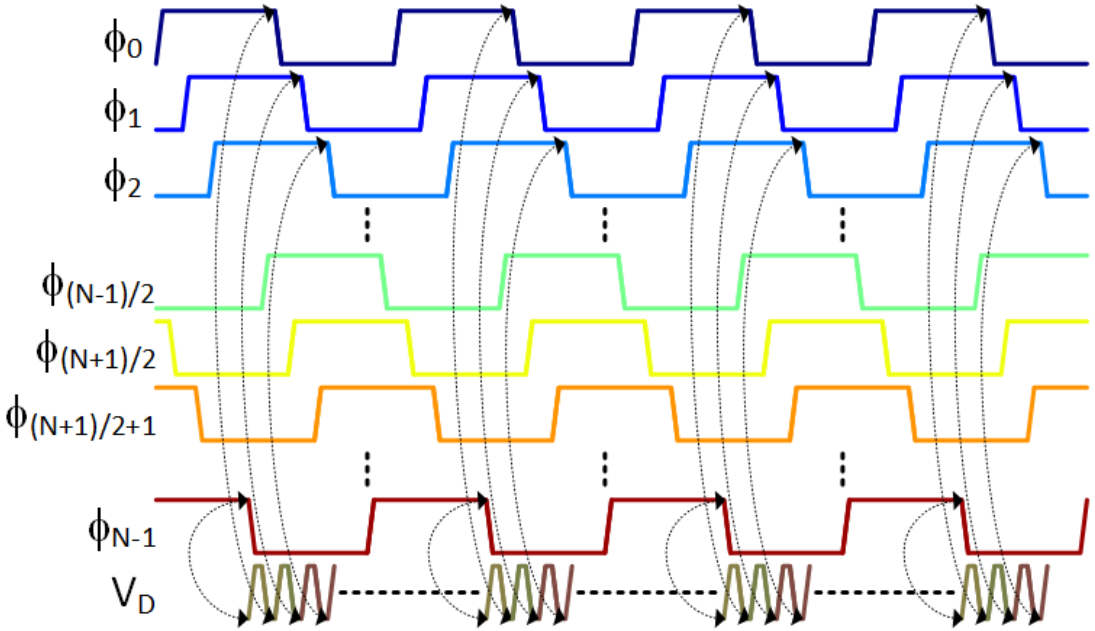


[Nguyen, et. al., accepted to TCAS-2]

- Original SCPA limits high-frequency operation:
  - PMOS transistors are slow
  - Parasitics must be (dis)charged every cycle → Power loss $\propto f_{rf}$
- Solution: Use multiple phases in edge-combining (XOR)

Generalized Edge-Combining (EC)

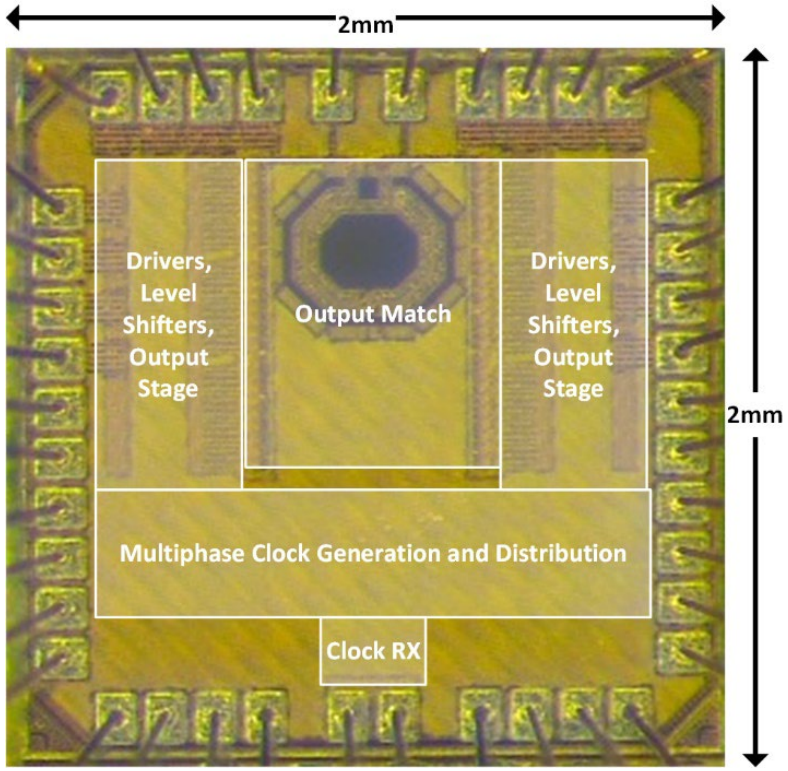


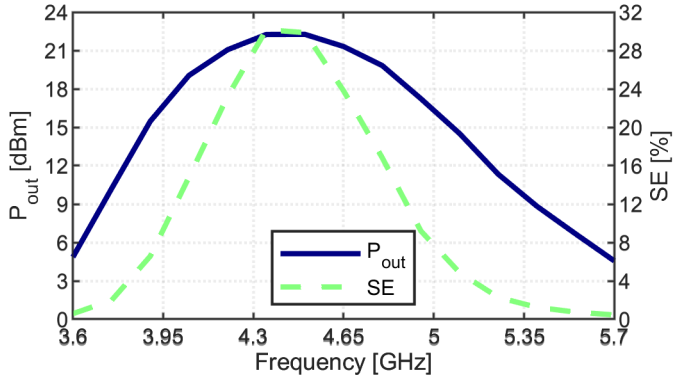


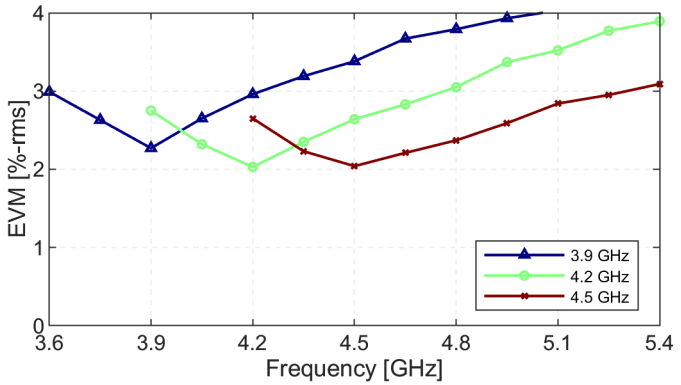
[Nguyen, et. al., accepted to TCAS-2]

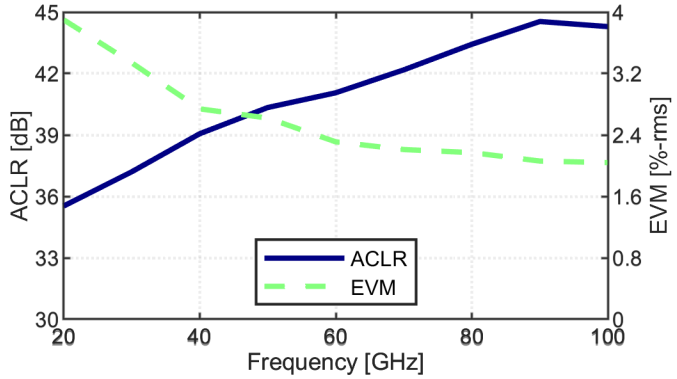
- Expand XOR to more than two inputs
- Generalize → combining by adding N-branches with N-phases
- Allows reduced frequency clock generation for given output → Also, no device must switch at output frequency

EC Tripling Class-D PA









Ref.	Topology	Tech.	Supply [V]	Freq. [GHz]	P_{out} [dBm]	SE/PAE/ η [%]
This Work	Class-D	65nm	2.4	4.5	22.3	30.2
[17]	Class-D^{-1}	65nm	2.1	3.3	23	35
[18]	Class-D^{-1}	65nm	3.0	4.5	26.7	27
[19]	Class-D	180nm	1.8	0.6	21	47

[Nguyen, et. al., accepted to TCAS-2]

- Fabricated 65nm prototype (MiM + UTM)
- Achieves operation at 4.5 GHz (fin=1.5GHz) Pout = 22 dBm @ SE = 30%
- Non-CE BPSK modulation shows good EVM/ACLR

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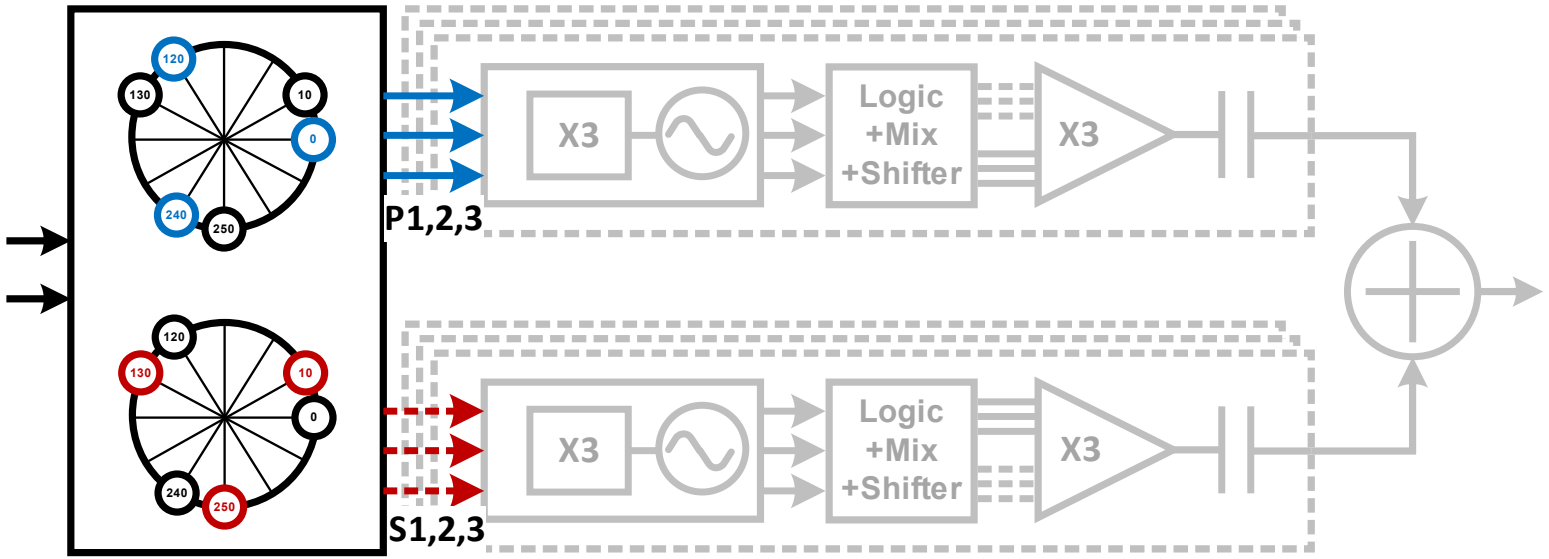
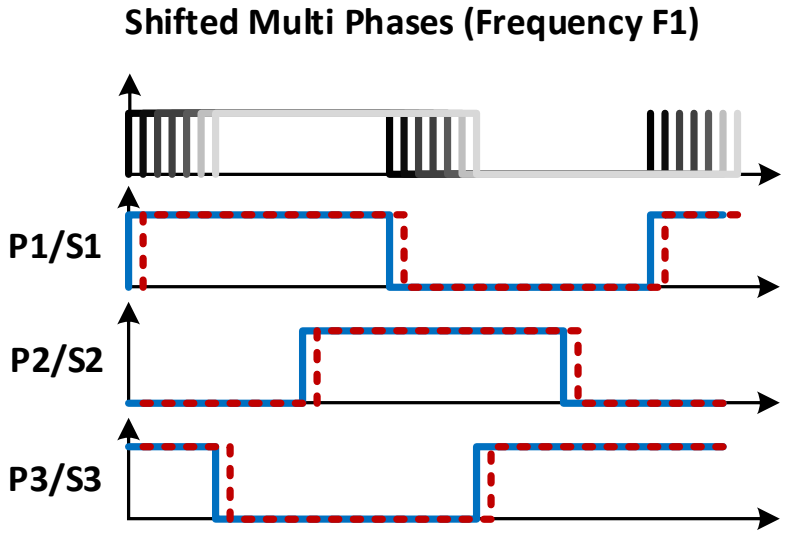
mmWave SCPA: Implementation - I

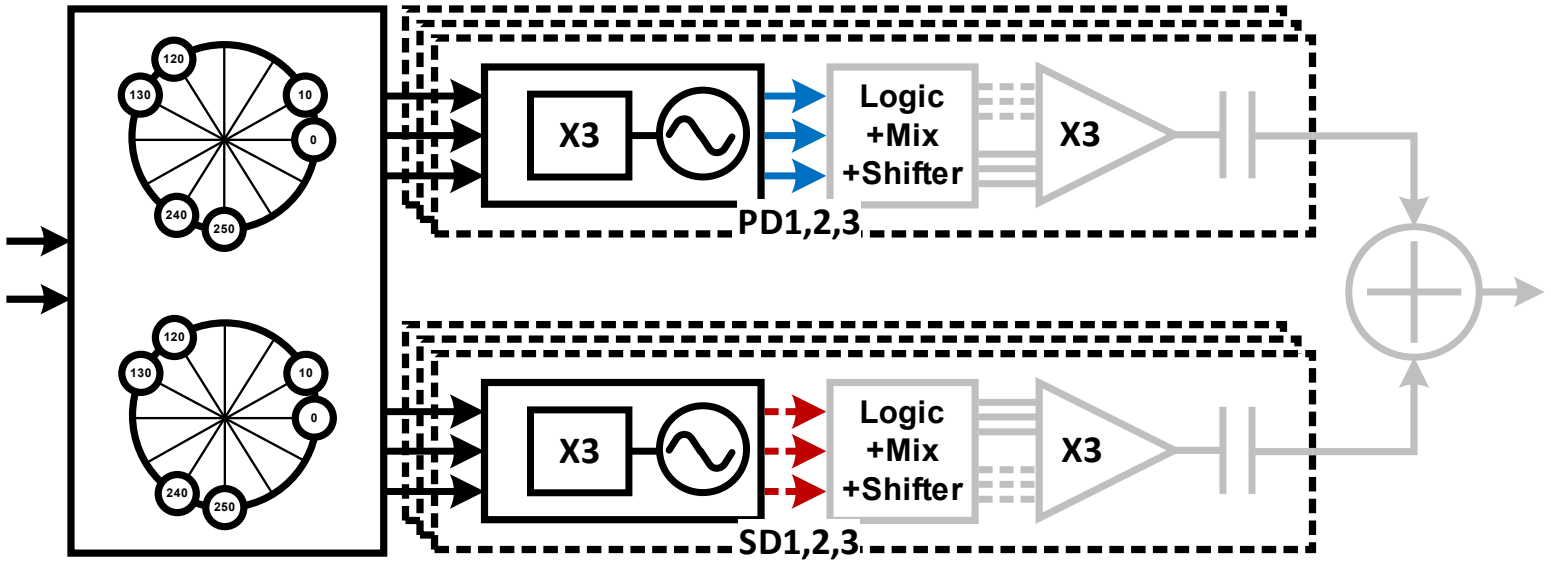


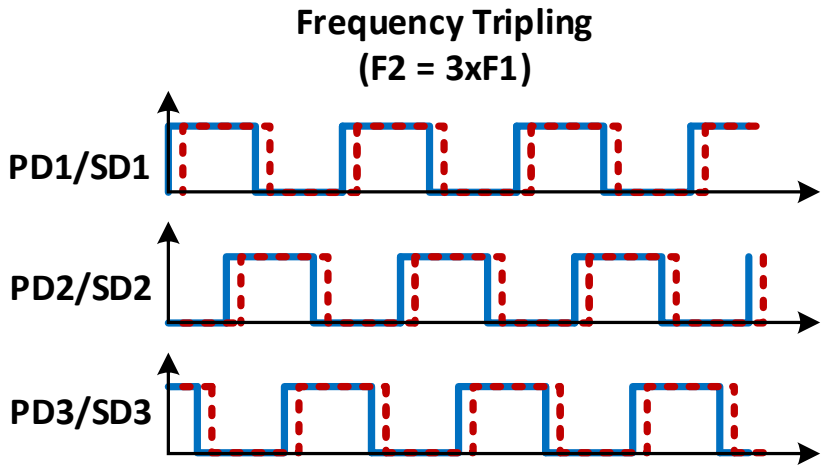


- Twelve phases generated at f_i
- Fed to the Edge-combining DLL network
- Input at *fi = fo/9 = 3.111GHz*

[Nguyen, et. al., JSSC 04, 2022]

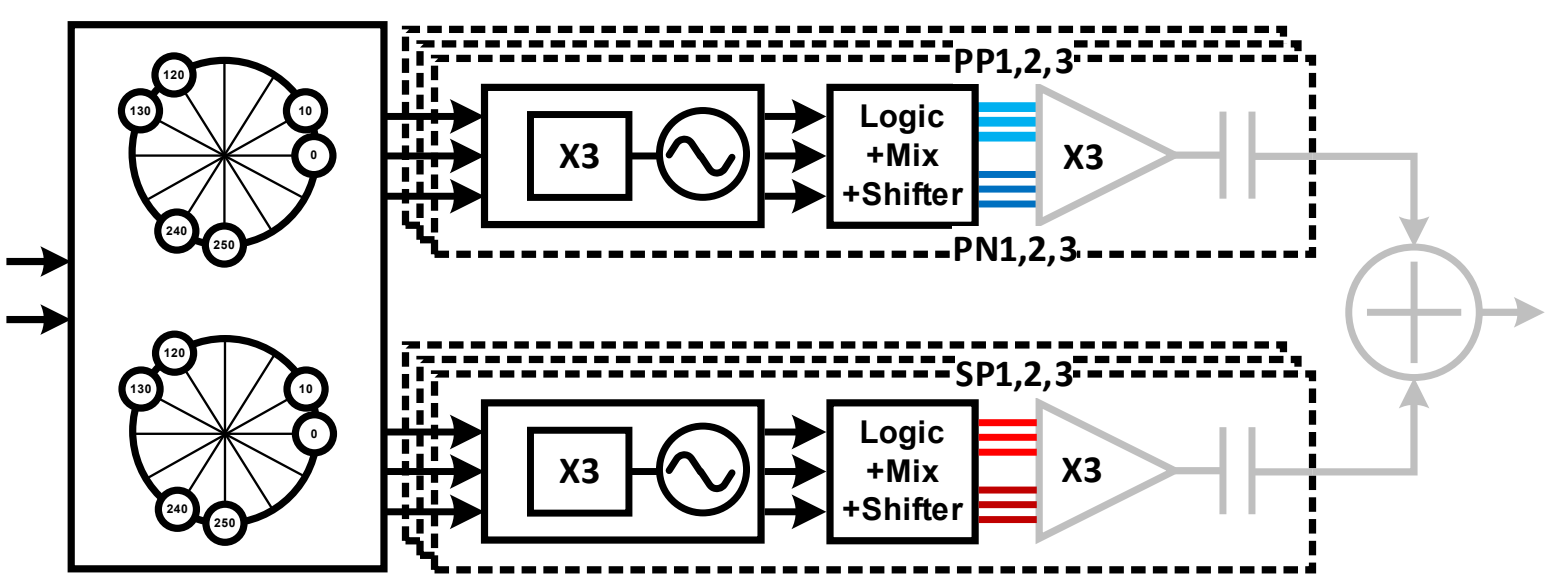
mmWave SCPA: Implementation - II

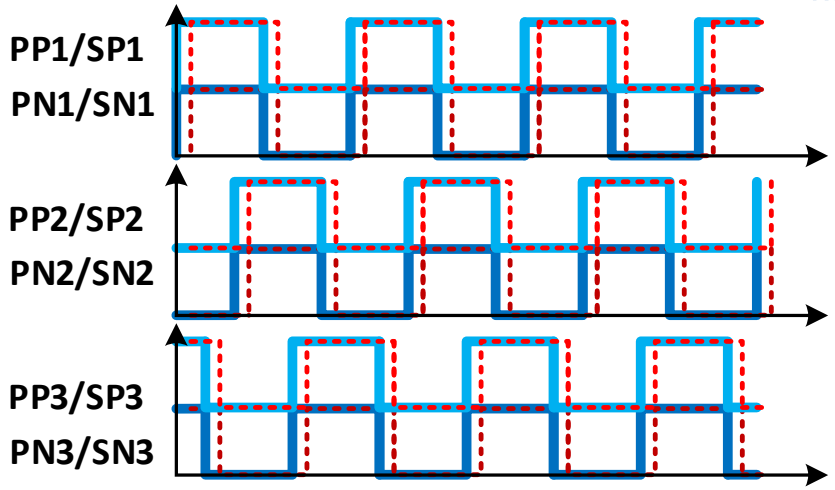




- DLL multiplied frequency by 3
- Multiphased output shifted with 30 degree phase-shifted
- $f_{i2} = f_o/3 = 9.333GHz$
- Tri-phased shifted -> Logic Mixer

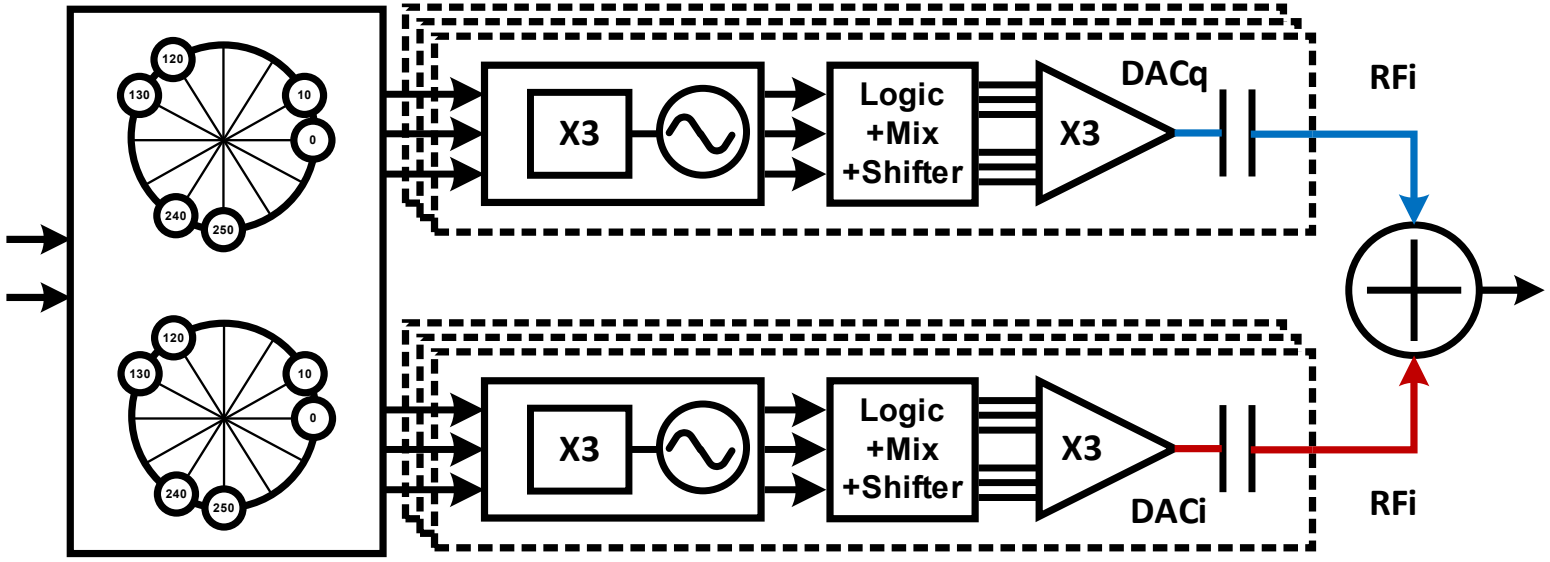
mmWave SCPA: Implementation - III

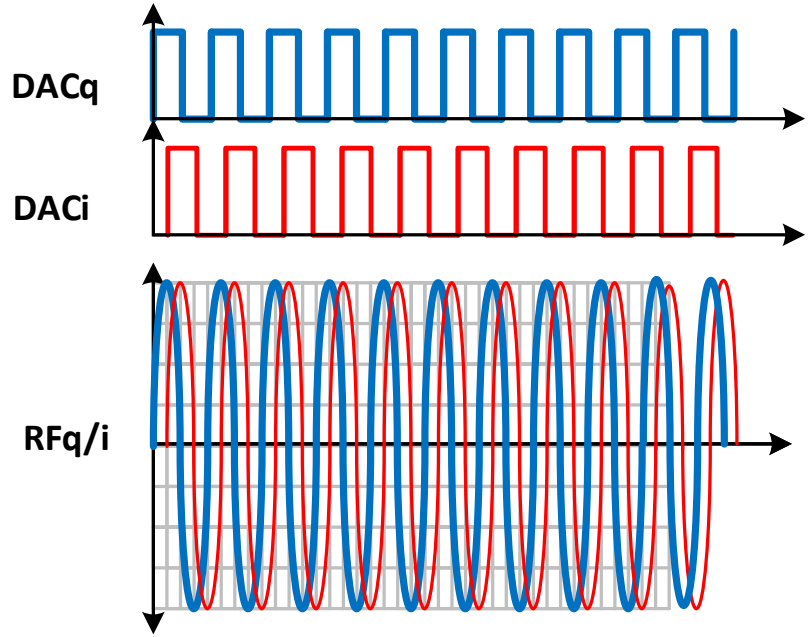




- Logic Mixer -> Buffed signal + level shifted signal
- Delay adjusted by the delay chain
- Optimization based exatraction simulation

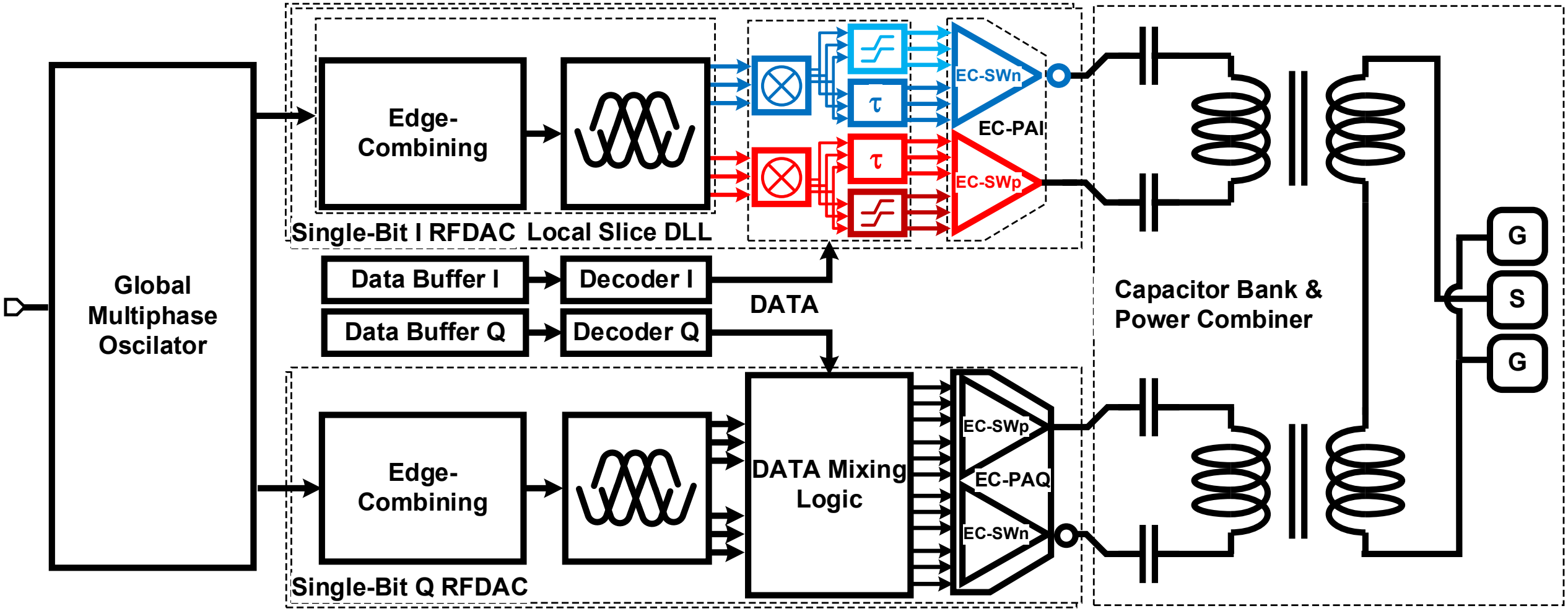
mmWave SCPA: Implementation - IV



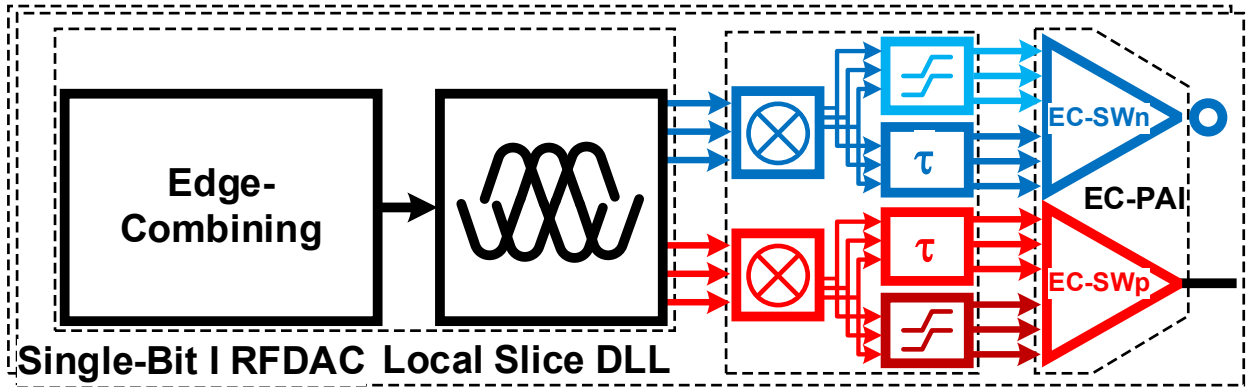


- Output phases shifted to 90deg.
- Impedance transformation after the capacitor array
- I/Q combination at the output

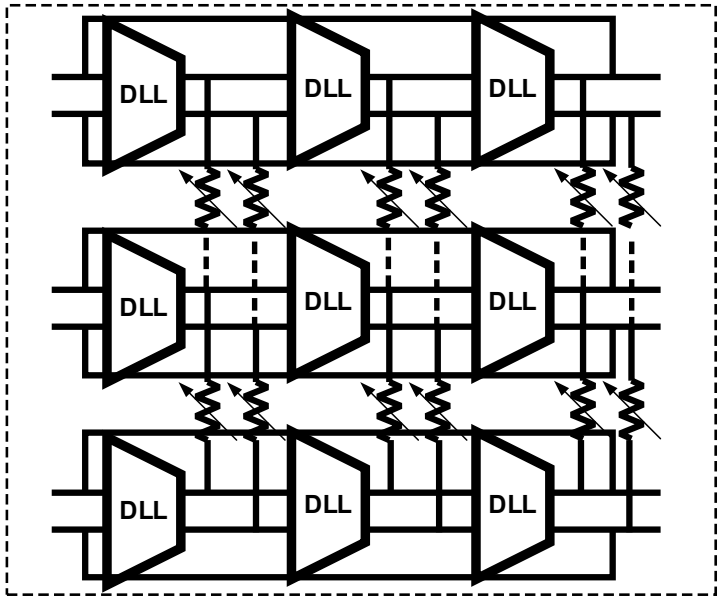
Top-level Block Diagram



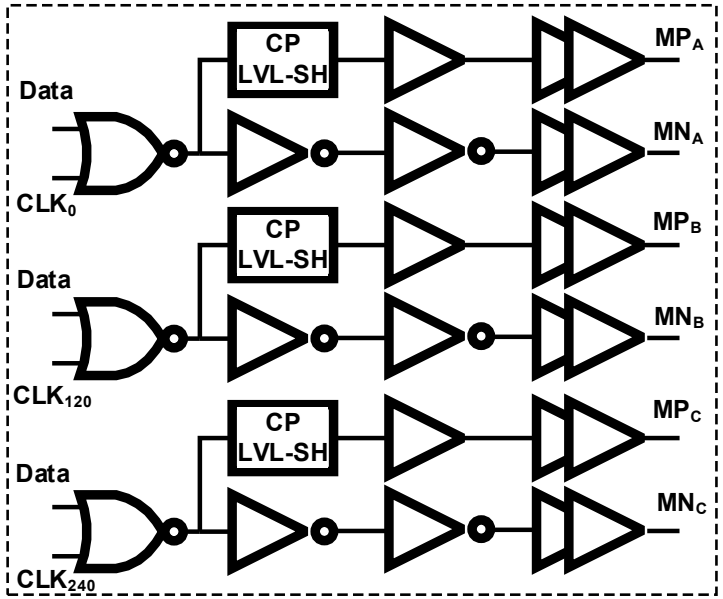
Single-slice mmWave SCPA Design



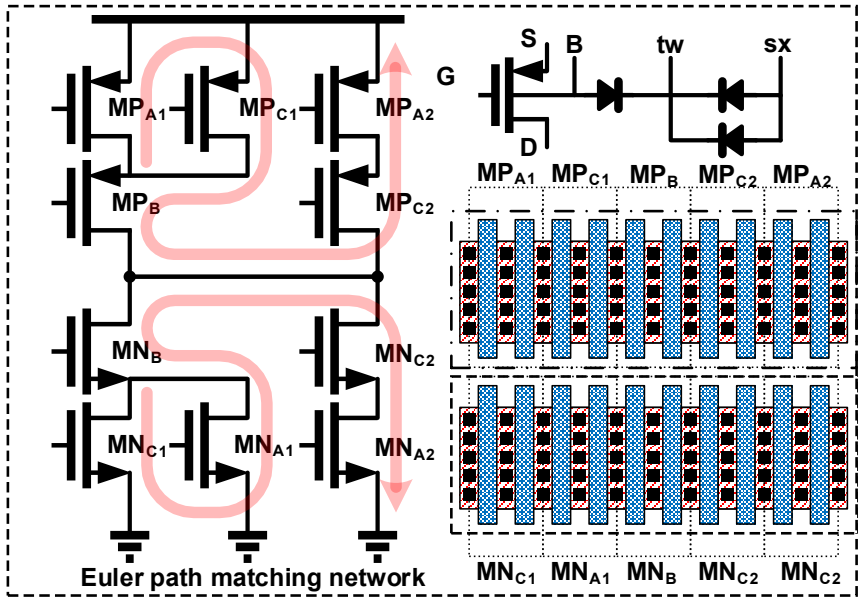
- Euler path for matching unit switched capacitor cell
- Deep-N-Well EGU- SLVT devices are used for faster switching and obtain better performance
- Coupled-DLL network provide in-phases for all unary unit-cells



DLL Matrix Network

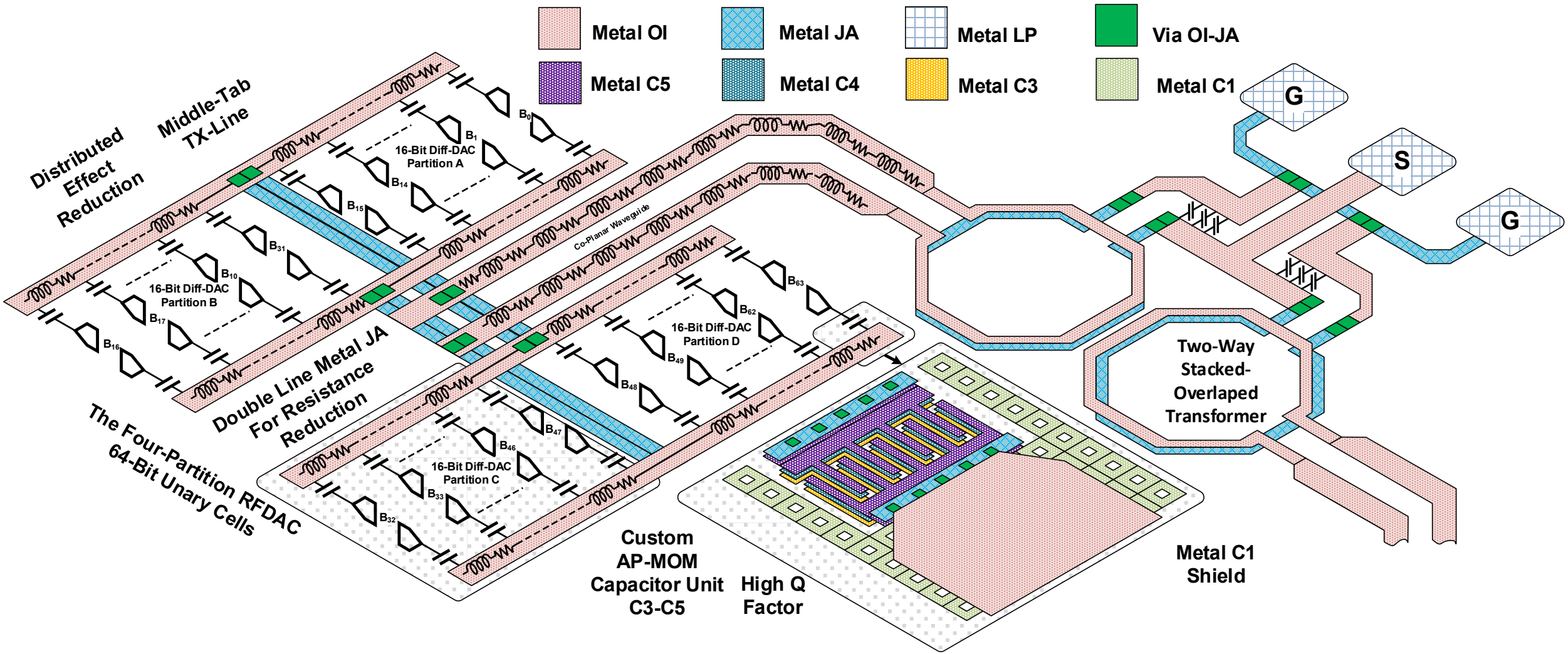


Single-slide-Driver

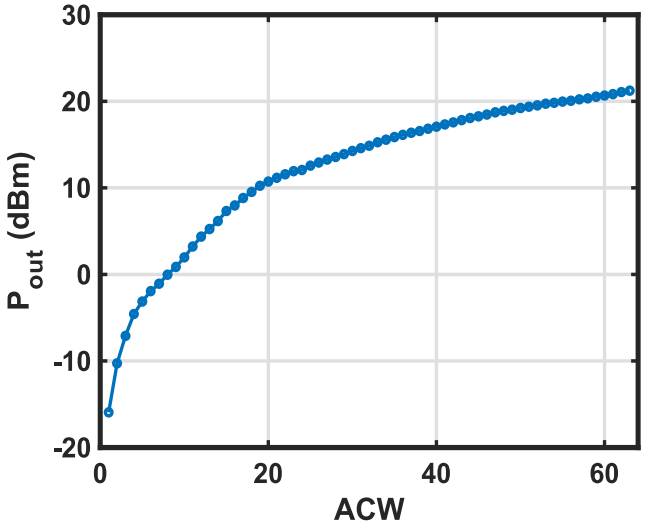


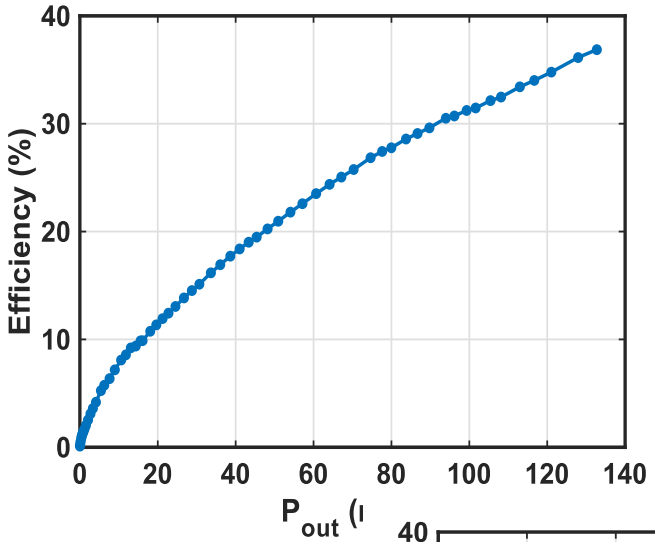
Unit-Cell Construction

mmWave SCPA Layout



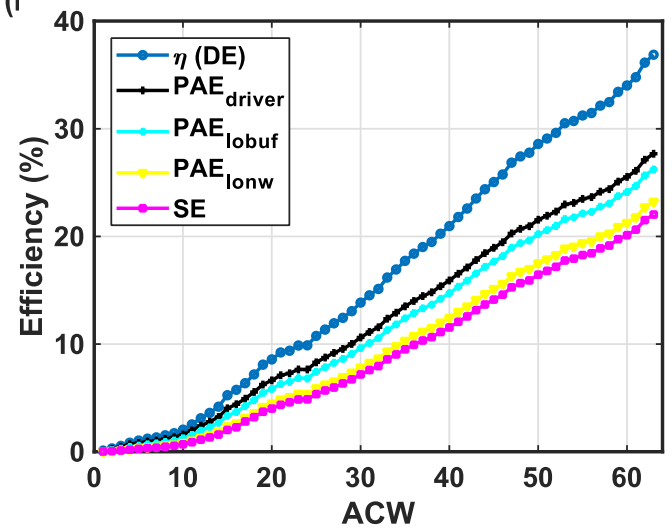
Measurement: Static Performance I

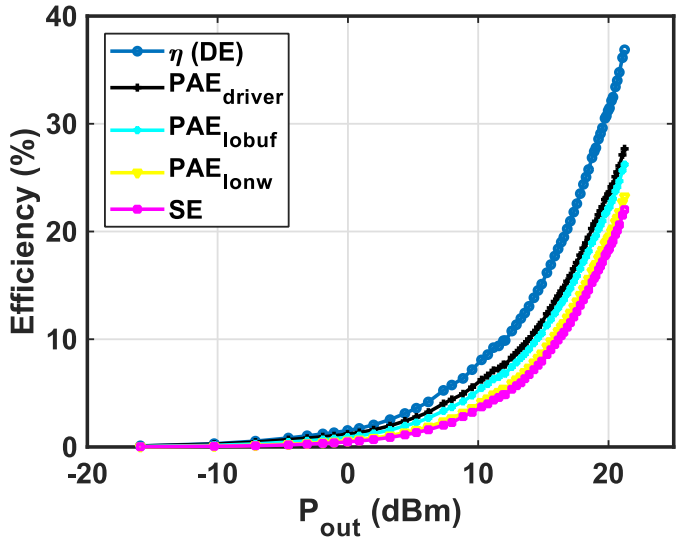




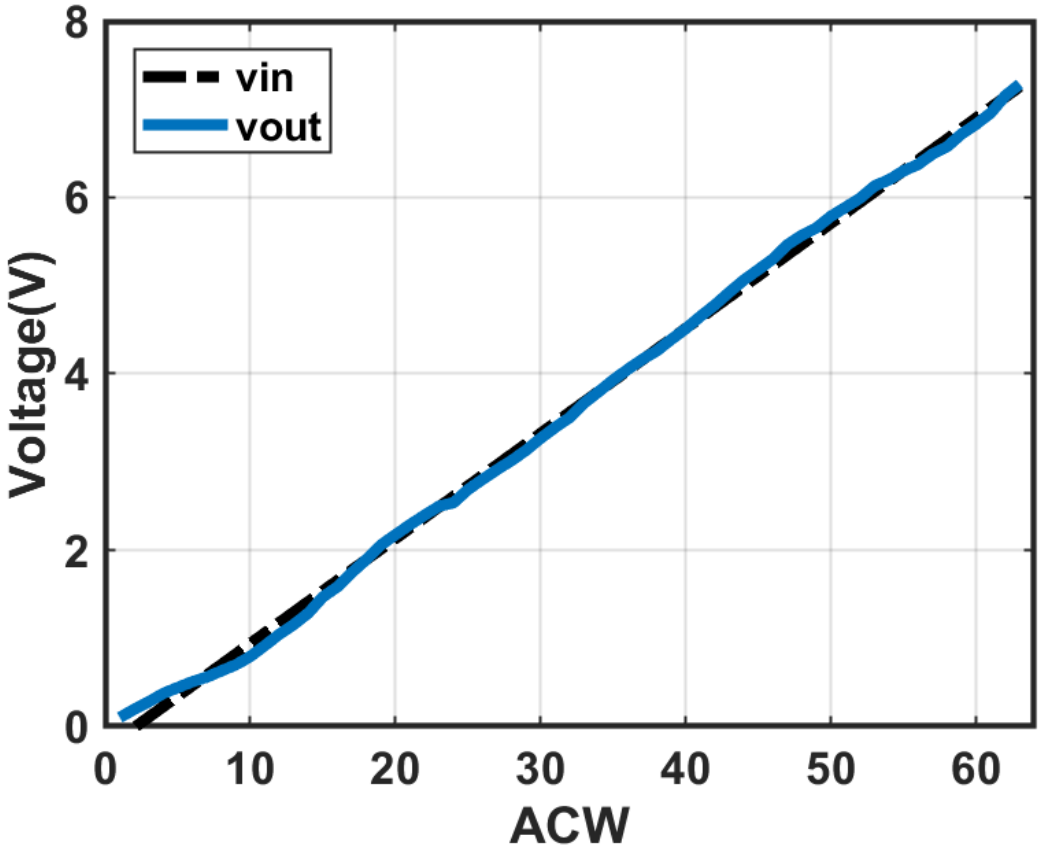
- P_{out} = 21.2dBm @ 27.9GHz
- Drain Efficiency (DE) = 36.7%

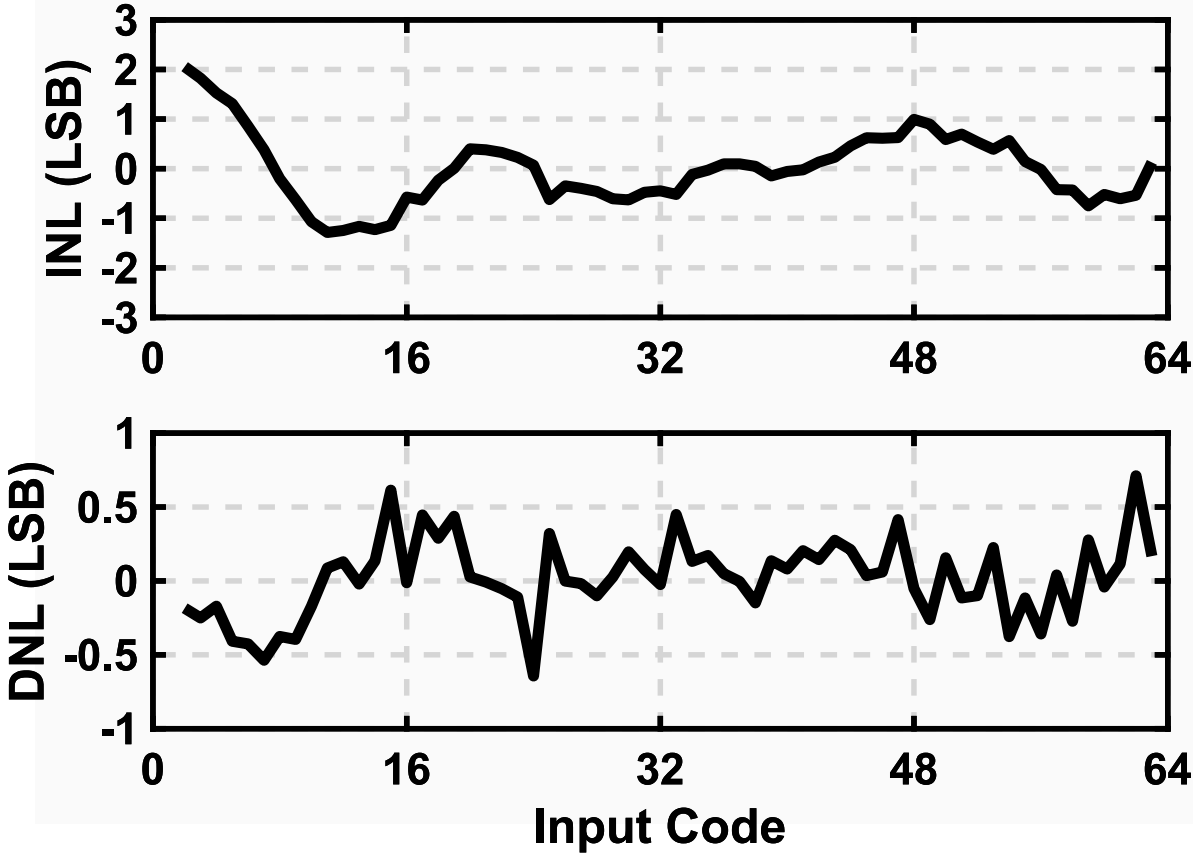
- System Efficiency (SE) = 22%





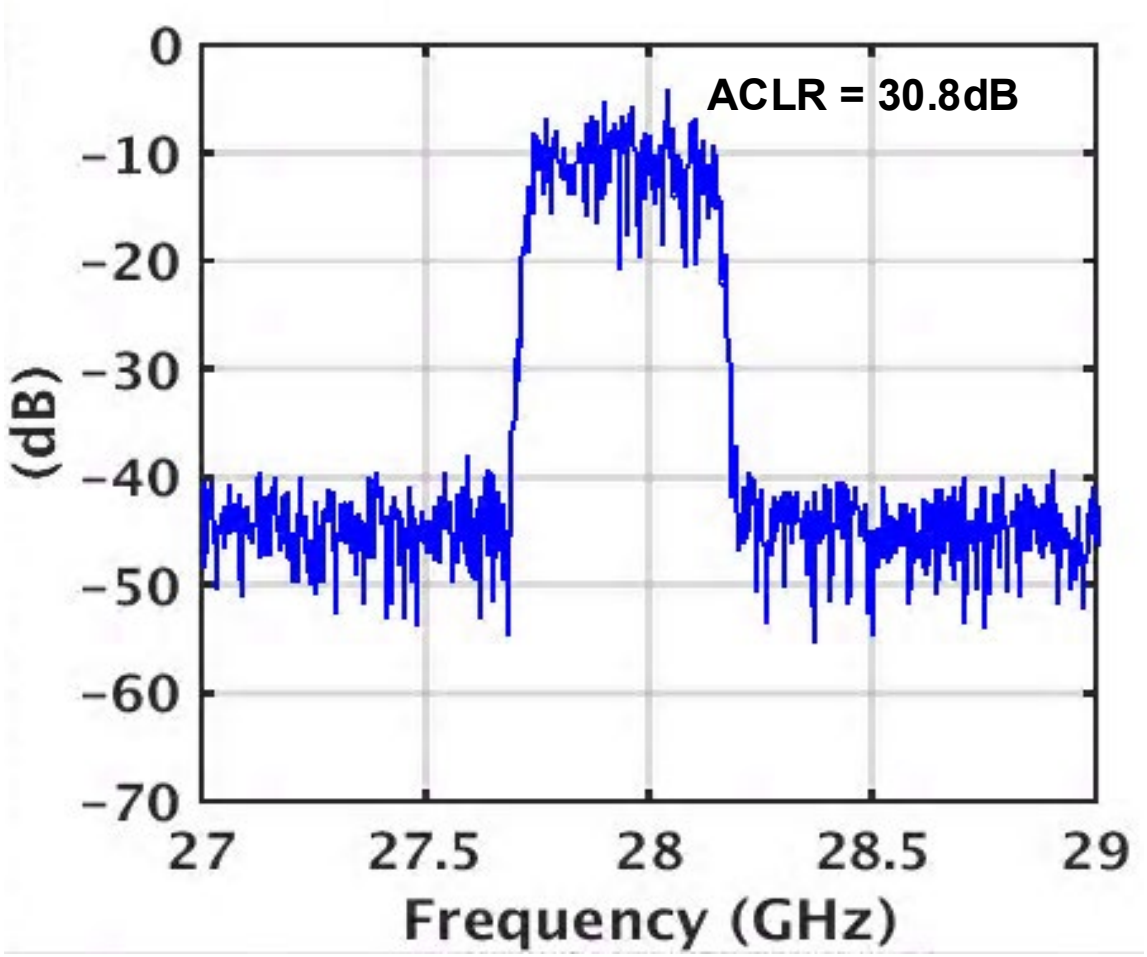
Measurement: Static Performance II

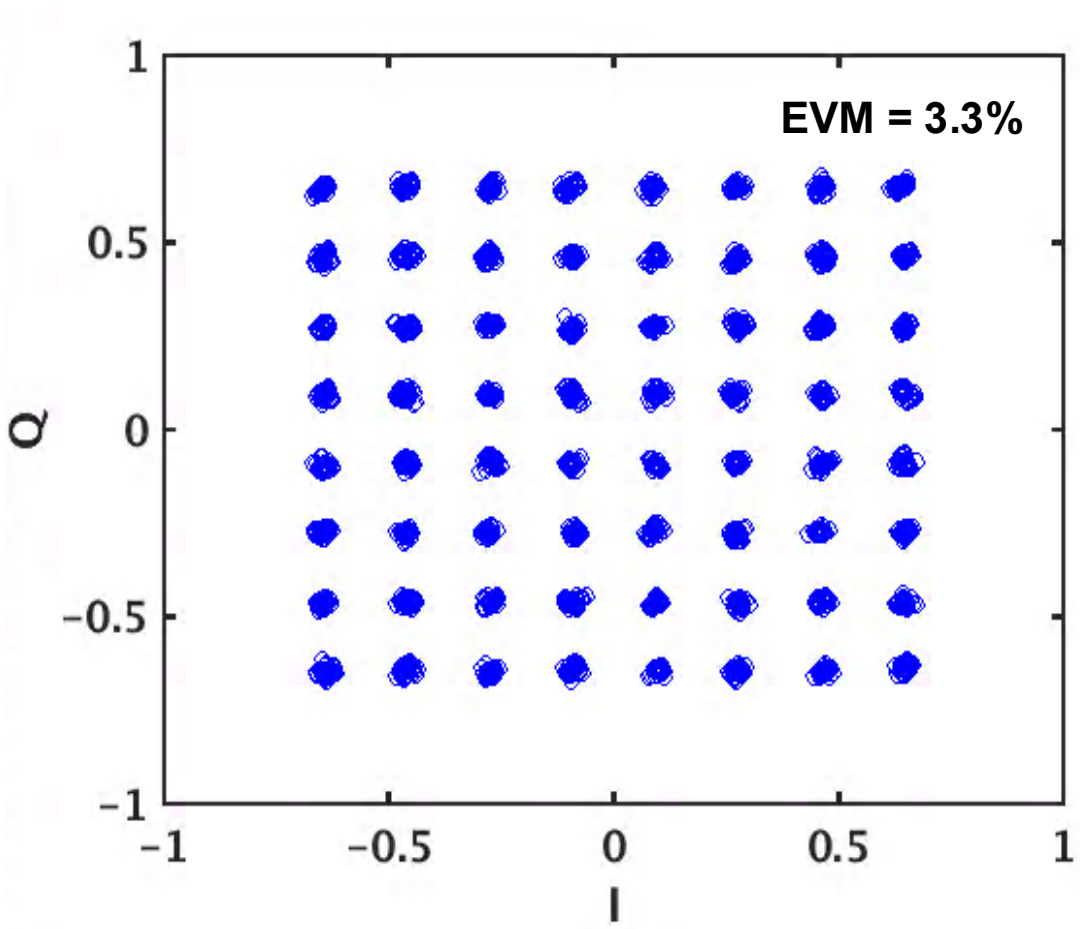




- AM – AM obtain nearly perfect linearity
- DNL = +/- 0.5LSB ; INL = +2/-1LSB

Measurement: Dynamic Performance





- EVM = 3.3% at (2.4Gb/s) with ACLR = 30.8dB

Outline

- Background and Motivation
- Switched-Capacitor Power Amplifier (SCPA) Introduction
- Recent Demonstrations of SCPAs
- mmWave SCPAs
  - Frequency multiplying class-D
  - Frequency multiplying SCPA
- **Conclusions**

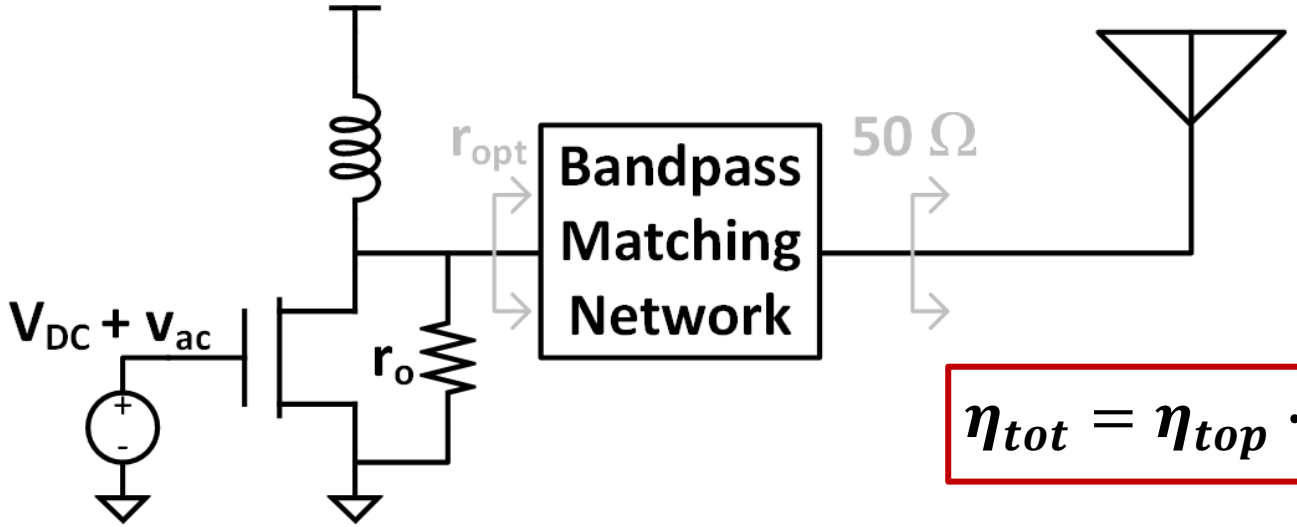
Conclusion

- SCPAs can be versatile, complete digital transmitters → Baseband to mm-Wave
- SCPAs are inherently linear and do not suffer compression like linear PA and current-mode DPAs
  - Lack of interfaces makes them inherently broadband
  - Switching operation makes them energy efficient
- Frequency limitations can be overcome by embedding frequency multiplication into the output stage

Questions

Power Amplifier Efficiency

Generic CMOS Power Amplifier



$$\eta_{tot} = \eta_{top} \cdot \eta_{div} \cdot \eta_{match}$$

- Three primary drivers of PA efficiency, η:
  - Topology (e.g., class-A, -B, -D, -E, etc.)
  - Voltage/current division at drain node
  - Loss in bandpass impedance matching network

PA Efficiency Breakdown

- Topology:
  - Current-mode (A: 50%, B:78.5%)
    - Determined by conduction angle
  - Switching/Voltage Mode (100%)
    - Achieved via pulse shaping
- Matching Network:
  - Losses in passive components (inductors)
  - Q_{NW} → dictated by impedance transform:

$$ex.:\ \eta_{match} = \frac{1 - \frac{Q_{NW}}{Q_{ind,shunt}}}{1 + \frac{Q_{NW}}{Q_{ind,series}}}$$

$$Q_{NW} = \sqrt{\frac{R_{antenna}}{R_{opt}} - 1}$$

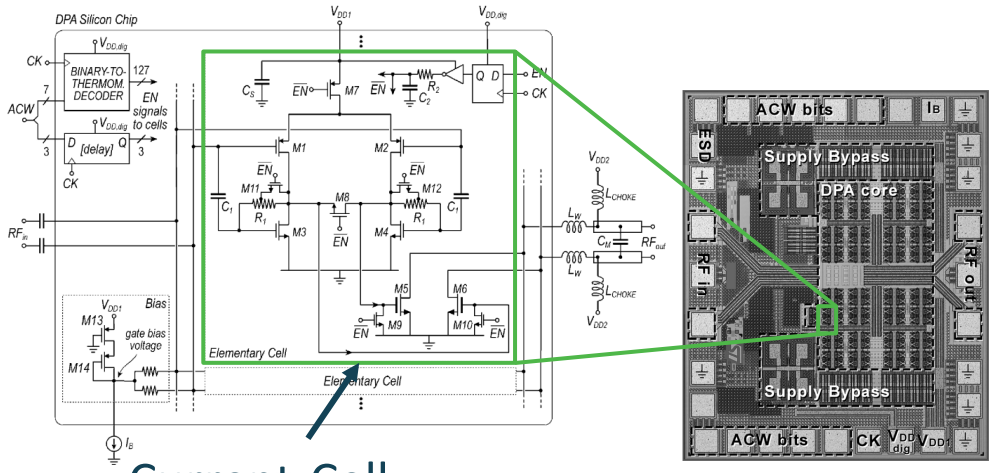
- Output division:
  - Current division:

$$\eta_{div} = \left(\frac{r_o}{r_{opt} + r_o}\right)^2$$

  - Voltage division:

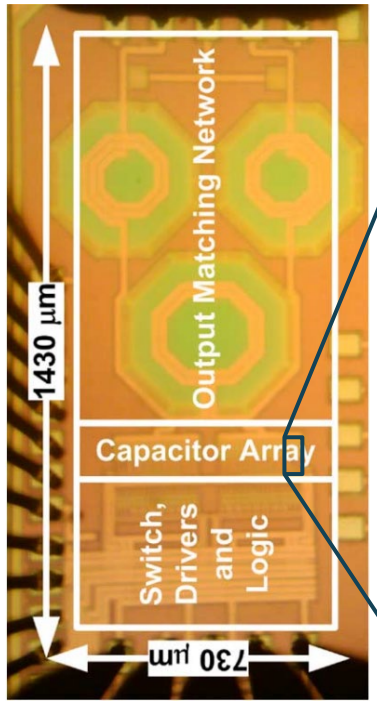
$$\eta_{div} = \left(\frac{r_{opt}}{r_{opt} + r_{sw}}\right)^2$$

Mixed-Mode TX – Slice Based Design

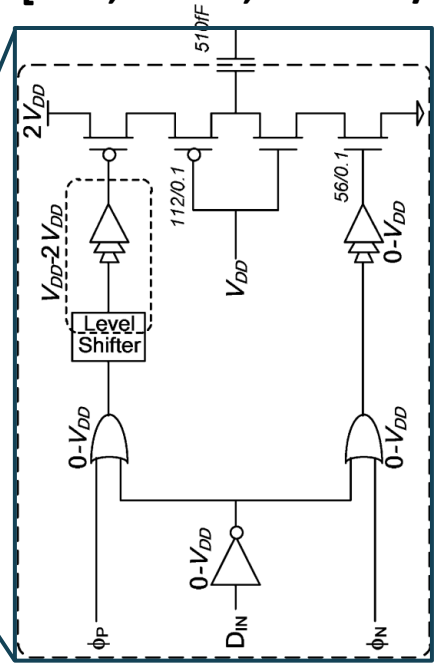


Current-Cell

[Presti, et. al., JSSC 7/2009]

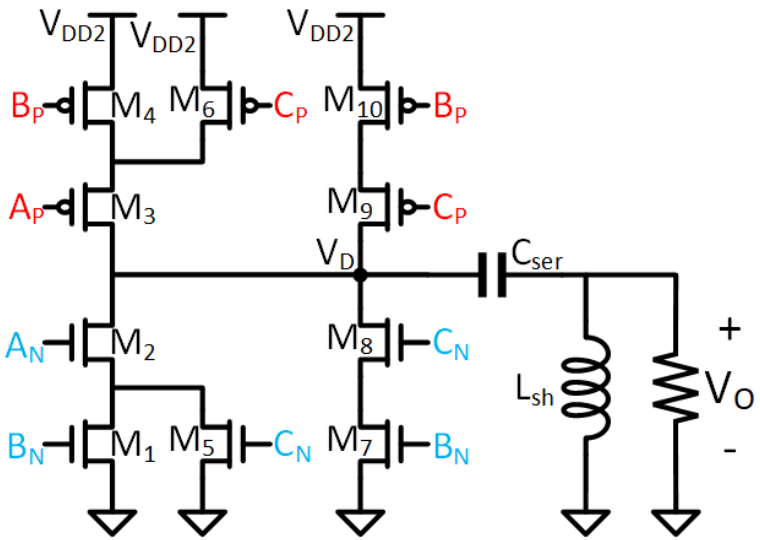


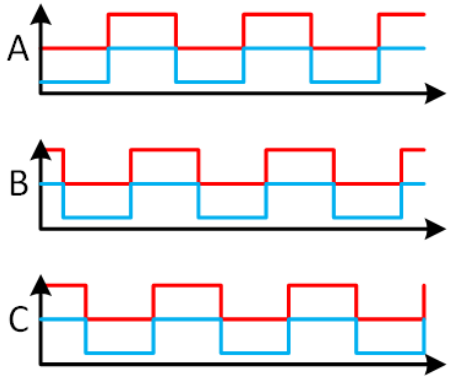
[Yoo, et. al., JSSC 12/2011]

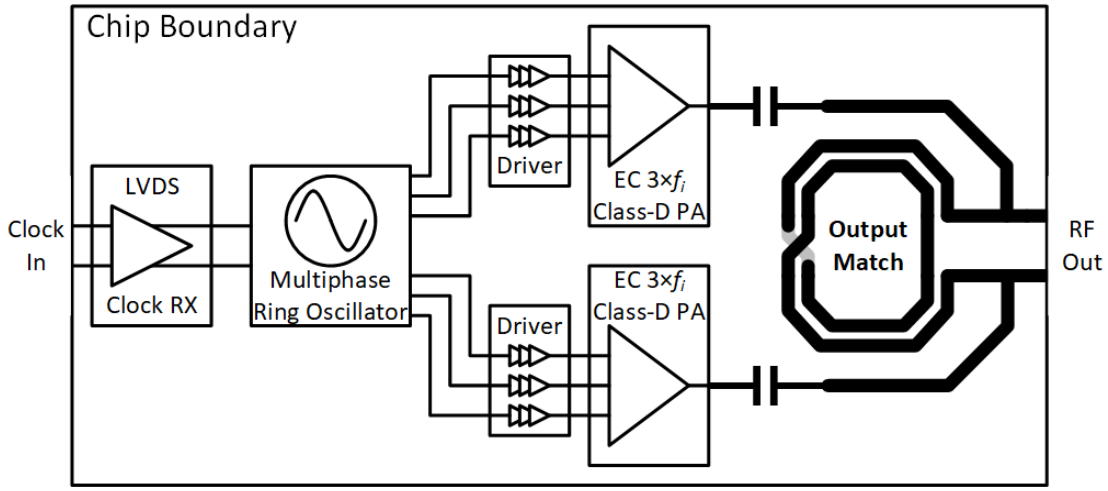


- Single SCPA slice is designed and re-used:
  - Focus on precision timing
  - Optimize one cell and tile it up to desired resolution!
  - No internal analog/RF interfaces!

Tripling EC Class-D PA



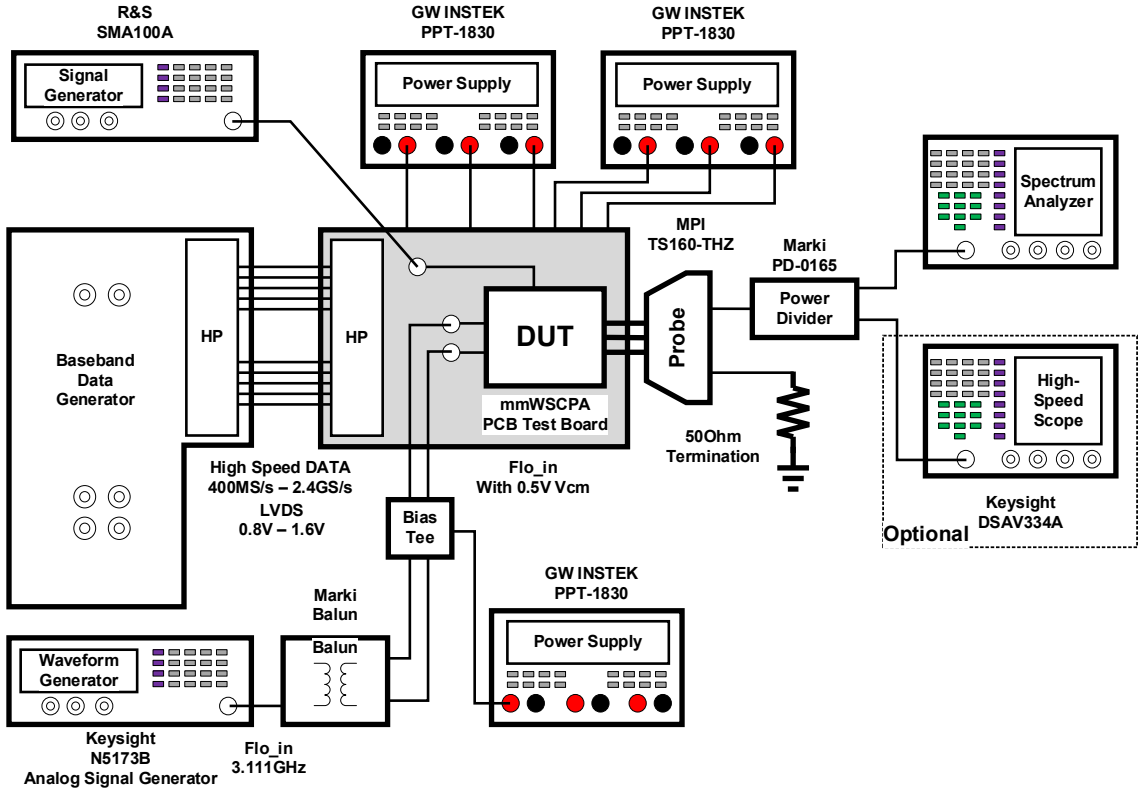


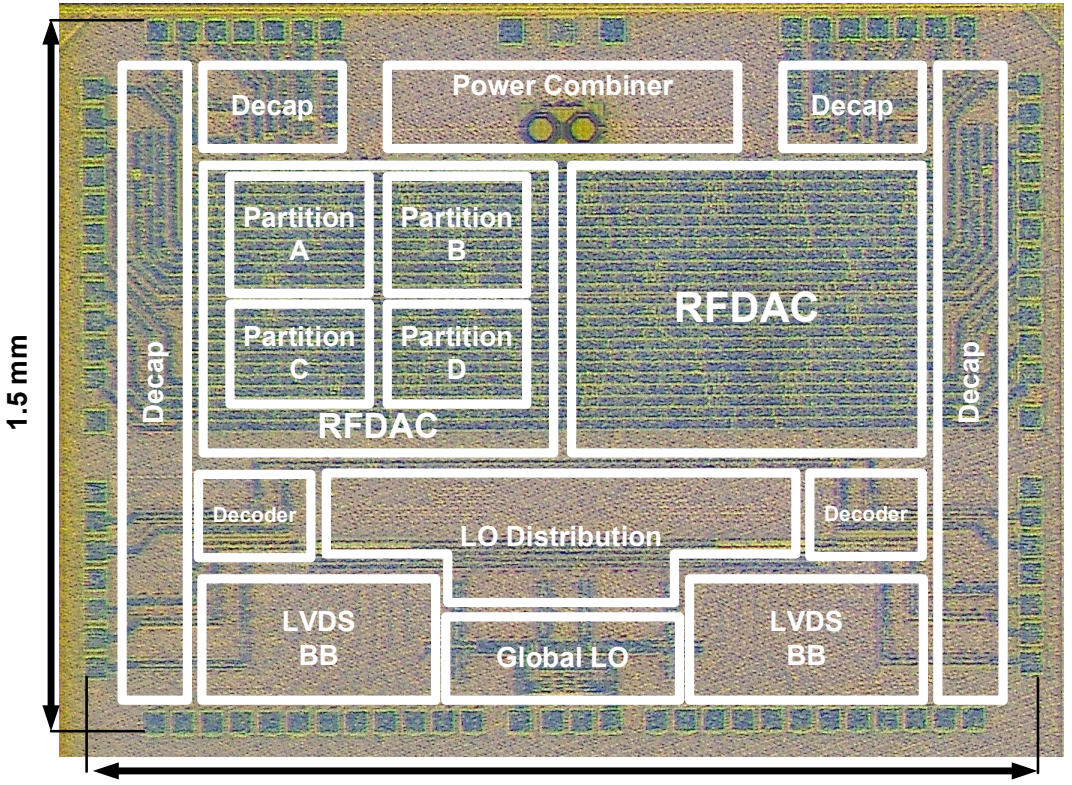


[Nguyen, et. al., accepted to TCAS-2]

- A tripling class-D PA was fabricated to demonstrate potential for Edge-combining
- XOR cell is compacted and reduced to minimize parasitics and save power
- Multiphase signals are generated using multiphase injection locked ring oscillator

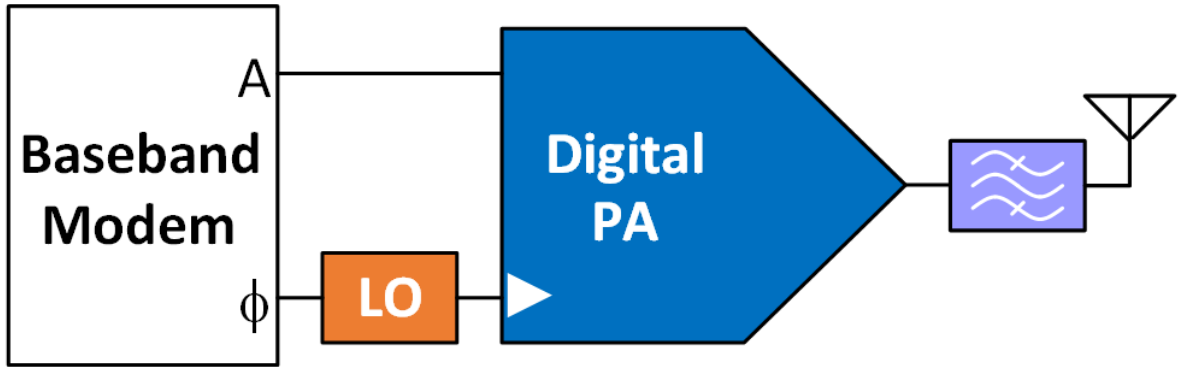
Testbench Setup and Die photo





- The prototype: 2x1.5mm2 on single FDSOI 22nm die
- Output is probed with the T40-THZ MPI
- Chip-on-Board assembly for input signal and power supplies

Digital Power Amplifiers : Polar Amplifiers



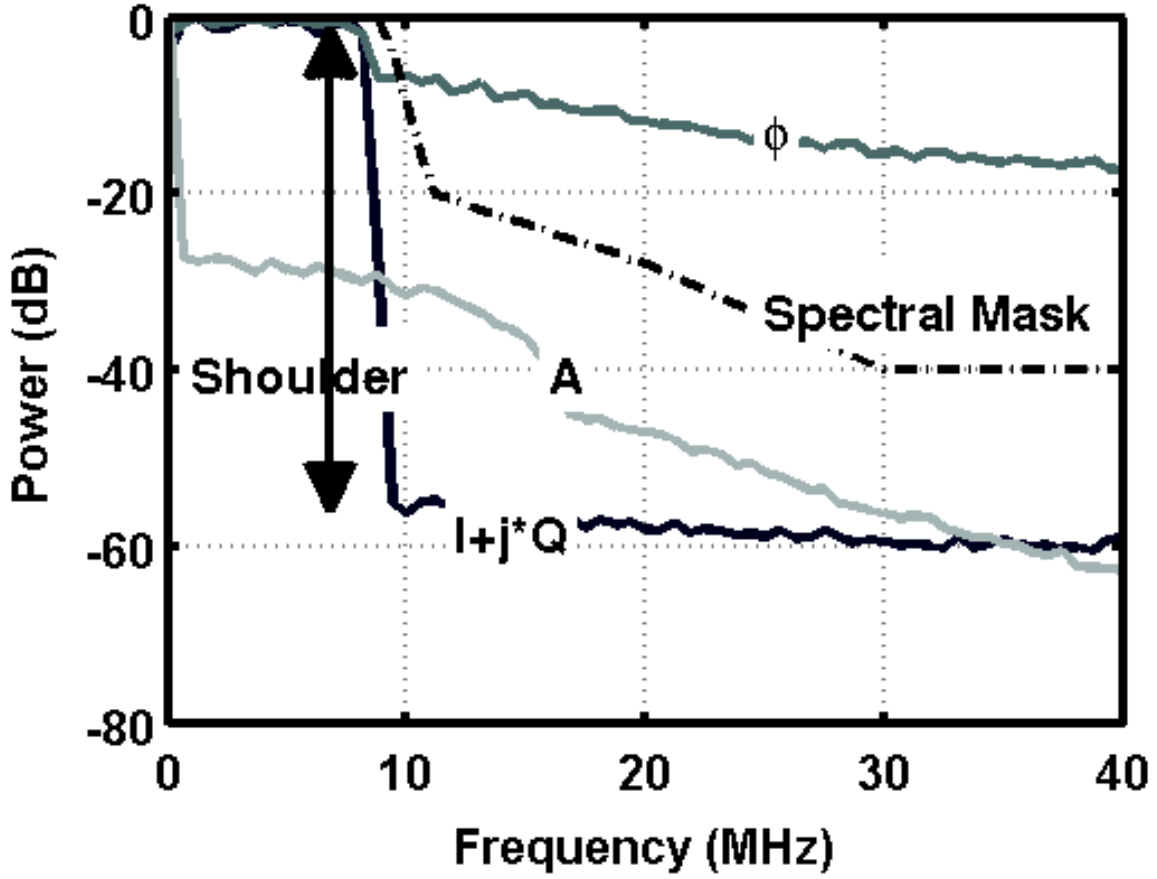
- In a polar RF DAC, inputs are the amplitude code:

$$A(t) = \sqrt{I^2(t) + Q^2(t)}$$

- The phase modulated RF clock/LO:

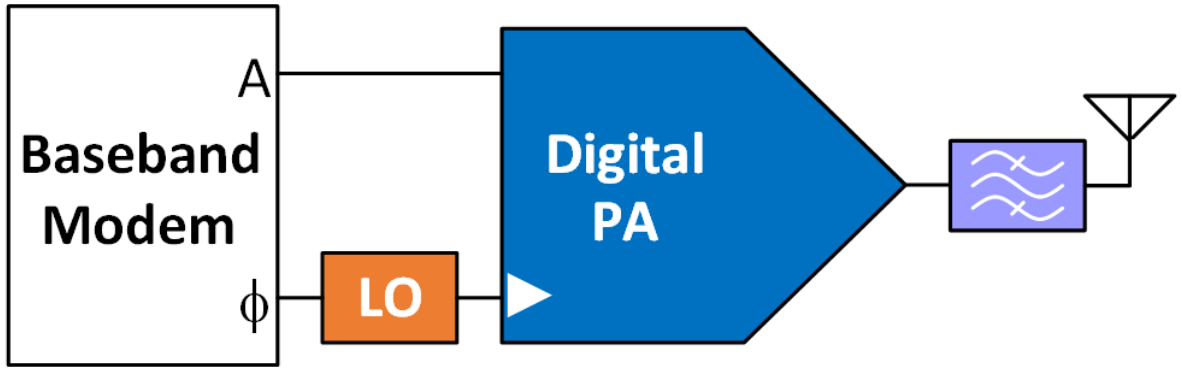
$$\emptyset(t) = tan^{-1}(\frac{Q(t)}{I(t)})$$

- Bandwidth expands due to non-linearity

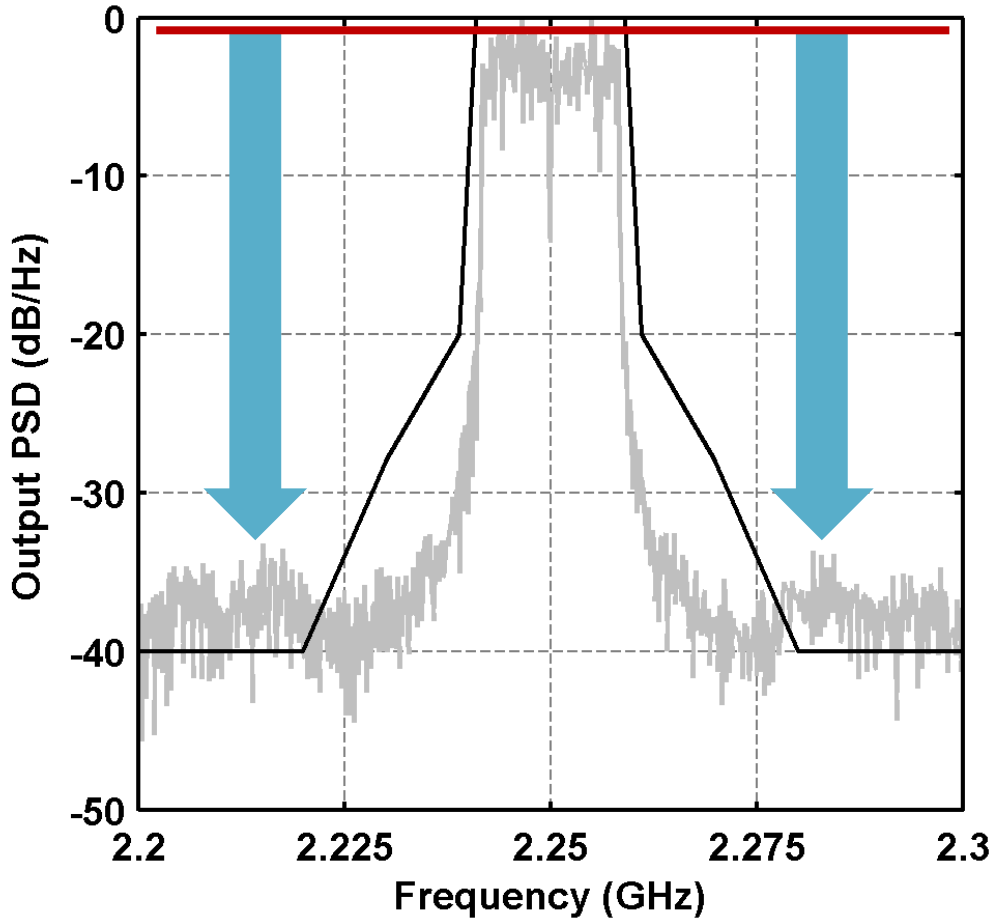


How much signal bandwidth do we need to include?

Polar SCPA: Timing Mismatch $A \rightarrow \phi$



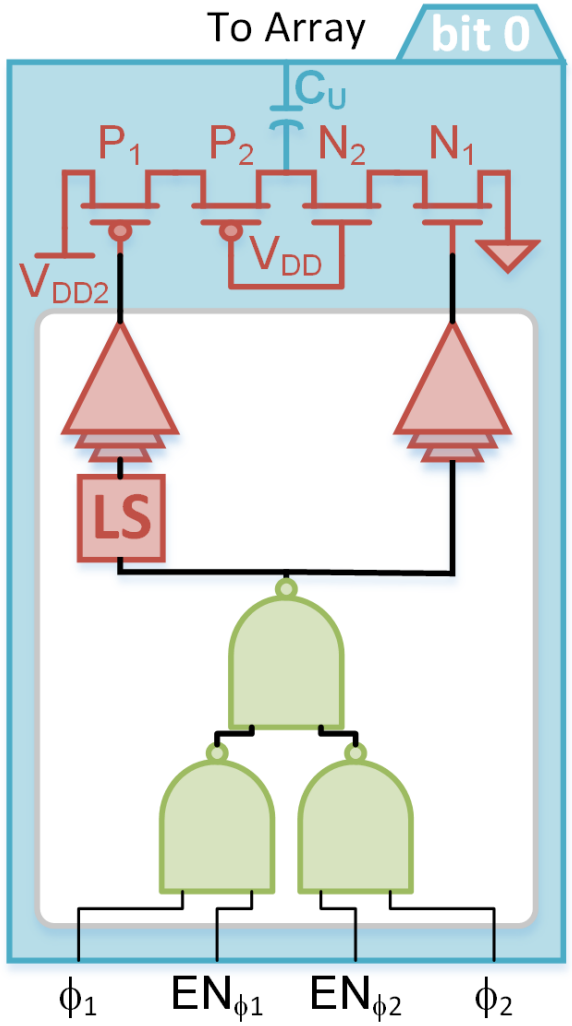
- Delay between A and ϕ leads to spectral distortion
- Distortion can be estimated as 3rd order intermodulation (IM3D):
- $IM3D \cong 2\pi \cdot (BW_{RF} + \Delta\tau)^2$
  - BW_{RF} → Signal Bandwidth
  - $\Delta\tau$ → Delay between A and ϕ



[L. Ye, et. al., JSSC 12/2013]

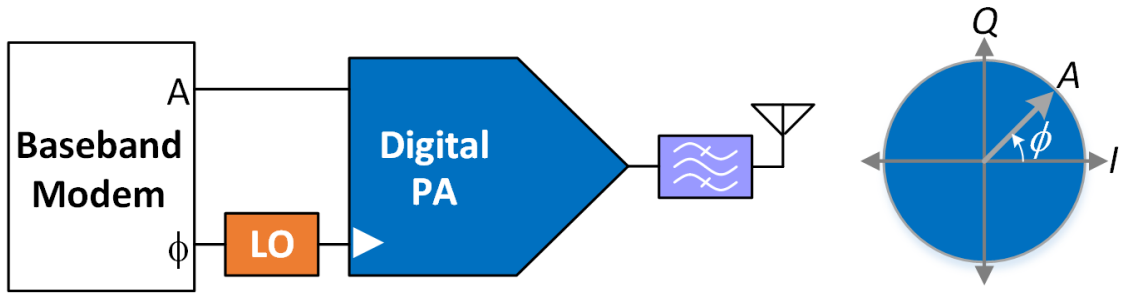
MP-SCPA: Slice modification

- To implement multiphase in an SCPA, only a minor modification to the polar slice:
  - AND gate is replaced by NAND-NAND MUX
  - Logic enforces $EN_{\phi1}$!= $EN_{\phi2}$
- Synthesized decoder modified to enable switching on phase ϕ_1 or ϕ_2, or to ground cell → fine phase interpolation with amplitude control

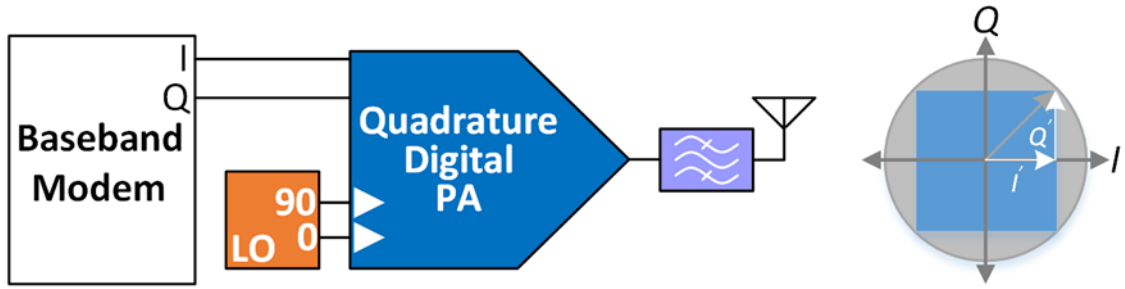


[Jin, et. al., ISSCC 2015]
[Yuan, et. al., JSSC 05/2016]

Polar vs. Cartesian DPA



- ✗ Requires conversions from I,Q Baseband to A,ϕ (CORDIC or Look Up Table)
- ✗ Bandwidth Expansion
- ✗ Delay Mismatch
- ✓ Achieves highest power efficiency



- ✓ No baseband conversions are required
- ✓ No bandwidth expansion
- ✓ No delay mismatch
- ✗ -3dB peak output power compared to Polar → reduced efficiency