Chapter 3. Input PF-Corrected SRM-Based VSD System

3.1 Introduction

One of the unique features of the SRM is it requires only a unipolar current for its four-quadrant operation, thus simplifying the converter topologies. This chapter considers the analysis and design of one such converter with minimum switches. It is the C-dump converter for use in non-bifilar wound SRM drive. The analysis of this topology includes the evaluation of the switching losses of the power switching devices and diodes, their current and voltage stresses, the relationship between the energy storage capacitor, the inductor and the duty cycle of the energy recovery circuit and the efficiency of the overall system for a given switching frequency. From the analysis, a design procedure for the converter circuit is developed. The theoretical analysis and design procedure, both validated with experimental results obtained from a laboratory prototype, are presented in this chapter. The computer simulation is performed to verify the theoretical analysis and experimental results.

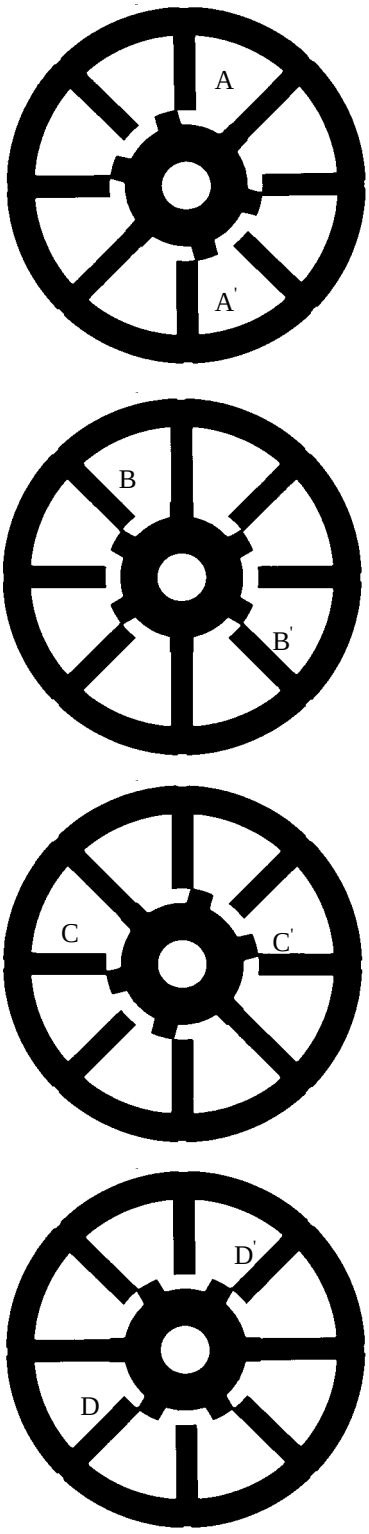
The PFC circuit has been introduced widely in small dc-to-dc power supplies [36-55] and in VSDs [56-63] very recently. The topologies for PFC circuits for small dc to dc power supplies and VSDs are very different. The predominant PFC circuit used in the dc-to-dc power supplies is the single switch boost topology where the power levels rarely exceed 1 kW. Beyond this power level, the bridge configurations are preferred as given in the reference [41]. The single switch boost topology is ideal for the appliance drives as they are quite feasible within the power level of 1 kW and mostly operate from a single-phase utility input. This topology is considered for the appliance VSD in this study. At the end of this chapter the input PF corrected SRM-based VSD system is proposed.

This chapter is constructed as follows. The principle of operation of SRM is introduced in Section 3.2. The C-dump converter which is one of the minimum switch per phase converter family is fully analyzed and experimentally verified with a significant power level in Section 3.3. The controllers developed for C-dump converter based SRM drive system are explained in Section 3.4. The validation of analysis and experimental and simulation results are presented in Section 3.5. The PF corrected SRM drive is proposed and experimental results are analyzed in Section 3.6. The key conclusions are drawn in Section 3.7.

3.2 Principle of Operation of SRM

The SRM operates on the reluctance principle [2, 9]. The reluctance property causes the rotor iron to be attracted in order to align itself to a minimum reluctance position with an applied magnetic field. Therefore, the iron rotor of a SRM rotates to remain aligned with the rotating magnetic field, produced by electronically commutated current through consecutive stator windings.

The SRM has salient rotor and stator poles as shown in Figure 3.1. The number of stator and rotor poles is generally different to ensure that the rotor is not in a position where the potential torque in all phases is zero. One machine phase consists of diametrically opposite stator pole windings which are connected in series. The SRM can operate with the loss of one phase, with reduced output power, which is not possible in other drives employing bridge type converters.



(i) Phase A is ready to be excited.

(ii) Phase A is in aligned position and Phase B is next to be excited.

(iii) Phase B will be turned off and Phase C will be excited.

(iv) Phase C is in aligned position and Phase D will be turned on.

Figure 3.1 Operation of an 8/6 SRM.

The electromagnetic torque of the SRM is produced by switching current into each phase winding in a sequence that is synchronized with rotor position. The expression for the electromagnetic torque of the SRM is the function of motor phase current and position as [2],

$$T_e\left(i_{ph},\theta_r\right)=\frac{1}{2}i_{ph}^2\cdot\frac{dL\left(i_{ph},\theta_r\right)}{d\theta}\ \text{, N·m.} \tag{3.1}$$

In equation (3.1), the torque is equal to the product of the square of the phase winding current and phase inductance slope, which implies that only unipolar current is required for the four quadrant operation of the SRM drive. Because of the squared current, the torque-speed characteristics of the SRM is comparable to the series dc motor at low speed.

The operational example of an 8/6 SRM is as follows [2]: Phase A in Figure 3.1(i) is about to be excited initially by applying current into the winding on stator poles A and A'. The flux is established through stator poles A and A' and adjacent rotor poles, which tends to pull those nearest rotor poles toward the stator poles A and A' in clockwise direction, respectively. When the rotor poles are aligned to the Phase A stator poles, the Phase A current is turned off as shown in Figure 3.1(ii). Now the Phase B is excited pulling another adjacent rotor poles as shown in Figure 3.1(iii). Likewise, consecutive energization of phase C and D result in alignment of stator poles with the adjacent rotor poles as shown in Figure 3.1(iv). It takes four phase energizations in sequence to move the rotor by 60^o in the 8/6 SRM. The switching of currents in the sequence of C-B-A-D results in the reversal of the rotor rotation as seen with the aids of Figures 3.1(i)-(iv).

The ideal single-phase inductance profile of an 250W 8/6 SRM is illustrated in Figure 3.2. Only one rotor pole pitch which is 60^o ranging between $-\theta_{r1}$ and $+\theta_{r1}$ is shown. The maximum inductance, L_a appears at 0^o which is the fully aligned position of rotor and also the minimum reluctance position. By appropriately positioning the phase currents relevant to the rotor position, a four-quadrant operation is obtained [2]. To generate the motoring torque, $+T_e\left(i_{ph},\theta_r\right)$, the phase current is switched on during the rising slope portion of the phase inductance as shown in Figure 3.2. If the phase current is applied on the falling slope portion of the phase inductance, regenerating torque, $-T_e\left(i_{ph},\theta_r\right)$, is produced. To control these operations adequately, the phase current should be switched off in each phase before the rotor poles and stator poles come into the aligned position.

The various rotor positions in Figure 3.2 can be expressed as follows [2]:

$$\left.\begin{aligned}\theta_{r1}&=\frac{\pi}{N_r}\\ \theta_{r2}&=\beta_s\\ \theta_{r3}&=\frac{1}{2}\left(\beta_r-\beta_s\right)\end{aligned}\right\}\ \text{, deg.} \tag{3.2}$$

where,

N_r = number of rotor poles

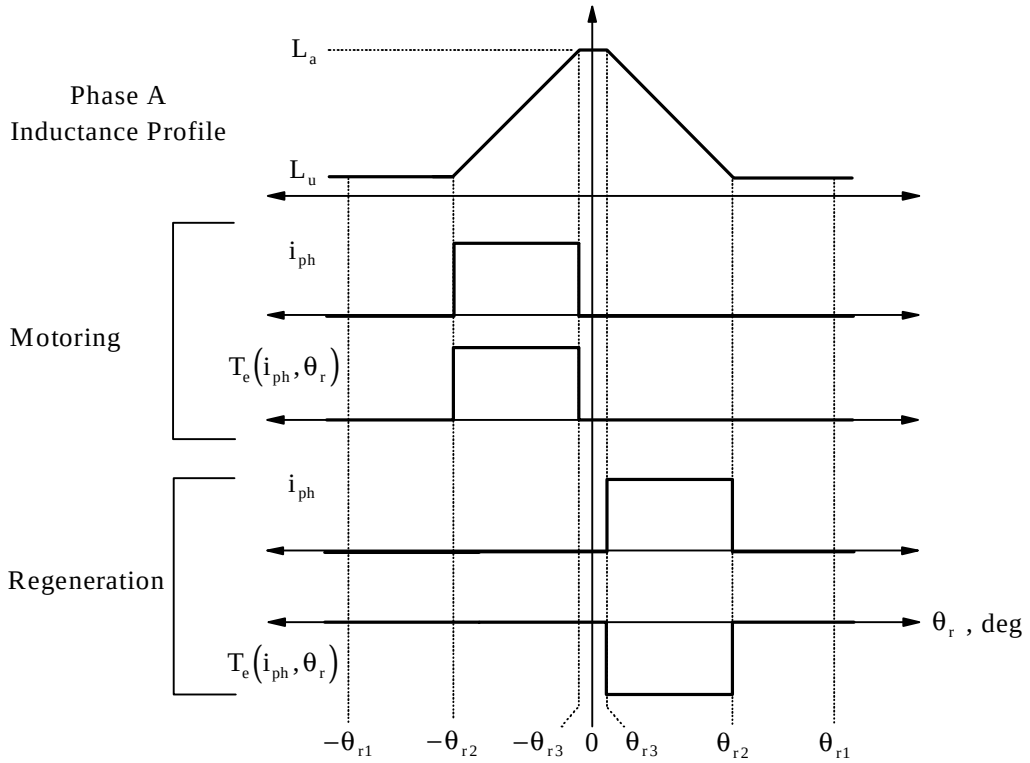


Figure 3.2 Ideal inductance profile and torque generation of the SRM.

β_r = rotor pole arc, deg (mechanical)
β_s = stator pole arc, deg (mechanical)

and these values for a prototype 250W, 8/6 SRM are listed in Appendix B. The corresponding rotor position in the left hand side of the aligned position can also be represented with equation (3.2) with negative sign.

3.3 Analysis and Design of C-Dump Converter-Based SRM Drive

The electromagnetic torque of the SRM is equal to the product of the square of the winding current and inductance slope which implies only a unipolar current is necessary for a four-quadrant operation of the SRM drive as explained in section 3.2. If only unipolar currents are sufficient for the operation, only one switch per phase for its current control is required. This is unlike ac machines which usually require two switches per phase. Many single switch per phase topologies are evolved for the SRM [15, 16, 26-33]. Four typical single switch per phase converter topologies are briefly reviewed in this section. One topology, C-dump converter circuit, is selected among them and will be applied to implementation of SRM- and PMBDC-based VSDs. The analysis of C-dump topology from the viewpoints of computation of switching losses of the power devices, voltage and current stresses and maximum voltage and current ratings of the power devices for a SRM drive of known power rating, ratings of the energy recovery capacitor, inductor and its duty cycle and efficiency of the overall circuit is performed in this section. Based on this analysis, the design procedure for the converter topology is derived.

Experimental results from a laboratory 250W SRM prototype and steady-state simulation of C-dump converter-based SRM drive are used to correlate the theoretical analysis and design procedure.

3.3.1 Overview of Single Switch per Phase Converter Topologies

Figure 3.3 shows the earliest of such a single switch per phase topology requiring a bifilar winding in the SRM [26]. While this is acceptable and feasible in low voltage machines such as for automotive applications, its use in other higher voltage applications is very limited due to the fact that the leakage inductances of the bifilar windings are not absolutely controllable resulting in high transient voltages during the current turn-off instants. These transient voltages could be as high as three to four times the dc link voltage, thus making this configuration unsuitable for higher dc link voltage operated machines.

The dc link voltage can be split into two equal halves to have a single switch per phase topology [15] as shown in Figure 3.4, but it has the drawback of requiring an even phase machine and the input voltage is reduced by half. The reduction in input voltage by half would approximately double the current as compared to the machine with a full dc link voltage input. This increases the losses both in the machine and converter.

The third single switch per phase topology is shown in Figure 3.5 [31]. Although this circuit uses full input dc voltage, but it has the drawback of partially dissipating the stored energy in the braking resistor, R_b, thereby both decreasing the efficiency of the topology and creating a problem in the cooling of the resistor. But in spite of such disadvantages, this topology is suitable for many low cost variable speed applications such as hand tools and appliances requiring only intermittent use.

To overcome the energy dissipation occurring in the R-dump circuit, the partial energy stored in the machine windings is directed to a capacitor for storage. It can subsequently be recovered.

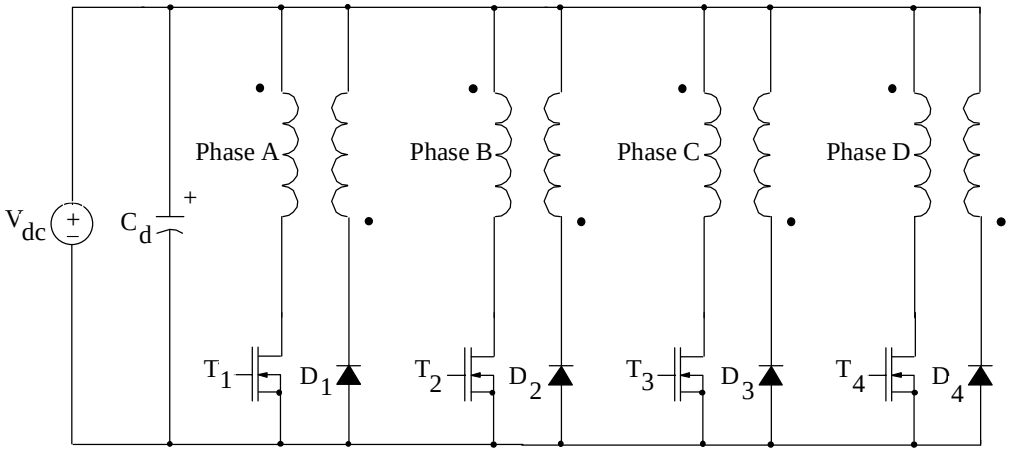


Figure 3.3 Single switch per phase converter for bifilar wound SRM.

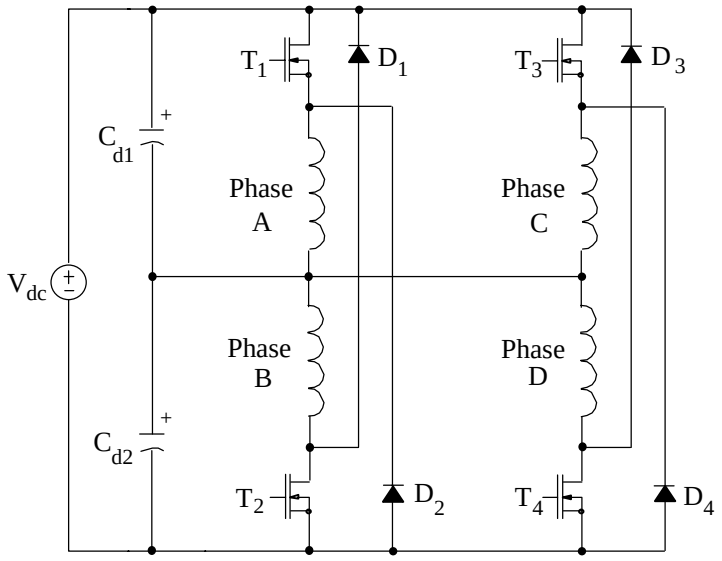


Figure 3.4 Single switch per phase converter with split dc power supply.

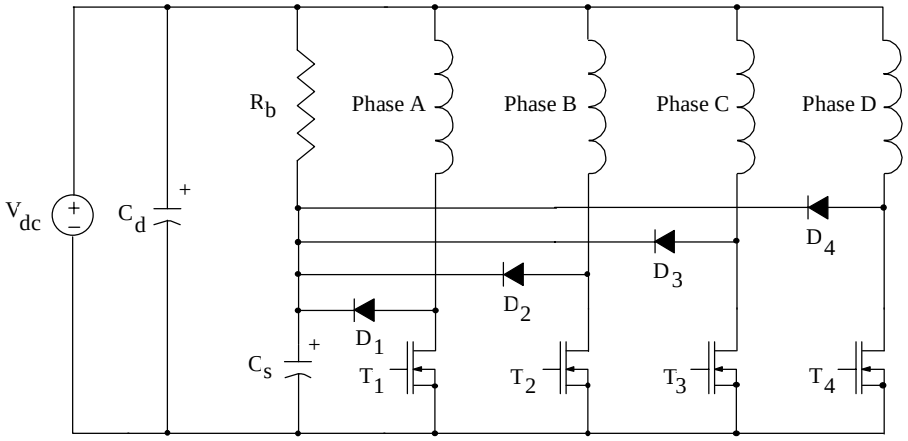


Figure 3.5 Single switch per phase converter with energy dissipating resistor.

Such a circuit is known as the C-dump converter [27]. The schematic diagram of a C-dump converter-based four-phase SRM drive is shown in Figure 3.6. The energy recovery requires an additional switch and a diode. Both the resonant recovery circuit and chopper recovery circuit approach have been described in [27]. The resonant recovery circuit has the drawback of high current and voltage stresses in the recovery switch and diode. Moreover, the operation of this circuit has been analyzed in a limited way with experimental correlation up to only a few watts. The C-dump converter topology has the advantages over the other single switch per phase configurations with the additional benefits of requiring no snubbers for the phase switches as their peak voltages are clamped by the energy storage capacitor, C_o. The voltage of C_o itself is controlled by the duty cycle of the chopper recovery circuit, thereby limiting the voltage stresses of the phase switches. This is a significant advantage compared to the resonant recovery circuit topology. Given these advantages, this topology is worthy of consideration for the SRM drives.

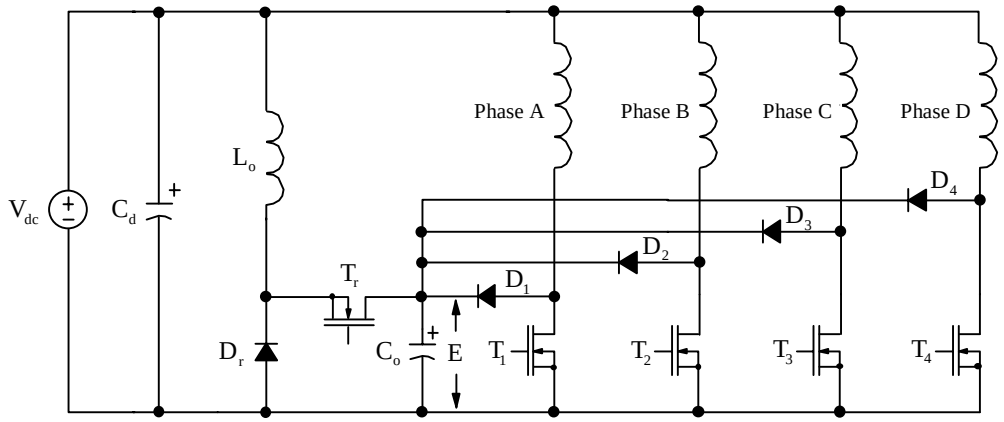


Figure 3.6 Single switch per phase converter with C-dump energy recovery circuit.

The summary of advantages of the C-dump converter topology is as follows:

(i) Single switch per phase topology.
(ii) Only single power supply is sufficient for gate drivers for phase switches because of all the phase switches have a common return.
(iii) Snubberless operations of phase switches are possible by voltage clamping action of the energy recovery circuit.
(iv) Independent control of phase is possible with only one switch per phase.
(v) Four-quadrant operation is possible by simply changing phase firing sequence and position.

The disadvantages of this topology are the low output power per switch VA ratio and the slightly lower system efficiency due to the additional energy recovery power stage.

3.3.2 Principle of Operation of the C-Dump Converter

A simplified single phase equivalent circuit of the C-dump converter-based four phase SRM drive power circuit is shown in Figure 3.7(i). This equivalent circuit is derived from Figure 3.6 under the assumption that all four SRM phases are identical. Figure 3.7(ii) is a symbolic expression of gate drive signals for main phase switch, T_1 and recovery switch, T_r versus current waveforms in motor phase winding, i_{ph} and in energy recovery inductor, i_r. The relationship between duty cycles of the main phase switch and recovery switch is also shown in Figure 3.7(ii). The various salient features labeled in Figure 3.7 will be explained in succeeding analysis section.

The operational modes are defined as illustrated in Figure 3.8(i). The equivalent circuits for defined five operational modes are shown in Figure 3.8(ii). Based on these figures, the operation of the equivalent circuit is described as follows [33]:

(i) When winding of Phase A is to be energized, T_1 is turned on applying the dc link voltage V_{dc} across the winding. Assume T_r is off now and the voltage across C_o is greater than V_{dc}.

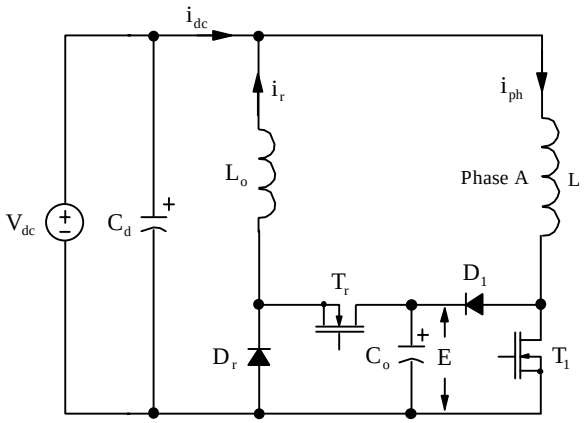


Figure 3.7(i) Equivalent C-dump converter circuit per phase.

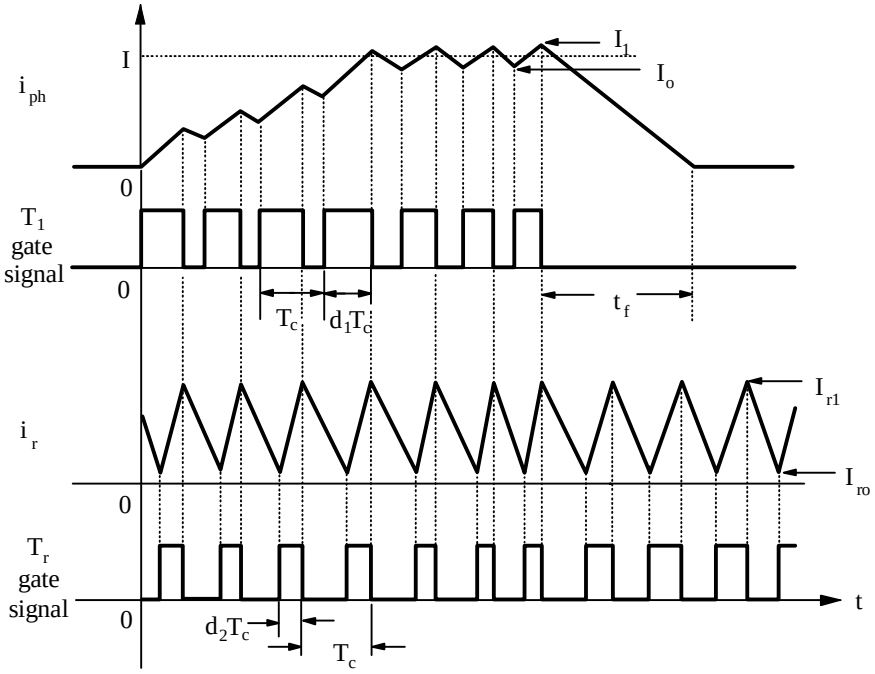


Figure 3.7(ii) Relationships between gate signals and currents.

(ii) Current is established in Phase A winding. If current exceeds the set value, T_1 is turned off. This enables D_1 to be forward-biased and connects C_o to phase winding and the source voltage, V_{dc}.

(iii) Part of the energy is transferred from machine winding to C_o and part to mechanical power. This increases the charge in C_o and hence its voltage, E.

(iv) If the winding current goes below a certain desired value, the phase switch T_1 is turned on again. Then reverse-biased D_1 redirects the current through V_{dc}, Phase A winding and T_r.

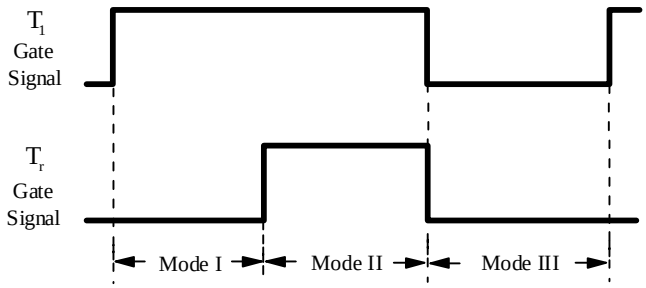
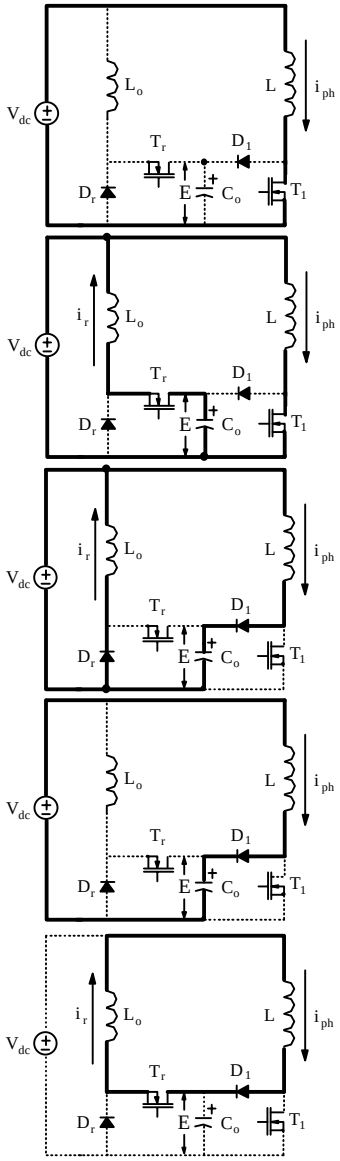


Figure 3.8(i) Definition of operational modes.



Mode I: T_1 on, T_r off

Mode II: T_1 and T_r on

Mode III: T_1 and T_r off

Mode IV: Commutation of a phase

Mode V: T_1 off, T_r on

Figure 3.8(ii) Five modes of operation of a phase.

(v) The excess energy stored in C_o is recovered by enabling T_1 which completes the circuit C_o, T_r, L_o and V_{dc}. T_r is turned off when E is at an acceptable preset level, $V_{dc} + \Delta V_1$ where ΔV_1 is the overvoltage at starting. Turning off T_r when a current flowing is accomplished due to the freewheeling diode D_r.

(vi) The turn off of the phase switch T_1 (or T_2 or T_3 or T_4) and auxiliary energy recovery switch T_r are synchronized to position C_o for receiving energy from machine windings and for independent control of the machine phases.

3.3.3 Analysis of C-Dump Converter-Based SRM Drive

In one switching period, each phase encounters five main modes of operation as shown in Figures 3.8(i) and (ii). The five modes of operation are explained and the respective mode equations are derived in this section [33].

Mode I : T_1 on and T_r off

The dc link voltage is supplying the magnetizing energy to the motor winding in this mode. The equation representing this mode is:

$$L\frac{di_{ph}(t)}{dt} + R \cdot i_{ph}(t) = V_{dc} - e_b . \tag{3.3}$$

From the above equation, the current during this period can be expressed as,

$$i_{ph}(t) = \frac{V_{dc} - e_b}{R} \cdot \left(1 - e^{-t/\tau_1}\right) + I_o \cdot e^{-t/\tau_1} \text{ , A.} \tag{3.4}$$

where

$$\tau_1 = \frac{L(i,t)}{R} \text{ , s.} \tag{3.5}$$

$$R = R_{ph} + R_{T_1}(on) \text{ , } \Omega. \tag{3.6}$$

$$e_b = \omega_m \cdot i_{ph}(t) \cdot \frac{dL(i,\theta)}{d\theta} \text{ , V.} \tag{3.7}$$

$L(i, \theta)$ is the motor winding inductance per phase, ω_m is the motor speed in rad/s, R_{ph} is the motor winding resistance per phase, $R_{T1}(on)$ is the on resistance of MOSFET switch T_1, I_o is the minimum phase current and θ is the rotor angle. Note that L, e_b, and τ_1 are current and time dependent because of rotor function and hence the initial current is time dependent. If the

winding resistance and the on resistance of the phase switch are neglected and assume that the phase current varies linearly, then the maximum and the minimum phase currents are given by:

$$I_1 = I_o + \frac{V_{dc} - e_b}{L} \cdot t_1 \text{ , A.} \tag{3.8}$$

$$I_o = I_1 - \frac{E + e_b - V_{dc}}{L} \cdot t_2 \text{ , A.} \tag{3.9}$$

$$\left.\begin{aligned} t_1 &= d_1 \cdot T_c \\ t_2 &= (1 - d_1) \cdot T_c \\ T_c &= 1/f_c \end{aligned}\right\} \text{ , s.} \tag{3.10}$$

where t_1 is the on time and t_2 is the off time of the phase switch in each PWM cycle, and f_c is the PWM carrier frequency in Hz. Equations (3.8), (3.9) and (3.10) can be combined to find the average duty cycle of the phase switch if the induced emf during on and off durations in a PWM cycle is approximately equal. Then the duty cycle d_1 is

$$d_1 = \frac{E - V_{dc} + e_{b2}}{E}$$

$$= h + \frac{e_{b2}}{E}. \tag{3.11}$$

where

$$h = \frac{E - V_{dc}}{E}. \tag{3.12}$$

and e_{b2} is the induced emf during the off time in a PWM cycle. It can be approximated as

$$e_{b2} = \omega_m \cdot I \cdot k(\theta) \text{ , V.} \tag{3.13}$$

where I is the average phase current in a PWM cycle, and

$$k(\theta) = \frac{dL(i,\theta)}{d\theta}. \tag{3.14}$$

If E is defined to be equal to base voltage V_b as

$$\left.\begin{aligned} E = V_b &= k(\theta)\cdot I_b \cdot \omega_{mb} \\ k(\theta) &= \frac{L_a - L_u}{\theta_{rp}/q} \end{aligned}\right\} \tag{3.15}$$

where

$$\left.\begin{aligned} \theta_{rp} &= \frac{2\pi}{P_r} \\ q &= \frac{P_s}{2} \end{aligned}\right\} \tag{3.16}$$

I_b is the base current, L_a and L_u are the aligned and unaligned inductances, respectively, ω_{mb} is the base speed, P_r is the number of rotor poles and P_s is the number of stator poles.

By substituting (3.15) in (3.13) and then in (3.11), and taking the average, we have the normalized expression of d_1 as,

$$d_1 = h + \omega_{mn} \cdot I_n \,. \tag{3.17}$$

where

$$\omega_{mn} = \frac{\omega_m}{\omega_{mb}} \text{ , pu.} \tag{3.18}$$

$$I_n = \frac{I}{I_b} \text{ , pu.} \tag{3.19}$$

The equation (3.17) clearly brings out the relationship between the energy storage capacitor voltage, dc link voltage, speed, phase current and the duty cycle of the phase switch. If speed increases, d_1 has to be increased if h is maintained constant. Note that in practical applications, h is a constant, and may be in the range of 0.2 to 0.3. From this equation, the impact of increasing E becomes evident. Increasing E, increases h and, hence, for a given maximum duty cycle and current, the maximum machine speed will decrease. This sets the limit on maximum speed of operation. So it is preferable to keep h at the minimum level. This will have other consequences as derived later. The maximum speed for 1 pu current is

$$\omega_{mn}(max) = d_1(max) - h(min) = (1-h) \text{ , pu.} \tag{3.20}$$

Mode II and III : T_1 and T_r both on and then off

The energy recovery switch is turned on after T_1 starts conducting. This indicates the transfer of the energy from capacitor C_o to the dc source and inductor L_o. The equations describing this mode of operation are

$$V_{dc} + R_o \cdot i_r + L_o \cdot \frac{di_r}{dt} = \begin{cases} E\ , & 0 < t < d_2 \cdot T_c \\ 0\ , & d_2 \cdot T_c < t < T_c \end{cases} \tag{3.21}$$

from which the current during on time of T_r is evaluated as,

$$i_r(t) = I_{ro} \cdot e^{-t/\tau_r} + \frac{E - V_{dc}}{R_o} \cdot (1 - e^{-t/\tau_r})\ ,\ 0 < t < d_2 \cdot T_c\ . \tag{3.22}$$

where I_{ro} is the minimum recovery current which becomes zero in the discontinuous current mode as shown in Figure 3.8(ii), R_o is the resistance of the energy recovery inductor, and its inductance is L_o giving,

$$\tau_r = \frac{L_o}{R_o}\ . \tag{3.23}$$

The equation for the current in the inductor, when T_r is off, is

$$i_r(t') = -\frac{V_{dc}}{R_o} \cdot (1 - e^{-t'/\tau_r}) + I_{r1} \cdot e^{-t'/\tau_r}\ ,\quad d_2 \cdot T_c < t < T_c\ . \tag{3.24}$$

where

$$t' = (1 - d_2)T_c\ . \tag{3.25}$$

and I_{r1} is the maximum recovery current. The duty cycle d_2 is variable and is determined by a feedback circuit to keep voltage across C_o constant as illustrated in Figure 3.7.

The machine phase current equation during T_1 on is similar to equation (3.4) in Mode I. During turn off, the phase current becomes

$$i_{ph}(t) = \frac{(E - V_{dc})}{R_{ph}} \left(1 - e^{-\frac{t}{\tau_{ph}}} \right) + I_o \cdot e^{-\frac{t}{\tau_{ph}}}\ \text{, A.} \tag{3.26}$$

where $\tau_{ph} = \dfrac{L}{R_{ph}}$.

Mode IV : Phase current commutation

In this mode, the current in the machine phase has to be brought to zero. During this time, the switch T_1 is turned off and the energy in the machine is partially transferred to the capacitor C_o, as shown in Figure 3.7. Let the time required to bring the current from i_1 to zero is t_f as shown in

Figure 3.8(ii). Then we have the phase current expression from equation (3.26), by substituting $t = t_f$ and $\tau_{ph} = \tau_x$,

$$i_{ph}(t) = \frac{(E - V_{dc})}{R_{ph}}\left(1 - e^{-\frac{t_f}{\tau_x}}\right) + I_o \cdot e^{-\frac{t_f}{\tau_x}} \text{ , A.} \tag{3.27}$$

Let $i_{ph}(t)=0$, and solve equation (3.27) for t_f, and then combine with equation (3.11),

$$t_f = \tau_x \cdot ln\left[1 + \frac{I \cdot R_{ph}}{h \cdot E}\right] \text{ , s.} \tag{3.28}$$

where

$$\begin{aligned} \tau_x &= \frac{L(t)}{R_{ph} + k(\theta) \cdot \omega_m} \\ &\cong \frac{L(t)}{k(\theta) \cdot \omega_m} \text{ , s.} \end{aligned} \tag{3.29}$$

if turn off is attempted during increasing inductance region. If machine inductance is constant and equal to its aligned value L_a, then

$$\tau_x \cong \frac{L_a}{R_{ph}} \text{ , s.} \tag{3.30}$$

From equation (3.28), it is clearly seen the commutation time is reduced with increasing h and speed.

The voltage increment in C_o, during this mode may be written as,

$$\Delta V_o = \frac{1}{C_o}\int\left(i + \frac{h \cdot E}{L_a} \cdot t\right)dt \text{ , V.} \tag{3.31}$$

Note the maximum value of ΔV_o is chosen for selecting the devices. The maximum value of ΔV_o is when i is equal to I, and t is equal to half of the switching frequency f_c, giving the maximum ΔV_o as,

$$\Delta V_o(max) = \frac{I}{C_o} \cdot \frac{1}{2 f_c} + \frac{h \cdot E}{2 C_o \cdot L_a} \cdot \frac{1}{4 f_c^2} \text{ , V.} \tag{3.32}$$

As this has to be restricted, the proper selection of E, C_o and f_c has to be coordinated for design. Expressing equation (3.32) in normalized units,

$$\Delta V_{on}(max) = \frac{I_n}{C_{on}} \cdot \frac{\pi}{f_{cn}} + \frac{\pi^2}{2} \cdot \frac{h \cdot E_n}{C_{on} \cdot L_{an} \cdot f_{cn}^2} \text{ , pu.} \tag{3.33}$$

where

$$\left.\begin{aligned} V_{on} &= V_o / V_b \text{ , } \quad V \\ V_b &= Z_b I_b \text{ , } \quad V \\ I_n &= I / I_b \text{ , } \quad pu \\ f_{cn} &= f_c / f_b \text{ , } \quad pu \\ C_{on} &= C_o / C_b \text{ , } \quad pu \\ E_n &= E / V_b \text{ , } \quad pu \\ L_{an} &= L_a / L_b \text{ , } \quad pu \\ L_b &= Z_b / 2\pi f_b \text{ , } \quad H \end{aligned}\right\} \tag{3.34}$$

V_b is the base voltage in V, I_b is the base current in A, f_b is the base frequency in Hz, C_b is the base capacitance in F, L_b is the base inductance in H and Z_b is the base impedance in Ω.

Mode V : Commutation mode with T_r on

In this mode, the current circulates through the machine phase, T_r and L_o, partially transferring the energy from the machine to the inductor L_o. The energy stored in L_o is transferred to dc source when T_r is turned off. This mode hence prevents all the energy transfer to the capacitor C_o. The expression for current in this mode is given as, if the starting current for this mode is i_3,

$$i(t) = i_3 \cdot e^{-t/\tau_y} \text{ , A.} \tag{3.35}$$

where

$$\tau_y = \frac{L_o + L(t)}{k(\theta) \cdot \omega_m} \text{ , s,} \tag{3.36}$$

and the inductance is rising. If the machine inductance is constant then,

$$\tau_y = \frac{L_o + L}{R_1} \text{ , s.} \tag{3.37}$$

3.3.4 C-Dump Converter Power Circuit Design

The SRM's average phase current is I and it has m phases. The ratings of the phase switches, diodes, and recovery switch and diode are derived from the previous analysis and given in Tables 3.1 and 3.2. Note the average recovery current is expressed as,

$$I_r = \frac{(I_{r1} + I_{ro})}{2} \text{ , A.} \tag{3.38}$$

The switching energy due to the reverse recovery charge in a diode is

$$E_{rr} = V_R \cdot Q_{rr} \text{ , J.} \tag{3.39}$$

where V_R is the maximum dc reverse voltage and Q_{rr} is the total reverse recovery charge in

Table 3.1
Ratings for key components in C-dump converter-based SRM drive.

Device	**Duty Cycle**	**Ratings**		
		Voltage	**Current**	
			Peak	**RMS**
Phase switch	d_1	$E + \Delta V_o$	I_1	$\frac{\left(I_1\sqrt{d_1}\right)}{\sqrt{m}}$
Phase diode	1- d_1	$E + \Delta V_o$	I_1	$\frac{\left(I_1\sqrt{1-d_1}\right)}{\sqrt{m}}$
Recovery switch	d_2	$E + \Delta V_o$	I_{r1}	$I_{r1}\sqrt{d_2}$
Recovery diode	1- d_2	$E + \Delta V_o$	I_{r1}	$I_{r1}\sqrt{1-d_2}$
C_o	1	$E + \Delta V_o$	I_1	$I_{r1}\sqrt{d_2}$
L_o	d_2	$E + \Delta V_o - V_{dc}$	I_{r1}	$I_{r1}\sqrt{d_2}$

Table 3.2
Losses for key components in C-dump converter-based SRM drive.

Device	**Duty Cycle**	**Losses**	
		Conduction	**Switching**
Phase switch	d_1	$\frac{d_1}{m} \cdot I_1^2 \cdot R_{T_1}(on)$	$\frac{1}{2} E \cdot I_1 \cdot f_c(t_r + t_f)$
Phase diode	1- d_1	$\frac{(1-d_1)}{m} \cdot I_1 \cdot V_f$	$\frac{(1-d_1)}{m} \cdot E_{rr} \cdot f_c$
Recovery switch	d_2	$d_2 \cdot I_{r1}^2 \cdot R_{T_r}(on)$	$\frac{1}{2} I_{r1} \cdot E \cdot f_c(t_r + t_f)$
Recovery diode	1- d_2	$I_{r1} \cdot (1-d_2) \cdot V_f$	$E_{rr} \cdot f_c$
C_o	1	$I_1^{\,2} \cdot \frac{d_1(1-d_1)}{m} \cdot ESR$	$I_{r1}^2 \cdot d_2 \cdot (1-d_2) \cdot ESR$
L_o	d_2	$d_2 \cdot I_{r1}^2 \cdot R_o$	—

diodes. *ESR* is the Equivalent Series Resistance of C_o and V_f is the forward voltage drop in diodes.

Phase Switches

The phase switch has to be rated for a maximum duty cycle of 1. The ripple in the current is neglected. Note that based on the application, the average d_1 can be estimated from equation (3.17).

Phase Diodes

Although it is not the case in practice the diodes have to be rated for a maximum duty cycle of 1 as in the case of the phase switches for the worst case scenario.

Incremental Voltage Rise in C_o

Considering the average current of the machine phase as I and the current ripple is small, the incremental voltage rise in C_o during the turn-off of T_1 is approximated as,

$$\begin{aligned}\Delta V_o &\cong \frac{1}{C_o}\cdot I\cdot t_{off}\\ &= \frac{1}{C_o}\cdot I\cdot(1-d_1)\cdot T_c\\ &= \frac{(1-d_1)}{f_c}\cdot\frac{I}{C_o}\ \text{, V.}\end{aligned} \tag{3.40}$$

Expressed in normalized units, this incremental voltage rise in C_o is ΔV_{on} and given by,

$$\begin{aligned}\Delta V_{on} &= \frac{\Delta V_o}{V_b} = \frac{(1-d_1)}{f_c}\cdot\frac{(I/I_b)}{C_o\cdot Z_b}\\ &= \frac{(1-d_1)}{f_c}\cdot\frac{I_n}{C_o\cdot(1/2\pi f_b C_b)}\\ &= \frac{2\pi(1-d_1)\cdot I_n}{C_{on}\cdot f_{cn}}\ \text{, pu.}\end{aligned} \tag{3.41}$$

From this expression, the energy recovery capacitor's value is obtained based on the minimum value of d_1, maximum value of I_n and desired value of ΔV_{on} given with a fixed f_{cn} as,

$$C_{on} = 2\pi\cdot\frac{I_n}{\Delta V_{on}}\cdot\frac{[1-d_1(min)]}{f_{cn}}\ \text{, pu.} \tag{3.42}$$

where $d_1(min)$ corresponds to the no-load duty-cycle.

Incremental Current in Machine Phases

During on time of machine phase switches, the current rises from I_o to I_1 providing an incremental rise of Δi with the application of dc link voltage to machine phases. Neglecting resistances of the machine phase and the switching devices, the following approximate relationship is evident for this condition:

$$L \cdot \Delta I = V_{dc} \cdot d_1 \cdot T_c - I \cdot \Delta L \,. \tag{3.43}$$

where L is the inductance at turn-on. Expressing this in terms of normalized units,

$$\Delta I_n = \frac{\left(\dfrac{2\pi d_1 \cdot V_{dcn}}{f_{cn}} - I_n \cdot \Delta L_n \right)}{L_n} \text{, pu.} \tag{3.44}$$

where

$$\left.\begin{aligned} V_{dcn} &= V_{dc}/V_b \\ \Delta L_n &= \Delta L/L_b \\ \Delta I_n &= \Delta I/I_b \end{aligned}\right\} \text{, pu.} \tag{3.45}$$

This current ripple in the machine phases influences the torque pulsations and hence its magnitude is an important parameter in the SRM drive system.

Switching Frequency

The switching frequency affects both ΔV_{on} and ΔI_n, as seen from equations (3.40) and (3.43). By rearranging both equations in terms of d_1, we have

$$d_1 = 1 - \frac{\Delta V_{on} \cdot C_{on} \cdot f_{cn}}{2\pi I_n}, \tag{3.46}$$

from equation (3.40). And from equation (3.43),

$$d_1 = \frac{\Delta I_n \cdot L_n \cdot f_{cn} + I_n \cdot \Delta L_n \cdot f_{cn}}{2\pi V_{dcn}}. \tag{3.47}$$

Hence, the minimum switching frequency is derived by canceling out d_1 from these two expressions resulting in,

$$f_{cn} = \frac{2\pi}{\left\{\frac{C_{on} \cdot \Delta V_{on}}{I_n} + \frac{1}{V_{dcn}}\left[L_n \cdot \Delta I_n + I_n \cdot \Delta L_n\right]\right\}} \text{ , pu} \tag{3.48}$$

All the relevant variables of the machine, energy recovery circuit, operating current, dc link voltage, current and voltage increments are related to the switching frequency. The design value for f_{cn} is chosen for maximum values of I_n, V_{dcn} and minimum values of ΔV_{on}, L_n, and ΔI_n. Conveniently choosing I_n and V_{dcn} to be 1 pu, the normalized minimum switching frequency is given by,

$$f_{cn} = \frac{2\pi}{\left[C_{on} \cdot \Delta V_{on} + L_n \cdot \Delta I_n + I_n \cdot \Delta L_n\right]} \text{ , pu.} \tag{3.49}$$

The smaller the value of voltage and current increments derived, f_{cn} will be larger. That could be offset by increasing the energy recovery capacitor and in the design stage of the machine by increasing the minimum inductance, i.e., corresponding to the unaligned position of the machine stator and rotor poles and maximizing the incremental inductance in the machine. Selected f_{cn} is often more than this minimum value for reasons of ripple torque and noise minimization.

Value of L_o

L_o follows based on the ripple requirement in i_r. If we assume the required ripple current is Δi_r, then during T_r on,

$$\left(E - V_{dc}\right) = L_o \cdot \frac{\Delta i_r}{d_2 \cdot T_c}. \tag{3.50}$$

By combining equations (3.11) and (3.50), L_o is given by

$$L_o = \frac{d_2 \cdot T_c \cdot h \cdot E}{\Delta i_r} = \frac{d_2 \cdot h \cdot E}{f_c \cdot \Delta i_r} \text{ , H.} \tag{3.51}$$

In normalized units, this inductor is L_{on} and given by,

$$L_{on} = 2\pi \cdot \frac{h}{f_{cn}} \cdot \frac{E_n}{\Delta i_{rn}} \cdot d_2 \text{ , pu.} \tag{3.52}$$

where,

$$\left.\begin{aligned} \Delta i_{rn} &= \Delta i_r / I_b \\ L_{on} &= L_o / L_b \end{aligned}\right\} \text{ , pu.} \tag{3.53}$$

and d_2 has to be calculated for a maximum of 0.5.

Recovery Current

The recovery current in L_o is found by equating the charging and discharging energy in C_o as,

$$(E - V_{dc}) \cdot d_2 \cdot T_c \cdot I_r = E \cdot I \cdot (1 - d_1) \cdot T_c . \tag{3.54}$$

It is approximately given by neglecting the losses in the inductor and T_r as,

$$h \cdot E \cdot d_2 \cdot T_c \cdot I_r = E \cdot I \cdot (1 - d_1) \cdot T_c . \tag{3.55}$$

from which

$$I_r = \frac{(1 - d_1)}{d_2} \cdot \frac{I}{h} \text{ , A.} \tag{3.56}$$

Note d_2 can at utmost be equal to d_1 and the recovery current magnitude is influenced by *I*, *h* and d_1. Note the recovery current identifies the VA rating of this subsystem circuit. Higher values of *h* are preferable in the design to minimize I_r and that would minimize the operational speed range as seen from expressions (3.17) and (3.20). A design trade-off is inevitable between the conflicting choices. Further, it must be noted higher *h* values also increase the switch and diode voltage ratings and preferably should not end in the switch voltage rating to go from 500 V to say 1000 V which could incur a severe cost penalty. These considerations, along with maximum speed of operation, have to be kept in perspective in the choice of *h* which invariably affects I_r and other parameters.

The recovered energy circulates through the converter and machine resulting in increased losses in machine windings, switches and circuit passive components due to increased phase current. This is the cause for increased VA rating of the converter and for a slight drop in efficiency compared to two switches per phase converter-based SRM drive system. The rating of the recovery circuit switch and its cooling play a critical role in the design of this converter circuit.

Design Example

Based on the above derivations, the device current ratings are chosen from the SRM's phase current *I*. Their voltage ratings are chosen based on *h* and hence *E*. The choice of *E* was made to be $2V_{dc}$ in prototype development giving a *h* of 0.5. The selection is motivated because the current commutation in the phase was obtained with a voltage of $-V_{dc}$, very much like the two switches per phase configuration and still kept the switch voltage ratings at less than 400V. This allowed no cost penalty for the diodes and switches because there is very little price difference between 250V, 300V and 400V devices at peak currents of 4A. The range of speed at 0.5 pu current comes to 1 pu and beyond it note the current is decreased to extend the speed range and to deliver the rated output.

For the given machine, with $\Delta I_n = 0.1\ pu$, $\Delta L_n = 0.001\ pu$ and $\Delta V_{on} = 0.01\ pu$, f_{cn} is calculated to be 185 pu by equation (3.49) and 284 pu was chosen for implementation. Note

ΔV_{on}, calculated using an f_{cn} of 284 pu gives 0.0033 pu, is within the assumed value of 0.01 pu. The value of the energy recovery inductor is based on the ripple current of 0.75 pu and is given to be 1.57 mH and hence 2 mH was chosen conservatively for implementation. All of the above completes the design of the power circuit. The base values and other system parameters of the prototype SRM drive are listed in Table 3.3.

Table 3.3
Base values and system parameters of the prototype SRM drive.

Base Values	
Speed, ω_{mb}	398rad/s
Frequency, $f_b = \omega_{mb} / 2\pi$	63.34Hz
Voltage, V_b	340V
Current, I_b	4A
Inductance, L_b	0.2135H
Capacitance, C_b	29.5μH
Impedance, Z_b	85Ω

System Parameters	
Switching Frequency	18kHz
Recovery Voltage, E	340V
$h = (E-V_{dc})/E$	0.5
Recovery Capacitor, C_o	100μF
Recovery Inductor, L_o	2mH
Aligned Inductance @I_b , L_a	0.0572H
Unaligned Inductance @I_b , L_u	0.00134H

3.4 Development of Controllers for the C-Dump Converter-Based SRM Drive System

In this section, the development procedure of a single-quadrant controller which consists of main and auxiliary PWM control circuits for C-dump converter-based SRM drive is explained. Even though only speed control loop is employed in main PWM control circuit, the detailed design process of the current and speed controllers are also introduced. The design results are verified with experiment and simulation.

3.4.1 Unified Design Procedure for PI Speed and Current Controllers for VSD Systems

A simplified block diagram of the C-dump converter-based SRM drive is shown in Figure 3.9. The proposed SRM drive system consists of a C-dump converter which is shown in Figure 3.6, its control circuit consists of the main and auxiliary PWM controllers, a four phase SRM with an 8-bit absolute encoder. This section is concerned with the design procedures of PI speed and current control circuits for the VSD system. A simplified block diagram of the generalized VSD system with speed and current loops is illustrated in Figure 3.10 [1]. The operation of a VSD system with speed and current control loops is as follows: the speed command, ω_r^*, is compared with the sensed speed feedback signal, ω_r, and applied to the speed PI controller. The output of the PI speed controller is the current command, i_a^*. The current error signal which is the difference between the commanded and the sensed current becomes the control voltage, V_c through PI current controller circuit. V_c is converted to a PWM switching signal and applied to the converter. The output of the converter block is the motor voltage, V_a, which is applied to the motor winding.

The inner current loop governs the performance of the closed loop VSD system because its bandwidth is wider than the one in the outer speed loop. The wide bandwidth of the current loop ensures the stable operation and fast dynamic response of the VSD system. The current feedback gain, H_c, has a constant value unless a low pass filter which represents similar transfer function as a filter in speed feedback loop is used.

Each functional block is represented with its own transfer function and summarized in Table 3.4. The details on derivation and reduction of each transfer function can be found in [1].

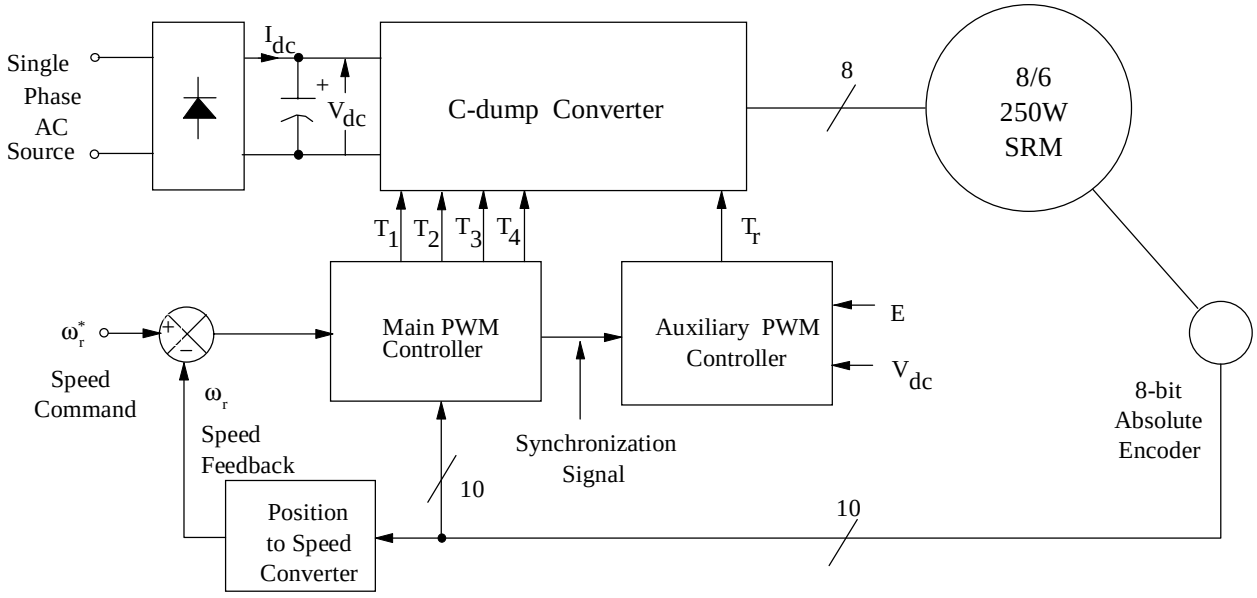


Figure 3.9 Block diagram of the proposed C-dump converter-based SRM drive system.

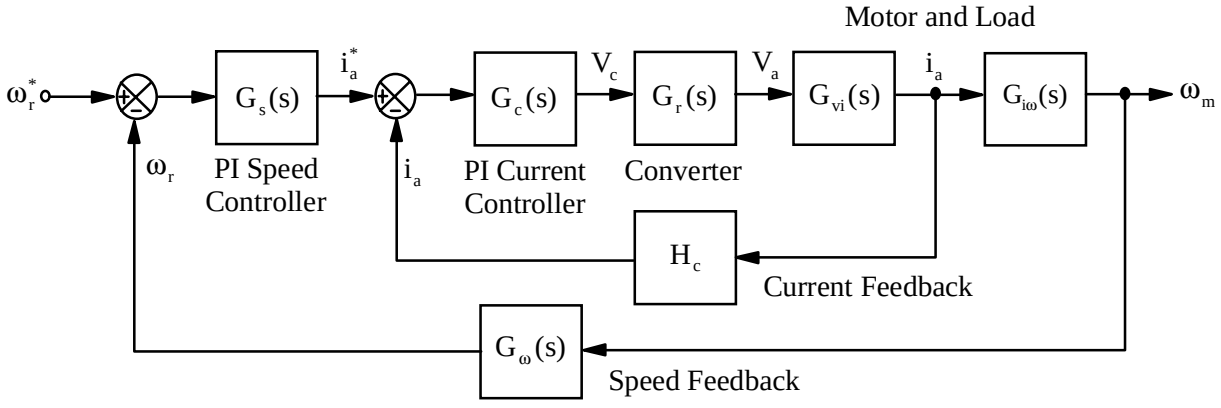


Figure 3.10 Generalized block diagram of a closed-loop VSD system with current and speed feedback.

Table 3.4
Transfer functions of functional blocks in a closed-loop VSD system.

Notation	Definition	Transfer Function
$G_s(s)$	PI Speed Controller	$\frac{K_s(1+sT_s)}{sT_s}$
$G_c(s)$	PI Current Controller	$\frac{K_c(1+sT_c)}{sT_c}$
$G_r(s)$	Converter, $V_a(s)/V_c(s)$	$\frac{K_r}{1+sT_r}$
$G_{vi}(s)$	From Motor Voltage to Current, $I_a(s)/V_a(s)$	$K_1\frac{1+sT_m}{(1+sT_1)(1+sT_2)}$
$G_{i\omega}(s)$	From Motor Current to Speed, $\omega_m(s)/I_a(s)$	$\frac{K_b}{B_t(1+sT_m)}$
$G_\omega(s)$	Speed Feedback Filter	$\frac{K_\omega}{1+sT_\omega}$

In Table 3.4, K_s and T_s is the gain and time constant of speed PI controller, K_c and T_c is the gain and time constant of current PI controller, K_r is the converter gain, and T_r is the time constant in a converter. K_1 is expressed as,

$$K_1 = \frac{B_t}{K_b^2 + R_a \cdot B_t}. \tag{3.57}$$

where, $B_t=B_1+B_l$, B_1 and B_l is the friction coefficient of motor and load, respectively. K_b is the back emf constant and R_a is the phase resistance of the motor.

T_m is the mechanical time constant of a motor with load,

$$T_m = \frac{J_t}{B_t}. \tag{3.58}$$

T_1 and T_2 are poles of the transfer function, $G_{vi}(s)$,

$$T_1 = \frac{1}{2K_2}\left(K_3 + \sqrt{K_3^2 - 4J_t \cdot L_a \cdot K_2}\right). \tag{3.59}$$

$$T_2 = \frac{1}{2K_2}\left(K_3 - \sqrt{K_3^2 - 4J_t \cdot L_a \cdot K_2}\right). \tag{3.60}$$

where,

$$\left.\begin{aligned} K_2 &= K_b^2 + R_a \cdot B_t \\ K_3 &= L_a \cdot B_t + J_t \cdot R_a \end{aligned}\right\} \tag{3.61}$$

and J_t is the moment of inertia of a motor with load. In the transfer function of speed feedback filter, $G_\omega(s)$, K_ω is the gain of the speed feedback filter and T_ω is the time constant.

Design of Current Controller

The simplified block diagram of the closed loop current control circuit is shown in Figure 3.11. The detailed reduction procedures are explained in [1] explicitly. The reduced order loop gain transfer function of the current control loop is obtained as,

$$\Delta(s) = G_c(s)G_r(s)G_{vi}(s)H_c \cong \frac{K}{(1+sT_1)(1+sT_r)}. \tag{3.62}$$

where

$$K \cong \frac{T_1}{2T_r}. \tag{3.63}$$

The current controller gain and time constant are obtained as,

$$K_c = \frac{K \cdot T_c}{K_1 \cdot K_r \cdot H_c \cdot T_m}. \tag{3.64}$$

$$T_c = T_2. \tag{3.65}$$

Then the transfer function of the current control loop becomes,

$$\frac{i_a(s)}{i_a^*(s)} = \frac{K}{H_c} \cdot \frac{1}{(1+K)+(T_1+T_r)s+(T_1 \cdot T_r)s^2}. \tag{3.66}$$

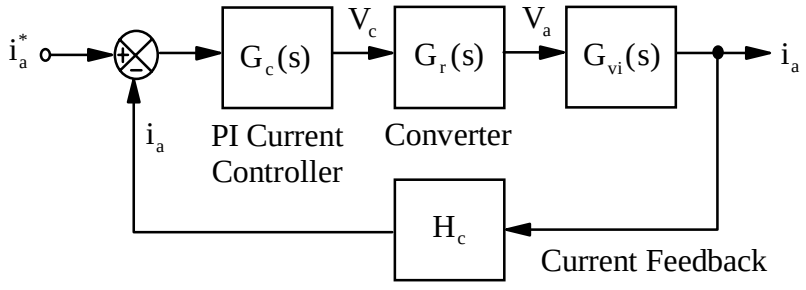


Figure 3.11 Block diagram of current control loop.

Design of Speed Controller

The simplified block diagram of the speed control loop is shown in Figure 3.12. The first order approximation of current loop transfer function expressed in equation (3.66) is performed to simplify the speed loop transfer function [1]. The reduced current loop transfer function is expressed as,

$$\frac{i_a(s)}{i_a^*(s)} \cong \frac{K_i}{(1+sT_i)}. \tag{3.67}$$

where,

$$\left.\begin{aligned} T_i &= \frac{T_3}{1+K_{fi}} \\ K_i &= \frac{K_{fi}}{H_c(1+K_{fi})} \\ K_{fi} &= \frac{K_c \cdot K_r \cdot K_1 \cdot T_m \cdot H_c}{T_c} \end{aligned}\right\} \tag{3.68}$$

where, $T_3 = T_1 + T_r$.

With this reduced current loop transfer function, the transfer function of the speed control loop is derived as,

$$\frac{\omega_m(s)}{\omega_r^*(s)} = \frac{1}{H_\omega}\left(\frac{1+4T_4 s}{1+4T_4 s+8T_4^2 s^2+8T_4^3 s^3}\right). \tag{3.69}$$

where, $T_4 = T_i + T_\omega$.

The gain and the time constant of the speed control loop is obtained as,

$$K_s = \frac{1}{2K_4 \cdot T_4}. \tag{3.70}$$

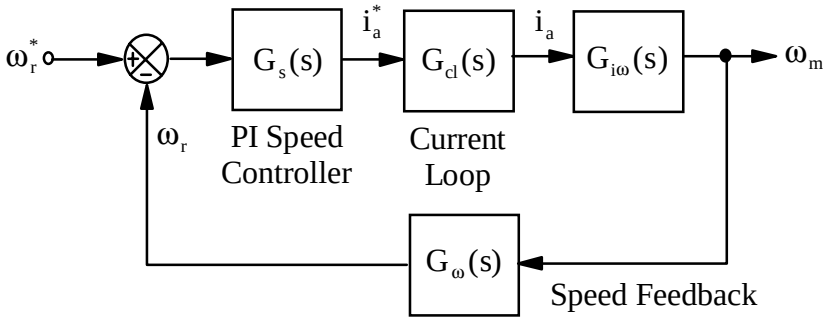


Figure 3.12 Block diagram of speed control loop.

$$T_s = 4T_4 . \tag{3.71}$$

where,

$$K_4 = \frac{K_i \cdot K_b \cdot H_\omega}{B_t \cdot T_m} . \tag{3.72}$$

The gain and the time constant equations for current and speed control loops, (3.64), (3.65), (3.70) and (3.71), will be utilized to design control loops for SRM-, PMBDC- and DCM-based VSD systems.

3.4.2 Main PWM Controller for the C-Dump Converter-Based SRM Drive system

The main PWM controller for C-dump converter based SRM drive consists of speed PI controller, triangular waveform generator and phase selection logic circuit as shown in Figure 3.13. The speed error signal, $\left(\omega_r^* - \omega_r\right)$, is applied to the input of the speed PI controller and its output signal is compared to triangular waveform to generate the main PWM signal. This signal is also used as the synchronization signal for the auxiliary PWM controller to match the switch turn off time instant between main and auxiliary PWM signals. The main PWM signal is distributed to the corresponding phase according to the rotor position information. An 8-bit absolute encoder for position sensing provides binary coded position information to an EEPROM (Electrically Erasable and Programmable Read Only Memory) which is programmed to decide the firing sequence and to generate four different advance angles for high speed operation. The distributed PWM signal goes to the optically isolated gate drive circuit to drive power switching device.

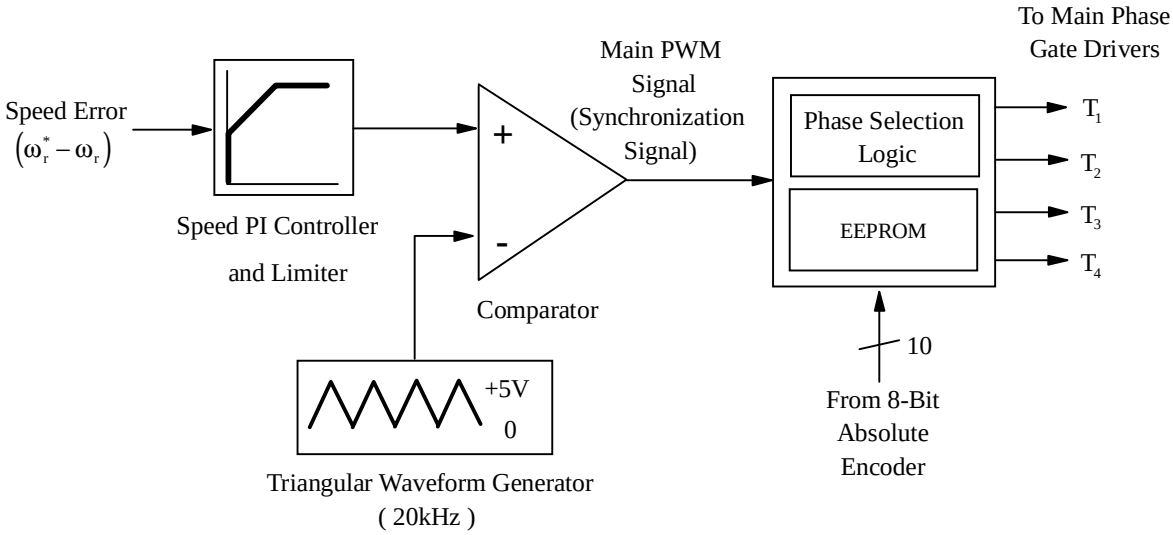


Figure 3.13 Block diagram of main PWM controller.

Design Example of a Speed Control Loop for a 250W 8/6 SRM-Based VSD System

A 250W 8/6 SRM-based VSD system has a speed control loop only. An inverting amplifier with a feedback network which consists of R_f and C_f is selected to implement the PI speed control circuit for the SRM-based VSD system as shown in Figure 3.14.

The transfer function of the implemented PI control circuit is found as,

$$G_s(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\left[\frac{\left(\frac{R_f}{R_i}\right)\left(1 + sC_f R_f\right)}{sC_f R_f}\right]. \tag{3.73}$$

By comparing the term in brackets in equation (3.73) with the transfer function $G_s(s)$ in Table 3.3, we have the expression of speed loop gain and time constant in terms of R_i, C_f and R_f as below:

$$K_s = \frac{R_f}{R_i}. \tag{3.74}$$

$$T_s = C_f \cdot R_f. \tag{3.75}$$

Therefore the implementation of PI speed controller shown in Figure 3.14 can be accomplished with equations (3.69), (3.70), (3.74) and (3.75). The designed gain values for PI speed controller are as follows:

Proportional gain: $K_s = \frac{R_f}{R_i} = 39$

Integral gain: $K_i = \frac{1}{C_f \cdot R_i} = 1$

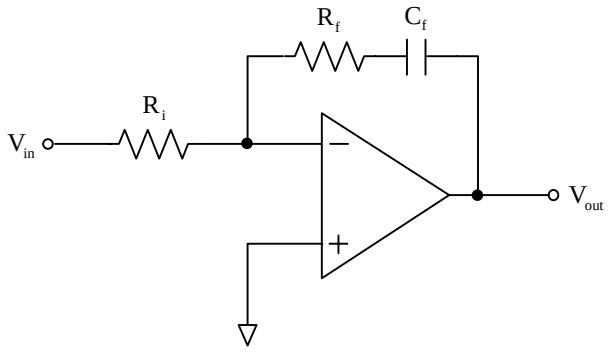


Figure 3.14 Realization of a PI speed controller for the SRM-based VSD system.

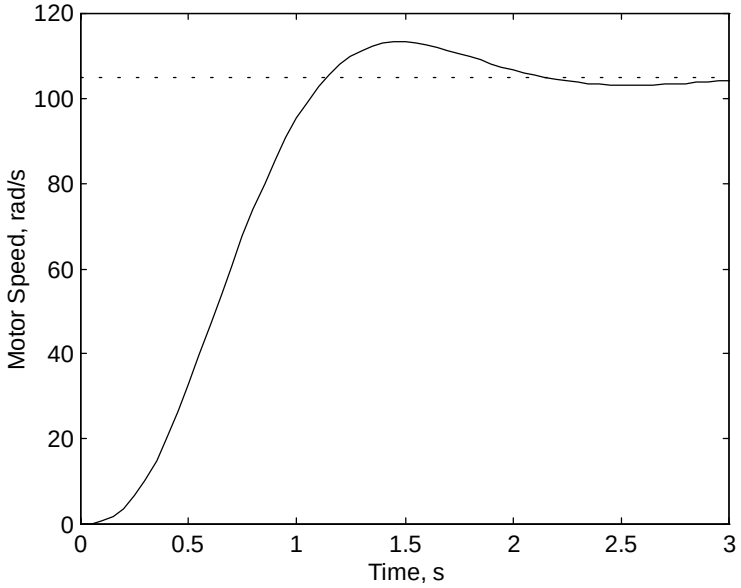


Figure 3.15 Simulated step speed response of the designed speed control loop for 250W SRM at 1,000r/min.

The step speed response at 1,000 r/min (104.72 rad/s) of the designed speed control loop with equation (3.68) is shown in Figure 3.15. The percent overshoot of the designed speed controller is about 9% and the rise time is about 0.65s. It should be mentioned that there is a soft start circuit in speed loop which has an equivalent pole to the zero of equation (3.68), that is, $s = -1/4T_4$. Therefore the zero of the equation (3.68) is canceled out.

3.4.3 Auxiliary PWM Controller for the C-Dump Converter-Based SRM Drive System

The control circuit for the recovery switch is illustrated in Figure 3.16. The main PWM signal is differentiated to generate a negative slope and then applied to the inverting input of a comparator. The difference between the voltage across the energy recovery capacitor, E, and the bus voltage, V_{dc}, which decides the on time of auxiliary PWM signal goes to the noninverting input of a comparator. The duty cycle of the recovery switch is produced by combining the main PWM signal and the output of a comparator through AND gate. The falling edges of both gate signals for the main and the recovery switches are synchronized to make both switches turning off at the same instant. In order to adjust the duty cycle of recovery switch automatically by the variation of the difference between E and V_{dc}, a differential amplifier is employed. The difference voltage is reduced to the logic level and then compared with inclined main PWM signal. The comparator output and main PWM signal is combined to synchronize the falling edges of both signals. The duty cycle of the recovery switch is designed to be proportional to the variation of E. As the level of E increases, the duty cycle increases and vice versa. This ensures the voltage level across C_o to be fairly constant. Thus the recovered energy will be proportional to the duty cycle of the recovery switch to maintain the voltage E to the predetermined level, which in this study $E = 2V_{dc}$.

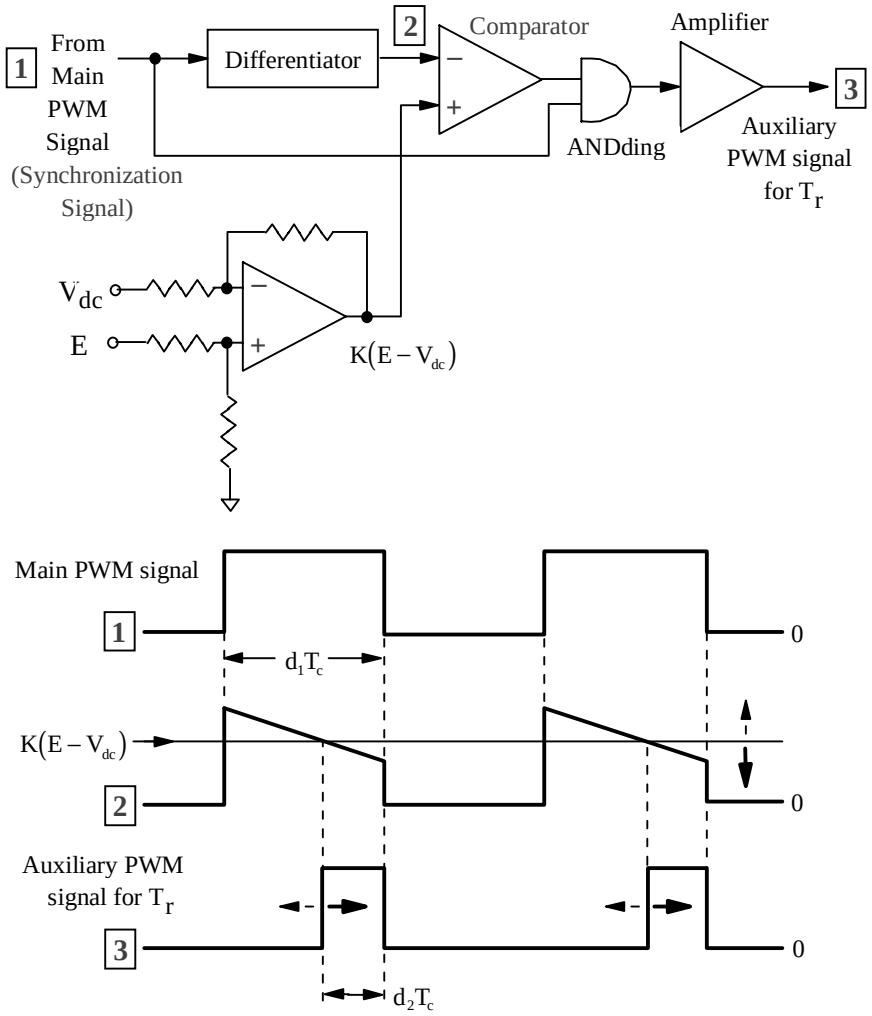


Figure 3.16 Simplified circuit diagram of the auxiliary PWM controller and its operational waveforms.

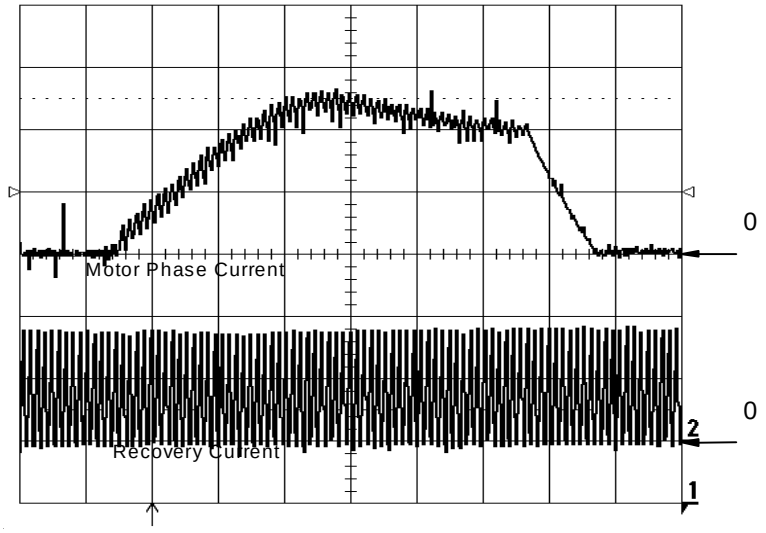
3.5 Design Verification of the Developed C-Dump Controller

3.5.1 Experimental Verification

In this section, the experimental waveforms of the motor phase current and recovery inductor current are measured to validate the developed controllers for C-dump converter based SRM drive system. A typical transient experimental waveforms of the main and recovery switch voltages and currents are also acquired to verify the operation of C-dump converter. The predicted and measured duty cycles of the main and recovery switch are illustrated to validate the derived analytical equations. The details of the prototype SRM drive system are given in Appendix B. The load is a dc brush generator whose friction, windage, and armature parameters are known. The controller has current limiting loops instead of current control loops in the present implementation. The implemented VSD system is speed controlled.

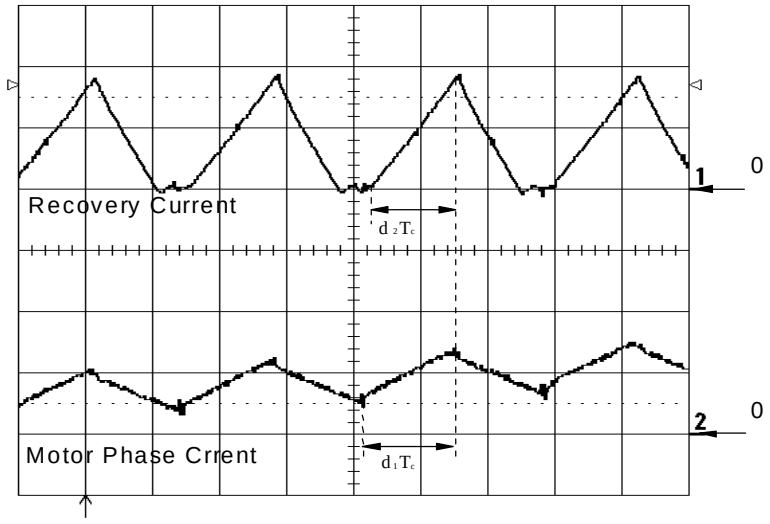
The typical waveforms of the measured motor phase current and recovery inductor current and its expanded waveforms are shown in Figures 3.17(i) and (ii) to verify the proposed control circuits experimentally. The pulse width modulated bus voltage applied to the motor phase generates a current waveform shown in Figure 3.17(i). The motor phase current is increased until it meets the peak value and is linearly decreased after the turn off of corresponding phase switch.

The magnitude of the recovery current is maintained with reasonably constant level allowing the proposed auxiliary control scheme to be validated experimentally. In the expanded waveforms, shown in Figure 3.17(ii), the duty cycle of the main phase switch is wider than the duty cycle of the recovery switch and the falling edges of both gate drive signals are synchronized as designed.



Vertical : 1A/div, Time : 0.5ms

Figure 3.17(i) Measured phase and recovery current waveforms of 8/6 250W SRM drive at 1,000r/min.



Vertical : 1A/div, Time : 20μs

Figure 3.17(ii) Expanded phase and recovery current waveforms of 8/6 250W SRM drive at 1,000r/min.

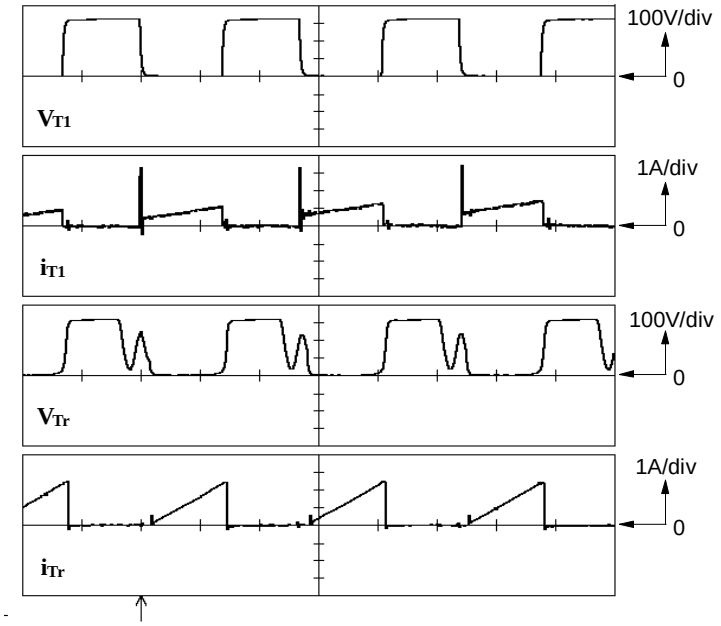


Figure 3.18 Transient experimental waveforms.

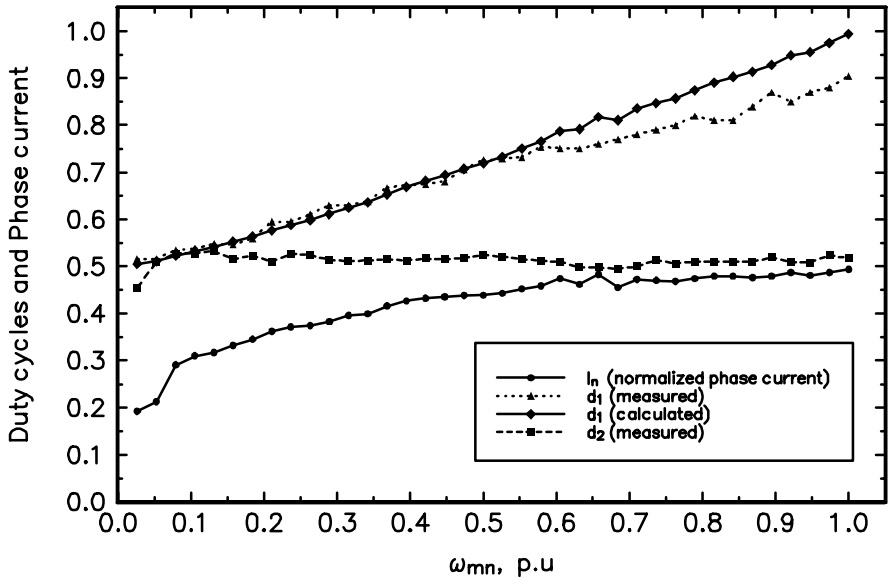


Figure 3.19 Duty cycles and phase current versus rotor speed.

A typical operational point of the SRM drive is shown in Figure 3.18 for the switch voltage and current in the phase and recovery circuit. The recovery circuit is operated with a marginally discontinuous current and it is inferred the recovery current derived from the expression (3.53) correlates very well experimentally. The incremental voltage in the energy recovery capacitor is contained within 0.01 pu as seen from the voltage across the switches with hardly any transient peaks.

A verification of the speed range as a function of the phase current and duty cycle is attempted in a steady-state and is shown in Figure 3.19. The machine current is 0.19 to 0.49 pu over a speed

range of 0.026 to 1 pu. The measured duty cycle closely follows the predicted values thus validating the assumptions and derivations.

3.5.2 Simulation of the C-Dump Converter-Based SRM Drive System

The verification of the analysis of the C-dump converter-based SRM drive is performed by the simulation with MATLAB software. The derived circuit equations in section 3.3.3 for each mode are rearranged in state space form by

$$\dot{x}_j = A_j \cdot x + B_j \cdot u \,. \tag{3.76}$$

where, x_j is the state vector which consists of all the system states in mode j. Among the five operational modes derived in section 3.3, three distinct modes are considered for simulation. Since there are three different operation modes, $j = 1, 2, 3$. A_j is the system matrix and B_j is the input matrix in mode j, respectively, and u is the input vector consisting of the system input functions. The numerical solutions of equation (3.76) are obtained with Backward Euler numerical integration algorithm due to its simplicity.

The single-phase SRM model is shown in Figure 3.20. The voltage loop equation is [2],

$$V_{ph} = R_{ph} \cdot i_{ph} + \frac{d\lambda\left(i_{ph},\, \theta_r\right)}{dt} \,. \tag{3.77}$$

where

V_{ph} = phase voltage, V
i_{ph} = phase current, A
R_{ph} = phase winding resistance, Ω
λ = flux linkages, Wb-turns
θ_r = rotor position, rad

The flux linkage is the function of phase current and rotor position and the relationship with motor phase inductance can be expressed as [2],

$$\lambda\left(i_{ph},\, \theta_r\right) = L\left(i_{ph},\, \theta_r\right) \cdot i_{ph} \,. \tag{3.78}$$

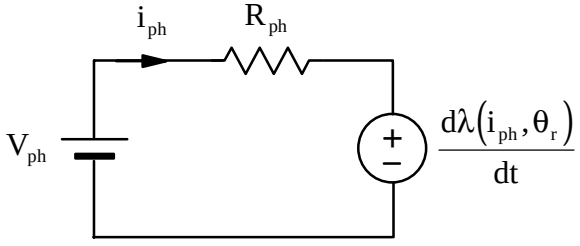


Figure 3.20 Single-phase SRM model.

The flux linkage and torque data which are both functions of phase current and rotor position were generated by SRMCAD software [69]. This three-dimensional data is illustrated in Figure 3.21(i) and (ii). Only one half of the full rotor pitch, that is, the rotor position from 0^o to 30^o, is shown in both plots. The other half of the flux linkages from 0^o to -30^o rotor position is the mirror image of the Figures 3.21(i) and (ii). The torque shown in Figure 3.21(ii) is generated from 0^o to 15^o rotor position for motoring operation. For regeneration, it should be generated in the rotor position from 0^o to -15^o. The torque generation is explained in section 3.2 in detail.

Three operational modes are considered for simulation are shown in Figure 3.22. Where R_1 indicates a parasitic resistance, i_r is the recovery current, λ_x is the flux of currently active phase, λ_y is the flux of previously active phase and E is the voltage across the energy storage capacitor C_o. The previously active phase is the phase that was energized before the current active phase. It is considered in simulation to provide the commutating current flows into the recovery capacitor.

The state vector x is selected as

$$x = [\, i_r \;\; \lambda_x \;\; \lambda_y \;\; E \,]^T . \tag{3.79}$$

The system input vector u is selected as

$$u = [V_{dc} \;\; V_a \;\; V_c \;\; V_d \,]^T . \tag{3.80}$$

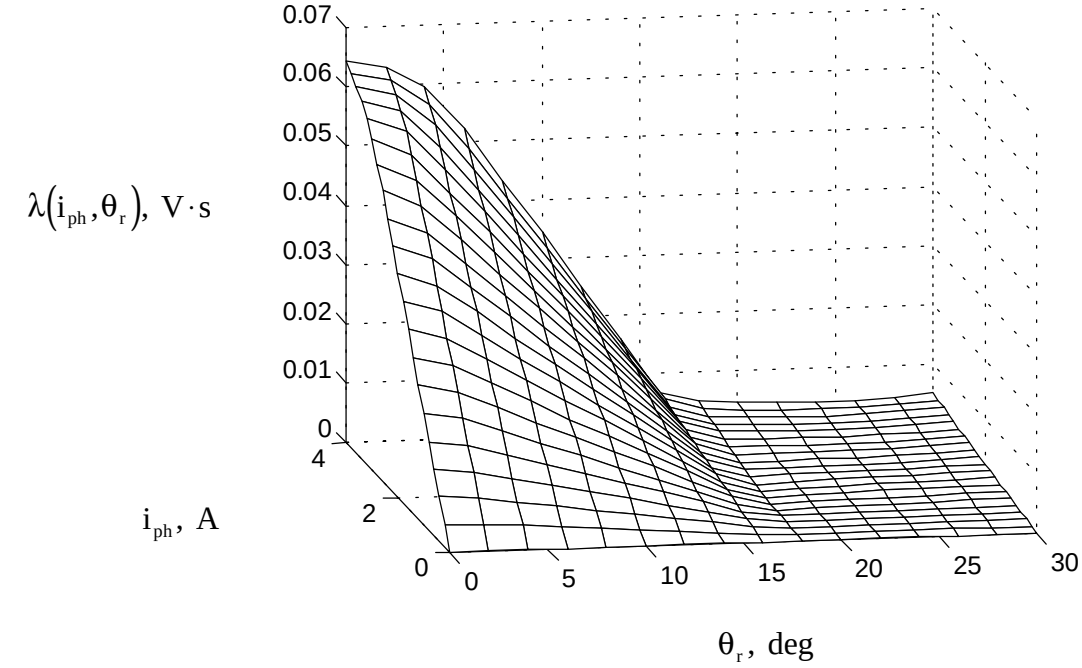
where, V_{dc} is the dc bus voltage. V_a, V_c and V_d are node voltage at node *a*, *c* and *d*, respectively.

Three sets of state equations are derived from three operational modes. Corresponding system and input matrices are summarized in Table 3.4.

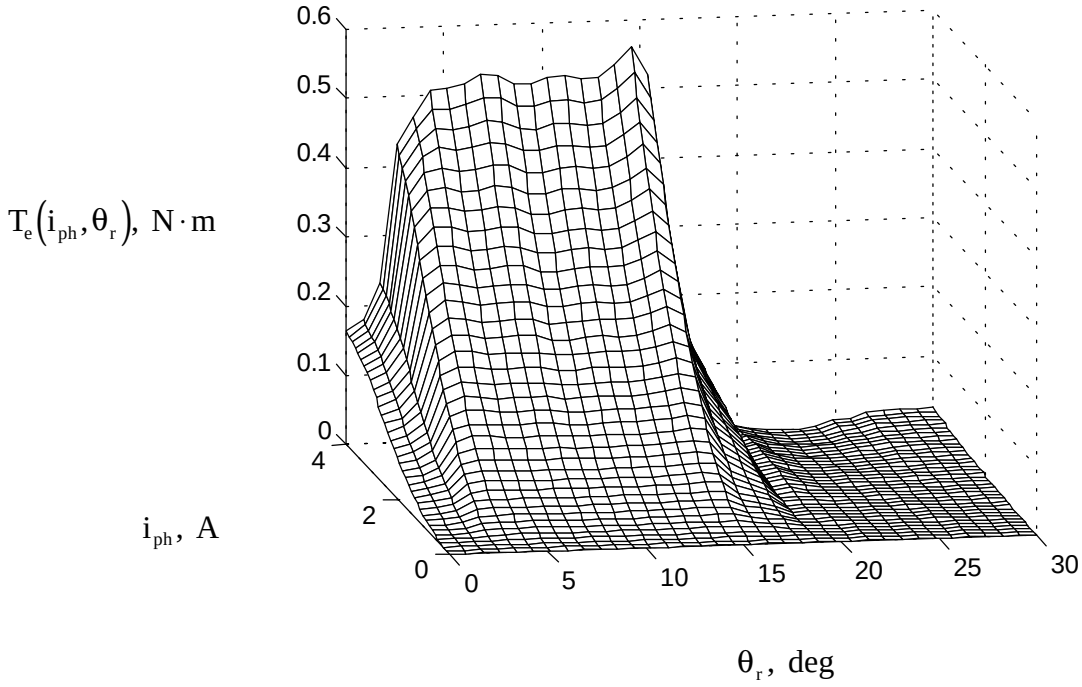
Figure 3.23 shows the flowchart for simulation of C-dump converter based SRM drive system. In order to complete the simulation of the SRM-based VSD system, the flux linkage and torque data for the prototype 8/6 250W SRM generated by SRMCAD software [69] should be provided.

The simulated four SRM phase currents are shown in Figure 3.24. The initial rising time in the simulated current shows much faster than the current obtained with the experiment, which is shown in Figure 3.17(i). The steady-state and turn-off current waveshapes match well with the experimental waveforms.

The expanded phase current and recovery current are shown in Figure 3.25 along with their PWM switching signals. The duration of switch on time and instant of the switch turn off time are simulated clearly as explained in section 3.4.2.

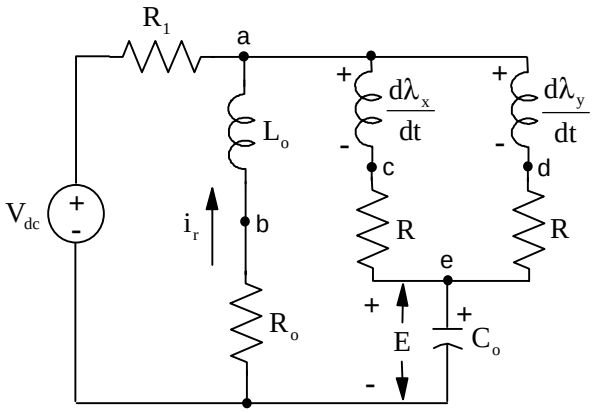


(i) Flux linkages

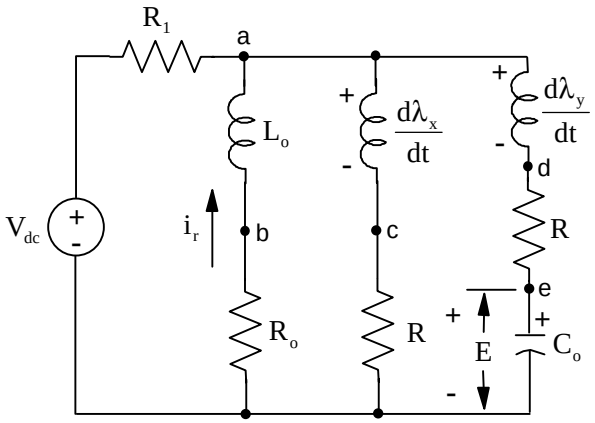


(ii) Torque

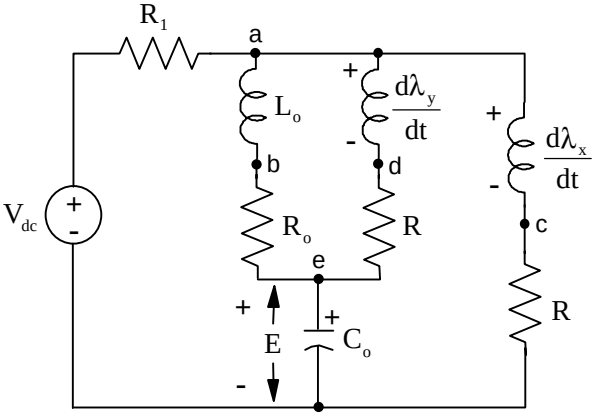
Figure 3.21 Flux and torque data versus motor phase current and rotor position for a prototype 8/6 250W SRM.



(i) Mode I: T_1 and T_r off



(ii) Mode II: T_1 on and T_r off



(iii) Mode III: T_1 and T_r on

Figure 3.22 Three modes of operation of a phase for simulation.

Table 3.5
System and input matrices for simulation of a C-dump converter based 250W SRM drive system.

Mode	A-Matrix	B-Matrix
I	$\begin{bmatrix} 0 & 0 & 0 & -\frac{2R_o}{L_oR} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{2}{RC_o} \end{bmatrix}$	$\begin{bmatrix} -\frac{R_o}{L_oR_1} & \left(\frac{1}{L_o}+\frac{R_o}{L_oR_1}\right) & \frac{R_o}{L_oR} & \frac{R_o}{L_oR} \\ 0 & 1 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 0 & 0 & \frac{1}{RC_o} & \frac{1}{RC_o} \end{bmatrix}$
II	$\begin{bmatrix} 0 & 0 & 0 & -\frac{R_o}{L_oR} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{RC_o} \end{bmatrix}$	$\begin{bmatrix} -\frac{R_o}{L_oR_1} & \left(\frac{1}{L_o}+\frac{R_o}{L_oR_1}\right) & \frac{R_o}{L_oR} & \frac{R_o}{L_oR} \\ 0 & 1 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 0 & 0 & 0 & \frac{1}{RC_o} \end{bmatrix}$
III	$\begin{bmatrix} 0 & 0 & 0 & -\left(\frac{1}{L_o}+\frac{R_o}{L_oR}\right) \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \frac{1}{C_o} & 0 & 0 & -\frac{1}{RC_o} \end{bmatrix}$	$\begin{bmatrix} -\frac{R_o}{L_oR_1} & \left(\frac{1}{L_o}+\frac{R_o}{L_oR_1}\right) & \frac{R_o}{L_oR} & \frac{R_o}{L_oR} \\ 0 & 1 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 0 & 0 & 0 & \frac{1}{RC_o} \end{bmatrix}$

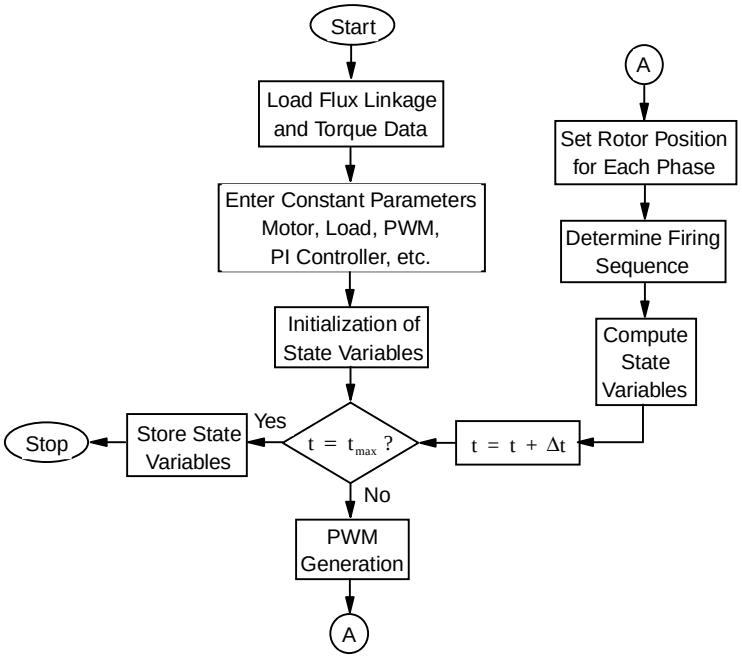


Figure 3.23 Flowchart for simulation of the C-dump converter-based SRM drive.

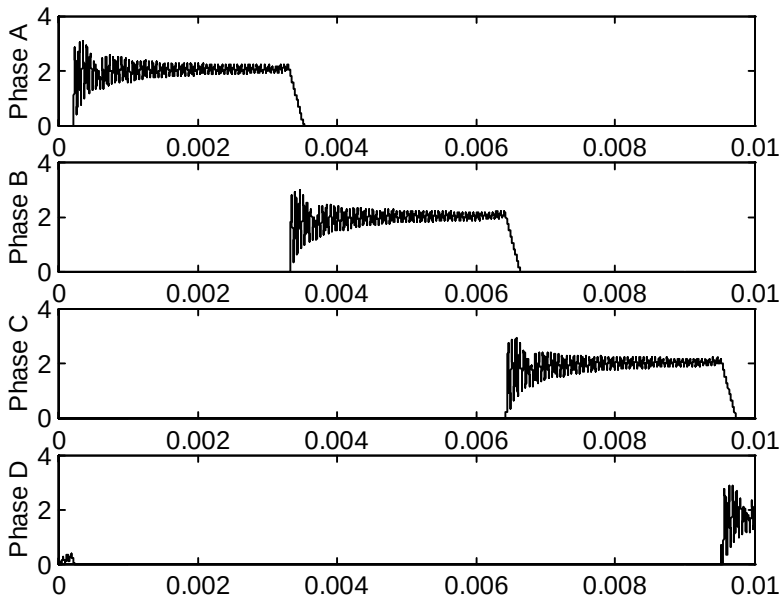


Figure 3.24 Simulated SRM phase currents at 1,000r/min.

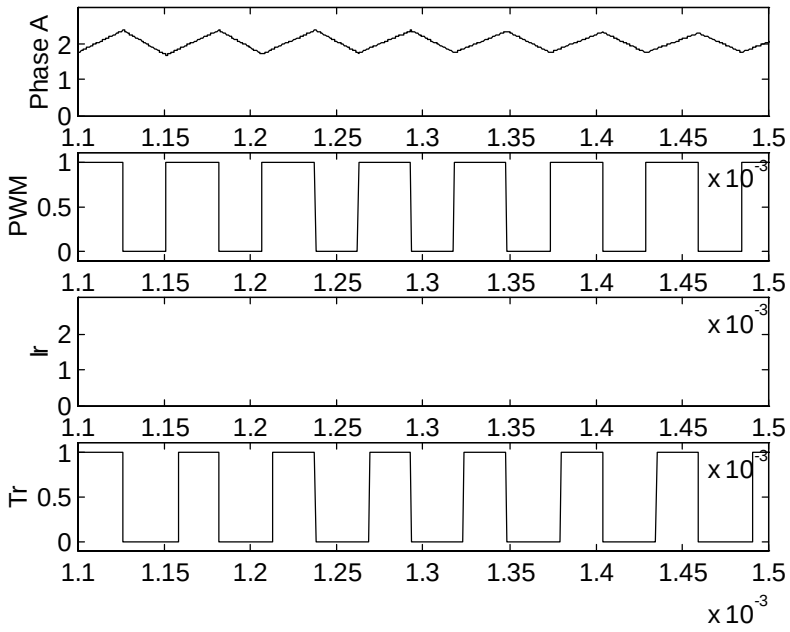


Figure 3.25 Expanded current and PWM switching signals
for main and recovery switches at 1,000r/min.

3.6 Input PF-Corrected VSD System with SRM

The development and analysis of C-dump converter for SRM-based VSD are presented in previous sections. In this section, the analytical and experimental results of the implementation of PF corrected C-dump converter-based SRM drive system in regard to efficiency and harmonic contents of the input supply current are introduced. The loss model of the C-dump converter-

based SRM drive system is derived to predict the drive system efficiency. The predicted efficiency of the 300W PFC preregulator is obtained with equation (2.14). Experimental results from a laboratory prototype SRM which has the maximum power output of 250W at 4200r/min are presented with measurements of efficiency, PF and input current harmonics with and without the PFC circuit. The parameters of the 250W SRM are shown in Appendix B.

3.6.1 Implementation of the Proposed System

The implementation details of the proposed system are given in this section. The PFC circuit was built for 120V ac input and 190V dc output with a power rating of 300W. The control of PFC circuit was achieved with a dedicated single chip controller UC3854 and the whole PFC circuit was packaged in 3"×3"×4" including the heatsink etc. The parameters for the prototype 300W PFC is shown in Appendix A. The design of the control circuit for the PFC stage is not discussed here because it may be obtained in many sources, such as [39, 70]. The outer dimensions of the SRM are 4.4"(diameter) and 3.75"(length) and an 8-bit absolute encoder is attached to the rotor shaft. The construction of the overall SRM-based VSD is based on the circuit diagram shown in Figure 3.26. The power circuit diagram of the C-dump converter shown in Figure 3.6 is used to build the C-dump converter based SRM drive system. The main and auxiliary controllers for the C-dump converter are implemented as explained in Section 3.4.

The experimental setup for the prototype C-dump converter-based SRM drive system with and without PFC front-end preregulator is shown in Figure 3.26. The proposed experimental setup consists of four subsystems: PFC preregulator or bridge rectifier, C-dump converter, SRM,

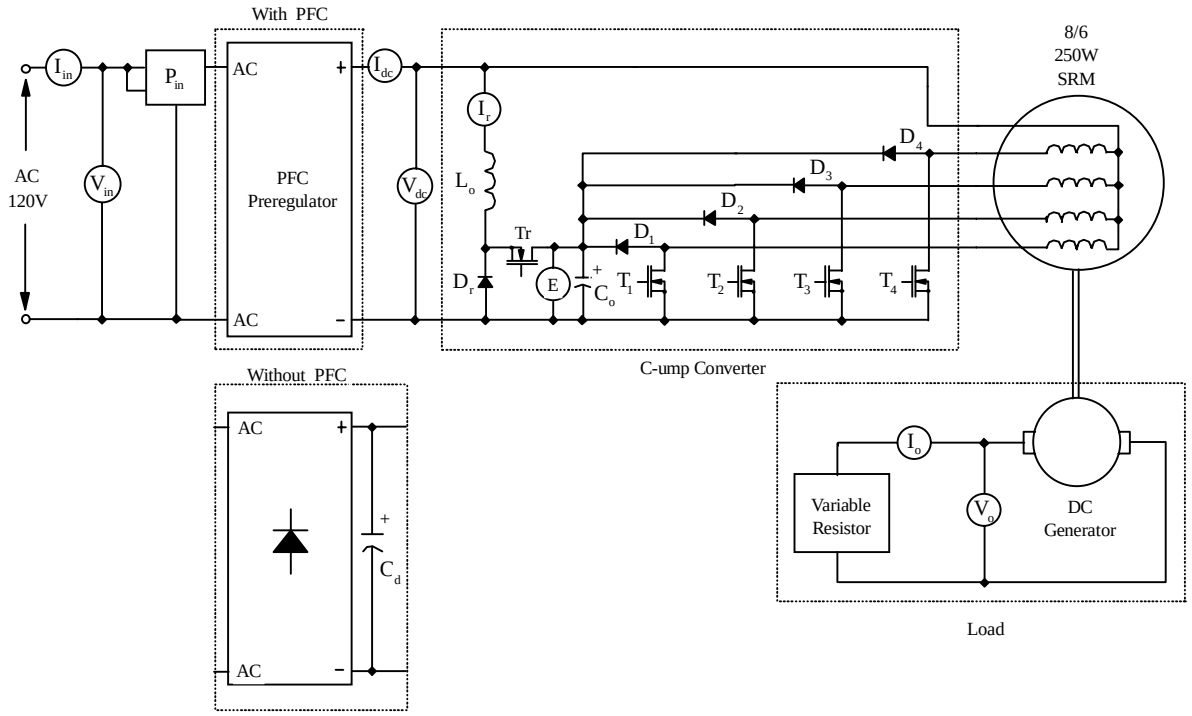


Figure 3.26 Test setup for C-dump converter-based SRM drive system with and without PFC circuit.

and dc generator load. The bridge rectifier circuit incorporates a single-phase bridge rectifier diode and filter capacitor as shown in Figure 1.4. This circuit will be replaced with a PFC preregulator module when the effect of PFC is evaluated. A dc voltmeter, represented as *E* in the figure, is connected across the recovery capacitor, C_o, to monitor the voltage across it. Other typical instrument connections are shown in Figure 3.26. All the ac and dc power is averaged and measured using voltmeters, ammeters and precision wattmeter. It is estimated the error in the reading is in the order of 1 to 2%. The load for the SRM drive system is a permanent magnet brush dc generator whose details are given in Appendix B.

3.6.2 Discussion on Experimental Method and Results

Experimental Method

The devised experimental setup can measure various currents and voltages of the SRM drive system with and without PFC regulator. The obtained experimental values will further be utilized to analyze and compare with the predicted values. The ac-dc-ac conversion scheme is required for this experiment. The ac-dc conversion stage will be either PFC preregulator or bridge diode rectifier circuit. The C-dump converter is used for dc-ac conversion stage for a 250W 8/6 SRM. The dc input voltage to the C-dump converter is maintained at 190V dc. To obtain 190V dc without PFC circuit, the ac input voltage was raised to 138V ac even though the input to PFC circuit was 120V ac only. This fact could have improved the efficiency of ac to dc converter in the rectifier case slightly as the rms input current declines due to the increase in supply voltage.

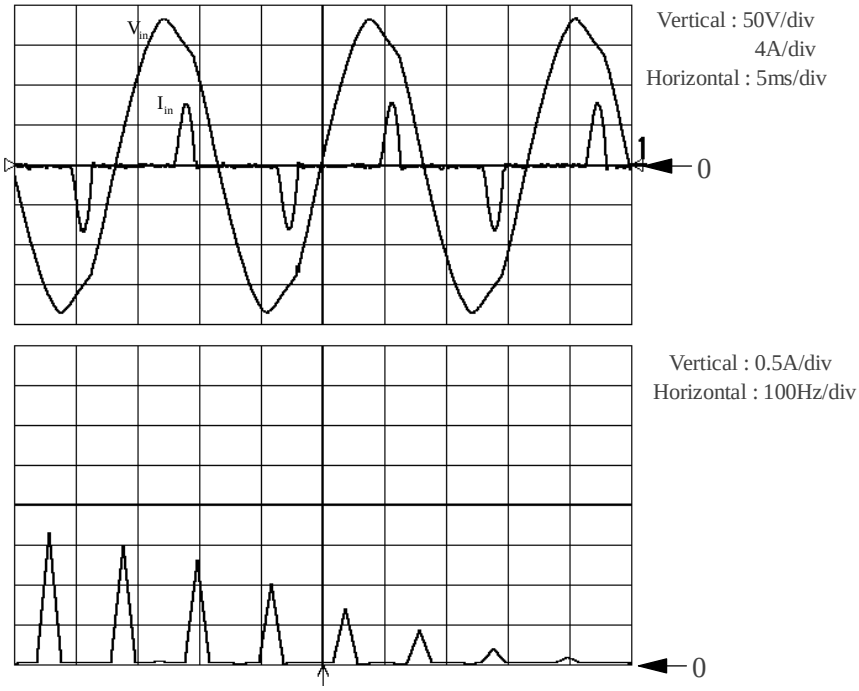
For proper comparison of the drive system with and without the PFC, the power which is proportional to the motor speed was set for each case. The tested speed range was from 100 to 2300r/min with 100r/min increment. This speed range is equal to the rated output power range which is from 4.17 to 95.83W with 4.17W increment. A small difference exists between the system with and without PFC over the entire speed range due to discrete steps in the sensitive load resistor bank connected to the dc generator.

Input Variables

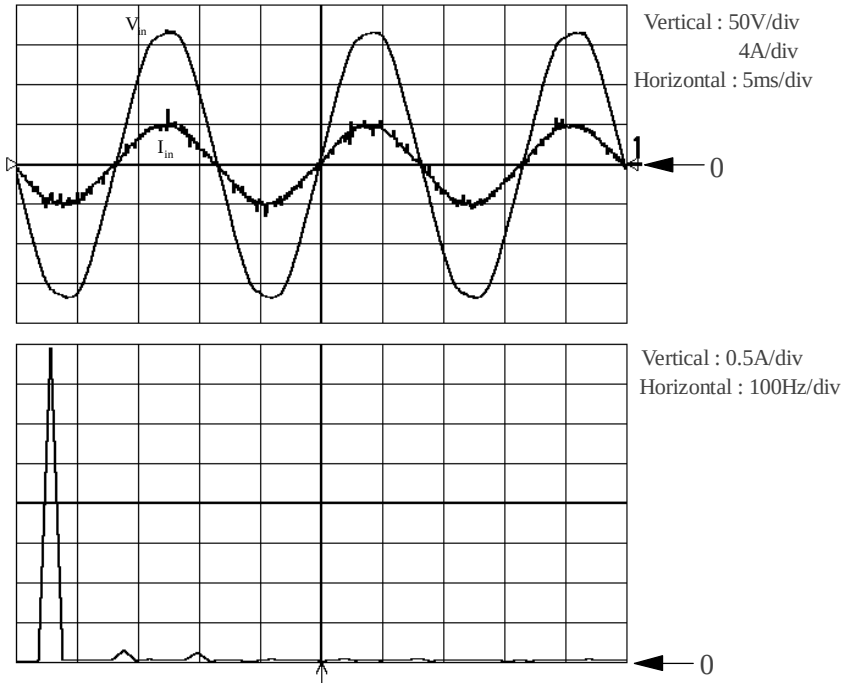
A sample input voltage and current with their harmonics spectra at 96W output power (2,300r/min) are shown in Figure 3.27(i) and (ii) for the case without and with the PFC circuit,

Figure 3.28 shows the comparison of the magnitude of current harmonics in input current with and without PFC. The modified Class D relative harmonic current limit values of the IEC 1000-3-2 [24] are applied to verify the effectiveness of PFC circuit. The magnitudes of the odd numbered current harmonics far exceed IEC limits without PFC. With PFC, it shows the proposed PF corrected SRM drive system meets IEC regulation with a meaningful margin.

The comparison based on input power factor and magnitude of input current is shown in Figure 3.29(i) and (ii), respectively. Increasing load attenuates the harmonics amplitudes and also improves the power factor. This may be attributed to the increase in the input current and better control of it in the PFC circuit, making the current follow the sinusoidal reference very closely. Note that by assuming the tracking error remains the same regardless of the peak magnitude, the percentage of the error current decreases as the peak current increases. Hence there is the



(i) without PFC regulator



(ii) with PFC regulator

Figure 3.27 Experimental waveforms of the line voltage, current and harmonics spectra of the line current without and with PFC regulator at 2,300 r/min.

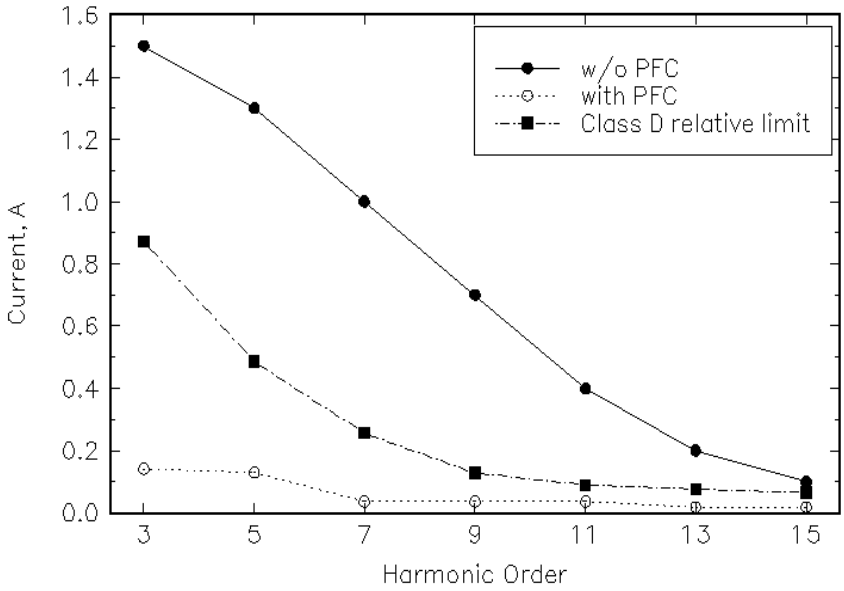


Figure 3.28 Comparison of the measured input current harmonics from Figure 3.27 with modified Class D limit.

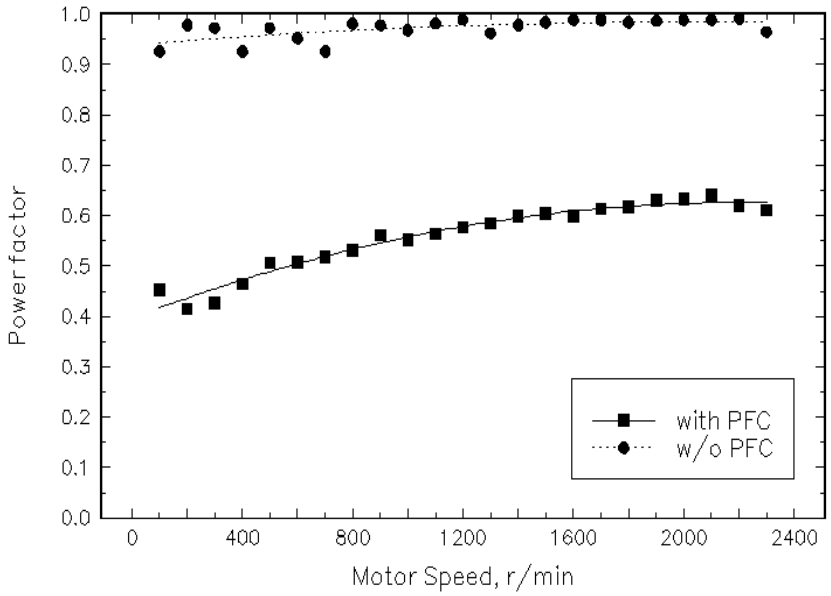


Figure 3.29 (i) Input power factor with and without PFC preregulator.

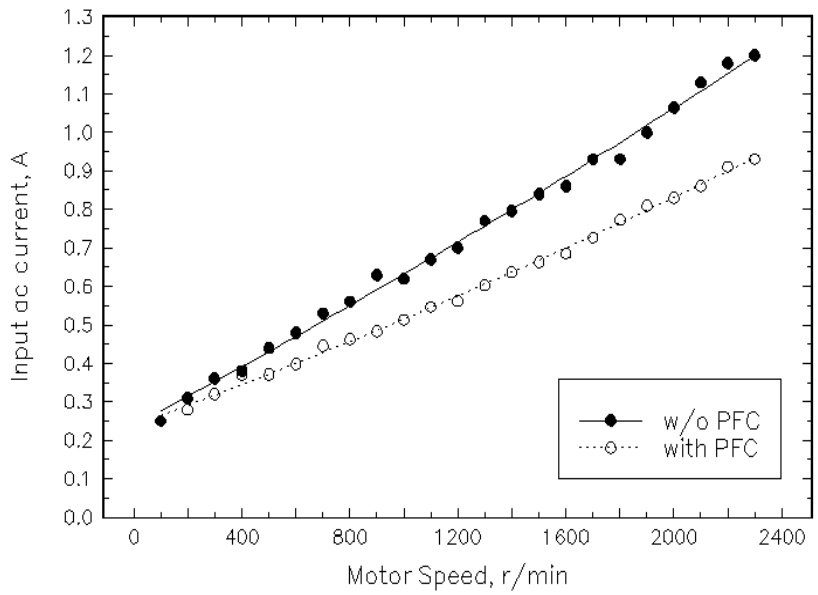


Figure 3.29 (ii) Magnitude of input ac current with and without PFC preregulator.

reduction of sideband harmonics and improvement in the input power factor. In the case of the simple bridge rectifier, the current conduction angle will increase with increasing load, contributing to the same phenomena discussed above for PFC. The required input ac current is less with PFC than one without PFC while using the same power output level. This phenomenon is more clear in higher output power range because the harmonic components are getting bigger without the PFC circuit, therefore the total rms input current is increasing as explained in equations (2.1) and (2.2).

Efficiency

The efficiency is calculated between the ac input and motor shaft output. The output power of the SRM is found as the sum of the dc generator output and its losses, and given by [1, 62],

$$P_o = V_o \cdot I_o + I_o^2 \cdot R_a + V_b \cdot I_o + P_{fw} \text{ , W.} \tag{3.81}$$

where,

V_o = output voltage of the dc generator
I_o = output current of the dc generator
R_a = armature resistance of the dc generator
V_b = brush drop of the dc generator
P_{fw} = friction and windage losses of the motor-generator set

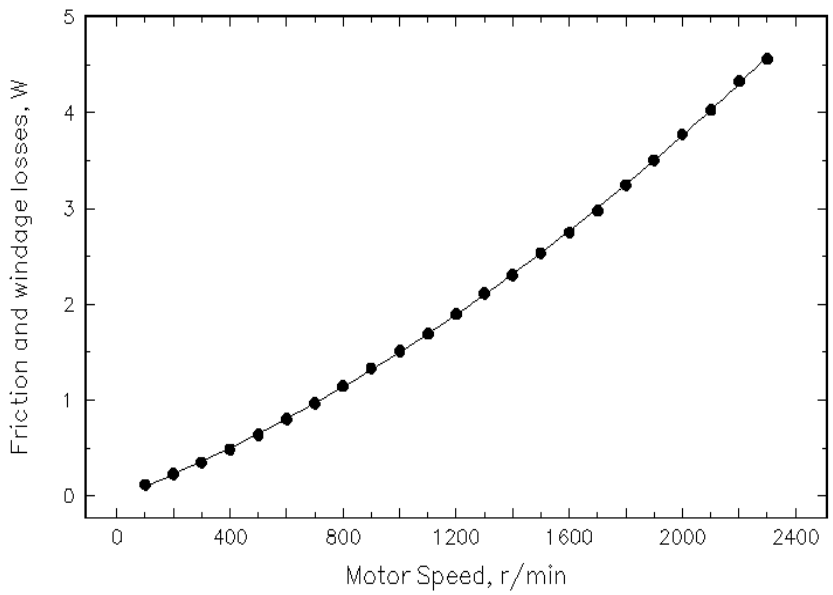


Figure 3.30 Friction and windage losses of a 250W SRM and Pittman DCM set.

The frictional and windage losses of the SRM plus dc generator as a function of speed is measured and plotted as shown in Figure 3.30.

The rated load current at n r/min is estimated as,

$$I_{or} \cong \frac{P_{or} - P_{fw}}{nK_b} \text{ , A.} \tag{3.82}$$

where K_b is the emf constant in V/(r/min) and P_{or} is the rated output of the dc generator given by [1],

$$P_{or} = P_b \times \left(\frac{n}{n_b}\right)^k \text{ , W.} \tag{3.83}$$

where P_b is the base power in W, n_b is the base speed in r/min, and k is the constant according to load characteristics such as, k=1 for constant load, k=2 for friction load and k=3 for fan type load.

The input power of the drive system is the sum of total losses in the drive system and the rated output power as explained similarly in equation (2.17). The loss model of the C-dump converter based four phase SRM drive system is derived in terms of phase current, recovery current and duty cycles of both main phase switch and recovery switch considering the loss equations in Table 3.2 and power component values used in the prototype drive system and given below:

$$\begin{aligned} P_{SRM} &= \left[0.25 + (2.20)d_1\right]I_1^2 + (5.08 - d_1)I_1 - (0.92)d_1 \\ &\quad + \left[0.39 + (0.60)d_2\right]I_r^2 + (2.02 - d_2)I_r + 1.84 \text{ , W.} \end{aligned} \tag{3.84}$$

The constant term is the sum of the switching losses of four phase diodes and the recovery diode. The losses due to high frequency effects and core losses in SRM are not considered in this model. The calculation process to predict the system efficiency is summarized in Figure 3.31. The phase current is evaluated as the sum of the input dc current, i_{dc} and recovery current, i_r as shown in Figure 3.7(i). The input dc current is estimated with the rated output power of the SRM. The recovery current is obtained with equation (3.56) considering duty cycle d_2=0.5.

The total losses in SRM drive system which includes C-dump converter and motor is found with equation (3.84). Without the PFC preregulator, the sum of the rated output power of the SRM, the total losses found with equation (3.84) and the bridge rectifier conduction losses explained in Table 2.2 becomes the system input power. The estimated input power of the SRM drive system is considered as the output of the PFC preregulator. The input power of the PFC circuit is obtained by adding total losses in the PFC circuit to the input power of the SRM drive

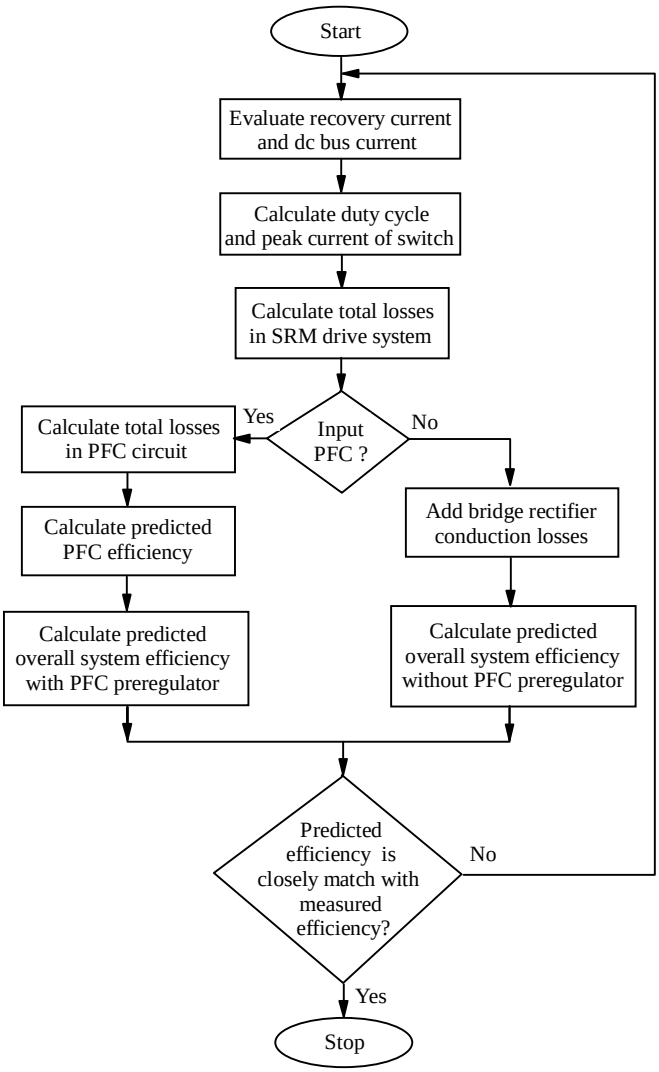


Figure 3.31 Efficiency calculation procedure for the SRM drive with and without PFC preregulator.

system. The overall SRM-based VSD system efficiency with the PFC preregulator is evaluated as the product of the PFC efficiency and the SRM drive system efficiency.

Efficiency and power output versus speed is shown in Figures 3.32(i) and (ii) to validate the calculation of losses in the machine and circuit components. The small deviation between measured and predicted efficiencies may be contributed by the additional ac resistance losses and core losses in the machine that are not accounted in the computation. Note that the output power is normalized to 75W, i.e. the nominal power output of the SRM at 1,800 r/min. The efficiency of the C-dump converter-based SRM drive system is shown in Figure 3.32(i) and the overall efficiency versus speed including the ac to dc conversion stage is shown in Figure 3.32(ii). All of them show an increasing trend of efficiency with increasing load. The low efficiency of the

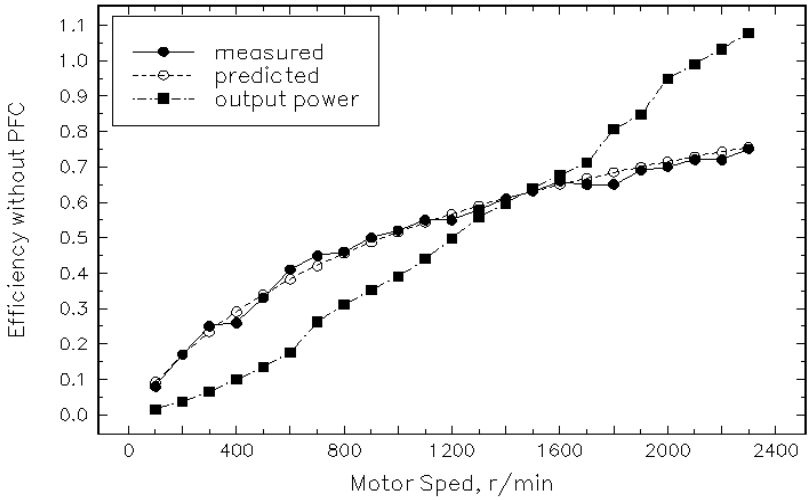


Figure 3.32(i) SRM drive system efficiency and normalized measured output without PFC preregulator.

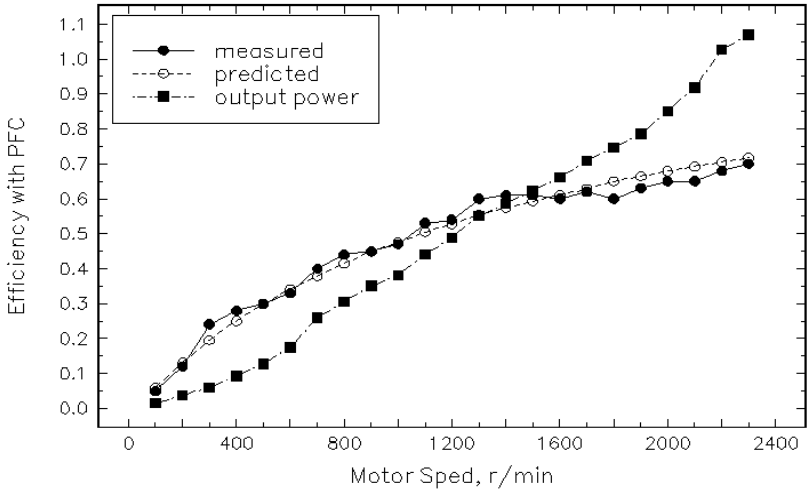


Figure 3.32(ii) SRM drive system efficiency and normalized measured output with PFC preregulator.

system is due to the poor efficiency of the C-dump converter as it has power switching devices with higher conduction drops and copper losses in recovery inductor and also due to the high winding resistances of SRM. The system without PFC has at least 2% greater efficiency compared to the one with PFC up to power levels of 90W. This is contributed by the switching losses in the PFC boost stage. In spite of the higher efficiency, it is important to consider the effect of the low power factor and rich harmonics generated by the bridge rectifier with larger filter capacitor. If efficiency is the only concern, the integration of a PFC circuit in the drive system is not viable.

The error of efficiency prediction for SRM drive system is compared in Figure 3.33 with and without PFC preregulator. The error shows relatively high up to 400r/min and settles down within ±10% beyond that speed. This indicates the developed loss model for the SRM-based

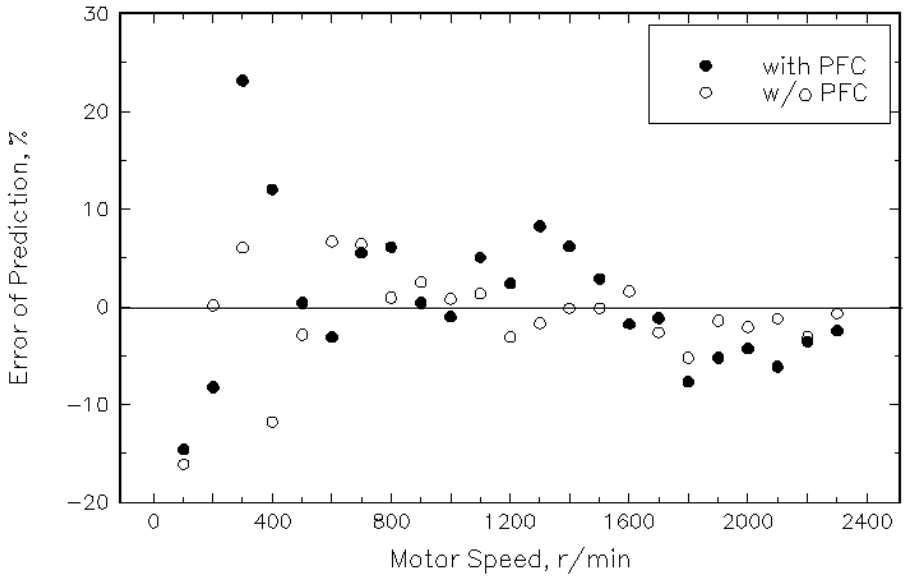


Figure 3.33 Efficiency prediction error versus SRM speed with and without PFC preregulator.

Table 3.6
Statistical analysis of efficiency prediction errors for SRM drive system with and without PFC preregulator.

	Fig. 3.25(i) with PFC	Fig. 3.25(ii) without PFC
Total Observation	23	23
Minimum Error	-14.57	-16.12
Maximum Error	23.15	6.69
Mean	0.58	-1.12
Median	-0.99	-0.69
Variance	60.94	26.31
Standard Deviation	7.81	5.13
Standard Error	1.63	1.07

VSD is not satisfactory to predict the efficiency in low speed, in this case less than 400r/min. The detailed statistical analysis results for the prediction error are tabulated in Table 3.5. The efficiency with PFC preregulator shows wider dispersion of error distribution.

3.7 Conclusions

This chapter addresses the analysis and design of the C-dump converter for a four phase SRM drive system and proposes the input PFC for the SRM-based VSD.

Analytical derivations are made for each identified mode of operation in the motor drive, and insights into the limits on maximum speed of operation is derived in terms of the C-dump capacitor voltage and other motor parameters. The ratings of the converter switches, diodes, inductors and capacitors are derived based on the analysis for a given SRM capacity. The key theoretical results were verified with a closed loop 250W laboratory SRM drive system. Also the analysis of the losses in the converter was included to aid in the computation of efficiency and hence in the overall efficiency of the SRM drive system. The main and auxiliary controllers for the C-dump converter have been developed and its performance has been validated with experiment and simulation. The developed controller may be suitable to the low cost SRM-based variable speed appliance drive system implementation. All of the above constitute original contributions in the analysis and design of the C-dump converter for SRM drive.

Input power factor correction for the SRM-based VSD system has been proposed for appliance applications and experimentally verified on a laboratory prototype SRM drive system. Its performance has been compared without a PFC regulator and found to be inferior in efficiency by 2% consistently, even though it is superior in input power factor and less in third order harmonics over the entire speed range of operation from 100r/min to 2,300r/min. For appliance applications, the introduction of the PFC circuit will enable a pure sinusoidal current from the ac supply and if that is going to be an important criterion, then it is recommended for integration with a clear understanding that it will lower the efficiency. This is a significant result arising from this study. While enhanced packaging size and increasing differential cost for the PFC-based SRM drive will be serious factors of concern in high volume appliance applications, it should be noted the effects of both can be mitigated, if not eliminated, in such a manufacturing environment.