Derivation of Parabolic Current Control with High Precision, Fast Convergence and Extended Voltage Control Application

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ABSTRACT

Current control is an important topic in modern power electronics system. For voltage source inverters, current control loop ensures the waveform quality at steady state and the fast response at transient state. To improve the current control performance, quite a few nonlinear control strategies have been presented and one well-known strategy is the hysteresis current control. It achieves fast response without stability issue and it has high control precision. However, for voltage source inverter applications, hysteresis current control has a wide switching frequency range, which introduces additional switching loss and impacts the design of harmonic filter. Other nonlinear current control strategies include one-cycle control, non-linear carrier control, peak current control, charge control, and so on. However, these control strategies are just suitable for specific topologies and it cannot be directly used by voltage source inverters.

The recently proposed parabolic current control solves the frequency variation problem of hysteresis current control by employing a pair of parabolic

carriers as the control band. By the use of parabolic current control, approximate-constant switching frequency can be achieved. Due to the cycle-by-cycle control structure, it inherently has fast response speed and high precision. These advantages make it suitable for voltage source inverters, including stand-alone inverters, grid connected inverters, active power filters, and power factor correction applications.

However, parabolic current control has some limitations, such as dead-time effects, only working as bipolar PWM, complex hardware implementation, non-ideal converging speed. These problems are respectively solved in this dissertation and solutions include dead-time compensation, the implementation on dual-carrier unipolar PWM, sensorless parabolic current control, single-step current control. With the proposed dead-time compensation strategy, current control precision is improved and stable duty-cycle range are extended. Dual-carrier PWM implementation of parabolic current control has smaller harmonic filter size and lower power loss. Sensorless parabolic current control decreases the cost of system and enhances the noise immunity capability. Single-step current control pushes the convergence speed to one switching operation with simple implementation. High switching frequency is allowed and power density can be improved. Detailed analysis, motivation and experimental verification of all these innovations are covered in this

dissertation.

In addition, the duality phenomenon exists in electrical circuits, such as Thevenin's theorem and Norton's theorem, capacitance and inductance. These associated pairs are called duals. The dual of parabolic current control is derived and named parabolic voltage control. Parabolic voltage control solves the audible noise problem of burst mode power converters and maintains high efficiency in the designed boost converter.

Derivation of Parabolic Current Control with High Precision, Fast Convergence and Extended Voltage Control Application

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GENERAL AUDIENCE ABSTRACT

Current control strategy is an important topic in power converter design. Good current control strategy helps to control the quality of input or output waveform of power conversion systems. This dissertation studied an attractive current control strategy named parabolic current control. Parabolic current control solves some drawbacks of conventional current control strategies with enhanced performance. However, it still has some application limitations. This dissertation proposed four new strategies to solve the application limitations of parabolic current control. Motivated by the duality phenomenon, a voltage control strategy named parabolic voltage control is also proposed, serving as the dual of parabolic current control. By the use of parabolic voltage control, audible noise in some power conversion systems can be eliminated and conversion efficiency can be ensured. All these new ideas in this dissertation are carefully derived in theory and verified by experimental test results.

To my wife

Li Liang

To my parents

Shuzhen Zhang

Shihui Liu

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influenced my understanding of life. I believe he is happy to know my Ph.D. graduation in heaven. My special thanks are for my wife Li Liang, for her deep love with me, her unconditional support to my Ph.D. study, her hard work on taking care of our son, and her great contribution to this family. Final thanks are for my son Lawrence C. Zhang, who wakes me up so many times in midnight and who makes my life so wonderful and meaningful.

Lanhua Zhang

09/16/2016 in Blacksburg

CONTENTS

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NOMENCLATURE

V_{DC}: Dc-side voltage of the voltage source inverter

u_{ac}: Ac-side voltage of the voltage source inverter

u_{ab} : Voltage output between two inverter legs

L : Inductor of the output filter

S : Control signal generated by parabolic current controller

S_{pn}: Symbol for inductor current analysis

i_L : Current through output inductor

i_{ref} : Current reference (command) of i_L

δ : Current tracking error, $\delta = i_L - i_{ref}$

T_p^* : Time of $S = 1$ at steady state

T_n^* : Time of $S = 0$ at steady state

D^* : Duty-cycle at steady state

δ^* : Current tracking error at steady state

δ_p^* : Positive peak of δ^*

δ_n^* : Negative peak of δ^*

δ_{p-p}^* : Peak-to-peak value of δ^*

δ_p : Positive peak of δ

δ_n : Negative peak of δ

δ_{avg} : Average current tracking error over a switching period

δ_{p-p}: Peak-to-peak value of

t_{DT} : Dead-time

ΔI_0 : Value of δ at the transition starting point

ΔI_1 : Value of δ at the first switching operation

ΔI_i : Value of δ at the i_{th} switching operation

e_i : Converging error, defined as $e_i = |\Delta I_i| - |\delta^*|$. ($i = 0,1,2...$)

U_p : Voltage of u_{ab} when $S = 1$, $U_p = V_{DC}$ in this paper

U_n : Voltage of u_{ab} when $S = 0$, $U_n = -V_{DC}$ in this paper

T^* : Switching period at steady state

A_m: Control parameter of PCC, defined as $A_m = \frac{T^*}{2L}(U_p - U_n)$

$F_{PA}(t)$: Positive control carrier of PCC

$-F_{PA}(\tau)$: Negative control carrier of PCC

$\Delta\delta$: Difference between transient current tracking error and steady state current tracking error, defined as $\Delta\delta = \delta - \delta^*$

$\Delta\delta_1$: Vertical distance between δ_p^* and corner point A in Fig. 6.3

$\Delta\delta_2$: Vertical distance between δ_p^* and δ^* value at the instant of point A in Fig. 6.3

ΔT : Adjusting time of T_p^* to achieve single-step current control

v_c^* : Steady state control voltage

Δv_c : Adjustment of control voltage to achieve single-step current control

v_c : Actual control voltage for duty-cycle generating, defined as $v_c = v_c^* - \Delta v_c$

Δd : Adjustment of duty-cycle to achieve single-step current control

V_{am} : Peak-to-peak value of triangle carrier for PWM generation

T_p : Actual time when S = 1, defined as $T_p = T_p^* - \Delta T$

t_{shift}: Shifted time to move the sampling instant ahead

$i_{L1}^{'}$: Sampled inductor current at time instant $1'$ in Fig. 6.6

$i_{L2}^{'}$: Sampled inductor current at time instant $2'$ in Fig. 6.6

K_p: Equivalent gain of single-step current control

H_v: Gain of power stage

$T_i(s)$: Loop gain of the current loop

f_c: Crossover frequency of the current loop

δ_{avg_DT} : Average value of current tracking error considering dead-time

t_{err}: PWM resolution error

δ_{avg_err} : Average value of current tracking error considering t_{err}

V_{DCS}: Dc voltage source, combing R_s to serve as a current-sinking voltage source

u_{ref}: Voltage reference of ac side output voltage u_{ac}

i_R: Current going through electronic load under resistor mode

u_{ref} : Output voltage reference of burst-mode converter

u_{co}: Output voltage of the burst-mode converter

δ_v : Voltage tracking error, $\delta_v = u_{co} - u_{ref}$

$\delta_{p\text{-}v}$: The positive peak of the voltage tracking error

$\delta_{n\text{-}v}$: The negative peak of the voltage tracking error

$\delta_{pp\text{-}v}$: The peak-to-peak value of the voltage tracking error

S_v : Enable signal for current loop of the burst-mode converter

f^* : Burst frequency of the burst-mode converter

$F_{pa-v}(t)$: Positive control carrier of parabolic voltage control (PVC)

$-F_{pa-v}(\tau)$: Negative control carrier of PVC

A_{m-v} : Control parameter of PVC

P_{in} : The input power of the boost converter

P_{sw-act} : The input power under switching-active mode

T_{on-v} : The time of switching-active mode

T_{off-v} : The time of standby mode

D_v: Duty-cycle of control signal S_v

i_{Lm} : Inductor current of burst-mode boost converter

$i_{Lm\_\max}$: The maximum limit of the inductor current i_{Lm}

i_{SW}: Switch current of the burst-mode boost converter

i_D: Diode current of the burst-mode boost converter

I_{cs}: The average current of i_D over a switching cycle

i_o: Load current of the burst-mode converter

V_{DS}: Drain-source voltage of MOSFET in the burst-mode boost converter

Chapter 1 Introduction

1.1 Overview on Current control

Voltage source inverters (VSIs) are widely used in modern active power filters (APFs), uninterrupted power supplies (UPSs) and grid-tied photovoltaic (PV) inverters [1]. In order to ensure the response speed during transition and performance in steady state, a current control loop with a fast response and high control precision is required [2]-[29]. For grid-tied PV inverters, the total harmonic distortion (THD) of the output current strongly relies on the control performance of the current loop. Other applications that would require a high performance current control loop include stand-alone systems such as UPS, where the current loop with fast transient performance is required to minimize the distortion of output voltage waveform. This necessity for improved current control dynamics becomes more apparent when there are non-linear loads such as half-wave or full-wave rectifiers.

In order to implement a current loop with fast response and high tracking precision, numerous current control methods have been proposed [2]-[54]. These control methods can be divided into linear control and nonlinear control.

1.2 Linear Current Control

Most well-known current control strategy in power electronics system is

proportional-integral (PI) control [2],[30]. Current is measured and compared with current reference and the difference is fed back to the PI controller. Output of the PI controller is usually compared with constant frequency triangle carrier to generate switching signal. The implementation is to design the PI controller based on system small signal model [3]-[16]. With desired phase margin and gain margin, higher bandwidth and high low frequency gain are both preferred to achieved fast response. For voltage source inverters, small signal model changes with different output voltage and load. Then the design of the control parameters has to fulfill the worst case and control performance would be impacted.

Since the delays in control loop reduce the phase margin, bandwidth, and low frequency gain, one effective way to improve the response speed of PI control is to minimize the delays in the control loop [17]. Delays in digital system mainly relies on computation delay and pulse width modulation (PWM) delay. Predictive control is usually used to compensate the computation delay [19]-[25]. Since it employs the previous system state and system model to emulate the system function and obtain the future state, additional emulation error may be introduced. A real-time computation method with dual-sampling mode is discussed in [17] to remove the computation delay. THD level is improved but detailed step response time is not discussed. PWM delay can be

reduced by updating duty-cycle twice in a switching period [26].

1.3 Nonlinear Current Control

Nonlinear current control strategies can be divided into two main groups [27]. One group is based on the manipulation of modulation carriers; including one-cycle control [36]-[38], nonlinear-carrier (NLC) control [42]-[44], and charge control [45]-[46]. All control methods in this group are originally proposed for power factor correction (PFC) or APF applications. The current control carriers in this group are specified by the application topology where they are compared to the feedback variables and generate the modulation scheme. Since these control methods operate cycle-by-cycle, a fast dynamic response can be achieved using a constant switching frequency. The other group of current control methods is based on direct current tracking error control with the most common implementation being hysteresis current control [47]-[54] and peak current control [55]-[58]. The basic implementation of hysteresis control generates the switching signal by comparing the current tracking error with a hysteresis band. The main advantage of hysteresis control is that it inherently has a fast transient response. A well-known drawback of hysteresis current control is the variation of the switching frequency. The switching frequency can be held constant by varying the width of the hysteresis band.

1.3.1 Nonlinear-carrier Control

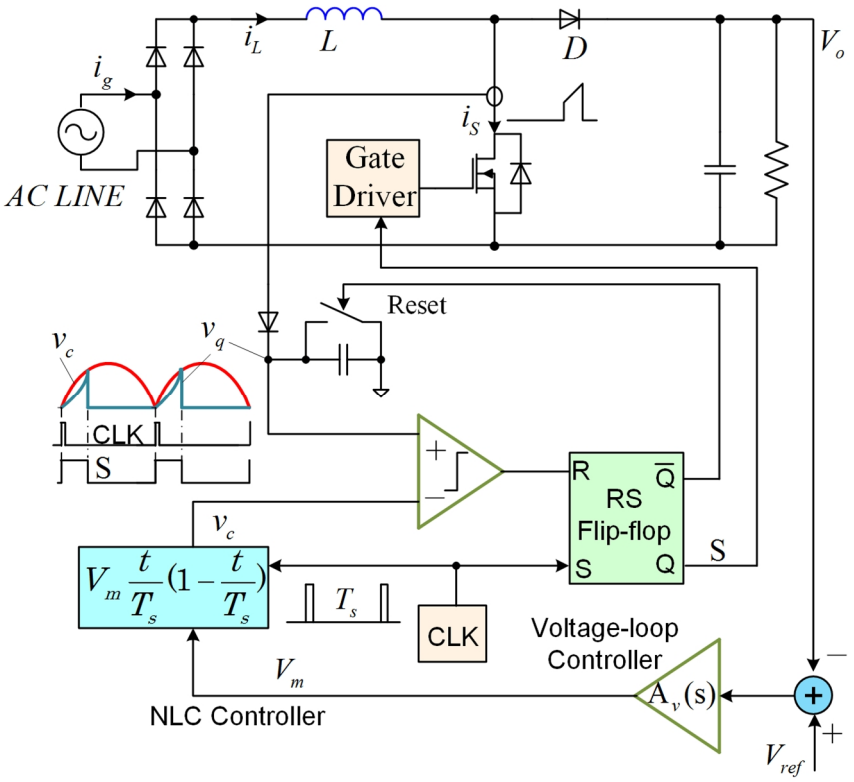


Fig. 1.1 Nonlinear-carrier control

Nonlinear-carrier (NLC) control was discussed in [42]-[44]. The control diagram of a boost PFC and its typical waveforms are shown in Fig. 1.1 [30],[42]. The derivation of NLC control is to see the input characteristic of the boost converter as an emulated resistor so the power factor correction is achieved. In Fig. 1.1, voltage loop controller generates the amplitude of the nonlinear carrier. The turn-off instant of the switch is controlled by the comparison between the nonlinear carrier and the integration of the switching current. The turn-on instant of the switch is controlled by the clock signal with constant switching frequency. Another NLC controller was derived based on

peak current sensing instead of the integration of switching current and it has the inherent instantaneous over-current protection for the main switch [42].

1.3.2 Peak Current Control

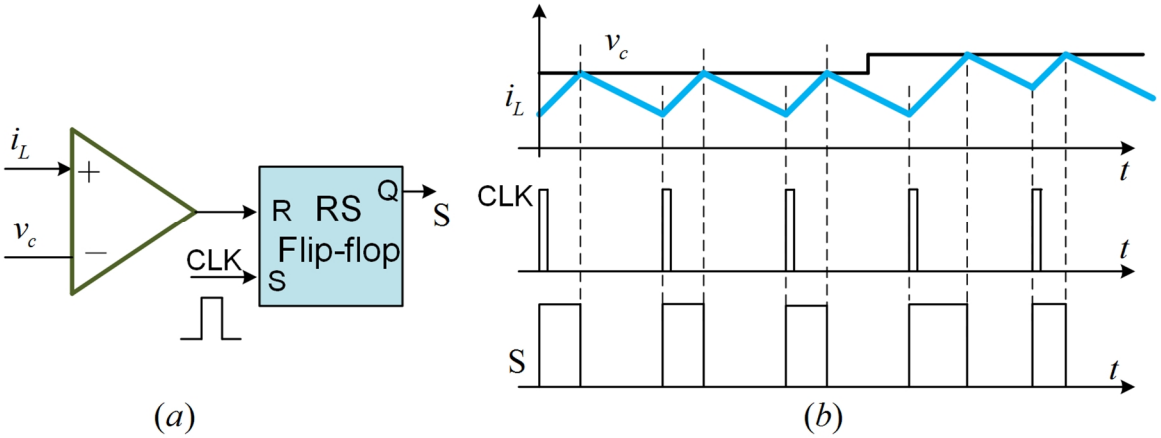


Fig. 1.2 Peak current control

Peak current control is first proposed in [55]. The waveforms of a buck converter with peak current control are shown in Fig. 1.2. v_c is the current reference. Inductor current i_L is measured and compared with v_c to determine the turn-off instant. When the inductor current intersects with the control voltage, top switch is turned off and inductor current starts to decrease. Turn-on signal comes from a clock with constant frequency. The stability of peak current controlled Buck converter relates to its duty-cycle [56]-[62]. With duty-cycle larger than 0.5, sub-harmonic oscillation problem would be noticed. To solve the sub-harmonic oscillation problem, slope compensation is proposed and widely employed [56]. Over-compensation impacts the control performance

so the compensation slope needs to be adjusted with different duty-cycle [63]. A unified three-terminal switch model of peak current control is discussed in [64]. Texas Instruments has the digital micro-controller TMS320F2803x with the function of peak current mode and slope compensation [65].

1.3.3 Hysteresis Current Control

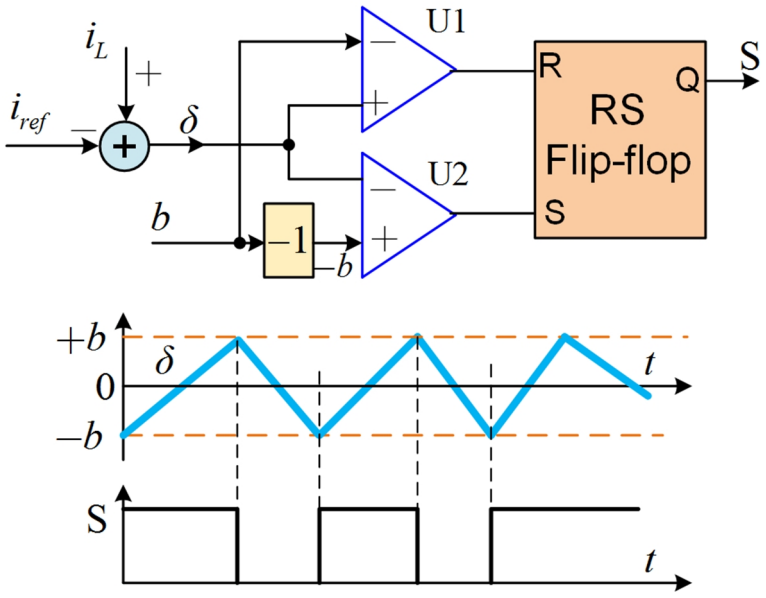


Fig. 1.3 Hysteresis current control

Hysteresis current control is proposed in [47] and the basic operation principles is show in Fig. 1.3. i_{ref} is the current reference and i_L is the measured inductor current. The difference between them is the current tracking error δ. Control band is (–b, +b). Operational principles includes: S=1, power switch is turned on and δ starts to increase until it intersects with control band +b; Then switch is turned off and δ starts to decrease until it

intersects with control band –b; After that, power switch is turned on again initializing next switching cycle. Due to the cycle-by-cycle operation, hysteresis current control has no stability issue and provides a fast current response with high precision [44]-[54].

However, for VSI applications, the well-known problem of hysteresis current control is the switching frequency variation. Switching variation problem would impact the design of harmonic filter and electromagnetic interference (EMI) filter. Switching loss would also increase with high switching frequency operation. Quite a few papers have proposed solutions to solve the switching frequency variation problem [48]-[54]. Constant switching frequency can be achieved by using a phase-locked-loop (PLL) [48],[49], current tracking error feedback [53], or adaptive control methods [54]. In order to implement these constant switching frequency methods, an additional control loop or digital controller is needed, increasing the system complexity and decreasing the system bandwidth.

1.3.4 One-cycle Controlled APF

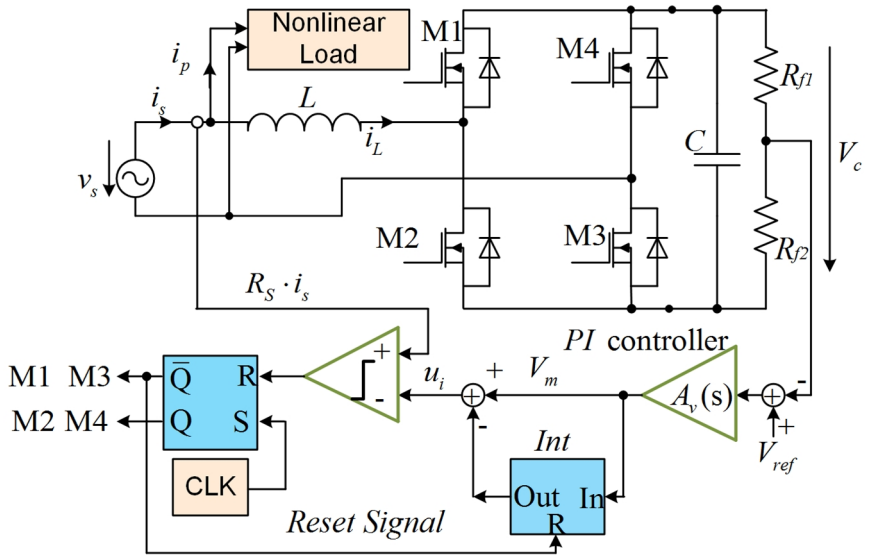


Fig. 1.4 One-cycle controlled APF

One-cycle control is discussed in [33]-[38]. The concept of one-cycle control is proposed in [36],[37] and a one-cycle controlled APF is proposed in [38]. Fig. 1.4 indicates a one-cycle controlled APF. The difference between traditional PWM and one-cycle control is discussed in [35]. It is concluded that one-cycle control is an improved PWM strategy with adjustable carrier slope-ratio.

Conventional APFs generate the current reference of the input inductor based on the measured harmonic current. To detect the harmonic current, various detecting strategies have been proposed, such as instantaneous reactive power theory [39], adaptive strategies [40],[41]. Another APF control strategy does not generate the current reference of the input inductor, such as the APF in Fig. 1.4. Instead, it just controls the sum current of APF and

nonlinear load to be sinusoidal with unity power factor. These two strategies are studied and compared in [33],[34]. It is concluded that the detected harmonic current is just a feedforward signal in dc-side voltage control loop and its existence impacts the current response in transition and current precision at steady state. Then it is not desired to detect the harmonic current in APF system.

Similar as NLC control, one-cycle controlled APF derives the control strategy based on treating the whole system as a pure resistor. In this way grid side current can be automatically controlled to be sinusoidal with unity power factor. In Fig. 1.4, voltage control generates the control voltage V_m. Control carrier is obtained based on subtracting the integration of V_m from V_m. The grid current is measured and compared with the control carrier. With this control strategy, PLL block is not required to get the phase of grid voltage. Thanks to the cycle-by-cycle operation, current response is very fast which makes it very suitable for APF application. However, the derivation does not consider the voltage drop on the input inductor and the APF shows current tracking error at steady state which requires additional compensation [38].

1.4 Objectives of The Work

Even the parabolic current control has fast response and high control precision with approximately constant switching frequency, it still has some

issues in actual applications. These issues include: 1) Dead-time impacts the control precision and switching frequency; 2) Parabolic current control cannot be directly used on dual-carrier PWM; 3) Traditional implementation of parabolic current control utilized analog comparison, which is sensitive to noise and make the circuit complex; 4) Parabolic current control still needs serval switching operations to converge to the steady state.

This dissertation will explore the possible solutions to solve these application limitations. Meanwhile, motivated by the duality phenomenon in electrical circuits, parabolic voltage control should be derived and applied to the proper applications.

1.5 Outline of The Dissertation

In this dissertation, seven chapters are included. Chapter 2 discusses the derivation of parabolic current control. After that, five topics are presented and each topic lasts for a single chapter. Chapter 3 discusses the effects of dead-time and proposed a compensation strategy with improved precision and switching frequency convergence. Chapter 4 presents the new strategy to implement PCC on dual-carrier PWM. Chapter 5 introduces a sensorless implementation of PCC, which eliminates the need of complex analog circuit with improved stability. Chapter 6 presents a single-step current control with faster convergence speed. Chapter 7 proposes the parabolic voltage control,

solving the audible noise of burst mode converter. Chapter 8 is the conclusion and future view of the dissertation.

1.6 List of Publications

Different parts of this dissertation have been published or are being published in international journals or conference proceedings. These publications are listed below.

L. Zhang, B. Gu, J. Dominic, B. Chen, C. Zheng, and J. -S. Lai, "A dead-time compensation method for parabolic current control with improved current tracking and enhanced stability range," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3892-3902, Jul. 2015

L. Zhang, J. Dominic, B. Gu, B. Chen, C. Zheng, and J. -S. Lai, "The implementation of parabolic current control for dual-carrier PWM", in *Proc. of IEEE APEC 2015.*, pp. 1487-1492, Mar. 2015

L. Zhang, R. Born, B. Gu, B. Chen, C. Zheng, X. Zhao, and J.-S. Lai, "A sensorless implementation of the parabolic current control for single-phase stand-alone inverters", *IEEE Trans. Power Electron.,* vol. 31, no. 5, pp. 3913-3921, May. 2016

L. Zhang, R. Born, and J.-S. Lai, "Single-Step Current Control for Voltage Source Inverters with Fast Transient Response and High Convergence Speed", *IEEE Trans. Power Electron.* under review.

L. Zhang, R. Born, X. Zhao, B. Gu, and J.-S. Lai, "A parabolic voltage control strategy for burst mode converters with constant burst frequency and eliminated audible noise", *IEEE Trans. Power Electron.,* vol. 31, no. 12, pp. 8572-8580, Dec. 2016

Chapter 2 Derivation of Parabolic Current Control

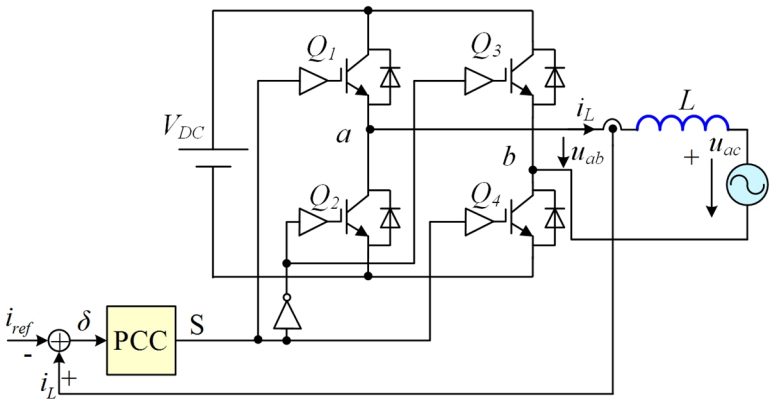


Fig. 2.1 Voltage source inverter with PCC

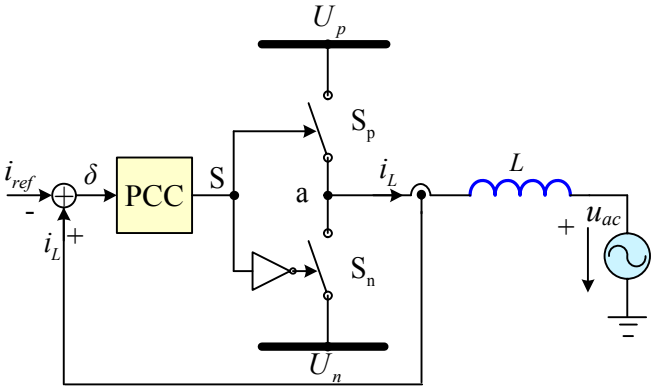


Fig. 2.2 Simpified diagram of a VSI with PCC

A typical single phase H-bridge VSI with PCC is shown in Fig. 2.1, where Q_1 Q_4 are turned on/off at the same time and Q_2 Q_3 are turned on/off at the same time. So Fig. 2.1 can be summarized into the diagram shown in Fig. 2.2 [27]. L is the output inductor. U_p and U_n are the positive and negative dc-bus voltage respectively, $U_p = V_{DC}, U_n = -V_{DC}$. S is the control signal generated by the parabolic current controller. S_p and S_n are the top and bottom switches.

When $S=1$, S_p is on and S_n is off, and when $S=0$, S_p is off and S_n is on. i_L, i_{ref} and δ represents inductor current, current reference, and current tracking error respectively. The current tracking error is defined as

$$\delta = i_L - i_{ref}. \tag{2.1}$$

δ_p and δ_n are the positive and negative peak values of the current tracking error respectively. Peak-to-peak value of δ is $\delta_{p\text{-}p}$. T_p is the turn-on time of switch S_p and T_n is the turn-on time of switch S_n. T is the switching period.

When $S=1$, ignore the resistor of the inductor [27]-[30],

$$L\frac{di_L}{dt} = U_p - u_{ac} > 0. \tag{2.2}$$

When $S=0$,

$$L\frac{di_L}{dt} = U_n - u_{ac} < 0. \tag{2.3}$$

Substitute (2.1) to (2.2),

$$L\frac{d\delta}{dt} = U_p - u_{ac} - L\frac{di_{ref}}{dt} \tag{2.4}$$

Considering $\frac{d\delta}{dt} = \frac{\delta_{p-p}}{T_p}$, (2.4) changes to

$$L\frac{\delta_{p-p}}{T_p} = U_p - u_{ac} - L\frac{di_{ref}}{dt}. \tag{2.5}$$

Similarly (2.3) changes to

$$-L\frac{\delta_{p-p}}{T_n} = U_n - u_{ac} - L\frac{di_{ref}}{dt}. \tag{2.6}$$

Combine (2.5) and (2.6)

$$L\delta_{p-p}(\frac{1}{T_P} + \frac{1}{T_n}) = U_p - U_n \tag{2.7}$$

Considering $T = T_p + T_n$ and $\delta_{p-p} = \delta_p - \delta_n = 2\delta_p = -2\delta_n$, (2.7) changes to

$$\delta_p = -\delta_n = \frac{T}{2L}(U_p - U_n)[\frac{T_p}{T} - (\frac{T_p}{T})]^2 = \frac{T}{2L}(U_p - U_n)[\frac{T_n}{T} - (\frac{T_n}{T})]^2 \tag{2.8}$$

It is seen in (2.8) that with different turn-on time or turn-off time and constant switching frequency, the value of δ_p or δ_n lines up a parabolic curve. If using this curve as current control band, constant switching frequency could be achieved. This is the main motivation of the parabolic current control. Then the operation principle of PCC is in Fig. 2.3. The parabolic carrier is given by

$$F_{PA}(t) = A_m[\frac{t}{T^*} - (\frac{t}{T^*})^2], \quad 0 \le t \le T^* \tag{2.9}$$

$$A_m = \frac{T^*}{2L}(U_p - U_n) \tag{2.10}$$

Where T^* is the desired switching period and also the period of the parabolic carrier. At steady state the desired switching period is

$$T^* = T_p + T_n. \tag{2.11}$$

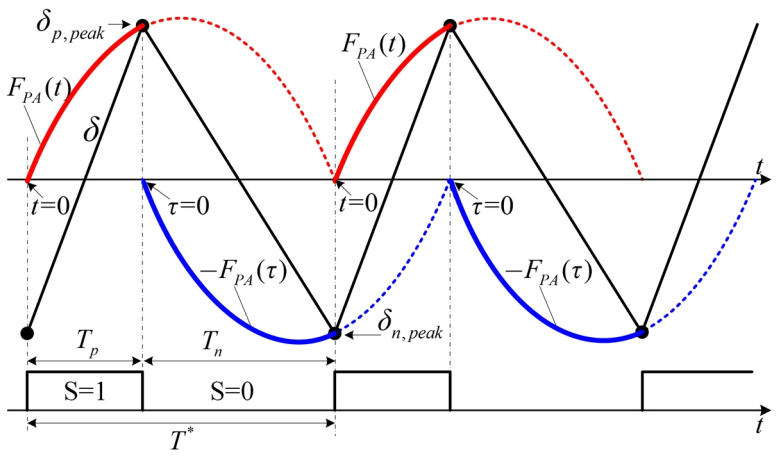


Fig. 2.3 Operation principle of PCC

As shown in Fig. 2.2 and Fig. 2.3, S_p is turned on during T_p and the inductor current increases. When the current tracking error δ intersects with the positive parabolic carrier F_{PA}(t), S_p is turned off and S_n is turned on. At the same time, the current tracking error begins to traverse to the opposite polarity parabolic carrier and the negative parabolic carrier starts to generate. The current tracking error decreases until it intersects with the negative parabolic carrier $-F_{PA}(\tau)$, then S_n is turned off and S_p is turned on again, initiating the transition into the next switching period. As a result, the current tracking error is precisely controlled in the parabolic carrier band and

$$\delta_p = -\delta_n = F_{PA}(DT^*). \tag{2.12}$$

Where D is the required duty-cycle at steady state and it is defined as

$$D = \frac{T_p}{T^*}. \tag{2.13}$$

Chapter 3 Dead-time Compensation

3.1 Introduction

In order to avoid the problem of shoot-through between the high-side and low-side switches in an inverter leg, dead-time is employed in pulse-width modulation (PWM) based VSIs. Due to the dead-time, the output voltage or current of VSIs becomes distorted and phase-shifted [68], [69]. For parabolic current controlled VSIs, dead-time has an impact on the current tracking precision, causes the deviation in the switching frequency, and decreases the usable duty-cycle range. Several methods have been proposed to eliminate or compensate the effect of dead-time for conventional PWM systems [68], [70]-[75]. The implementations proposed in [68] and [70] eliminate the need for dead-time in the modulation scheme based on the direction of the output current. When the direction of the output current is going out of the inverter leg, the top active switch and anti-parallel diode of the bottom switch conducts the current complementarily. The driver signal for the bottom switch can be disabled negating the requirement for dead-time. Similarly, when the direction of the output current is going into the inverter leg, the driver signal for the top switch can be disabled. This method relies on the direction of the output current, which can be determined by the conduction status of each switch.

Alternative methods of dead-time compensation include [74] and [75], which is implemented by adding a compensation voltage to the command voltage. The compensation voltage is obtained based on the dead-time, switching frequency, and direction of the output current. The compensation method based on the adjustment of the command voltage successfully eliminates the dead-time effects for conventional PWM inverters using constant frequency triangle carriers. Since there are no constant frequency triangle carriers in PCC inverters, these compensation methods are not able to be directly utilized.

In this chapter, the dead-time effect on PCC is analyzed, including the current tracking precision, switching frequency, and effects on the duty-cycle range. In order to eliminate the effects of dead-time on PCC, a compensation method by using an improved parabolic carrier is proposed. To verify the analysis of the dead-time effect on the current loop and the effectiveness of the proposed compensation method, a H-bridge VSI employing PCC has been designed and tested. Due to the improved current tracking precision and the increased duty-cycle range, the proposed compensation method is an effective method that eliminates the effects of dead-time on PCC.

3.2 Dead-Time Effect

3.2.1 Dead-time Analysis

In order to analyze the effect of dead-time on PCC it is necessary to illustrate the current path of an inverter leg in relation to output current direction. Fig. 3.1 (a) shows the typical configuration of a VSI with two IGBTs in an inverter leg with the direction of the current going out of the inverter leg being defined as positive. The current path in the switch leg is determined by the direction of the output current, as shown in Fig. 3.1 (b). When $i_L < 0$, if the bottom switch S_n is turned on, the current goes through S_n , during the same switching period when the switch is turned off the current freewheels through the antiparallel diode of the top switch S_p. Similarly, when $i_L > 0$, the current goes through either the top switch or the antiparallel diode of the bottom switch.

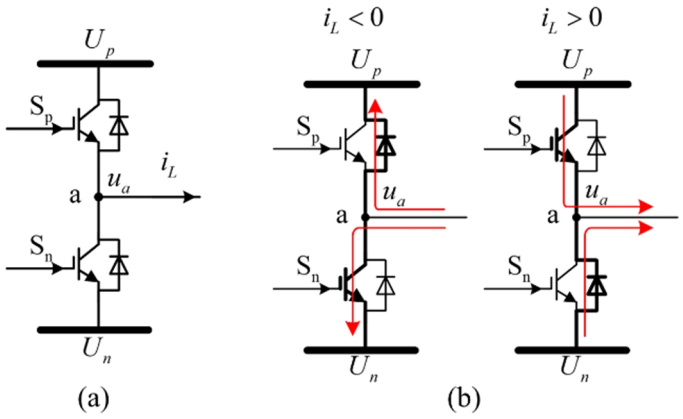


Fig. 3.1 Current path of an inverter leg in relation to current direction

The operation principle of PCC with dead-time is shown in Fig. 3.2 when

the output current is less than zero. As shown in the figure, the dead time t_{DT} occurs during the switch transition. When the current tracking error increases and intersects with the positive parabolic carrier at point C, the control signal S from PCC controller changes to zero and the top switch S_p is turned off. Due to the dead-time t_{DT}, the bottom switch S_n does not turn on immediately. The current continues in the same direction by freewheeling through the antiparallel diode of the top switch and the current tracking error keeps increasing during the dead-time. As a result, the current tracking error exceeds the positive parabolic carrier, which causes the current to overshoot. After the dead-time period the bottom switch is turned on and starts to conduct the current, causing the current tracking error to alternate its direction indicated at point B. Then the current tracking error decreases and intersects with the negative parabolic carrier at point E. S changes to one and the bottom switch S_n is turned off. Due to the direction of the output current, the antiparallel diode of top switch conducts the current immediately and the current tracking error alternates the direction without current overshoot. It can be seen that the current tracking error intersects with the negative parabolic carrier at point E instead of point G planned by the original carriers without considering the dead-time. It is important to note that due to the dead-time, a time delay t_a is present between points G and E. By combining the

desired switching period with the time delay t_a, the switching frequency can be calculated. The main effects of dead-time on PCC include a decrease in the switching frequency from the desired value and the average current tracking error in a switching period is not zero.

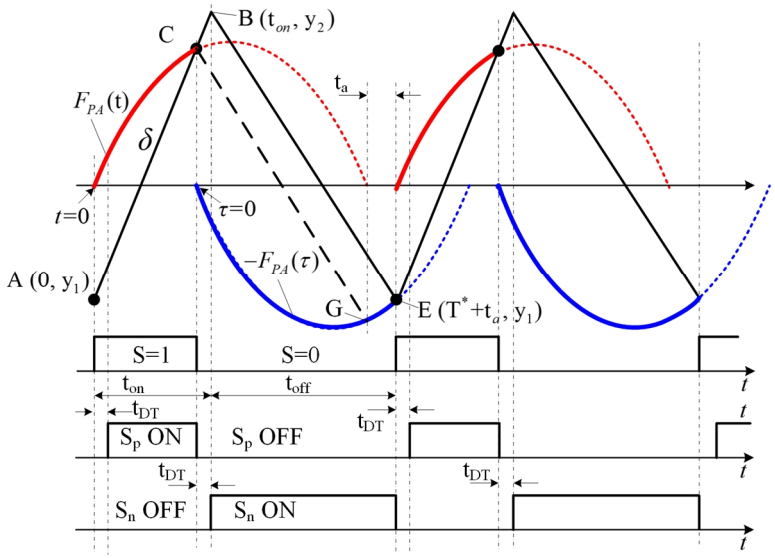


Fig. 3.2 PCC with dead-time when $i_L < 0$

3.2.2 Stability Range

Due to the dead-time and the corresponding time delay, when the duty-cycle is very small or very large, the current tracking error would miss one or more parabolic carriers. In Fig. 3.3 this is illustrated by the ideal PCC intersection being at point G, while the effects of dead-time cause the intersection of the current tracking error with the carrier to deviate to point F. The operating condition during this period is defined as an unstable state in this paper. Under this operating condition, the switching frequency is far away from the desired

point and voice-band noise may be present. The operation in the unstable state causes the peak-to-peak value of the current tracking error to increase and as a result the current tracking precision would be impacted negatively. In order to analyze the effects of dead-time on the current tracking precision and switching frequency, the stable duty-cycle range of a PCC system with dead-time should be determined first.

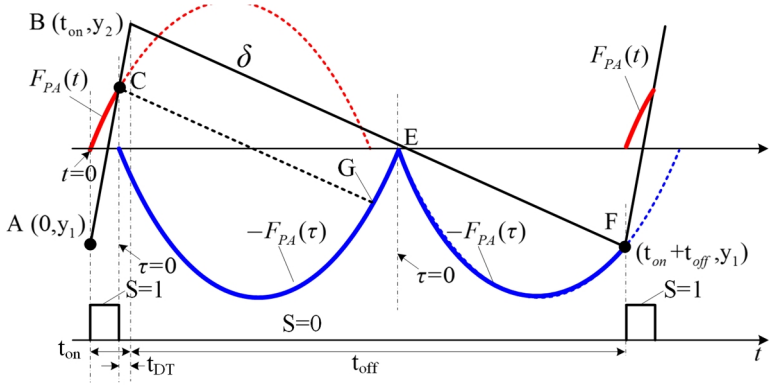


Fig. 3.3 Diagram for stability analysis when $i_L < 0$

In this chapter, the desired switching frequency f_s^* is 20 kHz and an output inductance of 3.3 mH is selected. The dc-bus voltage is set to 400 V, then $U_p = -U_n = 400$ V. $A_m = 6.061$ is obtained based on the selected parameters. A dead-time of 2 μs is employed in the switch transition. In the case of the small duty-cycle range, the boundary between stable operation and unstable operation occurs when the decreasing current tracking error intersects with the parabolic carrier at the start point of the second negative carrier, as shown in Fig. 3.3. The current tracking error intersects with the positive parabolic

carrier at point C and alternates its direction at point B. The current tracking error then misses the first negative parabolic carrier and intersects with the second negative carrier at point F. Based on geometrical relationship in the Fig. 5, the minimum stable duty-cycle can be obtained:

$$\begin{cases} m_2 = \dfrac{-F_{PA}(t_{off} - (T^* - t_{DT}))}{t_{off} - (T^* - t_{DT})} \\ \dfrac{t_{on}}{D} = \dfrac{t_{off}}{1-D} \\ m_1 t_{on} = -m_2 t_{off} \\ F_{PA}(t_{on} - t_{DT}) = y_1 + m_1(t_{on} - t_{DT}) \end{cases} . \qquad (3.1)$$

t_{on} and t_{off} are the time intervals when the current tracking error increases and decreases in a switching period. m_1 and m_2 are defined as the ramp rate of current tracking error during T_p and T_n in Fig. 2.3 respectively,

$$\begin{cases} m_1 = \dfrac{2A_m(1-D)}{T^*} \\ m_2 = \dfrac{-2A_m D}{T^*} \end{cases} . \qquad (3.2)$$

Solving (3.1) and (3.2) the minimum duty-cycle can be obtained with D_{min} = 0.116. The maximum duty-cycle can be obtained in a similar manner. The finial stable duty-cycle range for the operating condition $i_L < 0$ is given by

$$D \sim (0.116,\ 0.917). \qquad (3.3)$$

For the operating condition $i_L > 0$, the stable duty-cycle range is given by

$$D \sim (0.083,\ 0.884). \tag{3.4}$$

3.2.3 Current Tracking Precision

With the calculated operating duty-cycle range, the average current tracking error in a switching period can be obtained based on Fig. 3.2. The following equations hold true for the waveforms in Fig. 3.2:

$$\begin{cases} y_1 = -F_{PA}(t_{on} - t_a - t_{DT}) \\ F_{PA}(t_{on} - t_{DT}) = y_1 + \dfrac{y_2 - y_1}{t_{on}}(t_{on} - t_{DT}). \\ y_2 = y_1 - m_2 t_{off} \end{cases} \tag{3.5}$$

t_a is the time interval between the adjacent positive parabolic carriers or the adjacent negative parabolic carriers. t_{on} and t_{off} can be given by the product of the duty-cycle and the required switching period:

$$\begin{cases} t_{on} = D(T^* + t_a) \\ t_{off} = (1 - D)(T^* + t_a) \end{cases}. \tag{3.6}$$

Combining (10) and (11), the time interval between the adjacent carriers is:

$$t_a = -\frac{T^*(2D^2 - 2D + 1) + 2t_{DT}(1 - 2D) - \sqrt{T^{*2}(2D^2 - 2D + 1)^2 + 4t_{DT}\left[T^*(2D^2 - 2D + 1) - t_{DT}\right]}}{2(2D^2 - 2D + 1)}. \tag{3.7}$$

Substituting t_a into (3.5), y_1 and y_2 are obtained.

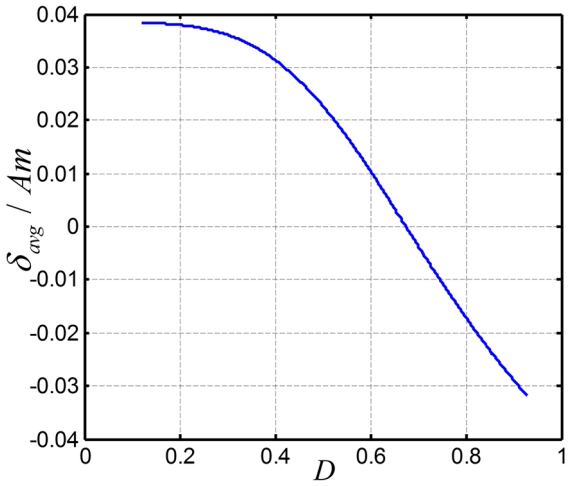
δ_{avg} is defined as the average current tracking error in each switching period,

which is given by:

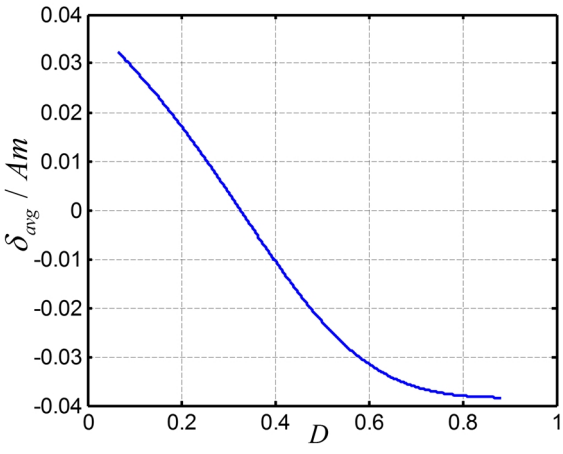
$$\delta_{avg} = \frac{1}{T^* + t_a} \int_0^{T^* + t_a} \delta dt = \frac{y_2^2 - y_1^2}{2(|y_1| + |y_2|)}. \tag{3.8}$$

The switching frequency is given by

$$f_s = \frac{1}{T^* + t_a}. \tag{3.9}$$

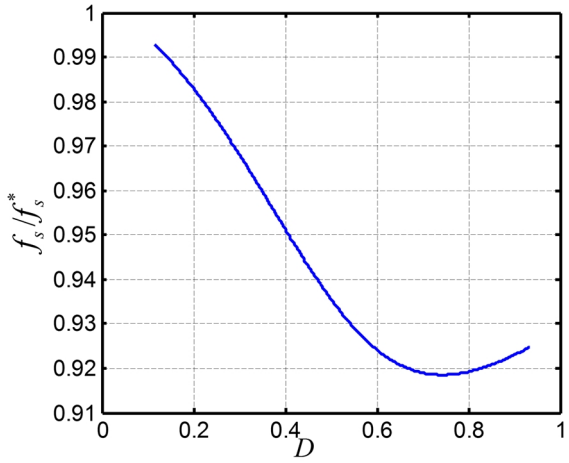


(a)

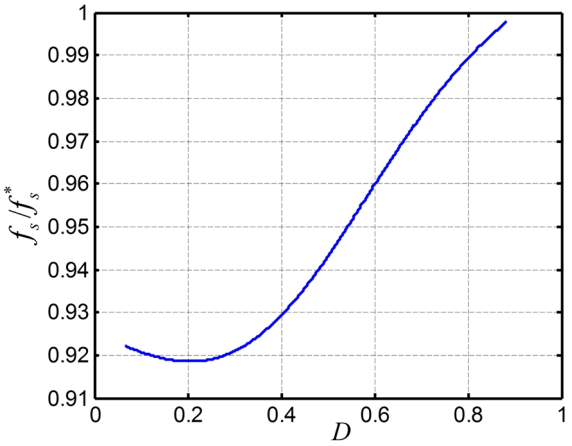


(b)

Fig. 3.4 δ_{avg} with dead-time: (a) δ_{avg} when $i_L < 0$; (b) δ_{avg} when $i_L > 0$.



(a)



(b)

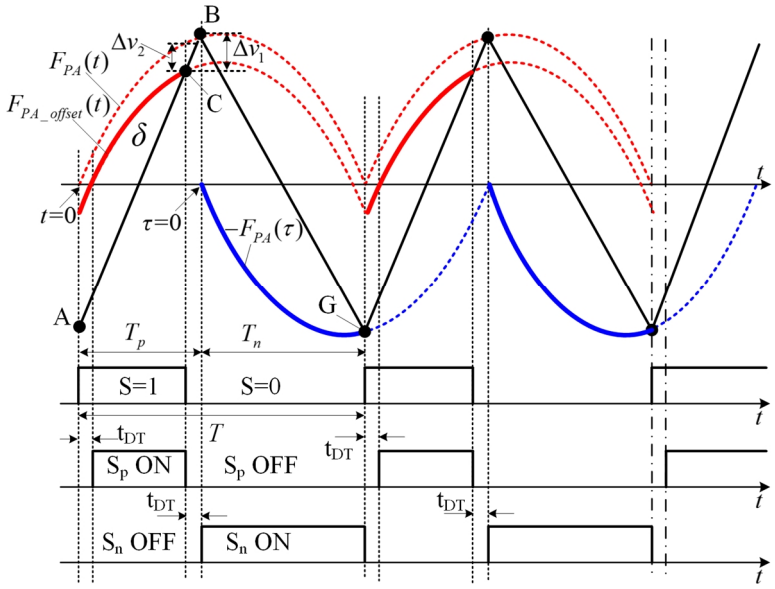
Fig. 3.5 Switching frequency with dead-time: (a) Switching frequency when $i_L < 0$; (b) Switching frequency when $i_L > 0$.

With the given circuit parameters, from (3.5) and (3.8), the average current tracking error δ_{avg} normalized to the parabolic carrier A_m versus the stable duty-cycle range are obtained under the operating conditions: $i_L < 0$ and $i_L > 0$, shown in Fig. 3.4. As the figures indicate, due to the dead-time, δ_{avg} deviates from zero and varies with the change of the duty-cycle. For both operating conditions when the output current direction is different, the

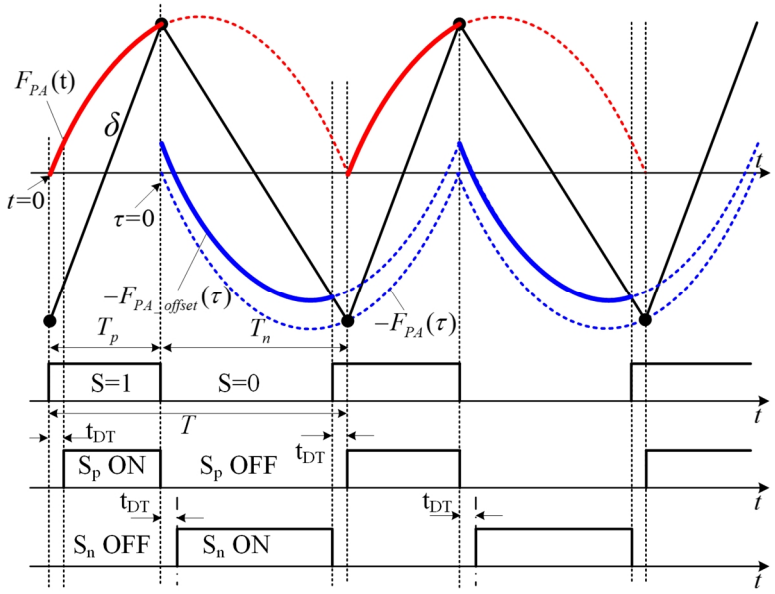
normalized switching frequency is obtained based on (3.9) and presented in Fig. 3.5. From the figure it is clearly evident that the dead-time causes the switching frequency to deviate to a value lower than the desired switching frequency of 20 kHz. Since the switching frequency and average current tracking error both vary with the duty-cycle indicate that the switching frequency of the VSI is not constant.

3.3 Proposed Compensation Method

In order to compensate for the effects of dead-time on the system, the parabolic current controller should generate the switching signal ahead of the signal for the conventional case as shown in Fig. 3.6. Fig. 3.6 (a) and Fig. 3.6 (b) shows the operating principle of the proposed compensation method for the operating conditions $i_L < 0$ and $i_L > 0$ respectively. In Fig. 3.6 (a), the intersection between the parabolic carrier and the current tracking error can be moved from point B to point C by using the improved carrier $F_{PA\_offset}(t)$. If the time between point B and point C is ensured to be equal to the dead-time t_{DT}, then the current tracking error would alternate its direction at point B, causing the current tracking error control to be the same as that in the ideal case shown in Fig. 2.3. Then the dead-time at the falling edge of S can be compensated and the current tracking error can be eliminated.



(a)



(b)

Fig. 3.6 Operating principle of PCC with the proposed dead-time compenstion method: (a) $i_L < 0$; (b) $i_L > 0$.

In order to determine the improved parabolic carrier, an offset Δv_2 is added to the original positive parabolic carrier, as shown in Fig. 3.6 (a). For the operating condition $i_L > 0$, the offset is added to the negative parabolic carrier,

as shown in Fig. 3.6 (b). The compensation offset Δv_2 can be calculated based on the geometrical relationship in Fig. 3.6 (a):

$$\begin{cases} \Delta v_2 = F_{PA}(T_p - t_{DT}) - (F_{PA}(T_p) - \Delta v_1) \\ \dfrac{\Delta v_1}{t_{DT}} = \dfrac{2F_{PA}(T_p)}{T_p} \end{cases}. \tag{3.10}$$

Then Δv_2 is obtained as

$$\Delta v_2 = A_m(\frac{t_{DT}}{T^*} - (\frac{t_{DT}}{T^*})^2) = F_{PA}(t_{DT}). \tag{3.11}$$

From this equation, it can be concluded that the compensation offset is constant related to dead-time t_{DT} and independent of time. The improved carrier $F_{PA\_offset}(t)$ and $F_{PA\_offset}(\tau)$ in Fig. 3.6 are given by

$$\begin{cases} F_{PA\_offset}(t) = F_{PA}(t) - \Delta v_2 = F_{PA}(t) - F_{PA}(t_{DT}) \\ F_{PA\_offset}(\tau) = -(F_{PA}(\tau) - \Delta v_2) = -(F_{PA}(\tau) - F_{PA}(t_{DT})) \end{cases}. \tag{3.12}$$

For the operating condition $i_L < 0$, since the top switch conducts the current immediately when the bottom switch is turned off, then no dead-time compensation is needed during the transition at the rising edge of the control signal *S*. Similarly, for the operating condition $i_L > 0$, no dead-time compensation is needed at the falling edge of *S*. As a result, no change is necessary for the negative carrier during $i_L < 0$ and for the positive carrier during $i_L > 0$.

At the same time for the operating condition $i_L < 0$, since the current

tracking error alternates its direction at point B, then the start point of the negative parabolic carrier needs to be delayed t_{DT} from the falling edge of *S*. Similarly, for the operating condition $i_L > 0$, the start point of the positive parabolic carrier needs to be delayed t_{DT} from the rising edge of S. As shown in Fig. 3.6, for both cases, with the proposed compensation method, the current tracking error is controlled to be the same as the ideal case shown in Fig. 2.3 and the average current tracking error is zero over the entire duty-cycle range. The peak values of current tracking error and current tracking error are also the same as that in Fig. 2.3. Thus the effect of dead-time on current tracking precision is eliminated. The time interval between adjacent parabolic carriers is eliminated, which means that the switching frequency deviation also goes to zero.

As well known, due to the tolerance of current sensor and conditioning circuits, the direction of the output current may be not precisely detected during zero crossing section. In order to avoid this issue, a hysteresis band is employed in this paper. If the output current is between the lower limit and higher limit of the hysteresis band, the controller suspends the dead-time compensation. Otherwise the controller works under the operating condition based on the detected direction of the output current.

3.4 Experimental Verification

In order to verify the effectiveness of the proposed compensation method a full-bridge VSI prototype with bipolar operation is designed and tested. In the experiment PCC is utilized as the current controller, which is implemented with a FPGA EP4CE15E22 from Altera shown in Fig. 3.7. Fairchild FGY75N60SMD IGBTs are used as the main switches in the experiment. The parabolic carrier, improved carrier, and current reference are generated by the digital-to-analog converter (DAC). Gating signals are generated by the FPGA with the required dead-time. The capacitance of the output filter is selected to be 50 μF. Using a constant dc output current reference and proper configuration of the load resistance, different duty-cycles can be tested. In order to test the performance of the controller over the entire duty-cycle range, the output resistor can be replaced with a dc power supply. Other circuit parameters are the same as stated in chapter II. The picture of the prototype is shown in Fig. 3.8 and the experimental results are shown in Fig. 3.13 to Fig. 3.21.

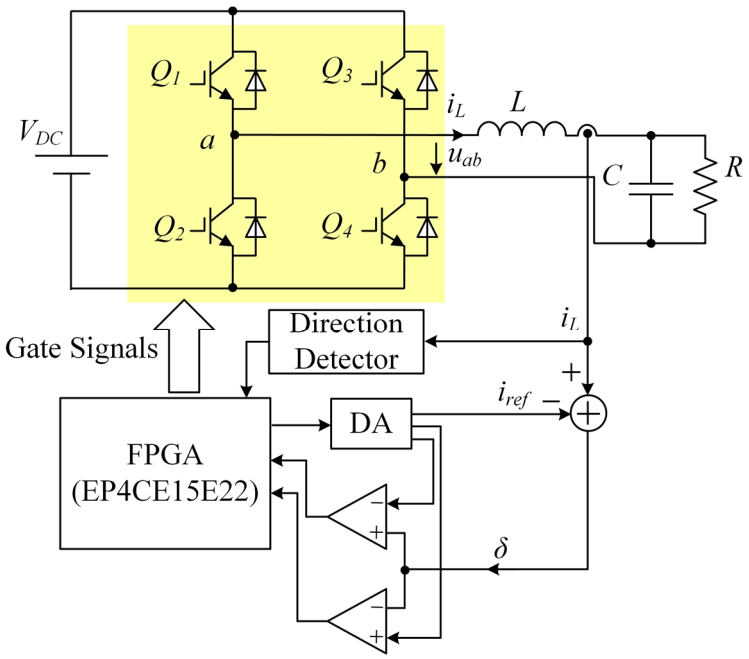


Fig. 3.7 Diagram of the prototype hardware

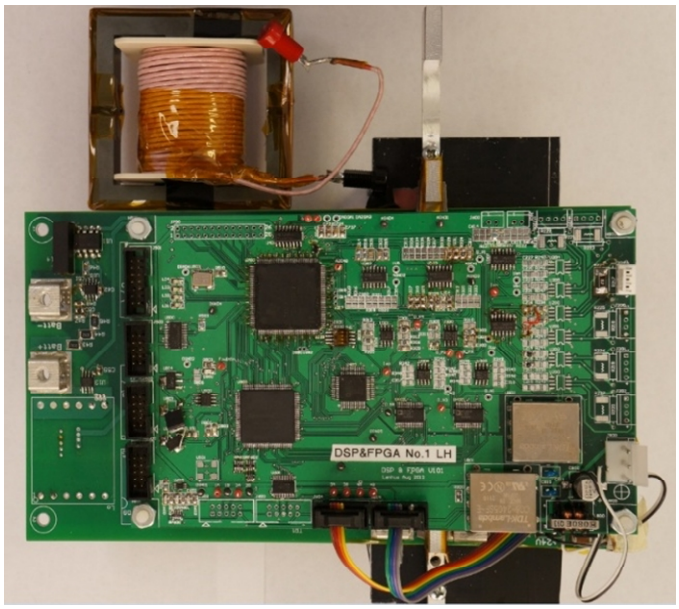


Fig. 3.8 Picture of the prototype hardware

Fig. 3.9 to Fig. 3.12 show the detailed experimental waveforms including current tracking error δ, output current of the inverter leg i_L, parabolic carriers $F_{PA}(t)$, - $F_{PA}(\tau)$, and improved parabolic carriers $F_{PA\_offset}(t)$, - $F_{PA\_offset}(\tau)$, under four different operating conditions: $i_L < 0$ and $D < 0.5$ in Fig. 3.9, $i_L < 0$ and

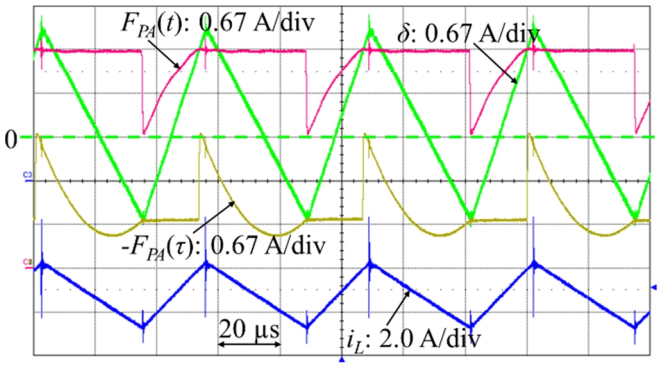
$D > 0.5$ in Fig. 3.10, $i_L > 0$ and $D < 0.5$ in Fig. 3.11, $i_L > 0$ and $D > 0.5$ in Fig. 3.12. It's clearly seen in Fig. 3.9 and Fig. 3.10 that the current tracking error exceeds the positive parabolic carrier and does not exceed the negative parabolic carrier under the operating condition $i_L < 0$. While in Fig. 3.11 and Fig. 3.12 the current tracking error exceeds the negative parabolic carrier and does not exceed the positive parabolic carrier under the operating condition $i_L > 0$.

The average current tracking error normalized to A_m is obtained by averaging the current tracking error δ in each switching period as listed in Table 3.1. It can be seen that the normalized average current tracking error with the proposed compensation method is significantly reduced under all operating conditions. As the experimental waveforms illustrate, current tracking error δ with the proposed compensation method has an average value close to zero, which means the average current tracking error is much smaller.

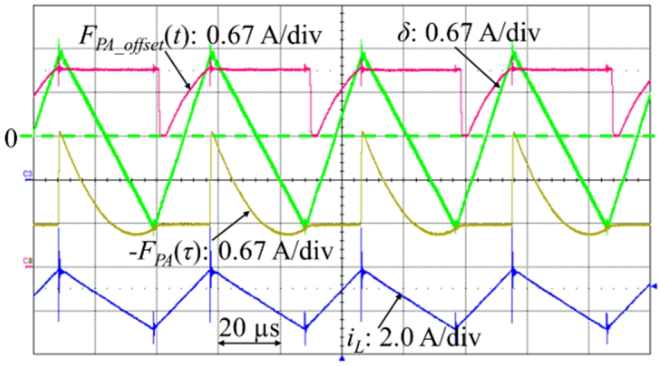
Table 3.1 Normalized experimental current tracking error

Operating condition	Err_test	Err_test_wi
i_{ref} = –5.3 A and D = 0.38	0.031	−0.010
i_{ref} = –5.3 A and D = 0.80	− 0.025	−0.007
i_{ref} = 4.7 A and D = 0.21	0.021	0.006
i_{ref} = 4.7 A and D = 0.61	− 0.035	0.006

(Err_test: Normalized experimental average current tracking error without compensation, Err_test_wi: Normalized experimental average current tracking error with the proposed compensation method.)

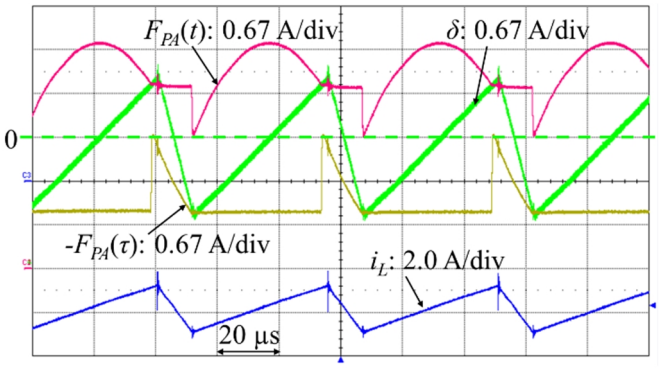


(a)

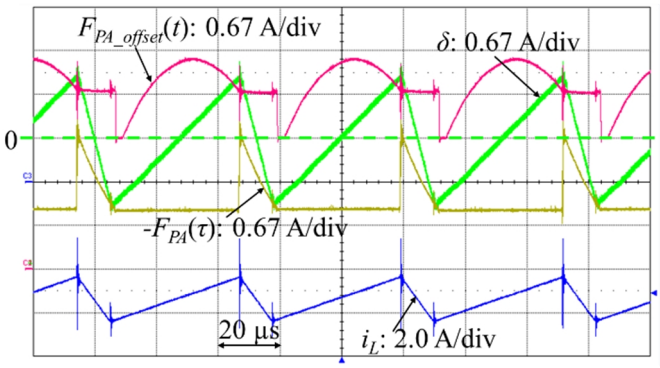


(b)

Fig. 3.9 Experimental waveforms with $i_{ref} = -5.3$ A and $D = 0.38$: (a) without compensation; (b) with compensation.

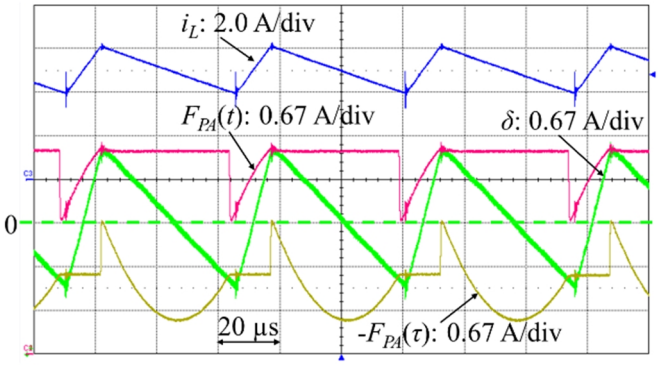


(a)

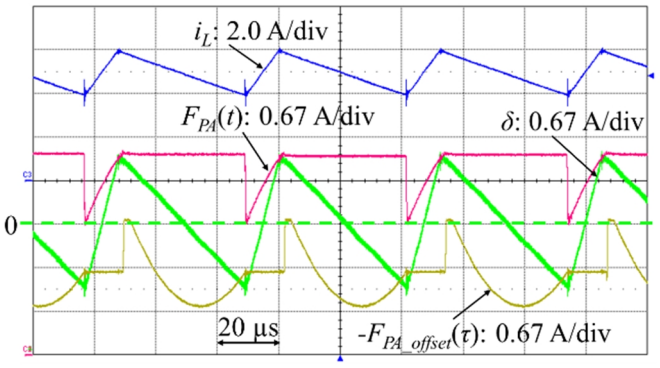


(b)

Fig. 3.10 Experimental waveforms with $i_{ref} = -5.3$ A and $D = 0.80$: (a) without compensation; (b) with compensation.

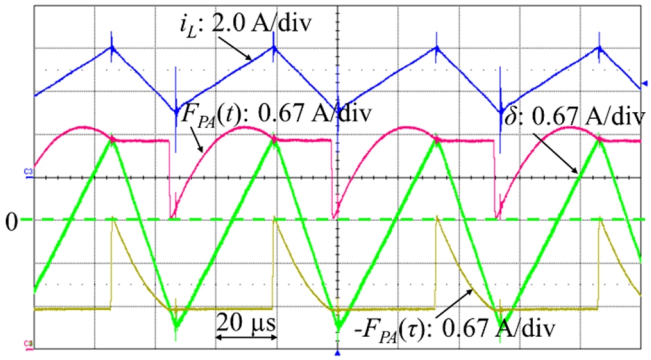


(a)

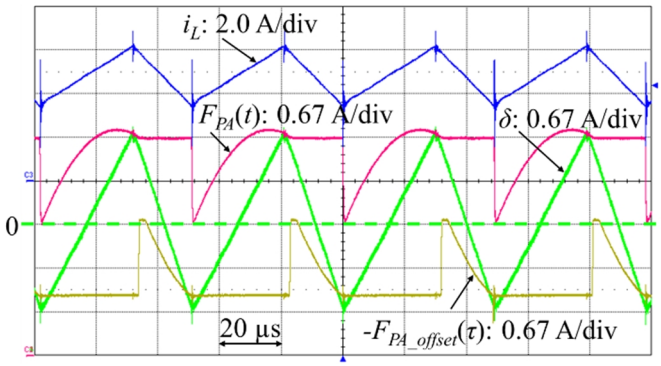


(b)

Fig. 3.11 Experimental waveforms with $i_{ref} = 4.7$ A and $D = 0.21$: (a) without compensation; (b) with compensation.



(a)



(b)

Fig. 3.12 Experimental waveforms with i_{ref} = 4.7 A and D = 0.61 (a) without compensation; (b) with compensation.

Fig. 3.13 and Fig. 3.14 show the comparison of normalized δ_{avg} versus duty-cycle, including experimental results without compensation and experimental results with compensation. In order to verify the analysis on the effect of dead-time, the calculated curves shown in Fig. 3.4 are also redrawn in Fig. 3.13 and Fig. 3.14. Fig. 3.13 is for the operating conditions $i_L < 0$ and Fig. 3.14 is for the operating condition $i_L > 0$. Under both $i_L < 0$ and $i_L > 0$, the normalized δ_{avg} from the experiment without compensation mainly matches with the results from calculation. For the entire duty-cycle range, compared with the

experiment results without compensation, δ_{avg} with the proposed compensation method is significantly decreased, indicating that the current tracking precision of PCC is highly improved.

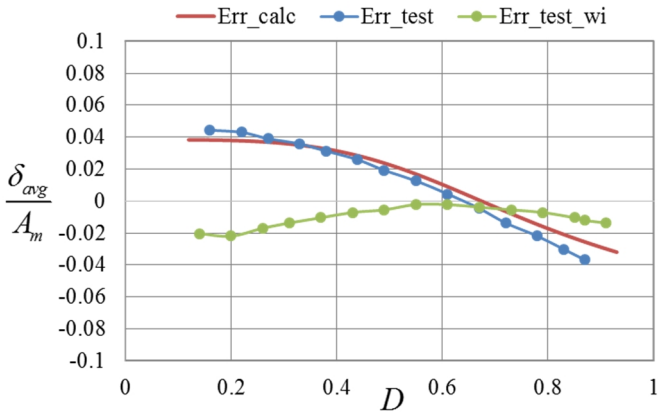


Fig. 3.13 Comparison of normalized δ_{avg} when $i_L < 0$: Err_calc: δ_{avg} based on calculation; Err_test: δ_{avg} from the experiment without compensation; Err_test_wi: δ_{avg} from the experiment with compensation.

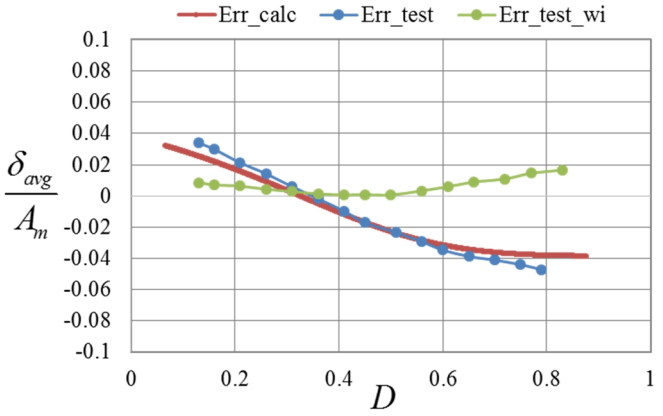


Fig. 3.14 Comparison of normalized δ_{avg} when $i_L > 0$: Err_calc: δ_{avg} based on calculation; Err_test: δ_{avg} from the experiment without compensation; Err_test_wi: δ_{avg} from the experiment with compensation.

Fig. 3.15 and Fig. 3.16 show the comparison of normalized switching frequency versus duty-cycle, including calculated results, experimental results without compensation, and experimental results with compensation. From Fig.

3.15 where $i_L < 0$ and Fig. 3.16 where $i_L > 0$, it is evident that the experimental switching frequency without compensation matches well with the calculated results. Meanwhile the deviation of the switching frequency with the proposed compensation method is much smaller than that without compensation.

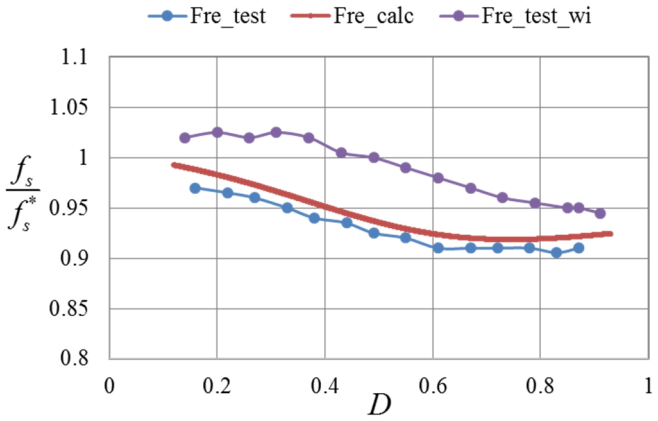


Fig. 3.15 Normalized switching frequency comparison when $i_L < 0$: Fre_calc: calculated switching frequency; Fre_test: switching frequency from the experiment without compensation; Fre_test_wi: switching frequency from the experiment with compensation.

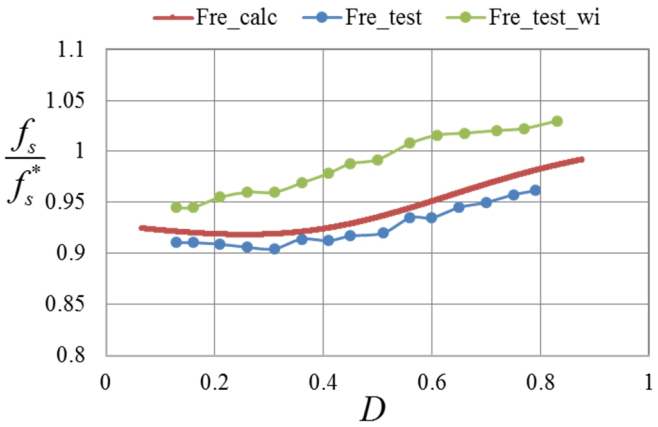


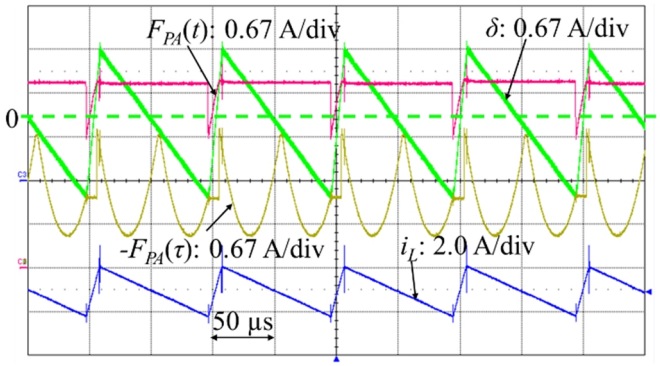
Fig. 3.16 Normalized switching frequency comparison when $i_L > 0$: Fre_calc: calculated switching frequency; Fre_test: switching frequency from the experiment without compensation; Fre_test_wi: switching frequency from the experiment with compensation.

As previous experimental results indicate, even with the proposed dead-

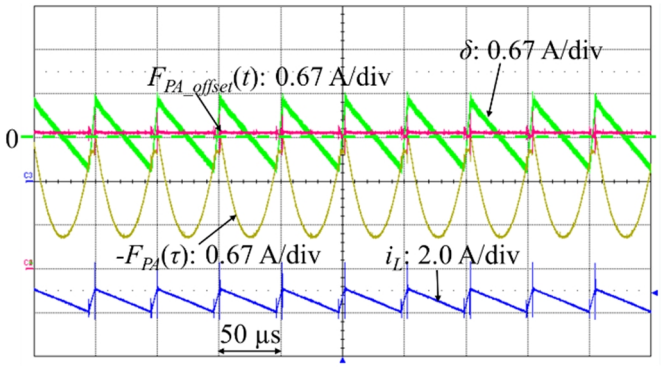
time compensation method, δ_{avg} still deviates slightly from zero and the switching frequency varies from the desired value. These deviations are mainly caused by the propagation delay of the system, including the turn-on delay and turn-off delay of the switches, bandwidth of the current sensor and conditioning circuits, propagation delay of the comparators and optocouplers, and the update rate of the digital-to-analog converters.

In order to verify the increased stable duty-cycle range introduced by the proposed compensation method, experiments at the extreme ends of the duty-cycle range are conducted as shown in Fig. 3.17 to Fig. 3.20. The experiments include four different operating conditions: i_{ref} = –5.3 A and D = 0.11 in Fig. 3.17, i_{ref} = –5.3 A and D = 0.91 in Fig. 3.18, i_{ref} = 4.7 A and D = 0.09 in Fig. 3.19, i_{ref} = 4.7 A and D = 0.89 in Fig. 3.20. As shown in these figures, under the operations without compensation, the current tracking error misses the intersection with the first parabolic carrier and goes into the unstable states. The switching frequency for these unstable cases are around 10 kHz, deviating far from the desired switching frequency and causing voice-band noise. For the operating conditions with the proposed compensation method, at the same duty-cycle, the current control is in the stable duty-cycle range. The peak-to-peak value of the current tracking error is reduced and switching frequency is maintained in the desired range. Due to the proposed compensation method,

the stable duty-cycle range for the operating condition $i_L < 0$ is increased from (0.12, 0.91) to (0.05, 0.96). For the operating condition $i_L > 0$, the stable duty-cycle range is increased from (0.09, 0.88) to (0.06, 0.94). As a result of the increased stable duty-cycle range, the utilization of the dc-bus voltage is improved.

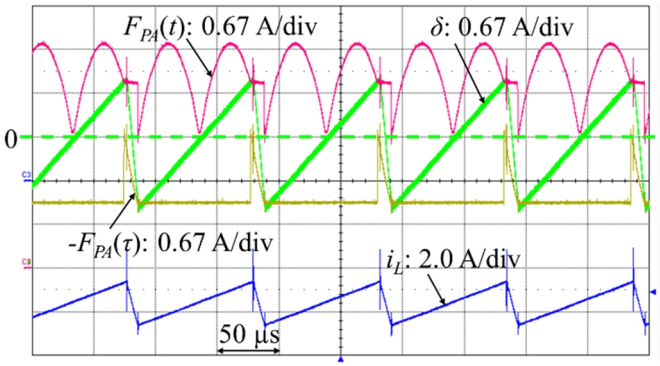


(a)

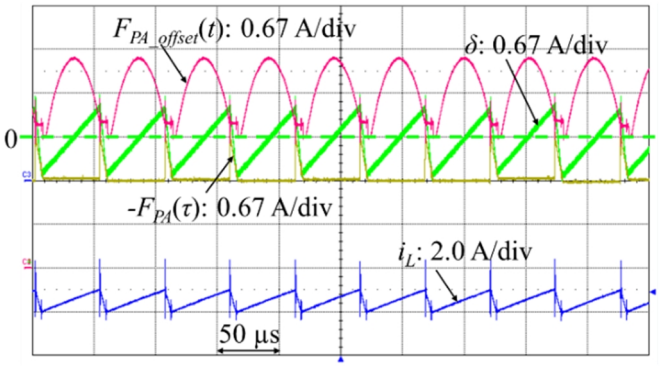


(b)

Fig. 3.17 Experimental waveforms when $i_{ref} = -5.3$ A and $D = 0.11$: (a) without compensation; (b) with compensation.

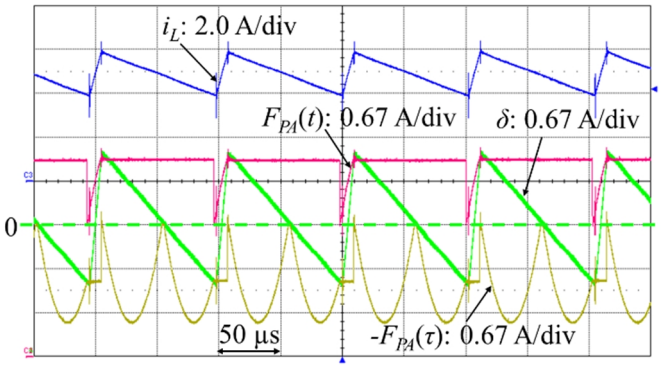


(a)



(b)

Fig. 3.18 Experimental waveforms with i_{ref} = –5.3 A and D = 0.91: (a) without compensation; (b) with compensation.



(a)

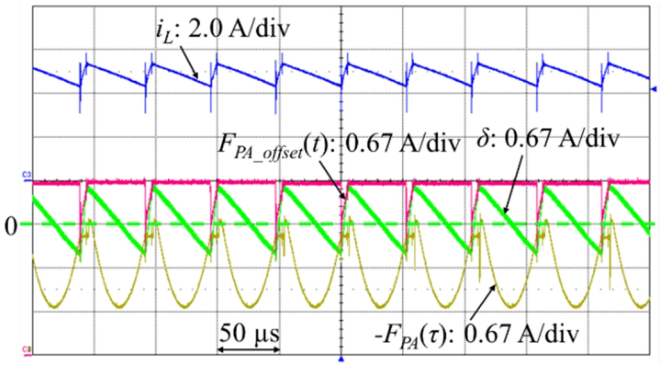


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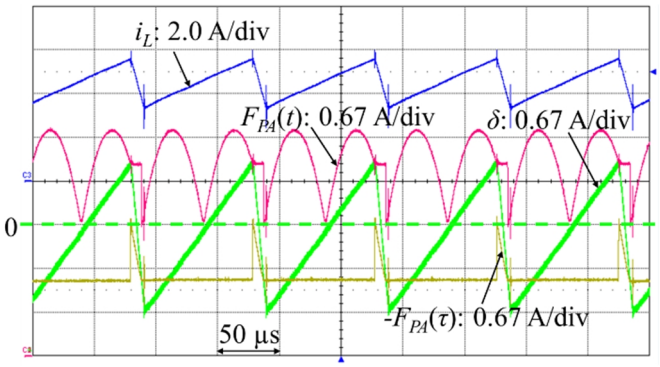
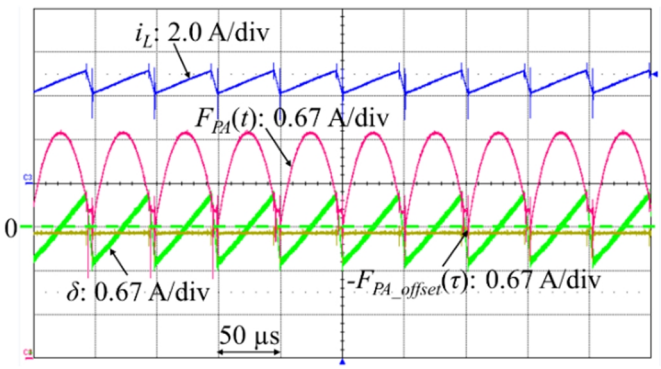
Fig. 3.19 Experimental waveforms with i_{ref} = 4.7 A and D = 0.09: (a) without compensation; (b) with compensation.



(a)



(b)

Fig. 3.20 Experimental waveforms with i_{ref} = 4.7 A and D = 0.89: (a) without compensation; (b) with compensation.

In order to verify the effectiveness of the proposed compensation method on

VSIs, the experiment with 5 A ac current reference has been conducted, with the experimental waveforms shown in Fig. 3.21. In order to analyze the switching frequency deviation, the spectrum of inverter output current i_L is measured as shown in Fig. 3.22. Compared with the operating condition without compensation, the current tracking error of the waveform using compensation has an average value closer to zero. As indicated by the location of the fundamental frequency on the spectrum, the waveform with compensation has a lower switching frequency deviation.

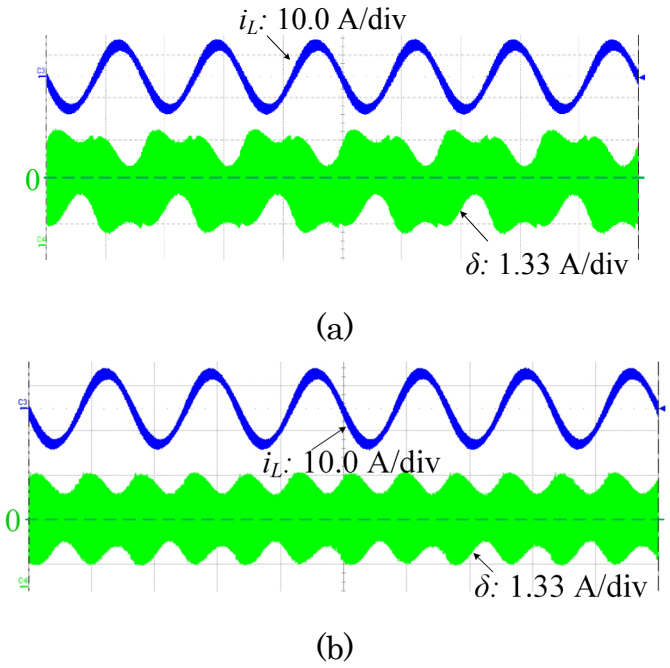
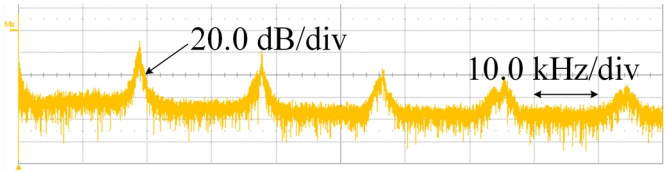
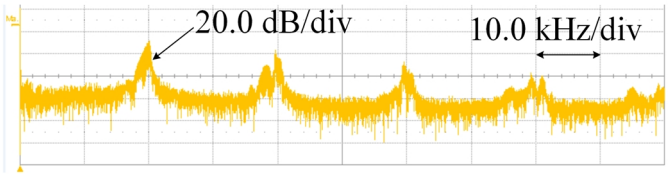


Fig. 3.21 Comparison of the δ_{avg} of the output current: (a) without compensation; (b) with compensation.



(a)



(b)

Fig. 3.22 Spectrum analysis of the output current: (a) without compensation; (b) with compensation.

3.5 Summary

In this chapter, the effects of dead-time on PCC is analyzed and a dead-time compensation method is proposed and verified. Key features of this chapter are as follows:

1) The effects of dead-time on PCC includes the impact on current tracking precision, the decrease of stable duty-cycle range, and the deviation of the switching frequency. For the operating condition without dead-time compensation, the stable duty-cycle range is derived, then the average current tracking error and switching frequency are analyzed over the stable duty-cycle range.

2) In order to compensate the dead-time effect, a compensation method with improved parabolic carrier is introduced. The improved carrier is

implemented by adding an offset to the original parabolic carrier based on the direction of the output current. The added offset can be derived from the dead-time and the parameters of the circuit.

3) With the proposed compensation method, the average current tracking error is reduced thus the current tracking precision is improved. Meanwhile, due to the proposed compensation method, the stable duty-cycle range is also increased and the deviation of the switching frequency is reduced.

Both the effects of dead-time on PCC and the effectiveness of the proposed compensation method are verified by experiment. From the experimental results, the proposed compensation method improves the current tracking precision, enhances the stable duty-cycle range and reduces the deviation of the switching frequency.

Chapter 4 Implementation of PCC on Dual-carrier PWM

4.1 Introduction

The dual-carrier modulation method [82] doubles the frequency of the output current ripple without increasing the switching frequency. Increasing the effective frequency of the output current reduces the current ripple magnitude, decreasing the output filter inductor core loss and improving system efficiency. Therefore, dual-carrier modulation method is widely employed in various VSIs such as APF and uninterrupted power supply (UPS). In order to improve the system performance, PCC would be the preferred method to implement the current control loop in these dual-carrier controlled VSIs. Since PCC was originally proposed for the bipolar modulation method it cannot be directly utilized for dual-carrier pulse-width modulation (PWM) modulation method.

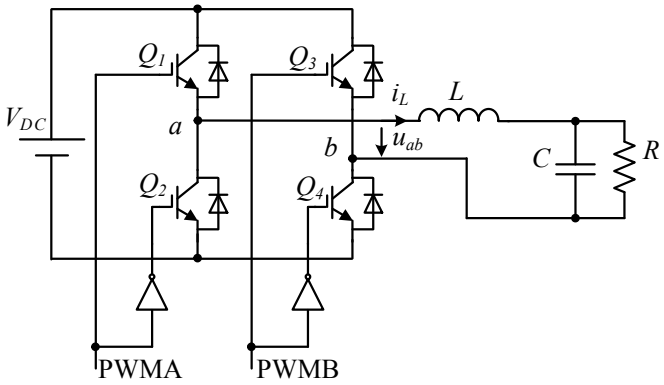
In this chapter, the basic operating principles of the dual-carrier PWM modulation method are introduced. By analyzing the relationship between switch status and output voltage of the full bridge, a state machine based method is proposed to implement PCC for dual-carrier PWM. The effectiveness of the proposed method is tested and verified on a full-bridge VSI.

4.2 Bipolar PWM and Dual-carrier PWM

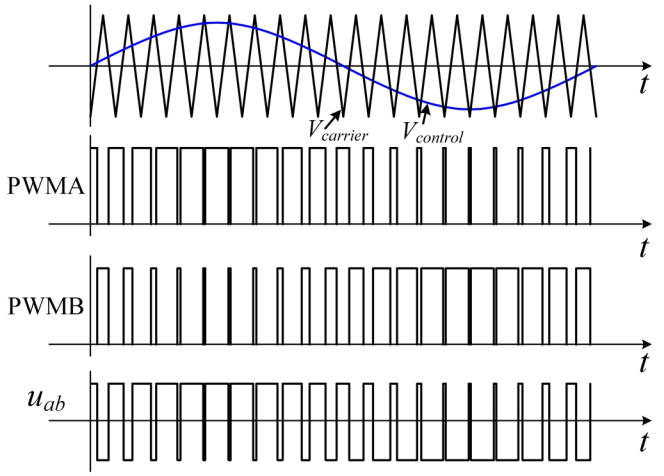
The basic operation principle of a conventional full-bridge inverter with bipolar modulation is shown in Fig. 4.1. L is the inductor of output filter and the output voltage of the full-bridge is defined as u_{ab}. The gate driving signal of PWMA and PWMB are generated simultaneously by the comparison between the control reference $V_{control}$ and triangle carrier $V_{carrier}$, causing the output voltage u_{ab} to be either $+V_{DC}$ or $-V_{DC}$. There is no zero state of u_{ab} that exists in this modulation method.

A typical single phase full-bridge VSI using PCC can be summarized into the diagram shown in Fig. 2.1, Fig. 2.2, Fig. 2.3. For bipolar modulation, $U_p = V_{DC}$ and $U_n = -V_{DC}$.

Operation principles of dual-carrier modulation method is shown in Fig. 4.2. The gate driving signals of PWMA and PWMB are generated by comparing $V_{control}$ and $-V_{control}$ with the triangular carrier respectively. Compared with the bipolar modulation method operating with same switching frequency, the frequency of output voltage u_{ab} of dual-carrier PWM is doubled and the polarity is changed to unipolar. As a result, the output current ripple is reduced and core loss of the output inductor is decreased, improving the system efficiency. Due to the frequency-doubling characteristic of dual-carrier PWM, dual-carrier modulation method is widely employed in VSIs.

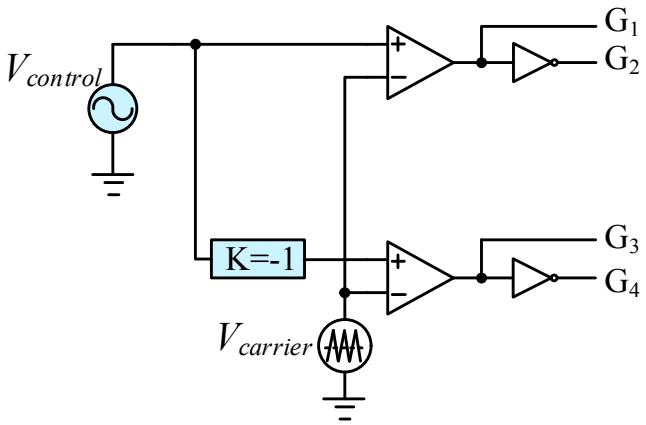


(a)

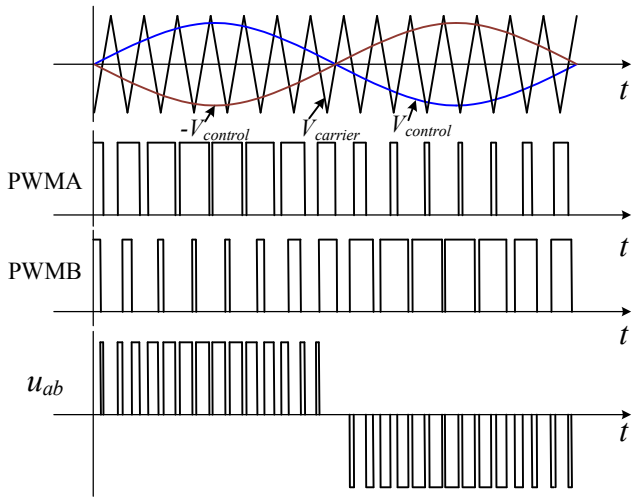


(b)

Fig. 4.1 Operating principle of bipolar modulation



(a)



(b)

Fig. 4.2 Operation of dual-carrier PWM

4.3 Proposed Method for Dual-carrier PWM

As aforementioned, PCC is proposed for any VSIs with two output states: U_p and U_n. Since dual-carrier modulation method has three output states (V_{DC}, 0, and $-V_{DC}$) and only two control states can be generated by the parabolic current controller ($S = 1$ and $S = 0$) PCC cannot be directly utilized for dual-carrier PWM. In order to use PCC for dual-carrier PWM VSIs, a mechanism needs to be established between the control signals of PCC and the PWM signal sequence for dual-carrier PWM.

4.3.1 State Machine

In order to analyze the output states of dual-carrier modulation method, the states of dual-carrier modulation method are redrawn in Fig. 4.3. Four PWM states are defined in this paper: state 0 for PWMA = 0 and PWMB = 0,

state 1 for PWMA = 0 and PWMB = 1, state 2 for PWMA = 1 and PWMB = 0, and state 3 for PWMA = 1 and PWMB = 1. Under the operating condition of $V_{control} > 0$, the output voltage u_{ab} has two voltage levels: V_{DC} and 0, involving three PWM states: state 2, state 3, and state 0. From this point of view, PCC can be employed by setting $U_p = V_{DC}$ and $U_n = 0$. Gate driving signals PWMA and PWMB need to be generated based on the control signal S, which is obtained from the parabolic current controller. By setting $U_p = 0$ and $U_n = -V_{DC}$, a similar method can be applied to the operating condition when $V_{control} < 0$. In order to translate the control signal S to PWM states, a state machine is proposed as shown in Fig. 4.4.

As shown in the state machine, starting from PWM state 2, if the control signal S changes from 1 to 0, it indicates that the current tracking error intersects with the positive parabolic carrier and the output voltage u_{ab} needs to be changed to 0 for the current tracking error to decrease. In Fig. 4.3, PWM state 3 and PWM state 0 can both generate the required zero output voltage. To match the state machine transition sequence with that of the dual-carrier PWM it is necessary to know what was the previous state of the system. Determining which state is the next is achieved by introducing a flag into the proposed state machine. If the flag status is 0, this indicates that the previous zero voltage was generated by PWM state 0, as shown in Fig. 4.3, then the next

PWM state should be PWM state 3. Otherwise if the flag status is 1, indicating the previous zero voltage was implemented by PWM state 3, then the next PWM state should be PWM state 0. Through this method, the state machine can produce the desired PWM states 2, 3, 2, 0, 2, 3, 2, 0…, which matches with the sequence of dual-carrier PWM shown in Fig. 4.3. Similarly, the state machine can also produce the state sequence 1, 3, 1, 0, 1, 3, 1, 0...for the operating condition $V_{control} < 0$. This means that the required PWM sequence of dual-carrier PWM can be simulated by the proposed stated machine.

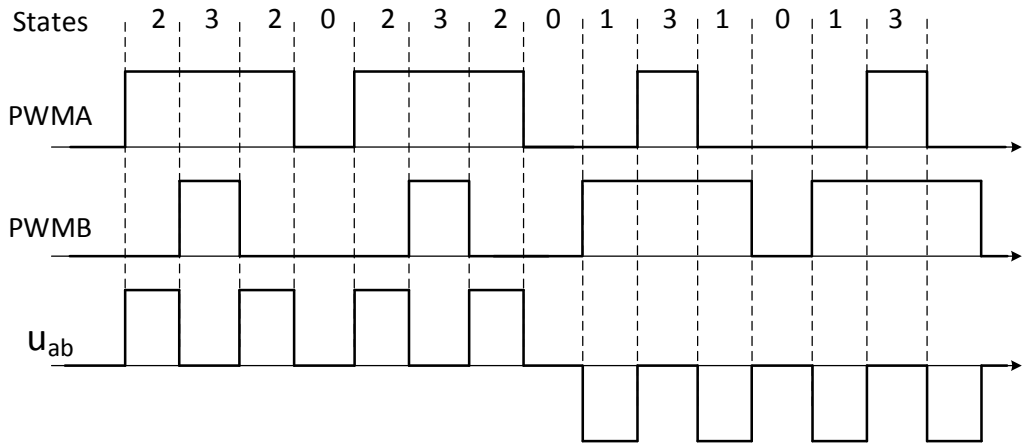


Fig. 4.3 Definition of PWM states of dual-carrier PWM

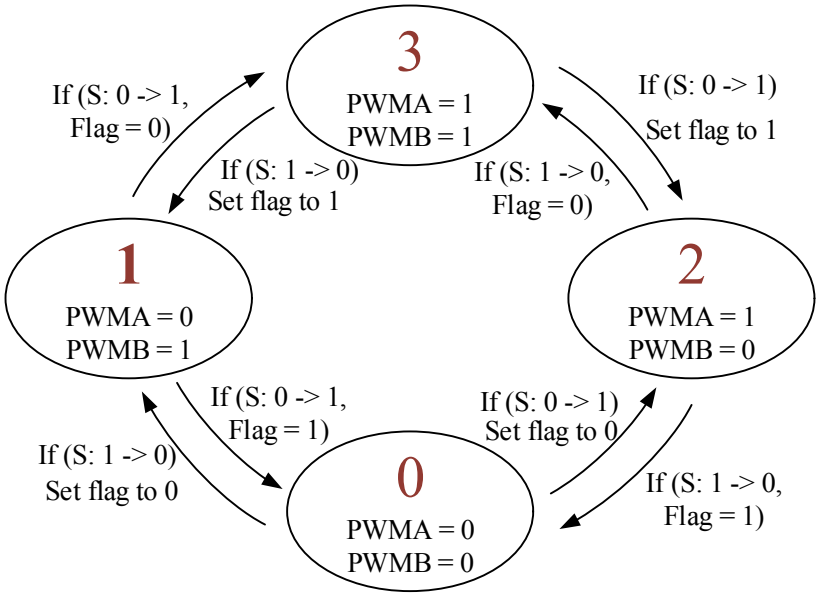


Fig. 4.4 Proposed state machine

4.3.2 Zero-crossing Operation

During the interval that the voltage of the ac-side crosses over zero, the proposed state machine can not automatically generate the PWM states sequence between $V_{control} > 0$ and $V_{control} < 0$ that ensures a continuous zero-crossing transition. In order to solve this issue, a zero-crossing mechanism needs to be added to the state machine.

For the stand-alone inverter, an algorithm is proposed for the zero-crossing transition as shown in Fig. 4.5 where a dead band is introduced. If the current tracking error δ is larger than V_{band}, the PWM state will be switched to PWM state 1. In this case, due to the polarity change of the ac-side voltage, the current tracking error is out of control and the PWM state machine needs to generate PWM state 1 to decrease the current tracking error. At the same time,

the zero-crossing transition can be completed. Similarly, if the current tracking error is smaller than $-V_{band}$, the PWM state machine needs to switch to PWM state 2. Through this method, the state machine can implement the operating transition during the transition of zero-voltage crossing in standalone mode. The value of V_{band} should be larger than the maximum of parabolic carrier $\frac{A_m}{4}$. In this paper, V_{band} is set to be $0.3A_m$.

For the grid-tied inverter, the transition signal can be generated by the phase-lock-loop (PLL) of the ac-side voltage.

If the ac-side voltage is larger than zero, PWM states sequence of the operating condition $V_{control} > 0$ needs to be generated. Otherwise if the ac-side voltage is below zero, PWM states sequence of the operating condition $V_{control} < 0$ needs to be generated. By the use of the phase information of grid voltage, the transition between the operating conditions $V_{control} < 0$ and $V_{control} > 0$ can be smoothly implemented.

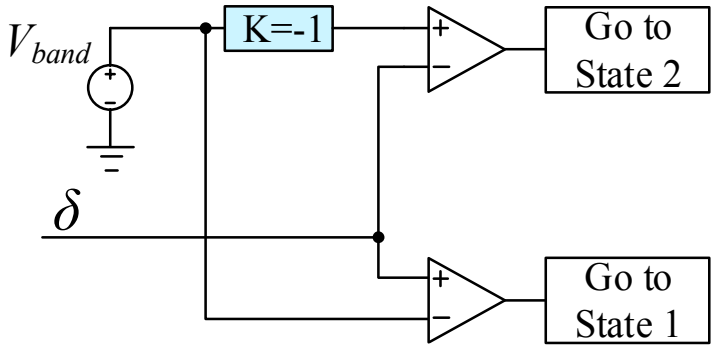


Fig. 4.5 Zero-crossing operation

4.4 Simulation

In order to verify the proposed PCC method for dual-carrier PWM, simulation is conducted in PSIM. A standalone full bridge inverter is employed as a simulation example. The switching frequency is set to 16 kHz and the equivalent frequency of the output voltage is 32 kHz. An output inductance of 3.3 mH and an output capacitor 4.7 μF are selected as the output filter. The dc-bus voltage is set to be 400 V, then for dual-carrier operation, $U_p - U_n = 400\ V$ and A_m = 1.894 can be obtained based on the equations in part II. In this simulation, a sinusoidal current reference is employed and a proper load resistor is selected as the ac-side load. No voltage loop is employed in this simulation because this simulation is just used to verify the performance of the current loop with proposed state machine. In this simulation case, the magnitude of the sinusoidal current reference is 13 A.

The simulation results of stand-alone mode inverter are shown in Fig. 4.6 to Fig. 4.8. Fig. 4.6 shows the waveform of inductor current, output voltage, and current tracking error. From the simulation results, the current tracking error as well as the output current can be well controlled. During the period that output voltage crosses over zero, the current tracking error is out of control until it intersects with the zero-crossing dead-band V_{band} or $-V_{band}$ shown in Fig. 4.8. Fig. 4.7 represents the PWM waveform of each inverter leg, full-bridge

output u_{ab}, positive parabolic carriers F_p, negative parabolic carrier F_n, current tracking error Err, and control signal of parabolic current controller PCC_S. From this simulation, it is can be seen that the parabolic current controller generates the control signal PCC_S by the comparison between the current tracking error and parabolic current carriers. Based on the control signal PCC_S, the state machine generates the PWM signals for both inverter legs, which matches the sequence requirement of the dual-carrier PWM controlled VSIs. As also can be seen in Fig. 4.7, the frequency of full bridge output doubles the switching frequency of switches, decreasing the current ripple and core loss. Detailed waveforms during zero-crossing period are shown in Fig. 4.8. The current tracking error is out of control for several switching period until it intersects with the dead-band V_{band}, then the output of the state machine changes from 2, 3, 2, 0, 2, 3… to 1, 3, 1, 0, 1, 3… to complete the zero-crossing transition.

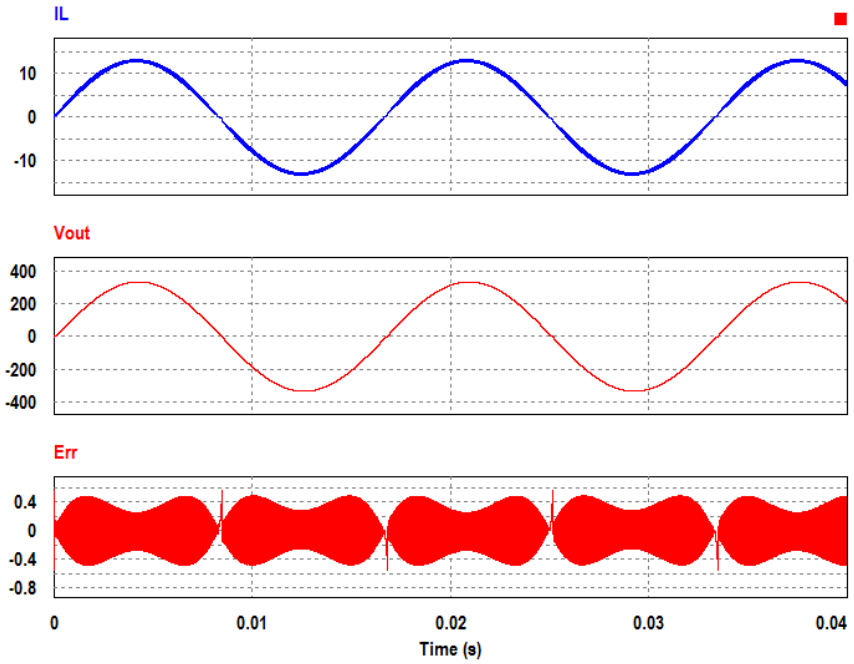


Fig. 4.6 Simulation results

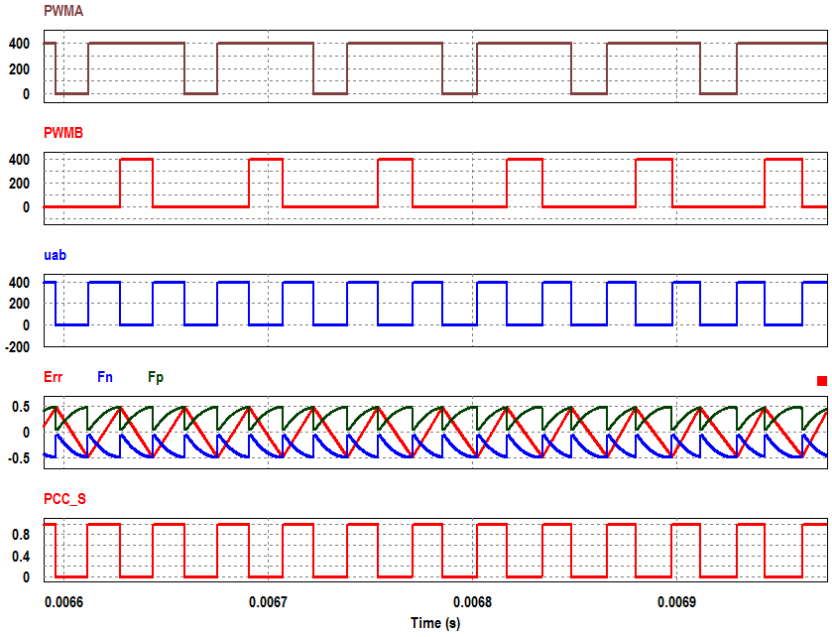


Fig. 4.7 Simulation results

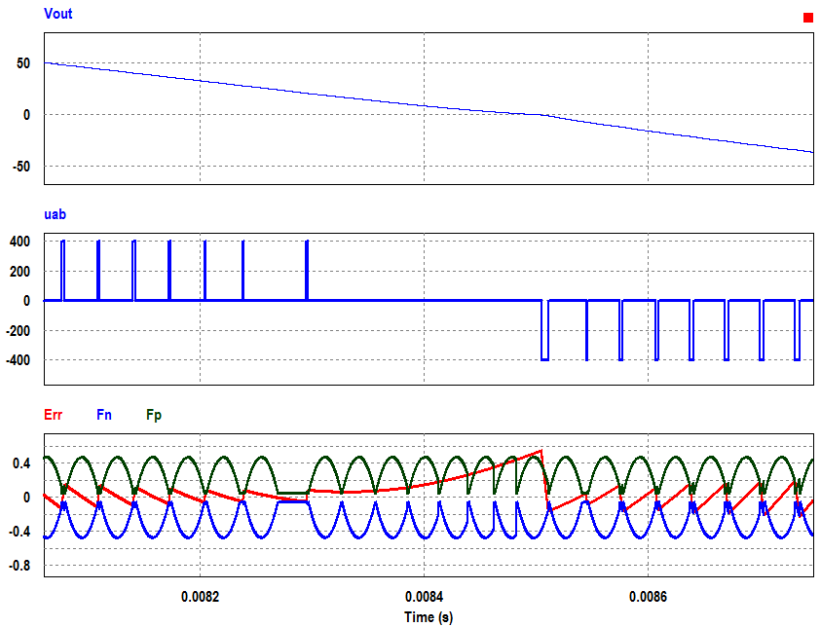


Fig. 4.8 Simulation results

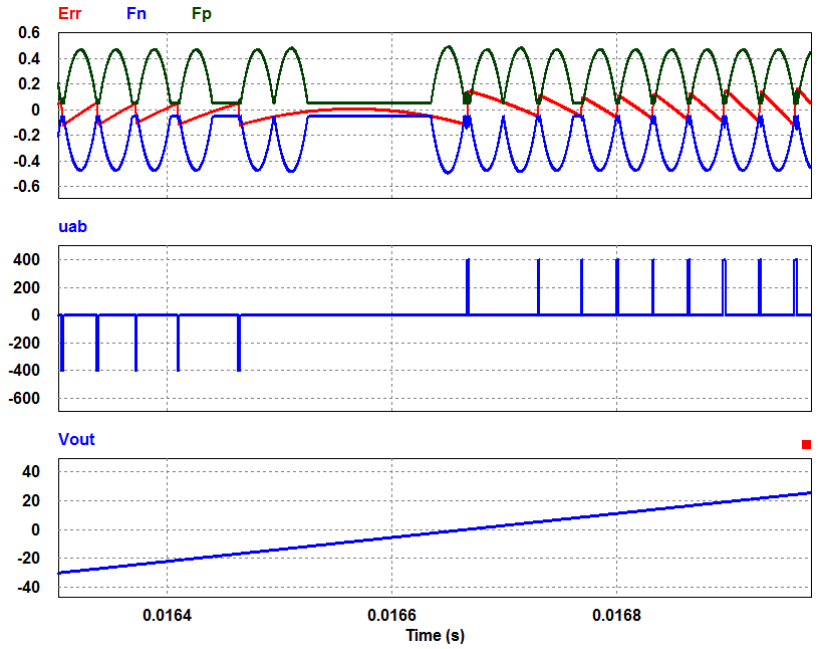


Fig. 4.9 Simulation results

The simulation of grid-tied inverter operation is also conducted and results are shown in Fig. 4.9. Compared with the standalone mode, the grid-tied inverter can use the phase of grid voltage to complete the zero-crossing

transition. In experimental test, a PLL is necessary to obtain the accurate phase information of the power grid. As shown in the simulation result, the state machine can finish the zero-crossing transition without waiting for the intersection between the current tracking error and dead-band. In addition, compared to the standalone inverter, the current tracking error of the zero-crossing transition is smaller and current control precision is higher.

4.5 Experimental Results

In order to verify the effectiveness of the proposed method, a full-bridge VSI prototype with dual-carrier operation is tested. In the experiment PCC is utilized as the current control loop, which is implemented with a FPGA chip EP4CE15E22 from Alter and digital-to-analog converter (DAC) from Analog Devices, Inc. (ADI). DAC is responsible to generate the analog signals for comparators including parabolic current carriers and the dead-band for zero crossing detection. Fairchild FGY75N60SMD IGBTs are utilized as the main switches. Gating signals are generated by FPGA. Other parameters are same as the configuration in simulation. The diagram of the prototype hardware is shown in Fig. 4.10. Using a sinusoidal current reference with constant magnitude and proper configuration of the load resistance, the experimental results of standalone mode inverter are obtained as shown in Fig. 4.11, Fig. 4.12, and Fig. 4.13.

In Fig. 4.11, the current tracking error, inductor current, and the spectrum of the inductor current, output voltage are illustrated. It is evident that the current tracking error is well controlled in the desired control band. The equivalent frequency of the output current ripple is 32 kHz, as the spectrum of the inductor current showing, indicating the system maintains a constant switching frequency. These test results prove the effectiveness of the proposed state machine method.

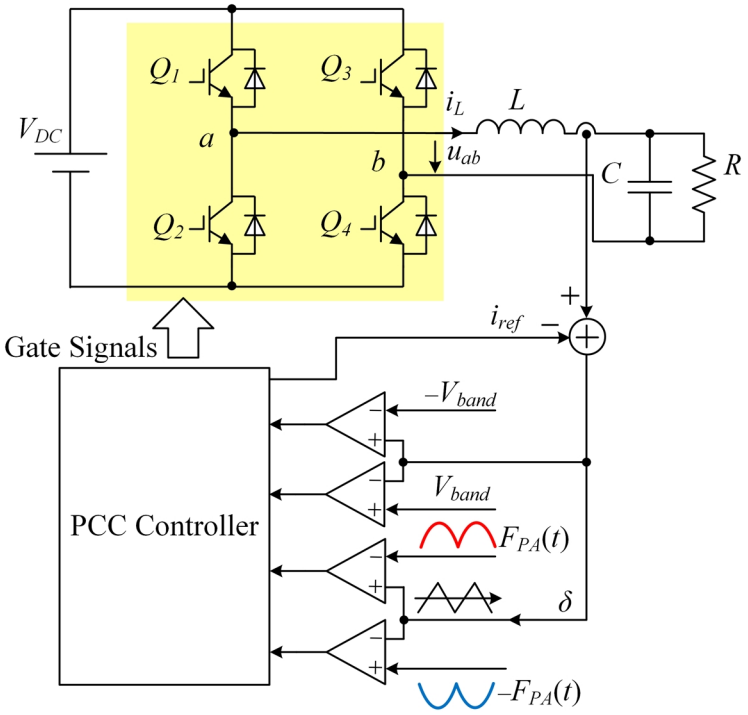


Fig. 4.10 Diagram of the prototype hardware

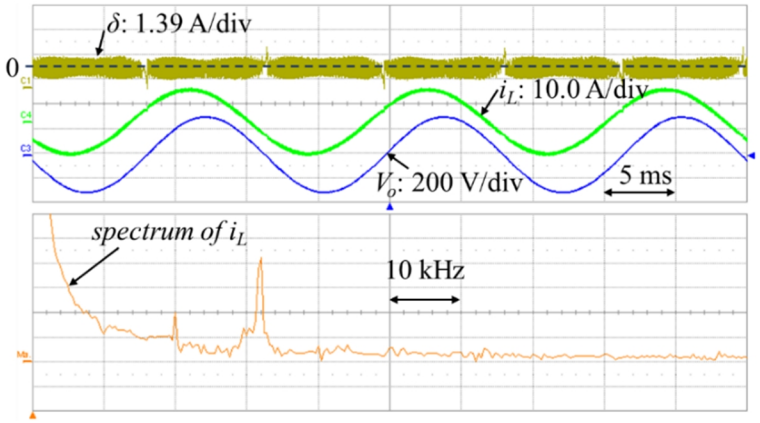


Fig. 4.11 Experimental results

Fig. 4.12 and Fig. 4.13 show the PWM signals of each leg and the current waveform of output inductor. Fig. 4.12 shows the operating condition that $V_{control} < 0$ and Fig. 4.13 shows the operating condition that $V_{control} > 0$. As seen from these two figures, the PWM sequence matches with the dual-carrier PWM shown in Fig. 4.2. It is evident that inductor currents are well controlled in both operating conditions.

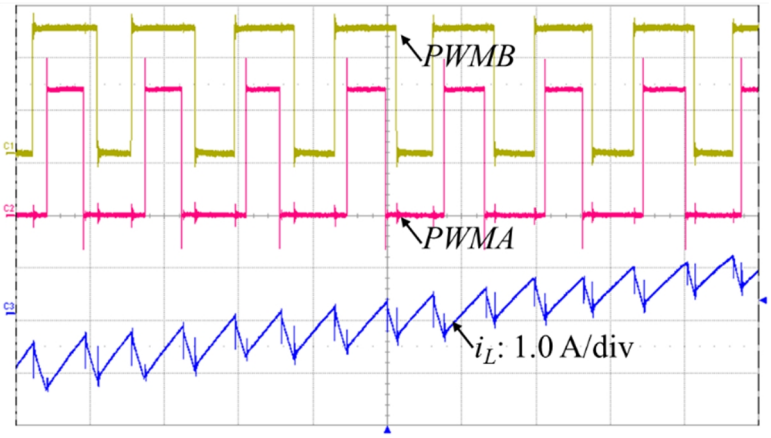


Fig. 4.12 Experimental results

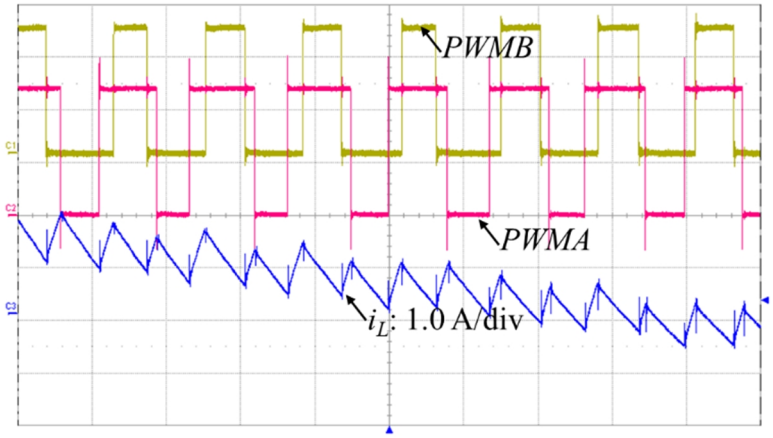


Fig. 4.13 Experimental results

4.6 Summary

In this chapter, a state machine based method is proposed to implement parabolic current control on dual-carrier PWM. The following distinctive features are described:

1) Operation principle of dual-carrier PWM is analyzed. Compared with conventional bipolar PWM, dual-carrier PWM has lower current ripple and reduced core loss.

2) A state machine method is proposed to implement PCC for dual-carrier PWM controlled VSIs. With the proposed method, the control signal of parabolic current controller is translated to the required sequence of dual-carrier PWM.

3) Zero-crossing methods are also discussed for different operating modes including standalone inverter and grid-tied inverter. For grid-tied mode inverter, zero-crossing transition can be implemented by the use of grid voltage information. A dead-band is introduced to help the stand-alone

inverter complete the zero-crossing transition.

The effectiveness of the proposed method is verified by simulation and experimental results. The state machine based parabolic current control method proposed in this paper also can be utilized in other unipolar modulation methods including asymmetrical unipolar modulation.

Chapter 5 A Sensorless Implementation of Parabolic Current Control

5.1 Introduction

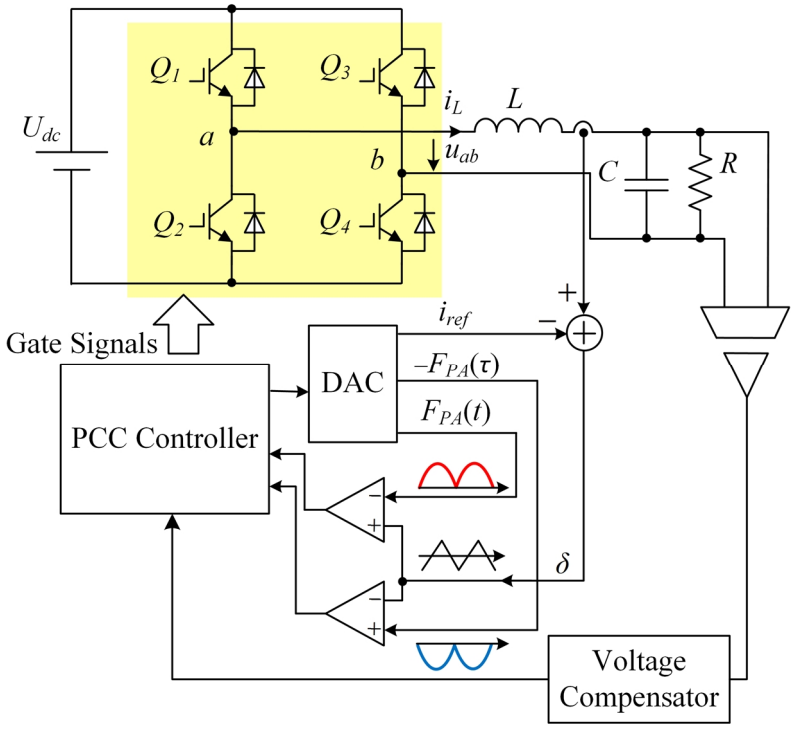


Fig. 5.1 Diagram of single phase inverter with PCC

A typical implementation of PCC is shown in Fig. 5.1. By using a compensator in the voltage loop, proper current reference i_{ref} is generated for the internal current control loop. To implement parabolic current control, both the current reference and parabolic carriers are generated by a digital-to-analog converter (DAC). A DAC with both high speed and high precision is required to generate precise parabolic carriers with minimized propagation

delay. A hall-effect-based current sensor is employed in the system to detect the current of the output inductor. Since the parabolic current controller needs the real-time current information of the inductor, the bandwidth and response speed of the current sensor are very important. Operational amplifiers act as current conditioners to obtain the current tracking error, δ. Next, the current tracking error is compared with the parabolic carriers to generate the required gating signals' sequence. Since the propagation delay of the comparators impacts the current tracking performance and the convergence of switching frequency, high precision comparators with small propagation delay are preferred. Thus, all the components involved in the current control loop including the current sensor, DACs, operational amplifiers, and comparators require high bandwidth, high resolution, and small propagation delay to ensure the performance of the current loop. These requirements both lower the reliability and increase the complexity of the control system.

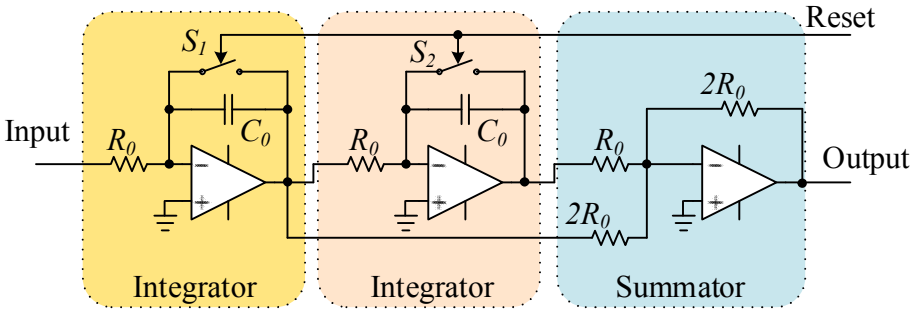


Fig. 5.2 Parabolic carrier waveform generator

Another implementation method of parabolic carriers is analog based

instead of digital [27]. The basic diagram is shown in Fig. 5.2. The DAC is replaced with operational amplifier based integrators and summators as the parabolic carrier generator. To generate the desired parabolic carriers, $T^* = R_0 C_0$ always holds true in the diagram. Additional analog switches S_1 and S_2 are required to reset the parabolic carriers. Since high precision of the parabolic carrier is required to ensure the control performance, operational amplifiers with very small input offset current are preferred. Furthermore, a precise voltage reference chip is required to generate the input voltage of the parabolic carrier generator. These precise analog components would increase the cost of the control system. In addition, compared with the DAC based implementation method, the adjustment of A_m in the operational amplifier based method is not flexible. To ensure system stability and maintain the proper operating range of the switching frequency, additional circuits are needed to limit the minimum value of the parabolic carriers, further complicating the system.

From this point of view, although the performance of PCC is very attractive, the implementation introduces additional cost and complexity to the system. Thus, it is desirable to find a current sensorless method to implement PCC [83]-[87]. Then current sensor and associated conditioning circuitry can be eliminated. Offset and bandwidth problem of the current sensor and update-

rate issue of DACs are eradicated as well. In this chapter, the basic operating principle of PCC is introduced and the inductor current is analyzed. Based on this analysis, a sensorless current control method is proposed and studied. Problems with having a dc offset on the ac-side output voltage are solved by using an additional control loop. Finally, an H-bridge VSI utilizing PCC is designed and tested to verify the effectiveness of the proposed sensorless control method.

5.2 Proposed Sersorless Control Method

5.2.1 Analysis of The Inductor Current

As shown in Fig. 2.2, if $S = 1$ and the top switch S_p is turned on, the following equation holds true:

$$L\frac{di_L}{dt} = U_p - u_{ac}. \tag{5.1}$$

If $S = 0$, the top switch S_p is off and the bottom switch S_n is on, then

$$L\frac{di_L}{dt} = U_n - u_{ac}. \tag{5.2}$$

For the full bridge inverter with bipolar modulation, combining the two equations above yields an additional control variable, S_{pn}, defined as:

$$S_{pn} = \begin{cases} 1, & (S = 1) \\ -1. & (S = 0) \end{cases} \tag{5.3}$$

Assuming the dc link voltage of the H-bridge inverter is V_{DC}, the following

equation is obtained by combining (5.1), (5.2), and (5.3)

$$L\frac{di_L}{dt} = S_{pn}V_{DC} - u_{ac} \tag{5.4}$$

From (7) the inductor current is derived for (8)

$$i_L = \frac{1}{L}\int (S_{pn}V_{DC} - u_{ac}) + i_{L0} \tag{5.5}$$

i_{L0} represents the initial inductor current and, for simplicity, i_{L0} can be set to zero. As can be seen from (5.5), the current of the inductor is based on the dc link voltage, switching status, and ac-side voltage.

By discretizing (5.5), the following equation is obtained,

$$i_L(k) = \frac{T_s}{L}\sum_{0}^{k}\left[S_{pn}(k)V_{DC} - u_{ac}(k)\right]. \tag{5.6}$$

Where T_s is the sampling period, $i_L(k)$ is the inductor current at sampling interval, k, and $u_{ac}(k)$ is the ac-side output voltage at sampling interval, k. By substituting the expression of $i_L(k\text{-}1)$ to (5.6), (9) is further discretized as

$$\begin{cases} i_L(k) = i_L(k-1) + \Delta i_L(k) \\ \Delta i_L(k) = \dfrac{T_s}{L}\left(S_{pn}(k)V_{DC} - u_{ac}(k)\right) \end{cases} \tag{5.7}$$

Thus, based on the inductor current of the previous time interval $i_L(k\text{-}1)$, the inductor current at time interval k can be calculated from the switching status S_{pn}, dc link voltage V_{DC}, and ac-side output voltage $u_{ac}(k)$. Based on the discretized result in (10), the current of the output inductor can be rebuilt or

emulated in a digital micro-controller.

5.2.2 Control Loop Design

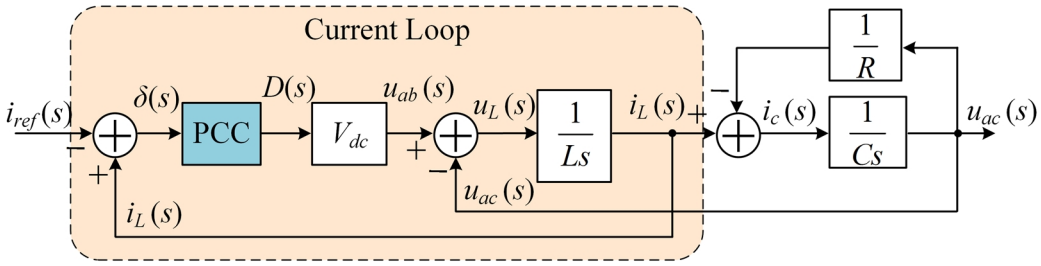


Fig. 5.3 Control block diagram

The control block diagram of the system using PCC as the internal loop is summarized and shown in Fig. 5.3. The inductor current i_L(s) is employed as the feedback of the current loop. The current tracking error, δ(s), is obtained by subtracting the current reference i_{ref}(s) from the inductor current i_L(s). PCC generates the proper duty-cycle D(s) for the power stage. The voltage across the output inductor is obtained by subtracting the ac-side voltage u_{ac}(s) from the H-bridge output u_{ab}(s). i_c(s) represents the current of the output capacitor.

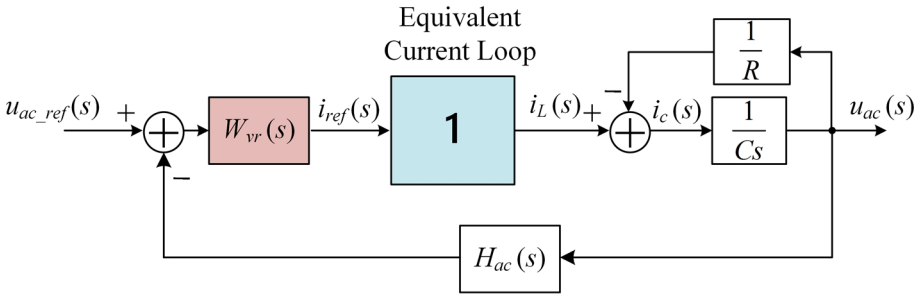


Fig. 5.4 Votlage loop control diagram

Since the parabolic current controller (PCC) ensures both a fast transient response and high control precision, the closed current loop can be simplified

to a control block with a gain of 1. The control block diagram of the whole system is shown in Fig. 5.4. $u_{ac\_ref}(s)$ is the ac-side output voltage reference. $W_{vr}(s)$ is the voltage loop compensator. The reference for the inductor current $i_{ref}(s)$ is generated by $W_{vr}(s)$. $H_{ac}(s)$ is both the sensing gain and the low-pass filter of the ac-side output voltage. Thus, the transfer function of the voltage loop is summarized as

$$T_v(s) = W_{vr}(s) \cdot H_{ac}(s) \cdot \frac{R}{RCs+1} \tag{5.8}$$

Even though PCC is employed in the current loop, the system performance still relies on the design of the voltage loop. To minimize the distortion of output voltage, a PI controller is used for voltage loop controller. The structure of the PI controller is

$$W_{vr}(s) = \frac{K_p(\tau_u s+1)}{\tau_u s}. \tag{5.9}$$

For the sensing gain and low pass filter $H_{ac}(s)$, the structure is designed as

$$H_{ac}(s) = \frac{H_v}{T_f s+1}. \tag{5.10}$$

T_f is the time constant of the low pass filter. 0.5 ~ 0.67 T^* is usually required to attenuate the ripple of the ac-side voltage. The bode plot of the voltage loop with different load resistance is shown in Fig. 5.5. A phase margin of 40 degrees and a bandwidth of 2.8 kHz is obtained. For digitally

implemented voltage loop controller, the computation delay of the controller needs to be considered. Typically, a block with model e^{-sT_c} would be introduced to the control loop. T_c is the sampling period of the digital voltage controller [88].

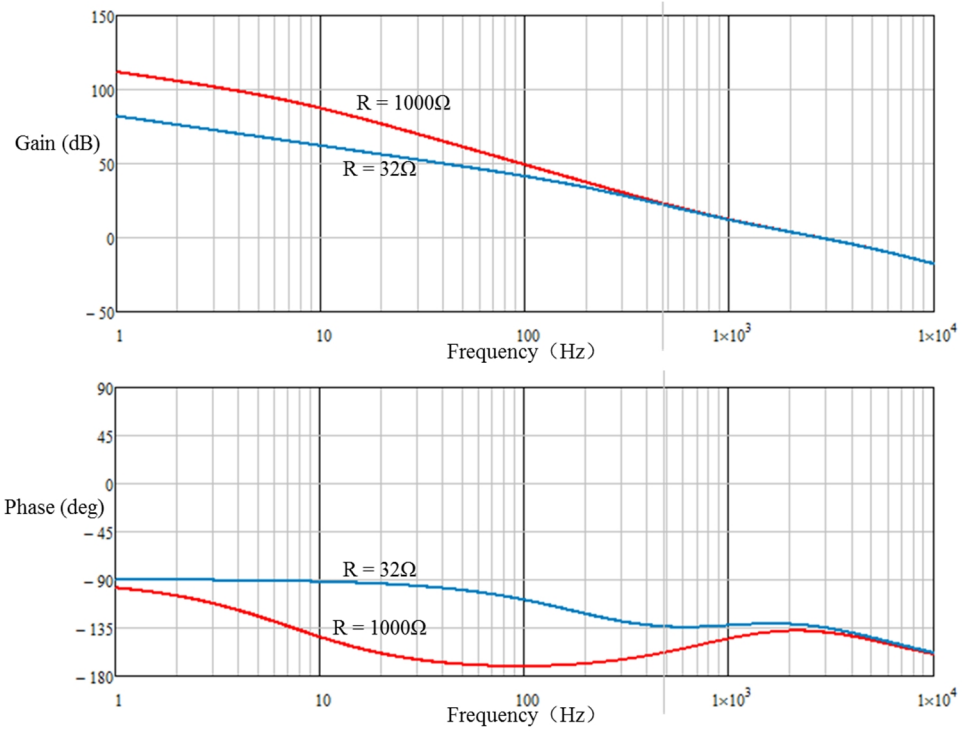


Fig. 5.5 Bode plot of voltage loop

5.2.3 Offset Elimination of The Ac-side Voltage

However, the current emulator cannot precisely imitate the inductor current based on (5.7). First, the inductance of the output inductor changes with current and temperature. Further, because of the dead-time and various propagation delays of the gate driver chip, the control signal S cannot precisely present the output voltage of the inverter legs. The control precision of dc link

voltage V_{DC} also impacts the precision of the emulated inductor current. Because the emulator works like an integrator to imitate the current, these errors would cause a dc offset on the emulated current which would have an effect on the ac-side voltage. For example, if the emulated current has a positive offset, that means the actual inductor current is smaller than the emulated current and the ac-side output voltage would be smaller than the required value. To correct this, the voltage loop controller needs to increase the reference of the inductor current. The error introduced by the current emulator causes the dc offset of the emulated current to keep increasing or decreasing until it reaches the range limit. For the digital controller, the variable could become saturated. Because the current tracking error is still well controlled within the parabolic band, an integrator is necessary for the voltage loop controller to generate a current reference with an increasing or decreasing dc offset. As a result of the employment of the integrator in the voltage loop controller and the increasing or decreasing dc offset on current reference, a dc offset would show up on the ac-side voltage, working with the integrator of the voltage controller to generate the required dc offset on the current reference.

In order to analyze the impact of the dc offset on the current reference, i_{ref}, and the emulated current, i_{L_emu}, a simulation is conducted in PSIM and the result is shown in Fig. 5.6. As the figure indicates, due to the impact of errors,

the dc offset on i_{L_emu} and i_{ref} continue to increase. However, the ac-side output voltage, u_{ac}, and the inductor current, i_L, can still be well controlled but a slight dc offset on u_{ac}. To derivate the relationship between the dc offset on i_{L_emu} and the dc offset on u_{ac}, $i_{L\_emu\_offset}$ and u_{ac_offset} are defined as the dc offset of i_{L_emu} and u_{ac}, respectively. Then u_{ac_offset} can be obtained based on the slope ratio of $i_{L\_emu\_offset}$ and the parameters of the voltage loop controller

$$u_{ac\_offset} = \frac{di_{L\_emu\_offset}}{dt} \cdot \frac{\tau_u}{K_p} \cdot \frac{1}{H_v} \tag{5.11}$$

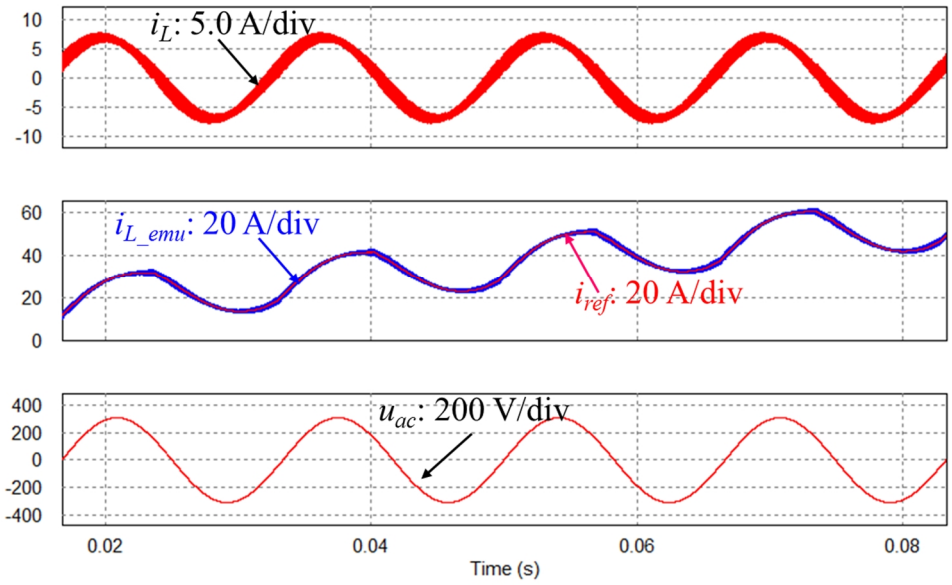


Fig. 5.6 Simulation results

Since the dc offset on the ac-side voltage relates to the slope ratio of $i_{L\_emu\_offset}$, as presented in (5.11), if the slope ratio of $i_{L\_emu\_offset}$ is controlled to be zero, the dc offset on u_{ac} can be eliminated. The slope ratio of $i_{L\_emu\_offset}$ is controlled by adding an adjusting voltage u_{adj} to (5.7), which changes (5.7) to

$$\Delta i_L(k) = \frac{T_s}{L}\left(S_{pn}(k)V_{DC} - u_{ac}(k) - u_{adj}\right) \tag{5.12}$$

The introduction of u_{adj} cancels the effect of the errors in the current emulator and makes the dc offset of i_{L_emu} a constant. To eliminate the dc offset of u_{ac}, the slope ratio of $i_{L\_emu\_offset}$ or the dc offset of u_{ac} can be utilized as the feedback. Because the dc offset on u_{ac} is too small to be precisely detected, whereas the slope ratio of $i_{L\_emu\_offset}$ can be easily obtained in the software, using the slope ratio of $i_{L\_emu\_offset}$ for the feedback is preferred. In this paper, i_{L_emu} is filtered and sampled to calculate the slope ratio of $i_{L\_emu\_offset}$. The control block of this loop is summarized and shown in Fig. 5.7.

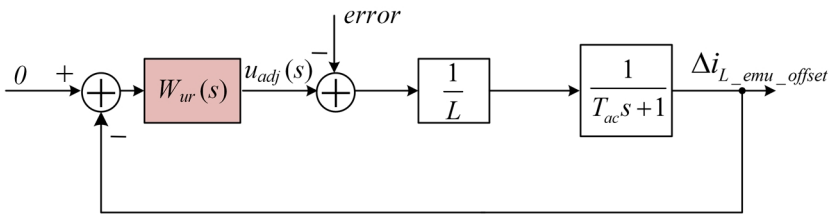


Fig. 5.7 Control blocks for dc offset elimination of u_{ac}

As shown in Fig. 5.7, the change of $i_{L\_emu\_offset}$ over an ac-line period, $\Delta i_{L\_emu\_offset}$, is utilized as the feedback and controlled to be zero. Error represents all aforementioned error causing the dc offset of the emulated current. As shown in (5.12), i_{L_emu} is integrated based on the inductance L and the applied voltage, hence the slope ratio of $i_{L\_emu\_offset}$ is proportional to difference between u_{adj}(s) and error. Because of the sampling period is one ac-line cycle, a 1-order block with the time constant T_{ac} is introduced to the control

diagram and T_{ac} is 16.67 ms in this paper. The transfer function of the control loop is found to be

$$T_{v\_\mathrm{emu}}(\mathrm{s}) = W_{ur}(\mathrm{s}) \cdot \frac{1}{L(T_{ac}\,\mathrm{s}+1)} \tag{5.13}$$

W_{ur}(s) is designed as an integrator, making T_{v_emu}(s) a typical I-type system. The dc offset on ac-side is effectively eliminated by controlling the slope ratio of $i_{L\_emu\_offset}$ to be zero.

5.3 Experimental Verification

5.3.1 System Diagram and Prototype Hardware

The algorithm of the proposed sensorless PCC method is shown in Fig. 5.1. A voltage sensor is still employed to sense the ac-side voltage u_{ac} for the system control. A current emulator employing the proposed current emulation method is introduced to the control diagram and implemented via a digital control chip. The emulator utilizes the control signal S, dc link voltage V_{DC}, and the inverter output voltage u_{ac} to rebuild the inductor current, as indicated by (5.12). The output current sensor and its associated circuits can be removed from the control system. A voltage regulator serves as the voltage loop controller to generate a reference of the inductor current. Parabolic carriers are digitally generated in the micro-controller and are also digitally compared with the

current tracking error. This removes the need for the hardware for generating the parabolic carriers such as DACs or amplifier based circuitry. Analog comparators are replaced by the digital comparison, that eliminates the sensitivity to the noise and improves the reliability of control system. A gating algorithm block generates the proper gating signals for all switches with proper dead-time. A control signal, *S,* is generated by the digital comparator, which is used by both the current emulator and the gating algorithm block. All blocks in the dashed frame can be implemented in a single micro-controller.

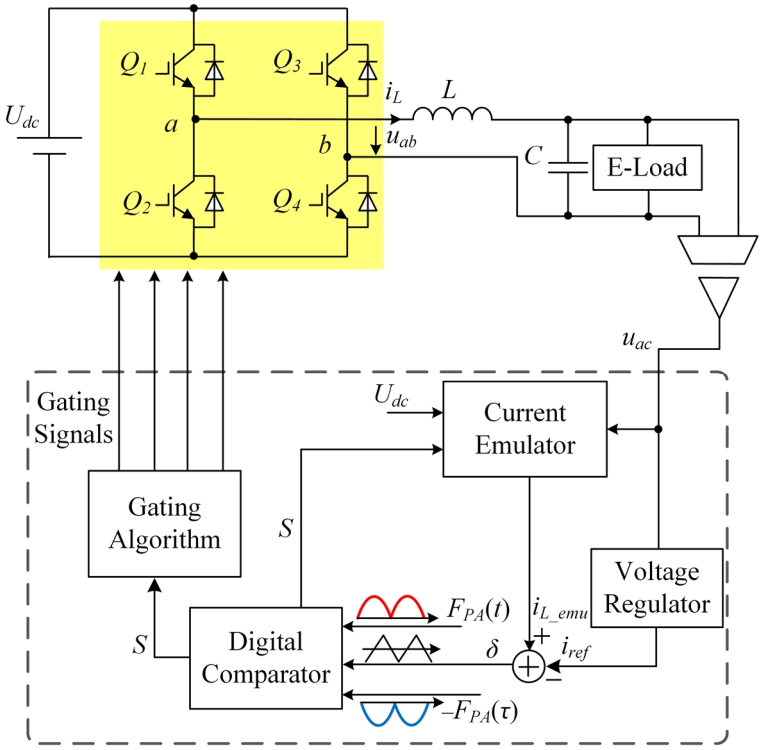


Fig. 5.8 Control diagram of sensorless PCC

Table 5.1 Prototype parameters

Description	Value
Output inductor (L)	3.3 mH
Output capacitor (C)	22 μF
Rated power	1.5 kW
Dc link voltage (V_{DC})	400 V
Ac-side voltage	220 V
Ac-side frequency	60 Hz
Switching frequency	20 kHz
Desired switching period (T^*)	50 μs
Current controller parameter (A_m)	6.061 A
Sampling period of current emulator (T_s)	200 ns

In order to verify the effectiveness of the proposed sensorless control method, an H-bridge VSI prototype with bipolar operation was built and tested. In the experiment, the proposed sensorless PCC strategy is utilized as the current control method. Fairchild FGY75N60SMD IGBTs are used as the main switches in the experiment. A FPGA EP4CE15E22 from Altera is used as the main controller. The inductor current emulator, PCC current controller, and voltage loop controller are all implemented in the FPGA chip. Gating signals are generated with the required dead-time. The capacitance of the output filter is selected to be 22 μF. Other circuit parameters are indicated in Table 5.1. A programmable AC electronic load, 63804 Chroma, serves as the load of the system, generating the required load change and working as a rectifier load to test the inverter performance. A picture of the prototype hardware is shown in

Fig. 5.9.

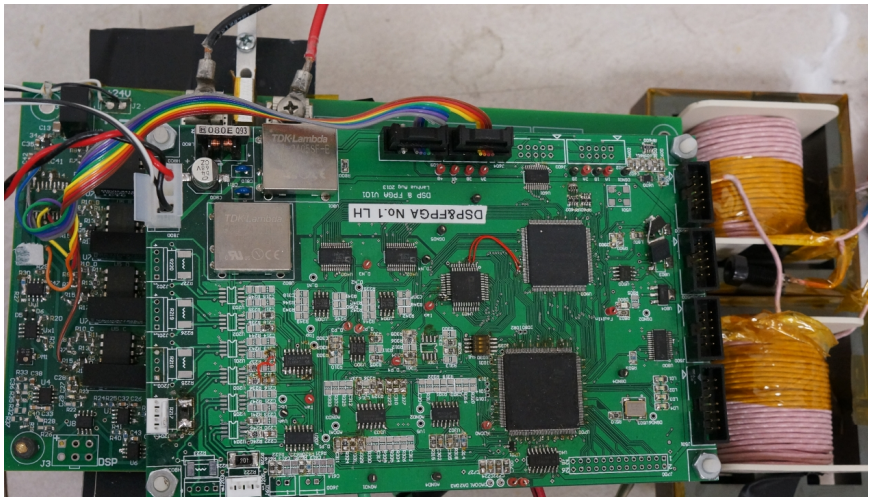
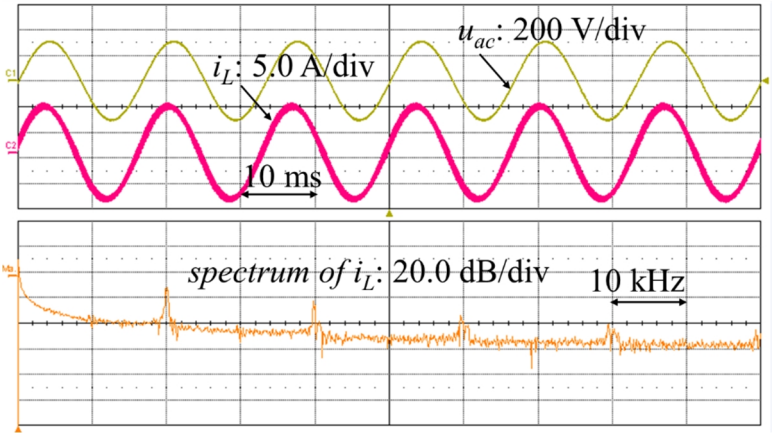


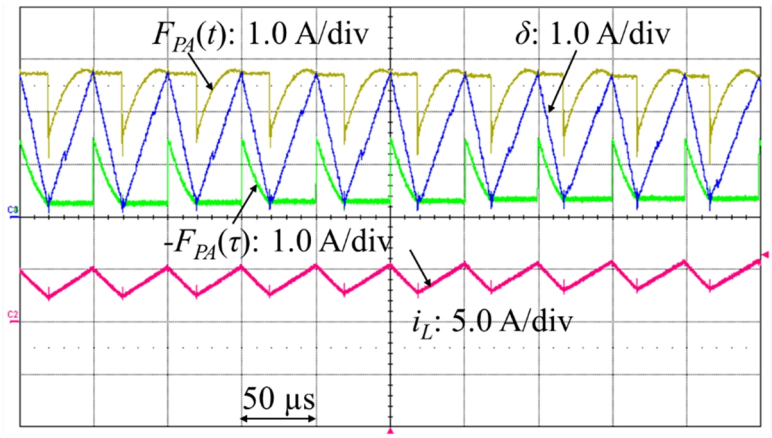
Fig. 5.9 Picture of the prototype hardware

5.3.2 Experimental Results

Experimental results are shown in Fig. 5.10 to Fig. 5.12. Fig. 5.10 shows the steady state waveforms including ac-side output voltage u_{ac}, inductor current i_L and its spectrum, current tracking error δ, and parabolic carriers $F_{PA}(t)$, $-F_{PA}(\tau)$. AC electronic load operates with resistor mode in steady state test. From Fig. 5.10 (a), it can be seen that the shape of i_L and u_{ac} are well controlled. The measured spectrum of inductor current shows the switching frequency converges to the desired value of 20 kHz. In Fig. 5.10 (b), the parabolic carriers and current tracking error are monitored on the prototype hardware. The figure shows the current tracking error, δ, remains within the parabolic control band, confirming that the inductor current precisely follows its reference.



(a)



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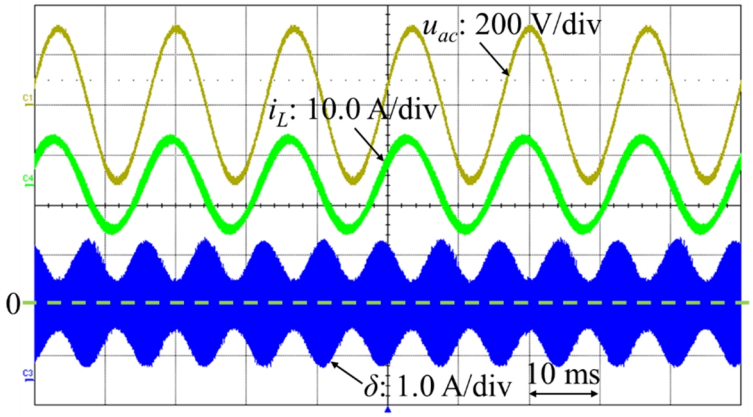
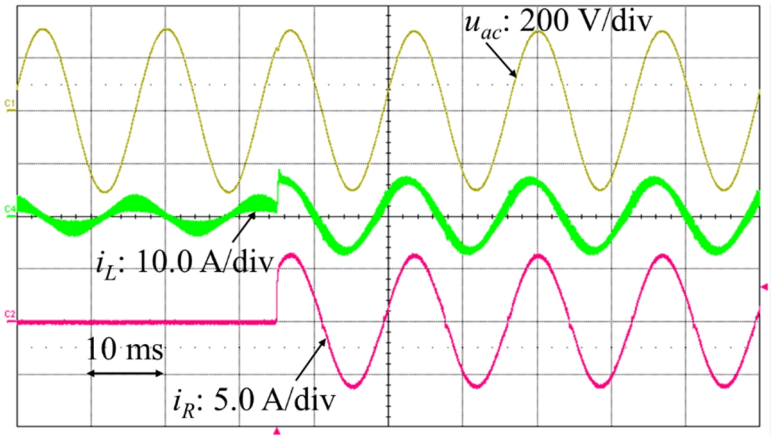


(c)

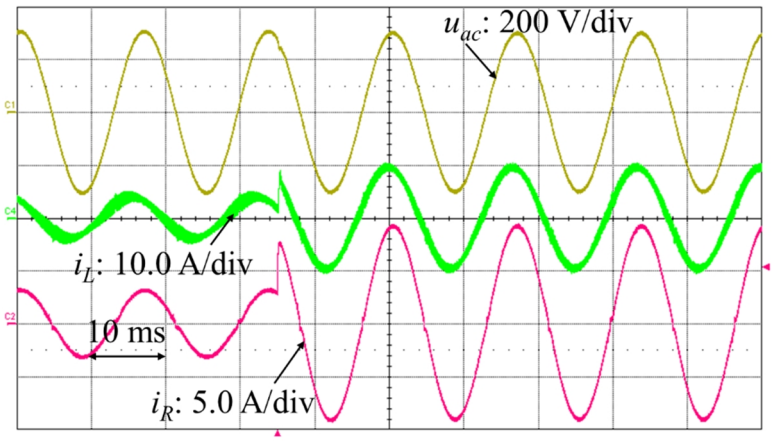
Fig. 5.10 Steady state experimental waveforms

In order to verify the transient performance of the proposed sensorless

control method, a transient response test and rectifier load test are conducted as shown in Fig. 5.11. The experimental waveforms include output voltage u_{ac}, output current i_R or i_{rect}, and inductor current i_L. Fig. 5.11 (a) shows the transient waveforms from no load to a 1 kW resistor load. Fig. 5.11 (b) shows the resistor load change condition from 500 W to 1.5 kW and Fig. 5.11 (c) shows the operating condition changing from 1.5 kW to 500 W. As can be seen from these waveforms, the control system is stable under all operating conditions. The distortion of output voltage waveforms during load change transition is controlled to be very small. Fig. 5.11 (d) shows the non-linear load operating condition, an H-bridge diode rectifier with 1000 uF capacitor with 100 Ω resistor load. Even with non-linear load, the shape distortion of the output voltage is still well controlled.



(a)



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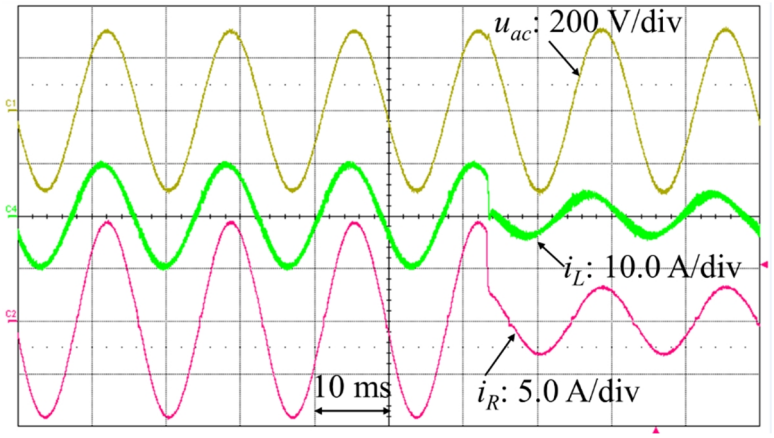

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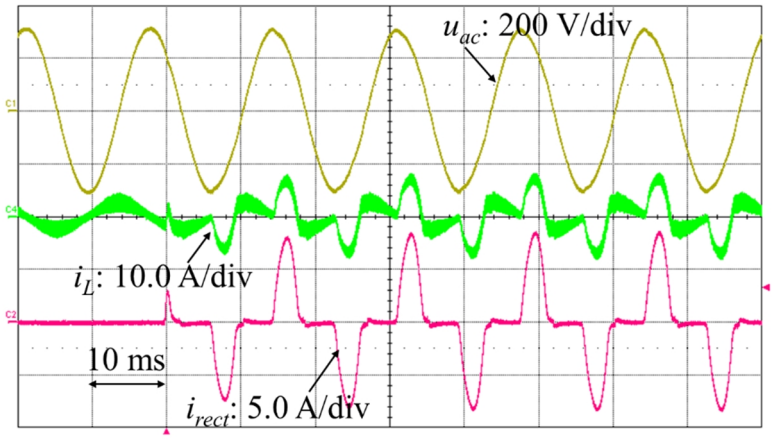
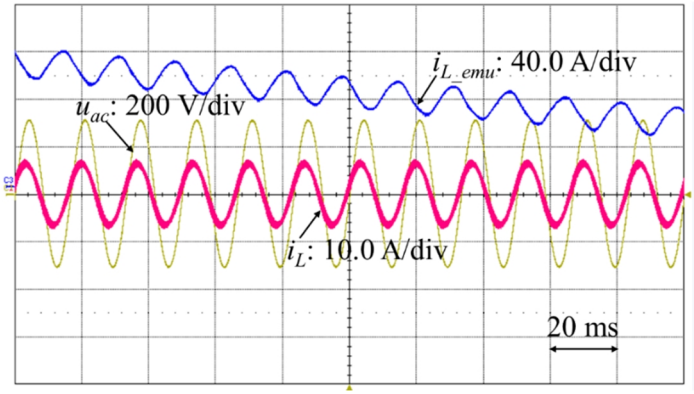


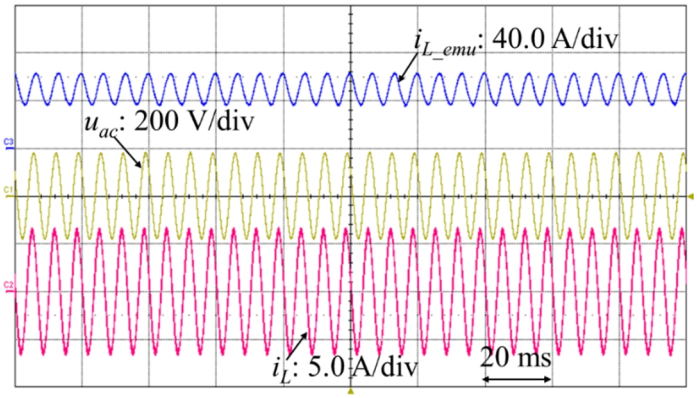
(d)

Fig. 5.11 Transient experimental waveforms

The elimination of the dc offset on the ac-side output voltage is tested and the waveforms are shown in Fig. 5.12. The emulated current i_{L_emu} is monitored by the DAC chip on the control board. Fig. 5.12 (a) shows the operating condition without an offset elimination loop. As can be seen in the figure, the dc offset on i_{L_emu} continuously decreases. Once the offset elimination loop is introduced to the system, i_{L_emu} is maintained at a constant, eliminating the dc offset on the ac-side output voltage, as shown in Fig. 5.12 (b). As measured by a multimeter, the dc offset voltage on u_{ac} is reduced from 0.43 V to 0.03 V.



(a)



(b)

Fig. 5.12 Offset elimination of the output voltage

5.4 Summary

In this chapter, a sensorless PCC method is proposed, analyzed, and verified. Key features of this chapter are as follows:

1) The traditional implementation methods of PCC are reviewed and compared. Hardware requirements, associated cost, and circuit complexity are discussed.
2) By analyzing the inductor current, an inductor current emulation method is proposed. This removes the need for the current sensor and its associated circuitry including the parabolic carrier generator, current conditioning circuitry, and comparators. Thus the system complexity is reduced. Related issues from the circuitry are solved, including the resolution problem and offset of the current sensor, the bandwidth and propagation delay of operational amplifiers and comparator, and the difficulty in generating precise parabolic carriers.
3) The comparison between the parabolic carriers and current tracking error is implemented with a micro-controller, changing the analog comparison to the comparison in program code. The noise sensitivity problem of the analog comparison is solved and system reliability is improved. Furthermore, since the parabolic carriers are generated digitally in a micro-controller, it is easier to adjust the magnitude and

frequency of the carriers.

4) The causes of the dc offset on the ac-side output voltage are analyzed. To eliminate this dc offset, an additional control loop is introduced to the current emulator. An implementation method and control loop design are illustrated.

The performance of the proposed sensorless PCC method is verified by experimental results. A hardware prototype employing the proposed sensorless method achieves good transient performance under the operating conditions of both a resistor load and a nonlinear load such as a rectifier load. The dc offset on the ac-side voltage is eliminated by the proposed control strategy. Constant switching frequency is achieved and current tracking error remains in the parabolic band.

Chapter 6 Single-Step Current Control

6.1 Introduction

With increasing requirements on system power density [77], especially with the fast development of wide bandgap (WBG) semiconductor devices [78]-[80], high switching frequency operation is becoming more popular. Because the filter size of a power electronics system is dependent on switching frequency, high switching frequency has become the most attractive and effective method to improve system power density [78]. Since PCC is the suitable solution for voltage source inverters (VSIs) due to its approximate-constant switching frequency, fast response, and high control precision, it is necessary to discuss the implementation of PCC with high switching frequency.

The initial implementation is based on analog circuits [27]. In [67], two implementations of PCC are discussed and compared, including an analog circuits based implementation and a digital-to-analog converter (DAC) based implementation. A sensorless implementation is also proposed in [67] to simplify the control complexity and improve the noise rejection capability. However, with the increase of switching frequency, all of these implementations carry some disadvantages. To achieve high frequency operation, an analog circuit based solution requires high bandwidth

operational amplifiers and high speed analog comparators. Similarly, a DAC based solutions requires DAC circuits with high conversion speed. Finally, since the sensorless solution proposed in [67] is based on current emulation strategy, the control error relies on the number of discretion time-steps in a switching period. Then with an increase of switching frequency, a micro-controller with high clock frequency is required to ensure the control precision. These disadvantages limit the switching frequency of PCC to 20 kHz range [27]-[67]. Thus, it is necessary to propose either a proper high-frequency implementation method for PCC or a new control scheme with similar or better performance.

In this chapter, the convergence of PCC will be analyzed then a new digital control strategy is proposed, named single-step current control (SSCC). Small signal model and dead-time effects are analyzed. The performance of the proposed SSCC is verified by prototype hardware of an H-bridge voltage source inverter.

6.2 Convergence Analysis of PCC

Convergence is defined as the iteration process towards the steady state from a transition state and it also indicates the stability of the control loop. The convergence process of PCC is firstly discussed in [28] and a similar discussion for parabolic voltage control is conducted in [81]. The basic

operation rules of PCC and its transition process are shown in Fig. 6.1 [28]. At steady state, with PCC, the current tracking error converges to δ^*, as indicated by the dashed line, with the turn-on time T_p^* and turn-off time T_n^*. D^* is the duty-cycle at steady state. The positive peak of δ^* is indicated by δ_p* and the negative peak of δ^* is indicated by δ_n*.

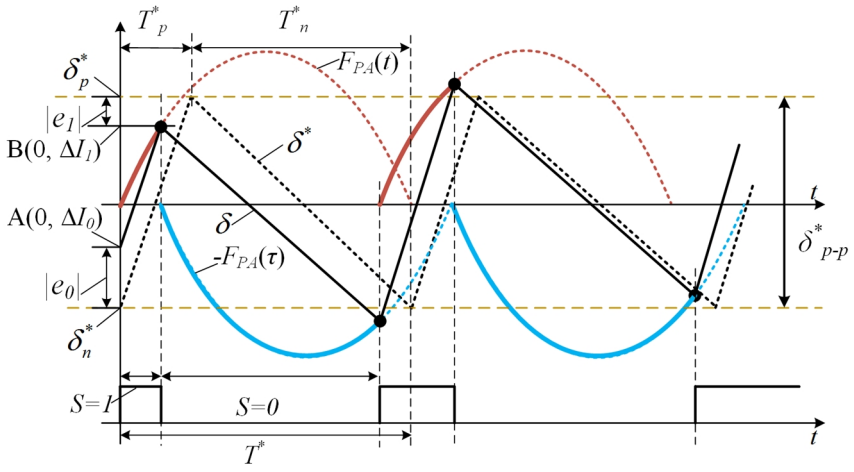


Fig. 6.1 Basic operation and convergence process of PCC

In Fig. 6.1, the transition starting point of δ is A(0, ΔI_0), and δ locates at B(0, ΔI_1) at the next switching operation. Converging error e_i is used to indicate the difference between transition and steady state after i times of switching transitions, and it is defined as $e_i = |\Delta I_i| - |\delta^*|$. $(i = 0,1,2...)$. Then the initial point A has a converging error e_0 and B has a converging error e_1 [28],[81]. The relation between e_0 and e_1 can be obtained based on the relations in the figure. Beginning with the same initial converging error $e_0 = -\dfrac{D^*(1-D^*)A_m}{2}$, the converging process across different duty-cycles can be

obtained after several iterations, as shown in Fig. 6.2. It is shown that with smaller $\left|0.5-D^*\right|$, the transient response is faster and the fastest converging speed is the condition $D^*=0.5$.

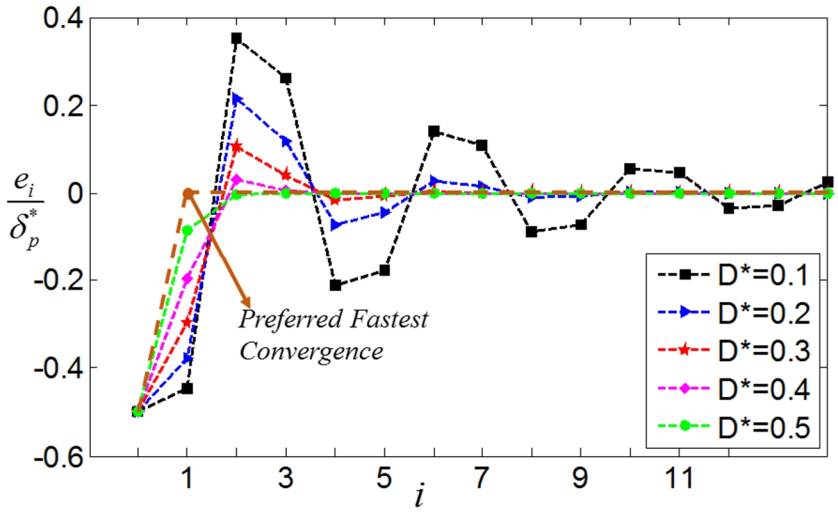


Fig. 6.2 Convergence of PCC

Although PCC converges within just a few switching operations, it is still desirable to converge to the steady state after just one switching operation, which is marked as preferred fastest convergence in Fig. 6.3. This observation promotes the need for a new control strategy with the fastest convergence, which will be discussed in the following section.

6.3 Proposed Single-Step Current Control

6.3.1 Single-Step Current Control

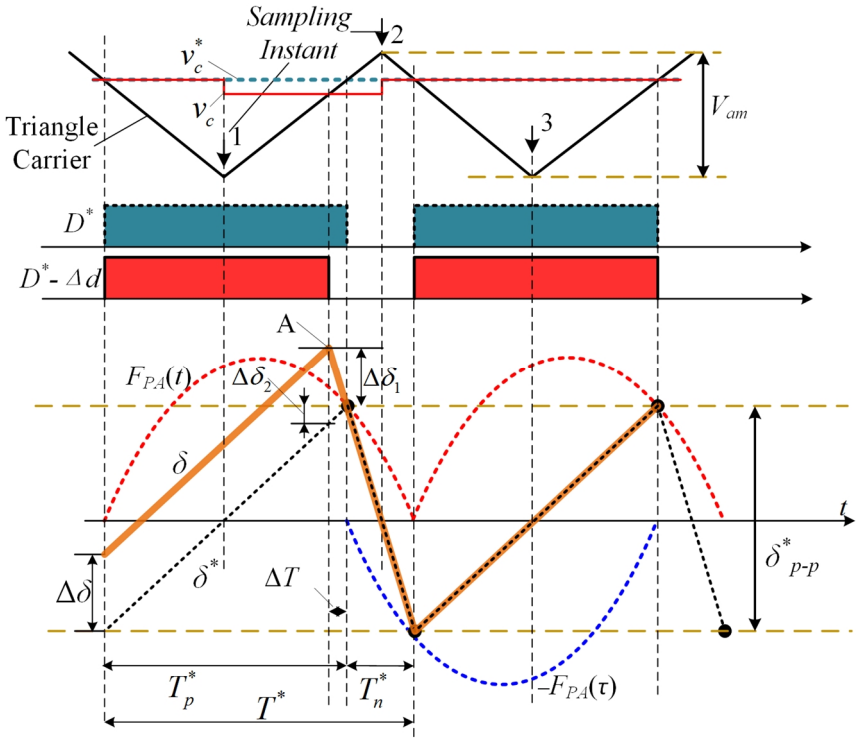


Fig. 6.3 Proposed single-step current control

In digital control systems, pulse-width modulation (PWM) is usually implemented by the comparison between a reference voltage and a triangle carrier, as indicated by Fig. 6.3. The new duty-cycle is usually updated at the bottom and top of the triangle carrier. In this figure, the static control duty-cycle D^* is generated by the comparison of control voltage v_c^* and the triangle carrier. In the proposed SSCC control strategy, the inductor current is sensed at the sampling instants, which is set at both the bottom and top of triangle carrier. Since at steady state the current tracking error δ is zero at these sampling instants, the deviation of δ can be easily obtained at these

sampling instants. Peak to peak current tracking ripple at steady state is defined as $\Delta\delta^*_{p-p}$. ΔT is the control variable generated by the proposed controller to adjust the duty-cycle. In Fig. 6.3, the current tracking error δ is sampled at time instant 1. It is evident that δ deviates from δ^* and proper control is required to adjust δ. The proposed control strategy with fast convergence process swiftly brings the current tracking error δ to converge to δ^* after just one switching operation, as indicated by A in Fig. 6.3. In this way, after the switching operation at A, the current tracking error matches δ^*.

To derive the adjusting time ΔT, the following equations are obtained from Fig. 6.3.

$$\Delta\delta = \delta - \delta^* \tag{6.1}$$

$$\Delta\delta = \Delta\delta_1 + \Delta\delta_2 \tag{6.2}$$

$$\frac{\Delta\delta_1}{\Delta T} = \frac{\delta^*_{p-p}}{T_n^*}, \frac{\Delta\delta_2}{\Delta T} = \frac{\delta^*_{p-p}}{T_p^*} \tag{6.3}$$

$$\frac{\Delta\delta}{\Delta T} = \delta^*_{p-p}\left(\frac{1}{T_p^*} + \frac{1}{T_n^*}\right) \tag{6.4}$$

$$\Delta T = \frac{\Delta\delta T_p^* T_n^*}{\delta^*_{p\text{-}p} T^*} = \frac{\Delta\delta}{\delta^*_{p\text{-}p}}(D^*(1-D^*)T^*) \tag{6.5}$$

Since $\delta^*_{p-p} = 2A_m(D^* - D^{*2})$ [27]-[28], the adjusting time can be obtained as

$$\Delta T = \frac{\Delta \delta T^*}{2A_m}. \tag{6.6}$$

Then the new turn-on time can be obtained as

$$T_p = T_p^* - \Delta T. \tag{6.7}$$

In Fig. 6.3, to implement this turn-on time adjustment, the new control voltage is updated at time instant 1. If the amplitude of the triangle carrier is V_{am}, then the adjustment of control voltage can be obtained as

$$\Delta v_c = v_c^* - v_c = \frac{2\Delta T V_{am}}{T^*}. \tag{6.8}$$

And the adjusting duty-cycle is

$$\Delta d = \frac{\Delta T}{\frac{T^*}{2}} = \frac{\Delta \delta}{A_m} \tag{6.9}$$

Similarly, if the transition happens at time instant 2, the turn-off time can be adjusted as well. Two sampling points in one switching cycle ensures high transient response speed. This proposed current control strategy is named single-step current control (SSCC).

Simulation results in PSIM are shown in Fig. 6.4. A square waveform source is used to add 1 A current perturbation to the feedback loop, which causes the current tracking error to jump 1 A at the perturbation instant. With the same perturbation added to SSCC and PCC with $D^* = 0.8$, it is seen that

SSCC recovers back to steady state after a single switching operation whereas PCC takes approximately 5 switching operations to recover.

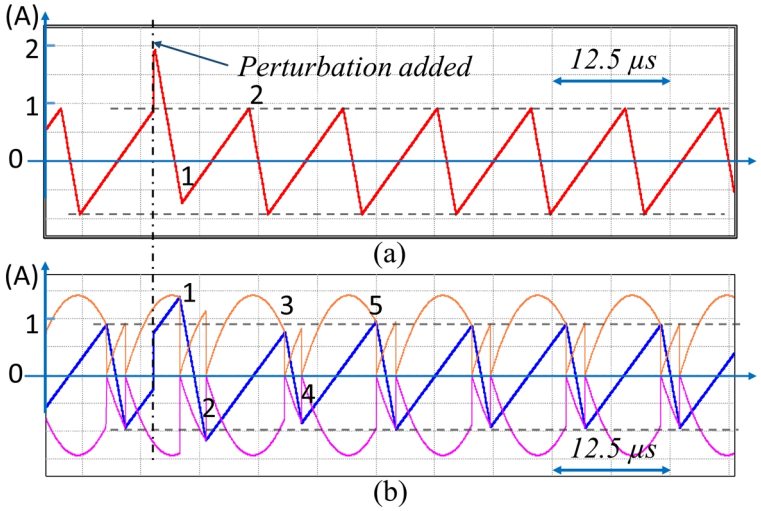


Fig. 6.4 Convergence speed comparison with PCC: (a) SSCC; (b) PCC.

6.3.2 Range of Current Tracking Error

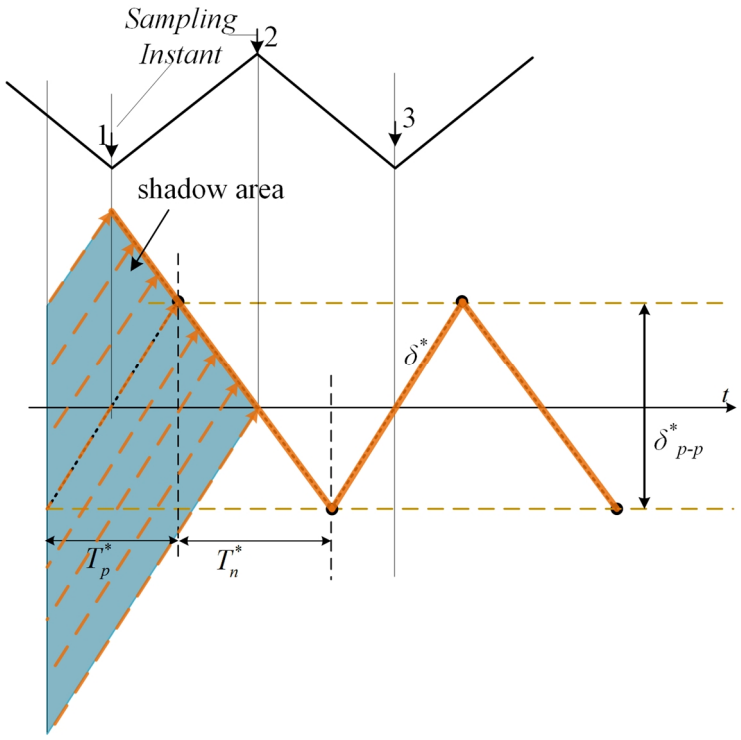


Fig. 6.5 Range of current tracking error

The current tracking error can converge to steady state after just one switching operation with SSCC. However, (6.9) has a limitation to the range of current tracking error. If the difference between transient current and steady state current is too large, the result of (6.9) could result a duty-cycle larger than one or smaller than zero, coming out a meaningless result. A shadow area is shown in Fig. 6.5 to indicate the range of current tracking error that (6.9) applies. At sampling instant 1, if the current tracking error δ falls into the shadow area, it can converge to steady state at the next sampling point. The possible current tracking errors in the shadow area are indicated by the dashed arrows. If δ is out of the shadow area, it is impossible to complete the convergence after one switching operation because the current slope ratio of the converter. Full duty-cycle is used if δ is below the shadow area and zero duty-cycle is used if δ is above the shadow area. Inductor current converges to the reference as fast as possible, limited by the maximum slope ratio of the converter.

6.4 Small Signal Model

6.4.1 Shift of Sampling Instant

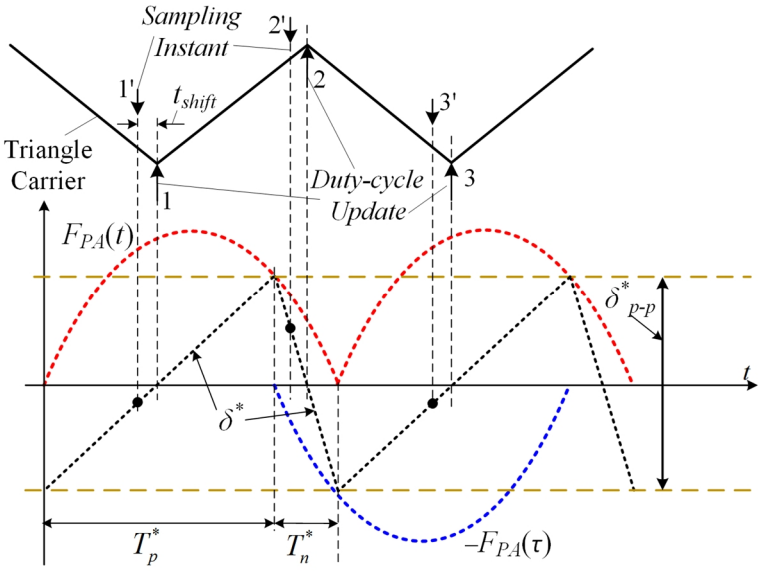


Fig. 6.6 Shift of sampling instant

In a digital signal processor (DSP), the updating instants of a new duty-cycle are usually set at the top and bottom of a triangle carrier. As indicated by Fig. 6.3, because of the conversion time of analog-to-digital conversion (ADC) and additional calculation time for duty-cycle adjustment, the new duty-cycle cannot be updated simultaneously at the sampling instant and the fastest update occurs in the next sampling instant. This introduces a half switching cycle control delay. To avoid this delay, the current sampling instant can be shifted ahead of the duty-cycle update instant, as indicated in Fig. 6.6. Sampling instant 1 is shifted to 1' and sampling instant 2 is shifted to 2'. The determination of t_{shift} relies on ADC conversion time and calculation time. To get correct current information at the top and bottom of the triangle carrier,

the sampled data requires compensation before calculating the next duty-cycle. In this way, the sampling instant and the duty-cycle update are separated and the half switching cycle control delay is avoided.

The compensation can be obtained based on the slope ratio of the current tracking error, which is determined by ac-side and dc-side voltage, inductance of output inductor, and shifted time t_{shift}. At current sampling instant 1',

$$i_{L1} = i_{L1}' + \frac{2A_m(1-D^*)t_{shift}}{T^*}, \tag{10}$$

where i_{L1}' is the sensed current at time instant 1' and i_{L1} is the calculated inductor current at instant 1. Similarly, at current sampling instant 2',

$$i_{L2} = i_{L2}' - \frac{2A_m D^* t_{shift}}{T^*}, \tag{11}$$

where i_{L2}' is the sensed current at instant 2' and i_{L2} is the calculated inductor current at instant 2.

6.4.2 Small Signal Model

From (6.9), the proposed current control strategy is equivalently a proportional controller then the small signal model and equivalent bandwidth can be analyzed. The control diagram is drawn in Fig. 6.7. K_p is the equivalent gain of SSCC and from (6.9),

$$K_p = \frac{1}{A_m}. \tag{6.12}$$

H_v indicates the gain of power stage,

$$H_v = 2V_{DC}. \tag{6.13}$$

$e^{-\frac{T^* s}{4}}$ is the PWM stage delay. It is seen that single-step current control is a special case of proportional current control. The transfer function of the current loop can be obtained as

$$T_i(s) = \frac{K_p H_v e^{-\frac{T^* s}{4}}}{Ls} = \frac{2V_{DC} e^{-\frac{T^* s}{4}}}{A_m Ls} = \frac{2e^{-\frac{T^* s}{4}}}{T^* s}. \tag{6.14}$$

Crossover frequency f_c is

$$f_c = \frac{1}{T^* \pi}. \tag{6.15}$$

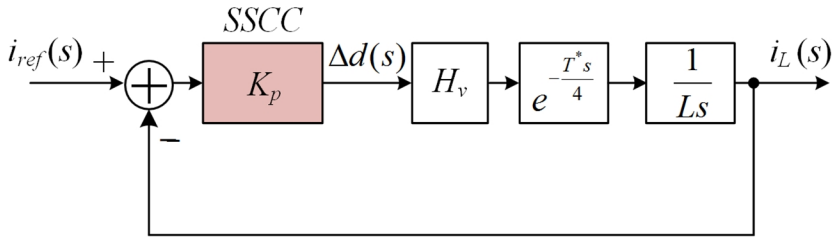
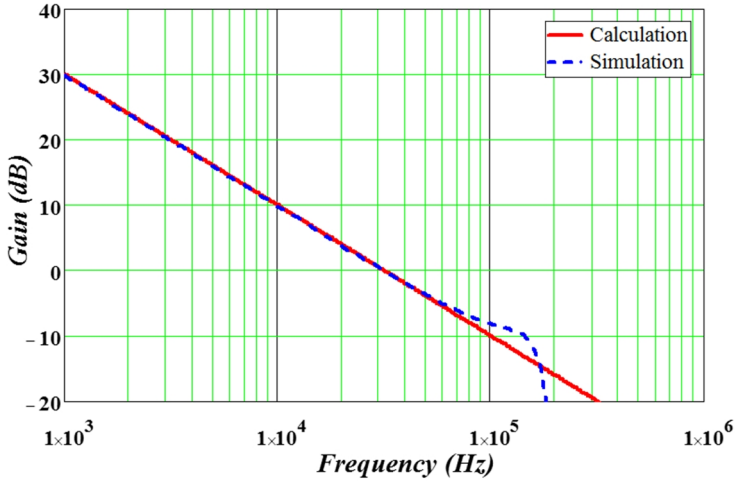
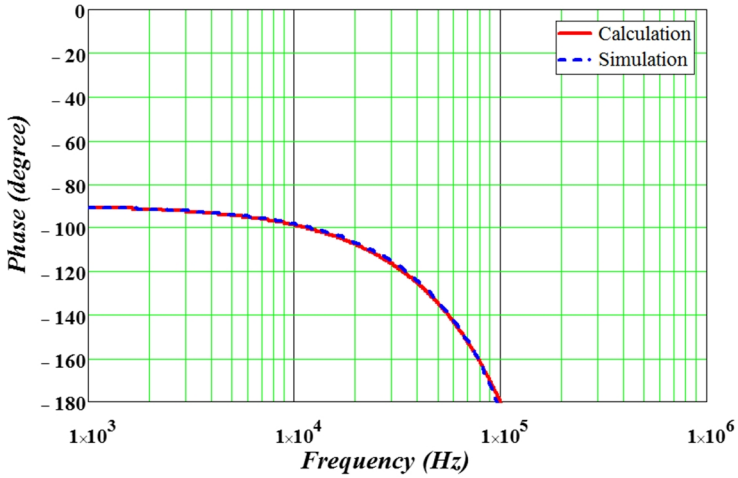


Fig. 6.7 Current loop diagram



(a)



(b)

Fig. 6.8 Bode plot of SSCC

As detailed later in this paper, a switching frequency of 100 kHz is chosen for the verification prototype. Here, we use that 100 kHz frequency for the verification of the small signal model. The transfer function bode plot of $T_i(s)$ is shown in Fig. 6.8 and a bandwidth of 31.8 kHz with a phase margin of 63 degrees is obtained, which is close to the one third of the switching frequency. Meanwhile the simulated bode plot matches well with the calculated result,

which proves the effectiveness of the derived small signal model.

6.5 Analysis of SSCC

6.5.1 *Dead-time Compensation*

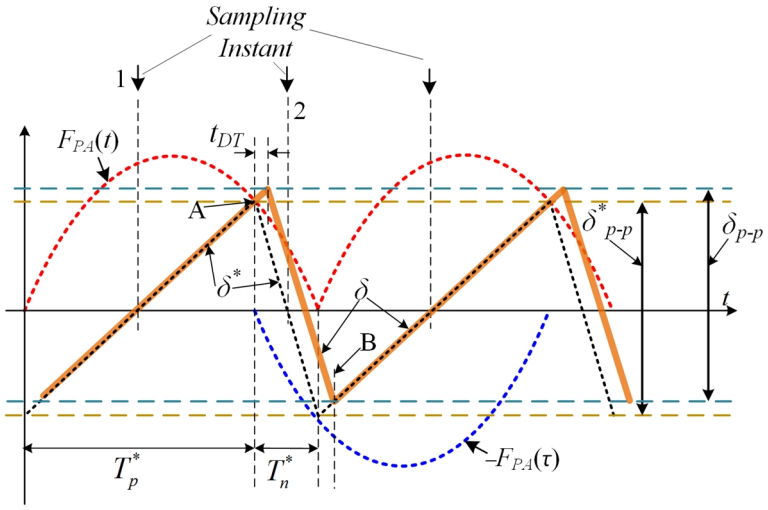


Fig. 6.9 Dead-time effect

As indicated by Fig. 6.9, if the current of the output inductor is below zero (current direction is defined in Fig. 2.2), when Q_1 and Q_4 are turned off at time instant A, output current still goes though the anti-paralleled diode of Q_1 and Q_4 and the current tracking error keeps increasing until Q_2 and Q_3 are turned on [66]. In this scenario, the current tracking error cannot match with δ^* and an overshoot is introduced. At time instant B, because the output current is below zero, the trend of current tracking error alternates simultaneously when the Q_2 and Q_3 are turned off. So dead-time t_{DT} would not impact this switching operation. Finally, the average value of current tracking error

deviates from zero and δ_{p-p} deviates from $\delta_{p-p}{}^{*}$. The average value of the current tracking error can be obtained based on the slope ratio of the current tracking error and dead-time

$$\delta_{avg\_DT} = \frac{2A_m(1-D)t_{DT}}{T^*}. \tag{6.16}$$

The effect of dead-time can be compensated by changing the adjusting time ΔT based on the direction of the output current. If output current is below zero, the adjusting time on falling slope of δ stays the same and the adjusting time on rising edge ΔT should be changed to

$$\Delta T = \frac{\Delta\delta T^*}{2A_m} + t_{DT}. \tag{6.17}$$

6.5.2 Error Effects

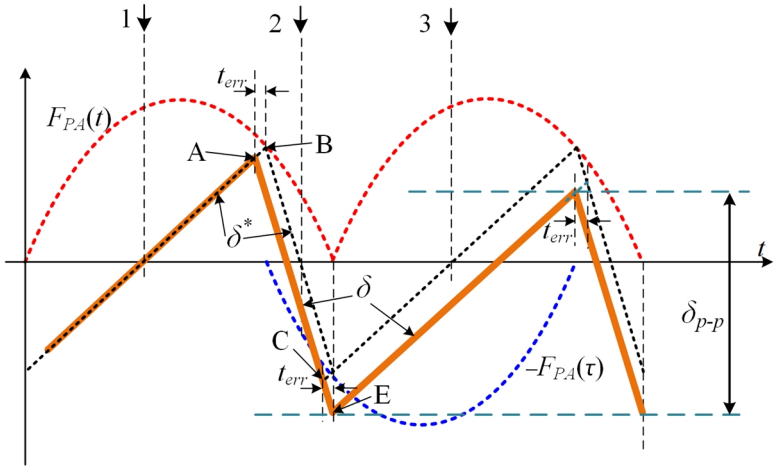


Fig. 6.10 Error effects

Next to dead-time, also other errors exist in digital converters, such as

PWM resolution error. For a new proposed control method, it is necessary to analyze the control performance with errors, because errors may cause the convergence of SSCC to fail. As indicated by Fig. 6.10, t_{err} is the PWM resolution error which causes a leading time of the turn-off instant and a lagging time of the turn-on instant. The rising slope of current tracking error is planned to turn off at point B to match with δ^*. Due to t_{err}, the turn-off point is changed to point A. After that, at the next sampling time instant 2, the turn-off instant is planned at point C. Due to t_{err}, the turn-off instant is changed to point E. At the next switching operation, because the same t_{err} remains, the current tracking error is stabilized. This proves control system immune to PWM resolution error.

Similar to the effect of dead-time, a tracking offset is introduced by t_{err}. The average value of the current track error with t_{err} can be obtained as

$$\delta_{avg\_err} = -\frac{\frac{2A_m(1-D^*)t_{err}}{T^*} + \frac{2A_m D^* t_{err}}{T^*}}{2} = -\frac{A_m t_{err}}{T^*}. \qquad (6.18)$$

6.5.3 Control Diagram

From (6.7) to (6.9), it can be seen that SSCC generates ΔT (or Δv_c) to adjust the duty-cycle. This adjustment is applied to the steady state duty-cycle D^* (or v_c^*). So the performance of the proposed current control strategy still

relies on the steady state duty-cycle D^* (or v_c^*). For VSIs, this can be obtained based on the ac-side voltage and dc-side voltage. However, the accuracy of calculated D^* cannot be ensured because of sensing error, parasitic elements, and calculation error. A proportional–integral (PI) controller is proposed to help provide an accurate D^*, as indicated in Fig. 6.11. In addition, the steady-state error caused by the PWM resolution error can be compensated by the PI controller as well. Since the PI controller is just to adjust the duty-cycle of steady state, the gain can be very small so the impact on the small signal model of SSCC can be neglected.

The system diagram is shown in Fig. 6.11. A bipolar modulation method is employed, which means Q_1 Q_4 share the same switching signal and Q_2 Q_3 share the same switching signal. Current tracking error is obtained by the subtraction between the sensed inductor current i_L and inductor current reference i_{ref} then fed into the SSCC block and a PI controller. Ac-side voltage is sensed to calculate the duty-cycle at steady state. For a stand-alone inverter, voltage reference is used to calculate the duty-cycle at steady state. A voltage loop is required to generate the current reference based on the output voltage on the ac-side.

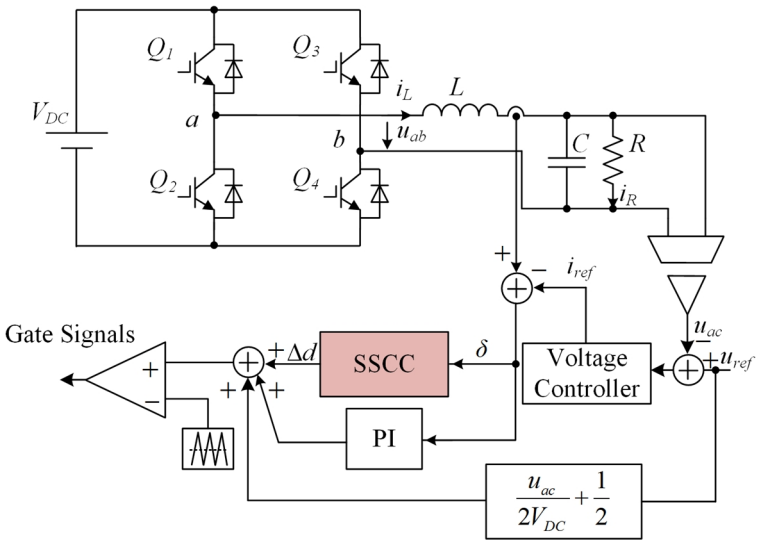


Fig. 6.11 System diagram

6.6 Experimental Verification

A hardware prototype is built to verify the proposed current control strategy. The control board includes a Texas Instruments (TI) microcontroller TMS320F28335 combined with current conditioning circuits to verify SSCC and an Altera FPGA EP4CE15E22 combined with DACs and comparators to verify the convergence speed of PCC. The power stage is a typical H-bridge voltage source inverter utilizing high speed Infineon IGBT IGW40N65F5 to achieve high switching frequency. Other circuit parameters are shown in Table 6.1.

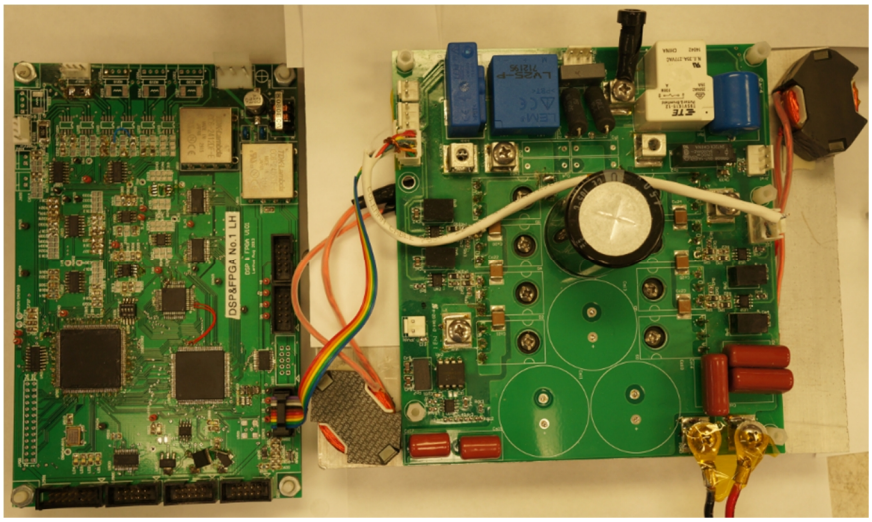


Fig. 6.12 Prototype hardware

Table 6.1 Prototype hardware parameters

Description	Value
Inductor (L)	700 μH
Output capacitor (C)	4.7 μF
Rated power	1.6 kW
Input voltage (V_{DC})	400 V
Output voltage	220 V
Ac-side frequency	60 Hz
Switching frequency	100 kHz
Parabolic Control Parameter	5.71 A

Experimental waveforms and setup are shown in Fig. 6.13 to Fig. 6.19. Fig. 6.13 shows the transient response with D^*=0.5 and a square current reference with 2.5 A amplitude and 60 Hz frequency. Here, it can be seen that the steady state current waveform is stable. In the zoomed-in current waveforms, full duty-cycle is used to track the step-up current reference and zero duty-cycle is used to track the step-down current reference, which ensures fast response

speed with constant switching frequency. To compare the convergence speed with PCC at various duty-cycles, a dc voltage source which can absorb current is required at the output side of the prototype inverter. To construct a simple voltage source with current-sinking capability, another dc power supply V_{DCS} and resistor load R_S are introduced, as indicated in Fig. 6.14. The current going though R_S is set to be larger than the maximum current of i_L, then V_{DCS} can still regulate the voltage across R_S without sinking current. Fig. 6.15 and Fig. 6.16 illustrate the convergence speed for both PCC and proposed SSCC. In Fig. 6.15, both parabolic current carriers, current tracking error, and inductor current are illustrated at a current step-up transition. It takes around 5 switching operations to transit to the new steady state. While in Fig. 6.16, with the help of the proposed SSCC, the new steady state is achieved after just one switching operation, proving the fast convergence speed of SSCC.

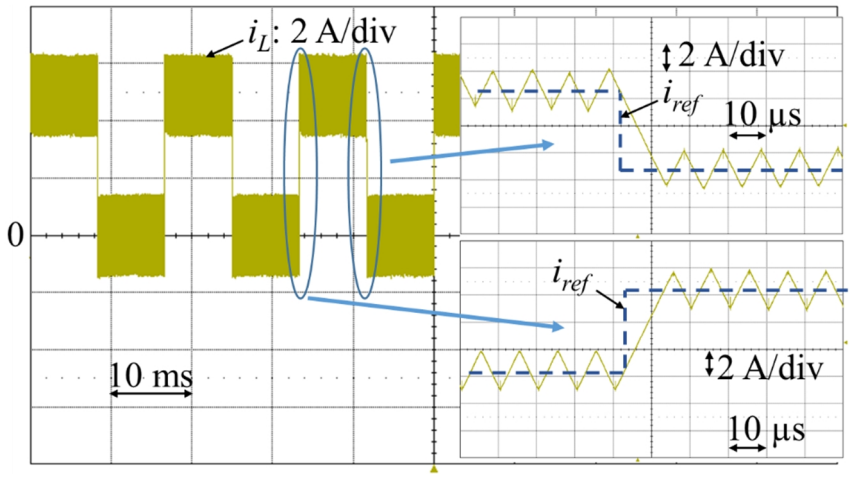


Fig. 6.13 Transient response test of SSCC

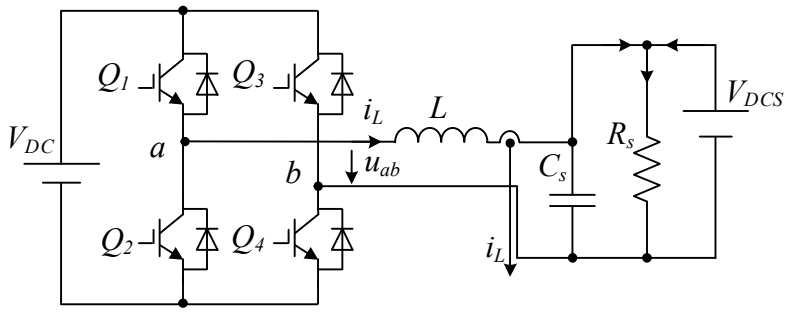


Fig. 6.14 Dc voltage source with current current-sinking capability

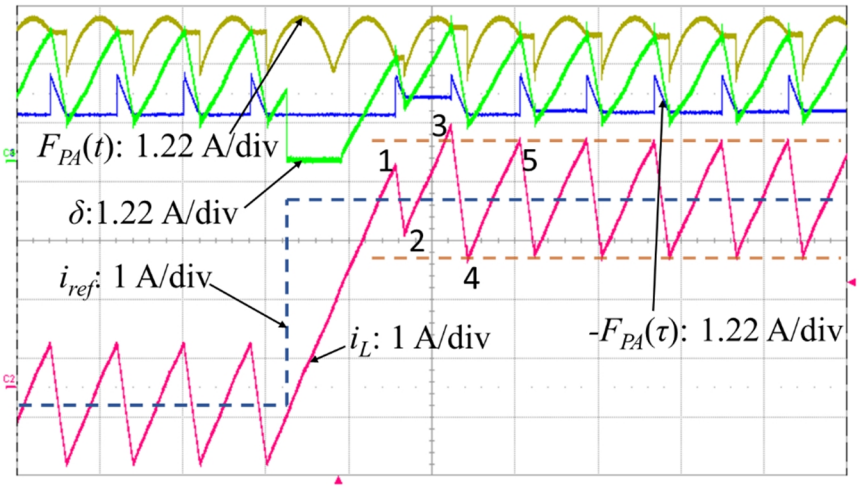


Fig. 6.15 Convergence process of PCC

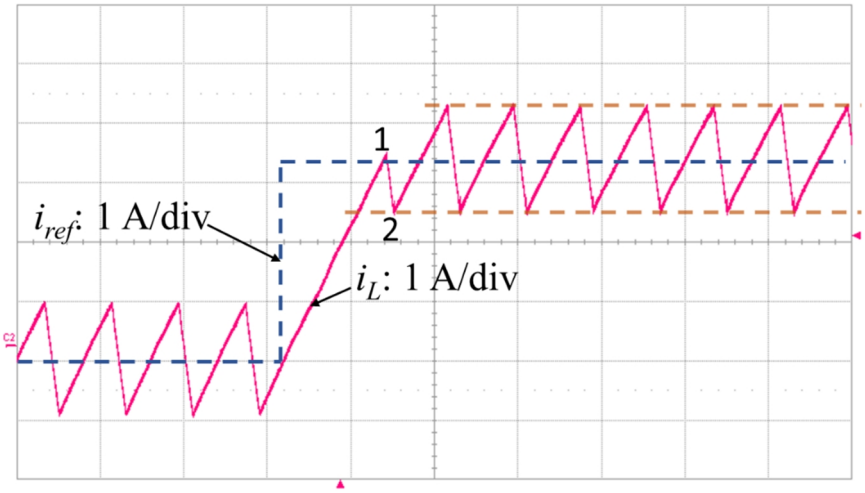


Fig. 6.16 Convergence process of SSCC

Stand-alone inverter test results are shown in Fig. 18 to Fig. 20. The system

configuration is the same as the diagram in Fig. 12. Ac-side output voltage is sensed and passed to the voltage regulator which generates a current reference for the internal current loop. Electronic load under resistor mode is used to test the load step change performance. From the experimental waveforms shown in these three figures, it can be seen that the fast response of the current loop limits voltage sag or overshoot during load transition and also helps to minimize the voltage distortion at steady-state.

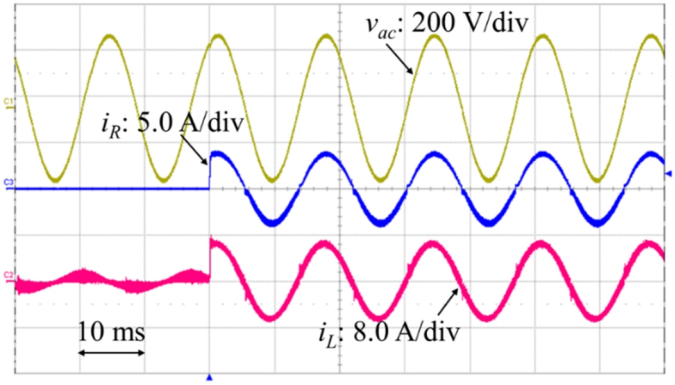


Fig. 6.17 Transient test from no load to 600 W

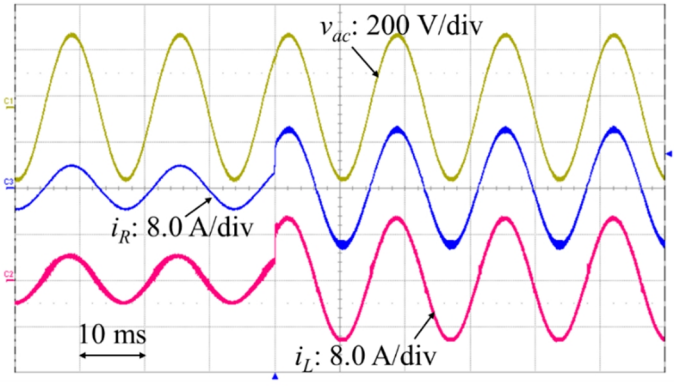


Fig. 6.18 Transient test from 600 W to 1600 W

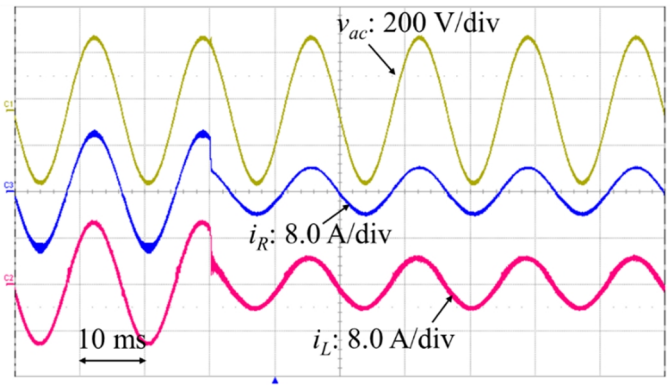


Fig. 6.19 Transient test from 1600 W to 600 W

6.7 Summary

In this chapter, inspired by the convergence analysis of parabolic current control, a new control strategy named single-step current control is proposed and verified by experimental results. Key features of this chapter include:

1) Based on the convergence analysis of parabolic current control, a new current control strategy is proposed and the derivation process is introduced in detail. The proposed control strategy achieves fast current response along with single-step convergence speed and constant switching frequency. Simulation initially verifies these results by comparing the convergence speed of single-step control with parabolic current control.

2) By shifting the sampling instant ahead and predicting the current at the duty-cycle update instant, effects of calculation and update delay in digital controller are eliminated and the only delay in the control loop is

PWM stage. In addition, the small signal model of the proposed control strategy is derived and simulation results match well with calculation results. From the analysis result, it is seen that single-step current control is a special case of proportional current control.

3) Dead-time compensation and error effects are studied. It is found that dead-time would introduce a dc-offset that can be compensated by changing the adjustment of duty-cycle. To generate an accurate duty-cycle at steady state, a PI controller is introduced to the control loop.

4) Experimental results confirm the fast convergence speed of the proposed single-step current control. In addition, a double-loop-controlled voltage source inverter is designed. Test results indicate that the fast response of signal-step current control ensures minimized voltage waveform distortion.

5) The proposed control strategy is fully compatible with Texas Instruments C2000 series micro-controller and the implementation is much easier than parabolic current control. Meanwhile, the switching frequency of the proposed strategy is pushed to 100 kHz, which is helpful for power density improvement.

Chapter 7 Parabolic Voltage Control

7.1 Introduction

With the rapid development of portable power electronic devices and the urgent demand for higher power density and lower environmental impact, the efficiency of power converters has become increasingly important [89]-[97]. To reduce the power loss of power converters, high conversion efficiency is required not only at full load but also with light load and no load conditions. To improve the conversion efficiency at light load and no load, burst mode control is widely employed in power converters [96]-[103].

The most common and simple burst mode strategy is hysteresis burst mode [89], [96]-[99]. With hysteresis burst mode control, the internal current loop is enabled or disabled by the converter output voltage V_o and the two hysteresis bands. When V_o intersects with the bottom hysteresis band, internal current loop is enabled and V_o starts to increase. Internal current loop is disabled when V_o intersects with the top hysteresis band. Burst frequency (frequency of the enable signal for the internal current loop) varies with the change of load if both the current limit and hysteresis band are fixed. These operation principles are indicated by the inductor current in Fig. 7.1, where a hysteresis burst mode boost converter is taken as an example. Under no load condition, the burst

frequency of the inductor current waveforms is very low. With an increase in load, the burst frequency also increases, initiating the frequency variation problem.

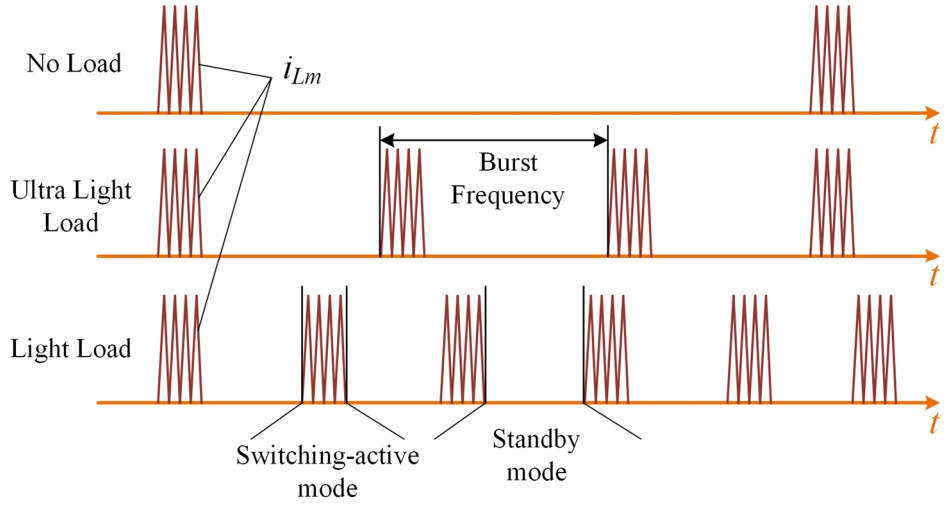


Fig. 7.1 Current waveforms of a burst mode converter with different load

Magnetizing components in power converters, such as inductors, transformers, and electromagnetic interference (EMI) filters introduce audible noise to the system when the variable burst frequency falls into the audible range 20 Hz ~ 20 kHz [98]-[103]. The cause and the undesired magnetic component's audible noise is discussed in [101]-[103]. For portable ac-dc power supplies, because they are close to consumers, the audible noise should be especially avoided [101]. To minimize this audible noise, both mechanical methods and electrical solutions are available [101]-[103]. Mechanical strategies are based on techniques that utilize gluing or potting methods to minimize vibrations or sound-isolation material to dampen the noise. Yet,

these mechanical methods increase the system complexity and manufacturing cost. Compared with mechanical methods, electrical methods are more effective without introducing additional cost [101]. One effective electrical method is to employ a constant, non-audible burst frequency [90],[100]. This method employs a sawtooth carrier, working with the reference current to generate the effective period of the switching-active mode. The voltage loop generates a current reference by a proper controller such as a PI controller. However, this voltage loop controller impacts system response speed and stability. Another audible noise reduction method is studied in [103]. This method monitors the burst frequency to adjust a current reference of the internal loop to limit the minimum frequency and stay away from the audible noise range. However, due to the detection of switching frequency and peak-current programming circuits, system complexity is increased.

This chapter proposes a parabolic voltage control (PVC) method, originating from parabolic current control (PCC), to more effectively eliminate the audible noise of burst mode power converters [27]-[67]. PCC strategy employs a pair of parabolic carriers as a control band to solve the switching frequency variation problem of hysteresis current control while maintaining both a fast transient response and a high control precision at steady state. Similarly, PVC employs a pair of parabolic carriers as the control band to generate control signals for

the internal current loop of the burst mode power converter, solving both the frequency variation and audible noise problems of burst mode converters.

In this chapter, a burst mode boost converter is employed as an example to derive the operating principles of PVC. After the derivation of PVC is completed, comparison between PVC and PCC is studied. Finally, prototype hardware of quasi-resonant boost converter is built and tested to verify the proposed PVC strategy.

7.2 Operation of the Hysteresis Controlled Boost Converter

7.2.1 Operation of the Hysteresis Controlled Boost Converter

A boost converter is taken as an example and the diagram is shown in Fig. 7.2. The operation principles are shown in Fig. 7.3. In order to improve the efficiency and simplify the control, burst mode with hysteresis voltage control is employed and quasi-resonant operation is achieved. As shown in Fig. 7.3, when u_{co} intersects with the voltage lower limit $u_{co\text{-}min}$, S_v is set to 1, then the converter is switched to switching-active mode and capacitor voltage starts to increase. When u_{co} intersects with the voltage upper limit $u_{co\text{-}max}$, S_v is set to zero, then the converter switches back into standby mode where the switch Q is turned off and the output voltage u_{co} decreases. u_{ref} is the reference for the output voltage u_{co}. Hysteresis voltage control introduces both a fast voltage

control response and a fixed output voltage ripple with a simple implementation. However, as aforementioned, the frequency of S_v varies with the change of load and introduces audible noise to the system.

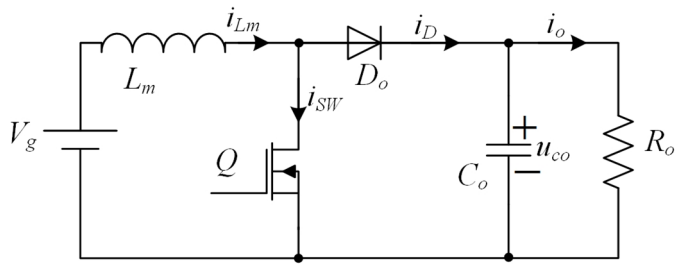


Fig. 7.2 Boost converter

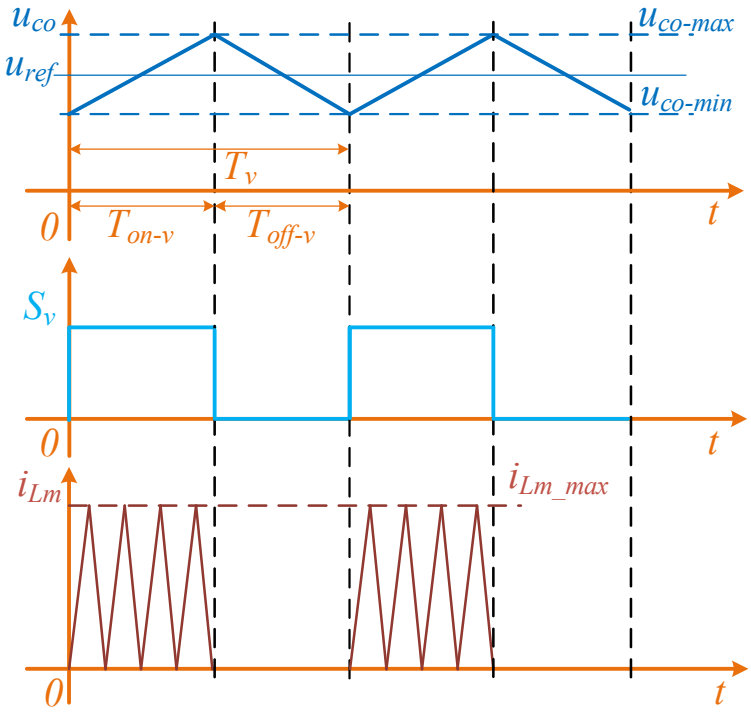


Fig. 7.3 Operating principles of the hysteresis controlled boost converter

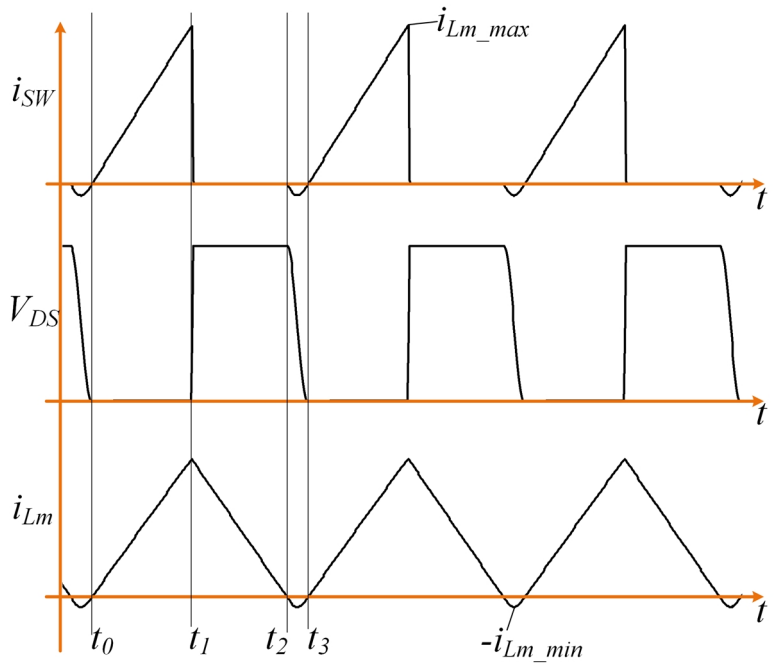


Fig. 7.4 Operation of boost converter under switching-active mode

The detailed operation principles of the switching-active mode is shown in Fig. 7.4. Under this operating mode, the turn-on time of the switch Q is controlled by the limit of the inductor current i_{Lm_max}. Once i_{Lm} reaches the current limit, the switch is turned off and i_{Lm} starts to decrease. Quasi-resonant transition starts when i_{Lm} decreases to zero. At the first valley of the drain-source voltage V_{DS}, the switch is turned on to achieve zero-voltage switching (ZVS). Valley turn-on is ensured by constant turn-off time. If the magnetizing current limit i_{Lm_max} is fixed, both the turn-on time and turn-off time of the switch are constant. The turn-on time is determined by the following equation,

$$t_1 - t_0 = \frac{L_m \cdot i_{Lm\_\max}}{V_g}. \tag{7.1}$$

Ignoring the voltage ripple on the output capacitor, the turn-off time of the switch at steady state can be obtained

$$t_2 - t_1 = \frac{L_m \cdot i_{Lm\_\max}}{u_{ref}}. \tag{7.2}$$

For quasi-resonant operation, the following equation holds true

$$t_3 - t_2 = \pi\sqrt{L_m C_{oss}}, \tag{7.3}$$

where C_{oss} is the output capacitance of the power switch.

The resonant peak current of the inductor is

$$i_{Lm\_\min} = \frac{u_{ref}}{2} \cdot \sqrt{\frac{C_{oss}}{L_m}}. \tag{7.4}$$

The input power under switching-active mode is

$$P_{sw-act} = \frac{\frac{1}{2} \cdot i_{Lm\_\max} \cdot (t_2 - t_0) - \frac{u_{ref}}{\pi} \cdot \sqrt{\frac{C_{oss}}{L_m}} \cdot (t_3 - t_2)}{t_3 - t_0} \cdot V_g. \tag{7.5}$$

To ensure quasi-resonant operation, burst mode control is extended to the whole load range. As shown in Fig. 7.3, the time of switching-active mode is defined as $T_{on\text{-}v}$ and the time of standby mode is defined as $T_{off\text{-}v}$. The duty cycle of control signal S_v is represented as D_v, which is defined as

$$D_v = \frac{T_{on-v}}{T_{on-v} + T_{off-v}} = \frac{T_{on-v}}{T_v}. \tag{7.6}$$

Then the input power of the boost converter is

$$P_{in} = D_v \cdot P_{sw-act}. \tag{7.7}$$

The full power of the designed boost converter is $P_{sw\text{-}act}$ because the full power is achieved by keeping S_v to be 1.

7.2.2 Variation of Burst Frequency

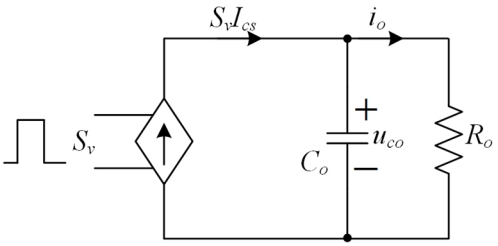


Fig. 7.5 Summarized diagram of the hysteresis controlled boost converter

In order to analyze the boost converter under hysteresis voltage burst mode, the boost converter is summarized to be a logic controlled current source with the output capacitor and load resistor, as shown in Fig. 7.5. i_o is assumed to be constant at steady state. The current source is controlled by S_v and the output of the current source is defined as S_vI_{cs}, where I_{cs} is the average current of i_D over a switching cycle. I_{cs} can be calculated by

$$I_{cs} = \frac{\frac{1}{2} \cdot i_{Lm\_\max} \cdot (t_2 - t_1)}{t_3 - t_0}. \tag{7.8}$$

As indicated by Fig. 7.3 and Fig. 7.4, $T_{on\text{-}v}$ and $T_{off\text{-}v}$ can be determined by

the charging power and discharging power, respectively,

$$\begin{cases} T_{on-v} = \dfrac{C_o(u_{co-\max} - u_{co-\min})u_{ref}}{P_{sw-act} - D_v \cdot P_{sw-act}} \\ T_{off-v} = \dfrac{C_o(u_{co-\max} - u_{co-\min})u_{ref}}{D_v \cdot P_{sw-act}} \end{cases}. \tag{7.9}$$

The burst frequency of the hysteresis controlled boost converter is obtained as

$$f_v = \frac{1}{T_{on-v} + T_{off-v}} = \frac{P_{sw-act}(1 - D_v) \cdot D_v}{C_o u_{ref}(u_{co-\max} - u_{co-\min})}. \tag{7.10}$$

The burst frequency of the operating condition D_v=0.5 is defined as f_v^*. By normalizing the burst frequency to f_v^*, the change of frequency over load can be obtained. As shown in Fig. 7.6, with light or heavy load, the burst frequency could drop to within the audible noise range.

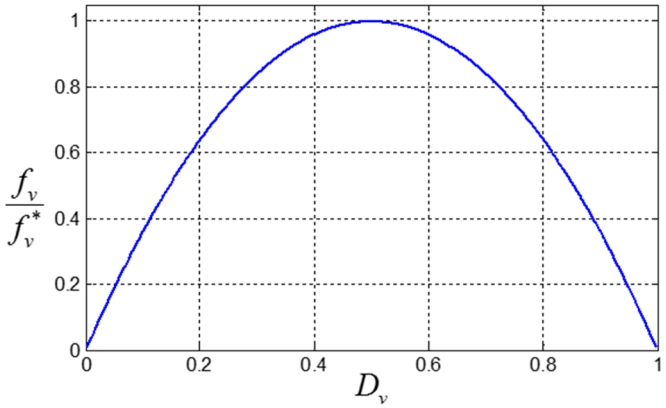


Fig. 7.6 Normalized burst frequency

7.3 Proposed Parabolic Voltage Control

7.3.1 Derivation of Parabolic Voltage Control

In Fig. 7.5, if S_v = 1, the output of the current source is I_{cs}. Here, the converter is under switching-active mode and the following equation holds true:

$$C_o \frac{du_{co}}{dt} = I_{cs} - i_o. \tag{7.11}$$

If S_v = 0, the converter is under standby mode and the output of the current source is zero, then

$$C_o \frac{du_{co}}{dt} = -i_o. \tag{7.12}$$

u_{ref}, u_{co}, δ_v represents the reference of the output voltage, output voltage itself, and voltage tracking error, respectively. The voltage tracking error is defined as

$$\delta_v = u_{co} - u_{ref}. \tag{7.13}$$

By substituting (7.13) to (7.11), the following equation holds true

$$C_o \frac{d\delta_v}{dt} = I_{cs} - i_o - C_o \frac{du_{ref}}{dt}. \tag{7.14}$$

The positive peak of the voltage tracking error is defined as $\delta_{p\text{-}v}$ and the negative peak of the voltage tracking error is $\delta_{n\text{-}v}$. The peak-to-peak value of the voltage tracking error $\delta_{pp\text{-}v}$ is obtained by

$$\delta_{pp-v} = \delta_{p-v} - \delta_{n-v}. \tag{7.15}$$

When $S_v = 1$, $\frac{d\delta_v}{dt}$ is seen as constant and $\frac{d\delta_v}{dt} \cong \frac{\delta_{pp-v}}{T_{on}}$. Similarly, when $S_v = 0$, $\frac{d\delta_v}{dt} \cong -\frac{\delta_{pp-v}}{T_{off}}$. Substitute them to (7.11) and (7.12), with some inspiration from [17],

$$\begin{cases} C_o \frac{\delta_{pp-v}}{T_{on}} = I_{cs} - i_o - C_o \frac{du_{ref}}{dt} \\ -C_o \frac{\delta_{pp-v}}{T_{off}} = -i_o - C_o \frac{du_{ref}}{dt} \end{cases}. \tag{7.16}$$

The peak-to-peak tracking error is obtained as

$$\delta_{pp-v} = \frac{TI_{cs}}{C_o}\left(\frac{T_{on}}{T} - \frac{T_{on}^2}{T}\right) = \frac{TI_{cs}}{C_o}\left(\frac{T_{off}}{T} - \frac{T_{off}^2}{T}\right). \tag{7.17}$$

Assuming the average tracking error of the voltage is zero, the following two equations hold true

$$\delta_{p-v} = -\delta_{n-v} = \frac{\delta_{pp-v}}{2}, \tag{7.18}$$

$$\delta_{p-v} = -\delta_{n-v} = \frac{TI_{cs}}{2C_o}\left(\frac{T_{on}}{T} - \frac{T_{on}^2}{T}\right) = \frac{TI_{cs}}{2C_o}\left(\frac{T_{off}}{T} - \frac{T_{off}^2}{T}\right). \tag{7.19}$$

It can be seen from (7.19), with a constant burst frequency, the value of δ_{p-v} is a parabolic curve. From this point of view, it is possible to achieve constant burst frequency by employing double parabolic carriers as the control band, as shown in Fig. 6.9. The parabolic control carriers with constant burst frequency and zero average tracking error are obtained as

$$\begin{cases} F_{pa-v}(t) = A_{m-v}[\dfrac{t}{T_v^*} - (\dfrac{t}{T_v^*})^2], \quad 0 \le t \le T_v^* \\ -F_{pa-v}(\tau) = -A_{m-v}[\dfrac{\tau}{T_v^*} - (\dfrac{\tau}{T_v^*})^2], \quad 0 \le \tau \le T_v^* \end{cases}, \tag{7.20}$$

where $A_{m-v} = \dfrac{T_v^* I_{cs}}{2C_o}$. As shown in Fig. 6.9, the original hysteresis band $u_{co\text{-}max}$ and $u_{co\text{-}min}$ are replaced by a pair of parabolic carriers. Internal current loop control signal S_v is determined by the comparison between voltage tracking error δ_v and parabolic control carriers. When S_v=1, the internal current loop is enabled and the voltage tracking error δ_v increases until intersecting with the positive parabolic carrier $F_{pa\text{-}v}(t)$. Then, S_v is set to 0 and the internal current loop is disabled. Operation goes into standby mode and δ_v starts to decrease, meanwhile the negative parabolic carrier generation begins. When S_v intersects with the negative parabolic carrier, S_v is set to 1 and the operation switches into switching-active mode, initiating the transition to the next burst cycle.

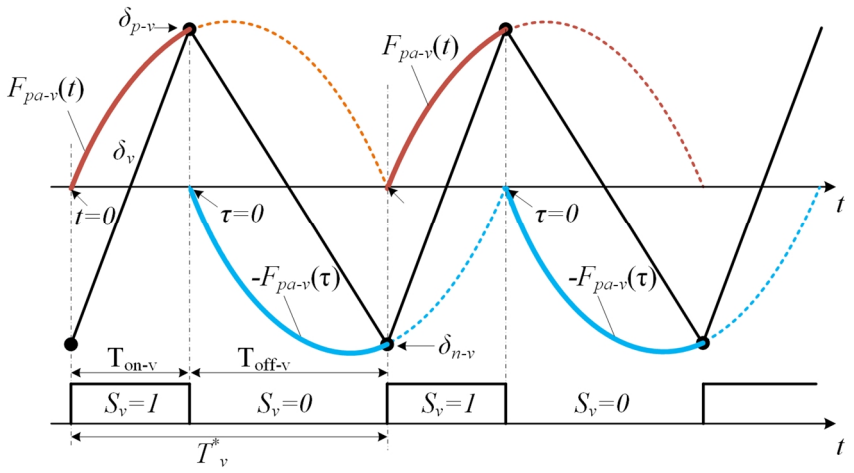


Fig. 7.7 Parabolic voltage control

7.3.2 Comparison with Parabolic Current Control

PCC solves the frequency variation problem of hysteresis current control with fast response and high control precision. To compare PVC and PCC, the simplified diagrams are shown in Fig. 7.8. The diagram of PVC is shown in Fig. 7.8 (a), including a controlled current source, load current source, and a storage capacitor. Fig. 7.8 (b) shows the diagram of PVC, which has a controlled voltage source, voltage source, and an inductor.

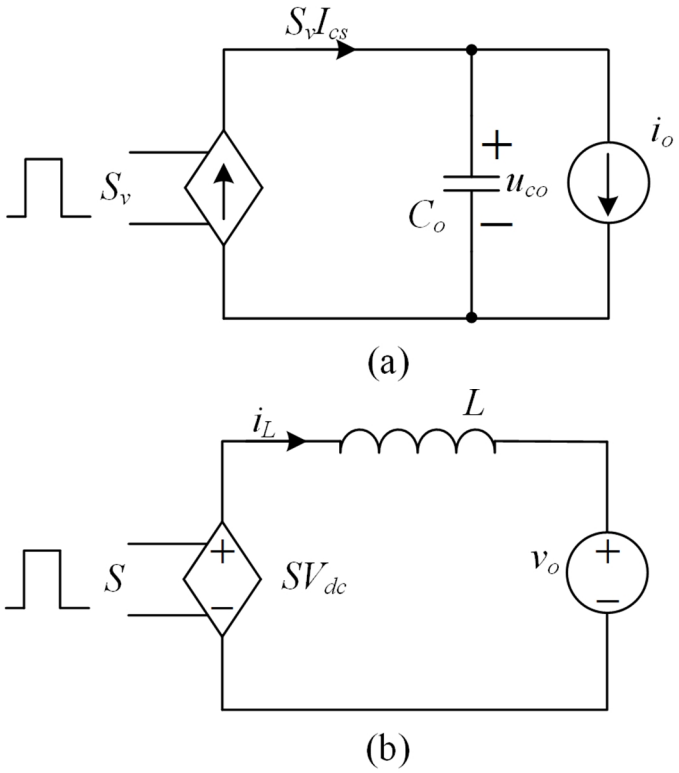


Fig. 7.8 Comparison between PVC and PCC. (a) Simplified diagram of PVC; (b) Simplified diagram of PCC.

By applying the Kirchhoff's current law (KCL) to Fig. 7.8 (a), the following equation can be obtained

$$C_o \frac{du_{co}}{dt} = S_v I_{cs} - i_o. \tag{7.21}$$

By applying the Kirchhoff's voltage law (KVL) Fig. 7.8 (b), the following equation can be obtained

$$L \frac{di_L}{dt} = SV_{dc} - v_o. \tag{7.22}$$

From this point of view, PCC is derived from the constitutive relation of the inductor while PVC is derived from the constitutive relation of the capacitor.

Since the dual of the inductor is capacitor, PVC can be seen as the dual of PCC [104]. Typical duals in electrical circuits are shown in Table 7.1.

Table 7.1 Duals in electrical circuits

Voltage	Current
Parallel	Serial
Resistance	Conductance
Impedance	Admittance
Kirchhoff's Current Law	Kirchhoff's Voltage Law
Thevenin's Theorem	Norton's Theorem
PVC Equivalent Model	PCC Equivalent Model

7.4 Experimental Verification

A PVC controlled boost converter is built and tested, as shown in Fig. 7.9 and Fig. 7.10, with the parameters shown in Table 7.2. As the diagram in Fig. 7.9 shows, to get the voltage tracking error, the output voltage of the boost converter is sensed and subtracted from the voltage reference. Parabolic carriers and the voltage reference are generated by digital-to-analog converters (DACs). To generate the control signal S_v, the PVC controller employs the signals obtained by the comparison between voltage tracking error and parabolic carriers. During the switching-active mode, the switch is turned on after the constant off period and turned off by the peak current control. The constant off period is implemented by the use of a 555 timer circuit. Since the

peak current limit i_{Lm_max} is constant, both the turn-on time and turn-off time are constant, achieving quasi-resonant operation and securing high efficiency over the whole load range.

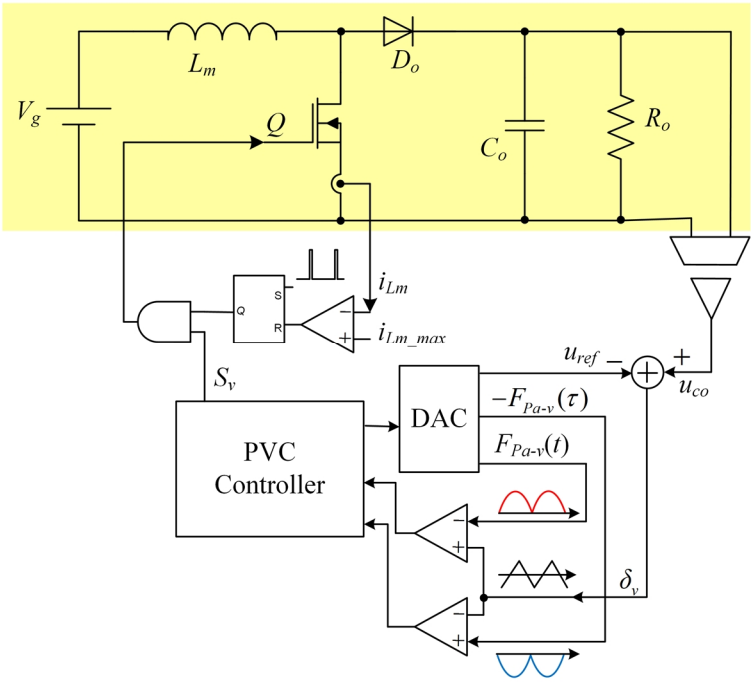


Fig. 7.9 Control diagram

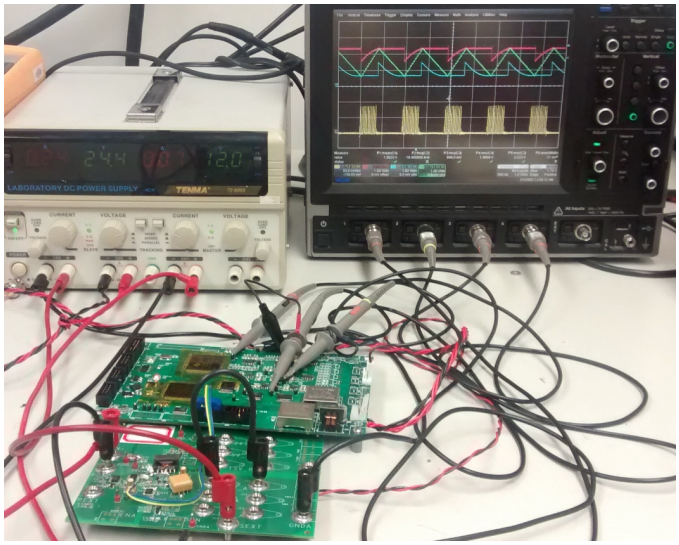


Fig. 7.10 Prototype hardware and test setup

Table 7.2 Prototype hardware parameters

Description	Value
Inductor (L_m)	29 μH
Output capacitor (C_o)	4.7 μF
Rated power	2 W
Input voltage (V_g)	12 V
Output voltage refercen (u_{ref})	24 V
Burst frequency (f_v)	22 kHz
Switching frequency	430 kHz
Parabolic Control Parameter	0.41 V

Experimental results are shown in Fig. 7.11 - Fig. 7.15. Fig. 7.11 shows the current of the switch and the voltage across the drain-source of the switch during switching-active mode. Constant-on and constant-off are achieved and zero-voltage-switching is obtained. Fig. 7.12 shows the output voltage ripple, current going through the switch, i_{sw}, and voltage across drain and source of the switch. Fig. 7.13 shows the steady state of the designed converter with 1.4 W output power. The parabolic control carriers, voltage tracking error δ_v, and switch current i_{sw} are also shown in this figure. As the test results show, constant burst frequency is achieved and output voltage ripple is well controlled. Since the implemented constant burst frequency is not in the audile noise range, audible noise is eliminated. Load change experimental waveforms are shown in Fig. 7.14 and Fig. 7.15, which show fast and stable transition during load change instant. Due to the quasi-resonant operation and the

extension of burst mode to whole load range, the system efficiency is above 96.5% over the whole load range, as shown in Fig. 7.16. This efficiency result is based on the measurement of Fluke 289 multi-meters, and the power consumed by control circuits or gate driving is not included.

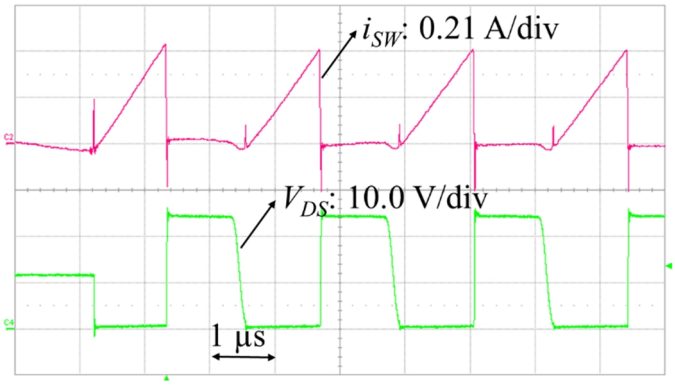


Fig. 7.11 Switch current and drain-source voltage

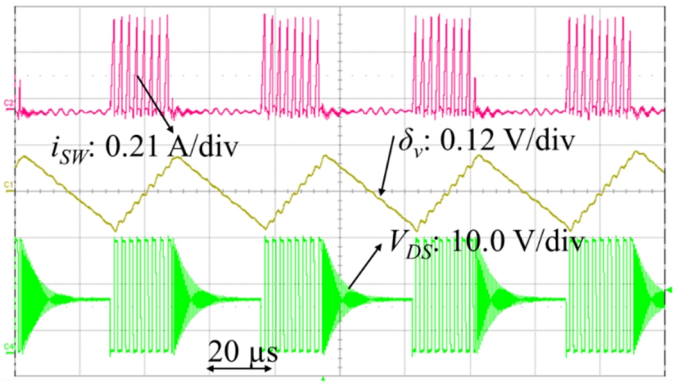


Fig. 7.12 Output voltage ripple, switch current, and drain-source voltage

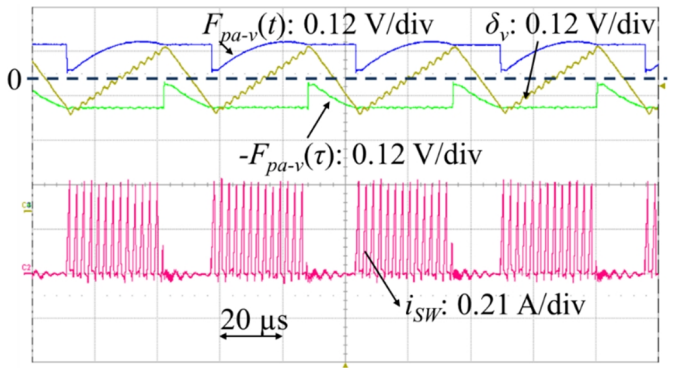


Fig. 7.13 Experimental result with 1.4 W output power

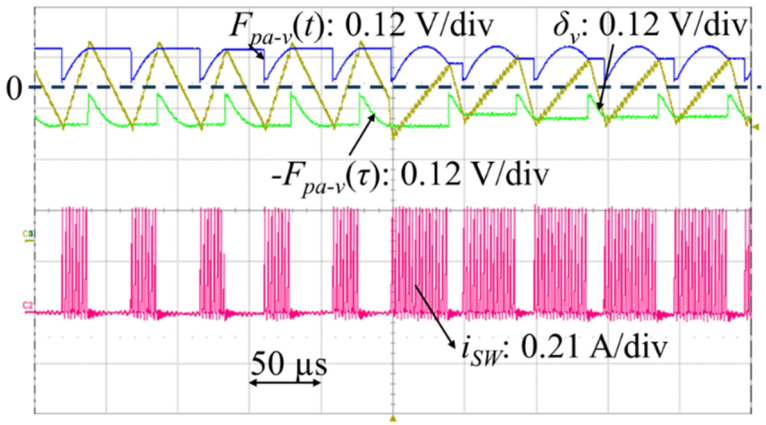


Fig. 7.14 Load change from 0.85 W to 1.64 W

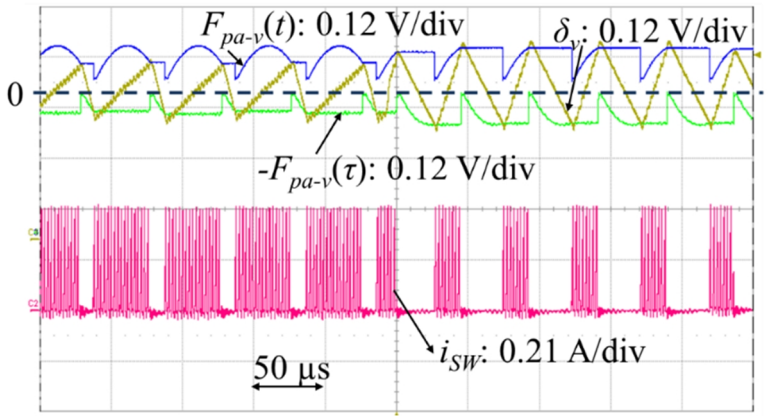


Fig. 7.15 Load change from 1.75 W to 0.85 W

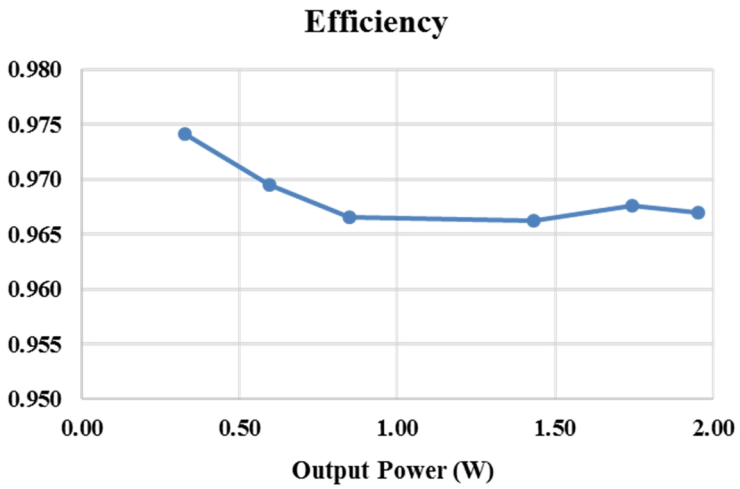


Fig. 7.16 Efficiency test results

To compare the frequency spectrum and voltage ripple of PVC with

traditional hysteresis control, a sinusoidal current load is utilized and the results are shown in Fig. 7.17 - Fig. 7.19. The sinusoidal current source has an amplitude of 33 mA with a dc offset, as indicated by the yellow line in Fig. 7.17 and Fig. 7.18. Fig. 7.17 shows the experimental waveforms under the control of PVC, including output voltage ripple, inductor current, and load current with zoomed-in views. Fig. 7.18 shows the waveforms under hysteresis control, in which a control band with a width of 0.2 V is employed. It is seen that the voltage ripple of PVC changes with load, while the voltage ripple of hysteresis control is controlled constantly within the hysteresis band. The frequency spectrums of inductor current are measured and shown in Fig. 7.19. It is evident that the spectrum of PVC is centralized around the designed point while the spectrum of hysteresis control is decentralized and drops to within the audible noise range.

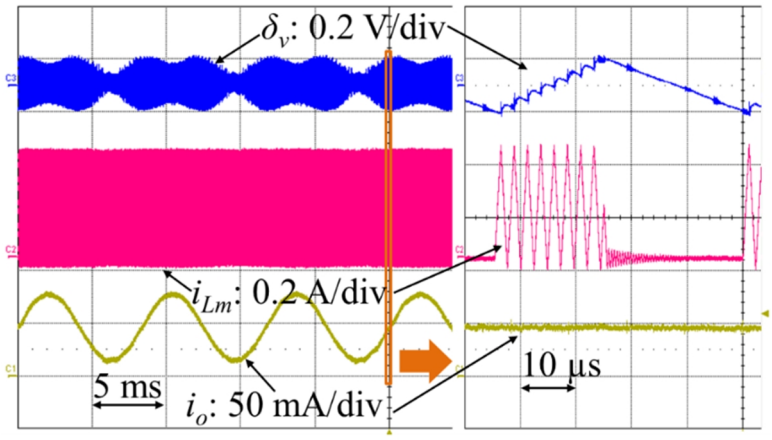


Fig. 7.17 Waveforms of PVC with sinusoidal load current

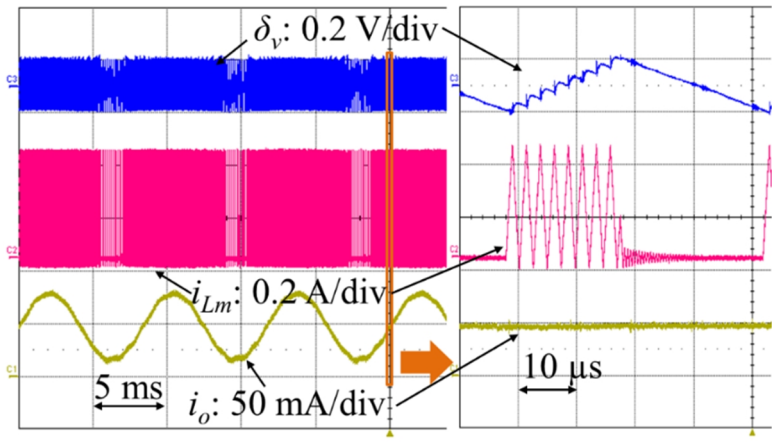


Fig. 7.18 Waveforms of hysteresis control with sinusoidal load current

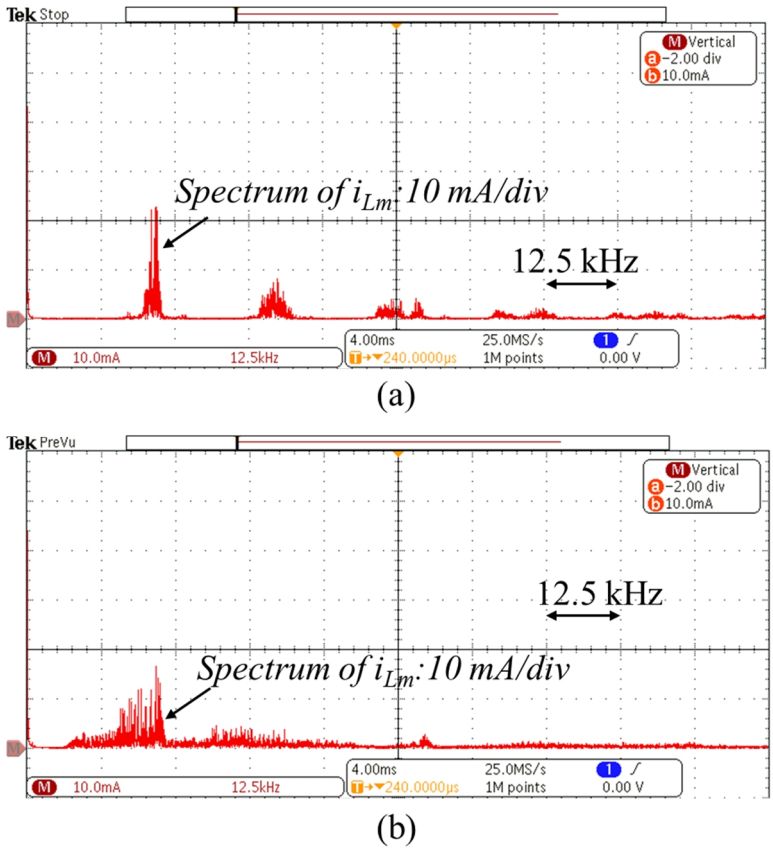


Fig. 7.19 Frequency spectrum of inductor current: (a) with PVC, (b) with hysteresis control.

7.5 Summary

In this chapter, based on the analysis of audible noise and burst frequency

variation problems with burst-mode controlled power converters, a parabolic voltage control method is proposed and experimentally verified. Key features achieved in this chapter include:

1) The burst frequency variation and audible noise problems of conventional burst-mode power converters are studied. Burst frequency change across different loads is analyzed. With a constant hysteresis control band, the burst frequency of power converters could introduce audible noise to the systems when the load is light or heavy.
2) The derivation of parabolic voltage control strategy is conducted based on the simplified circuit of the burst-mode controlled quasi-resonant boost converter. Control parameters of the proposed control strategy are obtained and operating principles are introduced. It is found that constant burst frequency can be implemented and audible noise can be eliminated.
3) By analyzing the derivation of parabolic current control and parabolic voltage control, the simplified circuits for both control strategies are obtained and a comparison between two methods is conducted. The conclusion that parabolic voltage control is the dual of parabolic current control is obtained.
4) Experimental results prove parabolic voltage control can provide stable

and fast control transition. Compared with hysteresis control, the frequency spectrum of parabolic voltage control is centralized, eliminating the audible noise of power converters. In addition, due to the quasi-resonant operation, the boost converter achieves >96.5% efficiency over the whole load range.

Chapter 8 Conclusion

8.1 Conclusions

Nonlinear current control and linear current control are reviewed and discussed in chapter 1. It is seen that parabolic current control is a good candidate for voltage source inverters with fast response and high control precision. However, parabolic current control has some application limitations as stated in the first chapter. This dissertation proposed four improved schemes to solve these issues and one extended duality application: parabolic voltage control.

The derivation of parabolic current control is covered in chapter 2. The summarized diagram of a voltage source inverter is used to derive the inductor current ripple with various duty cycle. It is found out that the inductor current ripple is a parabolic curve with the increase of duty-cycle. Then it is possible to obtain the constant switching frequency by utilizing the derived parabolic curve as the control band. This is the motivation of the invention of parabolic current control.

In chapter 3, the dead-time effects are analyzed and it is concluded that dead-time impacts the current tracking precision and stable duty-cycle range. To compensate the dead-time effects, a compensation strategy is introduced.

The improved carrier is implemented by adding an offset to the original parabolic carrier based on the direction of the output current. With the proposed method, the current tracking precision is improved and the stable duty-cycle range is increased.

In chapter 4, a state machine based method is proposed to implement parabolic current control on dual-carrier PWM strategy. Operation principle of dual-carrier PWM is analyzed. Compared with conventional bipolar PWM, dual-carrier PWM has lower current ripple and reduced core loss. A state machine method is proposed to implement PCC for dual-carrier PWM. With the proposed method, the control signal of parabolic current controller is translated to the required sequence of dual-carrier PWM.

In chapter 5, the traditional implementation methods of PCC are reviewed. It is found that the analog comparison based implementations require high resolution DACs and high bandwidth operational amplifiers, which makes the system complex. Based on the discretization of the inductor current, an inductor current emulation strategy is proposed. This removes the need for the current sensor and its associated circuitry. Thus the system complexity is reduced. The comparison between the parabolic carriers and current tracking error is implemented within the micro-controller, changing the analog comparison to the comparison in control program codes. The noise sensitivity

problem of the analog comparison is solved and system reliability is improved. Furthermore, since the parabolic carriers are generated digitally in a micro-controller, it is more flexible to adjust the magnitude and frequency of the carriers.

In chapter 6, based on the convergence analysis of parabolic current control, a new current control strategy is proposed and named single-step current control. The proposed control strategy achieves fast current response along with single-step convergence speed and constant switching frequency. By shifting the sampling instant ahead and predicting the current at the duty-cycle update instant, effects of calculation and update delay in digital controller are eliminated and the only delay in the control loop is PWM stage. The small signal model of the proposed control strategy is derived and simulation results match well with calculation results. The proposed control strategy is fully compatible with Texas Instruments C2000 series micro-controller and the implementation is easier than traditional parabolic current control.

In chapter 7, motivated by the duality phenomenon in electrical circuits, parabolic voltage control is derived. The new proposed control strategy is utilized by a burst-mode boost converter to eliminate audible noise problems along with high conversion efficiency. Constant burst frequency can be

implemented by the use of parabolic voltage control. Compared with hysteresis control, the frequency spectrum of parabolic voltage control is centralized, eliminating the audible noise of power converters. In addition, due to the quasi-resonant operation, the boost converter achieves >96.5% efficiency over the whole load range.

Hardware prototypes are built in chapter 3 to chapter 7 to verify all the proposed strategies. The performance of the proposed strategy is proven by the experimental results. It can be concluded that the objectives of this dissertation are met and the effectiveness of these five topics are verified.

8.2 Future Work

Meanwhile, some topics in this dissertation need further study:

1. For voltage output converters, the current reference comes from the voltage control loop. Under the condition of load step change, voltage sag still could be noticed. This is not caused by the current response speed. This is instead caused by the slow response of voltage loop. The load step change is reflected first on the current through the output capacitor. Meanwhile the capacitor current and inductor current shares the same current ripple at steady state. So capacitor current can be used as the

feedback of parabolic current control to solve the voltage sag issue under load step change condition.

2. For ultra-high switching frequency (500 kHz to MHz range) converters, even with the proposed senseless control or single-step current control, it is still hard to implement cycle-by-cycle control. Because the system clock limits the maximum switching frequency in sensorless control and calculation time limits the maximum switching frequency in single-step current control. Analog integrated circuit (IC) is a possible solution since this solution can itemize the design to meet the requirement of parabolic current control. Meanwhile, analog comparison is implemented inside the chip with high noise immunity. Since the cost for the design and fabrication of control chip is high, it is better to be supported by the customer or a IC company.

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