CHAPTER 8

CONCLUSIONS

Many of today's commonly used power converters have poor input current factor and rich harmonic current, which deteriorates the power line quality and interfere with other electronic equipment. To limit the input current harmonics, stringent regulations such as IEC 61000-3-2 have been enforced recently. These regulations have prompted many power supply manufacturers to intensify their efforts towards finding cost-effective solutions for complying with the regulations. Among the proposed solutions, the two-stage active PFC techniques seem to be the most popular approaches used by industry. To reduce the added component count and cost from the active PFC stage, the single-stage PFC techniques have been developed for low-power, cost-effective applications.

This dissertation presents the systematic research of the study and improvement of state-of-the-art integrated S^2PFC techniques. It covers the in-depth study of the S^2PFC input-current-shaping mechanism, circuit topology generalization and variation, study of bulk capacitor voltage stress and switch current stress, converter design and optimization, and evaluation of the state-of-the-art S^2PFC techniques with universal-line input. This dissertation also presents new S^2PFC techniques with a voltage-doubler rectifier front end to both significantly improve the performance and reduce the cost of S^2PFC converters for universal-line applications.

The original S^2PFC concept comes from the integration of the DCM boost rectifier and PWM DC/DC converter. To get better performance and smaller EMI filter, it is desirable to achieve CCM S^2PFC techniques. This dissertation research starts from the study of the common PFC condition of the CCM S^2PFC converters, in order to provide a general understanding and

design guideline for the existing CCM S^2PFC techniques. From the general CCM PFC condtion, the generalized two-terminal and three-terminal S^2PFC topologies are developed, with two families of feed-forward PFC cells. The brief comparison and evaluation about the two-terminal vs. three-terminal S^2PFC, the CS vs. VS S^2PFC, and the different two-component S^2PFC cells are also given with novel CCM S^2PFC topologies.

However, the key issues of the S^2PFC technique are not only meeting the IEC harmonics specifications, but also limiting the bulk-capacitor voltage stress and improving the converter efficiency. This dissertation further discovers the circuit parameters' impact on the capacitor voltage and switch current stress of the CCM S^2PFC converters with the support of the simulation and experimental data. As an example, the design considerations and processes of the CCM CS-S^2PFC converter are presented with in-depth design curves. The design consideration of the CCM VS-S^2PFC converter is also discussed. The experimental results prove the design and show the improved performance of the CCM S^2PFC converters over the DCM S^2PFC converter with universal-line input voltage.

After that, in order to show whether S^2PFC technique is a better solution than the conventional two-stage PFC technique, this dissertation further compares and evaluates the CCM two-stage and S^2PFC techniques, with universal-line input. The component values and ratings are given in a number of comparative plots to discover the difference between these two techniques. With universal-line input, it is found that the S^2PFC converter requires higher-rated components, especially the energy-storage capacitor for hold-up time. Besides, the S^2PFC converter suffers high voltage / current stress on the semiconductors and may have a low

efficiency. In conclusion, the penalties of the S^2PFC converter limit its power level for universal-line applications.

To reduce the bulk-capacitor voltage range and the associated penalties in the S^2PFC converters, this dissertation proposes a novel S^2PFC techniques with integrated voltage-doubler rectifier front end for universal-line applications. Based on the generalized feed-forward cell concept derived in Chapter 3, two families of VD S^2PFC circuits have been developed, with either DCM or CCM input inductor current. The comparison among the two-stage PFC, S^2PFC and the VD S^2PFC converters shows significant size reduction and performance improvements. Especially, the hold-up capacitance is reduced by more than 3 times, while the converter efficiency is increased by 8% than that of the existing S^2PFC converters. The experimental results of several different VD S^2PFC converters, from 100 W to 450 W output power, verifies the improved performance. It is concluded that the VD S^2PFC technique is a more cost-effective solution than the two-stage PFC for the IEC class D equipment, with universal-line input and converter input power up to 600 W. Besides, with the proposed VD S^2PFC technique, the existing power supplies with a voltage-doubler rectifier without input current shaping can be easily and quickly modified to meet the input current harmonics regulations with minimum added cost and size. The efficiency comparison shows the VD S^2PFC converter even has higher efficiency than the two-stage PFC converter does.

In addition, to further reduce the size and cost of the passive components and increase the power density of the converter, a novel interleaved DCM S^2PFC technique is proposed. With two interleaved DCM S^2PFC channels, the proposed converter has low input current ripple and small EMI filter. Besides, the DCM boost inductor size is also smaller than the CCM PFC inductor(s).

The comparison between the proposed converter and the VD CCM S^2PFC converter shows the proposed circuit has both smaller EMI filter and boost inductor size than those of the CCM S^2PFC converter. An universal-line input, 5V/90A (450W) - output prototype proves that the proposed interleaved DCM S^2PFC converter has the efficiency very close to the CCM S^2PFC converter. The discussions on the advantages and disadvantages on this proposed technique show that the interleaved DCM S^2PFC technique is an alternative solution to implement high-density, cost-effective converter with input power up to 600 W.

In conclusion, this dissertation provides the in-depth analysis and optimization of various S^2PFC techniques that result in low-harmonic, low-cost and high-efficiency power supply design. The innovative techniques are also developed in order to provide simple, cost-effective and efficient solutions to improve the power quality of power supplies which covers wide range of applications, from power adapters and computers to various communication equipment.

Several topics can be the potential future work of this research. The CCM S^2PFC converters with multi-feed-forward components need to be further studied. The in-depth study on the bulk-capacitor voltage stress is also very necessary, as well as a straightforward design approach of the VS S^2PFC converter. How to further improve the performance and reduce the cost of the CCM S^2PFC converters with universal-line input is also an interesting and important research topic.