Impact of Thermal Effects and Other Material Properties on the Performance and Electro-Thermal Reliability of Resistive Random Access Memory Arrays

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Amrita Chakraborty

(ABSTRACT)

As the semiconductor industry grapples with escalating scaling challenges associated with the floating gate MOSFET, alternative memory technologies like Resistive Random Access Memory (ReRAM) are gaining prominence in the scientific community. Boasting a straightforward device structure, ease of fabrication, and compatibility with CMOS (Complementary Metal-oxide Semiconductor) Back-end of Line (BEOL), ReRAM stands as a leading candidate for the next generation of non-volatile memory (NVM).

ReRAM devices feature nanoionics-based filamentary switching, outperforming flash memory in terms of power consumption, scalability, retention, ON/OFF ratio, and endurance. Furthermore, integrating ReRAMs within the CMOS BEOL/low-k Cu interconnect system not only reduces latency between the connectivity constraints of logic and memory modules but also minimizes the chip footprint.

However, investigations have revealed a significant concern surrounding ReRAMs—specifically, their electro-thermal reliability. This research provides evidence highlighting the critical influence of material properties, deposition effects, and thermal transport on the device's performance and reliability. Various material systems have undergone in this work scrutiny

to comprehend the impact of intrinsic material properties such as thermal conductivity, specific heat capacity, thermal diffusivity, and deposition effects like surface roughness on the electroforming voltages of ReRAM devices.

The reference device structure considered in this work is Cu/TaO_x/Pt, which has been compared with alternative configurations involving metals like Ru and Co as potential substitutes for Pt. Additionally, a new vehicle has been introduced to quantify cell degradation resulting from thermal cross-talk in crossbar Resistive Random Access Memory (ReRAM) arrays.

Furthermore, a novel methodology has been presented to predict cell degradation due to remote heating, taking into account the cell's location, the material properties of the device, and geometry of its electrodes. The experimental results presented in this study showcase filament rupture caused by remote heating, along with spontaneous filament restoration ensuing from the subsequent cooling of the ReRAM cell.

Impact of Thermal Effects and Other Material Properties on the Performance and Electro-Thermal Reliability of Resistive Random Access Memory Arrays

Amrita Chakraborty

(GENERAL AUDIENCE ABSTRACT)

As the demand for compact, high-speed logic-memory modules continues to surge, the diminishing silicon real estate in our gadgets poses a challenge in extending Moore's law to meet the scaling needs of the semiconductor device industry. To tackle this challenge, emerging memory technologies like Resistive Random Access Memory (ReRAM) are positioned as promising successors to flash memory.

ReRAM devices offer distinct advantages over flash memory, showcasing superior power consumption, scalability, long retention, a high ON/OFF ratio, and good endurance. Their compatibility with current CMOS (Complementary Metal-oxide Semiconductor) technology facilitates seamless integration. However, a significant concern associated with ReRAMs is their electro-thermal reliability.

This research delves into how material properties comprising a ReRAM device and fabrication factors, such as the surface roughness of the material, can impact the electrical and thermal reliability of a ReRAM cell. In this context, a novel methodology has been introduced to predict cell degradation within ReRAM crossbar arrays induced by thermal cross-talk, considering material properties and the geometry of the device. The new methodology has been thoroughly verified on manufactured ReRAM arrays with various composite

electrodes. The study also presents experimental results demonstrating the rupture of cell filaments due to remote heating, along with instances of spontaneous filament restoration due to subsequent cooling.

Dedication

To my parents.

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List of Publications

The research work presented in this dissertation has resulted in the following publications:

1. **Amrita Chakraborty**, Payton Fallen, Aaron DiFilippo, and Marius Orlowski. Electrical Characterization of ReRAM Arrays to Observe Thermal Cross-talk. (*Under Preparation*)

2. **Amrita Chakraborty**, Aaron DiFilippo, Sheena Deivasigamani, Calvin Hong, Anshu Madwesh, and Marius Orlowski. Methods to Enhance Electrical Conductivity of PEDOT:PSS-based Electrodes. (*Under Preparation*)

3. **Amrita Chakraborty**, Mohammad S. Al-Mamun, and Marius K. Orlowski. Thermal Reliability Issues in ReRAM Memory Arrays. In Dr. Yao-Feng Chang, editor, *Memristors - the Fourth Fundamental Circuit Element - Theory, Device, and Applications*, Chapter 0. IntechOpen, Rijeka, 2023.

4. **Amrita Chakraborty**, Mohammad Al-Mamun, and Marius Orlowski. Methodology for Mitigation of the Reliability of a Resistive RAM Memory Array Caused by Thermal Cross-Talk Between the Memory Cells. In *Electronic Materials Conference*, Santa Barbara, USA, June 2023. https://doi.org/10.48448/37e1-7q37

5. **Amrita Chakraborty**, Payton Fallen, and Marius Orlowski. Manufacturing of Highly Conductive Organic PEDOT:PSS Films for Electronic Devices. In *Electronic Materials Conference*, Santa Barbara, USA, June 2023. https://doi.org/10.48448/j8bt-sz62

6. Mohammad Al-Mamun, **Amrita Chakraborty**, and Marius Orlowski. Analysis of the Electrical ReRAM Device Degradation Induced by Thermal Cross-Talk. *Advanced Electronic Materials*, 9(4):2201081, 2023.eprint: https://onlinelibrary.wiley.com/doi/pdf/10.1002/aelm.202201081.

7. **Amrita Chakraborty**, Mohammad Al-Mamun, and Marius Orlowski. Inertness and Other Properties of Thin Ruthenium Electrodes in ReRAM Applications. In Dr. Yao-Feng Chang, editor, *Ruthenium - Materials Properties, Device Characterizations, and Advanced Applications*, Chapter 7. IntechOpen, Rijeka, 2023.

8. **Amrita Chakraborty**, Daniel Herrera, Payton Fallen, Daniel Hall, Nicholas Bampton, Thomas Olivero, and Marius Orlowski. Conductive organic electrodes for flexible electronic devices. *Scientific Reports*, 13(1):4125, March 2023. Number: 1 Publisher: Nature Publishing Group

9. **Amrita Chakraborty**, Mohammad Al-Mamun, and Marius Orlowski. Impact of Surface Roughness and Material Properties of Inert Electrodes on the Threshold Voltages and Their Distributions of ReRAM Memory Cells. *ECS Journal of Solid State Science and Technology*, 11(10):104007, October 2022. Publisher: IOP Publishing.

10. Mohammad Al-Mamun, **Amrita Chakraborty**, Yanlong Li, and Marius K. Orlowski. (Invited) Impact of Surface Roughness of the Electrodes on the Resistive Switching in ReRam Devices. *ECS Transactions*, 97(1):133, April 2020. Publisher: IOP Publishing.

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Chapter 1

Introduction

Humankind has always been fascinated by history and its restoration. The idea and the desire to conserve our knowledge and information in different mediums and pass it on to future generations has been of particular interest and importance to us. Memory and through extension memory devices in their current state have now become the medium that enables us to store and spread that knowledge and information. Starting from the Mesopotamian era writing systems to modern-day gadgets, we have come a long way through the evolution of storage systems and it has become one of the most remarkable, if not the most remarkable, achievements of human history. We see evidence of the first form of writing systems used for record-keeping dating as early as 3200 BC known as the "cuneiform" script developed by the Sumerians.[1, 2] This paved the way for a more pictorial writing system, the Egyptian Hieroglyphs, in the later part of the fourth millennium [1]. The word "Hieroglyphs" originates from the Greek word Hiero(meaning holy) and glypho(meaning writing) which essentially translates to "the God's word"[1]. As the human civilization evolved, current state-of-the-art storage mediums have come a long way from cuneiforms, hieroglyphs, bone carvings, bronze inscriptions, to Latin and other language alphabet systems, to the digital world. The modern world has seen its own evolution of storage mediums through vacuum tubes storing electrostatic charges, punch cards, magnetic tape, Hard Disk Drives, floppy disks, Compact discs (CD), Digital Versatile Disc (DVD), and Solid State Drives (SSD) etc, [3, 4].

Modern-day semiconductor memory technology has made "portable electronics" a reality.

The evolution of innovative technologies like Artificial Intelligence (AI), the Internet of Things (IOT), and autonomous vehicles on the semiconductor technology platform have garnered unparalleled attention. With the advent and popularity of modern semiconductor technology, there has been a burgeoning demand for data storage and with that, an increased necessity for higher packing density of memory devices in the technology. Over the past 30 years semiconductor device scaling has led to the shrinkage of device feature size from 1 μm to about 14 nm (channel length/half pitch) in accordance with the Moore's law but the industry now sees an obstruction to its scaling trends as we push the limits of Moore's law.

1.1 Scaling Issues in Semiconductor Memory Technology

The most significant issue currently plaguing the semiconductor industry is device scaling. The needs of applications like high-performance computing, mobile computing, and autonomous sensing are pushing the physical boundaries of device scaling. The scaling factor for a feature size is 0.7 every 2 years which can yield a device footprint factor of 0.5 [5, 6]. As the feature size goes smaller and smaller, it allows for more transistors to be installed in the same chip size. Figure 1.1 (a) shows the technological trend of device feature size scaling over the course of 60 years. Figure 1.1 (b) also shows how with the changing trends and device scale, Intel devices adapted to produce different device generations [6].

Non-volatile flash memory is the industry-standard prevalent memory technology [7]. Invented back in the 1980s, the flash memory is a MOSFET with a floating gate. Under the influence of a large applied voltage to the gate control (non-floating), the electrons undergo Fowler-Nordheim tunneling and are injected into the floating gate. These electrons remain

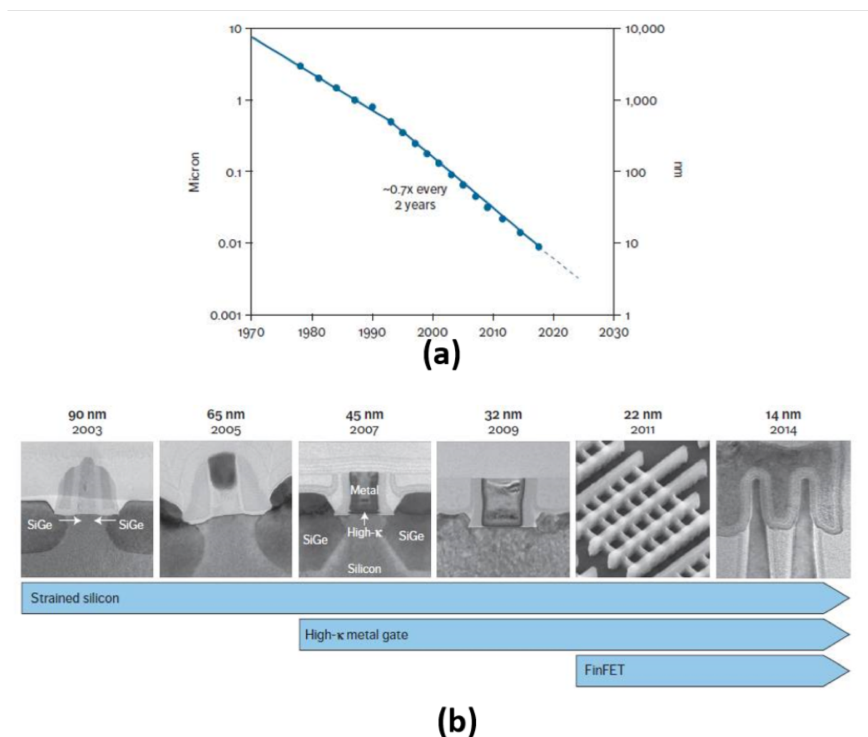


Figure 1.1: (a)Intel scaling trends of device feature size from 1970-2030; (b) Generations of Intel devices with shrinking feature size. Reprinted with permission from [6] ©2017 IEEE

at the floating gate even after the removal of the gate voltage. This happens because the floating gate surrounded by an insulator does not leave any path for leakage. Only when a voltage of opposite polarity is applied these charges accumulated at the floating gate can be erased. Thus the states "0" and "1" are defined by the presence and absence of charges at the floating gate. Inspite of the success of flash memory, they suffer from slow write-time and require high write voltage to keep up with the current needs of applications.

In addition to device scaling issues, and slow writing speeds, the current industry-standard CMOS architecture is such that the memory and the logic are in two different spots on the chip as per the Von Neumann architecture. This requires extended interconnect lines between the memory and the chip thus making the chip footprint larger and longer time delays [8]. Figure 1.2 illustrates how crucial interconnect delay can be in the case of device

feature scaling. For an industry that thrives on higher processing speeds and larger data storage ability, this scaling issue is of the greatest concern.

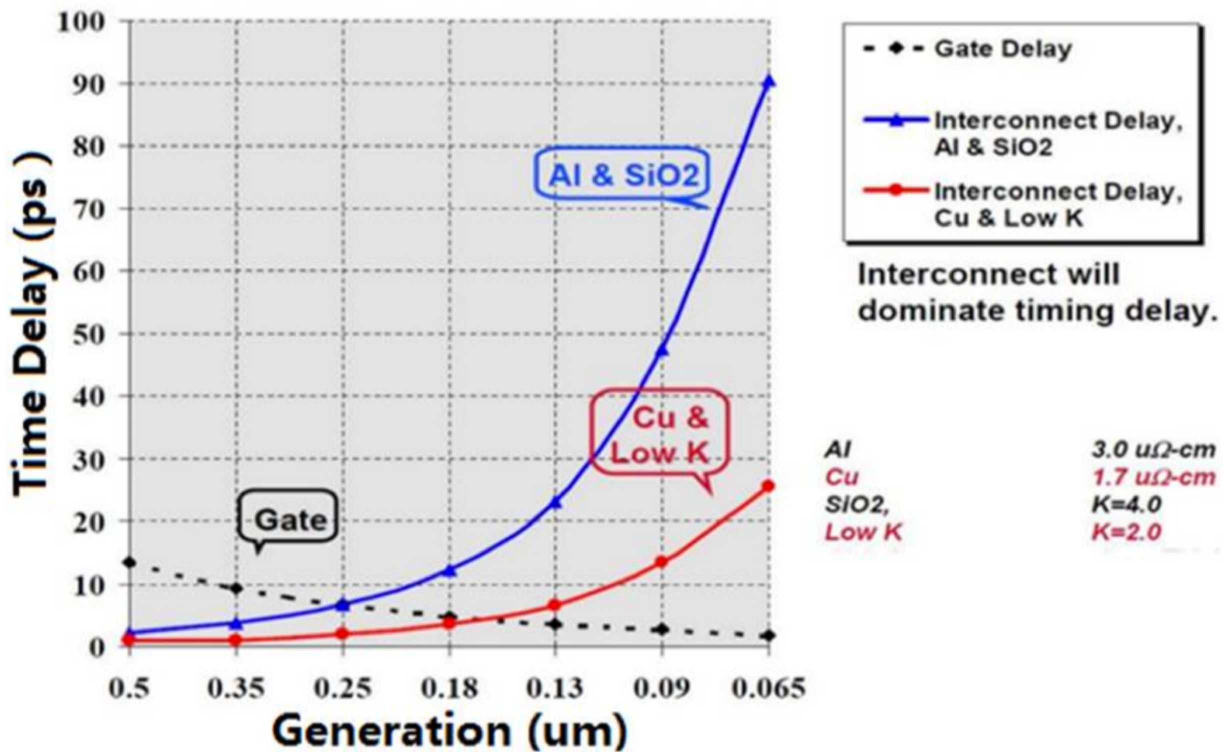


Figure 1.2: Delay as a function of feature size. Reprinted with permission from [8] ©1997 IEEE

1.2 Scope for Resistive Memory

With the above-mentioned scaling needs and issues in the foreground, there is a large scope for novel and revolutionary memory technologies that can adapt to and are compatible with the existing technology while mitigating the scaling issues.

1.2.1 Emerging Memory Technologies

Multiple new memory technologies have emerged and gained attention over the past two decades. Memory technologies like conductive bridge resistive memory (CBRAM), ferroelectric memory (FeRAM), metal-oxide resistive memory, phase change memory (PCM), nanoelectromechanical system (NEMS) memory, and spin-transfer torque magnetic memory (STTRAM) are being thoroughly researched as worthy contenders for novel technology. Memory like the PCM uses heat to cause a material phase change from amorphous to crystalline and vice-versa [9] which subsequently changes the device resistance. FeRAM as the name suggests, exploits the ferroelectric phenomenon for its memory operation [10]. The NEMS memory can be thought of as the miniature of the MEMS principle of operation where mechanical movements of nano-sized switches induce the memory switching process [11]. STTRAM on the other hand uses a completely different phenomenon of electron spins [12], while the CBRAM uses ionic redox reaction to change the resistive state of the memory. Out of all these novel technologies CBRAM and the STTRAM are found to be the most compatible with the current CMOS technology as these memories are thin film based and can be stacked into a 3-D crossbar structure thus increasing the packing density. Table 1.1 compares all of these memories as summarized in [5].

1.2.2 The Memristor

Leon Chua in 1971 proposed a fourth fundamental circuit element in addition to the resistor, capacitor, and inductor. This fourth element he named as the "memristor" (a portmanteau of the words memory and resistor) [13]. This new element relates the magnetic flux ϕ to charge q by a function M(q) known as the memristance (in accordance with the other 3 elements: resistance, capacitance, and inductance). Strukov et al. in 2008 [14] demonstrated that a

Parameter	Flash Memory	PCM	STTRAM	Resistive Memory	FeRAM	NEMS Memory
Scalability	moderate	good	moderate	good	moderate	poor
MLC	good	good	poor	good	poor	poor
Endurance	good	moderate	good	good	good	poor
3D Integration	moderate	good	moderate	moderate	poor	poor
Fabrication cost	good	good	moderate	moderate	moderate	poor
Write Energy	moderate	poor	moderate	moderate	good	moderate
Write Voltage	poor	good	good	good	good	good

Table 1.1: Comparison of flash memory with emerging memory technologies according to the ITRS roadmap.[5]

Pt/TiO_2/Pt device is a memristive device. This was later confirmed by Chua in [15] where he mentions that all resistive switching devices are memristive.

The mathematical equation governing the I-V characteristic of a memristor is given by:

$$V = R(w).I \tag{1.1}$$

$$\frac{dw}{dt} = I \tag{1.2}$$

where w is defined as the state variable of the device and R is its general resistance. As expected, the history of the biases applied to the device and the current state of the device determines the future state. Thus, the inputs and outputs are related to each other in a

distinctive way, unlike other circuit elements. This can be described by the generic equations:

$$V = R(w, I).I \tag{1.3}$$

$$\frac{dw}{dt} = f(w, I) \tag{1.4}$$

where w is again a set of state variables and R and f are functions of time.

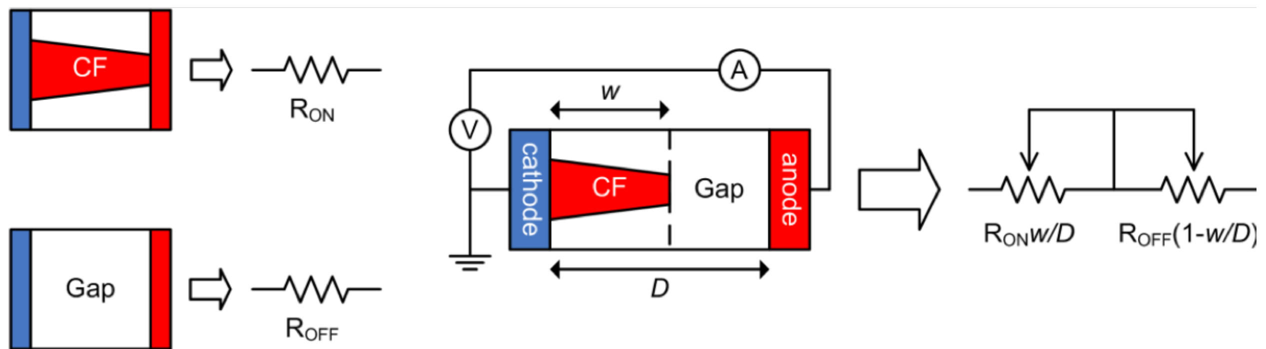


Figure 1.3: Equivalent circuit of the variable-resistor model for a memristor ©2008, Springer Nature Limited (Strukov, D., Snider, G., Stewart, D. et al. “The missing memristor found”. Nature 453, 80–83 (2008). https://doi.org/10.1038/nature06932)

Therefore, a resitive switching memory like a CBRAM can be visualized like a series connection of a high resistance and a low resistance element as seen in Figure 1.3 [14]. As the applied voltage varies, the boundary between the two resistances modulates. The physical equivalent of this changing boundary is the ionic migration under a high electric field within the solid electrolyte. This process of ionic migration will be discussed further in detail in the next sections. Thus, the memristance M(q) is given as:

$$M(q) = R_{off}\left(1 - \frac{\mu_V R_{on}}{D^2} q(t)\right) \tag{1.5}$$

where, R_{off} and R_{on} are the resistance of the two states (low and high) of the memristor, D is the electrolyte thickness, w is the thickness of the low resistive area of the electrolyte, μ_V is

the average ion mobility, and q is the electronic charge. The memristor finds its application as a nonvolatile memory because of its retention capability to store the memory states and data even when not connected to the power.

1.3 Resistive Random Access Memory (ReRAM)

In the past decade, resistive random access memory (ReRAM) has garnered substantial interest. A ReRAM finds its footing in the memory device community because of its non-volatility, low-power operation, better scalability, the scope for high-density architecture, simple device structure, fabrication ease, small footprint, and foremost its compatibility with CMOS technology [16, 17, 18, 19, 20, 21]. A ReRAM possesses many of the properties desired in an ideal memory technology.

1.3.1 ReRAM Device Structure

The ReRAM device is a two-terminal device consisting of a top electrode (also known as the active electrode), the bottom electrode (also known as the inert electrode), and the middle solid electrolyte layer which is the switching layer. Thus, a ReRAM device is essentially a Metal-Insulator-Metal (MIM) structure. Over the years researchers have investigated various materials as candidates for these metal and electrolyte layers. Figure 1.4 shows a basic MIM structure of a ReRAM cell.

Choice of Materials

Some of the common top electrode metals are Cu, Ag, and Ni. These metals are best suitable as active electrode because of their ability to generate metal ions very easily and

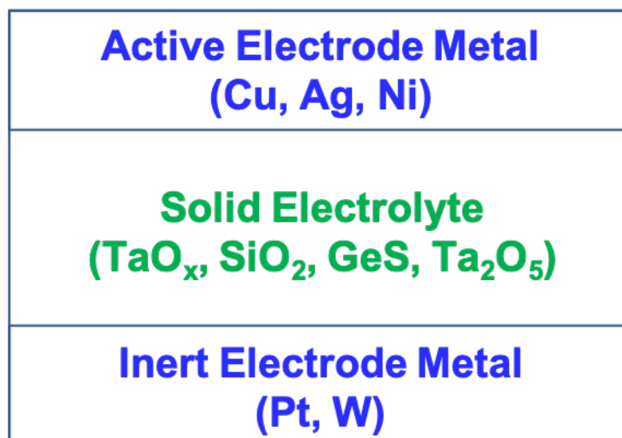


Figure 1.4: A basic MIM structure representing a ReRAM cell.

drift through the solid electrolyte for the switching mechanism. As elaborated by Lübben et. al in [22], and shown in Figure 1.5, the Gibbs free energy can be attributed to being a deciding factor when choosing the top active electrode for resistive switching. Lübben et. al show that based on the Gibbs free energy of the formation of different metal/metal cation couples, one can judge the reversibility of redox reactions. Metals that have their metal/metal-cation pairs with higher positive Gibbs free energy have a tendency to remain reduced with the contrary being true for those with negative energy in which case they tend to be oxidized and are difficult to reduce. Unlike these, Ag and Cu which have a very slight positive energy above the 0 kJ/mol tend to undergo very easily reversible redox reactions suitable for resistive switching. The mechanism of a redox reaction pertaining to ReRAMs has been elaborated in later sections.

A few popular metals used as the bottom inert electrode are Pt, W. The main criterion when selecting a bottom electrode is its ability to stop penetrating metal ions through it. Metals that create a strong diffusion barrier for the contributing metal ions for the nanofilament formation are best suited as the bottom inert electrode.

On the other hand, the solid electrolyte material (typically a metal oxide) should be chosen

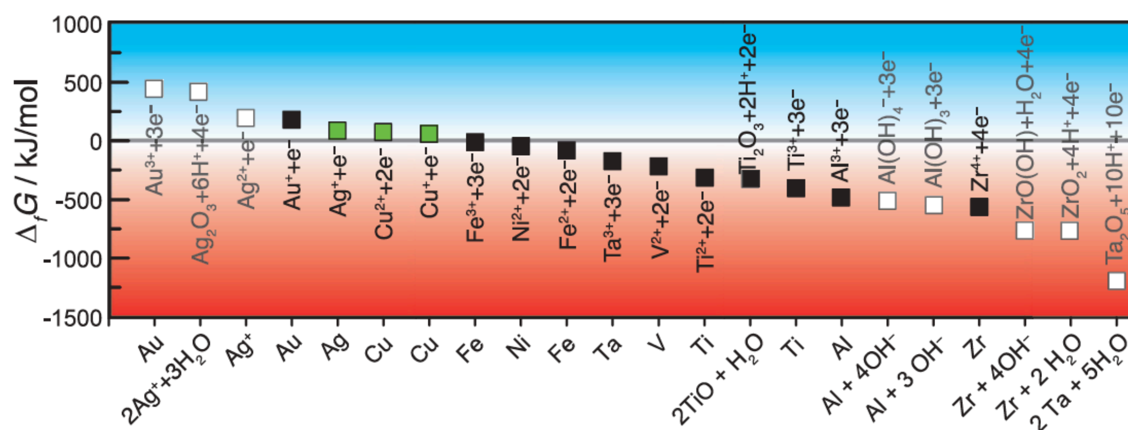


Figure 1.5: Gibbs free energy of formation for various metal/metal cation combinations at pH = 7. Elements of redox pairs with positive Gibbs free energy tend to stay reduced, while metals of pairs with negative energy tend to oxidize but are difficult to be reduced again. Redox couples are marked in gray when another redox couple is energetically more favorable to occur. The best electrode materials identified for ECM switching are slightly above 0 kJ mol_{-1} and therefore the redox reactions are easily reversible (green squares)[22] ©2019 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim reproduced with permission from John Wiley & Sons, Inc. (Lübben M, Valov I. "Active electrode redox reactions and device behavior in ECM type resistive switching memories", Adv. Electron. Mater. 2019;5(9):1800933. DOI: 10.1002/aelm.201800933)

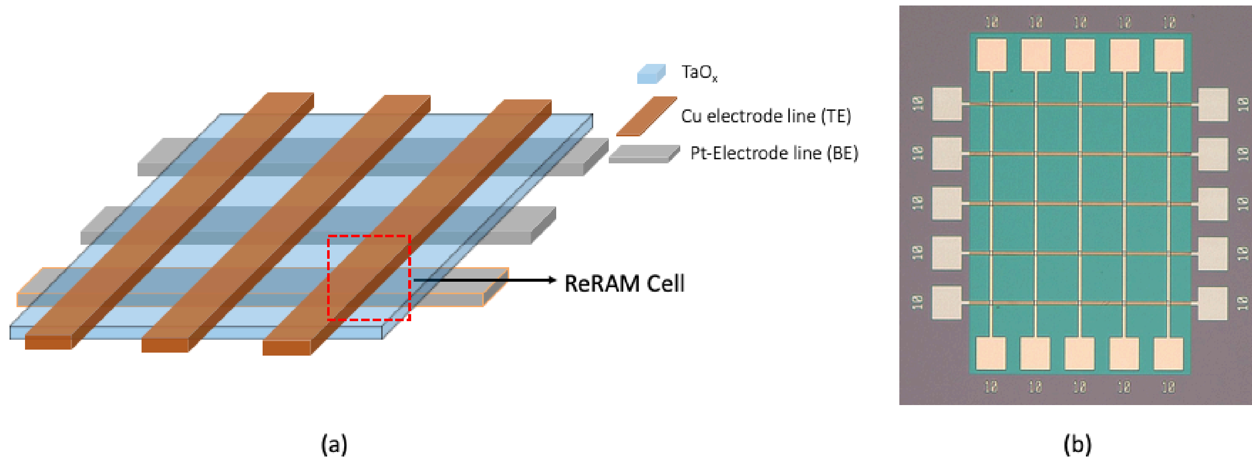


Figure 1.6: (a)Primary ReRAM device schematic for our work; (b) Optical image of a fabricated ReRAM array

such that it allows metal ions to drift through it with high mobility. A few common solid electrolyte materials used are oxides like SiO_2, TaO_x, Ta_2O_5, and chalcogenides such as GeSe, Cu_2S, Ag_2S, etc, [23, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33].

Device Architecture Used in this Work

In this present work, the ReRAM cells are arranged in a crossbar architecture of arrays. To make up the crossbar configuration, the top and bottom electrodes (TE and BE respectively) run perpendicular to each other, with a thin rectangular layer (sheet) of the solid electrolyte running between them. A ReRAM memory cell is situated at the intersection of each TE and BE. The device schematic of a standard ReRAM memory cell array is given in Figure 1.6 (a) and an optical image of a fabricated ReRAM array is shown in Figure 1.6 (b).

1.3.2 Switching Mechanism in ReRAMs

The process of switching in a ReRAM device occurs due to an electrochemical reaction happening at the interface of the top electrode and solid electrolyte under a sweeping bias known as the redox (reduction-oxidation) reaction. When no bias is applied across the electrodes, the oxidation and reduction reactions balance each other resulting in a net zero current. Based on the switching mechanism, ReRAMs can be either of two types:

1. Anion type
2. Cation type

Anion-type Switching in ReRAM

The switching in an anion-type ReRAM occurs because of the movement of negatively charged oxygen ions toward the TE (which is the active electrode) leaving behind a vacancy that eventually creates a vacancy filament after enough ions have migrated. When a negative bias is applied to the top electrode (like Cu) of a ReRAM, the Cu atom goes through a redox reaction at the Cu/electrolyte interface, given by the following equation:

$$Cu \rightarrow Cu^{+} + e^{-} \tag{1.6}$$

Because of the negative bias applied to the TE, the negatively charged electrons drift away from the TE and inject themselves into the solid electrolyte layer (let's consider it to be TaO_x). These electrons in turn can negatively charge the oxygen present in the oxide (solid electrolyte). As these newly formed O^{2-} ions drift towards the positively charged bottom

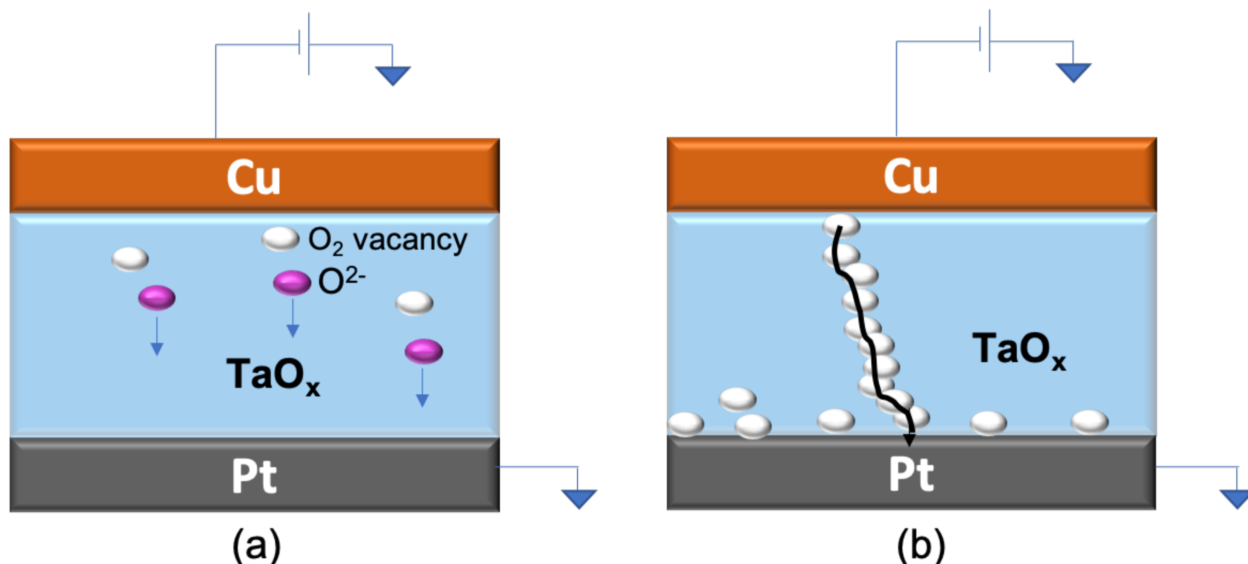
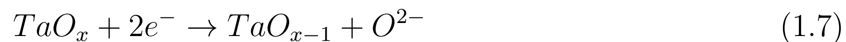


Figure 1.7: Filament formation in an anion-type ReRAM

electrode (BE) under the applied bias, they leave behind a neutrally charged oxygen vacancy.



$$TaO_x + 2e^- \rightarrow TaO_{x-1} + O^{2-} \tag{1.7}$$

This process continues thus creating a conductive vacancy filament hence changing the resistive state. This self-accelerating process ultimately creates a conductive path between the TE and the BE. Figure 1.7 illustrates the formation of a O_2 vacancy filament within a MIM structure.

The formation of a complete filament joining the TE to BE creates a low resistive state (LRS) from an initial high resistive state (HRS). To switch the states from LRS to HRS, an alternate sweeping bias is applied, when the oxygen ions recombine with its vacancy thus rupturing the filament and hence going back to the HRS state. As the device operation is based on ionic migration, it is also known as a nanoionics device [34]. This type of switching mechanism is also observed in WO_x [35, 36], HfO_x [37, 38, 39, 40, 41, 42], TaO_x [43], AlO_x

[44, 45], etc.

Cation-type Switching in ReRAM

In the case of a cation-type switching mechanism, the TE atom undergoes a redox reaction to migrate metal ions toward the BE to form a conductive filament. When positive voltage is applied to the TE, it oxidizes the electrode metal creating metal ions as shown in the following equation:

$$Cu \rightarrow Cu^{+} + e^{-} \tag{1.8}$$

The metal ions generated have high mobility and drift toward the BE through the solid electrolyte due to the applied electric field. At the interface of the electrolyte and the BE, these metal ions cease to penetrate the inert electrode (BE). These ions then get reduced back to metal atoms as given in the equation below:

$$Cu^{+} + e^{-} \rightarrow Cu \tag{1.9}$$

As more and more metal ions continue to accumulate at the BE, they slowly form a conductive filament between joining the TE and the BE. Since this kind of a device creates a conductive bridge between the two electrodes, these ReRAMs are called Conductive Bridge Random Access Memory(CBRAM). The formation of the complete filament changes the resistive state of the device from HRS to LRS. To switch back to the HRS state, a reverse sweeping voltage is applied (negative voltage sweep to TE), which creates triggers Joules heat at the point of highest resistance in the filament. This heat can then rupture the filament bringing the resistive state back to HRS. Figure 1.8 illustrates the switching mechanism in a cation-type device.

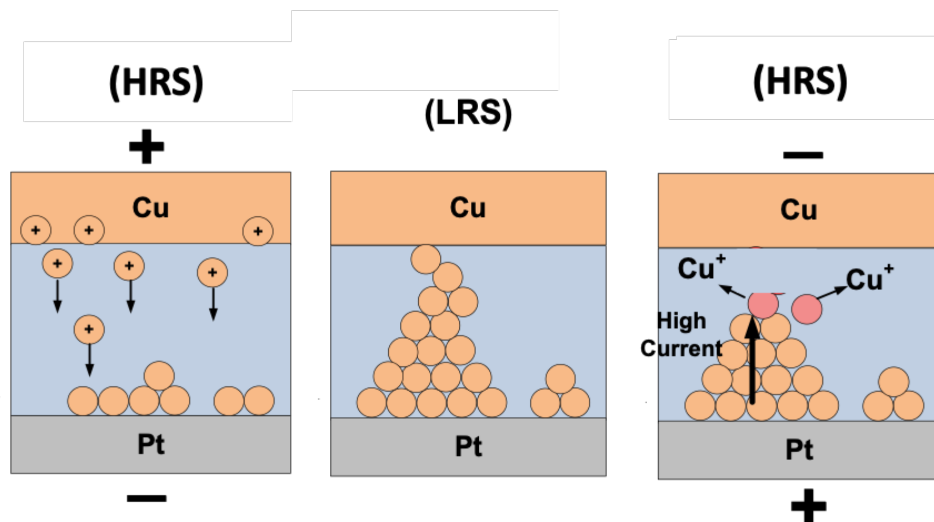


Figure 1.8: Switching in a cation-type ReRAM

The cation-type device is also very compatible with the current CMOS technology and possesses a high R_{off}/R_{on} ratio between the LRS and HRS. Also, besides inorganic electrolytes, organic polymers have been shown to exhibit switching characteristics in cation-type devices for Cu and Ag top electrodes [46] thus opening doors for flexible ReRAMs.

1.3.3 Fundamentals of ReRAM Memory Cell and its Performance Parameters

Now that we have established the basic switching mechanism involved in a ReRAM, we put our focus on the fundamentals and performance parameters. The ReRAM devices discussed in this work are cation-type and the $Cu/TaO_x/Pt$ is our standard reference device.

As established before, depending on the absence or presence of a conduction filament joining the TE and the BE, a ReRAM device is either in the high resistive state (HRS) or the low resistive state (LRS) respectively. When the device is in HRS, it is in OFF state, and can

represent logic '0', while in LRS it is in ON state and can represent logic '1'. The device resistance at LRS is called R_{on} and the resistance at HRS is R_{off}. The R_{off}/R_{on} ratio is one of the most crucial parameters for a ReRAM device's characteristics. The R_{on} can be controlled by a limiting current known as the compliance current (I_{cc}). These parameters are further explained in the next few paragraphs.

The FORM

As we already know the ReRAM is a metal-insulator-metal (M-I-M) structure that has a solid electrolyte layer (TaO_x in our case) in the middle and two electrodes- the top (Cu) and the bottom (Pt)on its two sides. When a high enough electrical stress is applied by an appropriate sweeping bias to the Cu electrode, a redox reaction is initiated at the Cu/TaO_x interface [47]. As a result, Cu^+ ions migrate into the TaO_x layer and start piling up on the Pt electrode where they recombine with electrons to form Cu atoms. Over time enough Cu atoms are accumulated, connecting the Cu and Pt electrodes together through this conducting filament path of Cu atoms [14]. The process when for the first time this filament is created for an untested cell is known as FORMING. The voltage at which the filament just creates the connection between the two electrodes is called the Forming voltage (V_{form}). V_{form} is the highest operating voltage for a ReRAM since the entire filament is built from scratch for the first time and is proportional to the thickness of the TaO_x layer. The TaO_x undergoes a soft breakdown during the FORMING operation.

The RESET

The partial rupturing of the Cu nanofilament connecting the Cu and the Pt electrode is known as RESET operation. RESET is essentially a thermal dissolution process caused by

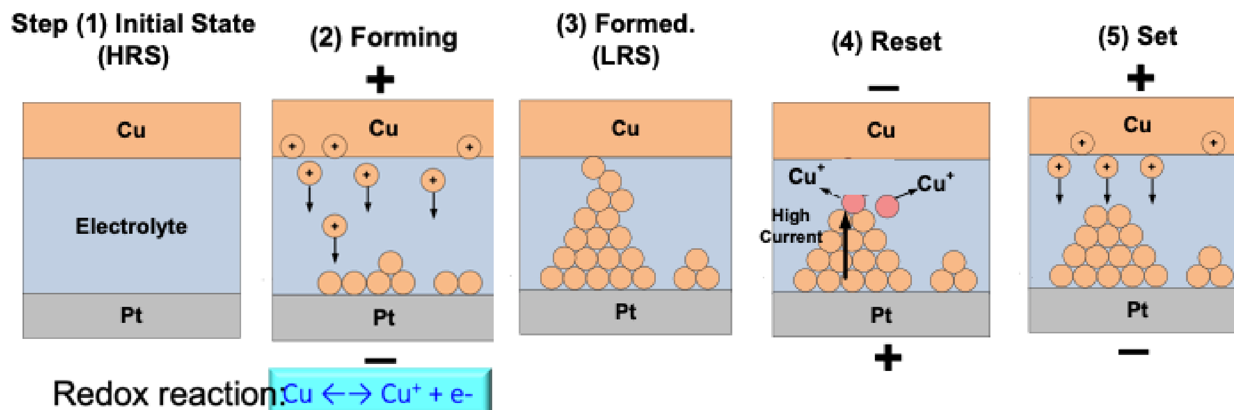


Figure 1.9: ReRAM switching operation

Joule heat. If we assume the shape of a filament to be conical, then the highest resistance of the filament is situated at the most tapered region of the cone. This region is also the region where the maximum Joule heat will be produced. When a negative sweeping bias is applied at the Cu terminal, it generates Joule heat which elevates the temperature of the narrowest filament region. This diffuses out a few atoms at that location and causes a fragment of the filament to rupture. The voltage at which this rupturing occurs is called the RESET voltage V_{reset}.

The SET

The SET operation is the process of restoring the filament back after a rupture to rebuild the connection between the Cu and the Pt electrodes. The voltage at which the filament just restores is called the SET voltage V_{set}. As this is only a partial restoration of the filament, it requires a lesser voltage compared to building the filament for the first time (V_{form}). Thus, $V_{set} < V_{form}$.

Figure 1.9 shows a schematic of the whole switching process of ReRAM operation and Figure 1.10 shows a typical I-V switching characteristics.

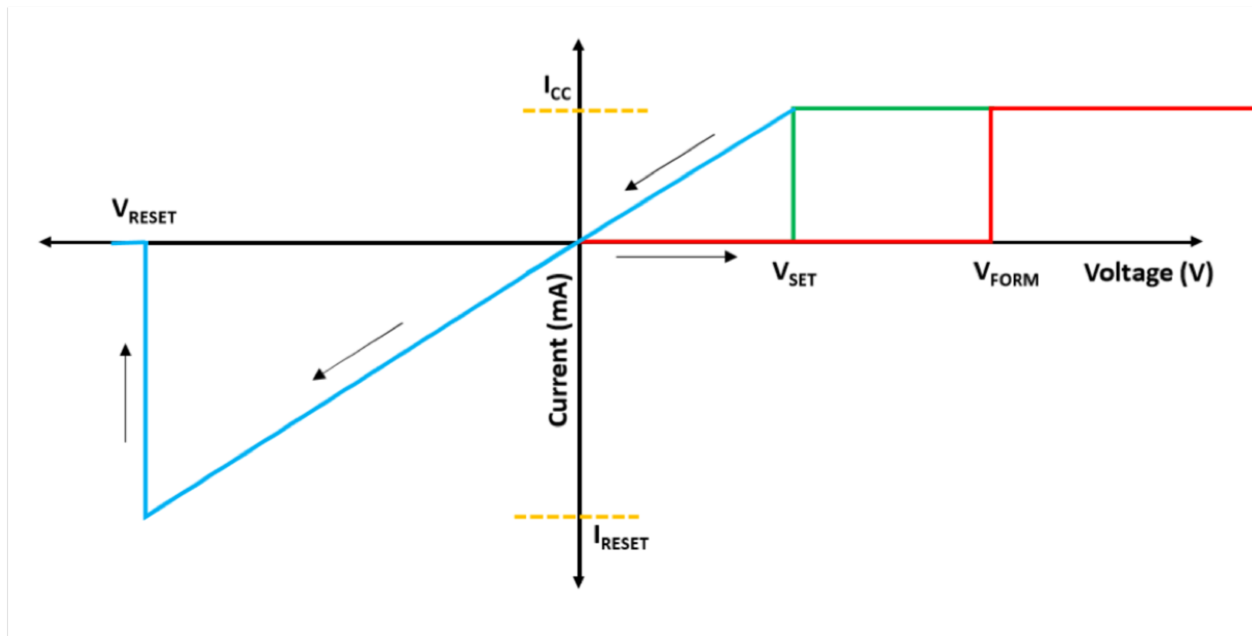


Figure 1.10: IV characteristics of ReRAM switching

The Compliance Current (I_{cc})

This is the user-defined current limit applied to a ReRAM cell during the FORM or SET procedures. This ability to limit the current flowing through the filament lets the user control and operate the device at a low current level. The redox reaction during the RESET process can thus be regulated. ReRAM testing has been performed for a broad range of I_{cc} for our measurements ranging from a few nA to a few mA depending on the requirement of the test. For a constant voltage ramp rate (rr), increasing the I_{cc} lowers the filament resistance. This is because as the I_{cc} increases, the filament becomes broader (grows in the lateral direction) by the accumulation of an increased number of atoms within the filament. On the other hand, as the RESET process is a thermally stimulated process the current during this process is not limited. A typical RESET current can range somewhere between a few mA to about 0.1 A.

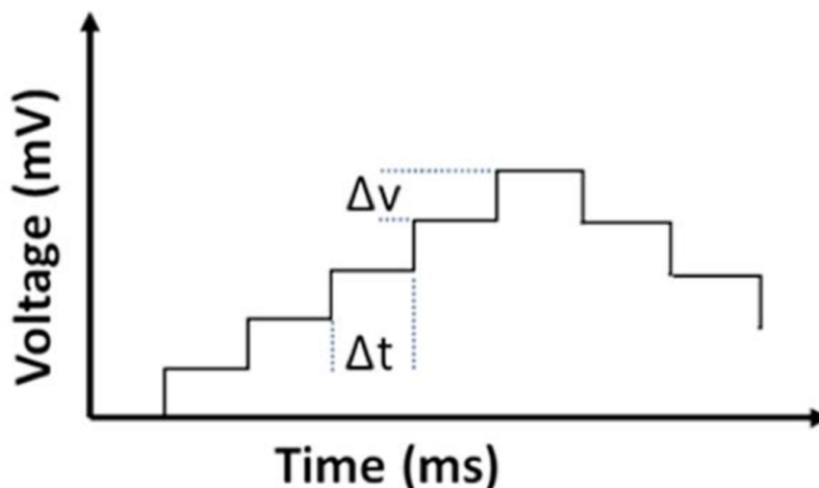


Figure 1.11: Voltage ramp rate

The Ramp Rate

So far it has been mentioned that to operate the ReRAMs we require a sweeping bias to be applied to the TE and the BE is generally grounded. The ramp rate (rr) or the sweep rate (ΔV/Δt) is the rate of application of the DC voltage to the ReRAM cell. For our ReRAM cell characterizations, we use the Keithley 4200A SCS (semiconductor characterization system). It has a ∼50 ms built-in time interval for each step. When a voltage is applied to the ReRAM cell, the user can define the step voltage to control the rr to be applied to the device. Figure 1.11 illustrates a plot to show the sweeping mode voltage. For example, if a user chooses a step voltage of 0.05 V/step, then the corresponding ramp rate at which a voltage is applied to the cell is 1 V/s ($=\frac{0.05V/step}{50\times10^{-3}s/step} = 1V/s$).

The R_{off}/R_{on} Ratio

The device resistance in a ReRAM is independent of the size of the cell, therefore the filamentary switching mechanism is a localized process. As mentioned earlier, the resistance

of a filament after a successful FORMING or SET operation is called the ON resistance (R_{on}). Since the filament connection between TE and BE creates a conductive path, the resistance is low. One of the governing factors of this resistance is the current limit I_{cc} that is thrusted upon the filament during its formation. Whereas, in the case of a successful RESET, the filament breaks partly disrupting the connection between the TE and the BE, and the resistance of the filament increases, called the OFF-state resistance (R_{off}). The R_{off}/R_{on} ratio is thus desirable to be very high ($\sim 10^5$) for a reliable operation of a ReRAM device [48]. A very large R_{off}/R_{on} ratio helps in realizing multiple bits in a single cell and can also increase the density of memory. This ratio requires to be at least $R_{off}/R_{on} > 10$ for a successful distinction between the two memory states [49].

The Retention Time

It is defined as the time duration that a memory cell can keep its memory state unchanged after successful programming. The retention time of a ReRAM cell is one of its many intrinsic characteristics to retain its existing memory content. According to commercial datasheets, commercial memory can retain its state for several years (∼10 years)[50, 51].

The Endurance

The Endurance of a ReRAM cell is defined as the maximum number of times a memory cell can undergo a full switching cycle of SET and RESET. There is a limit to the number of successful switching cycles a cell can perform after which the two memory states become indistinguishable because of electrical fatigue. Every time a cell is switched (SET/RESET), it suffers some permanent degradation to the cell. Over time as the cell undergoes more switching cycles, there comes a critical point after a certain number of cycles beyond which the

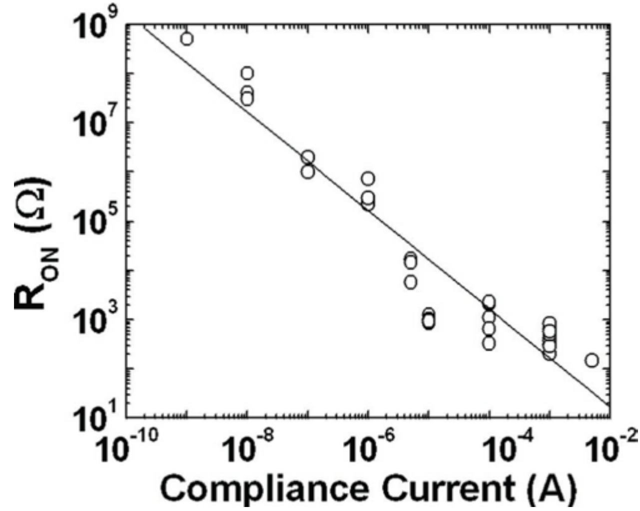


Figure 1.12: Dependence of on-resistance R_{on} on the compliance current I_{cc} for a $Cu/TaO_x/Pt$ device. ©The Japan Society of Applied Physics. Reproduced by permission of IOP Publishing Ltd. All rights reserved (Tong Liu et al. "Physics of the Voltage Constant in Multilevel Switching of Conductive Bridge Resistive Memory", 2013 Jpn. J. Appl. Phys. 52 084202. DOI 10.7567/JJAP.52.084202)

memory states become very much alike. The device is then assumed to reach its endurance limit.

1.3.4 I_{cc}-R_{on} Relation

As mentioned earlier, a high R_{off}/R_{on} ratio helps in multi-bit storage in a ReRAM cell. We also know that one of the most critical parameters to modulate the filament resistance is the I_{cc}. For different I'_{cc}s we can achieve a range of R_{on} and this I_{cc}-R_{on} relationship can be expressed by the equation below:

$$R_{on} = \frac{C}{I_{cc}^n} \tag{1.10}$$

The parameter C is found to be the minimum voltage required to SET a cell, and the fitting parameter n is found to be ≈ 1. Figure 1.12 depicts the I_{cc}-R_{on} relationship for a $Cu/TaO_x/Pt$ device. [52, 53].

1.4 Challenges in ReRAMs and Motivation for this Work

Although ReRAM may seem like the ideal candidate to solve the scaling and processing speed issues of flash memory, it comes with its own set of challenges. One of the main challenges is the integration of ReRAM into the CMOS back-end [54]. The choice of material is one of the biggest challenges in this regard [55]. Take the instance of the inert electrode, the material required to create a diffusion barrier for the active metal ions, should possess low miscibility, have an appropriate glue layer and heat transport layer, and also have a good thermal conductivity. The active metal layer on the other hand should be able to easily undergo the redox reaction to produce metal ions that will contribute to the formation of the conductive nanofilament. It is also required that the active metal does not react with the solid electrolyte switching layer which might hinder the redox reaction. The active metal layer should also have good adhesion to the selected solid electrolyte because adding a glue layer, in this case, is not an option. Lastly, in the case of the solid electrolyte, a dielectric with a moderate level of defects is desirable. In addition to these selection criteria, the chosen materials should also be compatible with the existing CMOS BEOL.

Another astonishing trait of ReRAMs is that two identical devices can have remarkably different switching behaviors on two different substrate layers [54, 55]. Device embedment has a fundamental impact on the intrinsic device performance. During resistive switching of ReRAMs the local temperatures can reach upto 900°C and in some cases even 1200°C have been recorded during RESET operations. This temperature is found to be much greater than the temperature CMOS BEOL is usually exposed to which is $\sim$120°C. At these elevated temperatures, the composition of the bottom electrode gets adversely affected and based on the choice of material, the electrode might loose its crystallinity and hamper the diffusion

barrier it creates for the active metal ions. This phenomenon have been observed in our work and has been discussed in Chapter 3.

Furthermore, as the RESET operation is mainly governed by the production of Joule heat, these elevated temperatures cause a high heat build-up within the cell. The ReRAM cell being arranged in a crossbar architecture has common connections to neighboring cells through common electrode lines. Thus, this heat build-up can escape through these metal conducting lines and affect the state of a neighboring cell (also observed in our experiments). When compared to an industry-standard crossbar architecture, our ReRAM arrays are similar to the vertical dimensions (layer thicknesses) but much wider in terms of planar area (electrode and dielectric layer widths). So one can imagine that the heat accumulation issue within the arrays will be a greater nuisance for in case of the densely packed commercial crossbar arrays.

Owing to the matter discussed above this current work finds its motivation in the investigation of the electro-thermal reliability of ReRAMs. This work tries to find a correlation between material properties, origin of thermal effects and their influences on device performance so that a robust and reliable electro-thermal model can be proposed.

1.5 Organization of this Dissertation

The primary aim of this research is to observe and investigate the origins and effects of heat on ReRAM device performance. Through this work, we try to scrutinize the reliability of ReRAM devices in the light of electro-thermal influences. We also focus on how the material properties of the ReRAM device composition and their alterations due to heating affect the device operation.

Chapter 1, lays the foundation of this work and delves into the motivation behind it. It introduces the Resistive Random Access memory technology and explains the device fundamentals, its operation, critical parameters, and challenges.

Chapter 2 describes the fabrication process of all the devices and samples investigated in this research. A detailed step-by-step processing recipe for the ReRAM devices fabricated at the Micro and Nano-fabrication and Characterization Lab at Virginia Tech is given.

Chapter 3 focuses on how surface roughness of device material, inertness of electrodes, and other material properties affect the performance and operation of a ReRAM cell. This chapter showcases the origins of thermal influence on the electrical performance of a ReRAM device.

Chapter 4 further deepens the understanding of the thermal effects on cell reliability. It introduces the cell-to-cell thermal crosstalk phenomenon observed in ReRAM device arrays. The effect of electrode material properties and electrode dimensions on cell performance and its subsequent effects on neighboring cell operation within an array have been discussed. The chapter also introduces a new parameter to characterize the degradation of a cell. It also proposes a prediction and mitigation methodology for the thermal cross-talk prevalent within ReRAM arrays.

Chapter 5 discusses the current phase of this research and explores the future directions that can be ventured. A novel 3-probe characterization method has been introduced to monitor two cells within the same array simultaneously. This new method enables us to observe how Joule heat generated at a primary cell can conduct through the electrodes and affect a neighboring cell. It is shown that this thermal conduction can adversely affect the state of the neighbor cell to the extent that it induces bit corruption.

Furthermore, this research has also investigated the scope of the use of organic polymers as

ReRAM device electrodes. The motivation for this lies in the work of Kang et.al [46], where it has been shown that organic polymers can be used as a switching layer to replace inorganic solid electrolytes. The appendix section of this dissertation discusses the findings of research performed on organic polymers. The research has successfully fabricated a highly conductive organic polymer and novel conductivity enhancement techniques have been proposed.

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Chapter 2

ReRAM Device Fabrication Process

2.1 Introduction

The fabrication and characterization of the ReRAM devices explored in this work have been performed at the Micro and Nano-Fabrication Lab located in Whittemore Hall, Virginia Tech. In this chapter, we discuss in detail the fabrication process involved in producing the ReRAM devices and additional samples that were created for this work.

The ReRAM devices discussed in this work are essentially Metal-Insulator-Metal (MIM) structures arranged in a crossbar architecture of arrays. Fig 2.1 shows the cross-sectional schematic of the device, indicating the various layers. These ReRAM devices have been processed on a thermally oxidized silicon 4-inch wafer purchased from University Wafer, Inc.

2.2 Materials Used in the ReRAM Device

Various materials have been investigated in literature to be used for the ReRAM MIM structures. In the previous chapter, we mentioned that for resistive switching, the top electrode metal undergoes a redox reaction in order to build the nanofilament. For the top electrode Ag, Cu, and Ni are some of the most common candidates.

There are also various contenders for the solid electrolyte layer such as SiO_2, TaO_x, HfO_2,

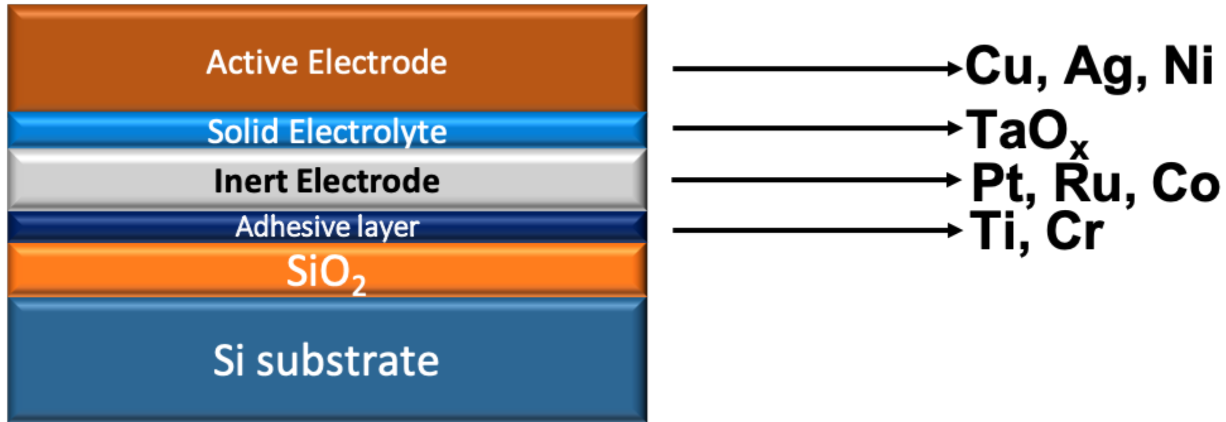


Figure 2.1: Cross-sectional schematic of a ReRAM device indicating different layers and materials used

Figure 2.2: Fabrication process flow of a Cu/TaO_x device

Ta_2O_5, etc. For the bottom inert electrode metals like Pt, Ta, W, etc have been reviewed in various research works.

In this current work, we primarily investigate Cu/TaO_x/Pt structures but also look into other metals like Ru, and Co to see how their material properties compare to that of our chosen materials to make a ReRAM device. As outlined in Chapter 1, we explore these material properties in detail in Chapter 3. In order to do so various metal and solid electrolyte deposition samples were created and were subjected to different testing environments. Thus, in this chapter, in addition to the fabrication process of our ReRAM devices, we also discuss the process of fabrication of these samples.

2.3 Fabrication Procedure of ReRAM Arrays

Fig 2.2 outlines the basic processing steps involved in the fabrication of our ReRAM devices. The major steps involved are:

- Wafer cleaning
- Thermal oxidation
- Photoresist spin-coating and Photolithography
- E-beam Physical Vapor Deposition (EBPVD)
- Lift-off

2.3.1 Wafer Cleaning

Wafer cleaning is the first and one of the most crucial steps of semiconductor processing in any device or sample fabrication. An improper cleaning step can introduce unwanted contamination resulting in degraded device performance, reliability issues, and can even cause complete device failure. Thus it becomes of utmost importance to have control over the particle density and size within the fabrication environment. To ensure a controlled environment of temperature, pressure, humidity, and photosensitivity and to limit or eliminate the presence of dust and other aerosols the fabrication process of our ReRAM devices are majorly conducted in a cleanroom environment. Based on the particulate density (#particles/volume), cleanrooms are designated to different standards (Federal Standard 209E or ISO TC 209). For example, a Class 10 (or ISO 3) cleanroom will have less than 10 particles per cubic foot. The Micro and Nano-fabrication lab where the ReRAM devices where

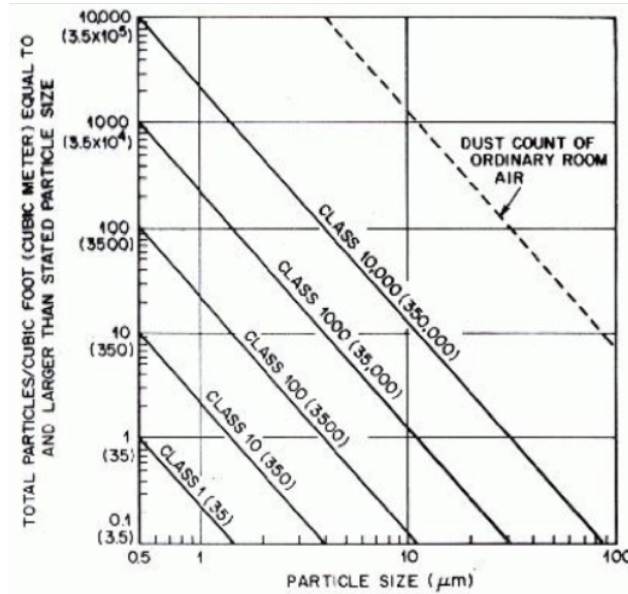


Figure 2.3: Various cleanroom classifications with particle sizes vs. particles/ft$_3$ [1]

fabricated in this work is a Class 1000 ($<$ 1000 particles per cubic foot). Figure 2.3 shows particle size vs. particles per cubic foot for various cleanrooms [1].

The cleaning process can be of two types: a)Dry cleaning, and b)Wet cleaning. In the case of dry cleaning, a chemical reaction occurs between a gas phase and the contaminants on the wafer. This reaction creates volatile compounds, thus cleaning the wafer surface. However, in this work, we have employed the wet cleaning process. In the case of wet cleaning solvents/acids/base solutions are used resulting in chemical reactions with the contaminants which produce soluble compounds. The most standardized cleaning procedure used in semiconductor processing was introduced by Werner Kern in 1965 [2] while working in the Radio Corporation of America (RCA) labs. These cleaning procedures known as RCA cleaning involve two processes: RCA 1 and RCA 2. The RCA 1 process is used to clean organic contaminants from the wafer whereas RCA 2 is used to clean off ionic compounds. A standard RCA 1 and 2 cleaning process is given below.

RCA 1 clean[3]:

1. Mix Ammonium hydroxide and De-ionized (DI) water (NH_4OH : DI water = 1 : 5).
2. The above solution is heated to the boiling point (∼70°C).
3. Add 1 part of Hydrogen peroxide H_2O_2 into the as-prepared solution.
4. Soak the wafer in the above solution bath for 10-15 minutes and subsequently rinse with DI water and dry with N_2.

RCA 1 clean creates a native oxide layer on Si which should be removed using BOE (Buffered Oxide etch) which is essentially a buffered hydrofluoric acid (BHF) solution.

RCA 2 clean [3]:

1. Mix Hydrochloric acid (HCl) with DI water (HCl : DI water = 1 : 6).
2. Heat the solution to its boiling point. (∼70°C)
3. Add 1 part of Hydrogen peroxide H_2O_2 into the as-prepared solution.
4. Soak the wafer in the above solution bath for 10-15 minutes and subsequently rinse with DI water and dry with N_2.

The cleaning procedure implemented in this work has been illustrated below:

1. Blow dry wafer with N_2
2. Soak wafer in acetone bath and ultrasonicate (∼ 10 minutes)
3. Soak wafer in IPA bath and ultrasonicate (∼ 10 minutes)
4. Rinse wafer using DI water
5. Blow dry wafer with N_2

Figure 2.4: a) Wet bench fume hood; b) Ultrasonicator

6. Soak wafer in aqua regia
7. Rinse wafer using DI water
8. Soak wafer in buffered hydrofluoric acid (BHF) (∼2 minutes)
9. Blow dry wafer with N_2
10. Place on a hot plate for dehydration bake (10 minutes 115°C)

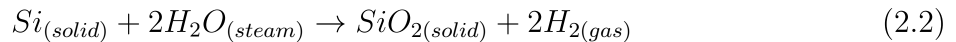
The wafers are first blow-dried with N_2 to remove any dust or non-sticky particulate matter on the wafer. Subsequently, wet organic solvents like acetone and isopropyl alcohol (IPA) are used to get rid of any surface oils and moisture. The silicon surface is hydrophobic in nature, so a good test to make sure the wafer is clean and devoid of any native oxide at the end of the cleaning process is to check the wettability of the wafer surface. A few drops of DI water on the wafer surface after cleaning can determine if there is any residual native oxide. Figure 2.4 shows the wet bench fume hood and the ultrasonicator used to perform the cleaning steps.

2.3.2 Thermal Oxidation

After cleaning, the next step in our device fabrication process is to create a layer of silicon dioxide (SiO_2) on the silicon surface. Using the process of thermal oxidation one can achieve a very pristine homogeneous thin layer of SiO_2 with very low defect density. The ease of oxidizing silicon is one of the major advantages of Si-based technology. This process is not essentially a deposition process but yields similar or even better results [4]. Through this method, one can achieve a high-quality oxide layer of thicknesses ranging from a few nanometers to about 2-3 μm. These oxide layers are used as isolation layers between the Si and the device region.

Thermal oxidation is a high-temperature process where the method is usually carried out at temperature ranges of 900-1200°C [4]. The process comprises of two kinds of oxidation: dry and wet. The chemical reactions involved in these two processes are given below:

$$Si_{(solid)} + O_{2(gas)} \rightarrow SiO_2, \tag{2.1}$$



$$Si_{(solid)} + 2H_2O_{(steam)} \rightarrow SiO_{2(solid)} + 2H_{2(gas)} \tag{2.2}$$

In the above equations, the solid Si is the silicon wafer surface. O_2 is supplied as a gas source for the dry oxidation step and H_2O is supplied in the form of steam for the wet process. The density of the oxide created in the wet process is low in comparison to the dry process but the oxidation rate of the wet process is higher. As mentioned before, the oxidation process is not a typical deposition method rather in this case the participating substrate (Si wafer) gets consumed during the process of oxide growth. Interestingly oxidation of Si occurs at room temperature as well, but the rate is extremely slow. A few tens of angstroms of native oxide that grow at room temperature can be easily etched away using BHF as mentioned

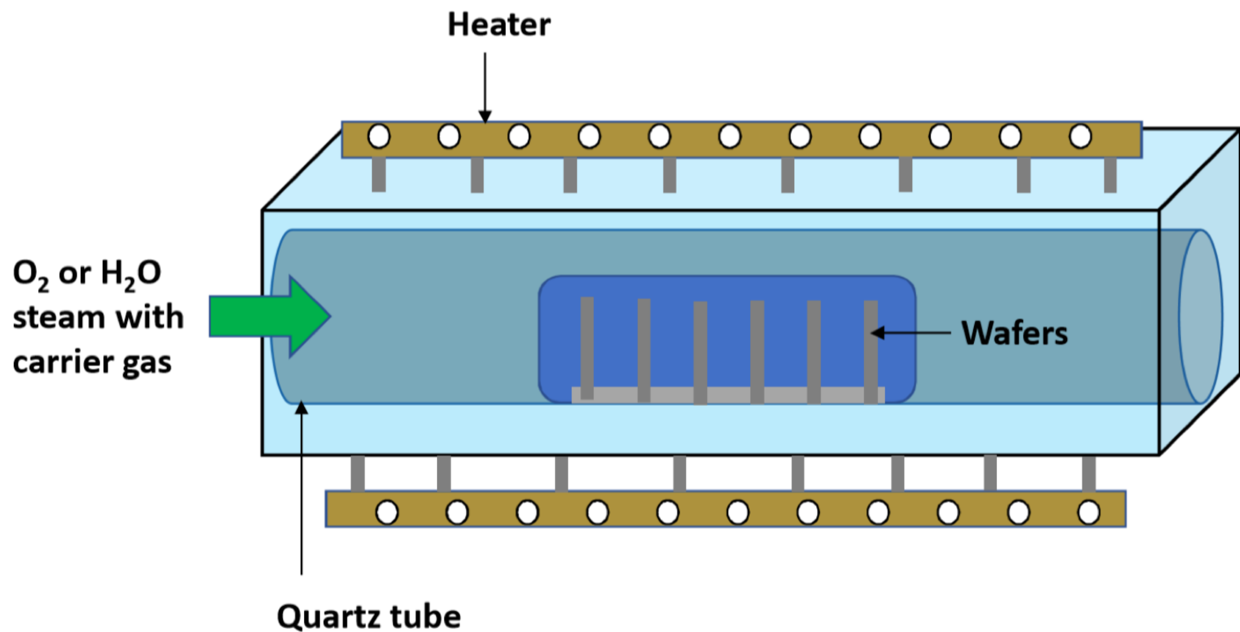


Figure 2.5: Schematic of a typical oxidation furnace

during the cleaning process.

To grow oxide thicknesses of a few hundreds of nanometers, as in our case, it is typical to use an electric resistance furnace for the high-temperature dry and wet oxidation processes. Figure 2.5 shows a schematic diagram of an oxidation furnace. Figure 2.6 shows images of the oxidation furnace used in this work. The dry oxidation process creates a high-quality oxide but is a slow process compared to the inferior-quality oxide created during the fast wet oxidation process. For our ReRAM devices, it is desired to have a thick isolation oxide layer to prevent any leaky unwanted currents flowing between the memory arrays. Hence, during the oxidation process, we perform the dry process (using O_2 gas flow) before and after we grow a thick oxide using the wet (H_2O steam) oxidation process. Therefore, the whole oxidation process comprises of two short (∼10 minutes) dry oxidation processes of with a long (∼2 hours) wet oxidation process sandwiched between them.

The oxidation furnace used in this work is shown in Figure 2.6. To begin the process, the

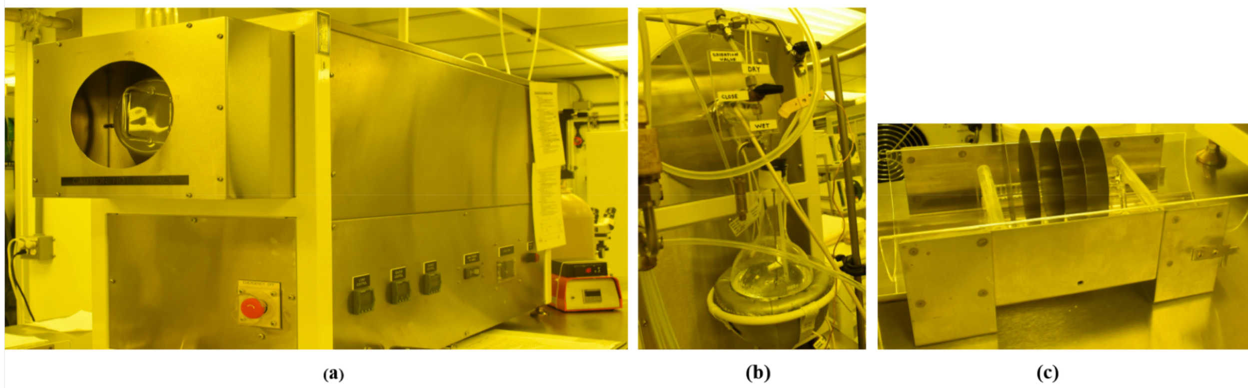


Figure 2.6: a) Oxidation furnace used in this work; b) O_2 & N_2 flow valve with the steam boiler; c) Quartz boat loaded with a cassette of wafers (from oxidation process used in this work)

chamber is set to 650°C and is purged with N_2 at a certain flow rate. Once the desired temperature is reached, a cassette of Si wafers placed on a quartz boat is introduced into the chamber. The temperature of the chamber is then increased to about 1050°C which is the desired oxidation temperature. The whole procedure of the oxidation process is outlined below:

1. Set chamber temperature = 650°C and N2 flow rate = 1L/min
2. Place wafer cassette on quartz boat and load into the chamber
3. Set steam boiler temperature = 95∼97°C & chamber temperature = 1050°C
4. Close N2 valve and open O2 valve with flow rate= 0.7 L/min
5. Time the Dry oxidation process for desired thickness
6. Open steam flow valve for the desired duration of wet oxidation
7. Close steam flow valve and run dry oxidation again for desired thickness

8. Close O2 flow valve, turn off steam boiler, set N_2 flow rate= 1L/min (purge with N_2 again)
9. Set chamber temperate to ambient temperature and wait for it to cool down
10. Take quartz tray loaded with wafer cassette out of the chamber
11. Turn off N_2 flow

The furnace is equipped with a thermocouple installed inside the chamber which ensures the desired set temperatures are met. The Deal-Grove model [5] can accurately predict the oxide thickness, which lets us estimate the time duration of the oxidation process. After the completion of the oxidation process, we measure the thickness of the oxide layer using an ellipsometer to ensure that the desired thickness is achieved. For our current work, we have tried to maintain an oxide thickness range of 700-800 nm.

2.3.3 Photoresist Spin-coating and Photolithography

The term "lithography" derives from the Greek words "lithos" meaning "stone" and "graphein" meaning "to write". In the semiconductor industry lithography plays a crucial role in device processing, as it is the method by which one can print complex device features onto the substrate. With evolving technology, the semiconductor industry now uses various methods of lithography such as photolithography, e-beam lithography, extreme UV lithography, etc. For the work presented in this dissertation, we have used the photolithography method to create the ReRAM device features onto our oxidized Si substrates.

The photolithography method exploits the photosensitive properties of certain materials and uses light exposure to print devices or integrated circuit features onto the substrate. We use a fused silica or glass plate with chrome features drawn on it known as a "photomask" which

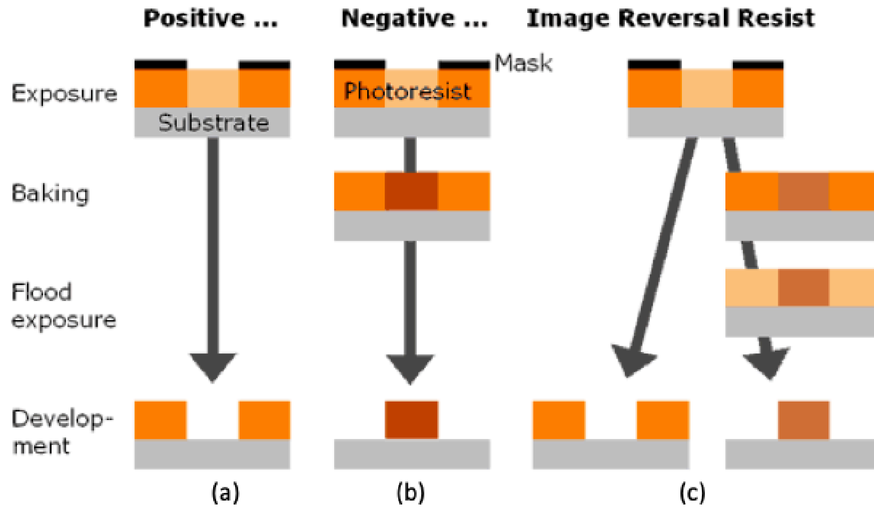


Figure 2.7: (a) Positive photoresist; (b) negative photoresist; (c) Image reversal [6]

is then projected onto a wafer covered in a photosensitive polymer called the "photoresist" and then exposed to UV light. The first step of photolithography is the spin-coating of the photoresist material explained in the next section.

I. Spin-coating Photoresist

A photoresist (PR) is a photo-sensitive polymer material that can be modulated for its solubility when exposed to controlled doses of ultraviolet light. The PR polymer changes its solubility by crosslinking with molecules following a UV exposure. The PR can be distinguished into two types, a positive PR and a negative PR. The positive PR when exposed to UV light, deteriorates in its strength and becomes more soluble compared to PR regions that are not under direct UV exposure. A negative PR on the other hand strengthens under UV exposure. Figure 2.7 (a) and (b) shows a schematic of positive and negative PR under UV exposure and their consequent development. In addition, a third kind of photoresist can be employed known as "Image reversal" photoresist. These resists are positive photoresists which after spin-coating are exposed to UV light twice (once with the photomask and once

without) and manipulated will result in a pattern similar to that of a negative resist (Figure 2.7(c)) [6]. For this work, we have employed the image reversal method. Image reversal resists are especially suitable if a user wants a resist to be used both positively and negatively for their photomasks. The advantages of a positive photoresist are its better resolution quality and thermal stability, a negative photoresist on the other hand is more challenging to develop and is very sensitive to processing environments. The image reversal method helps a user reap the benefits of a positive photoresist while obtaining results expected of a negative photoresist using the same photomask.

Spin coating photoresist is one of the most crucial steps in lithography, since variations within the photoresist thickness impact greatly the quality of a developed pattern, which in turn affects the subsequent deposition steps. Given below is the process recipe we follow for spin coating photoresist onto thermally oxidized Si wafers. The image reversal photoresist that we use is AZ 5214E-IR manufactured by the German company Merck. The below spin-coat recipe creates a 1.4 μm thick layer of PR on the wafer.

Spin-coat photoresist AZ 5214E-IR:

- Step 1: 15 sec @ 500 rpm
- Step 2: 45 sec @ 4000 rpm
- Step 3: 15 sec @ 500 rpm

II. Mask Alignment and UV Exposure

As mentioned before, the photomask is a quartz or glass plate with a chrome metal design. The photomask acts as the template to expose features onto PR spin-coated wafers. The photomasks are optically flat, with UV light passing through the bare quartz or glass regions

while the chrome regions are impervious to UV light. The chrome features are printed onto the quart plate using e-beam lithography.

Based on the distance between a photomask and the substrate during exposure, there can be 3 main categories: contact, proximity, and projection. As the name suggests, in contact printing the chrome side of the photomask is in direct contact with the photoresist spun on the substrate. This mode of printing gives excellent feature resolution but in reality, neither the photomask nor the substrate is completely flat thus creating irregularities within the features. This issue can be alleviated by pumping some atmospheric pressure. Proximity printing on the other hand avoids the issues that come with contact printing by maintaining a uniform distance between the mask and the substrate during exposure but suffers from poorer feature resolutions. Projection printing can be thought of as the best of both worlds where it avoids any contact-based issues but also delivers good resolution [7].

The wafer after PR spin-coating is loaded into a mask aligner where it is precisely aligned to the photomask as desired. Once the wafer and photomask are aligned as per the requirements, the wafer is exposed to a predetermined dosage of UV light for a specific time. This process of alignment and exposure to precise UV dosage (J/cm_3) requires a certain level of optimization in order to get features printed on the substrate. The optimization routine depends largely on PR thickness, UV wavelength, and exposure energy. A little deviation from the process recipe might end up creating overly exposed or under-exposed features after development. A wide range of UV wavelengths can be used depending on the available optical sources. For our work, we have used the 365 nm (i-line) UV wavelength with a mercury lamp as its source.

Figure 2.8 shows the mask patterns of the bottom electrode, solid electrolyte, and the top electrode used for this current work. The mask patterns are overlayed on top of each other in a cross-bar architecture. A ReRAM cell is created at the cross-section of every bottom

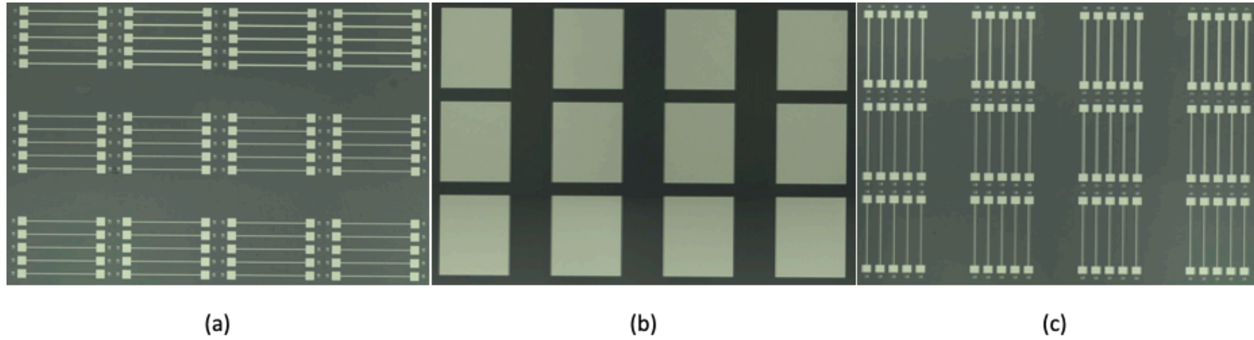


Figure 2.8: (a) Bottom electrode mask; (b) Solid electrolyte mask; (c) Top electrode mask

electrode, solid electrolyte, and top electrode. The width of the bottom and top electrodes for our devices range from 1-35 μm. Figure 2.9 shows the entire photomask. For each layer of the device, the photomask is rotated to the desired pattern for exposure.

Given below is the entire process recipe for spin-coating PR, UV exposure, post-exposure bake and development of PR:

1. Spin-coat photoresist AZ 5214E-IR:
   - Step 1: 15 sec @ 500 rpm
   - Step 2: 45 sec @ 4000 rpm
   - Step 3: 15 sec @ 500 rpm
2. Soft bake: 110°C, 50 secs
3. UV Exposure (with photomask): 30mJ/cm^2
4. Post Exposure Bake: 120°C, 2 mins [crucial step]
5. Flood Exposure (without photomask): 200mJ/cm^2
6. Develop: MIF 726, 60-70 secs

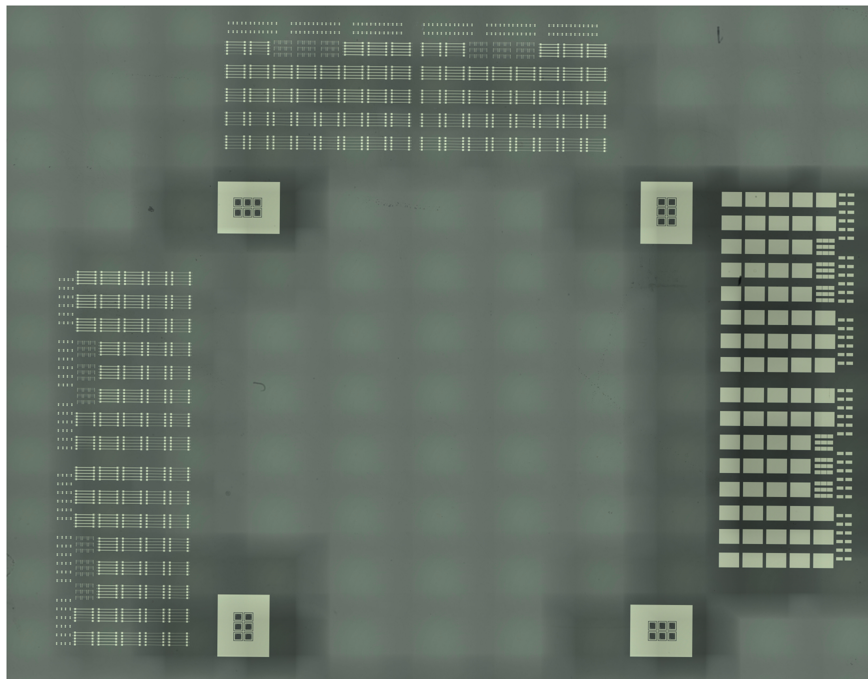


Figure 2.9: Entire mask used to fabricate ReRAM cells in this work. Clockwise from left: top electrode, bottom electrode, solid electrolyte

Figure 2.10 shows the image of the spin-coater and the mask aligner & exposure system used for this work.

III. Post Exposure Bake

The next step in the photolithography process is the post-exposure baking (PEB). We perform this step between the two exposure steps that we undergo (Mask exposure and flood exposure). This step is the most crucial one for image reversal. The post-exposure bake initiates the chemical reaction which results in the negative imaging of the photoresist in our case. The post-bake temperature and baking time have to be very precise to obtain the desired results. The temperature for post-exposure bake is usually higher than the pre-bake temperature.

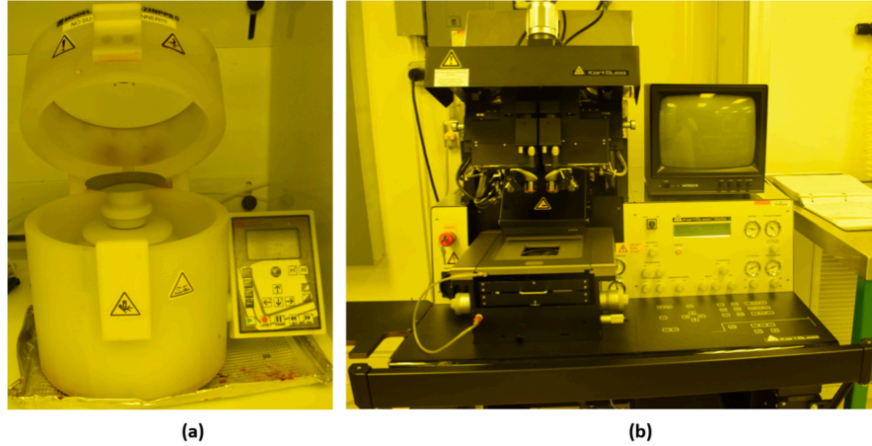


Figure 2.10: (a) Spin-coater; (b) Karl Suss MA-6 Mask Aligner

IV. Development

The final step of the lithography process is PR development. In this process, the photoresist is selectively removed as it dissolves in a developer solution when the exposed wafer is soaked in it. The wafer is immersed in the developer solution at a specific temperature for a specific time, resulting in patterned PR features on the wafer. MIF 726 developer is used for this work to develop AZ 5214E photoresist. The wafer is soaked MIF 726 for 60-70 secs after which the patterned image is clearly visible on the wafer. While soaking the process requires a bit of agitation. After the patterns are developed, the wafer is immediately rinsed with DI water to terminate the development process and blow-dried with N_2.

2.3.4 Physical Vapor Deposition

Once the wafers undergo the photolithography process and have been patterned, the next step is Physical Vapor Deposition (PVD). This method deposits thin films on the silicon substrate by physically transferring the source material from a crucible or a sputter target onto the substrate surface in its gaseous phase. The PVD equipment used for this work is the

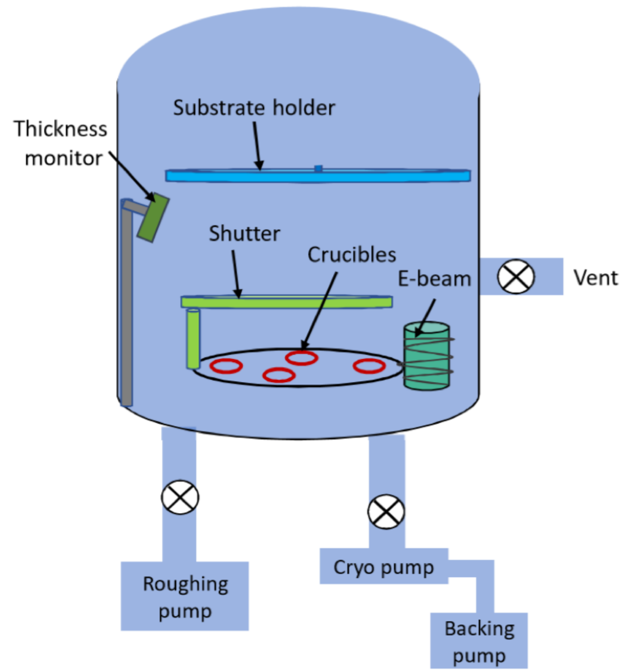


Figure 2.11: Schematic of a typical e-beam evaporation chamber

Kurt Lesker PVD 250. The specific method of PVD used in our work is called the e-beam PVD. The source material like the metals or the solid electrolyte used comes in the form of pellets These pellets of material are preconditioned in a crucible made of materials with high thermal stability, generally graphite. To start the deposition process, the substrate, and the crucible with the source material are placed inside the PVD chamber and are brought down to a very low pressure in the range of 2×10^{-6} - 4×10^{-6} Torr. Once this range of low pressure is achieved, an electron beam is focused on the crucible to melt the source material inside. Once the material reaches its evaporation point, it begins coating the inside of the chamber. The evaporated material deposition rate can be defined as the rate of mass accumulation on the wafer surface given by the following equation [7].

$$R_{deposition} = \sqrt{\frac{M}{2 \times \pi \times K \times \rho^2}} \times \frac{P_e}{\sqrt{T}} \times \frac{A}{4 \times \pi \times r^2} \tag{2.3}$$

Equation 2.3 shows that the rate of deposition is dependent on the deposition temperature T, the density of the source material ρ, and the chamber geometry. The deposition rate can be controlled by the user by modulating the e-beam current. The current also controls the e-beam density. In addition, the user can also control the e-beam lateral and longitudinal sweep amplitude and frequency. The PVD chamber is also equipped with a quartz crystal which monitors the rate of material deposition and the thickness of the film. The resonance frequency of the quartz crystal changes as more and more material gets deposited on it. The single quartz crystal has a finite lifetime at which point its resonant frequency has shifted considerably thus giving unreliable thickness data. At this point, the quartz crystal should be replaced which is a very inexpensive process.

The Kurt Lesker PVD system also requires the user to define the source material properties such as the material density, z-factor and tooling factor to accurately estimate the deposition rate and the thickness of the deposited material. Figure 2.11 shows a schematic of a typical e-beam PVD chamber, while Figure 2.12 shows the image of the chamber of the Kurt Lesker PVD 250 used in this work.

Table 2.1 shows the e-beam deposition parameters for the various thin films deposited in this work.

2.3.5 Lift-off

The last step in the successful patterning of a material layer on our substrate is the lift-off process. This process is employed in order to avoid intricate and sophisticated etching steps as used in the industry. While etching is suitable for ALD (Atomic Layer Deposition) deposited layers, the lift-off technique gives a good yield for PVD materials. The lift-off process is a technique to remove the photoresist and deposition material on top of it while

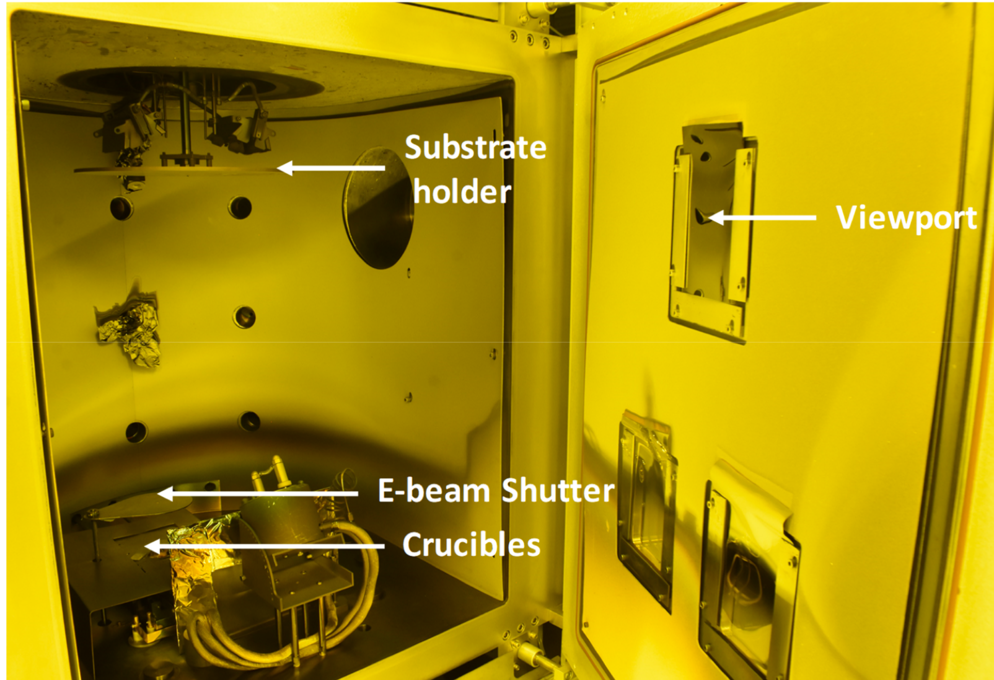


Figure 2.12: The Kurt Lesker PVD 250 e-beam evaporation chamber used in this work

Material	**Cu**	**TaO_x**	**Pt**	**Ti**	**Cr**	**Ru**	**Co**	**SiO_2**
Thickness (Å)	1500	250	500	200	200	500	500	300
Melting temperature (°C)	1085	1872	1768	1668	1907	2334	1495	1710
Chamber base pressure (Torr)	2.5×10^{-6}	1×10^{-6}	4×10^{-6}	1.9×10^{-6}	4×10^{-6}	1×10^{-6}	2×10^{-6}	2×10^{-6}
e-beam current (mA)	120	51	180	62	15	255	80	20
e-beam deposition rate (Å/s)	0.6	0.4	0.5	0.3	0.3	0.3-0.5	0.4	0.5
Density(gm/cm^3)	8.93	8.2	21.45	4.5	7.21	12.36	8.9	2.65
Tooling factor	140	140	140	140	140	140	140	140
Z-ration	0.437	0.3	0.245	0.628	0.305	0.182	0.343	1

Table 2.1: e-beam deposition parameters for various thin films used in current research work

keeping intact the intended deposition material directly in contact with the substrate. The image reversal technique employed during photolithography renders it possible for us to use the lift-off method because of its worthwhile undercut profile. The wafer after PVD is immersed in a PR-dissolving solvent such as acetone. The undercut profile of the PR achieved through image reversal creates an opening for the acetone to seep through and attack the sidewalls of the PR. As the PR dissolves into the acetone, the material deposited on top of PR gets lifted off the substrate within a few minutes while the materials deposited directly on top of the substrate remain in place. As no etching is involved in this patterned material transfer process, the substrate remains free from any etch-related damage. However, the biggest limitation of the lift-off technology is that it is limited to only a single metallization layer at a time and the sputtering technique will not work with it. Another drawback of this technology is that the lifted-off materials can float within the acetone solution and can potentially stick to the wafer which can create low yields. The lift-off process is primarily suited for research and development.

To summarize the whole fabrication process, Figure 2.13 gives a schematic representation of the process flow of depositing the Pt/Ti bottom electrode. The entire process is repeated two more times to create the solid electrolyte and the top electrode layer. Figure 2.14 represents the schematic of the cross-sectional view of a ReRAM cell after all the layers are deposited. Additionally, Figure 2.15(a) and (b) shows images of the fabricated ReRAM arrays. In both the images, horizontal electrode lines are the Pt electrodes and the vertical electrode lines are the Cu electrodes. Every cross-section of a Pt electrode and a Cu electrode is a ReRAM cell. The TaO_x layer is seen as the greenish rectangle encompassing the electrode lines of an array.

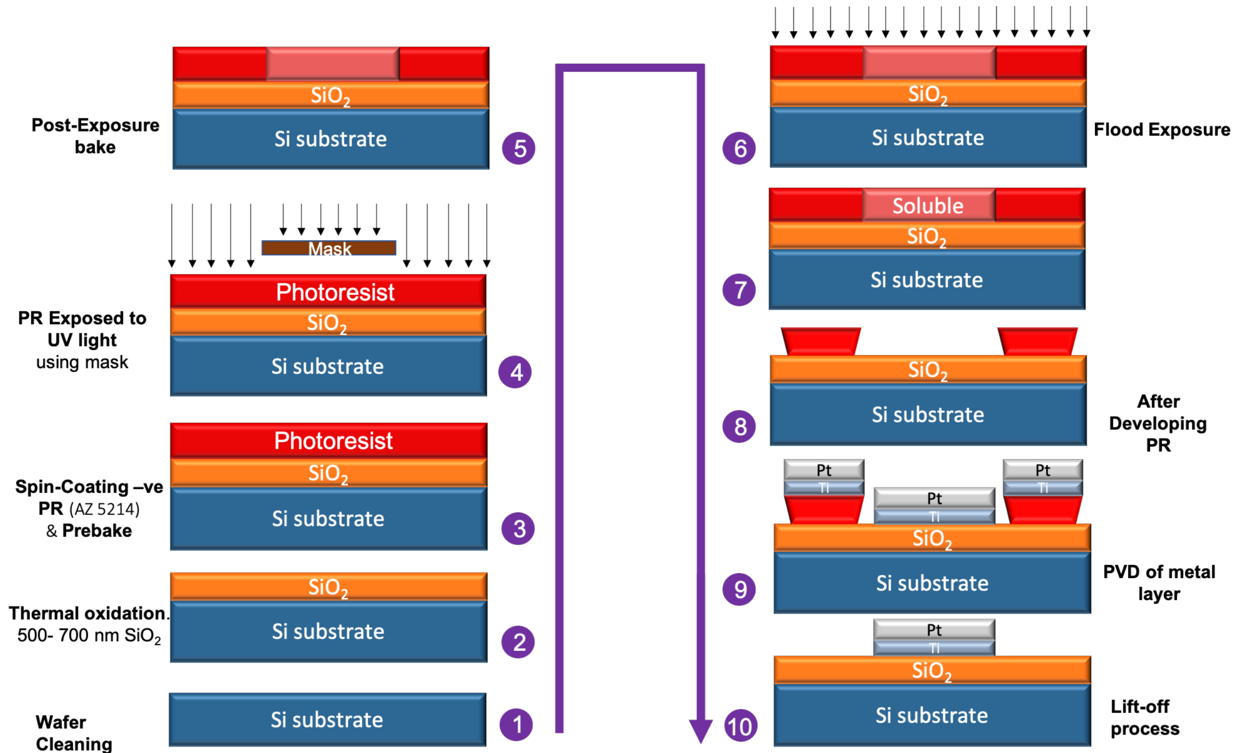


Figure 2.13: Complete process flow for fabrication of Pt/Ti bottom electrode layer

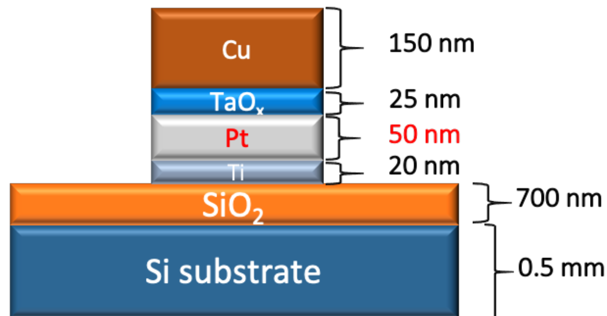


Figure 2.14: Cross-section of a completed Cu/TaO_x/Pt ReRAM memory cell with layer thickness specified (image not drawn to scale)

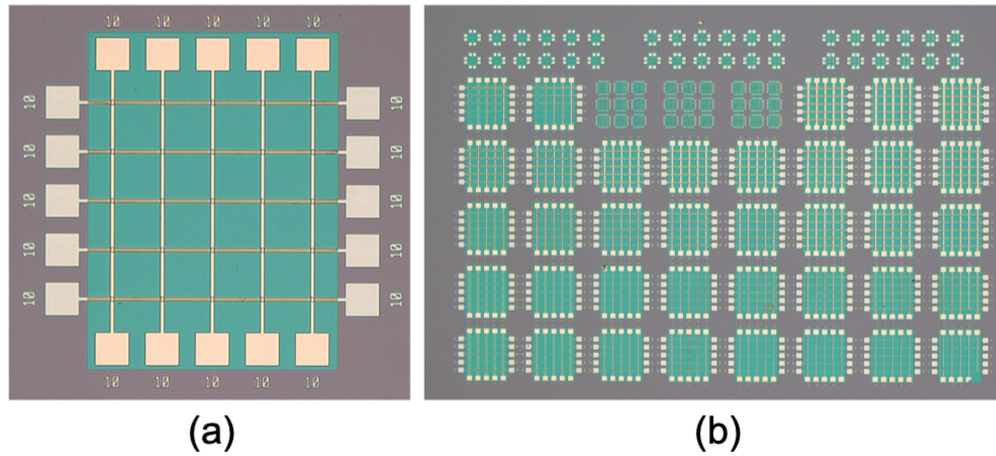


Figure 2.15: Image of a (a) fabricated 10μm $\times$ 10μm ReRAM array; (b) collection of multiple fabricated ReRAM arrays on a single wafer.

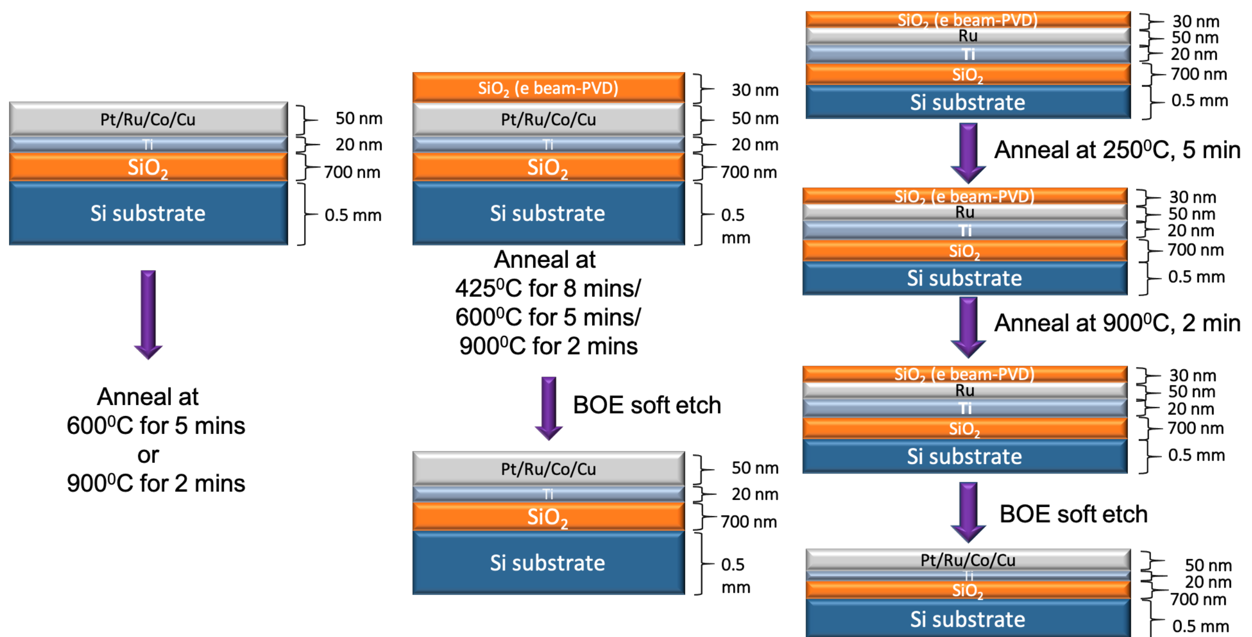


Figure 2.16: Samples created for surface roughness measurement under annealing conditions

2.4 Fabrication of Samples for Surface Roughness Measurement

In addition to characterizing the fabricated ReRAM cells, this work also investigates the effect of material properties on device performance including material surface roughness. To measure the surface roughness of the materials used in our ReRAM devices, multiple samples were created. These samples were blanket depositions of different materials outlined in Figure 2.16. Samples with blanket depositions of metals Pt, Ru, Co, and Cu were created. In addition, we also measured surface roughness on samples of e-beam PVD deposited SiO_2 and TaO_x (not shown in image) layers. Each PVD-deposited metal was subjected to different anneal temperatures for specific periods of time (shown in the image). Samples were also created, where metal layers were subjected to annealing temperatures with a passivation layer of e-beam PVD-deposited SiO_2 (30 nm). The SiO_2 passivation layer was etched off using BOE before the surface roughness measurement. Chapter 3 further details the surface roughness measurements carried out in this work.

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Chapter 3

Effect of Inertness, Surface Roughness, and Other Properties of Electrodes in ReRAM Applications

The following chapter has been reproduced from Ref. ***Amrita Chakraborty, Mohammad Al-Mamun, and Marius Orlowski. Inertness and Other Properties of Thin Ruthenium Electrodes in ReRAM Applications. In Dr. Yao-Feng Chang, editor, Ruthenium - Materials Properties, Device Characterizations, and Advanced Applications, Chapter 7. IntechOpen, Rijeka, 2023.*** *with minor changes.[1]*

Building nonvolatile memory such as ReRAM directly into a CMOS backend (BEOL) would reduce latency in connectivity-constrained devices and reduce chip's footprint by stacking NVM memory on top of the logic circuits. This co-integration is facilitated by a broad commonality between ReRAM and BEOL as both rely on the same basic metal–insulator–metal (MIM) structure. One good candidate for a ReRAM cell is the Cu/TaO_x/Pt device. As platinum is not an economic choice, a BEOL compatible replacement is desirable. A good candidate to replace Pt electrode is ruthenium (Ru), currently being used as a liner/diffusion barrier in sub-15 nm technology nodes and soon to supplant tungsten as

via, and Cu as interconnect materials. We report on extensive characterization of a Cu/TaO_x/Ru device and compare its performance/reliability with extant ReRAM devices. Against the background of well characterized non-Ru ReRAM devices, Cu/TaO_x/Ru cell constitutes a microlaboratory for testing a wide range of Ru properties with the Cu nanofilament as a probe. Since the temperature of the cell can be controlled internally from 27°C to ∼1100°C, thin Ru layers can be subjected to much more comprehensive tests than it is possible in the interconnect MIM structures and reveal/confirm interesting material properties, including the impact of embedment.

3.1 Introduction

This chapter looks at the material properties of various thin metal films from the perspective of their suitability for use as an inert electrode in resistive RAM (ReRAM) cells, such as Cu/TaO_x/Pt, Cu/TaO_x/Ru , etc.[2], that lends itself to be readily integrated into the CMOS back-end-of-line (BEOL) [3]. Advanced interconnects at 10 nm half-pitch pin, in order to overcome the scaling issues with Cu interconnects, increasingly pin hopes on ruthenium metallization, not only as a liner and diffusion barrier for Cu, but also as a stand-alone material for contact plug, via, and even interconnect lines [4, 5, 6]. Such integration of ReRAM memory into BEOL has the potential of reducing the latency in connectivity constrained computational devices and of bringing logic and memory closer together [7, 8, 9]. This cointegration is rendered possible and viable as low-k dielectrics and Cu/Ru/Co interconnect lines already prefigure a ReRAM device as a MIM structure, and the crossbar architecture of a typical two-terminal ReRAM memory array consists of electrode lines that may serve as

interconnect lines and vice versa with metal vias being replaced by ReRAM switching layer. The replacement of the via material with the switching layer leads to the concept of formation of conductive vias on the fly, by an application of an electric pulse after the IC chip has been already manufactured [10]. Building nonvolatile memory (NVM) directly into a CMOS low-k interconnect back-end, would not only reduce latency in connectivity-constrained computational devices but also reduce the footprint of a chip by stacking memory on top of the logic. Upon successful integration, the interconnect information bottleneck could be untied and morphed into several system architectures using the same basic universal hardware platform.

Given the auspicious circumstances, we elucidate in this chapter the material properties of different metal thin films in the light of comparison of the performance of different Cu/TaO_x/Metal ReRAM devices. In addition, as the ReRAM devices, such as Cu/TaO_x/Ru, Pt, Co, can be intrinsically and locally heated up to ca 1100°C, thin metal layers like that of Pt, Ru, Co, etc. can be subjected to much more comprehensive tests than it is possible in the interconnect MIM structures to reveal material properties of as a stand-alone and as an embedded material.

The ReRAM devices, by themselves, have recently been of great interest to both industry and academia as a potential replacement for a stand-alone volatile dynamic random-access memory (DRAM) and nonvolatile flash memories (NVM) that are nearing the end of their dimensional scaling roadmaps [8]. These two-terminal devices exhibit figure eight-like pinched current–voltage (I–V) hysteresis switching between a high resistance OFF state (R_{off}) and a low resistance ON-state (R_{on}) with memristive characteristics [11, 12, 13]. Resistive memory cells also hold promise for neuromorphic applications [14, 15, 16]. A specific subcategory of a ReRAM device, the conductive bridge random access memory (CBRAM) is being extensively explored as a promising candidate for a resistive memory device [17] and serves here

as a probe into Ru property materials. In general, a CBRAM device consists of an active anode, an insulating layer, and an inert cathode. The anode consists of Cu, Ag, or Ni, which can dissolve in the solid electrolyte layer [18, 19]. The resistive switching behavior can be explained by the formation and rupture of a Cu conductive filament (CF). The insulating layer, a dielectric, called also switching layer, such as Ta_2O_5, TaO_x, GeSe, GeS_2, Al_2O_3, and SiO_2 [20], allows for ion and defect electromigration when an electric field is applied. When a positive voltage is applied to the Cu electrode, Cu^+ cations are generated according to the redox reaction, $Cu \leftrightarrow Cu^+ + e^-$, dissolve, and migrate into the solid electrolyte [21]. Cu^+ cations, after traversing the switching layer under the influence of an electric field, are electrochemically reduced on the Pt cathode which acts as an effective diffusion barrier for Cu atoms. As more Cu atoms accumulate to form a nanoscale conductive filament (CF), shorting the two electrodes, in so-called FORM and SET processes. The FORM operation describes the formation of the CF for the first time in a virgin memory cell. The SET operation is the restoration of an already-formed conductive filament after it had been partially ruptured in the so called RESET operation. The ON state is characterized by the resistance of the Cu CF, R_{on}, and when the CF is ruptured the device reverts to a high resistance OFF-state, characterized by the off-resistance, R_{off}. The ON/OFF ratio of CBRAM is usually significantly higher than 10^3 [22] and potentially allows multilevel switching in a single memory cell to store more than one bit of data [23]. To date, $Cu/TaO_x/Pt$ based devices have proven to be one of the more popular types of CBRAM devices due to numerous reports of excellent unipolar and bipolar switching characteristics, device performance, retention, reliability, endurance, and yield [24, 25]. Commercialization of non-volatile memory products based on RS devices derived from a $Cu/TaO_x/Pt$ cell has also been reported [26].

Against this backdrop, the main focus of the chapter lies in the comparison between the $Cu/TaO_x/Ru$ and $Cu/TaO_x/Pt$ devices. As already mentioned, Ru is a good candidate to

	Work Fct.[eV]	Therm.Cond.[W/mK]	Melt.Temp.[°C]	S.R. at 27°C [nm]
Cu	4.7	386	1084	2.7
Pt	6.3	69	1770	1.8
Ru	4.7	116	2334	1.5
Co	5.0	69	1495	2.3

Table 3.1: Material properties of metals: Work function, thermal conductivity, and melting temperature, and surface roughness at 27°C after EBPVD deposition of metals used in our resistive switching devices.

replace Pt and has been already deployed in the earlier CMOS BEOL technology nodes supplanting Ta or TaN as the liner material [27**?**]. Ru is ca. 45 times less expensive than Pt and has similar inertness properties as Pt. Pt and Ru are both transition metals with almost identical outer shell structure: The electron configuration for Ru is $[Kr]4d^7 5s^1$ for Pt $[Xe]4f^{14} 5d^9 6s^1$, where Kr and Xe denote the noble gases, Krypton and Xenon, respectively. Ru has a single electron in the fifth orbital and 15 electrons in the fourth orbital, while the larger Pt atom has a single electron in the sixth orbital and 17 electrons in the incomplete fifth orbital. In addition, the Ru-Cu phase diagram shows negligible solid solubility between the two elements, even at 900°C, rendering Ru an excellent diffusion barrier for Cu diffusion [28]. The work function of Ru at 4.75 eV is comparable to that of Cu at 4.7 eV and much lower than that of Pt at 6.35 eV which has the highest work function among metals. The material properties of metals under consideration in this investigation are summarized in Table 3.1. The work function difference between Cu and Pt/Ru is partly responsible for the higher forming and set voltages in Ru devices as compared with Pt devices.

The chapter is organized as follows: In Section 3.2, we describe briefly the fabrication process of the ReRAM cells employed here. In Section 3.3 we establish the characteristic features of the electrical performance of a Cu/TaO_x/Pt device, serving as our baseline device, for comparisons with its counterparts, the Ru and Co devices. In Section 3.4 we discuss the

analogous electric characteristics of the Pt, Ru, and Co devices. In this framework, we discuss how the performance of one device differs from the performance of derivative devices and how these differences in performance can be related to their material properties. In Section 3.5, we analyze how the surface roughness (SR) properties of the metals, established by Atomic Force Microscope (AFM) measurements, have an impact on the electric performance of the respective devices. In Section 3.6, we present results on reliability and endurance tests of the three devices, which show that Ru shows markedly degraded reliability behavior compared with the Pt devices. In Section 3.7, we present evidence that different embedment scenarios of the same identical Ru device, lead to significantly different electrical performance and reliability of Ru devices. Finally, in Section 3.8, we present x-ray diffraction (XRD) studies of the pertinent layer systems annealed at elevated temperatures and show that at annealing temperatures higher than 425°C, interlayer reactions in terms of formation of ruthenium and copper silicide occur, and lead to degraded functionality, particularly of the Ru devices.

3.2 Fabrication of ReRAM Devices

Figure 3.1(a) shows the optical micrograph of the crossbar architecture and the device cross-section of a typical Cu/TaO_x/Pt resistive switch. The devices are fabricated in a crossbar array on a thermally oxidized Si substrate with a SiO_2 thickness of 730 nm. Both metal electrodes and the metal oxide were deposited by electron beam physical vapor deposition (EBPVD) and patterned by layer lift-off technique. A thin Ti layer of 25 nm was used between Pt/Ru/Co and SiO_2 to improve the adhesion of the Pt/Ru/Co layer. The thickness of the TaO_x switching layer is 25 nm. The width of metal lines varies between 5 and 35 m resulting in rectangular device areas of the device in the range of (5 to 35) × (5 to 35) μm^2. The distance between the metal lines is 150 m. All metal layers (Cu, Pt, Ru, Co, Cr, Ti)

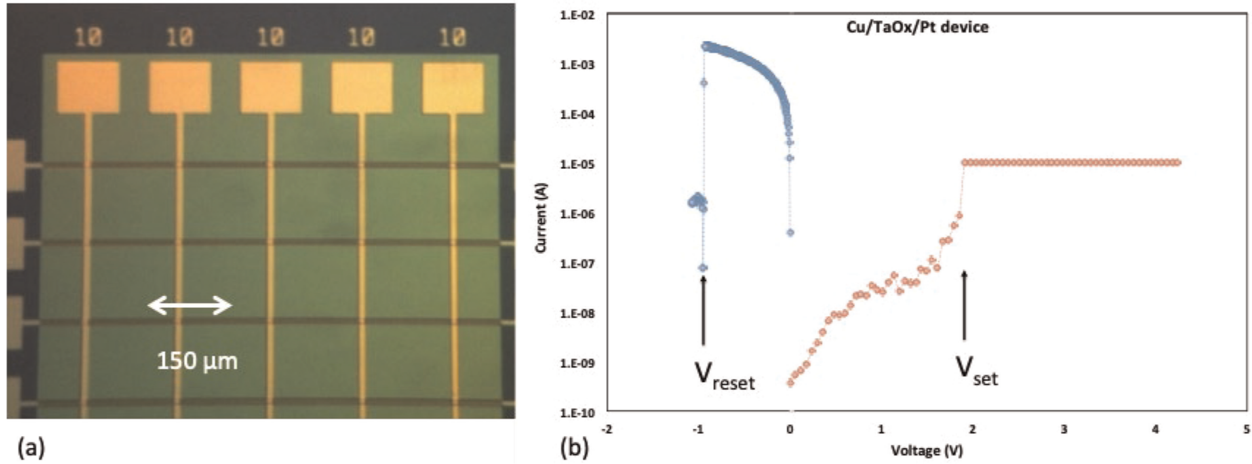

Figure 3.1: (a) Optical micrograph of the crossbar architecture of the $Cu/TaO_x/Pt$, $Cu/TaO_x/Ru$, and $Cu/TaO_x/Co$ devices. (b) Set and reset operation of the $Cu/TaO_x/Pt$ device with $I_{cc} = 10\mu A$. The I-V characteristics of $Cu/TaO_x/Ru$ and $Cu/TaO_x/Co$ devices look very similar. The critical switching voltages, V_{form}, V_{set}, and V_{res} for the $Cu/TaO_x/Pt$, $Cu/TaO_x/Ru$, and $Cu/TaO_x/Co$ devices are summarized in Table 3.2.

were deposited by EBPVD in a Kurt Lesker ebeam PVD-250 chamber. I–V characteristics were measured by a Keithley 4200-SCS at room temperature. The oxygen-deficient TaO_x (x $\approx$ 1.9) was deposited also in the PVD-250 chamber by evaporating Ta_2O_5 pellets without O_2 injection into the evaporation chamber. The thicknesses of Ru, Pt, Co, and Cu layers are 50, 50, 50, and 150 nm, respectively. The details of the sample manufacturing process have been given in [22, 29] where the role of the stoichiometry parameter x in TaO_x on resistive switching properties is being discussed in detail.

Figure 3.2 shows the cross-section view of five devices that have been manufactured for this study. Figure 3.2(a) shows the baseline device of $Cu/TaO_x/Pt$ including the two derivative devices, where Pt has been replaced by Ru and Co electrodes. Figure 3.2(b) shows a different embedment of an identical Cu/TaOx/Ru device as in Figure 3.2(a), where an additional TaO_x layer has been inserted below the device proper, between the 730 nm thick field oxide and the Ti glue layer. Figure 3.2(c) shows still another embedment case of the Ru device, where the Ti glue layer has been replaced by a Chromium (Cr) glue layer. The additional 30 nm

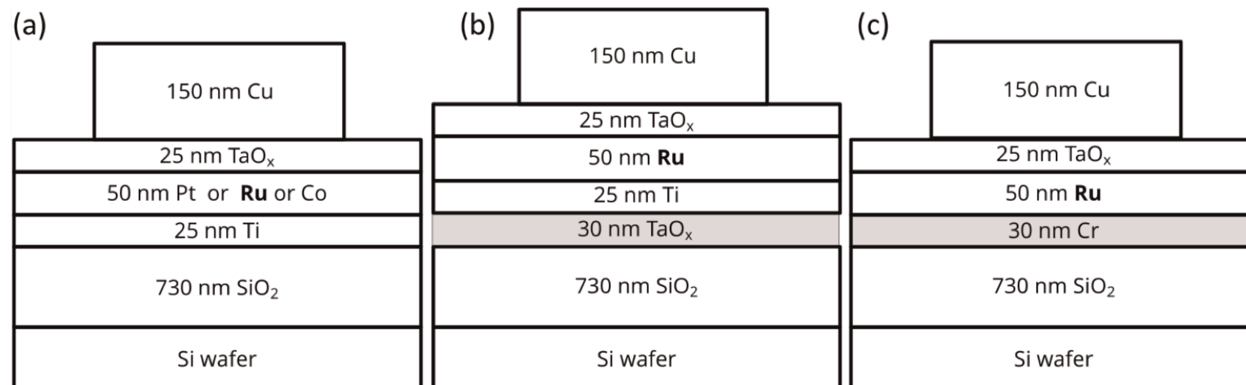

Figure 3.2: Cross-sections of the five ReRAM devices. (a) Baseline Cu/TaO_x/Pt device with two derivative devices, where Pt is replaced by Ru and Co. (b) Identical Ru device as in (a) but with additional TaO_x layer inserted between Ti glue layer and 730 nm thick field oxide. (c) another case of embedment of the Ru devices where the Ti glue layer has been replaced by a Cr glue layer.

thick TaO_x layer, and the Cr layer have also been deposited by EBPVD.

3.3 Electrical Properties of ReRAM Cell (Cu/TaO_x/Pt)

In this section, we establish the basic device properties of the Cu/TaO_x/Pt device. Those properties will serve as a baseline comparison for the performance of the Cu/TaO_x/Ru device. The analysis of the differences between those devices and the Cu/TaO_x/Co device allow us to assess the material properties of Ru. When a positive voltage applied to the Cu electrode of a Cu/TaO_x/Pt is swept at a constant voltage ramp rate rr [V/s], the current will remain substantially zero until a critical voltage.

V_{set} is reached, at which a Cu conductive filament (CF) is formed connecting the Cu and Pt electrodes with each other, and the cell switches from a high resistive state (HRS) characterized by R_{off} (1–900 MΩ) to a low resistive state (LRS) characterized by Ron (70 Ω–15 kΩ), yielding a ratio of R_{off}/R_{on} ≈ 103–107. When the voltage is swept back, ohmic behavior is observed until a negative voltage V_{res} is reached when the CF is ruptured and the

current collapses to a very small value. A typical log-scale I-V switching characteristic of the Pt device is shown in Figure 3.1(b). When the cell is set to an ON-state for the very first time, one speaks of a forming operation, characterized by the forming voltage, V_{form}. Since, during the set operation relatively few Cu atoms have to be added to pluck the gap of the ruptured filament, V_{set} is usually substantially smaller than V_{form}. For Cu/TaO_x/Pt devices, we find distribution V_{form} with a mean $V_{form,m}$ = 4.5 V and a standard deviation of σ = 0.6 V, the V_{set} distribution with a mean, $V_{set,m}$ = 2.8 V, and standard deviation, σ =0.6 V. The rupture of the CF is triggered mainly by Joules heating at a critical current $I_{res} = V_{res}/R_{on}$. The V_{res} distribution of our Cu/TaO_x/Pt devices is characterized by $V_{res,m}$ = -0.9 V and σ =0.3 V. The electric characteristics in terms of threshold voltages for all devices are summarized in Table 3.2. These distributions apply roughly both to a multitude of devices as well as to a single device that has been switched repeatedly. The endurance of the Pt devices depends on the I_{cc} current during the set operation. For not too low I_{cc} (>10 μA) and not too high I_{cc} (<5 mA), the device can be switched very often. Typically, in a few cases, a device was switched for 220 times, and it could still be switched even further. In most instances, a compliance current I_{cc} is imposed, lest the devices be damaged. No I_{cc} current limitation is applied during the reset operation. Ron of the LRS state depends on I_{cc} via Eq. (3.1), where the exponent n for cation filaments is very close to unity.

$$R_{on} = K/I_{cc}^n \tag{3.1}$$

The R_{on}–I_{cc} relation in Eq. (3.1) has been reported to be valid for numerous anode/ electrolyte/cathode material systems [30, 31, 32] with n ≈ 1. For Pt devices we obtain K = 0.29 V and n = 1.01. In ref. [2] it has been shown that the constant K in Eq. (1) is universally correlated to the minimum set voltage for all metallic conductive filaments reported so far. During the reset operation, the ReRAM cell is exposed to large currents which raises the

	$\mathbf{V_{form,m}}$ [V]	$\sigma_{\mathbf{form}}$ [V]	$\mathbf{V_{set,m}}$ [V]	$\sigma_{\mathbf{set}}$ [V]	$\mathbf{V_{res,m}}$ [V]	$\sigma_{\mathbf{reset}}$ [V]
$Cu/TaO_x/Pt$	4.5	0.6	2.8	0.6	-0.9	0.3
$Cu/TaO_x/Ru$	7.3	0.7	4.4	0.8	-3.4	0.7
$Cu/TaO_x/Co$	4.7	2.2	2.7	0.9	-1.0	0.6

Table 3.2: Critical switching voltages, V_{form}, V_{set}, and V_{res} for the $Cu/TaO_x/Pt$, $Cu/TaO_x/Ru$, and $Cu/TaO_x/Co$ devices along with their sigma distribution values.

temperature of the filament by depositing Joule's heat, primarily, in the Cu CF. When critical temperature in the filament has been reached, the Cu atoms begin to diffuse out and the filament is ruptured. The reset currents defined as $I_{res} = V_{res}/R_{on}$ are typically in a few mA range. Hence, most of the Joule's heat Q_{JH}1 deposited during the reset operation is given by Eq. (2)

$$Q_{JH} = \int_0^{t_{res}} \frac{V^2(t)}{R_{on}} dt = \int_0^{V_{res}/rr} \frac{rr^2 \times t^2}{R_{on}} dt = \frac{V_{res}^3 \times I_{cc}}{3 \times rr \times K} \tag{3.2}$$

where V_{res} is the reset voltage, $t_{res} = V_{res}/rr$ is the reset time. The reset ramp rate, *rr*, and the compliance current, I_{cc}, may be used to control amount of heat deposited in the cell. Depending on chosen values for I_{cc} and *rr*, Q_{JH} can vary from 3 to 60 μJ [33]. The possibility of controlling the dissipated heat in the filament in terms of compliance current, I_{cc}, and ramp rate, *rr* will be important for the characterization and analysis of the electrical performance of the Ru, Pt, and Co devices.

The geometrical shape of the filament has considerable implications for the reset operation. Three different shapes of Cu CF are shown in Figure 3.3. In Figure 3.3(a), a CF in the shape of a truncated cone with a sharp constriction at the top is shown. The bulk of its resistance is concentrated at the tip of the cone. Filaments with a sharp constriction at the top of the cone easily can be ruptured since the maximum Joules heat is deposited at the

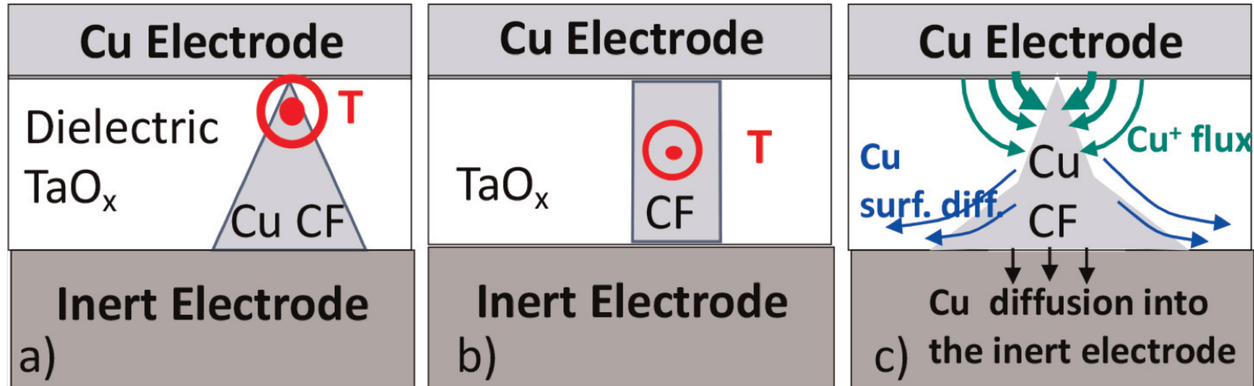

Figure 3.3: Three different shapes of the Cu filament that may occur at different SET operation conditions with location of the highest temperature during RESET operation indicated. (a) Highly resistive Cu CF with sharp constriction at the top of the cone. (b) a low resistance Cu CF of cylindrical shape. (c) Constructive and destructive Cu fluxes during formation of Cu CF.

tip and leads there to a high local temperature, which, in turn, triggers Cu out-diffusion and formation of a gap in the filament. When the filament is ruptured, the HRS state of the cell is being restored. In contrast, the cylinder shape of a robust Cu filament shown in Figure 3.3(b) leads to much lower resistance and the temperature hot spot is moving away from the Cu/TaO$_x$ interface to midway between the electrode interfaces, where it is much more difficult to reach high temperature and cause out-diffusion of a larger number of Cu atoms to form a gap. Experimentally, we consistently find that the rupture of a filament is more difficult at lower R_{on} resistance, that is, formed at higher I_{cc} than at high Ron resistance formed at low I_{cc}.

During the final stage of the set operation there are two Cu fluxes that are responsible for the formation of the filament as shown in Figure 3.3(c). The constructive flux occurs at the tip of the filament where the voltage drop is the largest and creates high electric field between the filament tip and the Cu electrode, which, in turn, allows for an enhanced transport of Cu^+ ions from the Cu electrode to the filament even after establishing the initial connection between the Cu filament and the Cu electrode. The role of I_{cc} is to limit

the resulting voltage drop and thus to set a limit on the electric field driving the Cu^+ ion transport. When sufficient number of Cu atoms is deposited at the tip, the resistance of the filament decreases, reducing the electric field at the tip and bringing the formation of the filament to a halt at a given I_{cc}. When I_{cc} is increased, then the electric field at the tip increases proportionally, triggering additional arrival of Cu^+ ions until the resistance of the filament drops sufficiently to reduce the electric field and, thus, to halt further Cu^+ ion transport. The destructive Cu flux is the Cu atom diffusion flux that weakens the base of the filament leading to a gradual change of the filament's shape from a truncated cone to cylinder-like shape. The second Cu flux has two components: (i) Lateral Cu diffusion along the TaO_x/inert electrode interface, and (ii) Cu diffusion into the inert electrode. The Cu atom diffusion flux out of the filament at the base is impacted by the thermal conductivity of the inert electrode. Ceteris paribus, the inert electrode with high heat conductivity will be able to remove heat at a higher rate than an electrode with low heat conductivity. The larger heat removal rate will result in lower attainable maximum temperature of the Cu CF. Hence, a cell with inert electrode of low thermal conductivity is bound to display enhanced Cu diffusion and structural weakening of the filament at a lower V_{res} voltages than high thermal conductivity electrode. The high temperature in the filament during the reset will trigger Cu diffusion near the base of the filament partly into the dielectric, partly along the TaO_x/inert electrode interface, and partly into the inert electrode if the inertness of the electrode be somehow compromised. The net result of those diffusion components is a weakening of the base of the cone and a gradual transformation of the shape of the filament from a sharply cone-shaped into a more cylinder-shape filament as shown in Figure 3.3(b). Once the shape of the filament is sufficiently close to that of a cylinder, it becomes very resistant to rupturing, and the number of switching cycles comes to a halt.

3.4 Comparison of Electrical Characteristics of Ruthenium (Cu/TaO_x/Ru) and Cobalt (Cu/TaO_x/Co) Devices to the Pt-based Device

The electrical characterization of the Ru device reveals that the device behaves very much like Pt and Co devices, albeit with some notable differences that can be all satisfactorily explained in terms of the material properties of the three metals given in Table 3.1.

Table 3.2 summarizes the critical switching voltages for the three devices and shows that all the critical voltages of the Ru devices are considerably higher than those of Pt devices: ΔV_{form}(Ru-Pt) = 2.7 V, ΔV_{set}(Ru-Pt) = 1.6 V, and ΔV_{res} (Ru-Pt) = 2.5 V. One notices that the work function difference $\Delta\phi(\mathrm{Ru,Cu})/q$ = 1.6 V between Pt and Ru corresponds exactly to ΔV_{set} = 1.6 V between Pt and Ru devices indicating that V_{set} values are being reached at the same strength of the electric field. Since the work function contributes to the internal electric field across the dielectric, this difference was to be expected. Comparing now V_{form} of Pt and Ru devices one notes that V_{form} for Ru is higher by 2.8 V than V_{form} for Pt, significantly higher than 1.6 V. This differential can be accounted in part by 1.6 eV as a difference of the work function between Pt and Ru, as discussed before.

The remaining voltage differential of 1.2 V can be attributed to the electric field enhancement factor that is correlated to the higher SR of Pt (1.8 nm) than that of Ru (1.5 nm). Higher SR, in general, causes a higher local field across the oxide at the same voltage, or in other words, the same critical field required for the Cu CF formation is reached at a lower voltage in Pt than in a Ru device. In Table 2, one observes also that V_{form} for Co device is only slightly higher than V_{form} for Pt device, despite a work function difference of $\Delta\phi(\mathrm{Pt-Co})/q$ = 1.3 V. Based on the work function argument, one would expect a higher V_{form} by about

1 V for Co devices than for Pt devices. However, one notes that the surface roughness of Co (2.4 nm) is significantly higher than that of Pt (1.8 nm). (SR will be discussed in more detail in Section 3.8.) The higher surface roughness of Co leads to a large enhancement factor of the local electric field due to the smaller curvature radius at the tip of the asperity. For a more detailed discussion of how the field enhancement factor correlates with SR, see ref. [34, 35]. The differences in SR explain that in order to reach a critical field required for the formation of a filament a lower voltage is needed in case of a rougher surface of Co than for smoother interfaces of Pt or Ru. Both effects help lower the V_{form} voltage of Co devices to a voltage only slightly higher than V_{form} for a Pt device. These comparisons show that for the filament formation the local electric field, and by extension, the surface roughness, is an important factor. One also notices that the surface roughness correlates well with the standard deviation of the V_{form} distributions of the three metals. The highest standard deviation observed for Co ($\sigma_{form(Co)}$ = 2.2 V) correlates well with highest surface roughness of SR(Co) = 2.4 nm of the cobalt devices, compared with the respective values of $\sigma_{form(Ru)}$ = 0.6 V and SR(Ru) = 1.5 nm for Ru, and $\sigma_{form(Pt)}$ = 0.6 V and SR(Pt) = 1.8 nm. for Pt devices.

Because of the work function difference between Pt and Cu of 1.6 eV, there is a considerable built-in field that favors Cu^+ ion transport toward the Pt electrode. In fact, it has been observed [36] that even at a TaO_x thickness of 25 nm, the work function difference is sufficiently high to set the device spontaneously into a conductive state after the device has previously been reset. This means that the electric field in the ruptured gap of the filament has reached the critical field of 3×10^6 V/cm [37] to set the device spontaneously. Not a single instance of spontaneous setting of the devices has been observed for the Ru and Co devices tested at the same conditions. Thus, the spontaneous forming of a ruptured filament is enabled by the high work function difference between Pt and Cu metal electrodes. Therefore, in

the absence of the built-in electric field, the electric field in Ru device has to be increased considerably by application of external bias to reach the critical field strengths in the TaO_x dielectric. It has been shown [37] that a field of $\approx 2.9\times10^6$ V/cm has to be reached in order to establish a Cu CF across a thin TaO_x dielectric layer, independently of the nature of the inert electrode.

Next, we discuss the large difference in V_{res}, between Ru and Pt device, ΔV_{res} (Ru-Pt) = 3.4–0.9 = 2.5 V, see Table 3.2. There is a general consensus that the rupturing of the Cu filament is attributed to the partial dissolution of the filament due to the Joules heating. The local temperature at the thinnest part of the filament can reach temperature in excess of 1084°C [38]. 1086°C is the melting temperature of Cu (see Table 3.1) and melting of Cu electrodes has been experimentally observed after excessive heating of a ReRAM cell [39, 40]. At such high temperature, the Cu atoms of the Cu CF diffuse out, may undergo the redox reaction in TaO_x, and are returned as Cu^+ ions by the electric drift fields back to the Cu electrode or stay immobilized in TaO_x material. The dissolution of the filament, triggered primarily by the Cu out-diffusion into the TaO_x matrix, depends on the critical temperature reached in the constriction of the CF. The overall balance of heat stored in the nanofilament is given by the resistive Joules heating of the nanofilament and via heat removal mainly by the heat sinks of the two relatively cold mesoscopic electrodes. The largest interface of the nanofilament is formed with the inert electrode (Pt, Ru, and Co) which forms the base of a truncated cone or a cylinder of the filament with the inert electrode (Figure 3.3). In this context, one notices that Ru has a thermal conductivity of 119 W/mK almost twice those of Co and Pt of 69 W/mK (Table 3.1). Thus, lower thermal conductivity of the inert electrode requires less Joules heating than an inert electrode with high thermal conductivity as the heat accumulates in the nanofilament in a shorter time than in the case of high thermal conductivity of the inert electrode. When inspecting the V_{res} voltages of the three devices

in Table 3.2, one notices that the V_{res} values for Pt (-0.9 V) and Co (-1.0 V) devices are essentially the same, which correlates again very well with the same thermal conductivities of the two metals of 69 W/mK.

Since the Cu filament in all three devices serves as our probe into the analysis of the material properties of the three inert electrode metals (Ru, Pt, Co), it is instrumental to ensure that the nature of the Cu CF probe is the same in the three devices. To this end, we have measured R_{on} dependence on I_{cc} of the three devices. We find that all devices display the same dependence given in Eq. (1) with exponent n being very close to 1, and the constants A of eq.(1), being 2.0 V, 0.5 V, and 0.5 V, for Ru, Pt, and Co devices. These values correlate very well with the V_{set} values for these devices given in Table 3.2. The high K value for Ru is consistent with the interpretation given in [2] that K reflects the lowest possible set voltage of the device.

Conductive filaments can also be fingerprinted by their temperature coefficient of resistance (TCR), α, as defined by the temperature dependence of the Ron resistance: $R(T) = R(T_o) \times [1 + \alpha(T - T_o)]$, which sensitively depends on the strength of the Cu filament. We have extracted the TCR from resistance measurements of Ron of Cu CF as a function of temperature, T. We find for a weak Cu CF of $R_{on} \approx 15k\Omega$ (corresponding to $I_{cc} = 10\mu A$) following TCR values for the three devices: TCR (Ru device) = 0.00236 K^{-1}, TCR(Pt-device) = 0.00235 K^{-1}, and TCR(Co device) = 0.00235 K^{-1}. It can be seen that they are almost identical. The same TCR measurements have been repeated for stronger (lower resistance) Cu CFs set at three orders of magnitude higher I_{cc}, I_{cc} = 10 mA. For I_{cc} = 10 mA we obtain much lower Ron value for the Cu filaments of 510 Ω, 230 Ω, and 315 Ω for the Ru, Pt, and Co devices, respectively. For the three robust CFs we obtain very similar TCR values are extracted: TCR (Ru device) = 0.0035 K^{-1}, TCR(Pt device) = 0.0036 K^{-1}, and TCR(Co device) = 0.0036 K^{-1}, which are, again, very similar. These values are typical of

strong Cu filaments; for comparison the TCR of bulk Cu is 0.0039–0.004 K^{-1}. These results ensure that in all the three devices the Cu filaments have the same properties conferring, thus, confidence that the Cu CF may serve as a reliable probe into the properties of the inert electrode materials Ru, Pt, and Co.

3.5 Surface Roughness Studies of Ru, Pt, Co, and Cu

In this section, we investigate the surface roughness of Ru, Pt, Co, and Cu thin films (50 nm) as a function of anneals at elevated temperatures for two cases: free and passivated metal surfaces. The impact of SR of metal electrodes on local field enhancement, dielectric breakdown, including ReRAM performance is well known and has recently attracted a lot of interest. A review of the impact of surface roughness on numerous devices and phenomena, including gas breakdown, dielectric breakdown in RF MEMS devices, in triboluminescence, MIM structures, capacitors, and ReRAM memory cells can be found in [34]. As early as 1928, Eyring et al. [41] found that logarithms of currents of extracted electrons from asperities display linear relation with the reciprocal of electric field strength at the tip of an asperity. The asperity has been modeled as a prolate spheroid of length c and base radius b. A field enhancement factor has been derived:

$$\beta = \left(\frac{c/r}{ln(2\frac{b}{r}) - 1} \right) \tag{3.3}$$

where $r = b^2/c$. For micro size asperities with $c = 16$ μm and $b = 0.7$ μm one obtains an enhancement factor of $\beta = 187$. Countless studies have confirmed since then the impact of the electric field enhancement factor on various physical systems [34].

Separately from the ReRAM devices, we have deposited by EBPVD blanket layers of the four

metals (Pt, Ru, Co, and Cu), each 50 nm thick, and using Rapid Thermal Annealing (RTA) annealed them at various temperatures with free and SiO_2-passivated surfaces – mimicking, thus, conditions that are likely to occur in the actual ReRAM cell during the switching events. Using Atomic Force Microscope (AFM), we have measured the surface roughness of the Pt, Ru, Co and Cu at room temperature, that is, just after their depositions by EBPVD, and after anneals using RTA of the free surfaces at 425°C for 8 min, 600°C for 5 min, and at 900°C for 2 min. As the SR of free surfaces after an anneal at 425°C, 600°C,and 900°C are not expected to be entirely representative of what may happen inside the memory cells, where the critical surfaces are interfaced with a SiO_2 or a TaO_x switching layer, we have passivated the surfaces of all metals with 30 nm SiO_2 layer and subjected the samples to the same anneals at 425°C for 8 min, at 600°C for 5 min, and at 900°C for 2 min. After the anneals are done, the 30 nm SiO_2 layer has been removed by a soft hydrofluoric (HF) etch, highly selective to the metals, to expose the surface of the inert metals for the subsequent AFM measurements. The results of surface roughness measurements are summarized in Table 3.3.

Several interesting observations can be drawn from Table 3.3. In general, the surface roughness of a free surface increases with increasing anneal temperature. This increase is much larger for free than for passivated surfaces. It can be seen that an anneal at 600°C or 900°C with a passivated surface, leads to a smoothing effect of the surface compared to a free metal surface. However, occasionally, some irregularities defy the general trend. For example, the surface roughness of Co annealed at 600°C is higher with passivation than without it. It is seen that at room temperature (27°C) out of the four metals the lowest surface roughness has ruthenium of 1.5 nm. The surface roughness of a free Pt surface increases moderately after the 600°C and 900°C anneals to 2.4 and 4.9 nm, respectively. When, however, Ru (Pt) is covered during the anneal with SiO_2, the surface roughness after 600°C anneal is mea-

sured to be only 1.4 nm (1.3 nm) and climbs to 2.1 nm (2.3 nm) at 900°C. Thus, the surface roughness of Ru and Pt with passivation, when annealed at 600°C, are even smaller than at 27°C. The low increase of surface roughness of Ru with temperature compared to other metals is consistent with the fact that Ru has the highest melting temperature (2334°C) of the four metals, see Table 1. The highest surface roughness of a free surface at 27°C is found for Cu and Co to be 2.7 nm and 2.3 nm, respectively. The surface roughness of Co increases to 2.8 nm after an anneal of 600°C for a free surface, but becomes very large for free surfaces annealed at 900°C yielding 14.0 nm for Co and 12 nm for Cu. One observes that with SiO_2 passivation the surface roughness increase is much more moderately and is capped at 5.0 nm for Co and by 6.5 nm for Cu. It is noted that the highest surface roughness for Cu and Co and correlates well with their low melting temperatures, Cu (1084°C) and Co(1495°C). The SR of Pt displays an intermediate behavior between Ru and Co. The SR of Pt is smaller than that of Co and Cu but is higher than that of Ru. After anneals at 425°C, 600°C, and 900°C with passivated surfaces, the SR Pt increases moderately slightly more than that of Ru. This correlates well with the melting temperature of Pt (T_m = 1770°C) and that of Ru (T_m = 2335°C). These results for surface roughness apply to thin layers deposited by EBPVD. Similar trends are expected to hold for other deposition techniques. It is known, for example, that SR of Pt films deposited by plasma-enhanced atomic layer deposition [42] is lower than that of PVD and lies usually below 1 nm. Nevertheless, because the metals are deposited by the same method where the deposition rate has been kept the same for all four metals, the surface roughness results should be indicative of their differences in material properties.

Figure 3.4 shows the AFM pictures of free surfaces of the metals at room temperature (27°C) and after an RTA anneal at 600°C for 5 min. One can see that the Ru surface is most stable of all metals, while the surface of Cu undergoes a significant reconstruction. The cases

	27°C	**F.S. 600°C 5 min**	**F.S. 900°C 2 min**	**SiO_2 425°C 8 min**	**SiO_2 600°C 5 min**	**SiO_2 900°C 2 min**
Pt	1.8	2.4	4.9	1.6	1.3	2.3
Ru	1.5	2.0	4.2	1.3	1.4	2.1
Co	2.4	2.8	14.0	7.3	5.0	2.4
Cu	2.7	4.4	12.0	4.1	3.0	6.5

Table 3.3: Surface roughness of metal surfaces in nm as a function of temperature and presence or absence of a SiO_2 passivation layer. F.S. denotes a free metal surface annealed at different temperatures. SiO_2 denotes the cases in which the metal was covered by a 30 nm SiO_2 during the anneal, and the SiO_2 was removed by a soft oxide etch after the anneal [34] ©The Electrochemical Society reproduced by permission of IOP Publishing. Chakraborty A, Al-Mamun M, Orlowski M. Impact of surface roughness and material properties of inert electrodes on the threshold voltages and their distributions of ReRAM memory cells" ECS J. Sol. St. Sci. Technol.2022;11:104007; DOI: 10.1149/2162-8777/ac9c91.

of Co and Pt lie in between, showing a strong correlation between surface roughness and the corresponding melting temperature. Thus, with the exception of Cu, the topology of the surface and surface roughness of the metals do not change appreciably. In case of Cu, however, a complete surface reconstruction is being observed. While at room temperature, the Cu surface resembles that of the inert electrode metals Pt, Ru, and Co, the Cu surface at 600°C shows the formation of large clumps or hillocks of more than 100 nm size in diameter, while the finer dendrites on those hillocks appear to have the same needle-like structure as Cu at the 27°C. The similarities extend even to the surface morphology as both surfaces for Cu and Co undergo surface reconstruction, particularly severe in the case of Cu and Co at 900°C. In Figure 3.5, the surface roughness of the metals is shown after being passivated and annealed at 600°C and 900°C with a SiO_2 passivation layer on top. Before the AFM measurement the SiO_2 layer has been removed by a soft HF etch.

At 600°C, for Cu and Co, one can see hillock formation with SR higher than that at 27°C but

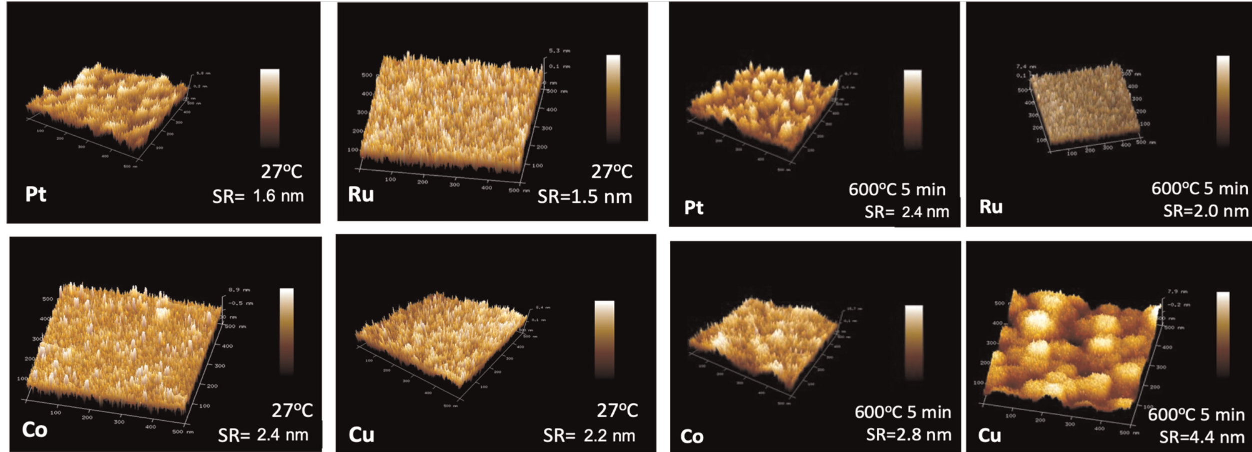

Figure 3.4: AFM pictures of free surfaces of Pt, Ru, Co, and Cu at 27°C and at annealed at 600°C for 5 min with the average surface roughness indicated [34] ©The Electrochemical Society reproduced by permission of IOP Publishing. Chakraborty A, Al-Mamun M, Orlowski M, "Impact of Surface Roughness and Material Properties of Inert Electrodes on The Threshold Voltages and Their Distributions of ReRAM Memory Cells" ECS J. Sol. St. Sci. Technol.2022;11:104007; DOI: 10.1149/2162-8777/ac9c91.

significantly smaller than that of the free surfaces annealed at the same temperatures. It can also be seen that for Ru and Pt the SR is much smaller than for free surfaces and even smaller than their SR at room temperature. Thus, with respect to the surface roughness, the metals Pt and Ru may rightfully be called inert metals with respect to the thermal properties of their surfaces. After a 900°C anneal, the topography of the Ru, Pt, and Co surfaces does not change much, and the SR increases moderately over those measured at 27°C and the anneal at 600°C. Overall, it can be concluded from Table 3.3 that a passivation layer suppresses the increase of SR with increasing temperature significantly.

We have also measured the surface roughness of the switching layers SiO_2 and TaO_x, deposited in both cases by PVD directly on oxidized Si-wafers. We obtain SR at room temperature of 0.9 and 1.0 nm, for SiO_2 and TaO_x, respectively, and annealed at 600°C the SR drops to 0.53 and 0.62 nm, respectively. The reflowing property of SiO_2 and TaO_x has a significant smoothing effect on the surface roughness of the inert electrode. Our results

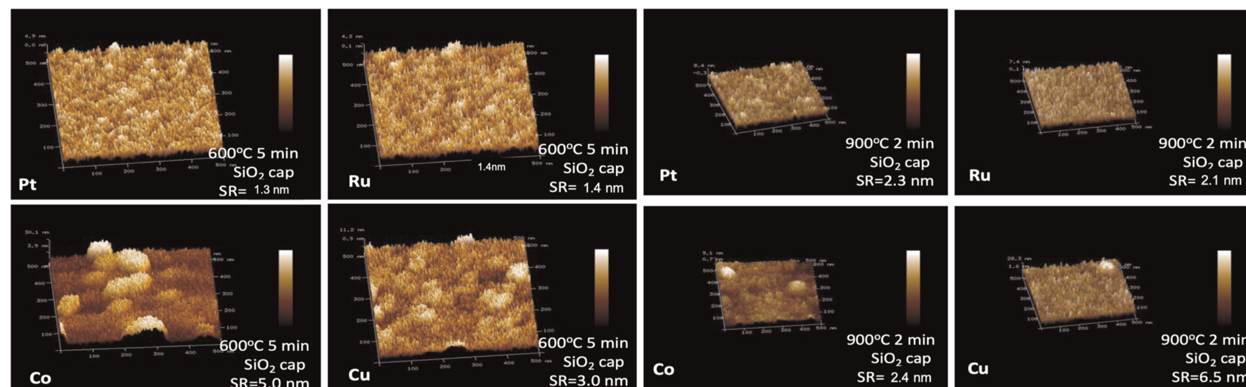

Figure 3.5: AFM pictures of passivated surfaces of Pt, Ru, Co, and Cu annealed at 600 and 900°C. Before taking AFM measurements the SiO2 passivation layer was stripped by a soft etch [34] ©The Electrochemical Society reproduced by permission of IOP Publishing. Chakraborty A, Al-Mamun M, Orlowski M. "Impact of Surface Roughness and Material Properties of Inert Electrodes on The Threshold Voltages and Their Distributions of ReRAM Memory Cells", ECS J. Sol. St. Sci. Technol.2022;11:104007; DOI: 10.1149/2162-8777/ac9c91.

confirm the findings that nanometer thin SiO_2 [43] and TaO_x [44] have much better reflow properties than their mesoscopic or bulk counterparts which need doping such as boron and/or phosphorous to lower the reflow temperature.

The reflow properties of SiO_2 and TaO_x layers have been confirmed by measurements of surface roughness of Ru covered with SiO_2, the electrolyte with the smallest native surface roughness. Even the mere deposition of SiO_2 has a smoothing effect. In case of Ru, the SR at room temperature is 1.5 nm, but when covered with PVD-SiO_2 the surface roughness of the SiO_2/Ru bilayer is only 1.2 nm. Since SR of SiO_2 deposited directly on the oxidized Si wafer is 0.9 nm, it can be seen that the composite surface roughness of the two layers is not additive and that SiO_2 exerts a smoothing effect. If the cumulative SR were additive, the SR would add up to 2.4 nm. Even more remarkably is the smoothing effect of SiO_2 at higher temperatures: the surface roughness of SiO_2 on Ru after the anneals of 250°C for 5 min, 600°C for 5 min, and 900°C for 2 min remains at a more or less constant value of 1.3 nm. This is contrasted with the surface roughness of a free Ru surface after the 900°C anneal

when the SiO_2 layer has been removed after the anneal of 2.5 nm and the SR of a free Ru surface after 900°C anneal of 4.2 nm. Thus, dielectrics such as SiO_2 or TaO_x display even stronger surface smoothing action at elevated temperatures. These results suggest a method of reducing the surface roughness of metals by depositing a thin sacrificial layer of dielectric such as TaO_x, or SiO_2 followed by an anneal at moderate temperatures such as 425°C before removing the passivation layer by a soft HF etch.

Finally, we wish to comment on how the surface roughness relates to the electric field enhancement factor, β, given in Eq. (3.3). The β enhancement factor depends largely on the curvature radius at the top of an asperity. Surface roughness, on the other hand, quantifies only the deviations of the asperities in the direction normal to the surface and does not account for the curvature radius of the tip. Nevertheless, as seen from Figure 3.4, the surface morphology of the four metals at room temperature is very similar and the respective field enhancements may still be expected to correlate well with the surface roughness as a lump parameter.

3.6 Degraded Reliability and Endurance of Cu/TaO_x/Ru Device

The major drawback of the Ru devices as compared to their Pt counterparts is their limited switching capacity. While Pt devices can be switched repeatedly back and forth for at least 220 times, Ru devices become non-resettable after several set-reset operations (usually less than 13), and sometimes even after the first set operation, when the set operation is performed at high I_{cc}. In some cases, it was even difficult to reset a high resistance Cu filament in a Ru device formed at I_{cc} as low as 5 μA. The failure of the Ru devices after a

few switching cycles is likely to be related to the specific geometric configuration of the Cu filament which may be caused either by the diminished stopping power of the Ru electrode for Cu diffusion into the Ru film or by an increased surface diffusion as compared to that for the Pt electrode.

It is well known that even in extant ReRAM devices, including Pt devices, it is difficult and sometimes impossible to reset the cell if the cell has been set at high I_{cc}. For a low I_{cc}, the shape of the CF can be approximated by a truncated cone as shown in (Figure 3.3(a)) where the bulk of the CF's resistance resides in the tip of the cone. Since during the reset, the power dissipated in the filament is equal to $I_{res}^2 \times R_{on}$, the highest temperature is reached in the constriction at the tip of the cone, where the rupturing of the filament is easy. At high I_{cc}, the Ron decreases sharply by adding Cu atoms to the upper section of the cone, rendering the filament's shape more and more cylindrical (Figure 3.3(b)). In this case, the maximum temperature, in the absence of any pronounced constriction, is reached in the middle section of the cylinder, where the low resistance filament is relatively strong. Hence, rupturing of the CF becomes difficult or impossible.

The cylindrical shape of the CF may also be obtained if the base of the cone in contact with Ru electrode erodes, see Figure 3.6. As the bottom base of the CF is reduced, while new Cu^+ ions are added from the top during the set operation, the shape of the filament will transform gradually into a cylindrical shape. There are several possible mechanisms for the erosion of the base of the filament: (i) Cu surface diffusion along the Ru interface (ii) crystallization of Ru and out-diffusion of Cu along the Ru grain boundaries, (iii) formation of Cu and Ru silicides. Those degradation mechanisms are depicted in Figure 3.6(a) and will be discussed further in Section 3.8. Whereas, with a nearly perfect stopping power, the shape of the filament in the Pt device can be assumed to remain conical with more or less sharp tip at the Cu electrode, the shape of the Cu filament in a Ru device is more

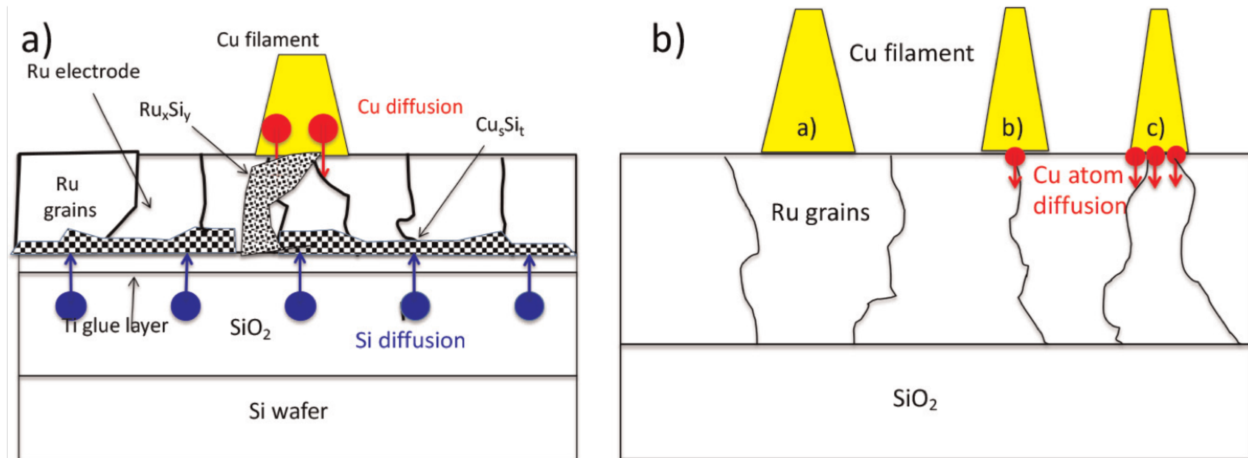

Figure 3.6: (a) Possible mechanisms of the hypothesized degradation of the Ru electrode. Elevated local temperatures in the immediate vicinity of the filament may cause Si diffusion into Ru, possibly along Ru grain boundaries and lead to Ru_xSi_y reactions. Cu may use the Ru grain boundaries as diffusion paths and may also undergo a silicidation reaction. (b) Relative location of the Cu filament with respect to the Ru grain boundaries likely to explain the large variability of performance see in Ru devices [36] ©The Electrochemical Society reproduced by permission of IOP Publishing. Al-Mamun M, King, S, Orlowski M. "Thermal and Chemical Integrity of Ru Electrode in Cu/TaO_x/ Ru ReRAM Memory Cell", ECS J. Sol. St. Technol.2019; 8: N220; DOI: 10.1149/2.0121912jss.

cylinder-like, especially, when the Ru device was self-annealed by undergoing several set-reset switching cycles. We find also a large variability of performance among Ru devices becoming noticeable after a few switching cycles. This variability may be explained by the relative location of the Cu filament with respect to the locations of the Ru grain boundaries as illustrated in Figure 3.6(b). When there is no such overlap, the cell would perform well for several switching cycles. If, however, there is an overlap of the base of the filament with one or more grain boundaries, then Cu atoms may be easily depleted from the filament via enhanced Cu diffusion along the grain boundaries. In this context, we wish to mention that in ref. [22] other related ReRAM devices, such as $Cu/TaO_x/Ti$ and $Cu/TaO_x/Ta$ have been compared to the benchmark device $Cu/TaO_x/Pt$ and were found significantly inferior to the Pt device. The Ru device is found to perform better than the Ti and Ta devices. As already mentioned, in terms of endurance Pt devices are by far best, switching over 200

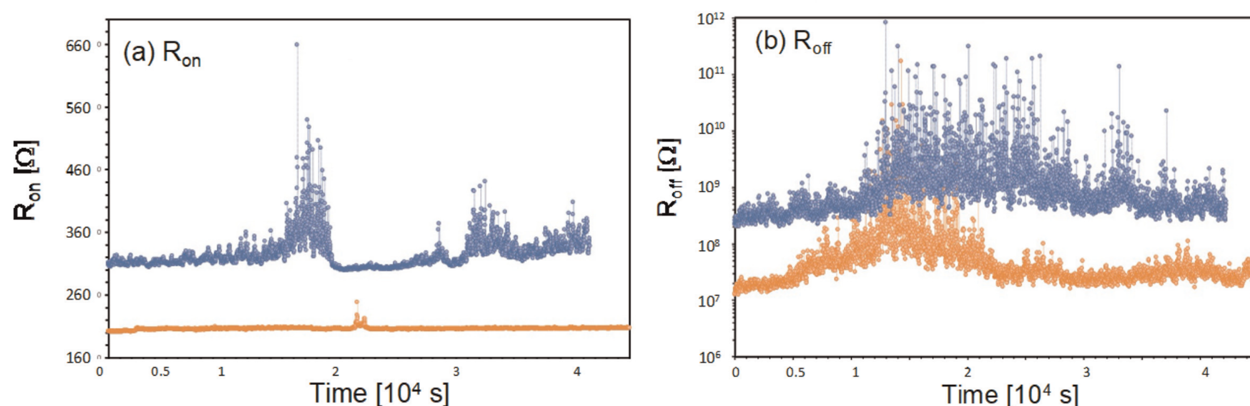

Figure 3.7: The retention of Ru and Pt devices (a) for the on-state characterized by Ron, and (b) for the off-state characterized by Roff [36] ©The Electrochemical Society reproduced by permission of IOP Publishing. Al-Mamun M, King, S, Orlowski M. “Thermal and Chemical Integrity of Ru Electrode in Cu/TaOx/Ru ReRAM Memory Cell”, ECS J. Sol. St. Technol.2019; 8: N220; DOI: 10.1149/2.0121912jss.

times, followed by Co devices that can be switched at optimum conditions up to 40 times, while Ru devices could be switched at best 13–14 times. The retention of both binary states characterized by R_{on} and R_{off} is or all three devices is good. In Figure 3.7 the retention of the on- and off-states for Ru and Pt devices is shown.

It can be seen from Figure 3.7 that the level of noise for Ru devices is higher than for Pt devices for both bit states, characterized by R_{on} and R_{off}. While R_{off} fluctuations of Ru devices are irrelevant as the outlier lie in the tens of GΩ range, the outliers for R_{on} are more of a concern, as its variation can be as high as 75%. Such large fluctuations could pose, inter alia, a problem for the multibit storage applications and for the stability of the sense amplifiers when reading the cell. For comparison the variations of R_{on} and R_{off} in Pt devices are less than 10% as discussed in more detail in ref. [36].

Before focusing on specific mechanisms that degrade the inertness properties of Ru films, we will discuss performance changes of nominally the same devices caused by their different integration scheme, called here the “embedment” aspect.

3.7 Impact of Embedment on the Performance of $Cu/TaO_x/Ru$ Devices

To study the relative degradation of $Cu/TaO_x/Ru$ vs. $Cu/TaO_x/Pt$ devices, we have manufactured two nominally identical $Cu/TaO_x/Ru$ devices (where the layers of the device proper have been processed at the same time), however embedded differently on the Si wafer as shown in Figure 3.2(b) and (c). The Ru device A has the same substrate as the Pt device, that is Ti(25 nm)/SiO_2(730 nm)/Si-wafer, while the Ru device B is manufactured on the layer stack Ti(20 nm)/TaO_x(30 nm)/SiO_2(730 nm)/Si-wafer. Thus, Ru device B has an additional TaO_x-30 nm layer inserted between SiO_2 and Ti layers as shown in Figure 3.2(b). We find that the Ru device B with the additional TaO_x layer shows much better performance (up to 37 switching cycles) than the Ru device A, at all test conditions, although to a varying degree. The degree of the improvement in the switching properties between the two embedment scenarios, depends on the amount of internal Joule's heat exposure and varies with the levels of applied compliance current and ramp rate, which control the amount of heat according to Eq. (2). The highest improvement of device B over the device A is found for $I_{cc} = 50\ \mu A$ and $rr = 0.2$ V/s (high heat dissipation), and little improvement in performance between the two devices can be observed for the condition $I_{cc} = 1\ \mu A$ and $rr = 2.0$ V/s (small heat deposition) - a regime where both devices perform the best. It is found that at $I_{cc} = 50\ \mu A$ and $rr = 0.2$ V/s the Ru device A does not display resistive switching behavior at all, i.e., the device is dysfunctional. The device A cannot be reset after the filament has been formed the very first time. However, when the reset ramp rate is increased fivefold to $rr = 1$ V/s – thus reducing the Joules heat dissipated in the device - the device A can be neither set nor, if the set operation is eventually successful, the device cannot be reset, that is, the resistive switching cell has been permanently damaged. In contrast, device B, with the additional

TaO_x, layer shows some resistive switching behavior for a few cycles (maximum 6). Hence, it can be concluded that high heating effects are detrimental to both devices. But, while Ru device B displays some, if small, degree of resistive switching behavior (5–6 switching cycles), Ru device A does not display resistive switching at all. Keeping the reset ramp rate at 0.2 V/s but now reducing the I_{cc} current from 50 μA to 1 μA, we observe improved resistive switching behavior for both devices with the frequency of the Ru devices B being twice as high (maximum 22 cycles) as for the Ru devices A (maximum 10 cycles). These results clearly demonstrate that the endurance of the device is directly related to the amount of heat deposited in the devices leading to some adverse reactions which are mitigated by the insertion of the TaO_x layer subjacent to the Ru film.

Another embedment case has been implemented when two identical devices Cu/ TaO_x/Ru have been fitted with different glue layers as shown in Figure 3.2(c) [3]. Here, the Ti glue layer for the inert electrode has been replaced with a Cr glue layer of 30 nm. It was found that the electric performance of nominally identical devices depends sensitively on the nature of the glue layer. We find that the V_{res} value for Ru/ Cr is 0.4 V larger (V_{res}(Ru/Cr) = -3.8 V) than for the Ru/Ti device (V_{res}(Ru/Ti) = -3.4 V). This could have been predicted on the grounds of four times higher thermal conductivity for Cr [94 W/m.K] than that of Ti [22 W/m.K] leading in the case of Ru/Cr to a much higher heat removal rate from the Cu CF during the reset operation, as discussed already in Section 3.4. In the case of Ru/Ti, the Joules heat generated in the filament cannot be as easily dissipated and lingers therefore for some time around the hot spot in the filament as in the case of the Ru/Cr device. Both embedment experiments suggest that the heat generated in the memory cell may trigger some kind of chemical or grain growth reactions that can be somewhat mitigated by the insertion of the TaO_x layer.

3.8 XRD Studies of Different Embedment of Ru Layers

In order to find out what kind of chemical reactions may occur in the Ru devices at various temperatures, we have manufactured among many auxiliary blanket multilayer structures on oxidized Si wafers following samples: (i) Ru(50 nm)/Si, (ii) Ru (50 nm)/SiO_2(611 nm)/Si, and (iii) Ru(50 nm)/Ti(40 nm)/TaO_x/SiO_2(611 nm)/Si that we consider here. The auxiliary samples are bound to avail some information on Ru crystallization and the presence of new materials such as silicides using the XRD technique. The XRD measurements have been performed on the three samples for three annealing conditions: (i) unannealed, that is, at 27°C, (ii) annealed at 600°C for 10 min, and (iii) annealed at 900°C for 30 min. In Figure 3.8(a), a Ru crystallization peak at 42.15° can be seen on the XRD spectra for all samples with a Ru layer at 27°C and after an anneal at 600°C, and 900°C. This is in agreement with XRD studies of similar layer systems reported in [45]. XRD signals for samples of Ru/Si at 300 K, Ru/Si after an RTP anneal at 600°C for 10 min, and for Ru/SiO_2/Si after an anneal at 600°C for 10 min are also shown in Figure 3.8(a). It is seen that a Ru_3Si_2 crystallization peak appears as a result of the 600°C anneal. An XRD signal (more of a shoulder than a peak) of ruthenium silicide Ru_2Si_3 at 44.7° is observed next to a broad Si wafer peak only after 900°C anneal as shown in Figure 3.8(a). This is in agreement with observations of Ru_2Si_3 XRD detection made in ref. [46]. We observe this peak on the following samples: Ru/Si, Ru/SiO_2/Si, Ru/Ti/SiO_2/Si, and Cu/Ru/Ti/SiO_2/Si. The strongest Ru_3Si_2 signal can be seen for the Ru/Si and Ru/SiO_2 samples. From comparison of Figure 3.8(b) with Figure 3.8(a) it, can be seen that the XRD signal at 44.7° is absent for the anneal at 600°C and also for the unannealed sample. It is seen that a Ru_3Si_2 crystallization peak appears as a result of the 600°C anneal. An XRD signal (more of a shoulder than a peak) of ruthenium silicide Ru_2Si_3 at 44.7° is observed next to a broad Si wafer peak only after 900°C anneal as shown in Figure 3.8(a). This is in agreement with observations of Ru_2Si_3 XRD detection made in

ref. [46]. We observe this peak on the following samples: Ru/ SiO_2/Si, Ru/Ti/SiO_2/Si, and Cu/Ru/Ti/SiO_2/Si. The strongest Ru_3Si_2 signal can be seen for the Ru/Si and Ru/SiO_2 samples. From comparison of Figure 3.8(b) with Figure 3.8(a) it, can be seen that the XRD signal at 44.7° is absent for the anneal at 600°C and also for the unannealed sample It is seen that a Ru_3Si_2 crystallization peak appears as a result of the 600°C anneal. The Ru_3Si_2 shoulder is either not there or very weak, as seen in Figure 3.8(b). From Figure 3.8b it is also seen that the Ru_3Si_2 peak at 41.7° disappears at 900°C, again in agreement with observations made in [45]. In layer structures of Figure 3.8(b) that have been capped with an additional Cu layer, the XRD spectra show formation of copper silicide at 44.8° only at 900°C as shown in Figure 3.9. Thus, at high temperatures Cu and Si may diffuse through Ru/Ti and Ru/Ti/TaO_x layers to undergo a copper silicide reaction.

In summary, the XRD studies have revealed formation of Ru grains, formation of two kinds of Ru silicides, Ru_2Si_3 and Ru_3Si_2, and that insertion of the TaO_x layer between SiO_2 and Ti acts as a diffusion barrier for Si and suppresses the Ru_3Si_2 reaction. The XRD study corroborates not only the difference in electrical performance between Pt and Ru device but also among the Ru devices embedded on different substrates. Considering these results, it appears that while the inertness properties of Pt and Ru are similar up to about 200°C, at elevated temperatures, Pt is by far more inert than Ru ensuring superior switching performance of the Cu/TaO_x/Pt over the Cu/TaO_x/Ru device.

3.9 Conclusions

Against the backdrop of analogously characterized Cu/TaO_x/Pt and Cu/TaO_x/Co devices, we have used electrical properties of a Cu/TaO_x/Ru ReRAM cell, to elucidate material properties of 50 nm ruthenium films. The circumstance that an electric switching operation

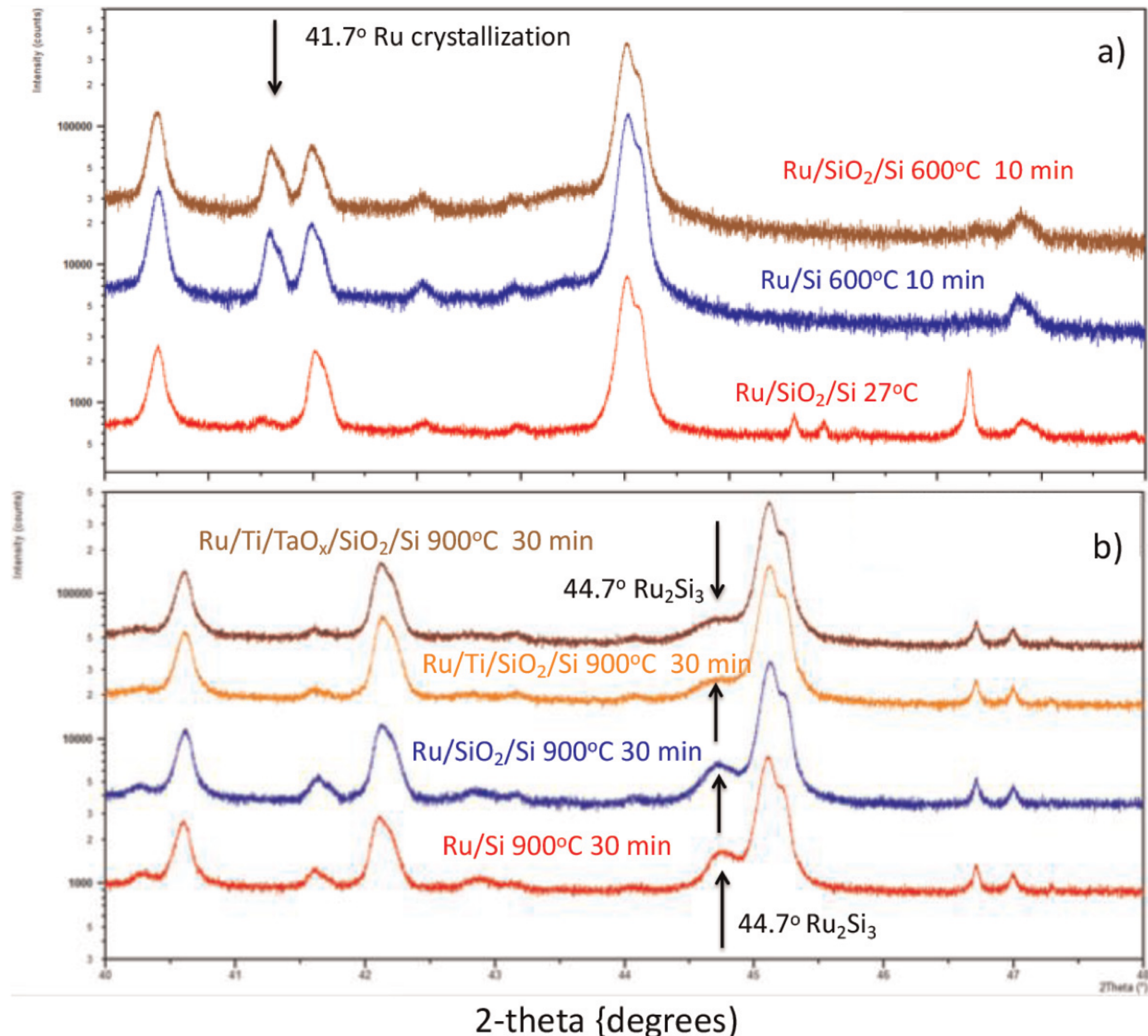

Figure 3.8: XRD spectra of (a) three-layer structures: $Ru/SiO_2/Si$ as deposited, Ru/Si and $Ru/SiO_2/Si$ after a 600°C 10 min anneal. The Ru crystallization peak has been also observed at other layer structures with a Ru layer only after a 600°C anneal. The peak is very weak at room temperature and disappears after an anneal at 900°C for 30 min. (b) Four-layer structures annealed at 900°C for 30 min: Ru/Si, $Ru/SiO_2/Si$, $Ru/Ti/SiO_2/Si$ and $Ru/Ti/TaO_x/SiO_2/Si$. On all structures a Ru_2Si_3 shoulder can be observed at 44.7°C next to a large signal 45.12°C which stems from the Si wafer as verified by XRD spectra on Si and SiO_2/Si structures [36] ©The Electrochemical Society reproduced by permission of IOP Publishing. Al-Mamun M, King, S, Orlowski M. “Thermal and Chemical Integrity of Ru Electrode in $Cu/TaO_x/Ru$ ReRAM Memory Cell”, ECS J. Sol. St. Technol.2019; 8: N220; DOI: 10.1149/2.0121912jss.

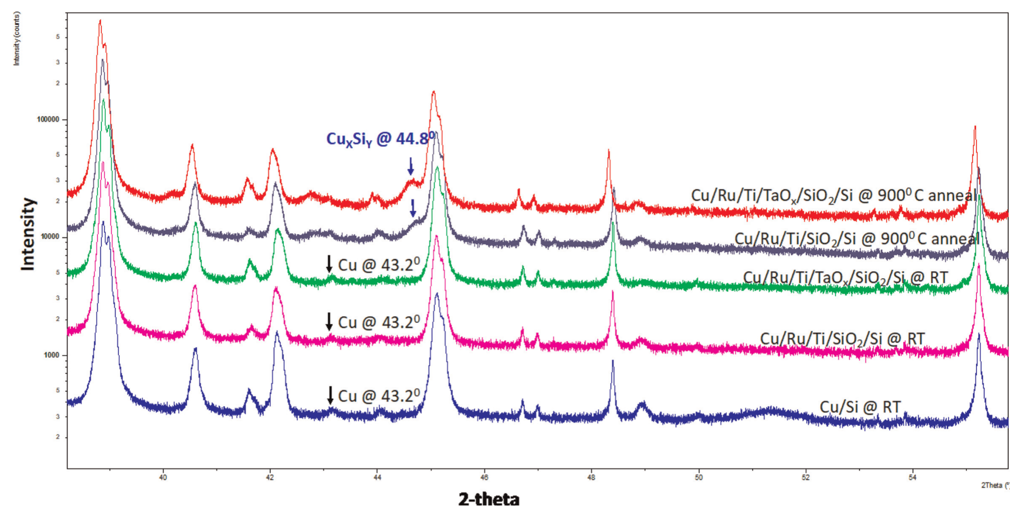

Figure 3.9: XRD spectra of the same layer structures as in Figure 8b but capped by Cu layer. A Cu silicide peak can be observed at 44.8° only after the anneal at 900°C [36] ©The Electrochemical Society reproduced by permission of IOP Publishing. Al-Mamun M, King, S, Orlowski M. "Thermal and Chemical Integrity of Ru Electrode in Cu/TaO_x/Ru ReRAM Memory Cell", ECS J. Sol. St. Technol.2019; 8: N220; DOI: 10.1149/2.0121912jss.

of a ReRAM cell allows to raise temperature of the Cu filament inside a ReRAM memory cell from 27°C up to ca. 1100°C, in a controlled way [47], turns the Cu/TaO_x/Ru device into a nano-laboratory for investigation of the material properties of Ru at different temperatures. The present electric analysis of the devices has been complemented by extensive material studies of relevant layer systems annealed at various temperatures using XRD, and by studies of the surface roughness of free and passivated metal surfaces, both unannealed as well as annealed at elevated temperatures, using AFM. From these studies, a consistent picture emerges allowing a compelling explanation of all differences of the ReRAM cell's electric characteristics in terms of the Ru material properties.

Cu/TaO_x/Ru devices compared to Cu/TaO_x/Pt devices have higher forming, set, and reset voltages. The higher V_{form} and V_{set} voltages can be partly or entirely attributed to the work function difference between Pt and Ru of 1.6 eV and partly to the significant difference in surface roughness between Pt and Ru. The higher V_{res} voltage for Ru device than for Pt

or Co devices is a consequence of much higher thermal conductivity of Ru than that of Pt and Co. It was also found that while Pt devices can be switched more than hundred times, the number of switching cycles of Ru devices is very limited. The performance deterioration of Ru devices is particularly conspicuous when the cell is exposed to high Joule's heat dissipation during the set and reset switching cycles. At low Joule's heat dissipation, the switching performance of both Ru and Pt devices is initially comparable. The Joules heat dissipation is, thus, a major factor determining the endurance properties of the device as it triggers degradation of the inertness properties of Ru caused by grain crystallization as well as silicide formation. The degraded integrity of the inert electrode appears to have a major impact on the Cu diffusional fluxes which, in turn, determine the geometrical shape of the Cu conductive filament. Additional embedment experiments have corroborated these conclusions. In an embedment experiment, an identical device proper is embedded in different ways on the Si wafer. It has been demonstrated that the electrical switching properties of nominally the same resistive switching device $Cu/TaO_x/Ru$, when embedded differently, $Cu/TaO_x/Ru/Ti/SiO_2/Si$ vs. $Cu/TaO_x/Ru/Ti/TaO_x/SiO_2/Si$, differ substantially. This is the result of chemical and structural interactions of the device proper with its immediate environment. The chemical and structural changes of Ru films are brought about by the nanometer dimension of the layers involved and triggered by Joule's heat deposition during the switching of the ReRAM cell. This finding points to a broader and critical impact of the device's embedment on its structural, material integrity, and, eventually, its electrical reliability and endurance properties. The insertion of a TaO_x layer between the SiO_2 and Ti glue layer suppresses the Ru crystallization and silicide reaction somewhat and, eo ipso, improves the electrical performance and endurance of the Ru device on the $Ti/TaO_x/SiO_2/Si$ substrate as compared to the Ru device manufactured on the Ti/ SiO_2/Si substrate. Embedment structures with different glue layers (Cr vs. Ti) have corroborated the role of thermal conductivity in determining the actual value of V_{res}. The surface roughness studies have

shown a strong impact of surface roughness on V_{form}, evidenced by the three devices. Furthermore, it turned out that the deposition of a sacrificial dielectric layer followed by an anneal leads to a drastic reduction of surface roughness of a metal.

Inert electrode	**Threshold voltages**	**Retention**	**Endurance cycling ability**	**BEOL integrability**
Ru	high (-)	(+)	<14 (-)	(++)
Pt	low (+)	(++)	>200 (++)	(-)

Table 3.4: Figure of merit comparison between Ru and Pt ReRAM device.(+) and (-) denote advantages and disadvantages, respectively.

The advantages and disadvantages of Ru over Pt devices are summed up in Table 3.4. The most important disadvantage of the Ru device is its limited switching cycling ability. This could be perhaps addressed in future work by minimizing Joule's heat exposure during the switching operations. The use of ruthenium in ReRAM cells appears to be viable if the internal temperature of the cell could be limited to temperature not exceeding ca 350°C, which puts a severe constraint on how the cells are being programmed and erased. Up to 440°C, Ru exhibits similar stopping power and inertness properties as Pt. Hence, the deployment of Ru in BEOL, where the temperature during a circuit operation does not exceed 140°C [48], appears to be viable. However, at elevated temperatures above ca 400°C, the inertness properties of Pt are vastly superior to those of Ru.

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Chapter 4

Thermal Reliability Issues in ReRAM Memory Arrays

The following chapter has been reproduced from Ref. ***Amrita Chakraborty, Mohammad S. Al-Mamun, and Marius K. Orlowski. Thermal Reliability Issues in ReRAM Memory Arrays. In Dr. Yao-Feng Chang, editor, Memristors - the Fourth Fundamental Circuit Element - Theory, Device, and Applications, Chapter 0. IntechOpen, Rijeka, 2023.*** *with minor changes.[1]*

A localized buildup of Joules heat occurs in a memory cell as a result of the switching of resistive memory (resistive random access memory, (ReRAM)) cells. In ReRAM memory crossbar architecture, heat accumulated in one cell transfers to nearby cells via shared electrode metal lines and impacts adversely the performance of the devices. The cell-to-cell heat transfer leads to reduced number of switching cycles (SWC) and, in specific circumstances, to a loss of a bit in the cell brought about by a rupturing of the nanofilament. This chapter identifies the main causes for the thermal ReRAM reliability issues, offers a detailed analysis of the intercell heat transfer, characterizes its effects on the electric behavior of cells, and describes the thermal cross-talk in terms of three key material properties: specific heat capacity, the mass given by the geometry of the

conductor material, and thermal conductivity of the electrode. By depositing several distinct composite inert electrodes, multiple ReRAM arrays have been manufactured to alter deliberately the thermal conductivity, specific heat capacity, and the electrode geometry. The proposed thermal analysis, based on those electrode properties, accurately anticipates the experimentally discovered variations in the degradation of electric output characteristics of the ReRAM devices operated under the same conditions.

4.1 Introduction

Since scaling limitations have been reached for conventional nonvolatile memory (NVM) that relies on metal-oxide-semiconductor field-effect transistors (MOSFETs) with a floating gate, it is essential to design substitute memory cells. Owing to its simple structure, strong miniaturization capacity, low power usage, high switching frequency, large ON/OFF resistance ratio, remarkable endurance, and retention features, resistive random access memory (ReRAM) is one of the leading contenders to supplant the existing NVM technology [2, 3, 4]. For neuromorphic applications, resistive memory cells are also very promising building elements [5, 6]. An authoritative review of the memristor technologies has been given recently by YF Chang [7]. The suitability of several types of nonvolatile and volatile memristive switches for neuromorphic applications has also been thoroughly reviewed [8]. The two-terminal resistive switching device, such as $Cu/TaO_x/Pt$, consists of two metal electrodes and a solid electrolyte insulating layer (in this case, TaO_x). In response to an appropriate applied electric field, the solid electrolyte film exhibits a transition between low and high states of resistance. In ReRAM devices called bipolar resistive devices, the switchover between a high resistance state (HRS), denoted by the resistance R_{off}, and a low resistance

state (LRS), denoted by the resistance R_{on}, takes place at a polarity opposite to that at which the transition between HRS and LRS occurs. The establishment and dissolution of conductive filaments (CFs) in the matrix of the insulating dielectric as a result of metal ions and charged defect electromigration as well as heat impacts account for the resistance switching effect [9]. Metallic cations of the so called active electrode (in our case, Cu) migrate in the electric field toward the second electrode, known as the inert electrode (such as Pt, Rh, Ru, and Co), where they are reduced to neutral atoms [10]. A metal nanofilament is created between the two electrodes as a result of the Cu metal atoms gradually accumulating at the interface of Pt and TaO_x. This mechanism is known as the "SET operation." The filament ruptures at a definite current I_{res} when an opposite bias is applied to the copper electrode. A relatively large current of a few milliamperes (mA) is flowing through the filament at that point, dissipating Joules heat, and thus triggering the copper atoms' out-diffusion from the body of the nanofilament. The RESET operation is the term used to describe the filament rupturing. Joule heating is essential during the RESET processes. The dominance of Joule heating in the RESET process has been thoroughly proven in several investigations [11, 12, 13, 14, 15, 16]. The R_{off}/R_{on} ratio degrades due to the self-heating effects of switching the cell, decreasing as the ambient temperature increases [17]. The computational reliability of neuromorphic computing systems based on ReRAM cells suffers noticeably from such variations in R_{on} and R_{off} of ReRAM cells [6]. In particular, a cell at higher temperature is more likely to produce an inaccurate output. ReRAM's heat stability is a separate issue for embedded memories used in automotive applications [18].

The temperature of the filament during the RESET procedure will rise, rendering the cell more unstable under the same operating conditions if the bottom electrode is thinner because less Joules heat generated in the nanofilament can be dissipated. Reference [19] provides a thorough overview of resistive switching processes. Repeated switching of a cell causes

the device to accumulate more Joules heat. It has been discovered [20, 21] that the Joules heat generated in a particular cell is preferably transferred along the copper and platinum electrodes, impacting the next cell positioned along the same electrode lines and impairing its electrical characteristics. Furthermore, it has been demonstrated [22, 23] that in case of a fragile nanofilament and enough heat delivered to it from a heated cell (HC), the nanofilament can be ruptured due to the cell-to-cell heat transfer, leading to an erasure of a programmed neighboring cell. In some other cases, a combination of the strength of the Cu nanofilament and the amount of heat transfer leads only to a temporary erasure of the bit, i.e., the ruptured filament recovers spontaneously after a few seconds of a cooling-off period [22, 23]. The objective of this research is to present a thermal methodology that explains the manifold occurrences of electric deterioration induced by thermal transport with reference to the composition, properties of the electrode material, and geometry of the electrodes.

The organization of the chapter is as follows. In Section 4.2, the fabrication process of our ReRAM devices is described. Various different composite inert electrodes have been fabricated to test the impact of thermal material properties on the thermally induced electrical degradation of the ReRAM cells. The thermal properties of the materials employed in the construction of the inert electrodes are listed in Table 4.1 and effective thermal conductivities are calculated in Table 4.2. The fundamental forming, setting, and resetting I–V characteristics are also presented and explained. In Section 4.3, we introduce the concept of a "marginal" device as a means to measure the amount of electrical degradation suffered by inactive cells subjected to remote heat transfer from the heated cell. In Section 4.4, we present thermal analysis based on material properties of the electrode material and its dimensions to predict the amount of degradation of cells subjected to thermal cross-talk. In this section, we show that approximate temperature of the heated cell and of the probed cells can be determined using our thermal analysis based on fundamental thermodynamic

Conductor	$\rho_{\mathbf{m}}$**[g/cm^3]**	$\mu_{\mathbf{th}}$**[W/mK]**	**c$_s$[J/gK]**	**k$_{th}$[cm^2/s]**	$\rho_{\mathbf{el}}$**[cm]**
Co	8.9	69	0.419	0.19	6.2×10^{-6}
Cr	7.2	94	0.460	0.28	12.5
Cu	9.0	396	0.395	1.11	1.7×10^{6}
Pt	21.7	69	0.134	0.24	10.6×10^{6}
Rh	12.4	150	0.242	0.5	4.3×10^{6}
Ru	12.4	116	0.239	0.39	7.1×10^{6}
Ti	4.5	18	0.544	0.07	42.0

Table 4.1: Material properties of the metal conductors used in the construction of the inert electrodes: mass density, ρ_m, thermal conductivity μ_{th}, specific heat capacity c_s, thermal diffusivity k_{th}, and electric resistivity ρ_{el}.

Co50 Ti30	**Cu150**	**Pt50 Ti30**	**Pt50 Cu100**	**Pt50 Cu200**	**Rh50 Cr30**	**Ru50 Ti30**	**Ru50 Cr30**
50	389	50	282	325	129	81	110

Table 4.2: Calculated effective thermal conductivity in W/(mK) of the inert composite and active electrodes investigated in this study. The thickness t_i of a material i is given in nanometers (nm). The effective thermal conductivity of two respective materials 1 and 2 is calculated as follows: $\mu_{eff} = (\mu_1 \times t_1 + \mu_2 \times t_2)/(t_1 + t_2)$.

mechanisms. We use selected cases of the manufactured composite inert electrodes to verify predictions of our thermal analysis. In Section 4.5, we summarize the main results of the chapter.

4.2 ReRAM Device Fabrication

Resistive random access memory devices are typically arrayed in a crossbar architecture at the junction of two parallel metal electrode lines, as shown in Figure 4.1(b). The cross-sections of our reference memory cell Cu/TaO_x/Pt and of the ReRAM devices derived from

the base line device are illustrated in Figure 4.2. The devices have been manufactured on silicon wafer [4] covered with a silicon dioxide (SiO2) layer that was 730 nm thick. One observes from Figure 4.2 that the inert electrode's design is the only difference between the seven various devices investigated here. Cu(100 nm, 150 nm, and 200 nm), Co(50 nm), Cr(30 nm), Pt(51 nm), Rh(51 nm), and Ti(28 nm) layers have been deposited by physical vapor deposition (PVD) using a Kurt Lesker electron-beam physical vapor deposition (EBPVD) equipment, and have been patterned using lift-off technology using photoresist with a thickness of 2 μm. Between Pt, Ru, Rh, Co, and SiO2, a thin Cr or Ti glue film of 30 nm was utilized to increase the adherence of the inert electrode proper layer and to also modify the thermal characteristics of the inert electrode composed of several materials (composite electrode). TaOx dielectric has a thickness of 25 nm. To deposit TaOx film, Ta2O5 pellets have been evaporated by electron beam in the evaporation chamber with oxygen-deficient atmosphere, resulting in oxygen-deficient TaO_x ($x \sim 1.9$). The rectangular device regions of the device are between (5 and 35) $\times$ (5 and 35) μm^2, depending on the metal line width, which ranges between 5 and 35 μm. The square dimension of the contact pads is 100 μm on the side, and the neighboring line pitch is 150 μm, as indicated in Figure 4.1(b). The memory cells employed in this study are thoroughly detailed in [22, 24, 25]. At room temperature, the I–V characteristics were carried out on a probe station with a Keithley 4200-SCS Semiconductor Parameter Analyzer. Keithley equipment lets one select the voltage step height to define the ramp rate, and it chooses the appropriate time step automatically. A ramp rate of 0.276 V/s is a result of a ratio of step height of 0.025 V and a time step of 91 ms, which is internally set by the Keithley analyzer.

Cu^+ ions are produced when a positive bias is provided to the top copper electrode in accordance with the redox reaction, $Cu \leftrightarrow e^+ + Cu^+$, and move into the body of TaO_x dielectric in the electric field to be reduced electrochemically at the surface of the Co, Pt,

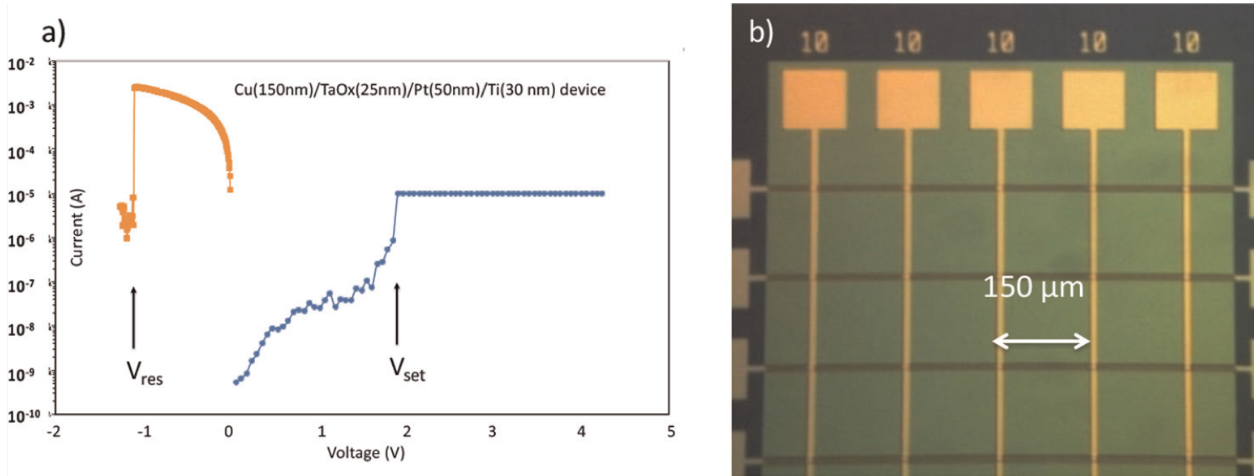

Figure 4.1: (a) An example of a SET and RESET operation of the Cu/TaO_x/Pt device with I_{cc} = 10 μA. (b) Photomicrograph of the crossline arrangement of the Cu/TaO_x/Pt, Cu/TaO_x/Ru, and Cu/TaO_x/Co devices.

a) 150 nm Cu / 25 nm TaO_x / 50 nm Pt / 30 nm Ti / 730 nm SiO_2 / Si wafer

b) 50 nm Pt / 30 nm Ti

c) 50 nm Pt / 100 nm Cu / 30 nm Ti

d) 50 nm Pt / 200 nm Cu / 30 nm Ti

e) 50 nm Ru / 30 nm Ti

f) 50 nm Co / 30 nm Ti

g) 50 nm Ru / 30 nm Cr

h) 50 nm Rh / 30 nm Cr

Figure 4.2: Resistive random access memory (ReRAM) arrays with different composite inert (bottom) electrodes that have been assembled, characterized, and analyzed in this work. All devices have the same TaOx switching film and the same active (top) Cu electrode, 150 nm thick. (a) The figure shows our baseline ReRAM device Cu/TaOx/Pt/Ti, (b) composite inert Pt/Ti electrode of the baseline device, and (c)–(h) various composite inert electrodes designed to modulate thermal properties of the electrode materials listed in Table 4.2. The thicknesses of the respective layers are also indicated.

Rh, or Ru counter-electrode, which serves, at the same time, as a reliable diffusion barrier for copper atoms. The copper atom dendrites on the inert electrode expand toward the Cu electrode as more and more Cu atoms gather, and a conductive filament (CF) made of copper atoms acting as building elements creates an electrically conductive channel from the inert Pt to the active Cu electrode. At a threshold voltage V_{set}, when the growing Cu CF makes contact with the Cu electrode, conductance abruptly starts to increase. During the RESET procedure, by applying a negative voltage to the copper electrode while grounding Pt electrode, the filament can be disrupted and the cell's resistance reverts to the HRS. At a threshold voltage, V_{reset}, the filament ruptures abruptly causing an abrupt drop of current in the I–V characteristic.

Figure 4.1(a) displays common I-V characteristics for RESET and SET operations. To ensure that the cell capacitor is completely depleted, the two grounded probe needles are put on the cell contacts for tens of seconds before any measurement is performed. The voltage of the Cu electrode is then ramped for the SET operation at a ramp rate (RR) in the interval [0.005 V/s to 3.00 V/s]. To prevent damage to the device, a limiting current, the so-called compliance current (I_{cc}) between 5 μA and 1 mA, is applied during the SET operation.

Table 4.1 lists the key physical properties of the electrode metals used during the manufacture of the devices and their inert electrodes are illustrated in Figure 4.2. In case of composite electrodes, such as the Pt/Cu electrode, the effective thermal conductivity is determined as an average of the weighted respective layer thicknesses that have been deposited. The resistance Ron of the LRS can be determined by the application of I_{cc} via equation (4.1):

$$R_{on} = C/I_{cc}^{n} \tag{4.1}$$

where C comes to a value of C = 0.29 V for $n \cong 1$ as extracted from experiments on the

$Cu/TaO_x/Pt$ devices. When n is unity, the constant C signifies the lowest voltage possible under which the device can be switched to the ON state, as demonstrated in [3]. This has been verified by delivering a constant bias to a cell to reset it while observing the time dependence of the current [3]. The cell may be switched to a conductive or ON-state for any voltage exceeding 0.286 V, but for voltages less than 0.286 V, the cell remains in the nonconductive state, i.e., OFF-state, even when the constant voltage is maintained for an extended time period. The relationship between R_{on} and I_{cc} enables the formation of both strong, low resistive, $R_{on} = 500\ \Omega$, at $I_{cc} = 0.2$ mA, and weak, highly resistive, $R_{on} = 50\ k\Omega$, Cu filaments at $I_{cc} = 5\ \mu$ A. The excellent retention and endurance of the $Cu/TaO_x/Pt$-type devices have been extensively discussed in [26].

The filament either does not develop at all for compliance current values below 5 μA or it becomes volatile and ruptures spontaneously without being stressed. Contrarily, cells with strong low-resistance Cu filaments are more likely to become inoperable when $I_{cc} > 0.25$ mA, indicating that the device has been permanently damaged and became non-resettable.

In this study, we are interested in the study of cells that, as shown in Figure 4.3, are connected to the heated device by a thermal conductance channel and have been placed into a LRS condition under predetermined levels of compliance current, I_{cc}, before the transfer of heat from the heated cell (HC) to the probed cell is being applied.

A repeated switching of a device results in the dissipation of Joules heat in that device, which can disperse to nearby devices placed along one of the metal lines common with the heated device, as further explained in [9, 21]. As long as the other array cells are switched to the conductive state, where the Cu nanofilament acts as a conductor for the heat transfer, even those devices that do not share any of the two electrode lines with the heated device may be impacted by the cell-to-cell heat transfer as well. Depending on the heat generated in the heated device, the kind of common electrode selected (Cu or Pt), and the distance

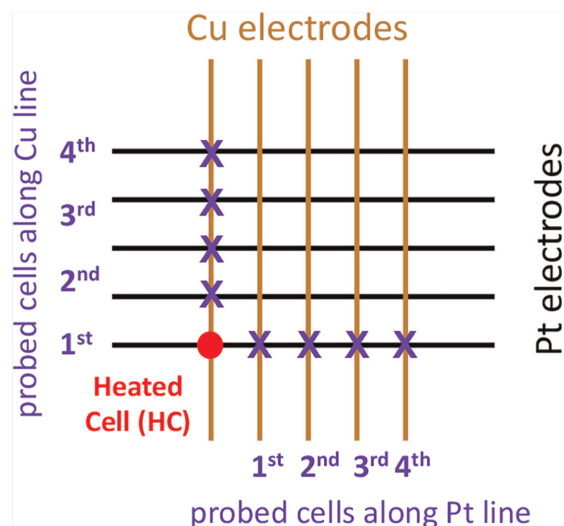

Figure 4.3: A schematic resistive random access memory (ReRAM) crossbar array shown for the baseline device. The cell marked by the red dot represents the heated cell (HC). The neighboring devices impacted by the heated cell are positioned alongside the Pt and Cu metal lines and marked by blue crosses. The neighboring probed cells are set prior to heating by the cell HC to an ON-state. Immediately after the heating by the HC cell comes to an end, the neighboring cells are checked to determine the corresponding maximum switching cycle (SWC).

between the probed and the heated device, this phenomenon permits to heat a neighboring cell in a controlled gradual way (see Figure 4.3).

The maximum temperature of the filament, according to Sun et al. [27], lies between 600°C and 900°C. The majority of the models published in the literature consider the mesoscopic electrodes to be a constant heat sink condition fixed at ambient temperature. Our findings completely disprove this presumption. Heat transfer between the array's cells is made possible by the electrode lines' significant heating. Joules heat in metallic nanofilaments with various wire cross-sections has been investigated by Fangohr et al. [28] who discovered that the temperature at the constriction can reach the high temperature of 1336 K. By using infrared (IR) detection, Uenuma et al. [29] observed a hot spot on the surface of the top electrode indicating the position of the nanofilament and estimated the temperature of the spot to lie well above 900°C. Sato et al. [30] calculated that the temperature of filaments

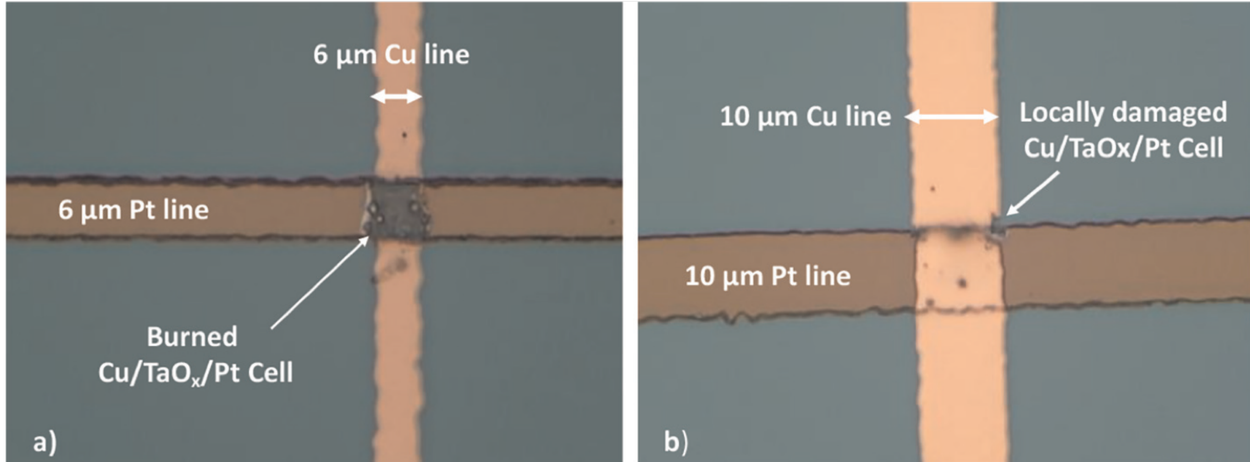

Figure 4.4: Damage to the Cu/TaO_x/Pt cells due to excessive heating. Both cells have been set and reset under the same conditions (i.e., the same voltage ramp rate and the same I_{cc} during the SET operation). (a) The cell on 6 μm Cu and Pt lines shows complete melting of Cu over the cell after three RESET-SET cycles. (b) The cell on 10 μm Cu and Pt lines shows local melting of Cu along the Pt lines after six RESET-SET cycles. After the damage is shown, both cells became inoperable.

with radii ranging between 10 nm and 40 nm will result in a 1000–1200°C temperature interval, depending on the filament's resistance. There exists, therefore, broad agreement that when the device is switched back and forth at a high frequency of SET-RESET cycles, the maximum temperature of the filament can readily surpass 900°C. In Ref. [31], it has been experimentally observed that frequent switching of a ReRAM cell leads to the incipient melting of the Cu electrodes including Cu pads. This gives a definite reference point for the local temperature of 1085°C, which is the melting temperature of copper. In Figure 4.4(a), it can be seen that the entire segment of the Cu electrode of a 6 μm wide device has been removed after three RESET cycles performed under the same bias conditions. Figure 4.4(b) shows the result of an irretrievably damaged cell after six identical RESET cycles as before for a 10 μm Cu and Pt line. We will discuss the impact of the line width on the cell temperature and severity of melting in Section 4 in more detail. Here, we wish to point out that from Figure 4.4(b) it can be seen that the location of local melting is visible on the perimeter of

the cell along the Pt electrode's edge, a preferable location of the nanofilament, where the TaO_x coverage is slightly less than on the planar surfaces, which is an intrinsic property of limited conformality of the EBPVD deposition. The Cu electrode above the cell is damaged by electromigration, which is triggered by current crowding at the nm-sized region where the Cu nanofilament makes contact with the Cu electrode. As a result, electromigration depletes the Cu atoms at this interface. The extremely high current densities and Joule heating that raise temperatures to the melting point of copper exacerbate this phenomenon, which is similar to the effects of electromigration in vias and contact holes.

4.3 Effects of Thermal Cell-to-Cell Cross-talk in ReRAM Arrays

N RESET-SET cycles were applied to heat the cell incrementally, in well-defined quanta of heat. It should be observed that compared to the RESET cycle, the heat dissipation during a SET cycle is extremely low and negligible. At the beginning of the voltage ramp, the current is less than 1 nA during the SET operation until V_set is reached, and then does not exceed the I_{cc} limit of less than 100 μA when threshold voltage V_set is surpassed. However, the current flowing through the device, when it is reset, is in the range of a few milliamperes (mA), i.e., at least more than two orders of magnitude higher. As a result, heating primarily occurs during RESET operations, and, therefore, resembles a triangular-shaped heat pulse with a pulse duration of several seconds given by $t_{res} = V_{res}/RR$ and pulse periods of 40–60 s, which correspond to the time needed to reposition the probe needles of the probe station between the application of changing bias conditions from RESET to SET. This indicates that when the cell gets heated up during the RESET operation, there follows a relatively lengthy cool-off period of about 40 s. As a result, the heating's duty cycle is less than about

0.05. The cell and the entire cell array will partially cool during the off-pulse period as a result of attending Newtonian heat losses. Only a portion of the heat deposited is kept in the cell, and this portion is described by the factor f_{loss}. As a consequence, it takes several cycles for the device to build up enough heat to achieve a target temperature in the cell. The number (N) of RESET-SET cycles, the magnitude of the voltage ramp rate (RR) applied, and the ON-resistance, R_{on} resistance of the nanofilament, can all be employed to modulate the amount of Joule heating generated at the heated memory device.

The electrical characteristics of a virgin cell have been found to be impaired when a neighboring device has been heated by the application of multiple RESET-SET cycles. This was found when all memory devices joined by a thermal path to the heated device were electrically characterized later. It has been observed that the electrical reliability of the neighboring device degrades significantly when subjected to this kind of remote heating. However, when the affected probed neighboring cell was examined again after 3–5 min or a longer cool-off time, this deterioration of electrical characteristics disappeared. We assume that after a period of time in the order of 2–5 min, the thermally induced degradation abates gradually. During the electric testing of the neighboring cells, we made sure beforehand that there exist no sneak pathways [32].

To measure the impact of the cell-to-cell heat transfer talk [20, 21] on neighboring cells, we have established the concept of a "marginal" memory cell as a convenient metric. Cell's property of displaying only a very small number of RESET-SET cycles is what we mean when we say that a cell is "marginal": We have configured a neighboring cell with an I_{cc} of just 10 μA and a voltage ramp rate of RR = 1.1 V/s to form a weak filament in the cell.

After specific number of consecutive RESET-SET switching cycles, such cell set at Icc = 10 μA turns volatile. RESET events that occur on their own, i.e., without any external bias, are one example of cell's volatility. When the cell's on-resistance Ron is adjusted at higher

and lower I_{cc}, the nature of marginality of the memory cell is further elucidated. The device cannot hold the LRS when I_{cc} = 7 μA is imposed on the SET operation. A nanofilament set at such low I_{cc} ruptures spontaneously. The ON state remains stable when the device is placed at higher level of I_{cc}, such as 10 μA, but even here only for a very limited number of consecutive SWC, usually 11–13, depending on the specific cell. When this number of SWC is reached, the cell's electrical performance turns erratic. To firm up this metric, 100 cells with an I_{cc} of 10 μA were tested, and the maximum number, M_x, of consecutive switching RESET-SET cycles was registered. We find that average maximum number of SWC is M_x = 12.7 cycles, with a standard deviation of =1.3 for such "marginal" cells.

To allow for a lengthy heating period during the RESET procedure, a low RR = 0.1 V/s has been selected. Because at low RR, the high reset current persists for a prolonged period of time, low RR allows for large deposition of heat in the cell. It has been demonstrated in [33] that the reset voltage V_{res} decreases as the voltage ramp rate, RR, decreases, according to $V_{res} \sim \sqrt[3]{RR}$. When the maximum number of SWC, (M_x), for the cell has been reached, the cell's performance becomes extremely unstable.

In contrast to the "marginal" cell, a cell set into the ON-state at high I_{cc} = 40–100 μA is very stable and may be switched very frequently (hundreds of times and more). In summary, a "marginal" memory cell marks the boundary line between the cell's volatile and stable switching performance. As a result, our "marginal' device with a filament formed at I_{cc} value of 10 μA, and allowing for at most M_x, of RESET-SET SWC, serves as the indicator for determining the severity of the cell-to-cell heat transfer.

It has been found consistently that such a marginal cell is very sensitive to the amount of heat being transferred between the cells. Any significant heat transfer is bound to reduce the maximum number M_x = 13 to a lower value, which serves then as the indicator of the degradation of electrical performance. As a result, the onset of the device's instability in

response to its local temperature is mirrored in the metric M_x. As a consequence of the heating by the neighboring cell, the heat dissipated locally by the cell's intrinsic switching is building on the heat provided by a remote source. The time it takes to change the contact needles on the probe station is approximately 50s in our experimental setup between the point at which the heat cell's heating is stopped and the probed cell's characterization begins.

The M_x for a remotely preheated cell is compared to the M_x of the same cell in the absence of remote heating, i.e., unstressed cell, to establish then the degradation metric defined as follows:

$$DEG = \frac{M_x(unstressed\ cell) - M_x(preheated\ cell)}{M_x(unstressed\ cell)} \tag{4.2}$$

As previously indicated, it has been discovered that the average M_x for a cell without remote heating (unstressed cell) is about 13 RESET-SET cycles. Based on 125 devices evaluated, the results of cell's deterioration of switching ability for devices positioned along the Cu and Pt electrode lines are displayed in Table 4.3 for four different devices with different inert electrodes. The maximum SWC are then used to determine the degree of degradation suffered by the cells due to the remote heating.

As seen in Table 4.3, for device 1 (our baseline and reference device), Cu(150 nm)/TaO_x/Pt(50 nm)/Ti(30 nm), 10 μm wide line, the deterioration of SWC for the first neighbor along the Pt line is approximately DEG = 67%. The fourth device, also attached to the Pt electrode, has a substantially reduced rate of degradation (DEG = 13%). The amount of thermal cross-talk depends on the distance in units of 150 μm between the heated and probed cells, or n$\times$ 150 μm, where n = 1, 2, 3, and 4 stand for the first, second, third, and fourth adjacent cells, respectively, as shown in Figure 4.3.

As seen from Table 4.3, for the device 1, the degradation of the adjoining cells positioned

	1. Cu(150 nm)/TaOx/Pt(50 nm)/Ti(30 nm)Next neighbors to the heat cell along Cu(150 nm) 10 m wide line				1. Cu(150 nm)/TaOx/Pt(50 nm)/Ti(30 nm)Next neighbors to the heat cell along Pt(50 nm) 10 m wide line			
prob. Cell#	I	II	III	IV	I	II	III	IV
M_x	2.6	3.3	3.9	4.3	4.8	6.1	7.8	11.3
DEG [%]	80	75	70	67	67	53	40	13
	2. Cu(150 nm)/TaOx/Pt(50 nm)/Cu(100 nm) Next neighbors to the heat cell along Cu(150 nm) 10 m wide line				2. Cu(150 nm)/TaOx/Pt(50 nm)/Cu(100 nm) Next neighbors to the heat cell along Pt(50 nm)/Cu (100 nm) 10 m wide line			
prob. Cell#	I	II	III	IV	I	II	III	IV
M_x	2.6	3.3	3.9	4.3	4.8	6.1	7.8	11.3
DEG [%]	57	41	0	0	23	1	0	0
	3. Cu(150 nm)/TaOx/Pt(50 nm)/Cu(200 nm) Next neighbors to the heat cell along Cu(150 nm) 10 m wide line				3. Cu(150 nm)/TaOx/Pt(50 nm)/Cu(200 nm) Next neighbors to the heat cell along Pt(50 nm)/Cu (200 nm) 10 m wide line) 10 m wide line			
prob. Cell#	I	II	III	IV	I	II	III	IV
M_x	2.6	3.3	3.9	4.3	4.8	6.1	7.8	11.3
DEG [%]	11	0	0	0	0	0	0	0
	4. Cu(150 nm)/TaOx/Pt(50 nm)/Ti(30 nm) Next neighbors to the heat cell along Cu(150 nm) 35 m wide line				4. Cu(150 nm)/TaOx/Pt(50 nm)/Ti(30 nm) Next neighbors to the heat cell along Pt(50 nm) 35 m wide line			
prob. Cell#	I	II	III	IV	I	II	III	IV
M_x	2.6	3.3	3.9	4.3	4.8	6.1	7.8	11.3
DEG [%]	65	52	40	33	43	31	19	0

Table 4.3: The average maximum number of RESET-SET switching cycles (SWC) and the amount of electrical degradation of neighboring devices alongside Cu and Pt electrode lines exposed to the remote heating by the heated cell for four different devices with different inert composite electrodes: 1. Pt(50 nm)/Ti(30 nm), 10 μm wide line, 2. Pt (50 nm)/Cu(100 nm), 10 μm wide line, 3. Pt(50 nm)/Cu(200 nm), 10 μm wide line, and 4. Pt(50 nm)/Ti (30 nm), 35 μm wide line.

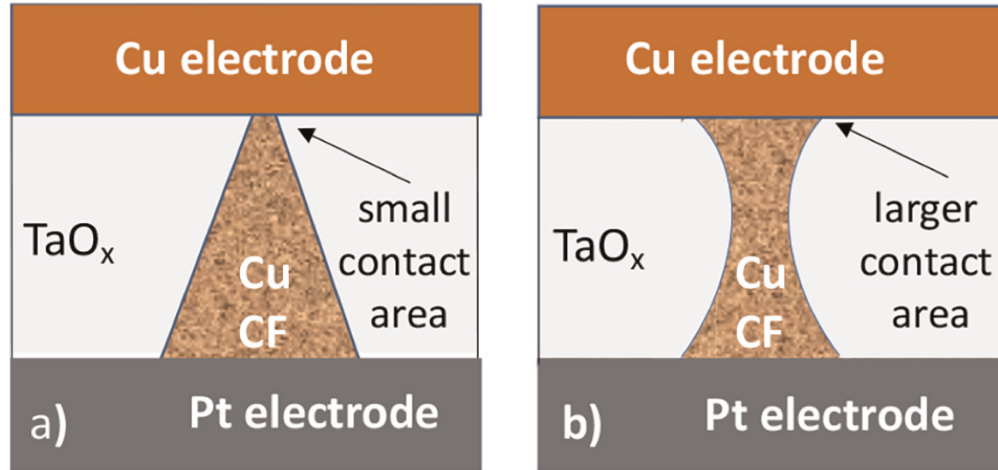

Figure 4.5: Hypothesized geometrical shapes of the Cu conductive nanofilament. (a) A truncated cone conventionally assumed with a small contact area with the Cu electrode. (b) An hour glass silhouette providing larger contact area with the Cu electrode.

alongside the Pt electrode is far less severe than that of the corresponding cells disposed alongside the Cu metal line, as extensively detailed in [21]. For example, the first neighbor along the Cu line to the heated cell suffers a degradation of 80% compared to 67% for first neighbor alongside the Pt line. At first, this result was unexpected to learn that the deterioration along the platinum metal line is less severe than that along the copper metal line [21], as one could anticipate that the geometry of the filament, due to its genesis, should have a larger contact footprint with the Pt electrode and a small contact footprint of the top part of the Cu CF with the copper electrode. Because of the above observation, one is forced to revise the hypothesized configuration of the filament from a truncated cone to something resembling more of an hour glass silhouette, which would exhibit similar size contact areas with Cu and Pt metal lines as shown in Figure 4.5. Given that it now has a larger contact area with the Cu electrode, the hourglass-shaped filament would more accurately represent our data. Consequently, it would be easier to understand why there is such a significant heat transfer from the filament along the Cu electrode line to the nearby cells along the Cu electrode. Apparently, the substantially higher cell-to-cell heat transport

along the copper electrode than alongside the platinum metal line is the root cause for the more severe deterioration in electrical performance of the cells positioned along the copper metal line.

From the heat conduction transport mechanisms, it is known that the product of the electrode's cross-section and its thermal conductivity determines the rate of heat transmission. The rectangular cross-section of the Pt/Ti electrode is two-and-one-half times smaller than that of the copper electrode, and the thermal resistivity of copper is about eight times smaller than that of weighted thermal resistivity of the composite Pt/Ti (see Table 4.2). As a result, Cu electrode's rate of heat transmission is in excess of 20 times that for the heat transfer rate for the platinum electrode. Hence, the adjacent cells positioned on the Cu electrode reach higher temperatures than the corresponding cells disposed along the platinum metal line.

4.4 Prediction and Verification of ReRAM Devices' Electric Degradation

The amount of I_{cc}, the number of consecutive RESET-SET SWC, N, and the rate at which the voltage ramps up during the RESET cycles, RR, can all affect how hot the heated cell (HC) (see Figure 4.3) becomes. For the RESET operation, a low RR = 0.1 V/s and/or a high I_{cc} that results in a strong low resistance Cu CF may be chosen to enhance heating by allowing for a lengthy heating period before the threshold voltage V_{res} is reached. Low ramp rate maximizes the cell heating because the current persists for a long time during the RESET operation until it reaches the critical value I_{res}. Eq. (4.3) [33, 34] can be used to compute the Joules heat (JH) dissipated in a device when an increasing voltage bias with a

constant voltage ramp rate is applied, and where the relationship between R_{on} vs. I_{cc} given in Eq. (4.1) is used to derive the final expression for JH.

$$JH = \int_0^{t_{res}} \frac{V^2(t)}{R_{on}} dt = \int_0^{V_{res}/RR} \frac{RR^2 \times t^2}{R_{on}} dt = \frac{V_{res}^3 \times I_{cc}}{3 \times RR \times C} \tag{4.3}$$

Here, $t_{res} = V_{res}/RR$ [33, 34] determines the time of voltage ramp rate application to effect the rupture. JH can range from 3 to 60 μJ depending on the I_{cc} and RR parameters that are used. The experimental values for R_{on} and V_{res}, and the applied voltage ramp rate, RR, solely determine the amount of JH, which is the energy that is being dissipated in the memory cell during the RESET action. The nanofilament, which is characterized by the ON-resistance R_{on}, and completely embedded in the dielectric, is the main source of heat generation. How the generated heat is being stored is a concern to which we advert now. Material's temperature as a result of the heat transfer rises according to Eq. (4.4):

$$Q = \Delta T \times c_s \times m \tag{4.4}$$

where the total mass $m = V \times \rho_m$. The energy that was dissipated within the memory array, JH, is determined by the experimental values for R_{on} and V_{res} and by the applied voltage ramp rate (RR). Eq. (4.4) shows, among other things, that the volume of the electrode affects how much the temperature difference ΔT increases. To calculate ΔT, one must determine the total mass of the electrode, which is determined by the product of the mass density ρ_m of the electrode material and by the electrode's total volume V (V = width$\times$ length$\times$ thickness) including also the contact pads' volume at both ends of the electrode. Evidently, the electrode's temperature increase ΔT is inversely correlated with both the thickness and the width of the electrode. As a result, the geometry, or the electrode's volume, controls how much the temperature may rise by ΔT. For the time being, let us suppose that the entire

amount of heat JH produced by the filament is held in the Cu conductive filament. The question of what temperature difference ΔT would be required to hold a heat of 10 μJ in a Cu CF then arises. It requires estimation of the mass density, specific heat, and volume of the Cu NF in order to be answered. The volume of the nanofilament equals 4.6×10^{-18}cm^3 if we assume that the nanofilament has the shape of a truncated cone with a radius of 9 nm at the base, 4.5 nm at the top, and 25 nm height (a calculation for an hourglass-shaped CF would be similar), which is limited by the thickness of TaO_x [35]. If the electrical resistivity of the Cu CF is assumed to be $\rho_{el} = 5 \times 10^{-4}$ Ω cm, which is around 20 times greater than that of bulk Cu, then this volume results in a R_{on} resistance of about 1000 Ω. At $I_{cc} = 10\mu$A, such a Ron value is in fact experimentally observed. Here, the resistivity of the Cu filament has to be larger than that of bulk copper, since CF consists of Cu atoms embedded in the matrix of TaO_x. Given that Ta_2O_5 has a mass density of 8.2 g/cm^3 and that of Cu is 9.0 g/cm^3, the filament's mass density must fall between the two values. If it does, then the total mass of Cu CF is about 4×10^{-17} g. Furthermore, the specific heat capacity of copper filament must fall between that of Ta_2O_5 of about 750 J/(gK) and Cu's 0.385 J/(gK). One may determine the temperature differential ΔT required to store such energy within the nanofilament alone using Eq. (4.4) and the extreme case of 750 J/(gK). Under these circumstances, the temperature differential from the ambient temperature is at least 3×10^8 K, which is 20-fold higher than the core temperature of the sun of 1.5×10^7 K. The temperature would be even higher (3×10^{11} K) if the specific heat capacity was at its other extreme, cs (Cu-CF) = 0.385 J/(gK). This is obviously impossible, and given the filament's incredibly small volume, it is evident that this amount of energy cannot be accommodated by the filament. Instead, the heat must be partially dissipated and partially stored, through the primary conductive heat transfer mechanism, at least in the two electrodes (Cu and Pt), and in the body of the nanofilament with its negligible contribution to the overall volume. Additionally, a significant portion of the energy conductively transferred to the electrodes will

be lost owing to Newtonian heat losses, such as buoyancy-driven convection and radiation, all the more as the metal lines display a relatively large surface-to-volume ratio [36]. Therefore, it is reasonable to suppose that only a small portion of JH will be accommodated in the body of the electrode over the course of a more or less continuous heating session during the reset procedure, or $\mathrm{Q_{st}} = JH \times \mathrm{f_{loss}}$, where $\mathrm{f_{loss}}$ signifies a portion of the heat still present in the material after the losses of heat to the environment. The relationship between the coefficient floss and the ambient temperature is $\mathrm{f_{loss}} \approx exp(-r\mathrm{t_{diss}})$, where r denotes the coefficient of heat transfer and tdiss the dissipation time [37]. The remnant heat, $\mathrm{Q_{Nst}}$, after considering the losses to the environment ($\mathrm{f_{loss}}$) and amount of cooling off ($\mathrm{f_{diss}}$) between the switching operations stored in the electrodes when a memory cell is quickly switched to and from N times is given then by Eq. (4.5).

$$Q_{Nst} = N \times Q_{st} \times f_{diss} = N \times Q_{JH} \times f_{loss} \times f_{diss} = c_s \times m \times \Delta T \tag{4.5}$$

where $\mathrm{f_{diss}}$ is a coefficient smaller than unity and reflects the heat dissipation time between SWC and accounts for both the heat loss that occurs when heat is transferred between heated and probed neighboring cells during the set operation as well as the cooling period between the set operation when no substantial current flows until $\mathrm{V_{set}}$ is reached or very little current flows when the bias exceeds $\mathrm{V_{set}}$ but is still limited by $\mathrm{I_{cc}}$. The mass of the two electrodes joined by the filament is now reflected in the mass parameter in Eqs.(4.4) and (4.5). To make practical use of Eq.(4.5), we avail ourselves of a valuable experimental reference [31] that can be used to calibrate Eq.(4.5). When a cell is repeatedly switched on and off under specific switching conditions for moderately large Ron and low value for RR, which were purposefully designed to increase the amount of heating, we witness melting of the copper electrode at the heated device that extends to the metal line pads [31]. It has also been noticed that the contact pads for the Pt electrodes are free of any visible distortion of

their square shape on account of much higher melting temperature of Pt (1768°C) than that of Cu (1085°C). The reflowing of the Cu electrode has been observed after 25 SWC for a cell whose heat dissipation according to Eq.(4.3) is JH = 40 μJ based on the values utilized for RR, as well as experimental values for Ron and Vres. Using c_s = 0.385 J/(gK), for Cu and c_s = 0.13 J/(gK) for Pt, respectively, we can compute the product $f_{loss} \times f_{diss}$ from Eq.(4.5) and arrive at $f_{loss} \times f_{diss} = 0.063$.

With this knowledge, it is now possible to determine the average temperature rise in the CF-electrode system utilized in the tests described in Table 4.1 after a single switching cycle, where one reset cycle has JH = 10 μJ. Since the contact pads are square in shape with 100 nm on the side, we can repeat the calculation using Eq. (4.4) and determine the T for the specific heat capacities of the Cu and Pt electrodes, c_s = 0.385 K/J/(gK) and c_s = 0.13 J/(gK), respectively. Using the heat released in one switching (reset) cycle of JH = 10 μJ and assuming tentatively $f_l$oss = 0.1, one can infer the temperature increase is ΔT = 27°C. Obviously, the temperature at first is not uniform along the electrode lines when the heated device begins to heat up, but as was already mentioned, due to the high thermal diffusivity, it quickly reaches the steady state. The highest temperature of the heated device will be transmitted to the adjacent cells resulting in lower temperature of the neighboring cells. For an isolated metal rod, the 1-D heat equation's solution can be used to accurately predict f_{diss} [38]:

$$\frac{\delta T}{\delta t} = k_{th} \frac{\delta^2 T}{\delta^2 x} + \frac{g}{c_s \rho_m} \tag{4.6}$$

where g is the heat produced, k_{th} is the thermal diffusivity, c_s represents the specific heat capacity, T denotes temperature, and ρ_m stands for the mass density. The explicit solution to Eq. (4.6) for the metallic rod with a heated end can be found in [38]. It should be observed that TaO_x has a thermal diffusivity of k_{th} = 0.02 cm^2/s, while the thermal diffusivities of Pt and Cu are much larger (see Table 4.1), thus approximating well the isolated rod model.

The time defined by $t_{ts} = L^2/k_{th}$ provides the typical time scale for Eq. (4.6). With a cell-to-cell distance L of 150 μm and a thermal diffusivity of Cu $k_{th} = 1.11$ cm^2/s, one can calculate t_{ts} to be ∼200 μs. In view of this, one is justified to evaluate Eq. (4.6) under steady-state conditions because the period of the pulse of the SET-RESET cycles is about 60 s, which is 3×10^5 times larger than t_{ts}. Under steady state, the temperature becomes a linear function of the spatial coordinate alongside the electrode. Surely, during the 60 s of idle time, the electrode will cool down as a result of Newtonian heat losses, and the amount of heat still stored in the electrode can be approximated using the parameter f_{loss} as previously explained. Thus, if a corner array cell is heated up, the temperature will be a linear function of a distance along both of the electrodes.

One can calculate the transit time, t_{tr}, needed for a given temperature value to travel the distance of D = 850 nm, from the heat device to the pad on the far end of the metal line using the equation $D = \sqrt{k_{th} \times t_{tr}}$. This duration is less than 10 μs for the copper electrode and 2.23 times larger for the platinum metal line on account of the latter's fivefold lower thermal diffusivity (see Table 4.1) as well as the smaller cross-section of the Pt metal line than the Cu line. This makes it plain that, for the neighboring devices being studied after the heated cell's heating has been terminated for 45–65 s, the temperature distribution is well approximated by a steady state. The result is a linear dependence of the temperature on the spatial coordinate designating the location of the neighboring cells. Considering that the first cell positioned on the Cu or Pt electrode is heated up to temperature T_c while the electrode's farthest end is kept at temperature $T_o < T_c$, the temperature decrease from device to device is given by $(T_c - T_o)\times150/(100+5\times150) = (T_c - T_o)\times0.18$, where 150 μm is the distance between two immediate neighboring cells and $100 + 5\times150 = 850$ μm is the total length between the heated device and the contact pad at the far end of the line. T_o at the very beginning of the heating will be still 27°C but it will rise as the heating keeps

persisting. When the heat loss from the neighboring cells that are the farthest away is taken into account, a reasonable estimate of f_{diss} is between 0.6 and 0.7. The estimate of f_{diss} enables us to estimate f_{loss} to be between 0.11 and 0.09, which renders our aforementioned choice of $f_{loss} = 0.1$ self-consistent. This determination is based on the experimentally extracted value $f_{loss} \times f_{diss} = 0.063$. As a result, heated cell's threshold temperature T_c decreases as heat is transmitted to the adjacent cells via one of the common electrodes. The robustness of the Cu CF determines the threshold temperature, T_c for the specific cell, at which the cell's instability sets in, and as a result, T_c is bound to increase with the increasing strength of the filament or its decreasing R_{on} resistance. The critical cell temperature for a weak filament with a R_{on} resistance value of several tens of kilo-ohms (kΩ) has been determined to be around 350°C.

The number of SWC precipitating a rupturing of a Cu filament of a specific strength can be used to estimate the temperature increase ΔT for a single RESET operation. We found previously that it took 25 cycles of heating of a heated cell with a robust Cu filament of R_{on} = 5 kΩ set at I_{cc} = 100 μA to see the beginning of the reflowing of the contours of the Cu electrode pads, indicating an incipient melting of the copper metal. As a result, we may estimate ΔT for a single cycle using the formula $\Delta T = (1085°C - 27°C)/25 = 42°C$. The experiment was then performed with the same probed and heated cells, except that the probed cell was initially set with a thin filament of high resistance Ron = 20 kΩ formed at I_{cc} = 20 μA, and we found that 7–8 heating cycles have been enough to cause the device to rupture. The temperature is raised by 42°C in one cycle, hence $42°C \times 8 + 25°C = 361°C$. Thus, a value of around 350°C represents a crucial temperature for rupturing the weaker Cu filament. However, a robust copper nanofilament with low resistance of a few hundred Ohms is likely to display a critical temperature needed to rupture it near the Cu melting temperature, i.e., 1085°C. The threshold temperatures Ti for a weak filament for each of the

five cells arranged along the Pt line are plotted in Figure 4.6, with the first cell serving as the heated device and the other four serving as remotely heated neighboring cells. The heated device stressed with 13 maximum RESET-SET cycles reaches the instability threshold of Tc = 350°C. The nearby cells will exhibit lower temperatures, $T_c \times f_{diss}$, $T_c \times {f_{diss}}^2$, $T_c \times {f_{diss}}^3$, and $T_c \times {f_{diss}}^4$, for the first, second, third, and fourth neighbors, respectively, as explained above.

In Figure 4.4, the temperature difference $\Delta T = T_c - T_i$ between each neighboring cell and T_c is shown. This temperature margin ΔT limits how many inherent heating cycles the cell can withstand before the cells becomes unstable. For the first neighboring cell, this difference is 130°C. Since each heating cycle increases the temperature effectively by 27°C, the cell can switch maximally for 130°C/27°C = 4.8 or 5 cycles, while the fourth neighboring cell has a temperature margin of (350 – 50°C) = 300°C, which allows for maximum 300°C/27°C = 11.1 $\simeq$ 11 cycles. Using our definition of degradation given in Eq. (4.2), these two cases would correspond to degradation of the first cell of (13 – 5)/13 = 62% for the first neighboring cell and (13 – 11)/13 = 15%, respectively, in perfect agreement with the experimentally measured values shown in Table 4.3.

The maximum SWC M_x can be computed in the same way for all other cells. The corresponding M_x numbers are also indicated in Figure 4.4. Thus, there is a striking match between the expected number of the extra permissible RESET-SET cycles and the respective experimental figures M_x(ave) provided in Table 4.3. It should be noted that the temperatures shown in Figure 4.6 represent a snapshot of a transient phenomenon when the peak temperatures have been reached just after the heating of the heat cell has been stopped. If the cells are then probed just afterwards, they display degraded switching properties in terms of reduced number of switching cycles, as evidenced in Table 4.3. The transient nature of this phenomenon precludes, however, the determination of the endurance and retention

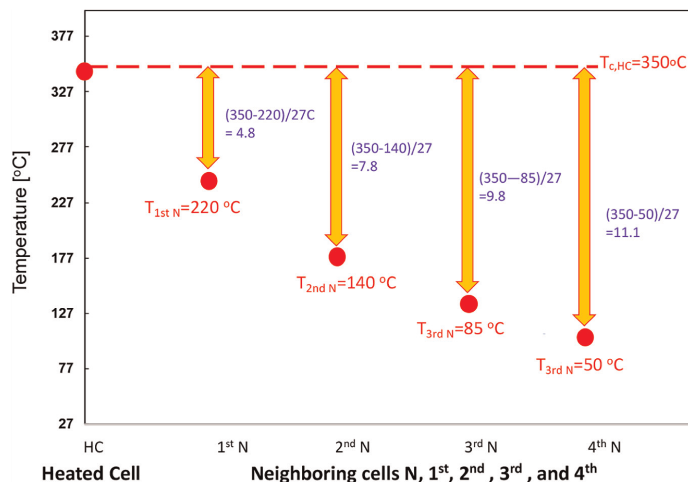

Figure 4.6: The red dots show the temperature of the heated cell when it reached a threshold temperature T_c of 350°C as well as of the four neighboring cells. The yellow double arrows indicate the temperature difference to the threshold temperature, which determines the amount of the cell's intrinsic heating to reach the threshold temperature at which the cell becomes unstable. Since one heating cycle increases the cell temperature by 27°C, the ratio of $(T_c - T_{iN})/27$ (where i = 1, 2, 3, 4) determines how many heating cycles the cell can tolerate before becoming unstable. For example, the fourth cell can tolerate 11 cycles before it becomes unstable, in very good agreement with the experimental degradation data.

properties.

We have tested the predictions based on the methodology described above by building ReRAM arrays with modified thermal properties of the electrodes. To accomplish it, we have manufactured, in addition to the Pt(50 nm) inert electrode, two composite Pt(50 nm)/Cu(100 nm) and Pt(50 nm)/Cu(200 nm) electrodes, as well as Rh(50 nm). It should be noted that for composite Pt/Cu electrodes, the intrinsic layers defining the memory cell are the same as for the Pt cell. The additional Cu layers present just two different embedment scenarios external to the cell proper, but are of crucial importance for the heat conduction properties. The key material characteristics of Cu, Pt, and Rh are listed in Table 4.1 and the effective thermal conductivities are calculated in Table 4.2. For the addition of Cu layers of 200 nm and 100 nm, respectively, the thermal conductivity of the bottom inert electrode increases 4 times, and the product $V \times c_s = m$ increases 1.95 and 1.47 times, respectively.

We now apply this methodology and compute the temperature for a single heating cycle by repeating the similar I–V measurements of the deteriorated cells applying the same RESET parameters used for calculating JH in Eq. (4.3). A temperature increment of 26.5°C for the Pt(50 nm) array, 18.1°C for Pt(50 nm)/Cu(100 nm), and 13.5°C for Pt(50 nm)/Cu(200 nm) has been measured, respectively, for one SWC. It is intuitively obvious that with the bottom electrode's increased ability to store and conduct heat, it will take more heating cycles to reach the same threshold temperature T_c upon reaching which the device is rendered unstable. Because of the bottom electrode's substantially better thermal conductivity, which causes a much faster transport of the heat pulse across the length of electrode, the maximum number of SWC is bound to increase.

The thermal diffusivity increased fivefold as a result of the composite inert electrode's enhanced thermal conductivity (Pt(50 nm)/Cu(200 nm), and the coefficient $f_d$iss for the Pt(50 nm) should have been at least three to four times smaller. This would suggest that the maximum number of switching steps for the ReRAM array with modified inert electrode with the same switching parameters should be 6–8 times greater, or 75–100 maximum SWC. The corresponding metrics (ΔT and M_x) for an array with Pt(50 nm)/Cu(100 nm) are ΔT = 18.0°C and a maximum RESET-SET cycle of approximately M_x = 25. Table 4.4 displays the information on the maximum RESET-SET cycles for the Rh electrode, the Pt/Cu(100 nm), and Pt/Cu(200 nm) inert electrodes.

The results of similar electrical degradation tests executed on the Pt(50 nm)/Cu (100 nm) and Pt(50 nm)/Cu(200 nm) ReRAM memory crossbar arrays in the same way as tests performed on Pt(50 nm) arrays are shown in Table 4.3 for devices #2 and #3, respectively. It is seen that the cells positioned along the Pt electrode do not degrade at all in the case of the Pt(50 nm)/Cu(200 nm) (device #3) inert electrode, while the first neighboring device positioned alongside the Cu electrode degrades only by 11% while the subsequent neighbors

Inert electr.	**Pt(50nm)/ Cu(200nm)**	**Pt(50nm)/ Cu(100nm)**	**Rh(50nm)**	**Pt(50nm)**
M_x	75	25	26	13
μ_{eff}[W/mK]	325	282	79	50

Table 4.4: The measured maximum M_x of RESET-SET SWC for a fragile filament set at the same value of I_{cc} for four different inert electrodes. The last column in the table shows our baseline device with the Pt(50 nm)/Ti(30 nm) with the maximum M_x of 13, as described already in Section 3. The effective thermal conductivity of the inert electrodes is also displayed to demonstrate palpably the clear correlation of maximum SW with the effective thermal conductivity of the inert electrode.

do not degrade at all. In contrast to the Pt(50 nm)/Ti(30 nm) ReRAM array (device #1), the local temperature for Pt(50 nm)/ Cu(200 nm) is clearly considerably lower due to the better thermal conductivity and specific heat capacity of the Pt(50 nm)/Cu(200 nm) electrode. Since fresh cells fail for a Pt(50 nm) electrode after just 13 times, but now for 72–90 times for a Pt(50 nm)/Cu (200 nm), this type of experimental testing undertaken for this study is rather laborious, but has been undertaken to demonstrate the accuracy of the predictions of our thermal analysis. As one would expect, the degradation data shown in Table 4.3 for the inert electrode Pt(50 nm)/Cu(100 nm) (device #2) lie between those of the Pt(50 nm) (device #1) and Pt(50 nm/Cu(200 nm) (device #3).

The suggested thermal study can be expanded to include the relationship between cell degradation and the width of the electrode lines. According to Eq. (4.4), the volume of the electrode grows proportionally with the width, causing the temperature difference ΔT to decrease with wider widths of the electrode lines. Pt and Cu lines (10 μm) have served as the standard for all of our tests thus far. We have gone over the analogous study for the 35 μm wide Pt line in the Pt(50 nm) ReRAM array. The mass of the platinum 35 μm metal line has risen, obviously, 3.5-fold compared with the 10 μm Pt line and the same applies to the respective product m $\times$ cs. However, because the Pt substance did not change, the

thermal conductivity remained constant. According to Table 4.3 degradation for the device #4 (Pt(50 nm) 35 μm wide inert electrode), electrical probing of the Pt(50 nm) line with a width of 35 μm, the surrounding cells' degradation is less severe than that of the Pt(50 nm) arrays' 10 μm Pt lines but slightly worse than that of the Pt(50 nm)/Cu(100 nm) 10 μm wide lines. At this point, it is instructive to revisit Figure 4.4 where it is shown that excessive heating leads to damaged (burned) cells. Both cells were operated under identical RESET-SET conditions featuring a Cu filament of the same resistance. The cell at the cross-section of 6 μm Cu and 6 μm Pt line shows severe damage just after three switching cycles. It is seen that the section of Cu electrode covering the cell has completely melted away. The cell at the cross-section of 10 μm Cu and 10 μm Pt line becomes inoperable after six of identical RESET-SET heating cycles and shows only a local melting of Cu along the ridge of the Pt line. The observation provided in Figure 4.4 confirms our thermal analysis: the wider Cu line provides not only more thermal mass to accommodate the temperature and therefore the maximum temperature decreases by 40%, but also larger heat loss to the heated cell because of larger heat transfer along the Cu electrode line. Therefore, more heating cycles are needed to cause localized Cu melting on a 10 μm wide electrode lines than on 6 μm wide lines.

Additionally, further support for our thermal analysis comes from earlier research [20], where it has been discovered that a ReRAM using Rh(50 nm)/Cr(30 nm) electrodes in place of Pt(50 nm)/Ti(30 nm) electrodes has nearly identical electric properties to a Cu/TaO_x/Pt/Ti memory cell. But, in contrast, for Pt/Ti devices, a cell set at I_{cc} = 10 μA with M_x of 15 grows to M_x = 26 for Rh/Cr devices. Because of higher thermal conductivity, the device Rh/Cr needs more of the identical SWC to reach the same T_c at which the device becomes inoperable. This is in line with our explanation of the thermal effects. In this particular case, we recall that the only purpose of Cr and Ti layers of 30 nm was to act as suitable

adhesion layers. But the two inert electrodes have different thermal conductivities of 150 W/mK and 94 W/mK for Rh/Cr, compared to 69 W/mK and 18 W/mK for the Pt/Ti bilayer combination. According to our thermal investigation, the m $\times$ c_s of the Rh and Pt electrodes are comparable, with the Rh electrode's product and being only marginally greater than the corresponding product for the Pt metal line (see Table 4.1). The product is about the same because Pt has 1.75 times higher mass density but 1.80 times lower specific heat capacity. As, however, Rh's thermal conductivity is 2 times greater than Pt's, we anticipate that using Rh as the electrode will result in cooler surrounding cells than using Pt as an inert electrode. The discovered boost of $26/15 = 1.73$ is within a reasonable interval of the estimates provided by our thermal investigation set forth in this work. In a way, the case of the narrower (10 μm wide) Rh(50 nm) electrode is the opposite of the case of the wider Pt(35 μm) electrode. The product m $\times$ c_s grew by a factor of 3.5 when the Pt line was wider, but the thermal conductivity remained constant when compared to a Pt line of 10 μm width. For the Rh 10 μm electrode, the product m $\times$ c_s is the same, but the thermal conductivity value has doubled.

In addition, different adhesive layers Ti and Cr have been added to two identical devices ($Cu/TaO_x/Ru$) in Figure 4.2 (compare inert electrodes (e) and (g)). As opposed to Ti, which has a thermal conductivity of 18 W/mK, Cr has a thermal conductivity of 94 W/mK, i.e., about five times higher. One discovers that the type of adhesive layer sensitively affects the electric performance of apparently equivalent devices. We discover that the Ru/Cr device's $V_{res} = -3.8$ V is 0.4 V higher than the Ru/Ti device's (V_{res}(Ru/Ti) $= -3.4$ V). According to our analysis, this outcome should have been readily anticipated. Compared to the Ru/Ti device, the Ru/Cr device sees a substantially higher rate of heat conduction from the Cu CF when the device is being heated during the RESET procedure. When using the Ru/Ti electrode, the heat produced in the Cu CF is not released quickly and remains in the area

near the hot point for a while because of Ru/Ti's low thermal conductivity. As a result, inert electrodes with lower thermal conductivities require less heating SWC than those with higher thermal conductivities because heat accumulates in the nanofilament at a faster rate with lower thermal conductivities, resulting in lower V_{res} voltage. A comparison of V_{res} values of the other devices is also useful. We discover that the V_{res} for the Co/Ti and Pt/Ti devices are, respectively, $V_{res}(Pt/Ti) = -0.9$ V and $V_{res}(Co/Ti) = -1.0$ V, i.e., statistically the same, which, once more, matches extremely well with the identical thermal conductivities of the two metals of 69 W/mK for both Pt and Co. Last but not least, there is a significant variance in V_{res} of around 2.5 V between Pt and Co devices and Ru devices, which is perfectly consistent with Ru's significantly higher heat conductivity than that of cobalt.

As a result, the impact of cell-to-cell heat transfer on the electrical performance of the device is shown to be influenced almost in equal parts by three mechanisms: (i) the electrode materials' specific heat capacity, (ii) thermal conductivity, and (iii) the product of volume and mass density of the electrodes, i.e., its total mass. Our thermal guidelines are able to predict quantitatively the amount of improvement or deterioration of the electrical degradation effects with reference to thermal material properties and geometrical shape of the electrodes, once our thermal methodology has been calibrated to a baseline array (here Cu/TaO_x/Pt/Ti device). Finally, we would like to address the issue of maximum SWC for different devices. Cu/TaO_x/Ru and Cu/TaO_x/Pt devices exhibit identical behavior at first, despite having differing V_{form}, V_{set}, and V_{res} threshold voltages, as demonstrated in Ref. [27]. The basic distinction between the two devices is the severely reduced cycling capability of the Ru devices. The Pt device may cycle through up to 100 SWC under optimal switching conditions, compared to the Ru device's mere 13 cycles. It was discovered that the Ru electrode's decreased inertness qualities were responsible for the reduced switching cycling ability. Similar to this, it was demonstrated in [39] that Cu/TaO_x/Ti and Cu/TaO_x/Ta devices had much

lower switching capabilities than $Cu/TaO_x/Pt$ devices.

4.5 Conclusion

We have provided a wealth of experimental data showing how the material properties and geometrical dimensions of the ReRAM electrodes affect the amount of cell-to-cell heat transfer, and, in turn, how the heat transfer affects the several appearances of degradation of the electrical performance of the resistive memory cells. The degree of device degradation has been quantified using a thorough thermal methodology of the heat transfer that takes into account the electrode materials' thermal conductivity, thermal diffusivity, specific heat capacity, and mass density. Although our memory arrays manufactured in a university laboratory match commercial ReRAM architecture only in terms of the vertical dimension, i.e., the thicknesses of the constitutive layers but exceed commercial products significantly in lateral dimensions, they still provide a great starting point for a reliable source of the essential physics and methodology true also for commercial ReRAM because the thermal reliability issues are driven by the same physical mechanisms and the same fundamental material properties. Actually, the heat density dissipated in state-of-the-art memory arrays is far worse than in our memory arrays, as demonstrated in [21], being about two orders of magnitude greater. The reliability problems and ReRAM degradation brought on by heat-cross-talk may thus be lessened with the help of the thermal analysis put forward here, which can act as a reliable road map for a suitable choice of materials or material combinations. There is currently no satisfactory answer to the question of what might be the best options for the inert electrode as far as their thermal properties are concerned. Low conductivity materials result in lower V_{res} value, which is obviously advantageous for the reduction of the heat dissipated in the arrays, and distant devices are mostly unaffected by the reduced thermal cross-talk alongside

the metallization lines. However, for low thermal conductivity electrodes, the Joules heat dissipated in a device lingers longer within the electrode materials and cell. In contrast, the rapid heat transport in the case of a high thermal conductivity electrode impacts by dint of the thermal cross-talk even the cells farthest from the heated cell. ReRAM arrays must be optimally designed and operated taking into account how the memory is being used in terms of programming and erasure cycles to minimize adverse thermal cross-talk effects.

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Chapter 5

Electrical Characterization of ReRAM Arrays to Observe Thermal Cross-talk

This chapter has been reproduced from a manuscript that is under preparation titled ***Electrical Characterization of ReRAM Arrays to Observe Thermal Cross-talk*** *authored by* ***Amrita Chakraborty, Payton Fallen, Aaron DiFilippo, and Marius Orlowski.****[1]*

In this chapter, we discuss the ongoing status of this research and the future scope of this work. As elaborated throughout this dissertation the primary focus of this work is the investigation of the heating effects within a ReRAM crossbar array structure. A huge part of this research has been dedicated to the exploration of how heat generated at one cell affects the functionality of its neighboring cells. Thus, at this stage of the research, it is of utmost significance that we employ novel characterization setups to capture this phenomenon.

5.1 Introduction

Our studies have provided sufficient evidence to demonstrate that the continuous switching of a ReRAM cell generates enough heat to influence the state and performance of its neighboring cells within an array. The majority of the heat is produced during the RESET operation.

In this process, due to thermal dissolution, a significant amount of heat accumulates locally within the nanofilament at its narrowest region, i.e. the region of highest resistance. This continuous heat buildup within the filament leads to the rupture of the filament, breaking the connection between the top electrode and the bottom electrode.

In our analysis in Chapter 4, we demonstrated that if all the heat were contained within the filament itself, it would make the filament hotter than the core of the sun. Clearly, this cannot be the case. Instead, the generated heat primarily dissipates from the cell through the two electrode lines and to the ambient via convection and radiation mechanisms[2]. If the duty cycle of switching a cell is too small, and the rate of heat dissipation produced during each cycle is not fast enough, the heat generated in previous cycles starts to accumulate at the switching cell and its electrode lines. Due to the crossbar architecture, a cell is connected to cells within the array via common electrode lines. Therefore, at some point, enough heat can build up and raise the temperature of the electrodes to a level that starts to influence the state of neighboring cells.

Although as expected, it has been observed that the degradation of neighboring cells is different for the top Cu electrode and the bottom Pt electrode on account of different thermal properties of the two metals. Figure 5.1 shows a schematic of a ReRAM array and illustrates the direction heat can transport through the common Cu and common Pt electrodes.

Equation 5.1 represents the novel parameter "Degradation(DEG)" that gives us a measure of how much a neighboring cell gets affected based on its distance from the heated cell. As shown in Chapter 4 Table 4.3, the degradation of neighboring cells is stronger in the case of a common Cu neighbor than a common Pt for the case of a Cu/TaO_x/Pt ReRAM device.

$$DEG = \frac{M_x(unstressed\ cell) - M_x(preheated\ cell)}{M_x(unstressed\ cell)} \tag{5.1}$$

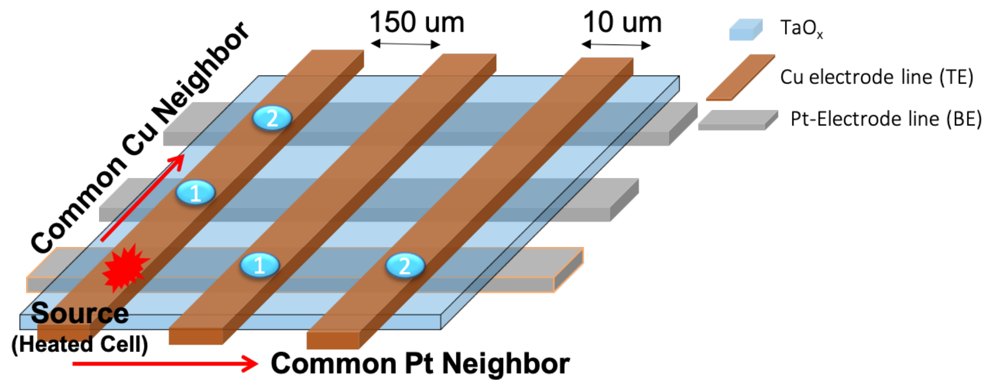

Figure 5.1: ReRAM array showing a source cell which is generating heat due to switching and its common Cu and common Pt neighbors

It has also been observed through our experiments that if a neighboring cell is initially kept at ON-state, and the primary switching cell is switched continuously, the generated heat can then rupture the filament of the neighboring cell thus changing its state from ON to OFF. In [3] the authors have showcased instances where they have observed this phenomenon. As seen in Figure 5.2(a), let us consider a heated cell (the primary switching cell) as the red cell. When the cell is heated, the heat can transport through the electrodes and can affect cell X_i and Y_j denoted by black plus signs. During one of the switching instances we found that a neighboring cell along the common Pt electrode, (X_i) also called probed cells, kept at an initial ON-state with R_{on}=15kΩ ruptured because of the thermal effect from the heated cell. Similar observations were made for a cell along the common Cu line where the probed cell was at an initial On-state with R_{on}=4.8kΩ. Interestingly, both these cells were observed to have their filaments spontaneously restored (Figure 5.2 (b) and (c)) once the effect of this secondary heating subsided.

This transient abrupt increase in the filament resistance forcing the probed cell to transition from ON-state to OFF-state and the spontaneous restoration of the filament after eventual

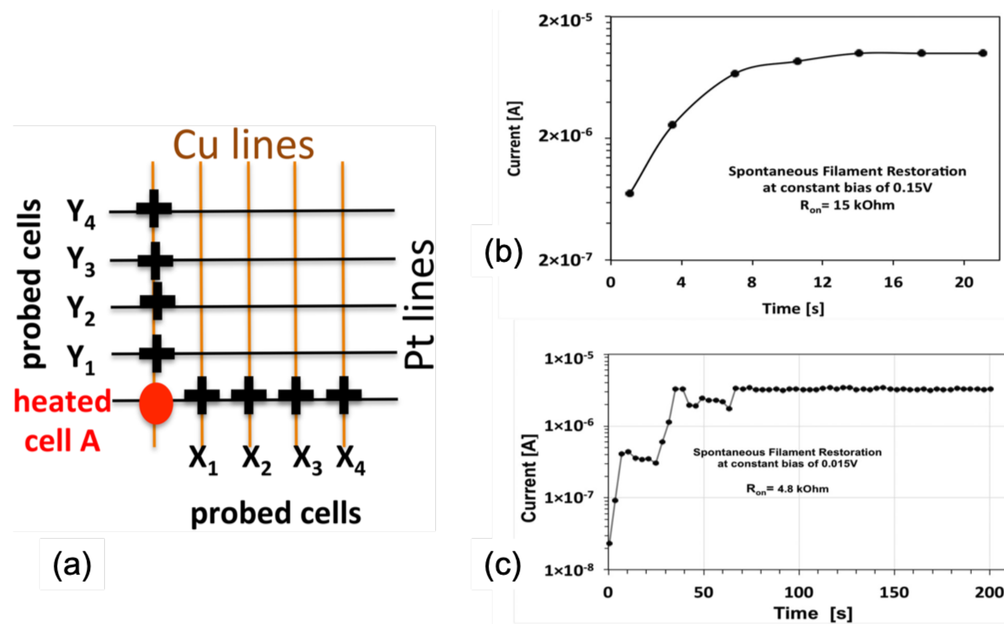

Figure 5.2: (a) Crossbar cell array showing heated and probed cells; (b)Increase of current indicating filament restoration through a cell X1 immediately after the heating of the source cell A (c) Increase of current indicating filament restoration through a cell Y1 immediately after the heating of the source cell A. Reproduced with permission [Al-Mamun, M., Orlowski, M. Electron tunneling between vibrating atoms in a copper nano-filament. Sci Rep 11, 7413 (2021). https://doi.org/10.1038/s41598-021-86603-6]

cooling can be attributed to a moderate heating incident. A *moderate* heating is a case where "there is sufficient amount of heat to cause the Cu atoms of the nanofilament to vibrate but not strong enough to allow outright out-diffusion of Cu atoms from their equilibrium sites in the TaO_x matrix that would weaken permanently the filament structurally"[3]. The increased resistance in this case is not due to the total rupture of the filament rather it is because the average distance between the vibrating Cu atoms has increased around an equilibrium position.

5.2 Concurrent Observation of Heated cell and Probed cell

Going forward, for clarity and ease of identification, we will refer to the main switching cell as the heated cell and to the adjacent cells as probed cells.

One of the significant constraints in characterizing thermal cross-talk between cells has been the two-probe experimental setup.

Two-terminal Setup

The measurement setup for a ReRAM cell I-V characterization is a two-terminal setup. A probed cell is influenced by the secondary heating discussed above simultaneously while a heated cell is being switched. Due to a two-terminal measurement setup, a probed cell cannot be monitored while a heated cell is in the process of switching. To monitor a probed cell periodically, a user would need to consecutively switch probes between a heated cell and the probed cell. We observed that it takes an adept user about 50 seconds to reposition needles on the probe station from one cell to the other. Consequently, even though we have

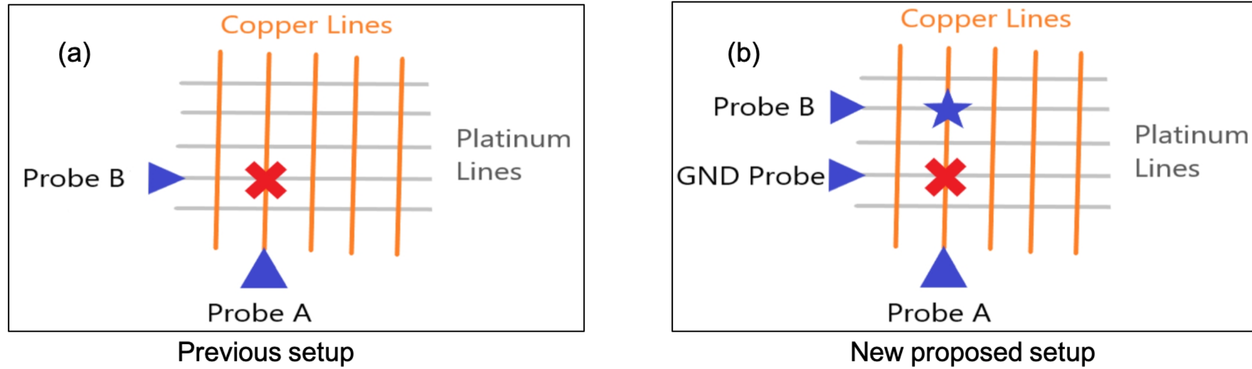

Figure 5.3: (a)Two terminal measurement setup; (b) New 3-terminal measurement setup to monitor thermal cross-talk

collected evidence of probed cell filament restoration due to its transition from HRS (High resistive state) to LRS (Low resistive state), we are unable to capture the transition of the cell from LRS (initial ON-state) to HRS (OFF-state). Therefore, a new experimental setup is required to observe thermal cross-talk between cells.

Proposed New Three-terminal Setup

Figure 5.3(b) shows the new proposed and employed measurement framework to monitor two cells simultaneously. In comparison to the previous setup, the new setup is a 3-terminal measurement. In an ideal scenario, we would desire a 4-terminal measurement, which would essentially be two 2-terminal measurements carried together. In that case, we would have been able to switch the heated cell independently of the probed cell and the probed cell would have been monitored using a completely separate analyzer. Unfortunately, currently, we have access to only one Keithley 4200A SCS to be used as our characterization system.

We devised an innovative characterization plan, illustrated in Figure 5.3(b). In this configuration, the red cross represents the heated cell, and the blue star denotes a neighboring cell. To observe thermal cross-talk between the two cells, a constant DC voltage is applied to

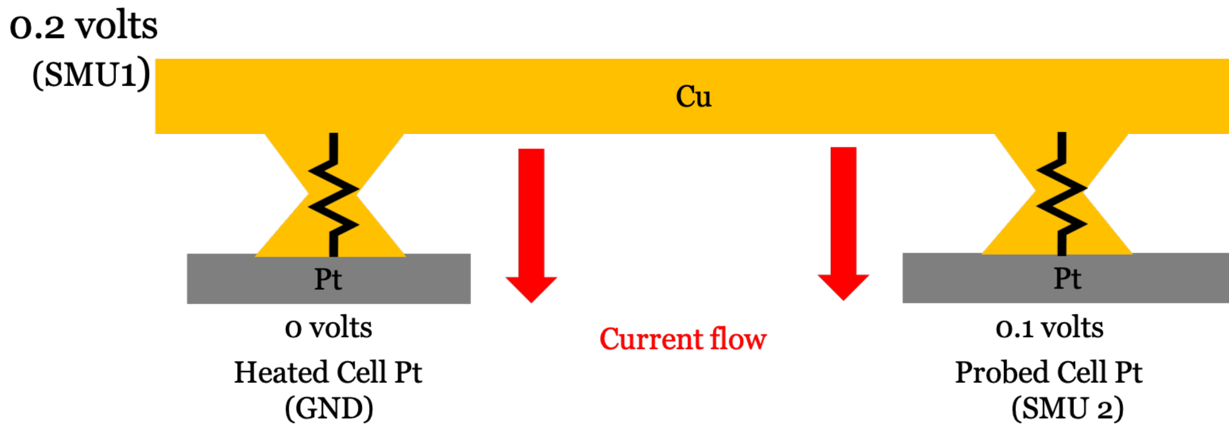

Figure 5.4: Lateral schematic of measurement setup showing voltage connections

both, in contrast to a switching scenario where a sweeping bias is applied, and the polarities of voltage change based on SET or RESET operations.

The purpose of a 3-terminal measurement is to apply a constant DC bias across a heated cell that is in the ON-state. A positive DC bias is applied to the Cu electrode of the heated cell, while the Pt electrode is grounded. As depicted in Figure 5.3(b), the Pt electrode of the probed cell (which is a common copper neighbor in this case and is also in the ON-state) receives a DC voltage, ensuring that the potential drop across the probed cell is insignificant. This voltage is set to be less than the minimum voltage required for SET operation or the influence of the voltage on the filament's structure, and any filament degradation (if present) occurs solely due to thermal cross-talk effects. The selection of a low voltage applied across the probed cell is deliberate, aiming to obtain only a current reading from the cell to discern whether the nanofilament within the cell has ruptured. In Figure 5.4, a lateral schematic illustrates the connection of the two cells through a Cu electrode, providing a representation of typically applied voltages and current directions. Observe that a positive voltage 0.2 V is applied to the Cu electrode, which gives a net 0.2 V across the heated cell and a positive 0.1 V is applied to the Pt electrode of the probed cell so that a net 0.1 V is applied across the

probed cell. SMU 1 and 2 are called “Source Measure Units”, which are the voltage sourcing units of Keithley 4200A SCS and GND is the ground terminal.

5.3 Measurement Results and Discussion

In order to observe thermal cross-talk and rupturing of filament of the probed cell, ReRAM cell pairs were tested for different I_{cc} settings. In most cases otherwise mentioned the chosen cell pairs were immediate neighbors within the array (heated cell and X_1 or Y_1, see Figure 5.2 (a)). In addition to filament rupture, we also want to register spontaneous restoration of filament as in case of a *moderate* heating. When a heated cell of a certain filament strength (eg. $R_{on} = \sim 750\ \Omega$) causes rupture of a weak filament strength (eg. $R_{on} = \sim 2.5\ k\Omega$) because of thermal cross-talk, it is observed that the filament of the probed cell does not undergo spontaneous restoration even in the case of excessive heating. This is because when a strong filament produces enough heat to rupture a weak fragile filament, in most cases the heat is sufficiently large to cause an out-diffusion of Cu atoms from the weak filament which causes irreparable damage, and the filament rupture is permanent. The cell has to go through a SET operation in order to replenish the ruptured region of the filament to build it back again.

Shown in Figure 5.5 is the remote heating operation of a weak filament (blue curve) by a strong filament (orange curve). These two cells are immediate neighbors to each other and share a common 10 μm Cu electrode. The heat generated at the heated cell (I_{cc}= 35 μA and R_{on}=760 Ω) permanently ruptured the filament of a weaker probed cell (I_{cc}= 15 μA and R_{on}=2.5 kΩ). It takes about 1.3 minutes for the heated cell to generate enough heat to rupture the probed cell. The heated cell consistently maintains a current flow of approximately 600 μA, while the probed cell initially conducts 40 μA. However, after about

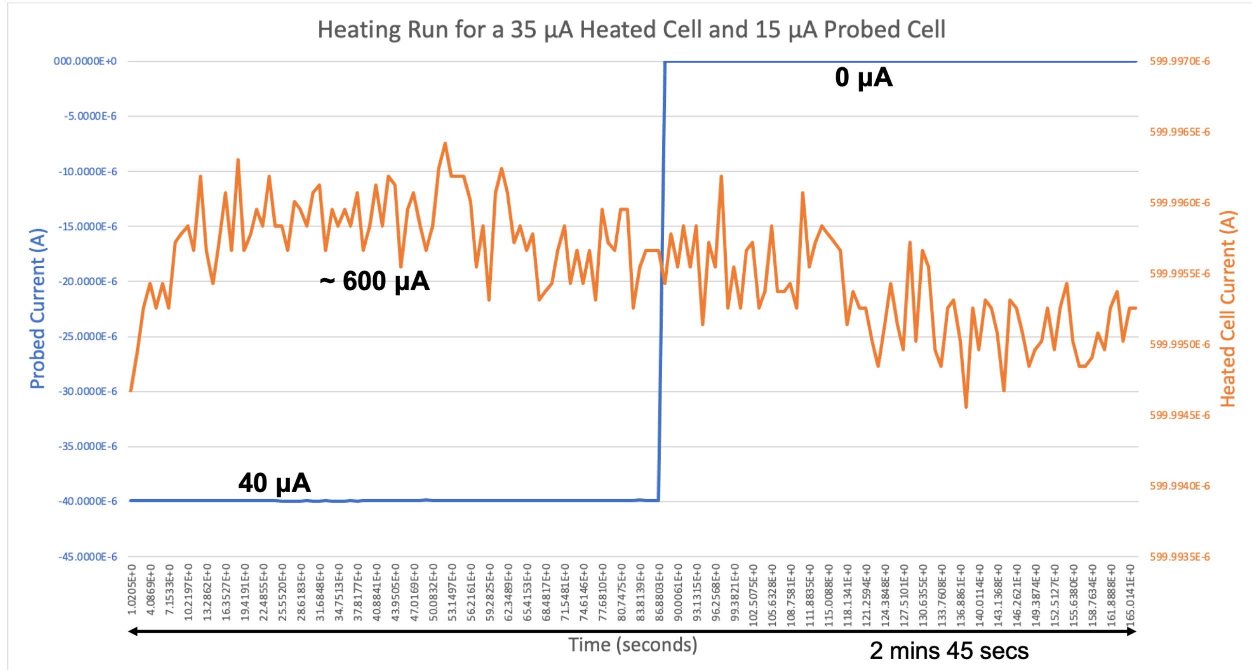

Figure 5.5: Current vs. time plot of a 3-terminal measurement. Heated cell current in orange (R_{on}=760 Ω) and probed cell current in blue (R_{on}=2.5 kΩ)

1 minute and 26 seconds, the cell experiences a rupture, as evidenced by a sudden drop in the current. This probed cell was later observed to not restore its filament spontaneously. Also, notice that the current of the probed cell is a negative current as it is the current measured at the Pt terminal and indicates the current direction (refer to Figure 5.4).

In contrast, our observations from multiple tests reveal that a probed cell, when SET with a higher I_{cc} (90 μA, R_{on}=∼ 150Ω), remains intact even when subjected to heating under the same conditions depicted in Figure 5.5. This provides evidence that a strong and robust filament exhibits resilience against thermal cross-talk and is somewhat shielded from degradation. However, it is worth noting that the drawback of such robust filaments is their inherent difficulty to switch (RESET) initially, owing to their robustness. Consequently, operating a ReRAM at very high I_{cc} and filament strength may not be ideal for achieving efficient resistive switching.

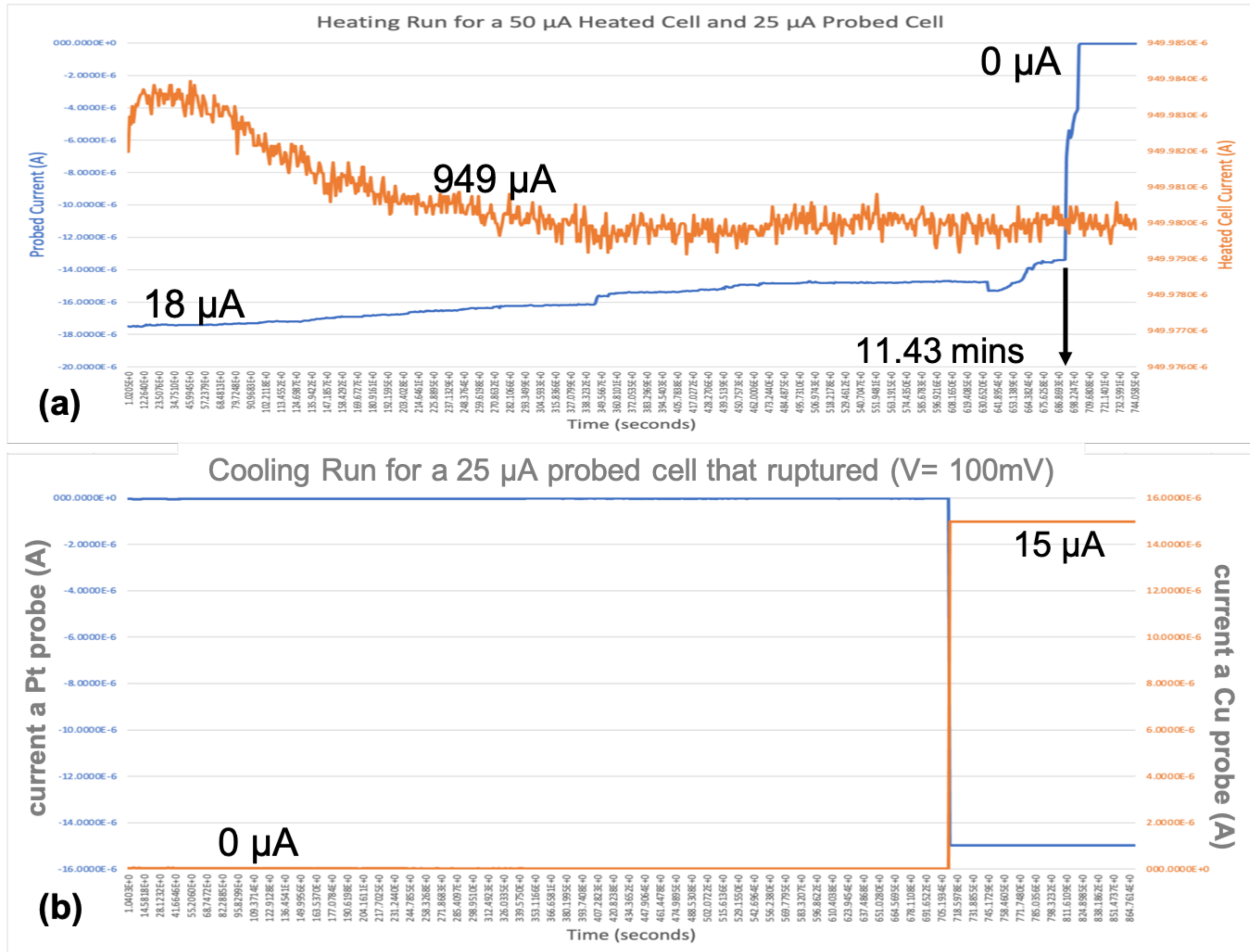

Figure 5.6: (a)Heating run, showing rupture of the filament of a I_{cc} = 25 μA probed cell; (b) Cooling run showing spontaneous restoration of the filament of initial strength R_{on}= 1 kΩ

Now that we have discussed the two extremities, let us focus on the case of *moderate heating*. The likelihood of observing a spontaneous restoration of a filament increases in a mid-range filament strength with moderate heating, where even though the filament does not conduct temporarily, it restores itself as the cell cools down. Figure 5.6(a) shows the rupture of a filament(blue) of I_{cc}=25 μA, R_{on}=∼ 1 kΩ. In Figure 5.6(b) we see that the filament has been restored spontaneously as the cell cooled. It is to be mentioned that during our testing, when a cell ruptures, we immediately stop the 3-terminal heating measurement and only observe the probed cell at a very low voltage of 100 mV.

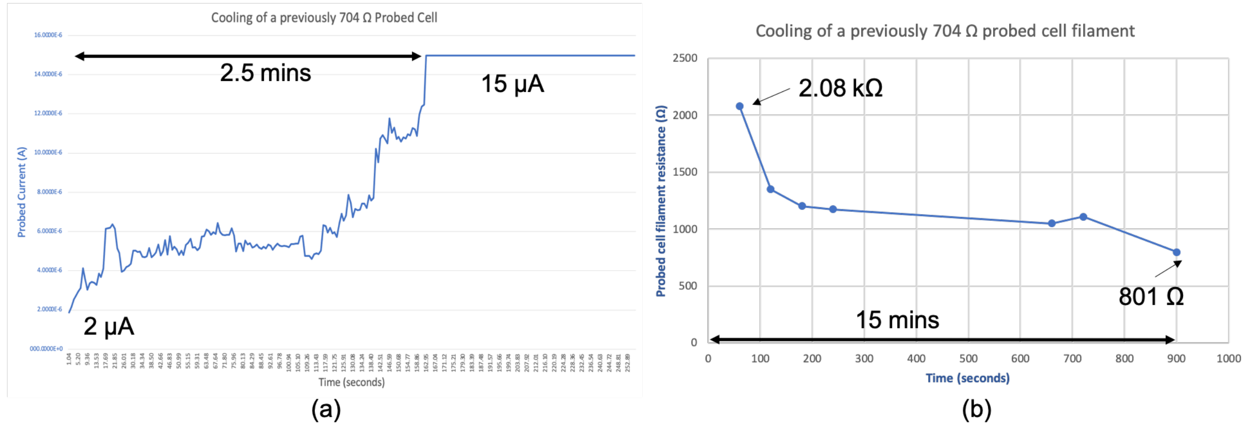

Figure 5.7: Cooling run showing spontaneous restoration of probed cell filament to its initial strength R_{on}= 704 Ω

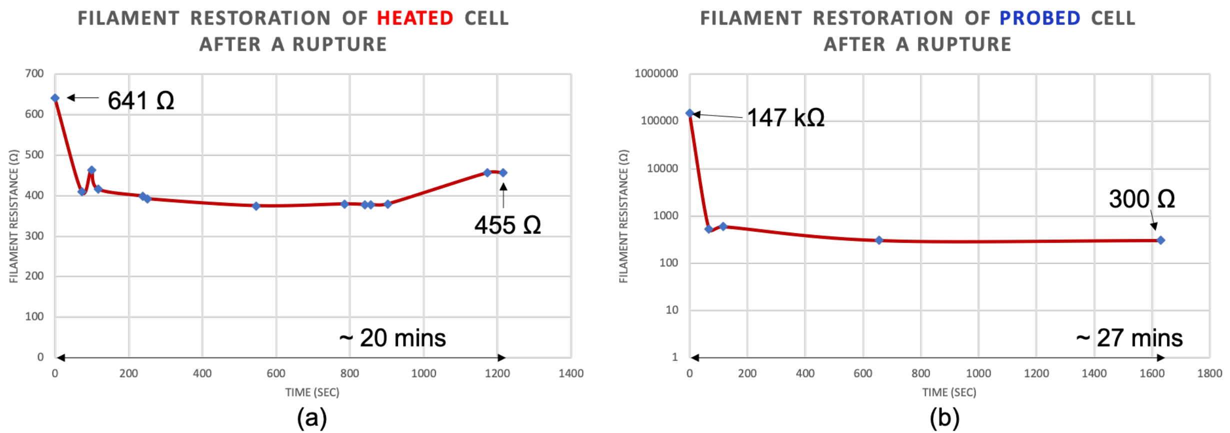

Figure 5.8: Cooling of a heated and probed cell after rupture

An additional example of the cooling process for a ruptured cell is illustrated in Figure 5.7. In this scenario, a probed cell with R_{on}= 704 Ω @ I_{cc}=35 μA experienced rupture due to heat generated by a heated cell with R_{on}= 154 Ω @ I_{cc}=90 μA. Remarkably, it took approximately 2.5 minutes for the cell to restore its filament, a significantly faster recovery compared to the probed cell filament depicted in Figure 5.6, which required about 12 minutes. The probed cell shown in Figure 5.7 (a) came back close to its original strength after a further 15 minutes of cooling as shown in Figure 5.7 (b). As seen in the figure, the filament resistance decreases from 2.08 kΩ to about 800 Ω, thus increasing in strength.

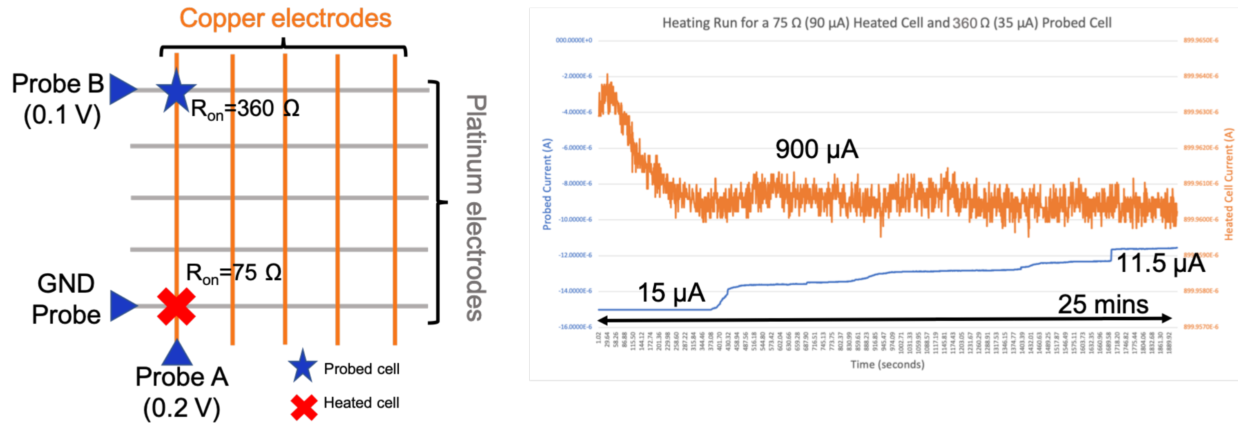

Figure 5.9: Filament weakening due to remote heating of the furthest cell in a common Cu configuration

In another scenario, we observed simultaneous degradation in both the heated cell and the probed cell during the heating phase. The initial resistances were R_{on}= 86 Ω for the heated cell and R_{on}= 329 Ω for the probed cell. Despite degradation, the heated cell did not undergo complete rupture. As depicted in Figure 5.8(a), the resistance of the heated cell filament decreased from 640 Ω to 455 Ω over approximately 20 minutes during the cooling period. Meanwhile, the probed cell filament strength reduced from 147 kΩ to about 300 Ω within the same timeframe (Figure 5.8(b)). Interestingly, the heated cell, acting as the primary source of heat, experienced the major impact of thermal effects. Although it was resilient enough not to rupture completely, it demonstrated a gradual recovery during the cooling phase. In contrast, the probed cell, initially the weaker of the two, exhibited a rapid recovery following rupture and even restored the filament back to its original strength.

The aforementioned findings are derived from experiments conducted on cell pairs situated as immediate neighbors that share a common Cu electrode. It is, therefore, intriguing to examine the impact of remote heating on cells positioned farther away from the heated cell. In our earlier investigations (Chapter 4), we demonstrated that the influence of remote heating diminishes as we move further along the same electrode line away from the heated cell. To

explore this phenomenon, we selected a cell pair within an array featuring 10 μm electrode widths, where the probed cell represents the farthest neighbor from the heated cell along the shared Cu electrode (refer to Figure 5.9). Results indicate that following an extended period of remote heating, the probed cell begins to conduct less current than initially, suggesting a weakening of the filament. It is noteworthy that in this particular case, the probed cell requires a more prolonged duration of remote heating compared to previous instances, and yet, it does not rupture; instead, it exhibits filament weakening. This aligns with our earlier discovery highlighting that the furthest neighbor along any common electrode line is the least degraded cell affected by thermal cross-talk.

In these experiments, we took measures to ensure that no cells within the arrays, other than the specific cell pair being tested, were in the ON-state. This precaution was implemented to prevent the occurrence of any sneak conductive paths.

5.4 Conclusion

This chapter introduced an effective methodology for characterizing thermal cross-talk within a ReRAM. The results clearly demonstrate the impact of remote heating on the resistive state of a probed cell. It is evident that excessive heating can lead to irreversible rupture of a fragile filament in a cell at ON-state, forcing the cell to transition into an OFF-state. Additionally, the study highlights that robust filaments remain unaffected by remote heating. Conversely, instances have been identified where moderate heating causes a semi-fragile filament to partially rupture or weaken. However, this filament restores itself as heating is ceased while the cell undergoes cooling. Furthermore, the chapter illustrated that a probed cell positioned furthest from the heated cell within a common Cu electrode line experiences significantly less degradation due to remote heating compared to cells that are immediate neighbors.

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Chapter 6

Summary and Future Works

6.1 Summary of Work

This research is primarily dedicated to investigating the factors influencing the performance and reliability of Resistive Random Access Memory (ReRAM). The study focuses on a $Cu/TaO_x/Pt$ device as the reference, frequently examining its performance in contrast to other electrode systems.

Following discussions on motivation, basic principles, and fabrication procedures in Chapters 1 and 2, Chapter 3 delves into the impact of intrinsic material properties, such as thermal conductivity and specific heat capacity, on ReRAM device performance. The exploration extends to understanding how these material properties, along with deposition factors like surface roughness, affect the electroforming voltages of ReRAMs. Three different ReRAM devices are considered, with the sole distinction being their inert electrodes—Pt, Co, and Ru. The chapter further investigates the inertness of these metals, with a specific focus on Ru compared to the widely used Pt. Ru is selected for its compatibility with CMOS Back-End-of-Line (BEOL) and economic viability relative to Pt. The chapter presents evidence concerning silicide reaction of Ru and conducts a figure-of-merit comparison between Pt and Ru based on electroforming voltages, retention rate, endurance, and BEOL integrability.

Extending the research further, Chapter 4 draws from findings in Chapter 3 to showcase how

elements such as thermal conductivity, melting temperature, mass density, and thermal diffusivity of electrode materials have a direct correlation to thermal transport within ReRAM device arrays. It has been observed through device characterization how remote heating can influence the state of a cell rendering it degraded. A degradation parameter, DEG, has been introduced to quantify the level of degradation of cells based on their vicinity to the heated cell. Further, a novel methodology has been proposed based on the fundamentals of thermodynamics and material properties to predict cell degradation.

Chapter 5 presents an inventive characterization method to measure and observe thermal cross-talk between cells. Evidence has been presented to show the rupturing of cell filaments due to remote heating. It has also been shown that under moderate heating, a ruptured filament can be restored spontaneously as the cell cools.

Additionally, the appendix section of this dissertation introduces a distinct line of research focused on Resistive Random Access Memories (ReRAMs). It showcases successful outcomes in fabricating electrodes made from organic polymer materials, presenting innovative techniques for enhancing the conductivity of these organic electrodes. The aim of this research segment is to pave the way for the development of a fully organic material-based ReRAM in the future. Previous studies have already demonstrated the efficacy of organic polymers as a switching layer in resistive memory. The incorporation of conductive organic electrodes represents a significant advancement, moving the research closer to the realization of an organic and flexible ReRAM.

6.2 Future Works

To further advance this research, a thorough and detailed investigation using the 3-terminal measurement method introduced in this study is essential to characterize thermal cross-talk

within ReRAM arrays. The current findings are limited to the examination of common Cu neighbors. Consequently, experiments involving common Pt neighbors need still to be conducted. Once a comprehensive understanding of the behavior of both common Cu and common Pt neighbors has been established, the scope of experiments can be expanded to include cells situated diagonally to the heated cell. These diagonal cells do not share a common electrode with the heated cell but may be influenced if a sneak path exists through the ON-state filament of a Cu or Pt neighbor.

Initiative has been taken for preliminary studies aimed at developing a model for our fabricated ReRAM arrays and simulating the heat transport behavior within them. Early findings of the simulations using program ANSYS align with our experimental results but require a more in-depth exploration of governing equations and underlying principles to accurately replicate the observed behaviors. Progress in the simulation model will also aid in validating the thermodynamic analysis predicting cell degradation, as presented in Chapter 4.

Furthermore, an extended research focus is required to investigate the impact of filament shape on thermal cross-talk. These future strategies will contribute to understanding the role of filament geometry in thermal transport within ReRAMs. Consequently, a robust model can be formulated to predict cell degradation and reliability, serving as a benchmark during the electrical characterization of such ReRAM device arrays.

Appendices

Appendix A

Conductive Organic Electrodes for Flexible Electronic Devices

This appendix chapter has been reproduced from Ref. ***Amrita Chakraborty, Daniel Herrera, Payton Fallen, Daniel Hall, Nicholas Bampton, Thomas Olivero, and Marius Orlowski. Conductive organic electrodes for flexible electronic devices. Scientific Reports, 13(1):4125, March 2023. Number: 1 Publisher: Nature Publishing Group*** *with minor changes.[1]*

The chapter reports on a novel process flow to manufacture conductive organic electrodes from highly conductive doped PEDOT:PSS polymer films that can be patterned and display a good adhesion to oxidized Si wafers as well as to flexible substrates, such as Mylar. Among other results, it is shown that multiple depositions of PEDOT:PSS increase the electrical conductivity by more than two orders of magnitude without increasing the film thickness of PEDOT:PSS significantly. An exponential dependence between sheet resistance and the number of PEDOT:PSS coatings has been found. The electrical conductivity of PEDOT:PSS can be increased by another two orders of magnitude doping with Cu nanoparticles when coated on the surface of a soft-baked PEDOT:PSS film. It is found, however, that both kinds of conductivity enhancement are not additive.

Adhesion of PEDOT:PSS to oxidized Si wafers and BoPET (Mylar) has been ensured by applying an oxygen plasma cleaning step before spin coating. The manufactured high-conductivity PEDOT:PSS film can be patterned using a sacrificial metal layer with subsequent etching of PEDOT:PSS in oxygen plasma, followed by the removal of the patterned segments of the sacrificial metal layer in an aqueous acid solution.

A.1 Introduction

Among the promising candidates for organic highly conductive films such as polyacetylene, polypyrrole (PPy), polyaniline (PANI), and poly(3-hexylthiophene) polymer (P3HT), poly 3,4-ethylene dioxythiophene: polystyrene sulphonate (PEDOT:PSS)[2] has attracted a lot of attention in various fields of application. The advantages of PEDOT:PSS include, mechanical flexibility and integrity, good thermal stability, high transparency in the visible range, light weight, easy processing and deposition by spin coating, spray coating, and ink-jet printing, and a variety of methods to increase conductivity by several orders of magnitude (still under active research), and a work function between 4.5 eV and 5.2 eV roughly comparable with work function of Cu of 4.7 eV, which is favorable for applications in hybrid crystalline silicon solar cells [3].

Successful application of PEDOT:PSS has been reported in optoelectronic devices as a transparent and flexible electrode [4, 5, 6, 7, 8, 9], in next-generation photovoltaics [10, 11] in energy devices, and in functional packaging layers [12, 13]. PEDOT:PSS conductive layers have successfully supplanted indium-tine oxide (ITO) films [14, 15, 16] as a transparent conductor. The high transparency in the visible range of PEDOT:PSS facilitates the application of PEDOT:PSS in semitransparent photovoltaics. The group of F. Zhang [17] reported fab-

rication of semitransparent polymer solar cells (PCS) with 9.40% power conversion efficiency and 24.6% visible transmittance and optimized PCS with a power conversion of 15.6% with high transmittance in the visible light range and low transmittance in the near infrared range [18]. X. Zhang et al. [19] have demonstrated highly conductive PEDOT:PSS transparent electrode prepared by a post-spin-rinsing method for polymer solar cells. In charge extraction and injection devices, PEDOT:PSS has been used as an effective buffer layer [20, 21, 22]. PEDOT composites serve as a redox-active component in energy storage cells [23, 24]. Additionally, bioelectronic devices [25, 26], and thermoelectric materials [27]] have taken advantage of PEDOT:PSS. Highly conductive PEDOT:PSS films have been reported for ITO-free liquid crystal display [28].

Despite all of its advantages, the electrical conductivity of pristine PEDOT:PSS films is on the order of 0.1 S cm^{-1}, which may be much larger than that of metal oxides such as TaO_x of 10^{-6} S cm^{-1} but is still significantly lower than the conductivity of metals such as Ta of roughly of 7×10^4Scm−1. Many different methods have been identified to enhance the electrical conductivity of PEDOT:PSS[28]. Before giving a brief review of the enhancement techniques, a deeper look into the properties and morphology of the PEDOT:PSS films is warranted to inform possible doping methods1. PEDOT:PSS consists of two components: the conductive PEDOT and the insulating PSS, whose oligomers entangle the PEDOT oligomers. The hydrophobic and water-insoluble PEDOT grains stay in the core surrounded by a shell of the hydrogen sulfate groups of the hydrophilic PSS chains which attach to the core surface and form a micelle structure. The thickness of the grain boundary is 30 Å–40 Å[29]. The positively charged PEDOT core is electrostatically bound to a PSS polyanion. During the deposition, due to its hydrophobic nature, PEDOT tends to stay away from water and settles at the bottom of the film while the hydrophilic and hygroscopic PSS strings, which are attracted to water, occupy the top portions of the film[30]. Thus, in wet films a phase

separation occurs between the PEDOT-rich bottom and PSS-rich top The subsequent thermal annealing at temperatures between 90°C and 130°C leads to improvement of electrical conductivity due to the decreased water absorption and increased density of PEDOT grains, being insufficient for remixing the two phases. The phase separation leads to two different lateral and perpendicular conductivities of the PEDOT:PSS films. While the lateral electric conductivity occurs via hopping of charge carriers, the perpendicular conductivity (roughly 3 orders of magnitude smaller) is dominated by space charge effects. After the spin coating deposition PEDOT:PSS consists of horizontal layers of flattened PEDOT grains separated from one another by quasi-continuous barriers of PSS ribbons.

Based on those properties of PEDOT:PSS films, there are three major strategies for enhancing its electrical conductivity: (a) increase the concentration of PEDOT grains while at the same time decrease the concentration of PSS, (b) to screen the electrostatic attraction between PEDOT and PSS and thus facilitate the electron hoping between bonds across the carbon skeleton, and (c) by introducing nanoparticles or nanocomposites to bridge the distance between PEDOT islands within the PSS bulk. An excellent review of those approaches has been given by the Sarifuddina group[2]. Z. Xiong et al.[31] have manufactured inkjet-printed thin films of PEDOT:PSS doped with silver nanoparticles with excellent electrical and optical properties. Patil et al.[32] also reported an enhanced conductivity of PEDOT:PSS by doping it with silver nanoparticles. R.-C. Zhang et al.[33] have demonstrated a one-step synthesis process for gold nanoparticles—PEDOT:PSS nanocomposites and their successful application as an alkaline direct ethanol fuel cell catalyst. O. Ghazy et al.[34] have incorporated silver particles prepared by gamma radiation to enhance the conductivity of PEDOT:PSS for the application of organic solar cells. L. Pham et al.[35] have demonstrated improved polymer conductivity when doped with Cu nanoparticles (NP).

The final step in the process integration to manufacture organic electrodes is the pattern-

ing of conductive polymers. The patterning of organic polymer films has been performed by various methods—vapor deposition through shadow masks, by ink-jet printing, soft and hard imprint lithography, and conventional photolithography[36, 37]. Ink-jet printing exhibits excellent roll-to-roll process capabilities and is the technique of choice for patterning of polymeric materials. However, its resolution is limited to 10–20 μm[37, 38]. Shadow-mask deposition is an ubiquitous technique for small-molecule patterning, but also suffers from resolution limitations in the range of around 25–30 μm[39]. Moreover, shadow-mask deposition requires a high-vacuum chamber. The smallest feature resolution down 10 nm has been demonstrated by imprint lithography[40, 41]. However, this technique is quite expensive and available only in highly specialized laboratories. Furthermore, in all of the aforementioned methods, challenging registration of related patterns on separate photomasks is a thorny issue and renders fabrication of multilayer devices difficult. Photolithography remains the most attractive patterning technique for the patterning of inorganic electronic materials as it is a standard patterning method in modern silicon-based semiconductor industry. However, until recent, photolithography has made little inroads in patterning of PEDOT:PSS, due to a lack of chemical compatibility with PEDOT:PSS. Traditional photolithography leads to a chemical deterioration of active organic materials upon exposure to process solvents for lithography[40]. Recently, Ouynag et al.[41] have reviewed current PEDOT:PSS patterning approaches using modified photolithography processes. Through properly selected materials, insertion of sacrificial protective layers, and etch processes, PEDOT:PSS can be patterned while avoiding this deterioration. Ouyang et al.[41] have demonstrated a process in which photoresist is deposited and patterned on top of a sacrificial silver layer, which is covering PEDOT:PSS layer. Next, using suitable silver etchant such as nitric acid, the silver interlayer is selectively removed, exposing PEDOT:PSS segments that can be etched by oxygen plasma. After stripping the photoresist and etching the remnant silver islands, PEDOT:PSS patterns can be manufactured on Si wafer substrates. Taylor et al.[42] have

also shown that even nanoscale PEDOT:PSS patterns can be realized by utilizing orthogonal solvents along with corresponding photoresist, and by introducing a new set of benign processes that involve new specially tailored photopolymers. Finally, it has been demonstrated that a picosecond laser direct ablation with 355 nm and 1064 nm wavelength pulses can be successfully used[43, 44, 45] to pattern PEDOT:PSS.

In summary, the important challenges with using PEDOT:PSS as for highly conductive films, remain to be patterning, adhesion to the substrate, material compatibility, and reaching conductivity in excess of 10^3 S cm^{-1}.

A.2 Device Fabrication

A commercial dispersion of PEDOT:PSS (1.3wt% dispersed in H_2O, conductive grade) in water was purchased from Sigma-Aldrich and used to deposit organic films. The dispersed solution has a composition of 0.5wt.% PEDOT and 0.8wt.% PSS. This PEDOT:PSS dispersion was spin-coated onto cleaned substrates. The cleaning was performed by first placing cleaved rectangular pieces of oxidized Si wafers and biaxially-oriented polyethylene terephthalate (BoPET called also Mylar) of size larger or equal to 1.5 cm $\times$ 1.5 cm into an acetone bath and sonicated for at least 10 min. Subsequently, the substrate pieces were then transferred into an isopropyl alcohol (IPA) bath and sonicated for a further 10 min. The substrates were then subsequently rinsed with deionized (DI) water followed by a blow dry with nitrogen and then placed onto a prewarmed hot plate (110°C) for 1–2 min to dehydrate.

Initial spin-coating of PEDOT:PSS did not succeed at all—no PEDOT:PSS could be detected on the wafer. The solution to the non-uniform coverage of PEDOT:PSS onto the substrates was the introduction of an O_2 plasma cleaning step immediately before spin-coating. Oxygen plasma in the SAMCO RIE chamber has been used with the power of 50W for 30 s at an

oxygen flow rate of 20 sccm. It was ensured that the reflective power is less than 1 Watt. (In the case of mylar, the substrate pieces were taped to an oxidized Si wafer carrier in order to prevent flipping over while the RIE chamber is outgassing.) Immediately after the plasma treatment, the samples were moved to the spinner. The best uniformity of the PEDOT:PSS films was achieved with a two-step recipe:

Step 1: Spin speed 500 rpm, ramp 200 rpm/s, duration 10 s.

Step 2: Spin speed 2000 (1500)rpm, ramp 500 rpm/s, duration 45 s.

The above two cycles were modified from a standard photoresist deposition. The ramping parameters and spinning times have been varied to obtain optimum uniformity results. The final thickness of the PEDOT:PSS films for the maximum spin speeds of 1500, 2000 and 3000 rpm were 65, 56, and 29 nm, respectively.

After spin-coating, the samples were soft-baked on a hot plate at temperature 120°C for 10 min to solidify the films. A lower temperature of 95°C has been used for the soft bake, compatible with the photoresist soft bake, but no difference in conductivity was observed.

The thickness of PEDOT:PSS films was measured with a Dektak profilometer and atomic force microscope (AFM), whose measurements were within $\pm$ 1 nm of each other. The uniformity of the PEDOT:PSS film both on oxidized Si wafers and on Mylar was also determined to be $+/-$ 2 nm. In the case of Mylar, it was found that for reliable thickness measurements, the area of the Mylar pieces must be at least 1.5 cm $\times$ 1.5 cm. Otherwise, the PEDOT:PSS exhibited rough edges and pooling of the material in the corners of the substrate. After patterning the PEDOT:PSS, the thickness of the PEDOT:PSS lines were $\sim$ 4 nm, and lower in the center than at the edges, caused by the etching of Ag sacrificial layers in HNO_3 solution.

The main body of research was devoted to the enhancement of electrical conductivity of the

PEDOT:PSS films. The pristine PEDOT:PSS at 2000 rpm exhibited a sheet resistance RS of about 1 MΩ/sq at a film thickness of 56 nm. According to the Eq. (1)

$$\sigma = \frac{1}{R_s \times t} \tag{A.1}$$

The electrical conductivity σ is the inverse of the product of sheet resistance and film thickness. Thus, a sheet resistance of 1 MΩ/sq at a film thickness of t = 56 nm corresponds to $\sigma = 0.18$ S/cm.

A number of different methods of enhancing PEDOT:PSS conductivity have been undertaken, including multiple spin coatings and doping the film with either Cu nanoparticles. Two kinds of Cu NP with 25 nm and 60−80 nm particle size from Sigma Aldrich[46] were used. Since Cu NP are easily oxidized in aqueous solutions at ambient temperatures, suspending Cu NP directly in the aqueous PEDOT:PSS dispersion was avoided.

Instead, both sizes of the Cu nano-powder (NP) were separately dispersed in ethanol at two different concentrations: 0.2, and 0.5 mg/ml. A solution of 10 ml ethanol with the mentioned concentrations of Cu NPs for each kind was prepared. This solution was then stirred for an hour followed by ultrasonication for another 1 h. The Cu-ethanol dispersion was then spin-coated on top of a PEDOT:PSS layer using the same spin-coating recipe as for the PEDOT:PSS.

In order to further prevent oxidation of the Cu NP, the as-spun film was not soft baked. Instead, the sample was allowed to air dry for at least 5 min, during which the excess ethanol evaporated. The spinning of the Cu dispersion onto PEDOT:PSS did not measurably increase the thickness of the PEDOT:PSS film.

In order to pattern PEDOT:PSS using conventional lithography, the PEDOT:PSS film must

be protected from exposure to the UV light during photoresist exposure. Additionally, PEDOT:PSS is damaged during photoresist deposition, development, and the removal step due to interaction with chemical reagents, especially the aqueous alkaline solutions used widely in conventional photolithography. Due to the acidity of PEDOT:PSS films, the crosslinking of traditional acid-sensitive photoresists is also adversely affected. Furthermore, acidic PEDOT:PSS films may cause decomposition of a positive photoresist layer. Chromium (Cr) or silver (Ag) thin films deposited by Physical Vapor Deposition (PVD) with a thickness of 100 nm were used as a protective layer on top of the photoresist during patterning. The Ag layers were superior to Cr layers, as the latter displayed partial peeling when rinsed in DI water, indicative of poor adhesion to the PEDOT:PSS film. After a photolithography step and development of the positive resist AZ 5214E-IR using the developer AZ300 MIF, the exposed Ag regions were etched in a 5:8 solution of HNO3: H2O for about 11–12 s, until visible removal of Ag was observed. After the 12 s HNO_3 etch the sample was rinsed twice in DI water. The uncovered PEDOT:PSS layer was removed in a Samco RIE chamber using oxygen plasma at 50 W for 30 s at an O_2 flow rate of 20 sccm. In the case of mylar, the rectangular pieces of mylar were taped down to the chuck to prevent lifting while the chamber is outgassing. Subsequently, the sample was sprayed with acetone for 30 s to remove the remaining photoresist material. Lastly, the remaining sacrificial Ag layer is removed when the samples are dipped in the HNO_3: H_2O (5:8) solution for 11–12 s, thus uncovering the patterned PEDOT:PSS.

The process flow of the photolithographic patterning of PEDOT:PSS is shown in Figure A.1. In Figure A.2 optical pictures of the patterns on oxidized Si wafers after every process step explained in A.1 are shown. Figure A.3 shows optical picture of the same photolithography patterning process on Mylar flexible substrate. Here, the optical pictures of step 2 and 6 are shown together with a piece of flexed Mylar with PEDOT:PSS patterns.

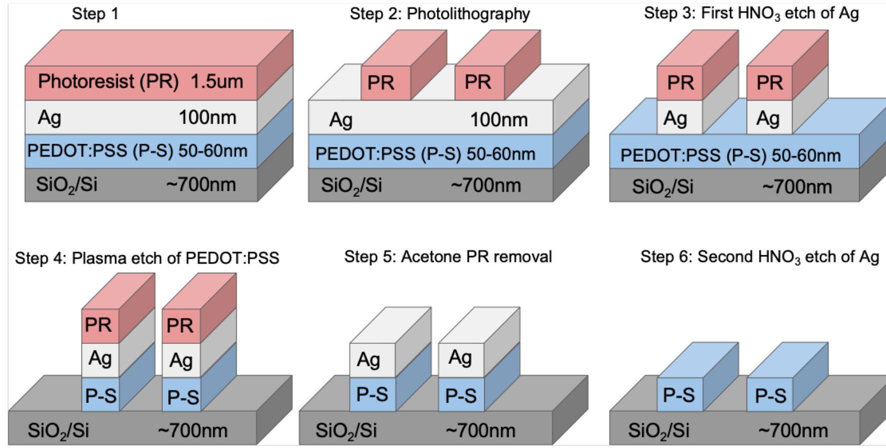


Figure A.1: Photolithography process flow to pattern PEDOT:PSS films on oxidized Si wafers and on Mylar flexible substrates using Ag as sacrificial layer to protect PEDOT:PSS from damage during the photolithography exposure and photoresist ashing.

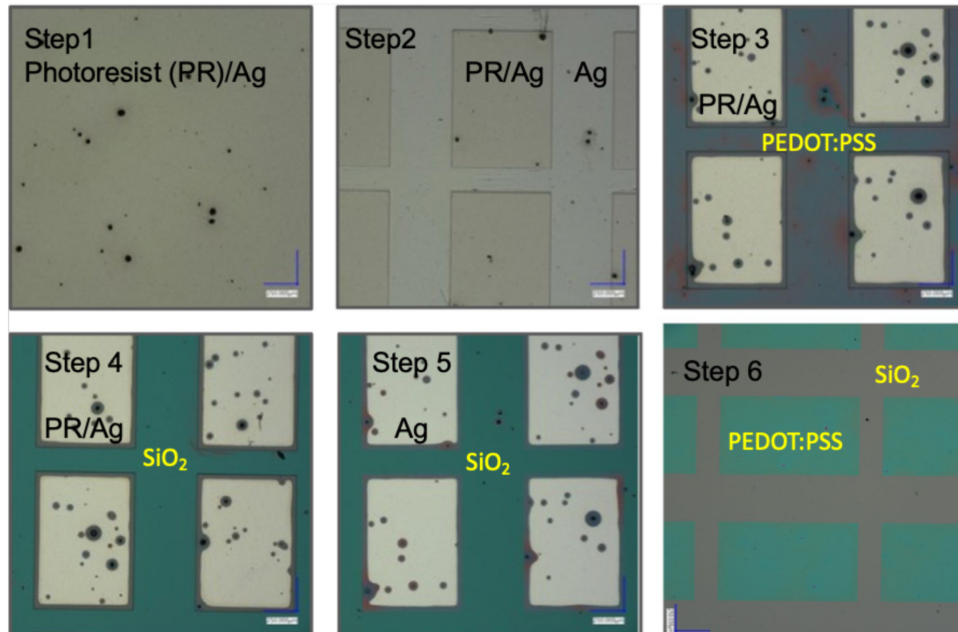


Figure A.2: Optical pictures of the patterning process of PEDOT:PSS on an oxidized Si wafer. The six steps correspond to the six steps of the photolithography process flow shown in Figure A.1

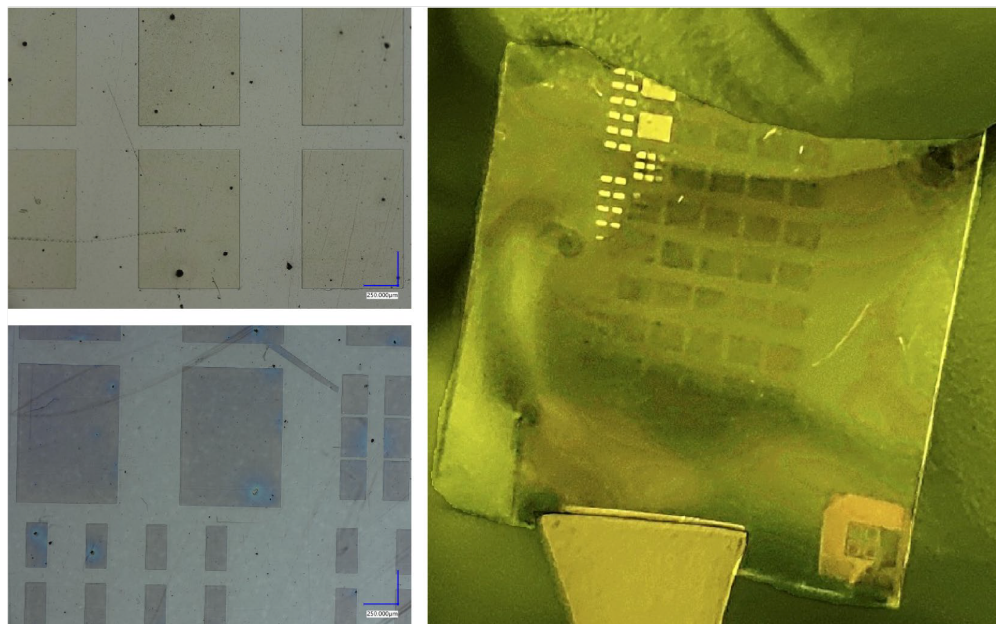


Figure A.3: PEDOT:PSS patterning on Mylar flexible substrate. (a) patterning of the photoresist of the layer stack PR/Ag/PEDOT:PSS/Mylar. (b) The final PEDOT:PSS patterns on Mylar. (c) 2 × 2 cm piece of Mylar with PEDOT:PSS patterns on it.

A.3 Results and Discussion

The most surprising result of conductivity enhancement of the PEDOT:PSS has been achieved by multiple spin coatings of the PEDOT:PSS and added Cu NP dispersion. The results are summarized in Table ??.

Sample #	**Description**	**Sheet resistance** [Ω/sq]
1	PEDOT:PSS 1 layer (2000 rpm)	1 M
2	PEDOT:PSS 1 layer (1500 rpm)	230 k
3	PEDOT:PSS 2 layers (1500 + 2000 rpm)	90 k

4	PEDOT:PSS 2 layers (3000 rpm)	85 k
5	PEDOT:PSS 2 layers (1500 rpm)	80 k
6	PEDOT:PSS 3 layers (1500 rpm)	60 k
7	PEDOT:PSS 3 layers (3000 rpm)	28 k
8	PEDOT:PSS 3 layers (1500, 1500, 3000 rpm)	12 k
9	PEDOT:PSS 3 layers (1500, 2000, 3000 rpm)	18 k
10	PEDOT:PSS 3 layers (1500, 3000, 1500 rpm)	21 k
11	PEDOT:PSS 1 layer+Cu(25 nm) 0.2 mg/ml @ 2000 rpm	1.2 k
12	PEDOT:PSS 2 layers+Cu(25 nm) 0.2 mg/ml @ 2000 rpm	467
13	PEDOT:PSS 2 layers+Cu(25 nm) 0.5 mg/ml @ 2000 rpm	459
14	PEDOT:PSS layer+Cu(25 nm) 0.2 mg/ml @ 2000 rpm+PEDOT:PSS layer	1.2 k
15	PEDOT:PSS 2 layers+Cu(60 nm) 0.2 mg/ml @ 2000 rpm	390
16	PEDOT:PSS 3 layers+Cu(60 nm) 0.5 mg/ml @ 1500 rpm	173

17	PEDOT:PSS 3 layers+3×Cu(60 nm) 0.5 mg/ml @ 1500 rpm PEDOT:PSS and Cu @1500 rpm	162
18	3x[PEDOT:PSS layer+Cu(60 nm) 0.5 mg/ml @ 1500 rpm]	1 k
19	PEDOT:PSS 3 layers (1500, 1500, 3000 rpm)+1×Cu(60 nm) 0.5 mg/ml	200
20	PEDOT:PSS 3 layers (1500, 3000, 1500 rpm)+1×Cu(60 nm) 0.5 mg/ml	261
21	PEDOT:PSS 3 layers (1500, 2000, 3000 rpm)+1×Cu(60 nm) 0.5 mg/ml	256
22	PEDOT:PSS 4 layers (1500, 2000, 3000, 3000 rpm)	4.8K
23	PEDOT:PSS 5 layers (1500, 2000, 3000, 3000, 3000 rpm)	2.3K
24	PEDOT:PSS 6 layers (1500, 2000, 3000, 3000, 3000, 3000 rpm)	972
25	PEDOT:PSS 6 layers (1500, 2000, 3000, 3000, 3000, 3000 rpm)+Cu (60 nm) 0.5 mg/ml	62

Table A.1: Samples with various processing steps and the resulting sheet resistance. The process steps to enhance electrical conductivity are discussed in the text.

The doubling of the PEDOT:PSS layer alone decreases the sheet resistance by more than

tenfold, from 1 MΩ/ sq (sample 1) to 90 kΩ/sq (sample 3) and 85 kΩ/sq (sample 4) depending on the spinning speed. A deposition of a third PEDOT:PSS layer reduced the sheet resistance further to 60 kΩ/sq (sample 6) and even to 28 kΩ/ sq (sample 7) depending on the spinning speed. Even more surprising is the finding that the thickness of the PEDOT:PSS coated twice (twice the entire coating cycle including the annealing step) and thrice does not change the final thickness appreciably. The thickness of a triple deposition at 1500 rpm, 3000 rpm and 1500 rpm gives a final thickness of 85 nm. If the depositions would be strictly additive it would be 65 + 29 + 65 = 159 nm. Of course, the spinning speed impacts the final thickness. Thus, for example a triple PEDOT:PSS deposition with consecutively higher speeds: 1500 rpm, 2000 rpm, and 3000 rpm gives a total film thickness of 72 nm, which is only 7 nm thicker than a single layer PEDOT:PSS deposited at 1500 rpm and far less than the additive number of 65 + 56 + 29 = 150 nm. As mentioned in the introduction during the spinning a vertical dephasing of the PEDOT and PSS components takes place. The wet film contains the conductive PEDOT strips at the bottom of the film and a PSS-rich solution at the upper part. During the subsequent soft bake at 120°C these segregated layers have insufficient time for remixing. The explanation for the phenomenon is given in Figure A.4, where the PSS-rich top layer and the PEDOT-rich bottom layer are shown in a schematically simplified way. There is, of course, no sharp transition between the two phases, but a gradual one, with high concentration of PSS at the top and lowest at the bottom with the reverse behavior of the PEDOT. As pointed out in the introduction, during the spin deposition of PEDOT:PSS the hydrophobic PEDOT-rich phase settles at the bottom of the film and the hydrophilic PSS-rich phase at the top of the PEDOT:PSS film. During the second spin coating the hydrophilic PSS top portion of the film gets exposed to water and is partially supplanted by PEDOT-rich phase.

The same happens during the third spin-coating (samples 6–10) with further lowering of

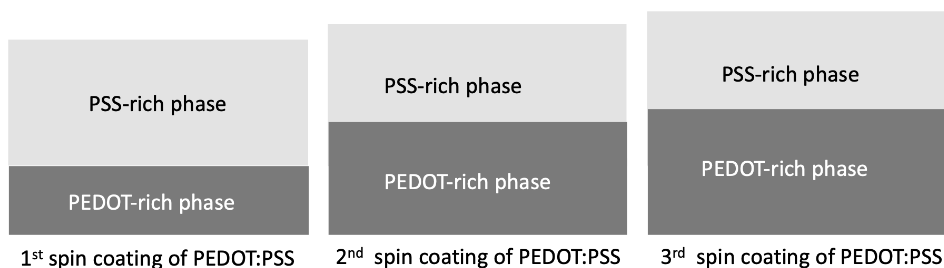


Figure A.4: Explanation of how multiple PEDOT:PSS coatings enhance the electrical conductivity of the film. As explained in the text, the thicknesses of a double layer, and a triple layer increase only very slightly over the thickness of a single layer. The multiple coatings help to supplant the PSS top portion of the layer with PEDOT:PSS ribbons.

the sheet resistance to 12 kΩ/sq (sample 8). As a result, the PEDOT-rich phase grows at the expense of the PSS-rich phase. As the conductive PEDOT-rich phase increases after repeated coating cycles, the electrical conductivity of the PEDOT:PSS film is significantly improved. During the second and third spin coating the wet film helps remove the PSS material and supplant it with conductive PEDOT phase. Consequently, the conductivity increases significantly. The spinning speed has an interesting effect on the conductivity of the PEDOT:PSS films. Sample 8 differs from sample 6 only in the spinning speed of the 3rd PEDOT:PSS layer of 3000 rpm instead of 1500 rpm. The higher speed during the third PEDOT:PSS deposition lowers the sheet resistance by a factor of 5 from 60 kΩ/ sq to 12 kΩ/sq. The explanation for this effect is consistent with explanation given in Figure A.4. The higher speed of the 3rd deposition does not decrease the thickness of the PEDOT:PSS film because the thickness of the overall film is given chiefly by the first coating while the subsequent depositions serve only to densify the PEDOT phase at the bottom portion of the layer forcing this increased connectivity between the PEDOT ribbons.

To verify this assumption, the sheet resistance of a single PEDOT:PSS layer spun at 1500 rpm has been found to be 230 kΩ/sq, (sample 2) i.e. 77% lower than the one with PEDOT:PSS spun at 2000 rpm (sample 1). Two layers of PEDOT:PSS both at spun at 3000 rpm (sample

4) resulted in 85 kΩ/sq roughly in the same range (80 kΩ/sq) as 2 layers spun at 1500 rpm (sample 5). Three layers of PEDOT:PSS (sample 7), with all three coatings spun at 3000 rpm, result in Rsq= 28 kΩ/sq. This demonstrates a tradeoff between the more denser phase of PEDOT attained at higher speed rates and the thickness of the layer. The denser PEDOT phase decreases Rsq while a thinner PEDOT:PSS layer tends to increase R_{sq}. Hence, the optimum solution consists in taking advantage of both factors by spinning the first two PEDOT:PSS layers at a lower rate to safeguard a thicker polymer film and add a third layer spun at higher speed to reach higher densification of the PEDOT phase. Samples 8, 9, and 10 show further combinations of the spinning speed combinations. Sample 9 with a sequence of spinning speeds (1500 rpm, 2000 rpm, 3000 rpm) shows a sheet resistance of 18 kΩ/sq. Sample 10 with the spinning speed combination (1500 rpm, 3000 rpm, 1500 rpm) yields a sheet resistance of 21 kΩ/sq. Sample 8, 9, and 10 show that it is advantageous to perform the first two depositions at low speed to provide a thicker PEDOT:PSS layer and use high speed during the third deposition to attain high PEDOT densification at the bottom of the layer.

To see the impact of multiple coatings, we have increased the number of sequential PEDOT:PSS coatings to six coatings, such that the sample with n coatings shares exactly the same (n-1) PEDOT:PSS layers as the sample with (n-1) coatings. In this particular sequence, the 1 × layer PEDOT:PSS sample is sample 2 deposited at 1500 rpm, the second sample is sample 3 with two layers deposited at 1500 rpm and 2000 rpm, respectively. Each additional PEDOT:PSS coating has been deposited at 3000 rpm to maximize the conductivity. The samples with 4 × PEDOT:PSS, 5 × PEDOT:PSS, and 6 × PEDOT:PSS are listed in Table A.1 as sample 22, 23, 24, respectively.

The results of the sheet resistance for the multiple coatings are given in Table A.2 and plotted in Figure A.5.

#P/S layers	**1**	**2**	**3**	**4**	**5**	**6**
R_{sq} in kΩ	230	90	18	4.8	2.3	0.98

Table A.2: Sheet resistance R_{sq} versus number of PEDOT:PSS (P/S) coatings

From Figure A.5 an exponential dependence of the sheet resistance as function of the number of PEDOT:PSS coatings has been found. The exponential trendline in Fig. 5 can be fitted by the following expression $R_{sq}(n) = 230\ k\Omega \times \exp[-(n-1)\times 1.28]$. Thus, it can be seen that further PEDOT:PSS coatings would provide diminishing returns. We will revisit the multiple coatings of PEDOT:PSS in the context of the efficiency of doping by Cu NP of multiple PEDOT:PSS coatings in reducing the overall sheet resistance. In our approach

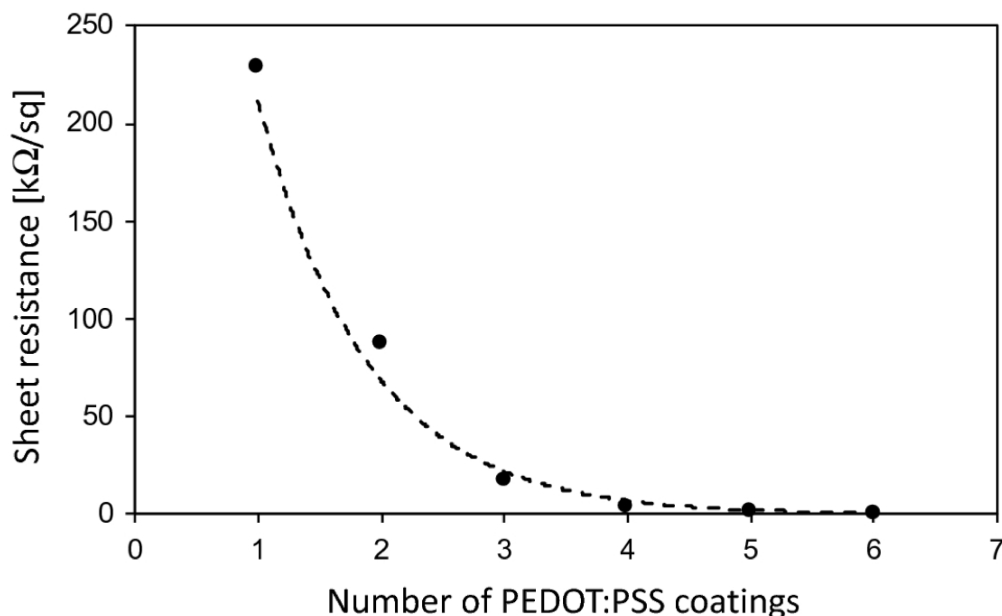


Figure A.5: The sheet resistance, R_{sq}, of the multiple PEDOT:PSS coatings as a functions of the number of coatings, n. An exponential dependence between $R_{sq}(n)$ and n is found and can be expressed as $R_{sq}(n) = 230\exp[-(n-1)\times 1.28]$ kΩ.

to add Cu NP to the film we have chosen to add Cu NP at the top after the soft-bake of the spin-coated PEDOT:PSS. In contrast to Ag and Au NPs[31, 33], which can be added to the PEDOT:PSS dispersion and spin coated together with it, the dispersion of Cu NP is

difficult and ineffective[47] because Cu is easily oxidized at ambient temperatures. In fact, our experiments confirmed this assessment. After mixing 0.5 mg/ml Cu(60 nm) NP with PEDOT:PSS in the same aqueous solution to deposit a single PEDOT:PSS layer doped with Cu NP, the sheet resistance of one PEDOT:PSS layer doped in such a way with Cu NP, increased slightly from 1 MΩ/sq to 1.2 MΩ/sq. (This sample is not being listed in the Table A.1, because such step increases the sheet resistance instead of lowering it). When incorporated Cu NP in an aqueous solution together with PEDOT:PSS, the oxidized Cu NPs cause even more isolation between the PEDOT ribbons. However, when spinning the PEDOT:PSS dispersion with the Cu NPs three times, the sheet resistance of the triple PEDOT:PSS(Cu NP) dropped to 44.4 kΩ/sq. (This sample is also not listed in the Table A.1). This result indicates that some of the Cu NP managed to avoid oxidation and enhanced the conductivity by helping bridge electrically the PEDOT ribbons. Of course, such problems would have been avoided, when instead of Cu NP, Au or Ag NPs would have been used. Still, since Cu NPs are more economical and more desirable because of their proven ReRAM switching properties, experiments have been continued with Cu NP being now dispersed in ethylene and deposited on top (to avoid any contact with moisture) of an annealed PEDOT:PSS.

Table A.1 shows that the addition of dispersion of Cu NP at the top of the PEDOT:PSS further dramatically increases the conductivity of the film. A single layer of PEDOT:PSS with 0.2 mg/ml Cu(25 nm) (sample11) lowers the sheet resistance from 1 MΩ/sq to 1.2 kΩ/sq. The combination of 2 layers of PEDOT:PSS with Cu deposited last (sample 12) gives a sheet resistance of 467 and 390 Ω/sq for 25 nm sized and 60 nm-sized Cu NP (sample 15), respectively, indicating that a larger size of Cu NPs is more effective in lowering the sheet resistance. A combination of 3 layers of PEDOT:PSS and with a top layer of Cu NP (60 nm) (sample 16) yields 173 Ω/sq. As can be seen from sample 17, the additional two Cu NP coatings resulted in a marginal improvement from 173 to 162 Ω/sq. Sample 18 is

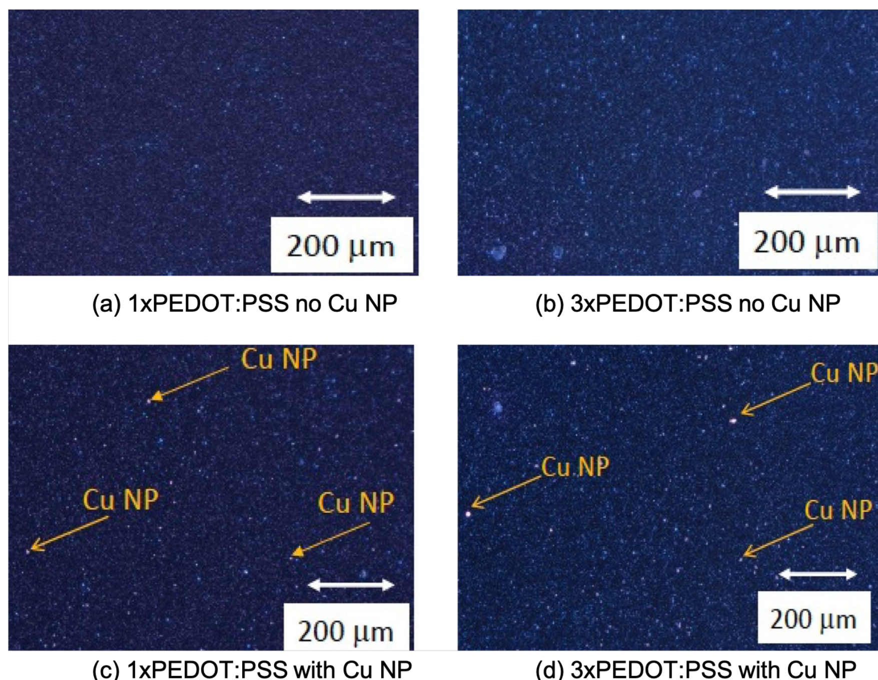


Figure A.6: Optical microscope picture of PEDOT:PSS with and without Cu NP. (a) single coating of PEDOT:PSS deposited at 1500 rpm with no Cu NP. (b) a triple coating of PEDOT:PSS at 1500 rpm with no Cu NP. (c) a single coating of PEDOT:PSS deposited at 1500 rpm doped with 0.5 mg/ml of Cu NP. (d) a triple coating of PEDOT:PSS deposited at 1500 rpm doped with 0.5 mg/ml of Cu NP.

similar to the sample 17, however in sample 17 the Cu dispersion on top of the three layers of PEDOT:PSS has been coated three times with Cu NP. In samples 14 and 18 we investigated the effect of Cu NP coating after deposition of every PEDOT:PSS layer. The resulting sheet resistance is rather high of 1.2 kΩ/sq and 1.0 kΩ/sq, respectively. The likely reason for the high resistance is that the efficacy of the Cu NP doping due to the Cu NP deposition on the first two PEDOT:PSS layers is degraded by the oxidation when aqueous PEDOT:PSS is being deposited on top of the Cu NP coating. It can, thus, be seen that the effects of multiple spin coatings of PEDOT:PSS and of Cu NP are by no means additive and depend sensitively on the sequence of coatings. In some cases they work synergistically, but in other combinations they can be detrimental to the lowering of sheet resistance. The multiple coatings of PEDOT:PSS, however, appear to be beneficial in all circumstances envisioned

#P/S layers	no Cu NP	w/Cu NP	Red. fact.
1	230	60	3.8
3	18	0.173	104
6	0.98	0.062	15.8

Table A.3: R_{sq} in units of kΩ for multiple coatings with and without Cu NP doping. The reduction factor (Red. Fact.) of R_{sq} by the Cu NP is also indicated.

here, since they increase the volume of the PEDOT-rich bottom layer and provide a larger potential for conductivity enhancement by metal NP doping, including the Cu NPs. At the same time, due to the nature of particle diffusion, the highest concentration of Cu NPs remains at the top portion of the PEDOT:PSS film that is initially the most resistive part of the film and rendering it significantly more conductive as shown in Figure A.6.

In Table A.3 the interaction between the number of PEDOT:PSS coatings and doping with Cu NP and its impact on Rsq is elucidated. It can be seen that the relative reduction due to addition of Cu NP is strongest for 3 PEDOT:PSS layer, where the reduction factor is more than two orders of magnitude. In case of 6 PEDOT:PSS layers the reduction factor is only one order of magnitude, whereas the reduction factor for a single PEDOT:PSS layer is less than 4. This particular behavior will become clear when the morphology of the doped and undoped PEDOT:PSS films with multiple coatings will be discussed further below.

The presence of Cu NP at the top of the PEDOT:PSS has the added advantage of making Cu^+ available for the resistive switching behavior as observed in many ReRAMs including in Cu/TaO_x/Pt[48] and Cu/P3HT(GNP)/Au[49] memory cells. As seen from Table A.1 larger size of Cu NP, 60 nm vs. 25 nm, helps also to enhance the electric conductivity of the film. Samples 19, 20, and 21 (samples with three PEDOT:PSS layers with Cu (60 nm) NP deposition) and samples 8, 9, and 10, also with three PEDOT:PSS layers with no Cu deposition show similar trends with respect to the spinning speeds of the PEDOT:PSS

depositions, confirming that lower spinning speed of the first two depositions followed by a high-speed deposition of the third layer yield the lowest sheet resistance.

The synergistic effect of multiple coatings, Cu dispersion, and the concomitant soft-bakes can be further optimized to attain even higher conductivities of the film. From Table A.1 it can be also seen that the concentration of Cu NP dispersion has a slight enhancement on the enhancement of the conductivity. The comparison of 0.2 mg/ml (sample 12) and 0.5 mg/ml (sample 13) shows that higher concentration of Cu NP in the dispersion leads to a slightly lower sheet resistance.

Since the method of Cu NP doping as a surface layer in conjunction with the multiple PEDOT:PSS coatings proved to be very effective, it was attempted to further optimize the Cu deposition process. In Table A.2 we show the results of samples with a triple PEDOT:PSS layer and different Cu NP deposition recipes with subsequent soft bakes at various temperatures are shown. For samples 26–29 the spinning speed of the Cu NP dispersion solution has been lowered from 1500 to 500 rpm in the attempt to increase the thickness of the Cu dispersion coating and thus the Cu concentration on top of the 3rd PEDOT:PSS layer. Then the quadruple layer systems have been annealed between room temperature and 120°C. From Table A.4 it can be seen that the change of the sheet resistance as function of soft bake at temperatures from 60°C to 120°C is insignificant. The soft bake at 60°C appeared to improve the sheet resistance only slightly, but the subsequent soft bakes at 90°C and 120°C degraded the sheet resistance by 6% and 21%, respectively.

Comparing samples 4 and 5 with two PEDOT:PSS layers it can be seen that the maximum spinning speed had a slight effect on the conductivity: the conductivity for the maximum speed of 3000 rpm for both PEDOT layers is 85 kΩ/sq and rotating both layers at 1500 rpm resulted in 80 kΩ/sq, while rotating the first PEDOT:PSS layer at 1500 rpm and the second at 2000 rpm resulted in a sheet resistance of 90 kΩ/sq (sample 3). Two PEDOT:PSS

Sample#	Description	Sheet resistance [Ω/sq]
26	PEDOT:PSS 3 layers + Cu(60 nm) 500 rpm; no soft bake	189
27	PEDOT:PSS 3 layers + Cu(60 nm) 500 rpm; soft bake @ 60 °C 10 min	184
28	PEDOT:PSS 3 layers + Cu(60 nm) 500 rpm; soft bake @ 95 °C 10 min	195
29	PEDOT:PSS 3 layers + Cu(60 nm) 500 rpm; soft bake @ 120 °C 10 min	234

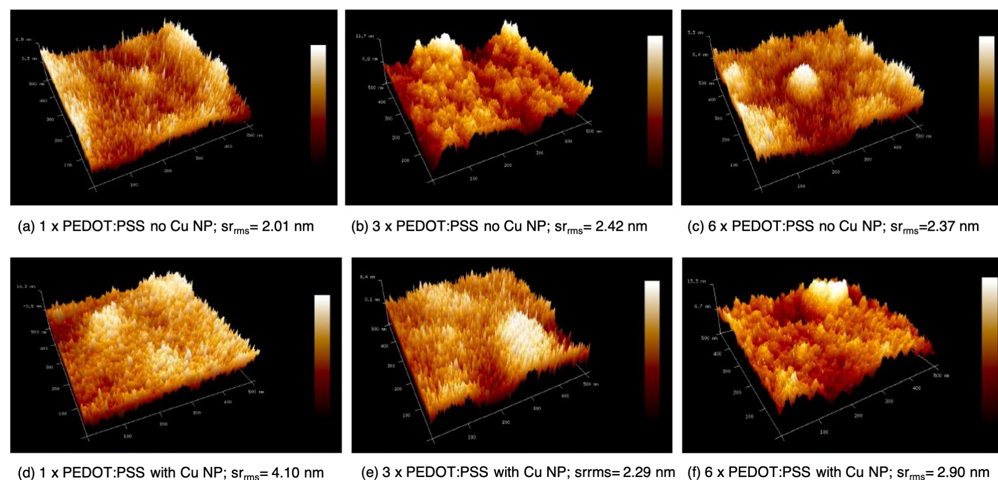
Table A.4: Impact of Cu NP deposition parameters and subsequent soft bake on the sheet resistance of the film.

layers at 2000 rpm (not listed in Table A.1) has a sheet resistance of 99.7 kΩ/sq. This result indicates that the sheet resistance increases with the spinning speed caused by the thinning of PEDOT:PSS layer with higher spinning speeds.

The two most promising approaches, i.e. the double PEDOT layer and doping with Cu NP were combined in two separate configurations. In the first configuration, the Cu NP were spun after the deposition of the first PEDOT layer at 2000 rpm. and the second configuration consisted in a double layer PEDOT:PSS deposition, followed by another deposition of the Cu NP. The first configuration yielded a sheet resistance of 1.2 kΩ/sq (sample 11) and the second resulted in a very low sheet resistance of only 467 Ω/sq (sample 12).

A.4 Morphology of the PEDOT:PSS Films

To characterize the PEDOT:PSS films morphologically optical microscope pictures of the PEDOT:PSS films for multiple coatings have been taken with and without Cu NP as well as Atomic Force Microscopy (AFM) to assess the surface roughness of the films. In Figure



(a) 1 x PEDOT:PSS no Cu NP; sr_{rms}= 2.01 nm (b) 3 x PEDOT:PSS no Cu NP; sr_{rms}= 2.42 nm (c) 6 x PEDOT:PSS no Cu NP; sr_{rms}=2.37 nm

(d) 1 x PEDOT:PSS with Cu NP; sr_{rms}= 4.10 nm (e) 3 x PEDOT:PSS with Cu NP; srrms= 2.29 nm (f) 6 x PEDOT:PSS with Cu NP; sr_{rms}= 2.90 nm

Figure A.7: AFM pictures of PEDOT:PSS of a single, triple, and sixfold coatings of PEDOT:PSS with and without Cu NP. The scanned area of all the plots is 500 nm $\times$ 500 nm. The root mean square surface roughness, sr_{rms}, is also indicated for the respective surface surface. (a) a single PEDOT:PSS no Cu NP; $sr_{rms} = 2.01$ nm, (b) a triple PEDOT:PSS no Cu NP; $sr_{rms} = 2.42$ nm, (c) a sixfold PEDOT:PSS no Cu NP; $sr_{rms} = 2.37$ nm, (d) a single PEDOT:PSS with Cu NP; $sr_{rms} = 4.10$ nm (e) a triple PEDOT:PSS with Cu NP; $sr_{rms} = 2.29$ nm, (f) a sixfold PEDOT:PSS with Cu NP; $sr_{rms} = 2.90$ nm.

A.6 the optical microscope pictures of 1-coating, and 3-coatings of PEDOT:PSS films with and without Cu NP are shown. It can be seen that multiple coatings increase the density of PEDOT:PSS particles seen in the pictures as small white dots. The triple coating of PEDOT:PSS has a more pronounced whitish tint compared with the single PEDOT:PSS coating, indicating a higher density of the PEDOT:PSS composites. The single PEDOT:PSS layer displays wider gaps between the PEDOT:PSS particles rendering the optical image contrast darker. In case of PEDOT:PSS films doped with Cu NP one can distinguish only part of them recognizable by an orange-reddish glow. They can be easily spotted because of the their relatively large size between 60 and 80 nm. If one tilts the sample only so slightly under the microscope, other Cu NP can be seen, when the orientation of their facets cause visible reflection of the light into the camera. The Cu NP appear to settle in places where the density of PEDOT:PSS particles is low. Thus, they tend to fall in the cavities between the PEDOT:PSS particles. Additional information can be gained from AFM pictures of the

surfaces of the corresponding PEDOT:PSS films. Of course, the AFM pictures are insensitive to the material differences. In Figure A.7, AFM pictures of selected PEDOT:PSS films are shown. In Table A.5, the root mean square (rms) surface roughness of the AFM plots for the respective samples, has been summarized.

It can be seen that for one coating of PEDOT:PSS the surface roughness with Cu NP is much higher than without Cu NP. This is plausible since the film thickness of 1×PEDOT is ca. 65 nm and the size of Cu NP is between 60 and 80 nm. Thus, inevitably, some Cu NP are bound to stick out, contributing to a higher surface roughness. Nevertheless, the relative low density of PEDOT:PSS particles are able to accommodate the Cu NP is the empty spaces between them as only a small upper part of the Cu NP is sticking out. In case of 3×PEDOT:PSS the film thickness is 85–90 nm and the density of PEDOT:PSS still low enough allowing sufficient free space to accommodate the Cu NP entirely in the film. From Table A.5 it can be seen that the surface roughness with Cu NP is now lower than without them (in contrast to the case with one coating and six coatings). The lower surface roughness with Cu NP is likely to be caused by the fact that now the PEDOT:PSS film thickness is larger than the largest Cu NP and the density of PEDOT:PSS composite particles is low enough to accommodate Cu NP entirely within the film. In case of 6×PEDOT, the film thickness is higher than for 3×PEDOT:PSS but the density of PEDOT:PSS is now so high that there are fewer empty spaces to accommodate the Cu NP, thus the surface roughness with Cu NP is somewhat higher than without them (see Table A.5). The results in Table A.5 correlate perfectly with the findings of the sheet resistance's dependence on the number of PEDOT:PSS coatings and the reduction factor of the sheet resistance due to the addition of Cu NP, shown in Table A.5. The Cu NP have the strongest, relative, impact when the film thickness is equal or larger than the size of Cu NP and the film can offer enough empty space between the PEDOT:PSS particles to accommodate the Cu NP entirely between them. In

PEDOT:PSS sample	no Cu NP	w/Cu NP
1 × PEDOT:PSS	2.01	4.10
3 × PEDOT:PSS	2.42	2.29
6 × PEDOT:PSS	2.37	2.90

Table A.5: rms surface roughness (SR) in [nm] of PEDOT:PSS films with multiple coatings with and without Cu NP doping.

addition to the doping techniques demonstrated here, other promising enhancement methods include doping of PEDOT:PSS with Au or Ag NPs or treatment of PEDOT:PSS with acids such as HNO_3, H_2SO_4. The optimum combination will depend on the integration issues of PEDOT:PSS electrodes with possible PEDOT:PSS switching layers into a final organic ReRAM cell. Although the manufacturing of high conductivity of the films is an important objective, the switching performance of a purely organic ReRAM memory cell is even more important, rendering the process integration and optimum combination of enhancement techniques, a non-trivial task.

A.5 Summary

We have presented new methods of enhancing the electrical conductivity of PEDOT:PSS layers. It was shown that multiple spin coatings of PEDOT:PSS by itself can lower the sheet resistance by more than two orders of magnitude, while not appreciably increasing the total thickness of the layer. It was found that the spinning speed of every coating plays a sensitive role, where the first coating should be deposited at a lower speed to establish the thickness of the final PEDOT:PSS layer. The subsequent coatings should be done at higher speeds which, apparently, lead to the growth and densification of the PEDOT ribbons at the bottom of the layer. An exponential dependence between the sheet resistance and the number of

PEDOT:PSS coatings has been demonstrated. Despite negative findings on the use of doping by Cu NP[47], Cu NP doping proved a viable conductivity enhancement technique, provided that it is deposited on an already baked PEDOT:PSS film, rather than pre-mixing the Cu NP with the aqueous dispersion of PEDOT:PSS. Coating the surface of PEDOT:PSS with Cu NP can result in reduction in the sheet resistance by four orders of magnitude. Higher concentrations and larger sizes of Cu NP help further decrease the sheet resistance, albeit not substantially. It was also demonstrated that these high conductivity PEDOT:PSS films can be patterned both on oxidized Si wafers and flexible Mylar substrate using sacrificial metal layer to protect PEDOT:PSS from the damage caused by the photolithography process.

Present results may be combined with already known techniques to further increase the conductivity of PEDOT:PSS such as acid treatment (H_2SO_4, H_3PO_4, or H_3BrO_3) and the doping of PEDOT:PSS with Au and Ag NPs. These options are reported in a different manuscript as given in Appendix B.

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Observation of Quantized and Partial Quantized Conductance in Polymer-Suspended Graphene Nanoplatelets. *Nanoscale Research Letters*, 11(1):179, April 2016.

Appendix B

Methods to Enhance Electrical Conductivity of PEDOT:PSS-based Electrodes

This appendix chapter has been reproduced from a manuscript that is under preparation titled ***Methods to Enhance Electrical Conductivity of PEDOT:PSS-based Electrodes*** *authored by* ***Amrita Chakraborty, Aaron DiFilippo, Sheena Deivasigamani, Calvin Hong, Anshu Madwesh, and Marius Orlowski.****[1]*

This chapter extends our prior study on enhancing Poly(3,4- ethylenedioxythiophene) Polystyrene Sulfonate (PEDOT:PSS) electrode conductivity. We explore various methods, including acid treatments, metal nanoparticle doping (Cu and Ag), multiple PEDOT:PSS layer depositions, and mono/multiatomic layer graphene insertion. Our findings reveal that optimizing PEDOT:PSS multilayer depositions and the treatment with nitric acid surpasses the effectiveness of additional methods using metal nanoparticles and graphene. This optimized process not only enhances PEDOT:PSS electrical conductivity but also proves less error-prone, more stable, and more cost-effective than using graphene layers and metal nanoparticles. Optimization factors include spinning speed, etchant concentration, and etching time. Compared to a single-layer PEDOT:PSS of the

same thickness, the optimized multilayer PEDOT:PSS treated with nitric acid shows a reduction in sheet resistance from 1 MΩ/sq to 7 Ω/sq. Additionally, we account for film aging to mitigate ambient-induced reliability effects.

B.1 Introduction

In our previous study [2], we introduced a novel method for producing conductive organic electrodes using doped PEDOT-PSS polymer films. Our findings revealed the extraordinary potential of these electrodes, showcasing their precision patterning and robust adhesion to diverse substrates, ranging from oxidized silicon wafers to flexible materials like Mylar. Effective substrate adhesion was achieved through a simple oxygen plasma cleaning step. To pattern the PEDOT:PSS films, we introduced a sacrificial silver metal layer to prevent chemical deterioration of PEDOT:PSS when exposed to standard photolithography process solvents. Key findings from reference [2] include a remarkable increase in electrical conductivity (by over two orders of magnitude) through multiple PEDOT-PSS depositions, without a significant increase in film thickness. An exponential relationship emerged as we observed a fundamental dependency between sheet resistance and the number of PEDOT-PSS coatings, deepening our understanding of the roles of PEDOT (the conductive component) and PSS (the non-conductive component) within PEDOT:PSS.

Furthermore, in our previous work [2], we explored the introduction of Cu nanoparticles (Cu NPs) as a doping agent, applied topically to soft-baked PEDOT-PSS films, revealing another remarkable leap in electrical conductivity—again, by two orders of magnitude. However, we encountered a notable counteractive effect: the two methods of conductivity enhancement, multiple PEDOT-PSS coatings, and Cu NP doping, did not simply add up as anticipated. In other words, combining these two methods did not yield cumulative improvements.

In this paper, we continue our exploration of ways to enhance the electrical conductivity of PEDOT:PSS layers and present novel techniques that extend and complement our previous work. Specifically, we examine treatments with nitric, phosphoric, and sulfuric acids, along with the effects of introducing noble metal nanoparticles and mono- and multi-layer graphene. While in our previous work, we explored the use of Cu NPs as a topical application and found that Cu bulk doping was ineffective due to Cu oxidation in aqueous solutions, in the new study, we use noble metal nanoparticles, namely silver (Ag), which enable electrically effective bulk doping of the PEDOT:PSS layers.

Nitric acid treatment emerges as a standout performer among the acid treatments, with its optimization as a focal point in our investigation. Our objective in this continued work is also to assess the compatibility of various conductivity enhancement methods and explore potential synergies. The dispersion of silver nanoparticles, whether applied topically or introduced as bulk doping, reveals promising effects—though interestingly, their conjunction with acid treatment does not yield further enhancements.

The incorporation of metal nanoparticles into PEDOT:PSS has garnered significant attention in previous research. For instance, Z. Xiong et al [3] achieved the successful production of inkjet-printed thin films of PEDOT:PSS doped with silver nanoparticles, yielding exceptional electrical and optical properties. Similarly, Patil et al [4] documented an increase in the conductivity of PEDOT:PSS through silver nanoparticle doping. In another study, R.-C. Zhang et al. [5] introduced a streamlined synthesis process for creating gold nanoparticle-PEDOT:PSS nanocomposites, showcasing their efficacy as catalysts in alkaline direct ethanol fuel cells. Furthermore, O. Ghazy et al.[6] harnessed silver particles prepared via gamma radiation to enhance the conductivity of PEDOT:PSS, particularly in the context of organic solar cells. Lastly, L. Pham et al. [7] provided compelling evidence of significant enhancements in polymer conductivity when Cu NPs were employed as dopants.

Similarly, the introduction of graphene, in both monolayer and triple-layer forms, presents its own enhancements, yet, like silver nanoparticles, it does not synergize with nitric acid treatment. The optimization of the nitric acid treatment takes into account the film aging and conductivity degradation caused by ambient-induced effects.

A significant finding in this study is the efficacy of the straightforward approach: combining multiple PEDOT:PSS depositions with optimized nitric acid treatment, while considering the impact of acid concentration and acid treatment time. This approach surpasses the efficacy of complex methods involving metal nanoparticles and graphene layers while providing a simpler and cost-effective means of enhancing PEDOT:PSS conductivity. Compared to a single-layer PEDOT:PSS of the same thickness, the optimized multilayer PEDOT:PSS treated with optimized nitric acid shows a reduction in sheet resistance from 1 MΩ/sq to 6.9 Ω/sq, marking a tenfold improvement over the lowest sheet resistance of 62 Ω/sq achieved with 6 PEDOT:PSS layers and topical dispersion of Cu nanoparticle doping reported in our previous work [2].

In a study by Wang et al. [8], single PEDOT:PSS films were subjected to treatment with phosphoric acid for durations of 0.5 minutes and 10 minutes. Their findings revealed that the use of phosphoric acid effectively removed the PSS component, resulting in improved electron extraction and enhanced performance of the solar cell devices. They concluded that an excess of PSS hindered electron collection within the devices. Our results support this conclusion and suggest that nitric acid treatment can further enhance the performance of solar cells. Additionally, the research conducted by F. Zhang's group[9] showcased the fabrication of semitransparent polymer solar cells (PCS) achieving a remarkable 9.40% power conversion efficiency and 24.6% visible transmittance. They also optimized PCS with a power conversion rate of 15.6%, exhibiting high transmittance in the visible light range and low transmittance in the near-infrared range[10]. Furthermore, X. Zhang et al.[11] demonstrated the production

of highly conductive PEDOT:PSS transparent electrodes using a post-spin-rinsing method for polymer solar cells.

The paper's structure is as follows: In the "Electrode Fabrication" section, we begin by briefly summarizing the fundamental manufacturing steps involved in depositing and patterning PEDOT:PSS layers, along with the methods to enhance the electrical conductivity of these films, which were previously covered in our earlier paper. We then shift our focus to providing a detailed account of the acid treatment process and the preparation and application of Ag NP dispersions.

Moving on to the "Results Section", we first present the individual effects of nitric, phosphoric, and sulfuric acids, as well as the effects of topical and bulk doping of PEDOT:PSS with silver nanoparticles. In this initial part, we concentrate on the outcomes of each technique in isolation.

Subsequently, in the latter part of the "Results Section", we delve into the synergistic effects that emerge when these techniques are combined with the multi-layer PEDOT:PSS deposition process. Finally, we summarize the most significant findings of the paper in the "Summary" section.

B.2 Electrode Fabrication

In this paper, we shift our focus towards the new methodologies we have investigated, as the comprehensive device fabrication process has been thoroughly detailed in our previous work[2]. Specifically, we delve into the acid treatment process involving nitric, sulfuric, and phosphoric acids, as well as the preparation of both topical and bulk silver nanoparticle dispersions. Furthermore, we assess the impact of environmental conditions on the organic

electrodes by subjecting them to storage in both standard laboratory settings and vacuum chambers for durations of up to 10 days. Before we delve into these novel enhancement methods, let's begin with a concise overview of the electrode fabrication process, which was extensively discussed in [2].

The fabrication of organic electrodes commenced with the utilization of a commercial dispersion of PEDOT:PSS in water. This dispersion was employed to deposit organic films onto cleaned substrates, which included oxidized Si wafers and flexible Mylar substrates. We utilized the spin-coating technique for film deposition, with the spin speed ranging from 1500 rpm to 3000 rpm. This choice of spin speed was especially crucial for multilayer PEDOT:PSS stacks, where each layer's speed, including speed ramps, had to be carefully selected to achieve the desired film thickness and the lowest achievable sheet resistance. The subsequent application of oxygen plasma cleaning significantly enhanced the uniformity of these films.

Following the spin-coating and soft-baking processes, we measured the film thickness using both a Dektak profilometer and an atomic force microscope (AFM). Remarkably, both methods produced measurements within a range of +/- 1 nm of each other, affirming the reliability of our measurements. Moreover, the uniformity of the PEDOT:PSS film, whether on oxidized Si wafers or flexible Mylar substrates, was found to be consistent within a tolerance of +/- 2 nm.

To pattern the PEDOT:PSS, we employed protective layers, specifically PVD-deposited silver (Ag) thin films. These layers were instrumental during photolithography, safeguarding the film from UV light exposure and chemical reagents. The photolithography process encompassed exposing the desired pattern and subsequently developing the positive resist AZ 5214E-IR. Following this, the exposed Ag regions underwent etching using an $HNO_3 : H_2O$ solution. This step was followed by rinsing and the subsequent removal of the PEDOT:PSS

layer through oxygen plasma treatment. In essence, the previous work[2] encompassed critical stages in the PEDOT:PSS film fabrication process, spanning deposition and uniformity measurement to precise photolithography-based patterning, with a specific emphasis on achieving superior electrical conductivity.

In the quest to optimize acid treatment techniques for PEDOT:PSS samples, we undertook a comparative study involving three acids: phosphoric, sulfuric, and nitric with their concentrations ranging from 0% to 100%. The duration of the acid treatment was varied from 1 second to 60 seconds. Our protocol involved employing each acid at a 100% concentration level, coupled with a brief 2-second treatment duration, which induced a significant reduction in the sheet resistance of PEDOT:PSS. In this initial experiment, the acid treatment was applied exclusively to a single layer of the PEDOT:PSS material. The acid method starts with the precise measurement of the desired acid concentration, followed by immersing PEDOT:PSS Si-wafer samples into the acid solution for the specified duration. Subsequently, the samples were promptly rinsed in DI water to eliminate any residual acid traces, ensuring the integrity of the results. As explained in more detail elsewhere[2], during the spin deposition of PEDOT:PSS, a vertical phase separation phenomenon occurs, segregating the PEDOT and PSS components. The resulting wet film accumulates conductive PEDOT strips at its base and a PSS-rich solution at the upper segment. This transition isn't abrupt but gradual, with the highest concentration of PSS at the top and the lowest at the bottom, exhibiting an inverse behavior for PEDOT. Regardless of whether the acid treatment targets a single or multiple layers of PEDOT:PSS, its core action involves the removal of PSS from the upper layer. The residue comprises a layer primarily composed of PEDOT, occasionally housing residual PSS inclusions, as illustrated in Figure B.1.

We conducted experiments involving the application of silver nanoparticles (Ag NPs) to multilayer PEDOT:PSS using both the topical and bulk doping approaches. For bulk doping,

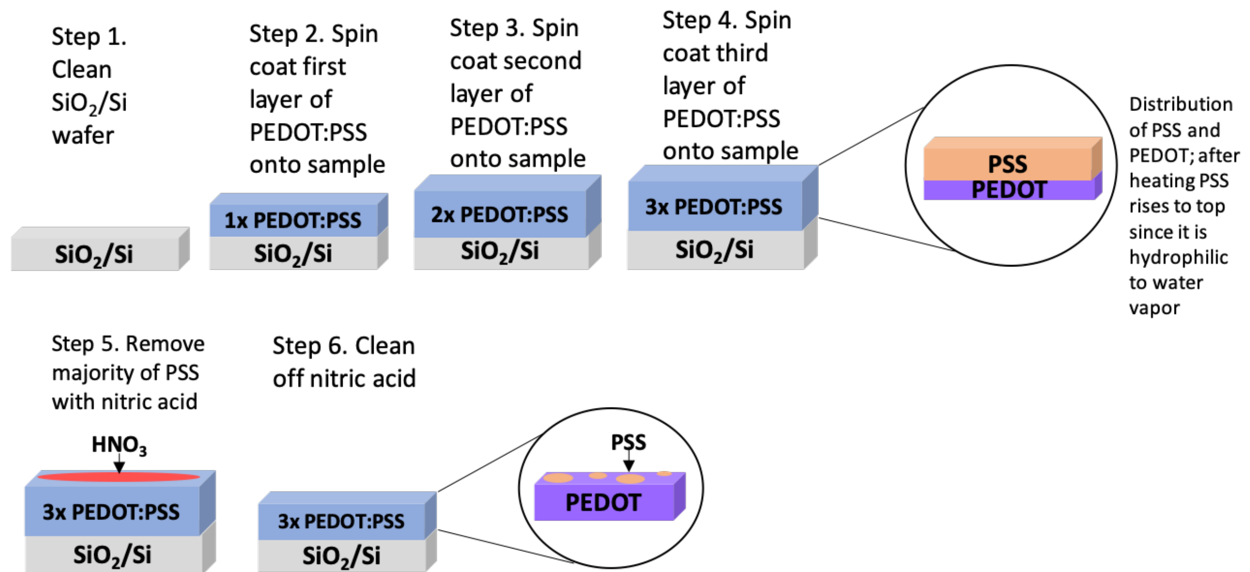

Figure B.1: Process of acid treating PEDOT:PSS layers

5mg of Ag NPs was combined with 10 ml of PEDOT:PSS solution to make a 0.5mg/ml concentration solution. The mixture was stirred for a minimum of 1 hour and subsequently sonicated for an additional hour. In contrast, for surface doping, a dispersion solution of Ag NPs in ethanol of the same 0.5mg/ml concentration was prepared, followed by the same stirring and sonication procedure employed in the bulk doping method. The dispersion of Ag nanoparticles in ethanol was subsequently spin-coated onto the surface of the PEDOT:PSS layer at 1500 rpm.

The choice of silver nanoparticle concentration at 0.5 mg/ml was informed by our earlier research involving copper nanoparticles[2]. In a prior study, we explored different concentrations of Cu NPs, specifically 0.2 mg/ml and 0.5 mg/ml, and determined that the latter (0.5 mg/ml) yielded the most favorable outcomes. To maintain consistency, we opted for the same concentration (0.5 mg/ml) when working with silver nanoparticles.

Regarding the silver nanoparticles, we had access to two powders from Sky Springs Nanomaterials, Inc., one with nanoparticles sizes ranging from 20-30 nm and another one with

nanoparticles ranging from 50-60 nm, with the larger sizes providing higher conductivity of the PEDOT:PSS (see next section).

The final enhancement method involved inserting a graphene monolayer between the oxidized Si wafer and PEDOT:PSS films, and the transfer process for the graphene monolayer consisted of several steps:

1. Cutting polyethylene terephthalate (PET) and the graphene-on-copper sheet into 1cm$\times$1cm squares and taping the graphene-on-copper sheet onto the PET.

2. Spin-coating the polymethyl methacrylate PMMA solution onto the graphene at 500 RPM for 5 seconds, followed by 2500 RPM for 45 seconds. The PMMA solution comprised 10 mL of PMMA solution mixed with 10 mL of anisole solvent, resulting in a final concentration of 4.5% PMMA. Approximately 4 to 5 drops of this PMMA solution were dispensed onto the graphene and spin-coated. An annealing step followed, with options including 50°C for 2 minutes.

3. Subsequently, PET was removed, and the sample was exposed to oxygen plasma at 30W of power, with a gas flow rate of 10 SCCM of oxygen gas, for 1 minute.

4. The copper foil was then etched away by floating it in a copper etchant ($FeCl_3$) for approximately 10 minutes until most of the copper was etched away.

5. The film was transferred into DI water using a glass slide, left in the DI water for about 10 minutes, and this process was repeated two more times with fresh DI water each time.

6. After the third DI bath, the graphene film was lifted onto the oxidized Si wafer sample, effecting the transfer of graphene to the wafer.

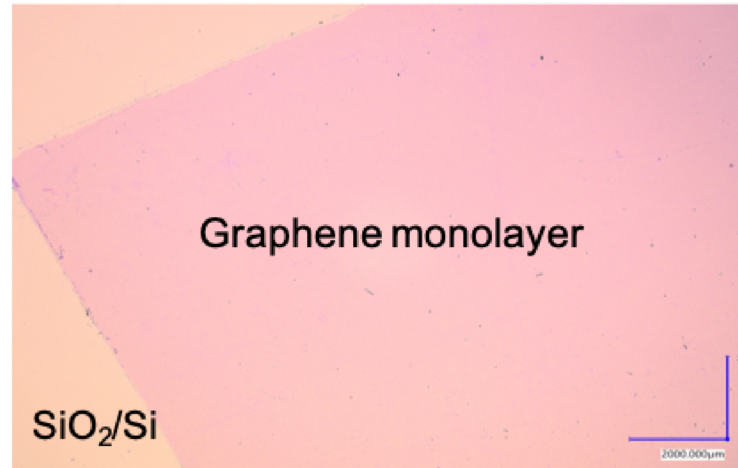

Figure B.2: Graphene monolayer transferred on to SiO_2/Si

7. The sample was then air-dried for 4 hours and placed in a vacuum chamber for 12-24 hours.

8. The PMMA was then removed, by initially baking the wafer at 85°C for 5 minutes, followed by a bake at 140°C for 15 minutes and then subsequently immersing the sample in warm acetone at 55°C for 1 hour.

9. Finally, the sample was cleaned with isopropyl alcohol cleaning solvent (IPA) for 30 minutes and dried to obtain graphene on oxidized Si wafer.

This comprehensive process ensured the successful transfer of the graphene monolayer onto the wafer. Figure B.2 shows the image a monolayer graphene transfered onto an oxidized Si substrate. The graphene trilayer is provided as a separate sample on 1 cm × 1 cm pieces of oxidized Si wafers by Graphenea. It consists of three graphene monolayers stacked directly upon each other.

The sheet resistance, denoted as R_sq, or the conductivity, symbolized as σ, of the PEDOT:PSS layers has been determined utilizing the four-probe measurement method[12]. These electrical properties, conductivity, and sheet resistance are interconnected and can be

Conductivity Enhancement Technique	Sheet Resistance [Ω/sq]
Nitric Acid (HNO_3) for 2s, 100% Concentration, 1 × PEDOT:PSS	172
Phosphoric Acid (H_3PO_4) for 2s, 100% Concentration, 1 × PEDOT:PSS	1.2 k
Sulfuric Acid (H_2SO_4) for 2s, 100% Concentration, 1 × PEDOT:PSS	220

Table B.1: Sheet resistance comparison between three acids

expressed through eq. (B.1):

$$\sigma = \frac{1}{R_{sq} \times t} \tag{B.1}$$

For instance, consider a pristine PEDOT:PSS film deposited at 2000 rpm, resulting in a film thickness (t) of 56 nm, and possessing a sheet resistance of R_{sq} equal to 1 MΩ/sq. According to Equation (B.1), this sheet resistance value corresponds to a conductivity (σ) of 0.18 S/cm.

B.3 Results and Discussion

We start our investigation by examining the impact of acid treatment on a single-layer PEDOT:PSS, specifically employing phosphoric, sulfuric, and nitric acid. Table B.1 provides the sheet resistance values obtained for these three acid treatments at a 100% concentration for 2 seconds. Notably, nitric and sulfuric acid outperform phosphoric acid by a factor of at least five, with nitric acid showing a slight advantage over phosphoric acid. These findings hold true across various acid concentrations and treatment durations, including the use of a 60% acid concentration for 1 minute. Given that nitric acid consistently delivers the best results, our subsequent focus will center on the nitric acid process. When we conducted experiments with nitric acid at a 100% concentration, we explored different treatment dura-

Conductivity Enhancement Technique	**Sheet Resistance** [Ω/sq]
1 × PEDOT:PSS + 100% HNO_3 for 1 min	130
1 × PEDOT:PSS + 80% HNO_3 for 1 min	171
1 × PEDOT:PSS + 60% HNO_3 for 1 min	181
1 × PEDOT:PSS + 40% HNO_3 for 1 min	201
1 × PEDOT:PSS + 20% HNO_3 for 1 min	1823

Table B.2: Sheet resistance as a function of acid concentration

tions: 1 second, 2 seconds, and 3 seconds. Our findings revealed that varying the treatment time had only a minor effect on sheet resistance, with the 2-second treatment showing a slight advantage. Our investigation then turned to the influence of nitric acid concentration on its ability to reduce sheet resistance. Given the well-known principle that more concentrated acid solutions tend to be more effective, we sought to ensure a fair comparison by extending the treatment time to 60 seconds for all acid concentrations. The outcomes of this study are presented in Table B.2. Not surprisingly, the 1×PEDOT:PSS samples, showed that a 100% nitric acid concentration resulted in the lowest sheet resistance, measuring 130 ohms per square, while the lowest concentration of 20% led to the highest sheet resistance, measuring 1823 Ω/sq. Interestingly, acid concentrations of 40%, 60%, and 80% produced comparable results in terms of sheet resistance, between 170 and 200 Ω/sq.

In Figure B.3 and Table B.3, we compare the sheet resistance of multilayer PEDOT:PSS stacks treated with 60% nitric acid to those without acid treatment. Nitric acid treatment significantly reduces sheet resistance by approximately two orders of magnitude for all numbers of PEDOT:PSS coatings. Notably, the best result achieved is 7.7 Ω/sq for 9 PEDOT:PSS layers treated with 60% nitric acid. This study extends the analysis beyond our previous work[2], for maximum number of PEDOT:PSS layers from 6 to 9. Adding the extra 3 layers results in a threefold decrease in sheet resistance, though further increases of number

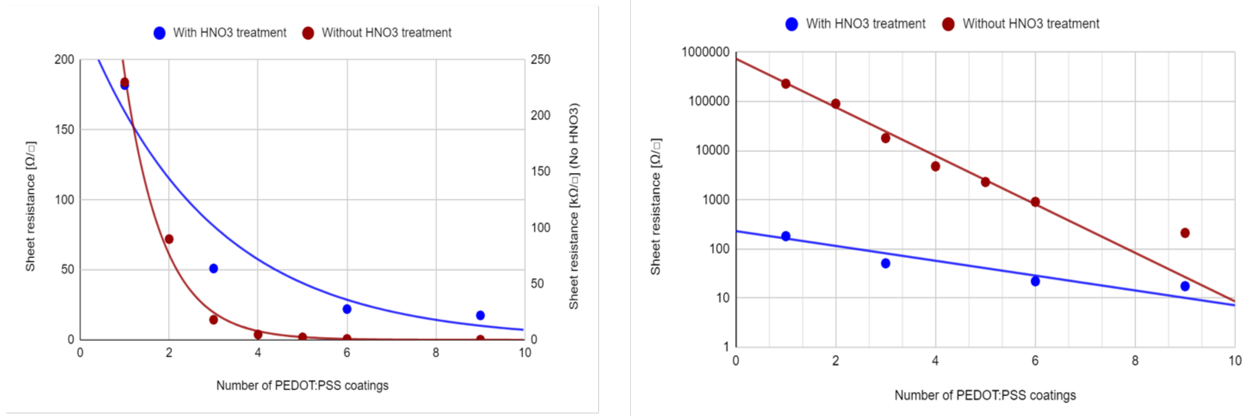

Figure B.3: Sheet resistance of multilayer PEDOT:PSS layer stacks as a function of the number of layers with and without nitric acid treatment.

Conductivity Enhancement Technique	**Sheet Resistance w/ 60% HNO_3 for 1 min** [Ω/sq]	**Sheet Resistance w/o HNO_3** [Ω/sq]
1 × PEDOT:PSS	181	230k
3 × PEDOT:PSS	51	18k
6 × PEDOT:PSS	22	906
9 × PEDOT:PSS	7.7	37.73

Table B.3: Sheet resistance of multilayer PEDOT:PSS layer stacks as a function of the number of layers with and without nitric acid treatment.

Conductivity Enhancement Technique	Sheet Resistance [Ω/sq]
1 × PEDOT:PSS + 1 × 0.5 mg/ml Ag NP in Ethanol (Topical Application)	464
1 × [PEDOT:PSS + 0.5 mg/ml Ag NP]	629 k
3 × PEDOT:PSS + 3 × 0.5 mg/ml Ag NP in Ethanol (Topical Application)	121
3 × [PEDOT:PSS + 0.5 mg/ml Ag NP]	30k

Table B.4: Sheet resistance of 1 × PEDOT:PSS and 3 × PEDOT:PSS with bulk and topical doping with Ag nanoparticles.

of layers yield by only marginal improvements. Our attention now shifts to the potential of silver nanoparticles (Ag NP) to enhance the electrical conductivity of PEDOT:PSS. Given silver's inert nature, we introduced it using two methods: bulk doping, where Ag NP dispersion was mixed with PEDOT:PSS solution, and topical application after a soft bake of the PEDOT:PSS. Two sizes of Ag NP, ranging from 20-30 nm and 50-60 nm, were employed. Our experiments reveal that larger Ag nanoparticles consistently yield higher conductivity values. Table B.4 compares bulk and topical applications of Ag NP for 1×PEDOT:PSS and 3×PEDOT:PSS. Topical Ag NP application results in significantly lower sheet resistance compared to the bulk method, demonstrating a three-order-of-magnitude improvement. This suggests that bulk doping with nanoparticles is ineffective due to potential issues such as inadequate accommodation of Ag NP within PEDOT:PSS and possible coating of Ag NP by PSS.

Given the inefficacy of bulk doping with Ag NP, we proceeded to compare the results with topical application of copper nanoparticles (Cu NP), a method utilized in our previous study. For 3×PEDOT:PSS layers, both Ag and Cu NP resulted in comparable sheet resistance values of 121-260 Ω/sq and 173-256 Ω/sq, respectively. Additionally, both types of nanoparticles produced similar effects on sheet resistance for 3×PEDOT:PSS layers treated

with 60% HNO 3 acid. Therefore, it can be concluded that Cu nanoparticle doping offers an economically advantageous alternative to silver particle doping.

The third approach aimed at reducing PEDOT:PSS sheet resistance involved introducing graphene on an oxidized Si wafer before PEDOT:PSS layer deposition. Two types of graphene were tested: a single large graphene monolayer and trilayer graphene, as described in the previous section. The sheet resistance for the graphene monolayer was measured at 20 kΩ/sq, while the trilayer graphene exhibited significantly lower resistance at 50 Ω/sq.

However, using trilayer graphene encountered adhesion issues with PEDOT:PSS. We addressed this challenge by subjecting the trilayer graphene to plasma treatment, significantly improving PEDOT:PSS adhesion. Unfortunately, this enhancement came at a cost, as the sheet resistance of the trilayer graphene deteriorated considerably. Moreover, it displayed a highly non-uniform distribution of sheet resistance, ranging from 14 Ω/sq to 4 kΩ/sq. Due to this substantial variability, further experiments involving trilayer graphene were largely abandoned. Nevertheless, we produced a single sample of 6×PEDOT:PSS on plasma-treated trilayer graphene, resulting in a sheet resistance of 1350 Ω/sq. One favorable outcome of this result is the absence of sheet resistance nonuniformity across the wafer. On the other hand, a graphene monolayer combined with 9 layers of PEDOT:PSS yielded a respectable sheet resistance of 36.4 Ω/sq. However, it still falls short of the sheet resistance achieved by 9xPEDOT:PSS treated with 60% nitric acid, which resulted in $R_sq = 7.7$ Ω/sq.

It's worth noting that the lower end of the sheet resistance spectrum for plasma-treated trilayer graphene, with values as low as 14 Ω/sq, offers some optimism for potential future studies. Addressing the non-uniformity issue remains a possibility, especially given that trilayer graphene is more manageable than transferring a graphene monolayer.

Now, let's explore the combined effects of multiple enhancement methods. To our knowl-

edge, the combined effects of different enhancement methods have been not yet reported. Firstly, we examine the combination of nitric acid treatment and silver nanoparticle doping. For 3×PEDOT:PSS, HNO_3 treatment alone results in a sheet resistance of 50 Ω/sq, while the addition of Ag NP as a topical application yields similar results, with the exception of one outlier at 25 Ω/sq due to the use of a newly shipped PEDOT:PSS. Therefore, it can be concluded that the addition of metal NP does not provide a significant improvement over nitric acid treatment alone. Another combination of interest is the joint use of nitric acid treatment and graphene insertion. While both methods independently reduce sheet resistance significantly, their combined effect appears negligible. For example, a 9×PEDOT:PSS layer treated with nitric acid achieves a sheet resistance of 7.7 Ω/sq, and when a graphene monolayer is added, the sheet resistance drops slightly to 6.9 Ω/sq. Overall, nitric acid treatment on its own proves to be the most effective method for enhancing PEDOT:PSS conductivity, with combinations offering no additional benefits. Furthermore, the nitric acid method is the least expensive and least complex when compared to metal nanoparticle doping and graphene insertion.

Now, we delve into the finer details of nitric acid treatment. Various concentrations from 0% to 100% and different treatment times were tested. The effectiveness of sheet resistance reduction was found to be relatively independent of treatment time within the 1-second to 1-minute range. To ensure consistent treatment duration and minimize possible human errors, a baseline procedure of 1-minute duration was adopted, with similar results observed for 30-second and 40-second durations.

Additionally, the stability of nitric acid treatment over time was assessed. Samples were allowed to sit for several days, and sheet resistance was measured periodically. The outcomes of the experiments are visually represented in Figure B.4. Over time, it is apparent that the sheet resistance experiences deterioration across all acid concentrations, eventually reaching

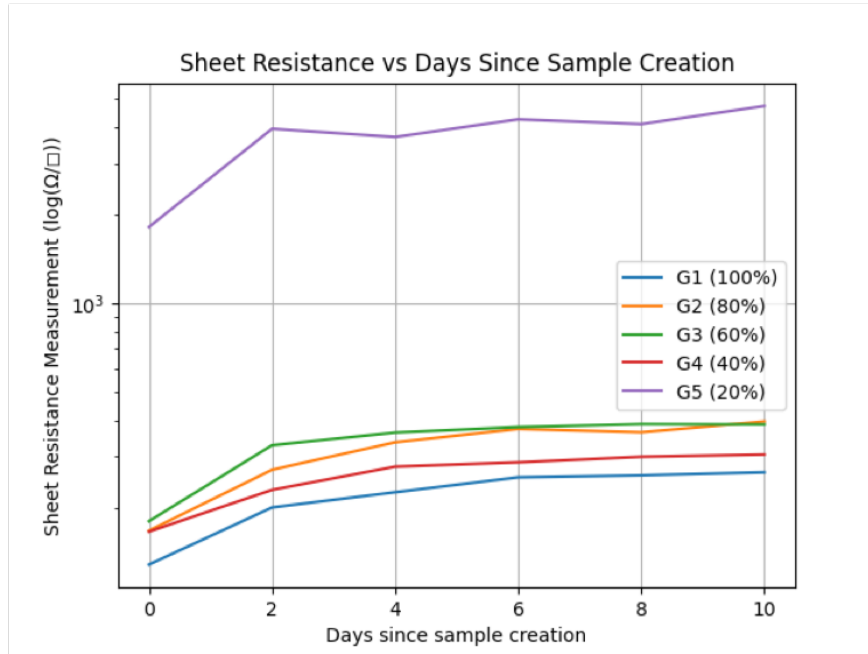

Figure B.4: Sheet resistance stability as a function of ambient exposure for 20%, 40%, 60%, 80% nitric acid concentration.

a point of saturation, and maintaining relatively constant values after approximately six days.

Figure B.5 illustrates the data in terms of sheet resistance degradation concerning the values immediately following the acid treatment. Here, the degradation D% is defined as,

$$D\% = \frac{(\text{sheet resistance at day measured} - \text{sheet resistance just after being manufactured})}{(\text{sheet resistance just after being manufactured})} \tag{B.2}$$

It is notable from Figure B.4 that the sheet resistance exhibits its most stable performance at a 60% concentration of acid. Consequently, for the experiments discussed earlier, we adopted the 60% nitric acid concentration as our baseline method.

The intriguing aspect of sheet resistance degradation following acid treatment prompted an investigation into its potential causes. One hypothesis proposed that the degradation

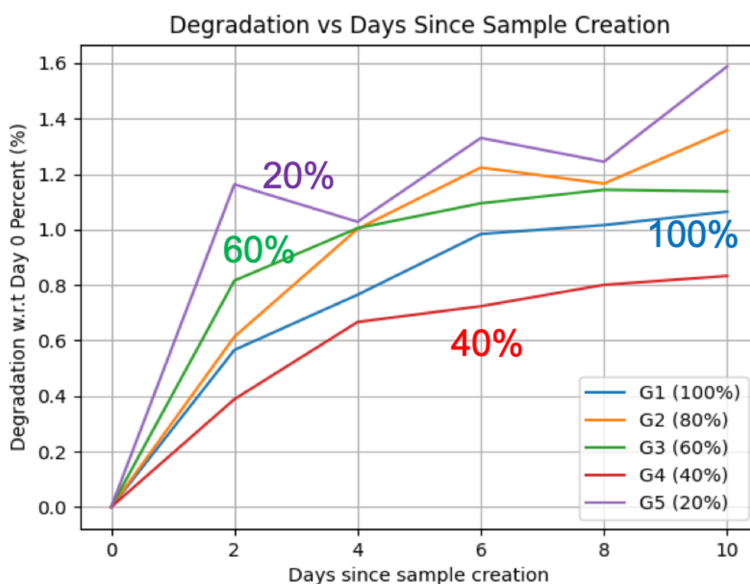

Figure B.5: Sheet resistance degradation as a function of ambient exposure for 20%, 40%, 60%, 80% nitric acid concentration.

might arise from a reaction between the PEDOT:PSS treated with acid and the ambient laboratory atmosphere. To validate this assumption, we created identical samples, placing some in the ambient laboratory atmosphere and others in a small vacuum chamber, from which the samples were removed for a brief period to measure sheet resistance.

Figure B.6 presents the results for samples stored in both ambient laboratory conditions and the vacuum chamber. Remarkably, there was no substantial difference observed in sheet resistance between the two environments. Consequently, we conclude that the degradation is not triggered by a reaction between the samples and the ambient atmosphere but rather stems from an internal reaction within the samples. This observation also explains why the degradation eventually reaches a saturation point over time.

Finally, we would like to discuss an observation, as previously mentioned. A recent shipment of PEDOT:PSS from Sigma-Aldrich consistently displayed a lower sheet resistance, approximately 2-3 times lower than the initial batch received approximately a year ago. While the

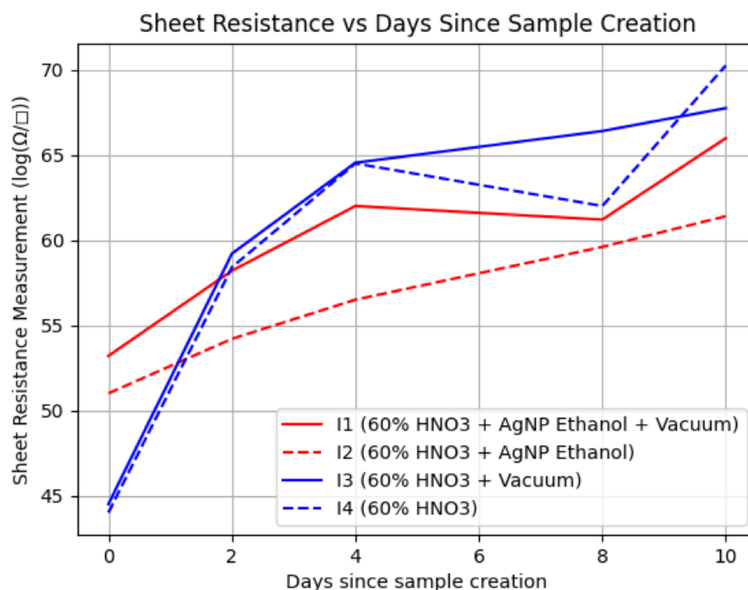

Figure B.6: Sheet resistance evolution as a function of time (days) for 60% nitric acid treatment and with topical Ag NP doping in lab atmosphere and in vacuum.

new material does show a slight improvement in conductivity, the observed trends and dependencies remain consistent with those of the older material. Sigma-Aldrich has not shared any details regarding the process changes that led to this conductivity improvement.

B.4 Summary

We have explored various methods to enhance the electrical conductivity of PEDOT:PSS films, including acid treatments, metal nanoparticle doping (Cu and Ag), multiple PEDOT:PSS layer depositions, and the insertion of mono/multiatomic layer graphene. Our investigations have revealed that while each of these methods individually leads to a substantial increase in electrical conductivity, their combined application does not yield further improvements.

In the realm of metal nanoparticle doping, we have observed that the topical doping method

outperforms bulk doping. Notably, in the case of Cu nanoparticles, which are unsuitable for bulk doping, we found them to be as effective as noble metal nanoparticles, offering a more cost-effective choice.

Furthermore, our optimization efforts led to a nitric acid treatment process that surpasses the effectiveness of additional methods involving metal nanoparticles and graphene. This optimized treatment involves nine layers of PEDOT:PSS and can reduce the sheet resistance from 1 MΩ/sq to 7 Ω/sq. However, it's worth noting that the electrical conductivity of PEDOT:PSS layers treated with acid degrades over time, albeit at a modest rate, stabilizing after a few days at a consistent level.

Regarding graphene's role in enhancing conductivity, we discovered that trilayer graphene, despite being a more cost-effective option than monolayer graphene, faces adhesion challenges with the PEDOT:PSS layer. Adhesion issues can be mitigated through topical plasma treatment, but this intervention has implications for uniformity and degrades the electrical conductivity gains. Nevertheless, the trilayer graphene method shows promise for enhancing conductivity, pending further research and development.

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